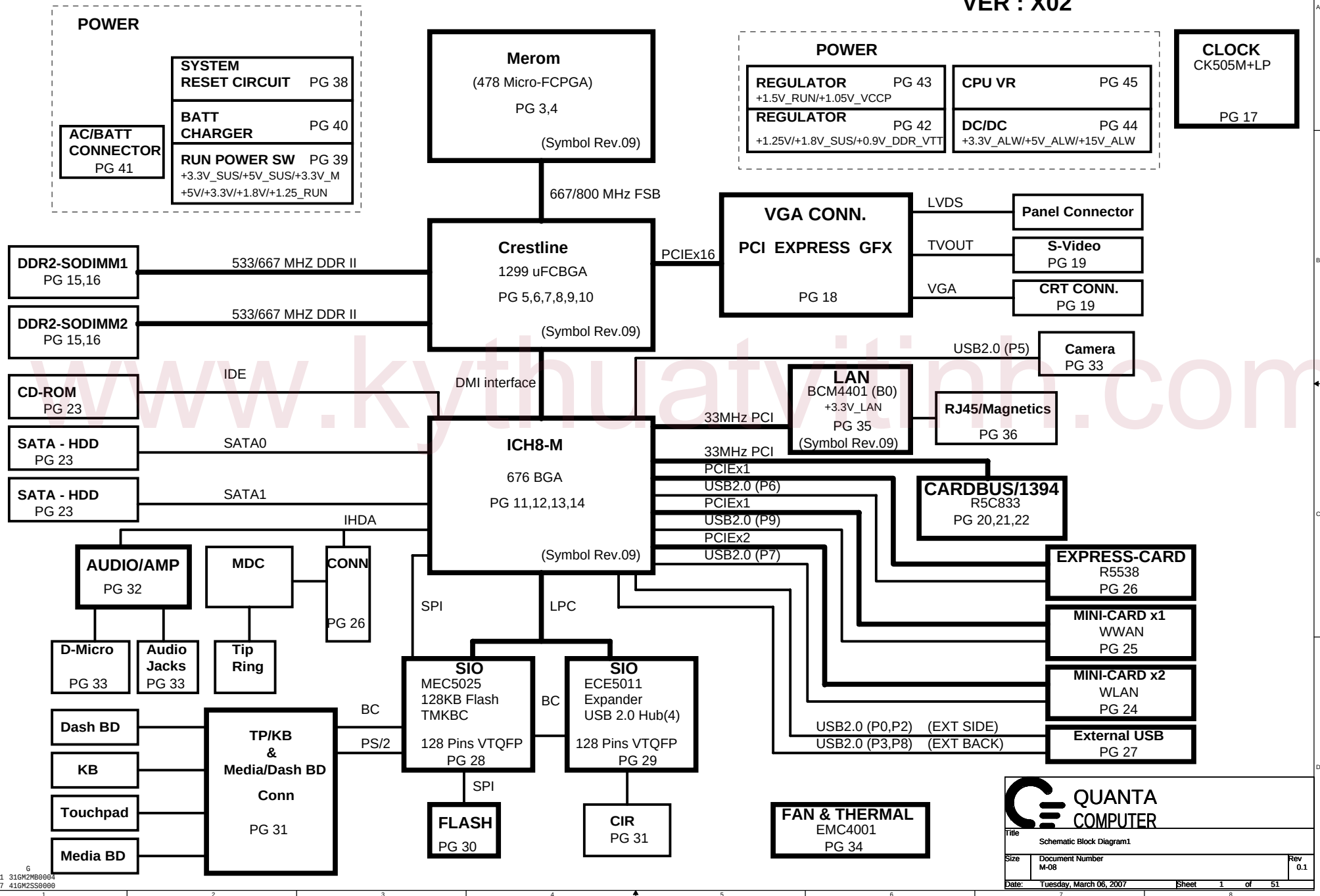


Corsica\Gilligan - DISCRETE

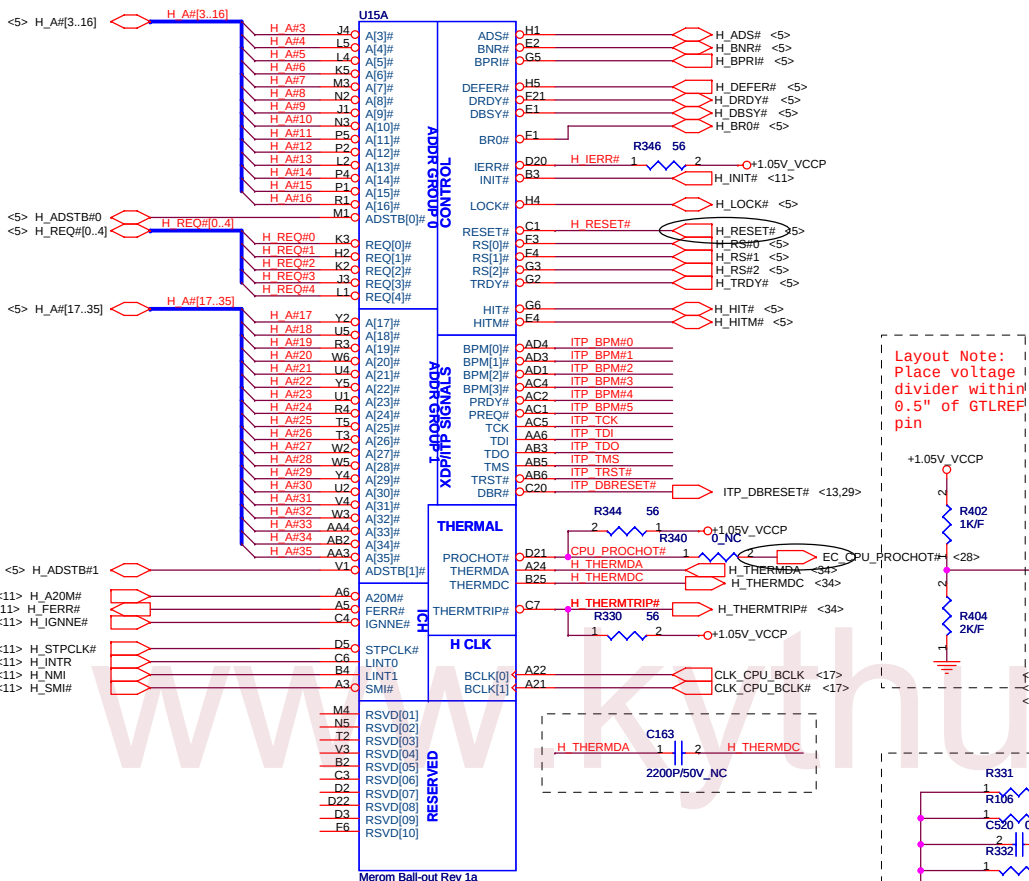
VER : X02



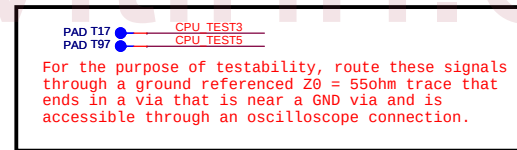
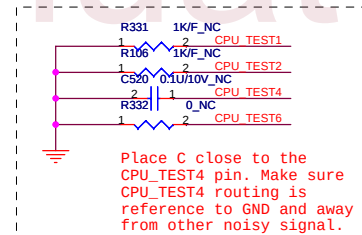
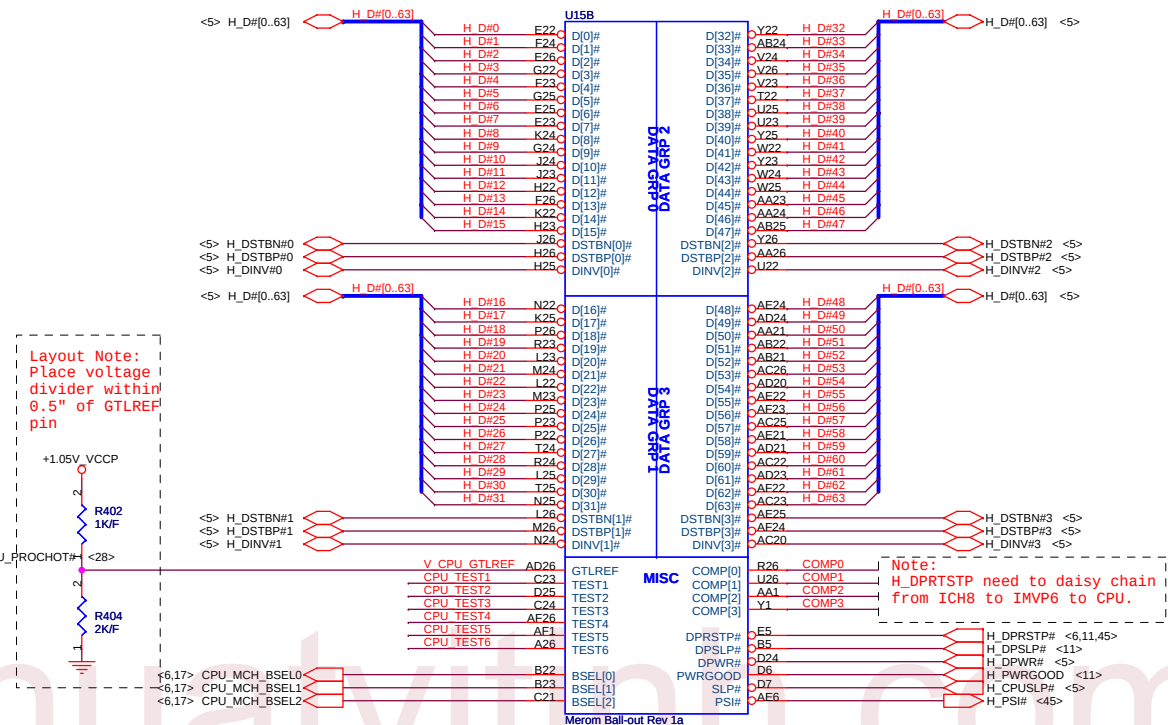
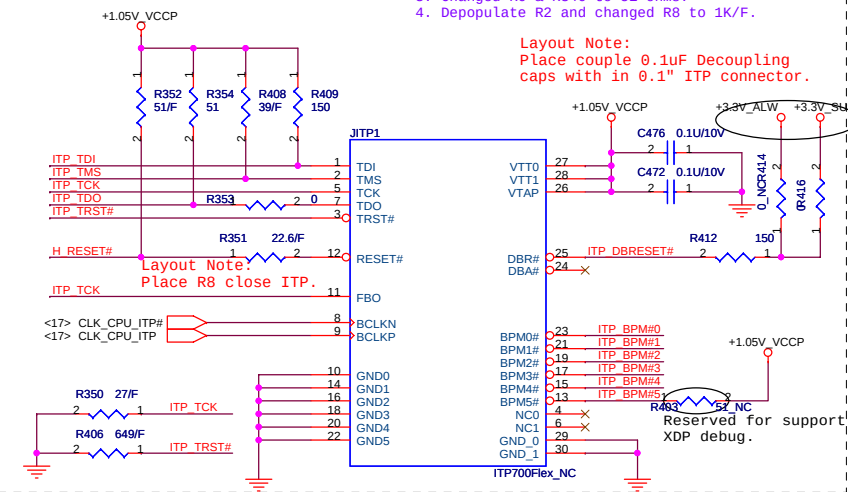
INDEX		
Pg#	Description	DNI LIST
1	Schematic Block Diagram	
2	Front Page	
3-4	Merom	
5-10	Crestline	
11-14	ICH8M	
15-16	DDRII SO-DIMM(200P)	
17	Clock Generator	
18-21	VGA	
22	LCD Conn. & SSP	
23	CRT Conn	
24	SATA & IDE Conn	
25	PCCARD/Conn & 1394	
26	Express Card & Smart Card	
27	Mini Card	
28	MDC Conn.	
29	SIO (MEC5004)	
30	SIO (MEC5018)	
31	SERIAL PORT & USB	
32	Flash ROM	
33	TP,BT & FIR	
34	Switch,Keyboard & LED	
35	FAN & Thermal	
36-37	Audio CODEC(STAC9200)/Phone Jack	
38-39	LOM (BCM5752)/Switch	
40-41	Docking Conn/Q-Switch	
42	System Reset Circuit	
43-44	Battery Selector & Charger	
45	DDR2_1.8VSUS, 0.9V	
46	1.5VSUS,1.05V(VTT)	
47	1.25V,1.05VM	
48	CPU_MAX8786(3phase)	
49	D/D Power	
50	RUN Power Switch	
51	VGA DC/DC	
52	DCIN/Batt Conn.	
53	PAD& SCREW	
54	EMI CAP	

Power & Ground			
Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (19V)	
PBATT+		MAIN BATTERY + (10~17V)	
PBATT+		SECOND BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~19V)	
RTC_PWR3_3V		RTC & +3.3V_RTC_LDO(3.3V)	
+VCC_CORE		CPU CORE POWER (1.5V)	RUNPWROK
+15V_ALW		LARGE POWER (15V)	SUS_ON
+3.3V_RUN		SLP_S3# CTRLD POWER	RUN_ON
+3.3V_SUS		SLP_S5# CTRLD POWER	SUS_ENABLE
+3.3V_ALW		8051 POWER (3.3V)	ALWON/THERM_STP#
+5V_RUN		SLP_S3# CTRLD POWER	RUN_ON
+5V_SUS		SLP_S5# CTRLD POWER	SUS_ON
+5V_HDD		HDD POWER (5V)	+5V_RUN
+5V_MOD		MODULE POWER (5V)	HDDC_EN
+5V_ALW		LCD/CHARGE POWER (5V)	
+VDDA		AUDIO ANALOG POWER (5V)	AUDIO_AVDD_ON
+1.5V_RUN		CALISTOGA/ICH7 POWER	RUN_ON
+1.05V_VCCP		CPU/CALISTOGA/ICH7 POWER	RUN_ON
+1_8V_SUS		SODIMM POWER	SUSPWROK_5V
+1.8V_RUN		SDVO POWER	RUN_ON
+0.9V_DDR_VTT		SODIMM POWER	RUN_ON
+3.3V_LAN		LAN POWER	AUX_EN
 GND	ALL PAGES	DIGITAL GROUND	
 AGND_JSL6260		CPU GND	
 AGND_TPS51120		DC/DC POWER GND	
 AGND1		VTT POWER GND	
 AGND2		VTT POWER GND	
 8731AGND		CHARGER GND	

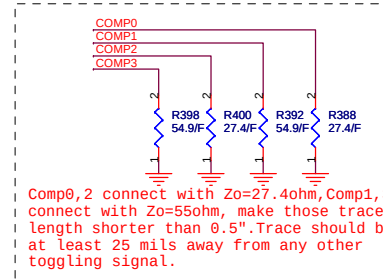
 QUANTA COMPUTER		
Title Index, DNI, Power & Ground		
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 2	of 51



Populate ITP700Flex for bringup

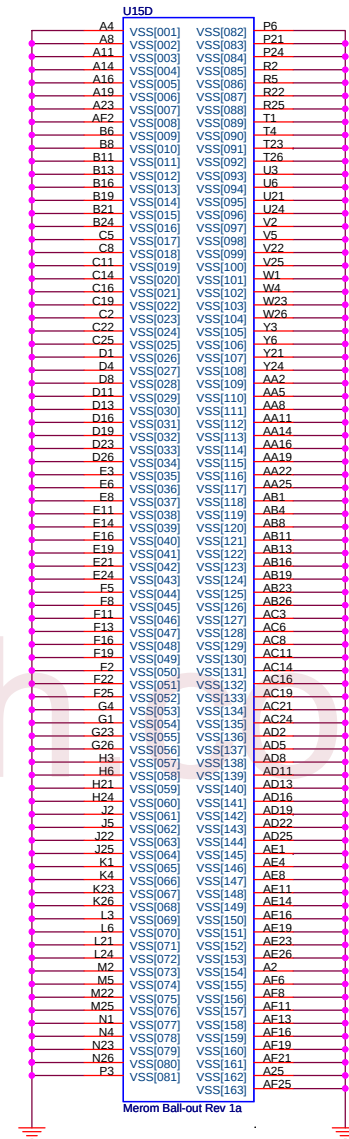
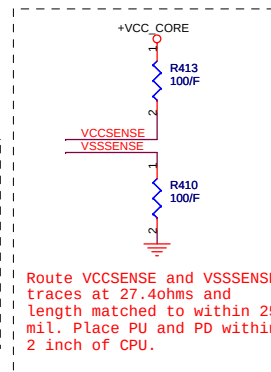
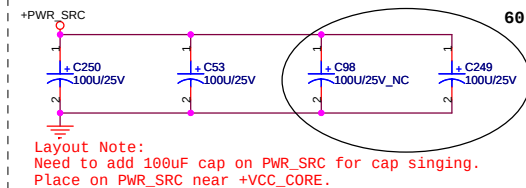
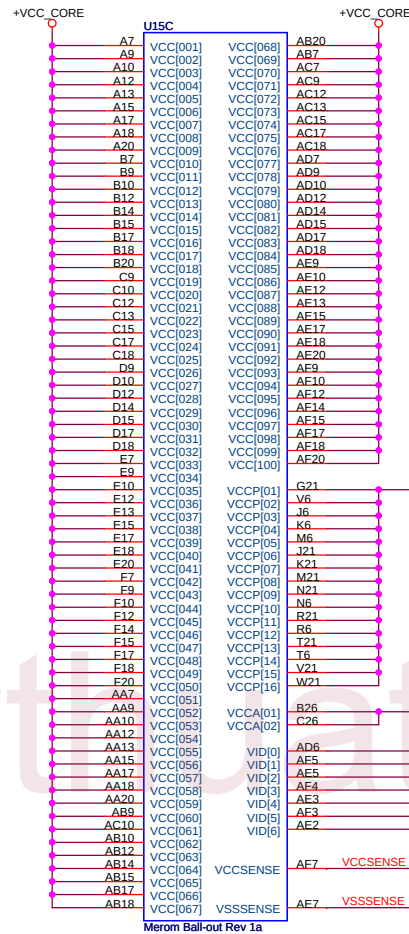
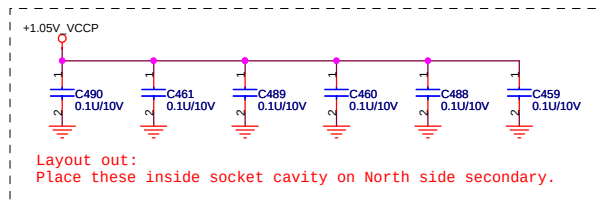
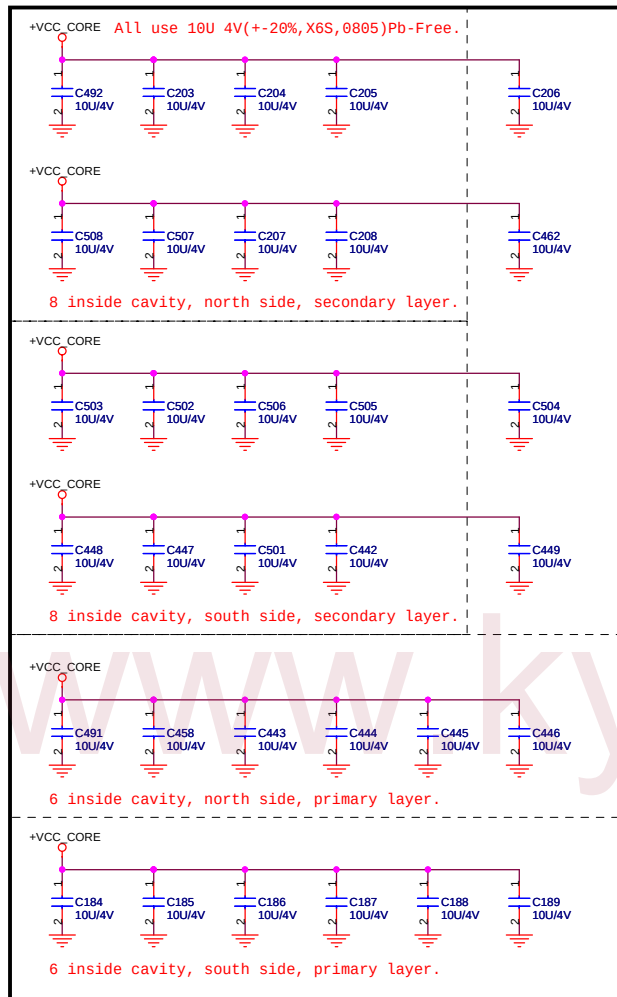


FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

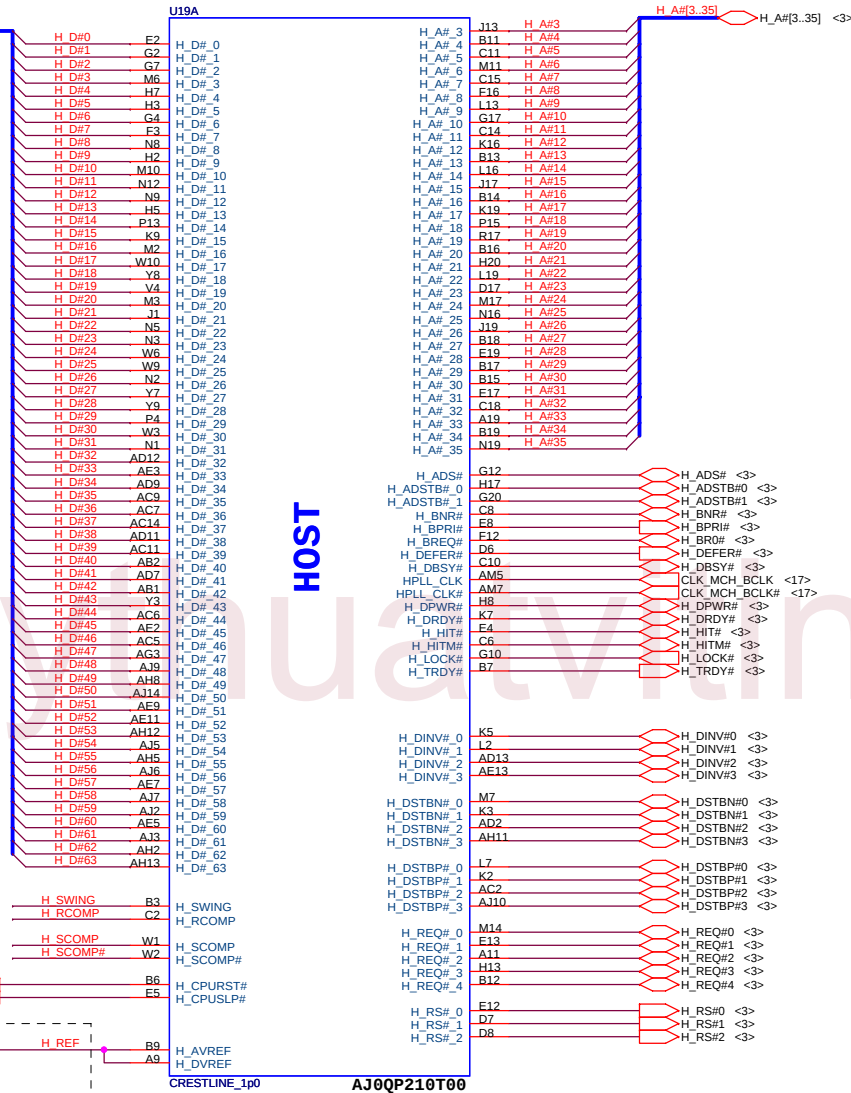
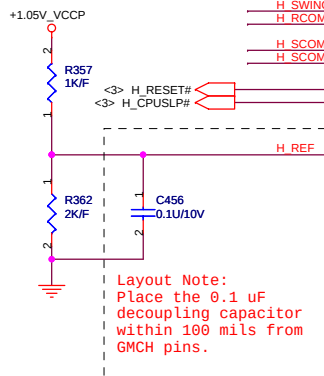
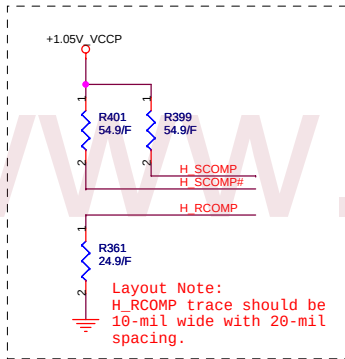
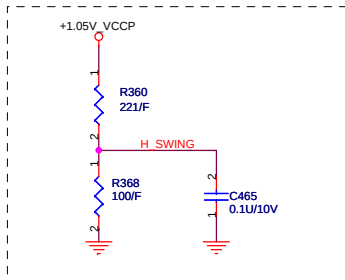


ITP700 layout guidelines				
Signal	Resistor Value	Connect To	Resistor Placement	
TDI	150 ohm ± 5%	VCCP	Place the pull-up near CPU	
TMS	39 ohm ± 1%	VCCP	Within 200ps of ITP connector	
TRST#	500 to 680 ohm ± 5%	GND	Place the pull-down near CPU	
TCK	27 ohm ± 1%	GND	Connect to TCK pin of CPU and then connect it to F80 pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector	
TDO	51 ohm ± 5%	VCCP	Place the pull-up near ITP	
RESET#	22.6 ohm ± 1% series resistor and pullup 51 ohm ± 1%.	VCCP	Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector.	

DELL CONFIDENTIAL/PROPRIETARY

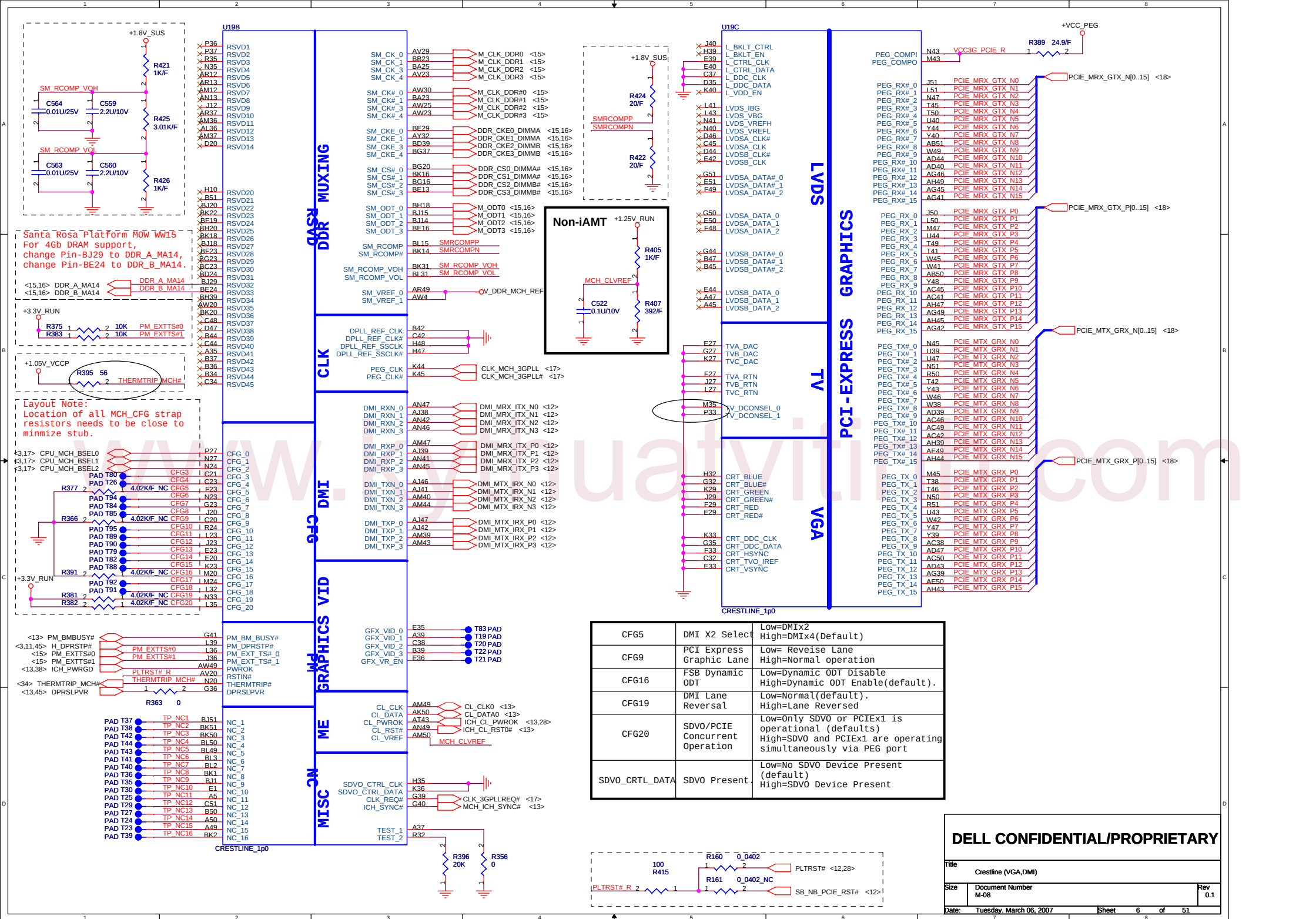


DELL CONFIDENTIAL/PROPRIETARY



DELL CONFIDENTIAL/PROPRIETARY

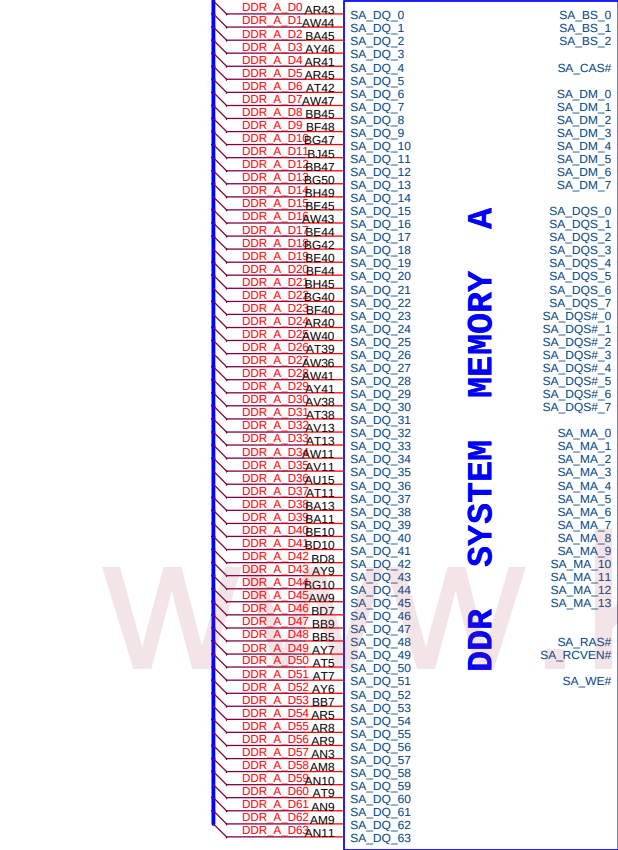
Title Crestline (HOST)		
Size M-08	Document Number M-08	Rev 0.1
Date Tuesday, March 06, 2007	Sheet 5	of 51



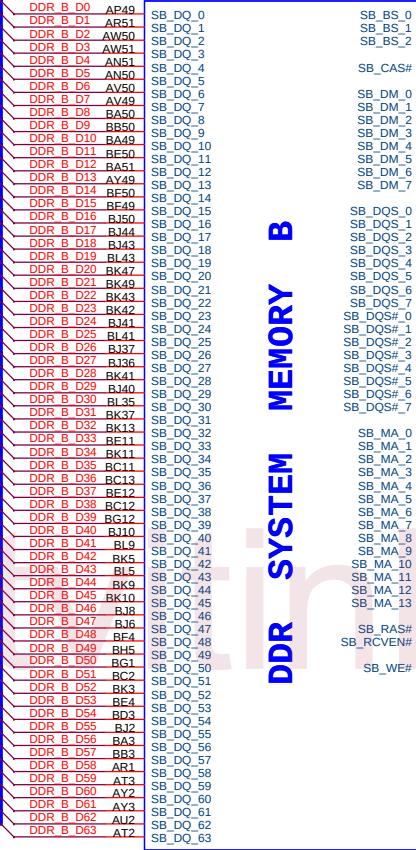
DELL CONFIDENTIAL/PROPRIETARY

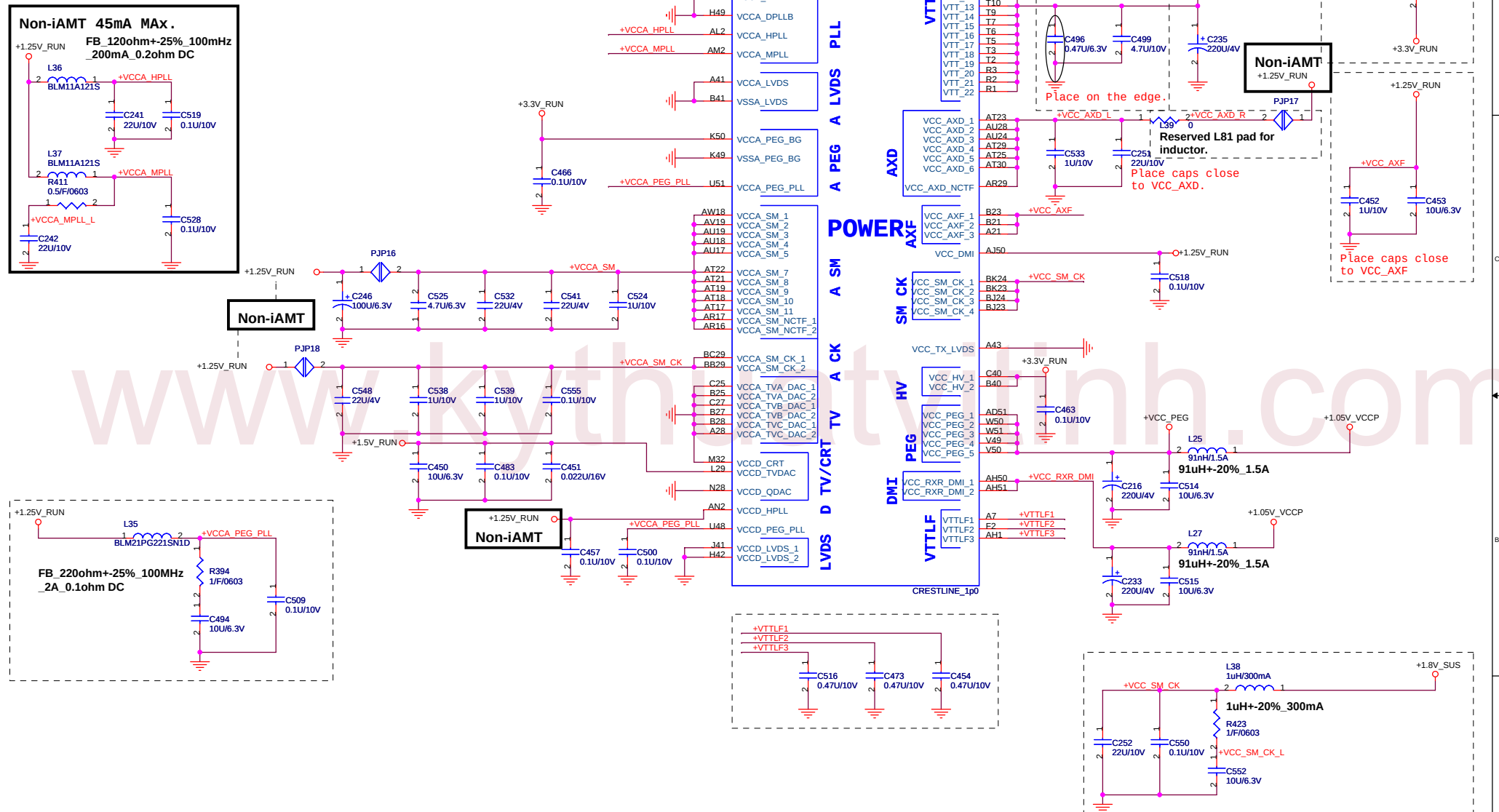
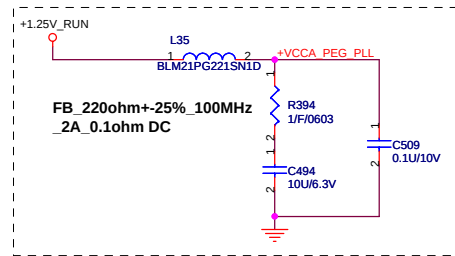
Title			
Crestline (VGA,DMI)			
Size	Document Number	Rev	
	M-08	0.1	
Date:	Tuesday, March 06, 2007	Sheet	6 of 51

<15> DDR_A_D[0..63]

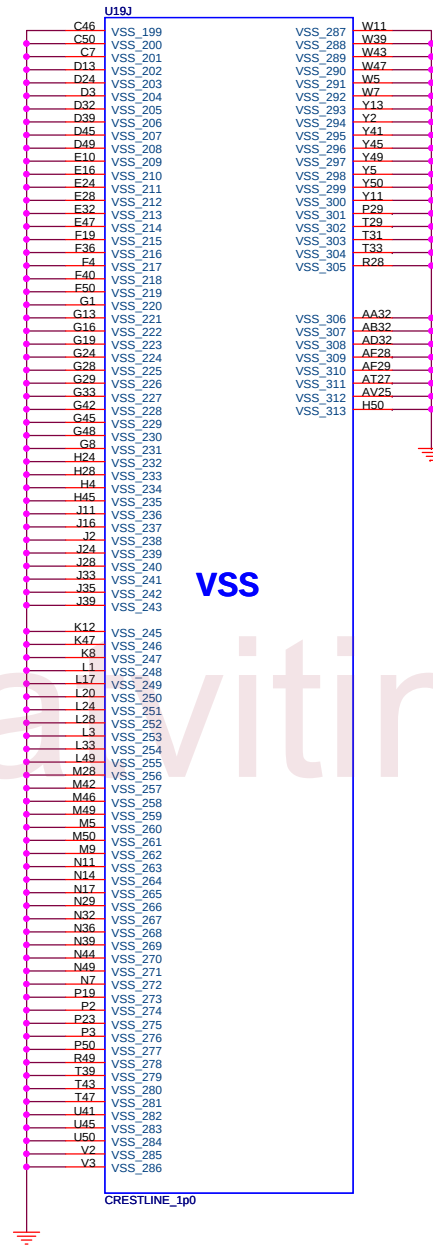
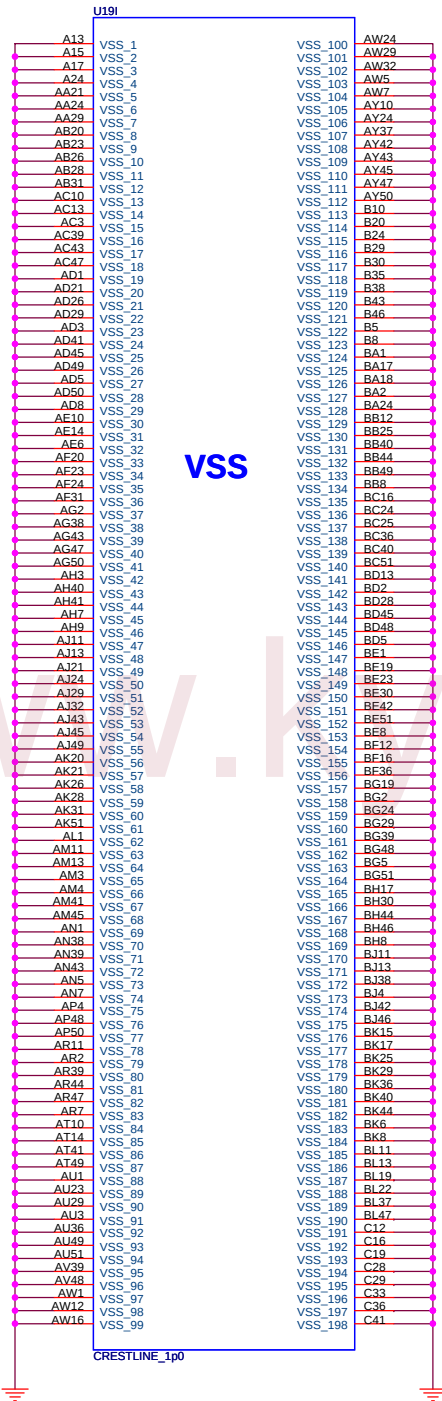


<15> DDR_B_D[0..63]



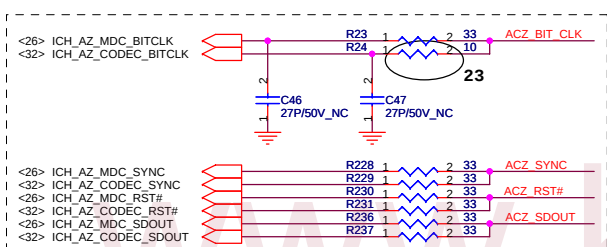
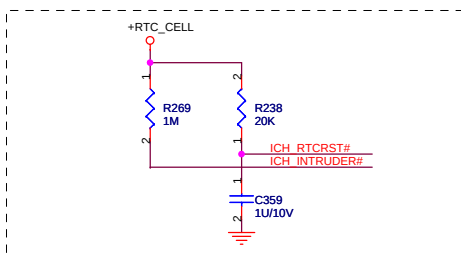
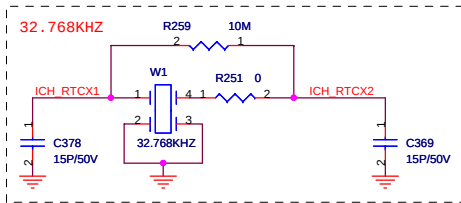


Title			
Crestline (POWER)			
Size	Document Number		Rev
	M-08		0.1
Date:	Monday, March 05, 2007	Sheet	9 of 51

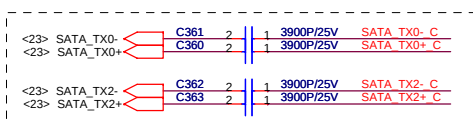


DELL CONFIDENTIAL/PROPRIETARY

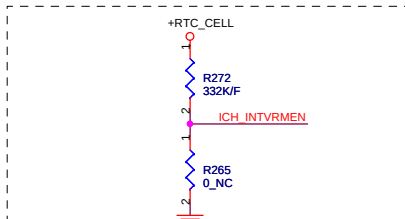
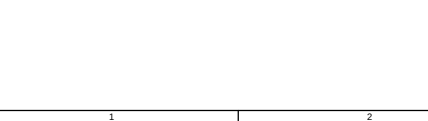
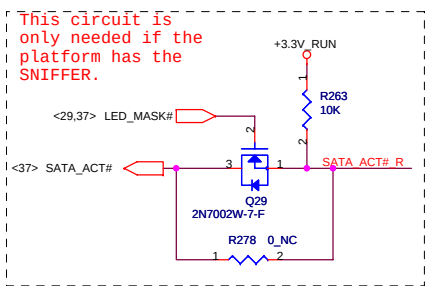
Title Crestline (VSS)		
Size M-08	Document Number M-08	Rev 0.1
Date Monday, March 05, 2007	Sheet 10	of 51



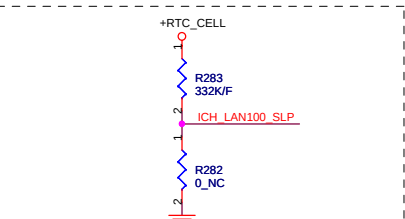
Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R23, R228, R230 & R236 should equal distance to the T split trace point as R24, R229, R231 & R237 respectively. Basically, keep the same distance from T for all series termination resistors.



Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.

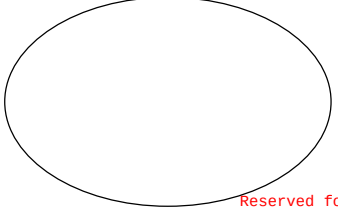
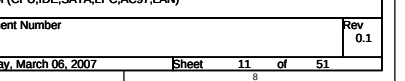
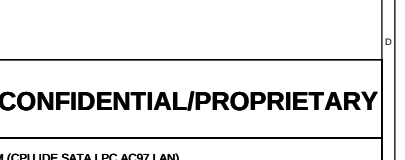
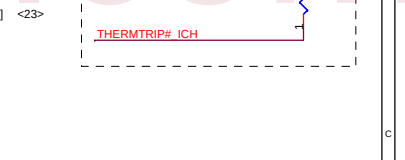
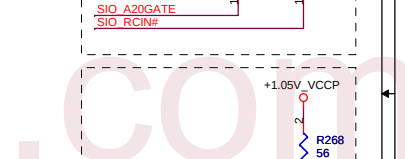
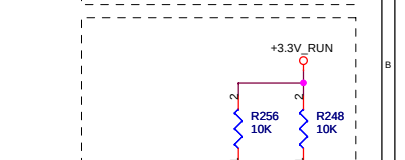
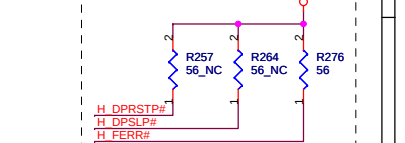
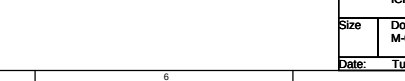
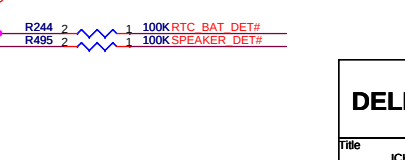
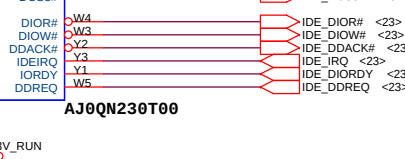
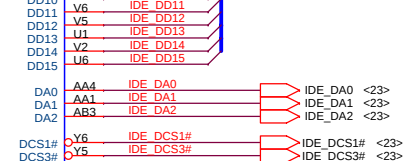
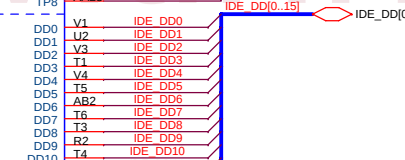
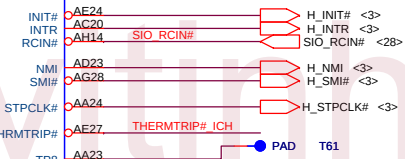
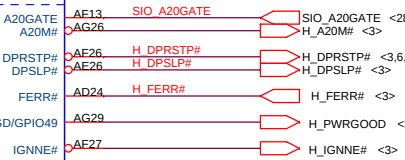
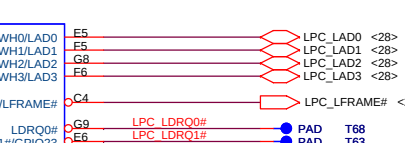
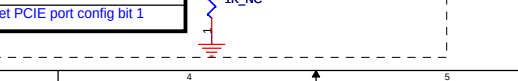
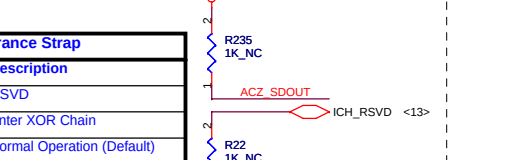
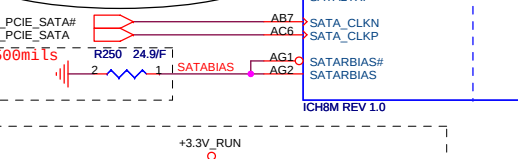
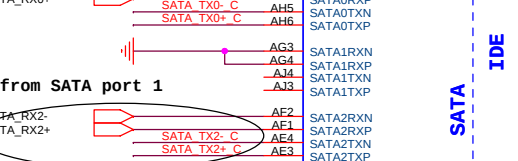
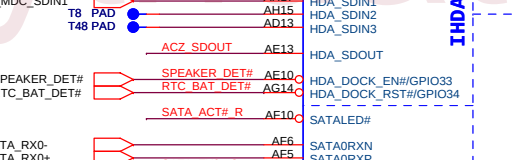
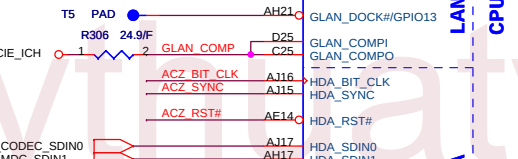
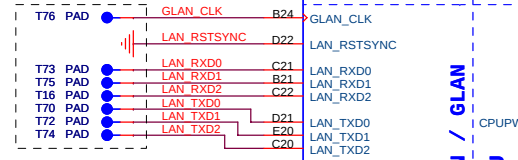


ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)		
ICH_INTVRMEN	Low = Internal VR Disabled	High = Internal VR Enabled(Default)

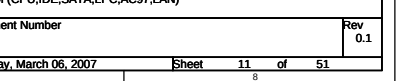
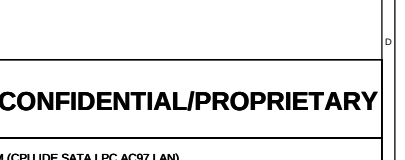
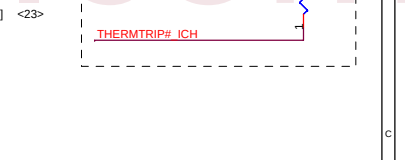
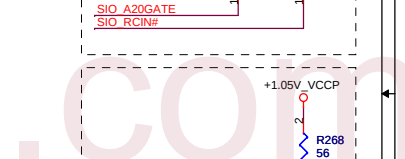
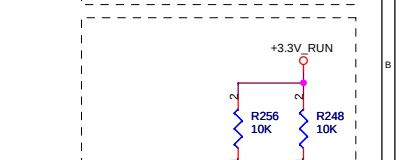
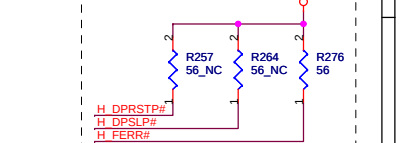
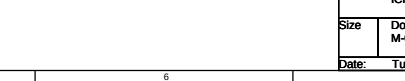
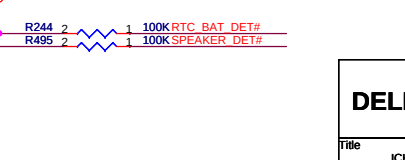
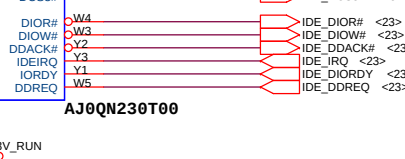
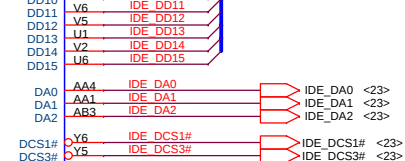
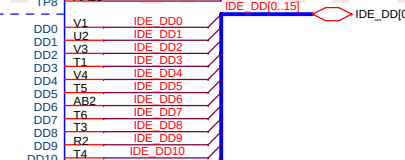
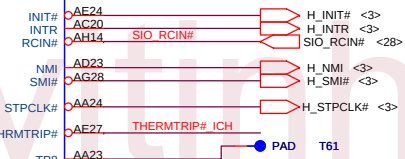
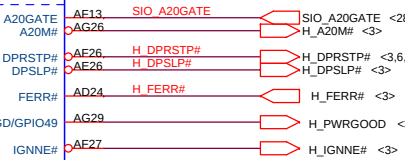
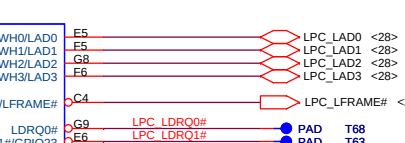
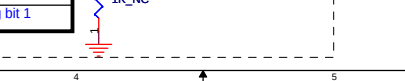
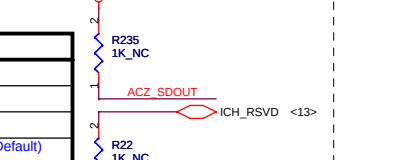
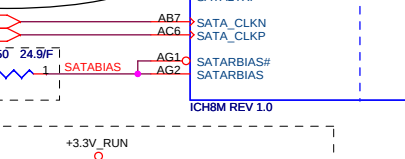
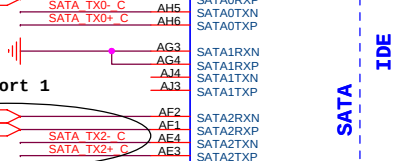
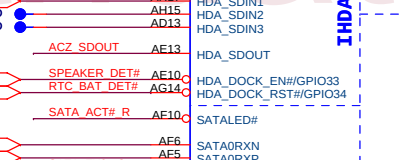
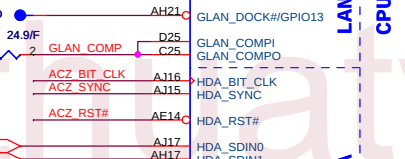
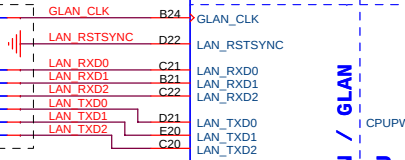
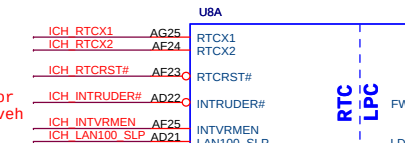
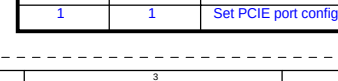
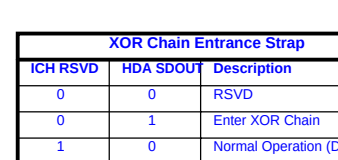
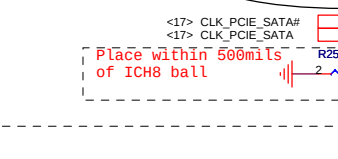
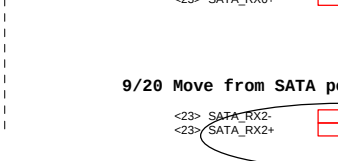
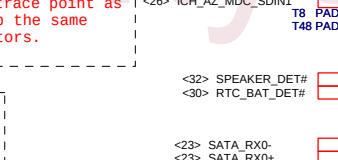
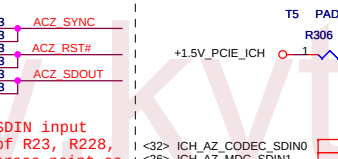
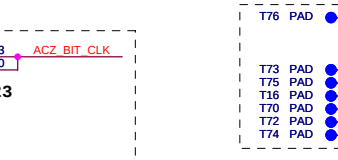


ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)		
ICH_LAN100_SLP	Low = Internal VR Disabled	High = Internal VR Enabled(Default)

Reserved for Intel Nineveh design.



Reserved for Intel Nineveh design.

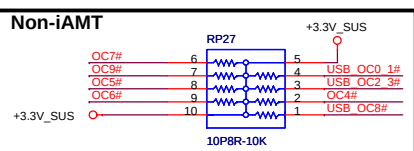


XOR Chain Entrance Strap		
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

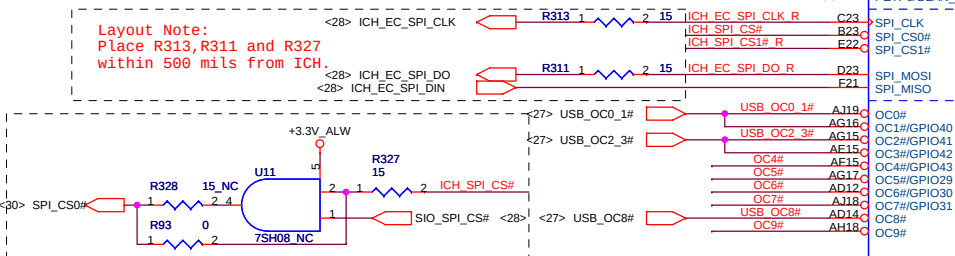
DELL CONFIDENTIAL/PROPRIETARY

Title ICH8-M (CPU,IDE,SATA,LPC,AC97,LAN)		
Size M-08	Document Number	Rev 0.1
Date: Tuesday, March 06, 2007	Sheet 11	of 51

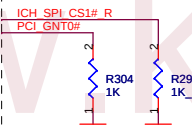
<25>	PCIE_TX1-		C90	1	2	0.1U/10V	PCIE_TXN1 C
<25>	PCIE_TX1+		C91	1	2	0.1U/10V	PCIE_TXP1 C
<24>	PCIE_TX2-		C101	1	2	0.1U/10V	PCIE_TXN2 C
<24>	PCIE_TX2+		C106	1	2	0.1U/10V	PCIE_TXP2 C
<24>	PCIE_TX3-		C114	1	2	0.1U/10V	PCIE_TXN3 C
<24>	PCIE_TX3+		C116	1	2	0.1U/10V	PCIE_TXP3 C
<26>	PCIE_TX4-		C127	1	2	0.1U/10V	PCIE_TXN4 C
<26>	PCIE_TX4+		C120	1	2	0.1U/10V	PCIE_TXP4 C



Layout Note:
Place R313, R311 and R327
within 500 mils from ICH.



OC4#	C876	1	2	0.1U/10V
OC5#	C871	1	2	0.1U/10V
OC6#	C872	1	2	0.1U/10V
OC7#	C873	1	2	0.1U/10V
OC9#	C878	1	2	0.1U/10V
USB OC8#	C874	1	2	0.1U/10V
USB OC0 1#	C875	1	2	0.1U/10V
USB OC2 3#	C877	1	2	0.1U/10V



Boot BIOS Strap			
		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

Short F2 and F3 at the package
and keep length to less than
500mils. Trace Impedance
should be 60ohms +/- 15%.

LOM	REQ0	GNT0	PIRQB
1394/MediaCard	REQ1	GNT1	PIRQC PIRQD

CB, NR, DCIF, PST#

A circuit diagram showing a 10k resistor connected to four signals: SB, NB, PCIE, and RST#. The resistor is represented by a zigzag line with terminals labeled 1 and 2. Terminal 1 is connected to ground, and terminal 2 is connected to the four signals.

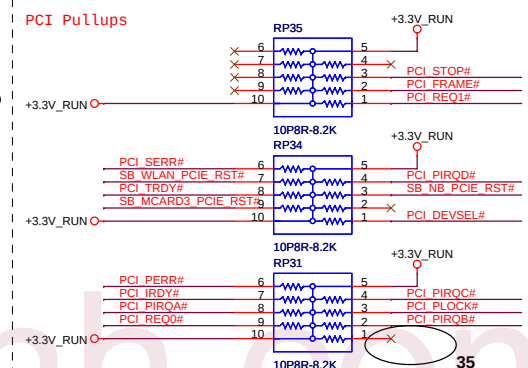
A16 away override strap.

RST#	Low = A16 swap override enabled. High = Default.
------	---

SB_MCAR3D_PCIE_RST#	R291	2	1	20K
SB_WWAN_PCIE_RST#	R314	2	1	20K
SB_WLAN_PCIE_RST#	R300	2	1	20K
SB_LOM_PCIE_RST#	R324	2	1	20K
SB_NB_PCIE_RST#	R302	2	1	20K

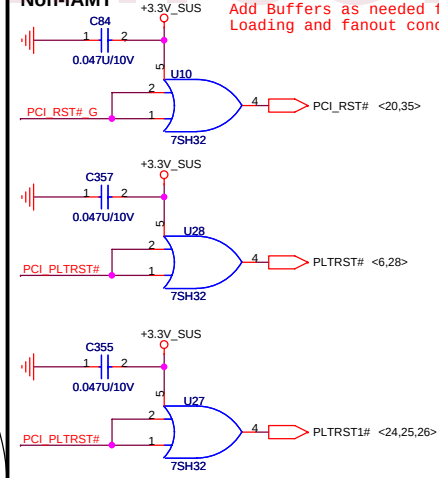
BIOS should not enable the internal GPIO pull up resistor.

Reserved for EMI.
Place resistor and cap
close to ICH.



Non-iAMT

Add Buffers as needed for Loading and fanout concerns.



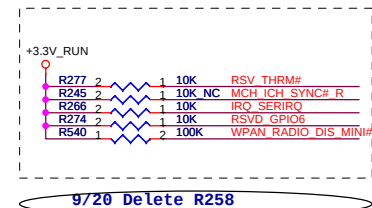
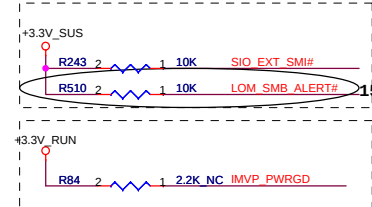
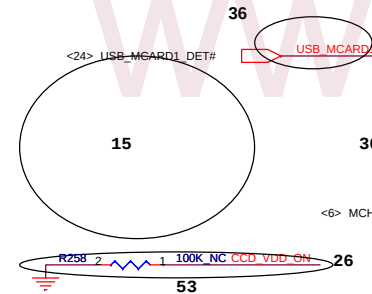
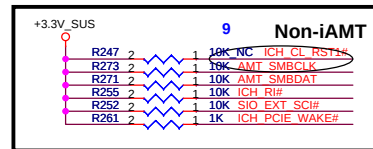
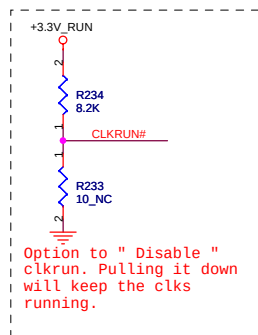
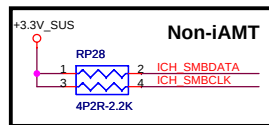
```
PCI_PIRQB: for LOM
PCI_PIRQC: for Media Card
PCI_PIRQD: for 1394
```

ICH8M REV 1.0

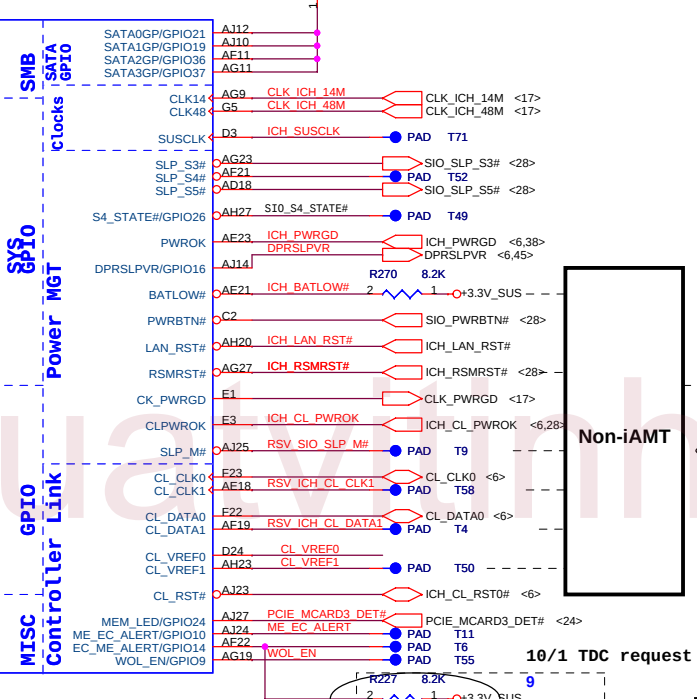
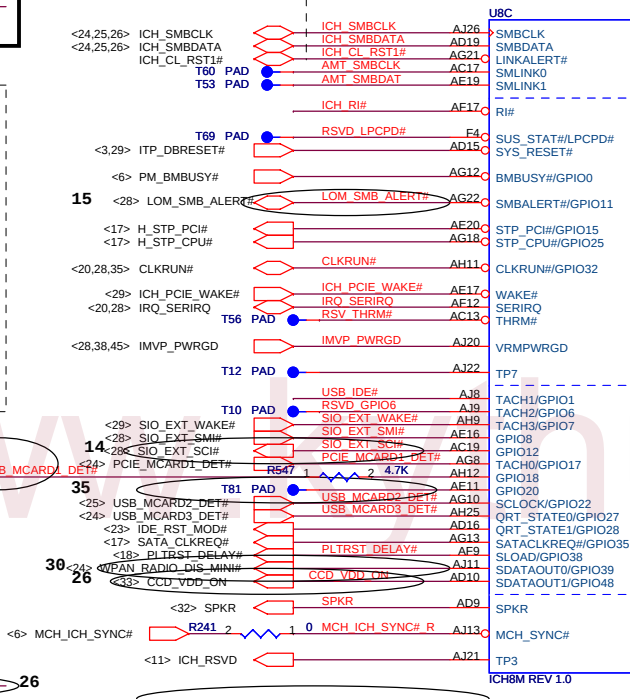
35

DELL CONFIDENTIAL/PROPRIETARY

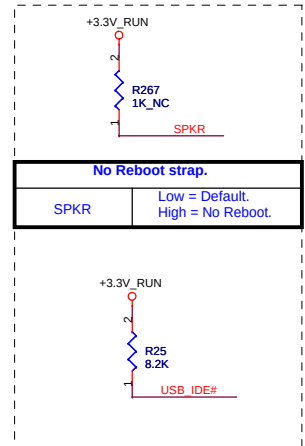
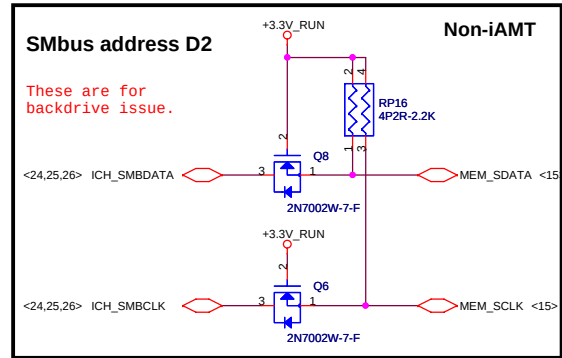
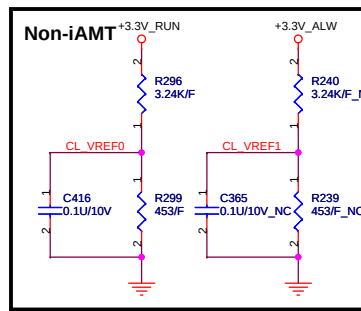
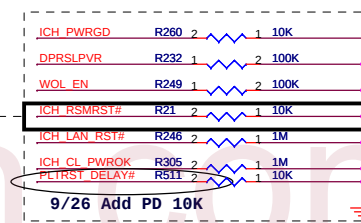
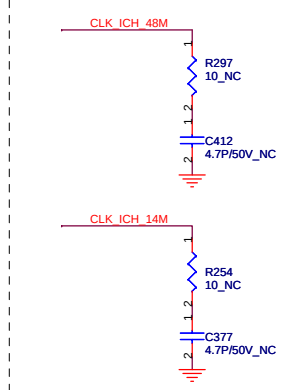
Title			
ICH8-M (USB,DMI,PCIE,PCI)			
Size	Document Number	Rev	
	M-08	0.1	
Date:	Tuesday, March 06, 2007	Sheet	12 of 51

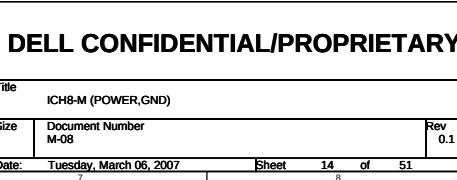


9/20 Delete R258

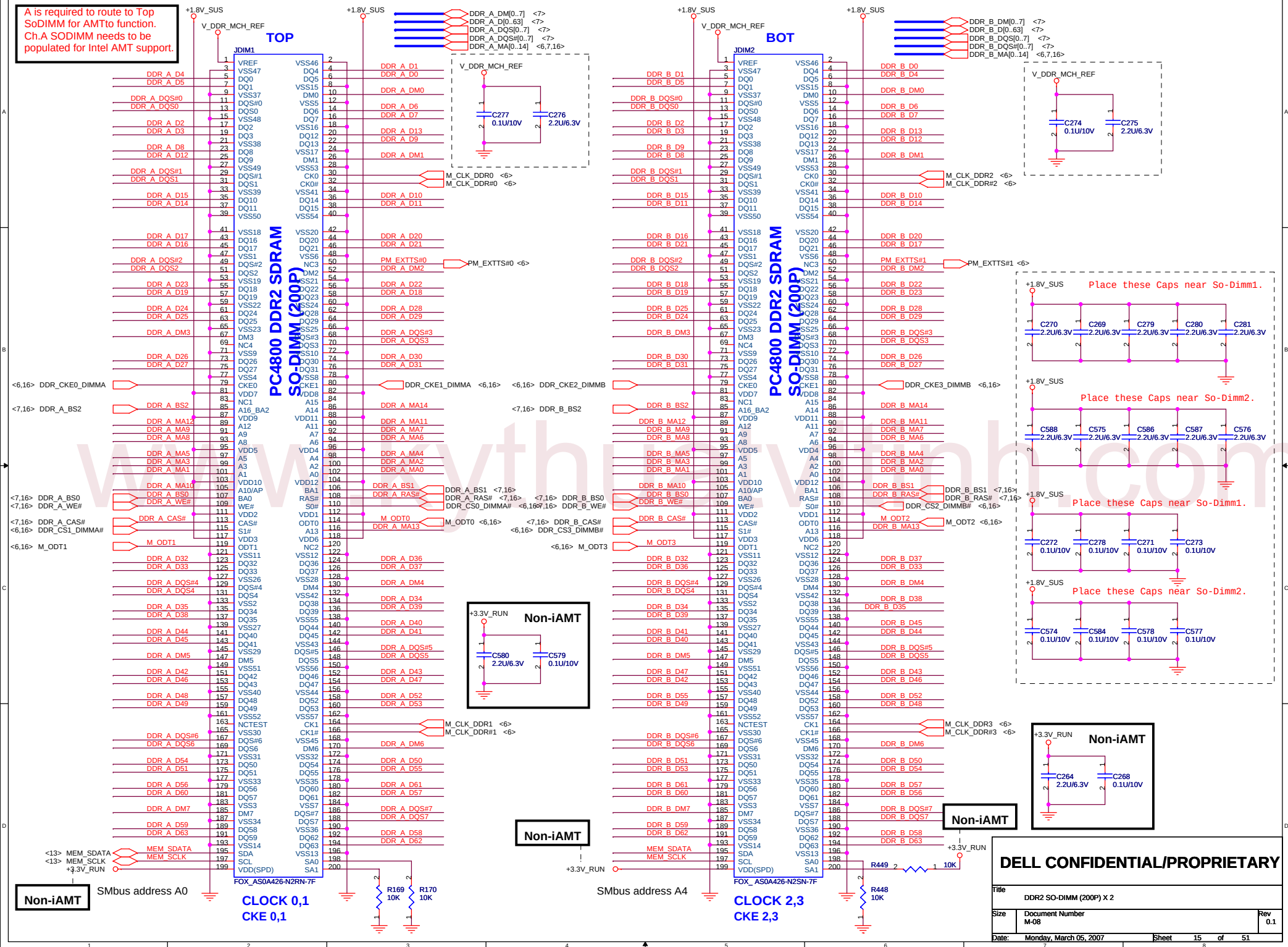


Place these close to ICH7.



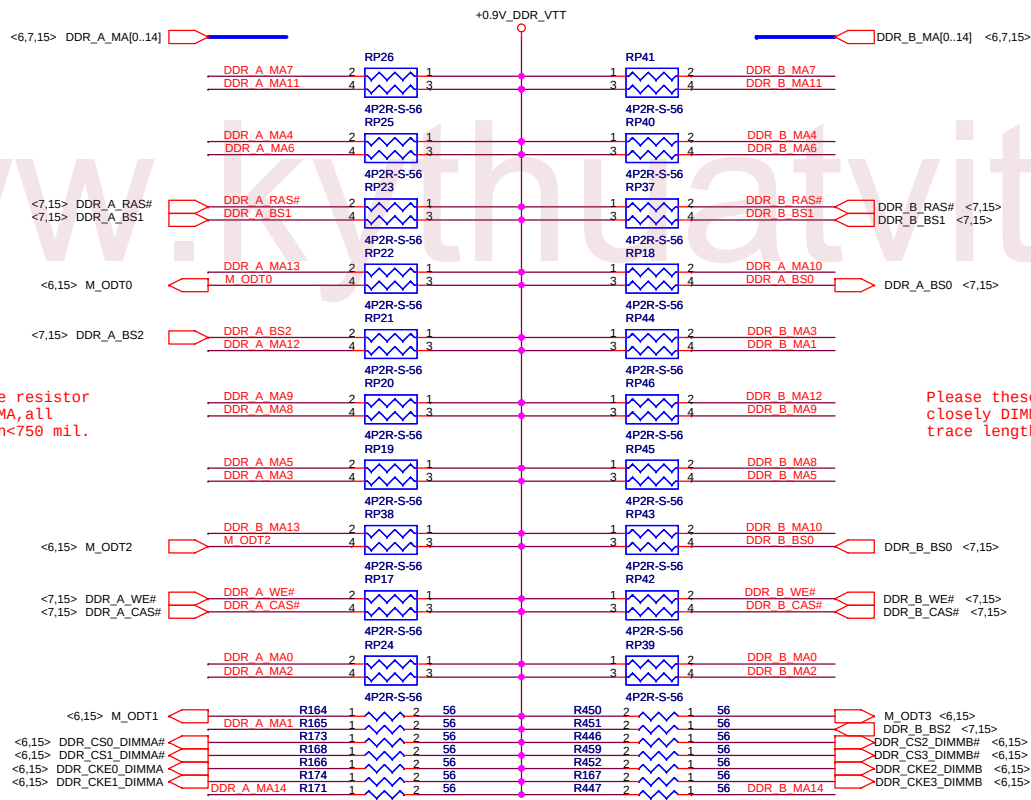


A is required to route to Top SoDIMM for AMT to function. Ch.A SODIMM needs to be populated for Intel AMT support.



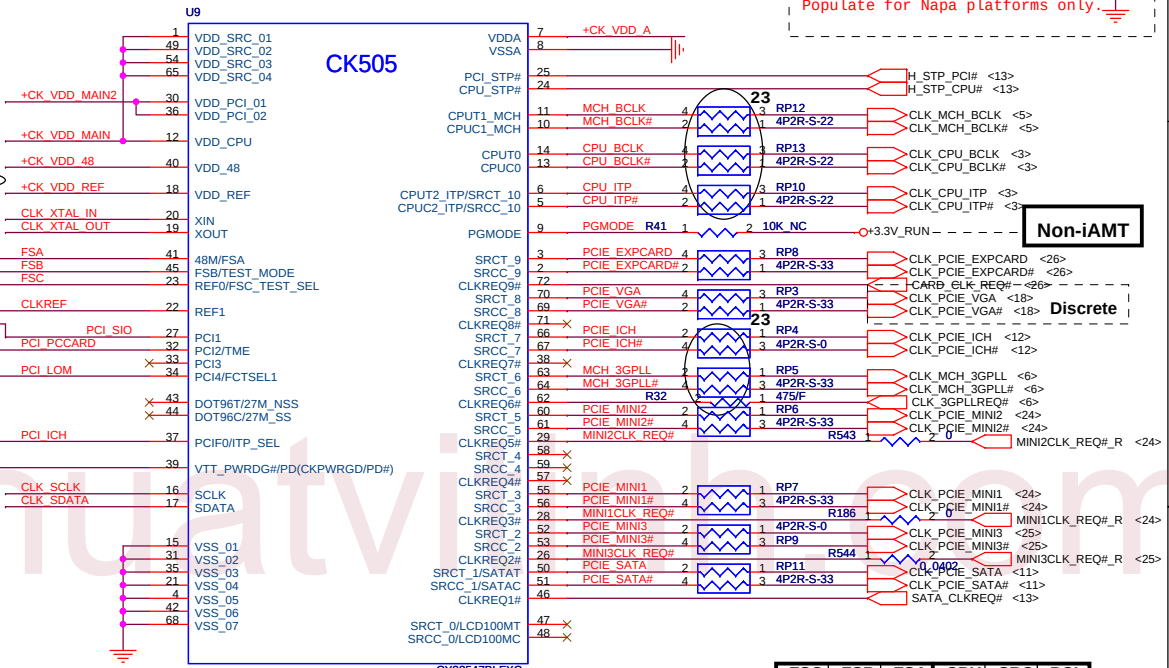
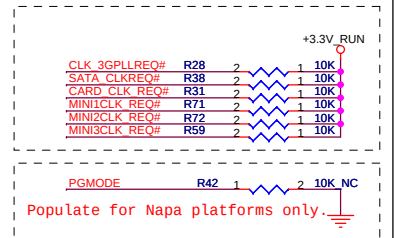
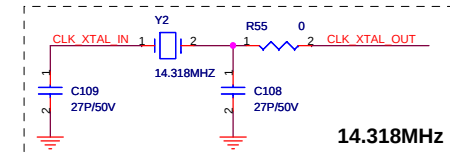
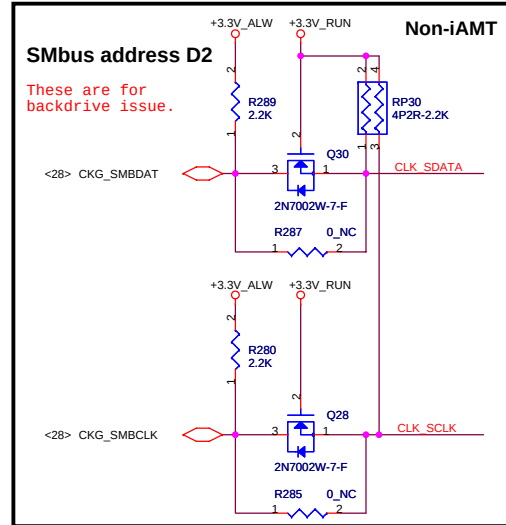
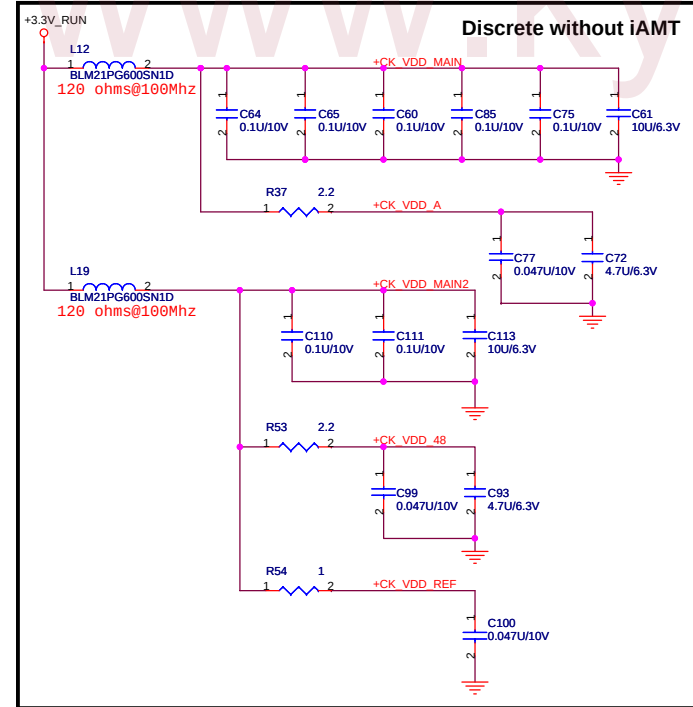
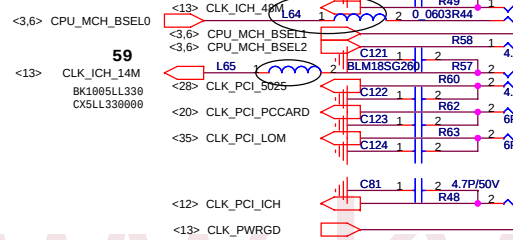
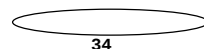
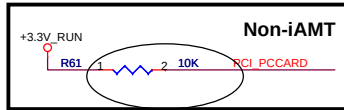
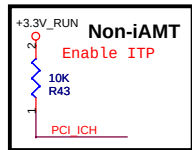
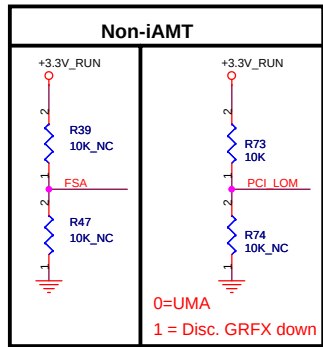
DELL CONFIDENTIAL/PROPRIETARY

Title				DDR2 SO-DIMM (200P) X 2			
Size		Document Number M-08				Rev 0.1	
Date:		Monday, March 05, 2007		Sheet		15 of 51	



Please these resistor
closely DIMMB,all
trace length<750 mil.

Title			
DDR2 RES ARRAY			
Size	Document Number		Rev
	M-08		0.1
Date:	Monday, March 05, 2007	Sheet	16 of 51



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

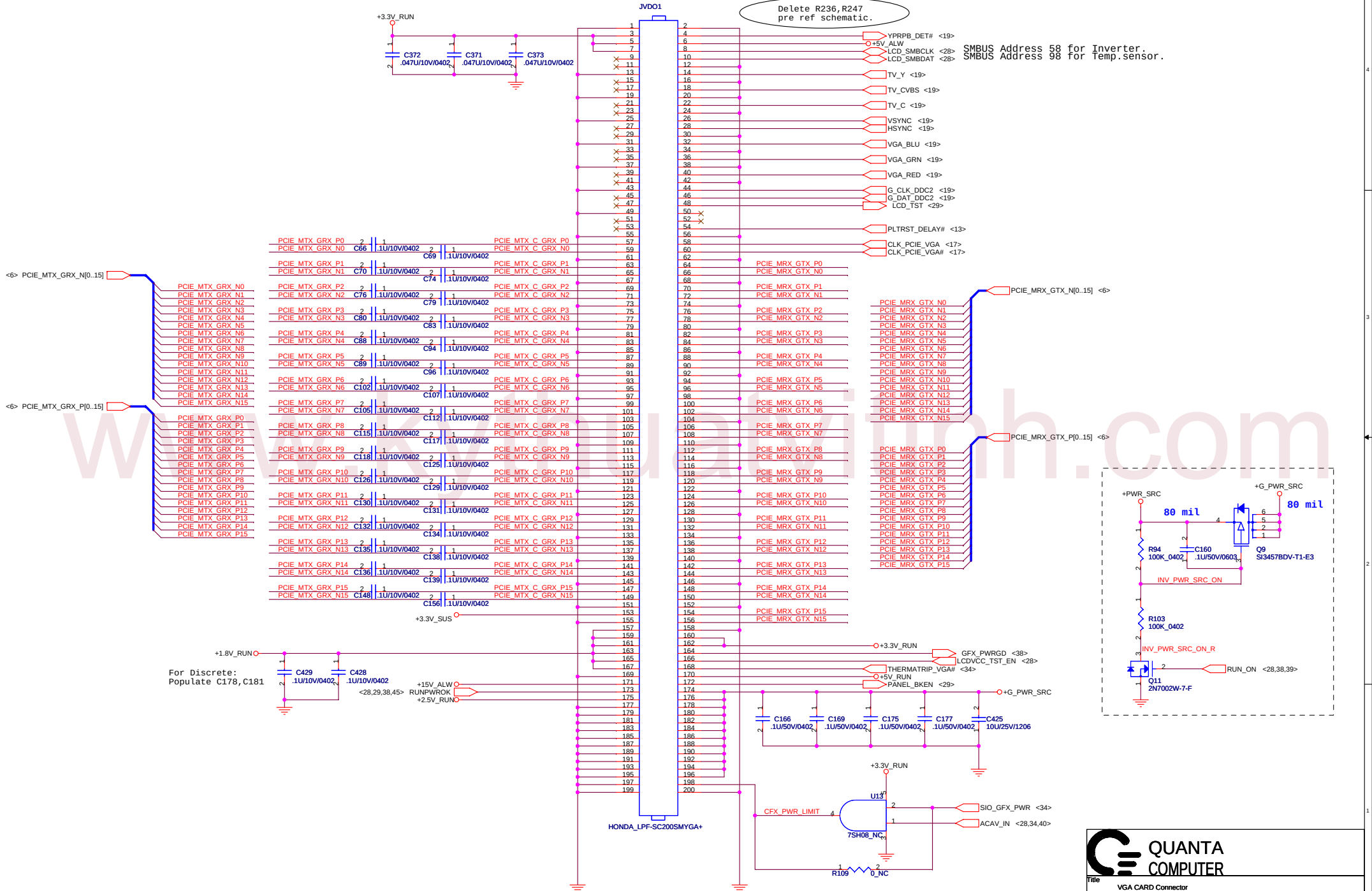
PCI_LOM = FCTSEL1

FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1= Disc. GRFX down	27Mout	27MSSout	SRC0	SRC0

YPRPB_DET: SIGNAL FROM SVIDEO CONNECTOR,
TO SWITCH TO COMPONENT OUT.

Delete R236,R247
pre ref schematic.

SMBUS Address 58 for Inverter.
SMBUS Address 98 for Temp.sensor.



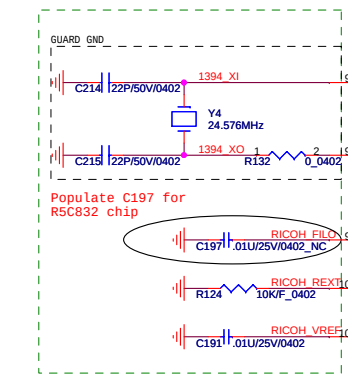
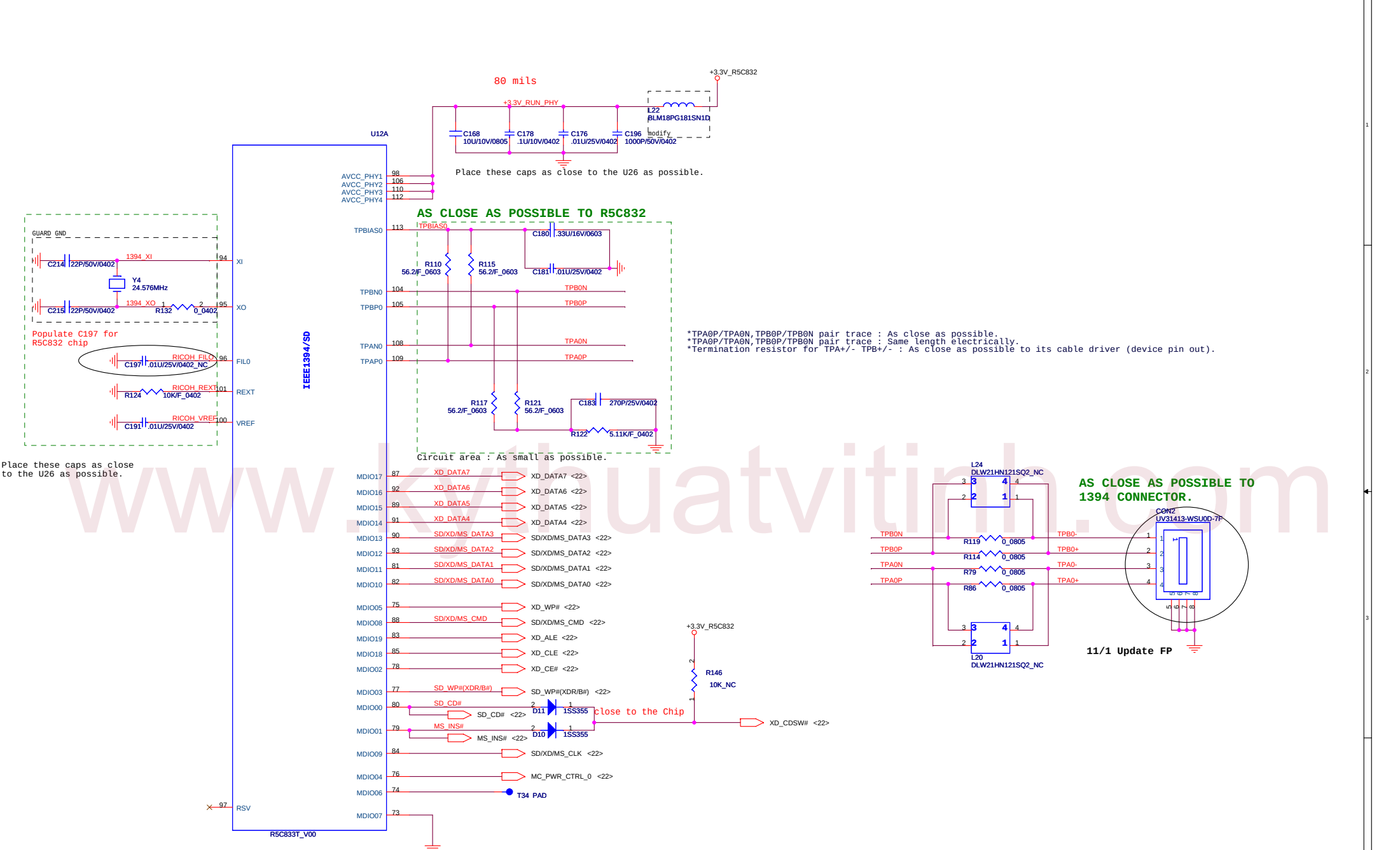
QUANTA
COMPUTER

Title
VGA CARD Connector

Size
FM1

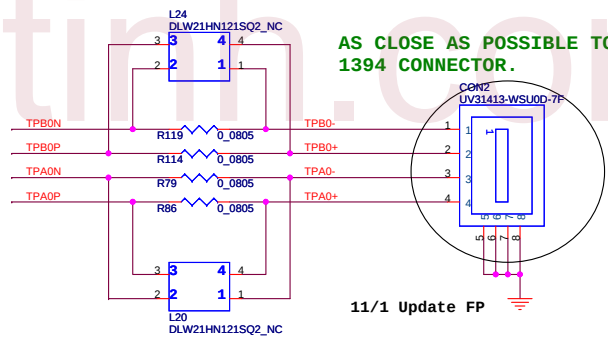
Date: Monday, March 05, 2007 Sheet 18 of 51

Rev
0.1



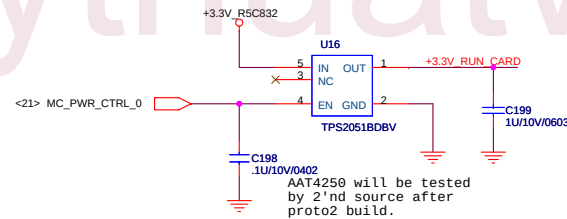
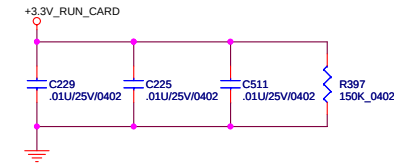
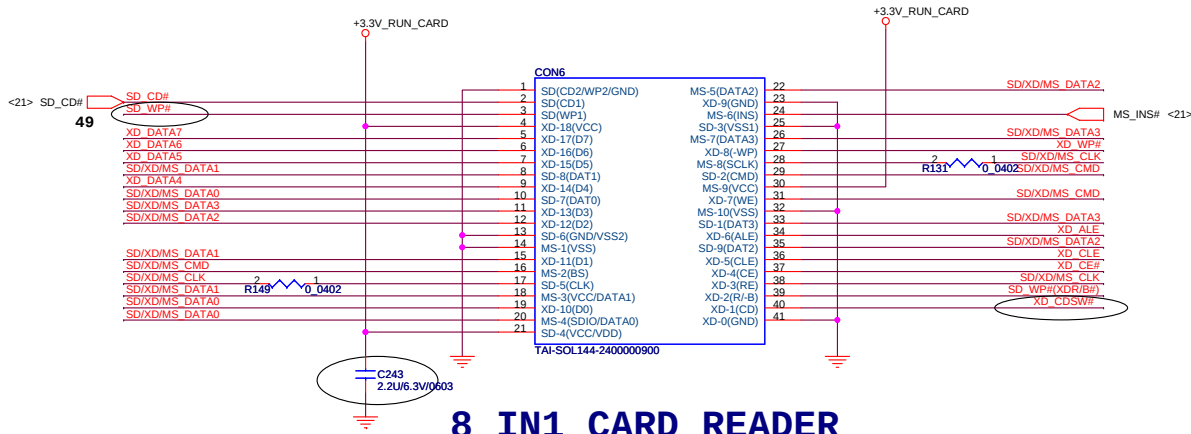
Place these caps as close to the U26 as possible.

*TPA0P/TPA0N, TPB0P/TPB0N pair trace : As close as possible.
*TPA0P/TPA0N, TPB0P/TPB0N pair trace : Same length electrically.
*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

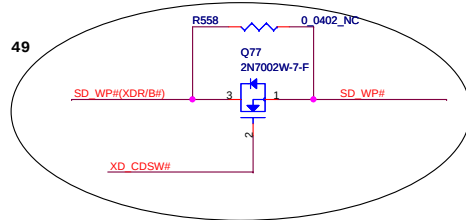


AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.

11/1 Update FP

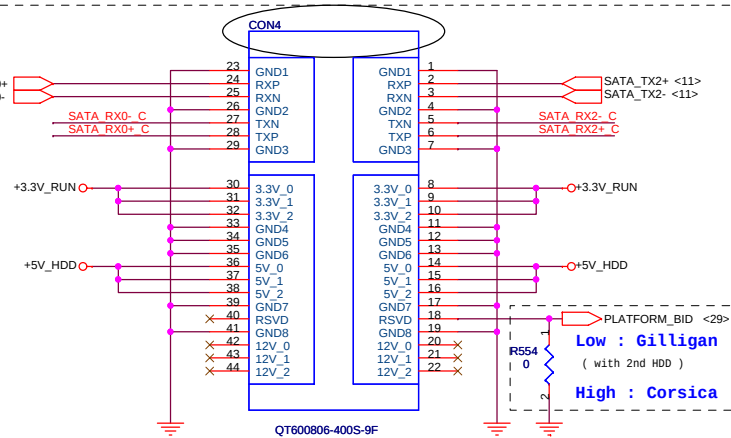


SD Protect

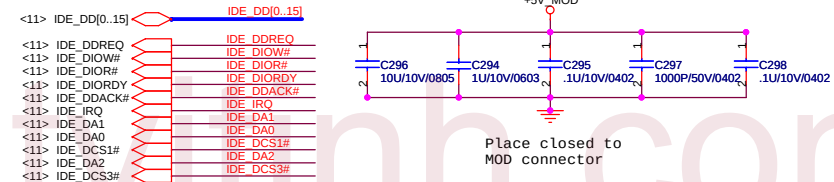
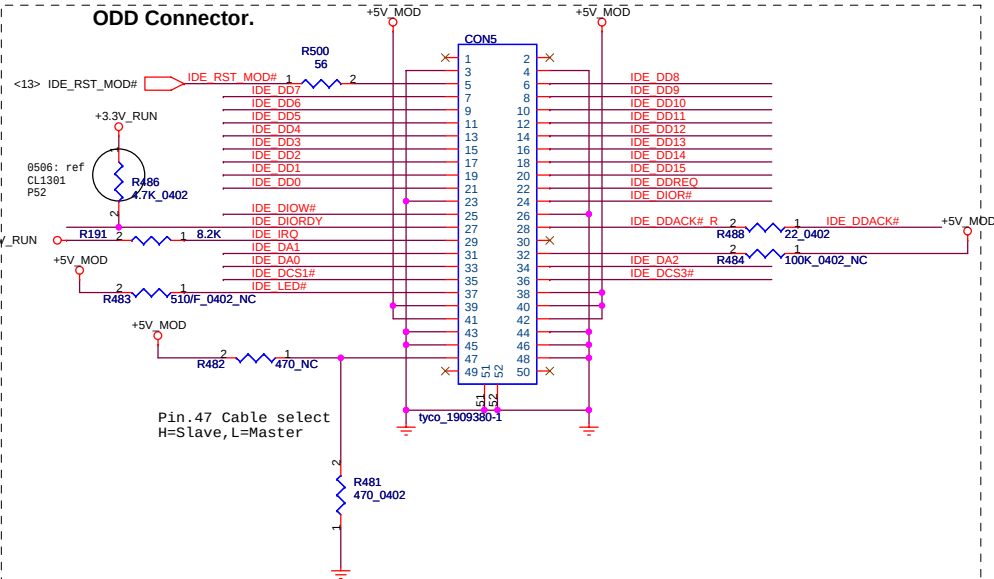


SATA 1 & 2 Connector.

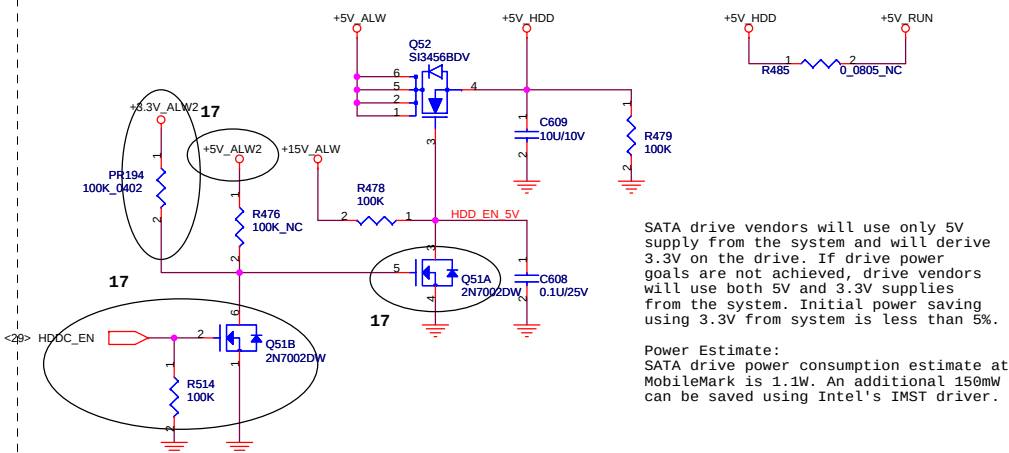
Corsica
DFHS22FR012



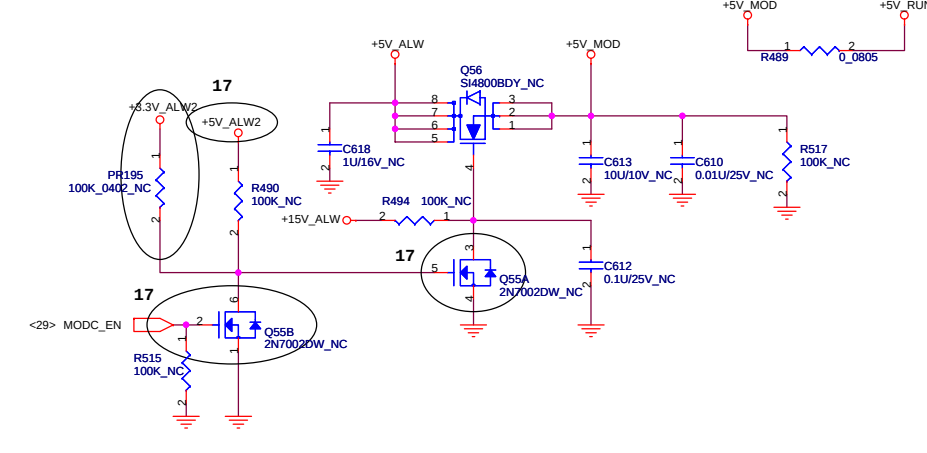
ODD Connector.



SATA PWR

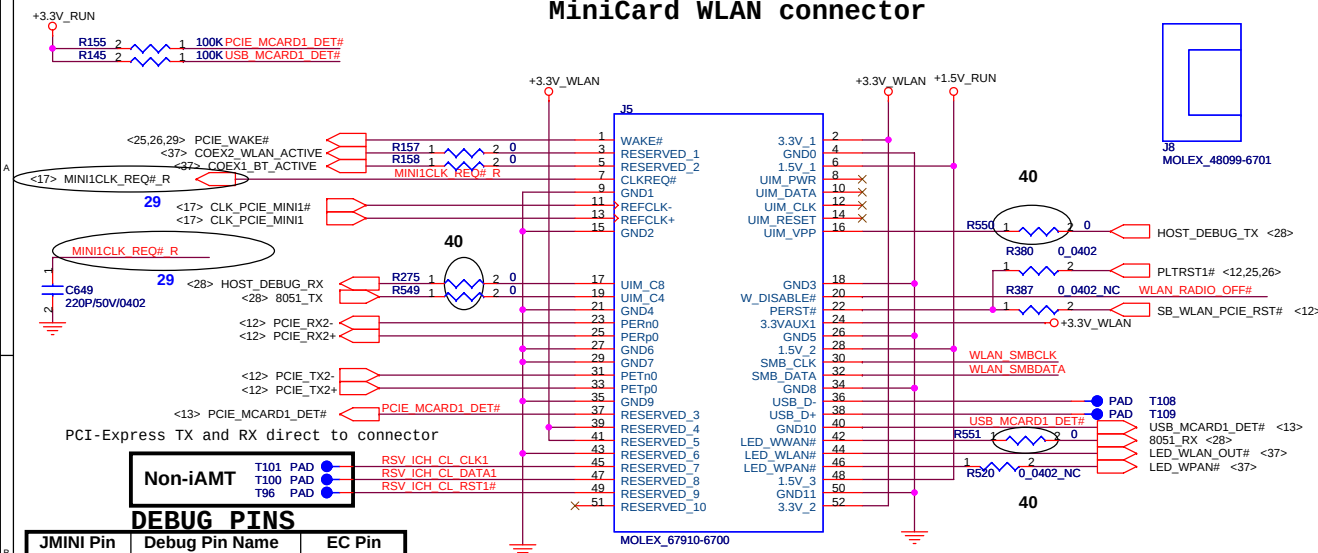


ODD PWR



Title SATA (HDD&CD_ROM)		
Size M-08	Document Number	Rev 0.1
Date: Monday, March 05, 2007	Sheet 23	of 51

MiniCard WLAN connector

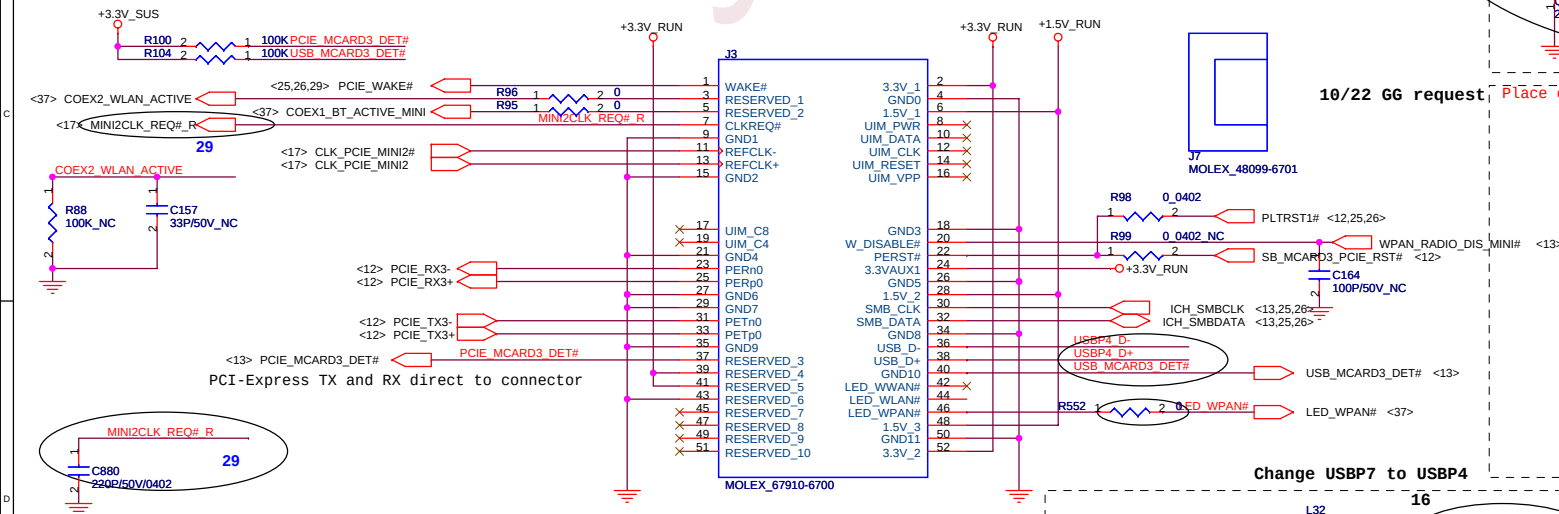


Non-IAMT

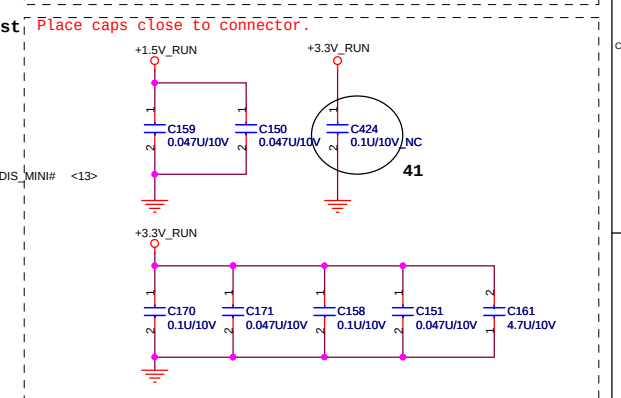
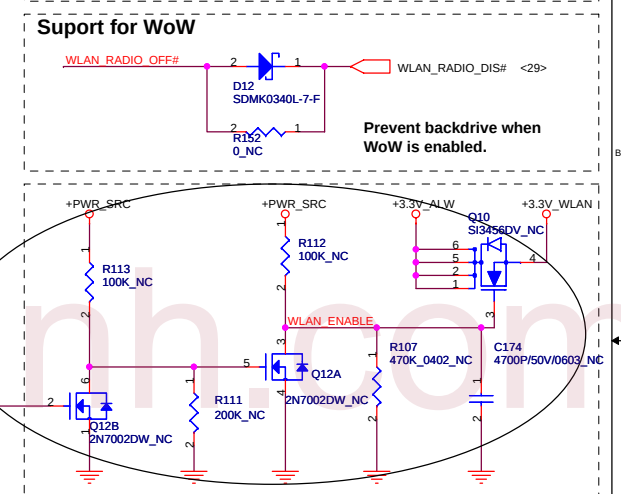
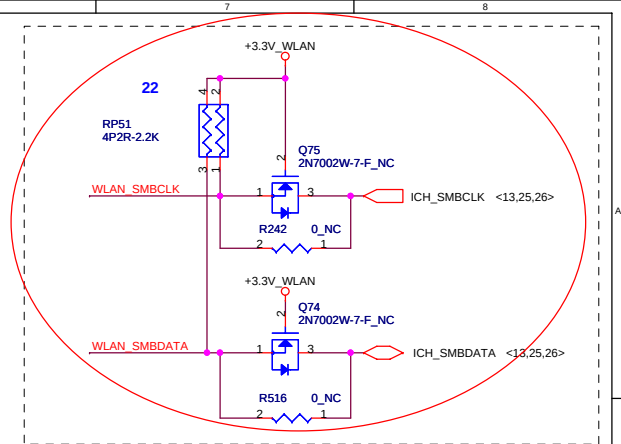
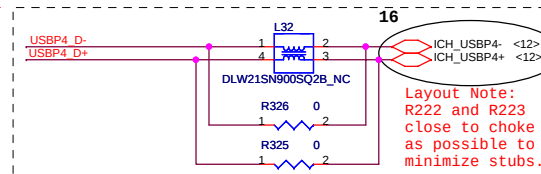
DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

MiniCard WPAN connector

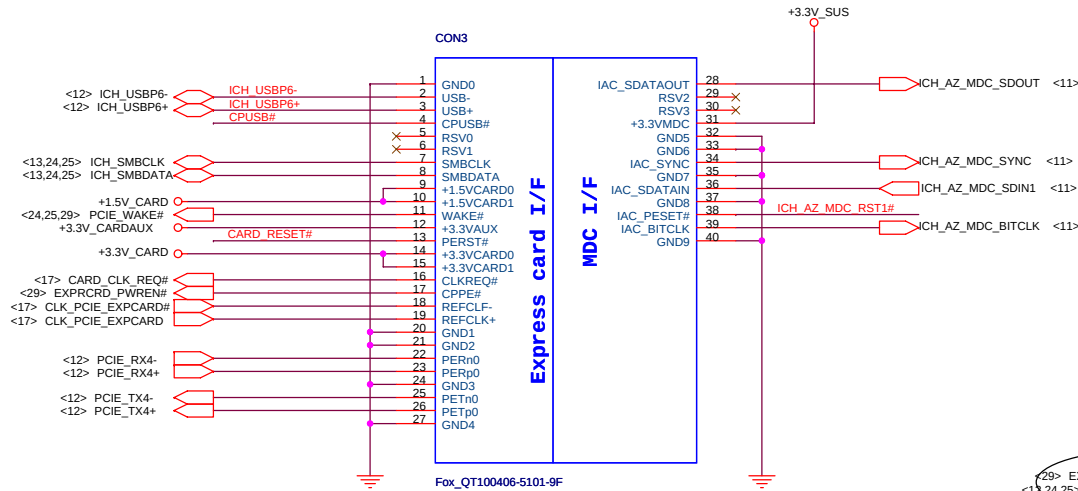


Change USBP7 to USBP4

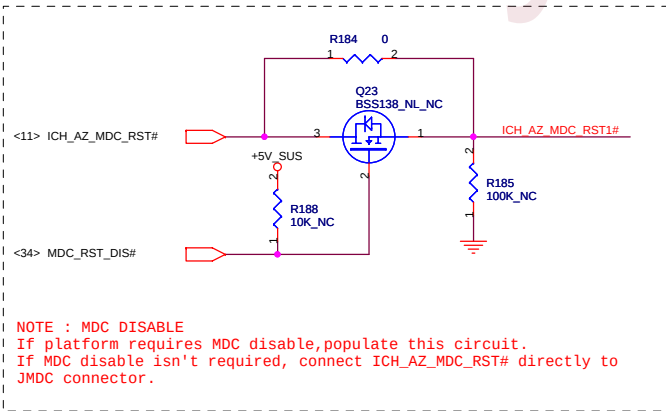
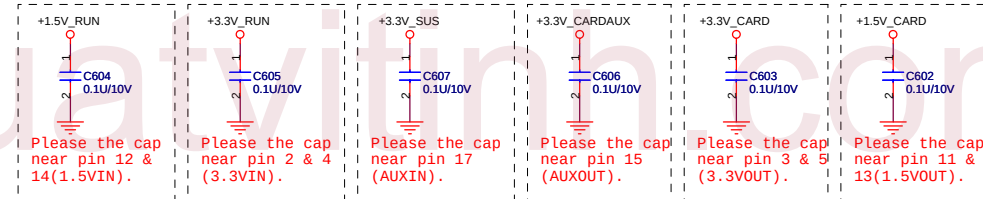
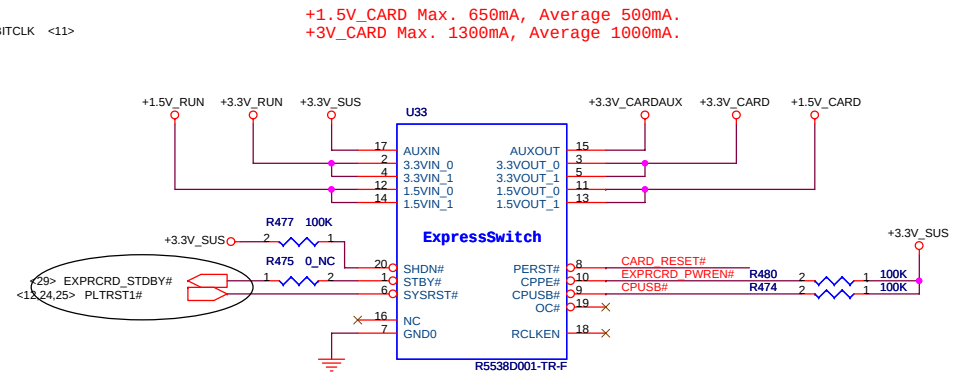


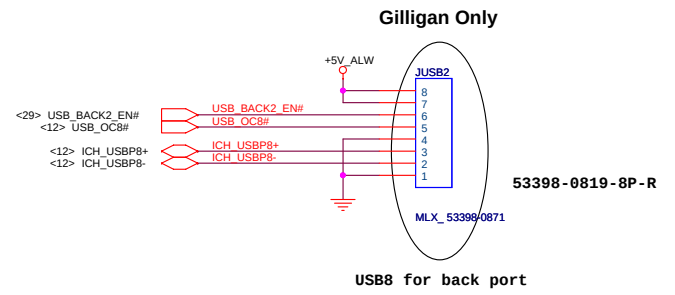
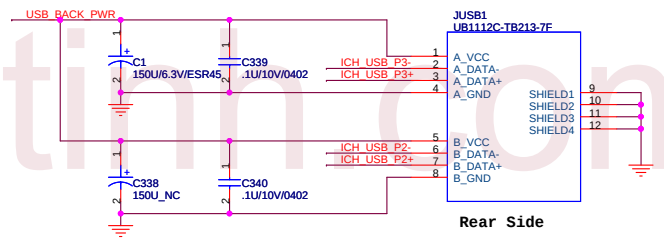
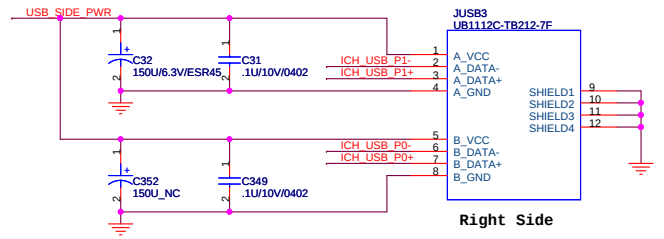
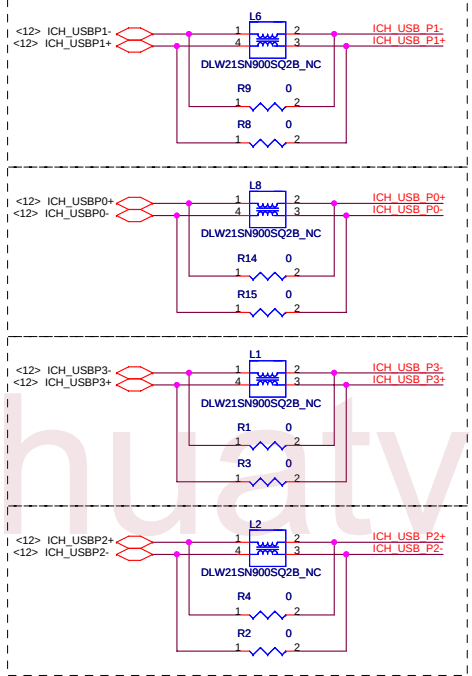
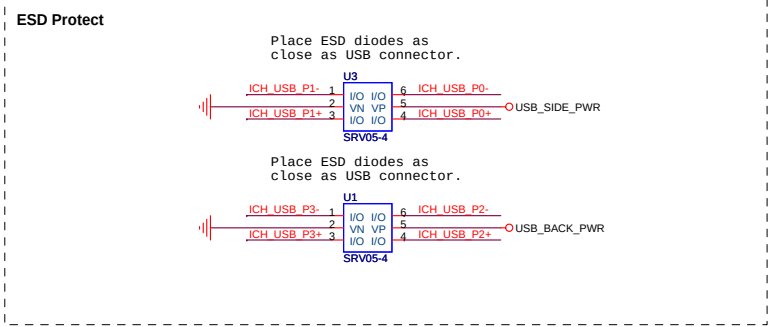
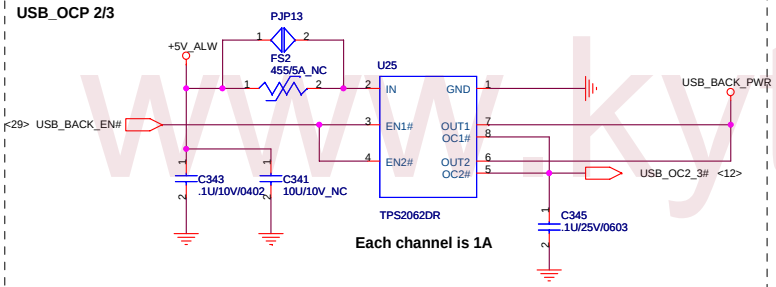
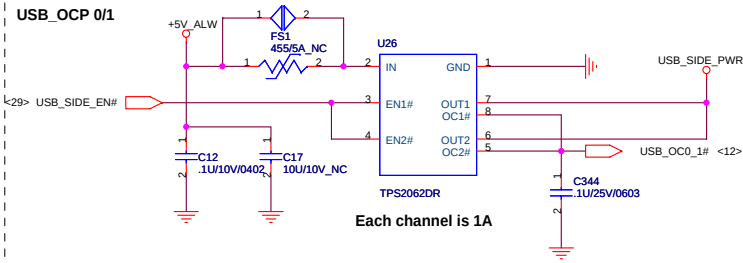
Title		
MINI-PCI		
Size	Document Number	Rev
M-08		0.1
Date:	Monday, March 05, 2007	Sheet 24 of 51

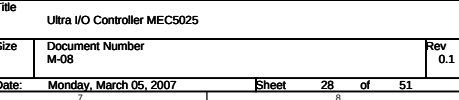
EXPRESS+MDC



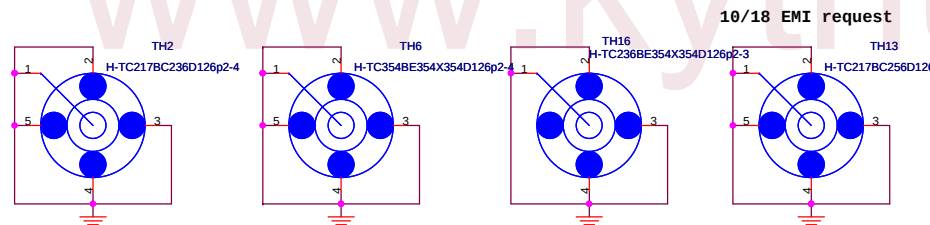
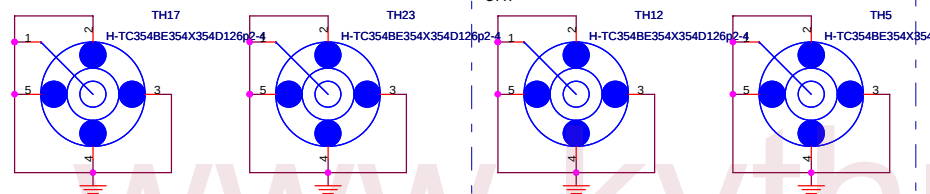
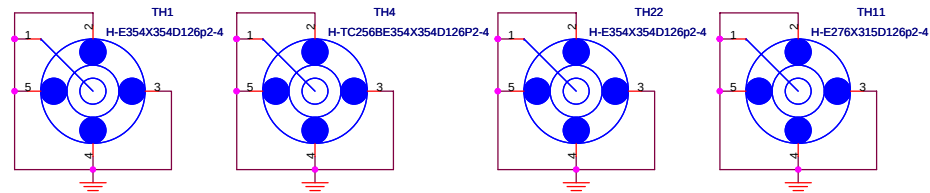
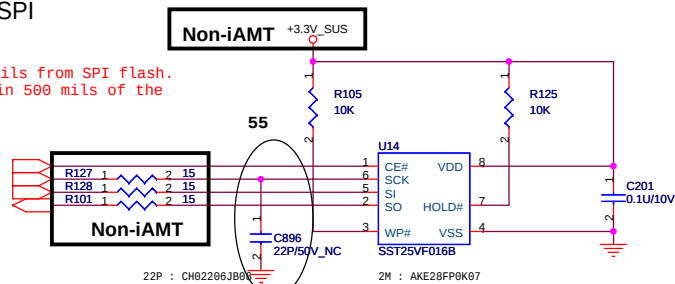
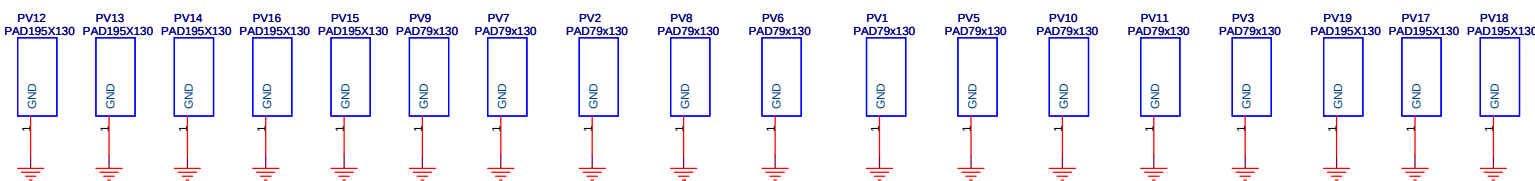
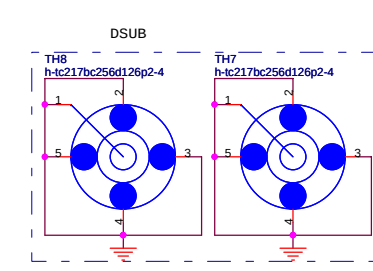
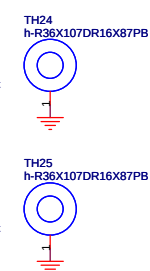
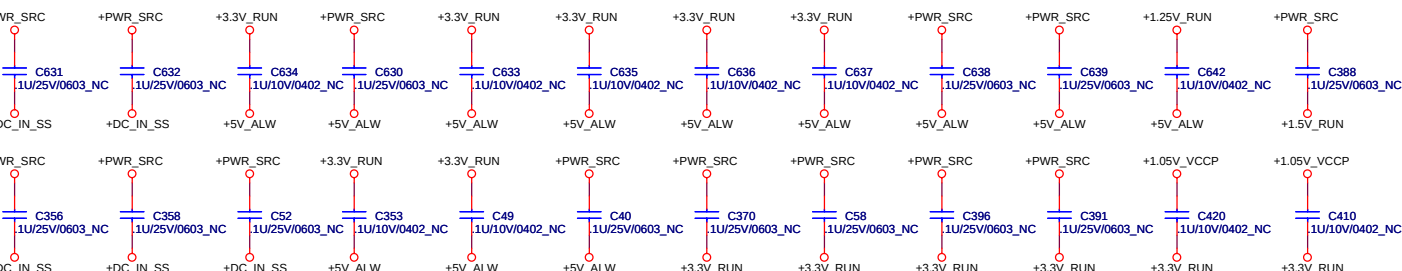
Update PN







Layout Note:
Place R471 within 500 mils from SPI flash.
Place R498 & R534 within 500 mils of the
MEC5025.

[illegible]

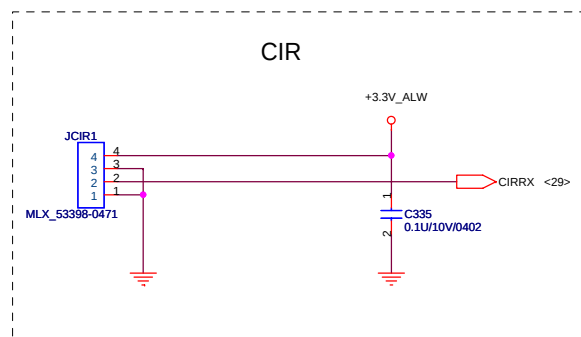
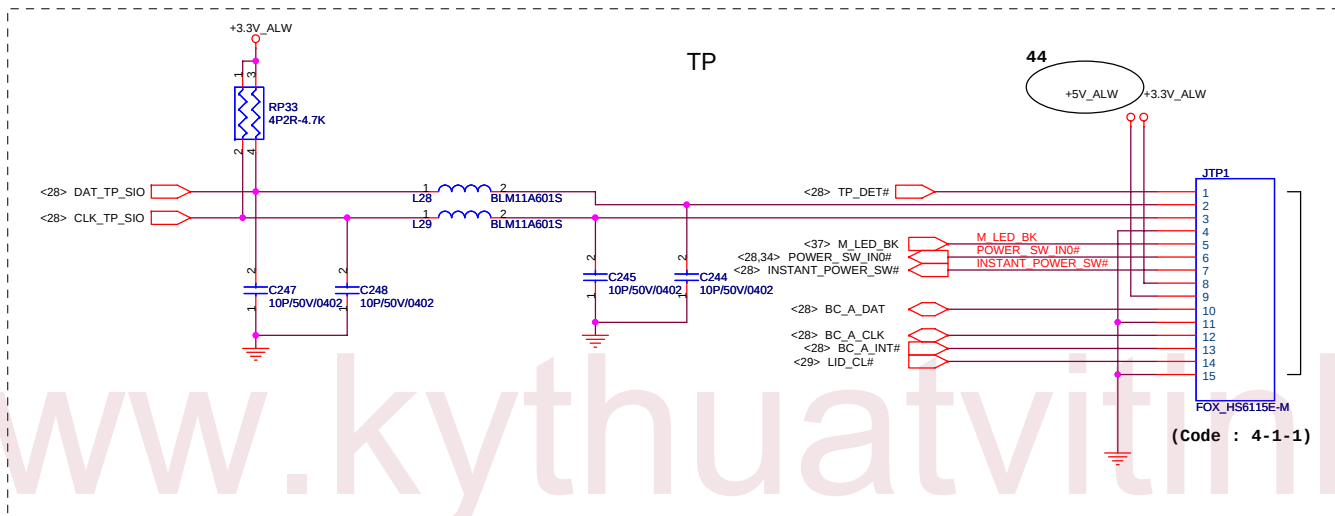
Title **FLASH, RTC & KC**

Size	Document Number M-08
------	-------------------------

Rev	0.1
-----	-----

Date: Monday, March 05, 2007

Sheet 30 of 51



INTERNAL SPEAKER AMP Update PN

52

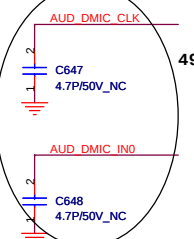
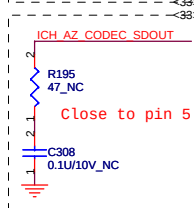
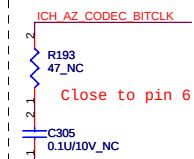
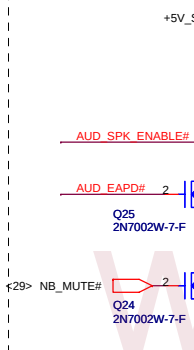
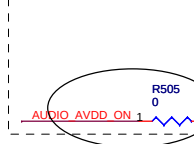
Package 1206 for THD+N performance for Vista Logo requirements.

AUD LINE OUT L C306 2 0.033U/25V/X7R/1206
AUD LINE OUT R C307 2 0.033U/25V/X7R/1206
AUD HP OUT L C326 2 1uF/25V/X7R/1206
AUD HP OUT R C329 2 1uF/25V/X7R/1206

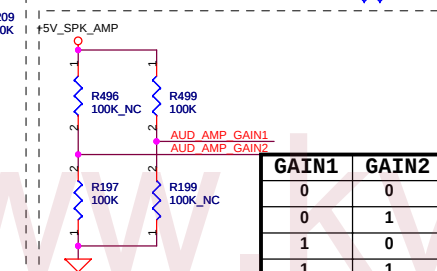
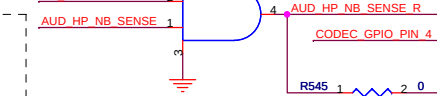
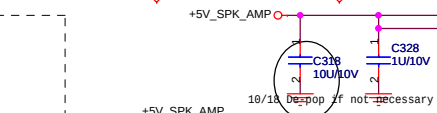
18/18 Change 2.2u if necessary

31

For MAX9789A, depop R505, pop R506.

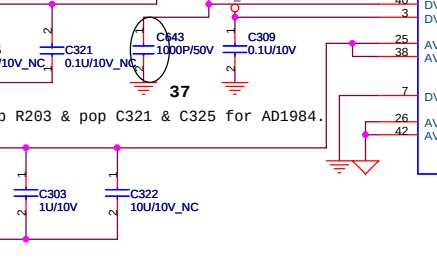
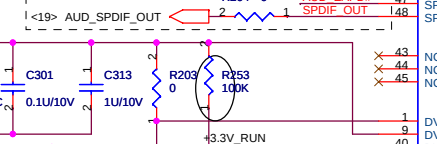


32



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

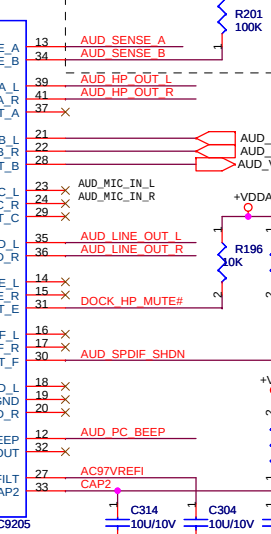
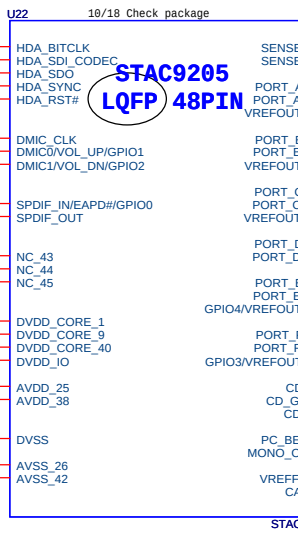
For Tuning.



Depop R203 & pop C321 & C325 for AD1984.

AZALIA (HD) CODEC

STAC9205 LQFP 48PIN

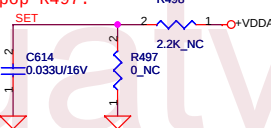


C304 must be 1U & Pop C320 & R200 for AD1984.

C1425/C331 value need to match with C326/C290. This value be chosen in PT phase.

For MAX9789A, depop C619, pop R504.

For MAX9789A, depop C614, pop R497.



REGEN

AUDIO AVDD_ON

AUDIO_AVDD_ON

REGEN

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

C1425/C331 value need to match with C326/C290. This value be chosen in PT phase.

For MAX9789A, depop C619, pop R504.

For MAX9789A, depop C614, pop R497.



REGEN

AUDIO AVDD_ON

AUDIO_AVDD_ON

REGEN

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

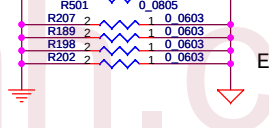
AUDIO_AVDD_ON

AUDIO_AVDD_ON

C1425/C331 value need to match with C326/C290. This value be chosen in PT phase.

For MAX9789A, depop C619, pop R504.

For MAX9789A, depop C614, pop R497.



REGEN

AUDIO AVDD_ON

AUDIO_AVDD_ON

REGEN

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

C1425/C331 value need to match with C326/C290. This value be chosen in PT phase.

For MAX9789A, depop C619, pop R504.

For MAX9789A, depop C614, pop R497.



REGEN

AUDIO AVDD_ON

AUDIO_AVDD_ON

REGEN

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

AUDIO_AVDD_ON

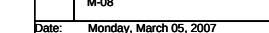
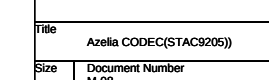
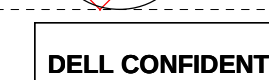
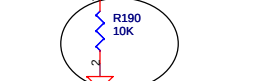
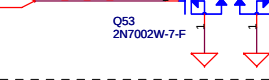
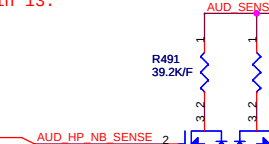
AUDIO_AVDD_ON

AUDIO_AVDD_ON

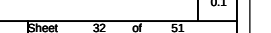
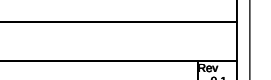
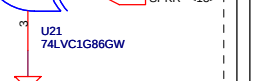
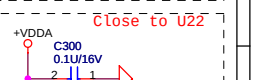
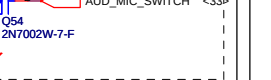
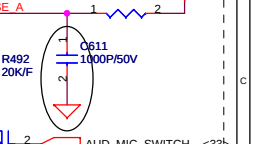
AUDIO_AVDD_ON

AUDIO_AVDD_ON

Layout Note: Close to U22 Pin 13.



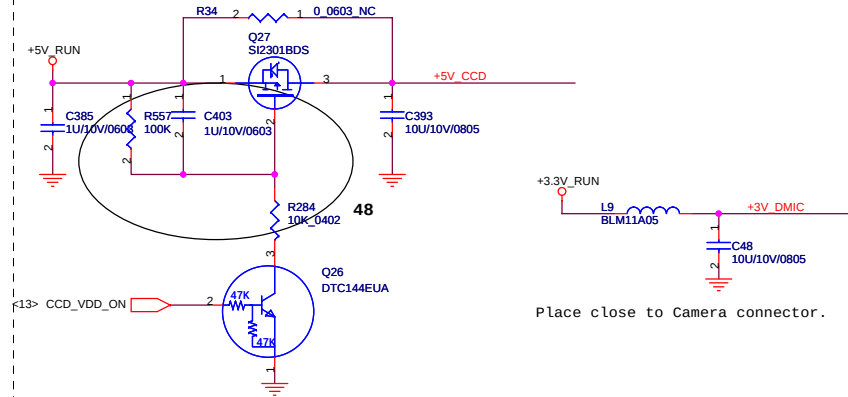
Layout Note: Close to U22 Pin 13.



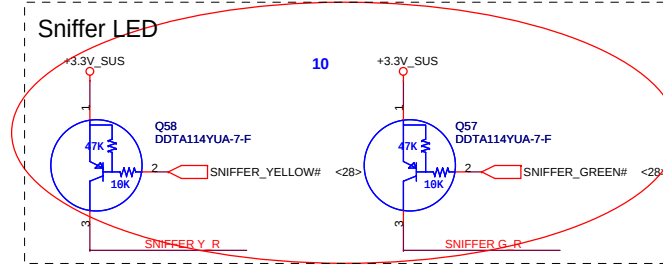
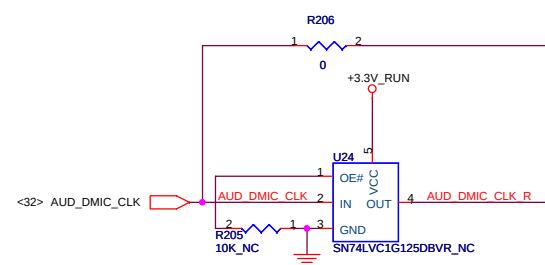
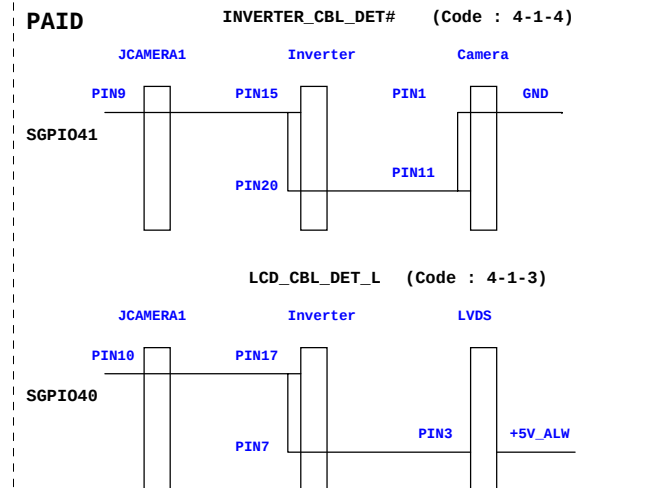
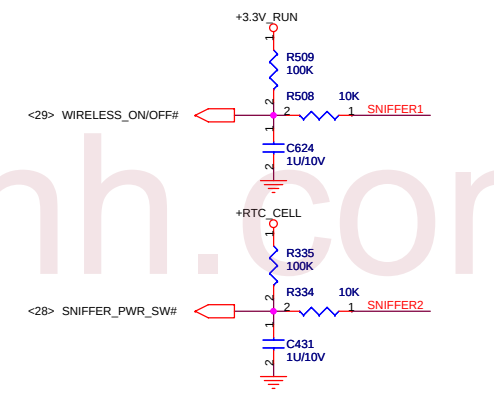
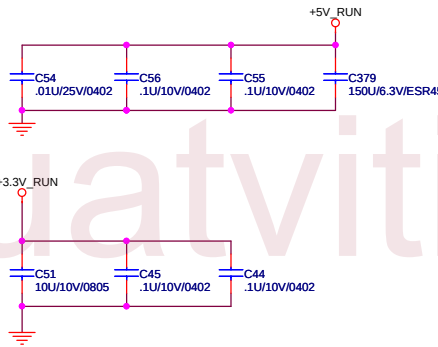
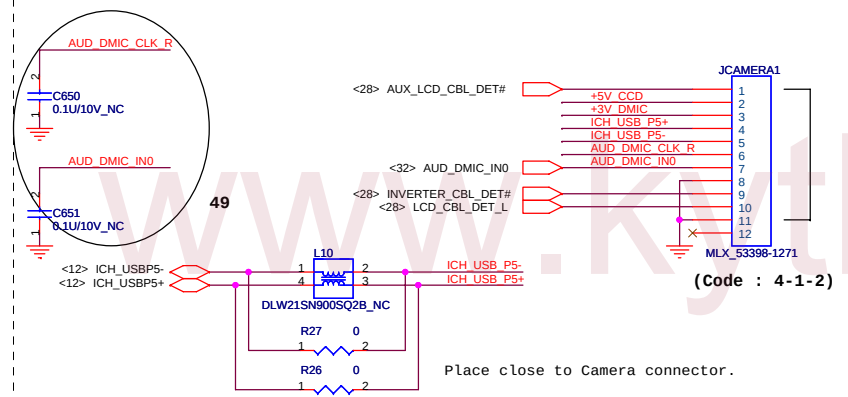
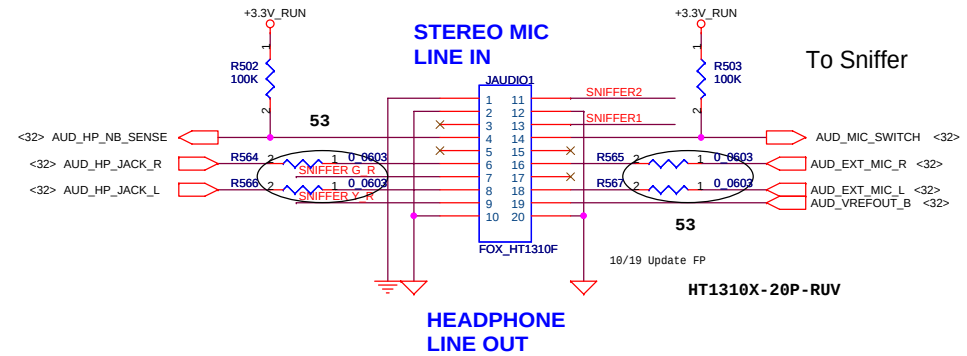
DELL CONFIDENTIAL/PROPRIETARY

Title	Azella CODEC(STAC9205)
Size	Document Number M-08
Date	Monday, March 05, 2007
Sheet	32 of 51
Rev	0.1

Digital Microphone & Camera

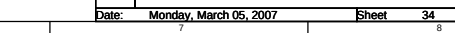
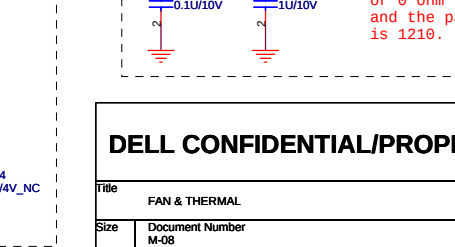
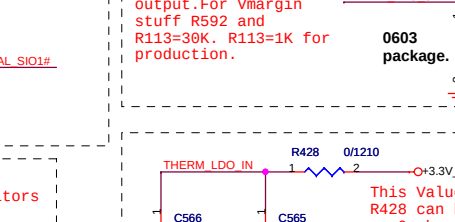
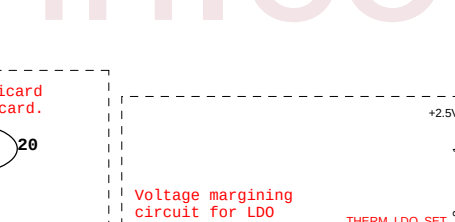
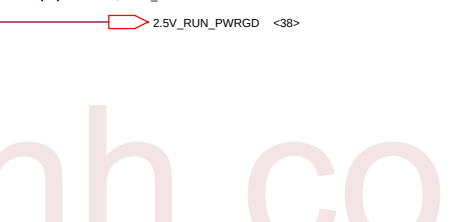
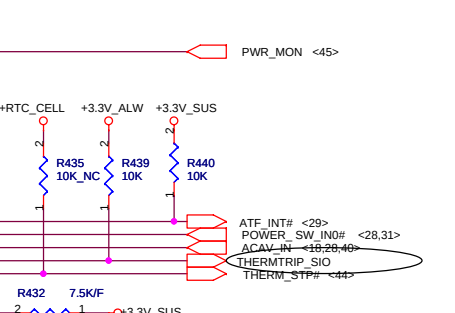
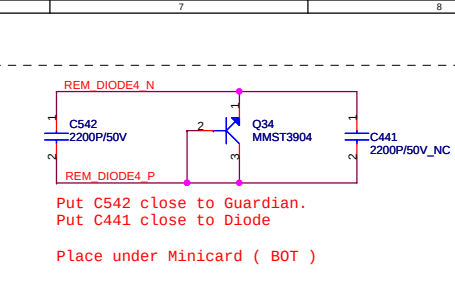


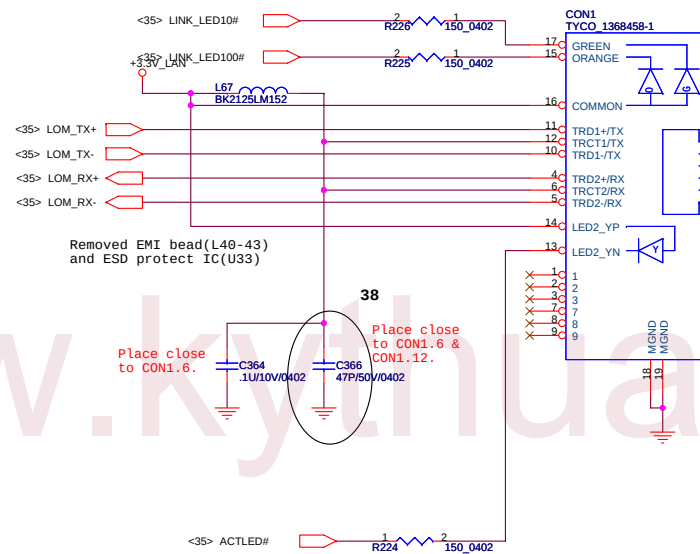
Update PN



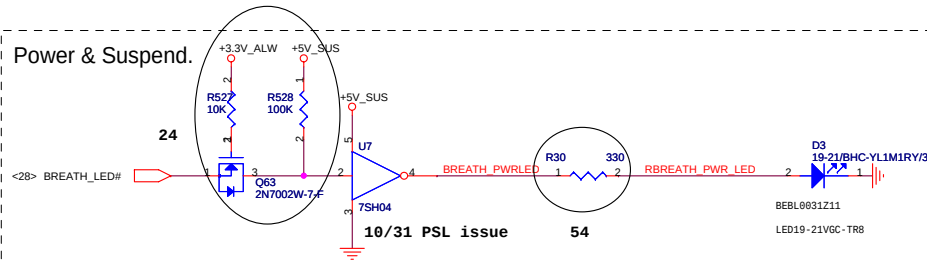
DELL CONFIDENTIAL/PROPRIETARY

Title			AUDIO CONN
Size	Document Number	Rev	
M-08		0.1	
Date:	Monday, March 05, 2007	Sheet	33 of 51

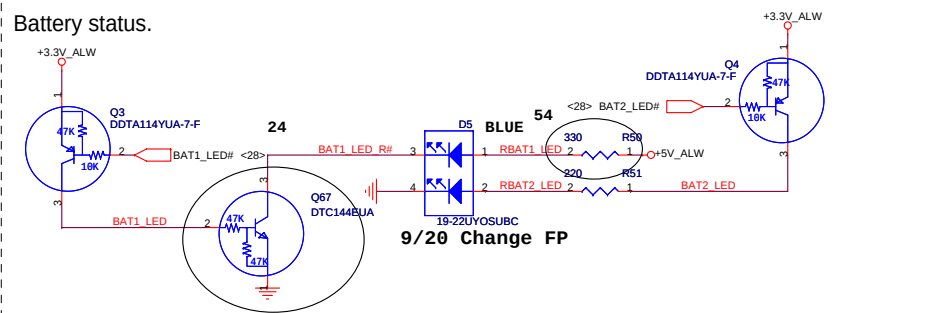




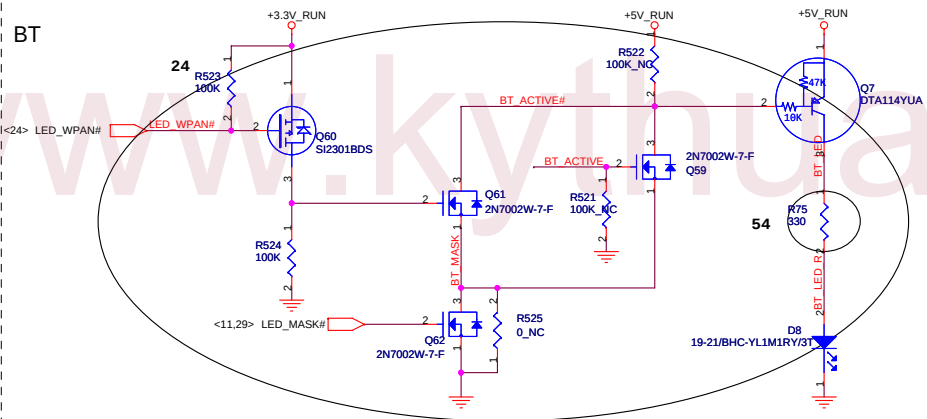
Power & Suspend.



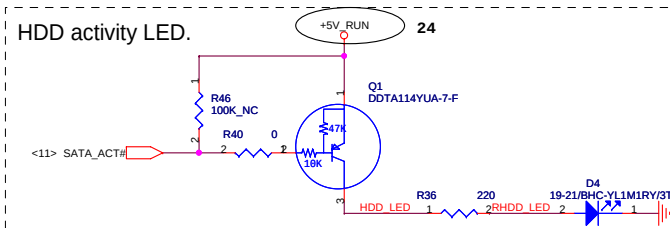
Battery status.



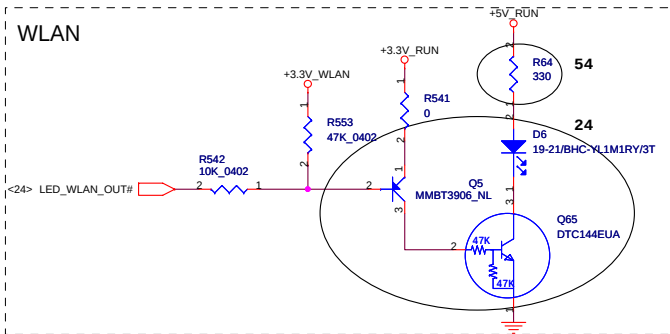
BT



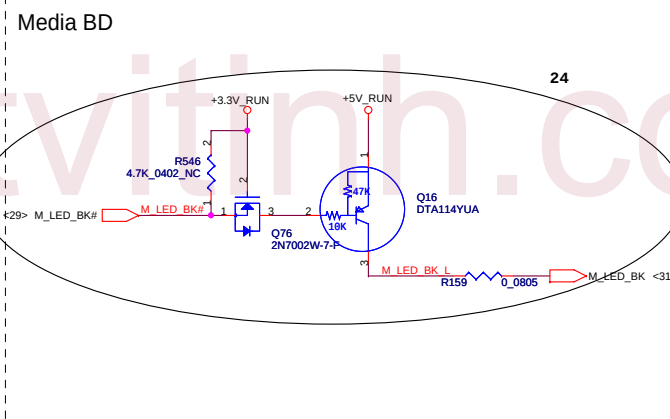
HDD activity LED.



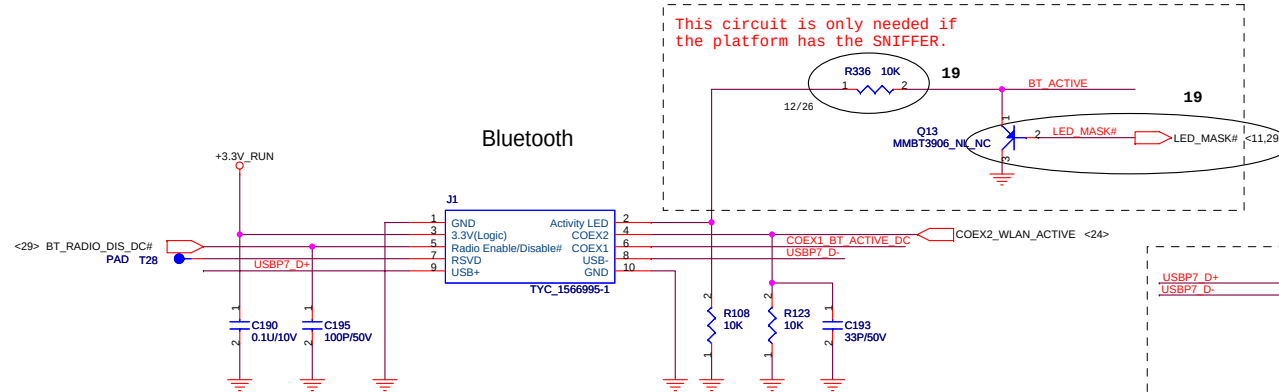
WLAN



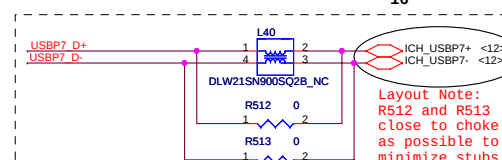
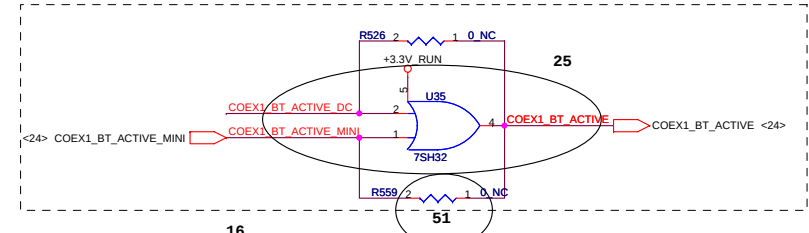
Media BD



Bluetooth



This circuit is only needed if the platform has the SNIFFER.



QUANTA COMPUTER

SWITCH & LED

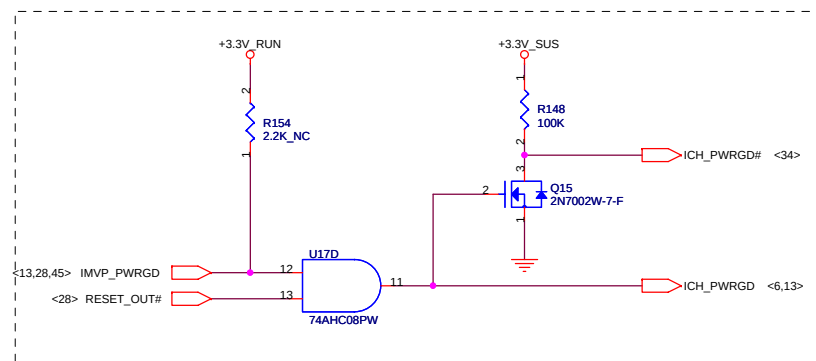
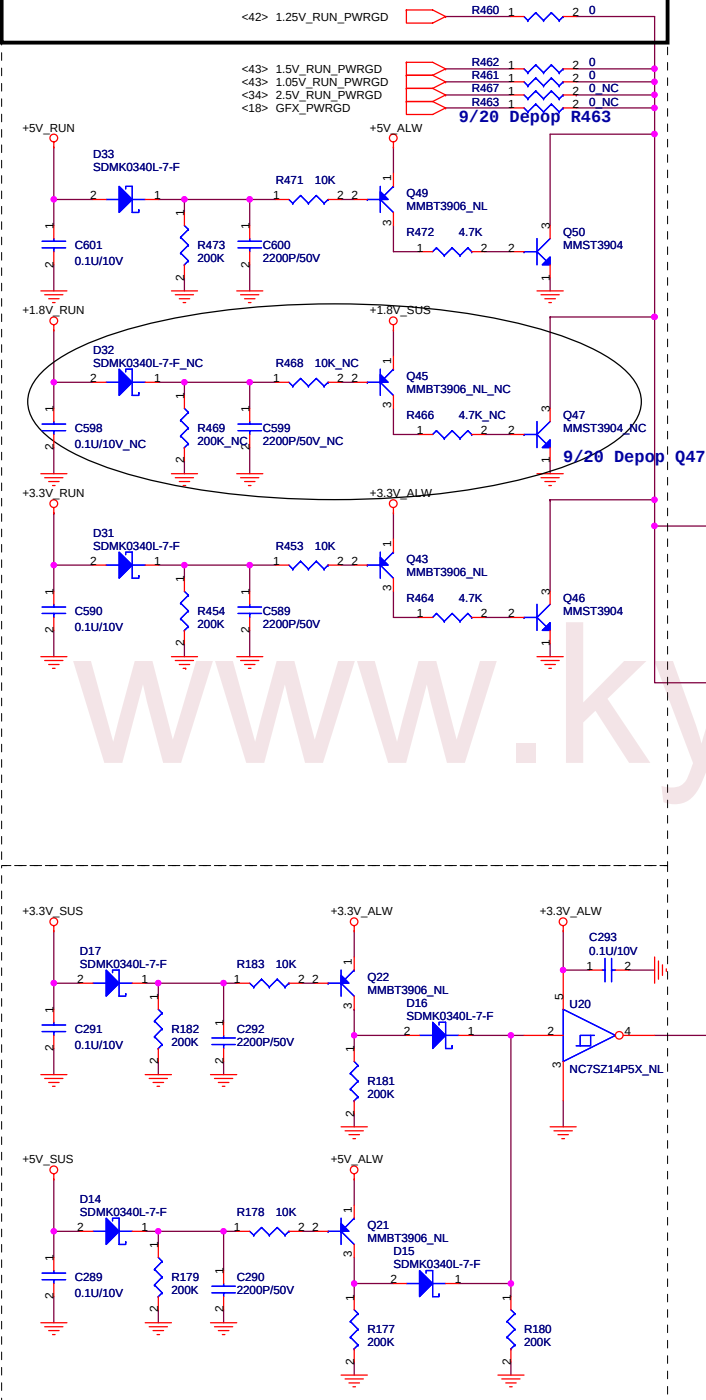
Size: Document Number FM1

Date: Monday, March 05, 2007

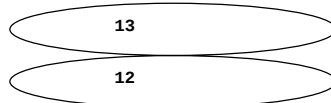
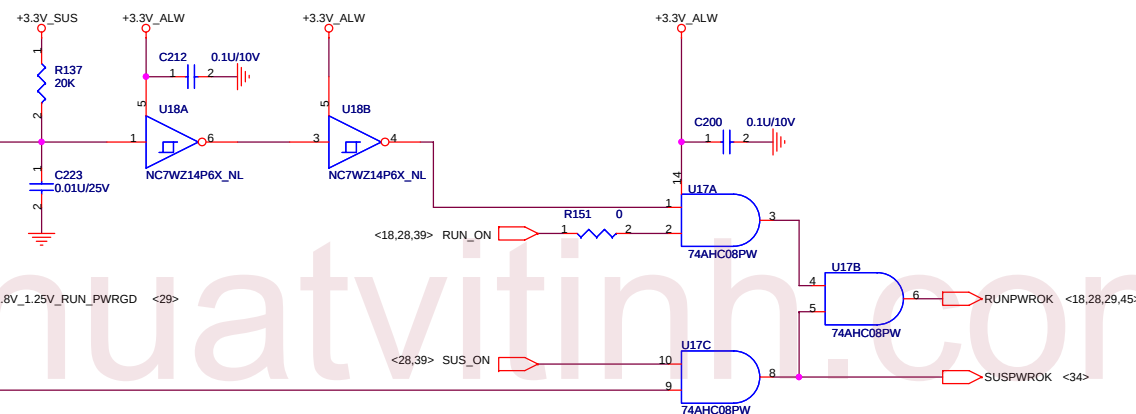
Sheet 37 of 51

Rev 0.1

Non-iAMT



Keep Away from high speed buses



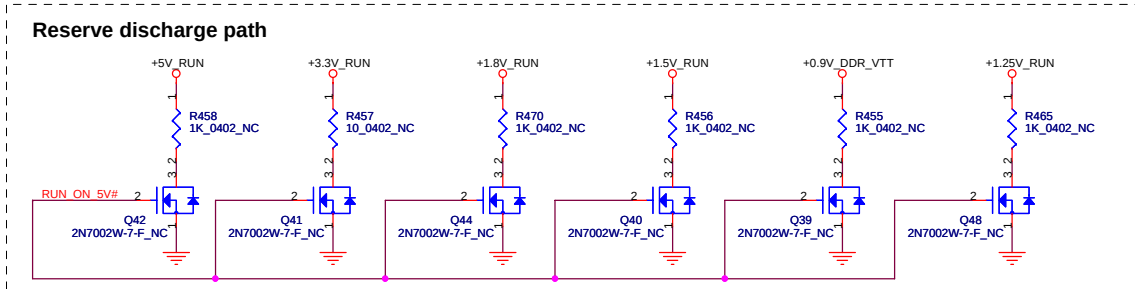
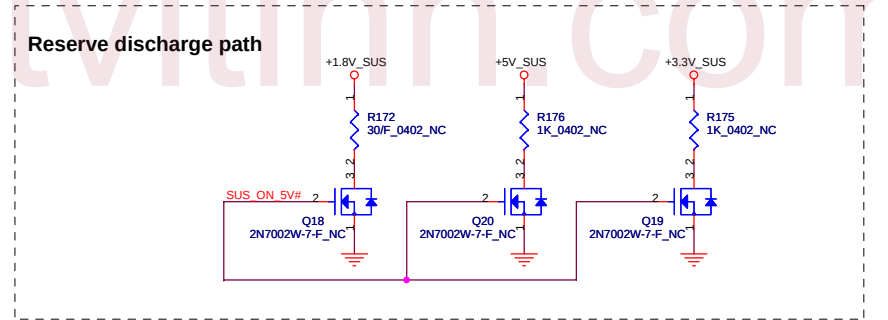
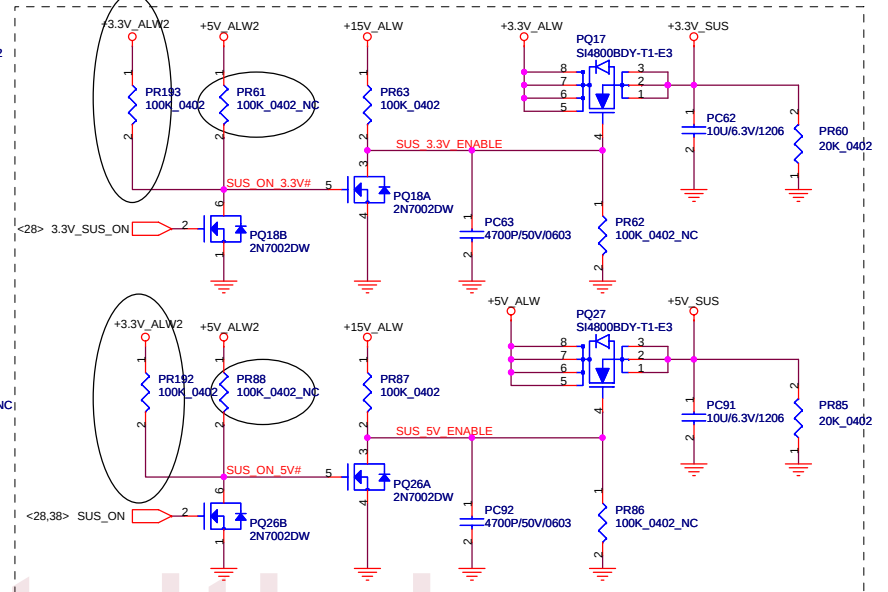
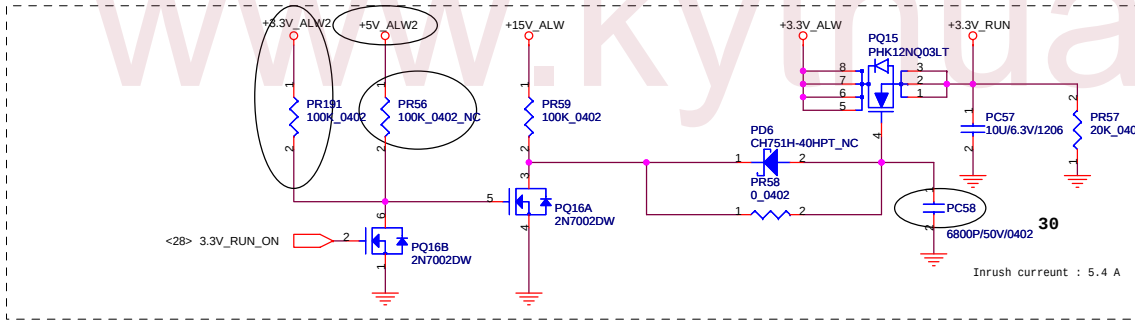
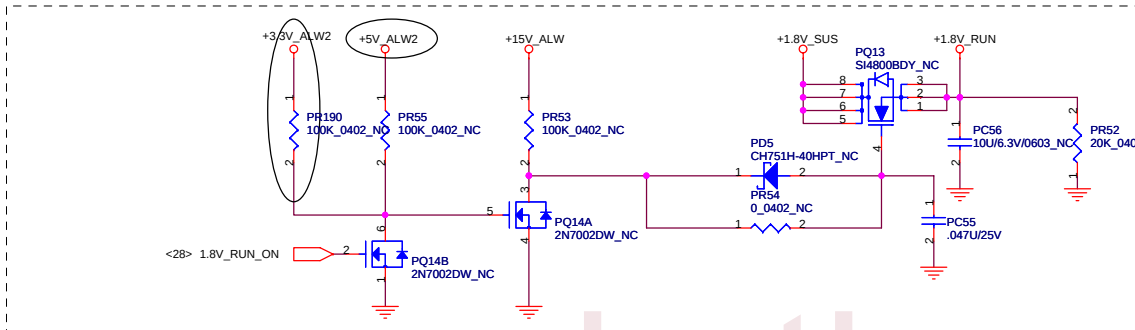
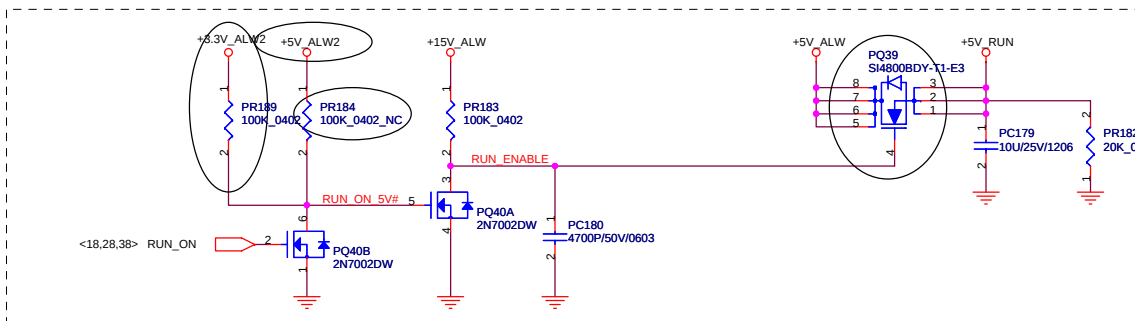
Title **System Reset Circuit**

Size	Document Number M-08
------	-------------------------

Date: Monday, March 05, 2007

Sheet 38 of 51

Rev	0.1
-----	-----



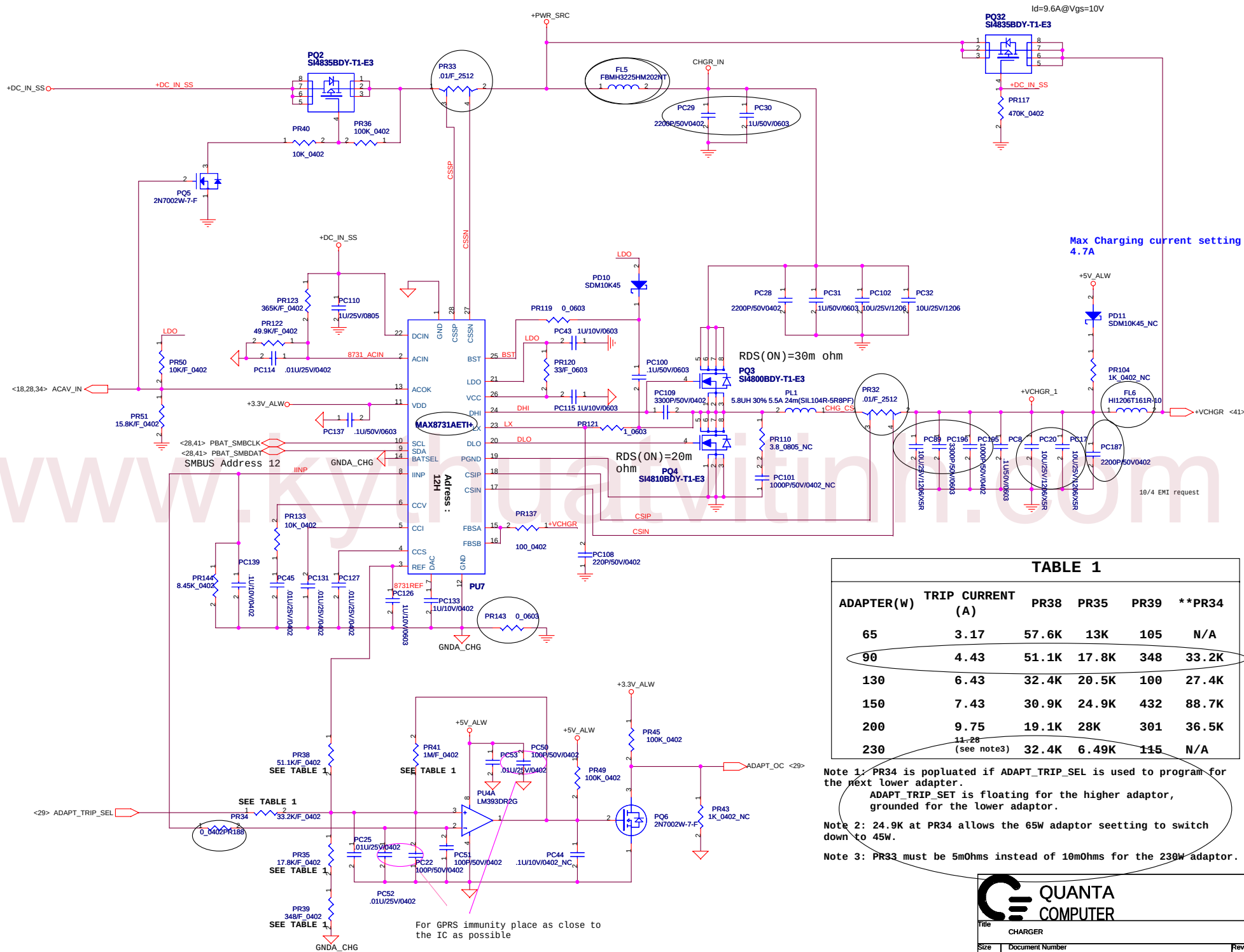


TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	PR38	PR35	PR39	**PR34
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28 (see note3)	32.4K	6.49K	115	N/A

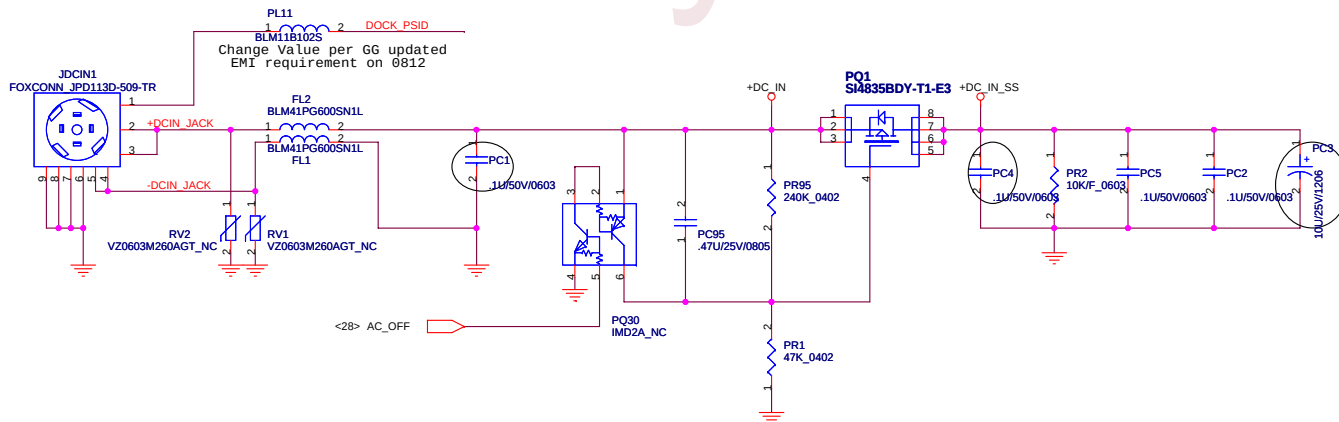
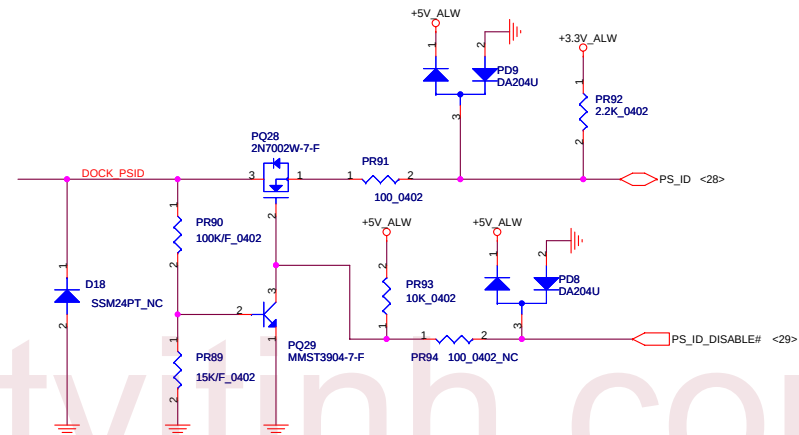
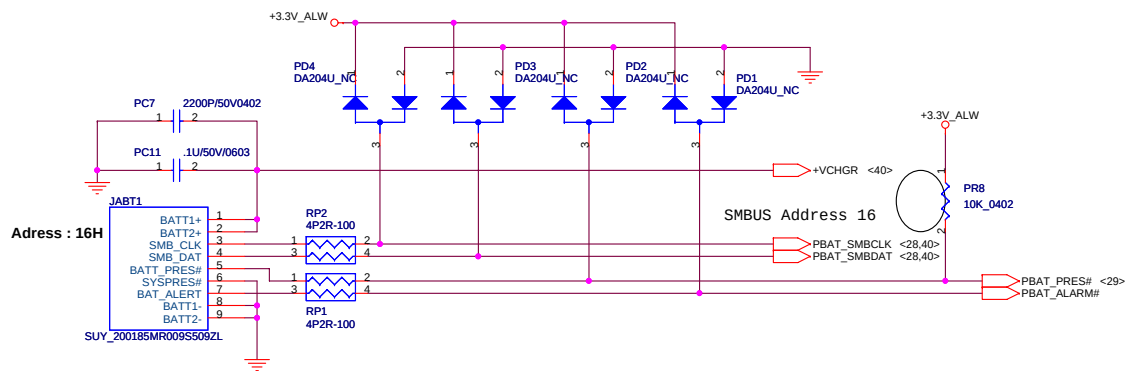
Note 1: PR34 is populated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

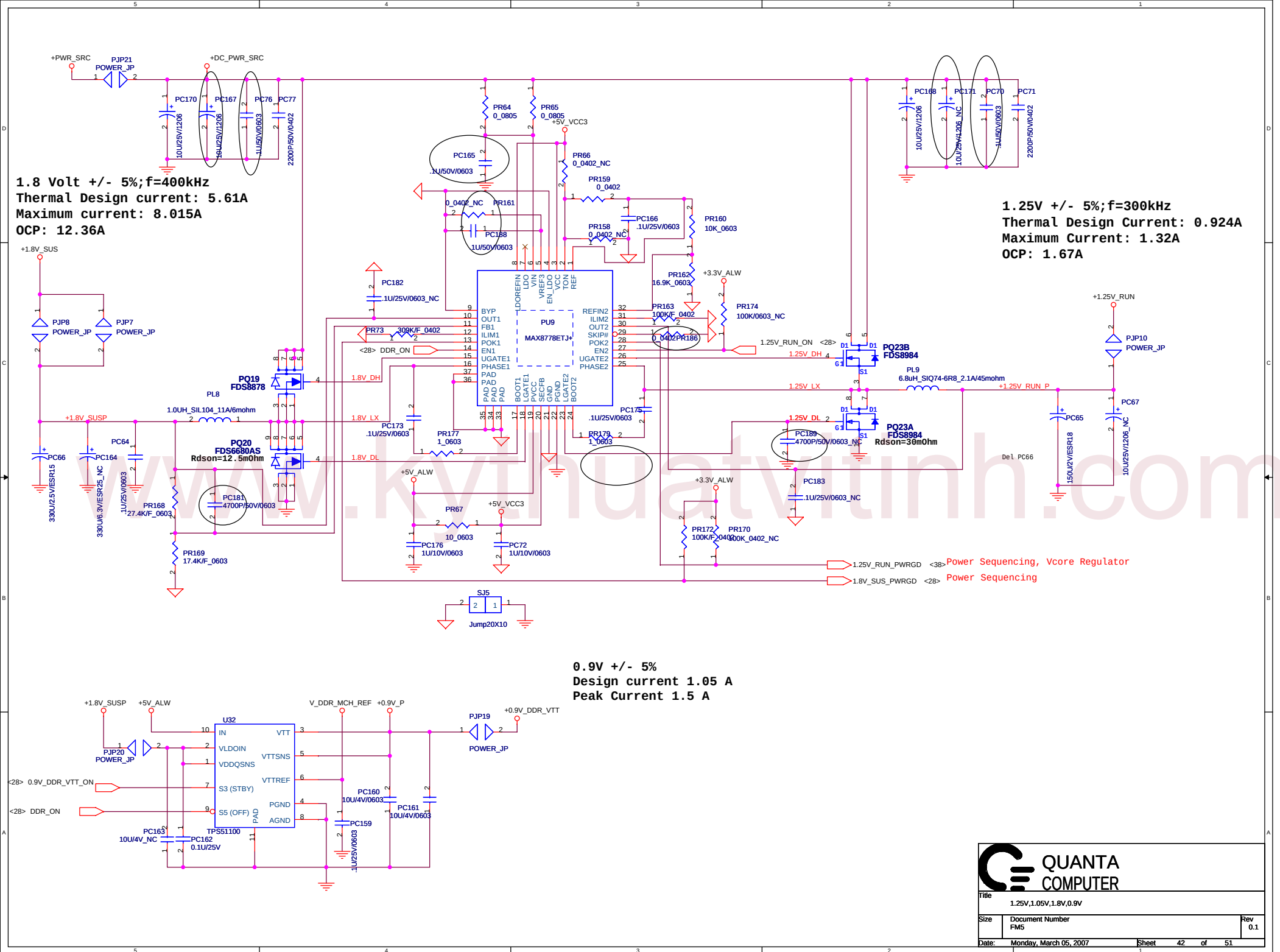
ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

Note 2: 24.9K at PR34 allows the 65W adaptor setting to switch down to 45W.

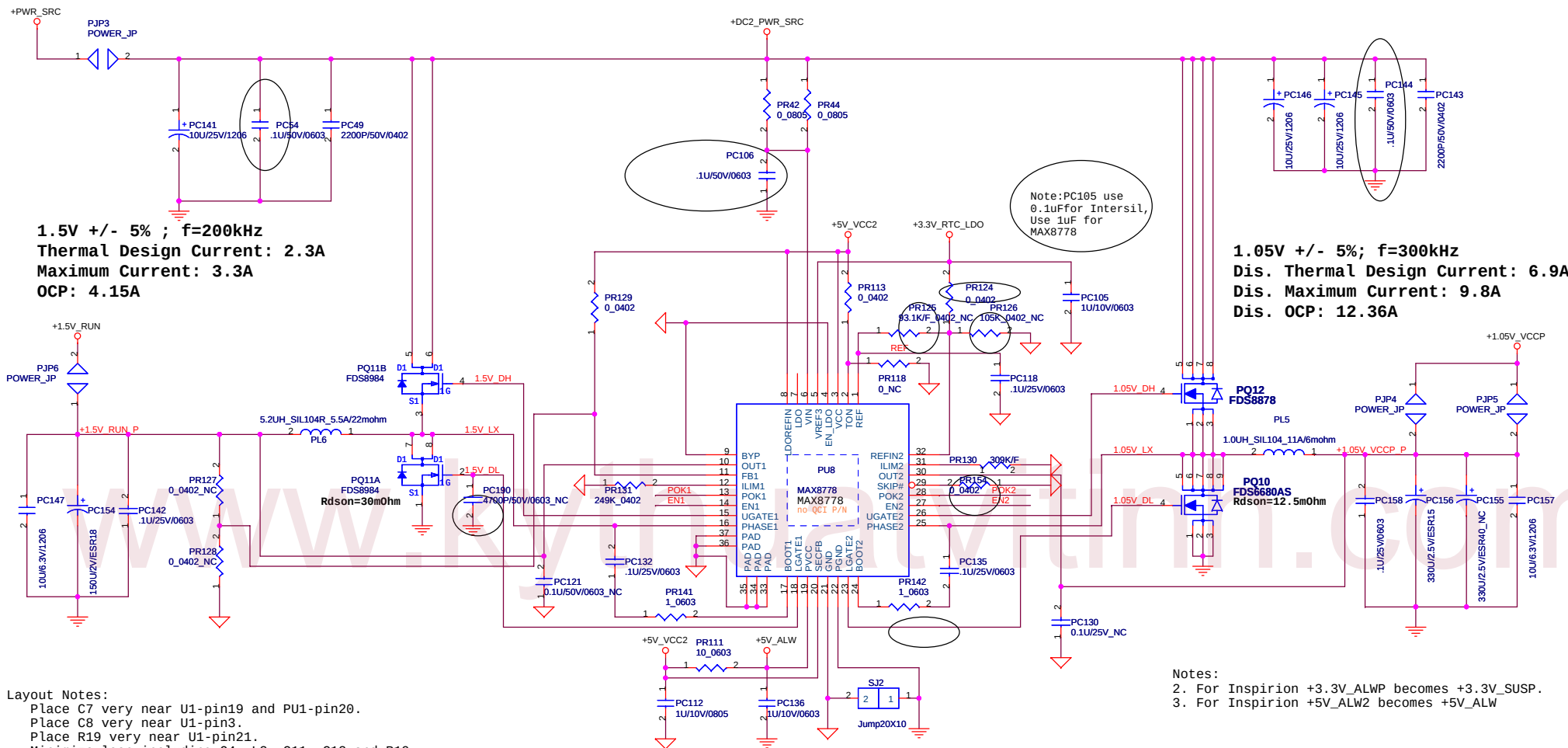
Note 3: PR33 must be 5mOhms instead of 10mOhms for the 230W adaptor.







+1.5V_RUN /+1.05V_VCCP /+3.3V_ALW /+3.3_RTC_LDO

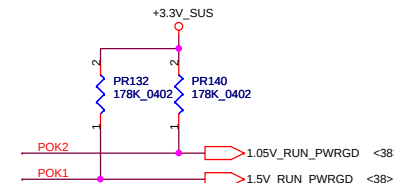


Layout Notes:

- Place C7 very near U1-pin19 and PU1-pin20.
- Place C8 very near U1-pin3.
- Place R19 very near U1-pin21.
- Minimize loop including Q4, L2, C11, C12 and R19.
- Minimize loop including Q2, L3, C17, C18, C19 and R19.
- Route GNDA_DC2 using at least 25 mil trace width.
- Minimize GNDA_DC2 trace length.
- Place C15 near U1-pin7.
- Place C20 near U1-pin5.
- Place R7 near U1-pin11.
- Place R12 near U1-pin31.
- Place R3, C10 near U1-pins 24 and 25.
- Place R2, C9 near U1-pins 16 and 17.
- Route +1.05V_BOOT, +1.05V_BOOST, +1.5V_BOOT, +1.5V_BOOST using 25mil trace width and minimize lengths.
- Connect large copper fill areas to PQ1, PQ2, PQ3 and Q4 signals for thermal improvement.
- Minimize length of +1.5V_RUN_PL and +1.05V_VCCP_PL.
- Place C1, C2, C3, C22 very near Q3-pins 5, 6, 7, 8.
- Place C4, C5, C6, C23 very near Q1-pins 5, 6, 7, 8.
- Route +DC2_PWR_SRC using 50 mil trace width and minimize length.
- Route OUT1 and OUT2 away from inductor and switch-node.
- Sense Vout directly at output bulk cap.

Notes:

- For Inspirin +3.3V_ALWP becomes +3.3V_SUSP.
- For Inspirin +5V_ALW2 becomes +5V_ALW



Title	1.5V,1.05V	Rev	1A
Size	Document Number FMS	Rev	1A
Date:	Monday, March 05, 2007	Sheet	43 of 51

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

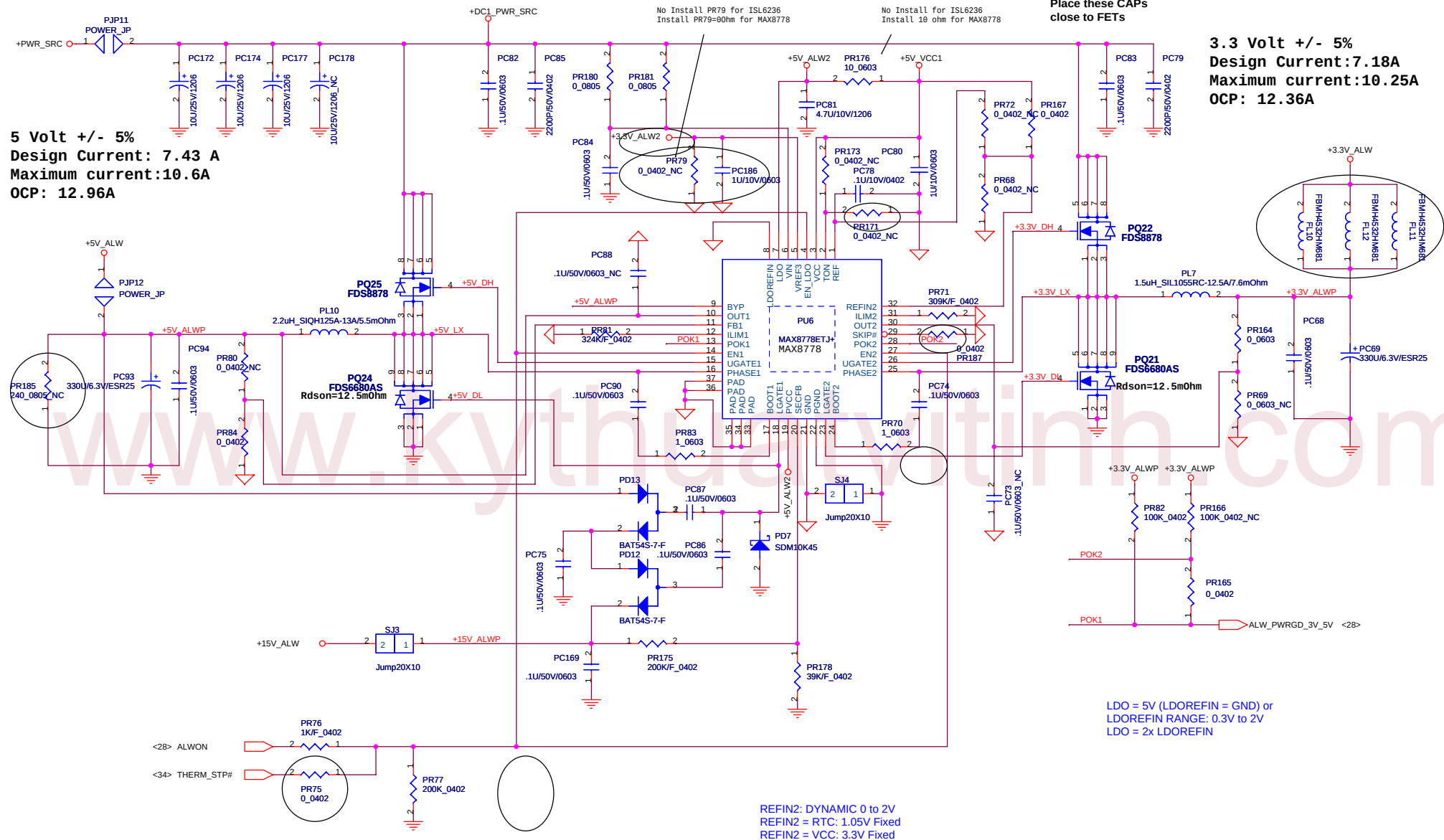
Ton:OUT1/OUT2 Switching Frequency
VDD 200kHz/300kHz
OPEN (REF): 400kHz/300kHz
GND: 400kHz/500kHz

**Place these CAPs
close to FETs**

**Place these CAPs
close to FETs**

3.3 Volt +/- 5%
Design Current:7.18A
Maximum current:10.25A
OCP: 12.36A

5 Volt +/- 5%
Design Current: 7.43 A
Maximum current:10.6A
OCP: 12.96A



LDO = 5V (LDOREFIN = GND) or
LDOREFIN RANGE: 0.3V to 2V
LDO = 2x LDOREFIN

REFIN2: DYNAMIC 0 to 2V
REFIN2 = RTC: 1.05V Fixed
REFIN2 = VCC: 3.3V Fixed



Title	3VALW,5V,3V, power on
-------	-----------------------

Size	Document Number FM5
------	------------------------

Rev	
1A	

Date: Monday, March 05, 2007

Sheet 44 of 51



POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+3.3V_ALW +3.3V_RTC_LDO +3.3V_WLAN +5V_ALW +15V_ALW	+1.8V_SUS +1.8V_LOM +3.3V_LAN +3.3V_SUS +5V_SUS	+0.9V_DDR_VTT +1.05V_VCCP +1.25V_RUN +1.5V_CARD +1.5V_RUN +3.3V_CARD +3.3V_CARDAUX +3.3V_R5C832 +3.3V_RUN	+3.3V_RUN_CARD +2.5V_RUN +5V_MOD +5V_RUN +5V_SPK_AMP +CPU_PWR_SRC +VCC_CORE +VDDA	+DC_IN +DC_IN_SS +PWR_SRC +RTC_CELL
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	OFF	ON
S5 S4/AC	ON	OFF	OFF	OFF	ON
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	ON

PCI TABLE

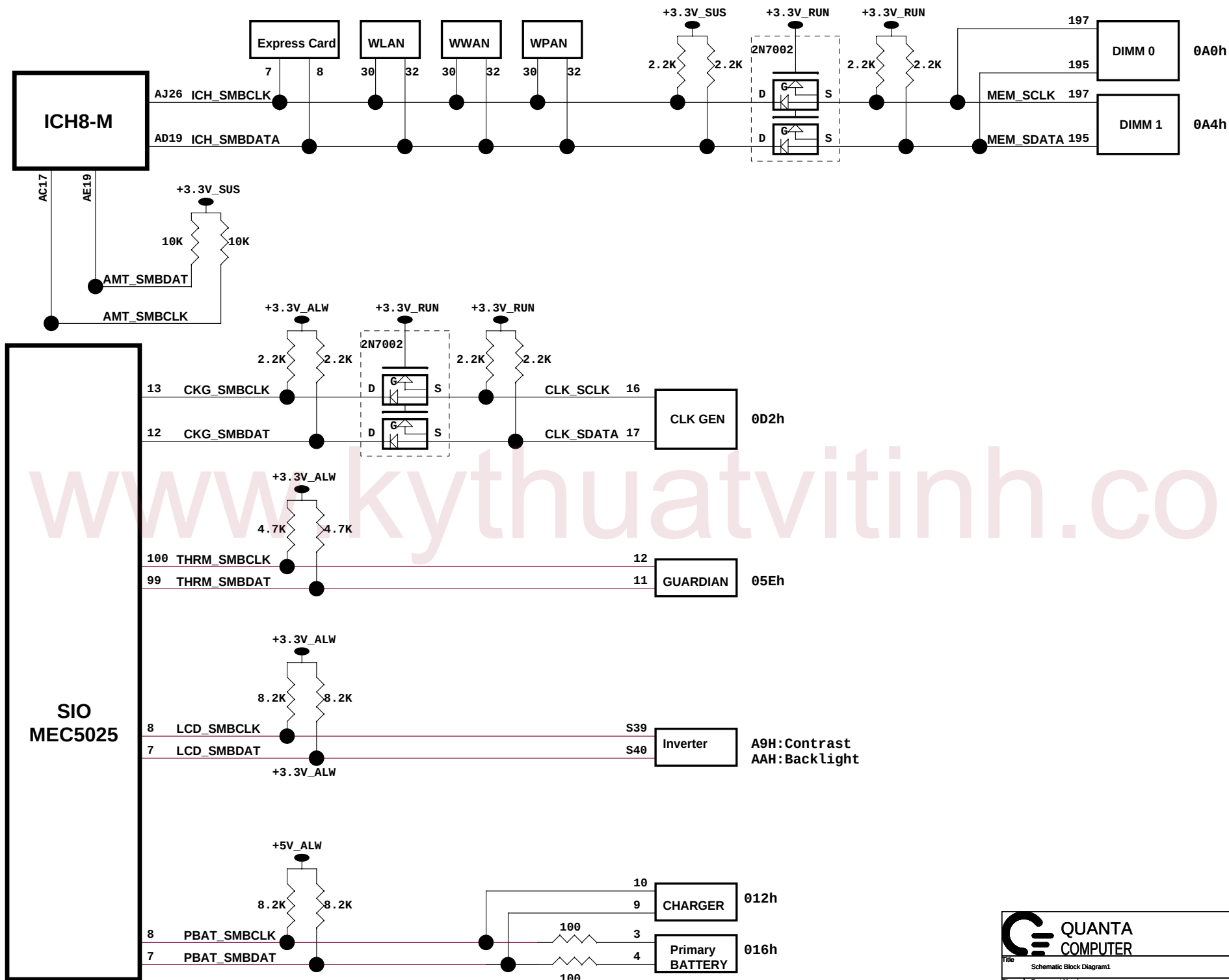
PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
BCM4401B	AD16	REQ#0 / GNT#0	PIRQB
R5C833	AD17	REQ#1 / GNT#1	PIRQC: Card reader PIEQD: 1394

ICH8-M

ECE 5011

USB PORT#	DESTINATION
0	Right Top
1	Right Bottom
2	Side TOP
3	Side Bottom
4	Ext. USB TOP
5	Digital Camera
6	Express Card
7	WPAN/Bluetooth
8	Ext. USB Bottom
9	WWAN
1	None
2	None
3	None
4	None

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 WPAN
Lane 4	Express Card
Lane 5	None
Lane 6	None



Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
C/G DISCRETE	1	39-45	7/13/2006					Update PWR schematics
	2	13,29	9/20/2006				S3 resume fail	Move PLTRST_DELAY# from EC to ICH8
	3	11	9/20/2006				2nd SATA HDD can't recognize	Move 2nd SATA from port 1 to port 2
	4	38	9/20/2006				Gfx card timing error	Disconnect GFX_PWRGD to system (Delete R463)
	5	38	9/20/2006				Gfx card timing error	Disconnect +1.8V_RUN detect circuit to system (Delete Q47)
	6	39-45	9/21/2006					Update PWR schematics
	7	23	9/21/2006					Add +1.8V_RUN for SATA buffer test (CON4.20-21-22-42-43-44)
	8	37	10/2/2006				Update WLAN LED implementation.With the current implementation, there is a possibility for backdrive from the WLAN LED control signal to +3.3V_RUN while in S3 / S4 / S5. With the voltage rail being +3.3V_WLAN, there is a high probability that the LED will be illuminated while in S3 / S4 / S5.	Please change the WLAN LED implementation to advice from Dell.
	9	13	10/2/2006				Intel has advised that the pull-up on LINKALERT# be depopulated and that the pull-up on GPIO14 be 8.2k. Please update.	Depop R247 & change R227 from 10K ohm to 8.2K ohm
	10	28,33	10/11/2006				In order to leverage the M07 implementation, the sniffer LED circuit needs to be modified. The MEC5025 pins are being changed from active high to active low.	Change back VC08 design, rename SNIFFER_YELLOW to SNIFFER_YELLOW#, SNIFFER_GREEN to SNIFFER_GREEN# and remove R507 and R510.
	11	28,29	10/11/2006				Move DOCK_SMB_PME from MEC5025 SGPIO37 to ECE5018/5011 GPIOC0.Move DOCK_SMB_ALERT# from ECE5018/5011 GPIOC0 to MEC5025 SGPIO37	DOCK_SMB_PME# should be pulled up to +3.3V_ALW DOCK_SMB_ALERT# should be pulled up to +5V_ALW
	12	28,38	10/11/2006				Add ATI_Intel to MEC5025 pin 14 and tie to GND.This connection should be labeled ATI_Intel.	Remove 3.3V_LAN_PWRGD circuit from page 38 Delete 3.3V_LAN_PWRGD from MEC5025 pin 14 Add a connection from the MEC5025 pin 14 and tie to GND.
	13	28	10/11/2006					Move ALW_PWRGD_3V_5V from MEC5025 pin 18 to pin 29
	14	13	10/11/2006					1) Move SIO_EXT_SCI# from ICH pin AG22 to ICH pin AC19 2) Delete R242 (delete DOCKED# signal)
	15	13	10/11/2006					Reserve LOM_SMBALERT# (ICH8 AG22) & PU resister
	16	24	10/16/2006					Change WPAN USB port from USBP7 to USBP4
	17	23,29	10/18/2006				Modify HDDC_EN and MODC_EN Circuits to Resolve Glitch Issue. unintentionally for a brief moment.With the current Dawson design, it has been shown that the +15V_ALW rail comes up before the +3V_ALW rail on the original HDDC_EN and MODC_EN circuits. This can cause a momentary glitch at the gate of the power FET, which may cause the FET to turn on unintentionally for a brief moment.	To resolve this issue, please use the HDDC_EN and MODC_EN circuits that are attached below. These new circuits resemble closely our other load switch circuits, but require an additional FET and changes the sense of the HDDC_EN and MODC_EN signals to active high. Please note the use of +5V_ALW2 on these circuits. The +5V_ALW2 voltage comes directly from the LDO output on the 3V/5V switcher in your M08 design.
	18	12,14	10/18/2006				WWAN Noise - ICH improvements. Add one .1 uF cap on each USB OC (over current) trace near the ICH. Add four .1uF caps in parellel to C813 close to the ICH pins. Add four .1uF caps in parellel to C825 close to the ICH pins.	Add C871~C878 for USB OC. Add C867~C870 in parellel to C825. Add C748,C864~C866 in parellel to C813.
	19	37	10/23/2006				Use LED_MASK# to control BT LED to prevent leakage	Add R336 & change Q13 to BJT
	20	34	10/23/2006				Change pull-up rail on 5V_CAL_SIO1# to +3.3V_SUS. Feedback from SMSC has indicated that the pull-up rail on 5V_CAL_SIO1# needs to change from +5V_SUS to +3.3V_SUS.This is necessary because the GPIO on the EMC4001 is 3V tolerant, not 5V.	Pullup is at reference designator R298.
	21	28	10/23/2006				Due to the power on defaults of the MEC5025, the pull-downs on the KSI lines of the MEC5025 need to be stronger, to avoid pulses from powering on certain power rails. Please do the following: 1. Change pull-down on SUS_ON to 2.7k 2. Change pull-down on RUN_ON to 2.7k	Change R355,R358 to 2.7K
	22	24	10/23/2006				Add SMBus isolation circuitry for WLAN.Add isolation circuitry for SMBus on WLAN.	
								 QUANTA COMPUTER
								Title: Change List
								Size: Document Number JM78 Rev 1A
								Date: Monday, March 05, 2007 Sheet 49 of 1

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
C/G DISCRETE	23	17	10/26/2006				Chipset side spec. Differetial CLK raise/fall slew rate is 2.5~8 V/ns, only express card and mini card is 0.6~4V/ns. BITCLK rise/fall slew rate in 1-3 V/ns &	Change serial resistors (PR4,PR5,PR10,PR12,PR13) to meet the CLK SPEC
	24	37	10/26/2006				Change LED control method	
	25	37	10/26/2006				Add OR gate for BT_ACTIVE	
	26	13	10/26/2006				M08 GPIO A14 update. Original EC5011 pin66 CCD_VDD_ON move to IC8 pinAD10 GPIO48 and add 100K ohm pull down.	Move CCD_VDD_ON from EC5011 pin66to IC8 pin AD10 GPIO48 and add 100K ohm pull down.
	27	25	10/26/2006				For Comm team suggestion (GG list), pop C217 for WWAN	
	28	39 - 45	10/31/2006				PWR team updat schemtics - 10/23	

QUANTA
COMPUTER

Title

Change List

Size

Document Number

Rev

1M7B

1A

Date:

Monday, March 05, 2007

Sheet

50

of

1

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	
C/G DISCRETE	29	24 - 25	11/1/2006				For EMI request, add RC circuit for Mini card clk request	Add R543, C880, R186, C649, R544, C181
	30	39	11/1/2006				For +3.3V_RUN inrush current, it may over OCP (12.36 A)	Change PC58 from 470 pF to 6800 pF
	31	32	11/3/2006				For AP - THN+D fail, change C306, 307 to 0.033uF/16V/X7R/1206 & C326, C329 to 1uF/16V/X7R/1206	Change C306, 307 to 0.033uF/16V/X7R/1206 & C326, C329 to 1uF/16V/X7R/1207
	32	32	11/3/2006				'PO' noise in resume from S3,S4,S5	Reserved the AUD_AMP_MUTE# for 'PO' noise
	33	39 - 45	11/09/2006				PWR team updat schemtics - 11/08	
	34	17	11/09/2006				Change R44 to 2.2K per Intel recommend value.	
	35	12 - 13	11/21/2006				Due to Intel-ICH8 uses GPIO20 pin AE11 as an Internal Strapping at power up	Move PCIE_MCARD2_DET# from GPIO20 to ICH8 GPIO5/PIRQH# pin B3.
	36	13	11/21/2006				GPIO18 is default as an output at power up, it will drive 1Hz output at power up. Per Intel this GPIO could not be connected to GND	Add 4.7K series - R547 resistor to separate it
	37	32	11/22/2006				There is potential back drive from the codec DVdd back to the AVdd supply due to an internal ESD diode	add 100kohm resistor (R253) between pin 40 and +3.3V_RUN and a 1000pF cap (C643 below) from Pin 40 to ground
	38	35 - 36	11/28/2006				GG list -- COMM team request	1.Change capacitor for U5 pin 79, 94,106 (VDDIO) (C18, C16, C25) to 47pF. 2.Change those three capacitors (C27, C37,C34) to 47pF 3.Add C644 - 47pF capacitor by the pin 57 of U5 4.Change L7 to 0805 package -BK2125LM152. & C23 to 47 pF 5.Add Ferrite Bead BK1608LM152 on 1.8V to EPHY_AVDD pin 57
	39	28-29	11/28/2006				Move DOCK_SMB_PME from MEC5025 SGPIO37 to ECE5018/5011 GPIOC0.Move DOCK_SMB_ALERT# from ECE5018/5011 GPIOC0 to MEC5025 SGPIO37	DOCK_SMB_PME# should be pulled up to +5V_ALW DOCK_SMB_ALERT# should be pulled up to +3.3V_ALW
	40	24	12/01/2006				GG list -- Seperate debug port with MINI-PCI if not necessary	Add 4 0ohm resistors for these pins
	41	24 - 25	12/01/2006				GG list -- Delete decoupling cap	Delete C222 & C424
	42	39 - 45	12/04/2006				PWR team updat schemtics - 12/04	
	43	32	12/08/2006				GG List -- Change audio AMP to TI solution	1.Change codec to TPA9040A4 2.Pop R505, C619 & C614; depop R506, R504 & R497
	44	31	12/13/2006				GG List -- Change power source for LED of dash board	Change JTP1.9 from +3.3V_RUN to +5V_ALW
	45	39 - 45	12/19/2006				PWR team updat schemtics - 12/19	
	46	28	12/25/2006				GG List -- Remove EC5025 pin15 GPIO4 AUD_AMP_MUTE# circuit.	NC R538
47	34	12/25/2006				GG List -- Add THERMATRIP_VGA# function	Pop R441,442,443 and Q35, C568 for THERMATRIP_VGA# trip.	
48	33	12/28/2006				Modify CCD power control soft start function	Change C403 , R284 connect method	



QUANTA
COMPUTER

Title

EMI & Screw hole

Size

Document Number

C & G UMA

Date

Monday, March 05, 2007

Sheet

50 of 51

Rev

2A

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	
C/G DISCRETE	49	22	1/11/2006				XD card detect function error	
	50	29	1/11/2006				Base on A16 GPIO : Change net name from BID2 to CHIPSET_ID1	
	51	37	1/24/2007				Add 0ohm_NC(R571) resistor pad connected from Coex1_BT_Active_MINI to Coex1_BT_Active	
	52	32	1/24/2007				Audio solution for pass EMI 225MHz and 451MHz radiation emission test.	Added R560, R561, R562 and R563 on AUD_SPK_L1, AUD_SPK_L2, AUD_SPK_R1, AUD_SPK_R2 trace
	52	33	1/24/2007				Audio solution for pass EMI 225MHz and 451MHz radiation emission test.	Added R564, R565, R566 and R567 on AUD_LINE_OUT,AUD_HP_OUT
	53	13	1/24/2007				GG List -- CCD_ON pull down R258 100K NC.	
	54	37	2/5/2007				Blue LED brightness is too high	Change R30,R50,R75,R64 & R36 from 220 ohm to 330 ohm
	55	30	2/12/2007				Prevent SPI CLK overshoot/undershoot issue	Add C896 for RC circuit but not pop it
	56	39 - 45	2/12/2007				PWR team updat schemtics - 2/12	
	57	29	2/12/2007				GG List -- CIR function intermediate issue	ECE5021 pin7 PWRGD need to pull-down to GND with 0 ohm - Add R568 PD resistor & R569 series resistor (NC)
	58	44	3/1/2007				PWR team updat schemtics - 3/1	
	59	17	3/2/2007				Per TDC COMM team request - Change L65 to	Fine tune 14M CLK - Change R57 from 33 to 15 ohm & L65 to BLM18SG260
	60	04	3/2/2007				Per reliability issue - Move C98 to C249	De-pop C98 & pop C249