GM3(B) Pacino Intel Discrete & UMA Block Diagram

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blank Page PG 47

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/+0.9V_DDR_VTT PG 49

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+15V_ALW PG 52

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667 MHZ DDR II

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Jacks x3
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QUANTA COMPUTER

Title	Schematic Block Diagram1	
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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,48,49,50,51,52,55	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,26,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,50,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,20,30,37,38,43,48,49,50,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,50,53,55	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,20,25,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	6,8,9,11,12,13,14,15,17,19,20,22,25,26,27,28,30,33,34,36,38,39,40,41,42,53,55	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	19,20,21,22,23,24,25,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,,53,55	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.25V_RUN	+1.25V	6,9,14,49,53	CALISTOGA/ICH8 POWER	1.25V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,37,48,55	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.5V	4,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	
+5V_ALW2	+5V	37,38.52,53	LED power source	LDO output	

GND PLANE	PAGE	DESCRIPTION
8731AGND	46	
AGND_0.9V	49	
AGND_DC/DC	52	
AGND_DC2	48	
AGND_DDR	49	
AGND_ISL6260	51	
GND	ALL	

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Title	Index & Power Status	
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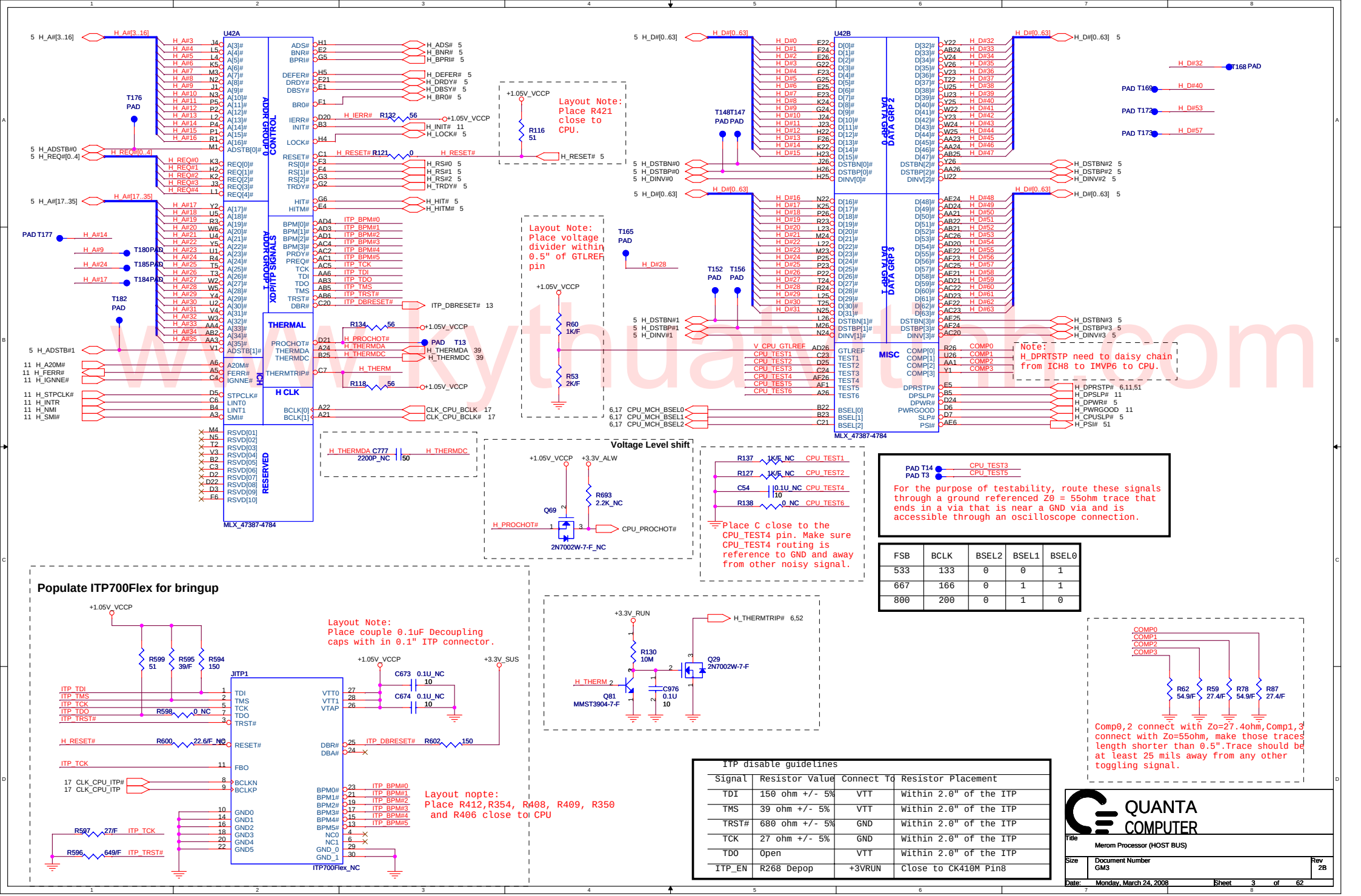

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 5%	GND	Within 2.0" of the ITP
TDO	Open	VTT	Within 2.0" of the ITP
ITP_EN	R268 Depop	+3VRUN	Close to CK410M Pin8

QUANTA COMPUTER

Title	Merom Processor (HOST BUS)	
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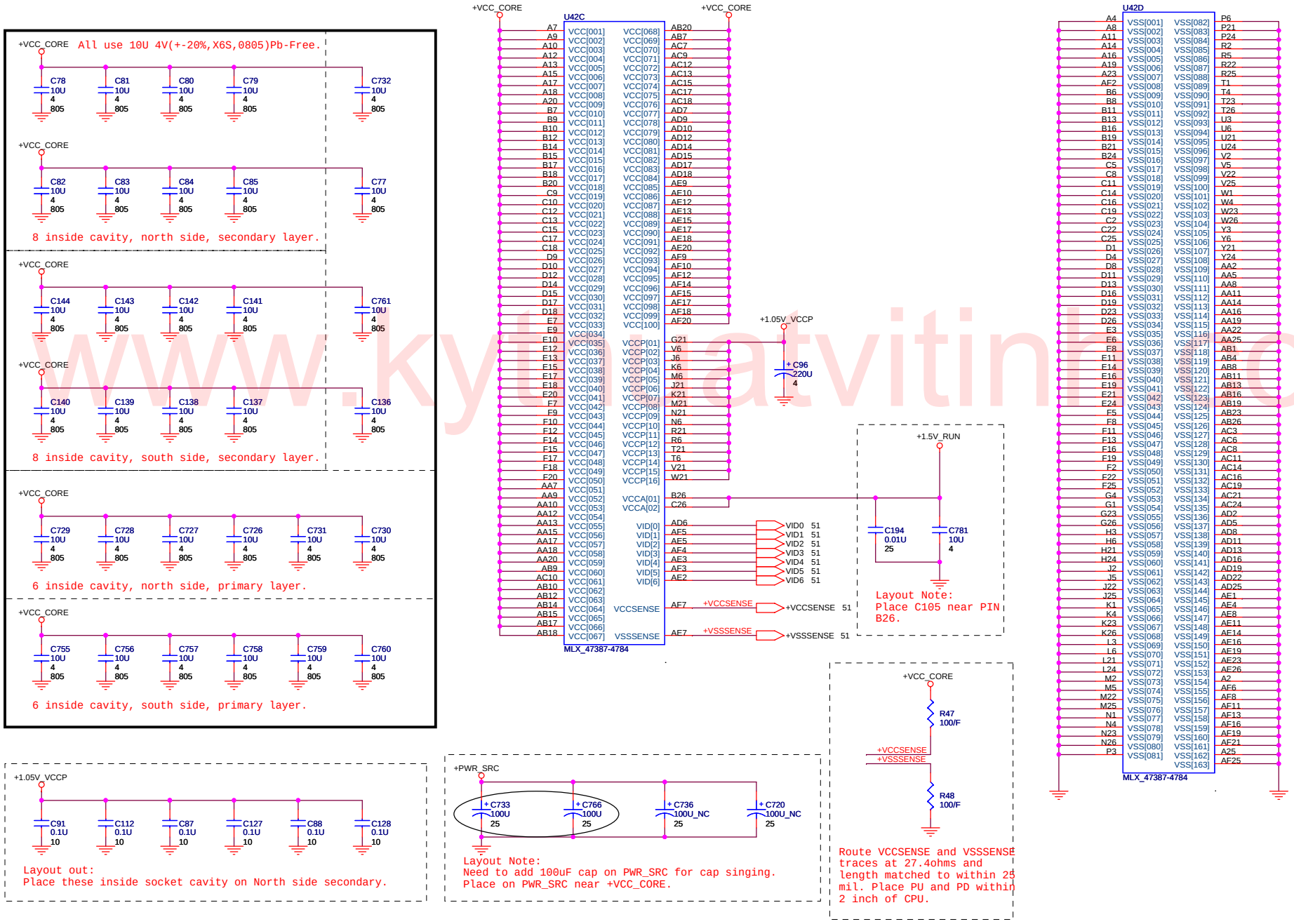

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Title	Merom Processor (POWER)	
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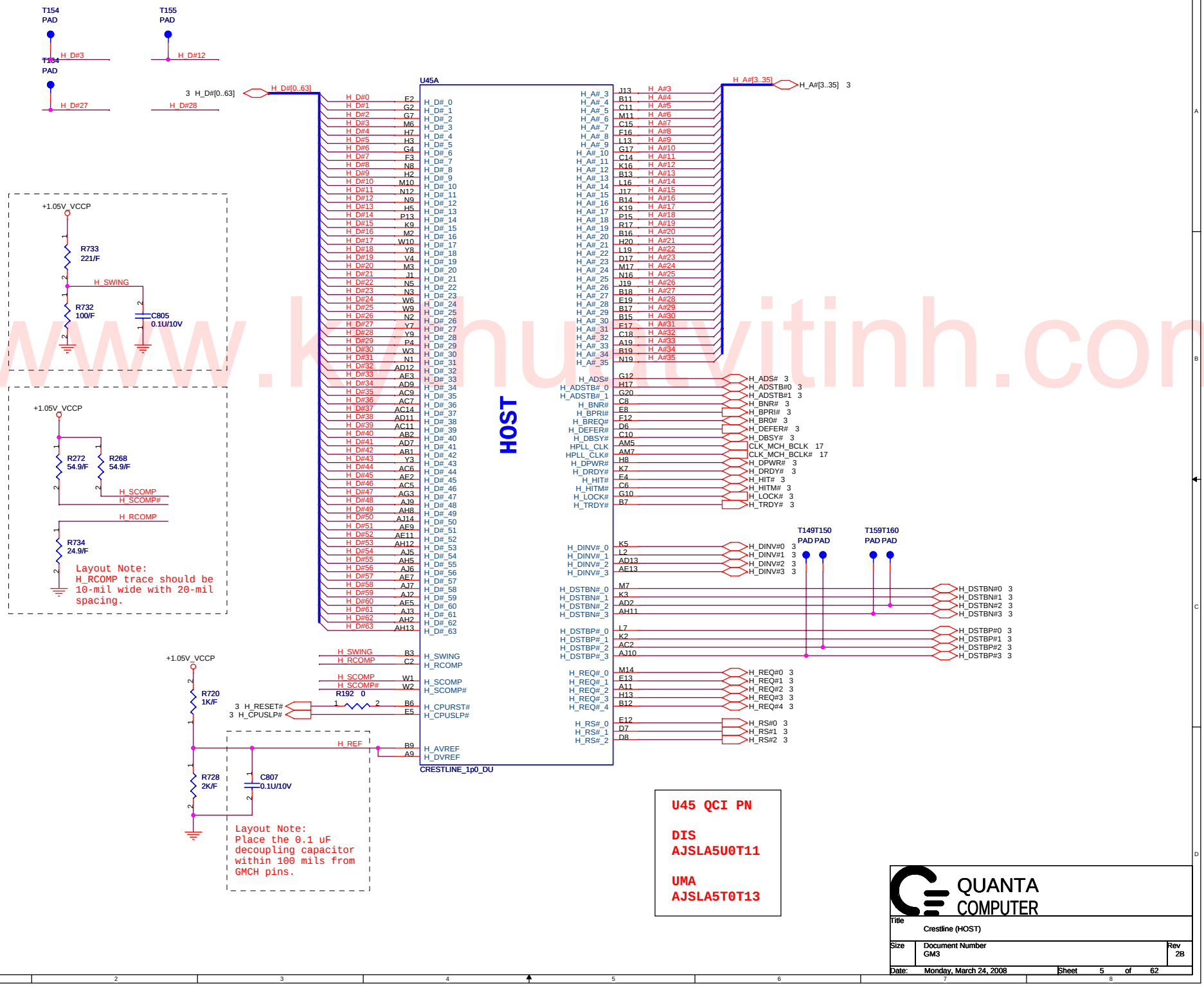

QUANTA COMPUTER		
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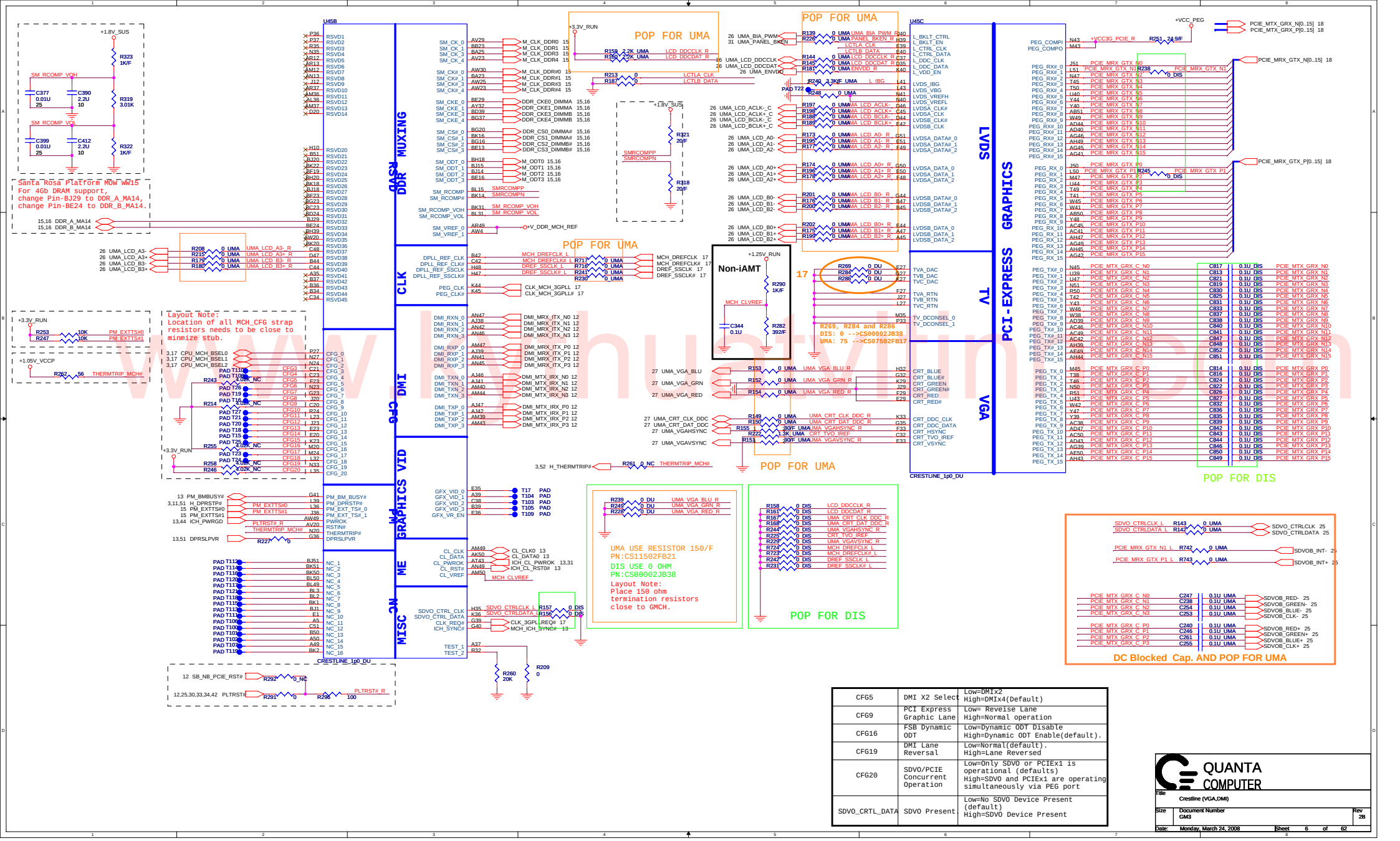

CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reveise Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present

QUANTA COMPUTER

Title	Crestline (VGA,DMI)		
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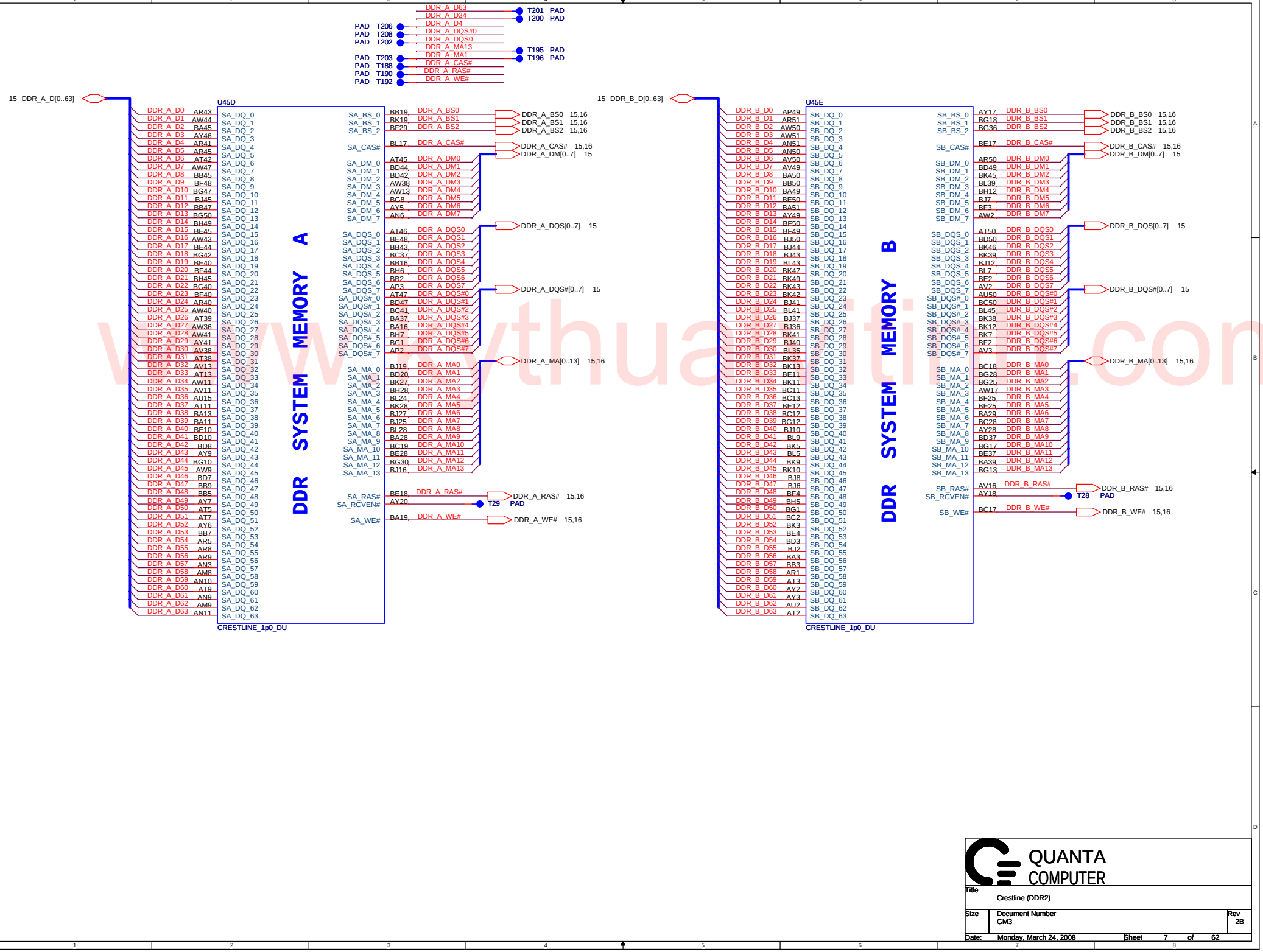

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Title	Crestline (DDR2)	
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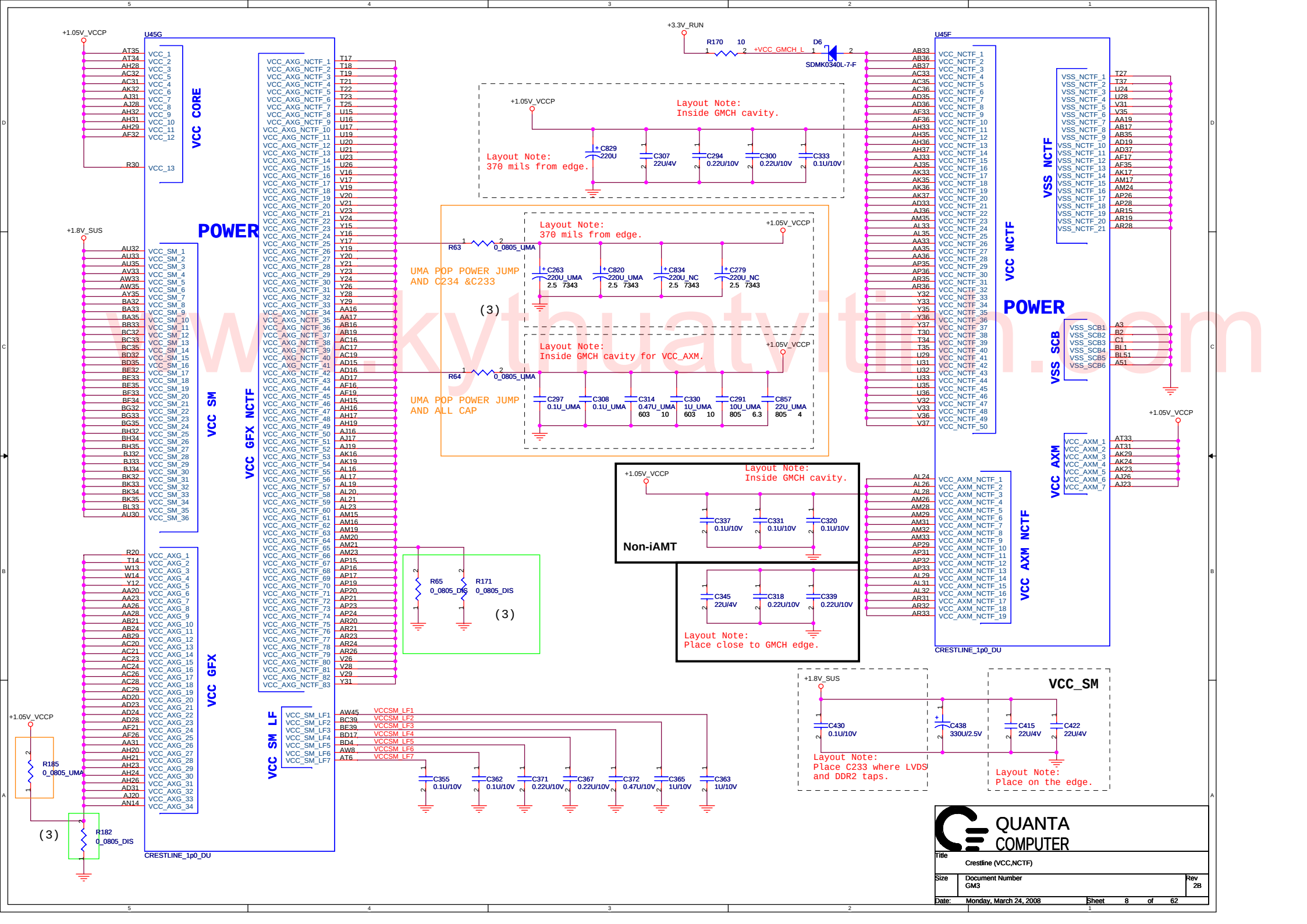
U45G
U45F
POWER
VCC CORE
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
VCC NCTF
VSS NCTF
VSS SCB
VCC AXM
VCC AXM NCTF
VCC_SM
+1.05V_VCCP
+1.8V_SUS
+3.3V_RUN
+VCC_GMCH_L
R170 10
D6
SDMK0340L-7-F
Layout Note:
Inside GMCH cavity.
Layout Note:
370 mils from edge.
C829 220U
C307 22U/4V
C294 0.22U/10V
C300 0.22U/10V
C333 0.1U/10V
R63 0_0805_UMA
R64 0_0805_UMA
UMA POP POWER JUMP
AND C234 &C233
(3)
C263 220U_UMA 2.5 7343
C820 220U_UMA 2.5 7343
C834 220U_NC 2.5 7343
C279 220U_NC 2.5 7343
Layout Note:
Inside GMCH cavity for VCC_AXM.
UMA POP POWER JUMP
AND ALL CAP
C297 0.1U_UMA
C308 0.1U_UMA
C314 0.47U_UMA 603 10
C330 1U_UMA 603 10
C291 10U_UMA 805 6.3
C857 22U_UMA 805 4
R65 0_0805_DIS
R171 0_0805_DIS
Non-iAMT
C337 0.1U/10V
C331 0.1U/10V
C320 0.1U/10V
C345 22U/4V
C318 0.22U/10V
C339 0.22U/10V
Layout Note:
Place close to GMCH edge.
R185 0_0805_UMA
R182 0_0805_DIS
C355 0.1U/10V
C362 0.1U/10V
C371 0.22U/10V
C367 0.22U/10V
C372 0.47U/10V
C365 1U/10V
C363 1U/10V
C430 0.1U/10V
C438 330U/2.5V
C415 22U/4V
C422 22U/4V
Layout Note:
Place C233 where LVDS
and DDR2 taps.
Layout Note:
Place on the edge.
CRESTLINE_1p0_DU
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Crestline (VCC,NCTF)
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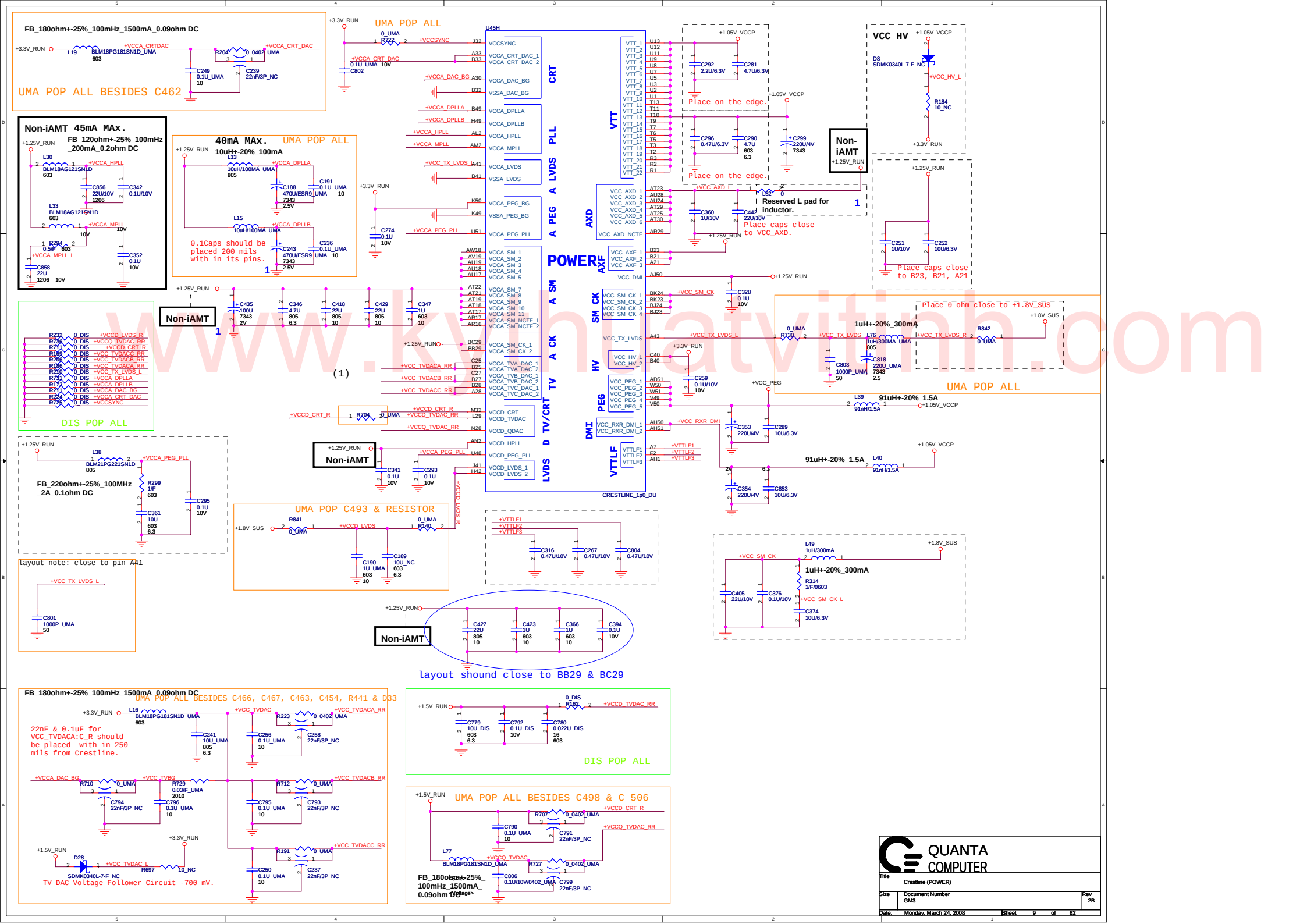

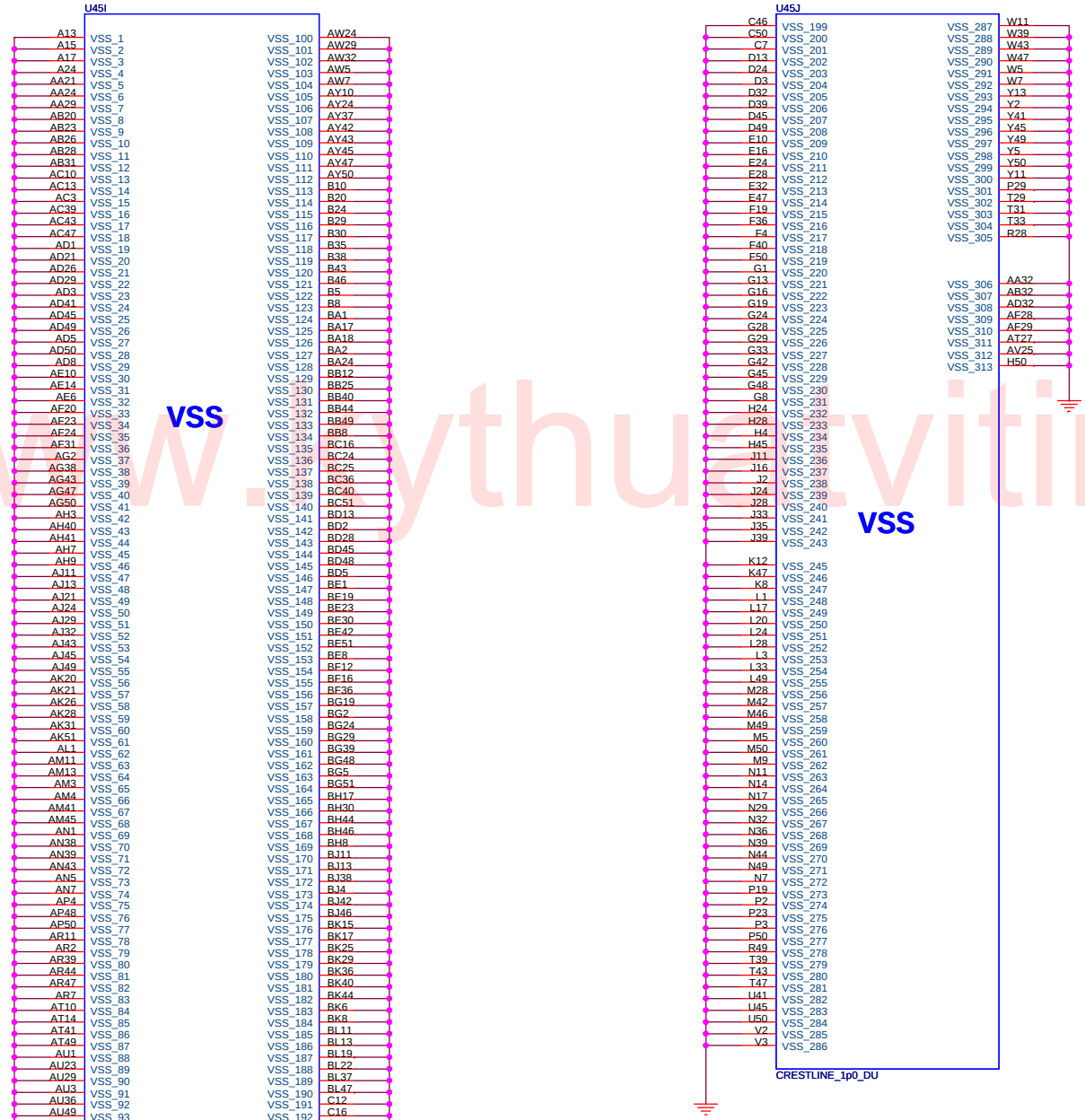

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Title	Crestline (VSS)	
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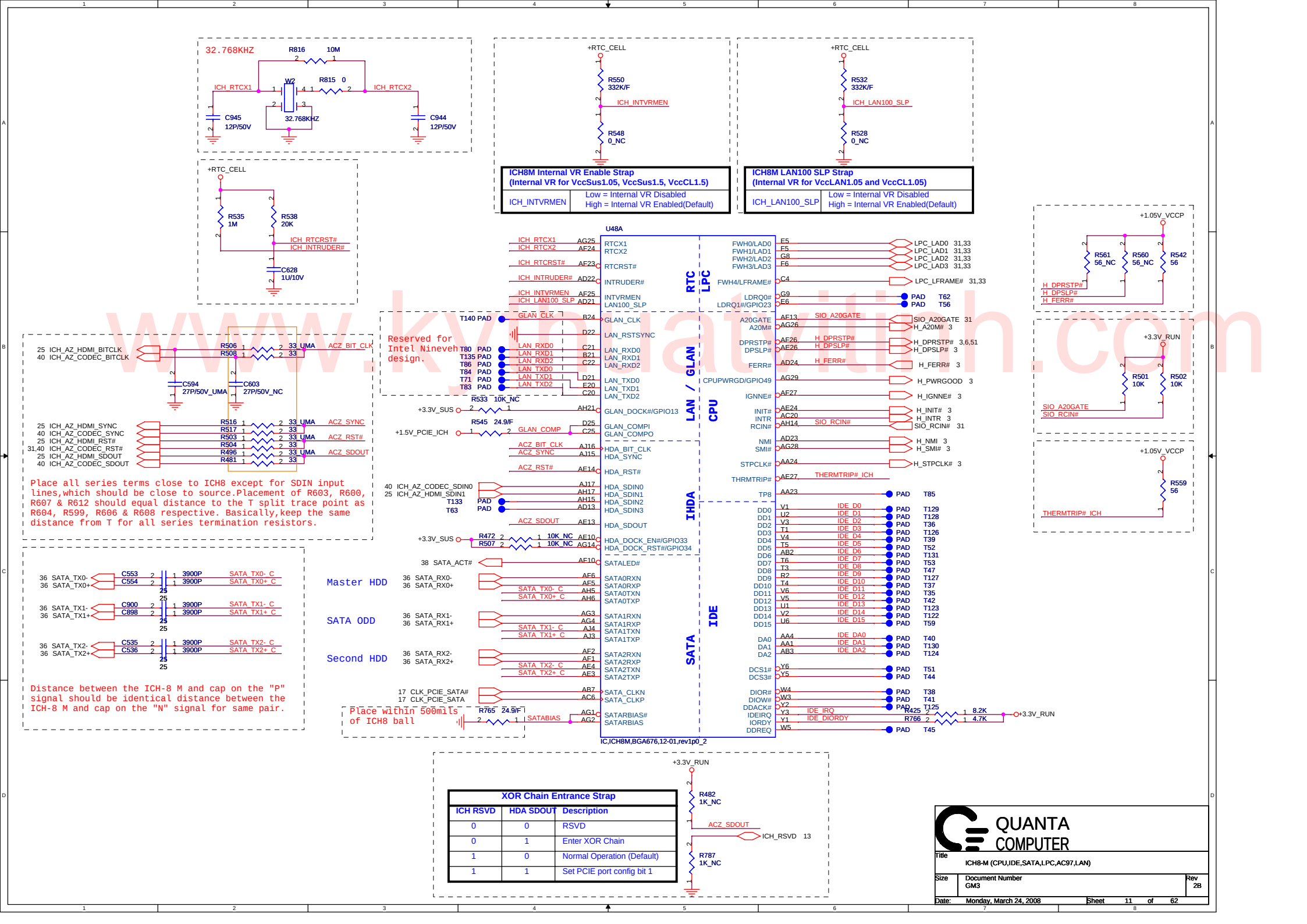
32.768KHZ
R816 10M
W2
R815 0
ICH_RTCX1
ICH_RTCX2
C945 12P/50V
32.768KHZ
C944 12P/50V
+RTC_CELL
R535 1M
R538 20K
ICH_RTCRST#
ICH_INTRUDER#
C628 1U/10V
+RTC_CELL
R550 332K/F
ICH_INTVRMEN
R548 0_NC
ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)
ICH_INTVRMEN
Low = Internal VR Disabled
High = Internal VR Enabled(Default)
+RTC_CELL
R532 332K/F
ICH_LAN100_SLP
R528 0_NC
ICH8M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)
ICH_LAN100_SLP
Low = Internal VR Disabled
High = Internal VR Enabled(Default)
U48A
RTC
LPC
GLAN
LAN
CPU
IHDA
IDE
SATA
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
IC,ICH8M,BGA676,12-01,rev1p0_2
T140 PAD
Reserved for Intel Nineveh design.
T80 PAD
T135 PAD
T86 PAD
T84 PAD
T71 PAD
T83 PAD
R533 10K_NC
+3.3V_SUS
R545 24.9/F
+1.5V_PCIE_ICH
GLAN_COMP
ACZ_BIT_CLK
ACZ_SYNC
ACZ_RST#
ACZ_SDOUT
T133 PAD
T63 PAD
R472 10K_NC
R507 10K_NC
+3.3V_SUS
38 SATA_ACT#
Master HDD
SATA ODD
Second HDD
SATA_TX0- C
SATA_TX0+ C
SATA_TX1- C
SATA_TX1+ C
SATA_TX2- C
SATA_TX2+ C
17 CLK_PCIE_SATA#
17 CLK_PCIE_SATA
Place within 500mils of ICH8 ball
R765 24.9/F
SATABIAS
Place all series terms close to ICH8 except for SDIN input lines,which should be close to source.Placement of R603, R600, R607 & R612 should equal distance to the T split trace point as R604, R599, R606 & R608 respective. Basically,keep the same distance from T for all series termination resistors.
Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-8 M and cap on the "N" signal for same pair.
+1.05V_VCCP
R561 56_NC
R560 56_NC
R542 56
H_DPRSTP#
H_DPSLP#
H_FERR#
+3.3V_RUN
R501 10K
R502 10K
SIO_A20GATE
SIO_RCIN#
+1.05V_VCCP
R559 56
THERMTRIP#_ICH
R425 8.2K
R766 4.7K
+3.3V_RUN
XOR Chain Entrance Strap
ICH RSVD | HDA SDOUT | Description
0 | 0 | RSVD
0 | 1 | Enter XOR Chain
1 | 0 | Normal Operation (Default)
1 | 1 | Set PCIE port config bit 1
+3.3V_RUN
R482 1K_NC
ACZ_SDOUT
ICH_RSVD 13
R787 1K_NC
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Title
ICH8-M (CPU,IDE,SATA,LPC,AC97,LAN)
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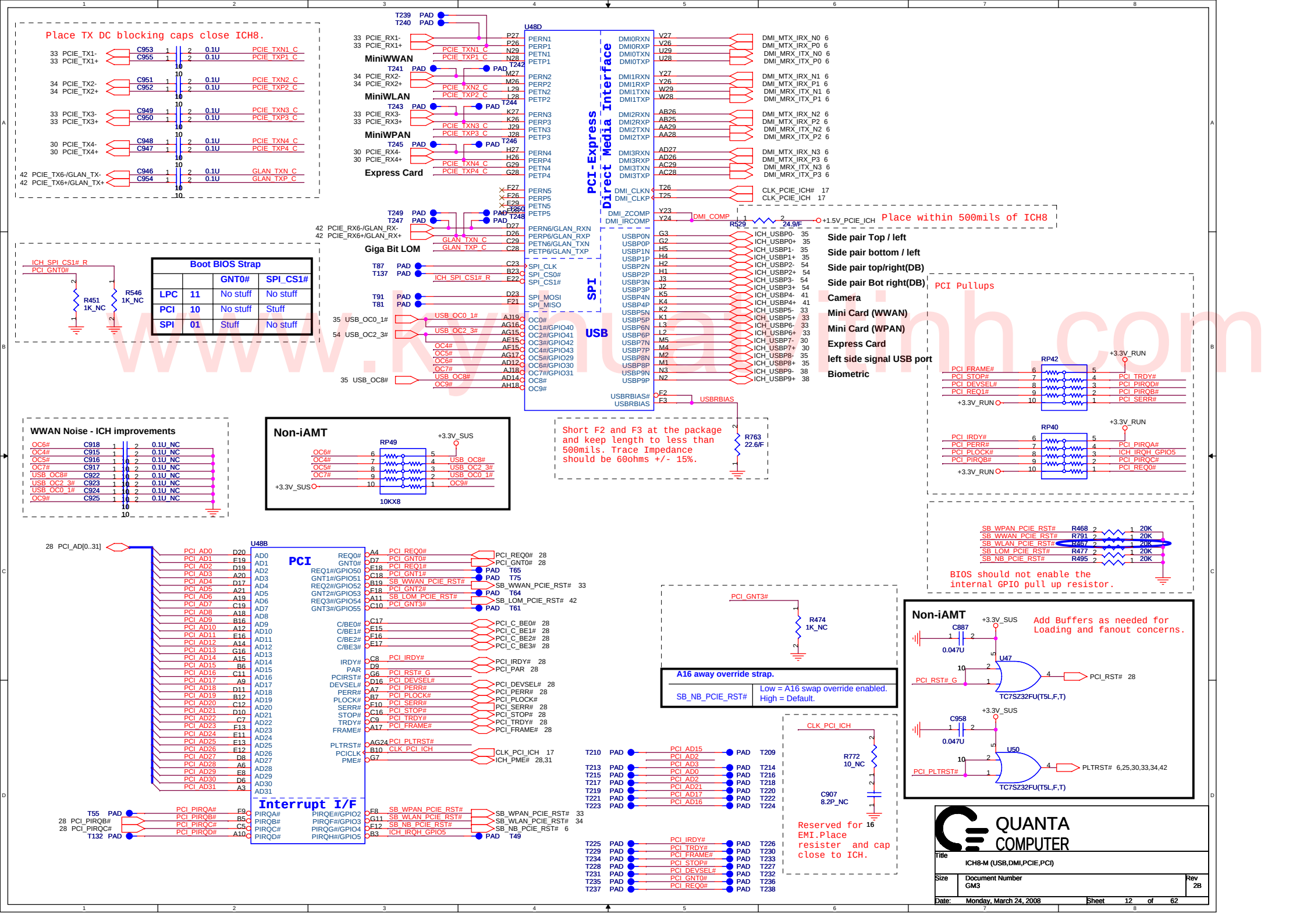
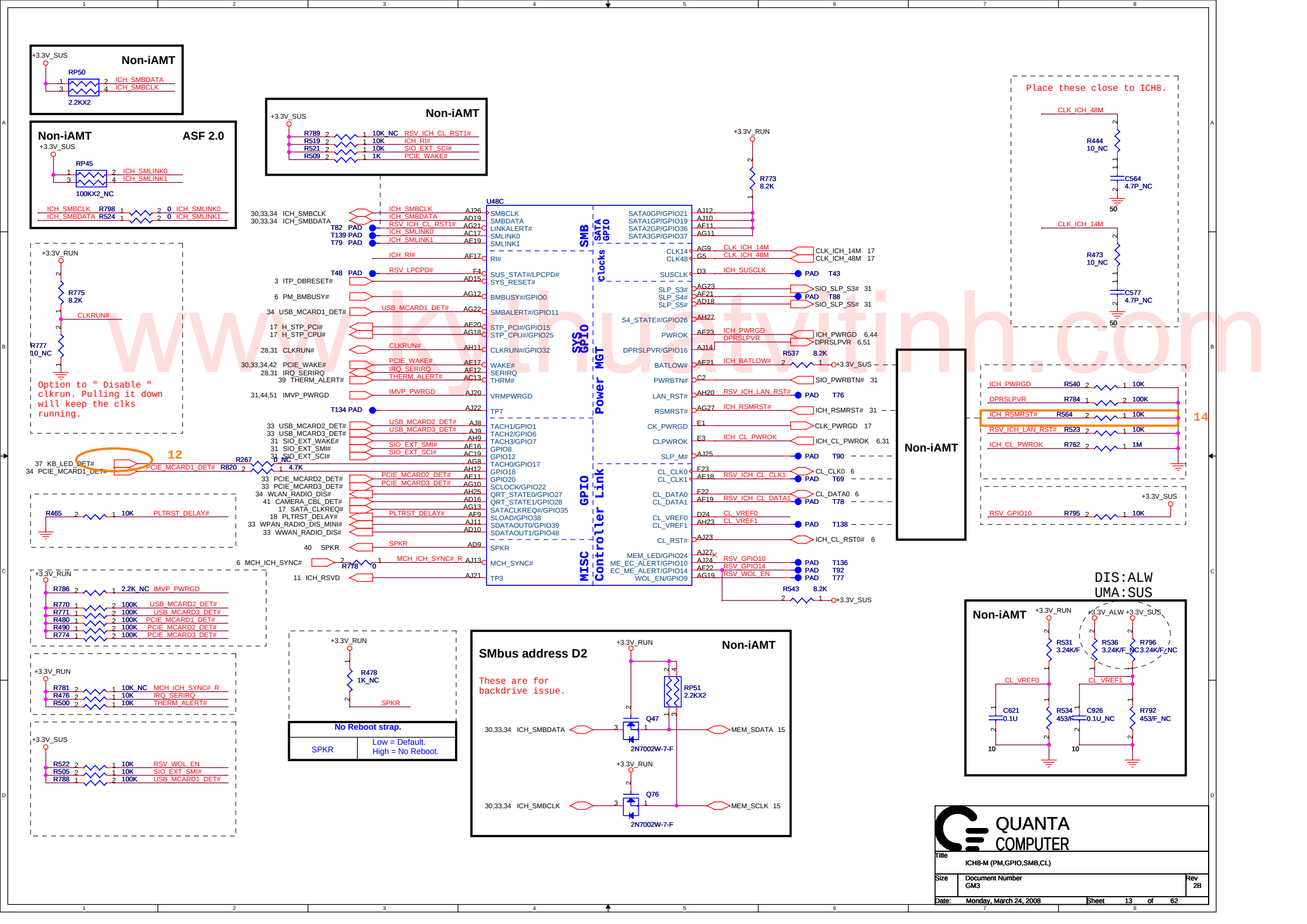
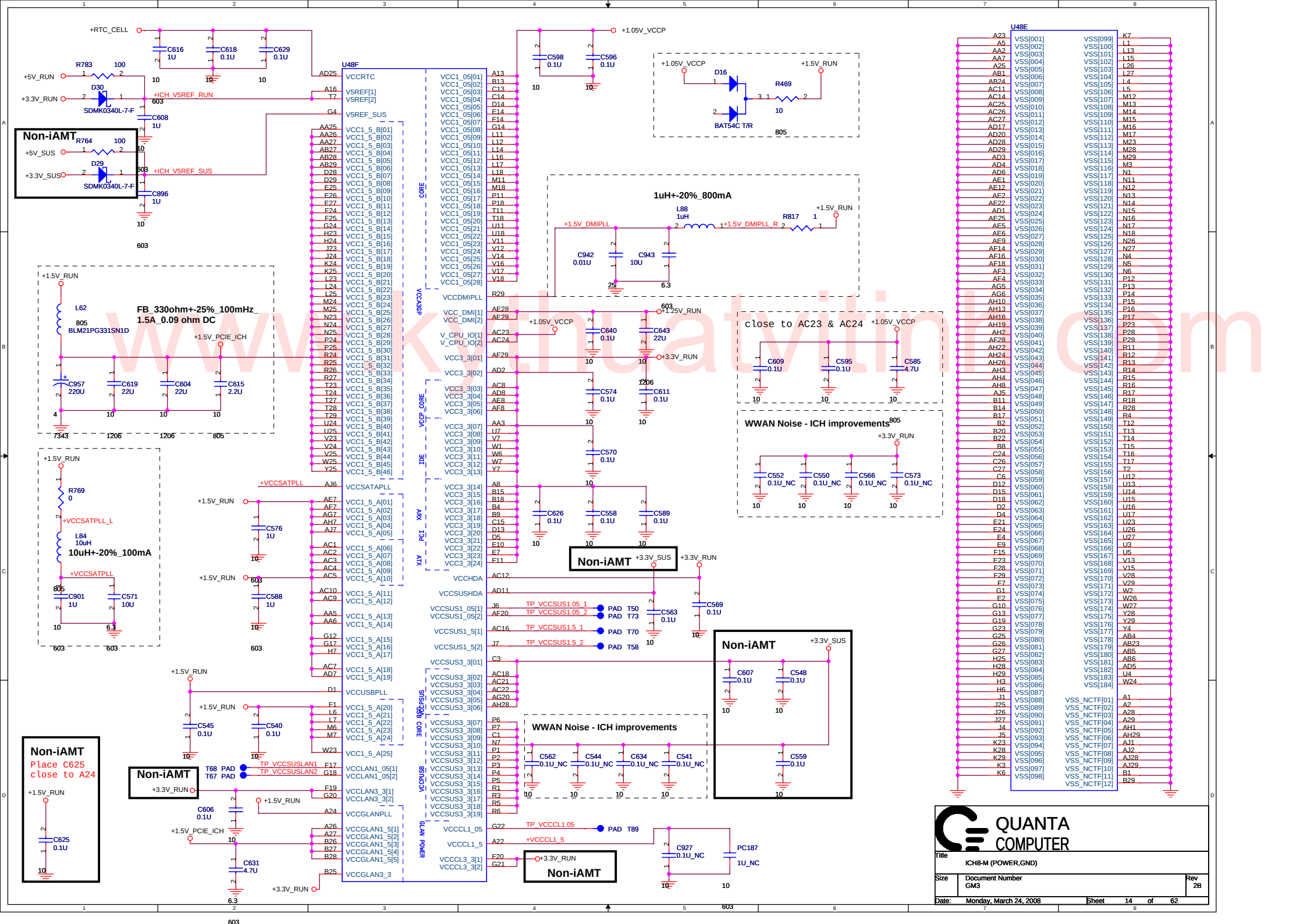
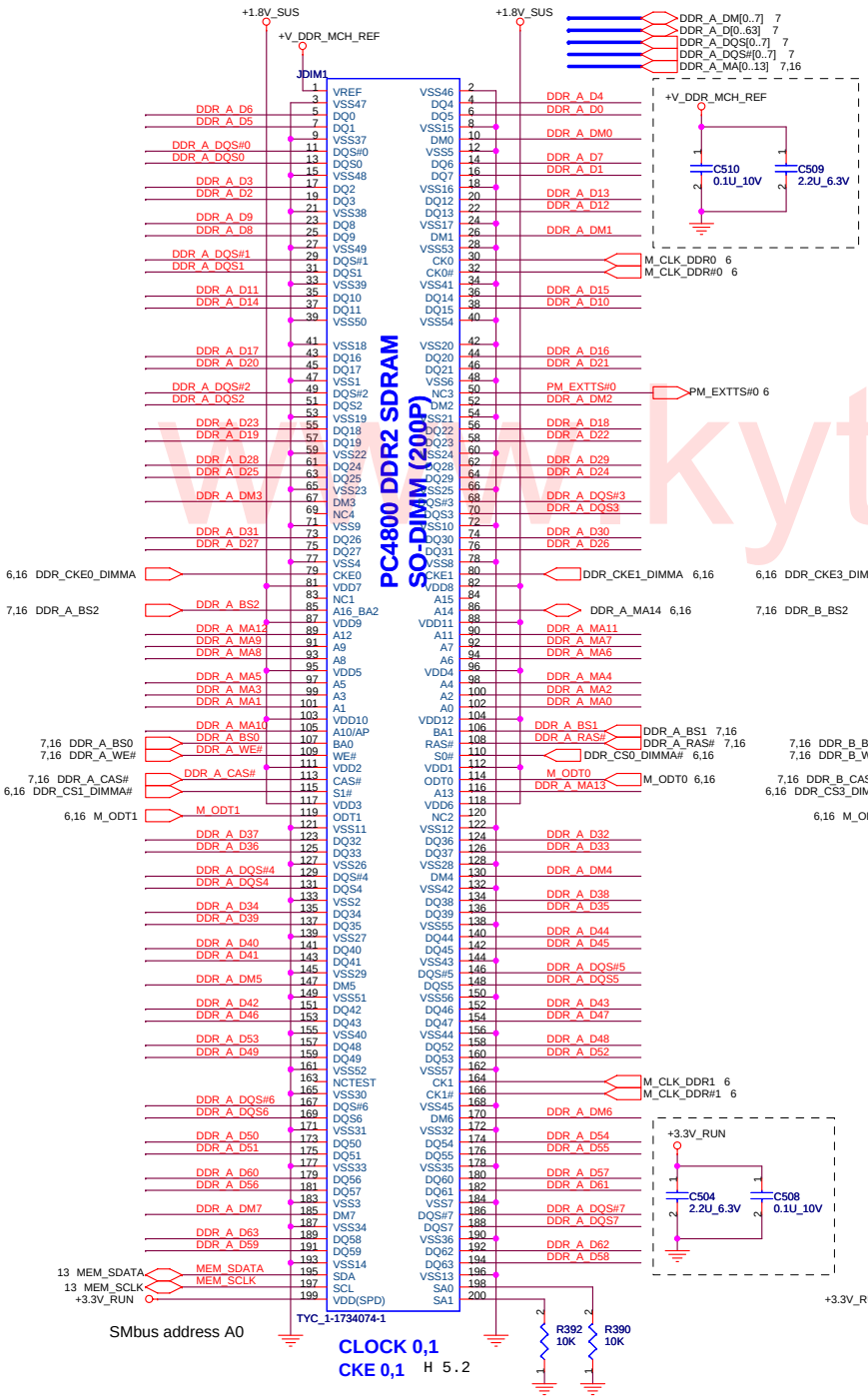

Place TX DC blocking caps close ICH8.
33 PCIE_TX1-
33 PCIE_TX1+
C953 C955 0.1U
PCIE_TXN1_C
PCIE_TXP1_C
34 PCIE_TX2-
34 PCIE_TX2+
C951 C952 0.1U
PCIE_TXN2_C
PCIE_TXP2_C
33 PCIE_TX3-
33 PCIE_TX3+
C949 C950 0.1U
PCIE_TXN3_C
PCIE_TXP3_C
30 PCIE_TX4-
30 PCIE_TX4+
C948 C947 0.1U
PCIE_TXN4_C
PCIE_TXP4_C
42 PCIE_TX6-/GLAN_TX-
42 PCIE_TX6+/GLAN_TX+
C946 C954 0.1U
GLAN_TXN_C
GLAN_TXP_C
U48D
PCI-Express Direct Media Interface
33 PCIE_RX1-
33 PCIE_RX1+
MiniWWAN
34 PCIE_RX2-
34 PCIE_RX2+
MiniWLAN
33 PCIE_RX3-
33 PCIE_RX3+
MiniWPAN
30 PCIE_RX4-
30 PCIE_RX4+
Express Card
42 PCIE_RX6-/GLAN_RX-
42 PCIE_RX6+/GLAN_RX+
Giga Bit LOM
DMI_MTX_IRX_N0 6
DMI_MTX_IRX_P0 6
DMI_MRX_ITX_N0 6
DMI_MRX_ITX_P0 6
DMI_MTX_IRX_N1 6
DMI_MTX_IRX_P1 6
DMI_MRX_ITX_N1 6
DMI_MRX_ITX_P1 6
DMI_MTX_IRX_N2 6
DMI_MTX_IRX_P2 6
DMI_MRX_ITX_N2 6
DMI_MRX_ITX_P2 6
DMI_MTX_IRX_N3 6
DMI_MTX_IRX_P3 6
DMI_MRX_ITX_N3 6
DMI_MRX_ITX_P3 6
CLK_PCIE_ICH# 17
CLK_PCIE_ICH 17
DMI_COMP
R529 24.9/F
+1.5V_PCIE_ICH
Place within 500mils of ICH8
SPI
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO
ICH_SPI_CS1# R
USB
35 USB_OC0_1#
54 USB_OC2_3#
35 USB_OC8#
ICH_USBP0- 35
ICH_USBP0+ 35
ICH_USBP1- 35
ICH_USBP1+ 35
ICH_USBP2- 54
ICH_USBP2+ 54
ICH_USBP3- 54
ICH_USBP3+ 54
ICH_USBP4- 41
ICH_USBP4+ 41
ICH_USBP5- 33
ICH_USBP5+ 33
ICH_USBP6- 33
ICH_USBP6+ 33
ICH_USBP7- 30
ICH_USBP7+ 30
ICH_USBP8- 35
ICH_USBP8+ 35
ICH_USBP9- 38
ICH_USBP9+ 38
USBRBIAS
Side pair Top / left
Side pair bottom / left
Side pair top/right(DB)
Side pair Bot right(DB)
Camera
Mini Card (WWAN)
Mini Card (WPAN)
Express Card
left side signal USB port
Biometric
ICH_SPI_CS1# R
PCI_GNT0#
R451 1K_NC
R546 1K_NC
Boot BIOS Strap
LPC 11 No stuff No stuff
PCI 10 No stuff Stuff
SPI 01 Stuff No stuff
PCI Pullups
PCI_FRAME#
PCI_STOP#
PCI_DEVSEL#
PCI_REQ1#
RP42
+3.3V_RUN
PCI_TRDY#
PCI_PIRQD#
PCI_PIRQB#
PCI_SERR#
PCI_IRDY#
PCI_PERR#
PCI_PLOCK#
PCI_PIRQB#
RP40
PCI_PIRQA#
ICH_IRQH_GPIO5
PCI_PIRQC#
PCI_REQ0#
WWAN Noise - ICH improvements
OC6# C918 0.1U_NC
OC4# C915 0.1U_NC
OC5# C916 0.1U_NC
OC7# C917 0.1U_NC
USB_OC8# C922 0.1U_NC
USB_OC2_3# C923 0.1U_NC
USB_OC0_1# C924 0.1U_NC
OC9# C925 0.1U_NC
Non-iAMT
RP49
10KX8
+3.3V_SUS
Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.
R763 22.6/F
SB_WPAN_PCIE_RST# R468 20K
SB_WWAN_PCIE_RST# R791 20K
SB_WLAN_PCIE_RST# R467 20K
SB_LOM_PCIE_RST# R477 20K
SB_NB_PCIE_RST# R495 20K
BIOS should not enable the internal GPIO pull up resistor.
28 PCI_AD[0..31]
U48B
PCI
PCI_REQ0# 28
PCI_GNT0# 28
PCI_GNT3#
R474 1K_NC
A16 away override strap.
SB_NB_PCIE_RST#
Low = A16 swap override enabled.
High = Default.
Non-iAMT
Add Buffers as needed for Loading and fanout concerns.
C887 0.047U
U47
TC7SZ32FU(T5L,F,T)
PCI_RST# G
PCI_RST# 28
C958 0.047U
U50
PCI_PLTRST#
PLTRST# 6,25,30,33,34,42
Interrupt I/F
SB_WPAN_PCIE_RST# 33
SB_WLAN_PCIE_RST# 34
SB_NB_PCIE_RST# 6
CLK_PCI_ICH
R772 10_NC
C907 8.2P_NC
Reserved for EMI.Place resister and cap close to ICH.
QUANTA COMPUTER
Title ICH8-M (USB,DMI,PCIE,PCI)
Size Document Number GM3 Rev 2B
Date: Monday, March 24, 2008 Sheet 12 of 62




U48F
U48E
Non-iAMT
Place C625 close to A24
FB_330ohm+-25%_100mHz_ 1.5A_0.09 ohm DC
10uH+-20%_100mA
1uH+-20%_800mA
WWAN Noise - ICH improvements
close to AC23 & AC24
+RTC_CELL
+5V_RUN
+3.3V_RUN
+5V_SUS
+3.3V_SUS
+1.5V_RUN
+1.05V_VCCP
+1.5V_PCIE_ICH
+1.5V_DMIPLL
+VCCSATAPLL
+ICH_V5REF_RUN
+ICH_V5REF_SUS
SDMK0340L-7-F
BAT54C T/R
BLM21PG331SN1D
TP_VCCSUS1.05_1
TP_VCCSUS1.05_2
TP_VCCSUS1.5_1
TP_VCCSUS1.5_2
TP_VCCSUSLAN1
TP_VCCSUSLAN2
TP_VCCCL1.05
+VCCCL1_5
QUANTA COMPUTER
ICH8-M (POWER,GND)
Document Number GM3
Rev 2B
Monday, March 24, 2008
Sheet 14 of 62

MASTER



SLAVE

Place these Caps near So-Dimm1.

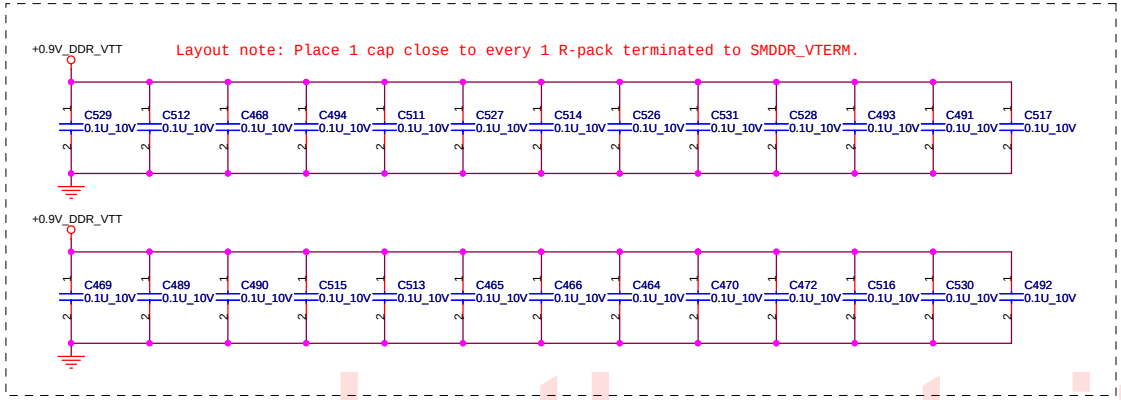
Place these Caps near So-Dimm2.

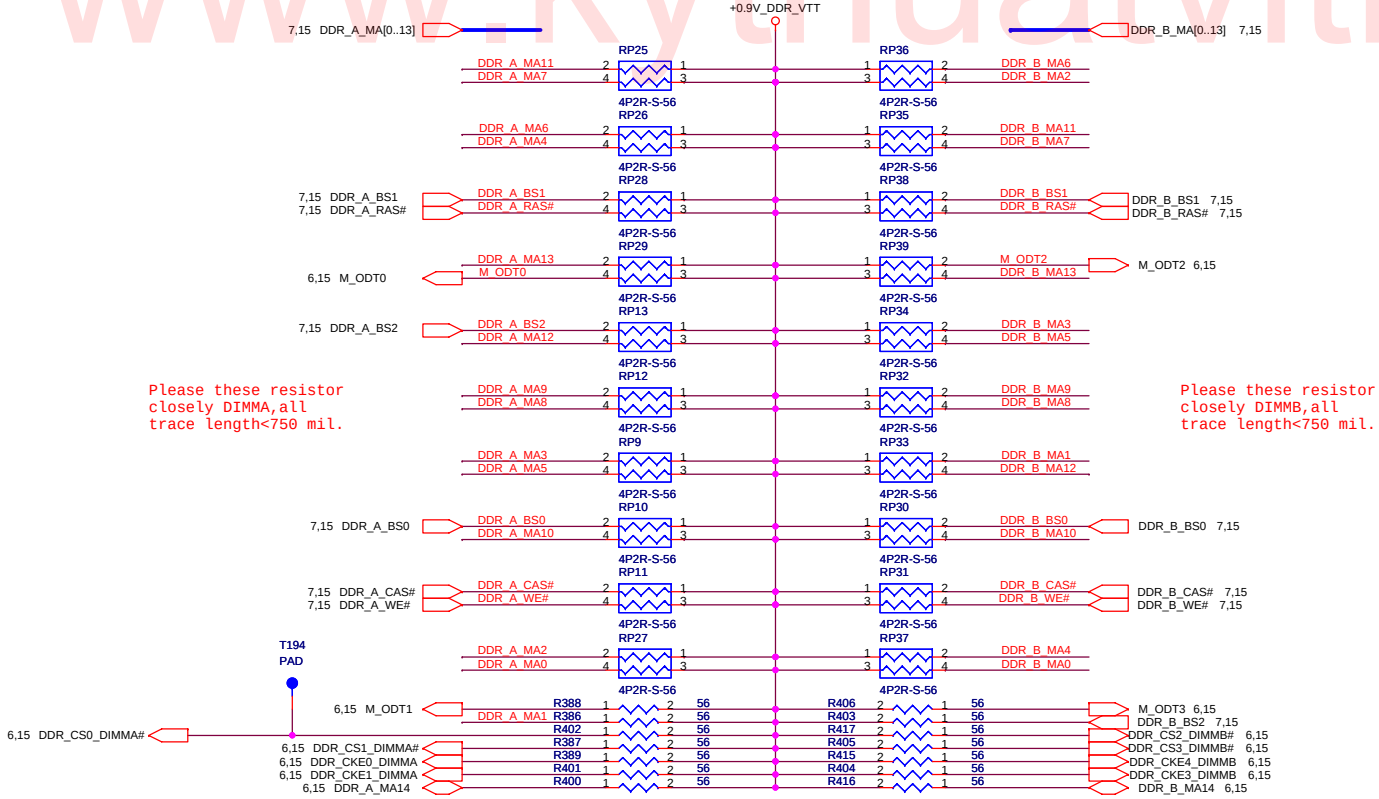
Place these Caps near So-Dimm1.

Place these Caps near So-Dimm2.

Title	DDR2_SO-DIMM (200P) X 2	
Size	Document Number GM3	Rev 2B
Date: Monday, March 24, 2008	Sheet 15 of 62	

QUANTA COMPUTER





QUANTA COMPUTER

Title	DDR2 RES. ARRAY	
Size	Document Number GM3	Rev 2B
Date: Monday, March 24, 2008	Sheet 16 of 62	

Add capacitor pads for improving WWAN.

C457 1 2 27P CLK_ICH_48M
C440 1 2 27P_NC CLK_ICH_14M
C431 1 50 2 27P_NC CLK_PCI_8512
C432 1 50 2 27P_NC CLK_PCI_PCCARD
C439 1 50 2 27P_NC CLK_PCI_ICH
50

Y2
CLK_XTAL_IN 1 2 CLK_XTAL_OUT
14.318MHZ
C437 33P 50
C443 33P 50
14.318MHz

U19
CK505
QFN64
SLG8SP513V

+CK_VDD_PCI 9
+CK_VDD_PLL3 4
+CK_VDD_48 23
+CK_VDD_SRC 16
46
62
+CK_VDD_MAIN 19
27
33
43
52
56
VDD_PCI VDD_REF VDD_PLL3 VDD_48 VDD_SRC VDD_CPU
VDD_IO VDD_IO VDD_IO VDD_IO VDD_IO VDD_IO VDD_IO
15 18 22 26 30 36 49 59 1
GND GND GND GND GND GND GND GND GND

13 SATA_CLKREQ# SATA_CLKREQ# R365 475
6 CLK_3GPLLREQ# CLK_3GPLLREQ# R364 475/F
33 CLK_LPC_DEBUG CLK_LPC_DEBUG R363 22_NC
28 CLK_PCI_PCCARD CLK_PCI_PCCARD R354 33
31 CLK_PCI_8512 CLK_PCI_8512 R353 33
12 CLK_PCI_ICH CLK_PCI_ICH R350 33
13 CLK_ICH_48M CLK_ICH_48M R375 33
3,6 CPU_MCH_BSEL0 L55 BLM18SG260 R372 8.2K
3,6 CPU_MCH_BSEL1 R374 8.2K
3,6 CPU_MCH_BSEL2 R367 8.2K
13 CLK_ICH_14M CLK_ICH_14M R366 33

SATA_CLKREQ# C 8
CLK_3GPLLREQ# C 10
PCI_PCCARD 11
PCI_SIO 12
27M_SEL 13
PCI_ICH 14
CR#_A/PCI-0 CR_B/PCI-1 TME/PCI-2 SRC5_EN/PCI-3 27M_SEL/PCI-4 ITP_EN/PCIF-5#
FSA 17
FSB 64
FSC 5
FSA/USB48 FSB/TEST_MODE FSC/TEST_SEL/REF
55
63
RESET# CK_PWRGD/PD#

CLK_XTAL_OUT 2
CLK_XTAL_IN 3
XOUT XIN
CLK_SDATA 6
CLK_SCLK 7
SDATA SCLK
GND 65

CPU-0 61 CPU_BCLK RP5 0 CLK_CPU_BCLK 3
CPU-0# 60 CPU_BCLK# CLK_CPU_BCLK# 3
CPU-1 58 MCH_BCLK RP7 0 CLK_MCH_BCLK 5
CPU-1# 57 MCH_BCLK# CLK_MCH_BCLK# 5
SRC-8/CPU_ITP 54 CPU_ITP RP17 0 CLK_PCIE_MINI1 34
SRC-8#/CPU_ITP# 53 CPU_ITP# CLK_PCIE_MINI1# 34
SRC-0/DOT96 20 DOT96_SSC RP4 0_DIS CLK_PCIE_VGA 18
SRC-0#/DOT96# 21 DOT96_SSC# CLK_PCIE_VGA# 18
SRC-1/SE1 24 27M_NSS RP8 0_DIS CLK_VGA_27M_NSS 19
SRC-1#/SE2 25 27M_SS CLK_VGA_27M_SS 19
SRC-2/SATA 28 PCIE_SATA RP16 0 CLK_PCIE_SATA 11
SRC-2#/SATA# 29 PCIE_SATA# CLK_PCIE_SATA# 11
CR#_C/SRC-3 31 PCIE_MINI3 RP18 0 CLK_PCIE_MINI3 33
CR#_D/SRC-3# 32 PCIE_MINI3# CLK_PCIE_MINI3# 33
SRC-4 34 MCH_3GPLL RP20 0 CLK_MCH_3GPLL 6
SRC-4# 35 MCH_3GPLL# CLK_MCH_3GPLL# 6
PCI_STOP#/SRC-5 45 H_STP_PCI# 13
CPU_STOP#/SRC-5# 44 H_STP_CPU# 13
SRC-6 48 PCIE_EXPCARD RP24 0 CLK_PCIE_EXPCARD 30
SRC-6# 47 PCIE_EXPCARD# CLK_PCIE_EXPCARD# 30
CR#_F/SRC-7 51 MINI1CLK_REQ#_C R394 475/F MINI1CLK_REQ# MINI1CLK_REQ# 34
CR#_E/SRC-7# 50 CARD_CLK_REQ#_C R395 475/F CARD_CLK_REQ# CARD_CLK_REQ# 30
SRC-9 37 PCIE_MINI2 RP21 0 CLK_PCIE_MINI2 33
SRC-9# 38 PCIE_MINI2# CLK_PCIE_MINI2# 33
SRC-10 41 PCIE_ICH RP23 0 CLK_PCIE_ICH 12
SRC-10# 42 PCIE_ICH# CLK_PCIE_ICH# 12
CR#_H/SRC-11 40 PCIE_LOM RP22 0 CLK_PCIE_LOM 42
CR#_G/SRC-11# 39 PCIE_LOM# CLK_PCIE_LOM# 42

13

to ATI VGA

+3.3V_RUN
H_STP_PCI# R397 10K
H_STP_CPU# R396 10K

Silego need pull up but other?

CLK_LPC_DEBUG FOR DEBUG
NEED POP RESISTOR

POP RESISTOR FOR UMA

to MCH DPLL_REF_CLK
DOT96_SSC 4 RP6 0_UMA 3 MCH_DREFCLK 6
DOT96_SSC# 2 1 MCH_DREFCLK# 6

to MCH DPLL_REF_SSCLK
27M_SS 2 RP14 0_UMA 1 DREF_SSCLK# 6
27M_NSS 4 3 DREF_SSCLK 6
13

CPU_ITP 2 RP15 0_NC 3 CLK_CPU_ITP 3
CPU_ITP# 4 1 CLK_CPU_ITP# 3
POP for ITP use

+3.3V_RUN
CLK_3GPLLREQ# R355 10K
SATA_CLKREQ# R356 10K
CARD_CLK_REQ# R398 10K
MINI1CLK_REQ# R399 10K
PCI_PCCARD R343 10K_NC

PCI_SIO R352 10K_NC
PCI_ICH R341 10K_NC

UMA without iAMT

+3.3V_RUN
L58 BLM21PG600SN1D 805 120 ohms@100Mhz
+CK_VDD_MAIN
C459 0.1U C476 0.1U C486 0.1U C462 0.1U C473 0.1U C485 0.1U C487 10U_NC
10 10 10 10 10 10 6.3

L51 BLM21PG600SN1D 805 120 ohms@100Mhz
R359 2.2 +CK_VDD_PCI C446 0.1U 10
R391 2.2 +CK_VDD_PLL3 C461 0.1U 10
R358 2.2 +CK_VDD_48 C448 0.1U C447 4.7U 10 6.3
R377 2.2 +CK_VDD_SRC 603 C460 0.1U 10

Non-iAMT

SMbus address D2
These are for backdrive issue.

+3.3V_RUN
RP3 2.2KX2
26,31,39 SMBDAT1 Q40 2N7002W-7-F CLK_SDATA
26,31,39 SMBCLK1 Q39 2N7002W-7-F CLK_SCLK

+3.3V_RUN
R339 10K_NC
PCI_ICH
R340 10K_NC

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

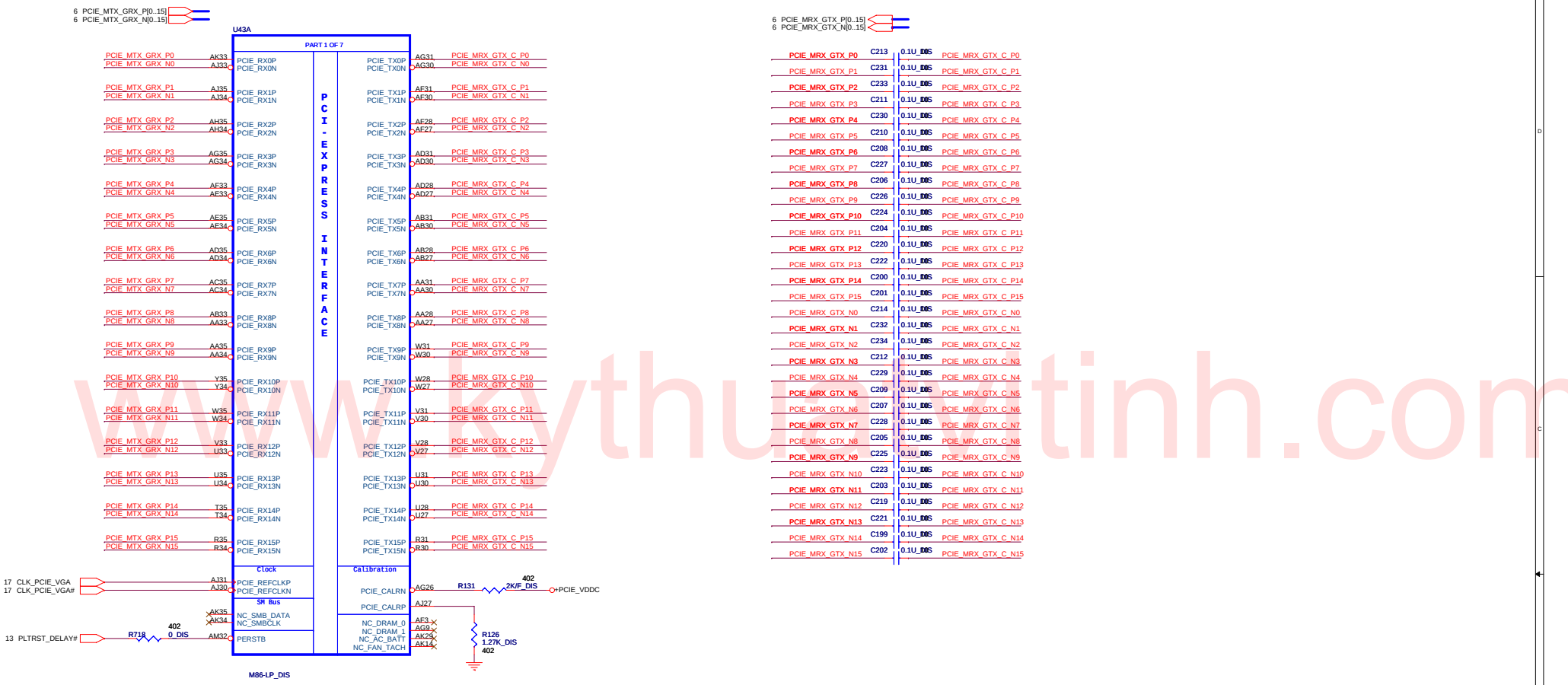
+3.3V_RUN
R351 10K_DIS
27M_SEL
R342 10K_UMA

27M_SEL

27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/ 100M_T	96/ 100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout

QUANTA COMPUTER

Title	CLOCK GENERATOR	
Size	Document Number GM3	Rev 2B
Date: Monday, March 24, 2008	Sheet 17 of 62	



QUANTA COMPUTER

Title	VGA-M82-S (PCIe)	
Size	Document Number GM3	Rev 2B
Date: Monday, March 24, 2008	Sheet 18 of 62	

MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GPIO9	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	X	0	0	0
256MB	X	0	0	1
64MB	X	0	1	0
512MB	X	1	0	0

Memory Straps	RAM_ TYPE_CFG3	RAM_ TYPE_CFG2	RAM_ TYPE_CFG1	RAM_ TYPE_CFG0
400 MHz 256MB(16M*16) Hynix	1	1	1	1
400 MHz 256MB(16M*16) Qimonda	1	1	1	0
500 MHz 256MB(16M*16) Hynix	1	1	0	1
500 MHz 256MB(16M*16) Qimonda	1	1	0	0
500 MHz 256MB(16M*16) Samsung	1	0	1	1

8/15: The strap on VIP[3] is for enabling HD Audio on M86.

VRAM SIZE

VRAM TYPE

HDMI CONN

LVDS

HDMI

CRT

DIS only

Layout Note: Place 150 ohm termination resistors close to ATI CHIP.

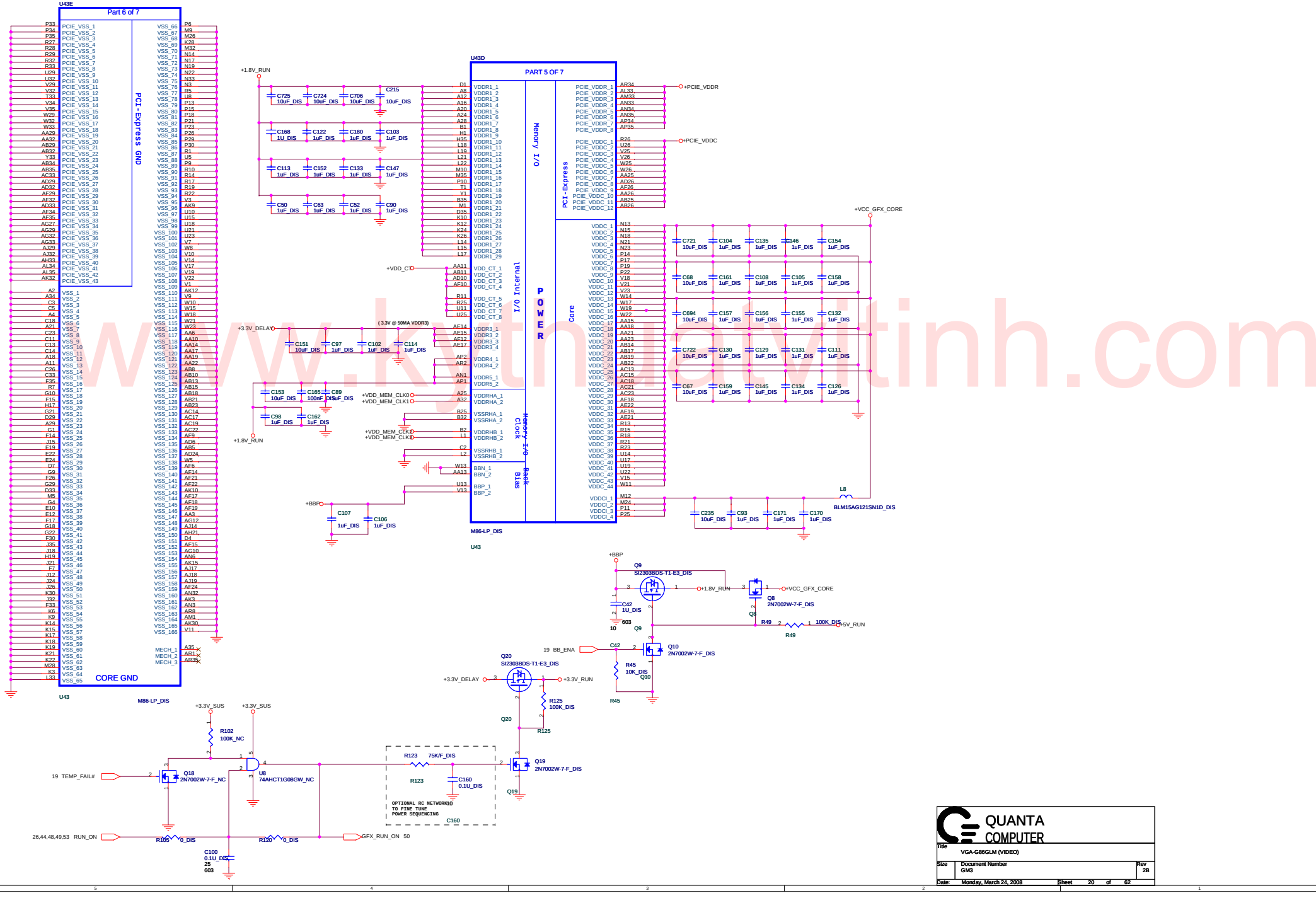
GPIO_23_CLKREQB DRIVES LOW DURING RESET

PLACE VREF DIVIDER AND CAP CLOSE TO ASIC

PLACE OR RESISTORS CLOSE TO ASIC

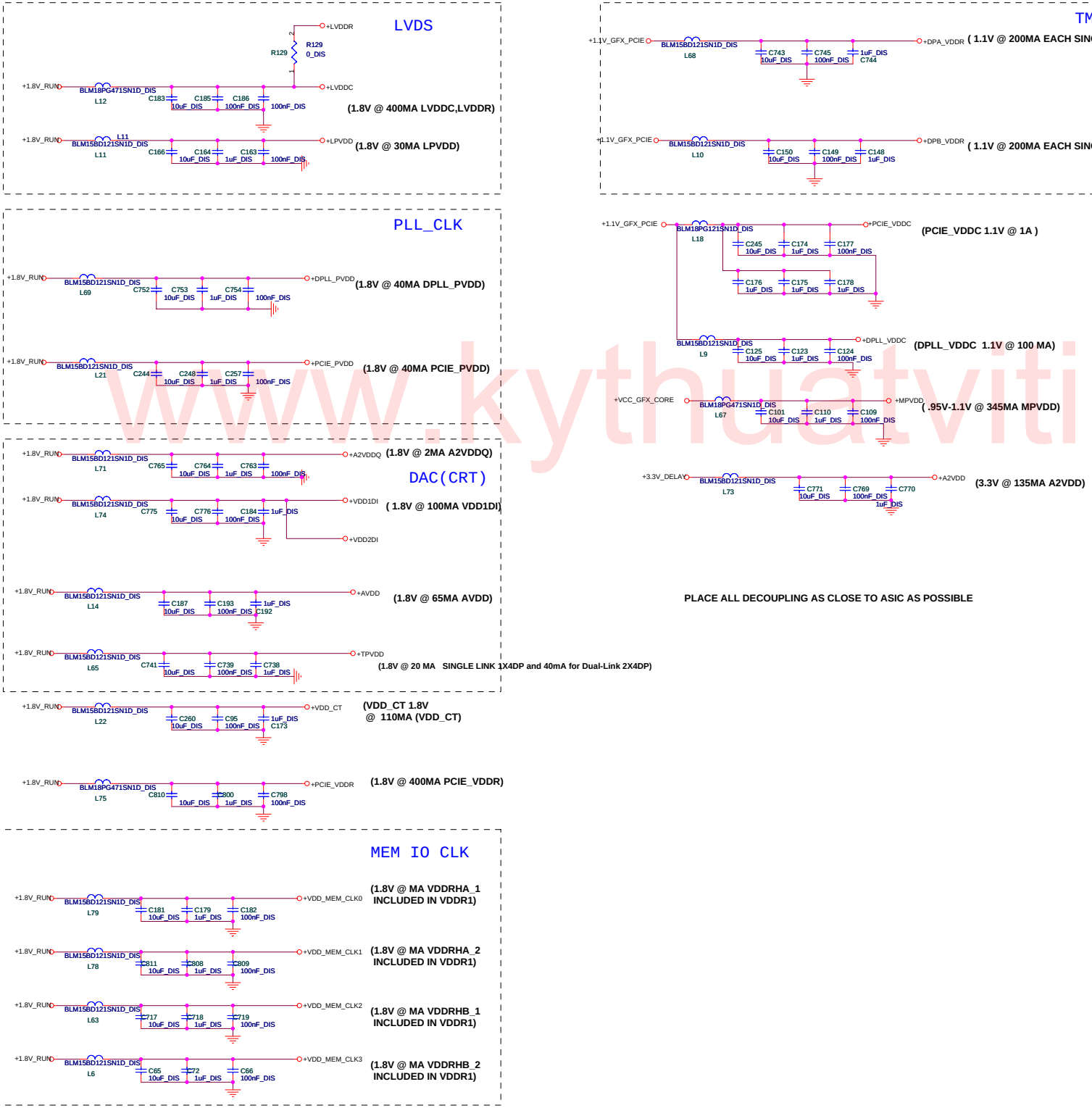
Title	VGA-G86GLM (VIDEO)
Size	Document Number GM3
Rev	2B
Date:	Monday, March 24, 2008
Sheet	19 of 62

QUANTA COMPUTER



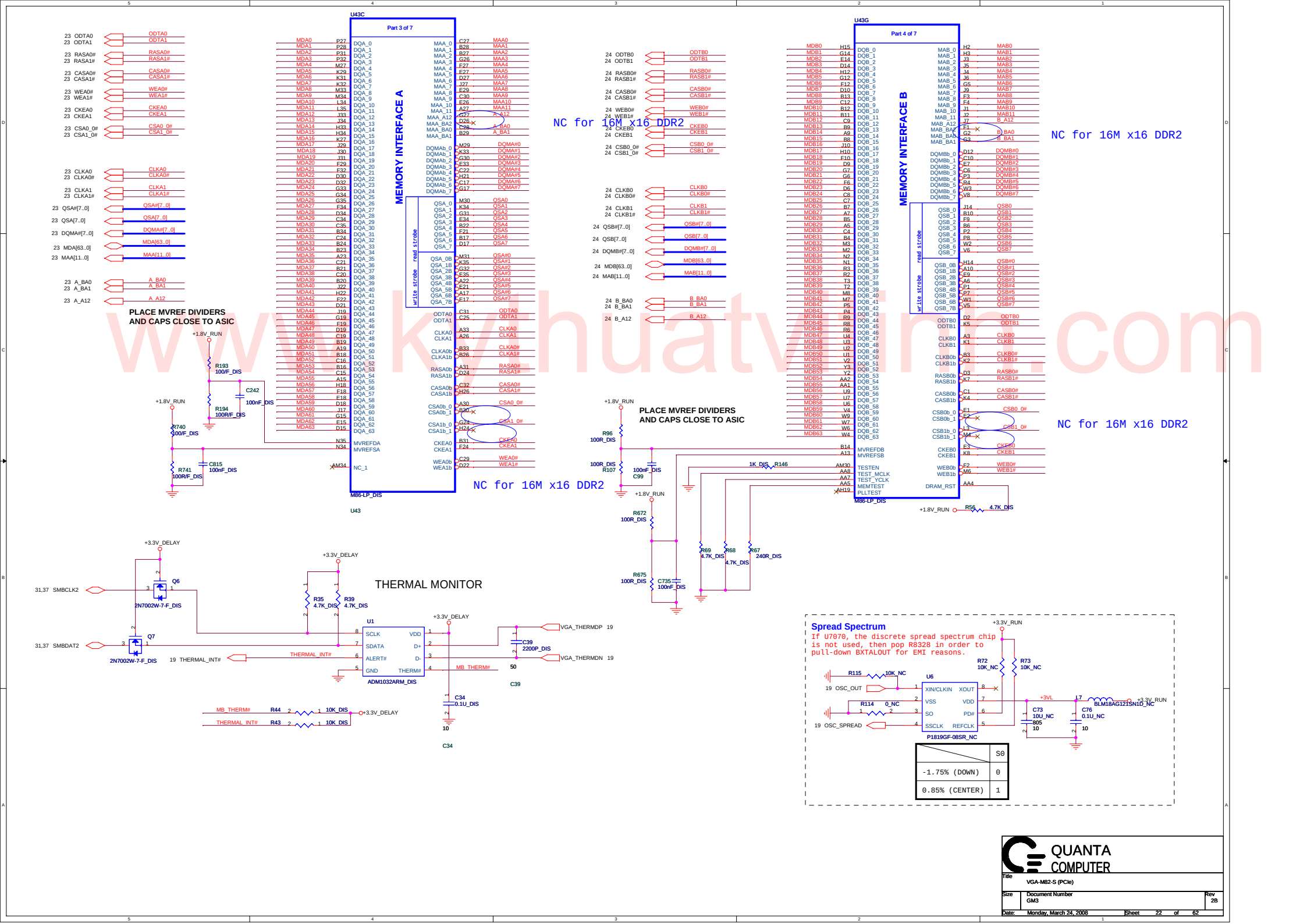
Title	VGA-G86GLM (VIDEO)
Size	Document Number GM3
Rev	2B
Date:	Monday, March 24, 2008
Sheet	20 of 62

QUANTA COMPUTER



QUANTA COMPUTER

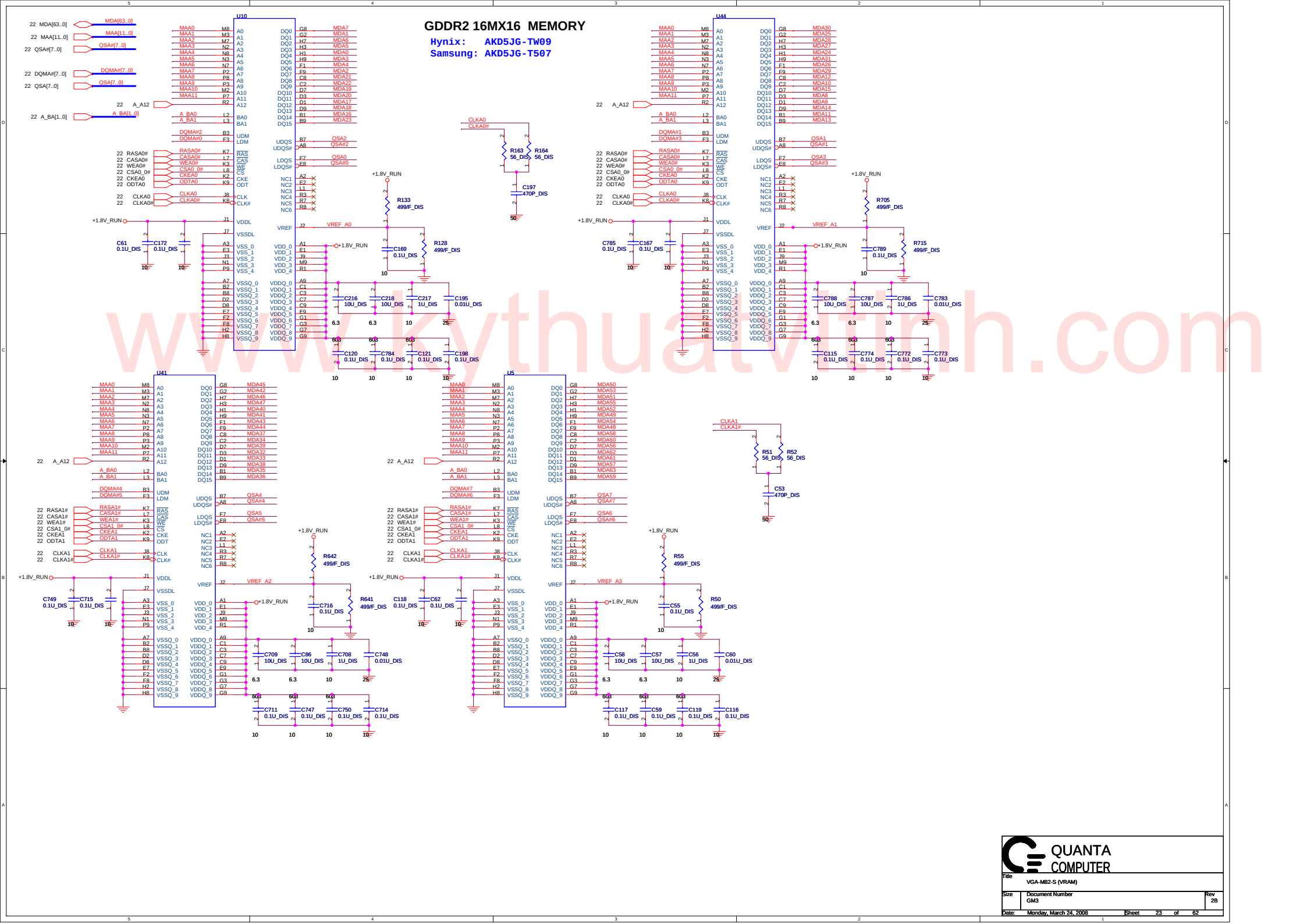
Title	VGA-G86GLM (VIDEO)	
Size	Document Number GM3	Rev 2B
Date: Monday, March 24, 2008	Sheet 21 of 62	


U43C
Part 3 of 7
MEMORY INTERFACE A
U43
M86-LP_DIS
NC for 16M x16 DDR2
PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC
U43G
Part 4 of 7
MEMORY INTERFACE B
NC for 16M x16 DDR2
NC for 16M x16 DDR2
PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC
THERMAL MONITOR
ADM1032ARM_DIS
2N7002W-7-F_DIS
2N7002W-7-F_DIS
P1819GF-08SR_NC
Spread Spectrum
If U7070, the discrete spread spectrum chip
is not used, then pop R8328 in order to
pull-down BXTALOUT for EMI reasons.
-1.75% (DOWN) 0
0.85% (CENTER) 1
QUANTA COMPUTER
VGA-M82-S (PCIe)
GM3
Monday, March 24, 2008
Sheet 22 of 62

GDDR2 16MX16 MEMORY

Hynix: AKD5JG-TW09

Samsung: AKD5JG-T507



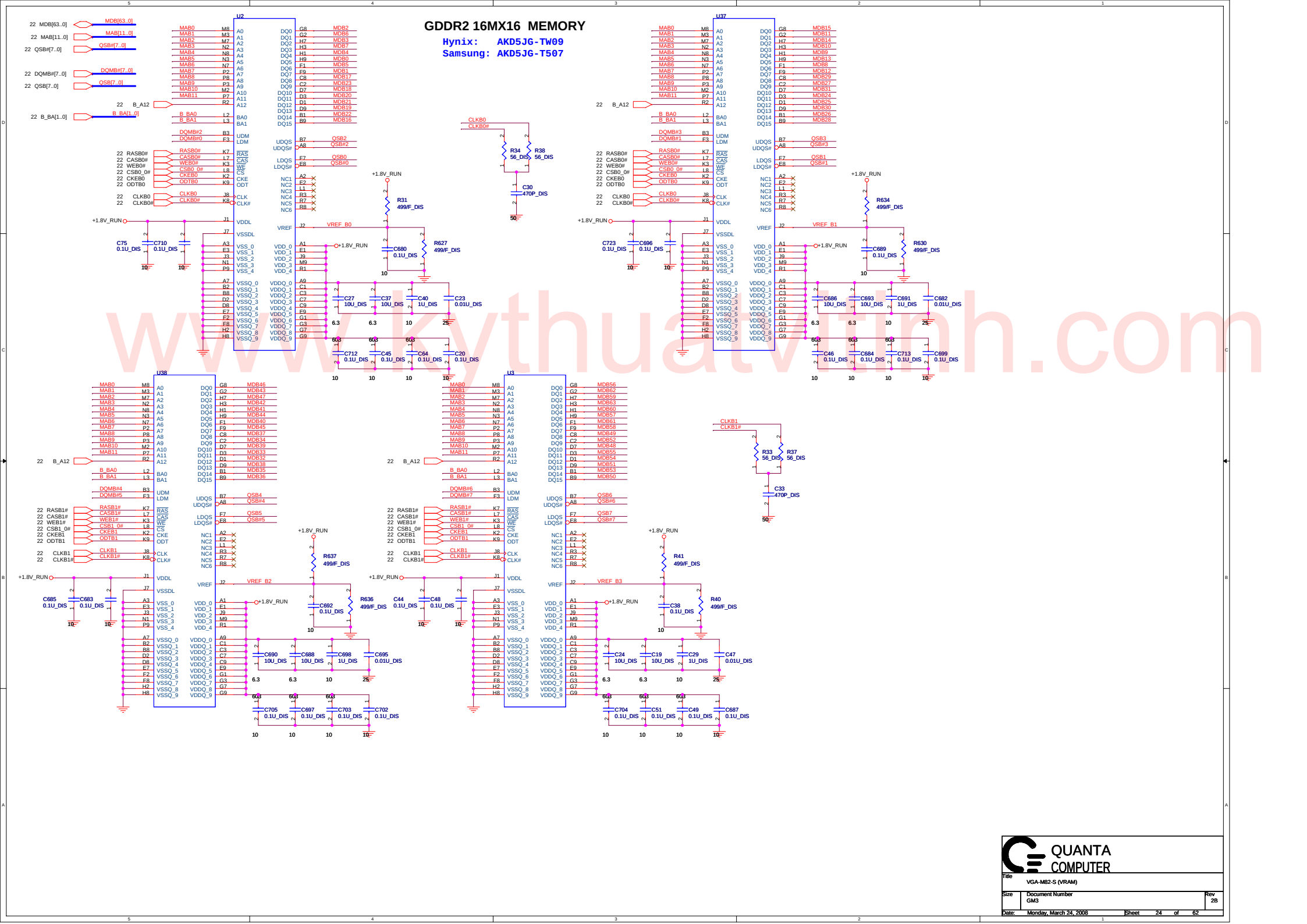
QUANTA COMPUTER

Title	VGA-M82-S (VRAM)	
Size	Document Number GM3	Rev 2B
Date: Monday, March 24, 2008	Sheet 23 of 62	

GDDR2 16MX16 MEMORY

Hynix: AKD5JG-TW09

Samsung: AKD5JG-T507



Title	VGA-M82-S (VRAM)
Size	Document Number GM3
Rev	2B
Date:	Monday, March 24, 2008
Sheet	24 of 62

QUANTA COMPUTER

DIS:CXCG900U000 / EXC24CG900U

UMA:CXCG240U000 / EXC24CG240U

FM6 use 5.6K

POP FOR UMA
DEPOP FOR DIS

DIS Used 6.8K CS26802JB11
UMA Used 2.2K CS22202JB18

Pop for ATI Graphic

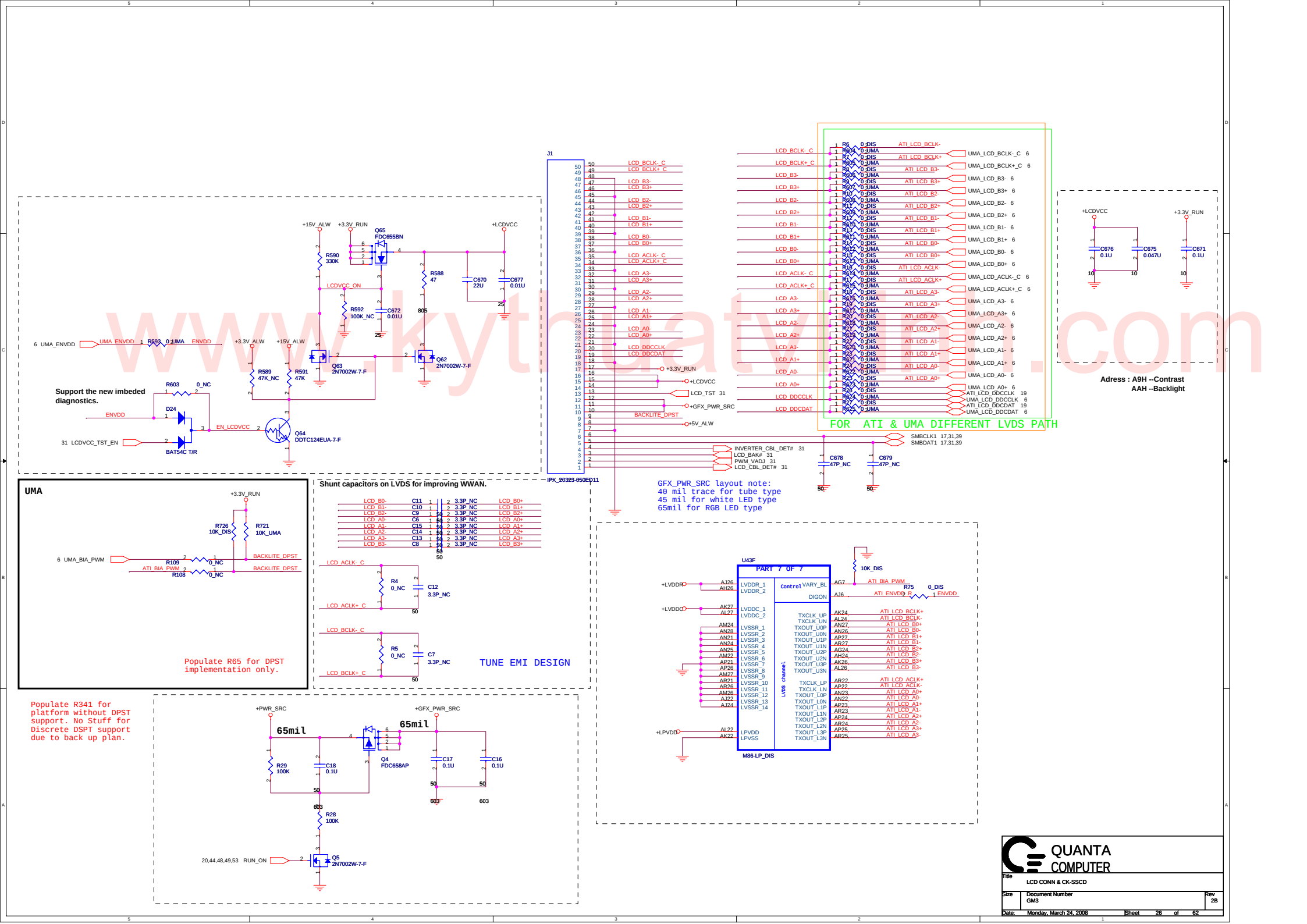
Reserve for EMI and close to HDMI CONN

QUANTA COMPUTER

Title: SII 1362

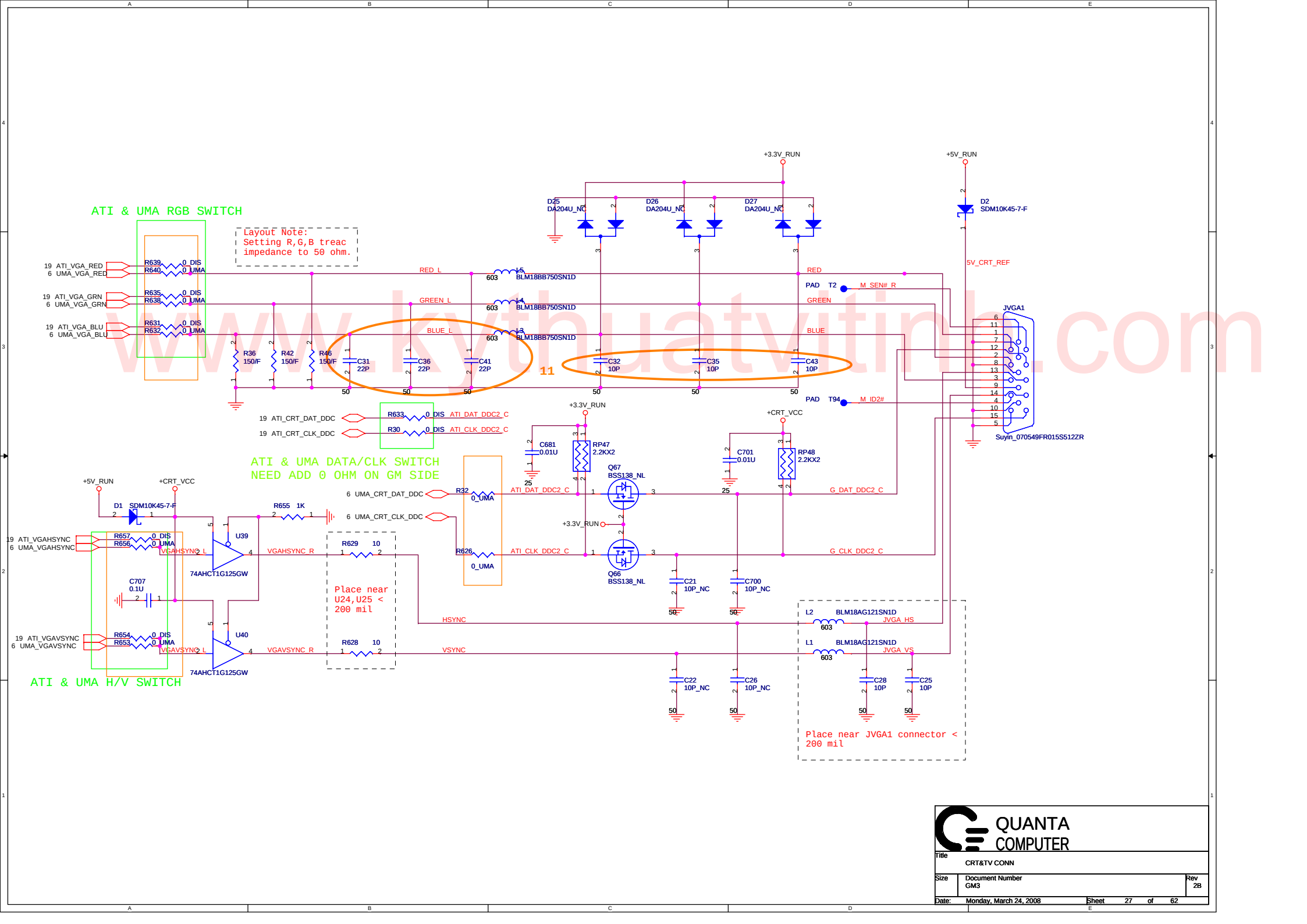
Size: C&D | Document Number | Rev: 2B

Date: Monday, March 24, 2008 | Sheet 25 of 62



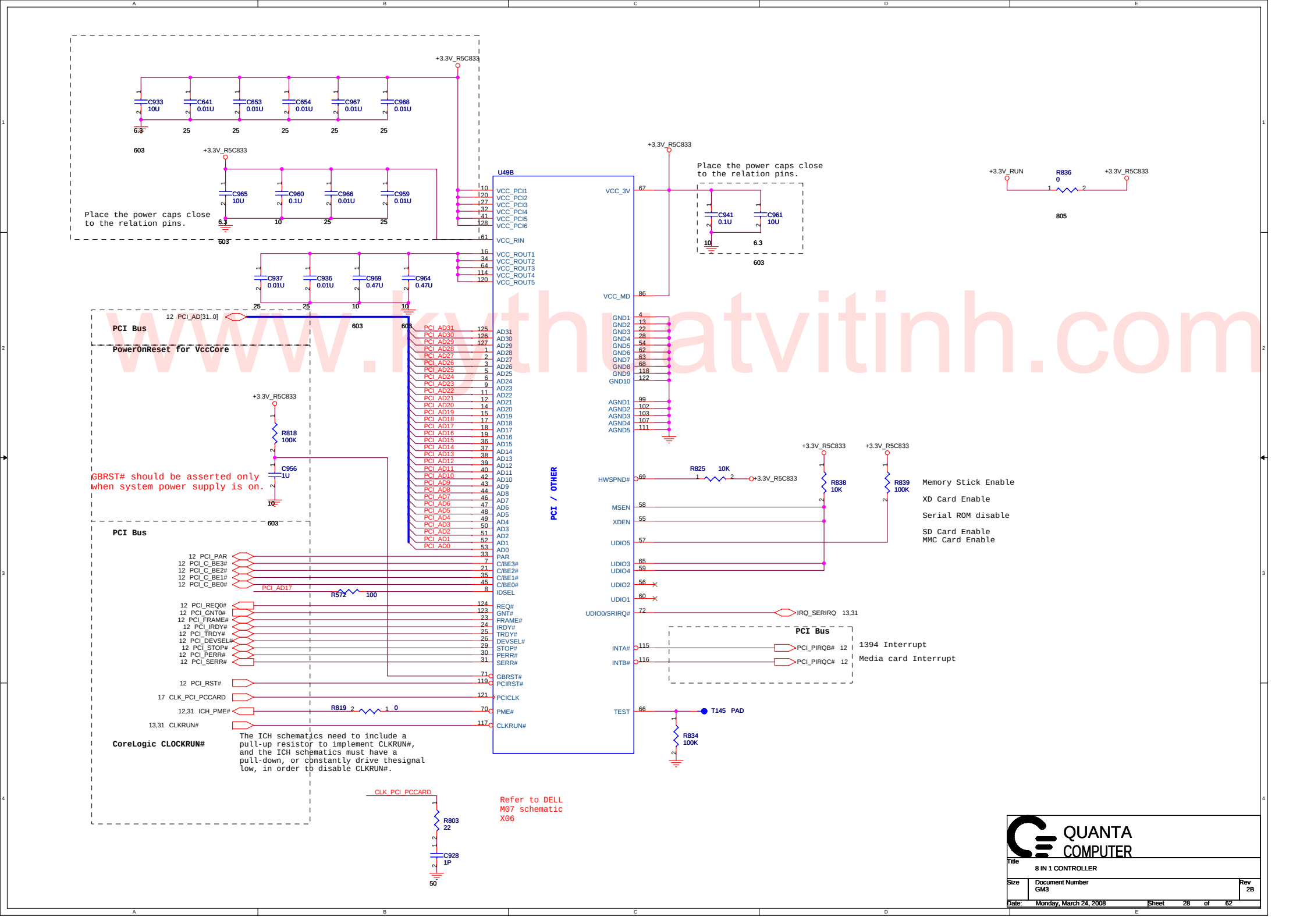
QUANTA COMPUTER

Title	LCD CONN & CK-SSCD	
Size	Document Number GM3	Rev 2B
Date: Monday, March 24, 2008	Sheet 26 of 62	



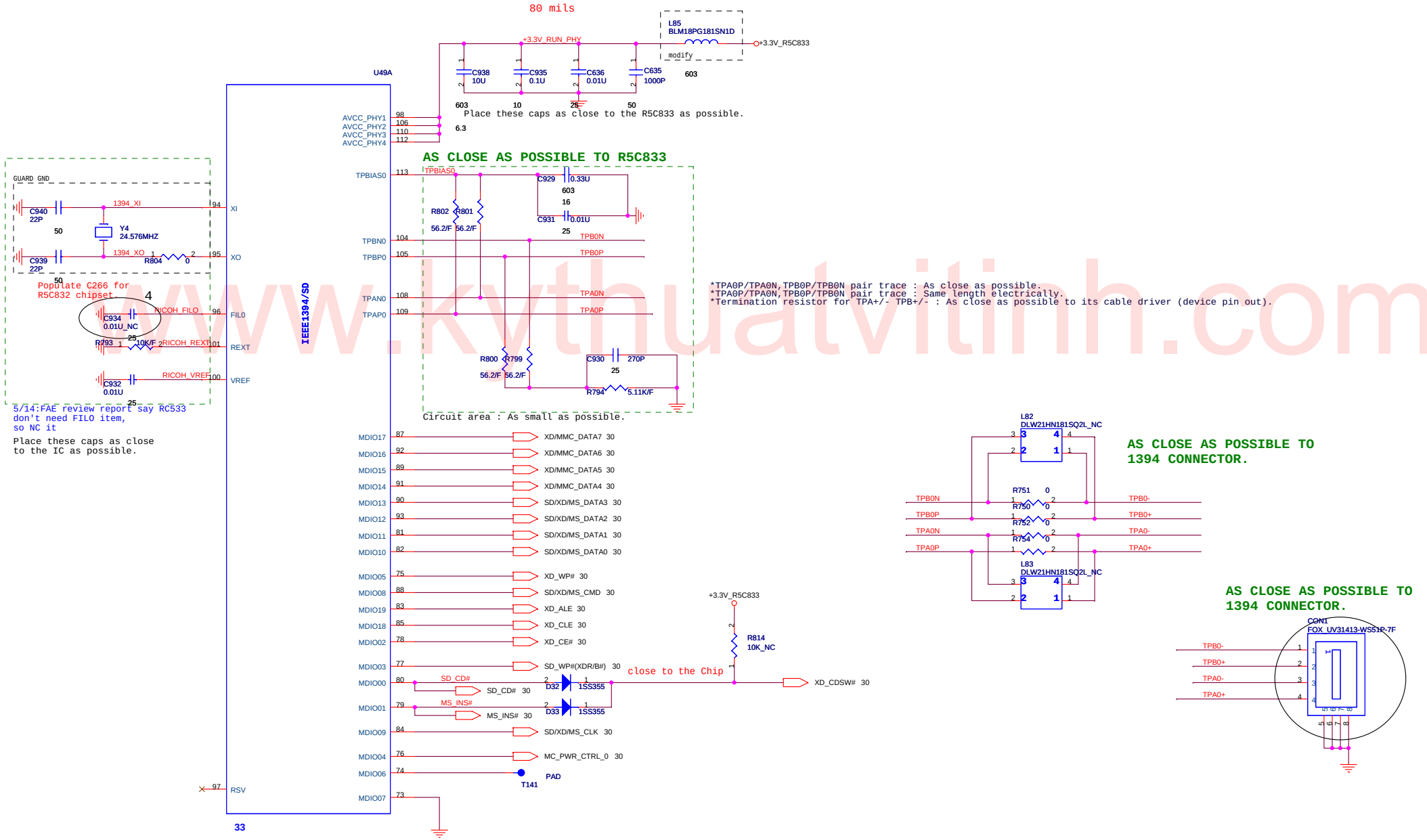
QUANTA COMPUTER

Title	CRT&TV CONN	
Size	Document Number GM3	Rev 2B
Date: Monday, March 24, 2008	Sheet 27 of 62	



QUANTA COMPUTER

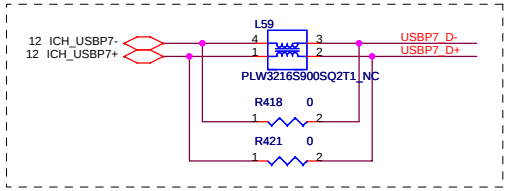
Title	8 IN 1 CONTROLLER	
Size	Document Number GM3	Rev 2B
Date: Monday, March 24, 2008	Sheet 28 of 62	

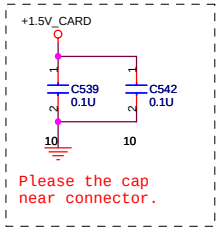


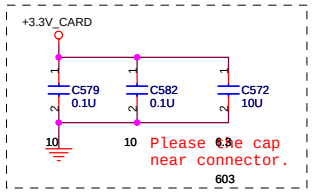
QUANTA COMPUTER			
Title	IEEE 1394		
Size	Document Number GM3		Rev 2B
Date: Monday, March 24, 2008		Sheet 29 of 62	

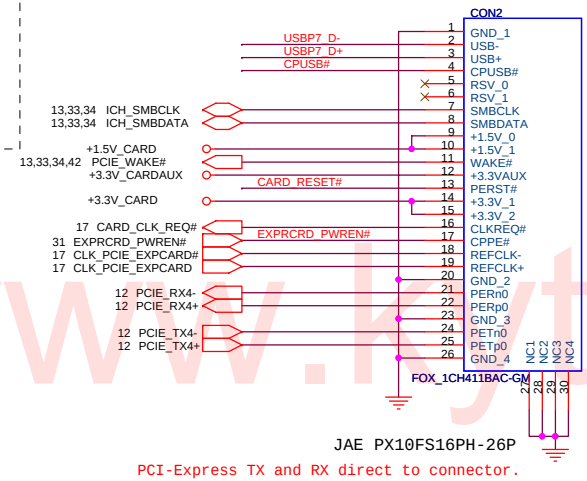
Express Card

+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



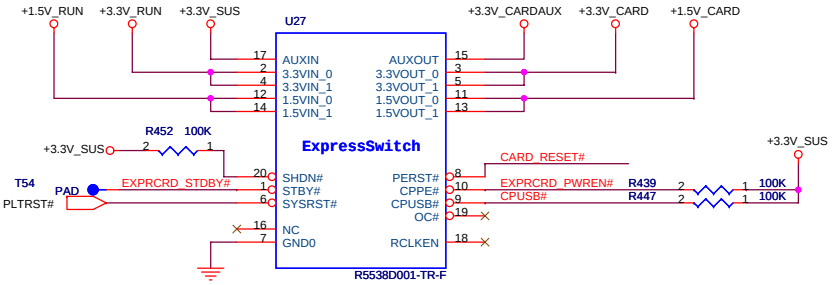


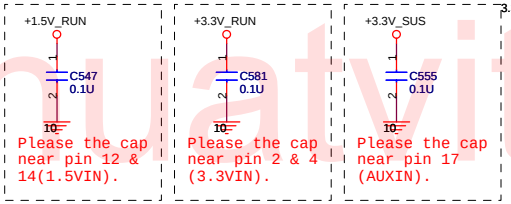


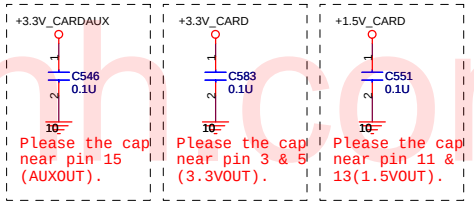


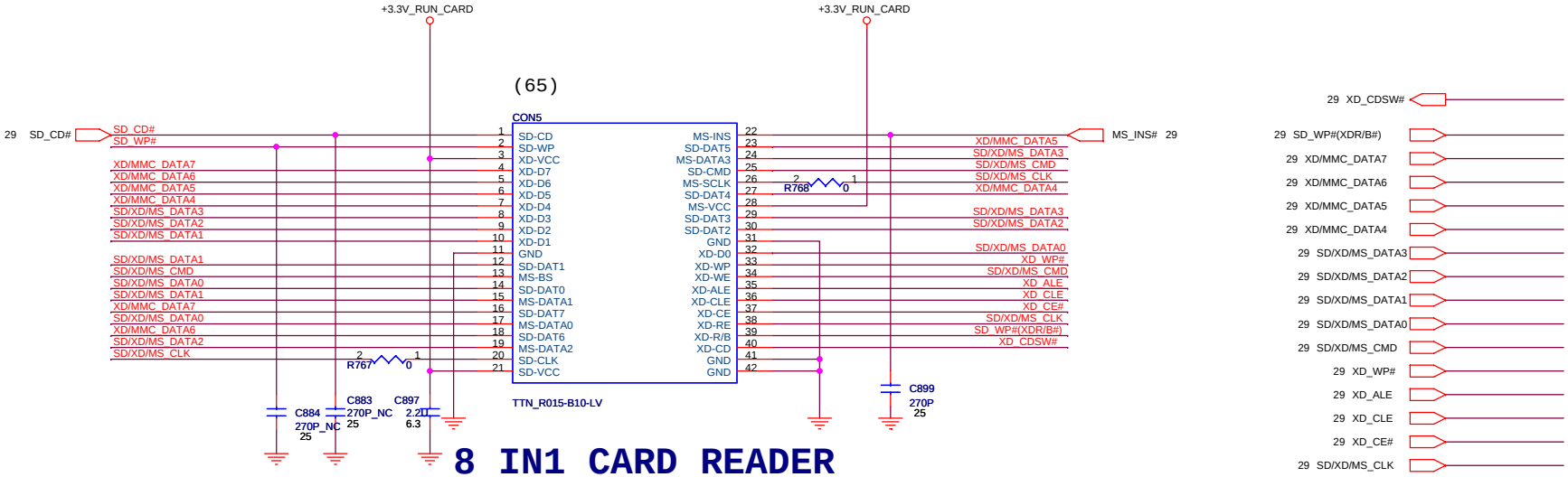
JAE PX10FS16PH-26P

PCI-Express TX and RX direct to connector.

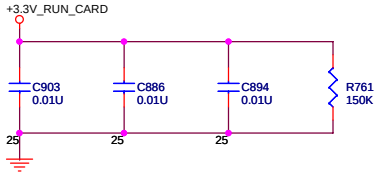


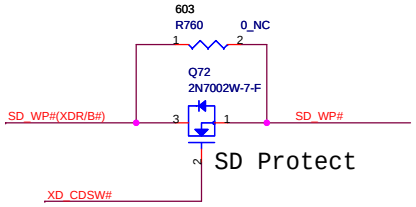


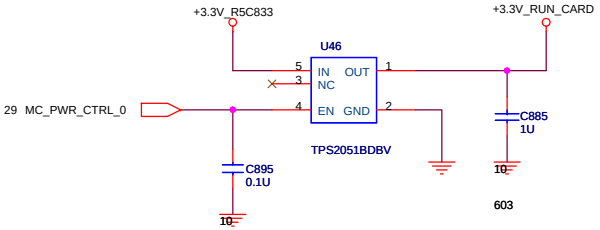




8 IN1 CARD READER

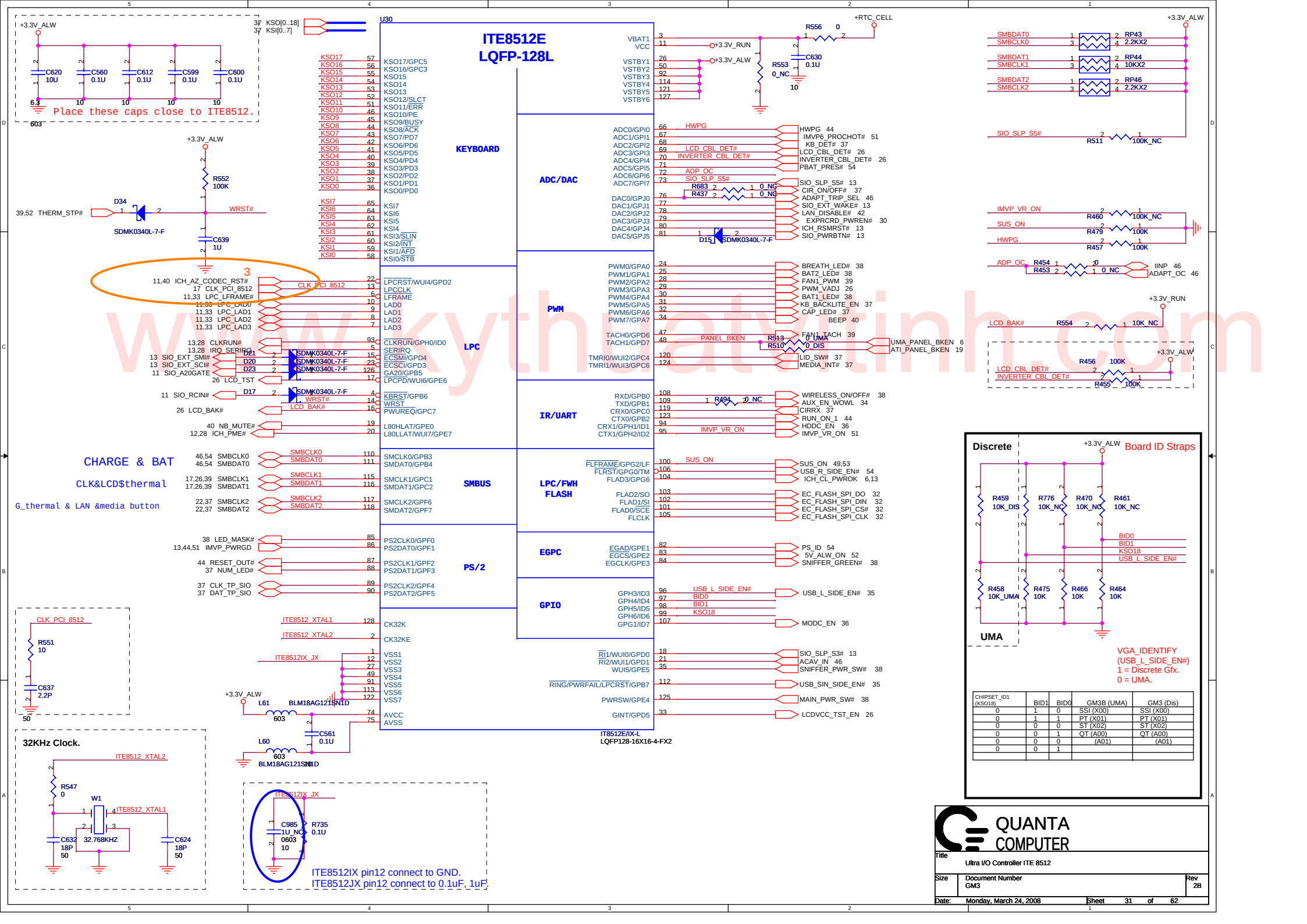






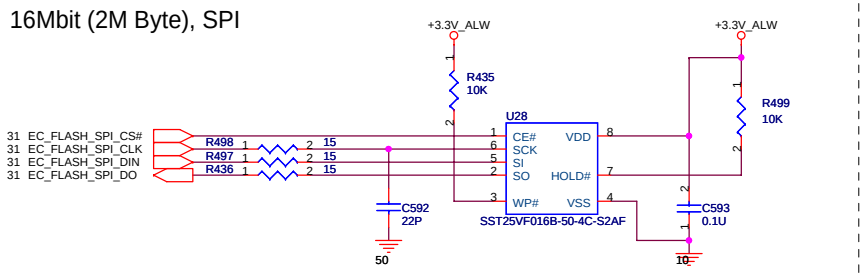
QUANTA COMPUTER

Title	ExpressCard/SmartCard	
Size	Document Number GM3	Rev 2B
Date: Monday, March 24, 2008	Sheet 30 of 62	

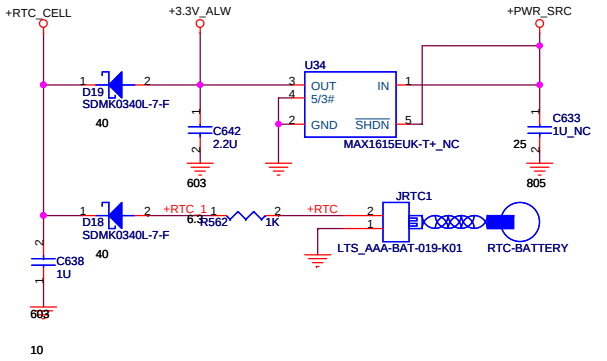


CHIPSET_ID1 (KSO18)	BID1	BID0	GM3B (UMA)	GM3 (Dis)
0	1	0	SSI (X00)	SSI (X00)
0	1	1	PT (X01)	PT (X01)
0	0	0	ST (X02)	ST (X02)
0	0	1	QT (A00)	QT (A00)
0	0	0	(A01)	(A01)
0	0	1		

16Mbit (2M Byte), SPI



RTC BATTERY



QUANTA COMPUTER

Title	Ultra I/O Controller ECE5028	
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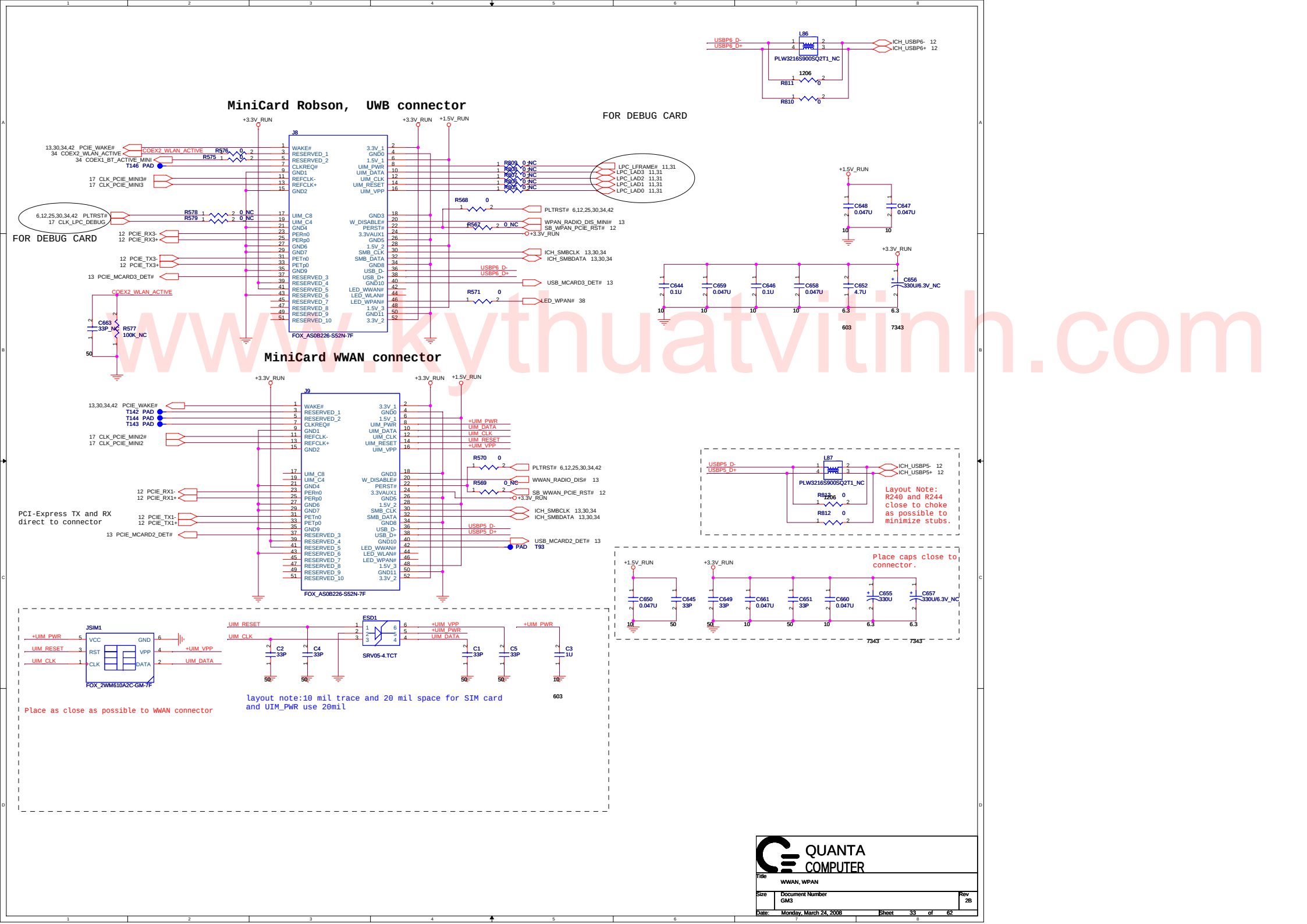
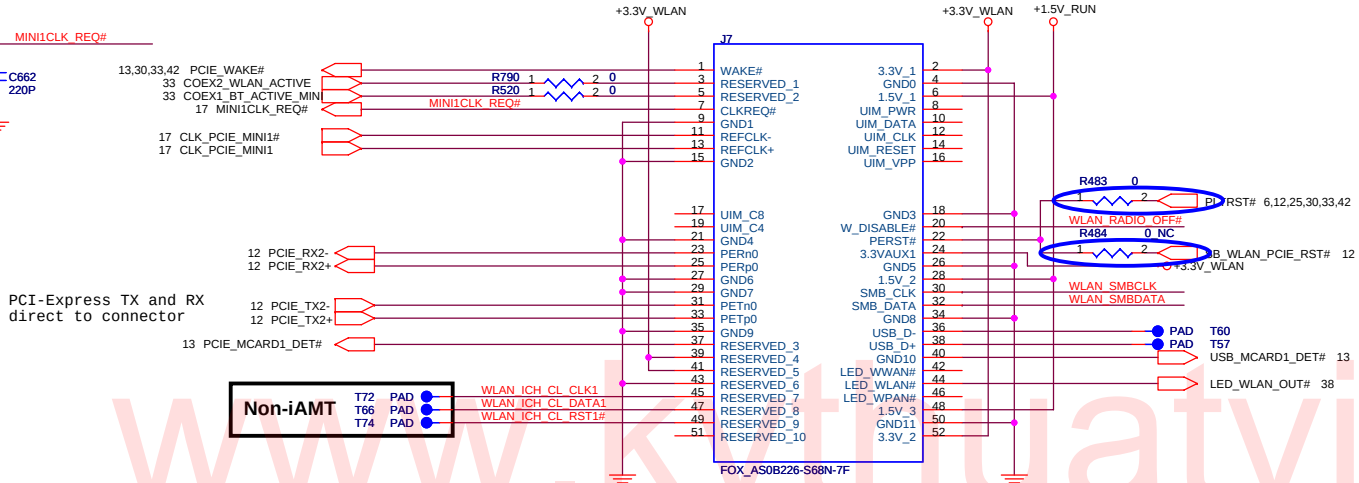
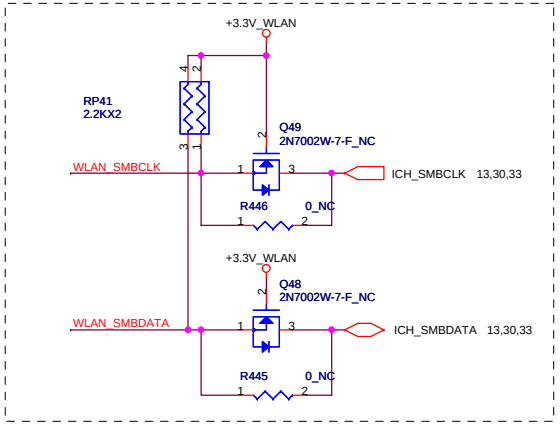
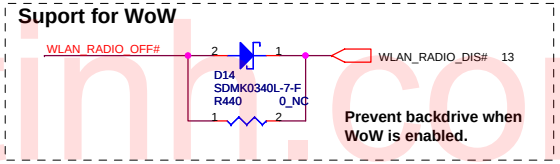
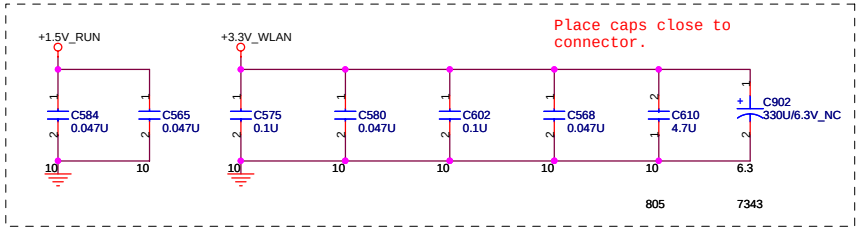


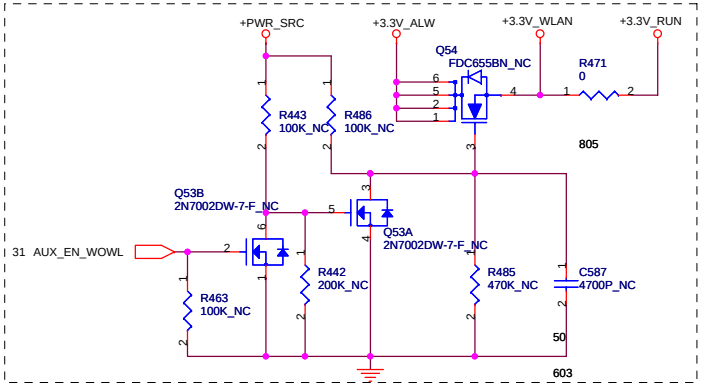
MiniCard WLAN connector











QUANTA COMPUTER

Title	WLAN	
Size	Document Number GM3	Rev 2B
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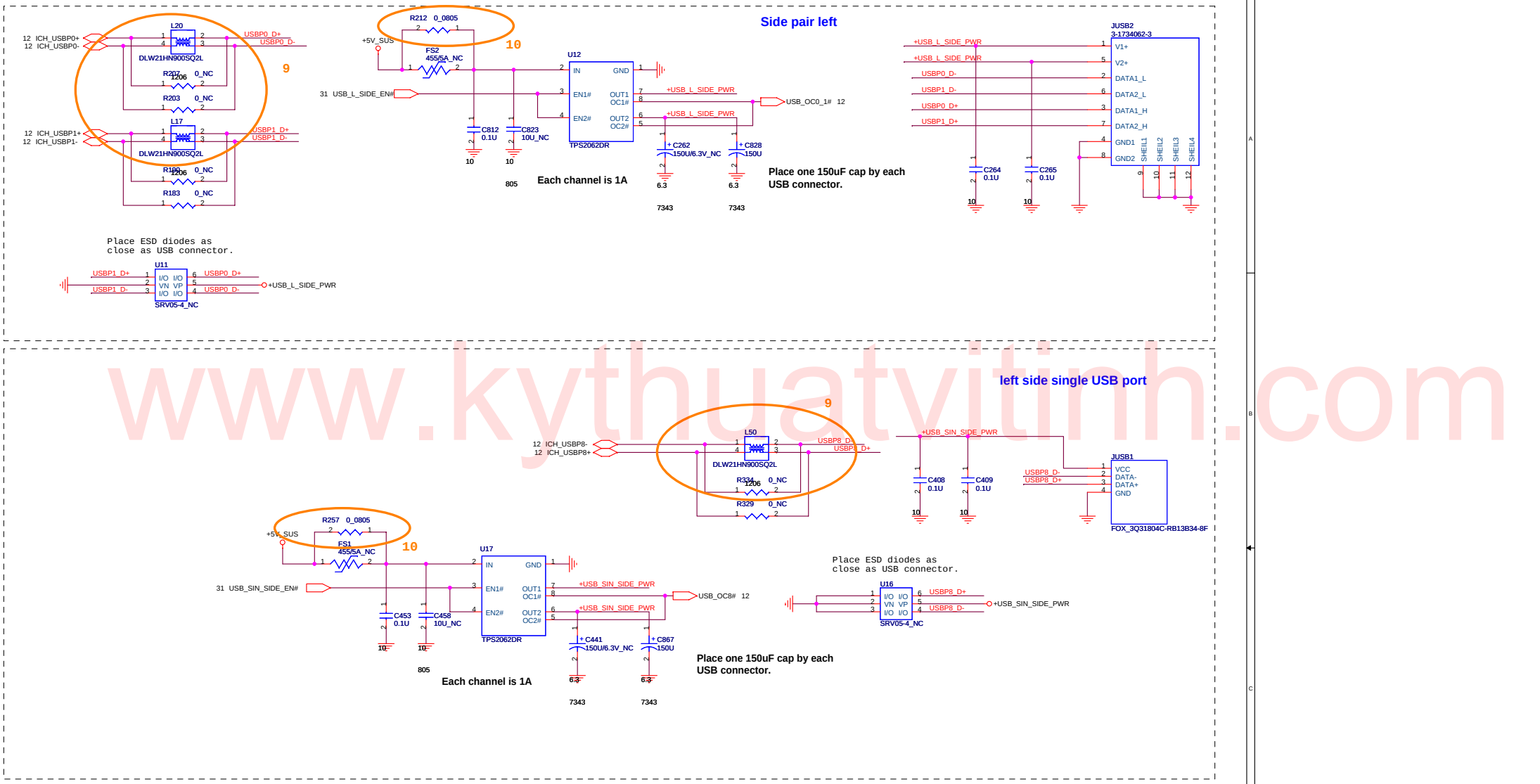

QUANTA COMPUTER

Title	External USB	
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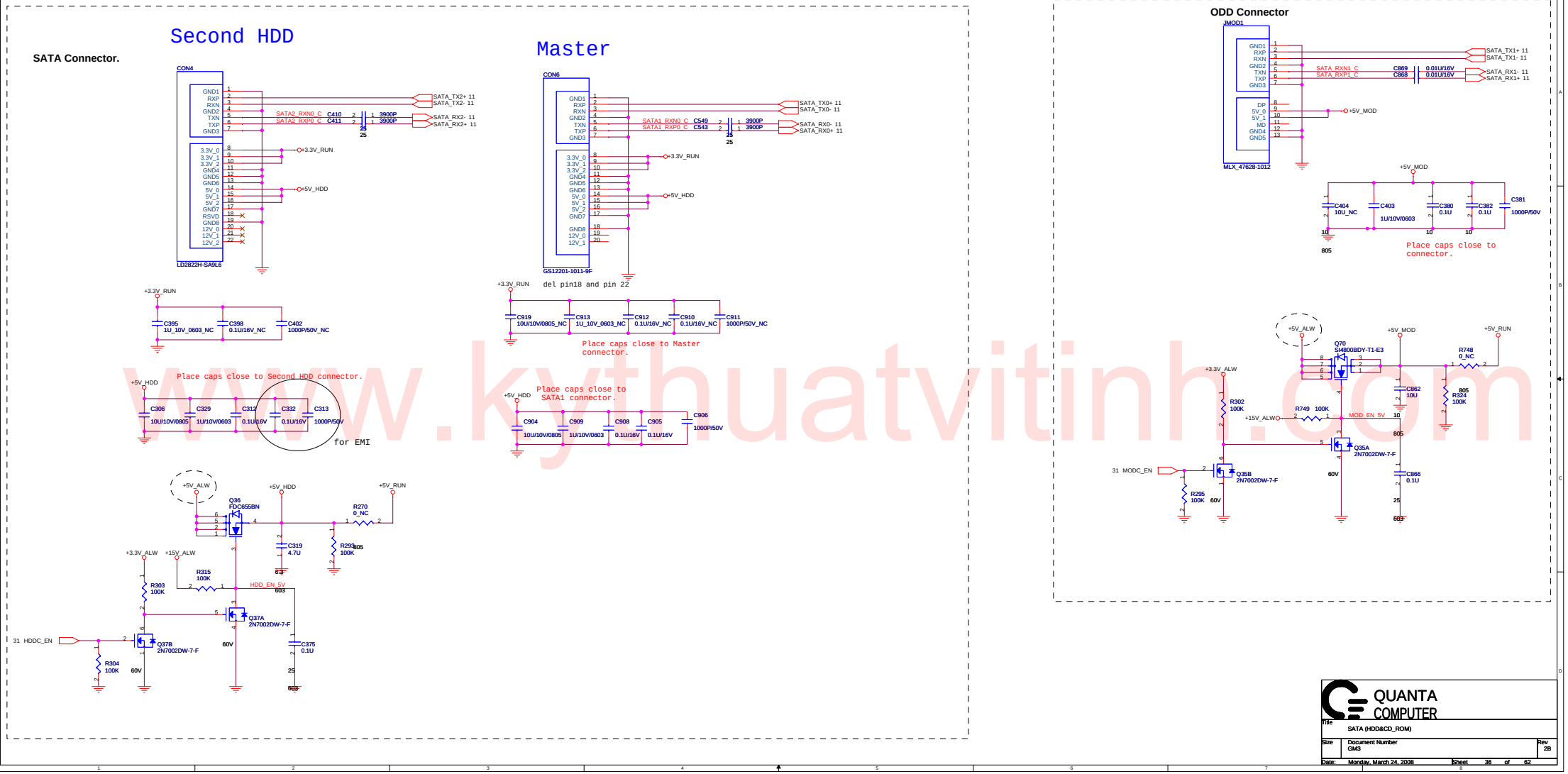
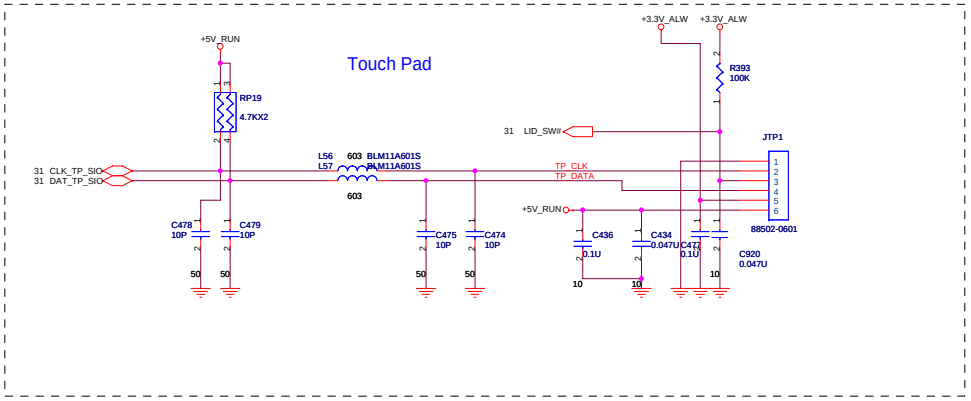
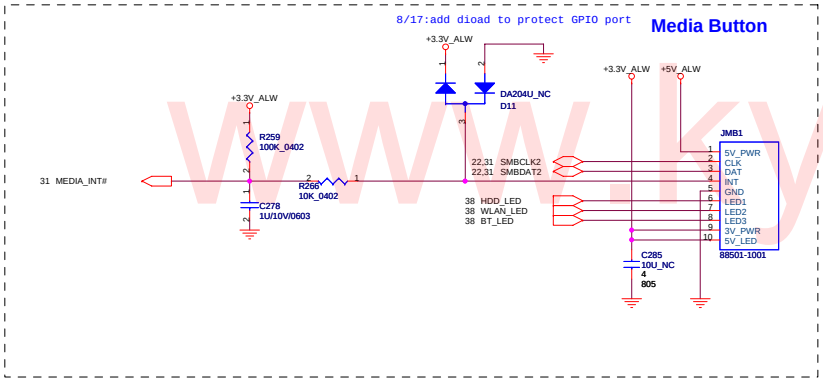
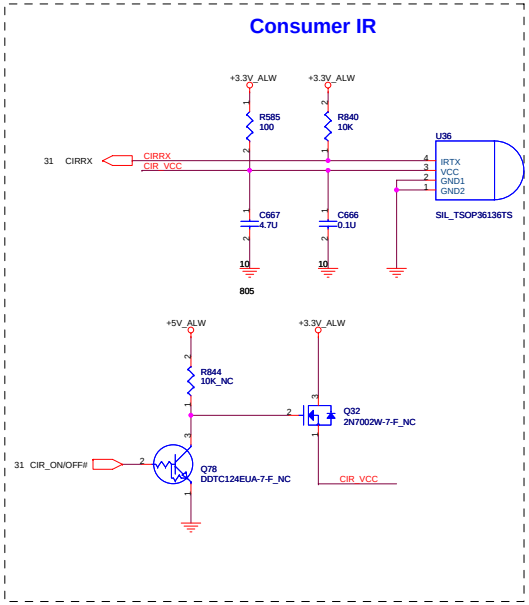
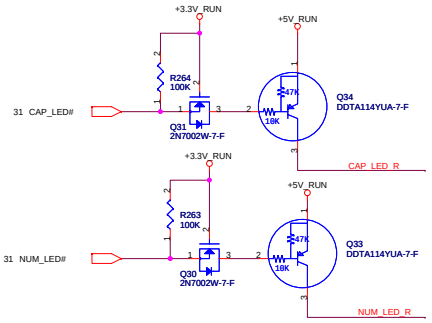
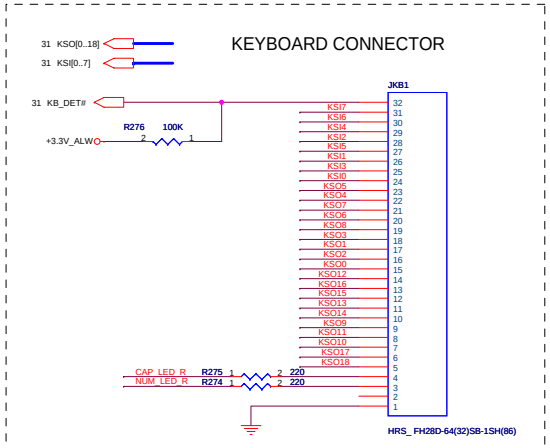


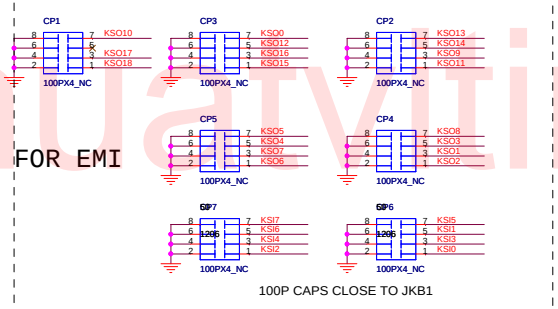




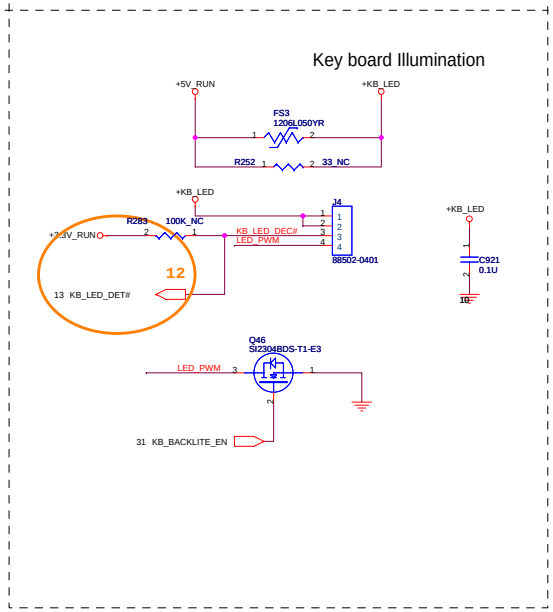








FOR EMI



QUANTA COMPUTER

Title	TOUCH PAD, BULE TOOTH & FIR	
Size	Document Number GM3	Rev 2B
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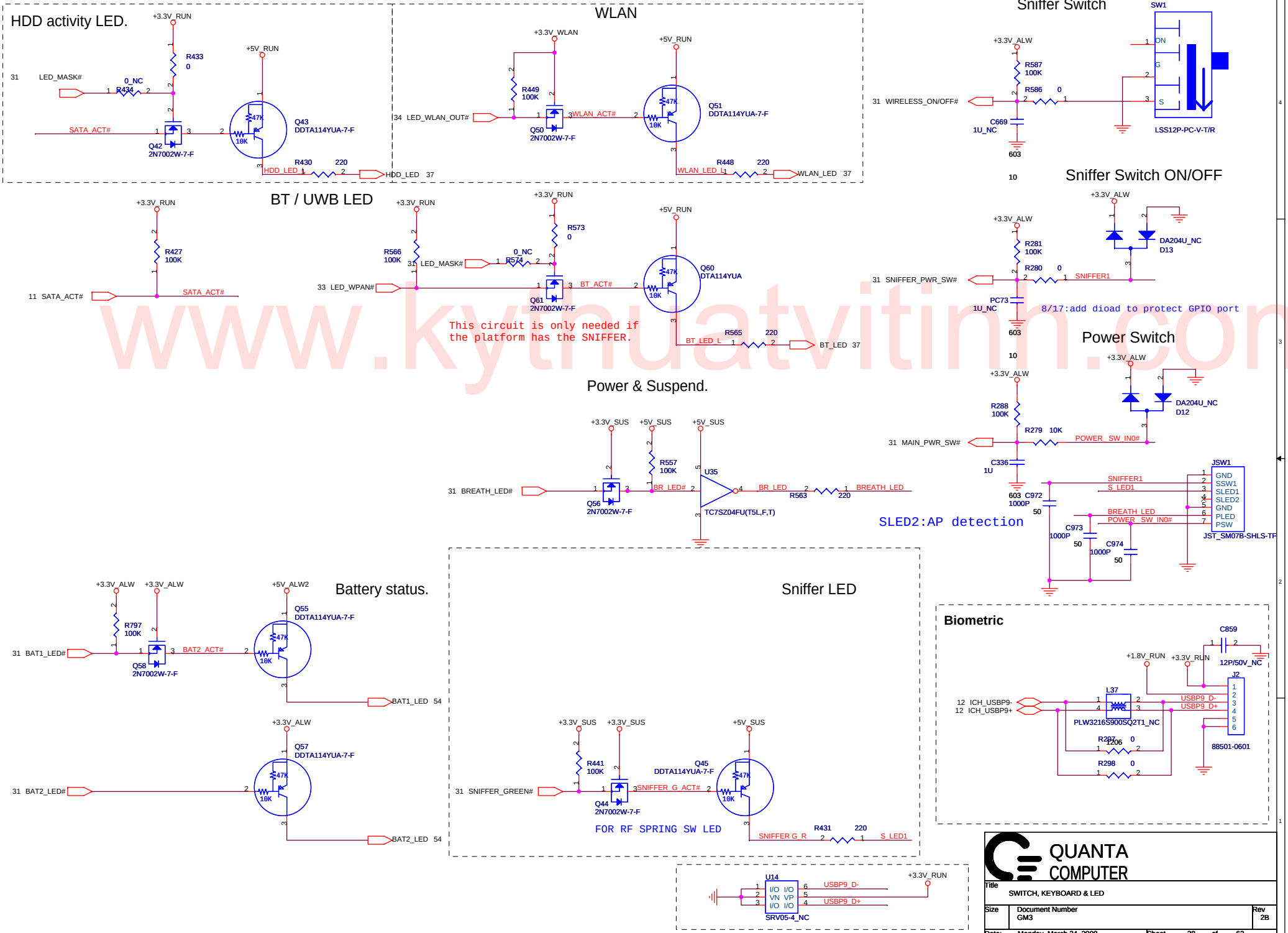

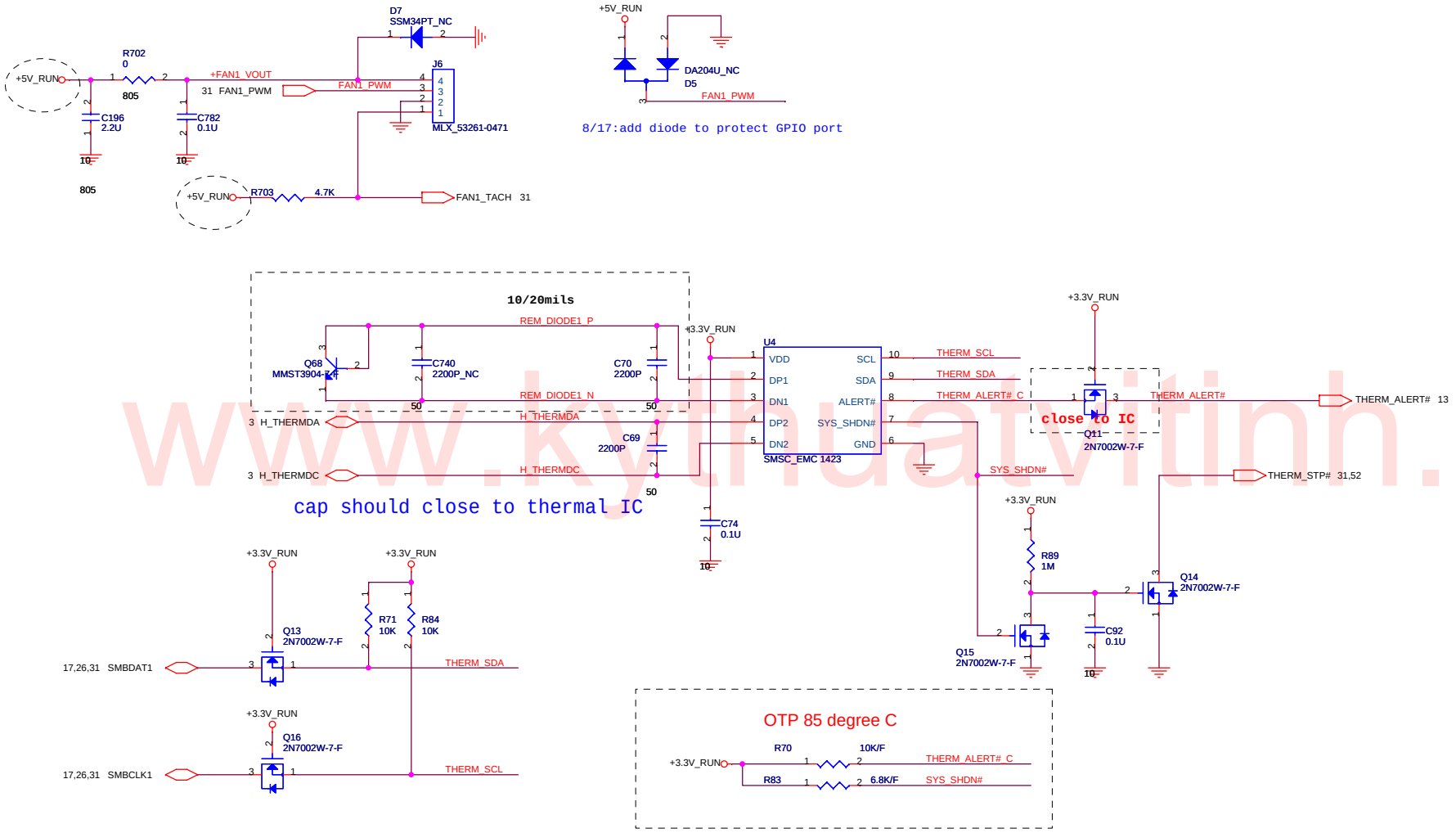

QUANTA COMPUTER

Title	FAN & THERMAL	
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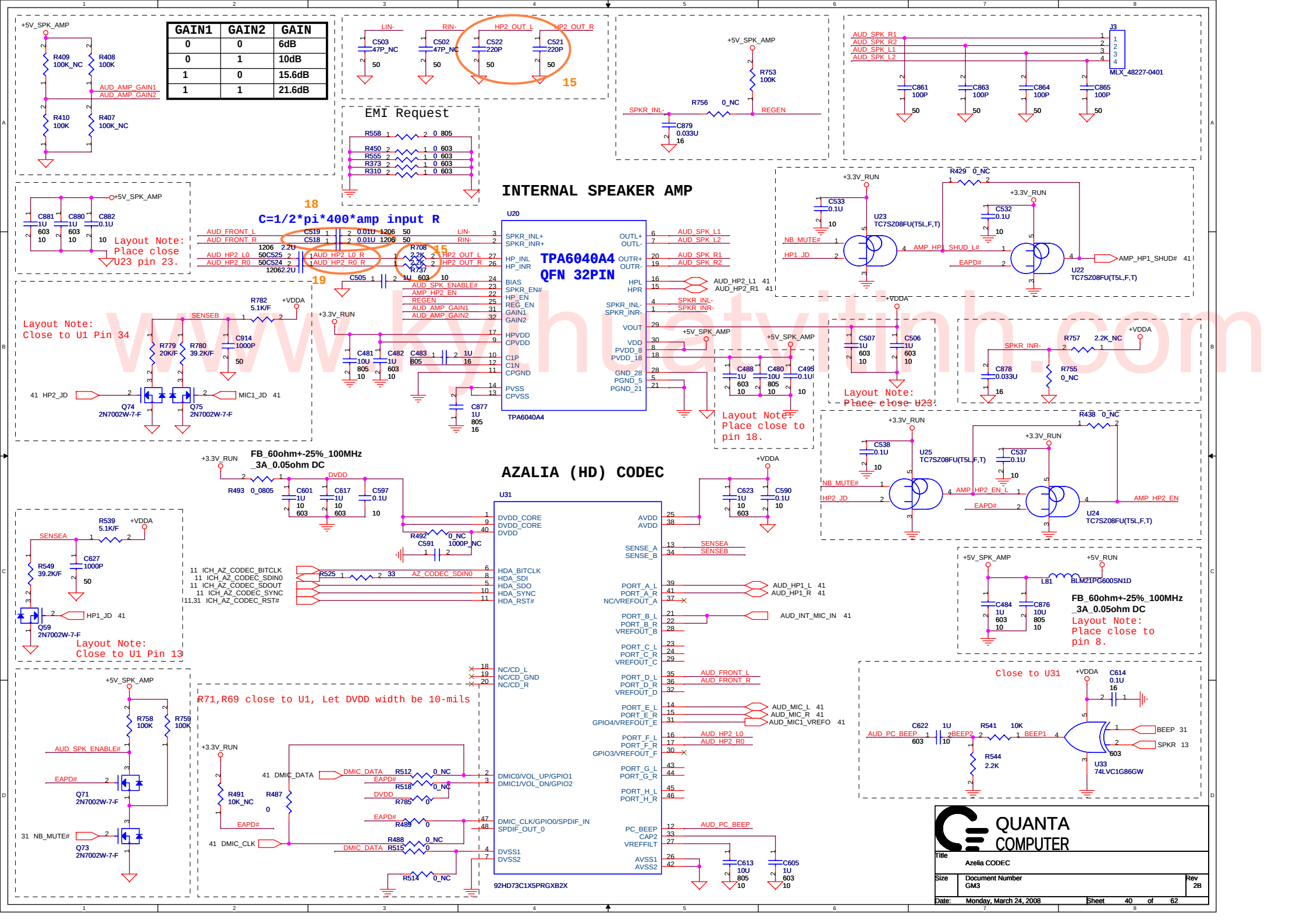

Headphone Jack
Stereo MIC Jack

Array Microphone & Camera

+3.3V_RUN
R289 100K
CAMERA_CBL_DET#

JCAMERA1
USBP4_D+
USBP4_D-
+3.3V_CCD
40 DMIC_DATA — L36 22 ohm — 603 DMIC_DATA_R
40 DMIC_CLK — L35 — 603 DMIC_CLK_R
13 CAMERA_CBL_DET# — CAMERA_CBL_DET#
I-pex 20374-010E-1

DMIC_DATA
C358 33P_NC 50

+3.3V_CCD trace width
use 25 mils

+3.3V_RUN — L41 BLM18AG121SN1D 603 — +3.3V_CCD
C373 10U 805 10
C364 10U 805 10
DMIC_CLK
C357 33P_NC 50

12 ICH_USBP4-
12 ICH_USBP4+
L46 PLW3216S900SQ2T1_NC
USBP4_D-
USBP4_D+
R312 1206 0
R313 0

JACK 2 (MIC)
JACK 1
(HP2)
JACK 3 (HP)

JAUDIO1
40 AUD_MIC1_VREFO
40 AUD_MIC_L
40 AUD_MIC_R
40 AUD_HP2_L1
40 AUD_HP2_R1
AUD_HP1_L1
AUD_HP1_R1
40 MIC1_JD
40 HP2_JD
40 HP1_JD
MIC1_JD
HP2_JD
HP1_JD
48227-1501

R419
MIC1_JD
100K R414
+3.3V_RUN
HP2_JD
100K R412
HP1_JD
100K

+VDDA
R584 100K
U51A LM358ADR2G
C665 2.2U 805 10
R835 100K
R826 0
JP11 HS8102E
INT_MIC_C_L+
C664 2.2U 805 10
R581 1K
R580 1K
INT_MIC_2_L+
INT_MIC_2_L-
C962 0.1U 603 16
C963 0.1U 603 16
INT_MIC_L1+
INT_MIC_L1-
R832 10K
R833 10K
INT_MIC_L0+
INT_MIC_L0-
U51B LM358ADR2G
INT_MIC_IN_OP
C970 0.1U 603 16
AUD_INT_MIC_IN 40
+VDDA
C971 0.1U 10
R583 1K
R582 1K
INT_MIC_C_L-
C668 2.2U 805 10
D22 SM05_NC
R837 100K

Layout Note:
Place close to CODEC.

15
40 AUD_HP1_L — C567 1206 2.2UF 50V — AUD_HP1_L2
40 AUD_HP1_R — C586 1206 2.2UF 50V — AUD_HP1_R2
R738 2.2K
R739 2.2K
AUD_HP1_L0
AUD_HP1_R0
40 AMP_HP1_SHUD#
C578 1206 2.2U 25
U29
INL
INR
SHDNR
SHDNL
C1P
C1N
PVSS
SVSS
OUTL
OUTR
NC1
NC2
NC3
NC4
NC5
NC6
SVDD
PVDD
PGND
SGND
MAX4411ETP
AUD_HP1_L1
AUD_HP1_R1
+3.3V_RUN
C557 1U 805 16
C556 2.2U 1206 10
AUD_HP1_L0
AUD_HP1_R0
C986 220P 50
C987 220P 50
15

QUANTA COMPUTER

Title	AUDIO CONN	
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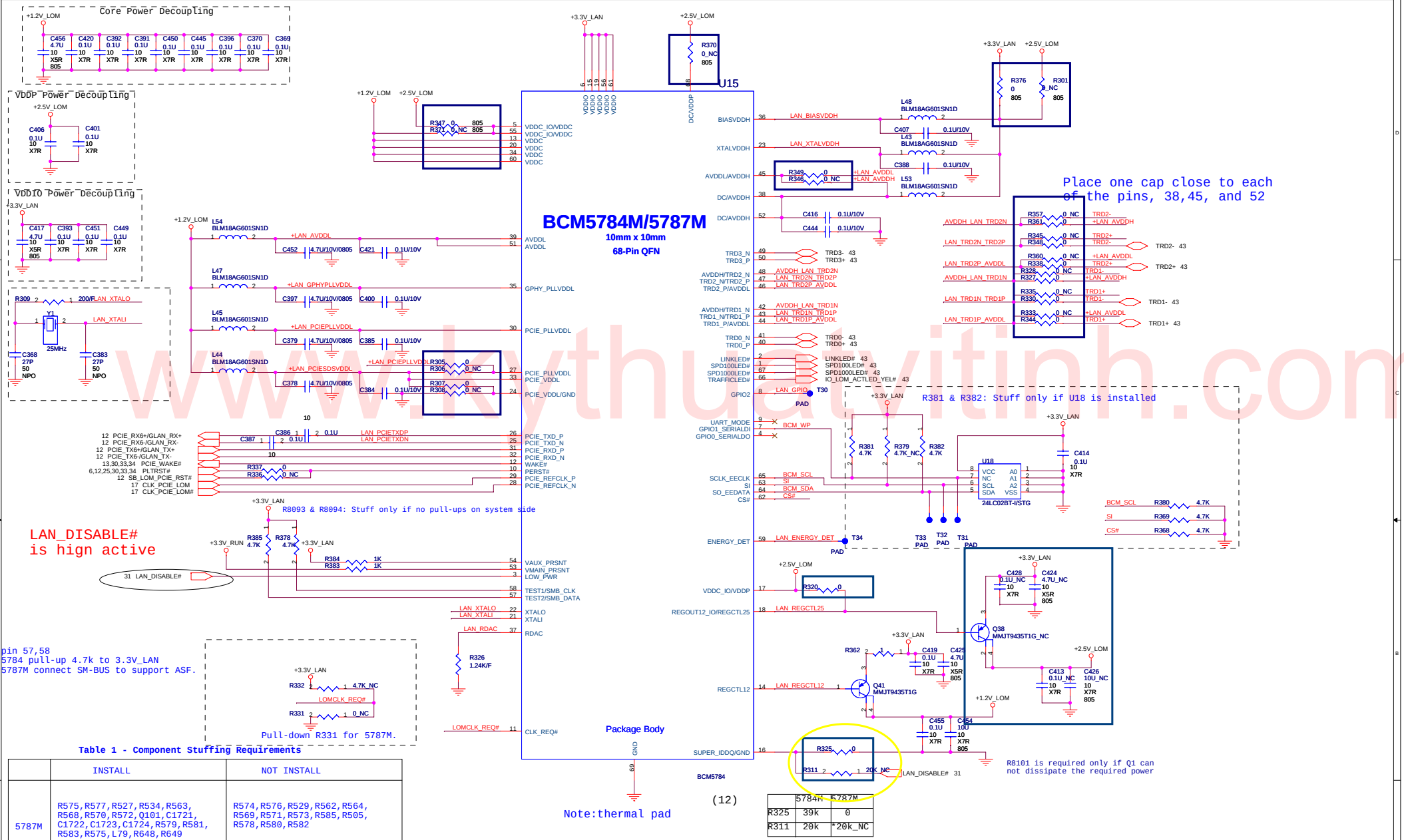
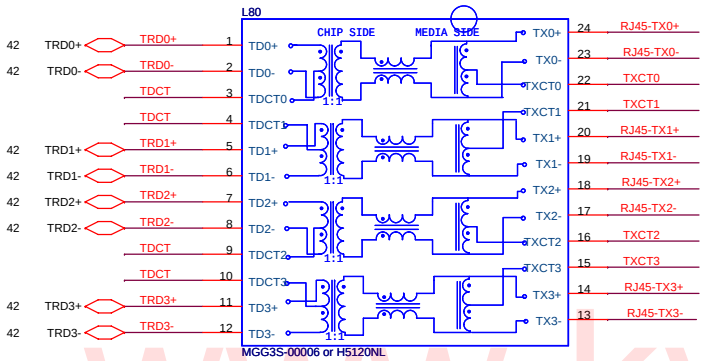


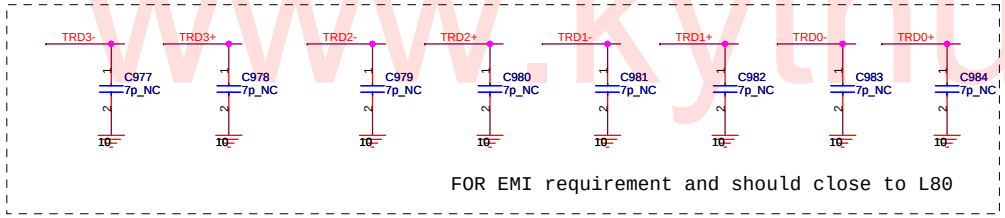
Table 1 - Component Stuffing Requirements

	INSTALL	NOT INSTALL
5787M	R575,R577,R527,R534,R563, R568,R570,R572,Q101,C1721, C1722,C1723,C1724,R579,R581, R583,R575,L79,R648,R649	R574,R576,R529,R562,R564, R569,R571,R573,R585,R505, R578,R580,R582
5784	R574,R576,R529,R562,R564, R569,R571,R573,R585,R505, R578,R580,R582	R575,R577,R527,R534,R563, R568,R570,R572,Q101,C1721, C1722,C1723,C1724,R579,R581, R583,R575,L79,R648,R649

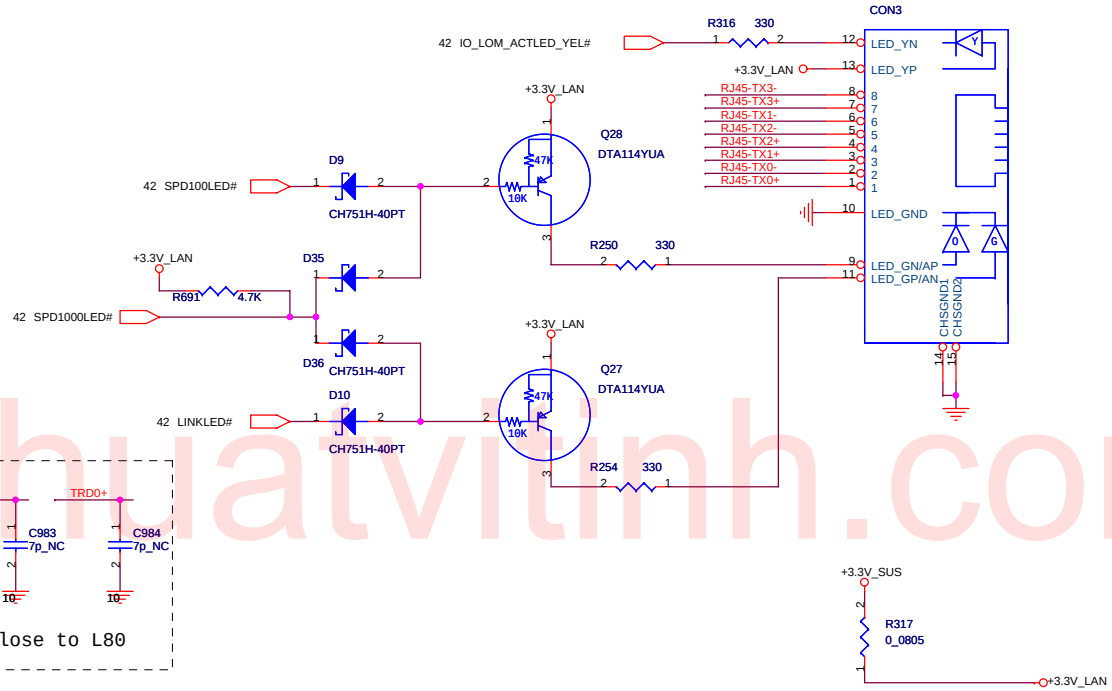
	5784M	5787M
R325	39k	0
R311	20k	*20k_NC

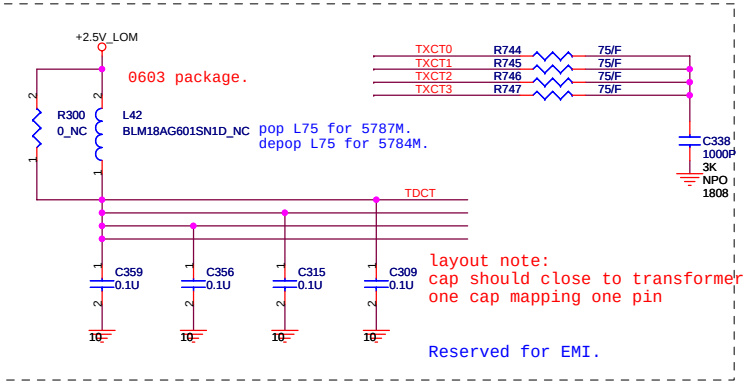
TRANSFORM

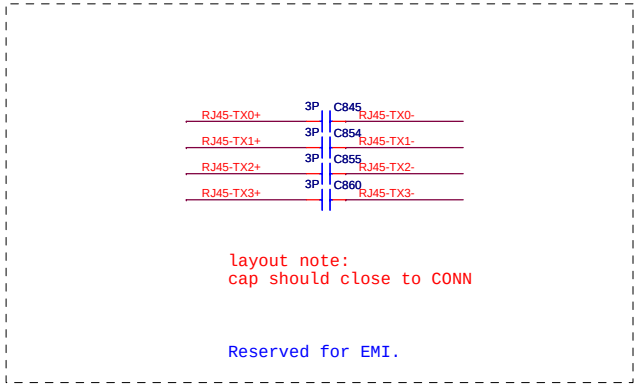




RJ-45 Connector







QUANTA COMPUTER

Title	LAN SWITCH	
Size	Document Number GM3	Rev 2B
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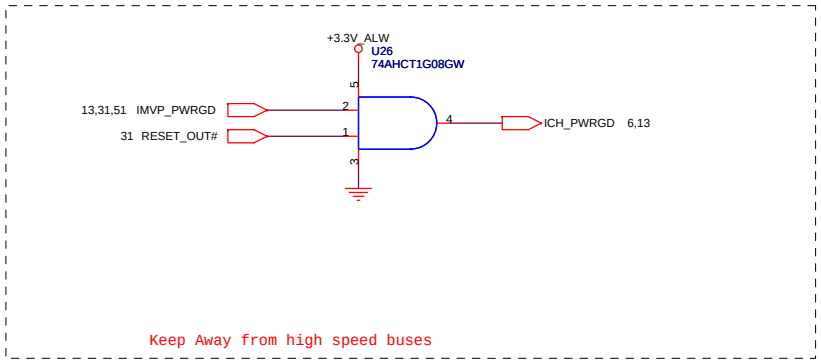

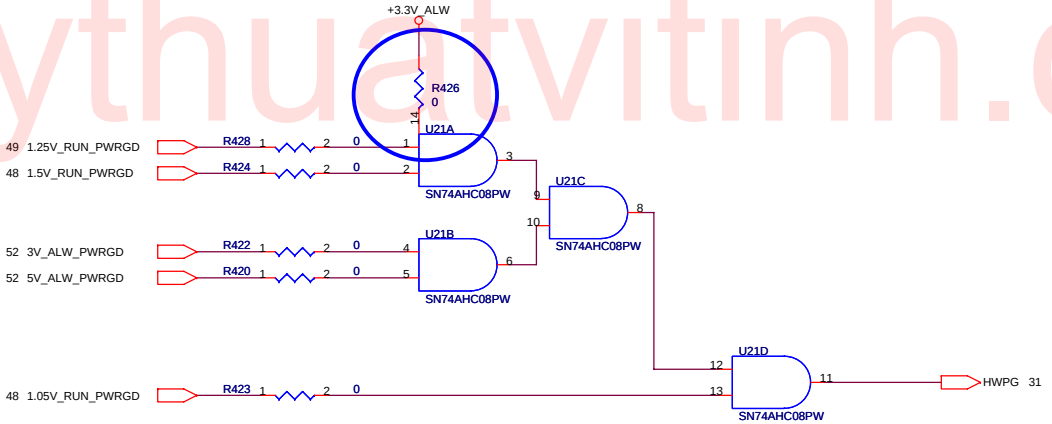

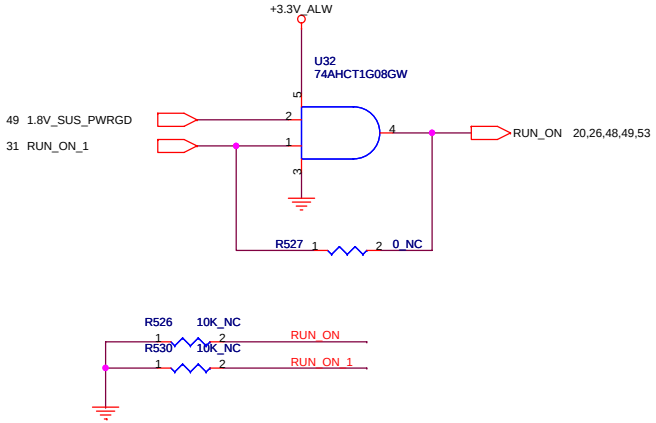

QUANTA COMPUTER

Title	System Reset Circuit	
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TH1
H-C394D126P2

TH2
H-TC276BC236D126P2

TH3
H-TC276BC236D126P2

TH4
H-TC394BC315D126P2

TH5
H-TC394BC315D126P2

TH6
H-C256D130P2

TH7
H-TC276BC354D126P2

TH8
H-TC394BC276D126P2

TH9
h-c315d189p2

TH10
H-C315D157I197P2

TH11
H-C315D157I197P2

TH12
H-C315D126P2

TH13
H-C256D126P2

TH14
H-C433D433N

TH15
H-C276D126P2

TH16
H-TC394BC236D126P2

TH17
H-C315D157I197P2

TH18
H-C315D157I197P2

TH19
H-TC276BC236D110P2

TH20
H-C315D157I197P2

TH23
H-TC197BC236D65P2

TH24
H-TC197BC236D65P2

TH25
H-TC197BC236D104P2

TH26
H-TC197BC236D65P2

TH27
H-TC197BC236D104P2

TH28
H-TC197BC236D65P2

TH29
H-TC275BC492D110P2

TH30
H-TC394BC315D126P2

TH31
h-tr8x9bc276d126p2

TH33
H-C118D118N

TH34
h-c236d110p2

TH35
h-c236d110p2

TH32
h-o71x118d31x78p2

TH36
h-o71x118d31x78p2

QUANTA COMPUTER

Title	Battery Selector	
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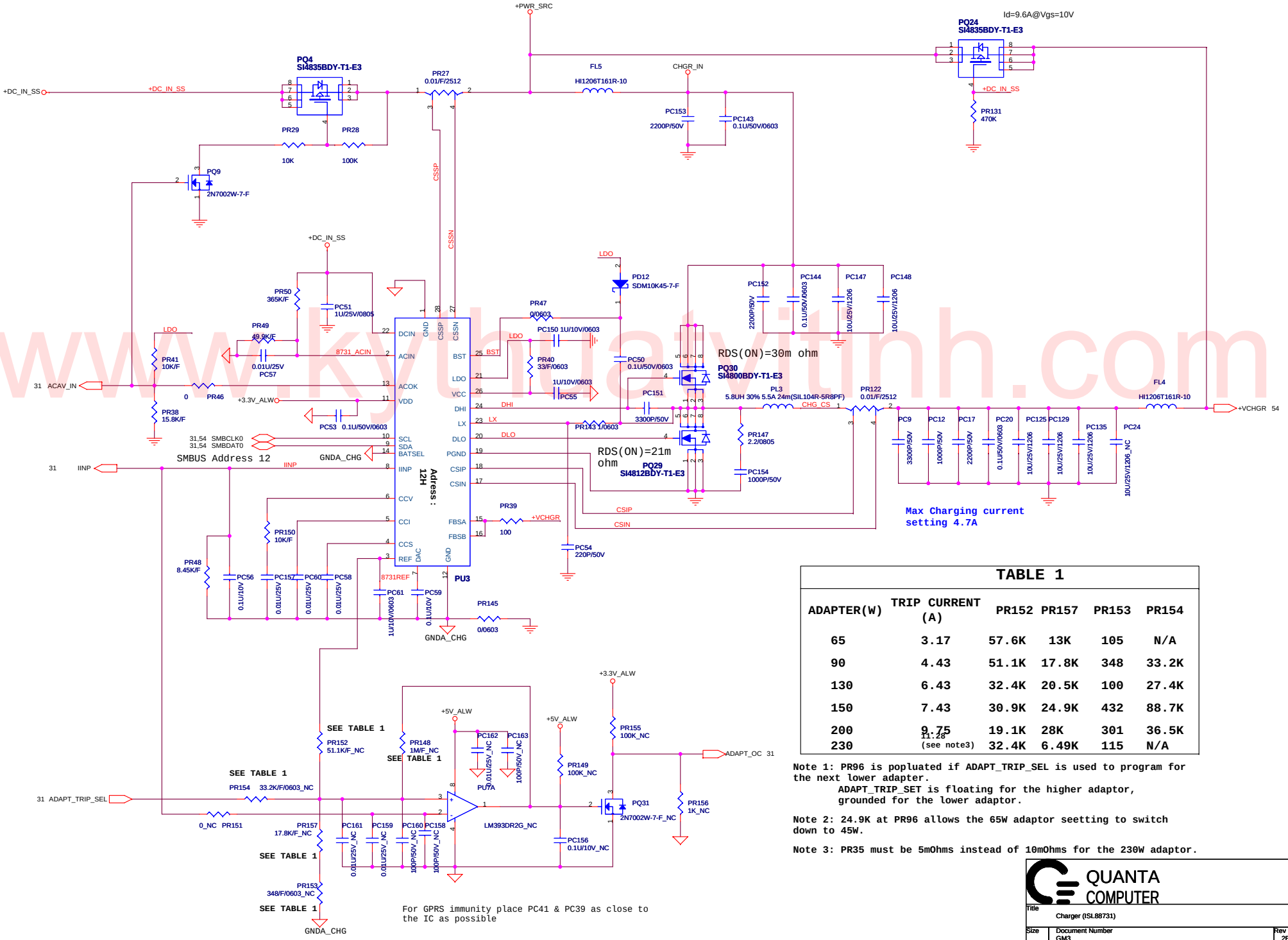

TABLE 1					
ADAPTER(W)	TRIP CURRENT (A)	PR152	PR157	PR153	PR154
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28 (see note3)	32.4K	6.49K	115	N/A

Note 1: PR96 is popluated if ADAPT_TRIP_SEL is used to program for the next lower adapter.
ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

Note 2: 24.9K at PR96 allows the 65W adaptor seetting to switch down to 45W.

Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.

QUANTA COMPUTER

Title	Charger (ISL88731)	
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QUANTA COMPUTER

Title		
Size	Document Number GM3	Rev 2B
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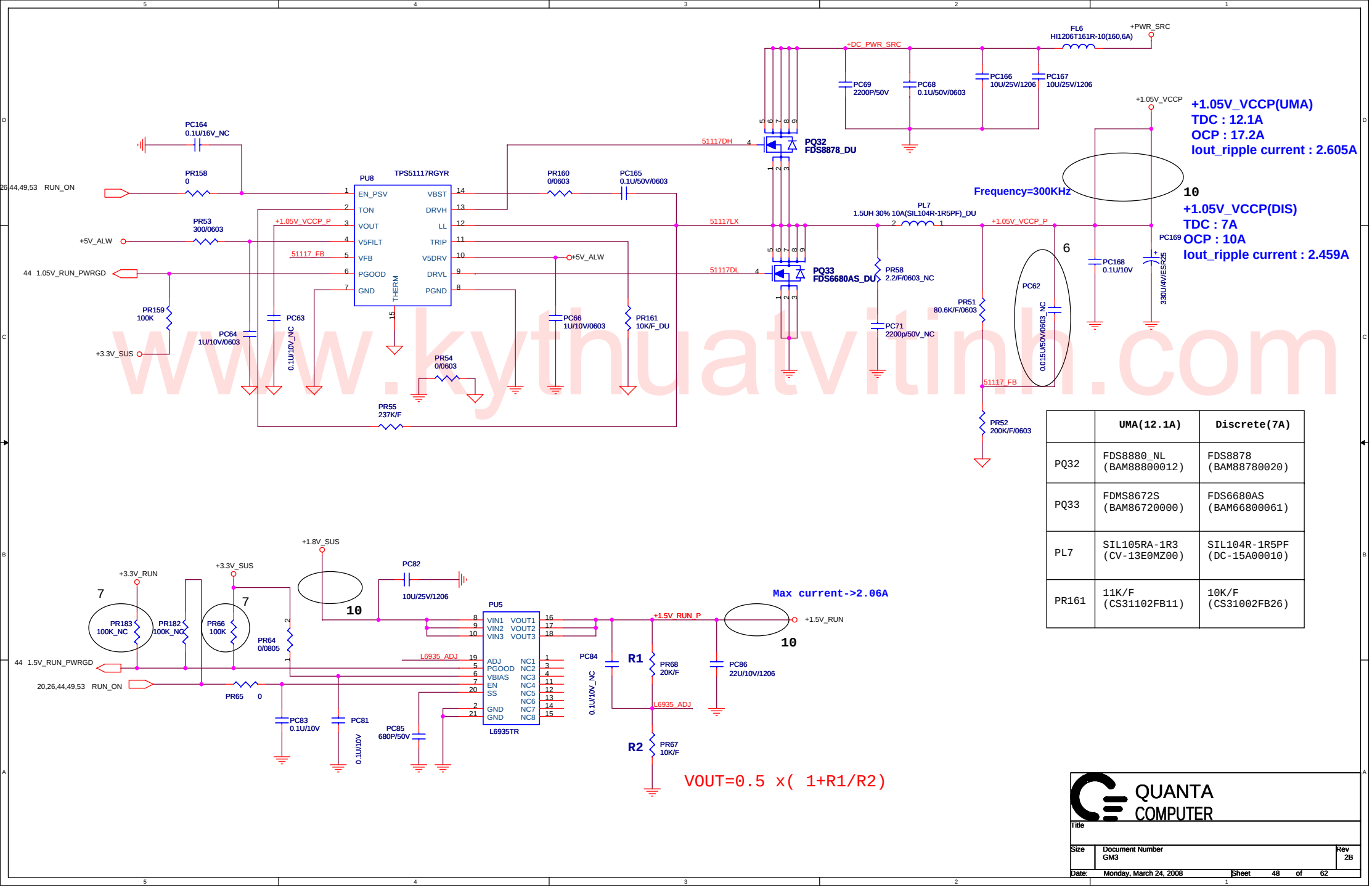

	UMA(12.1A)	Discrete(7A)
PQ32	FDS8880_NL (BAM88800012)	FDS8878 (BAM88780020)
PQ33	FDMS8672S (BAM86720000)	FDS6680AS (BAM66800061)
PL7	SIL105RA-1R3 (CV-13E0MZ00)	SIL104R-1R5PF (DC-15A00010)
PR161	11K/F (CS31102FB11)	10K/F (CS31002FB26)

QUANTA COMPUTER

Title

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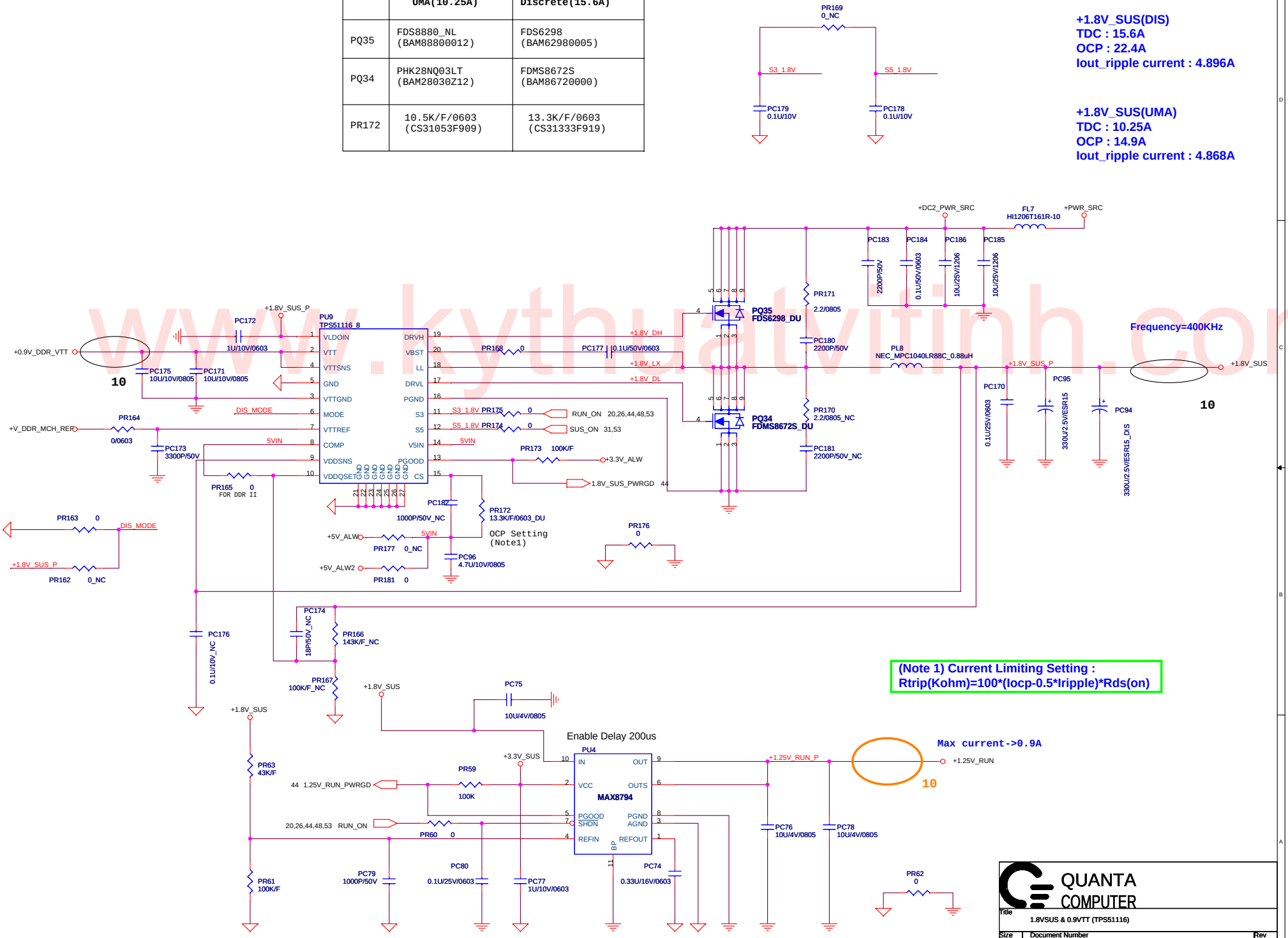
	UMA(10.25A)	Discrete(15.6A)
PQ35	FDS8880_NL (BAM88800012)	FDS6298 (BAM62980005)
PQ34	PHK28NQ03LT (BAM28030Z12)	FDMS8672S (BAM86720000)
PR172	10.5K/F/0603 (CS31053F909)	13.3K/F/0603 (CS31333F919)

+1.8V_SUS(DIS)
TDC : 15.6A
OCP : 22.4A
Iout_ripple current : 4.896A

+1.8V_SUS(UMA)
TDC : 10.25A
OCP : 14.9A
Iout_ripple current : 4.868A



QUANTA COMPUTER

Title	1.8VSUS & 0.9VTT (TPS51116)	
Size	Document Number GM3	Rev 2B
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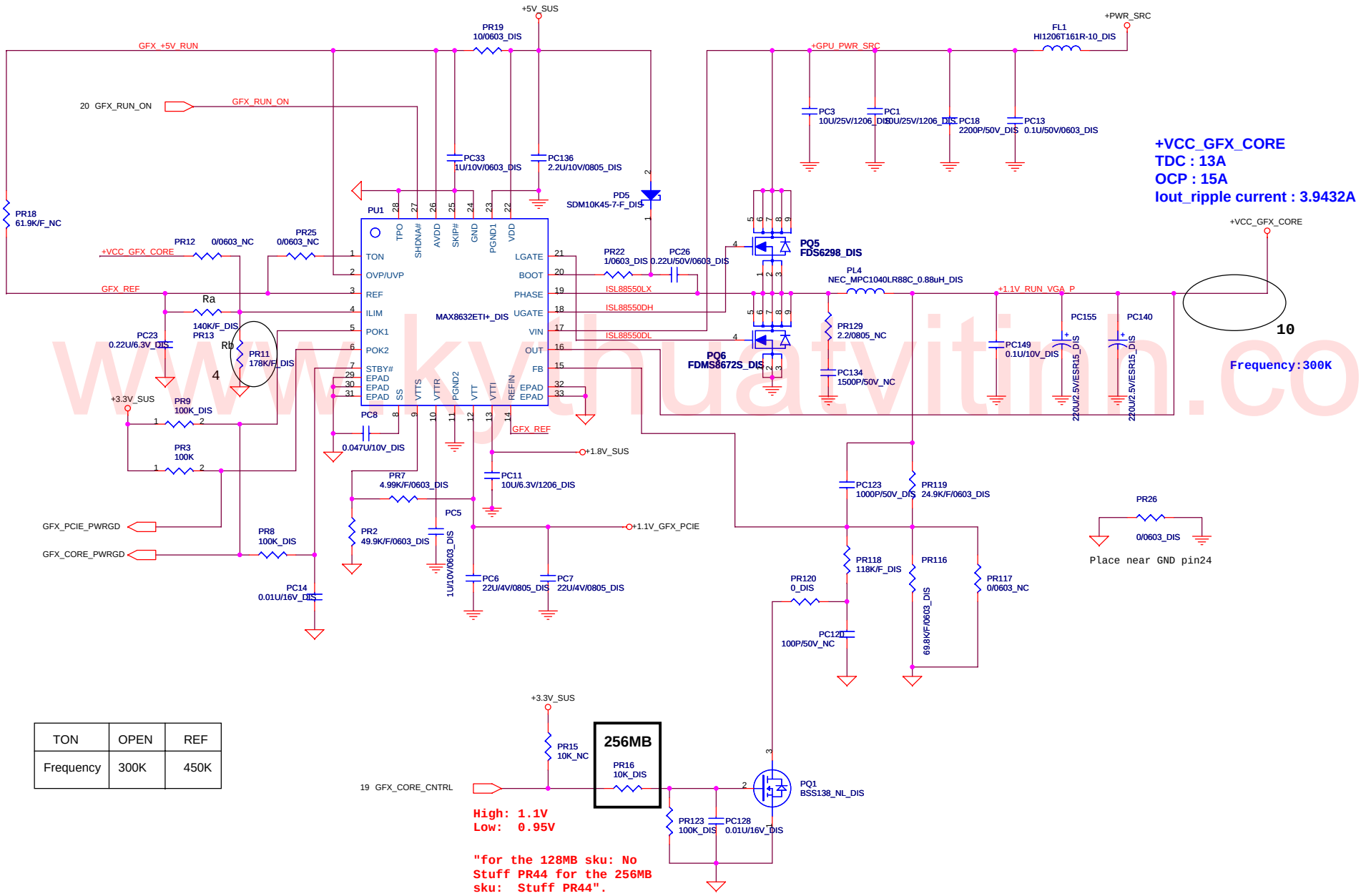

TON	OPEN	REF
Frequency	300K	450K

ILIM	Iovp=(2*(Rb/(Ra+Rb))*0.1*(1/RDSON)+(I_DELTA/2)
SKIP#	AVDD = Low-noise, forced-PWM mode. GND = Pulse-skipping operation.
OVP/UVP	The overvoltage limit is 116% of Vout. The undervoltage limit is 70% of Vout.

QUANTA COMPUTER

Title	VGA DC/DC	
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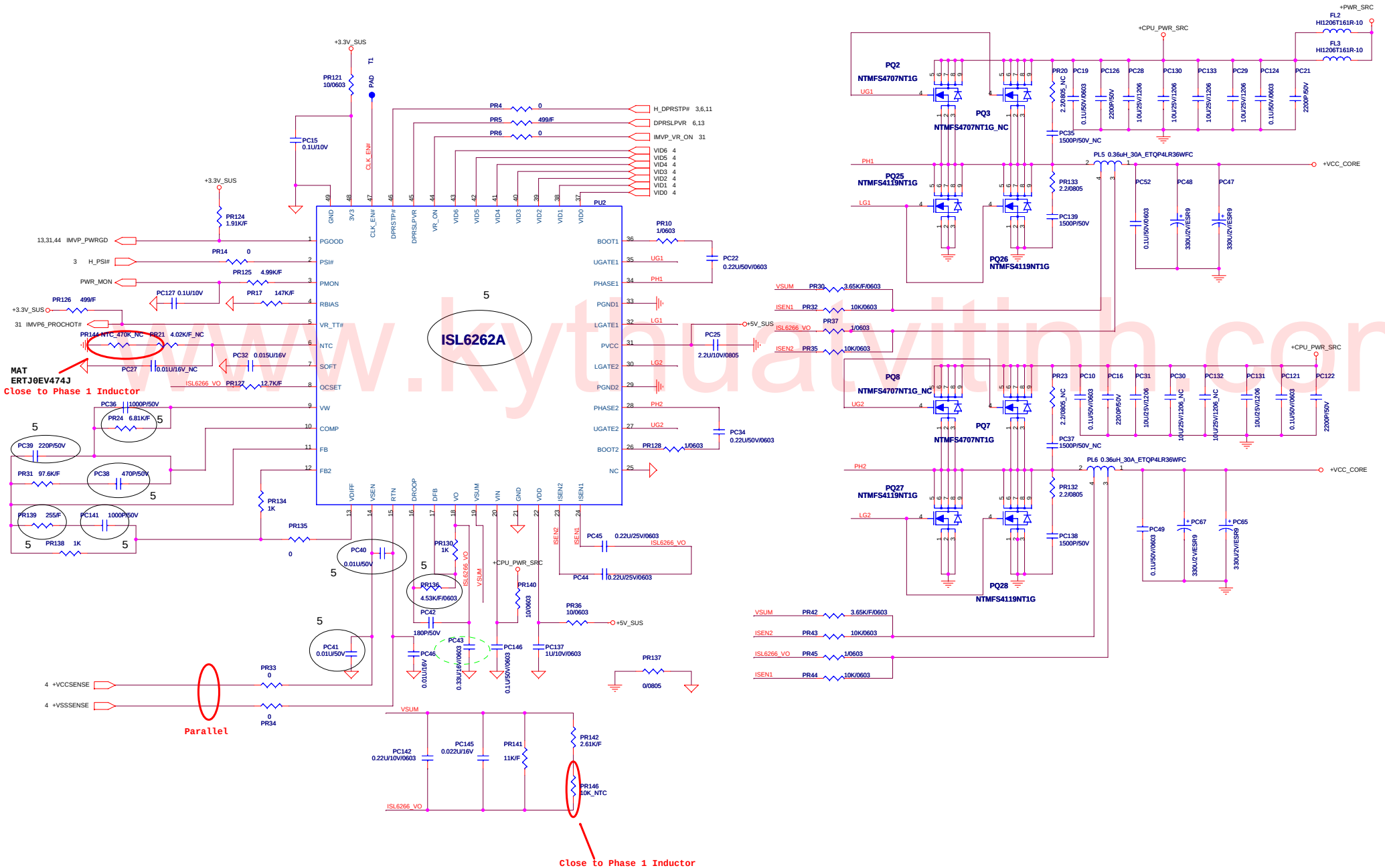

QUANTA COMPUTER		
Title	CPU_Core_2Phase (ISL6266)	
Size	Document Number GM3	Rev 2B
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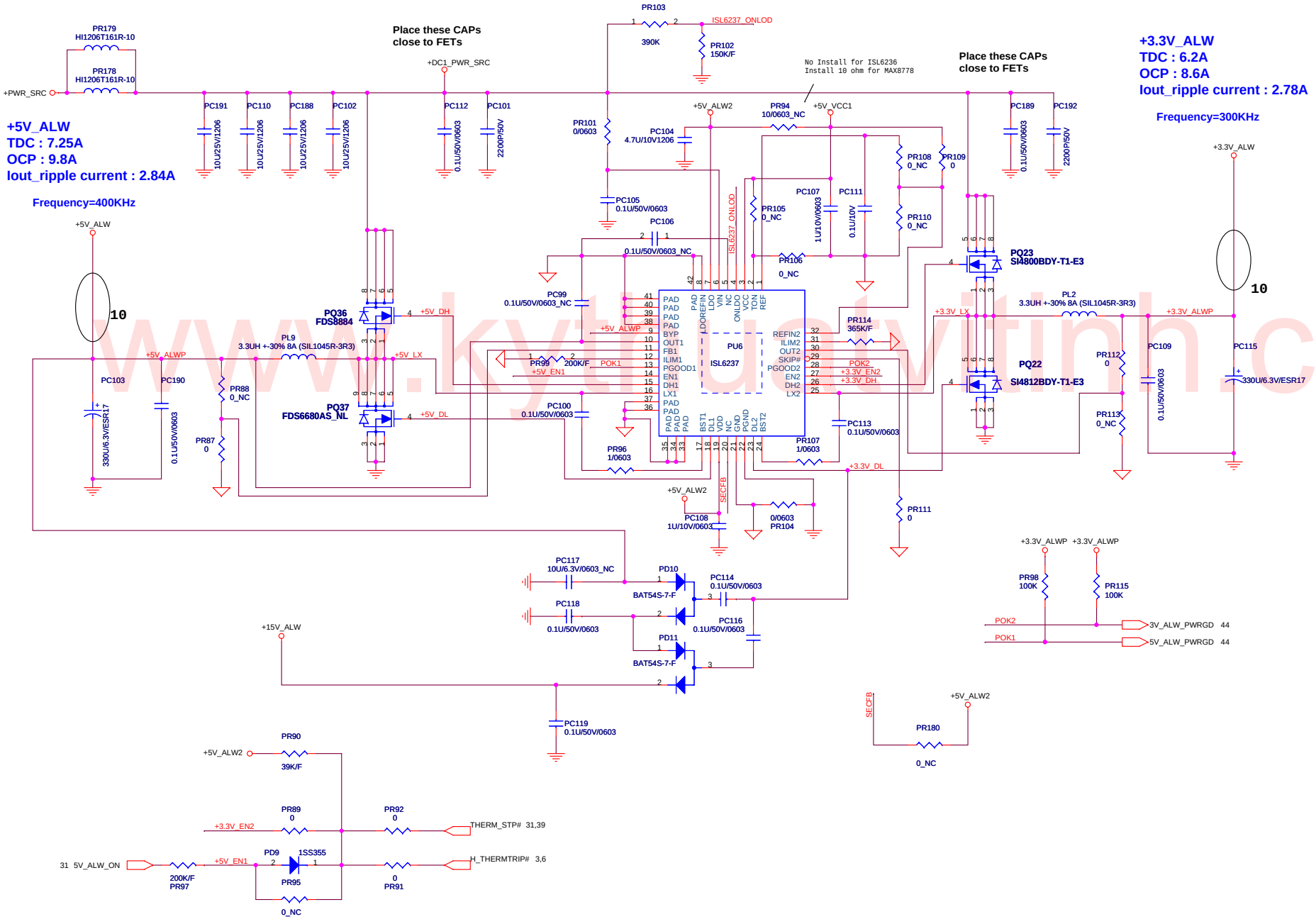
DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW



Title	VGA DC/DC		
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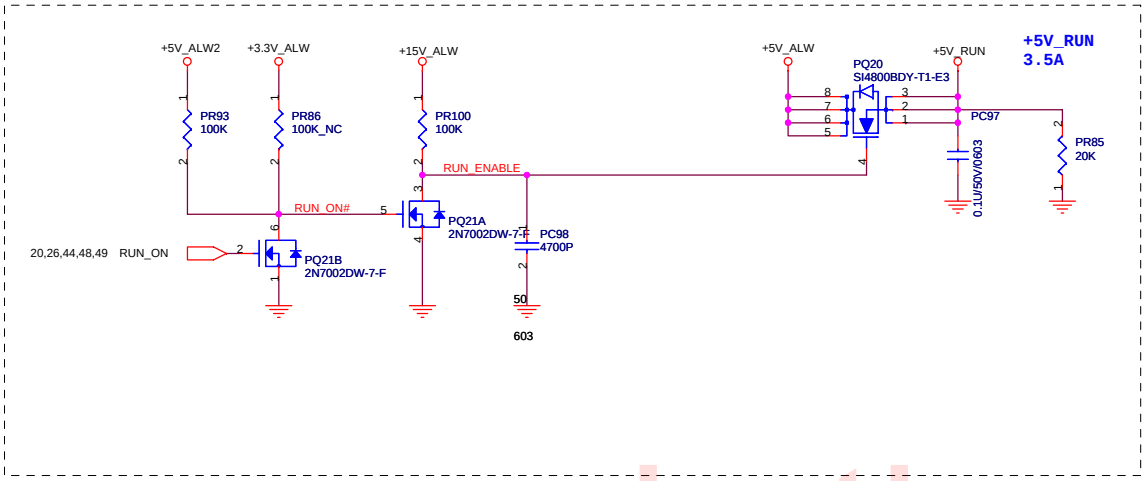
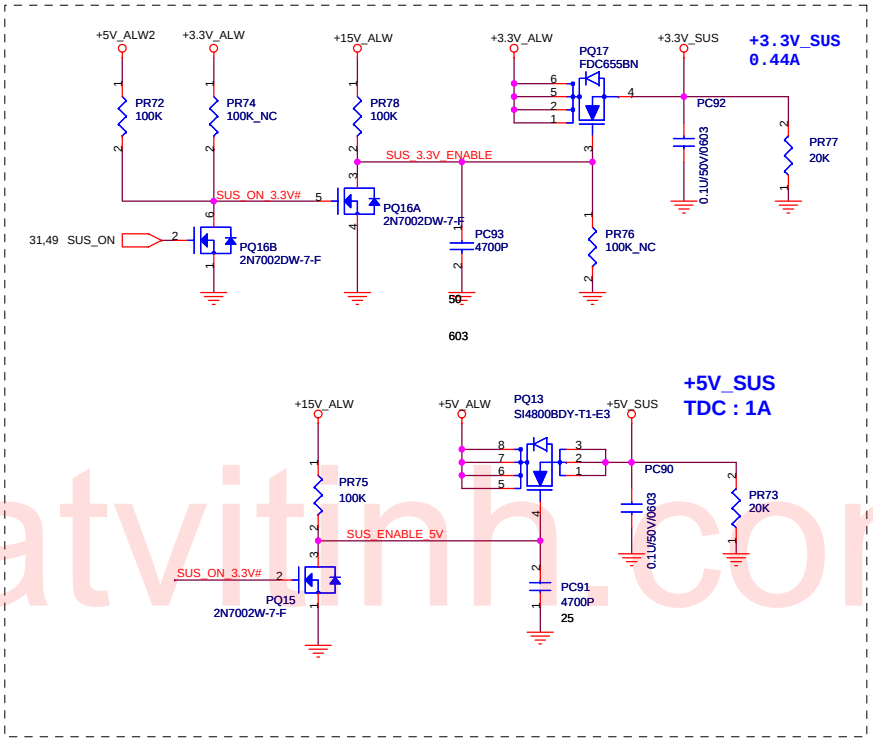
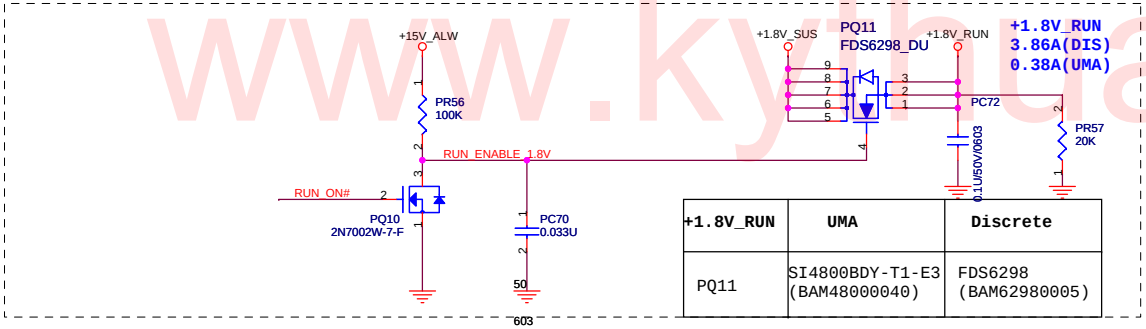
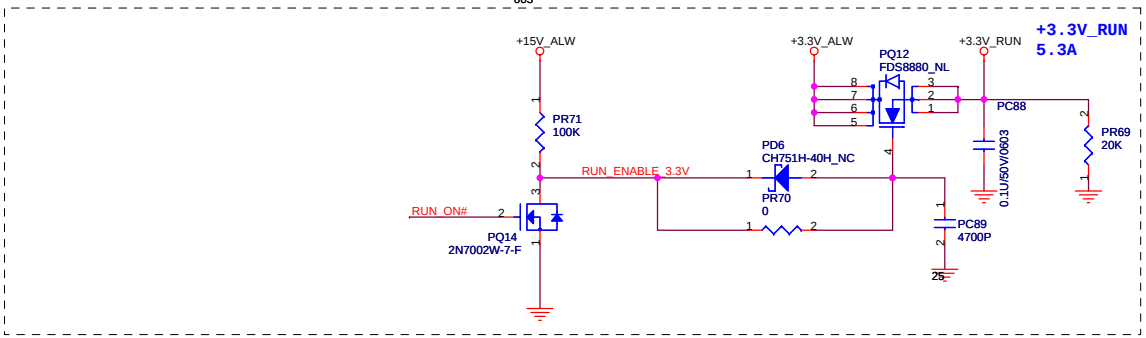
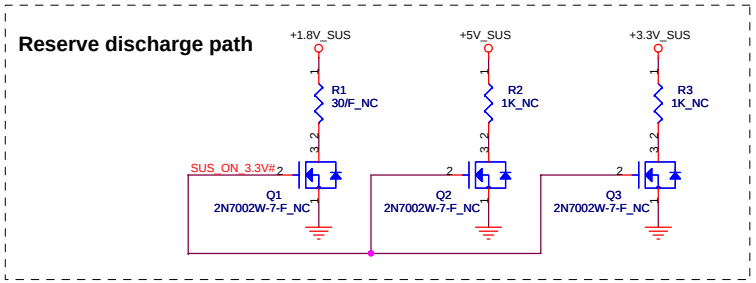


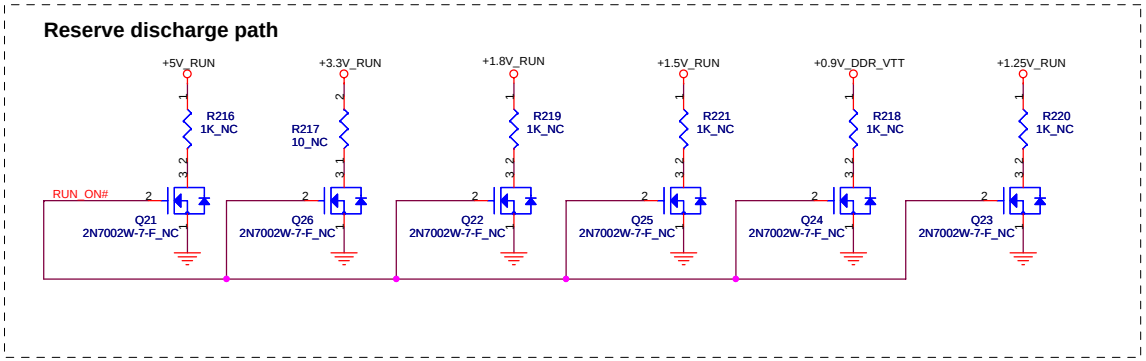




+1.8V_RUN	UMA	Discrete
PQ11	SI4800BDY-T1-E3 (BAM48000040)	FDS6298 (BAM62980005)







QUANTA COMPUTER

Title	RUN POWER SW	
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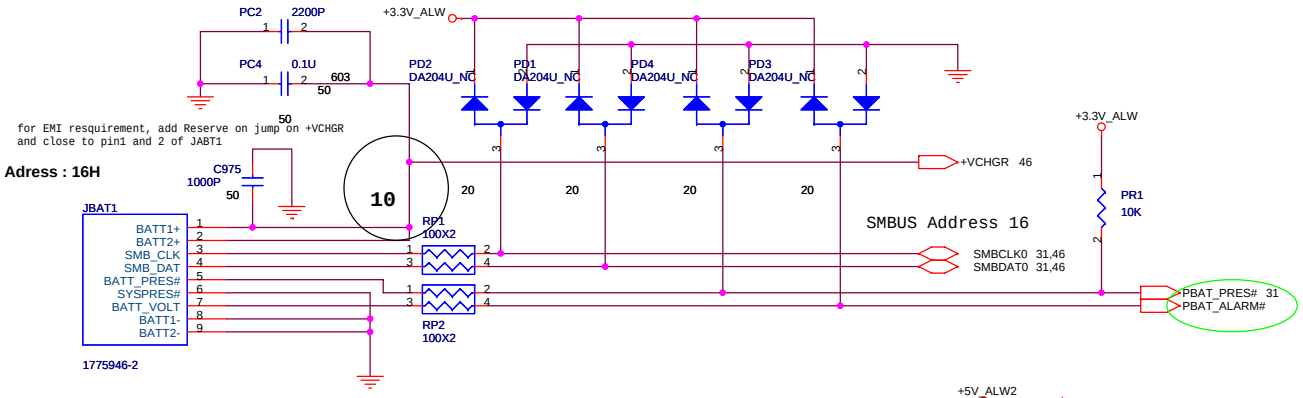

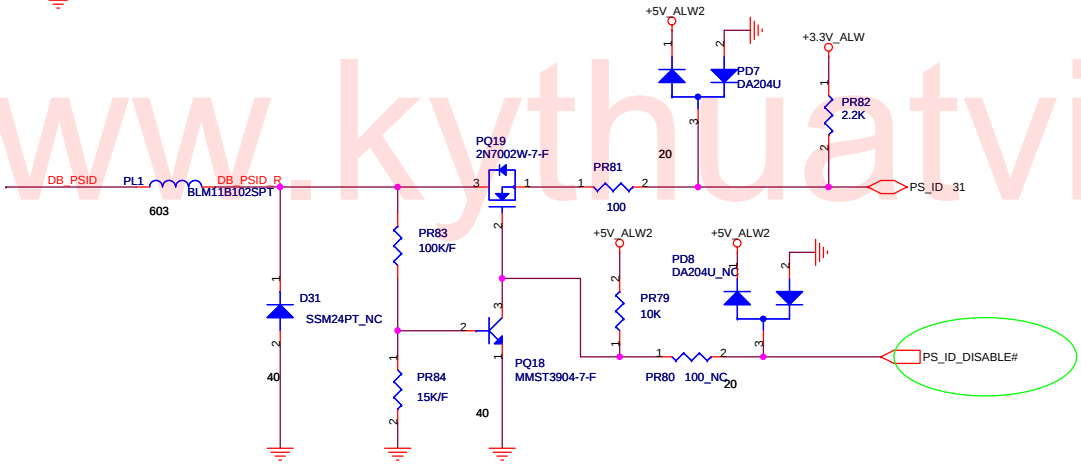

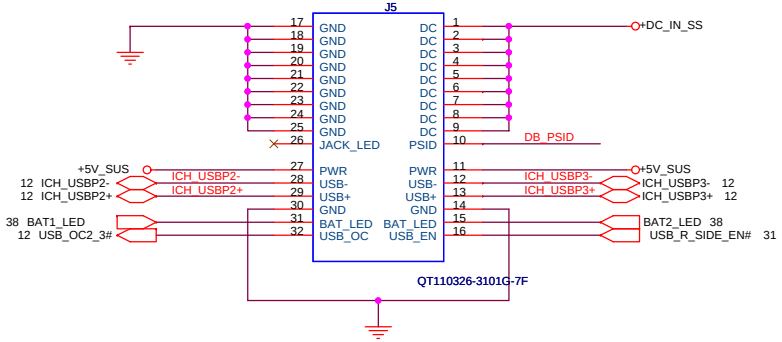

8/15: move the righT side USB and DC-in connector schematic to DB.
so change BTB(J14) CONN to 32pin

QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
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Reserved for EMI.

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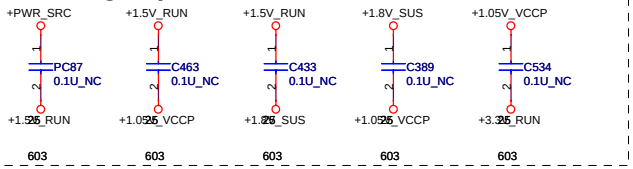
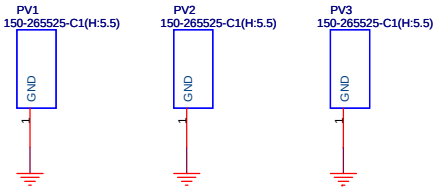
Stitching caps





Page 26
SATA (HDD&CD_ROM)

Page 27
PCCARD /CONN

Page 31
SIO(MEC5025)

Page 38
Azelia CODEC

Page 40
LAN(BCM5755M)

Page 48
1.5VRUN,1.05V(VTT)

Place C860,C216,C1426 close to PQ33.
Place C862,C222,C1427 close to PQ73.

Page 49
1.25V,1.8V,0.9V

Place C867,C254,C1428 close to PQ91.
Place C863,C253,C1429 close to PQ92.

Page 51
CPU_MAX8786(3phase)

Page 52
D/D Power

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Title	EMI CAP	
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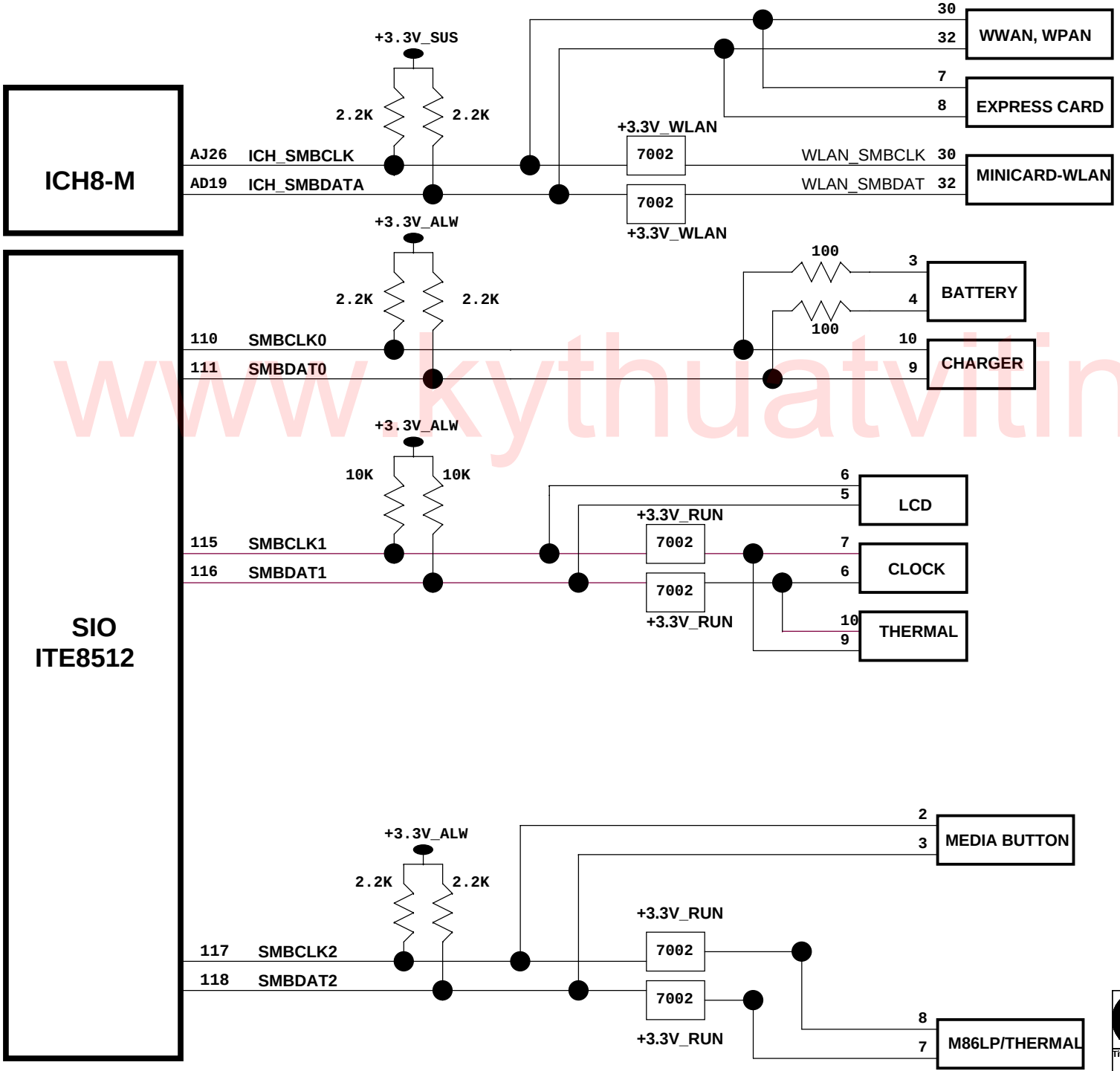

QUANTA COMPUTER

Title	SMBUS BLOCK	
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH					
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH					
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH					
S5 (SOFT OFF) / M1	LOW	HIGH	LOW					
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH					
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH					
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW					

PM TABLE

State \ power plane	+3.3V_ALW +3.3V_RTC_LDO +3.3V_WLAN +5V_ALW +15V_ALW	+1.8V_SUS +1.8V_LOM +3.3V_LAN +3.3V_SUS +5V_SUS	+0.9V_DDR_VTT +1.05V_VCCP +1.25V_RUN +1.5V_CARD +1.5V_RUN +3.3V_CARD +3.3V_CARDAUX +3.3V_R5C832 +3.3V_RUN	+3.3V_RUN_CARD +2.5V_RUN +5V_MOD +5V_RUN +5V_SPK_AMP +CPU_PWR_SRC +VCC_CORE +VDDA	+DC_IN +DC_IN_SS +PWR_SRC +RTC_CELL
S0	ON	ON	ON		ON
S3	ON	ON	OFF		ON
S5 S4/AC	ON	OFF	OFF		ON
S5 S4/AC don't exist	OFF	OFF	OFF		ON

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
BCM4401B	AD16	REQ#0 / GNT#0	PIRQB
R5C833	AD17	REQ#1 / GNT#1	PIRQC: Card reader PIEQD: 1394

	USB PORT#	DESTINATION
ICH8-M	0	Right Top
	1	Right Bottom
	2	Side TOP
	3	Side Bottom
	4	Ext. USB TOP
	5	DIgital Camera
	6	Express Card
	7	WPAN/Bluetooth
	8	Ext. USB Bottom
	9	WWAN
ECE 5011	1	None
	2	None
	3	None
	4	None

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 WPAN
Lane 4	Express Card
Lane 5	None
Lane 6	None

QUANTA COMPUTER

Title	Schematic Block Diagram1	
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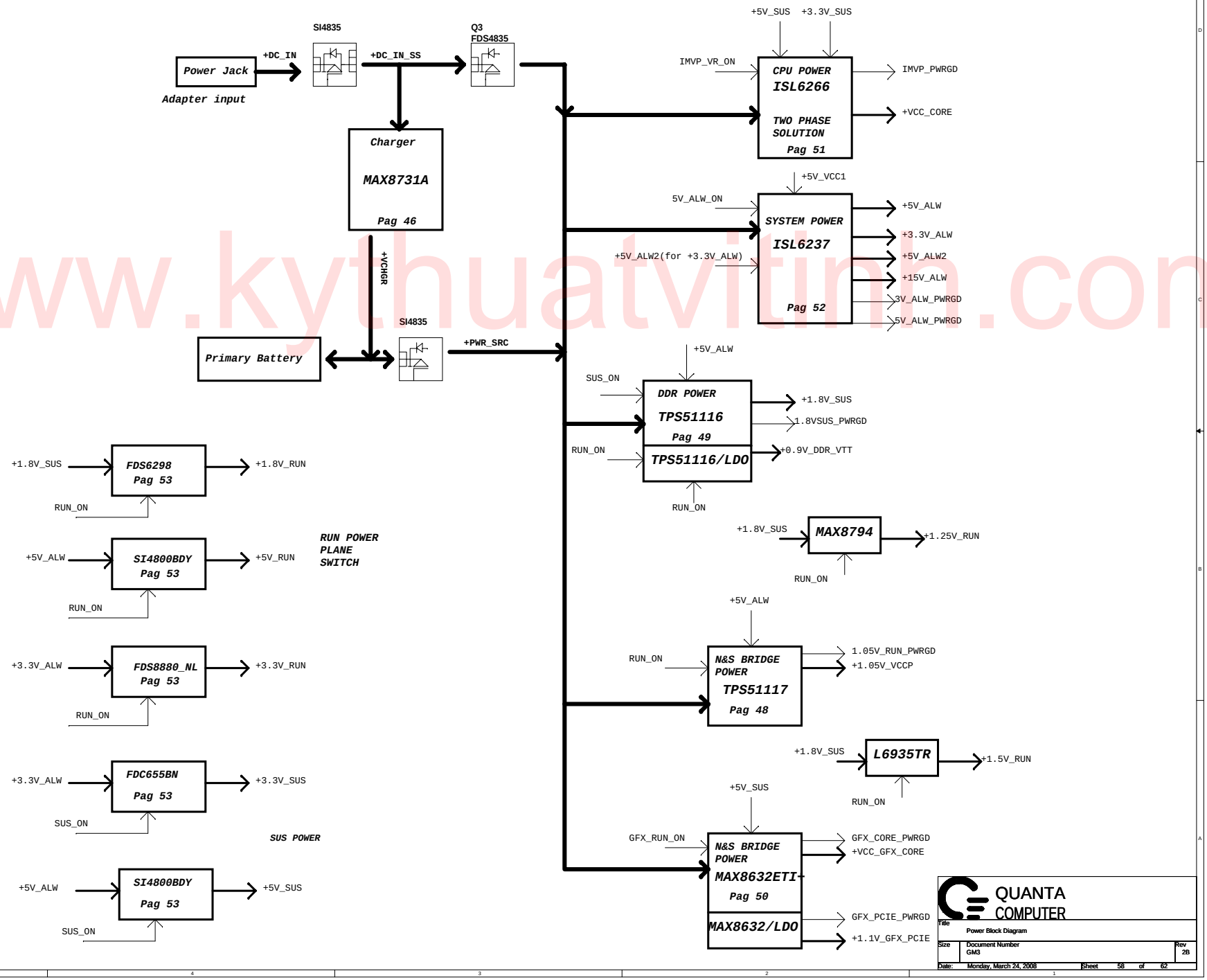
GM3 Power Design Block Diagram
2007/09/06



Model	Item	Page	Date	Rev.	Description
Pacino of Intel	1	All	7/25	1A	Base on David.Lin 070725 1400 release preliminary schematic to check the all part PCB footprint. I found there are some parts not had footprint and update it. The change location as below. There are some concern need to highlight: 1. Dichanged to CH751H-40PT. 2. LB4 & LB5 need to changed to Dell PSL part. 3. LAN jack need to double check. 4. JKB1, JMOD1, JP1, L15 need to get the spec for create new layout footprint and apply for new P/N. 5. JDIM1 & JDIM2 should be combined to one JDIM. U12, L27, L28, C225, C226, D4, L9, U3, JDIM2, D1, LB4, LB5, U14, U18, U22, U23, U25, BT2, CON2, CON3, L34, L35, Q10, U11, U13,ESD1, CON7, D15, D38, D39, D40, JACHER1, JKB1, JMOD1, JP1, L15, R1, Q7, Q67, SW1, U28, U41, FL1, FL3, FL4, FL7, FL8, FL9, FL10, FL11, JDC201, PC125, PC139, PC151, PC153, PC161, PL3, PL4, PL10, PL11, PL12, PQ13, PQ24, PQ42, PQ43, PQ44, PQ45, PR84, PU1, PU4, PU9.
	2	39	8/13	1A	FAE review schematic and recommend add C8466 & C8356 between MEM_DIODE1_P and MEM_DIODE1_N. This is just a reservation in case there's any noise coupling issue happening. Then have 2 different filter cap locations (one near EMC1423 and the oyher near the OTP 3904 diode) to try to reduce the noise. Of cource, only one cap can be installed.
	3	25	8/13	1A	FAE review schematic and recommend add poly switch and 0.1u cap colse to 5V_RUN of HDMI CONN to avoid NB reboot.
	4	29	8/15	1A	FAE review schematic, NC FIL0 pin since SCB33 don't need cap to GND
	5	19	8/15	1A	The strap on VIP[3] is for enabling HD Audio on M86. so pull to high.
	6	54	8/15	1A	move the right side USB and DC-in connector schematic to DB. so change BTB(J2) CONN to 32pin
	7	19	8/15	1A	8/15 FAE review schematic: reverse TMDS signal for working property. change voltage allocation resistor to make sure the input clock swing level is at 1.8V
	8	39	8/16	1A	8/16:per SPEC recommend: use 7002 to avoid the leakage current from 3V_SUS.
	9	37-39	8/17	1A	8/17:add diode to protect below GPIO port,p39---FAN1_PWM p38---SNIFFER1 and POWER_ SW_IN0#, p37---MEDIA_INT
	10	52	8/20	1A	8/20: For FAE suggestion. Charge pump from +5V LDO, might cause high ripple voltage. Add PC116 10U/0.3V/0603.
	11	52	8/20	1A	Since FDS8878 Rq too big,change PQ44 to FDS8884.
	12	52	8/20	1A	Change PR225 to 180K and PR224 to 294K for setting current limit.
	13	52	8/20	1A	For FAE recommend , PD16 could be deleted.
	14	49	8/20	1A	Change PR85 to 143K for 1.82 output voltage
	15	48	8/20	1A	Due to output ripple current too big ,cheange PL25 from 0.88uH to 1.5uH.
	16	48	8/20	1A	PR449 should be cancelled, not necessary
	17	48	8/20	1A	Change PR452 to 9.09k for OCP
	18	48	8/20	1A	For FAE recommend. PC447 no stuff, reserved.
	19	48	8/20	1A	Add PC78 for meet output ripple current.
	20	48	8/20	1A	Change PR102 to 4.53K and PR105 to 49.9k for setting VTT=1.1V. (VTTS =REFIN/2=1V)
	21	38	8/22	1A	Added LED level shift for support white LED need used 5V drive.
	22	22	8/23	1A	add level shift circuit to protect thermal IC
	23	42	8/23	1A	add level shift circuit to provent ALW and LAN plan interconnect
	24	13 31 37 40 48 55	8/24	1A	Check single net and correct by JM
	25	52	8/27	1A	Due to SIL1045R-3RBPF will be EOL, change PL11,PL12 to SIL1045R-3R3.
	26	37	8/27	1A	change KB pin number to 32 pin
	27	43	8/28	1A	change LED of LAN jack control signal to LINKLED
	28	43	8/28	1A	Co-layout SIM card connector and WTB together
	29	37	8/28	1A	Dell had update K/B pin define to 34 pin and re-define pin definition
	30	31	8/28	1A	KSO18 is output pin, so change to pin 85, and KB_DET# from pin 85 change to pin 70.
	31	39	8/28	1A	reverse 1-4 pin definitiom for thermal team design
	32	28, 12	8/29	1A	change R5c833 PCI_PIRQD# to PCI_PIRQB# for AMD platform signal control requirement
	33	37	8/29	1A	due to move keyboard light sensor to media button board, add KB_BACKLITE_SET function to media button connector pin 10.
	34	37	8/29	1A	change keyboard pin number to 32 pin
	35	48	8/29	1A	For Dell recommend,change 1.5V LDO from MAX8794 to ST L6935.
	36	49	8/29	1A	For TI FAE recommend,connect PC76 to GND.
	37	35	8/30	1A	For support power USB function, change power to 5V_ALW
	38	31	8/30	1A	change IRVP6_PROCHOT# from pin 88 to GPI 1 for design requirement. and pin88 assign to 5V_ALW_ON
	39	25,43,38	8/30	1A	for EMC team requirement, reserve cap, ESD protect, common choke at CON side
	40	52	8/30	1A	Add PC180 for reserve MAX8778 IC.
	41	52 53	8/30	1A	Due to Pacino need to support USB charger function,change following item. 1.Change power plan from +5V_ALW to +5V_ALW2:pin9 ,pin7,pin19, PC116 and PR156 2.Add a load switch PQ42 for +5V_ALW to +5V_SUS
	42	28	8/31	1A	refer M86 platform, change to 100 ohm
	43	22	9/2	1A	Reserve external spread spectrum circuit for ATI graphic using
	44	48	9/3	1A	change PR455 to 237K from 178K to setting switching operating frequency at around 300 KHz
	45	52	9/3	1A	For FAE recommend, change PD14 input power from "+5V_ALW2" to "+5V_ALW" and PC116 can be NA.
	46	52	9/3	1A	For FAE recommend, connnet pin20 to pin19 for ISL6236 (or MAX8778) can populate on ISL6237 location.
	47	49	9/3	1A	Change PC155 to correct net name "+1.8V_SUS_P".
	48	20	9/3	1A	M86 internal thernal protect function pin is high active, re-design protect logic circuit for it.
	49	54	9/3	1A	for EMI requirement, add Reserve on jump on +VCHGR and close to pin1 and 2 of JABT1
	50	38	9/3	1A	Reserve ESD protector at J4 pin1 (+3V_RUN)for Biometric (close to J4)
	51	46	9/3	1A	Add PC39 for reserve debug noise issue.
	52	48	9/3	1A	Change PU5 pin6 through PR58 to +3.3V_SUS.
	53	49	9/3	1A	Change PR79 from 10K to 0ohm.
	54	50	9/3	1A	For reserve EMI sunnber, add PR157 and PC117.
	55	48	9/3	1A	For DELL recommend , reserve PC143 and PC144 for TI controller.
	56	38	9/3	1A	For DELL recommend , Add GPIO pin to mask HDD and BT LED active
	57	17, 33, 34	9/3	1A	for WLAN card using CLK_REQ pin, so change CLK_PCIE_MINI1 to WLAN and CLK_PCIE_MINI3 to WPAN.
	58	26, 6	9/3	1A	add third pair LVDS signal to support 24bit panel
	59	31	9/4	1A	delete JACK_LED_DET# pin for DC jack design, so move KSO18 to pin99.
	60	46	9/5	1A	Reserve a 0 ohm PR59 resister for EA test.
	61	48	9/5	1A	Add PC145 for ST FAE recommend.
	62	37	9/6	1A	Add KB_BACKLITE_EN control circuit on MB side
	63	37	9/6	1A	Add 3_ALW at pin 5 for Lid switch IC power pin
	64	42	9/6	1A	Reserved BCM5784M SUPER_IOOQ circuit.
	65	30	9/8	1A	add MMC card function at card reader connector

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Model	Item	Page	Date	Rev.	Description
Pacino of Intel	1	12,13, 17,25, 69	9/27	2A	modify SST design issue: 1. delete unnecessary 0 ohm resistor 2. select correct frequence for DIS/UMA(R351&R342) 3. CARD_CLK_REQ# pull high 4. PLTRST_DELAY# pull down to avoid floating. 5. NC R451 to set Boot BIOS Strap for LPC interface
	2	52 ,50	10/2	2A	For second source concern, change below item. 1. Change PD9 from BAS316 to 1SS355 2. Change PD5 from CHS01H-40PT to SDM10K45-7-F 3. Change PQ1 from BSS138-7-F to BSS138_NL
	3	8	10/3	2A	use 0805 0 ohm to instead of jump(1/8W, 1.6A per resistor)
	4	19	10/3	2A	pull high the GPIO 0 & GPIO 1 to enable PCIE FULL TX OUTPUT SWING and PCIE TRANSMITTER DE-EMPHASIS function to solve no display problem.
	5	41	10/15	2A	The camera pin assignment changed : 2 pin camera power pin and they are 3.3 V ..
	6	40	10/15	2A	change resister setting for STA92HD73C chip
	7	46 52	10/15	2A	Due to SI4810BDY-T1-E3 will be EOL, change PQ29 and PQ22 from SI4810 to SI4812.
	8	19	10/16	2A	Due to VDDR4 and VDDR5(option reference source voltage) use 1.8V_RUN, FAE suggust DVPDATA use 1.8V pull high
	9	33	10/17	2A	remove external SIM card CONN that on MB side
	10	13	10/17	2A	It is multi_function pin(SMBALERT#/GPIO11). Before bios programming, the PIN function is SMBALERT.If it is pull high to 3.3_RUN, the ICH8 will be alert by this pin. It cause the S3 can't normally sleep when system cold boot first time. so change to SUS power
	11	38	10/18	2A	Sniffer behavior is reverse, so modify design at PT stage
	12	42	10/18	2A	change to 5784 design
	13	40	10/22	2A	change TPA6040A4 symbol design to meet SPEC definition
	14	19	10/22	2A	FAE suggust: Ground R28/62B/B2B and Implement R2SET to GND even if DAC2 is unused.
	15	43	10/23	2A	for factory requirement---increase pad length for SMT yield rate
	16	41	10/24	2A	for DELL SPEC---change camera conn pin definition
	17	31, 37	10/25	2A	modify LED Key board Illumination schematic and remove EC pin 68
reserve	18	44	10/29	2A	HWPG monitor change: change 3V/5V_ALW_PWRGD to GFX_PCIE/CORE_PWRGD
reserve	19	12,13, 14,31	10/29	2A	create +3.3V_S5 and +5V_S5 power at ICH part to fix ITE chip SUS resume problem, and move LID_SW# to pinj 68 and pin 120 for S5_ON using
	20	35	10/30	2A	add FSUSB31KBX to control USB signal can be passed above SUS, and USB_SIN_SIDE_EN# can control whether USB can supply power for external device at S5 mode
reserve	21	53	10/30	2A	For EE request , add two power rail "+3.3V_S5" and "+5V_S5" for south-bridge battery mode.
	22	48	10/30	2A	1.5V_RUN_PWRGD pull-high to RUN_ON for solve glitch issue.
	23	38,54	10/30	2A	add 1000p cap and close to connector for EMI
	24	35	10/30	2A	change LCD connector pin definition for LED panel: 1. change pin 8 form GND to +5V_ALW 2. change pin 16 from GND to LCD_VCC
	25	31	11/1	2A	change GPIO design 1. delete pin 83 SNIFFER_YELLOW# 2. move 5V_ALW_ON to pin 83 3. swap pin 108 WIRELESS_ON/OFF# and pin 35 SNIFFER_PWR_SW#
	26	38	11/1	2A	change GPIO design 1. swap WIRELESS_ON/OFF# and SNIFFER_PWR_SW# 2. remove SNIFCircuitFER_YELLOW#
	27	31	11/5	2A	change GPIO design for fix thermail no function issue 1. NC ADAPT_OC and ADAPT_TRIP_SEL 2. add #V_ALW_ON function at pin 76
	28	3	11/5	2A	Modify H_THERMTRIP# Voltage Level shift circuit.
	29	41	11/6	2A	add one GND pin for Audio precision dB value
reserve	30	37	11/8	2A	add circuit to control CIR power
	31	49	11/12	2A	Add PR181 for reserve +5V_ALW2.
	32	43	11/12	2A	for EMI requirement, add 7p cap close to LAN switch
	33	37	11/13	2A	for DELL requirement, add fuse between +5V_RUN and +KB_LED
	34	31	11/13	2A	use pin 14(WRST#) to monitor THERM_STP# function
	35	25	11/13	2A	for Silicon image FAE suggestion: 1. EMI may come from the impedance mis-match, that'll get distorted waveform . Try to replace the common choke with (i.e 22 ohm) resistor. 2. Try to reduce the source termination resistor (i.e 300 ohm --> 150 ohm) to get cleaner eye . 3. change AVCC33V to 3.3V_RUN
	36	25	11/13	2A	per FAE suggestion:change C525 and C524 to 2.2u for batter Audio precision
	37	50	11/13	2A	Chnage PR11 to 100Kohm for set correct O.C.P.
	38	50	11/13	2A	For EE request, set VGA voltage to 0.95V/1.1V. Change PR116 to 69.8K and PR118 to 118K.
	39	4	11/13	2A	Base on acoustic team test ,add two EC-cap for noice issue. Stuff C733 and C766.
	40	52	11/13	2A	Base on test result, change PR114 to 294K for set OCP.
	41	48	11/13	2A	Change PR161 to 11K for set correct OCP.
	42	48	11/13	2A	For 1.05V jitter issue, chnage below item. UMA: Change output CAP from 390U/2.5V/ESR10 to 330U/4V/ESR25 Discrete: 1. Change output CAP from 390U/2.5V/ESR10 to 330U/4V/ESR25 2. Add PC62 1500PF
	43	48	11/13	2A	Change 1.05V UMA PQ33 from FDS6676AS to FDMS8672S for improve efficiency.
	44	49	11/13	2A	Base on EA report test , stuff PR171 and PC188 for reduce hiogh side VDS ring.
	45	46	11/13	2A	Due to software support UL function via "IINP", no stuff UL circuit.
	46	13	11/14	2A	add 4.7k on PCIE_MCARD1_DET# trace to solve WLAN card detect issue
	47	19	11/15	2A	change GPIO pin from 3.3V_RUN to 3.3V_delay to solve leakage problem between 3.3V_RUN and 3.3v_delay(4ms) when boot.

QUANTA COMPUTER

Model	Item	Page	Date	Rev.	Description
Pacino of Intel	1	32	11/26	2B	Change RTC connector because ME modifyr.
	2	31	11/26	2B	Exchange 'SNIFFER_PWR_SW#' AND 'WIRELESS_ON/OFF#. per EC limition.
	3	31	11/26	2B	Change NUM_LED# from SIO pin98 to pin 88 and used Pin 98 for BID only per EC limition.
	4	54	11/26	2B	Change PSID relation parts to +5V_ALW2 for power saving in S5.
	5	38	11/26	2B	Change Sniffer Switch power rail from RUN plane to ALW plane.
	6	43	11/26	2B	Added LINK1000# for BCM cann't support GLAN LED drived by LINKLED#/SPD100LED#.
	7	45	11/27	2B	Modify Screw hole base on ME update.
	8	17	11/29	2B	Link to MCH DPLL clock is wrong. Change to correct link.
	9	31	11/30	2B	Fine tune GPIO define for EC.
	10	37	12/04	2B	Change MMB LED power source from 5V_ALW2 plane to 5V_ALW for power saving and avoid LED flash when AC in.
	11	22	12/04	2B	Check AMD +3.3V_DELAY power plane connection component for AMD new update REF133-7 file.
	12	40	12/19	2B	Change Audio AMP thermal PAD leave to NC.
	13	31	12/26	2B	Change SMBus pull hihg resistor form 2.2k to 10k for LED panel flash.
	14	37	12/26	2B	since we will use WLAN and BT LED to show function at factory side. Change power supply of Cap and Num LED from 5V_ALW2, 3.3V_ALW to 5V_RUN and 3.3V_RUN.
	15	19	12/26	2B	Change HDMI detect circuit to solve external panel feed back voltage shortage then caude ATI chip can't switch to HMDI mode problem.
	16	37	12/26	2B	Change the Media board power from 3V_ALW to 5V_ALW2 to solve LED flash issue when AC/Bat plug in.
	17	37	12/26	2B	Change the lid switch IC power source from 3.3V_SUS to 3.3V_ALW to avoid system can enter S4 mode but wake up fail problem
	18	48	1/3	2B	Change PC85 to 680P for meet sequence.
	19	50	1/3	2B	Change PR7 to 4.99K for adjust +1.1V_GFX_PCIE rail.
	20	53	1/3	2B	Change PQ11 from SO8 to power package footprint.
	21	48 49 50 52	1/3	2B	Change PR161 ,PR172 ,PR11 ,PR114 to correct resistance for reliability request.
	22	35	1/4	2B	remove USB charge circuit
	23	26	1/7	2B	pull DPST signal to high for setting 100% duty cycle
	24	31	1/7	2B	pin12 should reserve 1u cap for ITE8512JX using
	25	19	1/7	2B	modify HDMI detect circuit to fix the monitor detection problem..
	26	55	1/7	2B	create EMI spring
	27	31	1/11	2B	per TXC report, we should change W1 cap to 18p
	28	41	1/11	2B	per IDT FAE suggestion, serial 22 ohm on DMIC_CLK can help DMIC performance
	29	37	1/11	2B	add 10u cap at JMB1, let 3.3V_ALE get lower drop voltage on MMB side.
	30	6, 19	1/11	2B	EMI demand add 33p cap on RGB signal.

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Pacino of Intel	1	25	2/14	3A	add level shift to separate the data and CLK of VGA IC and HDMI TV, and also reduce stray capacitance.
	2	25	2/14	3A	change diode to reduce stray capacitance per WPI suggestion
	3	12,28,31	2/14	3A	use pin-22 monitor ICH_AZ_CODEC_RST# to delay NB_MUTE# signal for solve PO noise issue
	4	50	2/20	3A	For Reliability calculate , change PR11 from 150K to 178K.
	5	51	2/20	3A	Due to C4E hung up issue, change v_core power IC from ISL6266A to ISL6262A. Below is change list. 1. PU2: Change PN from AL006266000 to AL006262025 2. PR24: Change PN from CS28252FB15 to CS26812FB13 3. PC39: Change PN from CH11006JB18 to CH12206KB14 4. PC38: Change PN from CH12704JB07 to CH14706KB18 5. PR139: Change PN from CS11002JB32 to CS12552FB18 6. PC141: Change PN from CH22206KB16 to CH21006JB10 7. PC40,PC41: Change PN from CH1336K1B02 to CH31006KB18 8. PR136: Change PN from CS23833F911 to CS24533F921
	6	48	2/20	3A	For 1.05V OVP issue in Vista , no stuff PC62.
	7	25	2/20	3A	Due to L6935 has improved powergood issue, no stuff PR183 and stuff PR66.
	8	48	2/15	3A	add HDMI solution per Silicon image suggestion 1. Change R233 to 650 ohm 2. Remove external RC between HDMI +/- signal. add HDMI EMI solution DIS:CXCG900U000 / EXC24CG900U; UMACXCG240U000 / EXC24CG240U
	9	35	2/23	3A	add common chock for EMI solution Quanta PN: DC09004A014
	10	35	2/25	3A	cange power jump to 0805 resistor
	11	27	2/25	3A	add filter CAP for EMI
	12	13, 37	2/25	3A	by ICH-8 GPIO-17 dectect the LED keyboard connector
	13	17	2/26	3A	exchange 27SS and 27NSS / DREF_SSCLK# & DREF_SSCLK for follow CLK GEN spec. design.
	14	13	2/27	3A	ICH_RSMRST# pull down for RTC timer issue when plug in AC
	15	40, 41	2/27	3A	MUST ADD 2.2K-OHM RESISTORS TO PREVENT AMPLIFIER CLIPPING and ADD 220PF CAPACITORS TO ALLOW PROPER DYNAMIC RANGE MEASUREMENTS
	16	19	22/29	3A	Add 10k ohm on HDMI_DET to ensure Vin on test fixture input 2.4V the voltage not drop under 2V spec. definition.
	17	9	03/03	3A	Based on SR_check 1.6, UMA should pull down 75 ohm on TV_DAC pins if disable TV-out function.
	18	40	03/05	3A	Change C518, C519 from 0.033uF to 0.01uF per Dell audio update requirement.
	19	40	03/20	3A	Change net name of "AUD_HP2_L1" between R708 & C525 to "AUD_HP2_L0_R" and "AUD_HP2_R1" between R708 & C525 to "AUD_HP2_R0_R" for the original net name same as U20.15 & U20.16 will cause the HP2 no function.

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