# Kirin (FX2 with NS) VER : 1A

**DDRII-SODIMM1** PG 7,8
**DDRII-SODIMM2** PG 7,8
533 MHz DDR II

**AMD S1**
**Turion 64 Rev.F Dual-Core/ Sempron Rev.F Single-Core**
Dual-Core 35W / Single-Core 25W
(638 S1g1 socket)
PG 3,4,5,6

***HT_LINK***

**CPU VR** PG 37
**CLOCKS** PG 13
**Thermal Monitor** PG 35
**SYSTEM** PG 38
**VCCP DDR II** PG 39
**BATT CHARGER** PG 36
**AC/BATT Conn.** PG 41
**RUN POWER SW** PG 40

**Panel Connector** PG 18 — LVDS
**VGA Conn.** PG 19 — VGA

**RS485 A12**
465 FCBGA
PG 9,10,11,12

PCI-E(1) → **Express Card** PG 25
USB2.0(P1)
PCI-E(2) → **Mini Card (WLAN)** PG 24
USB2.0(P5)
USB2.0(P0,P2) → **USB Conn. Right Side x2** PG 28
USB2.0(P4,P6) → **USB Conn. Back side x2** PG 28

**SATA - HDD** PG 23 — SATA II
**Fixed PATA ODD** PG 23 — IDE

***A_LINK***

**SB600 A13**
549 BGA
PG 14,15,16,17

AC97/Azalia
33MHz PCI
LPC

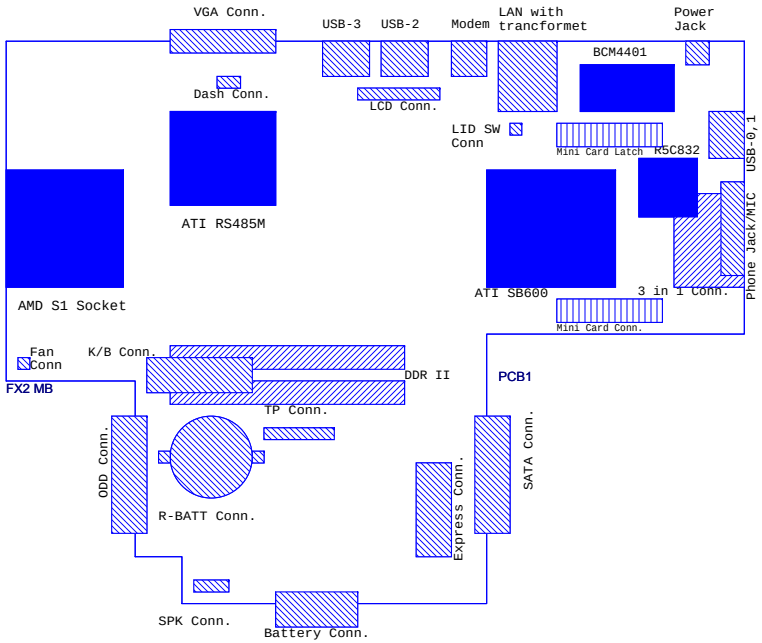
**BCM4401 (B0)** PG 33 → **RJ45/Magnetics** PG 34
**3 in 1 Card R5C832** PG 20,21 → **3 in 1 Conn.** PG 22
**Mini PCI(for debug)** PG 42

**AUDIO** PG 31 → **Audio Jacks** PG 32
**MDC** PG 26 → **Tip Ring** PG 26

**KBC**
NS97551/87541
PG 27

***X-Bus***

**KB Conn.** PG 35
**Touch Pad** PG 30
**Flash ROM** PG 27



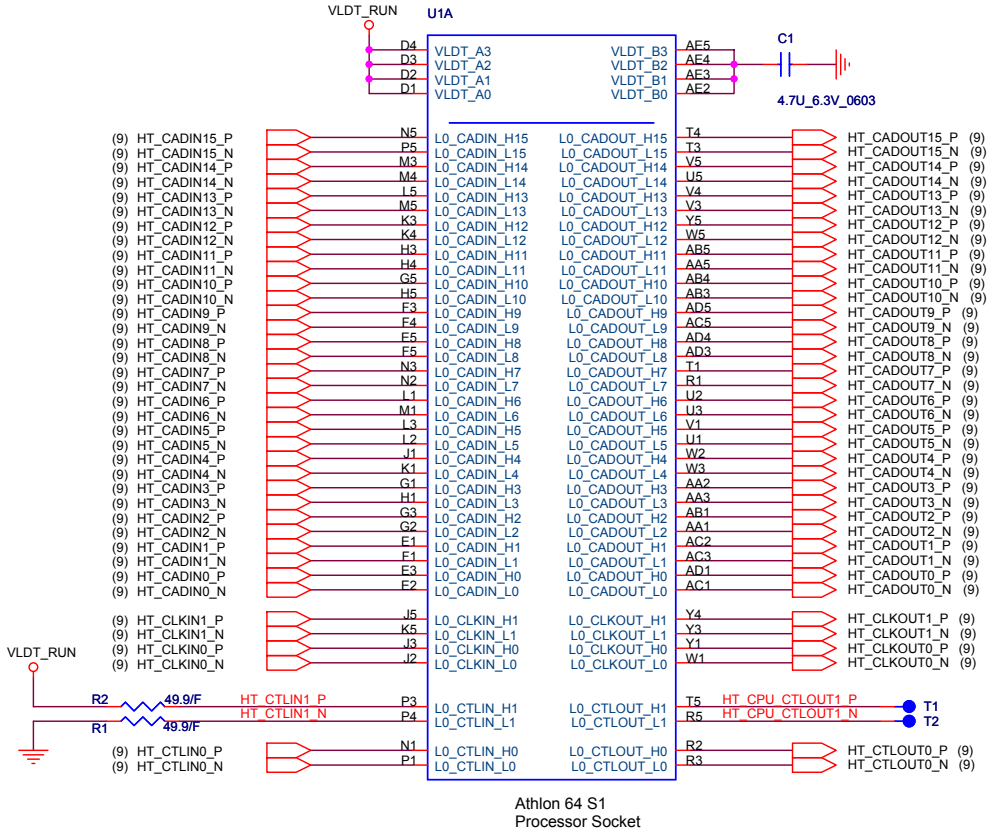

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | BLOCK DIAGRAM | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 1 of 47 | |

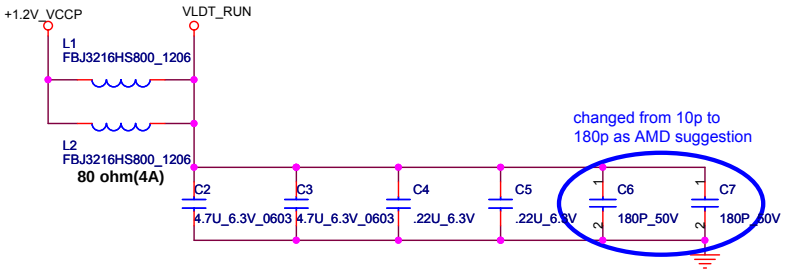
## INDEX

## PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE




Athlon 64 S1
Processor Socket




## LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | ATHLON64 HT I/F | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 3 of 47 | |

# Processor DDR2 Memory Interface

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

PLACE THEM CLOSE TO CPU WITHIN 1"

for +0.9V_DDR_VTT feedback

+1.8V_SUS

R3 2K/F

R4 2K/F

CPU_M_VREF

C8 .1U_10V

C9 1000p_50V

(39) VTT_SENSE

VTT_SENSE

C677 470P_50V

R6 39.2/F

R5 39.2/F

R566 0

+0.9V_DDR_VTT

U1B

MEMVREF, VTT_SENSE, MEMZN, MEMZP

MA0_CS_L3, MA0_CS_L2, MA0_CS_L1, MA0_CS_L0

MB0_CS_L3, MB0_CS_L2, MB0_CS_L1, MB0_CS_L0

MB_CKE1, MB_CKE0, MA_CKE1, MA_CKE0

MA_ADD15 … MA_ADD0

MB_ADD15 … MB_ADD0

MA_BANK2, MA_BANK1, MA_BANK0

MB_BANK2, MB_BANK1, MB_BANK0

MA_RAS_L, MA_CAS_L, MA_WE_L

MB_RAS_L, MB_CAS_L, MB_WE_L

MA0_CLK_H2, MA0_CLK_L2, MA0_CLK_H1, MA0_CLK_L1

MB0_CLK_H2, MB0_CLK_L2, MB0_CLK_H1, MB0_CLK_L1

MB0_ODT1, MB0_ODT0, MA0_ODT1, MA0_ODT0

DDR II: CMD/CTRL/CLK

Athlon 64 S1
Processor Socket

U1C

MB_DATA63 … MB_DATA0

MB_DM7 … MB_DM0

MB_DQS_H7 … MB_DQS_L0

MA_DATA63 … MA_DATA0

MA_DM7 … MA_DM0

MA_DQS_H7 … MA_DQS_L0

To SODIMM socket B (Far)

To SODIMM socket A (near)

DDR: DATA

Athlon 64 S1
Processor Socket

+0.9V_DDR_VTT

C10 4.7U_6.3V_0603, C11 4.7U_6.3V_0603, C12 4.7U_6.3V_0603, C13 4.7U_6.3V_0603, C14 .22U_6.3V, C15 .22U_6.3V, C16 .22U_6.3V, C17 .22U_6.3V

+0.9V_DDR_VTT

C18 1000p_50V, C19 1000p_50V, C20 1000p_50V, C21 1000p_50V, C22 180P_50V, C23 180P_50V, C24 180P_50V, C25 180P_50V

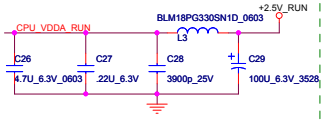
QUANTA COMPUTER

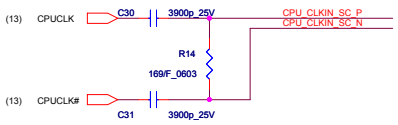
| | | |
|---|---|---|
| Title | ATHLON64 DDRII MEMORY | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 4 of 47 | |

# ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

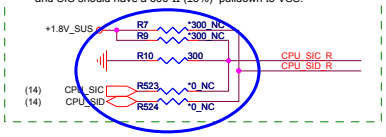
## CPU_VDDA_RUN



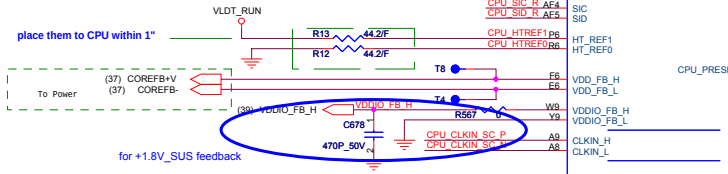

R14 close U1 within 600 mil , C30 & C31 close U1 within 1250 mil

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.

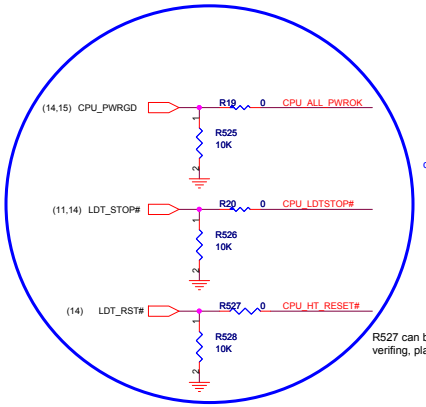



for CPU rev.F , if for rev.G , populate R7,R9,R523,R524 and depopulate R10

place them to CPU within 1"




for +1.8V_SUS feedback




change for SB600 from SB460

R527 can be used for EMI verifing, place close to CPU


add port to Page 35 U36 Thermal IC

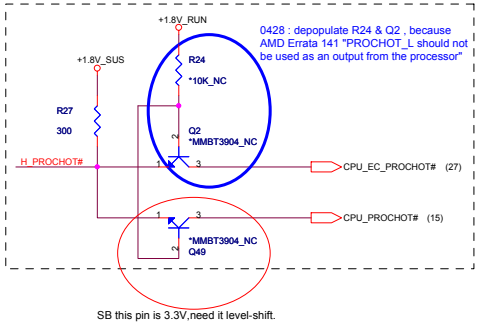



AMD NPT S1 SOCKET
Processor Socket

PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low powerstate. PSI_L should be connected to the power supply controller, if the controller supports "skipmode, or diode emulation mode". PSI_L is asserted by the processor during the C3 and S1 states.

ROUTE AS 80 Ohm DIFFERENTIAL PAIR PLACE IT CLOSE TO CPU WITHIN 1"

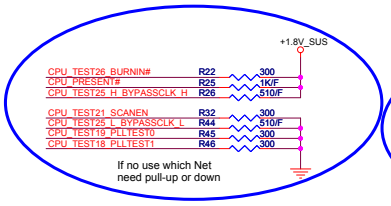
change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down




0428 : depopulate R24 & Q2 , because AMD Errata 141 "PROCHOT_L should not be used as an output from the processor"

SB this pin is 3.3V,need it level-shift.

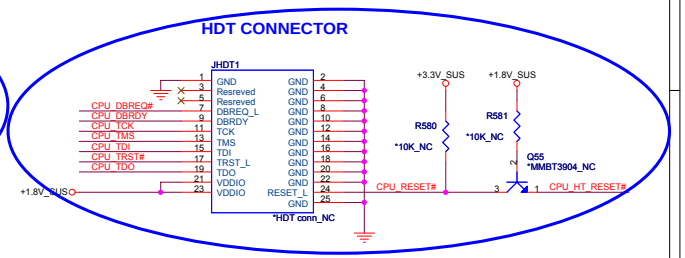
delete ED5 H_THERMTRIP# circuit




If no use which Net need pull-up or down

add HDT connector for debug convenience

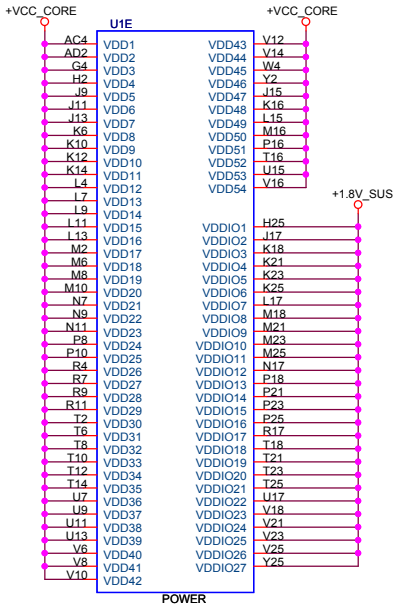
## HDT CONNECTOR

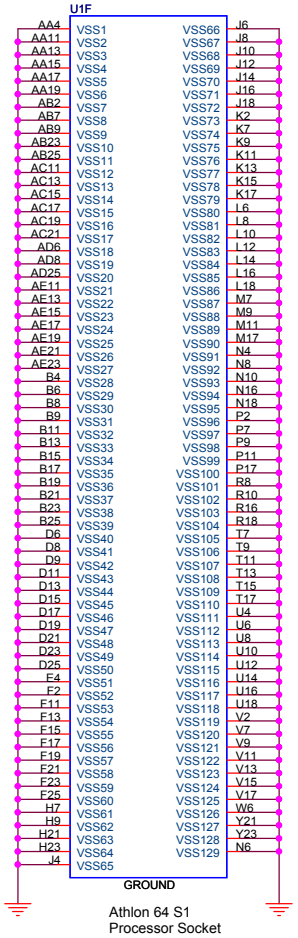


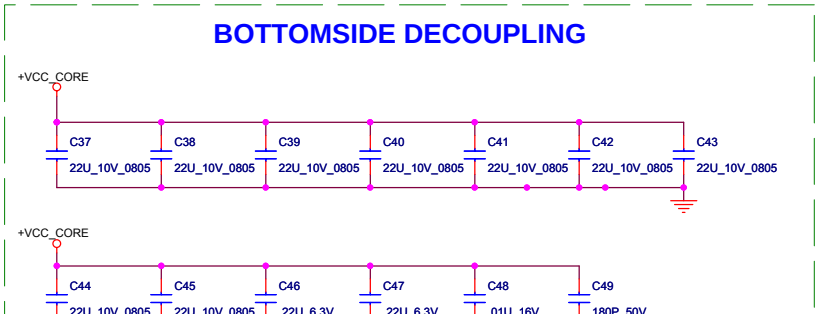

delete ED5 thermal sensor

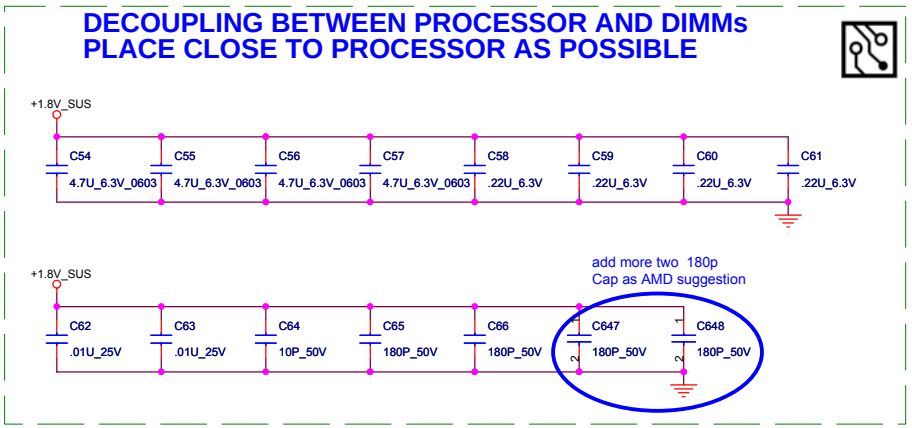
| | | | |
|---|---|---|---|
| Title | ATHLON64 CTRL & DEBUG | | |
| Size | Document Number FX2 | | Rev 1A |
| Date: Friday, May 05, 2006 | | Sheet 5 of 47 | |

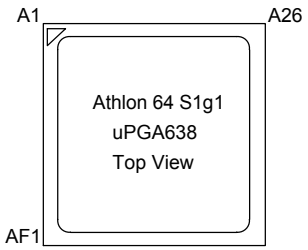
QUANTA COMPUTER



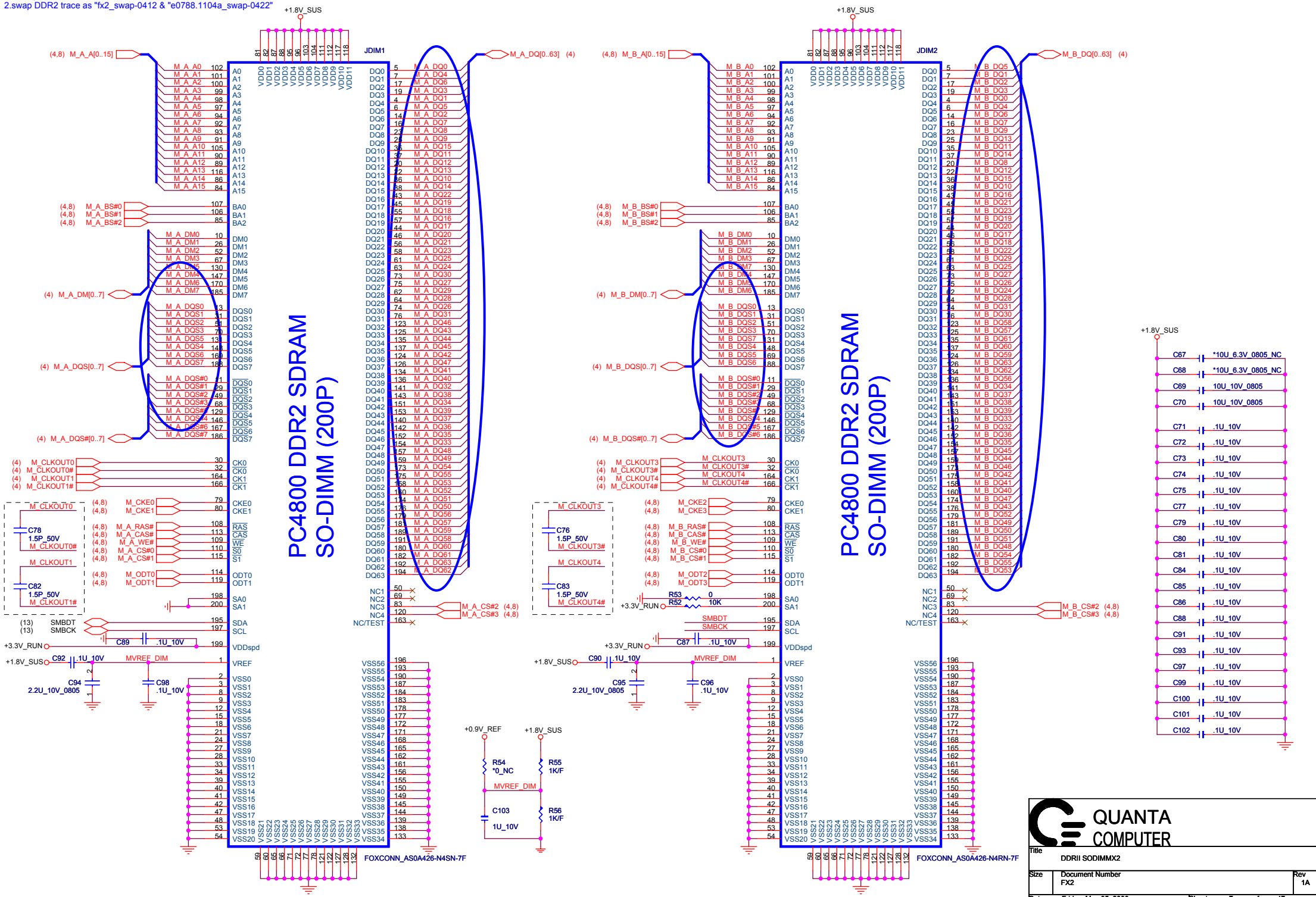




# PROCESSOR POWER AND GROUND

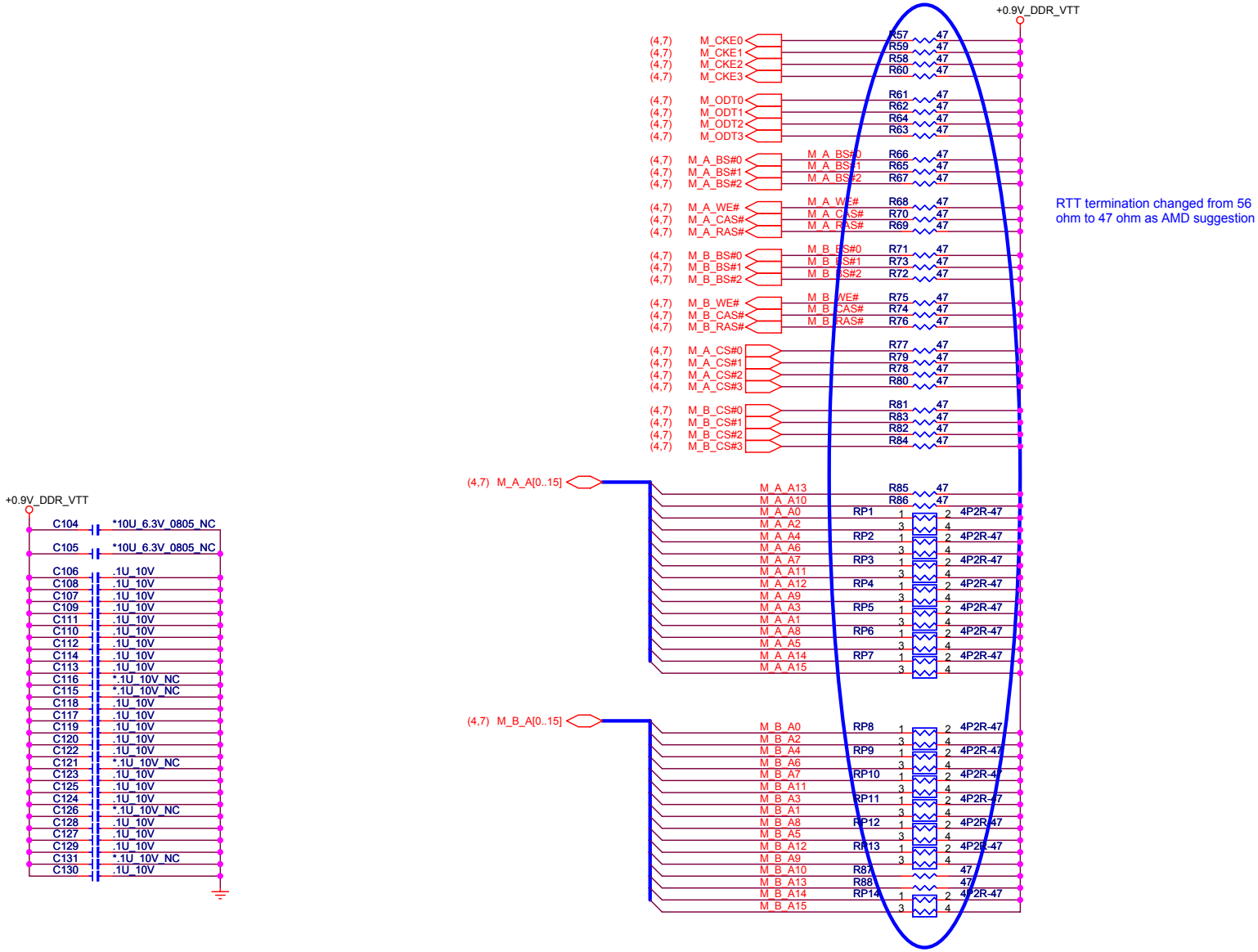
QUANTA COMPUTER

| | | |
|---|---|---|
| Title | ATHLON64 PWR & GND | |
| Size | Document Number FX2 | Rev 1A |
| Date: Thursday, May 04, 2006 | Sheet 6 of 47 | |

1.Change DDR2 socket(P/N, Description, footprint, part reference, value)
2.swap DDR2 trace as "fx2_swap-0412 & "e0788.1104a_swap-0422"

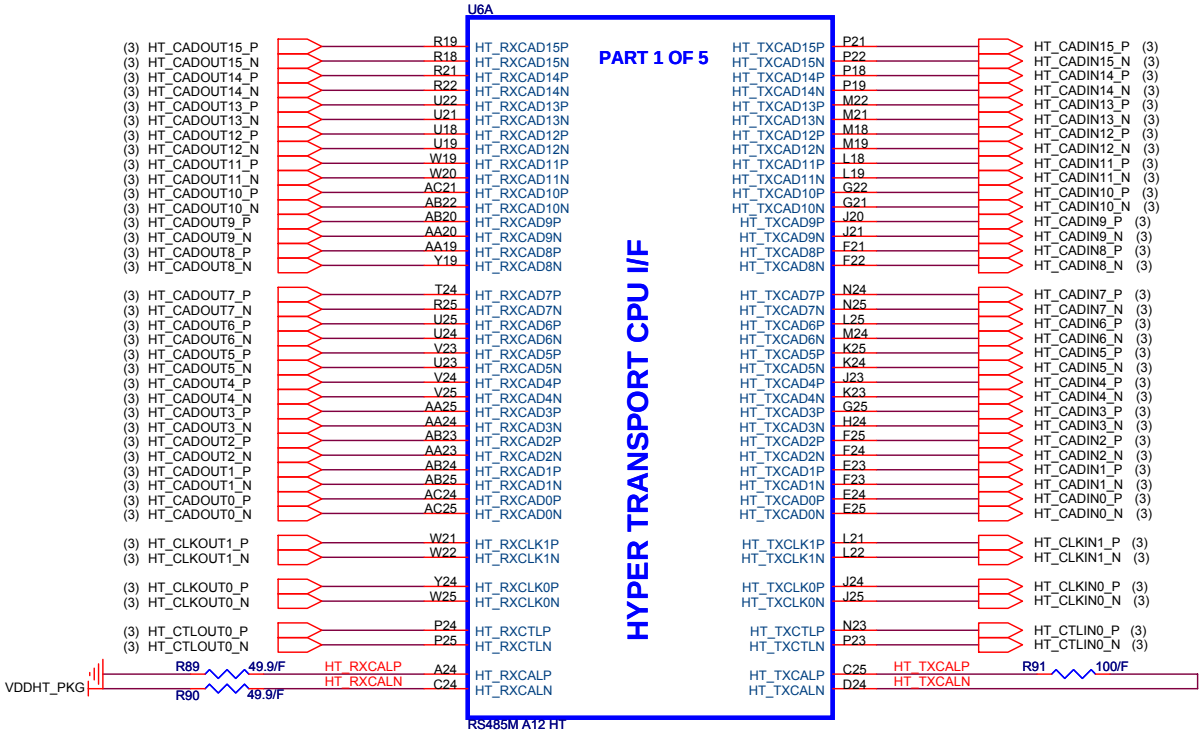



| | | |
|---|---|---|
| Title | DDRII SODIMMX2 | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 7 of 47 | |



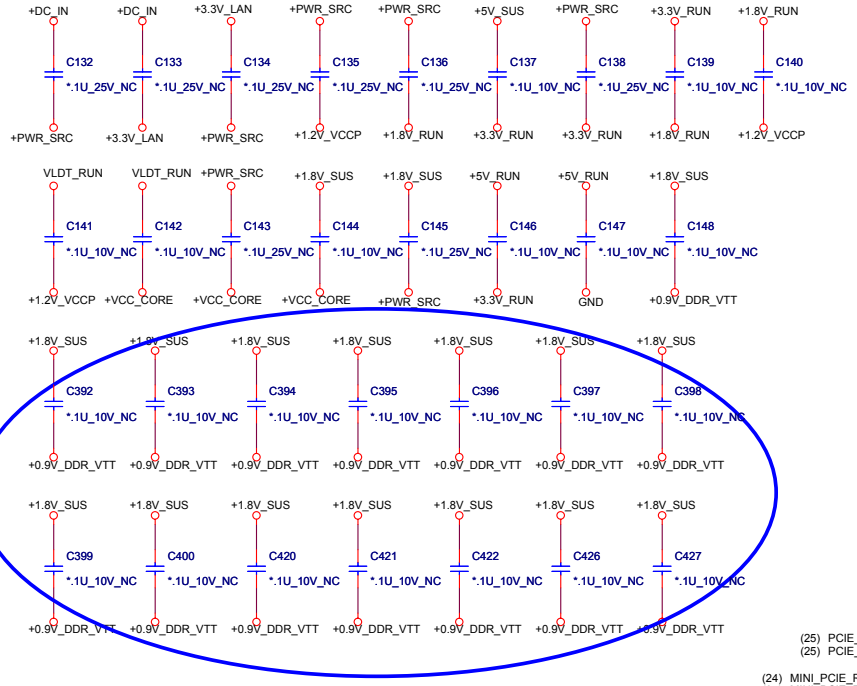

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | DDRII TERMINATION | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 8 of 47 | |

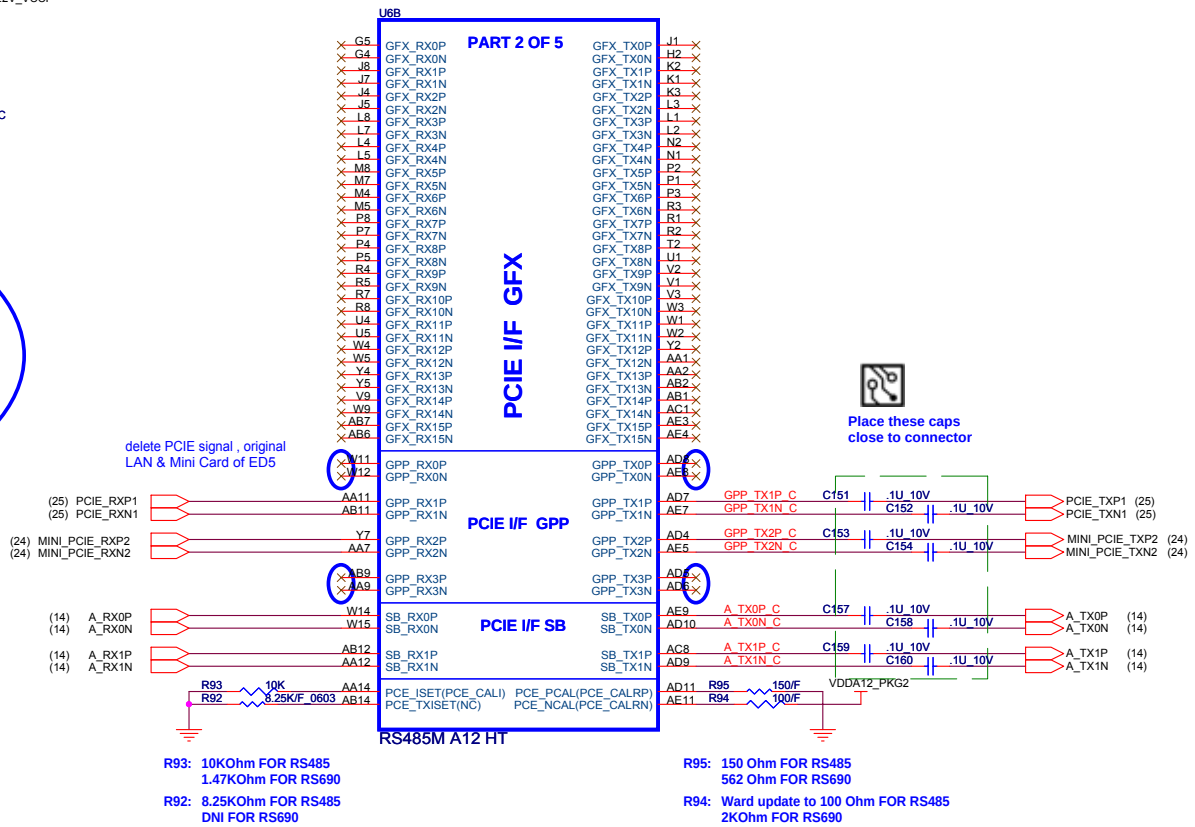



QUANTA COMPUTER

| | | |
|---|---|---|
| Title | RS485-HT LINK0 I/F | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 9 of 47 | |




reserve more 14 Cap. between +0.9V_DDR_VTT & +1.8V_SUS




**R93: 10KOhm FOR RS485**
**1.47KOhm FOR RS690**

**R92: 8.25KOhm FOR RS485**
**DNI FOR RS690**

**R95: 150 Ohm FOR RS485**
**562 Ohm FOR RS690**

**R94: Ward update to 100 Ohm FOR RS485**
**2KOhm FOR RS690**

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | RS485-PCIE LINK I/F | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 10 of 47 | |

+1.8V_RUN L4 — BK1608HS600 — HTPVDD — C161 10U_10V — C162 4.7U_6.3V

+1.8V_RUN L5 — BK1608HS600 — AVDDQ — C163 10U_10V — C164 2.2U_10V

+3.3V_RUN L6 — BK1608HS600 — AVDD_NB — C165 4.7U_6.3V — C166 .1U_10V

+1.8V_RUN — R96 0_0603 — AVDD1 — C167 2.2U_10V

+1.8V_RUN L7 — BK1608HS600 — PLLVDD — C168 10U_10V — C169 4.7U_6.3V

added as FM1 application for ED5

+3.3V_RUN — RP15 4P2R-2.2K — Q7 2N7002W-7-F — DDCDAT — DAT_DDC2 (19)

+3.3V_RUN — Q8 2N7002W-7-F — DDCCLK — CLK_DDC2 (19)

+1.8V_RUN +3.3V_RUN — R110 10K — R111 10K — LDT_STOP# NB

(5,14) LDT_STOP# — Q9 MMBT3904

close to NB

(19) VGA_RED — R104 150/F
(19) VGA_GRN — R105 150/F
(19) VGA_BLU — R106 150/F

deleted caused by Svideo defeature

external trace become to internal trace

U6C

AVDD_NB — B22 AVDD1, C22 AVDD2
AVDD1 — G17 AVSSN1, H17 AVSSN2, A20 AVDDDI, B20 AVSSDI
AVDDQ — A21 AVDDQ, A22 AVSSQ
C171 .1U_10V

C_R — 139
Y_G — 140
COMP_B — 141

CRT/TVOUT:
RED — C21
GREEN — C20
BLUE — D19
DACVSYNC — A5
DACHSYNC — C6
RSET — B21 (715/F R107)
DACSCL — B6
DACSDA — A6

(19) VSYNC
(19) HSYNC
DDCCLK R108 0
DDCDAT R101 0

PLLVDD — A10 PLLVDD(PLLVDD18), B10 PLLVSS
HTPVDD — B24 HTPVDD, B25 HTPVSS

PWR MGT:
(14,23,24,25,33) ALINK_RST#
(27) NB_PWRGD
R109 0 NB_RST# — C10 SYSRESET#
C11 POWERGOOD
R102 0 LDT_STOP# NB — C5 LDTSTOP#
(14) ALLOW_LDTSTOP — B5 ALLOW_LDTSTOP

CLOCKs:
R112 10K — C23 HTTSTCLK
(13) HTREFCLK — B23 HTREFCLK
TV_SWITCH — C2 TVCLKIN
R124 10K
(13) NB_OSC — B11 OSCIN
T50 — A11 OSCOUT(PLLVDD12)
PLLVDD12

(13) NBSRC_CLKP — F2 GFX_CLKP
(13) NBSRC_CLKN — F1 GFX_CLKN
(13) SBLINK_CLKP — G1 SB_CLKP
(13) SBLINK_CLKN — G2 SB_CLKN

MIS.:
R116 *3K_NC by default — LOAD_ROM#
R115 *2.7K_NC DFT_GPIO0 — D6 DFT_GPIO0
R118 *2.7K_NC DFT_GPIO2 — C8 DFT_GPIO2
R120 *2.7K_NC DFT_GPIO3 — C7 DFT_GPIO3
R119 *2.7K_NC DFT_GPIO4 — B8 DFT_GPIO4
R121 *2.7K_NC DFT_GPIO5 — A8 DFT_GPIO5
D1 RB751
(14) BMREQ# — B2 BMREQb
(18) PHL_CLK — A2 I2C_CLK
(18) PHL_DATA — B4 I2C_DATA
R583 *0_NC — AA15 THERMALDIODE_P
R584 *0_NC — AB15 THERMALDIODE_N
(16) SB_NB_THRMDA
(16) SB_NB_THRMDC
T65 — C14 TMDS_HPD
T68 — B3 DDC_DATA
C3 TESTMODE
+3.3V_RUN — R123 2K/F — STRP_DATA — A3 STRP_DATA
R126 4.7K/F

PART 3 OF 5

LVDS:
TXOUT_L0P — B14 — TXLOUT0+ (18)
TXOUT_L0N — B15 — TXLOUT0- (18)
TXOUT_L1P — B13 — TXLOUT1+ (18)
TXOUT_L1N — A13 — TXLOUT1- (18)
TXOUT_L2P — H14 — TXLOUT2+ (18)
TXOUT_L2N — G14 — TXLOUT2- (18)
TXOUT_L3P — D17 — T47
TXOUT_L3N — E17 — T48

ED5 is single ch , change to dual ch as FM1

TXOUT_U0P — A15 — TXUOUT0+ (18)
TXOUT_U0N — B16 — TXUOUT0- (18)
TXOUT_U1P — C17 — TXUOUT1+ (18)
TXOUT_U1N — C18 — TXUOUT1- (18)
TXOUT_U2P — B17 — TXUOUT2+ (18)
TXOUT_U2N — A17 — TXUOUT2- (18)
TXOUT_U3P — A18 — T49
TXOUT_U3N — B18 — T46

TXCLK_LP — E15 — TXLCLKOUT+ (18)
TXCLK_LN — D15 — TXLCLKOUT- (18)
TXCLK_UP — H15 — TXUCLKOUT+ (18)
TXCLK_UN — G15 — TXUCLKOUT- (18)

LPVDD — D14
LPVSS — E14
C172 .1U_10V — C170 4.7U_6.3V

RS485: LVDDR18A=1.8V

CHECK TO 2200HM

L8 BK1608HS600 — +1.8V_RUN
L10 BK1608HS600 — L9 BK1608HS600

LVDDR18D_1 — A12
LVDDR18D_2 — B12
LVDDR18A_1 — C12
LVDDR18A_2 — C13

LVSSR1 — A16
LVSSR3 — A14
LVSSR5 — D12
LVSSR6 — C19
LVSSR7 — C15
LVSSR8 — C16
C173 .1U_10V — C174 4.7U_6.3V
C175 .1U_10V — C176 4.7U_6.3V
LVSSR12 — F14
LVSSR13 — F15

LVDS_DIGON — E12 — LCD_PON — R114 0 — LCD_POWER_ON (18)
LVDS_BLON — G12 — LVDS_BLEN
LVDS_BLEN — F12 — T146

DVO:
DVO_D0(GPP_TX4P) — AD14 — T51
DVO_D1(GPP_TX4N) — AD15 — T52
DVO_D2(NC) — AE15 — T54
DVO_D3(GPP_RX4P) — AD16 — T53
DVO_D4(GPP_RX4N) — AE16 — T55
DVO_D5(NC) — AC17 — T57
DVO_D6(NC) — AD18 — T56
DVO_D7(GPP_TX5N) — AE19 — T58
DVO_D8(GPP_TX5P) — AD19 — T59
DVO_D9(GPP_RX5N) — AE20 — T60
DVO_D10(GPP_RX5P) — AD20 — T64
DVO_D11(NC) — AE21 — T63

DVO_VSYNC(NC) — AD13 — T67
DVO_DE(NC) — AC13 — T66
DVO_HSYNC(NC) — AE13 — T69
DVO_IDCKP(NC) — AE17 — T71
DVO_IDCKN(NC) — AD17 — T70

RS485M A12 HT

R125 2K/F — LCD_PON
R127 2K/F — LVDS_BLON
R128 2K/F — LVDS_BLEN

LOAD_ROM#: LOAD ROM STRAP ENABLE

High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE

0428 : reserve for NB thermal Diode

reserve 0 ohm to connect "LVDS_BLON" to LCD conn directly

R129 0_NC — +3.3V_RUN — LVDS_BLON — U40 NC7SZ08P5X_NL
(27) FPBACK_EN — R591 100K — NB_PWRGD — U7 NC7SZ08P5X_NL
R130 0 — BLON (18)

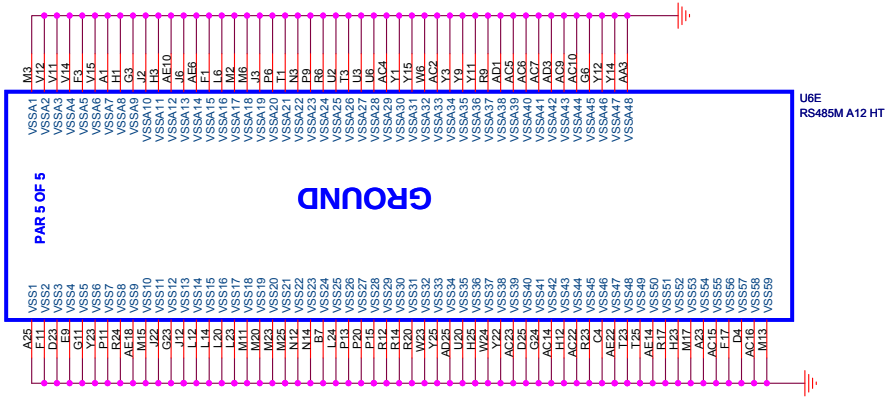
0504 : change "FPBACK_EN" from connected with "LVDS_BLEN" directly to connected with "LVDS_BLON" by a AND gate

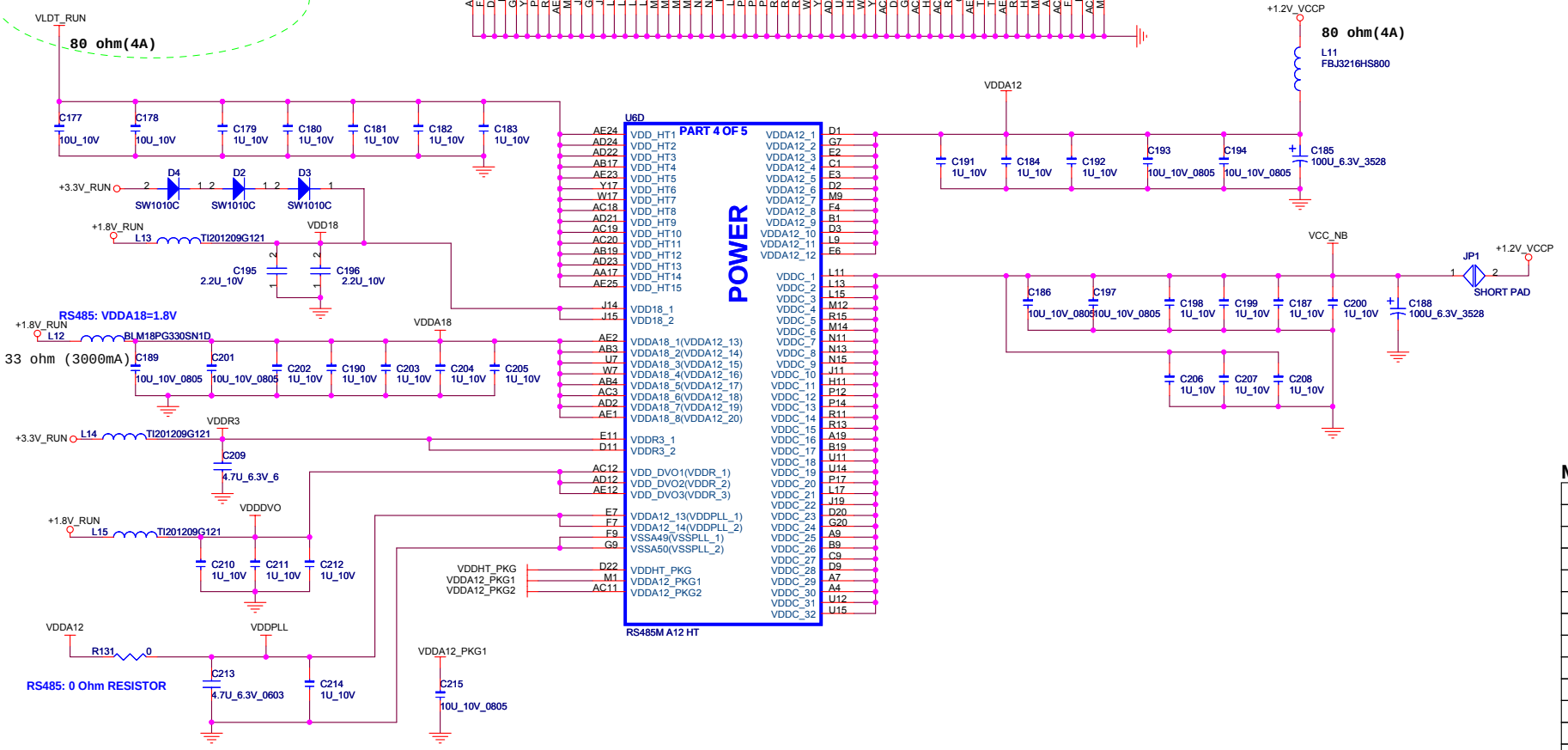
| | RS485 | RS690 |
|---|---|---|
| OSCOUT(A11) | OSCOUT | PLLVDD12 |
| DVO_D0(AD14) | DVO_D0 | GPP_TX4P |
| DVO_D1(AD15) | DVO_D1 | GPP_TX4N |
| DVO_D3(AD16) | DVO_D3 | GPP_RX4P |
| DVO_D4(AE16) | DVO_D4 | GPP_RX4N |
| DVO_D7(AE19) | DVO_D7 | GPP_TX5N |
| DVO_D8(AD19) | DVO_D8 | GPP_TX5P |
| DVO_D9(AE20) | DVO_D9 | GPP_RX5N |
| DVO_D10(AD20) | DVO_D10 | GPP_RX5P |

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | RS485-LVDS | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 11 of 47 | |

SUGGEST REMOVE L11 BEAD SAME AS CPU
1.2 PLAN FSB UNDER THIS PLAN



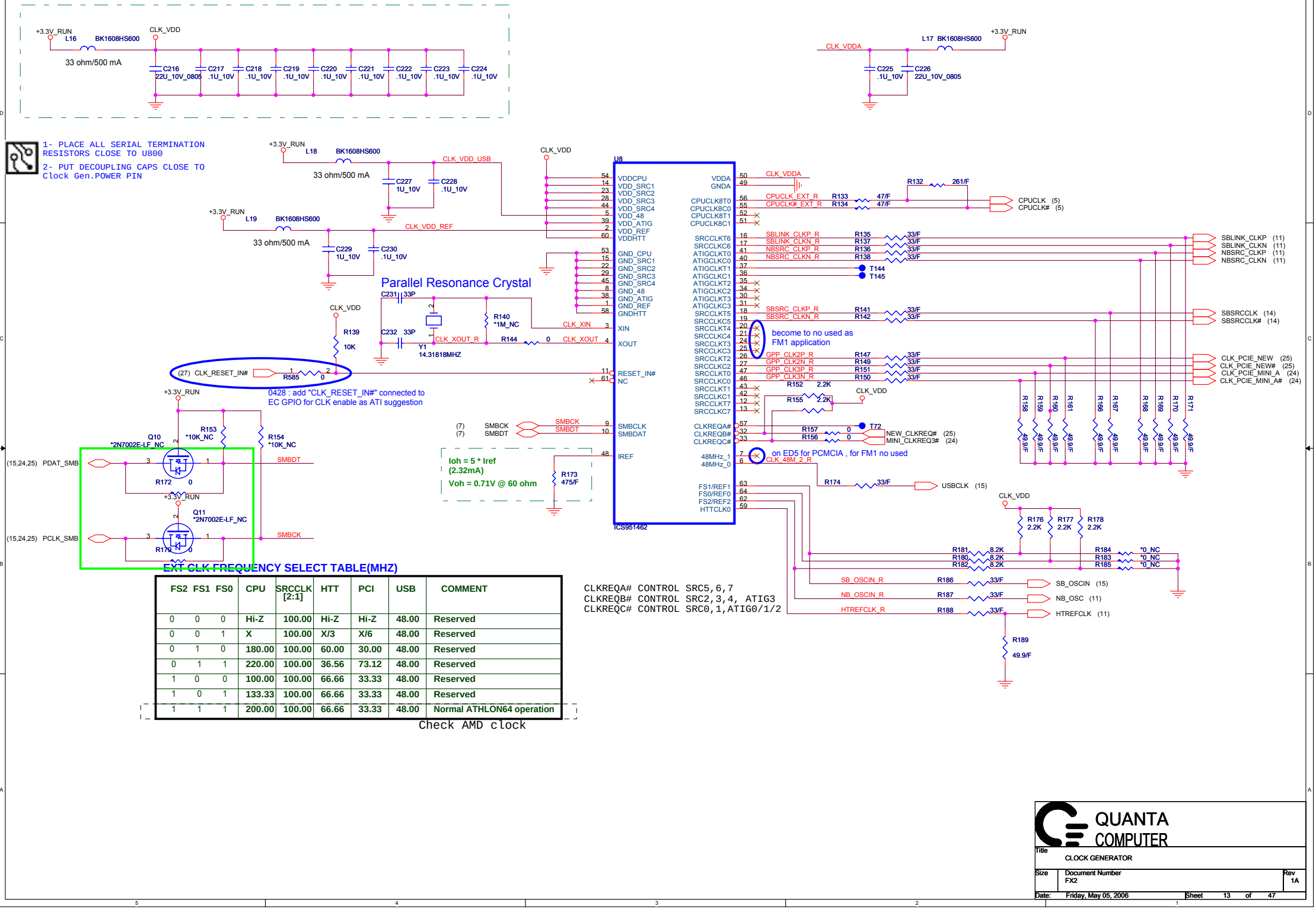




## NB RS485 POWER STATES

| Power Signal | S0 | S1 | S3 | S4/S5 | G3 |
|---|---|---|---|---|---|
| VDDHT | ON | ON | OFF | OFF | OFF |
| VDDR | ON | ON | OFF | OFF | OFF |
| VDD18 | ON | ON | OFF | OFF | OFF |
| VDDC | ON | ON | OFF | OFF | OFF |
| VDDA18 | ON | ON | OFF | OFF | OFF |
| VDDA12 | ON | ON | OFF | OFF | OFF |
| AVDD | ON | ON | OFF | OFF | OFF |
| AVDDDI | ON | ON | OFF | OFF | OFF |
| PLLVDD | ON | ON | OFF | OFF | OFF |
| HTPVDD | ON | ON | OFF | OFF | OFF |
| VDDR3 | ON | ON | OFF | OFF | OFF |
| LPVDD | ON | ON | OFF | OFF | OFF |
| LVDDR18D | ON | ON | OFF | OFF | OFF |
| LVDDR18A | ON | ON | OFF | OFF | OFF |

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | RS485-POWER | |
| Size | Document Number FX2 | Rev 1A |
| Date: Thursday, May 04, 2006 | Sheet 12 of 47 | |




## EXT CLK FREQUENCY SELECT TABLE(MHZ)

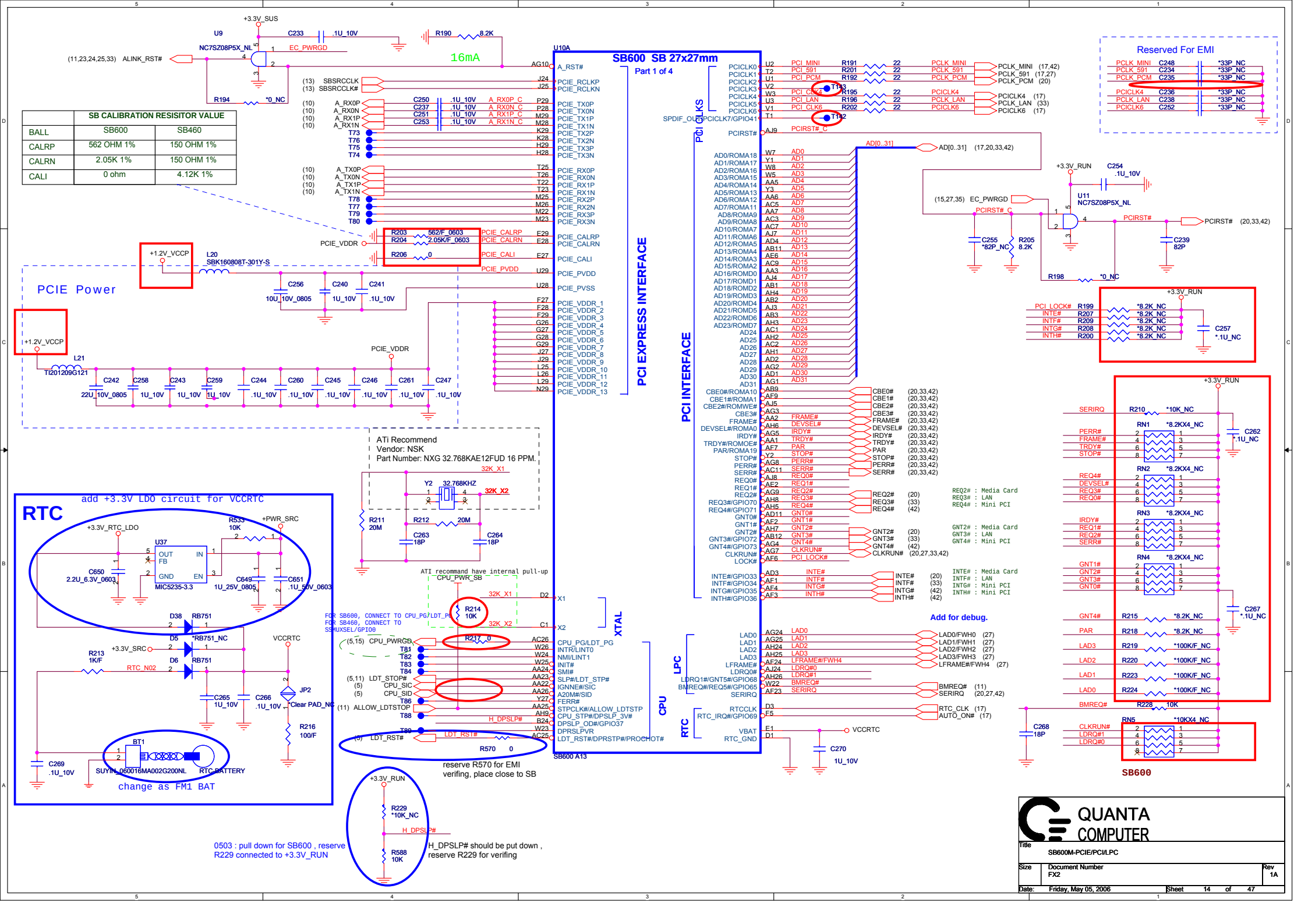
| FS2 | FS1 | FS0 | CPU | SRCCLK [2:1] | HTT | PCI | USB | COMMENT |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Hi-Z | 100.00 | Hi-Z | Hi-Z | 48.00 | Reserved |
| 0 | 0 | 1 | X | 100.00 | X/3 | X/6 | 48.00 | Reserved |
| 0 | 1 | 0 | 180.00 | 100.00 | 60.00 | 30.00 | 48.00 | Reserved |
| 0 | 1 | 1 | 220.00 | 100.00 | 36.56 | 73.12 | 48.00 | Reserved |
| 1 | 0 | 0 | 100.00 | 100.00 | 66.66 | 33.33 | 48.00 | Reserved |
| 1 | 0 | 1 | 133.33 | 100.00 | 66.66 | 33.33 | 48.00 | Reserved |
| 1 | 1 | 1 | 200.00 | 100.00 | 66.66 | 33.33 | 48.00 | Normal ATHLON64 operation |

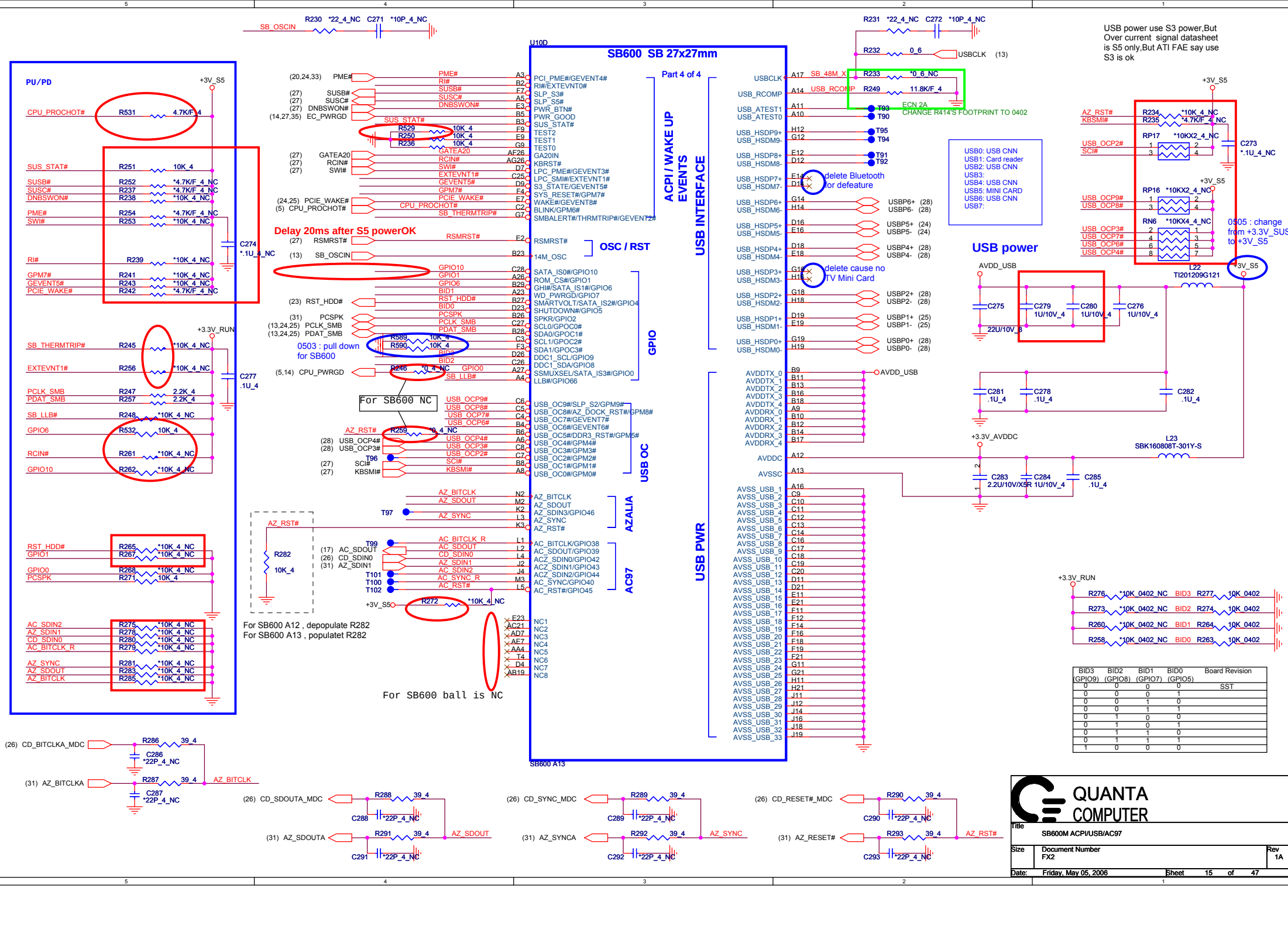
CLKREQA# CONTROL SRC5,6,7
CLKREQB# CONTROL SRC2,3,4, ATIG3
CLKREQC# CONTROL SRC0,1,ATIG0/1/2

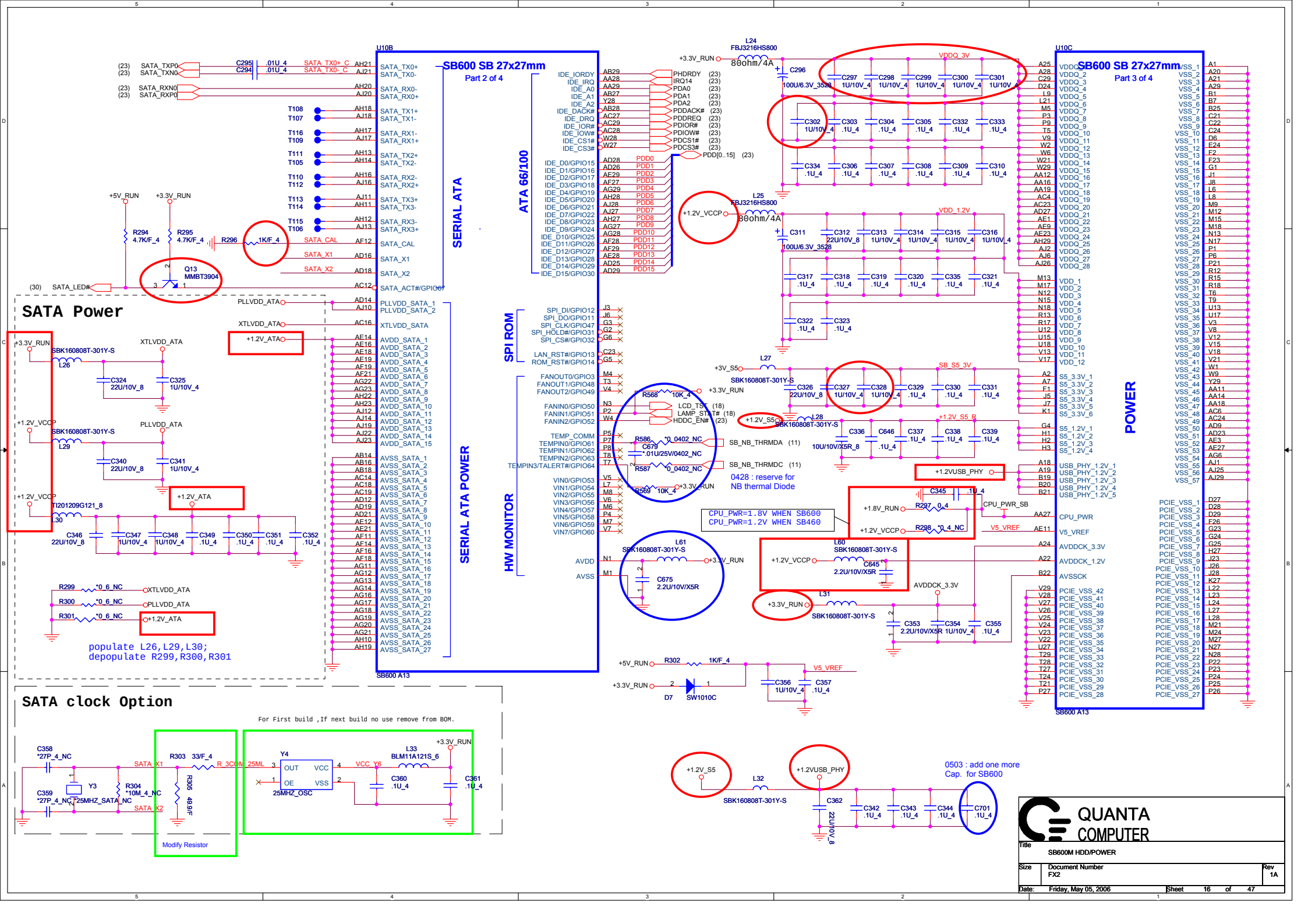
Check AMD clock

QUANTA COMPUTER

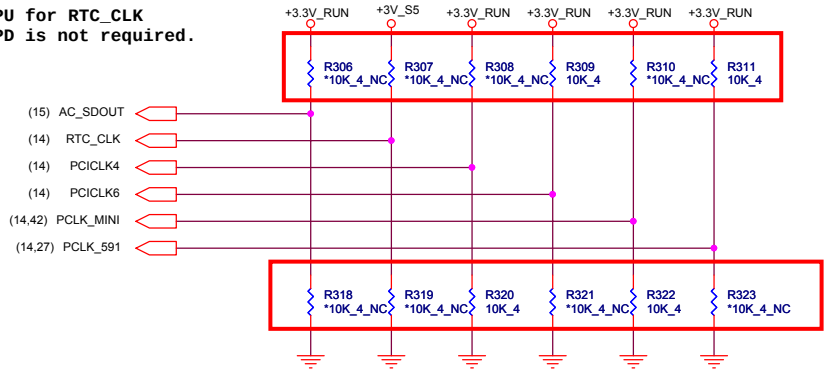
| | | |
|---|---|---|
| Title | CLOCK GENERATOR | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 13 of 47 | |


SB600 SB 27x27mm
Part 1 of 4
U10A
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
XTAL
CPU
LPC
RTC
SB600 A13
PCIE Power
RTC
add +3.3V LDO circuit for VCCRTC
change as FM1 BAT
ATi Recommend
Vendor: NSK
Part Number: NXG 32.768KAE12FUD 16 PPM.
ATI recommand have internal pull-up
reserve R570 for EMI
verifing, place close to SB
0503 : pull down for SB600 , reserve
R229 connected to +3.3V_RUN
H_DPSLP# should be put down ,
reserve R229 for verifing
Add for debug.
Reserved For EMI
SB600
SB CALIBRATION RESISITOR VALUE
BALL | SB600 | SB460
CALRP | 562 OHM 1% | 150 OHM 1%
CALRN | 2.05K 1% | 150 OHM 1%
CALI | 0 ohm | 4.12K 1%
QUANTA COMPUTER
Title: SB600M-PCIE/PCI/LPC
Size: Document Number: FX2
Rev: 1A
Date: Friday, May 05, 2006
Sheet 14 of 47


SB600 SB 27x27mm
U10D
Part 4 of 4
SB600 A13
PU/PD
ACPI / WAKE UP EVENTS
USB INTERFACE
OSC / RST
GPIO
USB OC
AZALIA
AC97
USB PWR
USB power
Delay 20ms after S5 powerOK
For SB600 NC
For SB600 A12 , depopulate R282
For SB600 A13 , populatet R282
For SB600 ball is NC
0503 : pull down for SB600
USB power use S3 power,But Over current signal datasheet is S5 only,But ATI FAE say use S3 is ok
delete Bluetooth for defeature
delete cause no TV Mini Card
USB0: USB CNN
USB1: Card reader
USB2: USB CNN
USB3:
USB4: USB CNN
USB5: MINI CARD
USB6: USB CNN
USB7:
ECN 2A
CHANGE R414'S FOOTPRINT TO 0402
0505 : change from +3.3V_SUS to +3V_S5
QUANTA COMPUTER
SB600M ACPI/USB/AC97
FX2
1A
Friday, May 05, 2006
15 of 47


SB600 SB 27x27mm
Part 2 of 4
SB600 SB 27x27mm
Part 3 of 4
SERIAL ATA
ATA 66/100
SPI ROM
HW MONITOR
SERIAL ATA POWER
POWER
SATA Power
SATA clock Option
populate L26,L29,L30;
depopulate R299,R300,R301
CPU_PWR=1.8V WHEN SB600
CPU_PWR=1.2V WHEN SB460
0428 : reserve for
NB thermal Diode
0503 : add one more
Cap. for SB600
For First build ,If next build no use remove from BOM.
Modify Resistor
SB600 A13
QUANTA
COMPUTER
SB600M HDD/POWER
Friday, May 05, 2006
16 of 47

SB600 has 15K internal PD for AC_SDOUT
15K internal PU for RTC_CLK
,External PU/PD is not required.

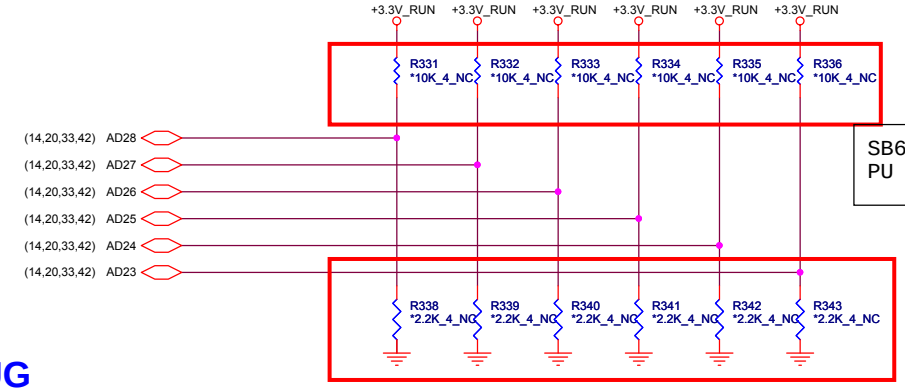




delete SB460 setting

## REQUIRED STRAPS

| | AC_SDOUT | RTC_CLK | PCI_CLK4 | PCI_CLK6 | PCLK_MINI PCLK_591<br>PCI_CLK0 PCI_CLK1 |
|---|---|---|---|---|---|
| PULL HIGH | USE DEBUG STRAPS | INTERNAL RTC<br>DEFAULT | USE INT. PLL48<br>DEFAULT | CPU IF=K8<br>DEFAULT | H, H = PCI ROM<br>H, L = SPI ROM<br>L, H = LPC ROM DEFAULT<br>L, L = FWH ROM |
| PULL LOW | IGNORE DEBUG STRAPS<br>DEFAULT | EXTERNAL RTC | USE EXT. 48MHZ | CPU IF=P4 | |



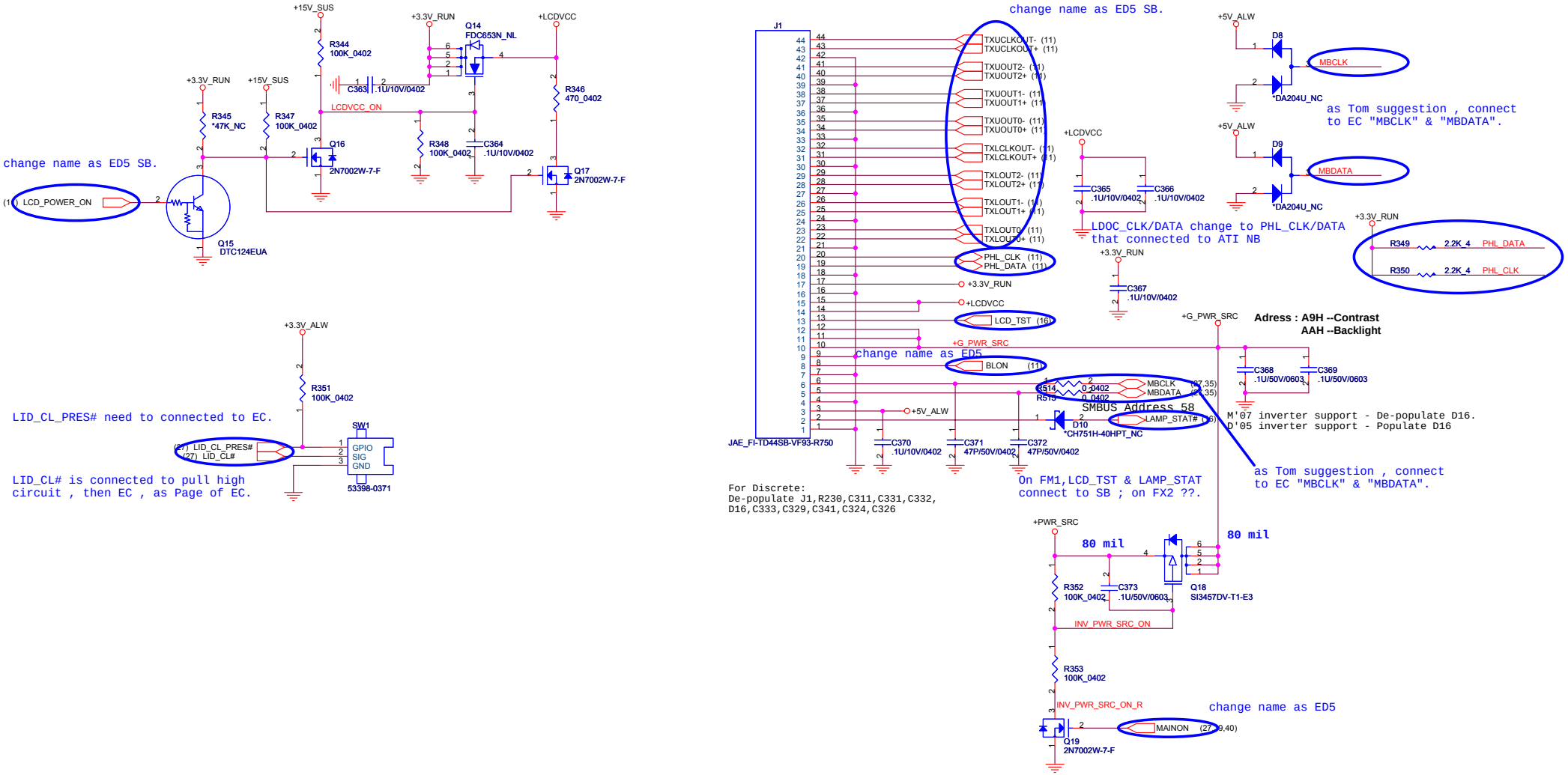

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

## DEBUG STRAPS

| | PDACK# | PCI_AD28 | PCI_AD27 | PCI_AD26 | PCI_AD25 | PCI_AD24 | PCI_AD23 |
|---|---|---|---|---|---|---|---|
| PULL HIGH | USE LONG RESET<br>DEFAULT | Use Long Reset<br>DEFAULT | USE PCI PLL<br>DEFAULT | USE ACPI BCLK<br>DEFAULT | USE IDE PLL<br>DEFAULT | USE DEFAULT PCIE STRAPS<br>DEFAULT | boot fail time disabled<br>DEFAULT |
| PULL LOW | USE SHORT RESET | Use Short Reset | BYPASS PCI PLL | BYPASS ACPI BCLK | BYPASS IDE PLL | USE EEPROM PCIE STRAPS | boot fail time enabled |
| | SB460 Only | SB600 Only | | | | | SB600 Only |

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | SB600M STRAPS | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 17 of 47 | |

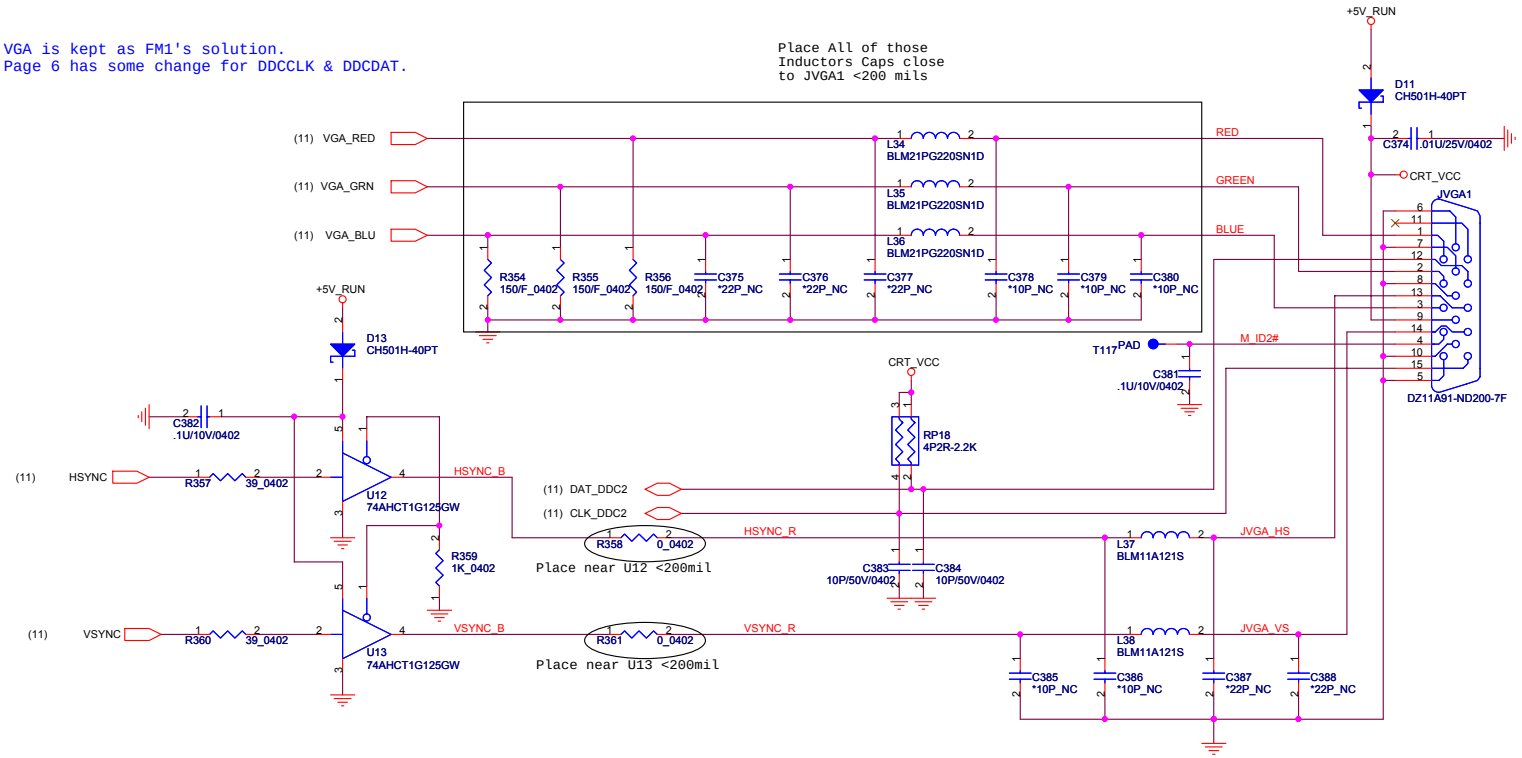



QUANTA COMPUTER

| | | |
|---|---|---|
| Title | LCD CONN | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 18 of 47 | |

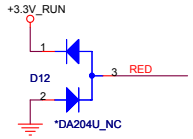
VGA is kept as FM1's solution.
Page 6 has some change for DDCCLK & DDCDAT.

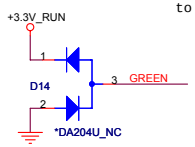
Place All of those
Inductors Caps close
to JVGA1 <200 mils

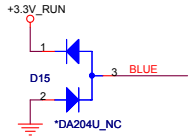



Place near U12 <200mil

Place near U13 <200mil

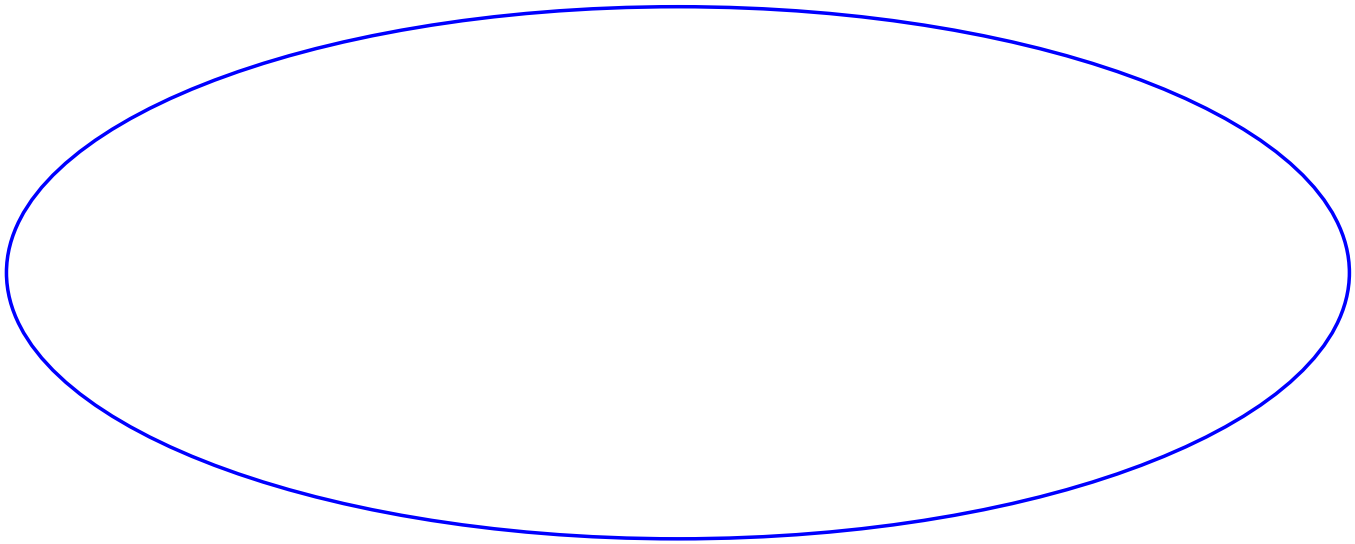



Place D4,D5,D6 close
to JVGA1 <200 mils

delete Svideo for defeature



QUANTA COMPUTER

| | | |
|---|---|---|
| Title | CRT | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 19 of 47 | |

change name for ED5
copy ED5 to FX2
Waiting to check

+3.3V_R5C832
C401 10U/10V/0805
C402 .01U/25V/0402
C403 .01U/25V/0402
C404 .01U/25V/0402
C405 .01U/25V/0402
C406 .01U/25V/0402
C407 10U/10V/0805
C408 .01U/25V/0402
C409 .1U/10V/0402
C410 .01U/25V/0402
Place the power caps close to the relation pins.
C413 .01U/25V/0402
C414 .01U/25V/0402
C415 .47U/10V/0603
C416 .47U/10V/0603
U15B
VCC_PCI1 10
VCC_PCI2 20
VCC_PCI3 27
VCC_PCI4 32
VCC_PCI5 41
VCC_PCI6 128
VCC_RIN 61
VCC_ROUT1 16
VCC_ROUT2 34
VCC_ROUT3 64
VCC_ROUT4 114
VCC_ROUT5 120
VCC_3V 67
VCC_MD 86
Place the power caps close to the relation pins.
C411 .01U/25V/0402
C412 10U/10V/0805
+3.3V_RUN
+3.3V_R5C832
R371 0_0805
(14,17,33,42) AD[0..31]
PCI Bus
PowerOnReset for VccCore
Route GBRST# to GPIOG3 (pin 91) of the SIO companion chip ECE5011, and name the signal CBUS_GRST#. If CBUS_GRST# is controlled by the sysem, then C850 does not need to apply.
If R374 is populated, both C417 and R372 can be depop.
R372 100K_0402
(27) CBUS_GRST#
R374 *0_NC
C417 1U/10V/0603
GBRST# should be asserted only when system power supply is on.
AD31 125
AD30 126
AD29 127
AD28 1
AD27 2
AD26 3
AD25 5
AD24 6
AD23 9
AD22 11
AD21 12
AD20 14
AD19 15
AD18 17
AD17 18
AD16 19
AD15 36
AD14 37
AD13 38
AD12 39
AD11 40
AD10 42
AD9 43
AD8 44
AD7 46
AD6 47
AD5 48
AD4 49
AD3 50
AD2 51
AD1 52
AD0 53
PAR 33
C/BE3# 7
C/BE2# 21
C/BE1# 35
C/BE0# 45
IDSEL 8
REQ# 124
GNT# 123
FRAME# 23
IRDY# 24
TRDY# 25
DEVSEL# 26
STOP# 29
PERR# 30
SERR# 31
GBRST# 71
PCIRST# 119
PCICLK 121
PME# 70
CLKRUN# 117
PCI / OTHER
R5C832T_V00
GND1 4
GND2 13
GND3 22
GND4 28
GND5 54
GND6 62
GND7 63
GND8 68
GND9 118
GND10 122
AGND1 99
AGND2 102
AGND3 103
AGND4 107
AGND5 111
R373 10K_0402
Route to GPIOG6 (pin 94) on the SIO companion chip ECE5011, with the signal named CB_HWSPND#
HWSPND# 69
R375 *0_NC
CB_HWSPND# (27)
R517 10K_0402
pull down to disable MS & XD
MSEN 58
XDEN 55
UDIO5 57
UDIO3 65
UDIO4 59
UDIO2 56
UDIO1 60
UDIO0/SRIRQ# 72
R376 10K_0402
R377 100K_0402
Memory Stick disable
XD Card disable
Serial ROM disable
SD Card Enable
MMC Card Enable
SERIRQ (14,27,42)
Waiting to check LINK SB460 SERIRQ PIN PCLK_PCM
PCI Bus
R559 10K_0402
INTA# 115
INTB# 116
INTE# (14)
1394 Interrupt
Media card Interrupt
TEST 66
T118 PAD
R380 100K_0402
Waiting to check LINK SB460 PCI CLKS PIN PCLK_PCM
PCI Bus
(14,33,42) PAR
(14,33,42) CBE3#
(14,33,42) CBE2#
(14,33,42) CBE1#
(14,33,42) CBE0#
AD17
R378 100_0402
(14) REQ2#
(14) GNT2#
(14,33,42) FRAME#
(14,33,42) IRDY#
(14,33,42) TRDY#
(14,33,42) DEVSEL#
(14,33,42) STOP#
(14,33,42) PERR#
(14,33,42) SERR#
(14,33,42) PCIRST#
(14) PCLK_PCM
as ED5 application
+3.3V_RUN
Q43 *DTC144EUA_NC
(15,24,33) PME#
R379 *0_NC
(14,27,33,42) CLKRUN#
CoreLogic CLOCKRUN#
The ICH schematics need to include a pull-up resistor to implement CLKRUN#, and the ICH schematics must have a pull-down, or constantly drive thesignal low, in order to disable CLKRUN#.
PCLK_PCM
R381 *10_NC
C418 *10P_NC
Refer to DELL M07 schematic X06

QUANTA COMPUTER
Title: 5C832/PCI
Size: Document Number: FX2
Rev: 1A
Date: Friday, May 05, 2006
Sheet 20 of 47

deleted 1394 for defeature

3.AVCC_PHY3V, connection with +3.3V_R5C832 power
4.AVCC_PHY3V, Inductor Required between +3.3V_R5C832 and AVCC_PHY

80 mils

+3.3V_R5C832

+3.3V_RUN_PHY

C423 10U/10V/0805

C424 .1U/10V/0402

C419 .01U/25V/0402

C425 1000P/50V/0402

L43 BLM18PG181SN1D

modify

U15A

Place these caps as close to the U15 as possible.

AVCC_PHY1 98
AVCC_PHY2 106
AVCC_PHY3 110
AVCC_PHY4 112

TPBIAS0 113

94 XI
95 XO
96 FIL0
101 REXT
100 VREF

5.TPBN1 & TPBP1, Short to GND
if the 1394 Port Is Not Used

TPBN0 104
TPBP0 105

TPAN0 108
TPAP0 109

IEEE1394/SD

MDIO17 87
MDIO16 92
MDIO15 89
MDIO14 91
MDIO13 90 SD/XD/MS_DATA3 SD/XD/MS_DATA3 (22)
MDIO12 93 SD/XD/MS_DATA2 SD/XD/MS_DATA2 (22)
MDIO11 81 SD/XD/MS_DATA1 SD/XD/MS_DATA1 (22)
MDIO10 82 SD/XD/MS_DATA0 SD/XD/MS_DATA0 (22)

MDIO05 75
MDIO08 88 SD/XD/MS_CMD SD/XD/MS_CMD (22)
MDIO19 83
MDIO18 85
MDIO02 78

changed for SD/MMC/SDIO only

MDIO03 77 SD_WP#(XDR/B#) SD_WP#(XDR/B#) (22)
MDIO00 80 SD_CD# SD_CD# (22)

MDIO01 79
MDIO09 84 SD/XD/MS_CLK (22)
MDIO04 76 MC_PWR_CTRL_0 (22)
MDIO06 74 T119 PAD

97 RSV

MDIO07 73

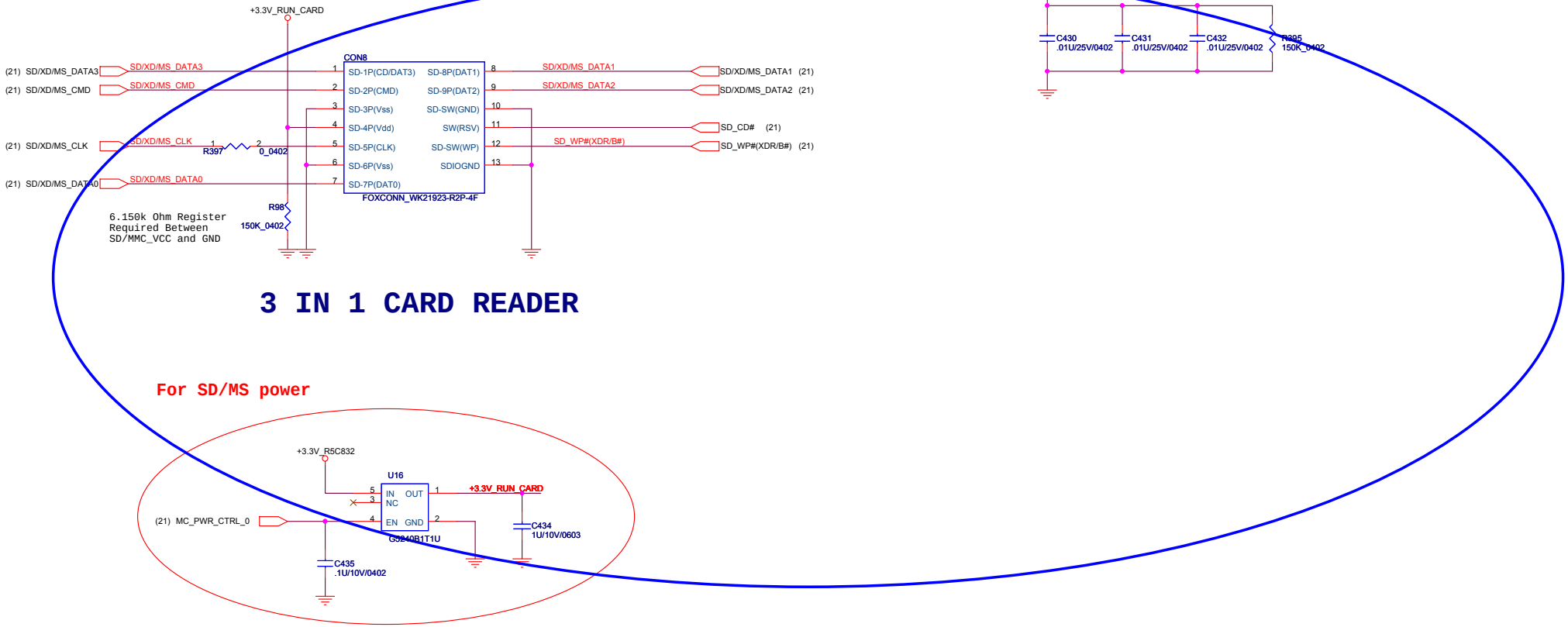
R5C832T_V00

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | CARD READER | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 21 of 47 | |

DO NOT INSERT SD/MMC SIMULTANEOUSLY.

changed for SD/MMC/SDIO only




# 3 IN 1 CARD READER

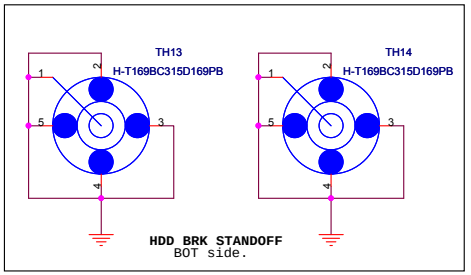
For SD/MS power



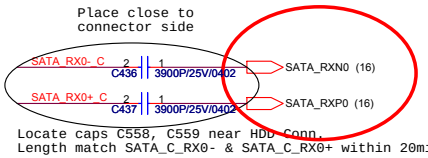

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | CARD READER CONN | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 22 of 47 | |

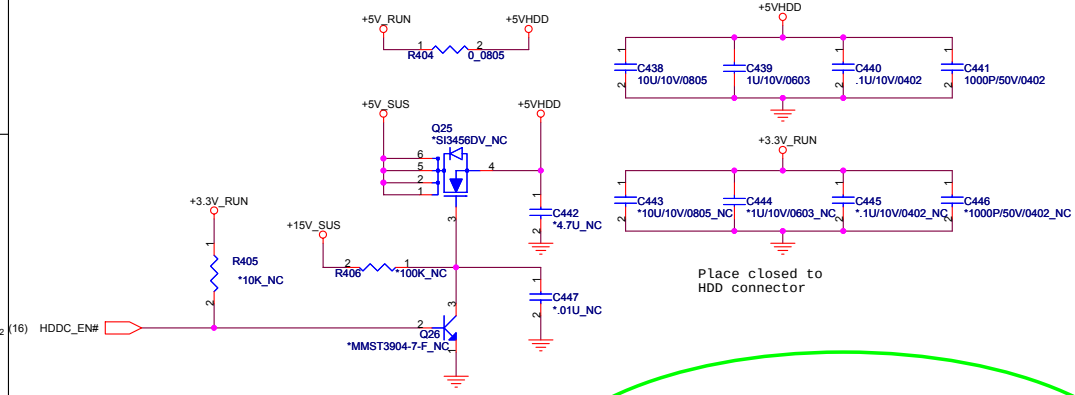
# SATA HDD




Place close to connector side



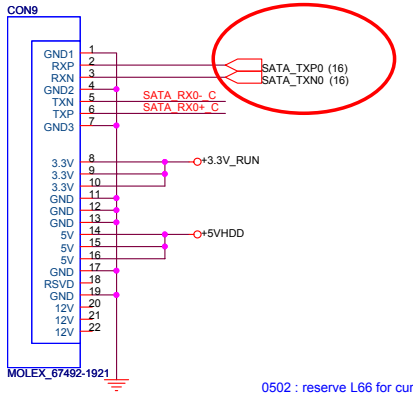

Locate caps C558, C559 near HDD Conn.
Length match SATA_C_RX0- & SATA_C_RX0+ within 20mils.

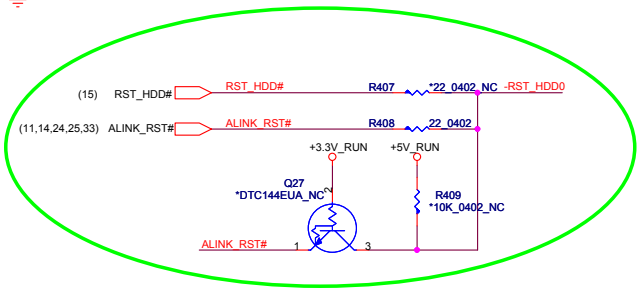



Place closed to HDD connector

SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

Power Estimate:
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.



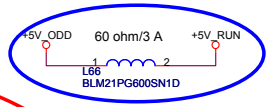

change name for ED5

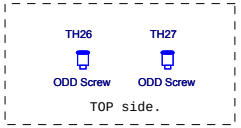
copy ED5 to FX2

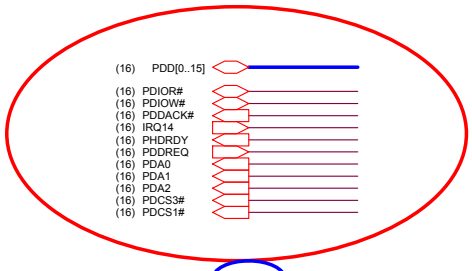
Waiting to check

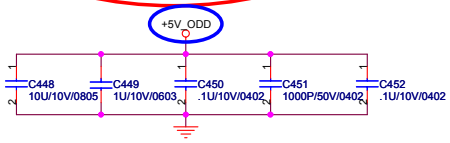
# PATA ODD

0502 : reserve L66 for current measurement , can be removed and short directly after RTS ; and change +5V_RUN to +5V_ODD for ODD side power



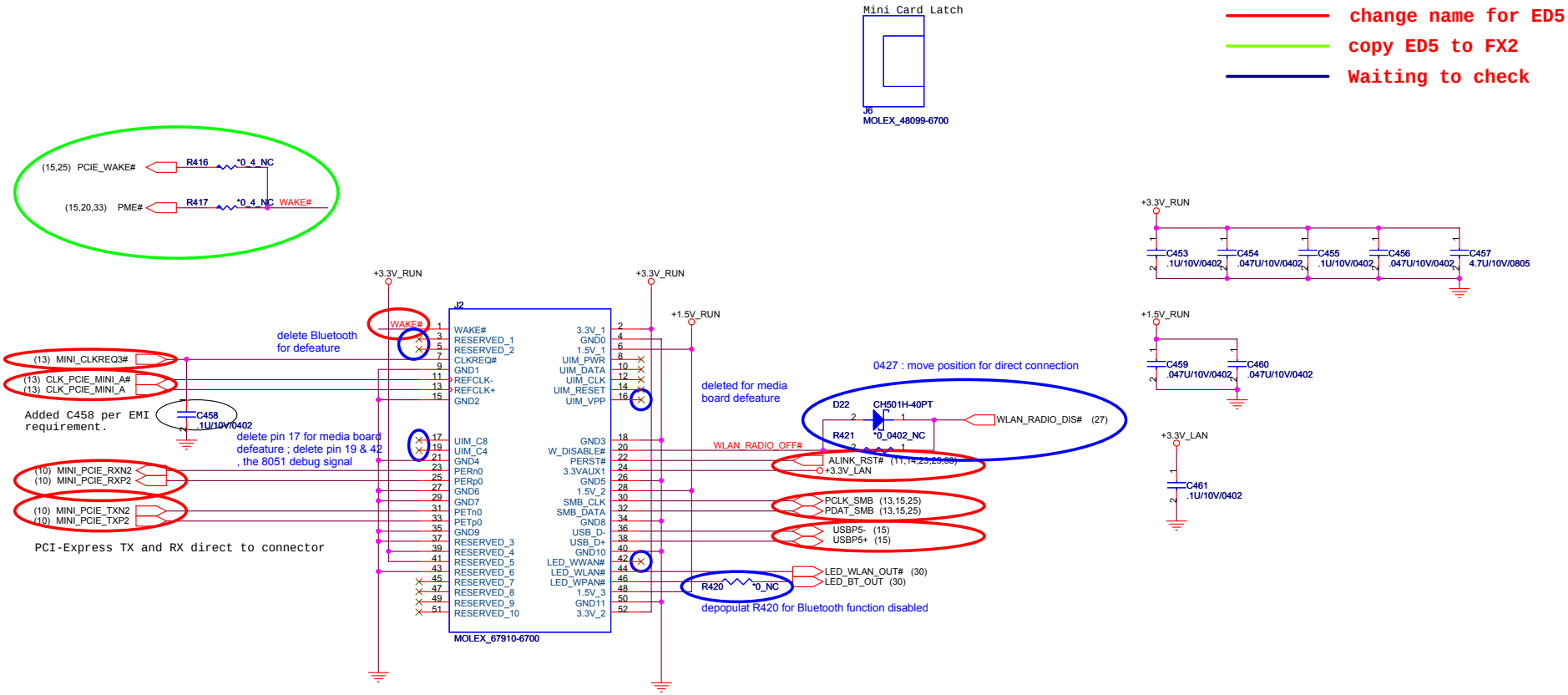




Place closed to MOD connector




| | | | |
|---|---|---|---|
| Title | SATA HDD & PATA ODD | | |
| Size | Document Number FX2 | | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 23 of 47 | | |

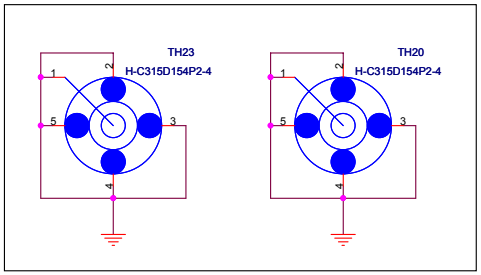
# MINI CARD




QUANTA COMPUTER

| | | |
|---|---|---|
| Title | MINI Card | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 24 of 47 | |

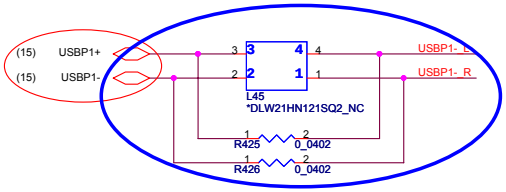
# Express Card

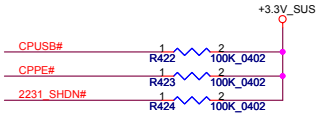



change name for ED5
copy ED5 to FX2
Waiting to check

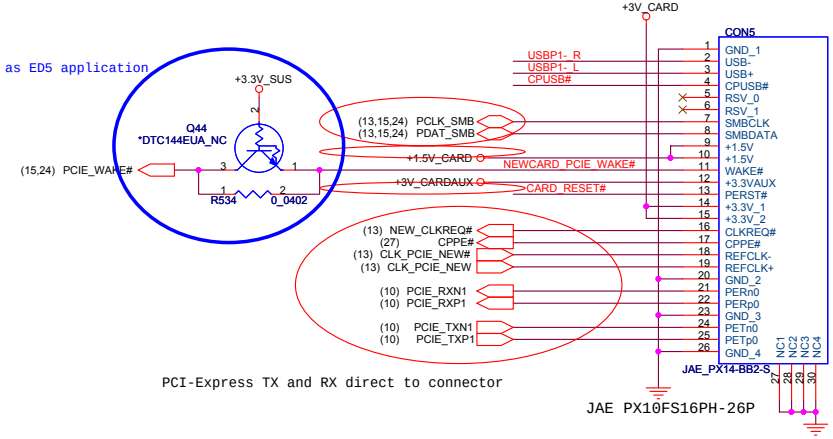
**NEW CARD GUIDE POST**
TOP side.

swap traces as "fx2_swap-0412"



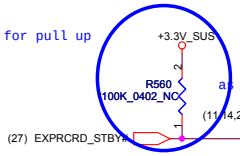

as ED5 application




PCI-Express TX and RX direct to connector

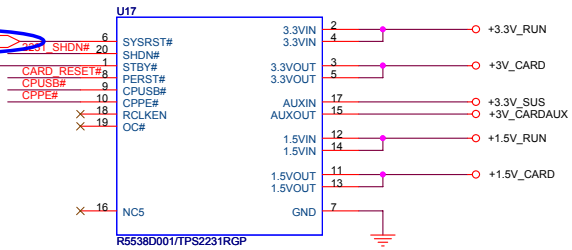
JAE PX10FS16PH-26P

reserve for pull up

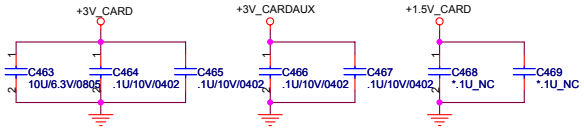


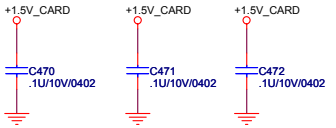

as ED5 application

+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

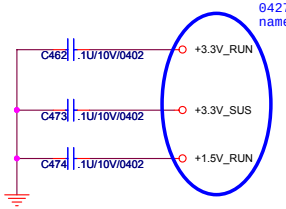



**+1.5V_CARD Max. 650mA, Average 500mA**
**+3V_CARD Max. 1300mA, Average 1000mA**




0427 : change from only net name to symbol "power point"




QUANTA COMPUTER

| | | |
|---|---|---|
| Title | Express Card | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 25 of 47 | |

# MDC INTERFACE

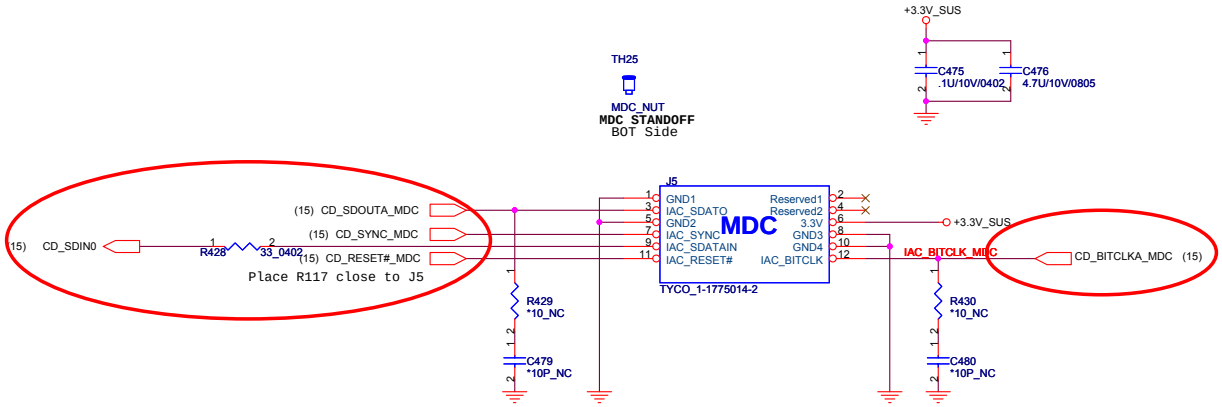
## MDC Layout Notes

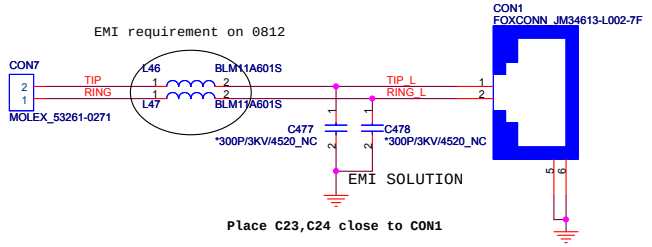
1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Tip and Ring connector pitch = 25 mils
4. Keep out area from Tip and Ring to other signals = 100 mils
5. Power and Ground minimum trace width to connector = 20 mils
6. Route Tip and Ring on one layer only (top or bottom)
7. Modem internal cable wire size = 26 AWG
(stranded or twisted pair wire)

change name for ED5

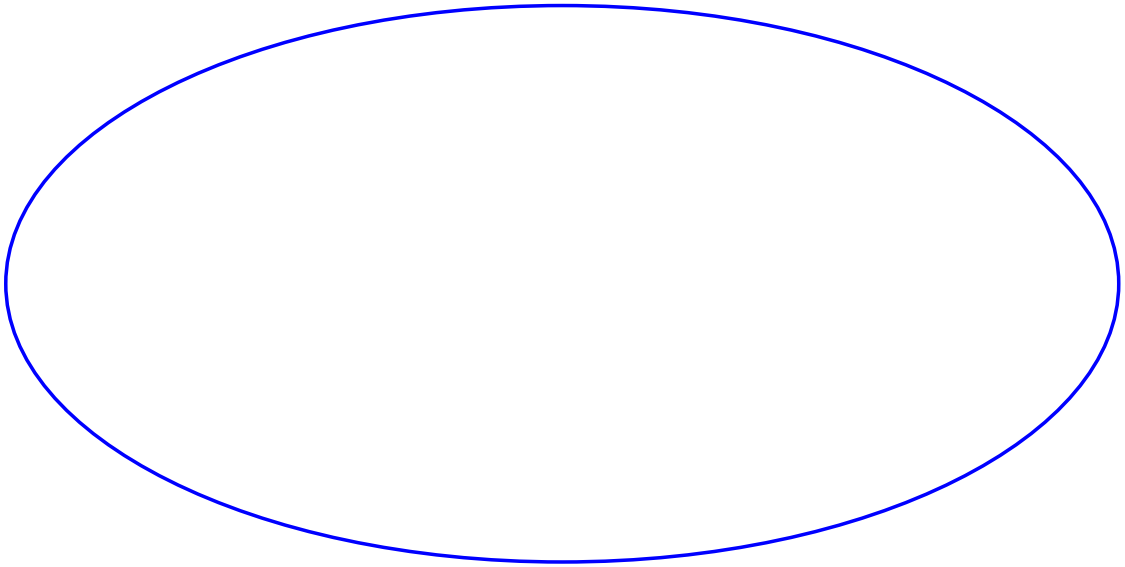
copy ED5 to FX2

Waiting to check




delete Bluetooth
for defeature



QUANTA COMPUTER

| | | |
|---|---|---|
| Title | MDC CONN | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 26 of 47 | |

EC pin updated as "FX2 KBC GPIO define v14"

| I/O Address | | |
|---|---|---|
| BADDR1-0 | Index | Data |
| 0 0 | 2E | 2F |
| 0 1 | 4E | 4F |
| 1 0 | (HCFGBAH, HCFGBAL) | (HCFGBAH, HCFGBAL)+1 |
| 1 1 | Reserved | |

add R468 for +3.3_SRC & R516 connected to +3.3V_ALW as power concern about the leakage; create +3.3V_97551.

+3.3V_SRC to +3.3V_97551

delete pull up circuit of BT_PWERON#

SHBM=1: Enable shared memory with host BIOS

0502 : added as Loki's suggestion

delete pull up circuit of RF_SW#, TV_SENSE#_D, MONITOR_PLUG#

as FM1

Instant on power switch input only

modify for thermal protect

0427 : change from BREATH_LED to BREATH_LED#

PBAT_SMBCLK/DAT : Charger, Battery
MBCLK/DATA : LCD, Password, CPU internal thermal diode

+3.3V_SRC to +3.3V_97551

U21
ST Micro M29W008AB/AMD-29LV081B/SST39VF080

delete PLCC32 connector

delete HWPG_1.8V

C501 *1U/10V_4_NC FOR 97551 ONLY

DIRECTLY 50 mS
HWPG_591 ===> NB_PWRGD ===> EC_PWRGD
NORTH BRIDGE SOUTH BRIDGE

# EC & FALSH ROM

QUANTA COMPUTER

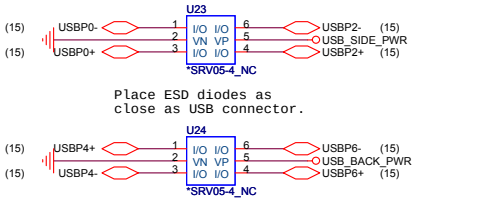
| | | |
|---|---|---|
| Title | PC97551 & FLASH | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 27 of 47 | |

change name for ED5

copy ED5 to FX2

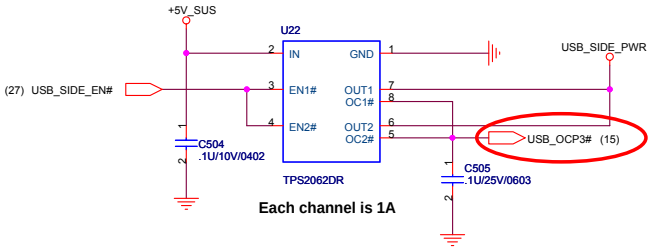
Waiting to check

8Mbit (1M Byte), SPI

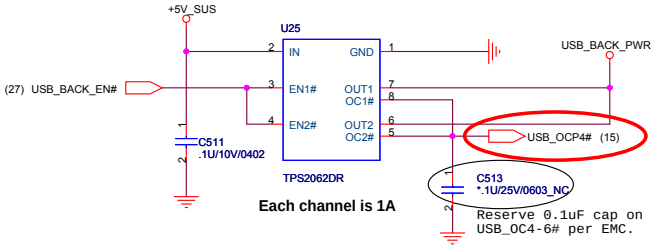



Place ESD diodes as close as USB connector.



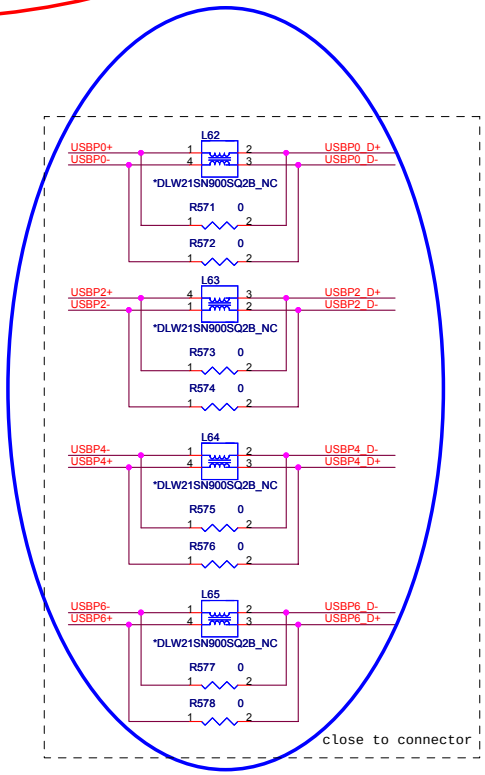




Each channel is 1A

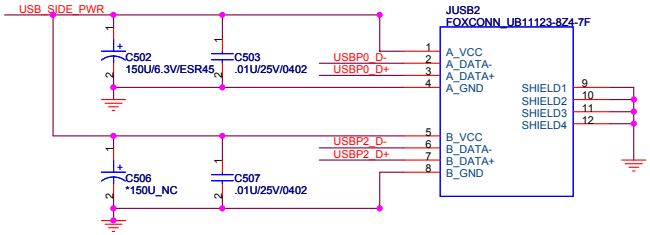


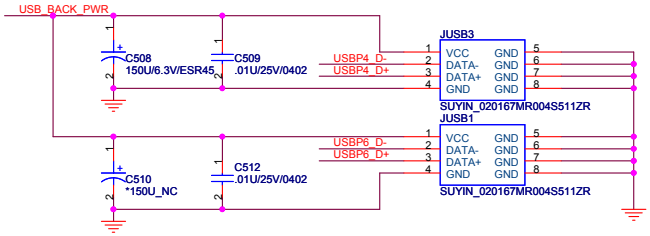

Each channel is 1A

Reserve 0.1uF cap on USB_OC4-6# per EMC.




add for EMI suggestion ,
0502 : swap P0/P2 traces as "fx2-swap-0502"




QUANTA COMPUTER

| | | |
|---|---|---|
| Title | USB | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 28 of 47 | |

TH3 H-C197D63P2
TH12 H-C197D63P2
TH1 HOLE-C315D126P2-4
TH2 H-C197D63P2
TH4 H-C197D63P2
TH18 H-C197D63P2
TH21 H-C197D63P2
TH16 H-C110D110N
TH22 H-C110D110N
PAD1 e-354x315R
PAD2 e-394x315L
PAD3 e-315x354D
0427 : add 3 pads for EMI need
TH7 H-C197D63P2
TH8 H-C197D63P2
TH10 H-C217D98P2-8
TH11 H-C217D98P2-8
TH24 H-C197D63P2
TH5 H-C197D63P2
TH17 H-C197D63P2
change footprint from
"H-C315D98P2-4" to "H-C217D98P2-8".
PV4 PAD138X98_H:4
PV10 PAD138X98_H:4
PV9 PAD138X98_H:4
PV8 PAD138X98_H:4
PV2 PAD138X98_H:4
PV7 PAD138X98_H:4
PV5 PAD138X98_H:3.5
PV3 PAD138X98_H:4
PV1 PAD138X98_H:3.5
PV6 PAD138X98_H:4
PV11 PAD138X98_H:4
0505 : delete PV12 , caused interference with
power component , EMI confirm no concern
+3.3V_RUN C514 *.1U_NC +1.5V_RUN
+3.3V_RUN C515 *.1U_NC +1.5V_RUN
+3.3V_SUS C516 *.1U_NC +5V_SUS
+3.3V_RUN C517 *.1U_NC +5V_SUS
+3.3V_RUN C518 *.1U_NC +5V_SUS
+PWR_SRC C519 *.1U_NC +5V_SUS
+PWR_SRC C520 *.1U_NC +5V_SUS
+PWR_SRC C521 *.1U_NC +5V_SUS
+PWR_SRC C522 *.1U_NC +5V_SUS
+PWR_SRC C523 *.1U_NC +3.3V_RUN
+PWR_SRC C524 *.1U_NC
+PWR_SRC C525 *.1U_NC
DC_IN+ C526 *.1U_NC
+1.5V_RUN C527 *.1U_NC
+1.5V_RUN C528 *.1U_NC
+1.5V_RUN C529 *.1U_NC
+1.5V_RUN C530 *.1U_NC
+1.5V_RUN C531 *.1U_NC
+1.5V_RUN C532 *.1U_NC
+1.5V_RUN C533 *.1U_NC
+3.3V_SUS C534 *.1U_NC
+PWR_SRC C535 .1U/25V/0603
+PWR_SRC C536 .1U/25V/0603
+PWR_SRC C537 .1U/25V/0603
+PWR_SRC C538 .1U/25V/0603
+PWR_SRC C539 .1U/25V/0603
+PWR_SRC C540 .1U/25V/0603
0502 : reserve 20 pcs of 4700pF stiching Cap. from +1.8V_SUS to GND for EMI concern
+1.8V_SUS C681 *4700P/25V/0402_NC
+1.8V_SUS C682 *4700P/25V/0402_NC
+1.8V_SUS C683 *4700P/25V/0402_NC
+1.8V_SUS C684 *4700P/25V/0402_NC
+1.8V_SUS C685 *4700P/25V/0402_NC
+1.8V_SUS C686 *4700P/25V/0402_NC
+1.8V_SUS C687 *4700P/25V/0402_NC
+1.8V_SUS C688 *4700P/25V/0402_NC
place close to CPU
+1.8V_SUS C689 *4700P/25V/0402_NC
+1.8V_SUS C690 *4700P/25V/0402_NC
+1.8V_SUS C691 *4700P/25V/0402_NC
+1.8V_SUS C692 *4700P/25V/0402_NC
+1.8V_SUS C693 *4700P/25V/0402_NC
+1.8V_SUS C694 *4700P/25V/0402_NC
+1.8V_SUS C695 *4700P/25V/0402_NC
+1.8V_SUS C696 *4700P/25V/0402_NC
+1.8V_SUS C697 *4700P/25V/0402_NC
+1.8V_SUS C698 *4700P/25V/0402_NC
+1.8V_SUS C699 *4700P/25V/0402_NC
+1.8V_SUS C700 *4700P/25V/0402_NC
place close to DDR II connector

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | EMI & Screw hole | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 29 of 47 | |

change name for ED5

copy ED5 to FX2

Waiting to check

+3.3V_RUN

(16) SATA_LED# — Q30 DTA114YUA — HDD_LED_S

(27) CAPSLED# — Q31 DTA114YUA — CAP_LED_S

+3.3V_ALW

(27) BATLED0# — Q32 DTA114YUA — BAT1_LED

(27) NUMLED# — Q33 DTA114YUA — NUM_LED_S

(27) BATLED1# — Q34 DTA114YUA — BAT2_LED

(27) SCROLED# — Q35 DTA114YUA — SCRL_LED_S

0427 : change from BREATH_LED to BREATH_LED#

+3.3V_SUS

(27) BREATH_LED# — U26 TC7SZ04FU

R460 200_0402 BREATH_PWRLED — D35 19-21VGC/TR8

HDD_LED_S — R461 200_0402 HDD_LED — D36 19-21VGC/TR8

BAT2_LED — R462 470_0402 RBAT2_LED

BAT1_LED — R463 470_0402 RBAT1_LED — D37 19-22SURSYGC/S530-A2/TR8

NUM_LED_S — R464 200_0402 NUM_LED

CAP_LED_S — R465 200_0402 CAP_LED

SCRL_LED_S — R466 200_0402 SCRL_LED

LED_WLAN_OUT_R — R467 200_0402 LED_WLAN_OUT

+3.3V_RUN

(24) LED_WLAN_OUT# — Q36 DTA114YUA — LED_WLAN_OUT_R

Touch Pad

+5V_RUN

RP19 4P2R-S-4.7K

(27) TBCLK

(27) TBDATA

L50 BLM11A601S

L51 BLM11A601S

TP_CLK

TP_DATA

JTP1 Molex-52808-0629-6P

C543 10P C546 10P C545 10P C544 10P

+5V_RUN

C542 1U_10V C541 .047U

+5V_RUN

JDASH1 SUYIN_127183MA010G513ZR

NUM_LED

CAP_LED

SCRL_LED

LED_WLAN_OUT

LED_BT_OUT

(24) LED_BT_OUT

(27,35) POWER_SW#

(27) INSTANT_POWER_SW#

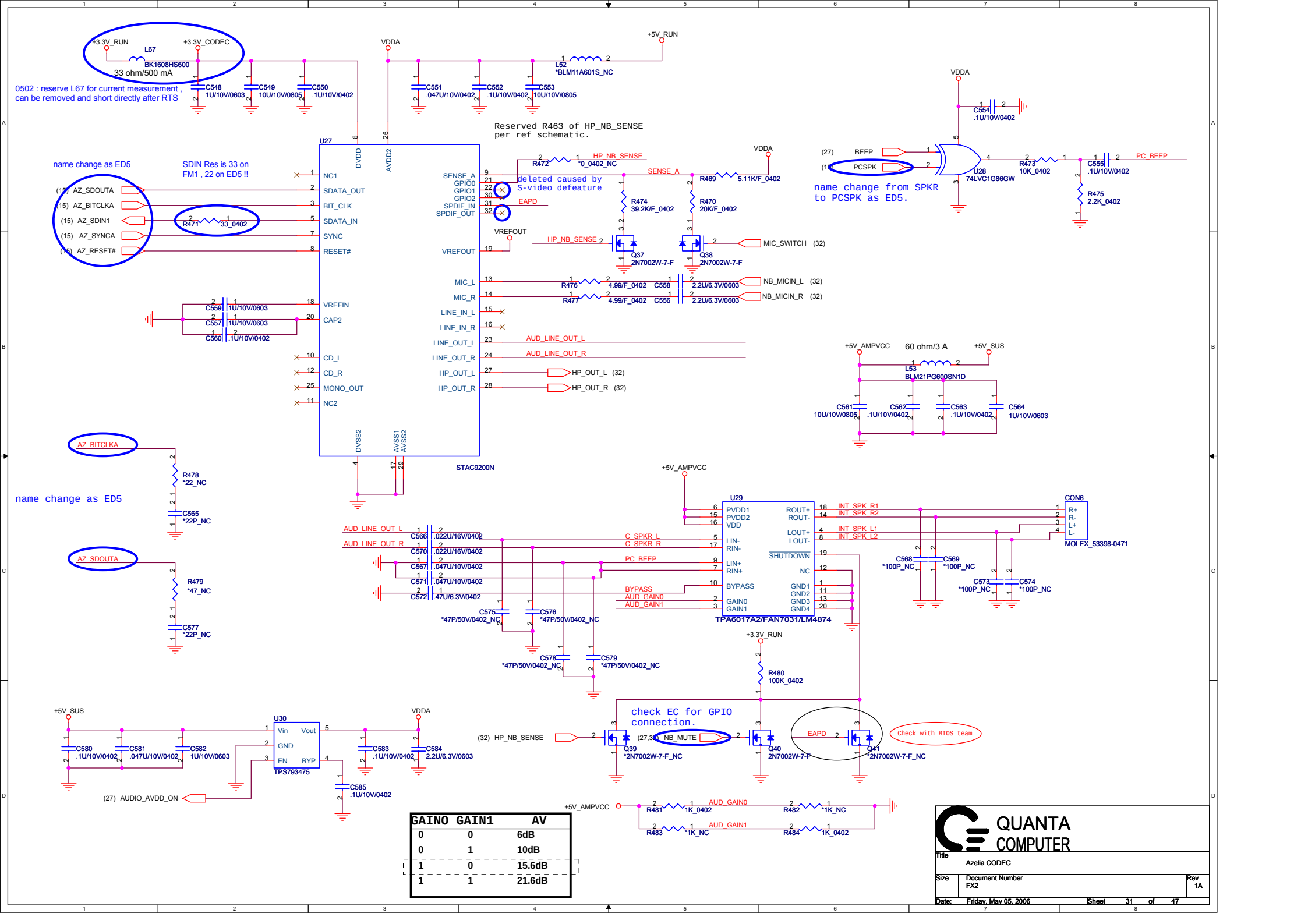
FM1 media board changed to TP only as DM5

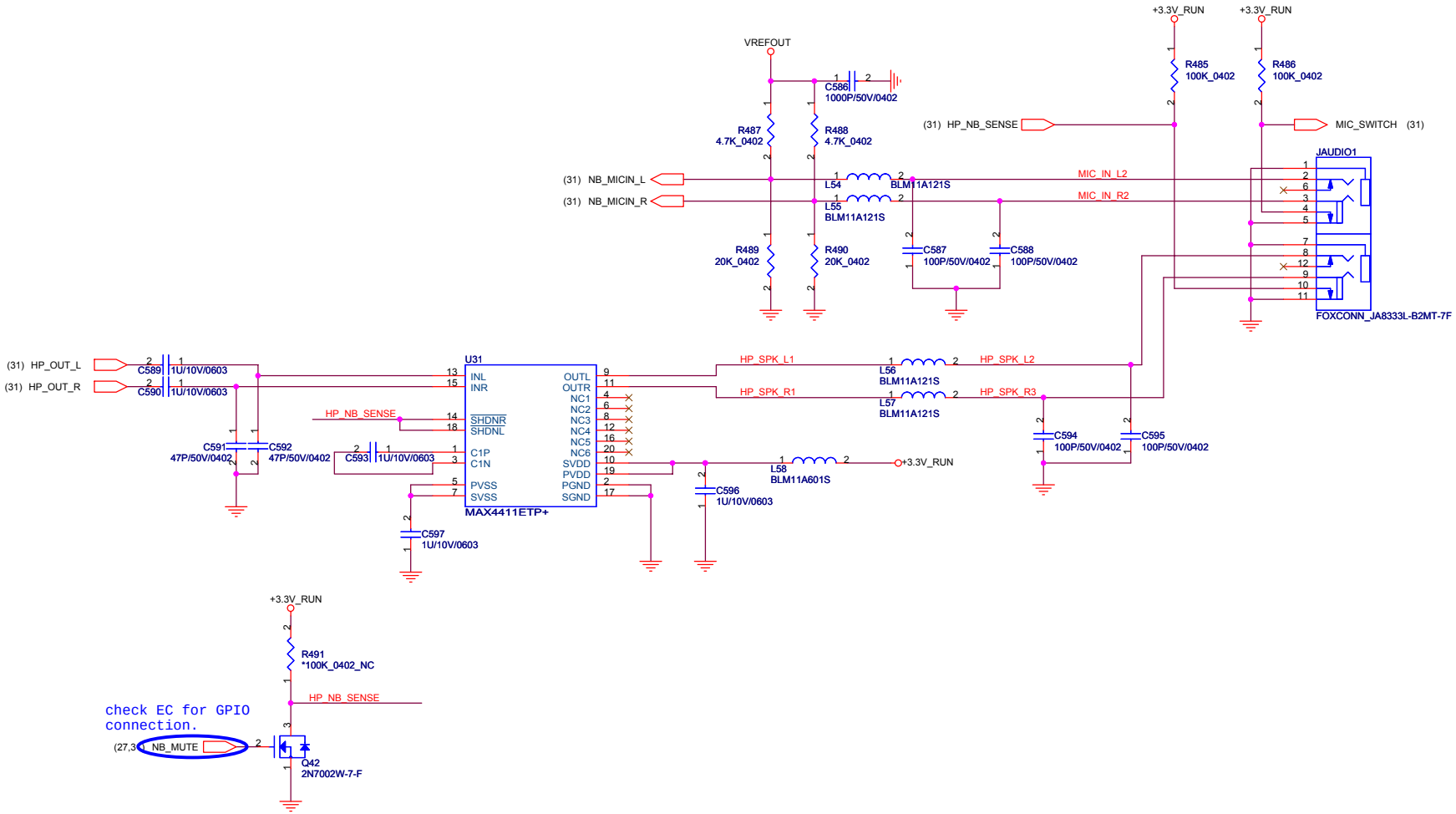
QUANTA COMPUTER

Title: SWITCH & TP & LED

Size: Document Number: FX2 Rev: 1A

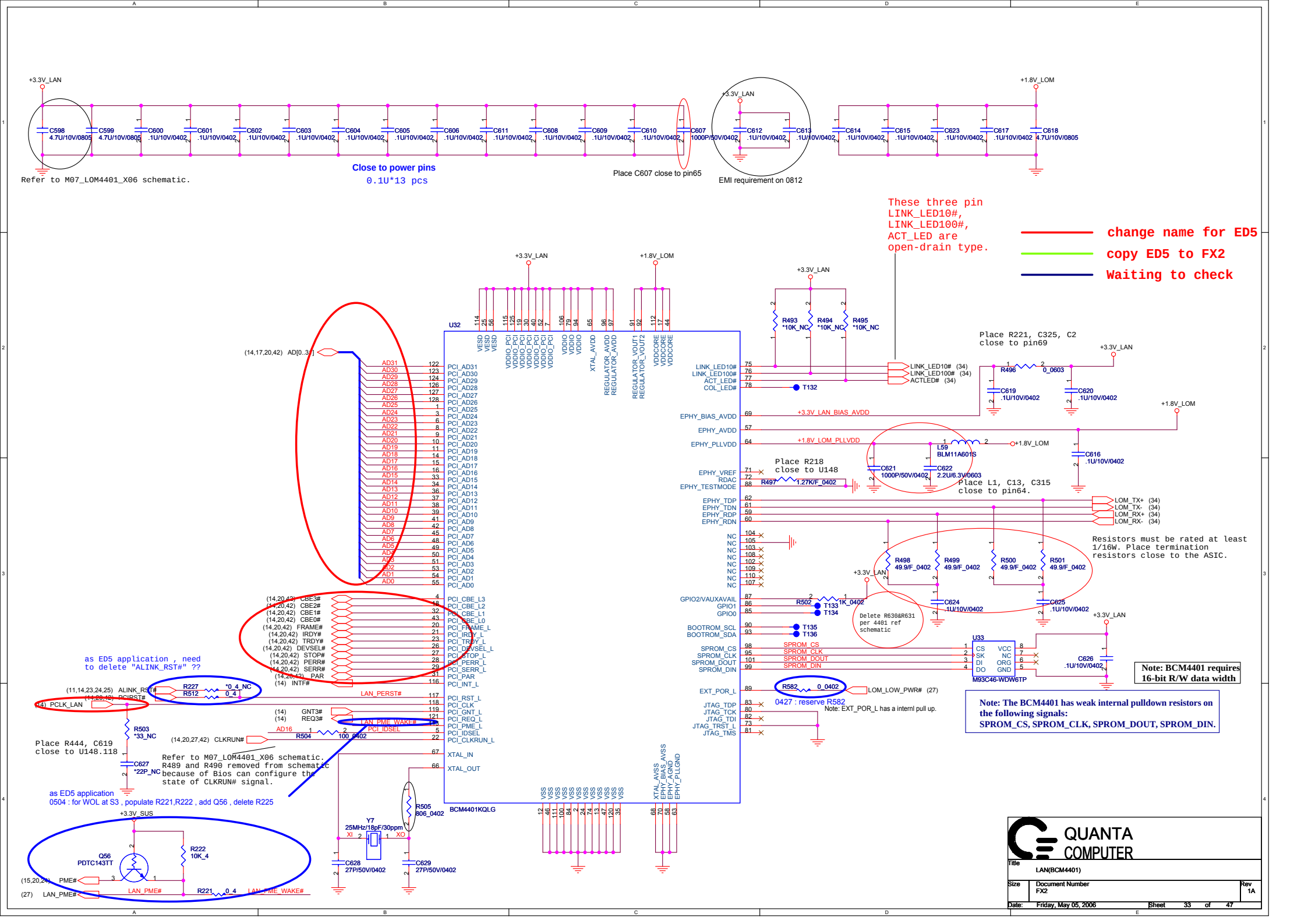
Date: Friday, May 05, 2006 Sheet 30 of 47

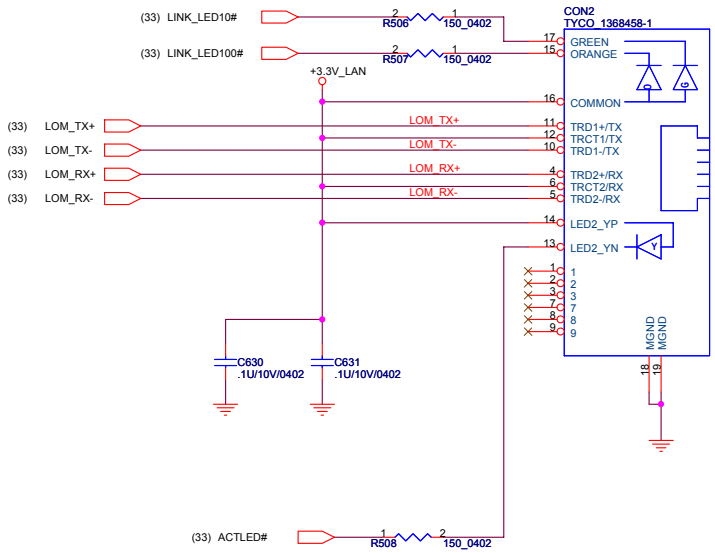

+3.3V_RUN
+3.3V_CODEC
L67
BK1608HS600
33 ohm/500 mA
0502 : reserve L67 for current measurement , can be removed and short directly after RTS
C548 1U/10V/0603
C549 10U/10V/0805
C550 .1U/10V/0402
VDDA
+5V_RUN
L52 *BLM11A601S_NC
C551 .047U/10V/0402
C552 .1U/10V/0402
C553 10U/10V/0805
Reserved R463 of HP_NB_SENSE per ref schematic.
U27
STAC9200N
name change as ED5
SDIN Res is 33 on FM1 , 22 on ED5 !!
(15) AZ_SDOUTA
(15) AZ_BITCLKA
(15) AZ_SDIN1
(15) AZ_SYNCA
(15) AZ_RESET#
R471 33_0402
NC1
SDATA_OUT
BIT_CLK
SDATA_IN
SYNC
RESET#
DVDD
AVDD2
SENSE_A
GPIO0
GPIO1
GPIO2
SPDIF_IN
SPDIF_OUT
R472 *0_0402_NC
HP_NB_SENSE
SENSE_A
R469 5.11K/F_0402
deleted caused by S-video defeature
EAPD
R474 39.2K/F_0402
R470 20K/F_0402
VREFOUT
Q37 2N7002W-7-F
Q38 2N7002W-7-F
MIC_SWITCH (32)
MIC_L
MIC_R
R476 4.99/F_0402
R477 4.99/F_0402
C558 2.2U/6.3V/0603
C556 2.2U/6.3V/0603
NB_MICIN_L (32)
NB_MICIN_R (32)
LINE_IN_L
LINE_IN_R
LINE_OUT_L
LINE_OUT_R
HP_OUT_L
HP_OUT_R
AUD_LINE_OUT_L
AUD_LINE_OUT_R
HP_OUT_L (32)
HP_OUT_R (32)
VREFIN
CAP2
C559 1U/10V/0603
C557 1U/10V/0603
C560 .1U/10V/0402
CD_L
CD_R
MONO_OUT
NC2
DVSS2
AVSS1
AVSS2
(27) BEEP
(15) PCSPK
U28 74LVC1G86GW
R473 10K_0402
C555 .1U/10V/0402
R475 2.2K_0402
PC_BEEP
name change from SPKR to PCSPK as ED5.
C554 .1U/10V/0402
+5V_AMPVCC
60 ohm/3 A
+5V_SUS
L53 BLM21PG600SN1D
C561 10U/10V/0805
C562 .1U/10V/0402
C563 .1U/10V/0402
C564 1U/10V/0603
AZ_BITCLKA
R478 *22_NC
C565 *22P_NC
name change as ED5
AZ_SDOUTA
R479 *47_NC
C577 *22P_NC
U29
TPA6017A2/FAN7031/LM4874
PVDD1
PVDD2
VDD
LIN-
RIN-
LIN+
RIN+
BYPASS
GAIN0
GAIN1
ROUT+
ROUT-
LOUT+
LOUT-
SHUTDOWN
NC
GND1
GND2
GND3
GND4
C_SPKR_L
C_SPKR_R
PC_BEEP
BYPASS
AUD_GAIN0
AUD_GAIN1
INT_SPK_R1
INT_SPK_R2
INT_SPK_L1
INT_SPK_L2
CON6
MOLEX_53398-0471
C566 .022U/16V/0402
C570 .022U/16V/0402
C567 .047U/10V/0402
C571 .047U/10V/0402
C572 .47U/6.3V/0402
C575 *47P/50V/0402_NC
C576 *47P/50V/0402_NC
C578 *47P/50V/0402_NC
C579 *47P/50V/0402_NC
C568 *100P_NC
C569 *100P_NC
C573 *100P_NC
C574 *100P_NC
R480 100K_0402
check EC for GPIO connection.
(32) HP_NB_SENSE
(27,31) NB_MUTE
Q39 *2N7002W-7-F_NC
Q40 2N7002W-7-F
Q41 *2N7002W-7-F_NC
EAPD
Check with BIOS team
+5V_SUS
U30
TPS793475
Vin
Vout
GND
EN
BYP
C580 .1U/10V/0402
C581 .047U/10V/0402
C582 1U/10V/0603
C583 .1U/10V/0402
C584 2.2U/6.3V/0603
C585 .1U/10V/0402
(27) AUDIO_AVDD_ON
+5V_AMPVCC
R481 1K_0402
R482 *1K_NC
R483 *1K_NC
R484 1K_0402
AUD_GAIN0
AUD_GAIN1
GAINO GAIN1 AV
0 0 6dB
0 1 10dB
1 0 15.6dB
1 1 21.6dB
QUANTA COMPUTER
Title: Azelia CODEC
Size: Document Number FX2
Rev: 1A
Date: Friday, May 05, 2006
Sheet 31 of 47




QUANTA COMPUTER

| | | |
|---|---|---|
| Title | AUDIO CONN | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 32 of 47 | |


+3.3V_LAN
C598 4.7U/10V/0805
C599 4.7U/10V/0805
C600 .1U/10V/0402
C601 .1U/10V/0402
C602 .1U/10V/0402
C603 .1U/10V/0402
C604 .1U/10V/0402
C605 .1U/10V/0402
C606 .1U/10V/0402
C611 .1U/10V/0402
C608 .1U/10V/0402
C609 .1U/10V/0402
C610 .1U/10V/0402
C607 1000P/50V/0402
Refer to M07_LOM4401_X06 schematic.
Close to power pins
0.1U*13 pcs
Place C607 close to pin65
C612 .1U/10V/0402
C613 .1U/10V/0402
EMI requirement on 0812
+1.8V_LOM
C614 .1U/10V/0402
C615 .1U/10V/0402
C623 .1U/10V/0402
C617 .1U/10V/0402
C618 4.7U/10V/0805
These three pin LINK_LED10#, LINK_LED100#, ACT_LED are open-drain type.
change name for ED5
copy ED5 to FX2
Waiting to check
U32
BCM4401KQLG
R493 *10K_NC
R494 *10K_NC
R495 *10K_NC
T132
Place R221, C325, C2 close to pin69
R496 0_0603
C619 .1U/10V/0402
C620 .1U/10V/0402
L59 BLM11A601S
C621 1000P/50V/0402
C622 2.2U/6.3V/0603
C616 .1U/10V/0402
Place R218 close to U148
R497 1.27K/F_0402
Place L1, C13, C315 close to pin64.
R498 49.9/F_0402
R499 49.9/F_0402
R500 49.9/F_0402
R501 49.9/F_0402
C624 .1U/10V/0402
C625 .1U/10V/0402
Resistors must be rated at least 1/16W. Place termination resistors close to the ASIC.
R502 1K_0402
T133
T134
Delete R630&R631 per 4401 ref schematic
T135
T136
U33
M93C46-WDW6TP
C626 .1U/10V/0402
Note: BCM4401 requires 16-bit R/W data width
R582 0_0402
0427 : reserve R582
Note: EXT_POR_L has a internl pull up.
Note: The BCM4401 has weak internal pulldown resistors on the following signals:
SPROM_CS, SPROM_CLK, SPROM_DOUT, SPROM_DIN.
as ED5 application , need to delete "ALINK_RST#" ??
R227 *0_4_NC
R512 0_4
R503 *33_NC
C627 *22P_NC
Place R444, C619 close to U148.118
Refer to M07_LOM4401_X06 schematic. R489 and R490 removed from schematic because of Bios can configure the state of CLKRUN# signal.
R504 100_0402
as ED5 application
0504 : for WOL at S3 , populate R221,R222 , add Q56 , delete R225
+3.3V_SUS
Q56 PDTC143TT
R222 10K_4
R221 0_4
LAN_PME#
LAN_PME_WAKE#
Y7 25MHz/18pF/30ppm
C628 27P/50V/0402
C629 27P/50V/0402
R505 806_0402
QUANTA COMPUTER
Title: LAN(BCM4401)
Size: Document Number FX2
Rev: 1A
Date: Friday, May 05, 2006
Sheet 33 of 47

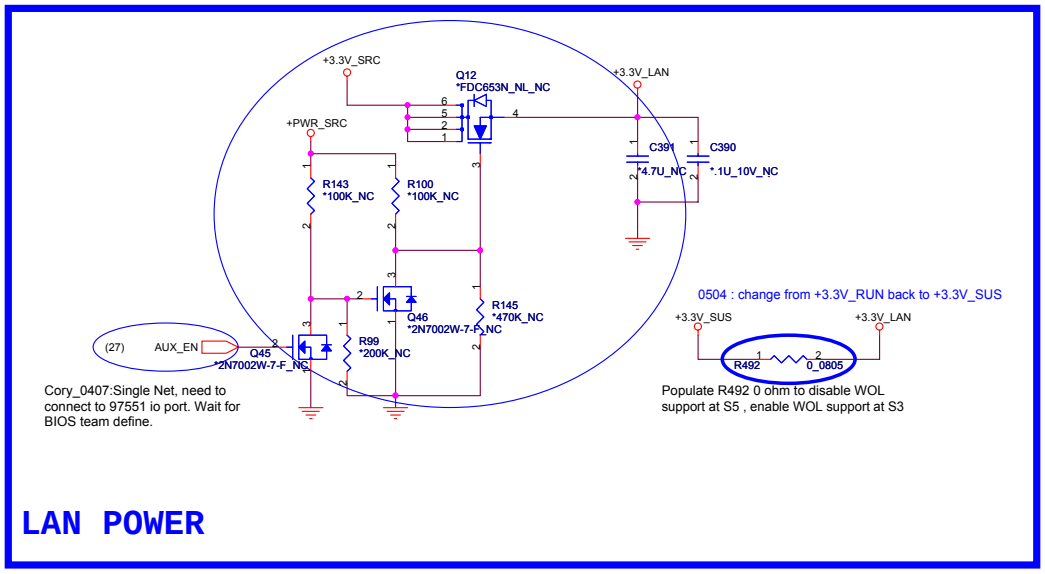



change name for ED5

copy ED5 to FX2

Waiting to check

copy DM5 to FX2




QUANTA COMPUTER

| | | |
|---|---|---|
| Title | LAN JACK | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 34 of 47 | |

add Thermal IC as FM1

H_THERMDA&h_THERMDC
trace routing = W:10/S:10

(5) CPU_TEST4_THERMDA
(5) CPU_TEST5_THERMDC

Place C653 close to U36

C653 2200P/50V/0402

+3.3V_SUS
R536 7.5K/F_0402

U36 EMC4000

(18,27) MBDATA
(18,27) MBCLK

SMDATA
SMBCLK
LDO_SHDN#_ADDR
DP2
DN2
+3V_SUS
VSUS_PWRGD
+RTC_PWR3V
+3V_PWROK#
POWER_SW#
THERMTRIP1#
THERMTRIP2#
THERMTRIP3#
VSET
HW_LOCK#
VSS
FAN_DAC
FAN_OUT
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5

ATF_INT#
VCP1
VCP2
LDO_POK
DN1
DP1
THERMTRIP_SIO
ACAvail_Clr
SYS_SHDN#
VDD_5V
LDO_OUT
LDO_OUT
LDO_IN
LDO_IN
DP3
DN3
LDO_SET

+3.3V_SUS
R552 10K_0402
ATF_INT# (27)

delete single net "VCP1" & "VCP2"

R55310K_0402
+3.3V_RUN

+3.3V_SUS
R537 49.9/F_0402
+3VSUS_THRM

C655 .1U/10V/0402

VCCRTC
C658 .1U/10V/0402

SUSPWROK
R539 1K_0402

EC_PWRGD#
R540 1K_0402

(27,30) POWER_SW#

THERMTRIP1#

Place Q50 at bottom of CPU

REM_DIODE1_N & REM_DIODE1_P
trace routing = W:10/S:10

REM_DIODE1_N
REM_DIODE1_P

Place C656 close to the pins as possible.

C656 2200P/50/0402
Q50 MMST3904-7-F
C657 *2200P_NC

Place C657 close to the Q50

R541 10K_0402
+3.3V_ALW
THERMTRIP_SIO (27)

ACAV_IN (27,36)

THERM_SYS_PWR# (27,38)

R555 *10K_0402_NC
VCCRTC

+5V_RUN
+2.5V_RUN

+3.3V_SUS
R554 10K_0402
C663 .1U/10V/0402
R542 147K/F_0402
R543 41.2K_0402
C664 2200P/50V/0402
R544 1K_0402
VSET
HW_LOCK#
FAN1_VOUT

+3.3V_RUN_IN
R545 0_1210
+3.3V_RUN

REM_DIODE3_N & REM_DIODE3_P trace routing = W:10/S:10

REM_DIODE3_P
REM_DIODE3_N
LDO_SET

C668 2200P/50V/0402
Q51 MMST3904-7-F
C669 *2200P_NC

Place C668 close to U36

Place Q51 Near the SO-DIMM.

Place C669 close to Q51

+3.3V_RUN
R535 10K_0402
FAN1_TACH (27)
R538 0_0402

FAN1
FAN1_VOUT
FAN1_TACH_FB
D39 *CH751H-40HPT_NC
C654 22U/10V/1206
J3 VCC SIG GND
MOLEX_53398-0371

+5V_RUN
C659 10U/10V/0805
C660 .1U/10V/0402

+2.5V_RUN
C661 10U/10V/0805
C662 .1U/10V/0402

Place C659~C662, C665~C667, close to U36

+3.3V_RUN_IN
C665 1U/10V/0603
C666 .1U/10V/0402
C667 *10U_NC

Notes:
Vset=(Tp-70)/21
3.3*(R543/R542+R543)=(Tp-70)/21
Where Tp=70 to 101 degree C

Set trip point=85 degree C
Vset = (85-75)/16= 0.625 V
Guardian II temp-tolerance= +/-3 degree C

+3.3V_SUS
R546 100K_0402
EC_PWRGD#
(14,15,27) EC_PWRGD
Q52 2N7002W-7-F

VLDT_RUN
R549 2.2K_0402

+3.3V_SUS
R547 8.2K_0402
THERMTRIP1#
Q53 MMST3904-7-F
C670 .1U/10V/0402
(5) H_THERMTRIP#

C670 needs to be placed near Guardian IC.

+2.5V_RUN
R548 *31.5K_NC
LDO_SET
R550 1K_0603

Voltage margining circuit for LDO output.
For Vmargin, stuff R548 and R550=30K.
R550=1K for production

as FM1 keyboard matrix & "e0788.1104a_swap-0422"

JKB1
HRS_FH28D-50(25)SB-1SH(86)

(27) MY9 MY9 1
(27) MY10 MY10 2
(27) MY8 MY8 3
(27) MY13 MY13 4
(27) MY12 MY12 5
(27) MY14 MY14 6
(27) MY15 MY15 7
(27) MY11 MY11 8
(27) MY0 MY0 9
(27) MY2 MY2 10
(27) MY1 MY1 11
(27) MY3 MY3 12
(27) MY7 MY7 13
(27) MY5 MY5 14
(27) MY6 MY6 15
(27) MY4 MY4 16
(27) MY16 MY16 17
(27) MX7 MX7 18
(27) MX4 MX4 19
(27) MX6 MX6 20
(27) MX2 MX2 21
(27) MX5 MX5 22
(27) MX3 MX3 23
(27) MX1 MX1 24
(27) MX0 MX0 25

+3.3V_SUS
RP20 10KX8 MX7 MX4 MX6 MX2 MX0 MX1 MX3 MX5
RP21 10KX8 MY2 MY1 MY3 MY7 MY16 MY4 MY6 MY5
RP22 10KX8 MY10 MY8 MY13 MY12 MY0 MY11 MY15 MY14

CA1 *220PX4_NC MX7 MX4 MX6 MX2 MX0 MX1 MX3 MX5
CA2 *220PX4_NC MX7 MX4 MX6 MX2
CA3 *220PX4_NC MY7 MY1 MY2 MY3 MY16 MY4 MY6 MY5
CA4 *220PX4_NC MY7 MY1 MY2 MY3
CA5 *220PX4_NC MY10 MY8 MY13 MY12 MY0 MY11 MY15 MY14
CA6 *220PX4_NC MY10 MY8 MY13 MY12

+3.3V_SUS
R513 10K_0402
MY9
C638 *220P/50V/0402_NC

KBC

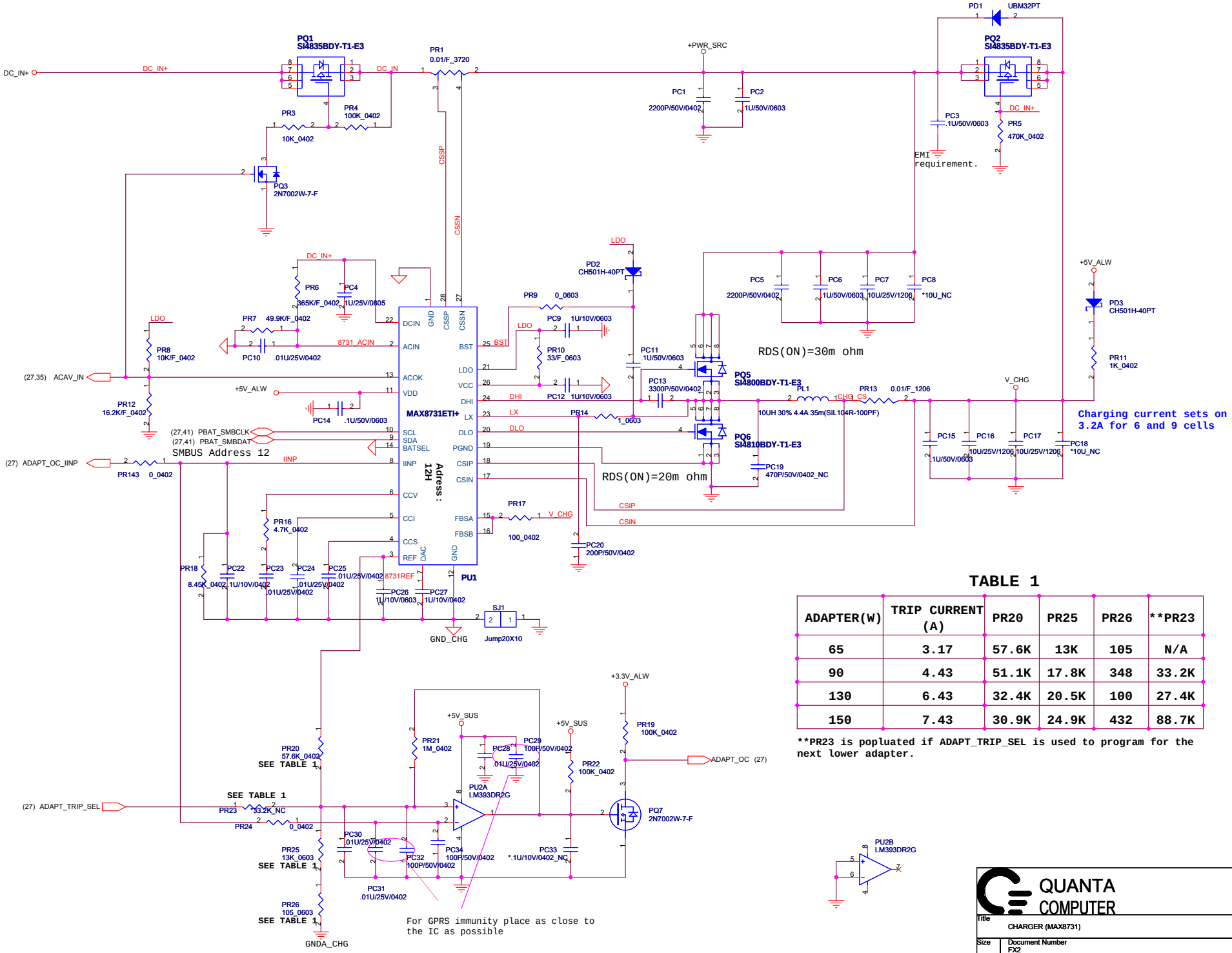
wait to discuss !!

(27,38,39,40) SUSON
+1.8V_SUS
+3.3V_ALW
+3.3V_SUS
+3.3V_SUS
R557 10K_0402
R556 100K_0402
U38
C671 *.047U_NC
U39
SUSPWROK
Q54 3904
C672 1U/50V/0603
TC7SZ04FU
TC7SZ08FU

0427 : change Q54 from 2N7002W-7-F to 3904 ; C672 from .1U/10V/0402 to .1U/50V/0603 as voltage level & timing concern

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | KB & THERMAL & FAN | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 35 of 47 | |



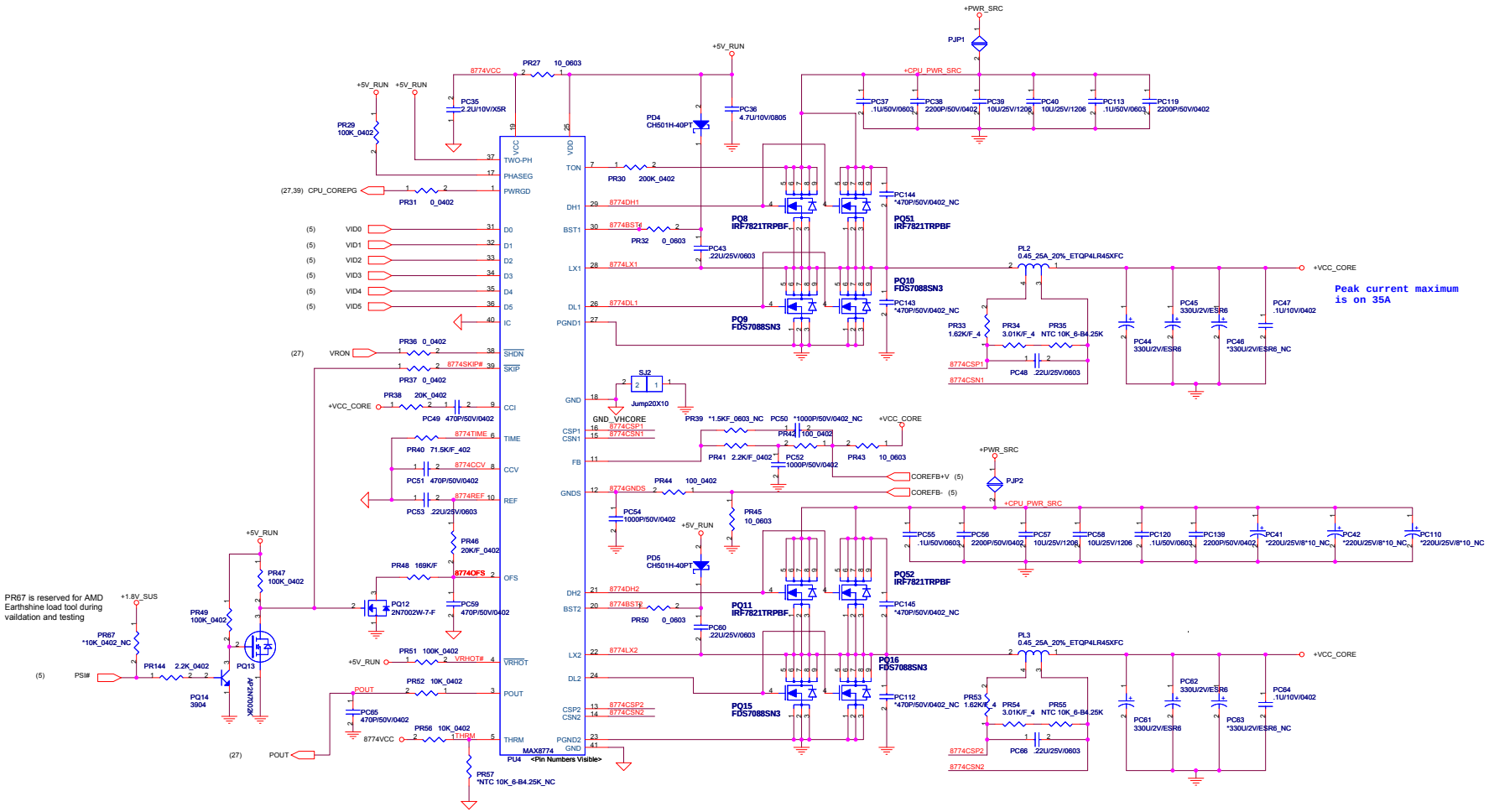

## TABLE 1

| ADAPTER(W) | TRIP CURRENT (A) | PR20 | PR25 | PR26 | **PR23 |
|---|---|---|---|---|---|
| 65 | 3.17 | 57.6K | 13K | 105 | N/A |
| 90 | 4.43 | 51.1K | 17.8K | 348 | 33.2K |
| 130 | 6.43 | 32.4K | 20.5K | 100 | 27.4K |
| 150 | 7.43 | 30.9K | 24.9K | 432 | 88.7K |

**PR23 is popluated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | CHARGER (MAX8731) | |
| Size | Document Number FX2 | Rev 1A |
| Date: 2005/4/21 | Sheet 36 of 47 | |

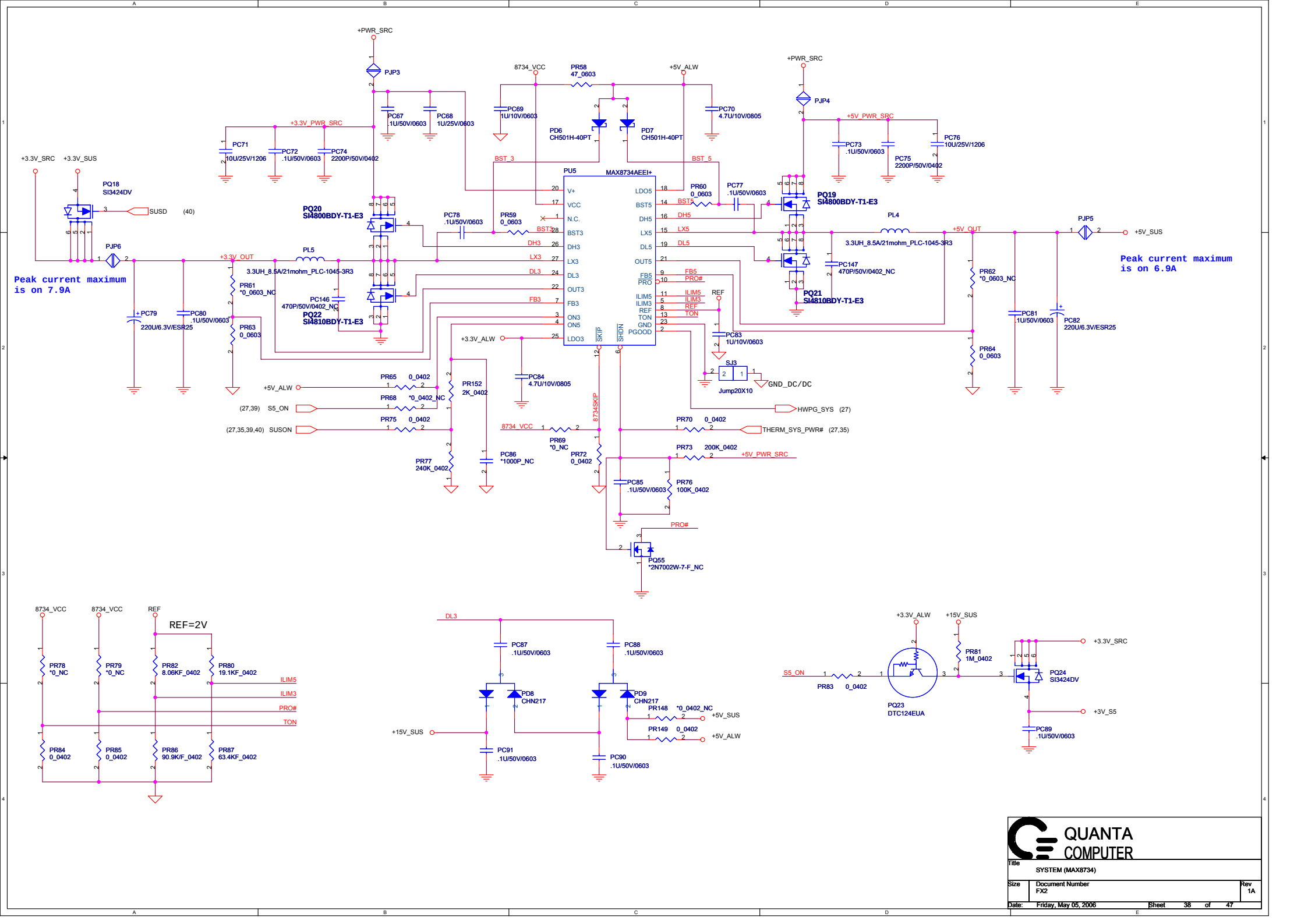



| D5 | D4 | D3 | D2 | D1 | D0 | Output |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1.5500V |
| 0 | 0 | 0 | 0 | 0 | 1 | 1.5250V |
| 0 | 0 | 0 | 0 | 1 | 0 | 1.5000V |
| 0 | 0 | 0 | 0 | 1 | 1 | 1.4750V |
| 0 | 0 | 0 | 1 | 0 | 0 | 1.4500V |
| 0 | 0 | 0 | 1 | 0 | 1 | 1.4250V |
| 0 | 0 | 0 | 1 | 1 | 0 | 1.4000V |
| 0 | 0 | 0 | 1 | 1 | 1 | 1.3750V |
| 0 | 0 | 1 | 0 | 0 | 0 | 1.3500V |
| 0 | 0 | 1 | 0 | 0 | 1 | 1.3250V |
| 0 | 0 | 1 | 0 | 1 | 0 | 1.3000V |
| 0 | 0 | 1 | 0 | 1 | 1 | 1.2750V |
| 0 | 0 | 1 | 1 | 0 | 0 | 1.2500V |
| 0 | 0 | 1 | 1 | 0 | 1 | 1.2250V |
| 0 | 0 | 1 | 1 | 1 | 0 | 1.2000V |
| 0 | 0 | 1 | 1 | 1 | 1 | 1.1750V |
| 0 | 1 | 0 | 0 | 0 | 0 | 1.1500V |
| 0 | 1 | 0 | 0 | 0 | 1 | 1.1250V |
| 0 | 1 | 0 | 0 | 1 | 0 | 1.1000V |
| 0 | 1 | 0 | 0 | 1 | 1 | 1.0750V |
| 0 | 1 | 0 | 1 | 0 | 0 | 1.0500V |
| 0 | 1 | 0 | 1 | 0 | 1 | 1.0250V |
| 0 | 1 | 0 | 1 | 1 | 0 | 1.0000V |
| 0 | 1 | 0 | 1 | 1 | 1 | 0.9750V |
| 0 | 1 | 1 | 0 | 0 | 0 | 0.9500V |
| 0 | 1 | 1 | 0 | 0 | 1 | 0.9250V |
| 0 | 1 | 1 | 0 | 1 | 0 | 0.9000V |
| 0 | 1 | 1 | 0 | 1 | 1 | 0.8750V |
| 0 | 1 | 1 | 1 | 0 | 0 | 0.8500V |
| 0 | 1 | 1 | 1 | 0 | 1 | 0.8250V |
| 0 | 1 | 1 | 1 | 1 | 0 | 0.8000V |
| 0 | 1 | 1 | 1 | 1 | 1 | 0.7750V |

| D5 | D4 | D3 | D2 | D1 | D0 | Output |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0.7625V |
| 1 | 0 | 0 | 0 | 0 | 1 | 0.7500V |
| 1 | 0 | 0 | 0 | 1 | 0 | 0.7375V |
| 1 | 0 | 0 | 0 | 1 | 1 | 0.7250V |
| 1 | 0 | 0 | 1 | 0 | 0 | 0.7125V |
| 1 | 0 | 0 | 1 | 0 | 1 | 0.7000V |
| 1 | 0 | 0 | 1 | 1 | 0 | 0.6875V |
| 1 | 0 | 0 | 1 | 1 | 1 | 0.6750V |
| 1 | 0 | 1 | 0 | 0 | 0 | 0.6625V |
| 1 | 0 | 1 | 0 | 0 | 1 | 0.6500V |
| 1 | 0 | 1 | 0 | 1 | 0 | 0.6375V |
| 1 | 0 | 1 | 0 | 1 | 1 | 0.6250V |
| 1 | 0 | 1 | 1 | 0 | 0 | 0.6125V |
| 1 | 0 | 1 | 1 | 0 | 1 | 0.6000V |
| 1 | 0 | 1 | 1 | 1 | 0 | 0.5875V |
| 1 | 0 | 1 | 1 | 1 | 1 | 0.5750V |
| 1 | 1 | 0 | 0 | 0 | 0 | 0.5625V |
| 1 | 1 | 0 | 0 | 0 | 1 | 0.5500V |
| 1 | 1 | 0 | 0 | 1 | 0 | 0.5375V |
| 1 | 1 | 0 | 0 | 1 | 1 | 0.5250V |
| 1 | 1 | 0 | 1 | 0 | 0 | 0.5125V |
| 1 | 1 | 0 | 1 | 0 | 1 | 0.5000V |
| 1 | 1 | 0 | 1 | 1 | 0 | 0.4875V |
| 1 | 1 | 0 | 1 | 1 | 1 | 0.4750V |
| 1 | 1 | 1 | 0 | 0 | 0 | 0.4625V |
| 1 | 1 | 1 | 0 | 0 | 1 | 0.4500V |
| 1 | 1 | 1 | 0 | 1 | 0 | 0.4375V |
| 1 | 1 | 1 | 0 | 1 | 1 | 0.4250V |
| 1 | 1 | 1 | 1 | 0 | 0 | 0.4125V |
| 1 | 1 | 1 | 1 | 0 | 1 | 0.4000V |
| 1 | 1 | 1 | 1 | 1 | 0 | 0.3875V |
| 1 | 1 | 1 | 1 | 1 | 1 | 0.3750V |

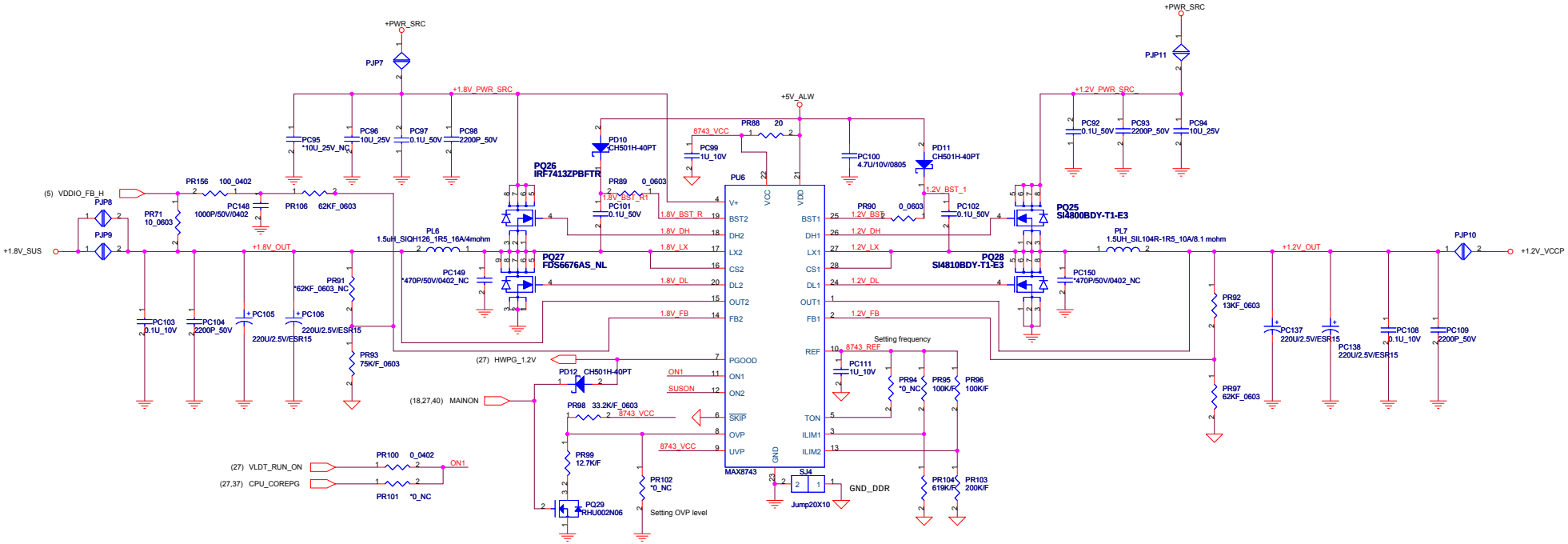
QUANTA COMPUTER

| | | |
|---|---|---|
| Title | VHCORE (MAX8774) | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 37 of 47 | |

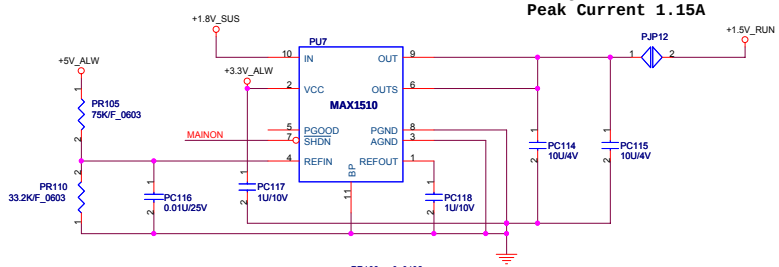



QUANTA COMPUTER

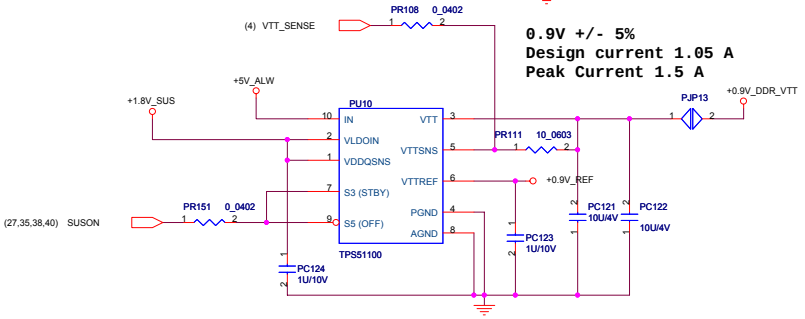
| | | |
|---|---|---|
| Title | SYSTEM (MAX8734) | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 38 of 47 | |

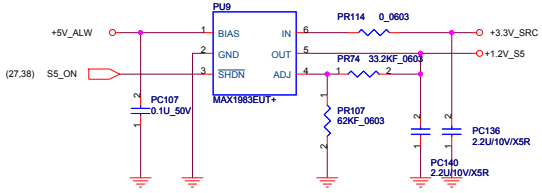



**1.5 Volt +/- 5%**
**Design current 0.7A**
**Peak Current 1.15A**

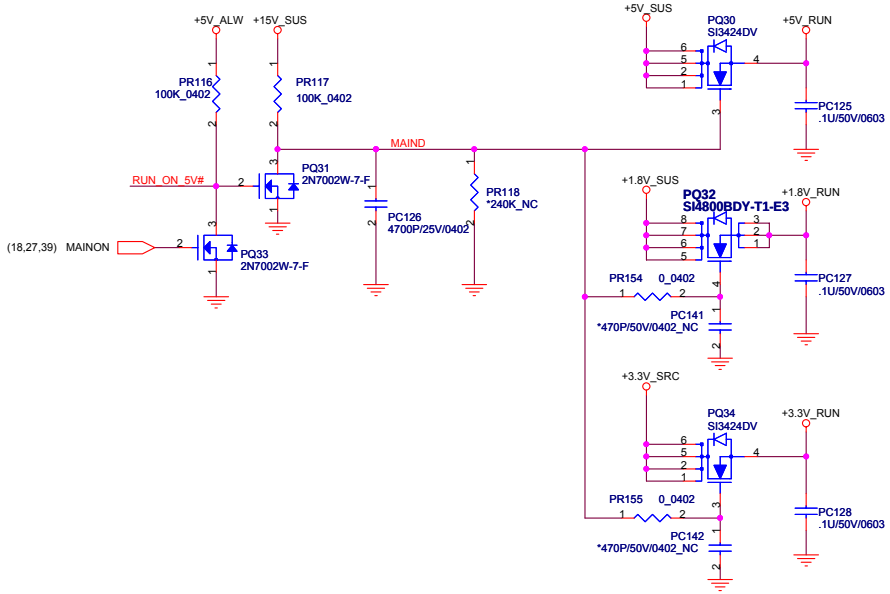


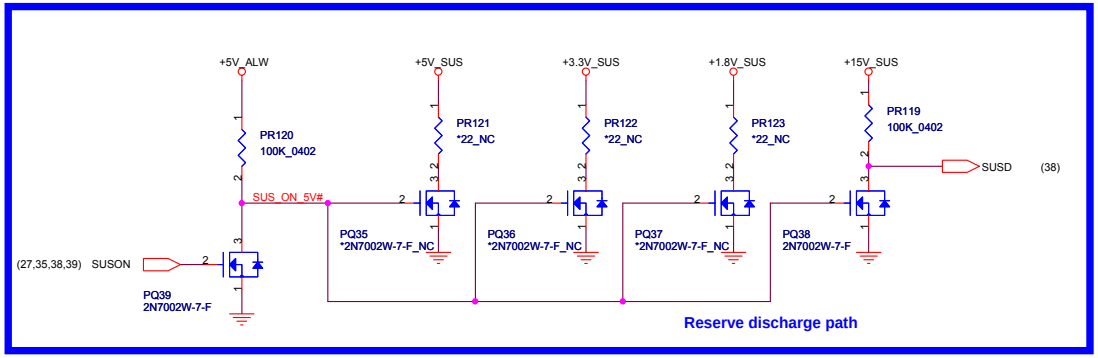

**0.9V +/- 5%**
**Design current 1.05 A**
**Peak Current 1.5 A**

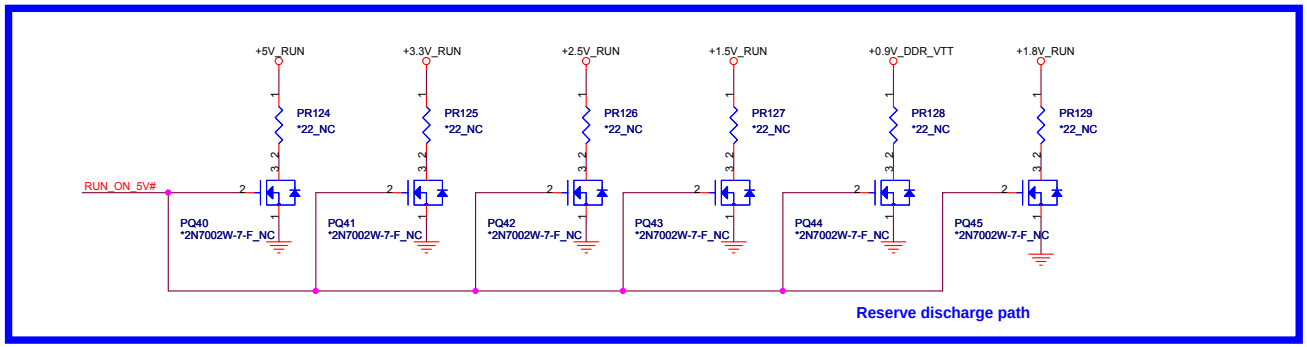



| | | |
|---|---|---|
| QUANTA COMPUTER | | |
| Title | VCCP | |
| Size | Document Number FX2 | Rev 1A |
| Date: 2005/4/21 | Sheet 39 of 47 | |

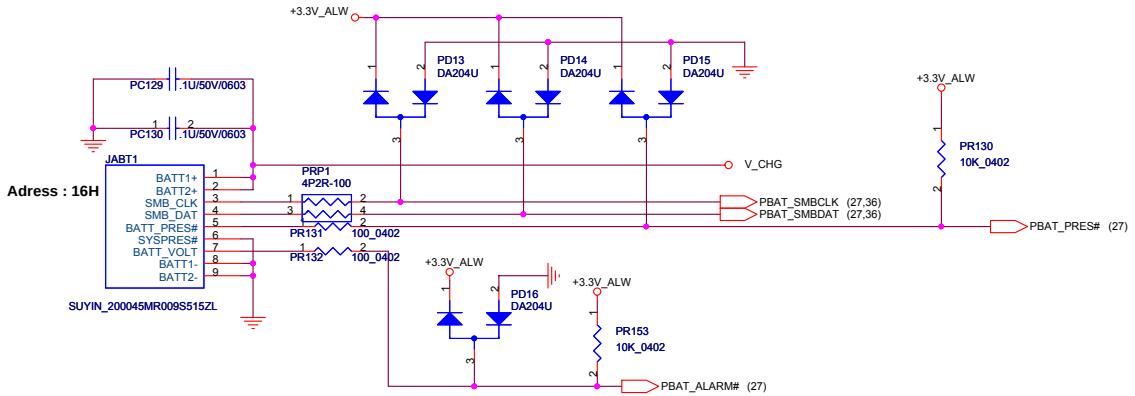


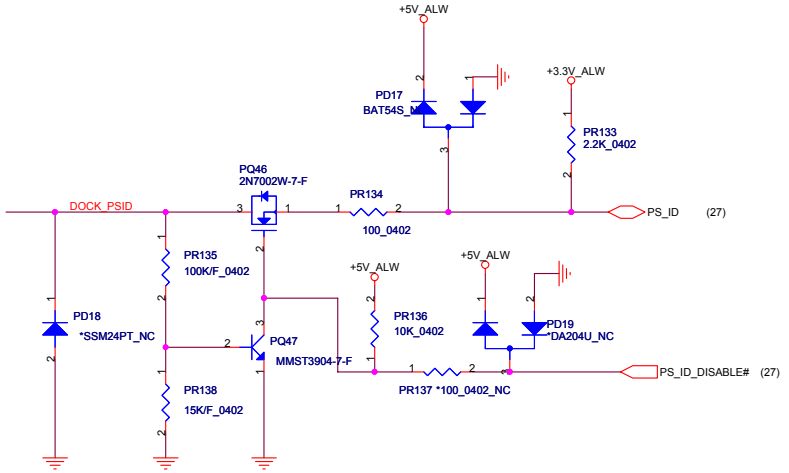



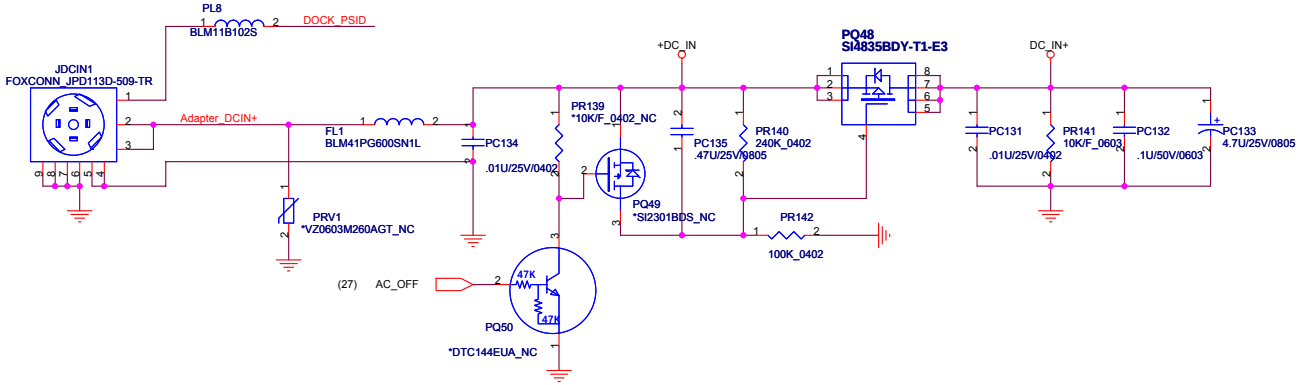




QUANTA COMPUTER

| | | |
|---|---|---|
| Title | RUN POWER SW | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 40 of 47 | |



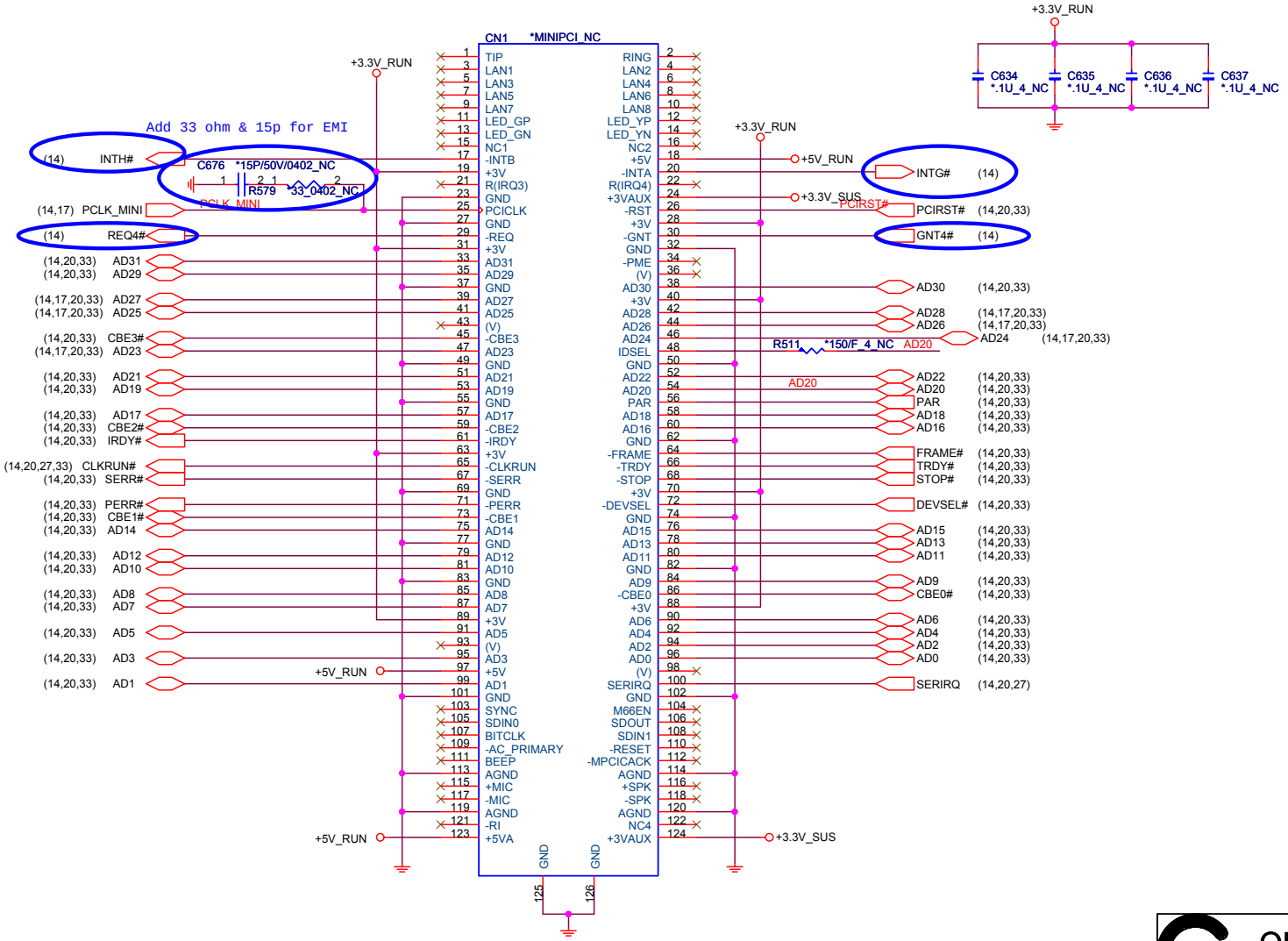




QUANTA COMPUTER

| | | |
|---|---|---|
| Title | DCIN,Batt | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 41 of 47 | |

ID Select : AD20
Interrupt Pin : INTG# , INTH#
Request Indicate : REQ4#
Grant Indicate : GNT4#

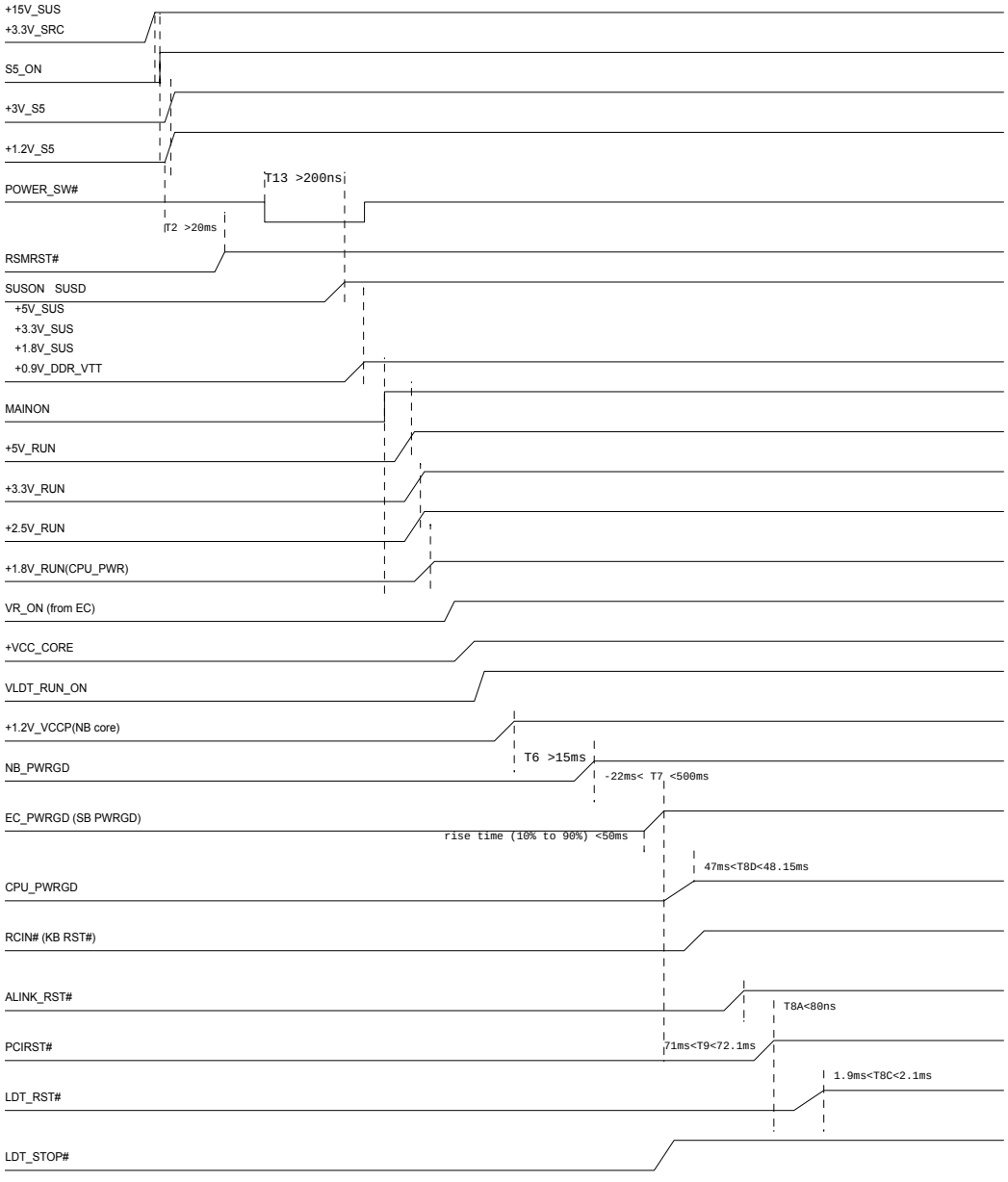
# DEBUG PURPOSE ONLY




MPC

| | | |
|---|---|---|
| QUANTA COMPUTER | | |
| Title | MINI PCI(for debug) | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 42 of 47 | |

# Power On Sequence

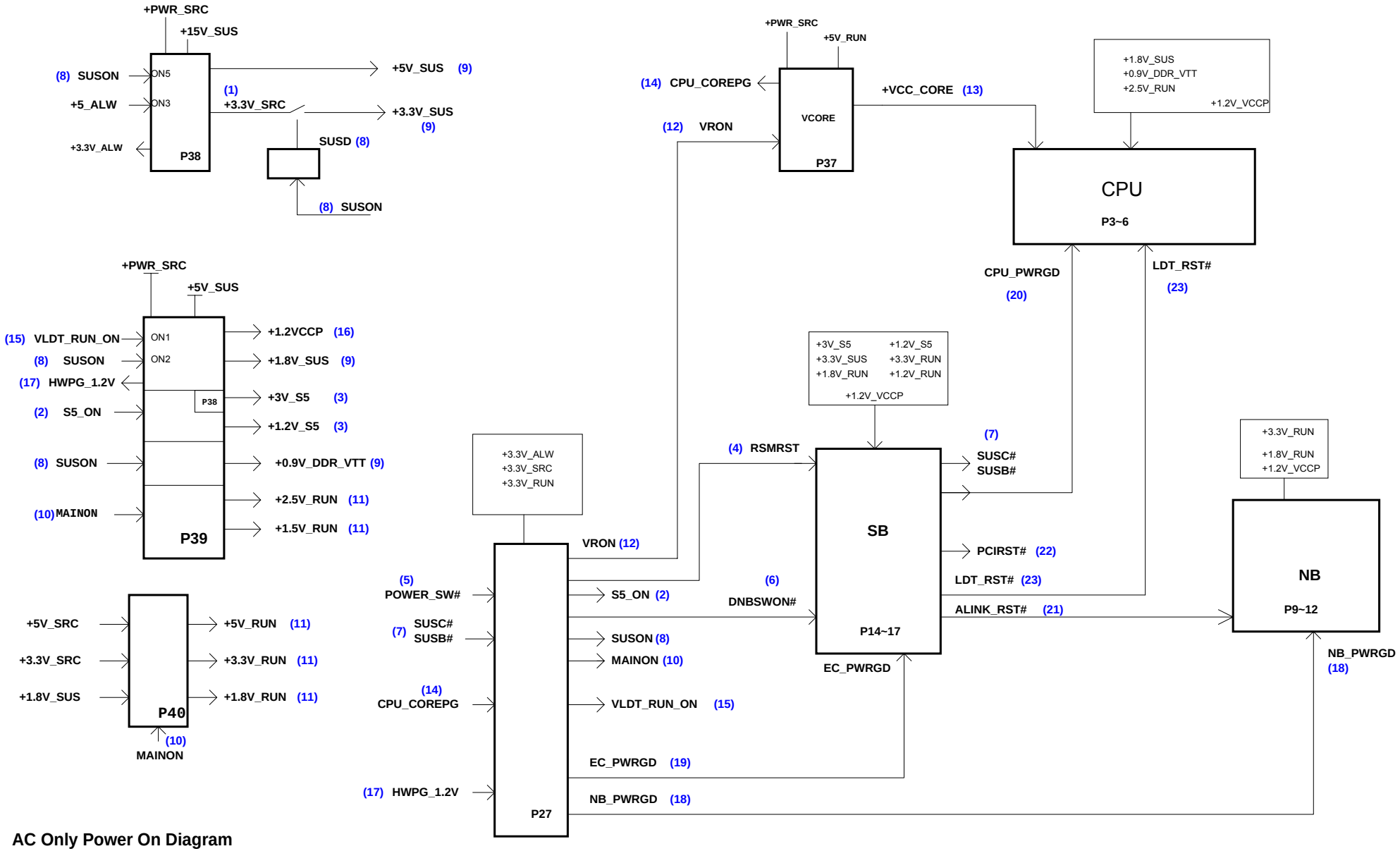



T6: NB core voltage to NB_PWRGD
T7: NB_PWRGD to SB_PWRGD
T8D: SB_PWRGD to CPU_PWRGD

T8A: ALINK_RST# to PCIRST#
T9: SB_PWRGD to PCIRST#
T8C: PCIRST# to LDT_RST#

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | Power On Sequence | |
| Size | Document Number FX2 | Rev 1A |
| Date: Wednesday, May 10, 2006 | Sheet 43 of 47 | |

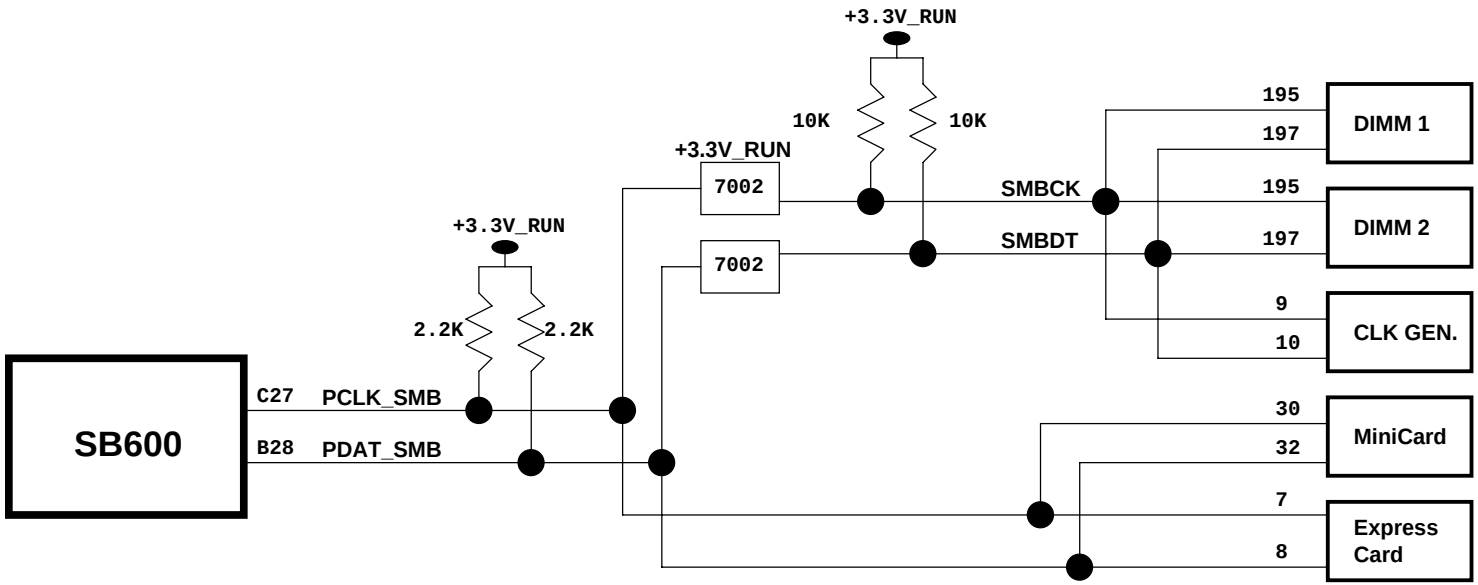


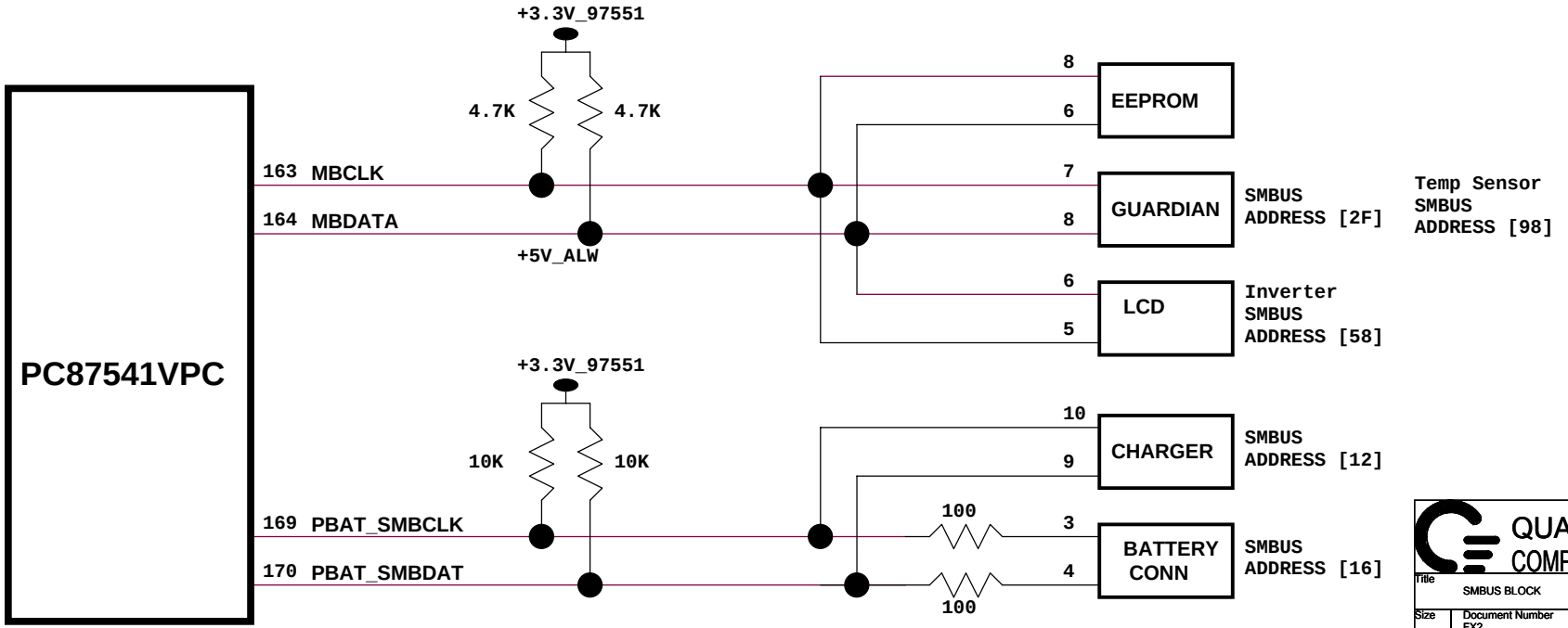

## AC Only Power On Diagram

(1) +3.3V_SRC
(2) S5_ON
(3) +3V_S5, +1.2V_S5
(4) RSMRST
(5) POWER_SW#
(6) DNBSWON#
(7) SUSC#, SUSB#
( 8 ) SUSON, SUSD
( 9 ) +5V_SUS
+0.9V_DDR_VTT, +3.3V_SUS, +1.8V_SUS
(10) MAINON
(11) +5V_RUN, +3.3V_RUN
+2.5V_RUN, +1.8V_RUN, +1.5V_RUN
(12) VRON
(13) +VCC_CORE
(14) CPU_COREPG
(15) VLDT_RUN_ON
(16) +1.2_VCCP
(17) HWPG_1.2V
(18) NB_PWRGD
(19) EC_PWRGD
(20) CPU_PWRGD
(21) ALINK_RST#
(22) PCI_RST#
(23) LDT_RST#

QUANTA COMPUTER

| | | |
|---|---|---|
| Title | Power On Diagram | |
| Size | Document Number FX2 | Rev 1A |
| Date: Thursday, May 04, 2006 | Sheet 44 of 47 | |




QUANTA COMPUTER

| | | |
|---|---|---|
| Title | SMBUS BLOCK | |
| Size | Document Number FX2 | Rev 1A |
| Date: Friday, May 05, 2006 | Sheet 45 of 47 | |