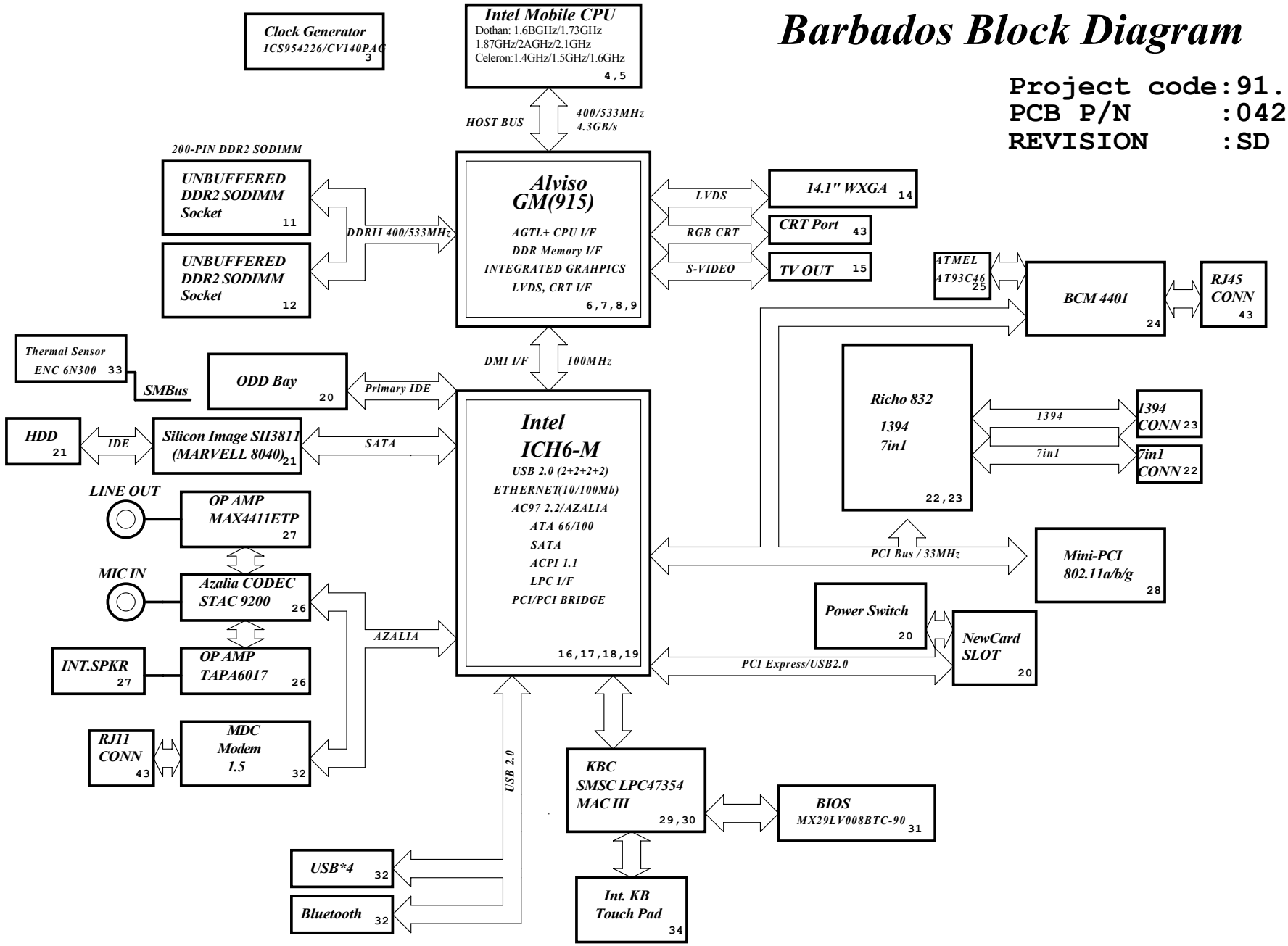
Barbados Block Diagram

Project code:91.4C401.001
PCB P/N :04242
REVISION :SD



System DC/DC MAX8734A 39	
INPUTS	OUTPUTS
PWR_SRC	+5VSUS +3VSRC
Battery Charger MAX1909 42	
PWR_SRC	BATT+
System DC/DC MAX8743 40	
PWR_SRC	+1.05VRUN +1.5VSUS
CPU DC/DC ISL6217 38	
PWR_SRC	VCC_CORE
DDR2 DC/DC TI 51116 41	
PWR_SRC	+1.8VSUS +0.9VRUN +0.9VSUS_DDR2VREF

PCB LAYER
L1:TOP
L2:Signal
L3:GND
L4:Signal
L5:Signal
L6:VCC
L7:GND
L8:BOT

<Core Design>

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Alviso Strapping Signals and Configuration

Pin Name	Strap Description	Configuration page 7
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott **1 = Dothan** (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled** (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V** (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present** (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

For Dothan B stepping

	CPU		NB			CLOCK		
	BSEL1	BSEL0	CFG2	CFG1	CFG0	FS_C	FS_B	FS_A
100MHZ	0	1	1	0	1	1	0	1
133MHZ	0	0	0	0	1	0	0	1

PCI TABLE

DEVICE	IDSEL	IRQ	REQ# / GNT#
LAN Broadcom BCM4401/BCM5507	AD16	PIRQC#	REQ4# / GNT4#
MINIPCI SLOT	AD19	PIRQB# PIRQD#	REQ3# / GNT3#
R5C832	AD17	PIRQA# PIRQC#	REQ1# / GNT1#

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0],ACZ_SYNC, ACZ_SDOUT,ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

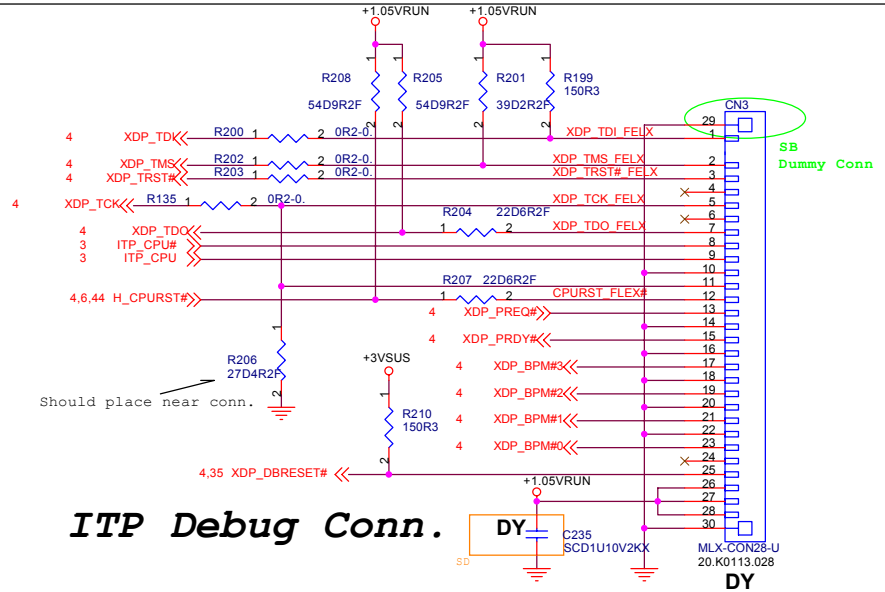
ICH6-M IDE Integrated Series Termination Resistors

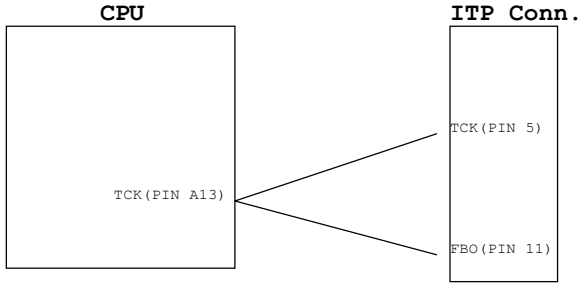
DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

ICH6-M Strapping Signals and Configuration

Pin Name	Strap Description	Note
ACZ_SDOUT	0=Normal(default) 1=XOR Test mode	
ACZ_SYNC	0=Normal(default)	1=Reserved
DPRSLPVR	0=Normal	1=Reserved
EE_CS	0=Normal	1=Reserved
EE_DOUT	0=Normal	1=Reserved
GNT[5]#/GPO[17]#	0=PCI cycles to FWH 1=PCI cycles to LPC (default)	Selects memory range to FWD to out of PCI
GNT(6)#/GPO(16)#	0="Top block swap" mode 1=Normal(default)	"Top block swap" inverts A16 on cycles to FWH
GPIO[25]	0=Internal 2.5V DISEN(default) 1=ENABLE Internal Vcc2_5VRM	
INTVRMEN	0=Internal VccSus1.5V DISEN (default) 1=ENABLE Internal VccSus1.5VVRM	
LINKALERT#	1=Normal(requires external PU)	0=Reserved
REQ[4:1]	XOR Test Chain Selection	Requires external resistors
SATALED#	0=Normal(default)	1=Reserved
SPKR	0=Normal(default) 1=NO Reboot	
TP[3]	0=Enter XOR Test mode 1=Normal(default)	

NOTE: All strap signals are sampled on the rising edge of the ICH6-M's PWROK signal.





+2.5VRUN +2.5VRUN 7,9,14,15,18,36,43,44
+5VRUN +5VRUN 14,15,18,20,21,26,28,30,33,34,36,38,43,44
+12V +12V 14,23,33,36,43,44
+1.5VRUN +1.5VRUN 5,7,9,17,18,20,36,44
VCC_CORE VCC_CORE 5,36,38,44
+1.05VRUN +1.05VRUN 3,4,5,6,7,9,10,16,18,33,36,40,44
LCDVDD LCDVDD 14,44
+3VRUN +3VRUN 3,4,9,11,12,14,15,17,18,19,20,21,22,23,26,27,28,29,30,32,33,35,36,38,43,44

+5VALW +5VALW 14,30,36,39,43,44
+3VALW +3VALW 4,14,20,22,29,30,31,33,34,39,43,44

BATT+ BATT+ 42,43
DC_IN+ DC_IN+ 42,43,44
PWR_SRC PWR_SRC 14,29,38,39,40,41,42,43,44
VCCRTC VCCRTC 16,18,29,33

+0.9VSUS_DDR2VREF +0.9VSUS_DDR2VREF 7,11,12,41,44
+5VSUS +5VSUS 18,26,27,32,33,36,39,40,41,43,44
+3VSUS +3VSUS 14,17,18,19,20,24,25,27,28,32,33,35,36,39,40,41,43,44
+1.5VSUS +1.5VSUS 18,36,40,44

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Title: ITP CONN/Table Of Content

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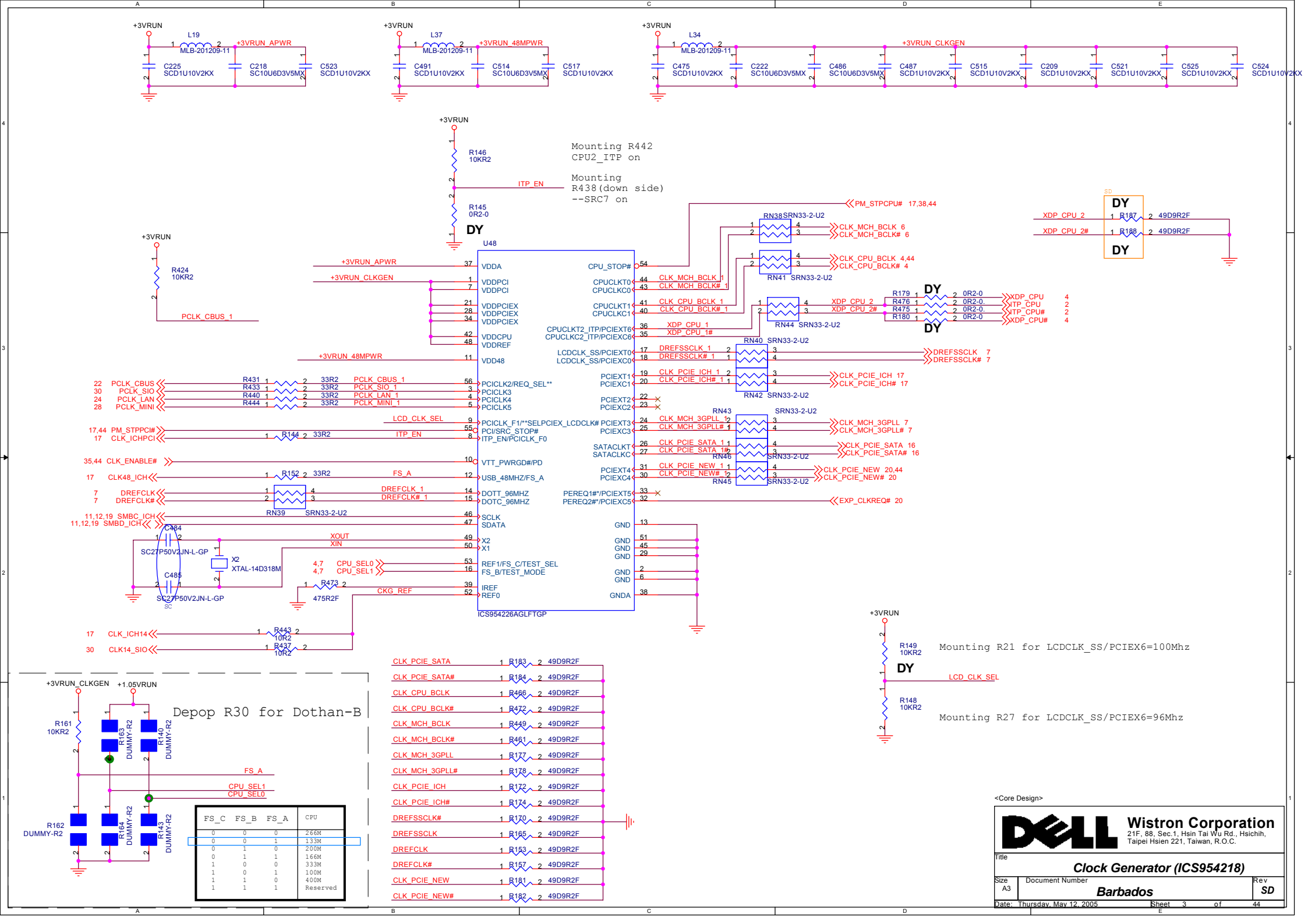
+3VRUN
L19
MLB-201209-11
+3VRUN_APWR
C225 SCD1U10V2KX
C218 SC10U6D3V5MX
C523 SCD1U10V2KX
L37
MLB-201209-11
+3VRUN_48MPWR
C491 SCD1U10V2KX
C514 SC10U6D3V5MX
C517 SCD1U10V2KX
L34
MLB-201209-11
+3VRUN_CLKGEN
C475 SCD1U10V2KX
C222 SC10U6D3V5MX
C486 SC10U6D3V5MX
C487 SCD1U10V2KX
C515 SCD1U10V2KX
C209 SCD1U10V2KX
C521 SCD1U10V2KX
C525 SCD1U10V2KX
C524 SCD1U10V2KX
R146 10KR2
ITP_EN
R145 0R2-0
DY
Mounting R442
CPU2_ITP on
Mounting
R438(down side)
--SRC7 on
R424 10KR2
PCLK_CBUS_1
U48
+3VRUN_APWR
+3VRUN_CLKGEN
+3VRUN_48MPWR
VDDA
VDDPCI
VDDPCIEX
VDDCPU
VDDREF
VDD48
PCICLK2/REQ_SEL**
PCICLK3
PCICLK4
PCICLK5
PCICLK_F1/**SELPCIEX_LCDCLK#
PCI/SRC_STOP#
ITP_EN/PCICLK_F0
VTT_PWRGD#/PD
USB_48MHZ/FS_A
DOTT_96MHZ
DOTC_96MHZ
SCLK
SDATA
X2
X1
REF1/FS_C/TEST_SEL
FS_B/TEST_MODE
IREF
REF0
CPU_STOP#
CPUCLKT0
CPUCLKC0
CPUCLKT1
CPUCLKC1
CPUCLKT2_ITP/PCIEXT6
CPUCLKC2_ITP/PCIEXC6
LCDCLK_SS/PCIEXT0
LCDCLK_SS/PCIEXC0
PCIEXT1
PCIEXC1
PCIEXT2
PCIEXC2
PCIEXT3
PCIEXC3
SATACLKT
SATACLKC
PCIEXT4
PCIEXC4
PEREQ1#/PCIEXT5
PEREQ2#/PCIEXC5
GND
GNDA
ICS954226AGLFTGP
PM_STPCPU# 17,38,44
RN38 SRN33-2-U2
CLK_MCH_BCLK 6
CLK_MCH_BCLK# 6
CLK_CPU_BCLK 4,44
CLK_CPU_BCLK# 4
RN41 SRN33-2-U2
XDP_CPU_2
XDP_CPU_2#
RN44 SRN33-2-U2
R179 R476 R475 R180 0R2-0
XDP_CPU 4
ITP_CPU 2
ITP_CPU# 2
XDP_CPU# 4
RN40 SRN33-2-U2
DREFSSCLK 7
DREFSSCLK# 7
CLK_PCIE_ICH 17
CLK_PCIE_ICH# 17
RN42 SRN33-2-U2
RN43 SRN33-2-U2
CLK_MCH_3GPLL 7
CLK_MCH_3GPLL# 7
CLK_PCIE_SATA 16
CLK_PCIE_SATA# 16
RN46 SRN33-2-U2
CLK_PCIE_NEW 20,44
CLK_PCIE_NEW# 20
RN45 SRN33-2-U2
EXP_CLKREQ# 20
R187 49D9R2F
R188 49D9R2F
SD
R431 R433 R440 R444 33R2
PCLK_CBUS_1
PCLK_SIO_1
PCLK_LAN_1
PCLK_MINI_1
22 PCLK_CBUS
30 PCLK_SIO
24 PCLK_LAN
28 PCLK_MINI
17,44 PM_STPPCI#
17 CLK_ICHPCI
R144 33R2
35,44 CLK_ENABLE#
17 CLK48_ICH
R152 33R2
FS_A
7 DREFCLK
7 DREFCLK#
DREFCLK_1
DREFCLK#_1
RN39 SRN33-2-U2
11,12,19 SMBC_ICH
11,12,19 SMBD_ICH
C484
C485
SC27P50V2JN-L-GP
XOUT
XIN
X2
XTAL-14D318M
4,7 CPU_SEL0
4,7 CPU_SEL1
R473 475R2F
CKG_REF
17 CLK_ICH14
30 CLK14_SIO
R443 10R2
R437 10R2
+3VRUN_CLKGEN
+1.05VRUN
Depop R30 for Dothan-B
R161 10KR2
R163 DUMMY-R2
R140 DUMMY-R2
R162 DUMMY-R2
R164 DUMMY-R2
R143 DUMMY-R2
FS_A
CPU_SEL1
CPU_SEL0
FS_C FS_B FS_A CPU
0 0 0 266M
0 0 1 133M
0 1 0 200M
0 1 1 166M
1 0 0 333M
1 0 1 100M
1 1 0 400M
1 1 1 Reserved
CLK_PCIE_SATA R183 49D9R2F
CLK_PCIE_SATA# R184 49D9R2F
CLK_CPU_BCLK R466 49D9R2F
CLK_CPU_BCLK# R472 49D9R2F
CLK_MCH_BCLK R449 49D9R2F
CLK_MCH_BCLK# R461 49D9R2F
CLK_MCH_3GPLL R177 49D9R2F
CLK_MCH_3GPLL# R178 49D9R2F
CLK_PCIE_ICH R172 49D9R2F
CLK_PCIE_ICH# R174 49D9R2F
DREFSSCLK# R170 49D9R2F
DREFSSCLK R165 49D9R2F
DREFCLK R153 49D9R2F
DREFCLK# R157 49D9R2F
CLK_PCIE_NEW R181 49D9R2F
CLK_PCIE_NEW# R182 49D9R2F
+3VRUN
R149 10KR2
DY
LCD_CLK_SEL
R148 10KR2
Mounting R21 for LCDCLK_SS/PCIEX6=100Mhz
Mounting R27 for LCDCLK_SS/PCIEX6=96Mhz
<Core Design>
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Title
Clock Generator (ICS954218)
Size A3
Document Number
Barbados
Rev SD
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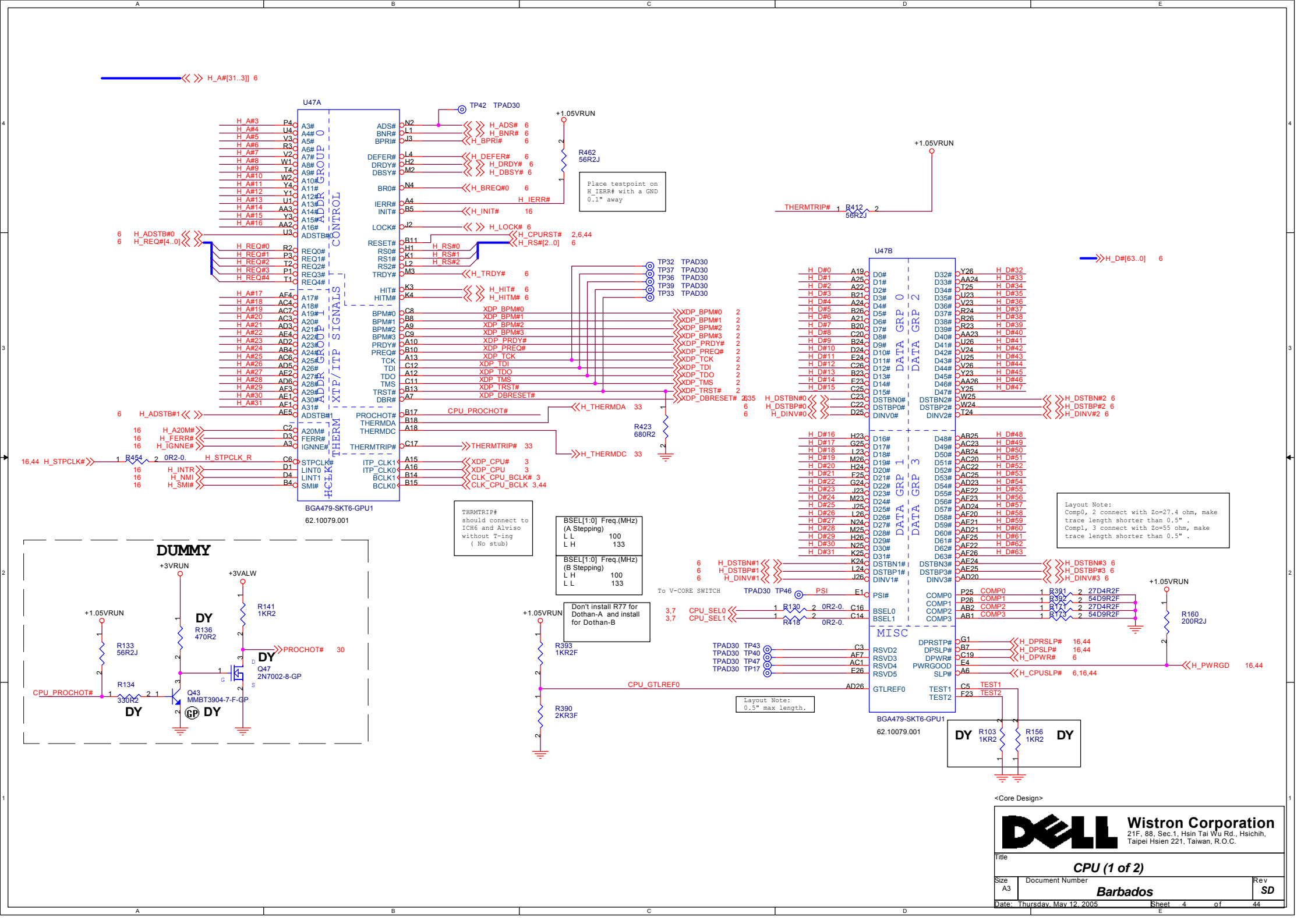

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Title: ***CPU (1 of 2)***

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At Dothan 400Mhz CPU application, POWER is 1.8V.
At Dothan 533Mhz CPU application, POWER is 1.5V.
At Celeron CPU .13 application, POWER is 1.8V.
At Celeron CPU .09 application, POWER is 1.5V.

U47C

BGA479-SKT6-GPU1
62.10079.001

R102 0R3-U
C130 SCD01U16V2KX
C128 SC10U6D3V5MX
R139 0R2-0
TP_VCCA1 TP_VCCA2 TP_VCCA3
TP45 TP44 TP142 TPAD30
CPU_D10
H_VID0 H_VID1 H_VID2 H_VID3 H_VID4 H_VID5
TP_VCCSENSE TP_VSSSENSE
R151 R147 54D9R2F NO STUFF

0.1u *10 150u *1
C211 C212 C210 C192 C187 C188 C181 C151 C152 C153 SCD1U10V2KX
TC9 ST220U2D5VD
Dummy 2 by layout

270u *4
10u *35
C479 C480 C493 C200 C184 C163 C190 C164 C140 C202 C196 C492 C167 C198 C482 C204 C172 C495 C494 C199 SC10U6D3V5MX

C194 C195 C214 C481 C168 C175 C177 C169 C193 C180 C191 C201 C165 C170 C171 SC10U6D3V5MX

Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

U47D

BGA479-SKT6-GPU1
62.10079.001

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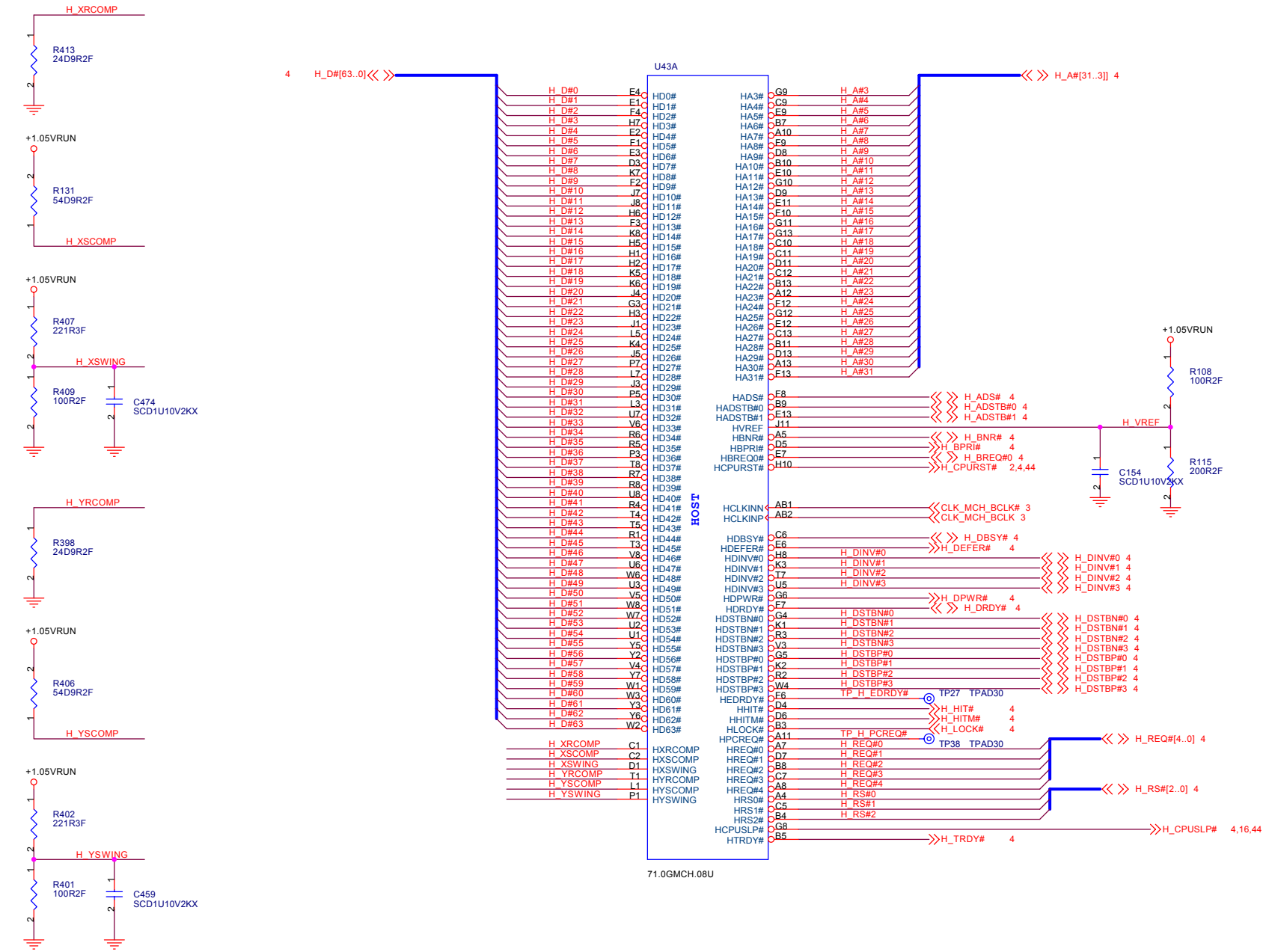

Place them near to the chip

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Title: GMCH (1 of 5)

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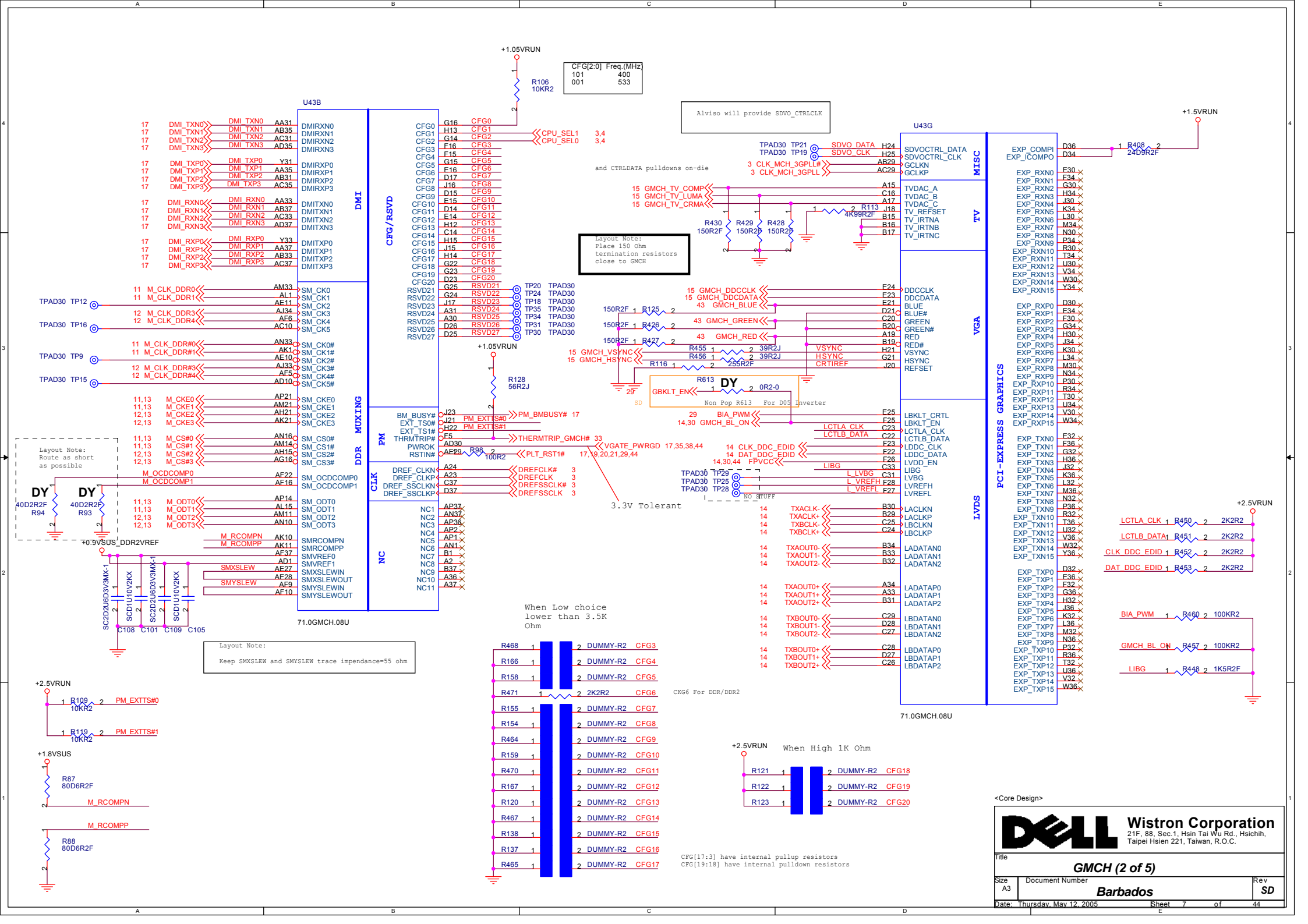
U43B
DMI
CRG/RSVD
PM
DDR MUXING
CLK
NC
U43G
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
+1.05VRUN
+1.5VRUN
+2.5VRUN
+1.8VSUS
+0.9VSUS_DDR2VREF
CFG[2:0] Freq.(MHz)
101 400
001 533
Alviso will provide SDVO_CTRLCLK
and CTRLDATA pulldowns on-die
Layout Note: Place 150 Ohm termination resistors close to GMCH
Layout Note: Route as short as possible
Layout Note: Keep SMXSLEW and SMYSLEW trace impendance=55 ohm
When Low choice lower than 3.5K Ohm
When High 1K Ohm
3.3V Tolerant
DY
Non Pop R613 For D05 Inverter
NO STUFF
CKG6 For DDR/DDR2
CFG[17:3] have internal pullup resistors
CFG[19:18] have internal pulldown resistors
71.0GMCH.08U
<Core Design>
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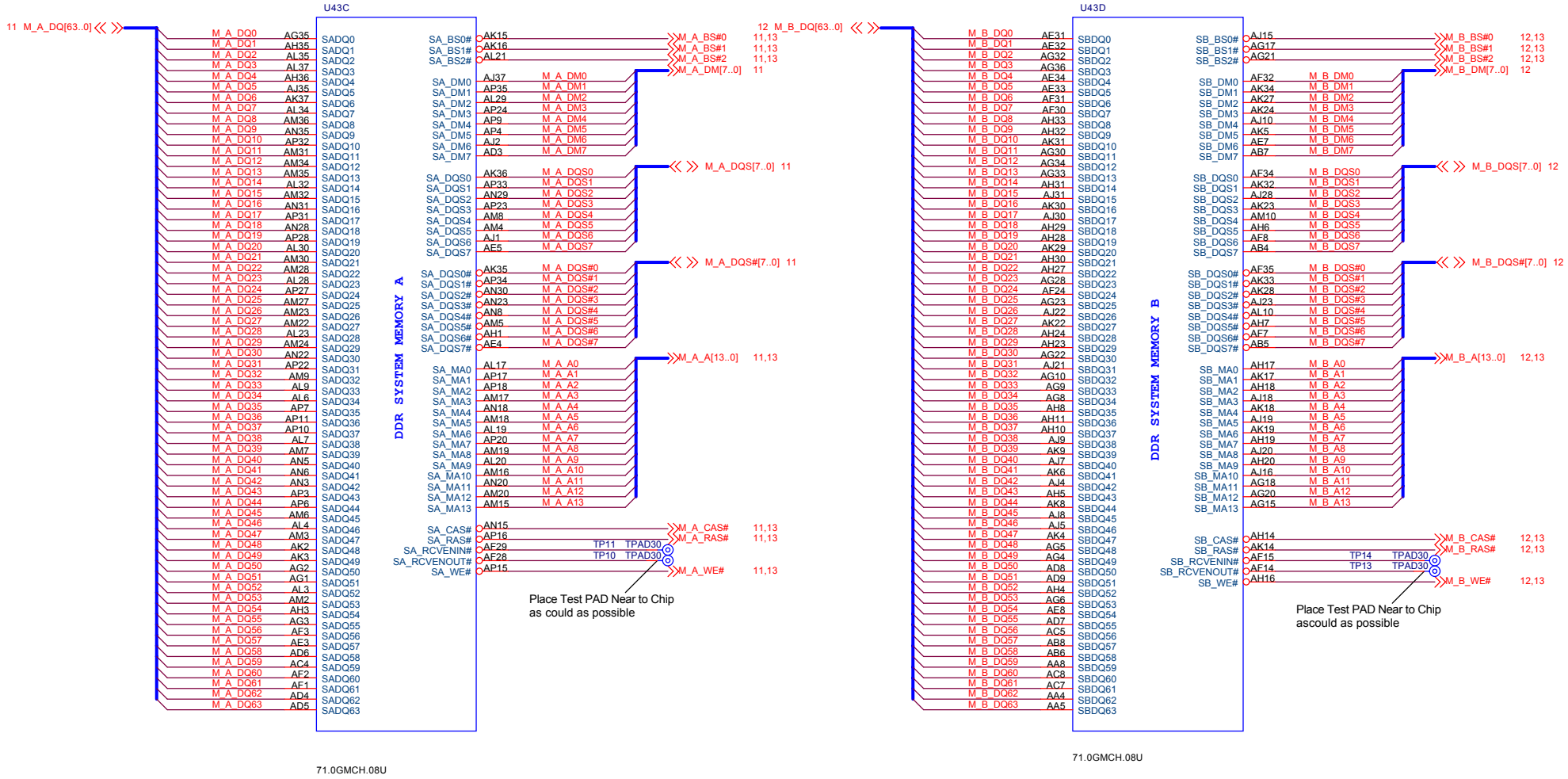

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Title: ***GMCH (3 of 5)***

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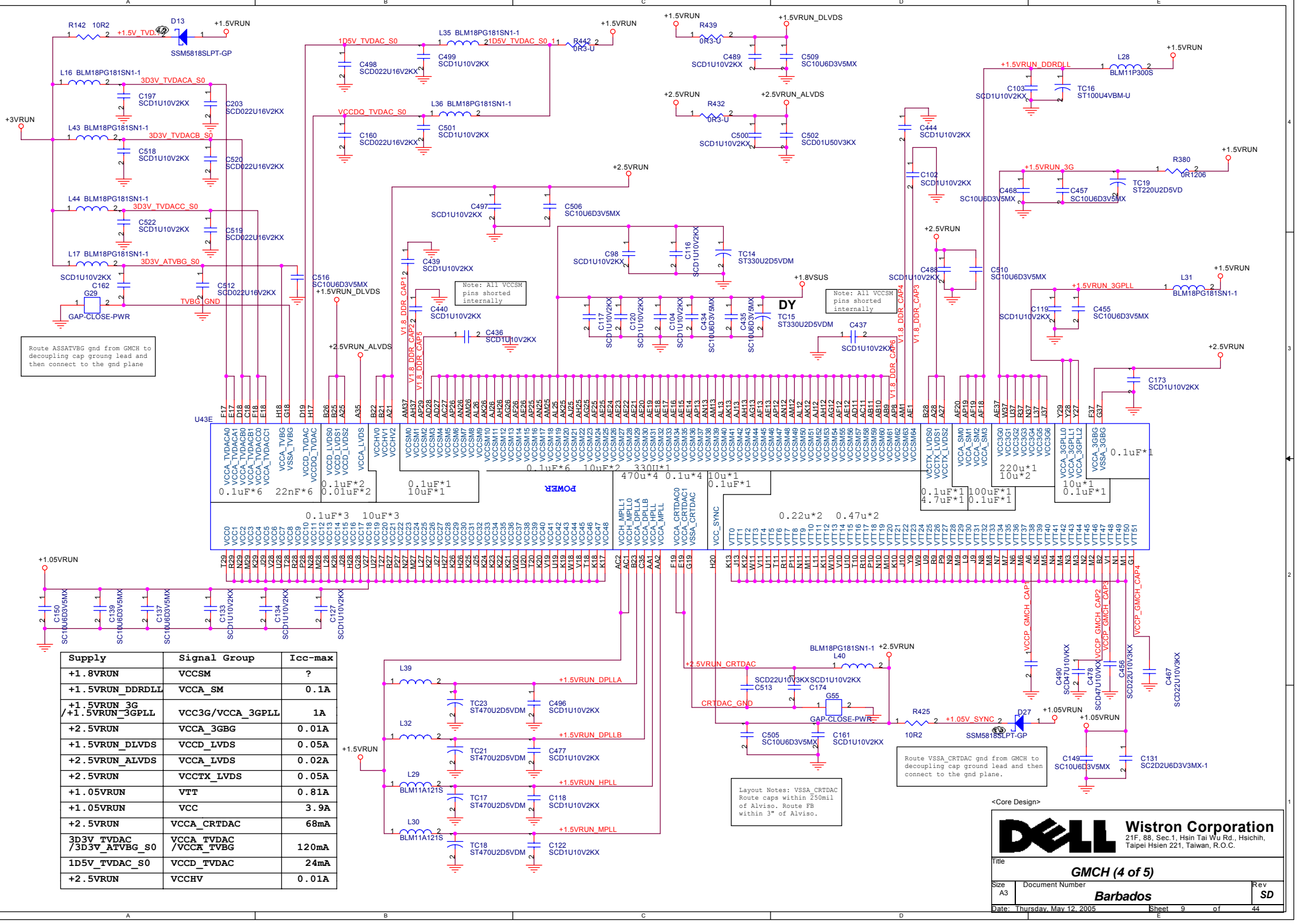

Supply	Signal Group	Icc-max
+1.8VRUN	VCCSM	?
+1.5VRUN_DDRDLL	VCCA_SM	0.1A
+1.5VRUN_3G /+1.5VRUN_3GPLL	VCC3G/VCCA_3GPLL	1A
+2.5VRUN	VCCA_3GBG	0.01A
+1.5VRUN_DLVDS	VCCD_LVDS	0.05A
+2.5VRUN_ALVDS	VCCA_LVDS	0.02A
+2.5VRUN	VCCTX_LVDS	0.05A
+1.05VRUN	VTT	0.81A
+1.05VRUN	VCC	3.9A
+2.5VRUN	VCCA_CRTDAC	68mA
3D3V_TVDAC /3D3V_ATVBG_S0	VCCA_TVDAC /VCCA_TVBG	120mA
1D5V_TVDAC_S0	VCCD_TVDAC	24mA
+2.5VRUN	VCCHV	0.01A

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Title: GMCH (4 of 5)

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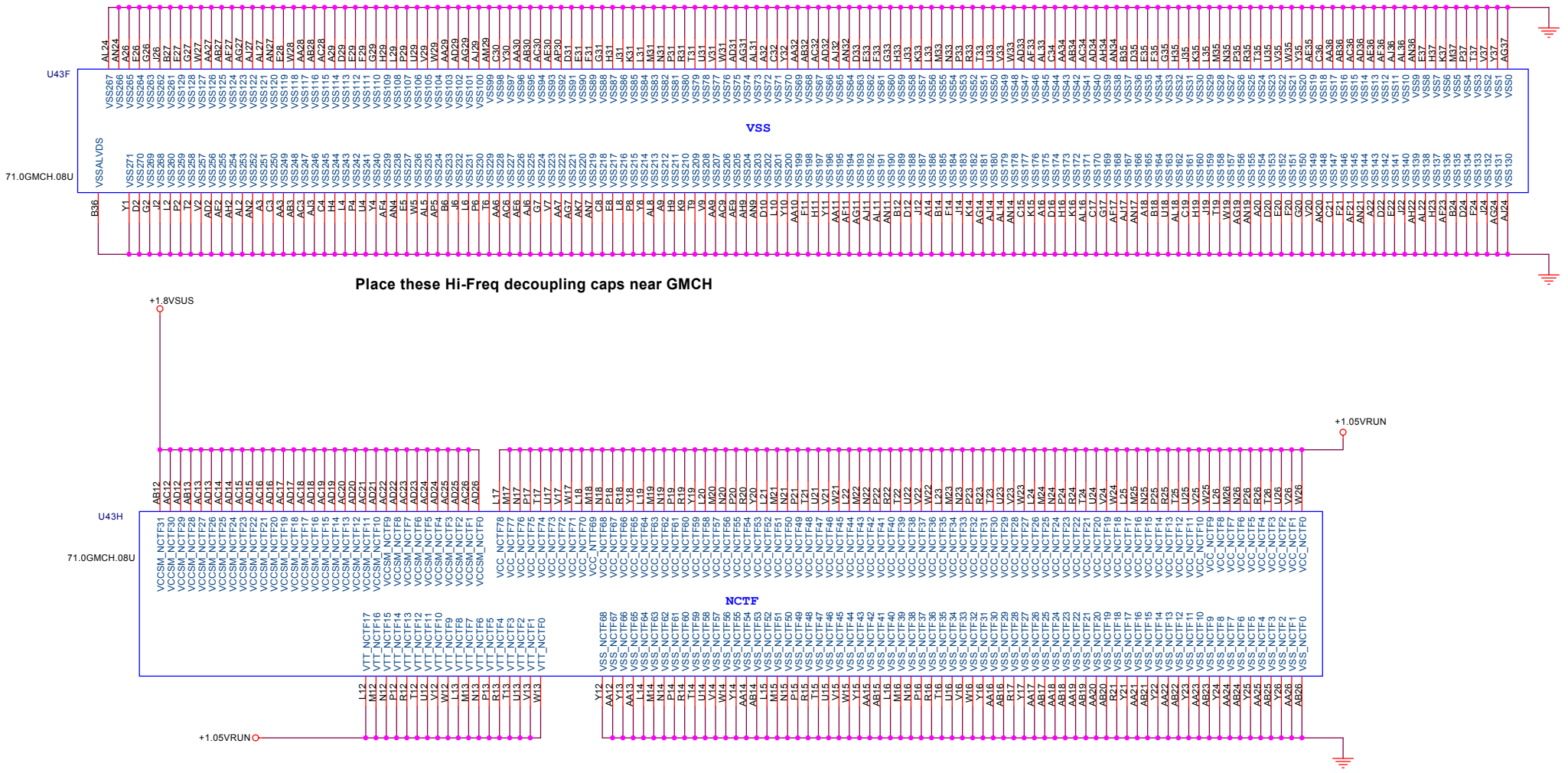

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Title	*GMCH (5 of 5)*	
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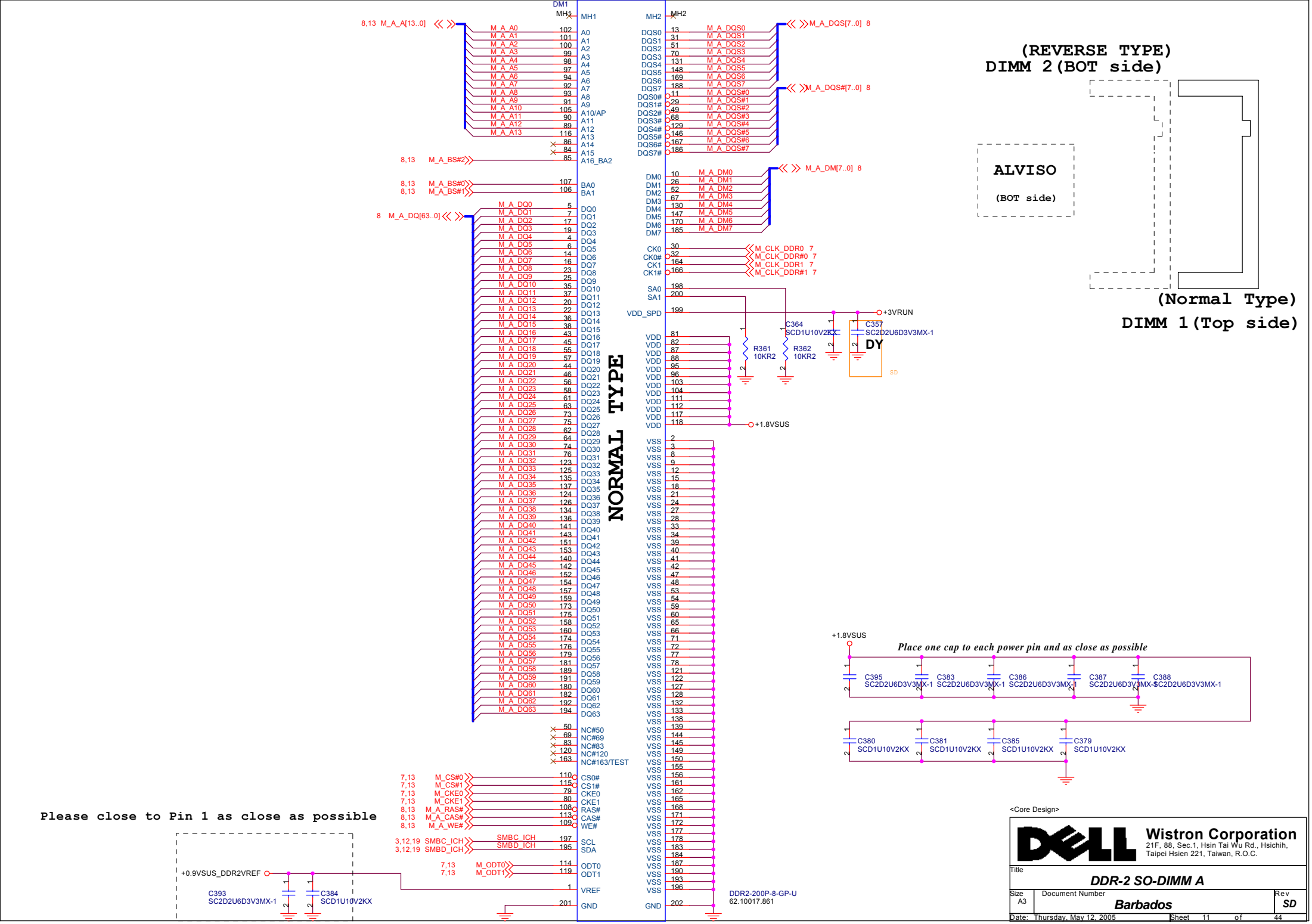
DM1
MH1
MH2
NORMAL TYPE
(REVERSE TYPE)
DIMM 2(BOT side)
ALVISO
(BOT side)
(Normal Type)
DIMM 1(Top side)
DY
SD
+3VRUN
+1.8VSUS
+0.9VSUS_DDR2VREF
Place one cap to each power pin and as close as possible
Please close to Pin 1 as close as possible
DDR2-200P-8-GP-U
62.10017.861
<Core Design>
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR-2 SO-DIMM A
Size A3
Document Number
Barbados
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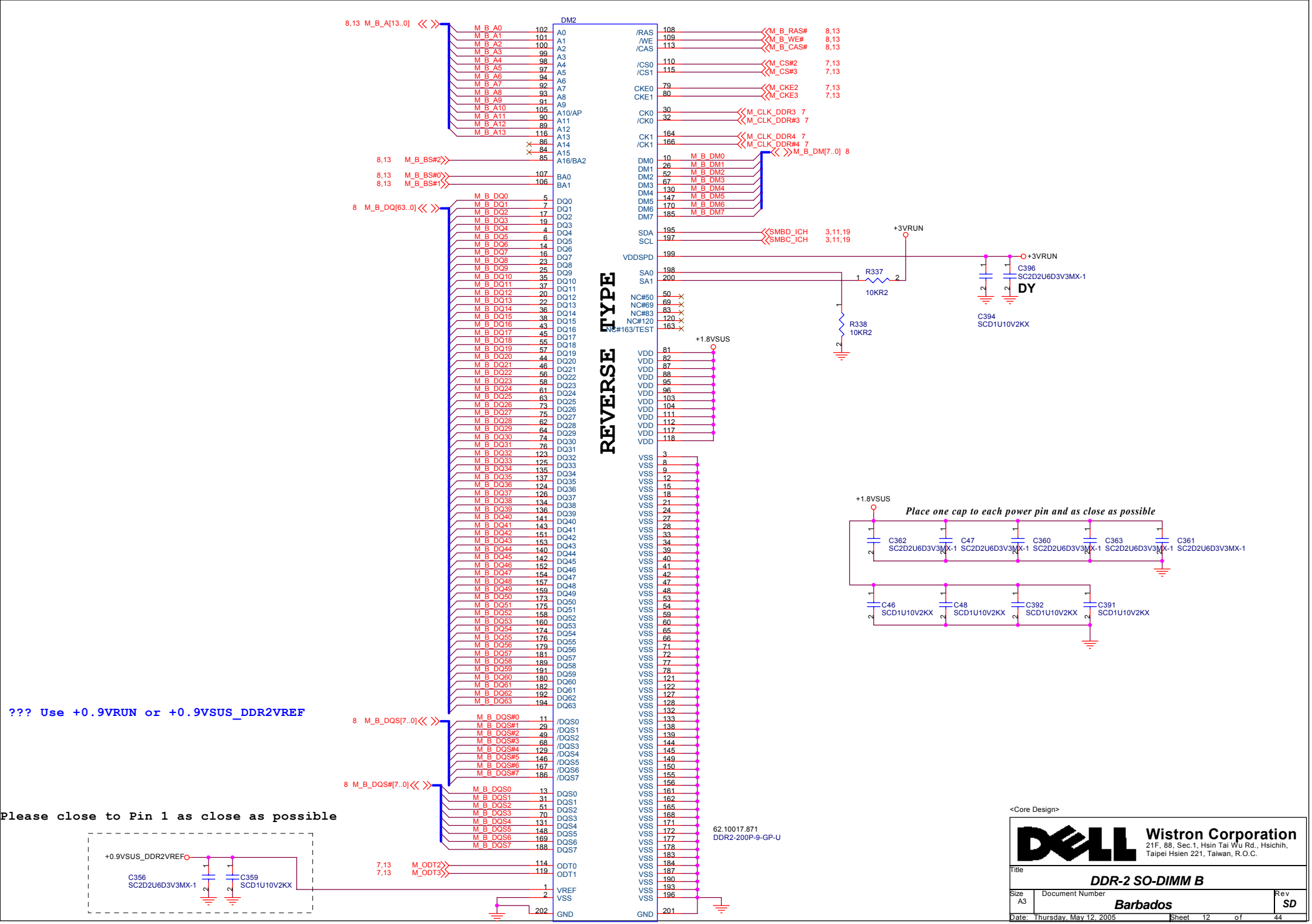
DM2
REVERSE TYPE
8,13 M_B_A[13..0]
M_B_A0 102
M_B_A1 101
M_B_A2 100
M_B_A3 99
M_B_A4 98
M_B_A5 97
M_B_A6 94
M_B_A7 92
M_B_A8 93
M_B_A9 91
M_B_A10 105
M_B_A11 90
M_B_A12 89
M_B_A13 116
A14 86
A15 84
A16/BA2 85
8,13 M_B_BS#2
8,13 M_B_BS#0 107
8,13 M_B_BS#1 106
BA0
BA1
8 M_B_DQ[63..0]
M_B_DQ0 5
M_B_DQ1 7
M_B_DQ2 17
M_B_DQ3 19
M_B_DQ4 4
M_B_DQ5 6
M_B_DQ6 14
M_B_DQ7 16
M_B_DQ8 23
M_B_DQ9 25
M_B_DQ10 35
M_B_DQ11 37
M_B_DQ12 20
M_B_DQ13 22
M_B_DQ14 36
M_B_DQ15 38
M_B_DQ16 43
M_B_DQ17 45
M_B_DQ18 55
M_B_DQ19 57
M_B_DQ20 44
M_B_DQ21 46
M_B_DQ22 56
M_B_DQ23 58
M_B_DQ24 61
M_B_DQ25 63
M_B_DQ26 73
M_B_DQ27 75
M_B_DQ28 62
M_B_DQ29 64
M_B_DQ30 74
M_B_DQ31 76
M_B_DQ32 123
M_B_DQ33 125
M_B_DQ34 135
M_B_DQ35 137
M_B_DQ36 124
M_B_DQ37 126
M_B_DQ38 134
M_B_DQ39 136
M_B_DQ40 141
M_B_DQ41 143
M_B_DQ42 151
M_B_DQ43 153
M_B_DQ44 140
M_B_DQ45 142
M_B_DQ46 152
M_B_DQ47 154
M_B_DQ48 157
M_B_DQ49 159
M_B_DQ50 173
M_B_DQ51 175
M_B_DQ52 158
M_B_DQ53 160
M_B_DQ54 174
M_B_DQ55 176
M_B_DQ56 179
M_B_DQ57 181
M_B_DQ58 189
M_B_DQ59 191
M_B_DQ60 180
M_B_DQ61 182
M_B_DQ62 192
M_B_DQ63 194
8 M_B_DQS[7..0]
M_B_DQS#0 11
M_B_DQS#1 29
M_B_DQS#2 49
M_B_DQS#3 68
M_B_DQS#4 129
M_B_DQS#5 146
M_B_DQS#6 167
M_B_DQS#7 186
8 M_B_DQS#[7..0]
M_B_DQS0 13
M_B_DQS1 31
M_B_DQS2 51
M_B_DQS3 70
M_B_DQS4 131
M_B_DQS5 148
M_B_DQS6 169
M_B_DQS7 188
7,13 M_ODT2 114
7,13 M_ODT3 119
VREF 1
VSS 2
GND 202
/RAS 108
/WE 109
/CAS 113
M_B_RAS# 8,13
M_B_WE# 8,13
M_B_CAS# 8,13
/CS0 110
/CS1 115
M_CS#2 7,13
M_CS#3 7,13
CKE0 79
CKE1 80
M_CKE2 7,13
M_CKE3 7,13
CK0 30
/CK0 32
M_CLK_DDR3 7
M_CLK_DDR#3 7
CK1 164
/CK1 166
M_CLK_DDR4 7
M_CLK_DDR#4 7
M_B_DM[7..0] 8
DM0 10
DM1 26
DM2 52
DM3 67
DM4 130
DM5 147
M_B_DM0
M_B_DM1
M_B_DM2
M_B_DM3
M_B_DM4
M_B_DM5
M_B_DM6
M_B_DM7
DM6 170
DM7 185
SDA 195
SCL 197
SMBD_ICH 3,11,19
SMBC_ICH 3,11,19
VDDSPD 199
SA0 198
SA1 200
NC#50 50
NC#69 69
NC#83 83
NC#120 120
NC#163/TEST 163
+3VRUN
R337
10KR2
R338
10KR2
C396
SC2D2U6D3V3MX-1
DY
C394
SCD1U10V2KX
+1.8VSUS
VDD 81
VDD 82
VDD 87
VDD 88
VDD 95
VDD 96
VDD 103
VDD 104
VDD 111
VDD 112
VDD 117
VDD 118
VSS 3
VSS 8
VSS 9
VSS 12
VSS 15
VSS 18
VSS 21
VSS 24
VSS 27
VSS 28
VSS 33
VSS 34
VSS 39
VSS 40
VSS 41
VSS 42
VSS 47
VSS 48
VSS 53
VSS 54
VSS 59
VSS 60
VSS 65
VSS 66
VSS 71
VSS 72
VSS 77
VSS 78
VSS 121
VSS 122
VSS 127
VSS 128
VSS 132
VSS 133
VSS 138
VSS 139
VSS 144
VSS 145
VSS 149
VSS 150
VSS 155
VSS 156
VSS 161
VSS 162
VSS 165
VSS 168
VSS 171
VSS 172
VSS 177
VSS 178
VSS 183
VSS 184
VSS 187
VSS 190
VSS 193
VSS 196
GND 201
62.10017.871
DDR2-200P-9-GP-U
Place one cap to each power pin and as close as possible
C362 SC2D2U6D3V3MX-1
C47 SC2D2U6D3V3MX-1
C360 SC2D2U6D3V3MX-1
C363 SC2D2U6D3V3MX-1
C361 SC2D2U6D3V3MX-1
C46 SCD1U10V2KX
C48 SCD1U10V2KX
C392 SCD1U10V2KX
C391 SCD1U10V2KX
??? Use +0.9VRUN or +0.9VSUS_DDR2VREF
Please close to Pin 1 as close as possible
+0.9VSUS_DDR2VREF
C356 SC2D2U6D3V3MX-1
C359 SCD1U10V2KX
<Core Design>
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Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR-2 SO-DIMM B
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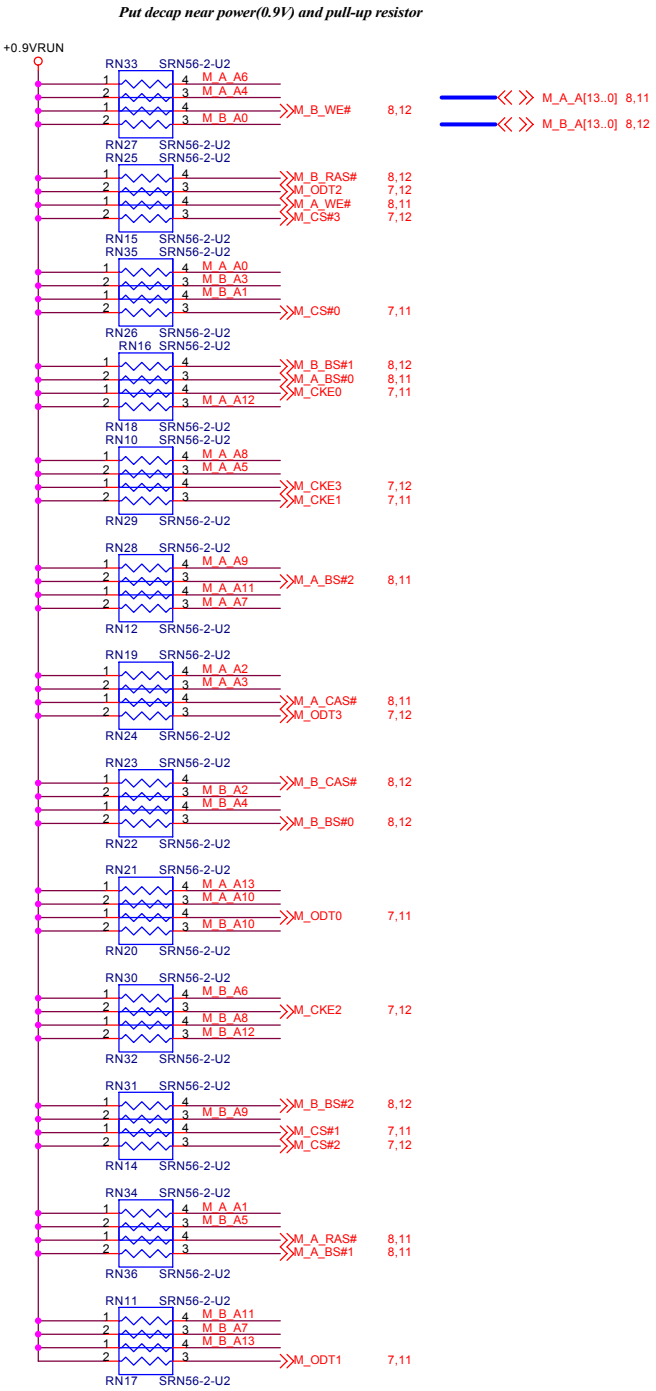
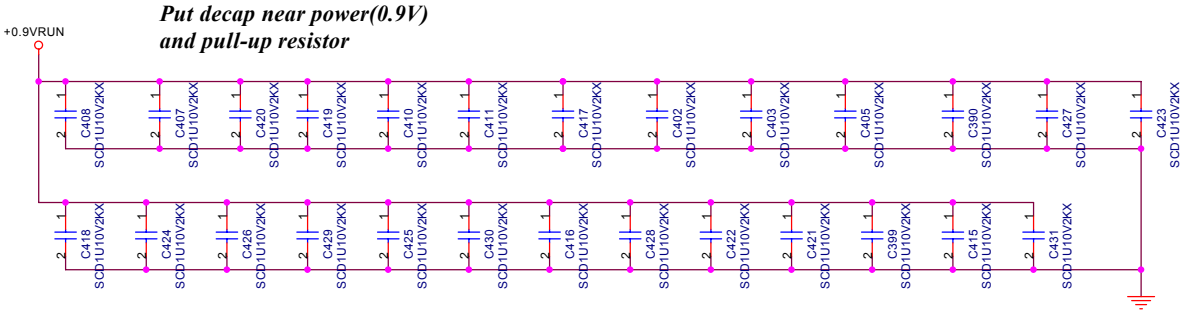
PARALLEL TERMINATION



Decoupling Capacitor



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Title: DDR-2 TERMINATION / STRAPS

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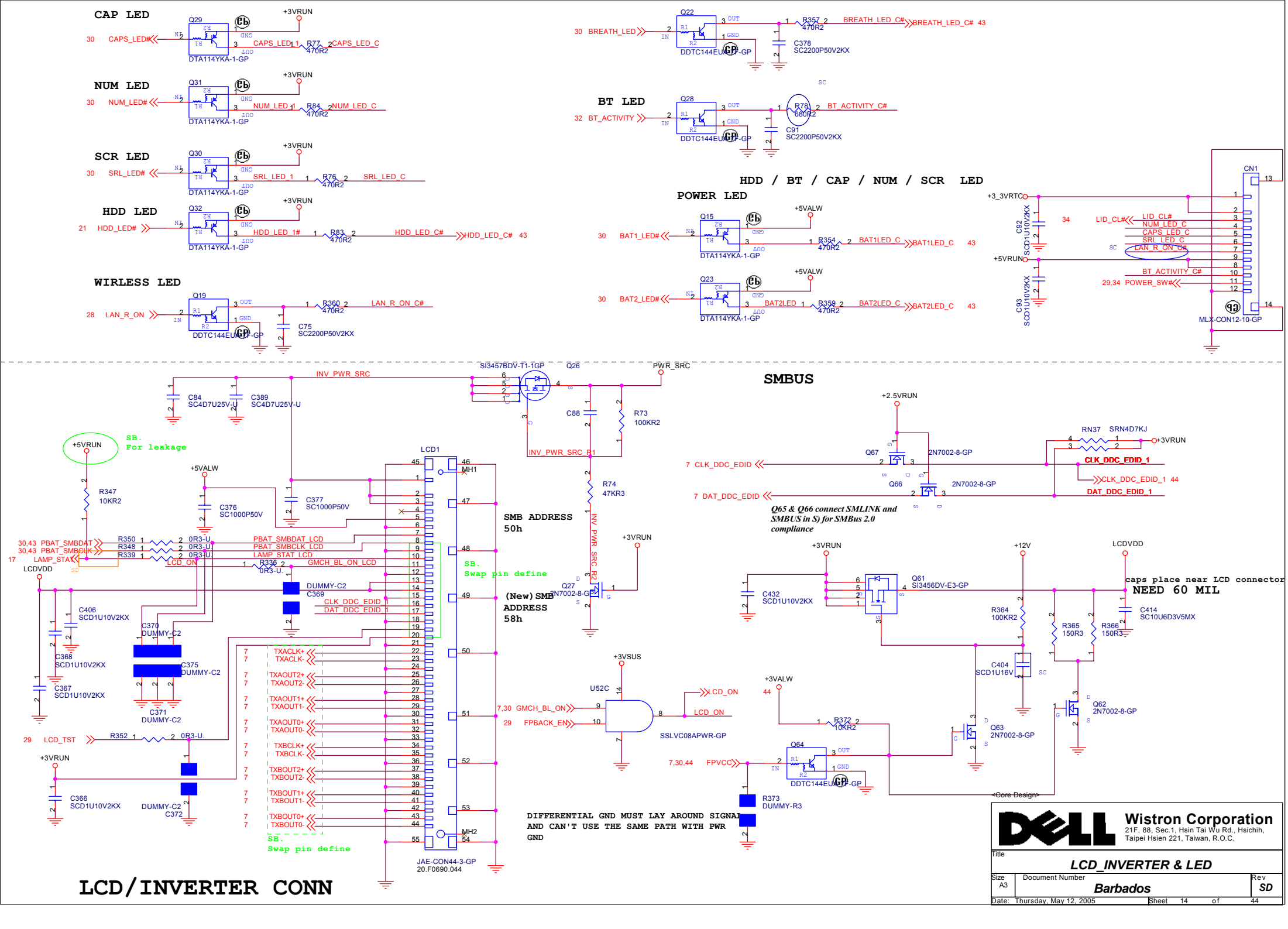
CAP LED
NUM LED
SCR LED
HDD LED
WIRLESS LED
BT LED
POWER LED
HDD / BT / CAP / NUM / SCR LED
SMBUS
LCD/INVERTER CONN
SB. For leakage
SB. Swap pin define
SMB ADDRESS 50h
(New) SMB ADDRESS 58h
DIFFERENTIAL GND MUST LAY AROUND SIGNAL AND CAN'T USE THE SAME PATH WITH PWR GND
caps place near LCD connector NEED 60 MIL
Q65 & Q66 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance
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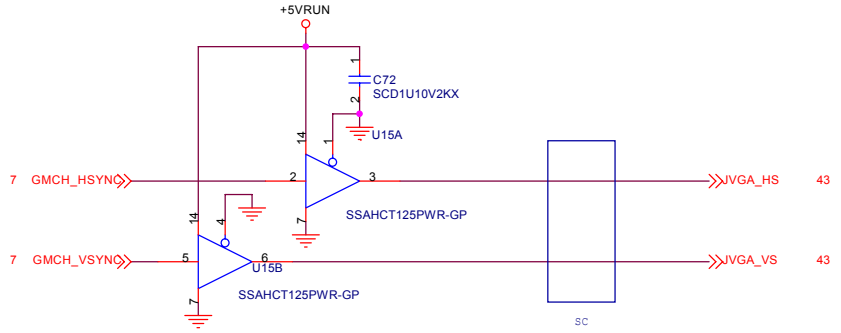
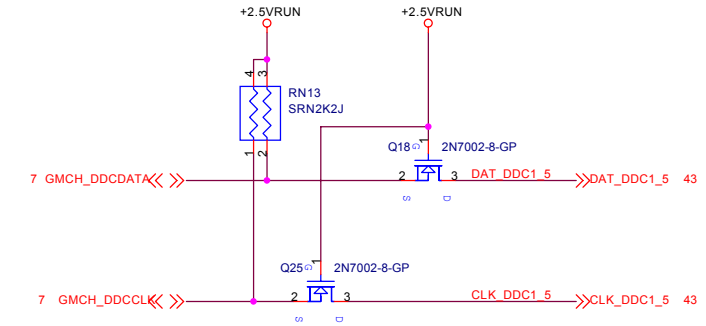
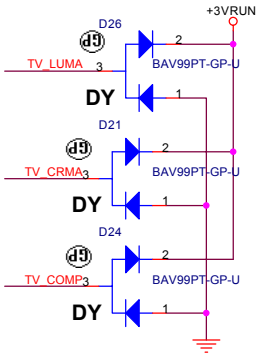
LCD_INVERTER & LED
Barbados
Thursday, May 12, 2005



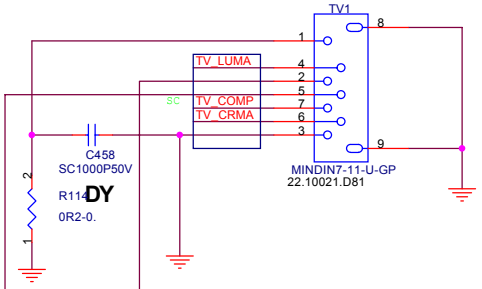
DDC_CLK & DATE LEVEL SHIFT

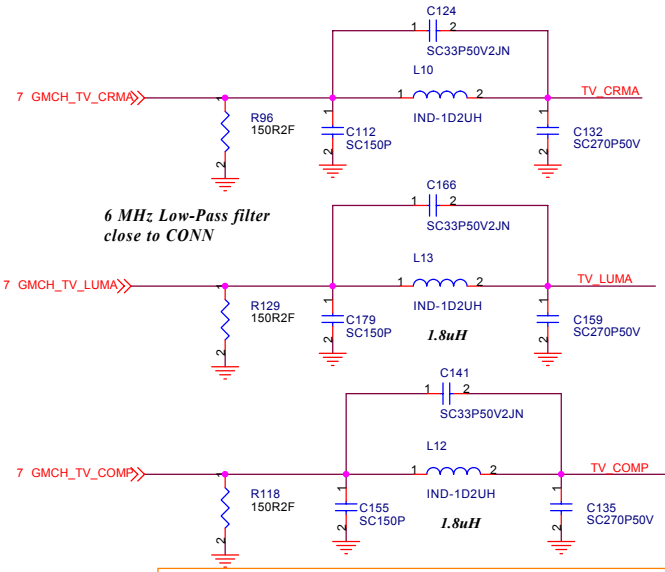


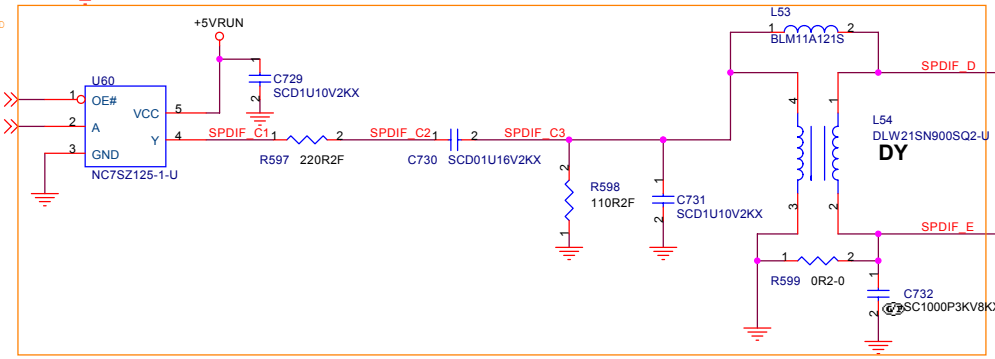
ESD Protection Diode



TVOUT CONN







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Title	*TV CONN.*	
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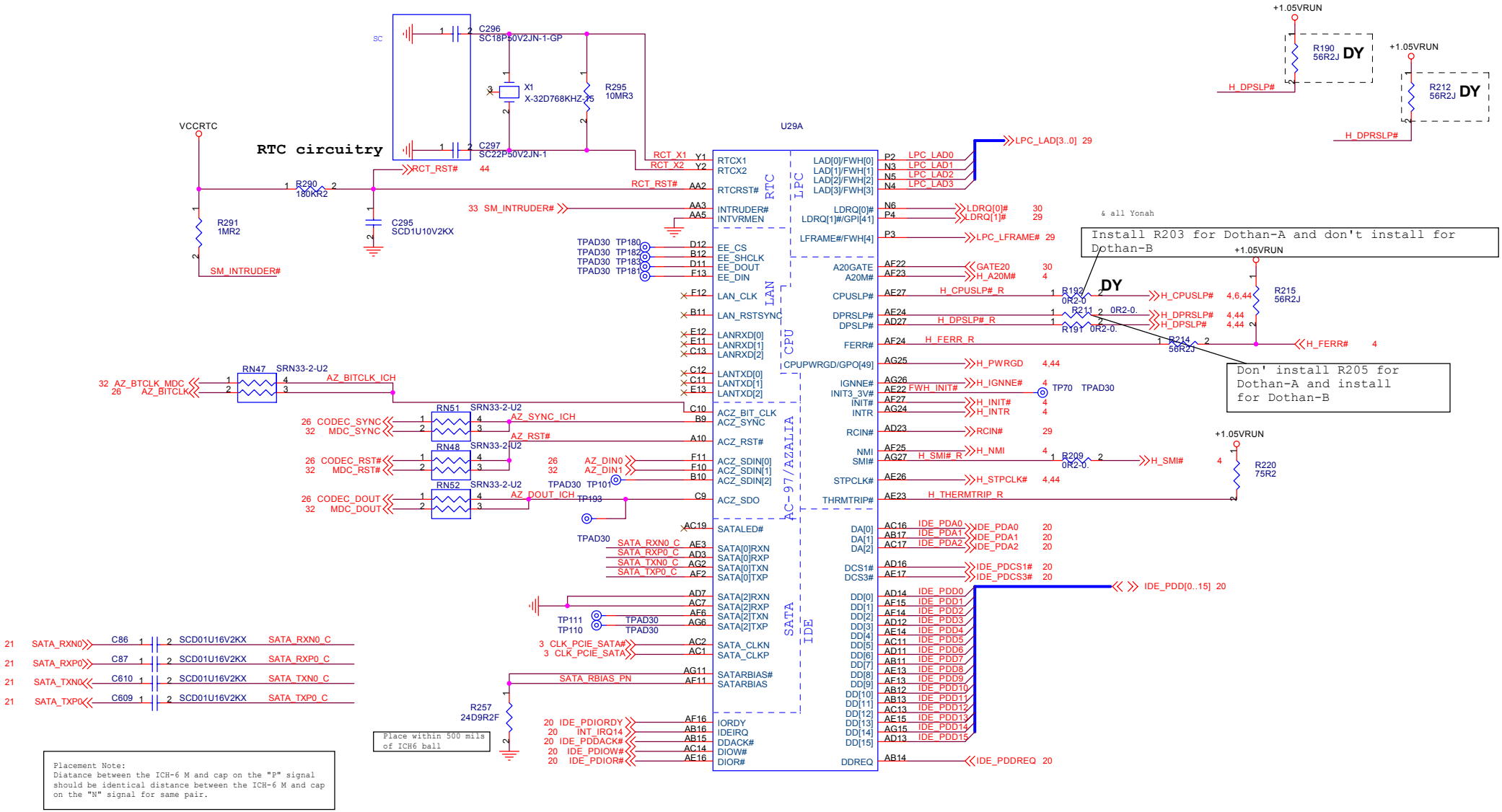

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Title: ICH6-M (1 of 4)

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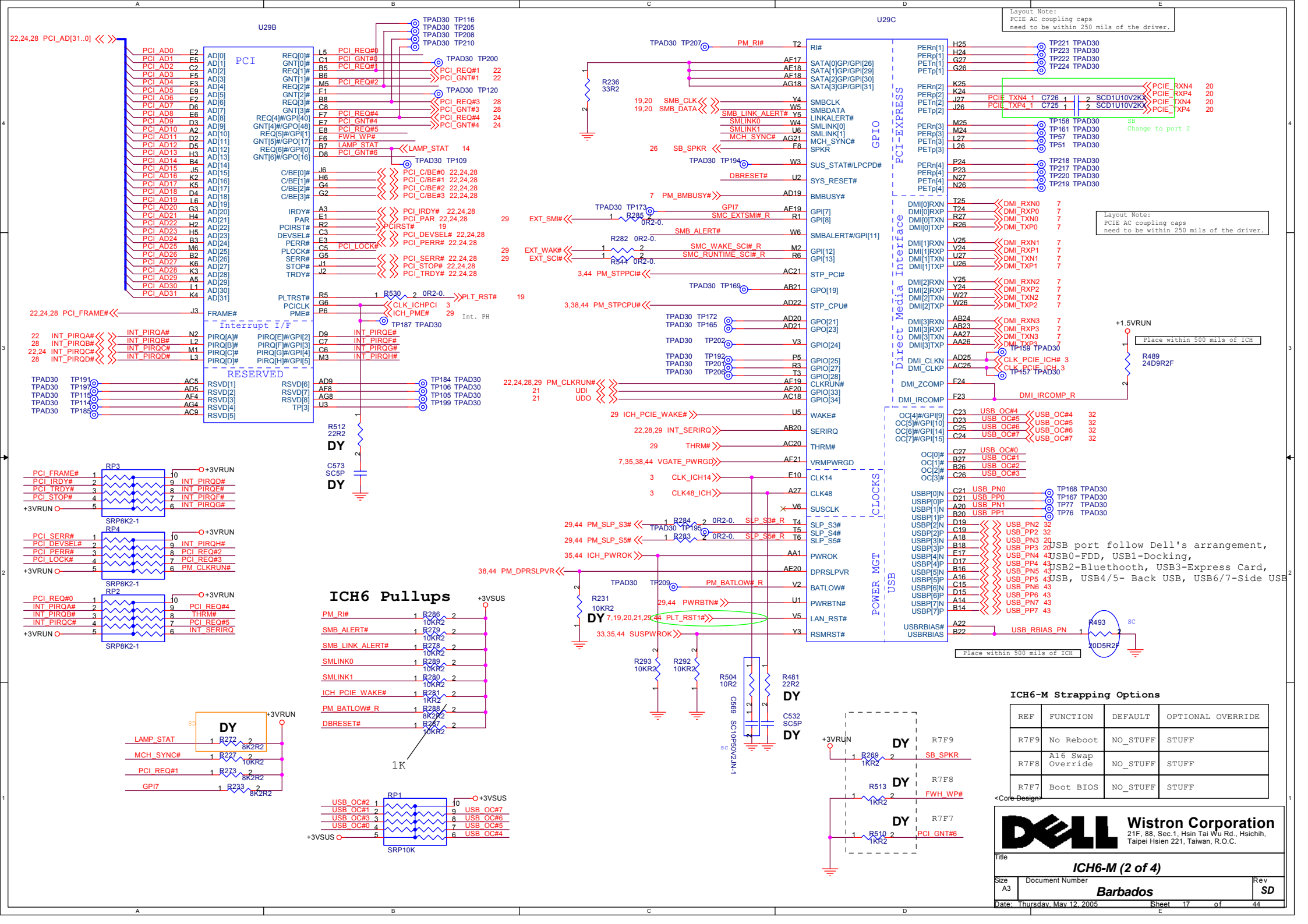
U29B
PCI
Interrupt I/F
RESERVED
U29C
GPIO
PCI-EXPRESS
Direct Media Interface
CLOCKS
USB
POWER MGT
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
Place within 500 mils of ICH
SB
Change to port 2
USB port follow Dell's arrangement,
USB0-FDD, USB1-Docking,
USB2-Bluethooth, USB3-Express Card,
USB, USB4/5- Back USB, USB6/7-Side USB
ICH6 Pullups
1K
DY
SRP8K2-1
SRP10K
SRP8K2-1
SRP8K2-1
SRP8K2-1
ICH6-M Strapping Options
REF
FUNCTION
DEFAULT
OPTIONAL OVERRIDE
R7F9
No Reboot
NO_STUFF
STUFF
R7F8
A16 Swap Override
NO_STUFF
STUFF
R7F7
Boot BIOS
NO_STUFF
STUFF
<Core Design>
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Title
ICH6-M (2 of 4)
Size
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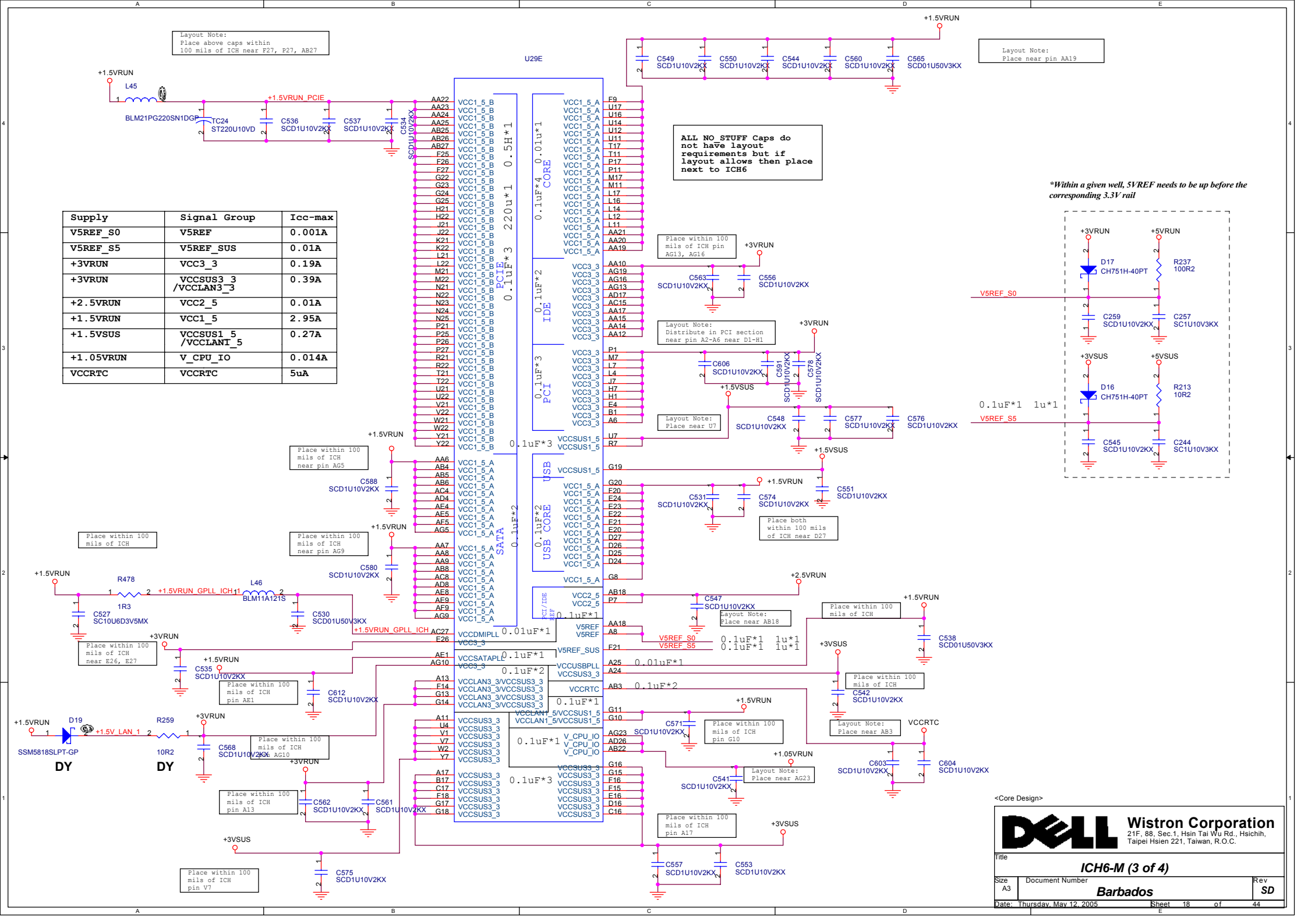
U29E
Layout Note:
Place above caps within
100 mils of ICH near F27, P27, AB27
Layout Note:
Place near pin AA19
ALL NO_STUFF Caps do not have layout requirements but if layout allows then place next to ICH6
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Supply | Signal Group | Icc-max
V5REF_S0 | V5REF | 0.001A
V5REF_S5 | V5REF_SUS | 0.01A
+3VRUN | VCC3_3 | 0.19A
+3VRUN | VCCSUS3_3 /VCCLAN3_3 | 0.39A
+2.5VRUN | VCC2_5 | 0.01A
+1.5VRUN | VCC1_5 | 2.95A
+1.5VSUS | VCCSUS1_5 /VCCLANI_5 | 0.27A
+1.05VRUN | V_CPU_IO | 0.014A
VCCRTC | VCCRTC | 5uA
Layout Note:
Distribute in PCI section
near pin A2-A6 near D1-H1
Layout Note:
Place near U7
Layout Note:
Place near AA18
Layout Note:
Place near AB3
Layout Note:
Place near AG23
Place within 100 mils of ICH near pin AG5
Place within 100 mils of ICH near pin AG9
Place within 100 mils of ICH near E26, E27
Place within 100 mils of ICH pin AE1
Place within 100 mils of ICH pin AG10
Place within 100 mils of ICH pin A13
Place within 100 mils of ICH pin V7
Place within 100 mils of ICH pin A17
Place within 100 mils of ICH pin G10
Place within 100 mils of ICH pin AG13, AG16
Place both within 100 mils of ICH near D27
<Core Design>
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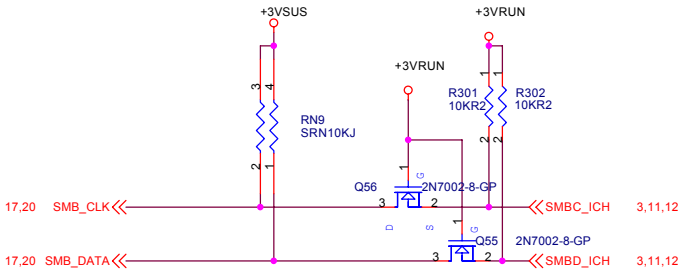
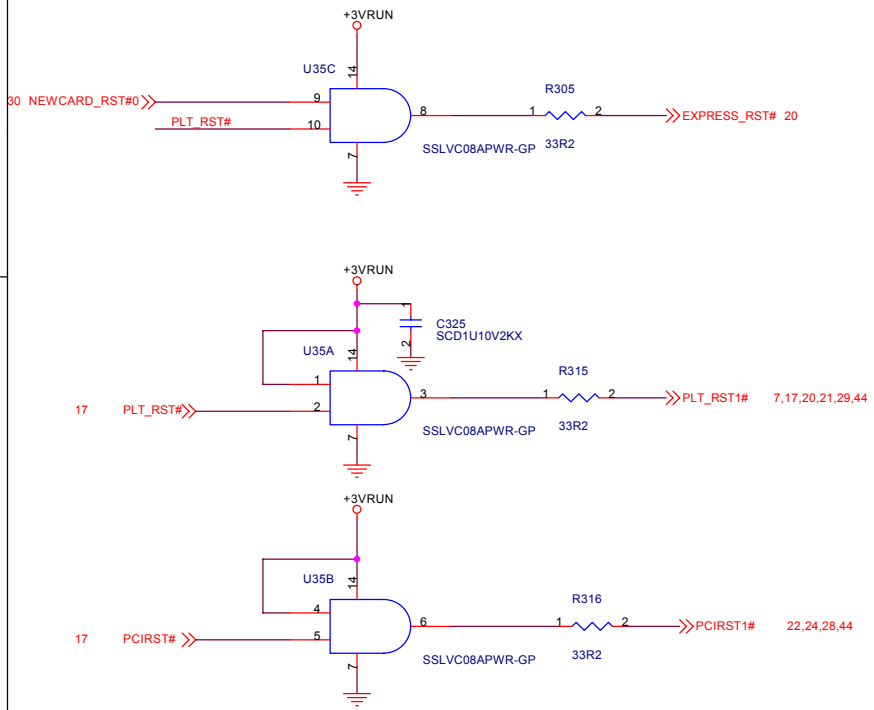
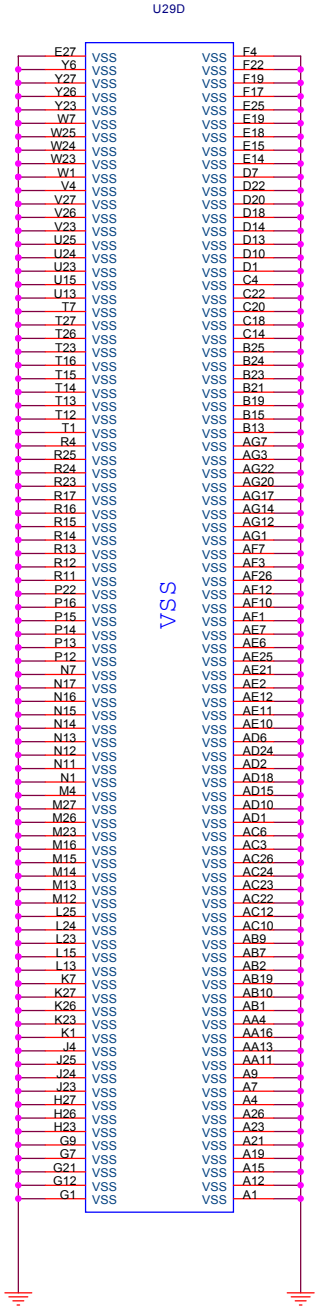
SMBUS



Q94 & Q95 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance





<Core Design>

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Title: *ICH6-M (4 of 4)*

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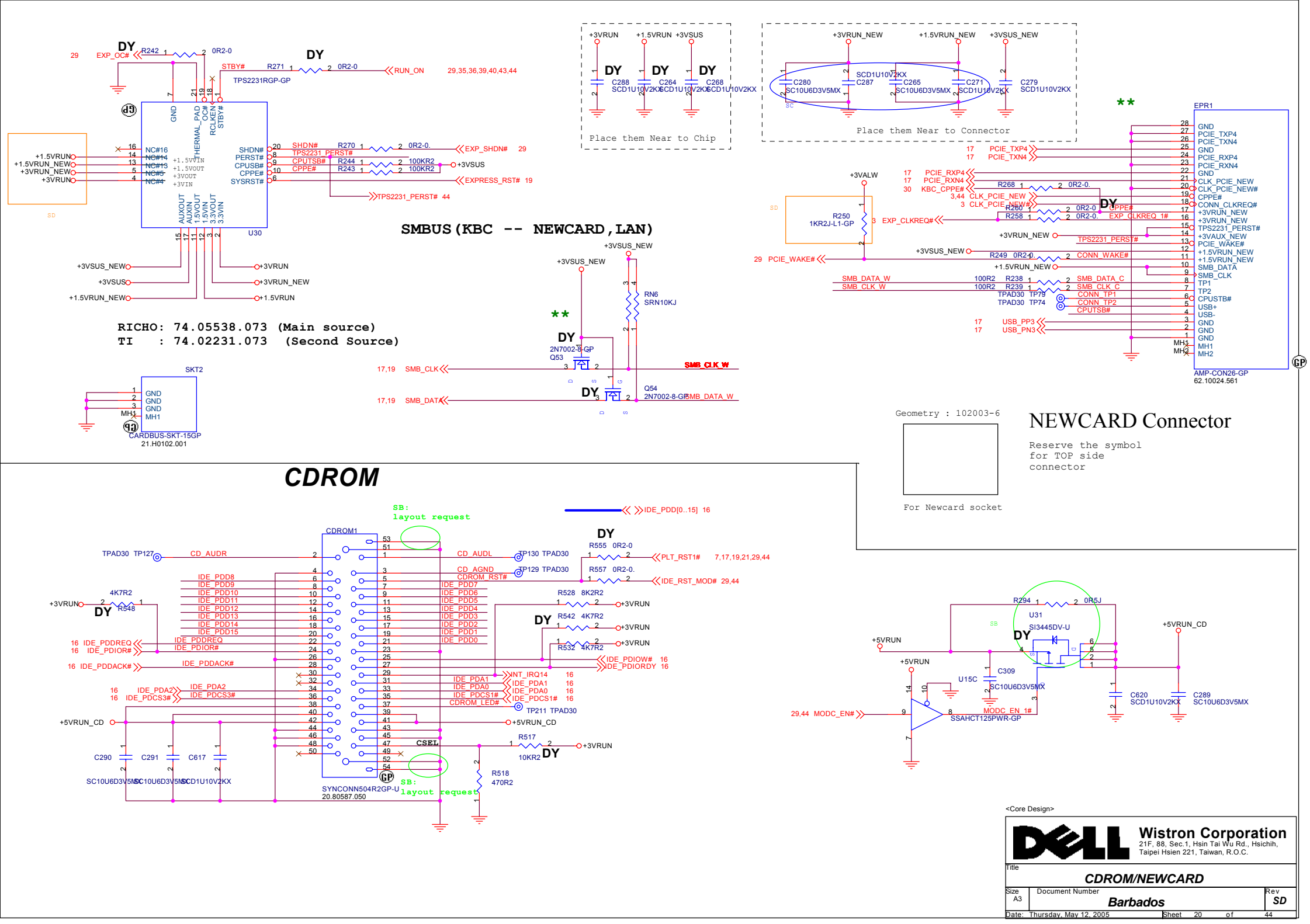
DY
29 EXP_OC# R242 1 2 0R2-0
STBY# R271 1 2 0R2-0 RUN_ON 29,35,36,39,40,43,44
TPS2231RGP-GP
GND THERMAL_PAD OC# RCLKEN STBY#
+1.5VRUN
+1.5VRUN_NEW
+3VRUN_NEW
+3VRUN
NC#16 NC#14 NC#13 NC#5 NC#4
+1.5VIN +1.5VOUT +3VOUT +3VIN
SHDN# PERST# CPUSB# CPPE# SYSRST#
SHDN# R270 1 2 0R2-0. EXP_SHDN# 29
TPS2231_PERST# CPUSB# R244 1 2 100KR2 +3VSUS
CPPE# R243 1 2 100KR2
EXPRESS_RST# 19
TPS2231_PERST# 44
AUXOUT AUXIN 1.5VOUT 1.5VIN 3.3VOUT 3.3VIN
U30
+3VSUS_NEW
+3VSUS
+1.5VRUN_NEW
+3VRUN
+3VRUN_NEW
+1.5VRUN
SD
+3VRUN +1.5VRUN +3VSUS
DY
C288 SCD1U10V2KX
C264 SCD1U10V2KX
C268 SCD1U10V2KX
Place them Near to Chip
+3VRUN_NEW +1.5VRUN_NEW +3VSUS_NEW
C280 SC10U6D3V5MX
C287 SCD1U10V2KX
C265 SC10U6D3V5MX
C271 SCD1U10V2KX
C279 SCD1U10V2KX
SC
Place them Near to Connector
SMBUS (KBC -- NEWCARD,LAN)
+3VSUS_NEW
RN6 SRN10KJ
**
DY
2N7002-8-GP Q53
17,19 SMB_CLK
SMB_CLK_W
Q54 2N7002-8-GP
17,19 SMB_DATA
SMB_DATA_W
RICHO: 74.05538.073 (Main source)
TI : 74.02231.073 (Second Source)
SKT2
GND GND GND MH1
CARDBUS-SKT-15GP
21.H0102.001
+3VALW
R250 1KR2J-L1-GP
EXP_CLKREQ#
29 PCIE_WAKE#
17 PCIE_TXP4
17 PCIE_TXN4
17 PCIE_RXP4
17 PCIE_RXN4
30 KBC_CPPE#
3,44 CLK_PCIE_NEW
3 CLK_PCIE_NEW#
R268 1 2 0R2-0.
R260 1 2 0R2-0 CPPE#
R258 1 2 0R2-0. EXP_CLKREQ_1#
TPS2231_PERST#
R249 0R2-0. CONN_WAKE#
SMB_DATA_W
SMB_CLK_W
100R2 R238 SMB_DATA_C
100R2 R239 SMB_CLK_C
TPAD30 TP79 CONN_TP1
TPAD30 TP74 CONN_TP2
CPUSTB#
17 USB_PP3
17 USB_PN3
EPR1
GND PCIE_TXP4 PCIE_TXN4 GND PCIE_RXP4 PCIE_RXN4 GND CLK_PCIE_NEW CLK_PCIE_NEW# CPPE# CONN_CLKREQ# +3VRUN_NEW +3VRUN_NEW TPS2231_PERST# +3VAUX_NEW PCIE_WAKE# +1.5VRUN_NEW +1.5VRUN_NEW SMB_DATA SMB_CLK TP1 TP2 CPUSTB# USB+ USB- GND GND GND MH1 MH2
AMP-CON26-GP
62.10024.561
Geometry : 102003-6
For Newcard socket
NEWCARD Connector
Reserve the symbol
for TOP side
connector
CDROM
SB: layout request
IDE_PDD[0..15] 16
CDROM1
TPAD30 TP127 CD_AUDR
CD_AUDL TP130 TPAD30
CD_AGND TP129 TPAD30
CDROM_RST#
IDE_PDD8 IDE_PDD9 IDE_PDD10 IDE_PDD11 IDE_PDD12 IDE_PDD13 IDE_PDD14 IDE_PDD15
IDE_PDD7 IDE_PDD6 IDE_PDD5 IDE_PDD4 IDE_PDD3 IDE_PDD2 IDE_PDD1 IDE_PDD0
16 IDE_PDDREQ IDE_PDDREQ
16 IDE_PDIOR# IDE_PDIOR#
16 IDE_PDDACK# IDE_PDDACK#
16 IDE_PDA2 IDE_PDA2
16 IDE_PDCS3# IDE_PDCS3#
IDE_PDA1 IDE_PDA0 IDE_PDCS1# CDROM_LED#
INT_IRQ14 16
IDE_PDA1 16
IDE_PDA0 16
IDE_PDCS1# 16
TP211 TPAD30
+5VRUN_CD
CSEL
R517 10KR2 +3VRUN
R518 470R2
SYNCONN504R2GP-U
20.80587.050
SB: layout request
R555 0R2-0 PLT_RST1# 7,17,19,21,29,44
R557 0R2-0. IDE_RST_MOD# 29,44
R528 8K2R2 +3VRUN
R542 4K7R2 +3VRUN
R532 4K7R2 +3VRUN
IDE_PDIOW# 16
IDE_PDIORDY 16
+3VRUN 4K7R2 R548
C290 SC10U6D3V5MX
C291 SC10U6D3V5MX
C617 SCD1U10V2KX
R294 1 2 0R5J
U31
SI3445DV-U
+5VRUN
+5VRUN_CD
U15C
C309 SC10U6D3V5MX
29,44 MODC_EN#
MODC_EN_1#
SSAHCT125PWR-GP
C620 SCD1U10V2KX
C289 SC10U6D3V5MX
<Core Design>
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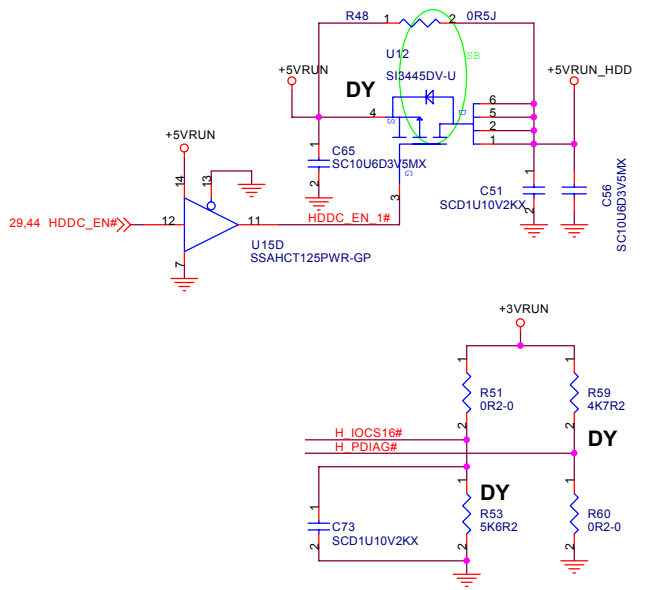
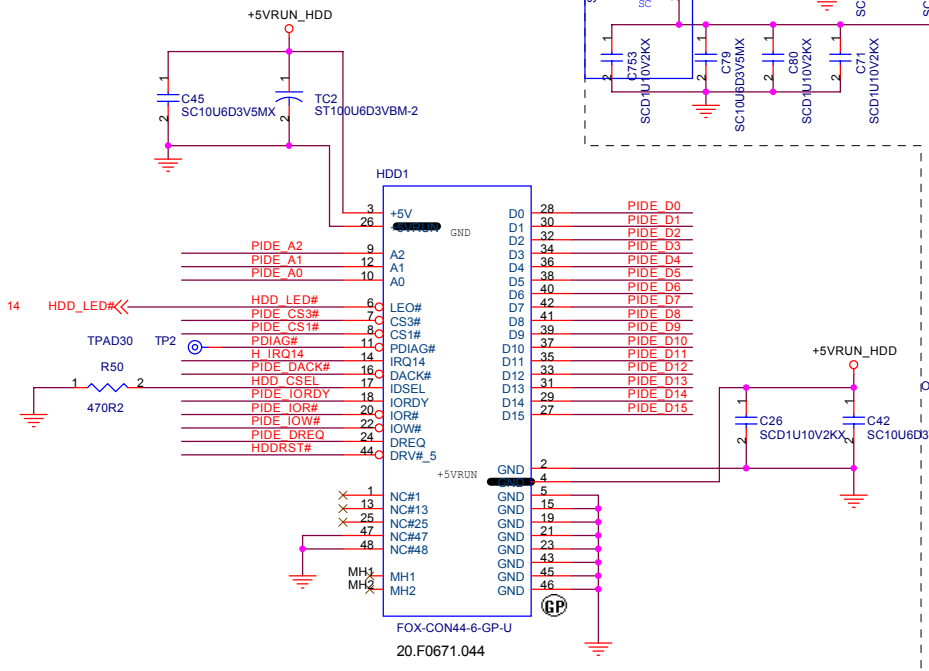
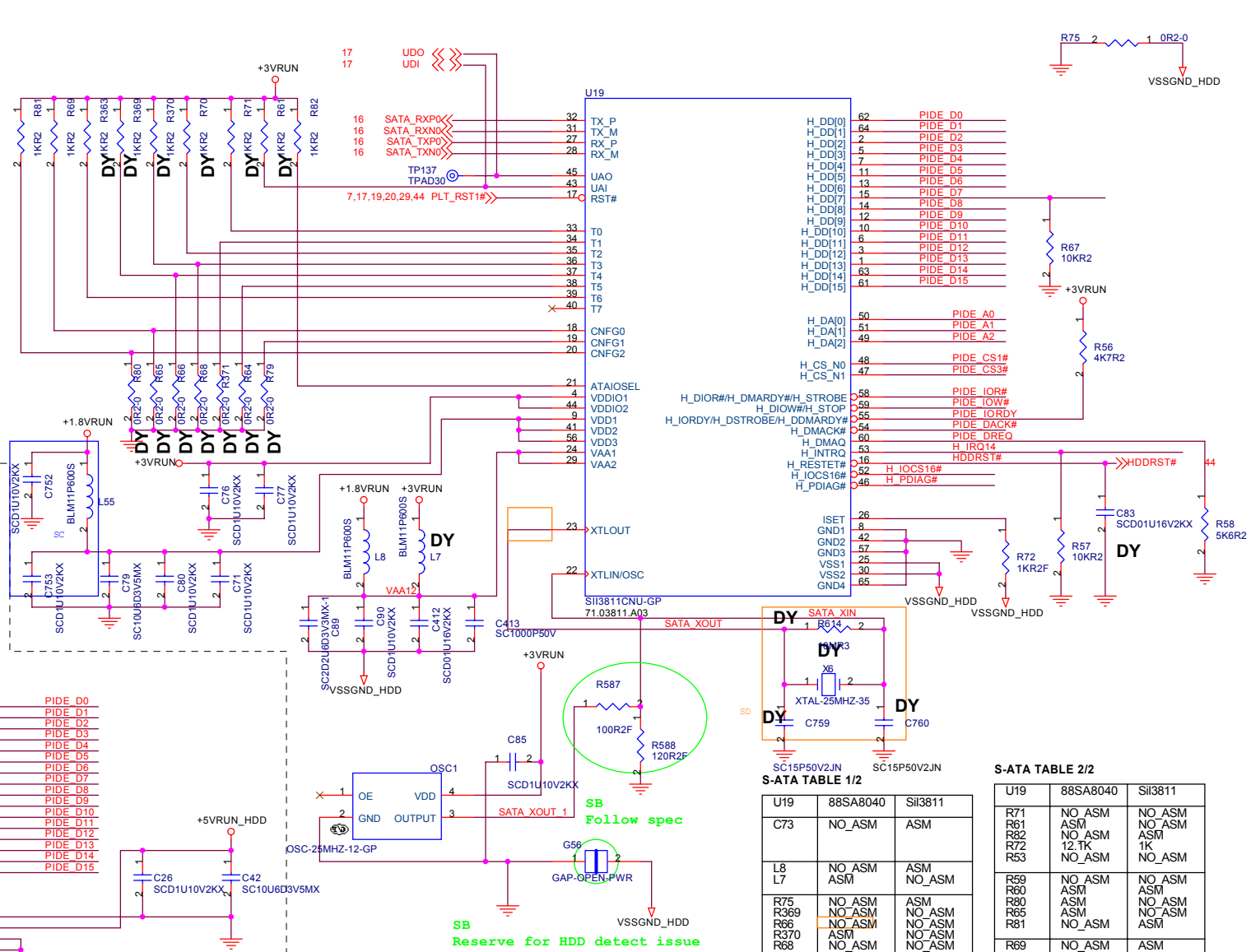
HDD power



HDD CONN





S-ATA TABLE 1/2

U19	88SA8040	Sil3811
C73	NO_ASM	ASM
L8 L7	NO_ASM ASM	ASM NO_ASM
R75 R369 R66 R370 R68	NO_ASM NO_ASM NO_ASM ASM NO_ASM	ASM NO_ASM NO_ASM NO_ASM NO_ASM
R363	NO_ASM	NO_ASM
R371 R70 R64	NO_ASM NO_ASM ASM	NO_ASM NO_ASM NO_ASM

S-ATA TABLE 2/2

U19	88SA8040	Sil3811
R71 R61 R82 R72 R53	NO_ASM ASM NO_ASM 12.1K NO_ASM	NO_ASM NO_ASM ASM 1K NO_ASM
R59 R60 R80 R65 R81	NO_ASM ASM ASM ASM NO_ASM	NO_ASM ASM NO_ASM NO_ASM ASM
R69 R79 R51	NO_ASM ASM NO_ASM	ASM NO_ASM ASM
R587 R588	0 ohm NO_ASM	100 ohm 120 ohm

<Core Design>

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Title: **SATA HDD/CD ROM**

Size: A3 | Document Number: **Barbados** | Rev: **SD**

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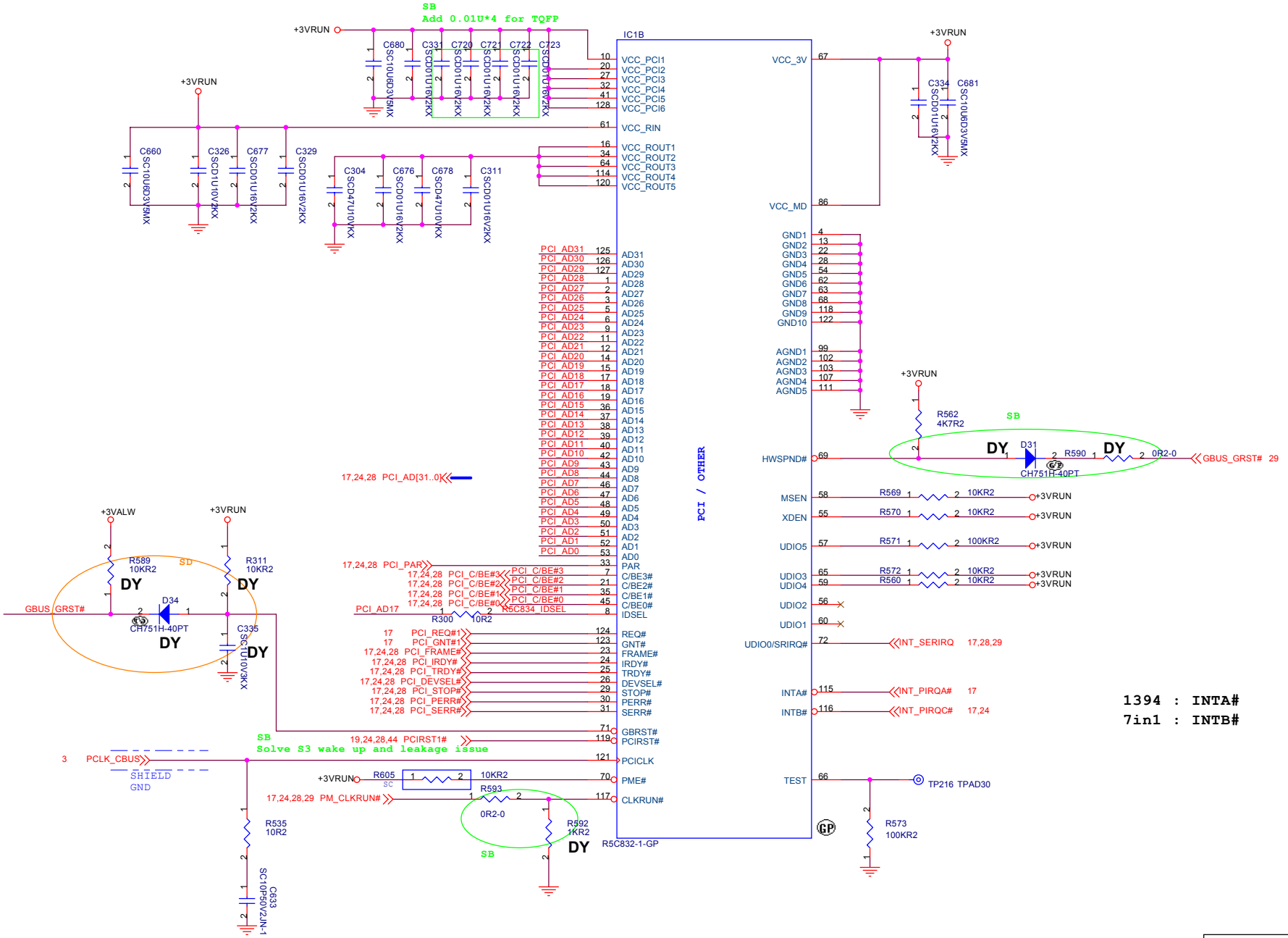
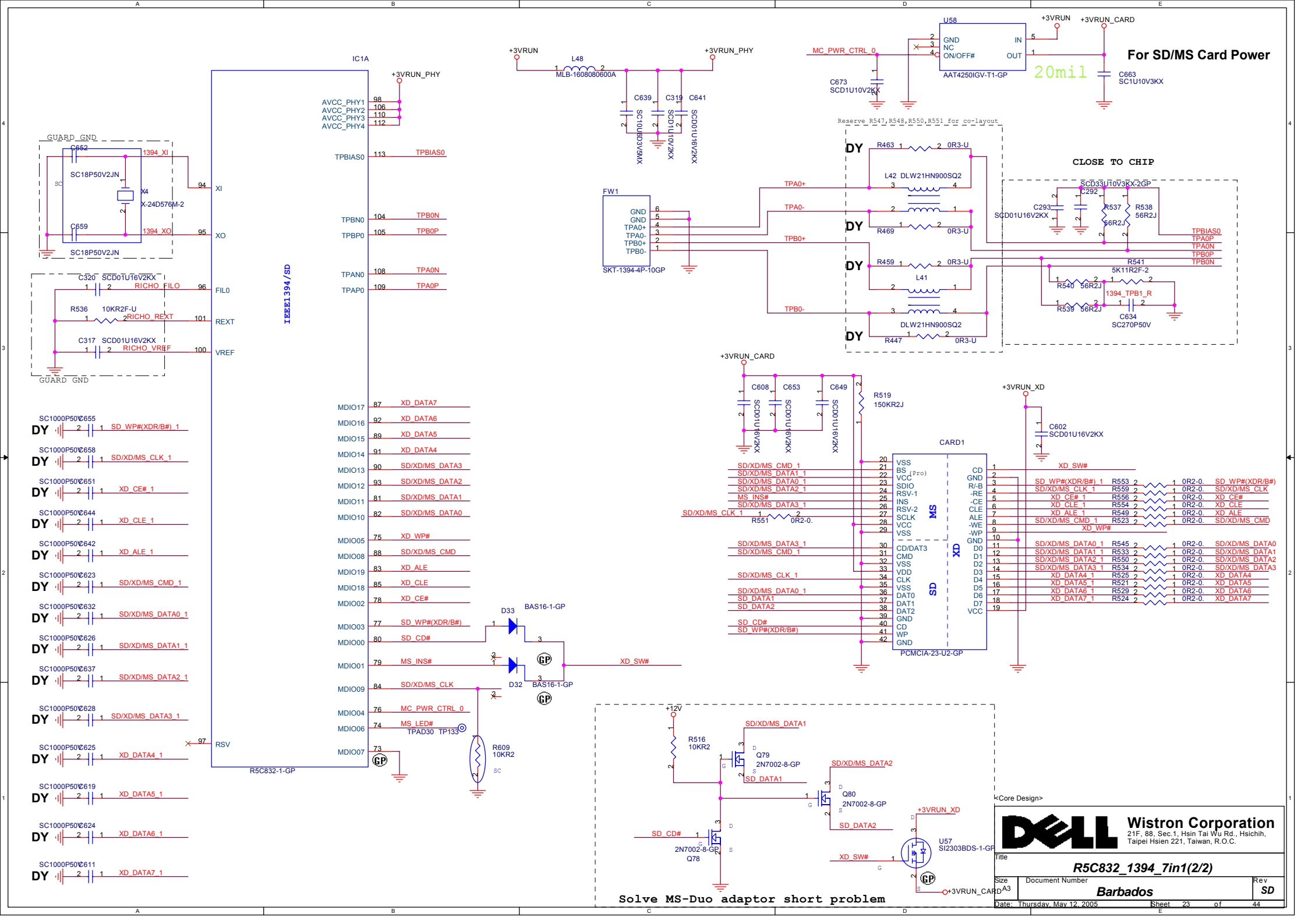
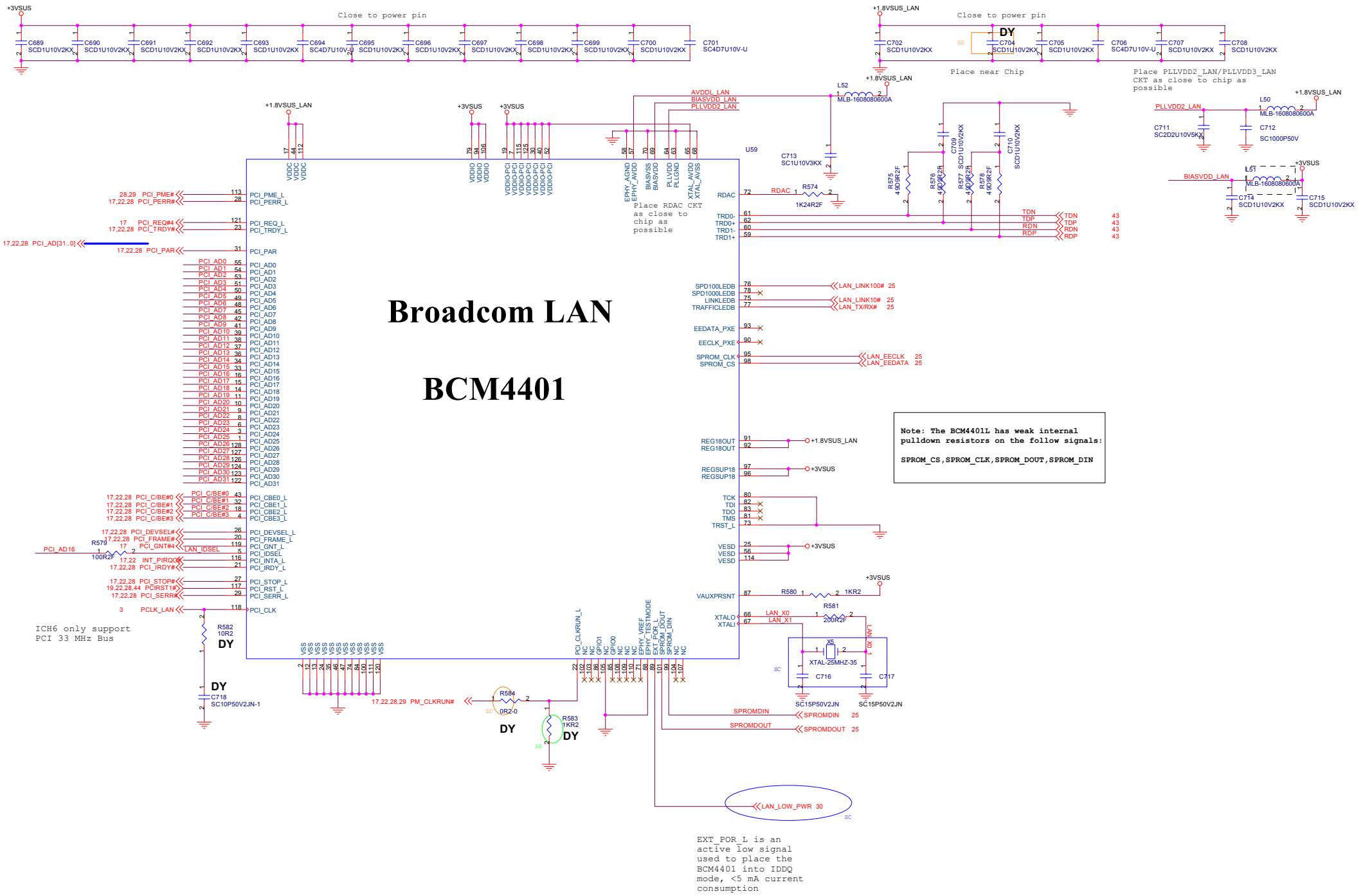


Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	R5C832_PCI(1/2)
Size: A3	Document Number: Barbados
Rev: SD	
Date: Thursday, May 12, 2005	Sheet 22 of 44


IC1A
IEEE1394/SD
R5C832-1-GP
GUARD_GND
SC18P50V2JN
X-24D576M-2
1394_XI
1394_XO
RICHO_FILO
RICHO_REXT
RICHO_VREF
10KR2F-U
SCD01U16V2KX
+3VRUN_PHY
AVCC_PHY1
AVCC_PHY2
AVCC_PHY3
AVCC_PHY4
TPBIAS0
TPB0N
TPB0P
TPA0N
TPA0P
XI
XO
FIL0
REXT
VREF
RSV
MDIO17
MDIO16
MDIO15
MDIO14
MDIO13
MDIO12
MDIO11
MDIO10
MDIO05
MDIO08
MDIO19
MDIO18
MDIO02
MDIO03
MDIO00
MDIO01
MDIO09
MDIO04
MDIO06
MDIO07
XD_DATA7
XD_DATA6
XD_DATA5
XD_DATA4
SD/XD/MS_DATA3
SD/XD/MS_DATA2
SD/XD/MS_DATA1
SD/XD/MS_DATA0
XD_WP#
SD/XD/MS_CMD
XD_ALE
XD_CLE
XD_CE#
SD_WP#(XDR/B#)
SD_CD#
MS_INS#
SD/XD/MS_CLK
MC_PWR_CTRL_0
MS_LED#
TPAD30 TP133
SD_WP#(XDR/B#)_1
SD/XD/MS_CLK_1
XD_CE#_1
XD_CLE_1
XD_ALE_1
SD/XD/MS_CMD_1
SD/XD/MS_DATA0_1
SD/XD/MS_DATA1_1
SD/XD/MS_DATA2_1
SD/XD/MS_DATA3_1
XD_DATA4_1
XD_DATA5_1
XD_DATA6_1
XD_DATA7_1
DY
+3VRUN
L48
MLB-1608080600A
+3VRUN_PHY
C639
C319
C641
SC10U6D3V5MX
SCD01U10V2KX
SCD01U16V2KX
FW1
SKT-1394-4P-10GP
TPA0+
TPA0-
TPB0+
TPB0-
Reserve R547,R548,R550,R551 for co-layout
R463
R469
R459
R447
0R3-U
L42 DLW21HN900SQ2
L41
DLW21HN900SQ2
CLOSE TO CHIP
SCD33U10V3KX-2GP
C292
C293
SCD01U16V2KX
R537
R538
56R2J
R540
R539
R541
5K11R2F-2
1394_TPB1_R
C634
SC270P50V
U58
GND
NC
ON/OFF#
IN
OUT
AAT4250IGV-T1-GP
MC_PWR_CTRL_0
C673
SCD1U10V2KX
+3VRUN
+3VRUN_CARD
20mil
C663
SC1U10V3KX
For SD/MS Card Power
+3VRUN_CARD
C608
C653
C649
R519
150KR2J
CARD1
PCMCIA-23-U2-GP
MS
SD
XD
VSS
BS
VCC
SDIO
RSV-1
INS
RSV-2
SCLK
CD/DAT3
CMD
CLK
DAT0
DAT1
DAT2
WP
CD
R/-B
-RE
-CE
CLE
ALE
-WE
-WP
D0
D1
D2
D3
D4
D5
D6
D7
+3VRUN_XD
C602
SCD01U16V2KX
XD_SW#
R553
R559
R556
R554
R549
R523
R545
R533
R550
R534
R525
R521
R529
R524
0R2-0.
D33
D32
BAS16-1-GP
R609
10KR2
+12V
R516
10KR2
Q79
Q80
Q78
2N7002-8-GP
SD/XD/MS_DATA1
SD/XD/MS_DATA2
SD_DATA1
SD_DATA2
SD_CD#
XD_SW#
U57
SI2303BDS-1-GP
+3VRUN_CARD
Solve MS-Duo adaptor short problem
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
R5C832_1394_7in1(2/2)
Size
A3
Document Number
Barbados
Rev
SD
Date: Thursday, May 12, 2005
Sheet 23 of 44



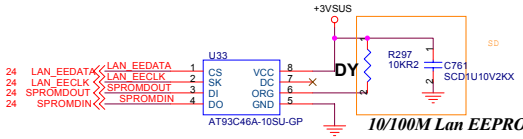
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BCM4401 10/100 LAN

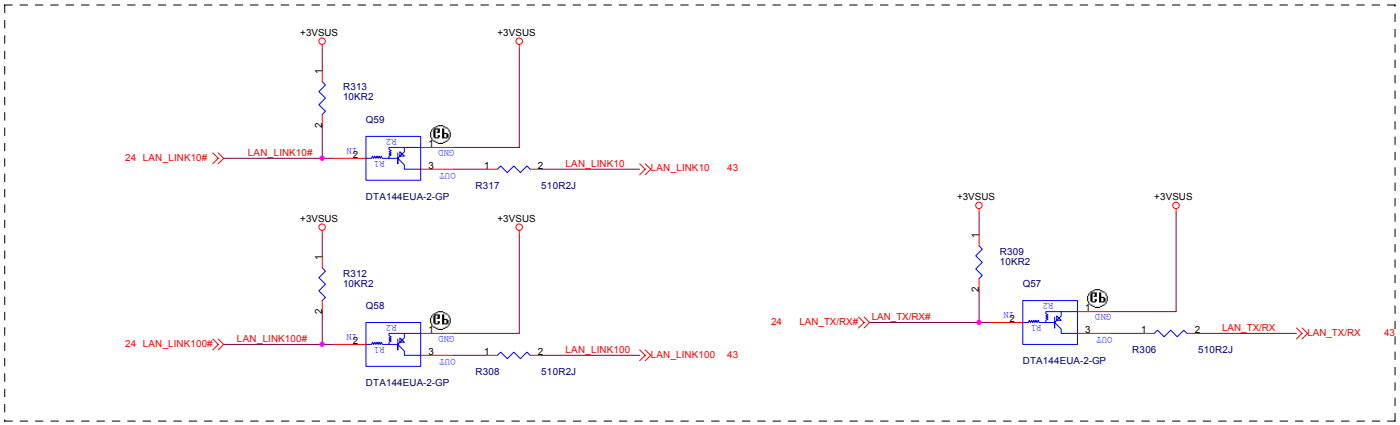
Size: Custom | Document Number: Barbados | Rev: SD

Date: Thursday, May 12, 2005 | Sheet 24 of 44



10/100M Lan EEPROM

Atmal: AT93C46-10SI "72.93C46.K01" (Main source)
ST : M93C46-W "72.93C46.E01" (2nd source)



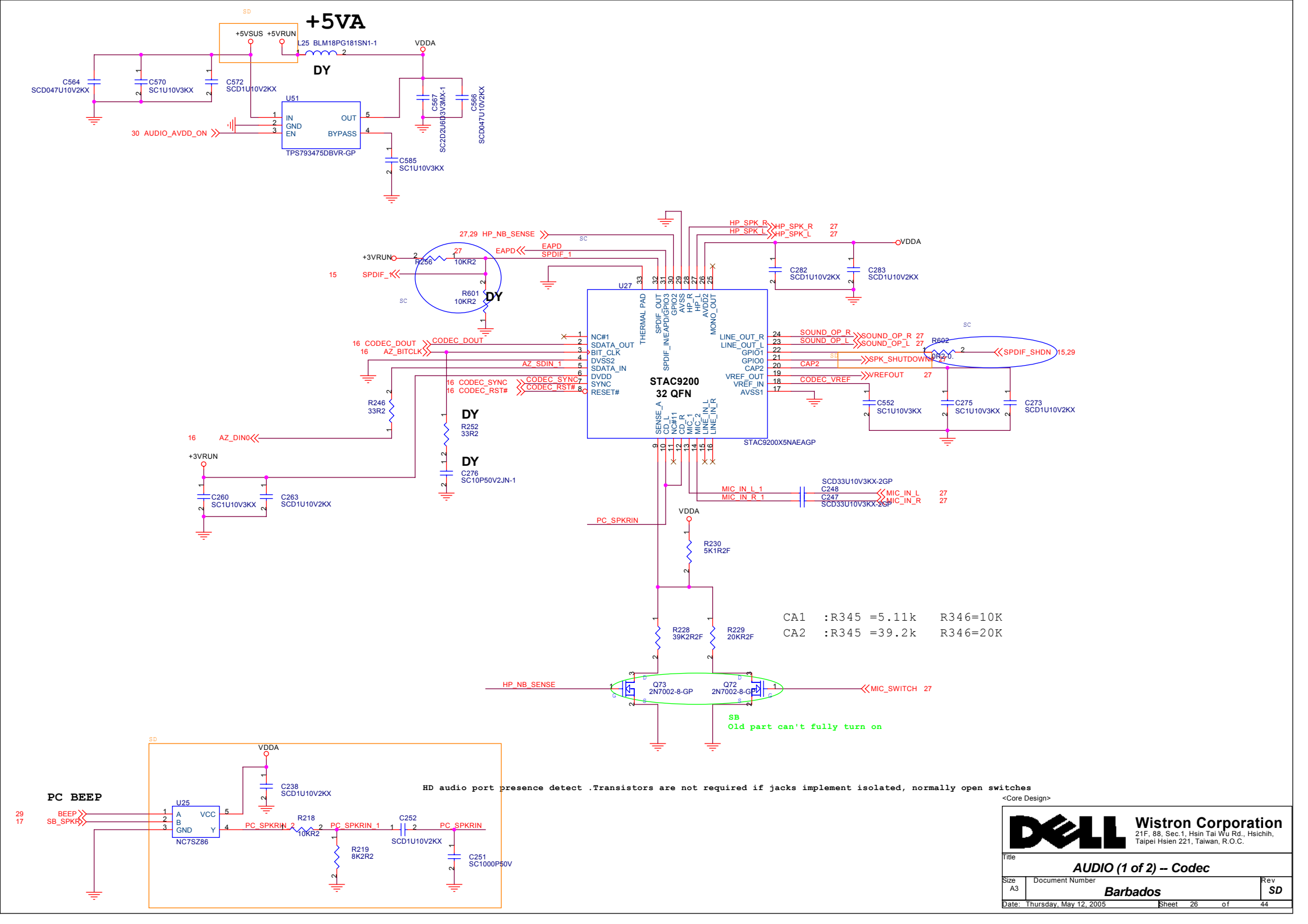
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN Transformer***

Size	Document Number	Rev
Custom	***Barbados***	***SD***

Date: Thursday, May 12, 2005 Sheet 25 of 44


+5VA
+5VSUS +5VRUN
L25 BLM18PG181SN1-1
VDDA
DY
C564 SCD047U10V2KX
C570 SC1U10V3KX
C572 SCD1U10V2KX
U51
IN
GND
EN
OUT
BYPASS
TPS793475DBVR-GP
30 AUDIO_AVDD_ON
C567 SC2D2U6V3MX-1
C566 SCD047U10V2KX
C585 SC1U10V3KX
27,29 HP_NB_SENSE
EAPD
SPDIF_1
+3VRUN
R256 10KR2
R601 10KR2
DY
HP_SPK_R
HP_SPK_L
C282 SCD1U10V2KX
C283 SCD1U10V2KX
U27
THERMAL PAD
SPDIF_OUT
SPDIF_IN/EAPD/GPIO3
GPIO2
AVSS
HP_R
HP_L
AVDD2
MONO_OUT
NC#1
SDATA_OUT
BIT_CLK
DVSS2
SDATA_IN
DVDD
SYNC
RESET#
STAC9200
32 QFN
STAC9200X5NAEAGP
LINE_OUT_R
LINE_OUT_L
GPIO1
GPIO0
CAP2
VREF_OUT
VREF_IN
AVSS1
SENSE_A
CD_L
NC#11
CD_R
MIC_1
MIC_2
LINE_IN_L
LINE_IN_R
SOUND_OP_R
SOUND_OP_L
SPK_SHUTDOWN#
CODEC_VREF
VREFOUT
R602 0R2.0
SPDIF_SHDN
C552 SC1U10V3KX
C275 SC1U10V3KX
C273 SCD1U10V2KX
16 CODEC_DOUT
16 AZ_BITCLK
AZ_SDIN_1
16 CODEC_SYNC
16 CODEC_RST#
R246 33R2
R252 33R2
C276 SC10P50V2JN-1
16 AZ_DIN0
+3VRUN
C260 SC1U10V3KX
C263 SCD1U10V2KX
MIC_IN_L_1
MIC_IN_R_1
SCD33U10V3KX-2GP
C248
C247
MIC_IN_L
MIC_IN_R
PC_SPKRIN
R230 5K1R2F
R228 39K2R2F
R229 20KR2F
CA1 :R345 =5.11k R346=10K
CA2 :R345 =39.2k R346=20K
HP_NB_SENSE
Q73 2N7002-8-GP
Q72 2N7002-8-GP
MIC_SWITCH
SB
Old part can't fully turn on
HD audio port presence detect .Transistors are not required if jacks implement isolated, normally open switches
PC BEEP
29 BEEP
17 SB_SPKR
U25
NC7SZ86
C238 SCD1U10V2KX
R218 10KR2
R219 8K2R2
C252 SCD1U10V2KX
C251 SC1000P50V
PC_SPKRIN_1
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO (1 of 2) -- Codec
Size A3
Document Number
Barbados
Rev SD
Date: Thursday, May 12, 2005
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NOTE: Input type select, input level tracking , and MIC bias (VREFOUT) switching are handled in software, per user controls are mixer GUI

Stereo MIC

LINE OUT

GAIN0	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

<Core Design>

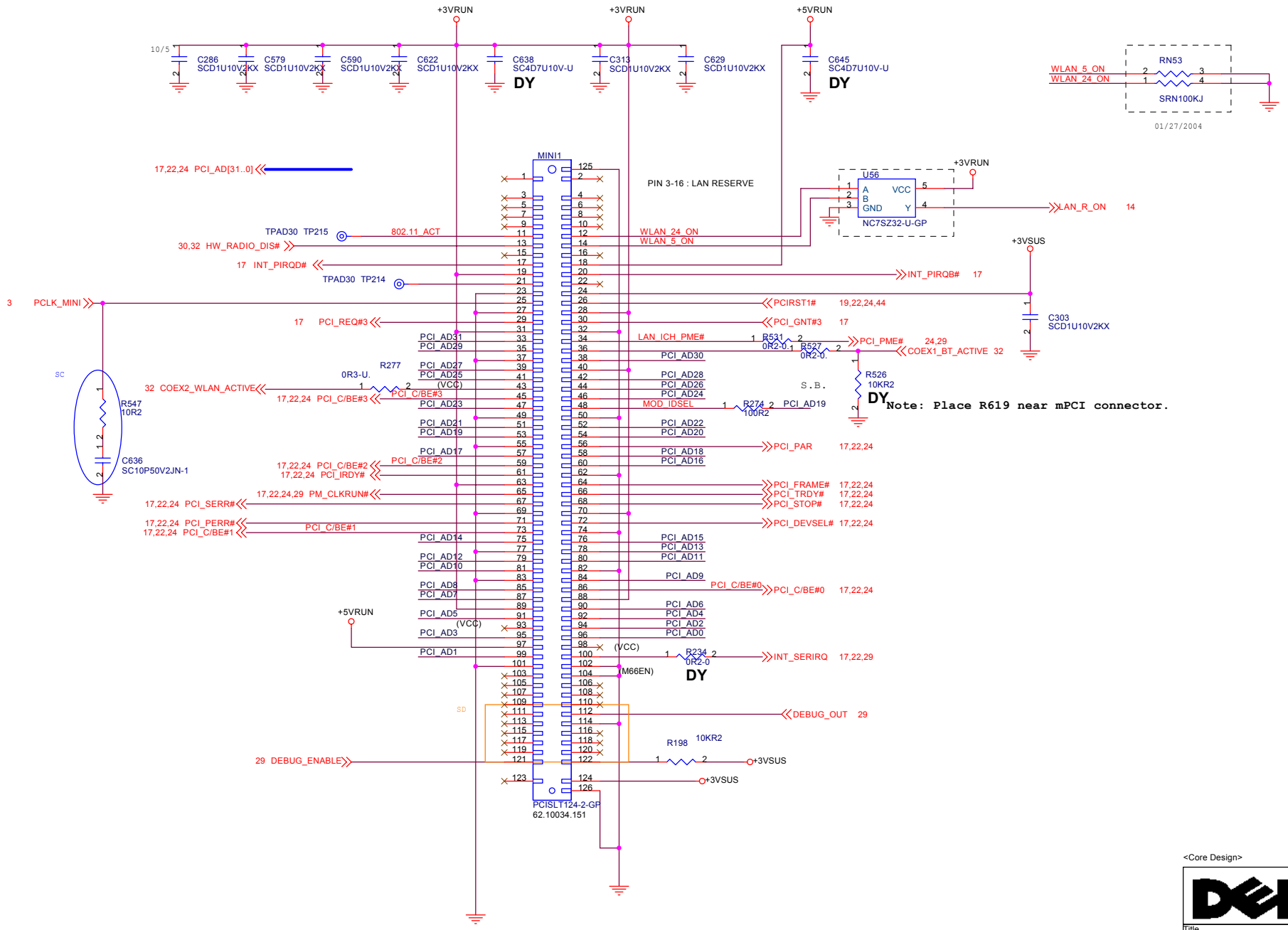
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO (2 of 2) --Phone Jack

Size: A3 | Document Number: Barbados | Rev: SD

Date: Thursday, May 12, 2005 | Sheet 27 of 44

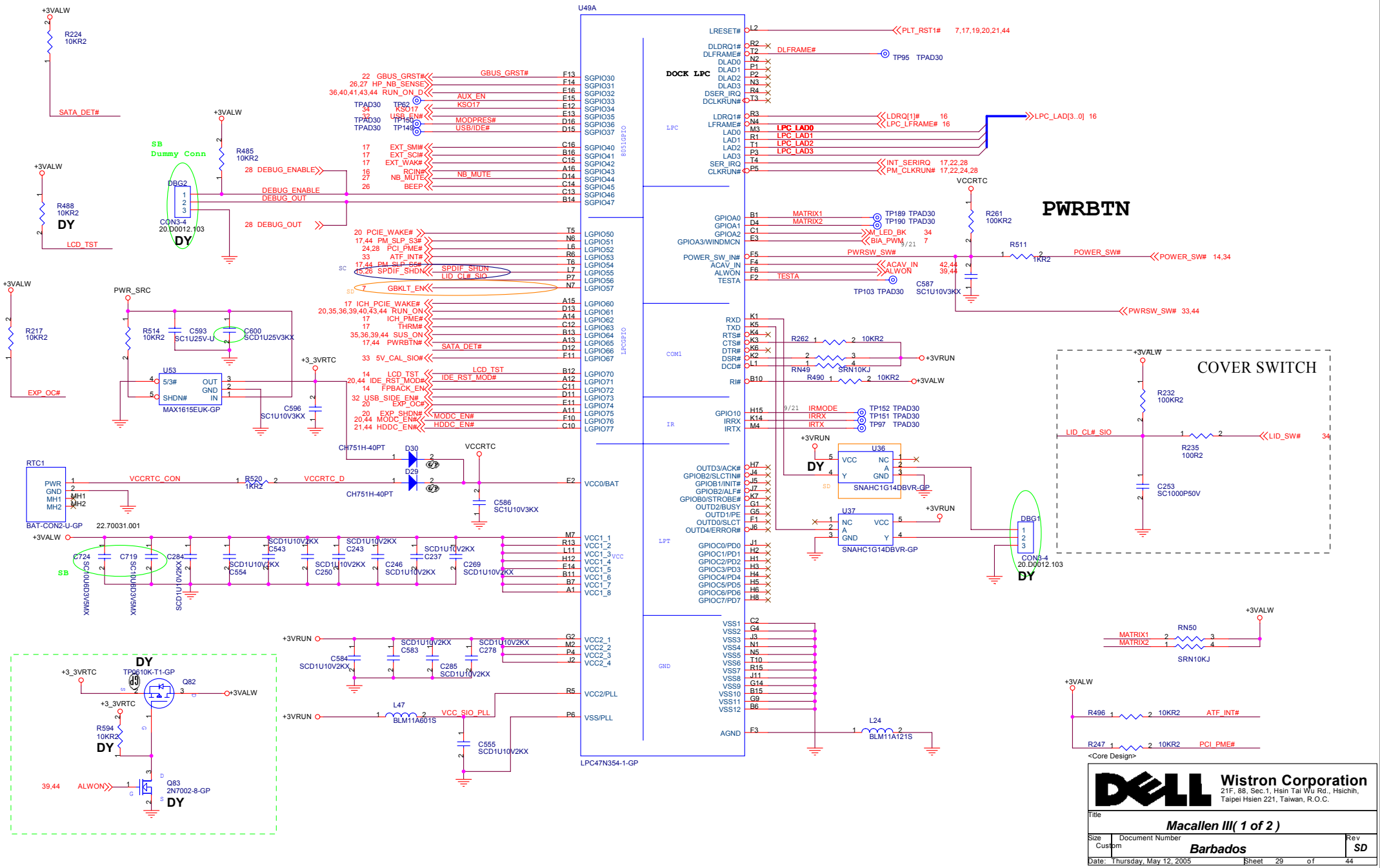
MINI PCI

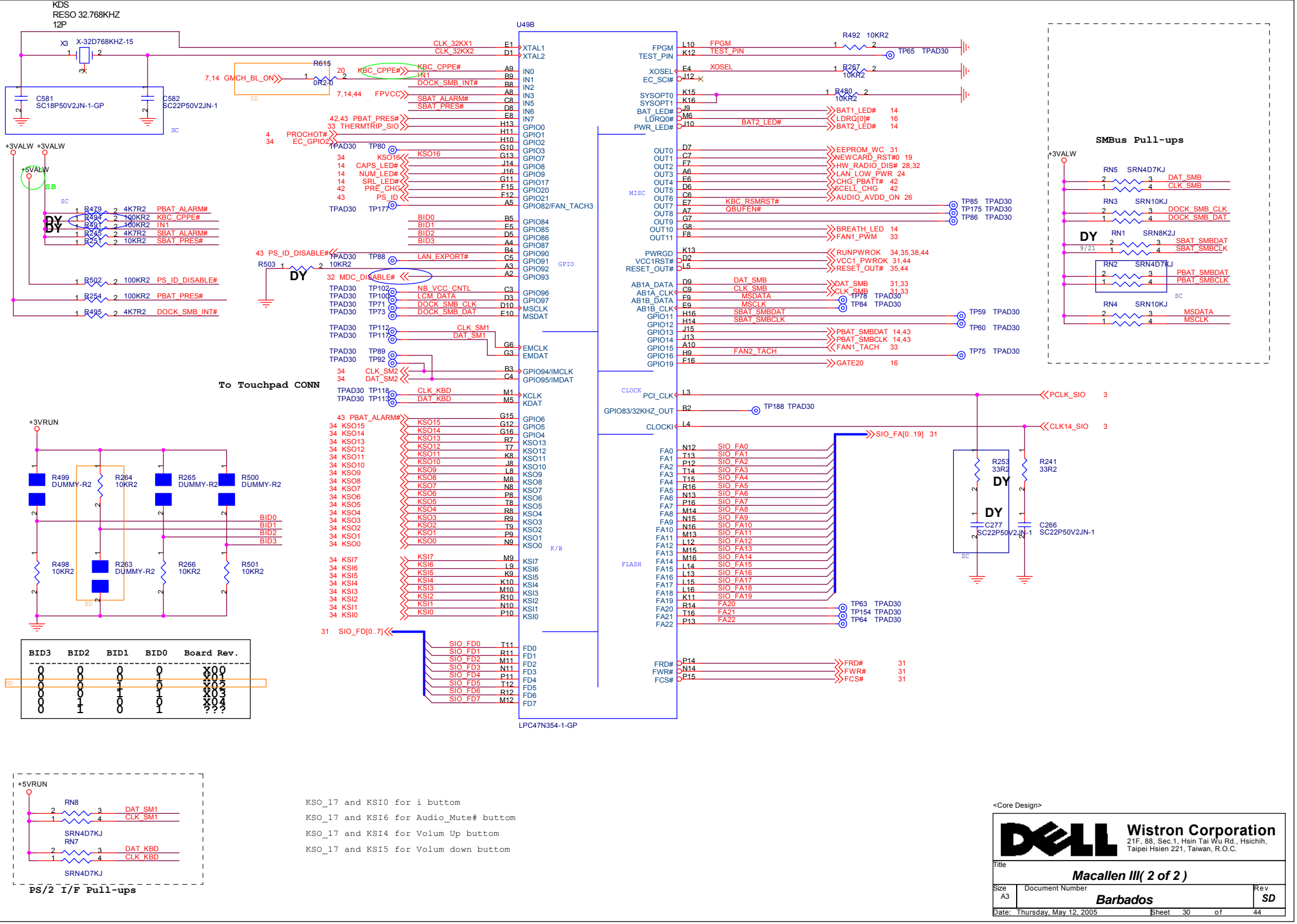


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***MINI-PCI***	
Size A3	Document Number ***Barbados***	Rev ***SD***
Date: Thursday, May 12, 2005	Sheet 28 of 44	


U49A
DOCK LPC
LPC47N354-1-GP
PWRBTN
COVER SWITCH
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Macallen III(1 of 2)
Size
Custom
Document Number
Barbados
Rev
SD
Date: Thursday, May 12, 2005
Sheet 29 of 44
<Core Design>



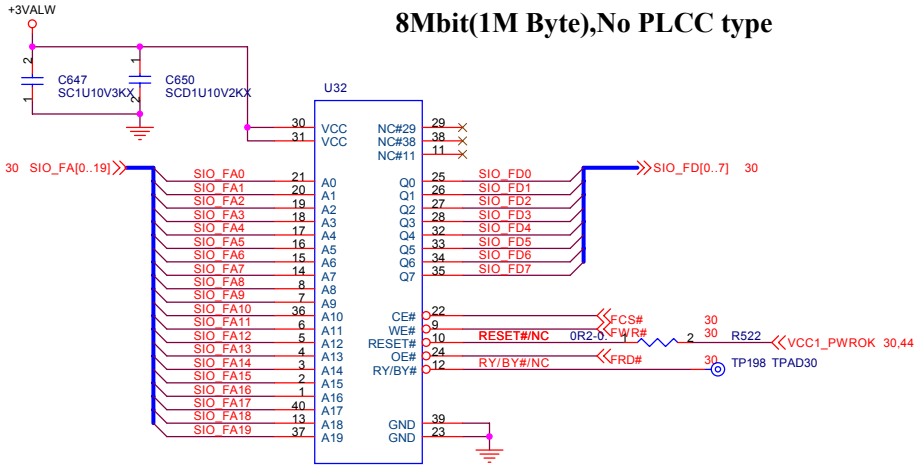
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

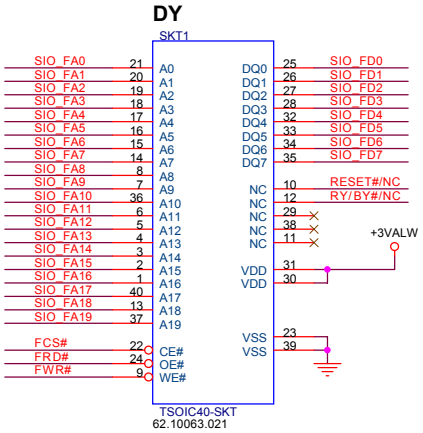
Title: Macallen III(2 of 2)

Size: A3 | Document Number: Barbados | Rev: SD

Date: Thursday, May 12, 2005 | Sheet 30 of 44

8Mbit(1M Byte),No PLCC type



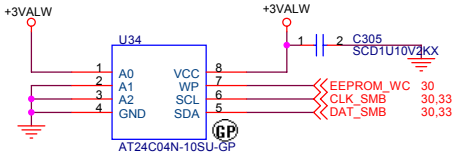


TSOIC 40 pin SOCKET
Co_layout with U28

MXIC: MX29LV008CTTI-90G "72.29008.G09" (Main sorce,LF,bottom boot block)
ST: M29W008AB-90 "72.29008.C09" (2nd sorce)

SMBus address A2

User Password



Atmel: AT24C04N-10SI "72.24C04.D01" (Main sorce)
ST : M24C04 "72.24C04.B01" (2nd sorce)

<Core Design>

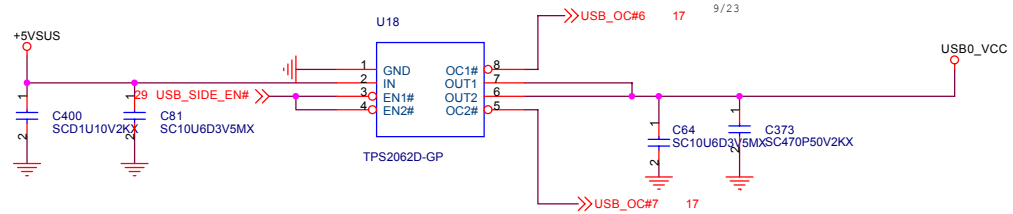
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS

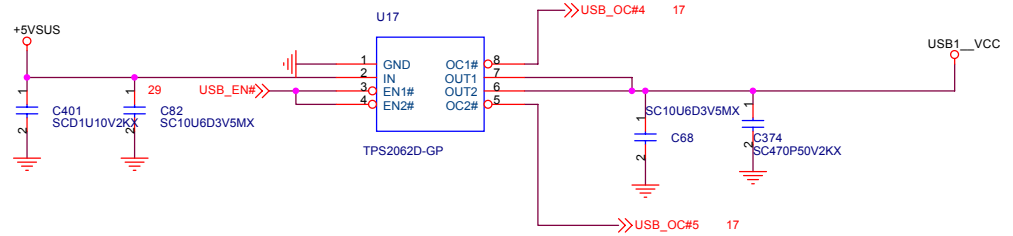
Size: A3 | Document Number: Barbados | Rev: SD

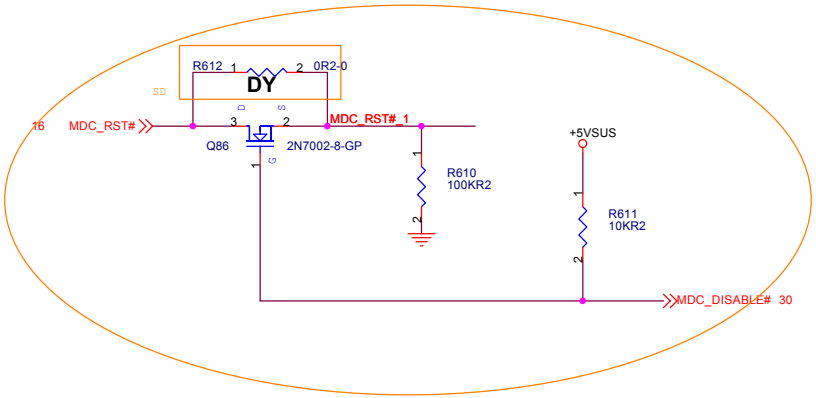
Date: Thursday, May 12, 2005 | Sheet 31 of 44

Dual USB0_VCC switch for USB6/USB7

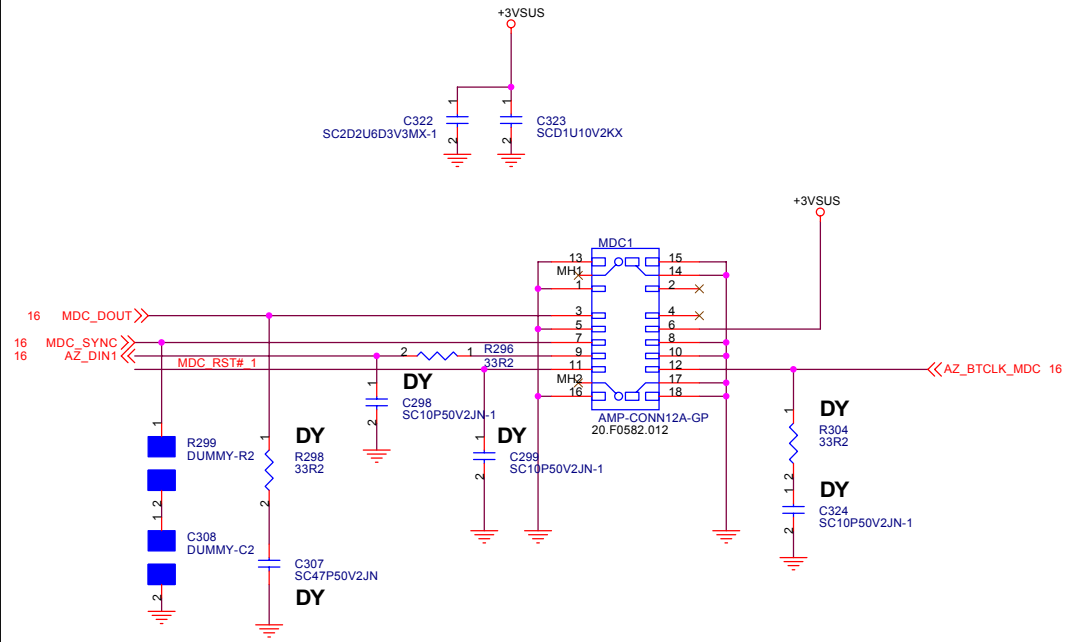


Dual USB1_VCC switch for USB4/USB5

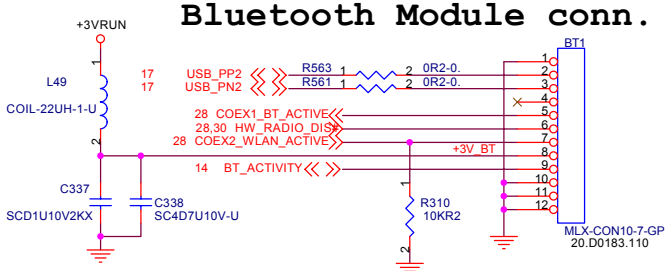




Modem Connector (Not Standard Type)



Bluetooth Module conn.

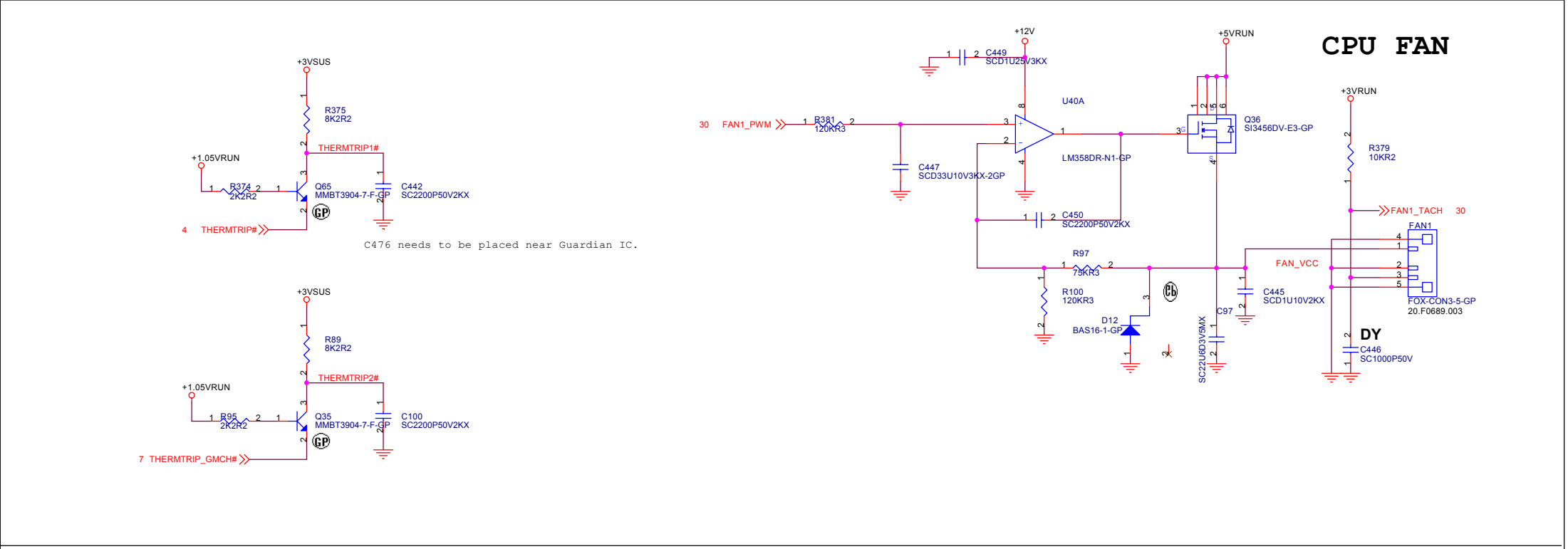


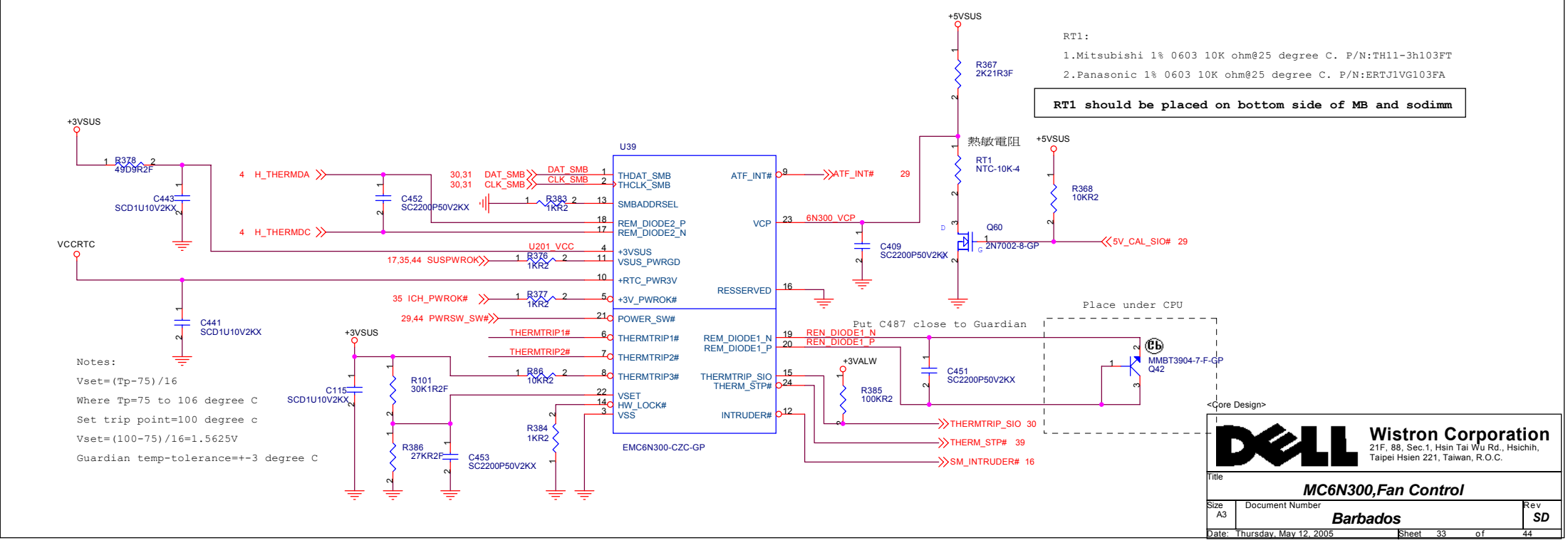
Note:Place R621 near CN13.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB / MDC /BT/FIR	
Size A3	Document Number Barbados	Rev SD
Date: Thursday, May 12, 2005	Sheet 32 of 44	





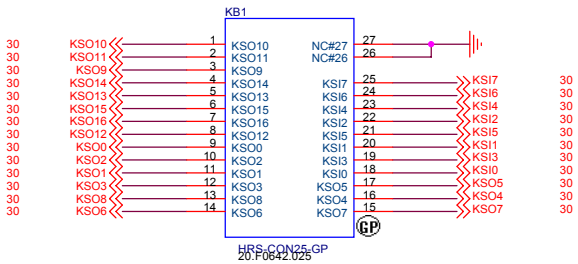
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

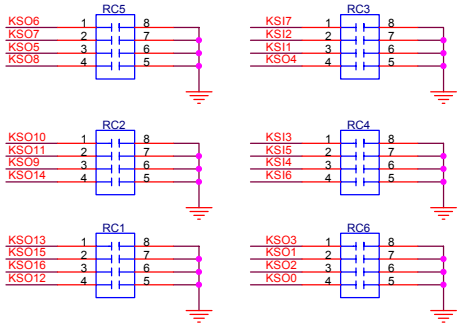
Title: *MC6N300,Fan Control*

Size	Document Number	Rev
A3	*Barbados*	*SD*

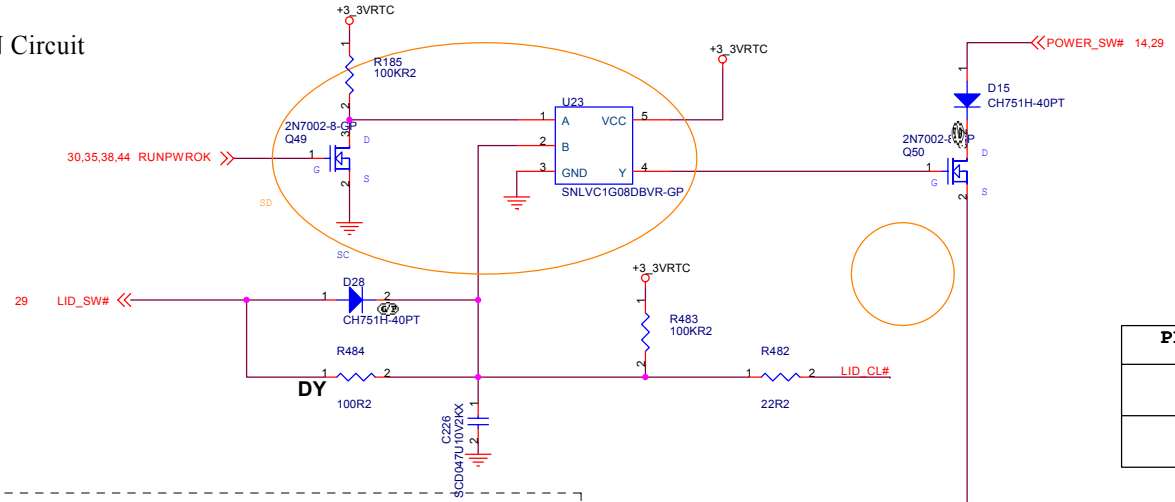
Date: Thursday, May 12, 2005 Sheet 33 of 44

KB CONN

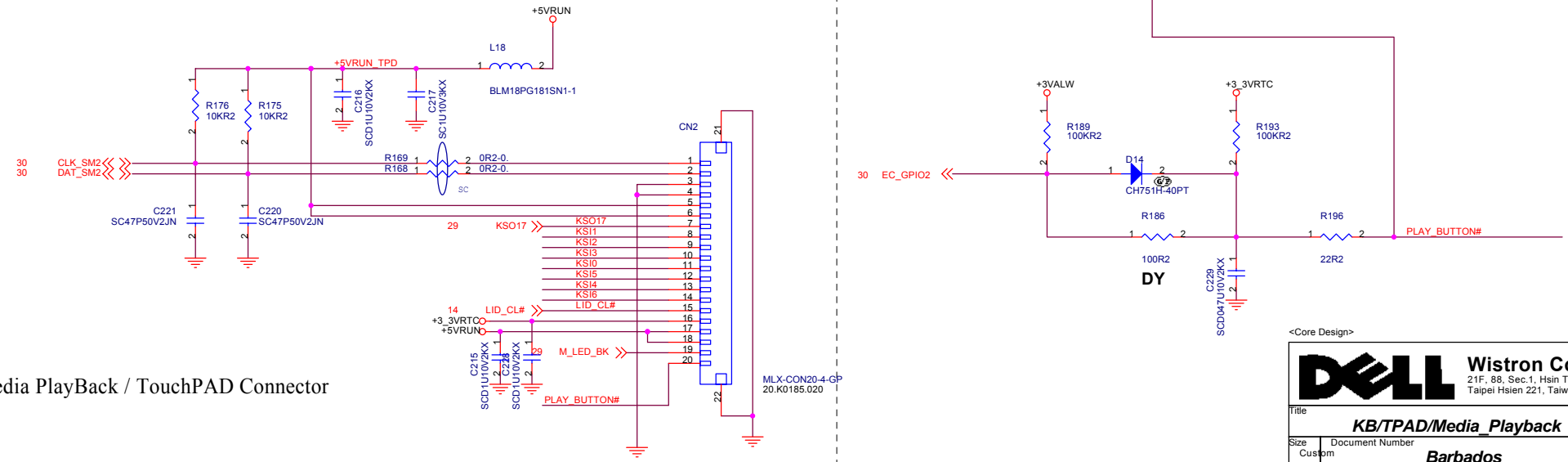




Instant ON Circuit



PLAY_PWR	PLAY_Button#
LOW	Regular Play Function
HIGH	Power On Function



Media PlayBack / TouchPAD Connector

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KB/TPAD/Media_Playback Conn

Size: Custom | Document Number: Barbados | Rev: SD

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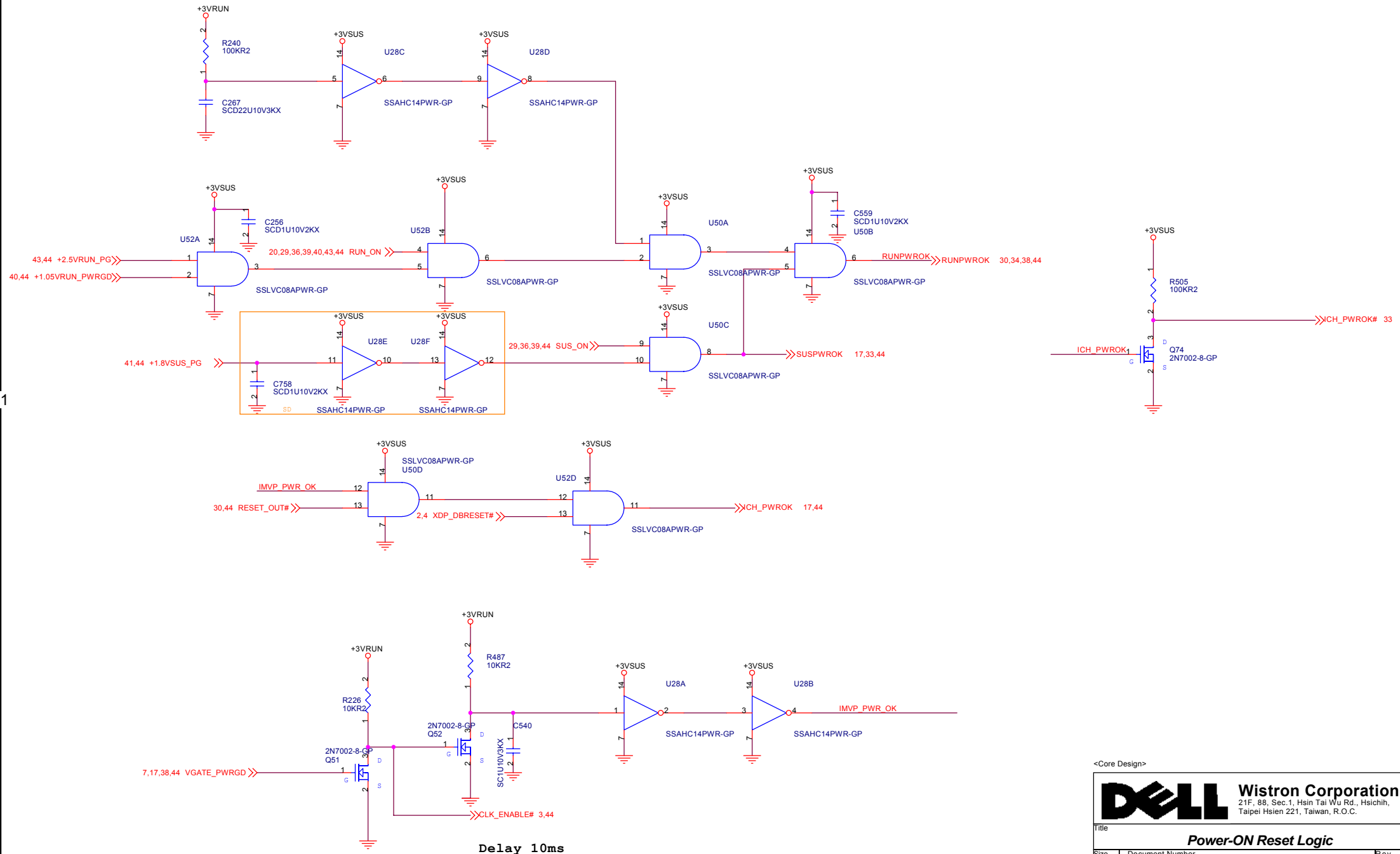

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power-ON Reset Logic***

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A3	***Barbados***	***SD***

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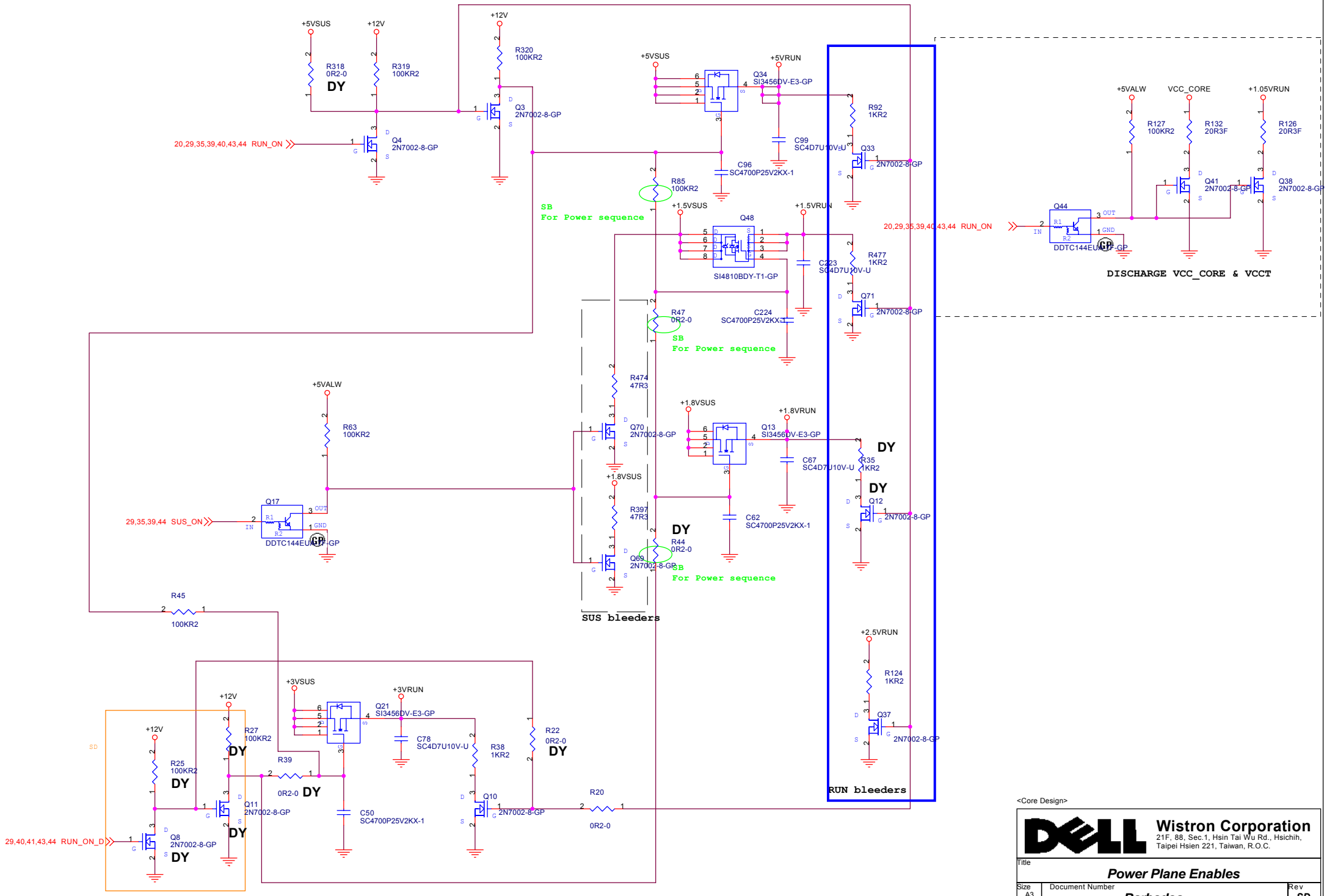

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enables

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A3	Barbados	SD

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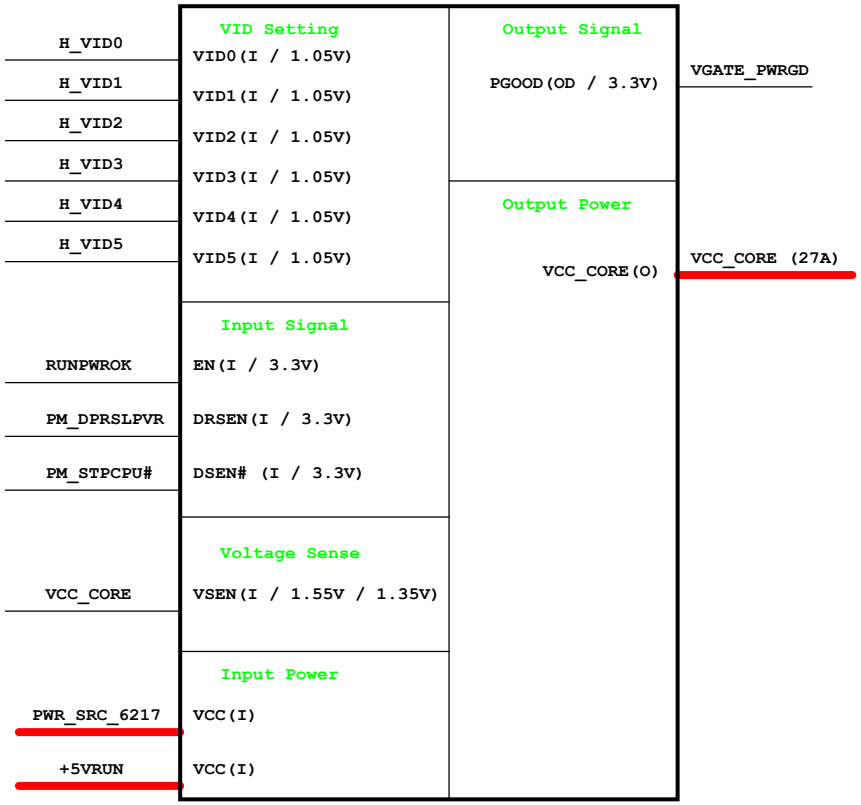
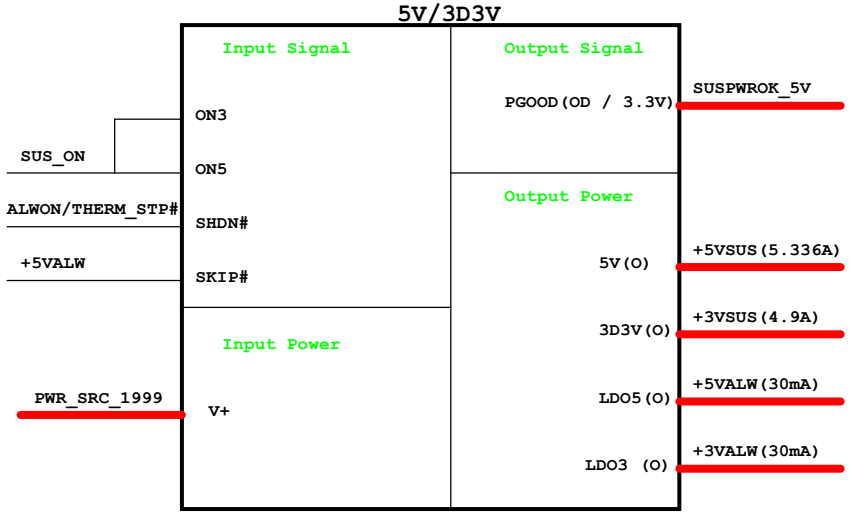
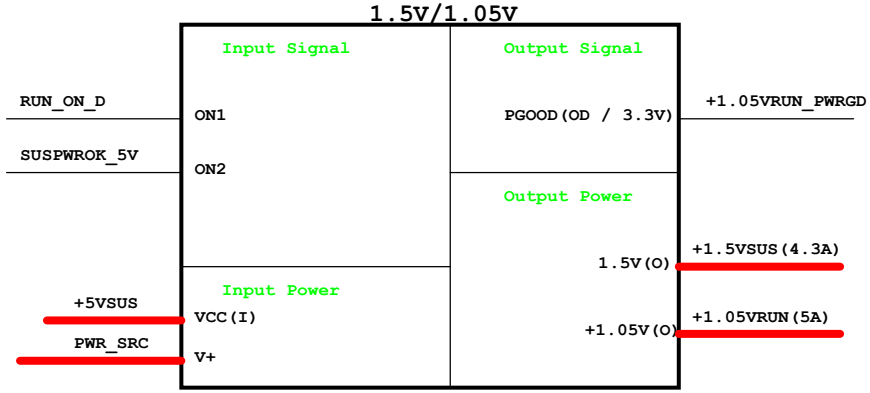
CPU_CORE ISL6217A



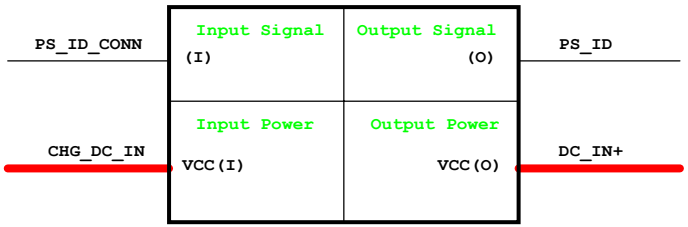
Max8734A 5V/3D3V



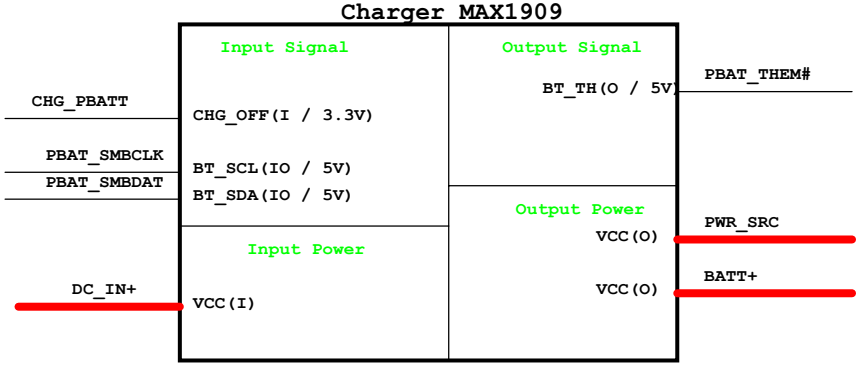
Max8743 1.5V/1.05V



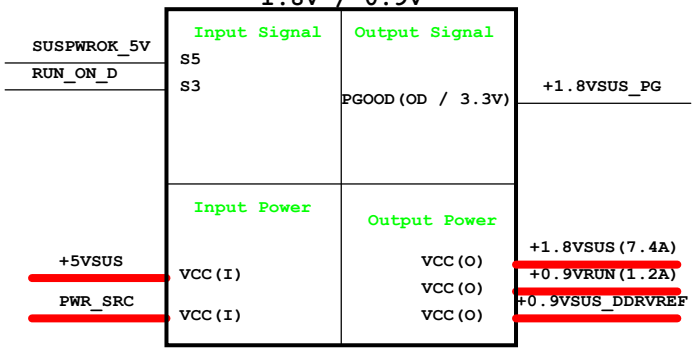
Adapter



Charger MAX1909



TI51116 1.8V / 0.9V



<Core Design>

Wistron Corporation
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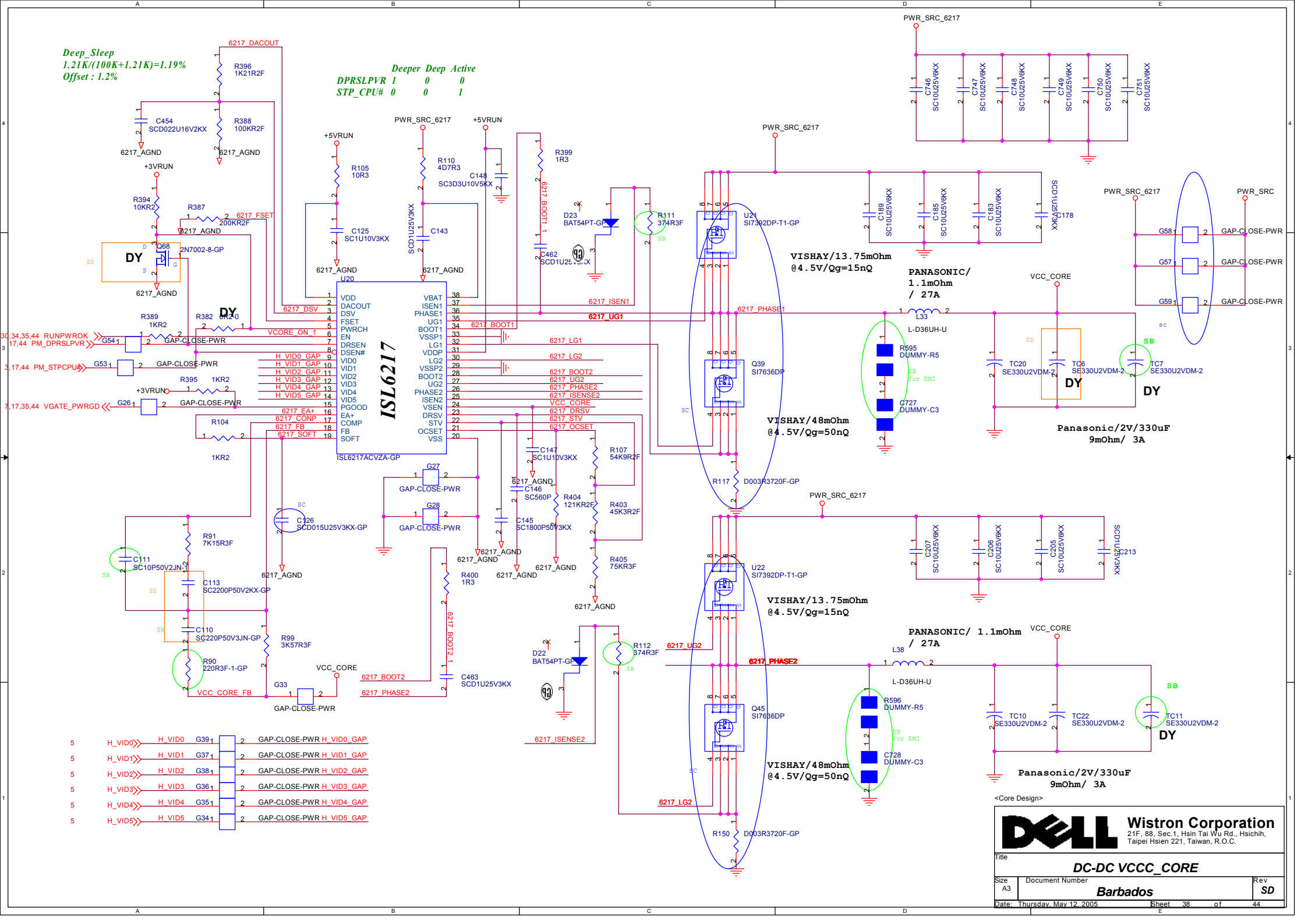
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

Size: A3 | Document Number: Barbados | Rev: SD

Date: Thursday, May 12, 2005 | Sheet 37 of 44


Deep_Sleep
1.21K/(100K+1.21K)=1.19%
Offset : 1.2%
Deeper Deep Active
DPRSLPVR 1 0 0
STP_CPU# 0 0 1
ISL6217
ISL6217ACVZA-GP
VISHAY/13.75mOhm
@4.5V/Qg=15nQ
VISHAY/48mOhm
@4.5V/Qg=50nQ
PANASONIC/
1.1mOhm
/ 27A
PANASONIC/ 1.1mOhm
/ 27A
Panasonic/2V/330uF
9mOhm/ 3A
Panasonic/2V/330uF
9mOhm/ 3A
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DC-DC VCCC_CORE
Barbados
SD
Date: Thursday, May 12, 2005
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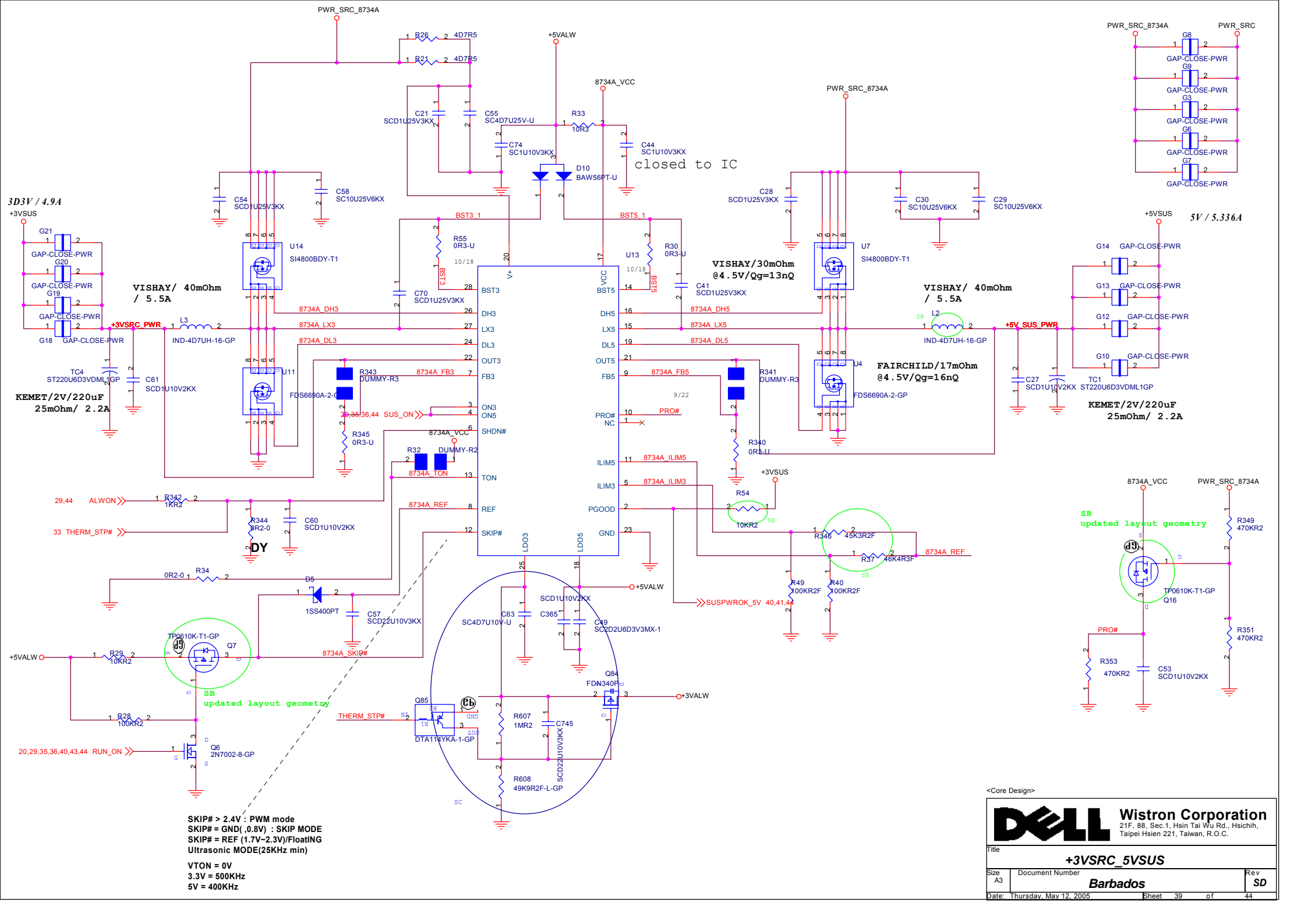
PWR_SRC_8734A
+5VALW
8734A_VCC
R26 4D7R5
R21 4D7R5
C21 SCD1U25V3KX
C55 SC4D7U25V-U
R33 10R3
C74 SC1U10V3KX
C44 SC1U10V3KX
closed to IC
D10 BAW56PT-U
3D3V / 4.9A
+3VSUS
C54 SCD1U25V3KX
C58 SC10U25V6KX
BST3_1
BST5_1
R55 0R3-U
R30 0R3-U
U14 SI4800BDY-T1
U13
C70 SCD1U25V3KX
C41 SCD1U25V3KX
VISHAY/ 40mOhm / 5.5A
8734A_DH3
8734A_LX3
8734A_DL3
+3VSRC_PWR
L3 IND-4D7UH-16-GP
G21 GAP-CLOSE-PWR
G20 GAP-CLOSE-PWR
G19 GAP-CLOSE-PWR
G18 GAP-CLOSE-PWR
TC4 ST220U6D3VDML1GP
C61 SCD1U10V2KX
KEMET/2V/220uF 25mOhm/ 2.2A
U11 FDS6690A-2-GP
R343 DUMMY-R3
8734A_FB3
29,35,36,44 SUS_ON
R345 0R3-U
8734A_VCC
R32 DUMMY-R2
8734A_TON
BST3
DH3
LX3
DL3
OUT3
FB3
ON3
ON5
SHDN#
TON
REF
SKIP#
V+
VCC
BST5
DH5
LX5
DL5
OUT5
FB5
PRO# NC
ILIM5
ILIM3
PGOOD
GND
LDO3
LDO5
8734A_DH5
8734A_LX5
8734A_DL5
8734A_FB5
PRO#
8734A_ILIM5
8734A_ILIM3
R341 DUMMY-R3
R340 0R3-U
R54
10KR2
+3VSUS
R346 45K3R2F
R37 46K4R3F
8734A_REF
R49 100KR2F
R40 100KR2F
SUSPWROK_5V 40,41,44
PWR_SRC_8734A
C28 SCD1U25V3KX
C30 SC10U25V6KX
C29 SC10U25V6KX
U7 SI4800BDY-T1
VISHAY/30mOhm @4.5V/Qg=13nQ
VISHAY/ 40mOhm / 5.5A
L2 IND-4D7UH-16-GP
+5V_SUS_PWR
U4 FDS6690A-2-GP
FAIRCHILD/17mOhm @4.5V/Qg=16nQ
C27 SCD1U10V2KX
TC1 ST220U6D3VDML1GP
KEMET/2V/220uF 25mOhm/ 2.2A
5V / 5.336A
+5VSUS
G14 GAP-CLOSE-PWR
G13 GAP-CLOSE-PWR
G12 GAP-CLOSE-PWR
G10 GAP-CLOSE-PWR
PWR_SRC_8734A
PWR_SRC
G8 GAP-CLOSE-PWR
G9 GAP-CLOSE-PWR
G3 GAP-CLOSE-PWR
G6 GAP-CLOSE-PWR
G7 GAP-CLOSE-PWR
29,44 ALWON
R342 1KR2
33 THERM_STP#
R344 0R2-0
C60 SCD1U10V2KX
DY
R34 0R2-0
D5 1SS400PT
C57 SCD22U10V3KX
8734A_SKIP#
TP0610K-T1-GP Q7
R29 10KR2
R28 100KR2
20,29,35,36,40,43,44 RUN_ON
Q6 2N7002-8-GP
SB
updated layout geometry
C63 SC4D7U10V-U
C365 SCD1U10V2KX
C49 SC2D2U6D3V3MX-1
+5VALW
Q84 FDN340P
+3VALW
Q85 DTA114YKA-1-GP
THERM_STP#
R607 1MR2
C745 SCD22U10V3KX
R608 49K9R2F-L-GP
SC
8734A_VCC
PWR_SRC_8734A
SB
updated layout geometry
R349 470KR2
TP0610K-T1-GP Q16
PRO#
R353 470KR2
C53 SCD1U10V2KX
R351 470KR2
SKIP# > 2.4V : PWM mode
SKIP# = GND(,0.8V) : SKIP MODE
SKIP# = REF (1.7V~2.3V)/FloatING
Ultrasonic MODE(25KHz min)
VTON = 0V
3.3V = 500KHz
5V = 400KHz
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
+3VSRC_5VSUS
Size A3
Document Number
Barbados
Rev SD
Date: Thursday, May 12, 2005
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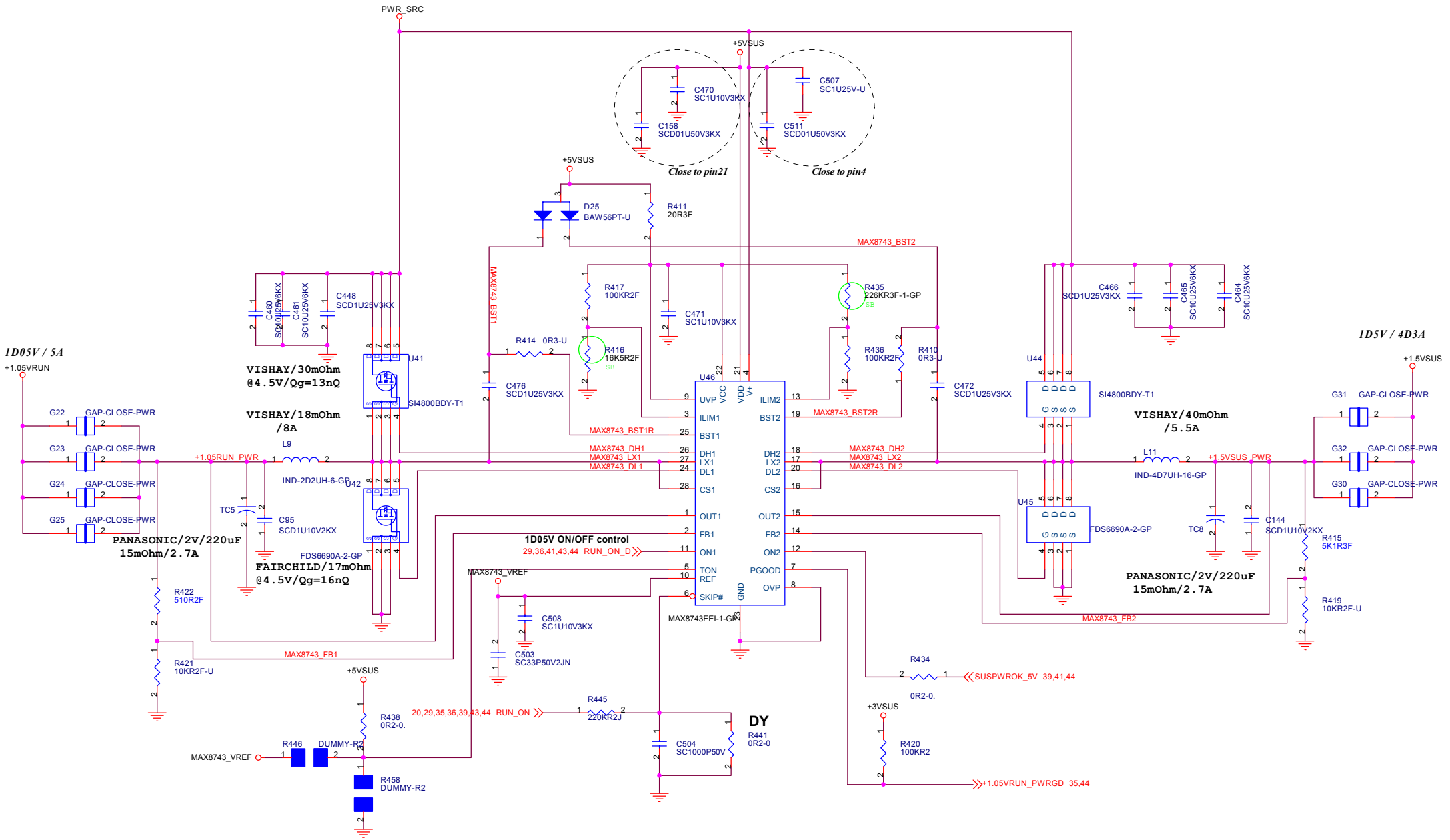

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **+1.5VSUS_1.05VRUN**

Size	Document Number	Rev
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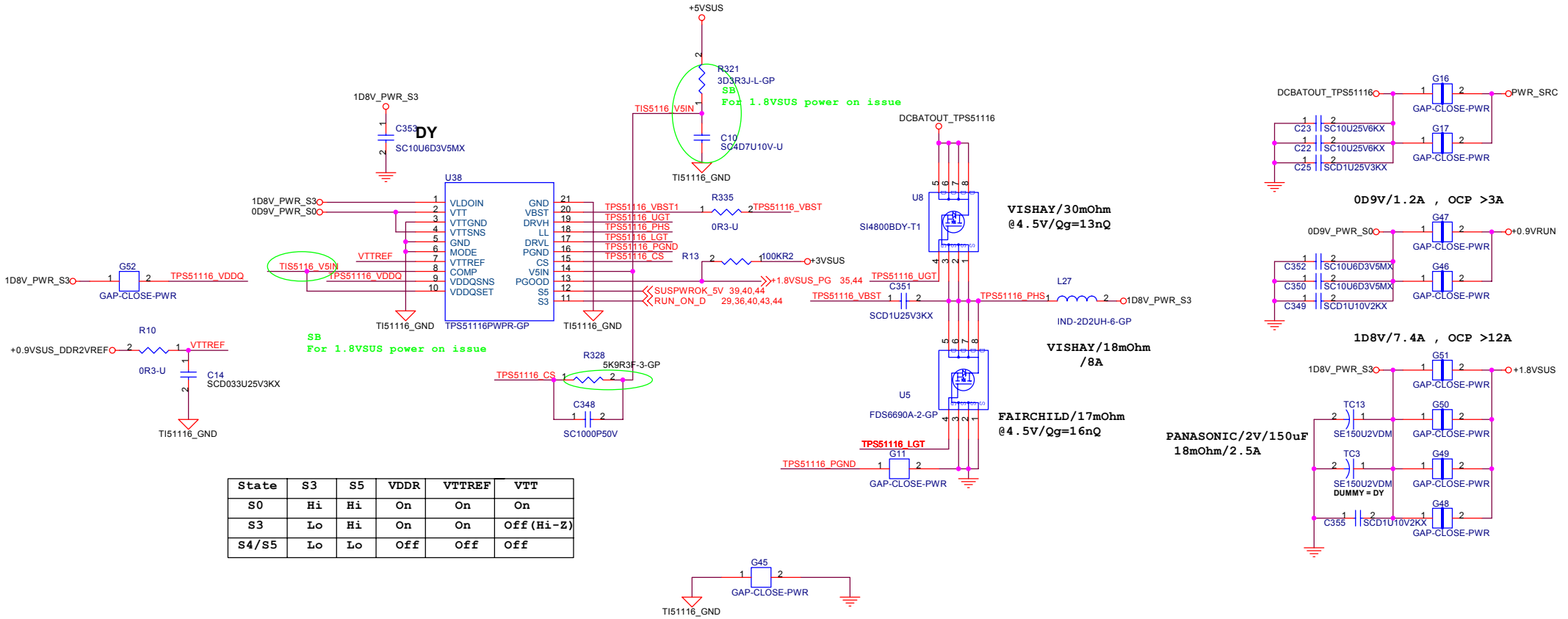
TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

<Core Design>

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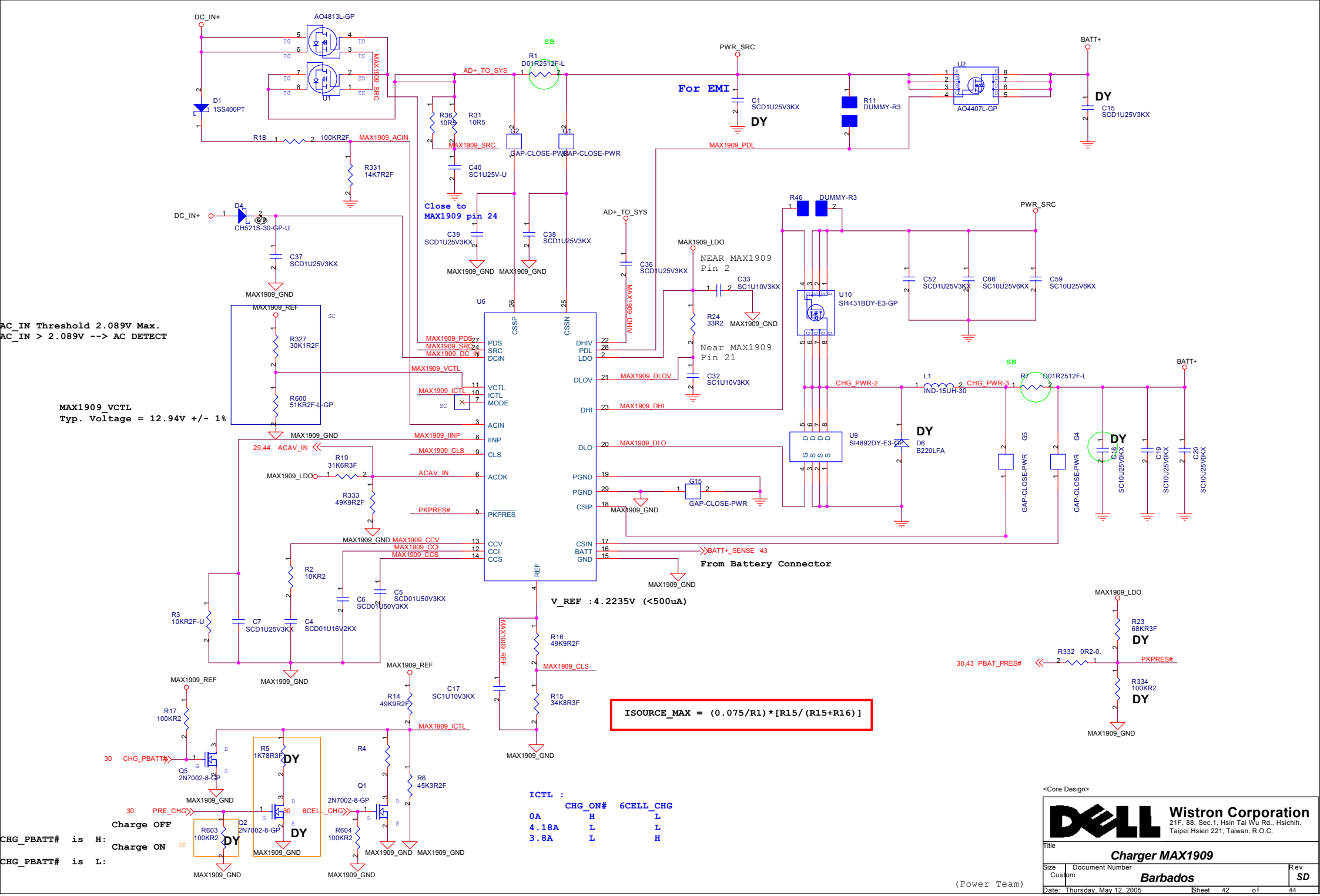
Taipei Hsien 221, Taiwan, R.O.C.

Title: *+1.8VSUS&0.9VRUN&DDR2_VREF*

Size: A3 | Document Number: *Barbados* | Rev: *SD*

Date: Thursday, May 12, 2005 | Sheet 41 of 44


DC_IN+
AO4813L-GP
MAX1909_SRC
D1
1SS400PT
R18 100KR2F
MAX1909_ACIN
R331 14K7R2F
SB
R1 D01R2512F-L
AD+_TO_SYS
PWR_SRC
For EMI
C1 SCD1U25V3KX
DY
R11 DUMMY-R3
U2
AO4407L-GP
BATT+
C15 SCD1U25V3KX
R36 10R5
R31 10R5
MAX1909_SRC
C40 SC1U25V-U
GAP-CLOSE-PWR
MAX1909_PDL
Close to MAX1909 pin 24
C39 SCD1U25V3KX
C38 SCD1U25V3KX
MAX1909_GND
D4
CH521S-30-GP-U
C37 SCD1U25V3KX
R46 DUMMY-R3
C36 SCD1U25V3KX
MAX1909_LDO
NEAR MAX1909 Pin 2
C33 SC1U10V3KX
R24 33R2
Near MAX1909 Pin 21
C32 SC1U10V3KX
U10 SI4431BDY-E3-GP
C52 SCD1U25V3KX
C66 SC10U25V6KX
C59 SC10U25V6KX
AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
MAX1909_REF
R327 30K1R2F
R600 51KR2F-L-GP
MAX1909_VCTL
Typ. Voltage = 12.94V +/- 1%
U6
CSSP
CSSN
PDS
SRC
DCIN
VCTL
ICTL
MODE
ACIN
IINP
CLS
ACOK
PKPRES
CCV
CCI
CCS
DHIV
PDL
LDO
DLOV
DHI
DLO
PGND
CSIP
CSIN
BATT
GND
REF
MAX1909_PDS
MAX1909_SRC
MAX1909_DC_IN
MAX1909_ICTL
MAX1909_IINP
MAX1909_CLS
MAX1909_DLOV
MAX1909_DHI
MAX1909_DLO
MAX1909_CCV
MAX1909_CCI
MAX1909_CCS
29,44 ACAV_IN
ACAV_IN
R19 31K6R3F
R333 49K9R2F
PKPRES#
CHG_PWR-2
L1 IND-15UH-30
CHG_PWR-3
R7 D01R2512F-L
U9 SI4892DY-E3-GP
D6 B220LFA
G5
G4
GAP-CLOSE-PWR
C18 SC10U25V0KX
C19 SC10U25V0KX
C20 SC10U25V0KX
G15
BATT+_SENSE 43
From Battery Connector
R2 10KR2
R3 10KR2F-U
C7 SCD1U25V3KX
C4 SCD01U16V2KX
C6 SCD01U50V3KX
C5 SCD01U50V3KX
V_REF :4.2235V (<500uA)
R16 49K9R2F
R15 34K8R3F
C17 SC1U10V3KX
R14 49K9R2F
MAX1909_ICTL
ISOURCE_MAX = (0.075/R1)*[R15/(R15+R16)]
R23 68KR3F
R332 0R2-0.
30,43 PBAT_PRES#
R334 100KR2
R17 100KR2
30 CHG_PBATT#
Q5 2N7002-8-GP
R5 1K78R3F
R4
R6 45K3R2F
Q1 2N7002-8-GP
30 PRE_CHG
Q2 2N7002-8-GP
R603 100KR2
6CELL_CHG
R604 100KR2
Charge OFF
Charge ON
CHG_PBATT# is H:
CHG_PBATT# is L:
ICTL :
CHG_ON# 6CELL_CHG
0A H L
4.18A L L
3.8A L H
(Power Team)
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Charger MAX1909
Size Custom
Document Number Barbados
Rev SD
Date: Thursday, May 12, 2005
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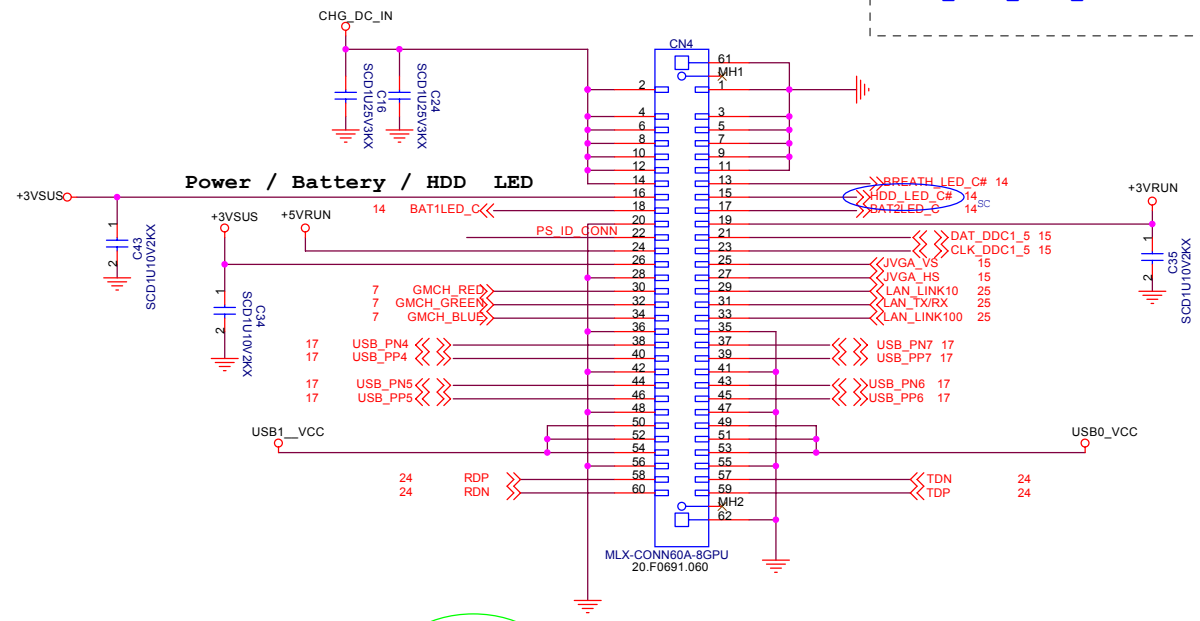
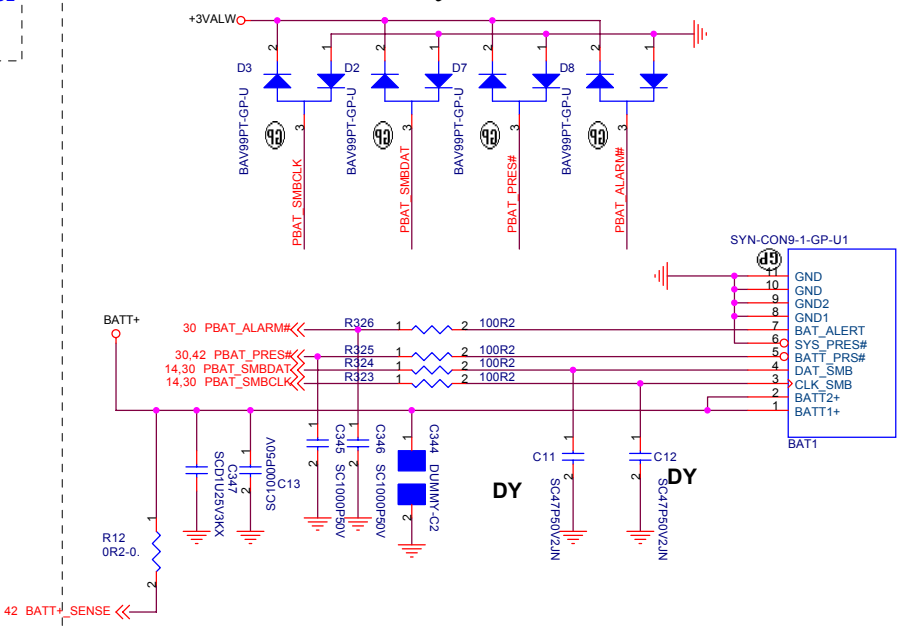
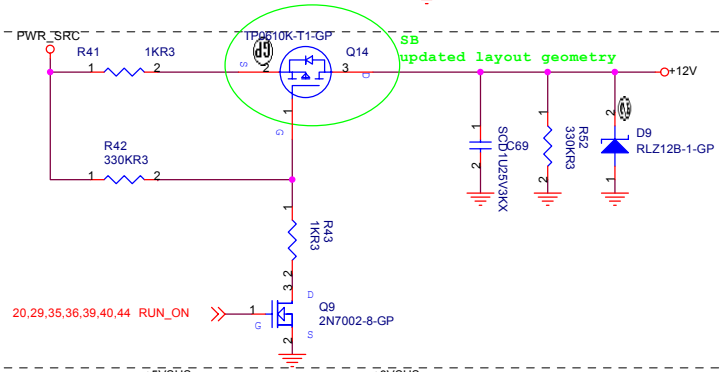
TV BD Conn

Layout Note:
Must be a ground return path for
CRT_R,CRT_G,CRT_B

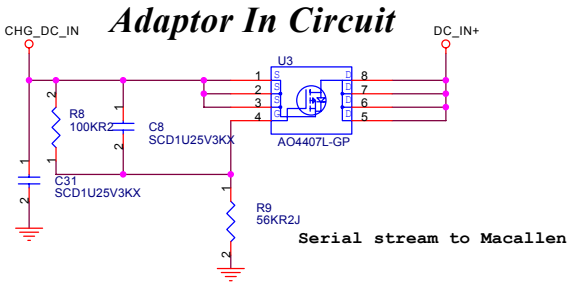


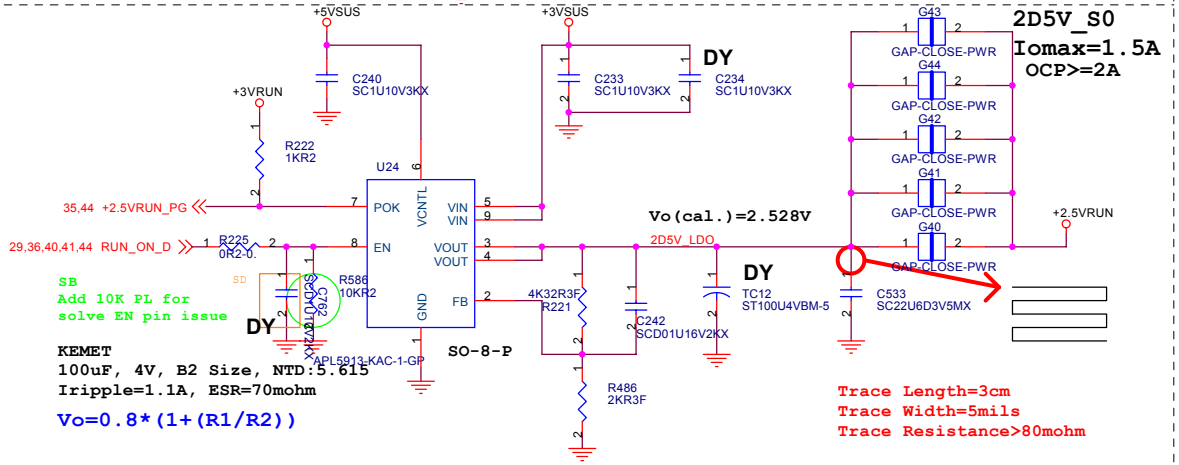
Battery Conn

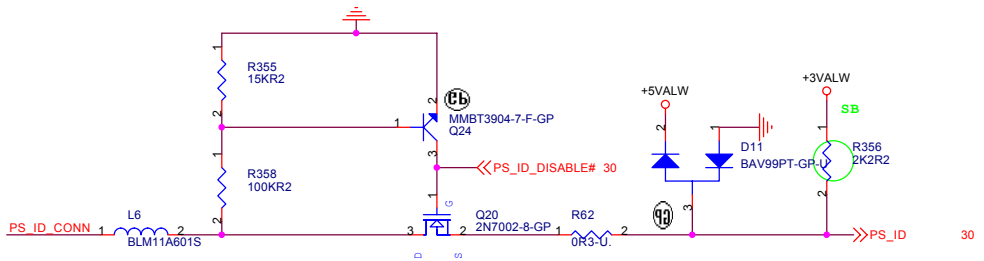




Adaptor In Circuit







<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Battery/TV/Adaptor Conn/+2.5VSUS

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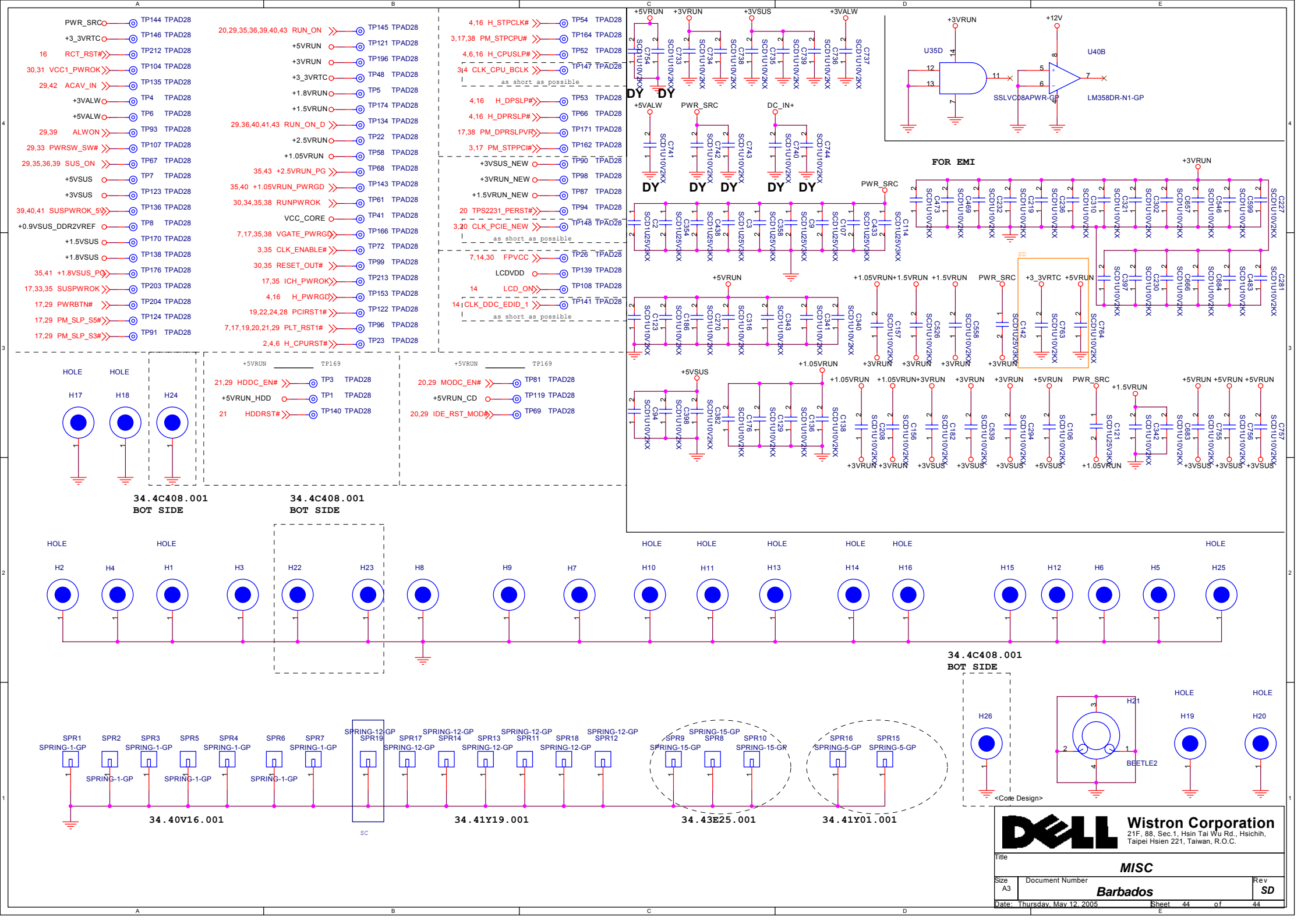
PWR_SRC TP144 TPAD28
+3_3VRTC TP146 TPAD28
16 RCT_RST# TP212 TPAD28
30,31 VCC1_PWROK TP104 TPAD28
29,42 ACAV_IN TP135 TPAD28
+3VALW TP4 TPAD28
+5VALW TP6 TPAD28
29,39 ALWON TP93 TPAD28
29,33 PWRSW_SW# TP107 TPAD28
29,35,36,39 SUS_ON TP67 TPAD28
+5VSUS TP7 TPAD28
+3VSUS TP123 TPAD28
39,40,41 SUSPWROK_5V TP136 TPAD28
+0.9VSUS_DDR2VREF TP8 TPAD28
+1.5VSUS TP170 TPAD28
+1.8VSUS TP138 TPAD28
35,41 +1.8VSUS_PG TP176 TPAD28
17,33,35 SUSPWROK TP203 TPAD28
17,29 PWRBTN# TP204 TPAD28
17,29 PM_SLP_S5# TP124 TPAD28
17,29 PM_SLP_S3# TP91 TPAD28
20,29,35,36,39,40,43 RUN_ON TP145 TPAD28
+5VRUN TP121 TPAD28
+3VRUN TP196 TPAD28
+3_3VRTC TP48 TPAD28
+1.8VRUN TP5 TPAD28
+1.5VRUN TP174 TPAD28
29,36,40,41,43 RUN_ON_D TP134 TPAD28
+2.5VRUN TP22 TPAD28
+1.05VRUN TP58 TPAD28
35,43 +2.5VRUN_PG TP68 TPAD28
35,40 +1.05VRUN_PWRGD TP143 TPAD28
30,34,35,38 RUNPWROK TP61 TPAD28
VCC_CORE TP41 TPAD28
7,17,35,38 VGATE_PWRGD TP166 TPAD28
3,35 CLK_ENABLE# TP72 TPAD28
30,35 RESET_OUT# TP99 TPAD28
17,35 ICH_PWROK TP213 TPAD28
4,16 H_PWRGD TP153 TPAD28
19,22,24,28 PCIRST1# TP122 TPAD28
7,17,19,20,21,29 PLT_RST1# TP96 TPAD28
2,4,6 H_CPURST# TP23 TPAD28
4,16 H_STPCLK# TP54 TPAD28
3,17,38 PM_STPCPU# TP164 TPAD28
4,6,16 H_CPUSLP# TP52 TPAD28
3,4 CLK_CPU_BCLK TP147 TPAD28
as short as possible
4,16 H_DPSLP# TP53 TPAD28
4,16 H_DPRSLP# TP66 TPAD28
17,38 PM_DPRSLPVR TP171 TPAD28
3,17 PM_STPPCI# TP162 TPAD28
+3VSUS_NEW TP90 TPAD28
+3VRUN_NEW TP98 TPAD28
+1.5VRUN_NEW TP87 TPAD28
20 TPS2231_PERST# TP94 TPAD28
3,20 CLK_PCIE_NEW TP148 TPAD28
as short as possible
7,14,30 FPVCC TP26 TPAD28
LCDVDD TP139 TPAD28
14 LCD_ON TP108 TPAD28
14 CLK_DDC_EDID_1 TP141 TPAD28
as short as possible
+5VRUN TP169
21,29 HDDC_EN# TP3 TPAD28
+5VRUN_HDD TP1 TPAD28
21 HDDRST# TP140 TPAD28
+5VRUN TP169
20,29 MODC_EN# TP81 TPAD28
+5VRUN_CD TP119 TPAD28
20,29 IDE_RST_MOD# TP69 TPAD28
HOLE H17
HOLE H18
HOLE H24
34.4C408.001
BOT SIDE
34.4C408.001
BOT SIDE
+5VRUN +3VRUN +3VSUS +3VALW
DY DY
+5VALW PWR_SRC DC_IN+
DY DY DY DY DY
FOR EMI
+3VRUN
PWR_SRC
+5VRUN
+1.05VRUN +1.5VRUN +1.5VRUN
PWR_SRC +3_3VRTC +5VRUN
+5VSUS
+1.05VRUN
+1.05VRUN +1.05VRUN +3VRUN +3VRUN +3VRUN +5VRUN PWR_SRC +1.5VRUN
+5VRUN +5VRUN +5VRUN
U35D
U40B
SSLVC08APWR-GP
LM358DR-N1-GP
HOLE H2
HOLE H4
H1
H3
H22
H23
H8
H9
H7
H10
H11
H13
H14
H16
H15
H12
H6
H5
HOLE H25
34.4C408.001
BOT SIDE
SPR1 SPRING-1-GP
SPR2 SPRING-1-GP
SPR3 SPRING-1-GP
SPR5 SPRING-1-GP
SPR4 SPRING-1-GP
SPR6 SPRING-1-GP
SPR7 SPRING-1-GP
SPR19 SPRING-12-GP
SPR17 SPRING-12-GP
SPR14 SPRING-12-GP
SPR13 SPRING-12-GP
SPR11 SPRING-12-GP
SPR18 SPRING-12-GP
SPR12 SPRING-12-GP
SPR9 SPRING-15-GP
SPR8 SPRING-15-GP
SPR10 SPRING-15-GP
SPR16 SPRING-5-GP
SPR15 SPRING-5-GP
34.40V16.001
SC
34.41Y19.001
34.43E25.001
34.41Y01.001
H26
<Core Design>
H21
BEETLE2
HOLE H19
HOLE H20
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
MISC
Size A3
Document Number
Barbados
Rev SD
Date: Thursday, May 12, 2005
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