

FIRENZE2-R

CPU : Intel Yonah/Merom (533/667MHz)
Chip Set : RS600ME & SB600
Remarks : Mobility Platform

Model Name : FIRENZE II R

PBA Name : MAIN

PCB Code : TPT : BA41-00714A
GCE : BA41-00715A

Dev. Step : MP (6-Layer)

Revision : 1.0

T.R. Date : 2006.01.11

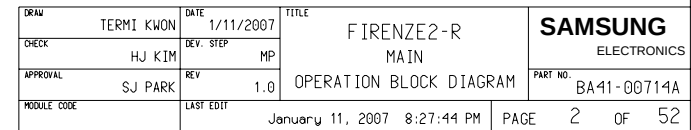
DRAW	CHECK	APPROVAL
TERMI	HJ KIM	SJ PARK

Owner : SEC Mobile R & D Signature : X

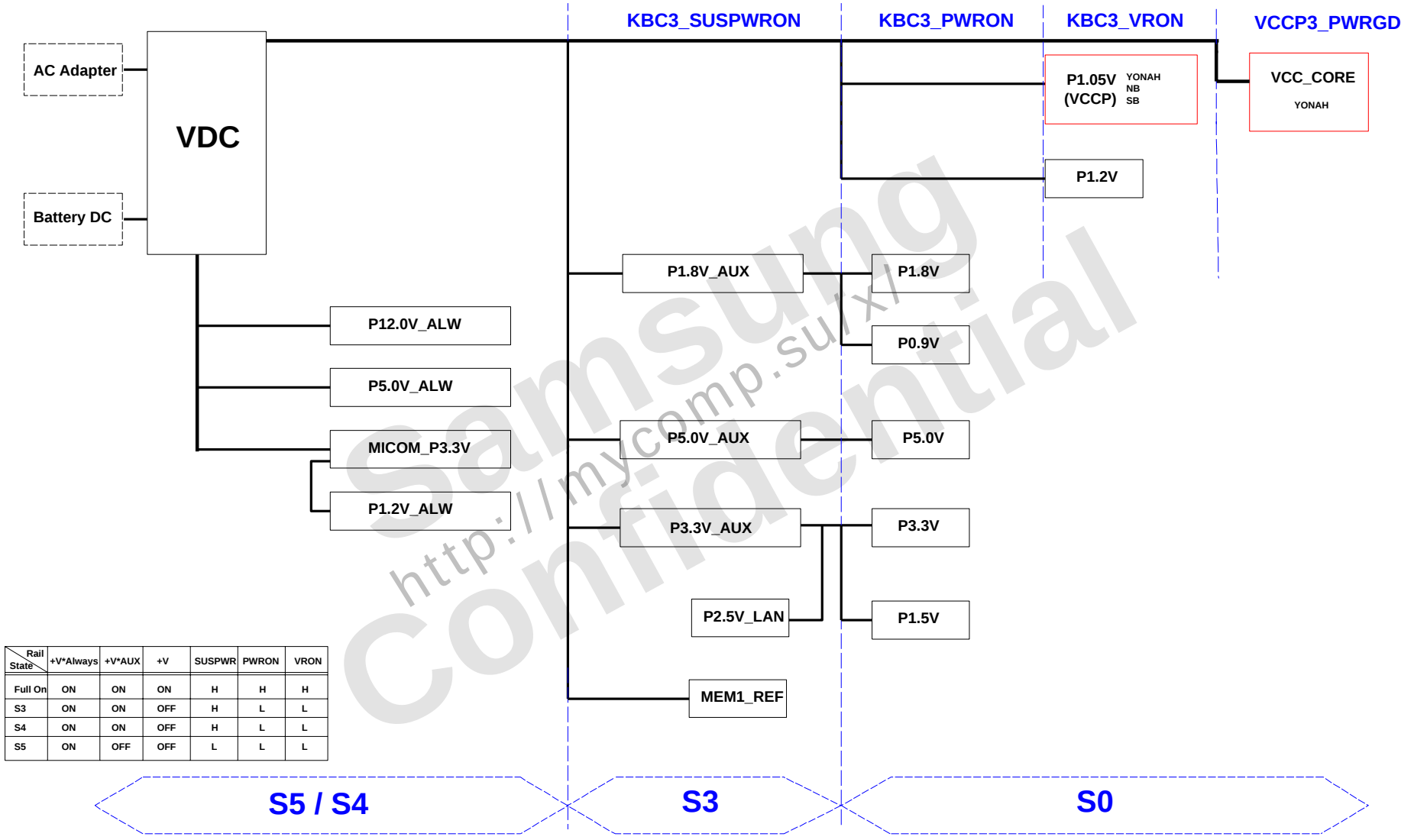
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DRAW	TERMI KWON	DATE	1/11/2007	TITLE	FIRENZE2-R	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		COVER	
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	1 OF 52	PART NO. BA41-00714A

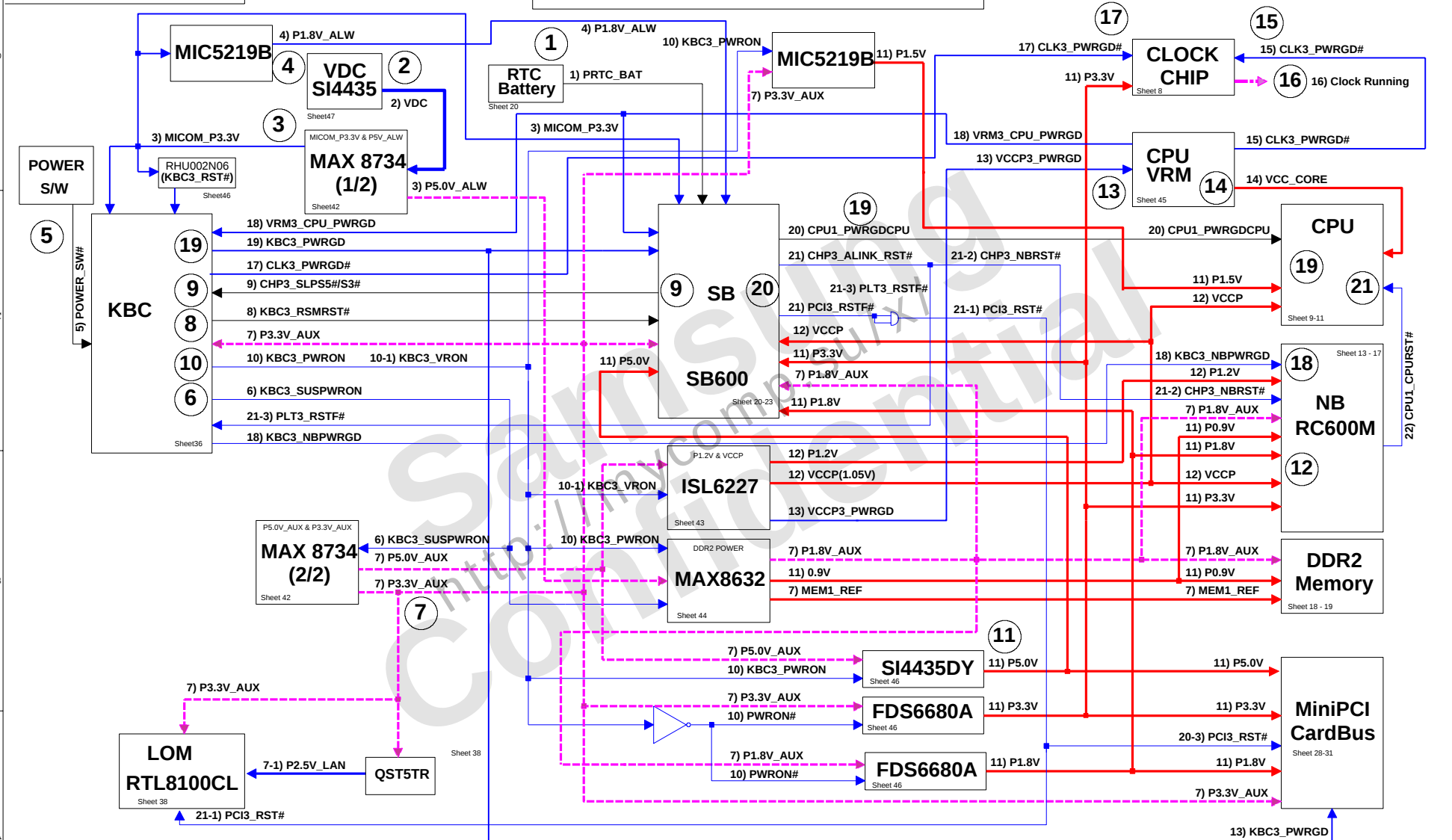


Power Diagram

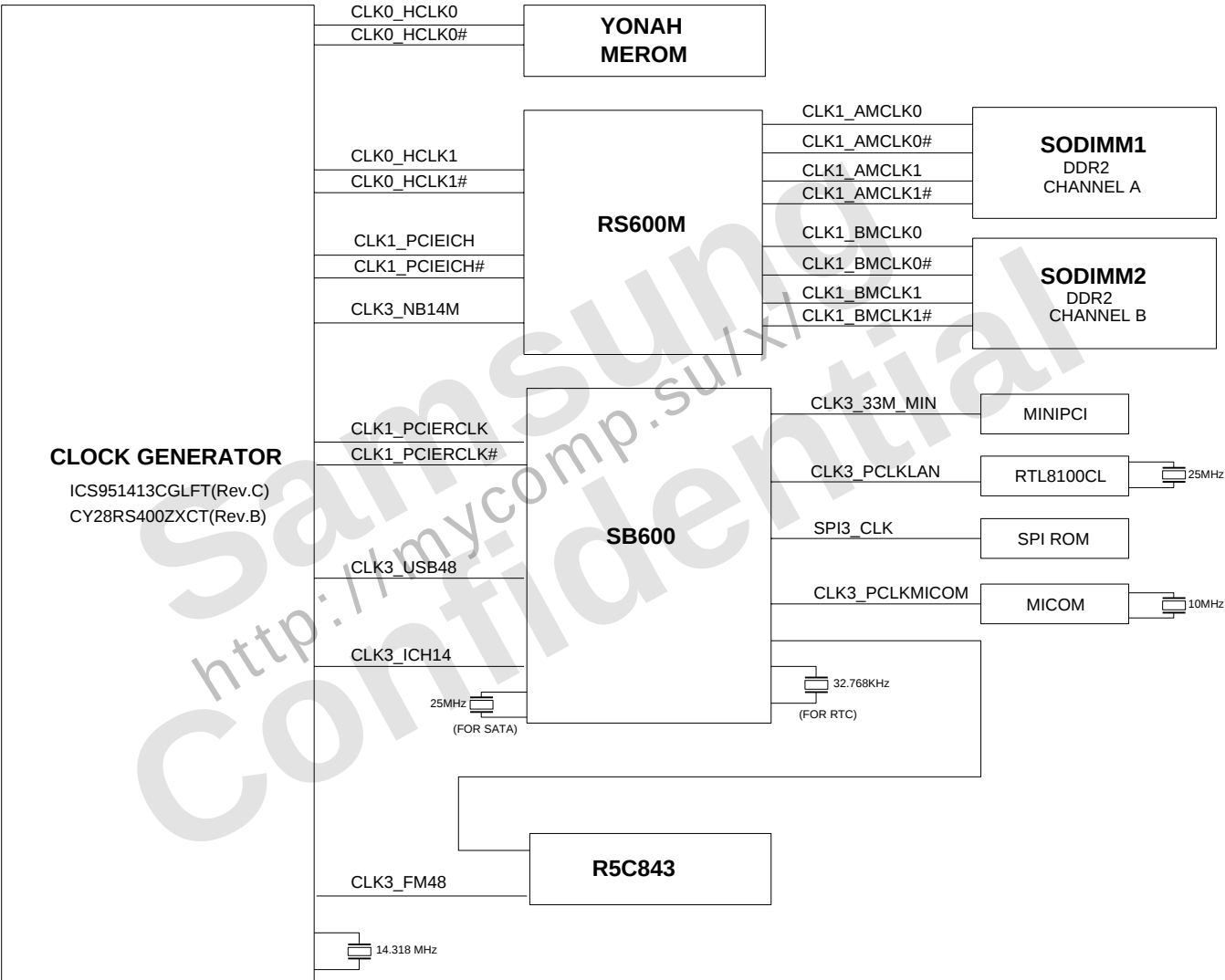


Rail State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	ON	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L

POWER SEQUENCE Rev. 0.1



DRAW	TERMI KWON	DATE	1/11/2007	TITLE	FIRENZE2-R	SAMSUNG ELECTRONICS PART NO. BA41-00714A
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0	POWER SEQUENCE		
MODULE CODE		LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	4 OF 52	



DRAW	TERMI KWON	DATE	1/11/2007	TITLE	FIRENZE2-R CLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			PART NO. BA41-00714A
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	5 OF 52	

d:/users/mobile62/mentor/licenze2 r/F2-R-SR 01

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB600	Real Time Clock
Crystal	25MHz	SB600	SATA
Crystal	10MHz	MICOM	HBS-2110B
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	25MHz	LAN	LOM

MVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6.0)	Voltage	VID(6.0)	Voltage	VID(6.0)	Voltage
0 0 0 0 0 0 0 0	1.5000 V	0 1 0 0 1 0 0 0	1.0000 V	1 0 0 1 0 0 0 0	0.4875 V
0 0 0 0 0 0 0 0	1.4875 V	0 1 0 0 1 0 0 0	0.9875 V	1 0 1 0 0 0 0 1	0.4750 V
0 0 0 0 0 0 0 0	1.4750 V	0 0 1 0 0 1 0 1 0	0.9750 V	1 0 0 1 0 0 0 1	0.4625 V
0 0 0 0 0 0 0 1	1.4625 V	0 0 1 0 0 1 0 1 0	0.9625 V	1 0 0 1 0 0 0 1	0.4500 V
0 0 0 0 0 0 0 1	1.4500 V	0 1 0 0 1 0 0 0	0.9500 V	1 0 1 0 0 0 0 1	0.4375 V
0 0 0 0 0 0 1 0	1.4375 V	0 0 1 0 0 1 0 1 0	0.9375 V	1 0 0 1 0 0 0 1	0.4250 V
0 0 0 0 0 0 1 0	1.4250 V	0 0 1 0 0 1 0 1 0	0.9250 V	1 0 0 1 0 0 0 1	0.4125 V
0 0 0 0 0 0 1 1	1.4125 V	0 0 1 0 0 1 0 1 1	0.9125 V	1 0 0 1 0 0 0 0	0.4000 V
0 0 0 0 0 1 0 0	1.4000 V	0 0 1 0 0 0 0 0 0	0.9000 V	1 0 1 1 0 0 0 0	0.3875 V
0 0 0 0 0 1 0 0	1.3875 V	0 1 0 0 0 0 0 0 1	0.8875 V	1 0 0 1 0 0 0 0	0.3750 V
0 0 0 0 0 1 0 1	1.3750 V	0 0 1 0 0 0 0 0 1	0.8750 V	1 0 0 1 0 0 0 1	0.3625 V
0 0 0 0 0 1 0 1	1.3625 V	0 0 1 0 0 0 0 0 1	0.8625 V	1 0 0 1 0 0 0 0	0.3500 V
0 0 0 0 0 1 1 0 0	1.3500 V	0 0 1 0 0 0 0 0 0	0.8500 V	1 0 0 1 0 0 0 0	0.3375 V
0 0 0 0 0 1 1 0 0	1.3375 V	0 0 1 0 0 0 0 0 0	0.8375 V	1 0 0 1 0 0 0 0	0.3250 V
0 0 0 0 0 1 1 0 0	1.3250 V	0 0 1 0 0 0 0 0 0	0.8250 V	1 0 0 1 0 0 0 0	0.3125 V
0 0 0 0 0 1 1 1 0	1.3125 V	0 0 1 0 0 0 0 0 0	0.8125 V	1 0 0 0 0 0 0 0	0.3000 V
0 0 0 0 0 1 0 0 0	1.3000 V	0 0 1 0 0 0 0 0 0	0.8000 V	1 0 0 0 0 0 0 0	0.2875 V
0 0 0 0 0 1 0 0 0	1.2875 V	0 0 1 0 0 0 0 0 0	0.7875 V	1 0 0 0 0 0 0 0	0.2750 V
0 0 0 0 0 1 0 0 0	1.2750 V	0 0 1 0 0 0 0 0 0	0.7750 V	1 0 0 0 0 0 0 0	0.2625 V
0 0 0 0 0 1 0 0 0	1.2625 V	0 0 1 0 0 0 0 0 0	0.7625 V	1 0 0 0 0 0 0 0	0.2500 V
0 0 0 0 0 1 0 0 0	1.2500 V	0 0 1 0 0 0 0 0 0	0.7500 V	1 0 0 0 0 0 0 0	0.2375 V
0 0 0 0 0 1 0 0 0	1.2375 V	0 0 1 0 0 0 0 0 0	0.7375 V	1 0 0 0 0 0 0 0	0.2250 V
0 0 0 0 0 1 0 0 0	1.2250 V	0 0 1 0 0 0 0 0 0	0.7250 V	1 0 0 0 0 0 0 0	0.2125 V
0 0 0 0 0 1 0 0 0	1.2125 V	0 0 1 0 0 0 0 0 0	0.7125 V	1 0 0 0 0 0 0 0	0.2000 V
0 0 0 0 0 1 0 0 0	1.2000 V	1 0 0 0 0 0 0 0 0	0.7000 V	1 0 0 0 0 0 0 0	0.1875 V
0 0 0 0 0 1 0 0 0	1.1875 V	1 0 0 0 0 0 0 0 0	0.6875 V	1 0 0 0 0 0 0 0	0.1750 V
0 0 0 0 0 1 0 0 0	1.1750 V	1 0 0 0 0 0 0 0 0	0.6750 V	1 0 0 0 0 0 0 0	0.1625 V
0 0 0 0 0 1 0 0 0	1.1625 V	1 0 0 0 0 0 0 0 0	0.6625 V	1 0 0 0 0 0 0 0	0.1500 V
0 0 0 0 0 1 0 0 0	1.1500 V	1 0 0 0 0 0 0 0 0	0.6500 V	1 0 0 0 0 0 0 0	0.1375 V
0 0 0 0 0 1 0 0 0	1.1375 V	1 0 0 0 0 0 0 0 0	0.6375 V	1 0 0 0 0 0 0 0	0.1250 V
0 0 0 0 0 1 1 0 0	1.1250 V	1 0 0 0 0 0 0 0 0	0.6250 V	1 0 0 0 0 0 0 0	0.1125 V
0 0 0 0 0 1 1 0 0	1.1125 V	1 0 0 0 0 0 0 0 0	0.6125 V	1 0 0 0 0 0 0 0	0.1000 V
0 0 0 0 0 1 1 0 0	1.1000 V	1 0 0 0 0 0 0 0 0	0.6000 V	1 0 0 0 0 0 0 0	0.0875 V
0 0 0 0 0 1 0 0 0	1.0875 V	1 0 0 0 0 0 0 0 0	0.5875 V	1 0 0 0 0 0 0 0	0.0750 V
0 0 0 0 0 1 0 0 0	1.0750 V	1 0 0 0 0 0 0 0 0	0.5750 V	1 0 0 0 0 0 0 0	0.0625 V
0 0 0 0 0 0 1 0 0	1.0625 V	1 0 0 0 0 0 0 0 0	0.5625 V	1 0 0 0 0 0 0 0	0.0500 V
0 0 0 0 0 0 1 0 0	1.0500 V	1 0 0 0 0 0 0 0 0	0.5500 V	1 0 0 0 0 0 0 0	0.0375 V
0 0 0 0 0 0 1 0 0	1.0375 V	1 0 0 0 0 0 0 0 0	0.5375 V	1 0 0 0 0 0 0 0	0.0250 V
0 0 0 0 0 0 1 0 0	1.0250 V	1 0 0 0 0 0 0 0 0	0.5250 V	1 0 0 0 0 0 0 0	0.0125 V
0 0 0 0 0 0 1 0 0	1.0125 V	1 0 0 0 0 0 0 0 0	0.5125 V	1 0 0 0 0 0 0 0	0.0000 V
		1 0 0 0 0 0 0 0 0	0.5000 V	1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V
				1 0 0 0 0 0 0 0	0.0000 V

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0, 1	SYSTEM PORT A
2, 3	SYSTEM PORT B
4	BLUETOOTH
5	DMB

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

DATE	1/11/2007	FIRENZE2-R MAIN BOARD INFORMATION	SAMSUNG ELECTRONICS	
TERM1 KWON				
CHECK	HJ KIM		MP	PART NO. BA41-00714A
DEVELOP				
APPROVAL	SJ PARK	REV	1.0	
MODULE CODE		LAST EDIT	January 11, 2007 8:27:44 PM	PAGE 6 OF 52

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DRAW	TERMI KWON	DATE	1/11/2007	TITLE	FIRENZE2-R	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	7 OF 52	

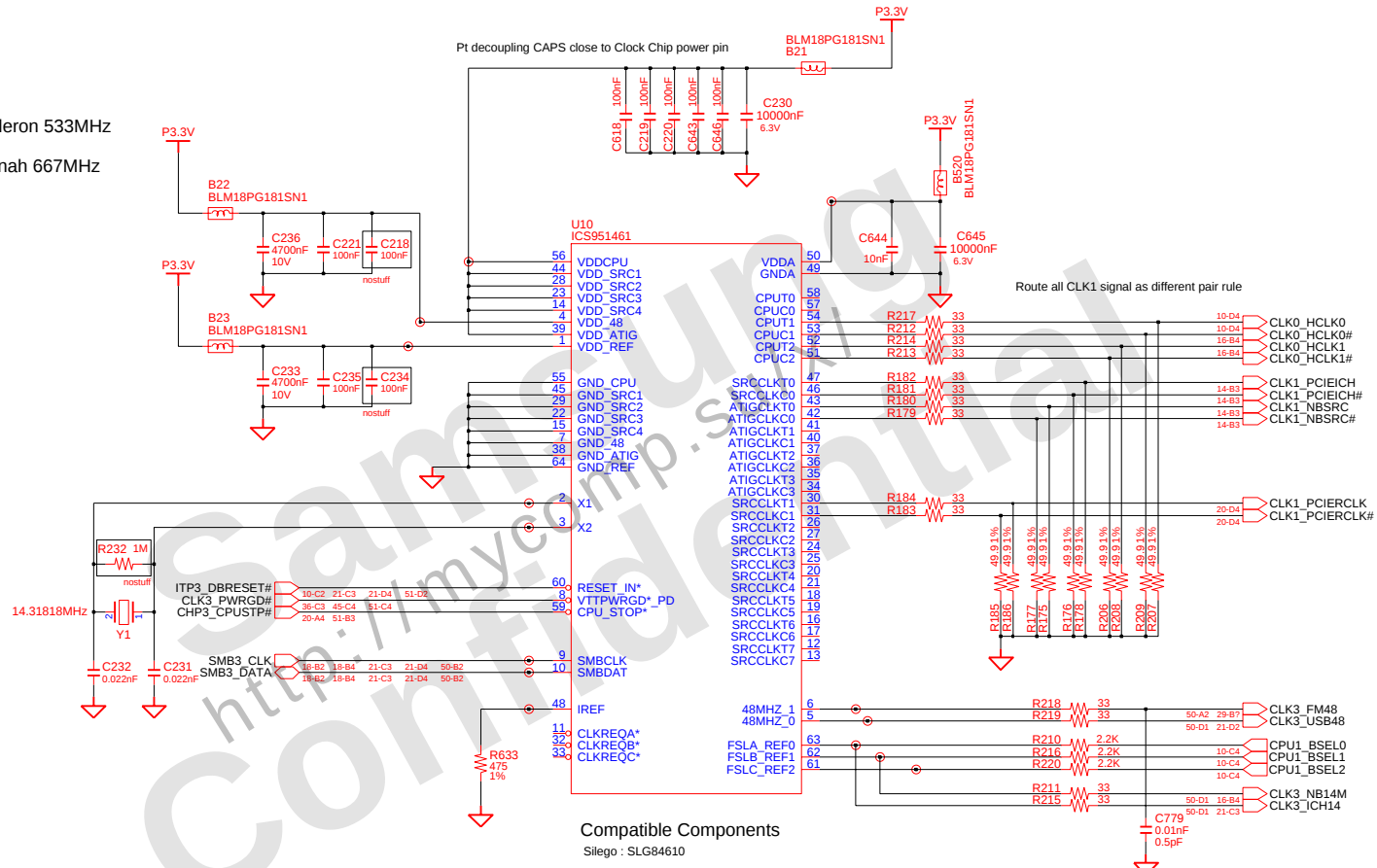
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 EXCEPT AS AUTHORIZED BY SAMSUNG.

CPU	FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
	0	0	0	266 MHz
	0	0	1	333 MHz
	0	1	0	200 MHz
	0	1	1	400 MHz
	1	0	0	133 MHz
	1	0	1	100 MHz
	1	1	0	166 MHz
	1	1	1	RSVD

Celeron 533MHz

Yonah 667MHz



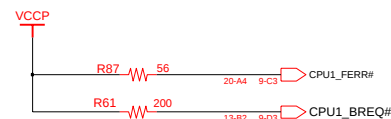
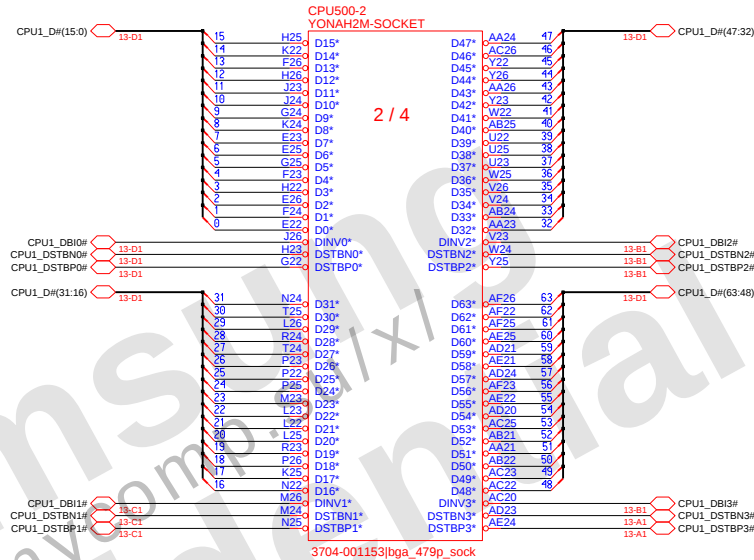
Compatible Components

Silego : SLG84610

Place all the series termination resistor as close as Clock Chip as possible

FSA, FSB, FSC of Clock chip are low threshold inputs
 $V_{ih_fs_min} = 0.7V$
 $V_{il_fs_max} = 0.35V$

DRAW	TERMI KWON	DATE	1/11/2007	TITLE	FIRENZE2-R MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			PART NO. BA41-00714A
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	8 OF 52	



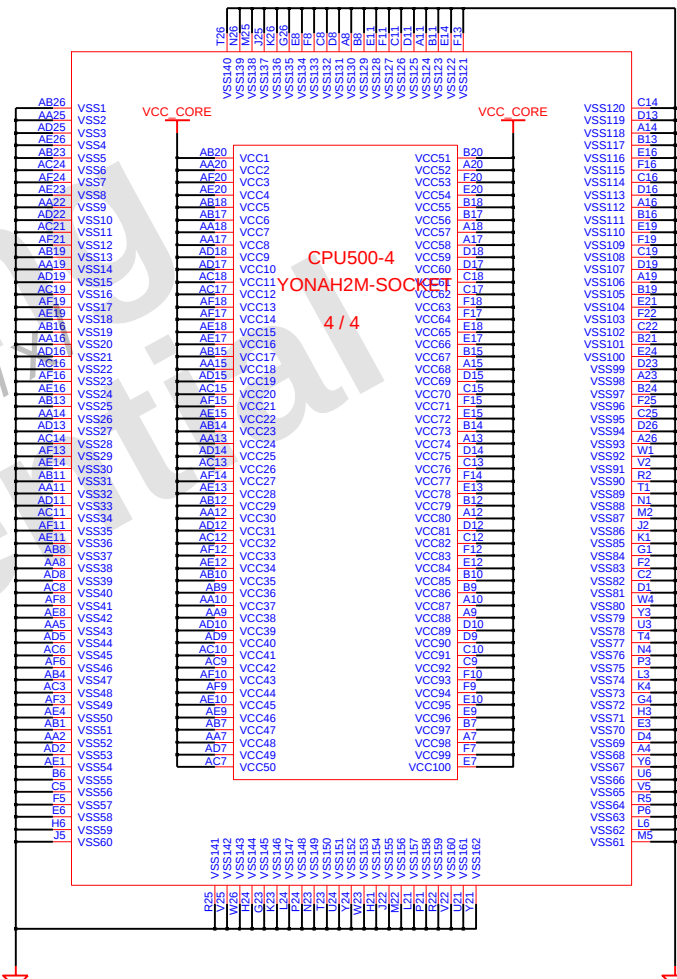
DRAM	TERMI KWON	DATE	1/11/2007	TITLE	FIRENZE2-R MAIN YONAH CPU (1/3)	SAMSUNG ELECTRONICS		
CHECK	HJ KIM	DEV. STEP	MP					
APPROVAL	SJ PARK	REV	1.0				PART NO.	BA41-00714A
MODULE CODE	LAST EDIT		January 11, 2007 8:27:44 PM				PAGE 9 OF 52	



Active Mode										Active/Deeper Sleep Dual Mode Region										Deeper Sleep/Extended Deeper Sleep Dual Mode Region																																							
VID(6:0)										Voltage										VID(6:0)										Voltage										VID(6:0)										Voltage									
0	0	0	0	0	0	0	0	0	0	15000 V	0	1	0	1	0	0	0	10000 V	1	0	1	0	0	0	1	0.8875 V	1	0	1	0	0	0	1	0.8875 V																									
0	0	0	0	0	0	0	0	1	1	14875 V	0	1	0	1	0	0	1	0.9875 V	1	0	1	0	0	1	0	0.7450 V	1	0	1	0	0	1	0.7450 V																										
0	0	0	0	0	0	1	0	1	0	14750 V	0	1	0	1	0	1	0	0.9750 V	1	0	1	0	0	1	1	0.4625 V	1	0	1	0	0	1	0.4625 V																										
0	0	0	0	0	0	1	1	1	1	14625 V	0	1	0	1	0	1	1	0.9625 V	1	0	1	0	1	0	1	0.4500 V	1	0	1	0	1	0	0.4500 V																										
0	0	0	0	0	1	0	0	1	0	14500 V	0	1	0	1	0	1	0	0.9500 V	1	0	1	0	1	0	1	0.4375 V	1	0	1	0	1	0	0.4375 V																										
0	0	0	0	1	1	1	0	1	0	14375 V	0	1	0	1	1	0	1	0.9375 V	1	0	1	0	1	1	0	0.4250 V	1	0	1	0	1	1	0.4250 V																										
0	0	0	0	1	1	0	1	0	1	14250 V	0	1	0	1	1	1	0	0.9250 V	1	0	1	0	1	1	1	0.4125 V	1	0	1	0	1	1	0.4125 V																										
0	0	0	0	1	1	1	1	1	1	14125 V	0	1	0	1	1	1	1	0.9125 V	1	0	1	1	0	0	0	0.4000 V	1	0	1	1	0	0	0.4000 V																										
0	0	0	1	1	0	0	0	1	0	14000 V	0	1	1	0	0	0	0	0.9000 V	1	0	1	1	0	0	1	0.3875 V	1	0	1	1	0	0	0.3875 V																										
0	0	1	0	0	0	1	0	1	0	13875 V	0	1	1	0	0	1	0	0.8875 V	1	0	1	1	0	0	1	0.3750 V	1	0	1	1	0	0	0.3750 V																										
0	0	0	0	1	0	1	0	1	0	13750 V	0	1	1	0	0	1	0	0.8750 V	1	0	1	1	0	1	1	0.3625 V	1	0	1	1	0	1	0.3625 V																										
0	0	0	0	1	0	1	1	1	1	13625 V	0	1	1	0	0	1	1	0.8625 V	1	0	1	1	1	0	0	0.3500 V	1	0	1	1	1	0	0.3500 V																										
0	0	0	1	1	1	0	0	1	0	13500 V	0	1	1	0	1	0	0	0.8500 V	1	0	1	1	1	1	0	0.3375 V	1	0	1	1	1	0	0.3375 V																										
0	0	0	1	1	0	1	0	1	0	13375 V	0	1	1	0	1	0	1	0.8375 V	1	0	1	1	1	0	1	0.3250 V	1	0	1	1	1	0	0.3250 V																										
0	0	0	1	1	1	1	0	1	0	13250 V	0	1	1	0	1	1	0	0.8250 V	1	0	1	1	1	1	1	0.3125 V	1	0	1	1	1	1	0.3125 V																										
0	0	0	1	1	1	1	1	1	1	13125 V	0	1	1	0	1	1	1	0.8125 V	1	0	1	1	0	0	0	0.3000 V	1	0	1	1	0	0	0.3000 V																										
0	0	1	0	0	0	0	0	0	0	13000 V	0	1	1	1	0	0	0	0.8000 V	1	0	1	0	0	0	1	0.2875 V	1	0	1	0	0	0	0.2875 V																										
0	0	1	0	0	0	1	0	1	0	12875 V	0	1	1	1	0	0	1	0.7875 V	1	0	1	0	0	1	0	0.2750 V	1	0	1	0	0	0	0.2750 V																										
0	0	1	0	0	1	0	1	0	1	12750 V	0	1	1	1	0	0	0	0.7750 V	1	0	1	0	1	0	1	0.2625 V	1	0	1	0	1	0	0.2625 V																										
0	0	1	0	0	1	1	0	1	0	12625 V	0	1	1	1	0	1	0	0.7625 V	1	0	1	0	1	0	0	0.2500 V	1	0	1	0	1	0	0.2500 V																										
0	0	1	0	1	0	0	0	0	0	12500 V	0	1	1	1	1	0	0	0.7500 V	1	0	1	0	1	0	1	0.2375 V	1	0	1	0	1	0	0.2375 V																										
0	0	1	0	1	0	1	0	1	0	12375 V	0	1	1	1	1	0	1	0.7375 V	1	0	1	0	1	1	0	0.2250 V	1	0	1	0	1	1	0.2250 V																										
0	0	1	0	1	0	1	1	0	1	12250 V	0	1	1	1	1	1	0	0.7250 V	1	0	1	0	1	1	1	0.2125 V	1	0	1	0	1	1	0.2125 V																										
0	0	1	1	0	1	1	1	1	1	12125 V	0	1	1	1	1	1	1	0.7125 V	1	0	1	0	1	1	0	0.2000 V	1	0	1	0	1	0	0.2000 V																										
0	0	1	1	0	0	0	0	0	0	12000 V	0	1	0	0	0	0	0	0.7000 V	1	0	1	0	0	0	0	0.1875 V	1	0	1	0	0	0	0.1875 V																										
0	0	1	1	0	0	1	0	1	0	11875 V	1	0	0	0	0	0	1	0.6875 V	1	0	1	0	1	0	0	0.1750 V	1	0	1	0	1	0	0.1750 V																										
0	0	1	1	0	1	0	1	0	1	11750 V	1	0	0	0	0	1	0	0.6750 V	1	0	1	0	1	0	1	0.1625 V	1	0	1	0	1	0	0.1625 V																										
0	0	1	1	0	1	1	0	1	0	11625 V	1	0	0	0	1	0	1	0.6625 V	1	0	1	0	1	0	1	0.1500 V	1	0	1	0	1	0	0.1500 V																										
0	0	1	1	1	0	0	0	0	0	11500 V	1	0	0	0	1	0	0	0.6500 V	1	0	1	0	1	0	1	0.1375 V	1	0	1	0	1	0	0.1375 V																										
0	0	1	1	1	0	1	0	1	0	11375 V	1	0	0	0	1	0	1	0.6375 V	1	0	1	0	1	1	0	0.1250 V	1	0	1	0	1	1	0.1250 V																										
0	0	1	1	1	1	0	0	0	0	11250 V	1	0	0	0	1	1	0	0.6250 V	1	0	1	0	1	1	1	0.1125 V	1	0	1	0	1	1	0.1125 V																										
0	0	1	1	1	1	1	1	1	1	11125 V	1	0	0	0	1	1	1	0.6125 V	1	0	1	0	0	0	0	0.1000 V	1	0	1	0	0	0	0.1000 V																										
0	1	0	0	0	0	0	0	0	0	11000 V	1	0	0	1	0	0	0	0.6000 V	1	0	1	0	0	0	1	0.0875 V	1	0	1	0	0	0	0.0875 V																										
0	1	0	0	0	0	1	0	1	0	10875 V	1	0	0	1	0	0	1	0.5875 V	1	0	1	0	0	1	0	0.0750 V	1	0	1	0	0	0	0.0750 V																										
0	1	0	0	0	1	0	1	0	1	10750 V	1	0	0	1	0	1	0	0.5750 V	1	0	1	0	0	1	0	0.0625 V	1	0	1	0	0	1	0.0625 V																										
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0	1	0	1	0	0	1	0	0	0	10375 V	1	0	0	1	1	0	1	0.5375 V	1	0	1	1	0	0	0	0.0250 V	1	0	1	1	0	0	0.0250 V																										
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0	1	0	0	0	1	1	1	1	1	10125 V	1	0	0	1	1	1	1	0.5125 V	1	0	1	1	1	0	0	0.0000 V	1	0	1	1	1	0	0.0000 V																										
											1	0	1	0	0	0	0	0.5000 V	1	0	1	0	0	0	0	0.0000 V	1	0	1	0	0	0	0.0000 V																										
																			1	1	1	0	0	0	0	0.0000 V	1	1	1	0	0	0	0.0000 V																										
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																			1	1	1	1	1	1	1	0.0000 V	1	1	1	1	1	1	0.0000 V																										
																			1	1	1	1	1	1	1	0.0000 V	1	1	1	1	1	1	0.0000 V																										
																			1	1	1	1	1	1	1	0.0000 V	1	1	1	1	1	1	0.0000 V																										
																			1	1	1	1	1	1	1	0.0000 V	1	1	1	1	1	1	0.0000 V																										
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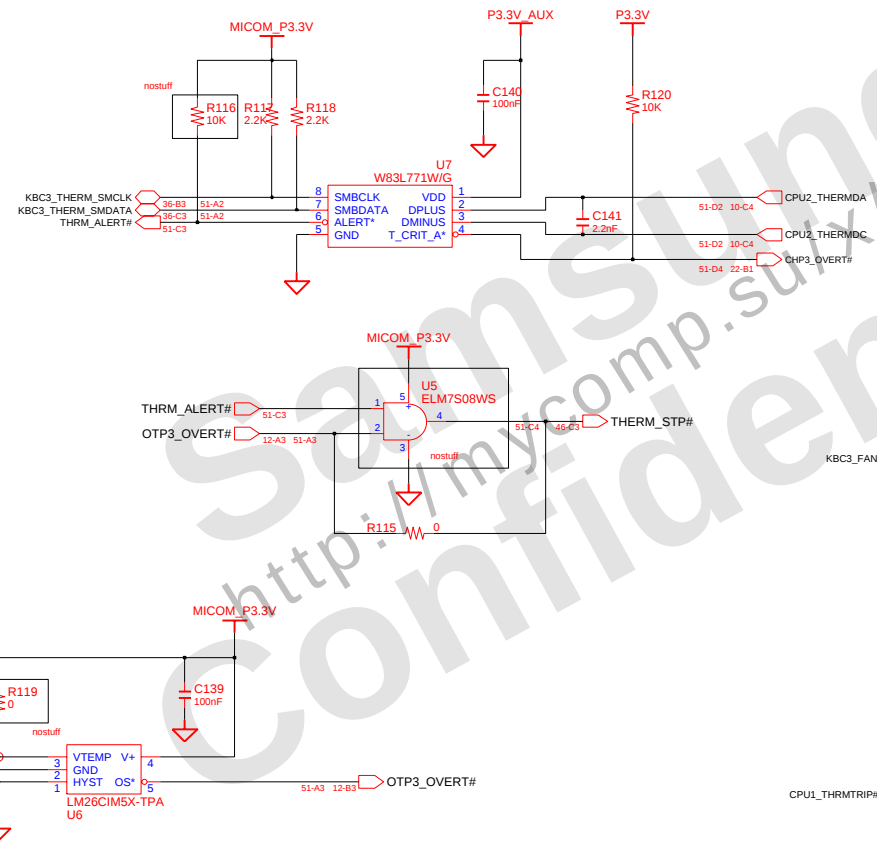
*Yonah Processor (2.33 GHz / 800 MHz : TBD)

ORAW	TERMI KWON	DATE	1/11/2007	TITLE	FIRENZE2-R	
CHECK	HJ KIM	DEV. STEP	MP	MAIN		
APPROVAL	SJ PARK	REV	1.0	YONAH CPU(2/3)	PART NO.	
MODULE CODE		LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	10 OF 52	

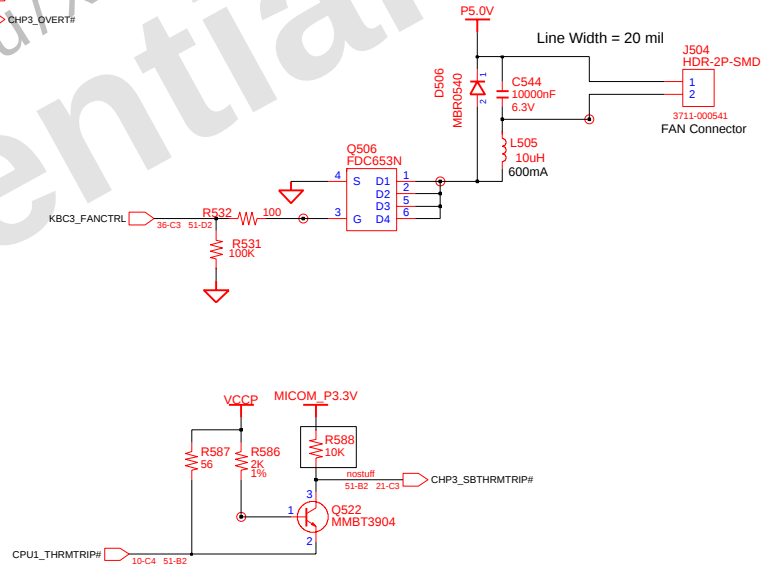


d:/users/mobile62/mentor/finenze2_r/F2-R-SR_01

CPU Thermal Sensor



FAN Control Logic



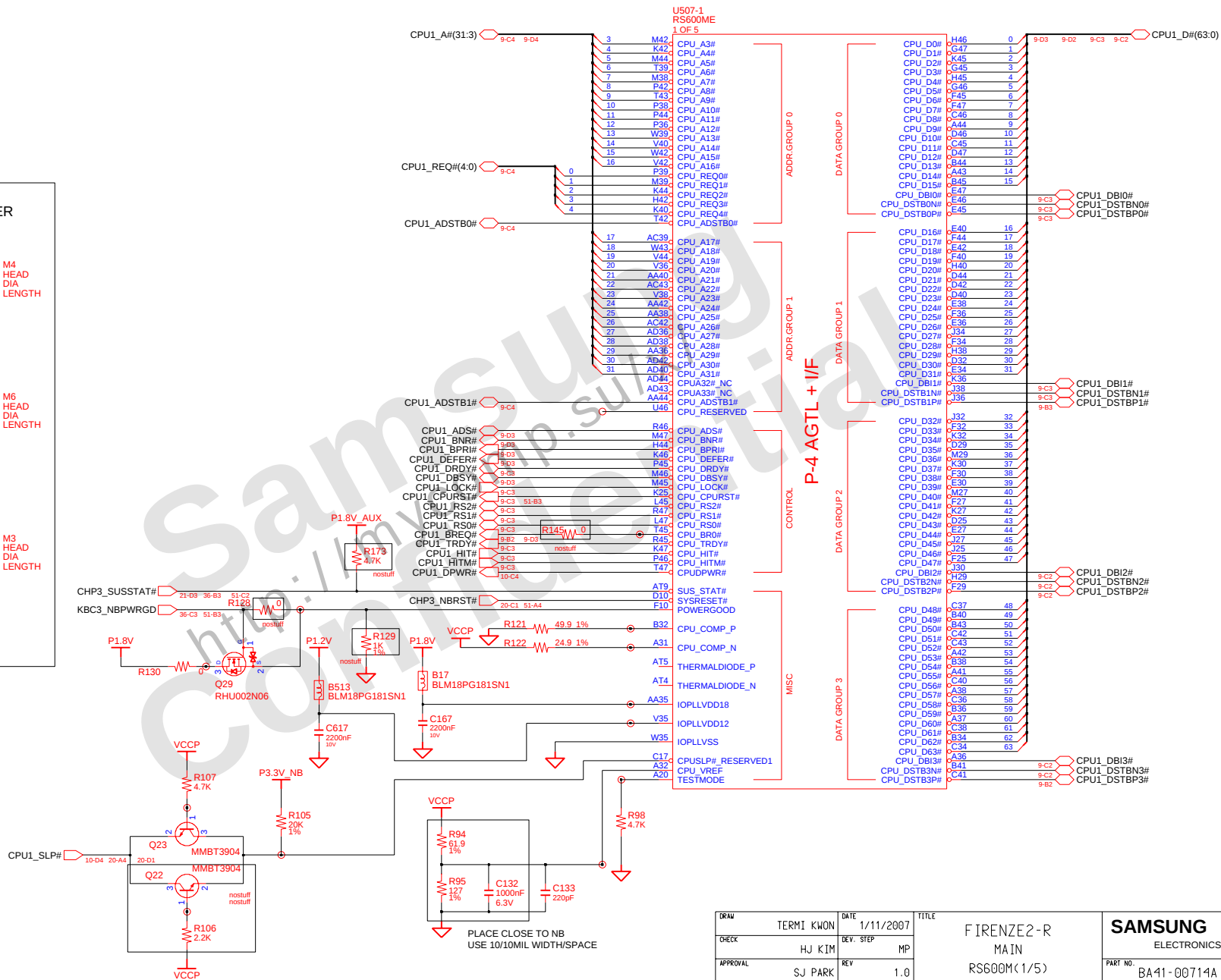
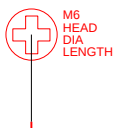
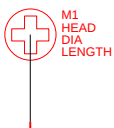
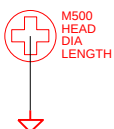
- Refer To Thermal Sensor Layout Guidelines.
- Place the Thermal Sensor close to a remote diode.
 - Keep traces away from high voltage (+12V bus)
 - Keep traces away from fast data buses and CRT signal.
 - Use recommended trace widths and spacings (10mil)
 - Place a ground plane under the traces.
 - Use guard traces flanking DXP and DXN and connecting to GND

DRAW	TERMI KWON	DATE	1/11/2007	TITLE	FIRENZE2-R MAIN	SAMSUNG ELECTRONICS PART NO. BA41-00714A
CHECK	HJ KIM	DEV. STEP	MP	REV	1.0	
APPROVAL	SJ PARK	LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	12 OF 52	

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DUCT + FAN SUPPORTER



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MEM1_ADQ(63:0) 18-04

MEM1_AMA(14:0) 18-04 19-C4

MEM1_ABS0 18-C4 19-C4
MEM1_ABS1 18-C4 19-C4
MEM1_ABS2 18-C4 19-C4
MEM1_ADM(7:0) 18-B4

MEM1_ADQS(7:0) 18-B4

MEM1_ADQS#(7:0) 18-A4

CLK1_AMCLK1# 18-C4
CLK1_AMCLK1 18-C4
CLK1_AMCLK2# 18-C4
CLK1_AMCLK2 18-C4MEM1_ACKE0 18-C4 19-D4
MEM1_ACKE1 18-C4 19-D4MEM1_ACS0# 18-C4 19-D4
MEM1_ACS1# 18-C4 19-D4MEM1_AODT0 18-B4 19-D4
MEM1_AODT1 18-B4 19-D4MEM1_AWE# 18-B4 19-C4
MEM1_ACAS# 18-C4 19-C4
MEM1_ARAS# 18-B4 19-C4MEM1_REF
R203 0
nostuff

MEM1_BDQ(63:0) 18-02

A CHANNEL

U507-3
3 OF 5
RS600ME

B CHANNEL

P1.8V_AUX

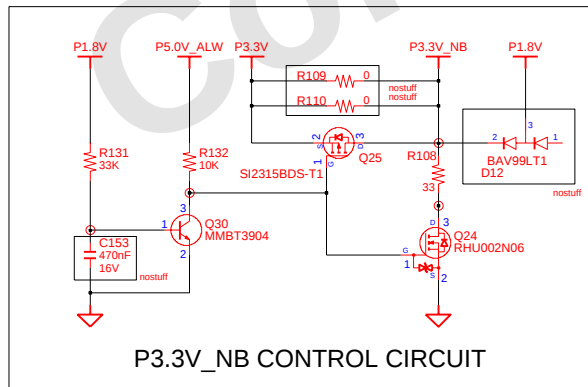
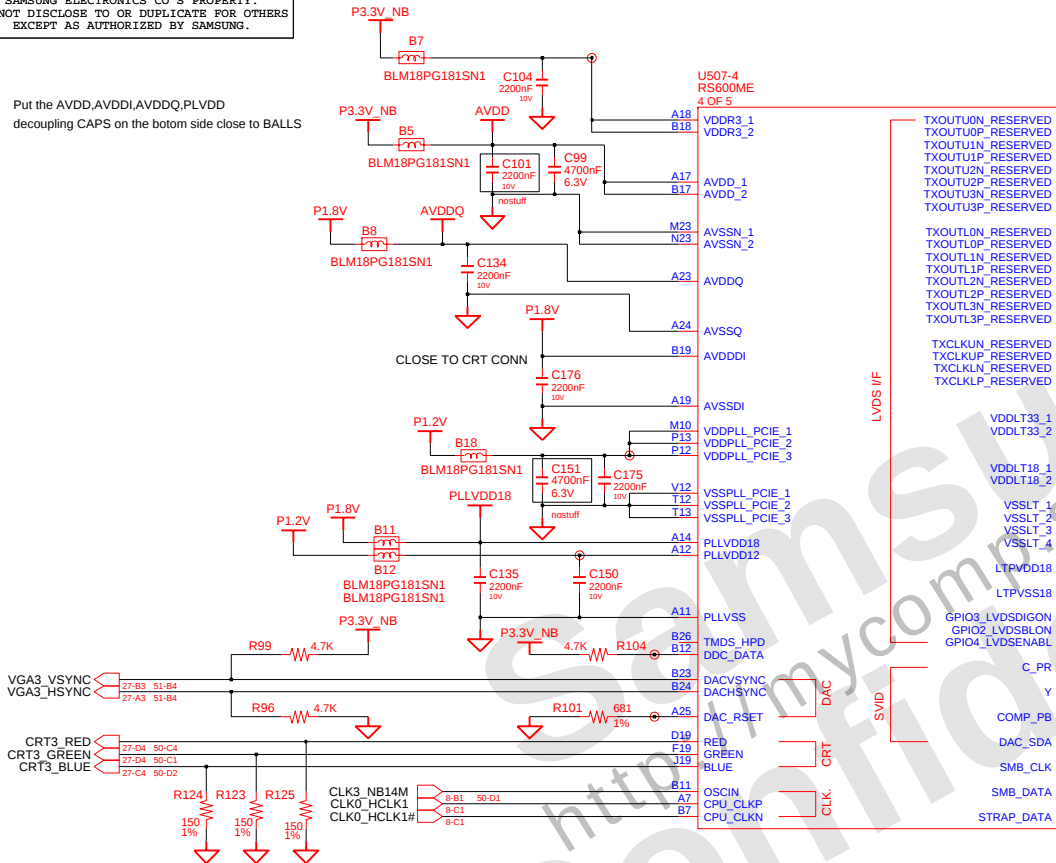
R172 40.2 1%

R171 40.2 1%

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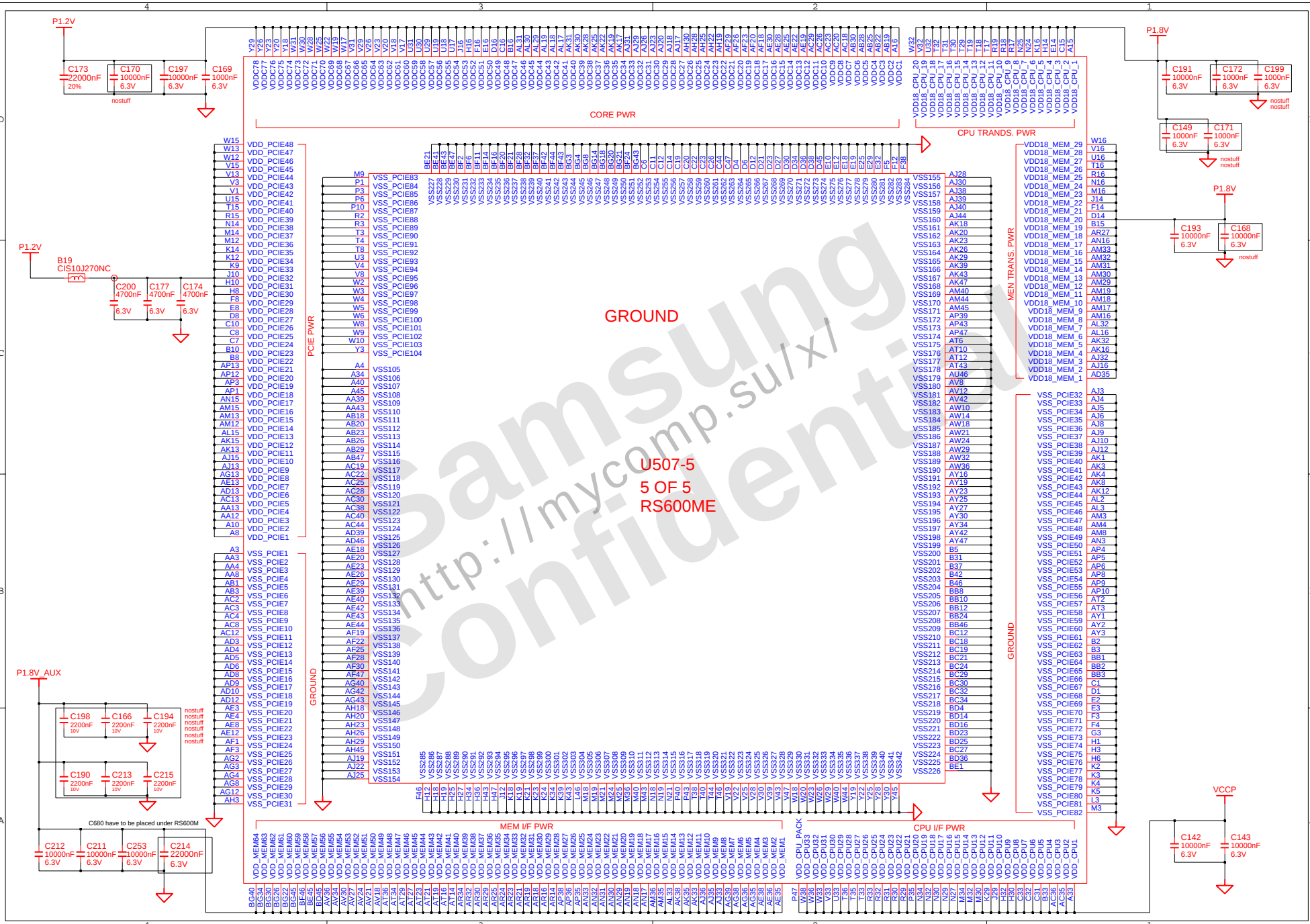
VGA3_VSYNC  27-B3 51-B4
VGA3_HSYNC  27-A3 51-B4

CRT3_RED  27-D4 50-C4
CRT3_GREEN  27-D4 50-C1
CRT3_BLUE  27-C4 50-D2



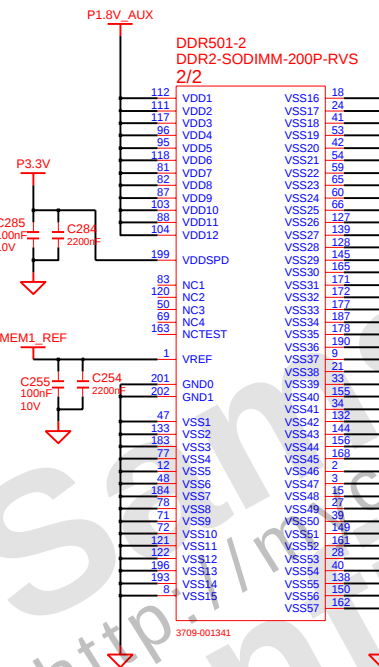
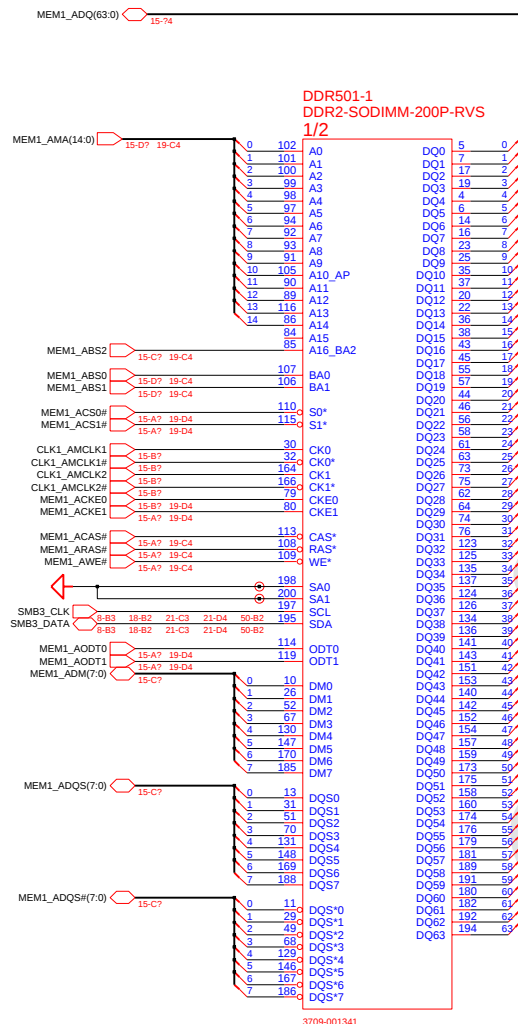
STRAP PIN	DESCRIPTION
DACHSYNC	Enable/Disable integrated graphics. 0 : Enable integrated graphics 1 : Disable integrated graphics
STRP_DATA	Debug strap configuration. This strap should not be set to "0" on production boards. 0 : Select Memory Channel A to be a debug bus 1 : Read debug straps from an external EEPROM, or disable debug mode when an EEPROM is absent.
DACVSYNC	Select configuration of the integrated graphics engine. 0 : Reserved 1 : Required setting for the RS600M
DDC_DATA	Select DDR2 or DDR3 signalling level for the memory interface. 0 : DDR3. On DDR3, it is necessary to put an isolation FET in series with the pull-up resistor on this strap to separate it from the I2C circuit during an NB reset 1 : DDR2

DRAW	TERMI KWON	DATE	1/11/2007	TITLE		FIRENZE2-R MAIN RS600M(4/5)	
CHECK	HJ KIM	DEV. STEP	MP				
APPROVAL	SJ PARK	REV	1.0			PART NO.	BA41-00714A
MODULE CODE	LAST EDIT		January 11, 2007 8:27:44 PM		PAGE	16	OF 52

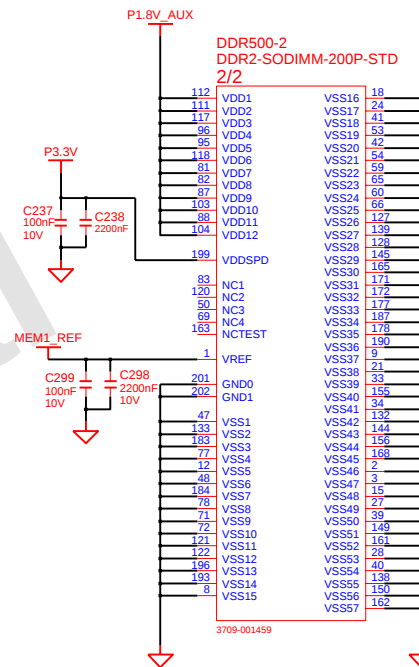
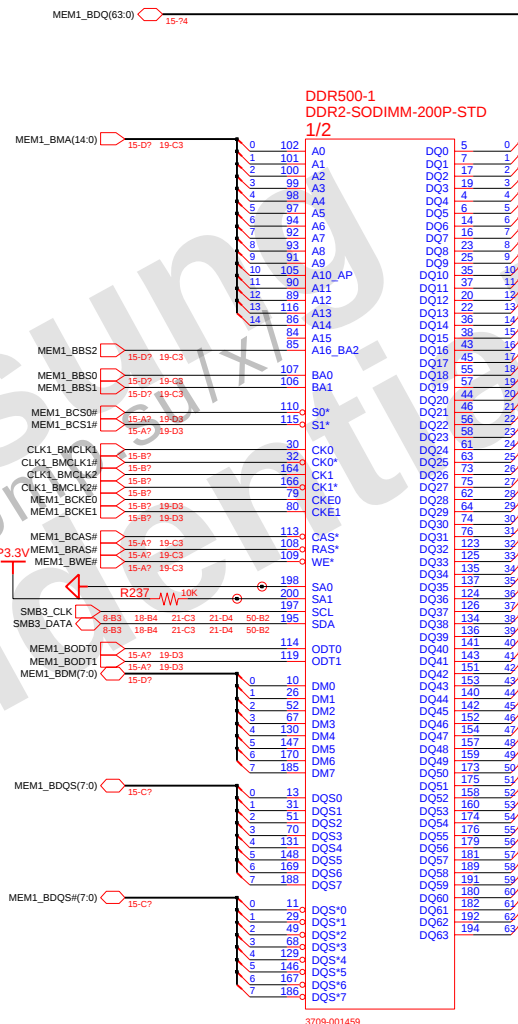


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J4 Height : 5.2mm

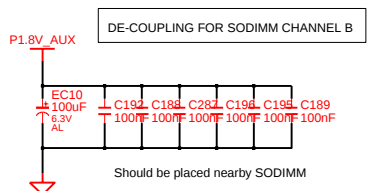
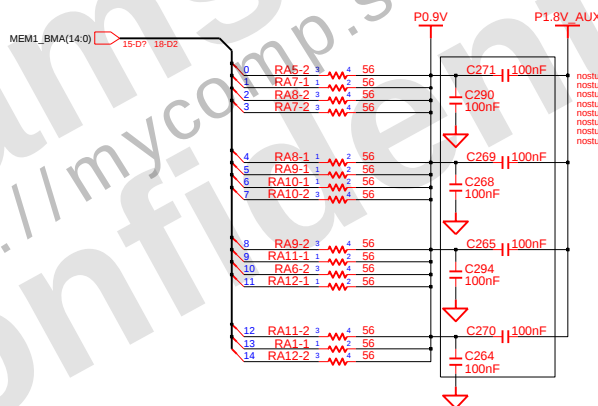
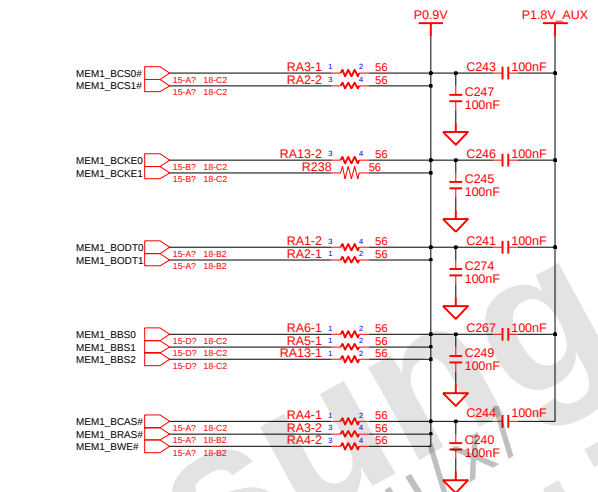
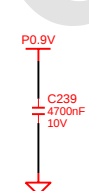
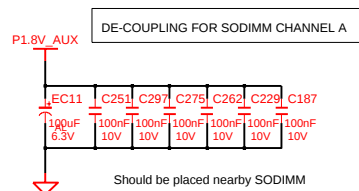
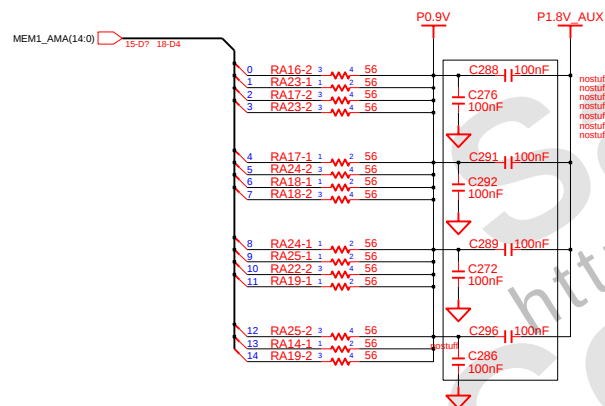
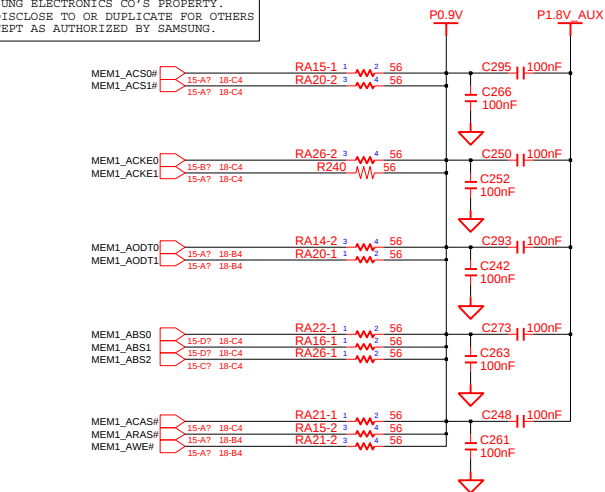


DDR1 Height : 9.2mm

DRAW	TERMI KWON	DATE	1/11/2007	TITLE	FIRENZE2-R MAIN	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		DDR2 - SODIMM	PART NO. BA41-00714A
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	18	OF 52

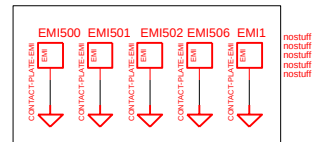
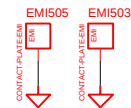
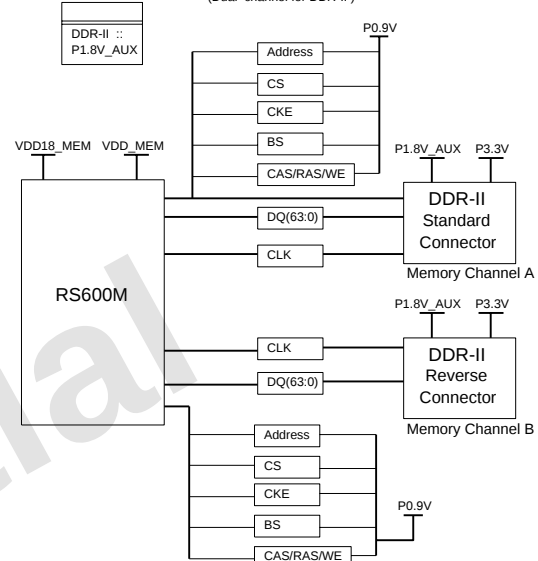
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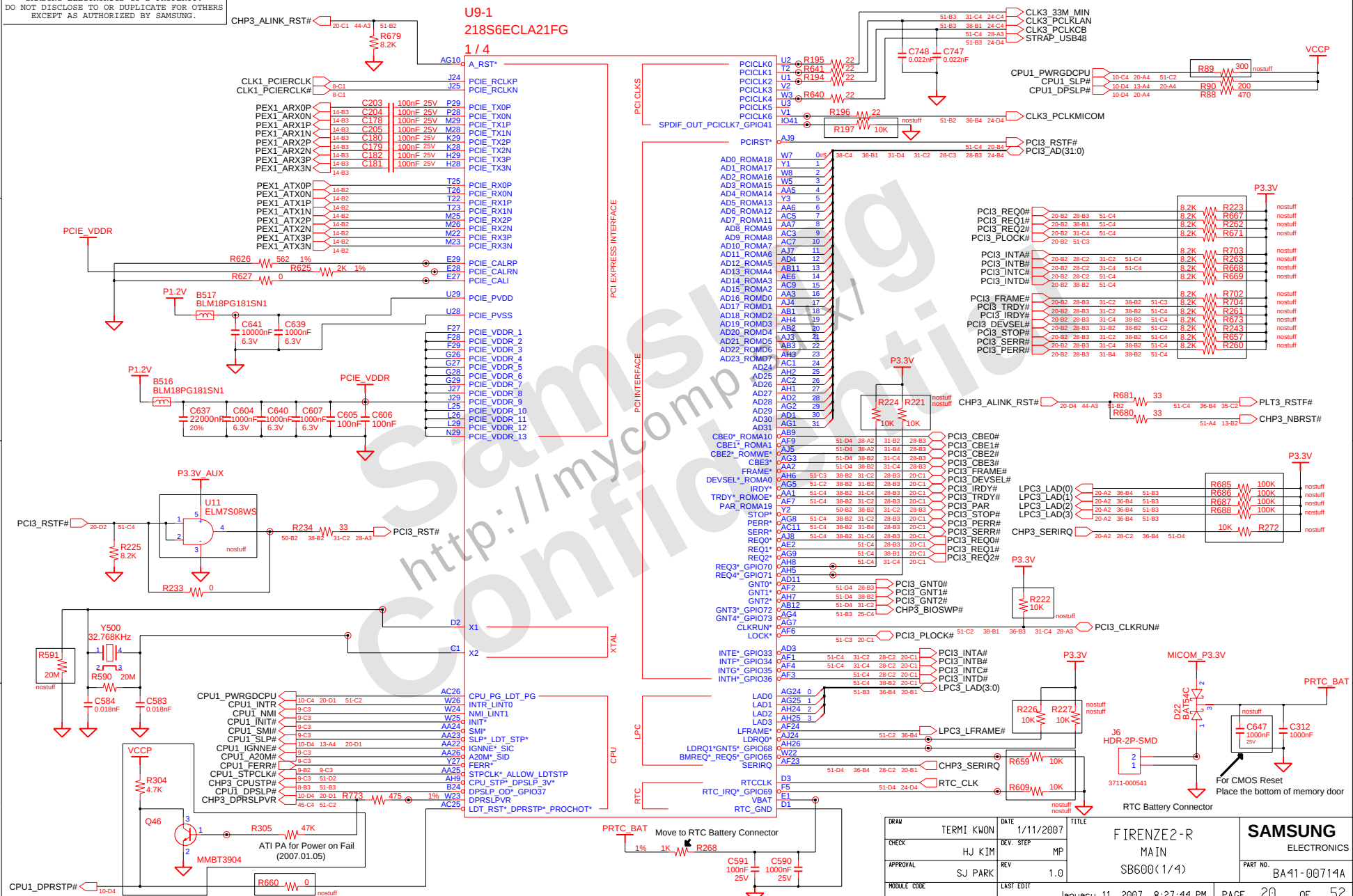


Memory Topology

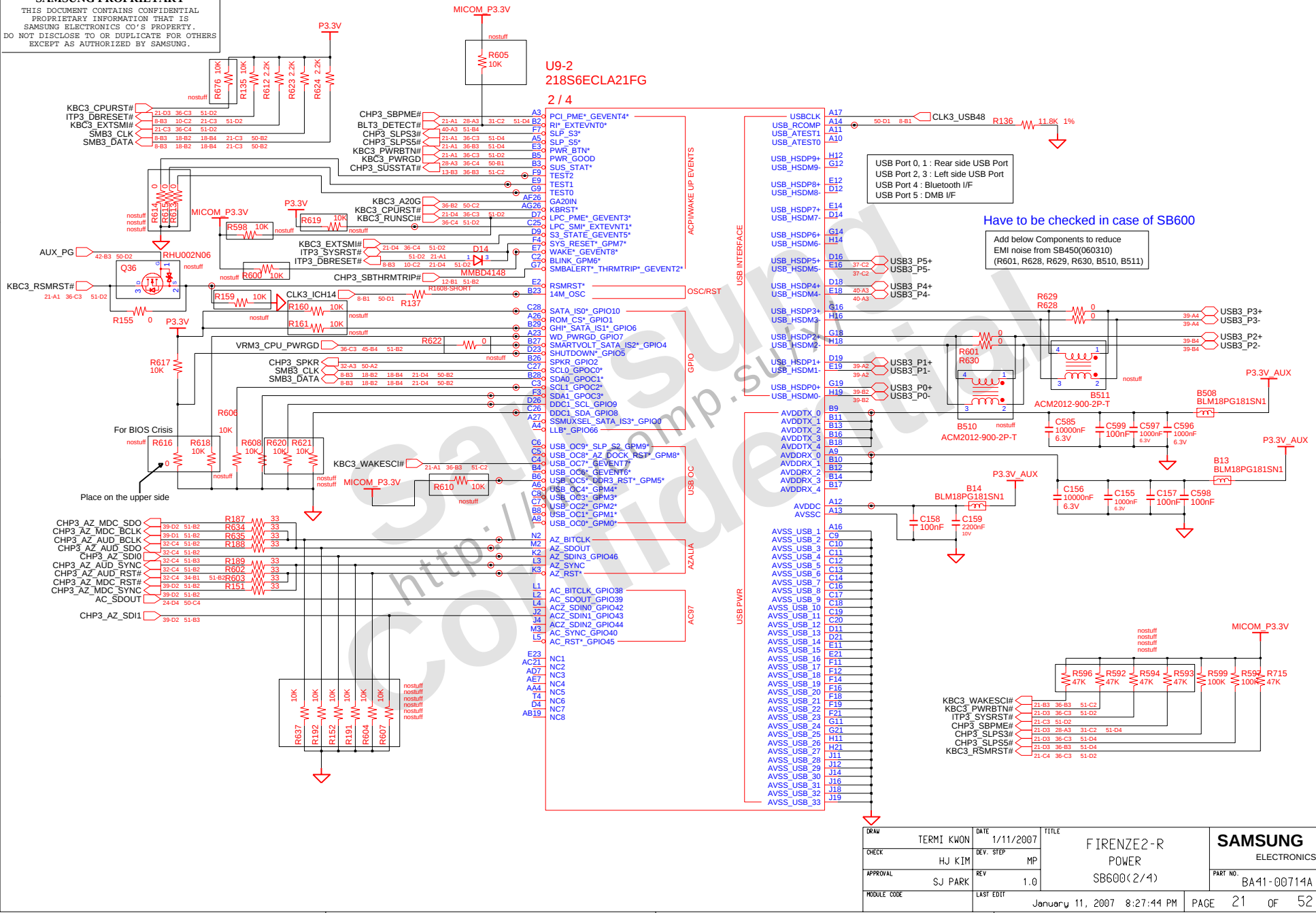
(Dual channel for DDR-II)



DRAW	TERMI KWON	DATE	1/11/2007	TITLE	FIRENZE2-R	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		MAIN	
APPROVAL	SJ PARK	REV	1.0		DDR2 - TERMINATION	PART NO.
MODULE CODE		LAST EDIT	January 11, 2007 8:27:44 PM			BA41-00714A
					PAGE	19 OF 52



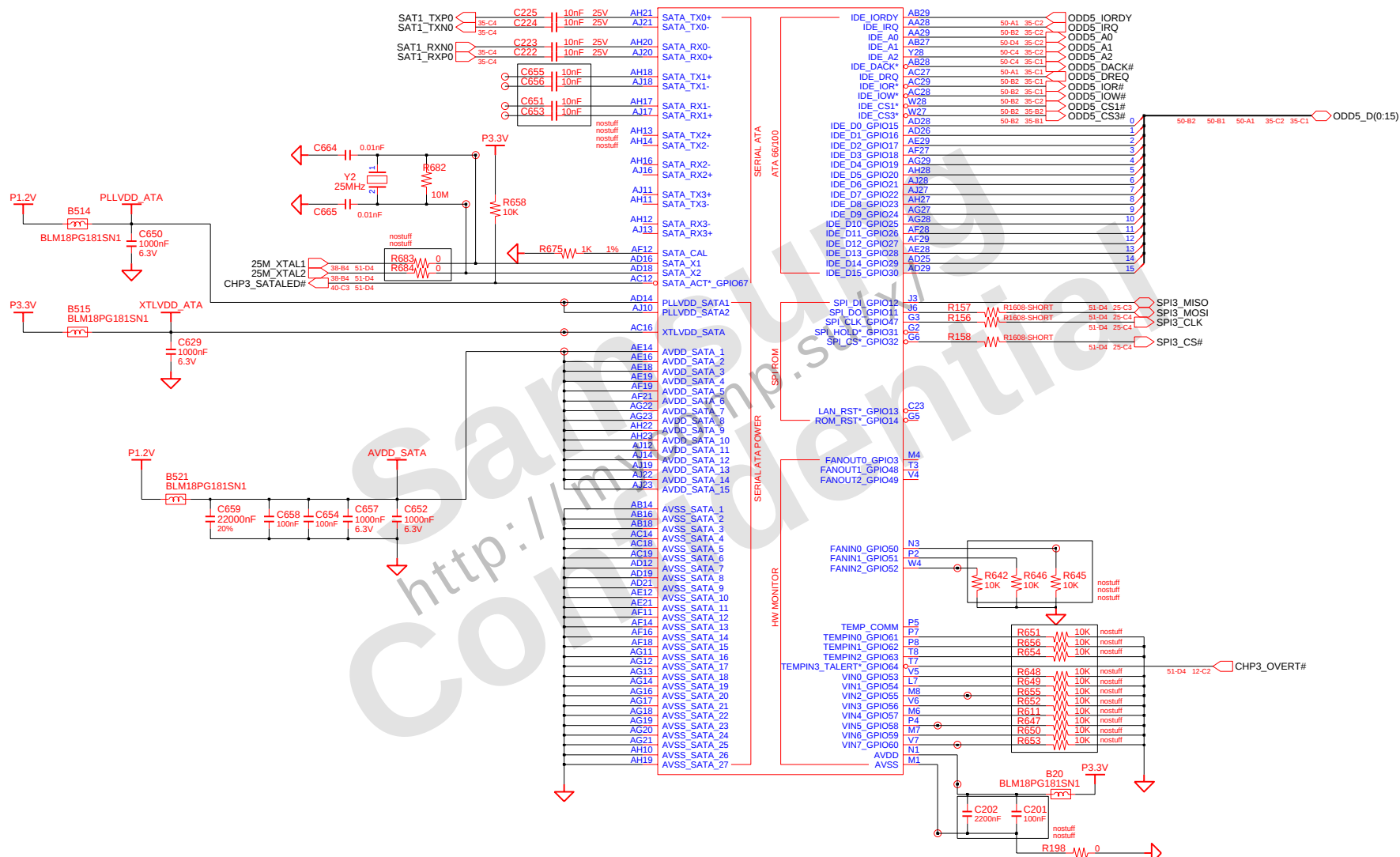
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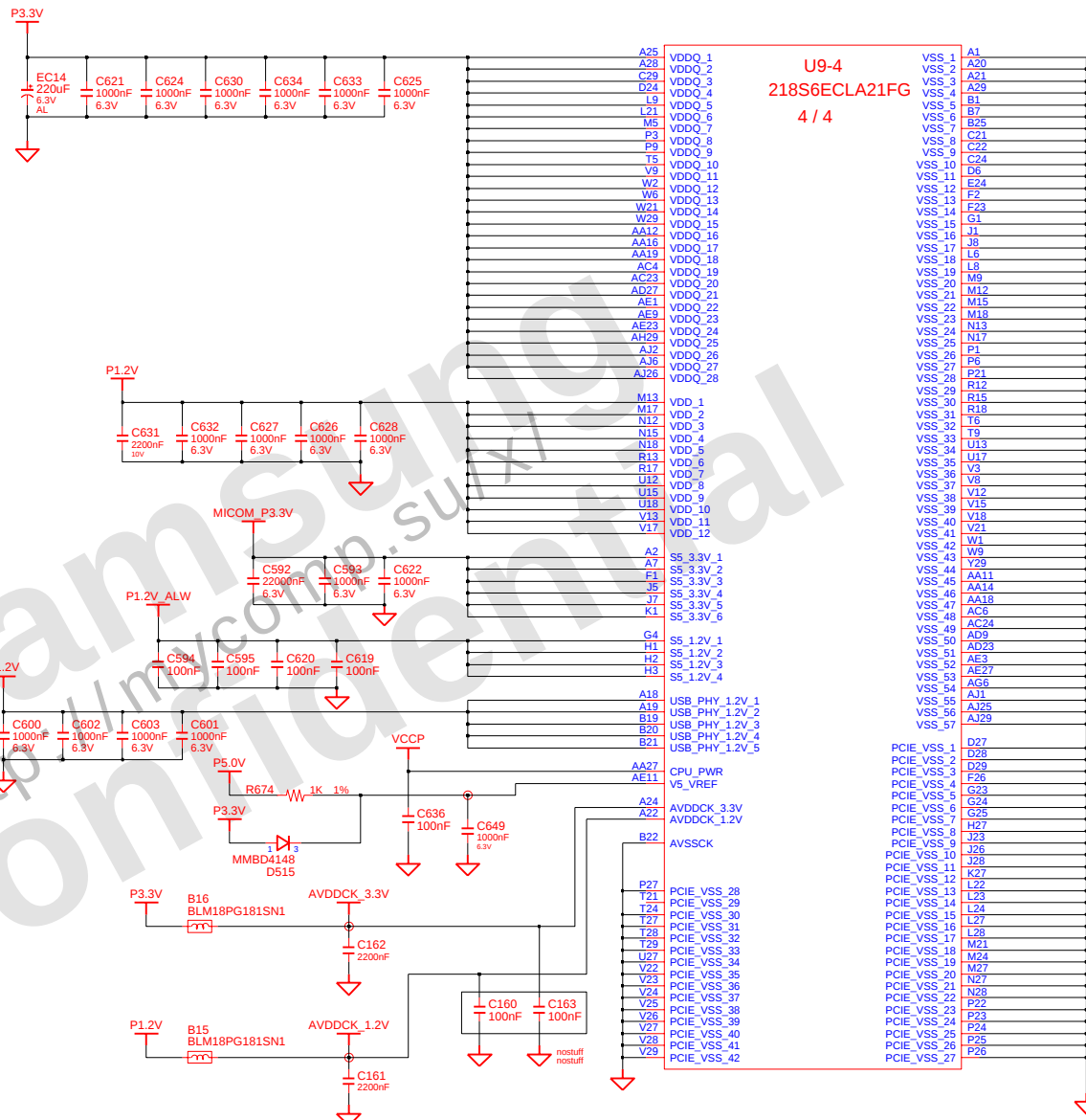
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U9-3
218S6ECLA21FG
3 / 4



DRAW	TERMI KWON	DATE	1/11/2007	TITLE	FIRENZE2-R MAIN SB600(3/4)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			PART NO. BA41-00714A
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	22 OF 52	

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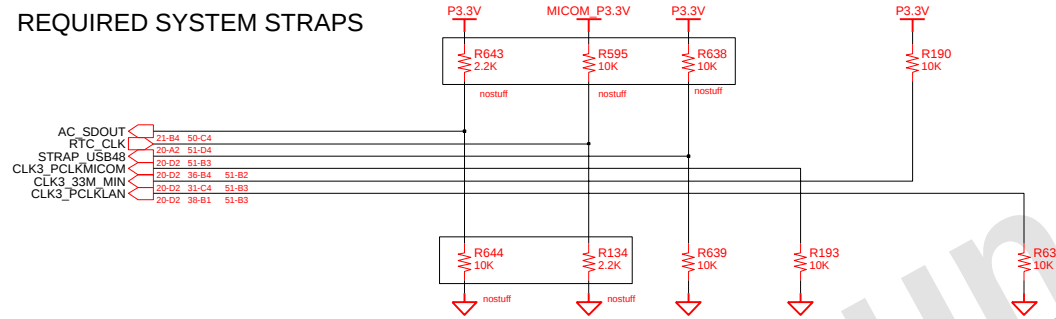


To Reduce EMI noise from SB450 (060310)

DATE	1/11/2007	TITLE	FIRENZE2-R MAIN SB600(4/4)	SAMSUNG ELECTRONICS
TERM1 KWON				
CHECK	DEV. STEP MP			
APPROVAL	REV 1.0			
SJ PARK		PART NO.	BA41-007114A	
MODULE CODE	LAST EDIT	January 11, 2007 8:27:44 PM		PAGE 23 OF 52

SB600 HAS AN INTERNAL PD FOR AC_SDOUT
SB600 HAS AN INTERNAL PU FOR RTC_CLK

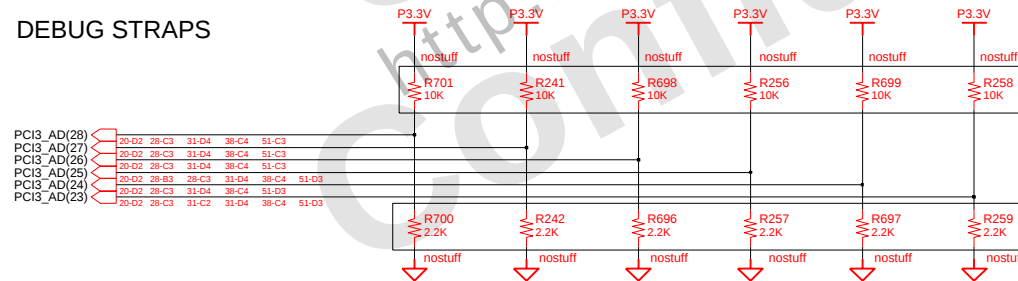
REQUIRED SYSTEM STRAPS



	AC_SDOUT	RTC_CLK	PCI3_CLK4	PCI3_CLK6	PCI3_CLK0	PCI3_CLK1
STRAP HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INTERNAL PLL48	CPU I/F = K8	ROM TYPE H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	
STRAP LOW	IGNORE DEBUG STRAPS	EXRERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK)	USE EXTERNAL 48MHz	CPU I/F = P4		

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

DEBUG STRAPS

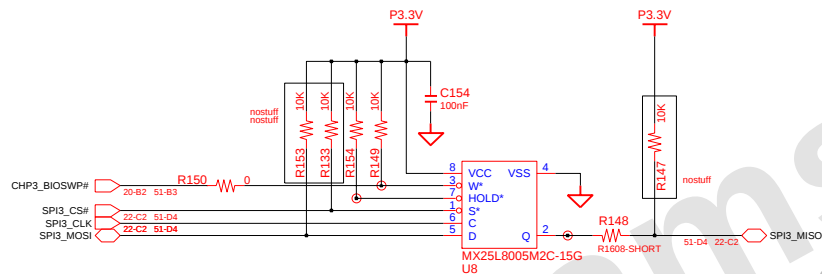


	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
STRAP LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

DRAW	TERMI KWON	DATE	1/11/2007	TITLE	FIRENZE2-R	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0		STRAPS	PART NO. BA41-00714A
MODULE CODE		LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	24	OF 52

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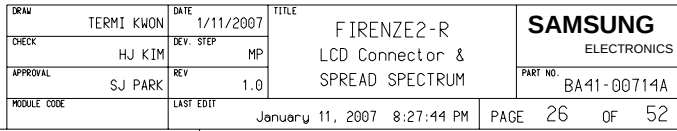
SPI3_CS#

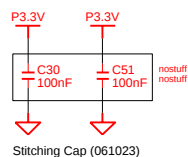
SB600 prior to A21 : Pulled up to P3.3V_ALW with 1Kohm resistor.
SB600 A21 and newer : No external pull-up resistor required.

- | | | | |
|----|---|----|---------------------------------|
| 02 | VERIFY REAL MODE | 66 | CONFIGURE ADVANCE CACHE REG. |
| 03 | DISABLE NMI | 6A | DISPLAY EXTERNAL CACHE SIZE |
| 04 | GET CPU TYPE | 6C | DISPLAY SHADOW MESSAGE |
| 06 | INIT. SYSTEM H/W | 6E | DISPLAY NON-DISPOSABLE SEGMENT |
| 08 | INIT. CHIPSET REG. | 70 | DISPLAY ERROR MESSAGE |
| 09 | SET IN POST FLAG | 72 | CHECK FOR CONFIGURATION ERROR |
| 0A | INIT CPU.REG | 74 | TEST REAL-TIME CLOCK |
| 0B | CPU CACHE ON | 76 | CHECK FOR KEYBOARD ERROR |
| 0C | INIT.CACHE TO POST | 7C | SETUP HARDWARE INTERRUPT VECTOR |
| 0E | INIT. I/O VALUE | 7E | TEST COPROCESSOR IF PRESENT |
| 0F | ENABLE THE L-BUS IDE | 80 | DISABLE ON-BOARD I/O PORT |
| 10 | INIT. POWER MANAGER | 82 | DETECT AND INSTALL EXT.RS232C |
| 11 | LOAD ALTERNATE REG. | 84 | DETECT AND INSTALL EXT.PARALLEL |
| 13 | PCI BUS MASTER RESET
WITH INITIAL POST VALUE | 86 | RE-INIT. ON-BOARD I/O PORT |
| 14 | INIT. KEYBOARD CONTROLLER | 88 | INIT. BIOS DATA ROM |
| 16 | CHECK CHECKSUM | 8A | INIT.EXTENDED BIOS DATA AREA |
| 18 | 8254 TIMER INIT. | 8C | INIT. FDD CONTROLLER |
| 1A | 8237 DMA CONTROLLER INIT. | 9A | SHADOW OPTION ROMS |
| 1C | RESET INTERRUPT CONTROLLER | 9C | SETUP POWER MANAGEMENT |
| 20 | TEST DRAM REFRESH | 9E | ENABLE H/W INTERRUPT |
| 22 | TEST 8742 KEYBOARD CONTROLLER | A0 | SET TIME OF DAY |
| 24 | SET ES SEGMENT REG. TO 4GB | A4 | INIT. TYPEMATIC RATE |
| 26 | ENABLE A20 | A8 | ERASE F2 PROMPT |
| 28 | AUTO SIZING DRAM | AA | SCAN FOR F2 KEY STROKE |
| 32 | COMPUTE THE CPU SPEED | AC | ENTER SETUP |
| 34 | TESET CMOS RAM | AE | CLEAR IN POST FLAG |
| 38 | SHADOW SYSTEM BIOS ROM | B0 | CHECK FOR ERRORS |
| 3A | AUTO SIZING CACHE | B2 | POST DONE-PREPARE TO BOOT O/S |
| 3C | CONFIGURE ADVANCED CHIPSET REG. | B4 | ONE BEEP |
| 3D | LOAD ALTER REG. WITH CMOS VALUE | B6 | CHECK PASSWORD (OPTION) |
| 42 | INIT. INTERRUPT VECTOR | B7 | ACPI INIT |
| 44 | INIT. BIOS INTERRUPT | BA | DMI INIT |
| 46 | CHECK ROM COPYRIGHT NOTICE | BE | CLEAR SCREEN |
| 47 | INIT. I20 SUPPORT IF INSTALLED | C0 | TRY BOOT WITH INT19 |
| 48 | CHECK VIDEO CONFIGURE AGAINST CMOS | D0 | INTERRUPT HANDLER ERROR |
| 49 | INIT. PCI BUS AND DEVICE | D2 | UNKNOWN INTERRUPT ERROR |
| 4A | INIT. ALL VIDEO BIOS ROM | D4 | PENDING INTERRUPT ERROR |
| 4C | SHADOW VIDEO BIOS ROM | D6 | SHUTDOWN 5 |
| 50 | DISPLAY CPU TYPE AND SPEED | D8 | SHUTDOWN ERROR |
| 52 | TEST KEYBOARD | DA | EXTENDED BLOCK MOVE |
| 54 | SET KEYCLICK IF ENABLED | DC | SHUTDOWN 10 |
| 56 | ENABLE KEYBOARD | 89 | ENABLE NMI |
| 58 | TEST FOR UNEXPECTED INTERRUPTS | 90 | INIT. HDD CONTROLLER |
| 5A | DISPLAY "PRESS SETUP" | 91 | INIT. LOCAL BUS HDD CONTROLLER |
| 5C | TEST RAM BETWEEN 512K AND 640K | 92 | JUMP TO USER PATCH 2 |
| 60 | TEST EXTENDED MEMORY | 94 | DISABLE A20 ADDRESS LINE |
| 62 | TEST EXTENDED MEMORY ADDRESS LINE | 96 | CLEAR HUGE ES SEGMENT REG. |
| 64 | JUMP TO USER PATCH 1 | 98 | SEARCH FOR OPTION ROMS |

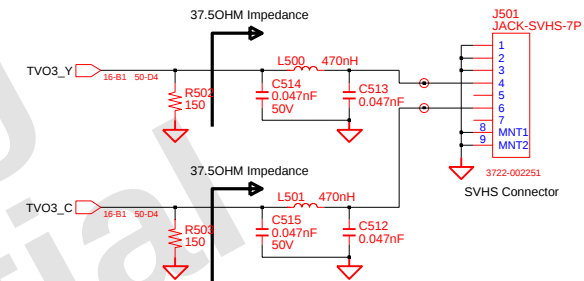
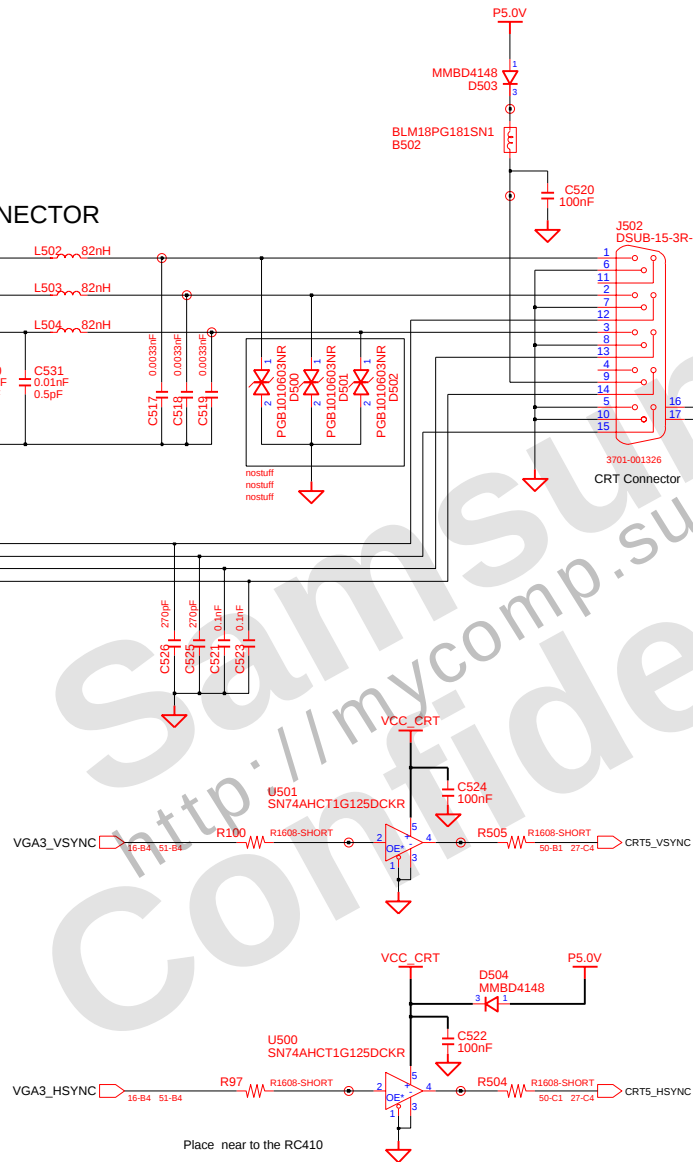
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CHECK	HJ KIM	DEV. STEP	MP			PART NO. BA41-00714A
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	25	OF 52

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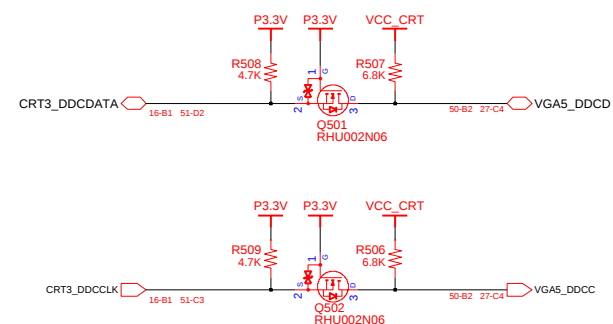




Stitching Cap (061023)



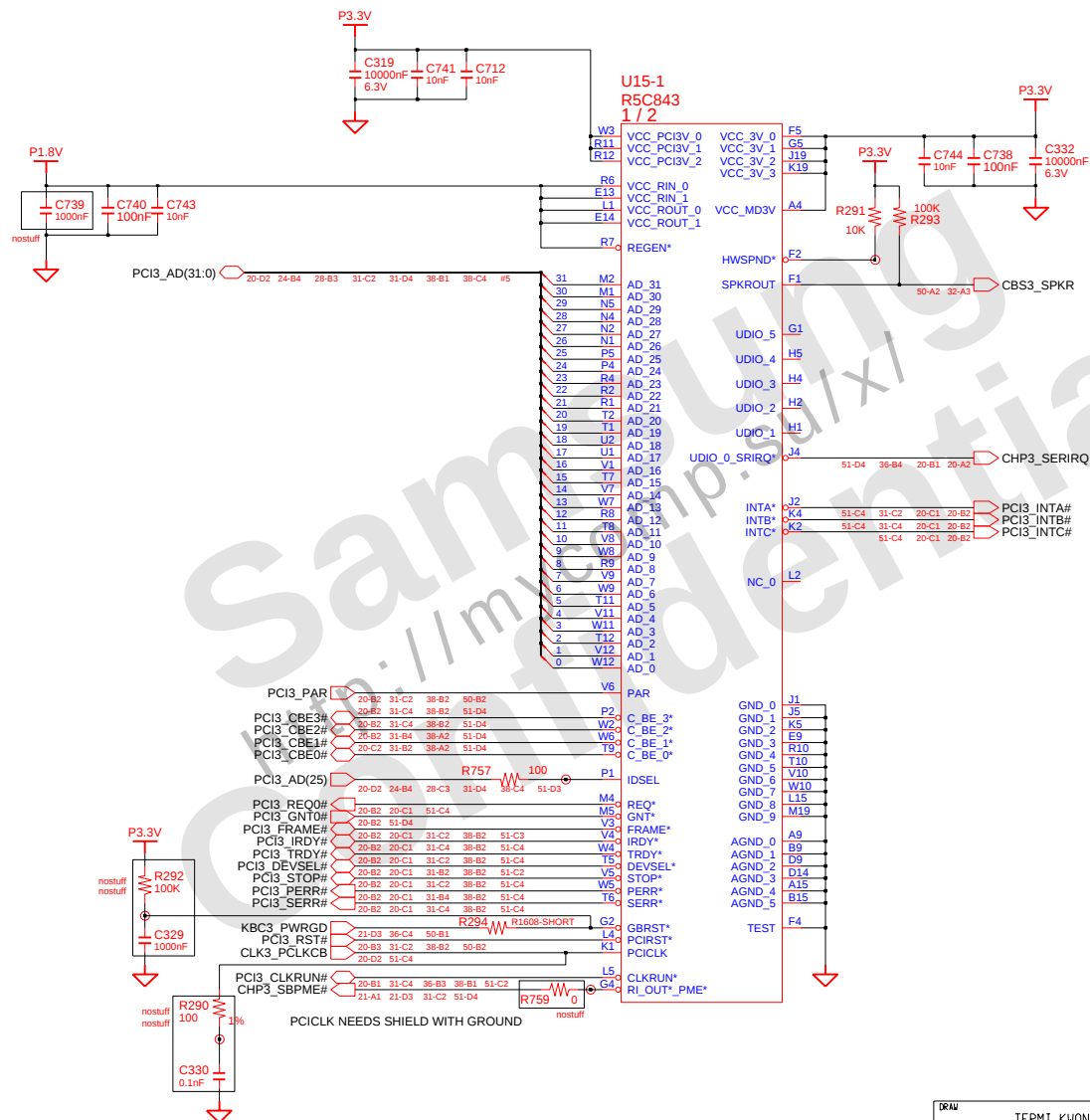
TV-OUT(S-VHS,COMPOSIT)



DRAM	TERM1 KWON	DATE	1/11/2007	TITLE	FIRENZE2-R	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	LAST EDIT		January 11, 2007 8:27:44 PM			
				PAGE	27	OF 52

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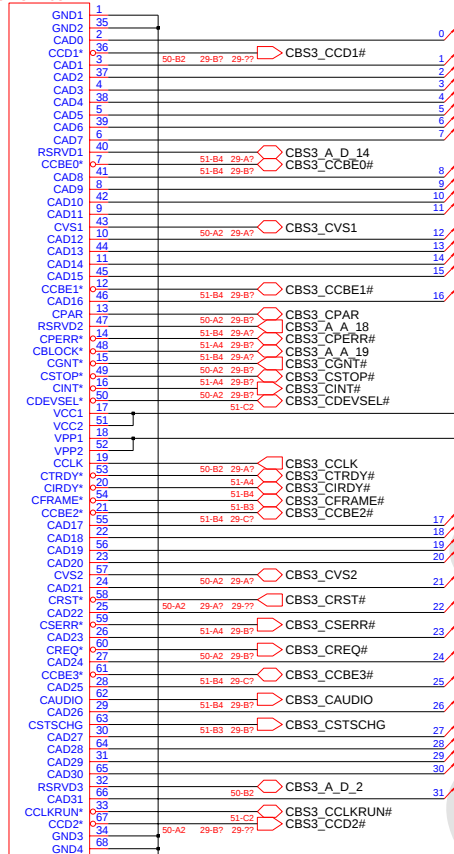
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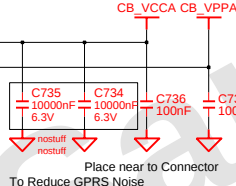
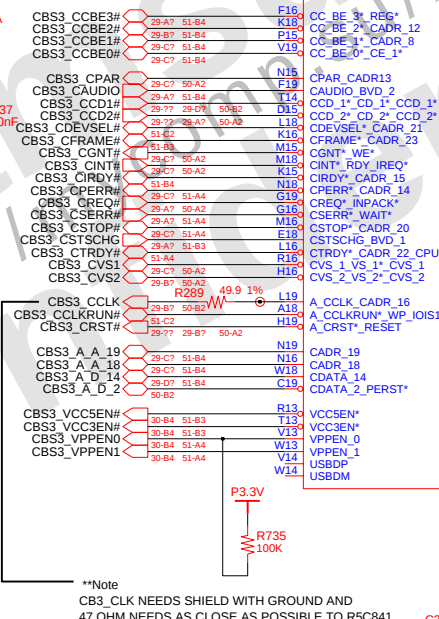
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APPROVAL	SJ PARK	REV	1.0		CARBUS(1/2)	PART NO.
MODULE CODE		LAST EDIT	January 11, 2007 8:27:44 PM			BA41-00714A
					PAGE	28 OF 52

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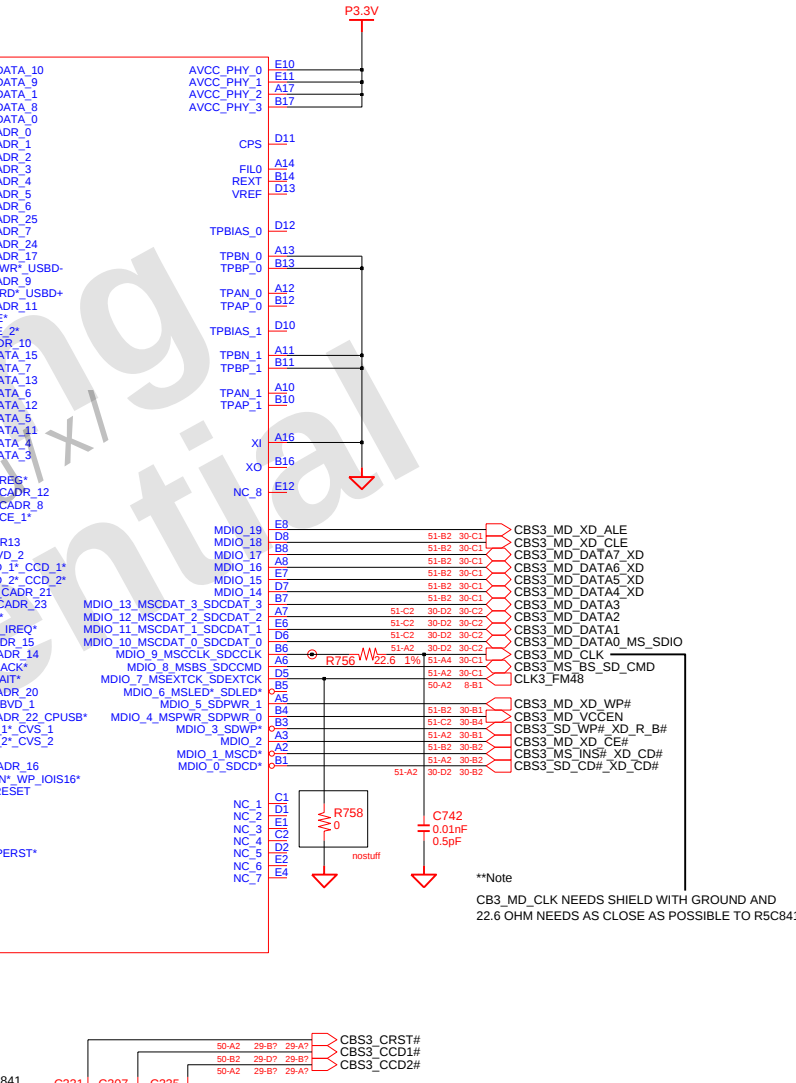
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J7
PCMCIA-68P-AJ8
PCMCIA-68P-MNT

At least 40mil path width

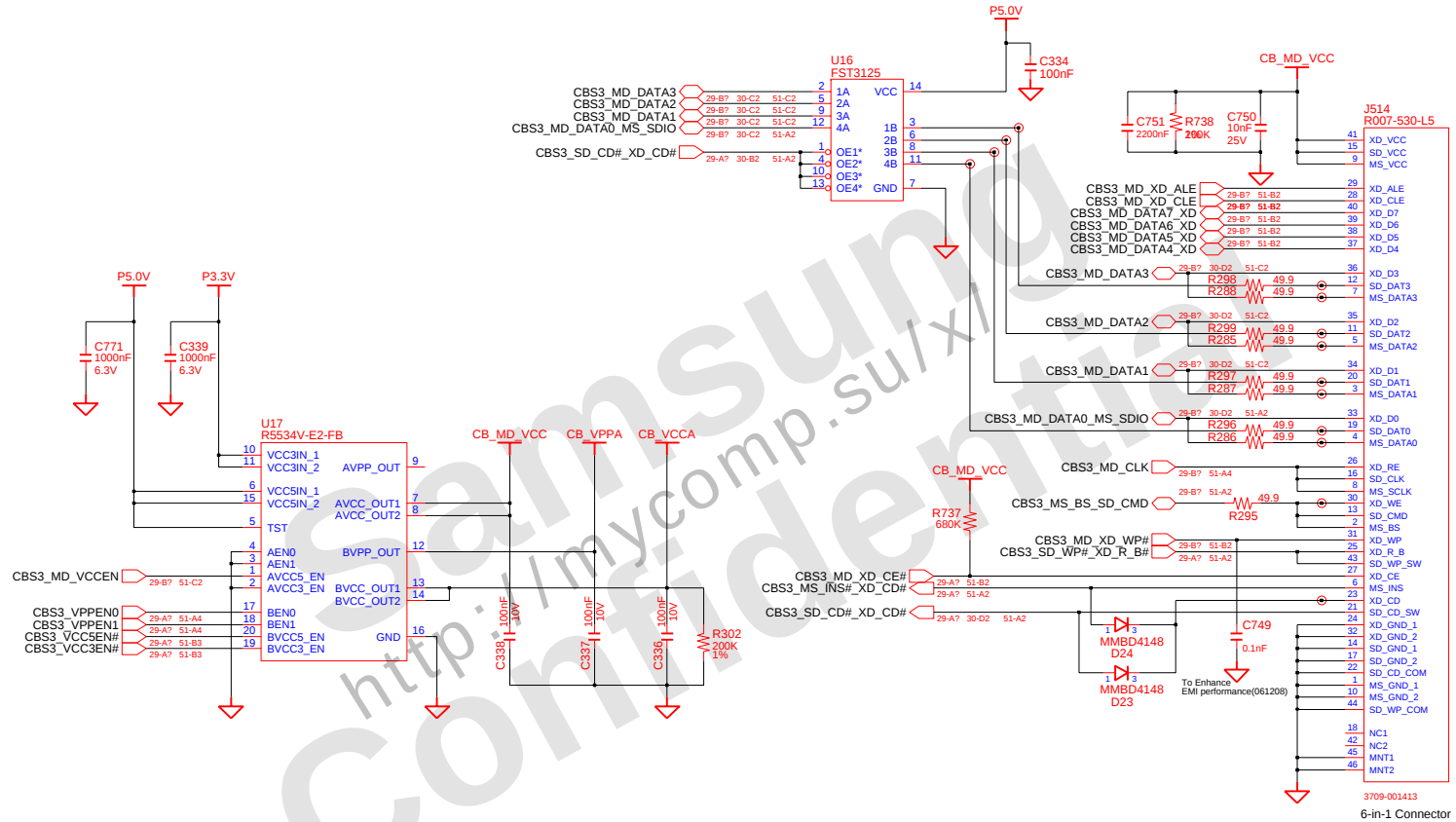
Place near to Connector
To Reduce GPRS Noise

**Note
CBS3_CLK NEEDS SHIELD WITH GROUND AND
47 OHM NEEDS AS CLOSE AS POSSIBLE TO R5C841

U15-2
R5C843
2/2

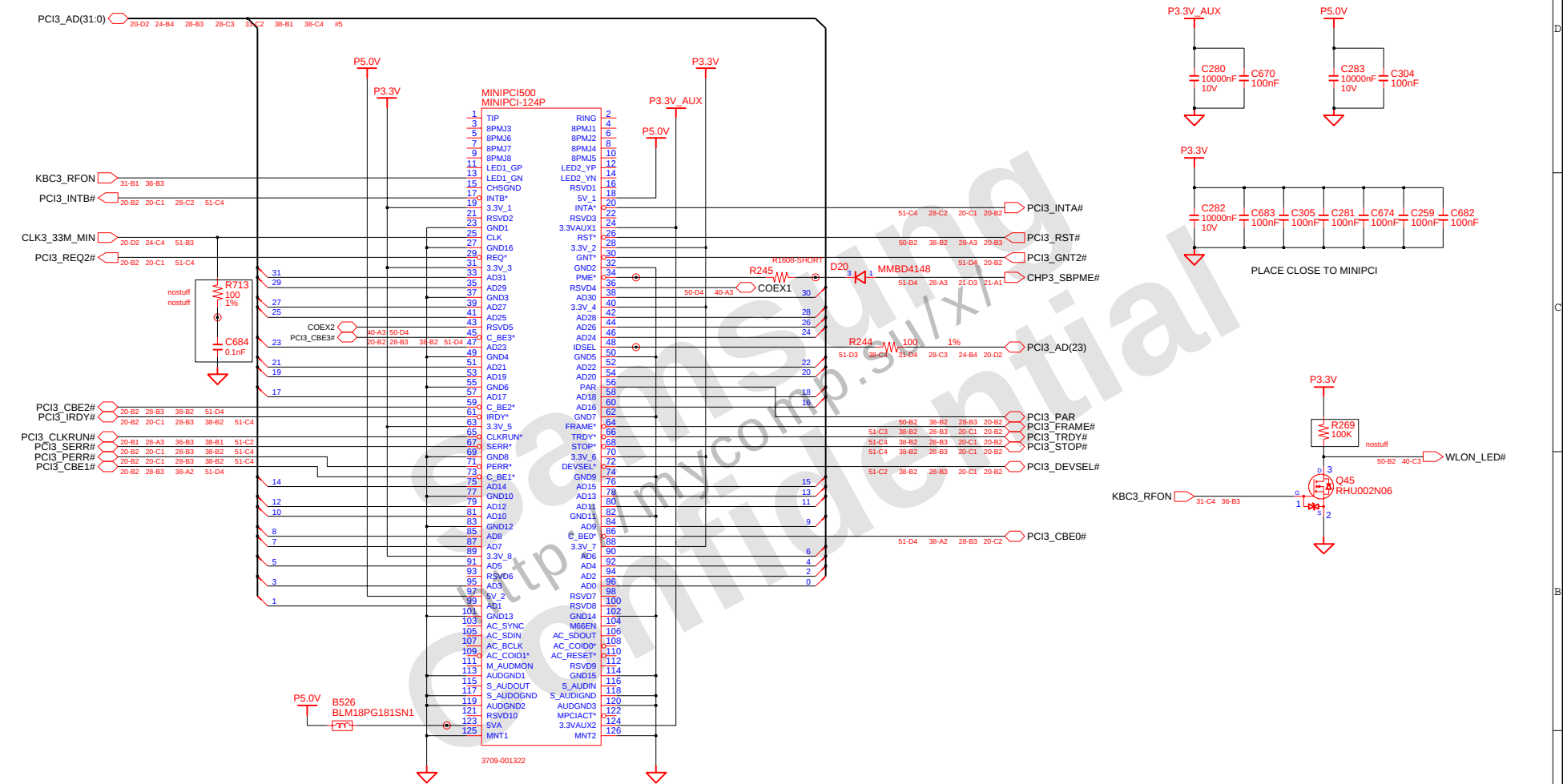
**Note
CBS3_MD_CLK NEEDS SHIELD WITH GROUND AND
22.6 OHM NEEDS AS CLOSE AS POSSIBLE TO R5C841

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CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0	CARDBUS(2/2)	PART NO.	
MODULE CODE		LAST EDIT	January 11, 2007 8:27:44 PM		BA41-00714A	
				PAGE	29 OF 52	



3709-001413
6-in-1 Connector

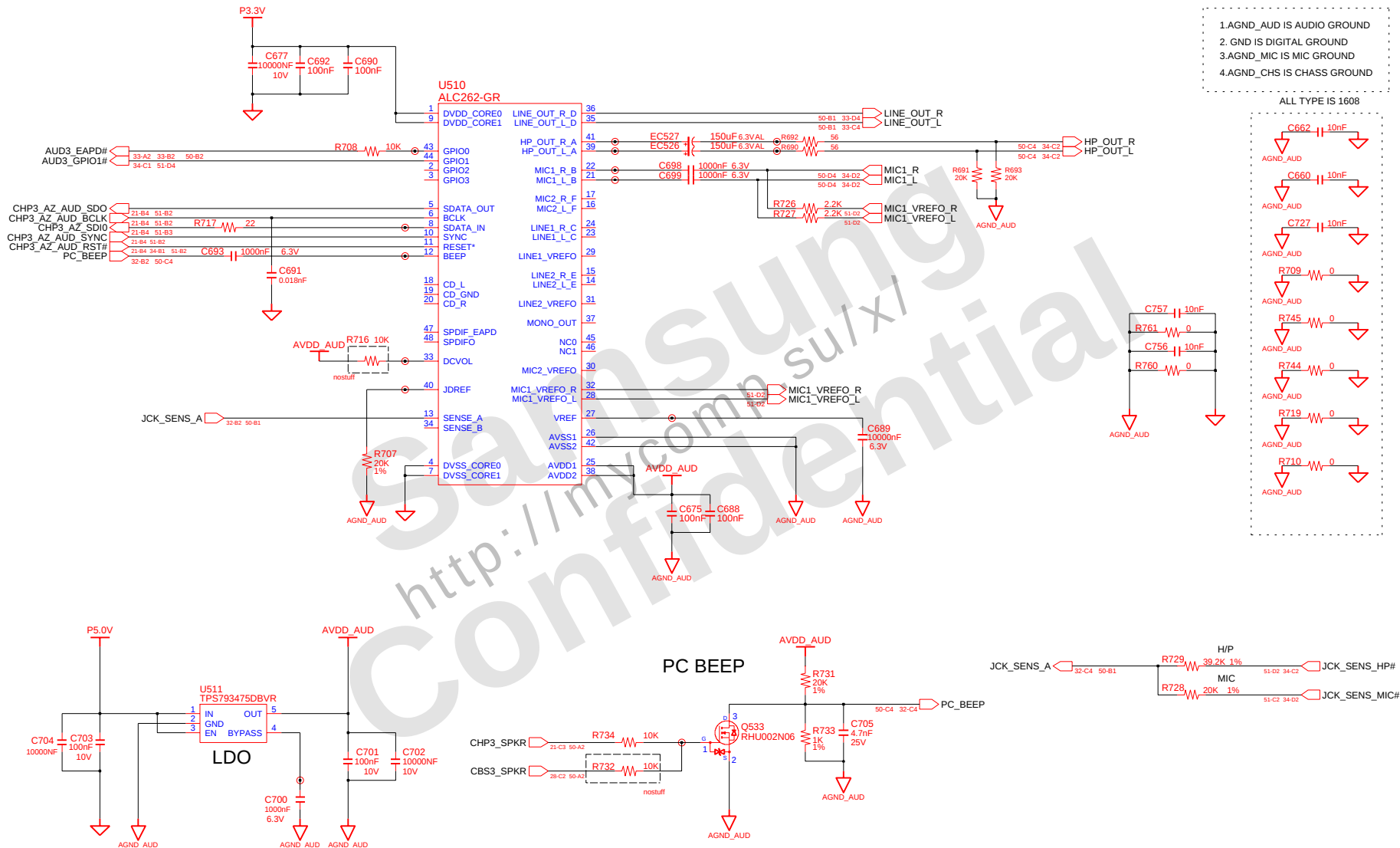
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CHECK	HJ KIM	DEV. STEP	MP			
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MODULE CODE		LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	30 OF 52	



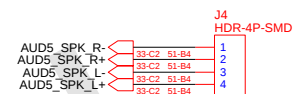
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CHECK	HJ KIM	DEV. STEP	MP			PART NO. BA41-00714A
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefi ned	LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	31	OF 52

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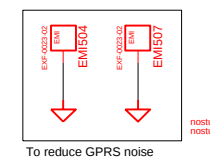
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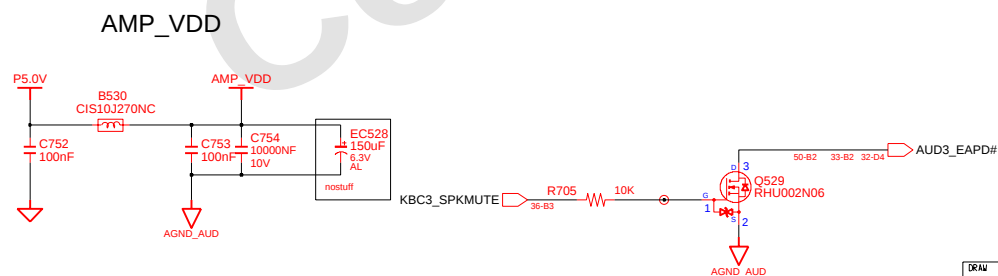
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CHECK	HJ KIM	DEV. STEP	MP			PART NO. BA41-00714A
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefi ned	LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	32 OF 52	



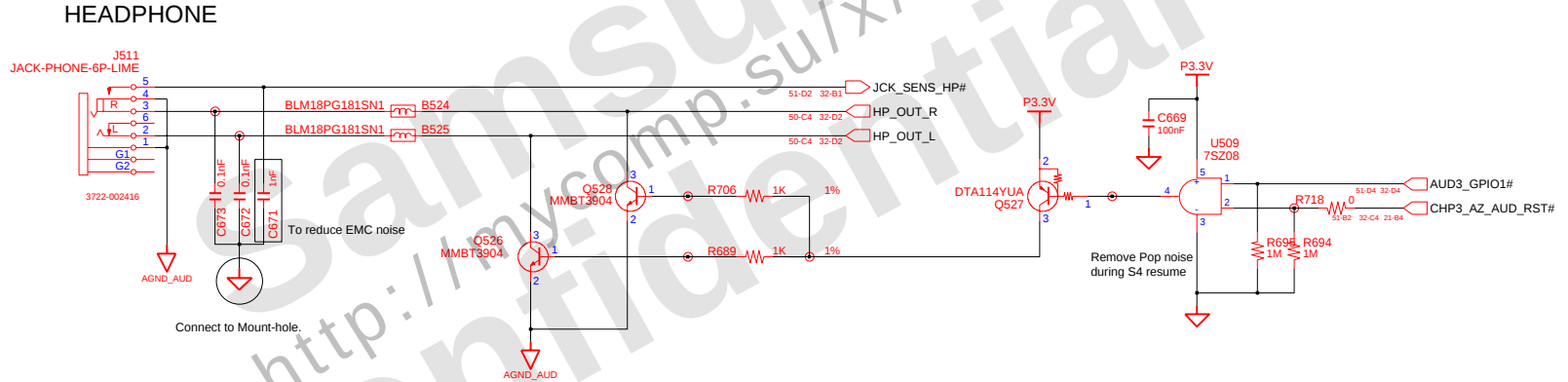
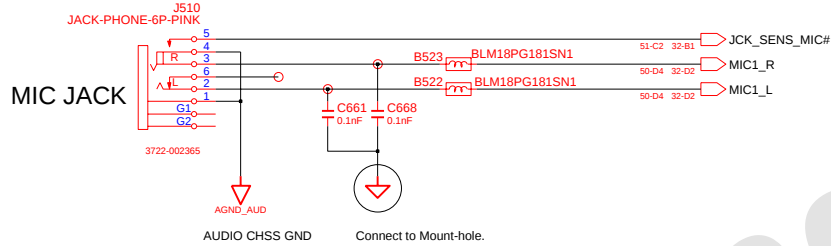
3711-000922
Should be written sign "L","R" on the PCB



To reduce GPRS noise



DRAM	TERM1 KWON	DATE	1/11/2007	TITLE	FIRENZE2-R MAIN LIMITER & AMP	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	January 11, 2007 8:27:44 PM			
				PAGE	33	OF 52
				PART NO.	BA41-00711A	



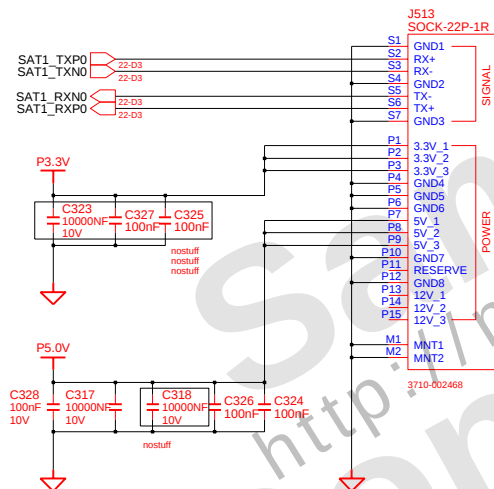
The traces led to Audio Jacks have the width over 10mil

DRAW	TERMI KWON	DATE	1/11/2007	TITLE	FIRENZE2-R MAIN UPPER & AUDIO CONN	SAMSUNG ELECTRONICS PART NO. BA41-00714A
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	34 OF 52	

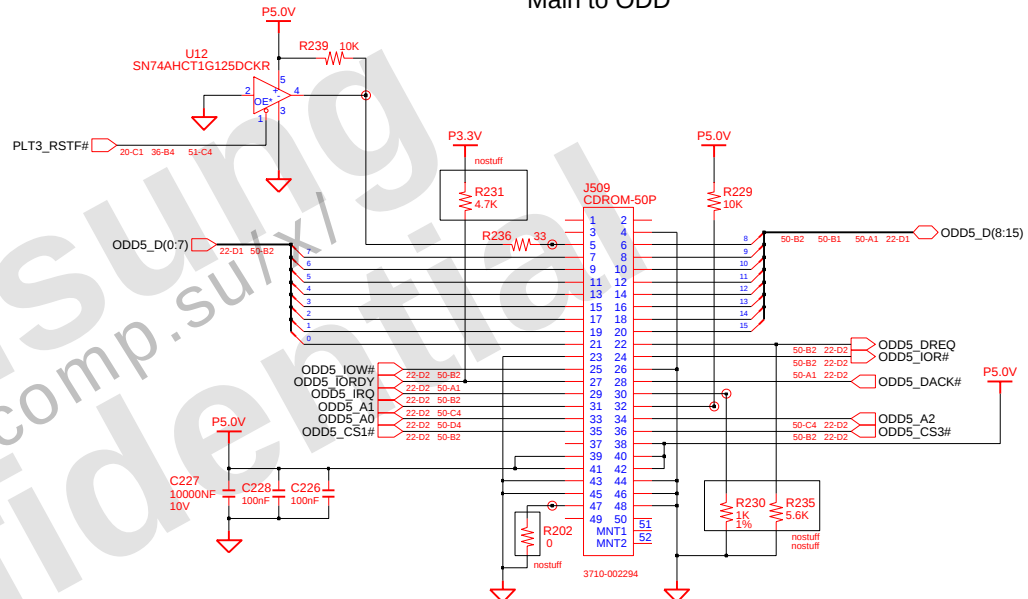
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Main to HDD



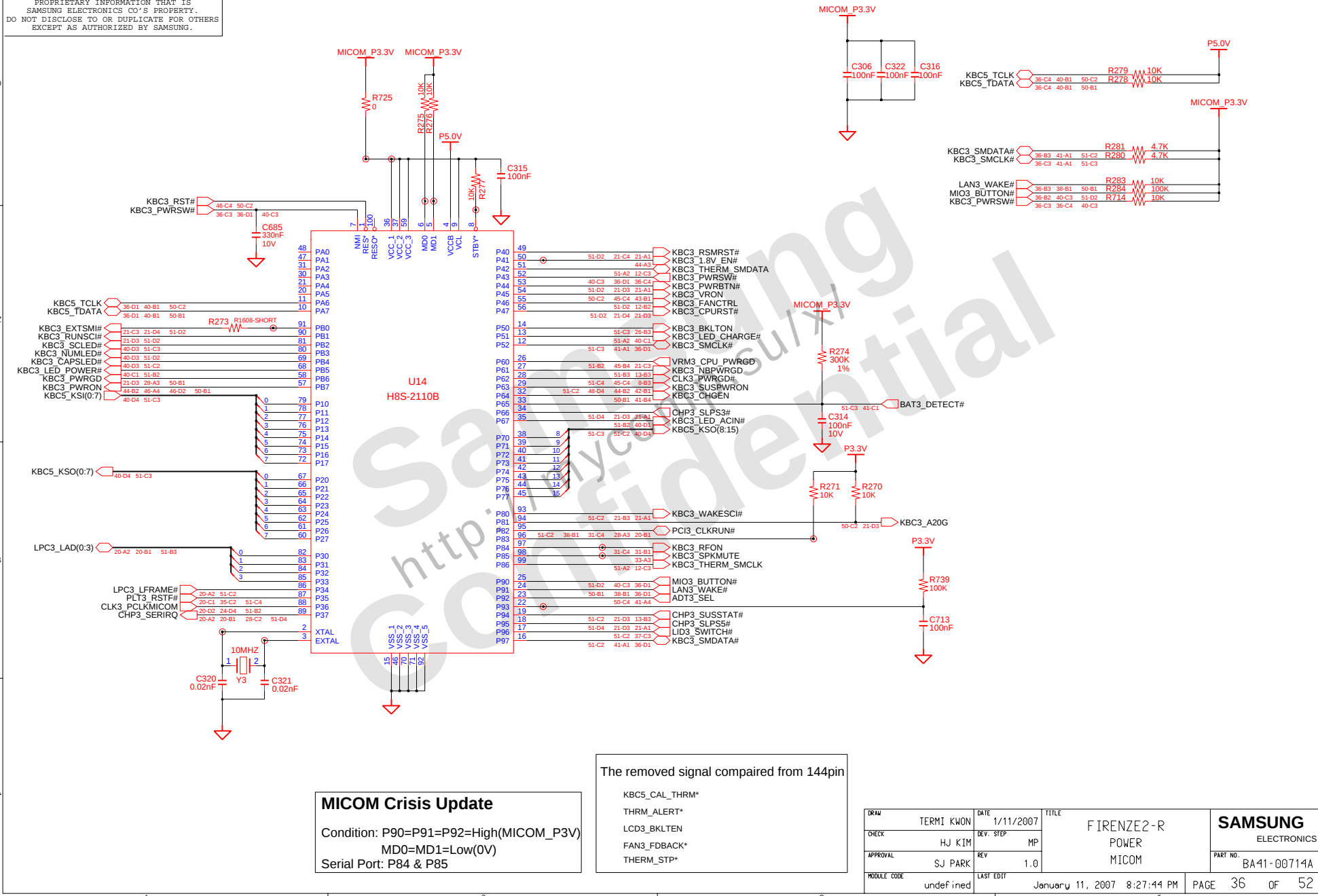
Main to ODD



DRAW	TERMI KWON	DATE	1/11/2007	TITLE	FIRENZE2-R POWER HDD & ODD	SAMSUNG ELECTRONICS PART NO. BA41-00714A
CHECK	HJ KIM	DEV. STEP	MP	REV	1.0	
APPROVAL	SJ PARK	LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	35 OF 52	
MODULE CODE	undefined					

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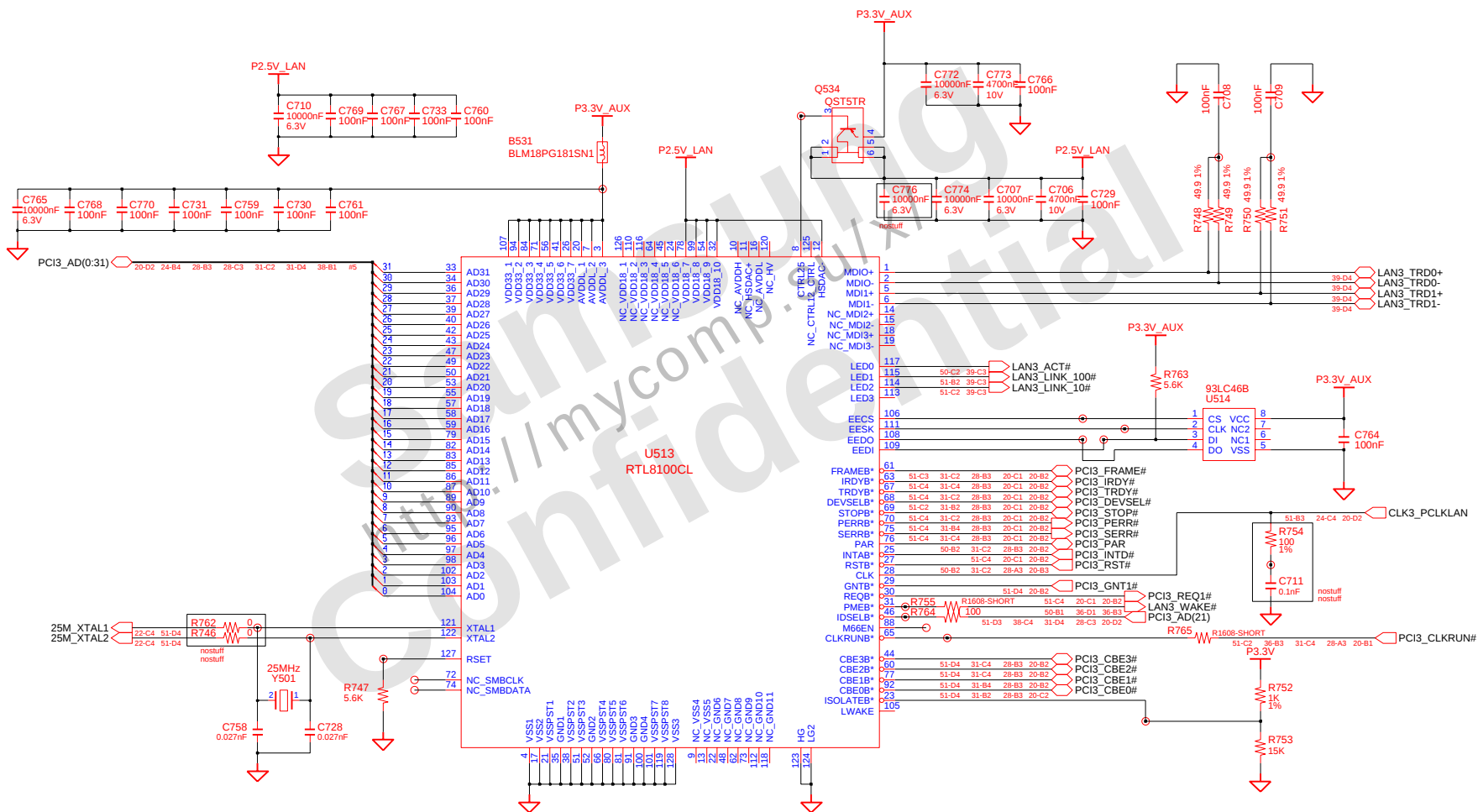
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LAN Controller (Only 10/100M)

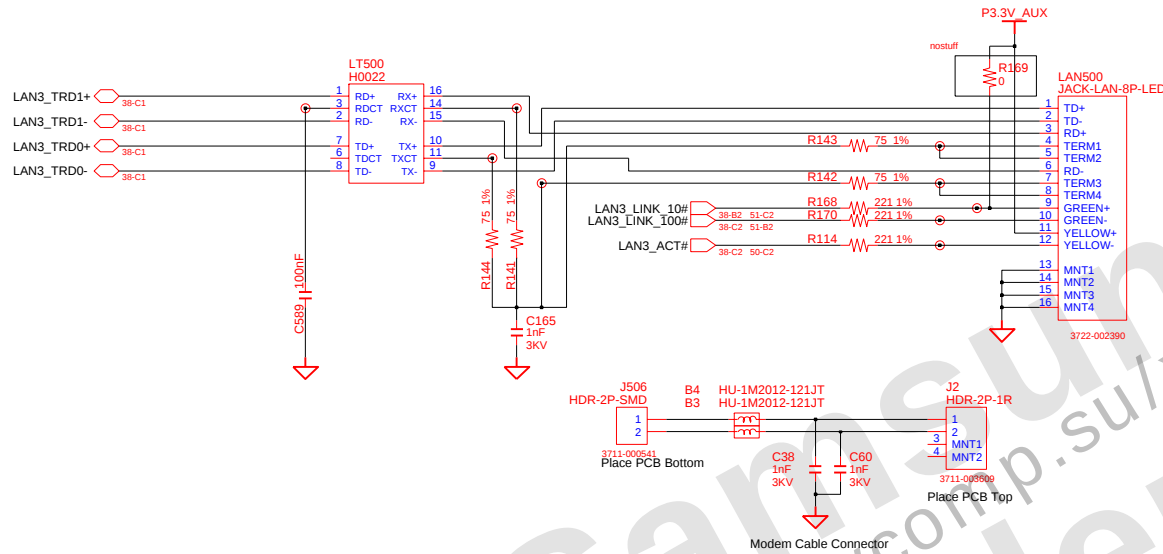


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APPROVAL	SJ PARK	REV	1.0		LAN	PART NO.
MODULE CODE	undefined	LAST EDIT	January 11, 2007 8:27:44 PM			BA41-00714A
					PAGE	38 OF 52

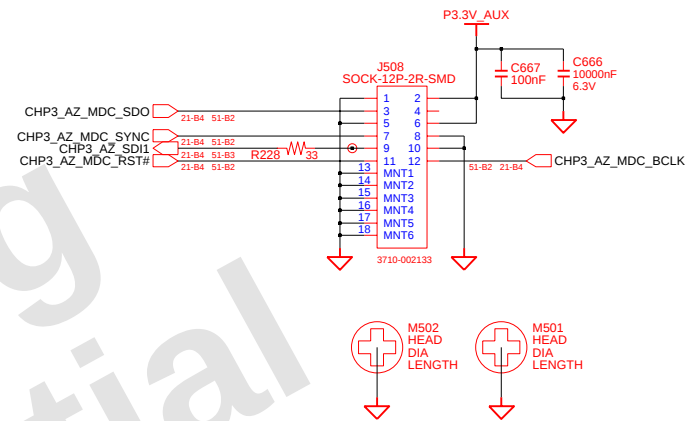
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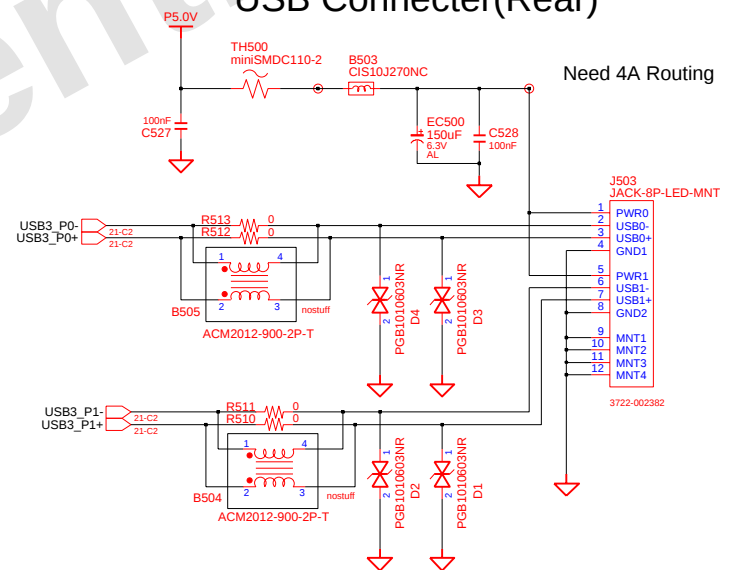
LAN Connector



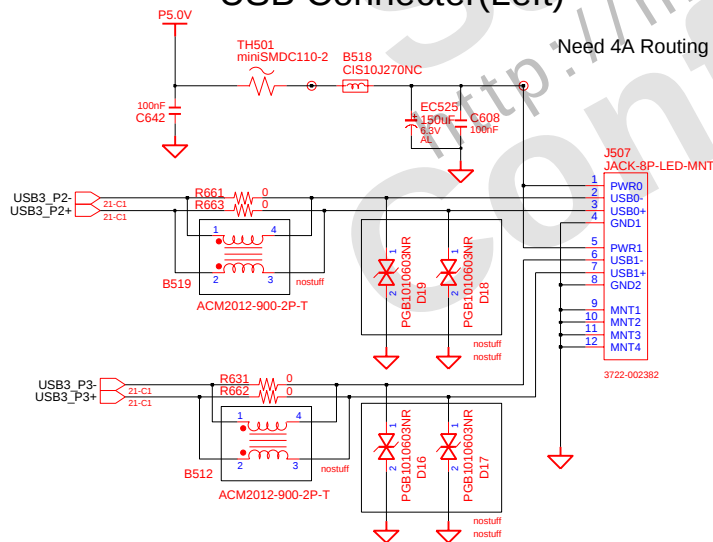
MDC Connector



USB Connector(Rear)



USB Connector(Left)

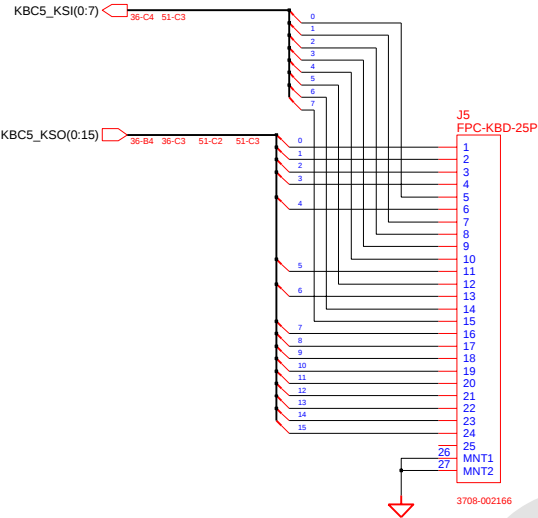


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MODULE CODE	undefined	LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	39	OF 52

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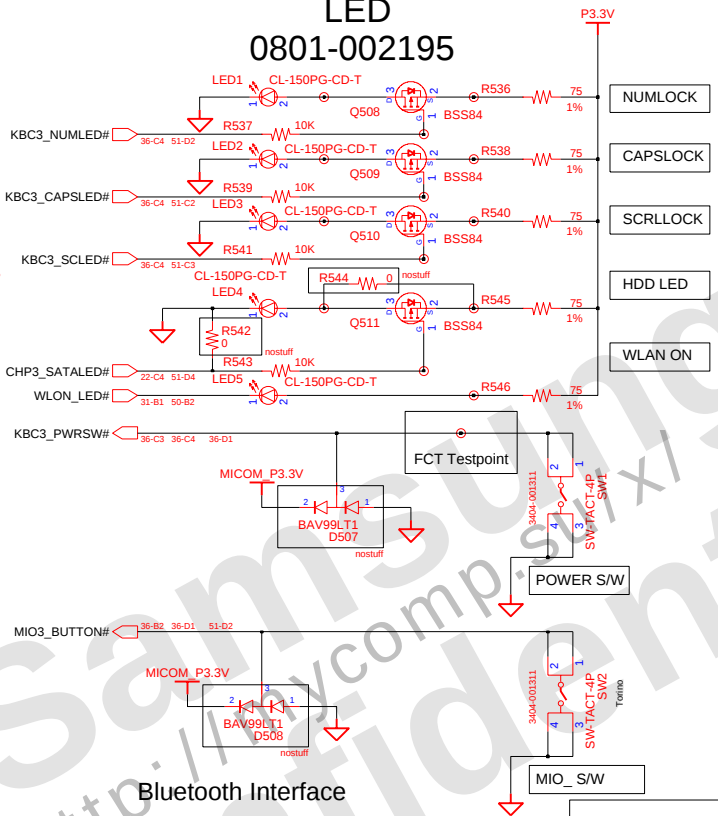
KEYBOARD

Same connector with Sedona

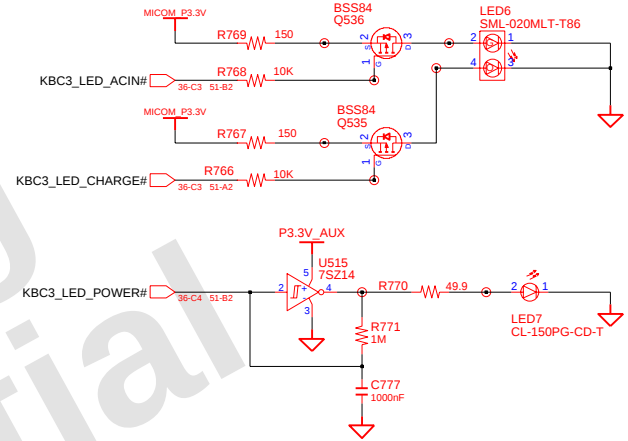


LED

0801-002195

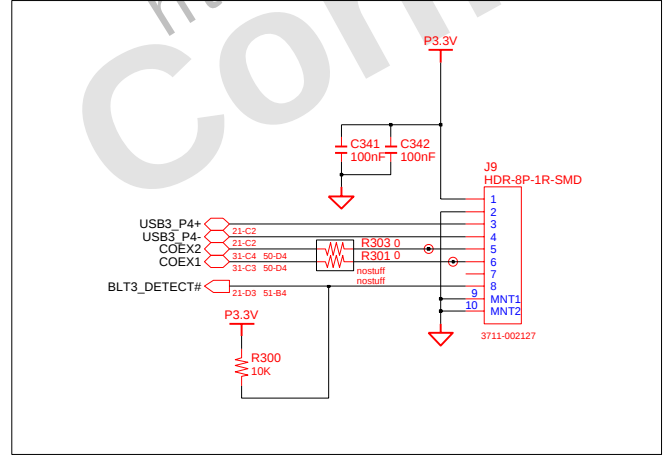


ADAPTERIN/CHARGING LED

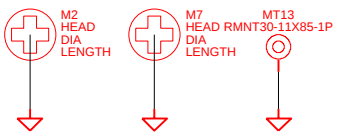
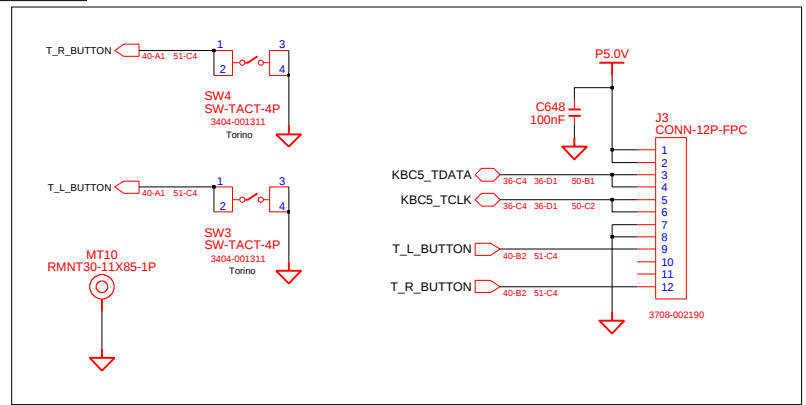


Bluetooth Interface

Factory Option

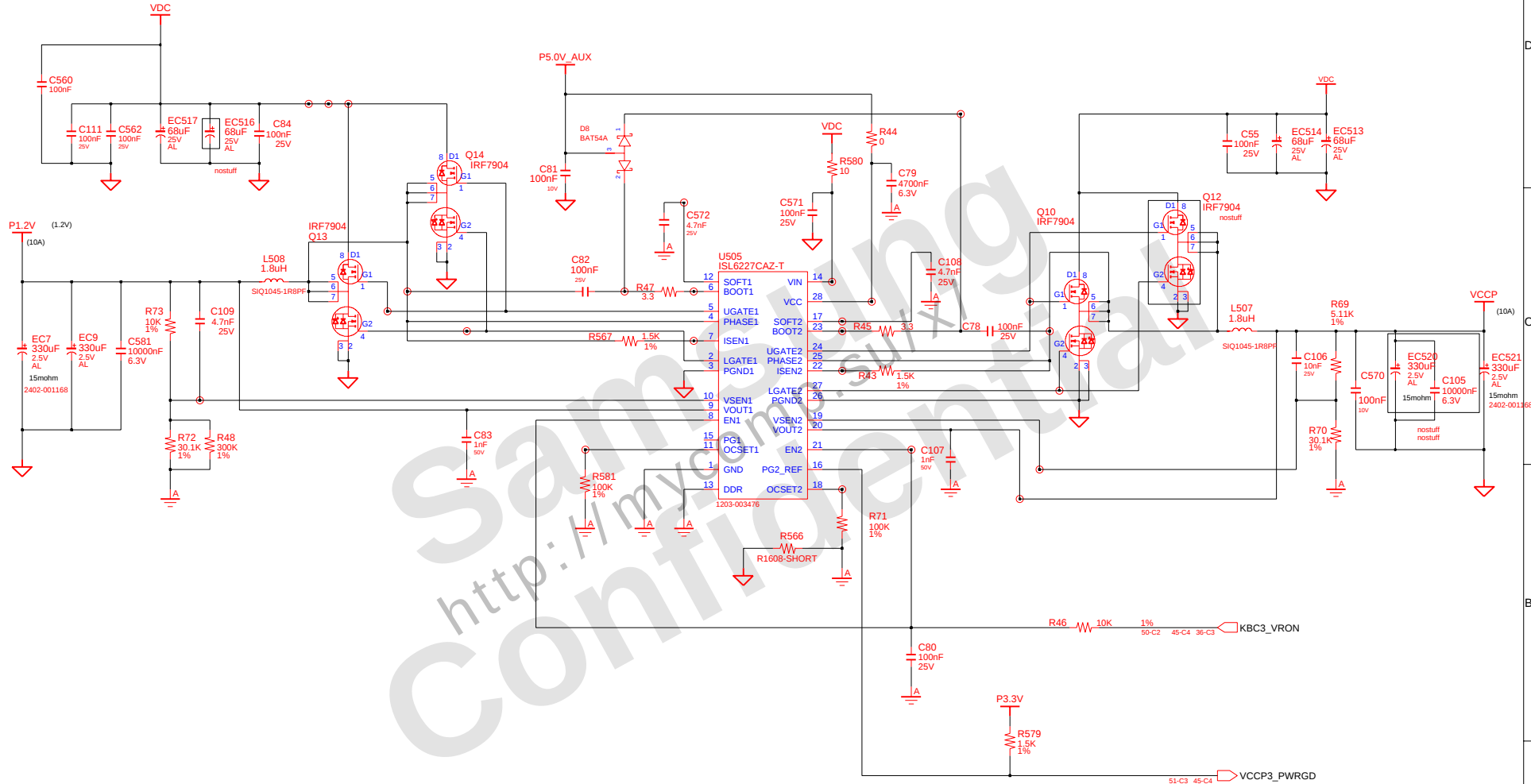


TOUCHPAD



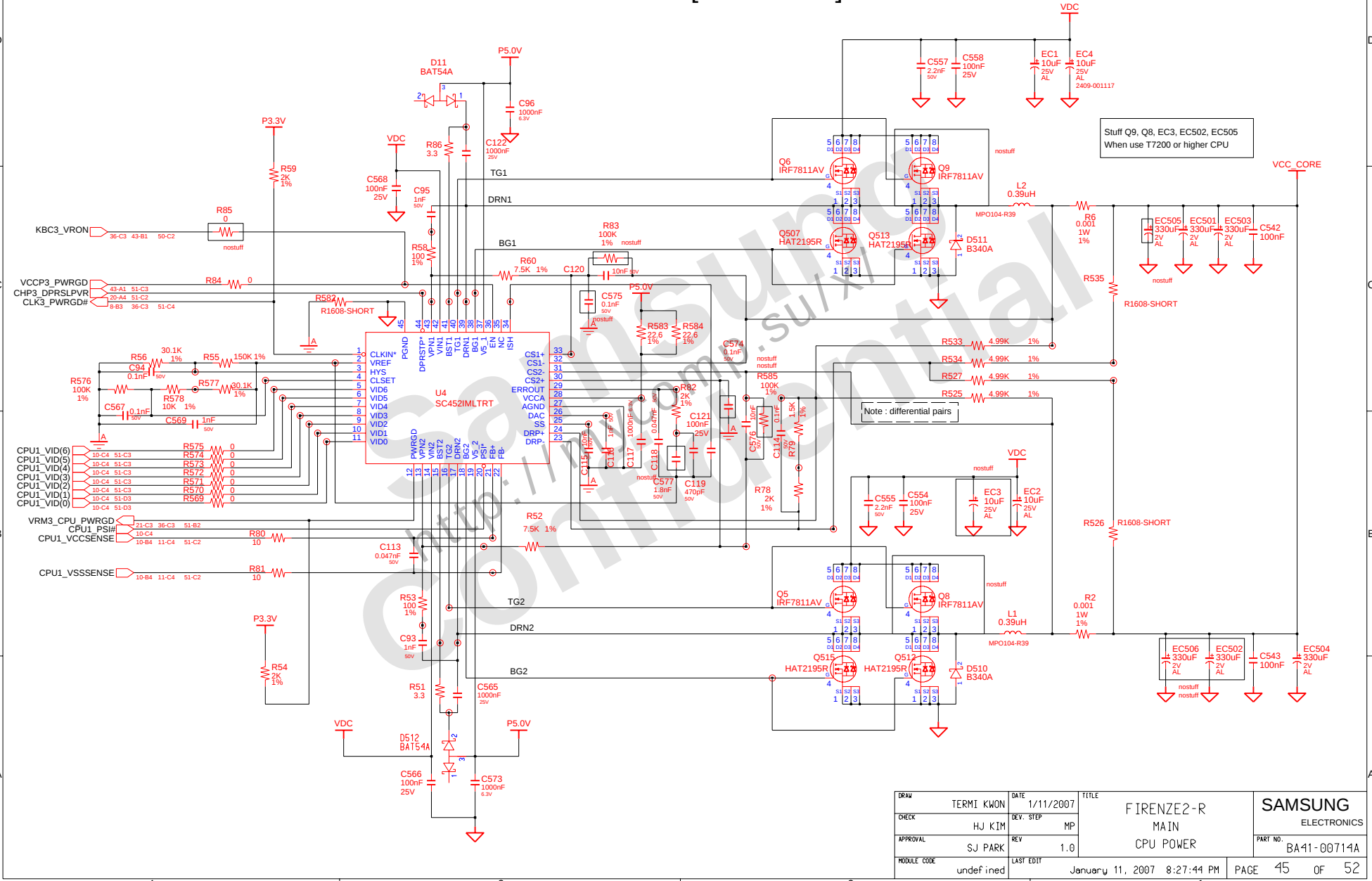
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APPROVAL	SJ PARK	REV	1.0	B'D TO B'D CONNECTOR	PART NO.	BA41-00714A
MODULE CODE	undefined	LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	40	OF 52

P1.2V(VCC_NB) & VCCP (1.05V)



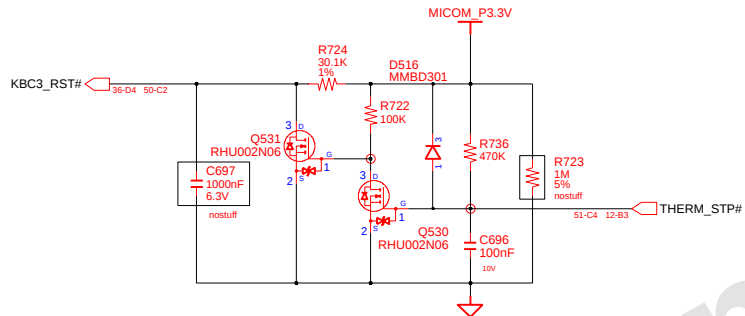
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APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	43	OF 52

CPU VRM [SEMTECH]

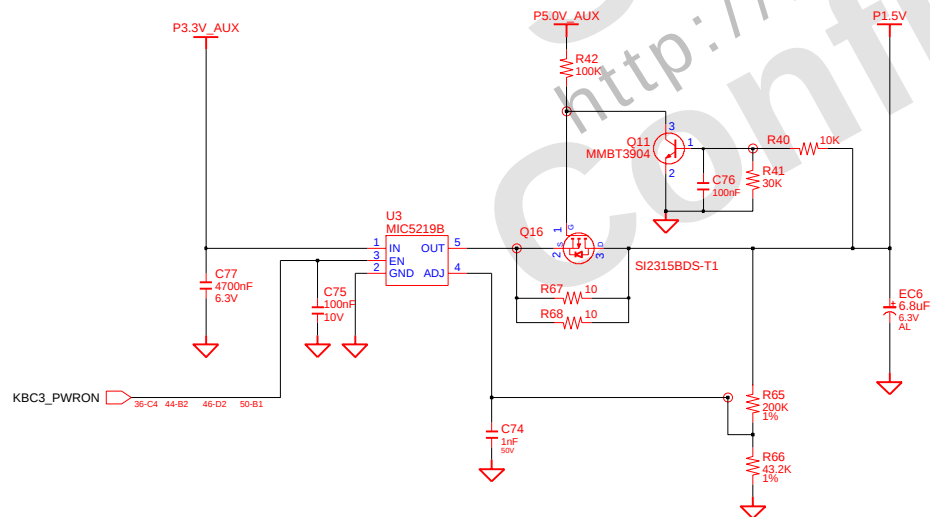


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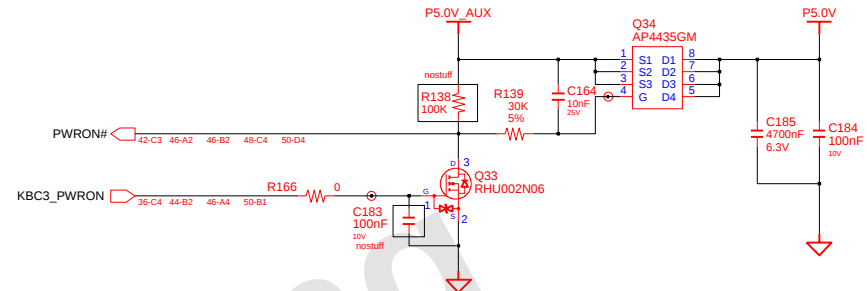
MICOM RESET



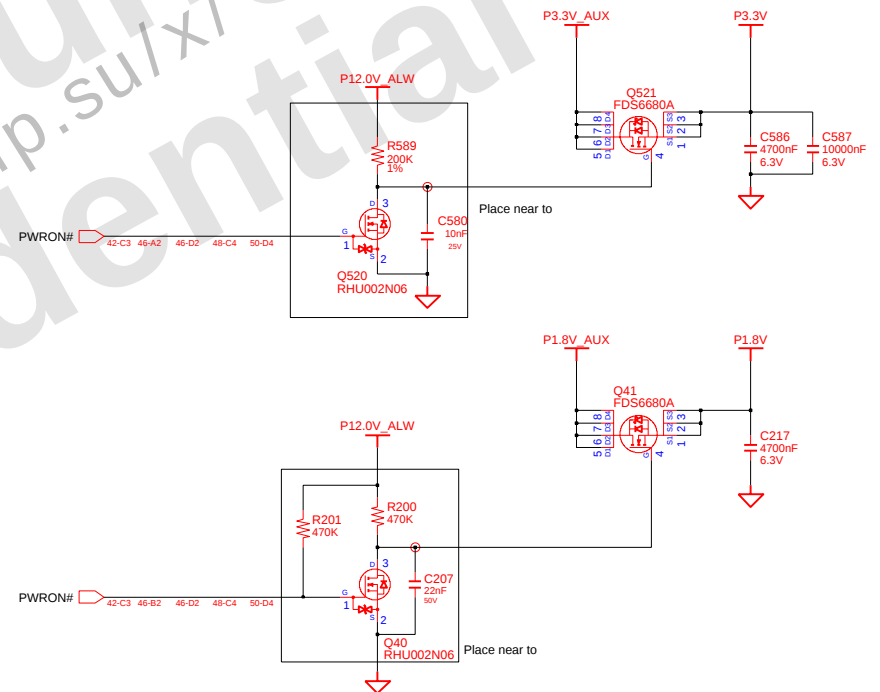
P1.5V POWER



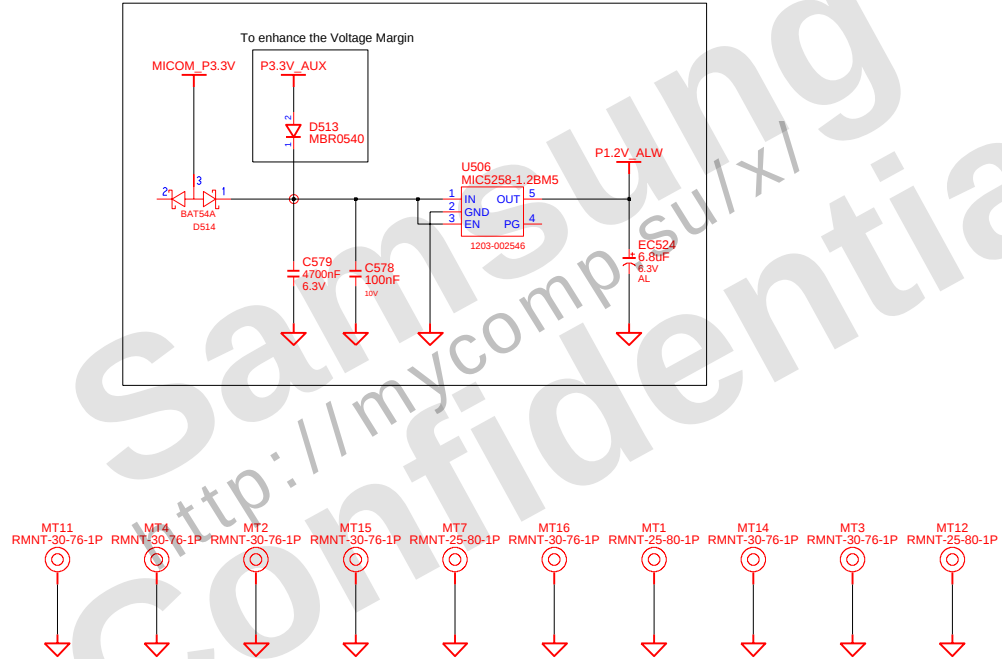
Switched Power On (P5V)



Switched Power On (P3.3V & 1.8V)



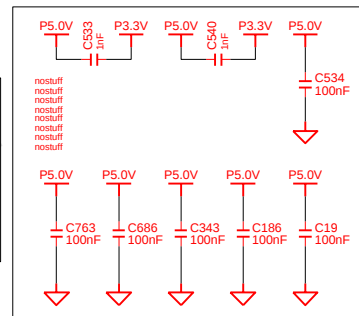
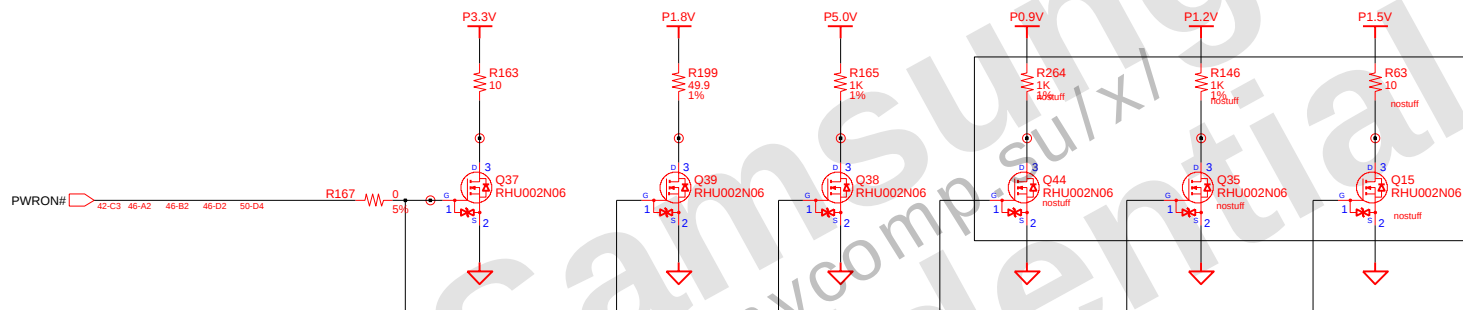
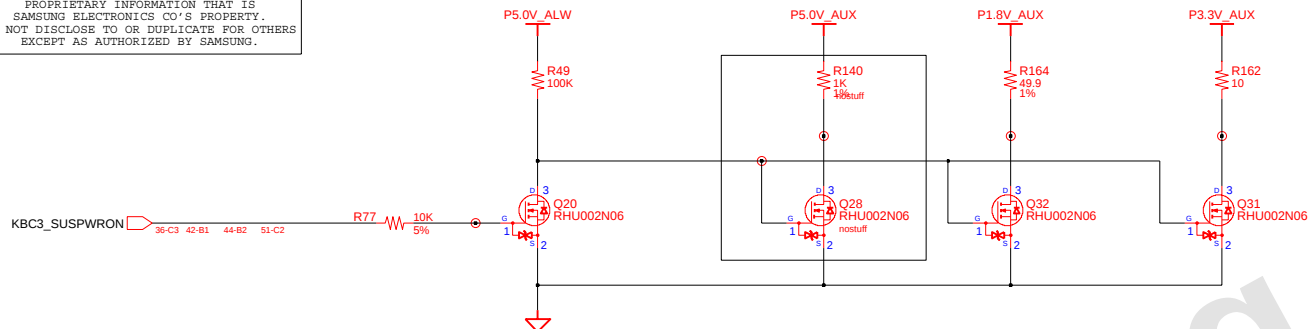
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			MP	MAIN			
APPROVAL	SJ PARK	REV	1.0	MICOM & SWITCHED POWER		PART NO.	BA41-00714A
MODULE CODE	undefined	LAST EDIT	January 11, 2007 8:27:44 PM			PAGE	46 OF 52



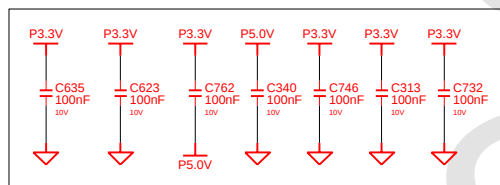
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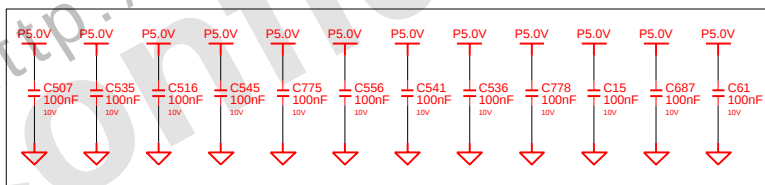
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To enhance DMB performance(060206)

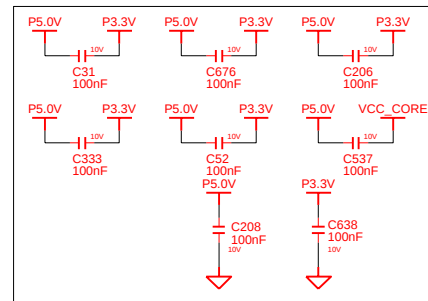


STICHING CAP

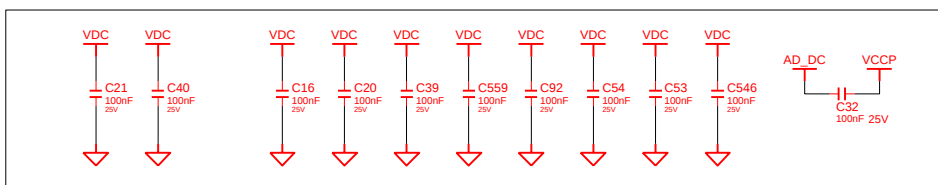


Decap for P5.0V Plane

To reduce BB noise(120 ~ 230MHz) from Power Line (2006/01/24 relate on EMI)



Stiching Cap for Power partition
 To reduce BB noise(120 ~ 230MHz) from Power Partition points (2006/01/24 relate on EMI)



Decap for VDC

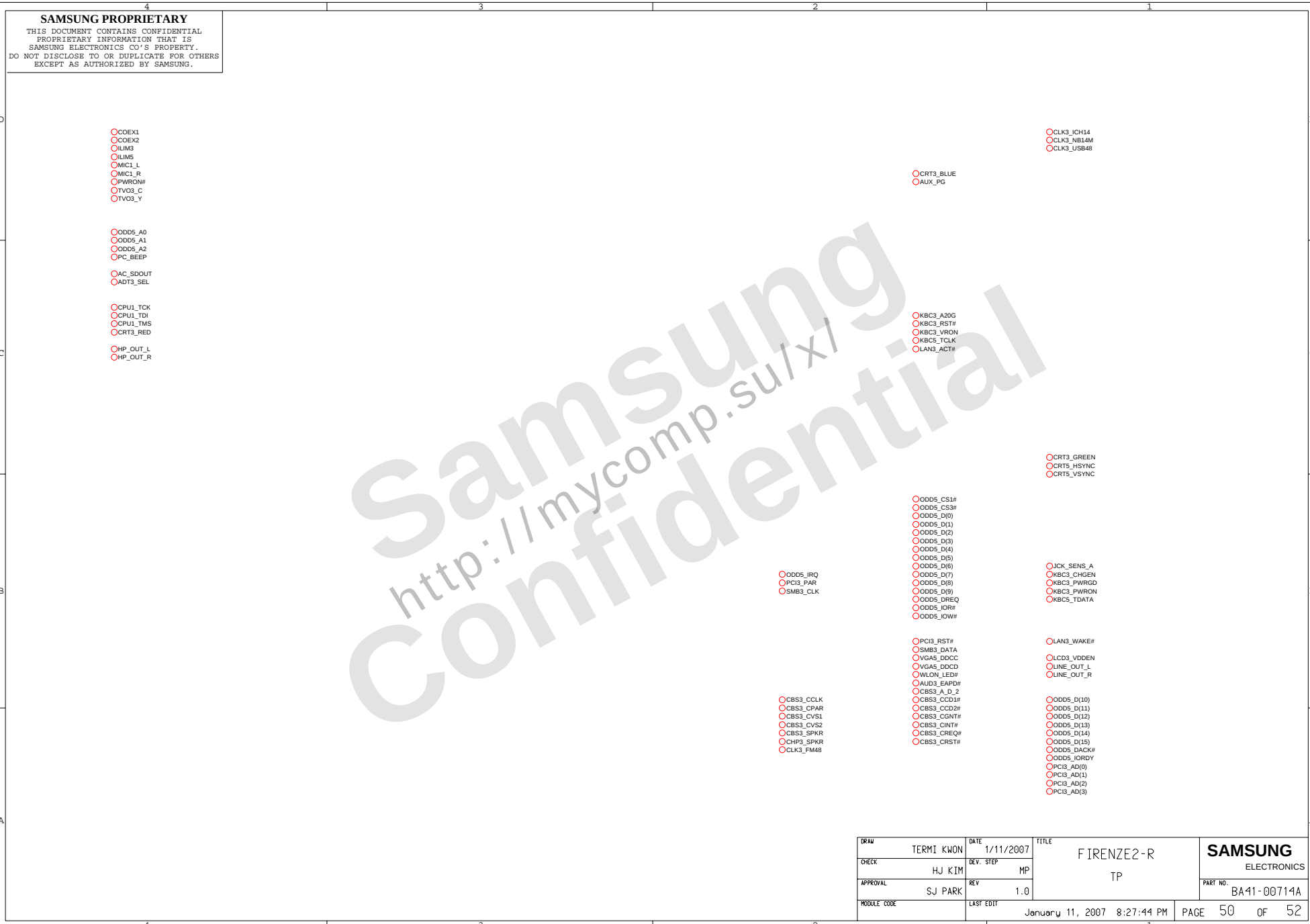
To reduce BB noise(120 ~ 230MHz) from Power Line (2006/01/24 relate on EMI)

DRAW	TERMI KWON	DATE	1/11/2007	TITLE	FIRENZE2-R MAINBD POWER ADAPT	SAMSUNG ELECTRONICS PART NO. BA41-00714A
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	48 OF 52	

REV1
1 O
2 O O3

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/D)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW	TERMI KWON	DATE	1/11/2007	TITLE	FIRENZE2-R	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0	TP		PART NO. BA41-00714A
MODULE CODE	LAST EDIT		January 11, 2007 8:27:44 PM		PAGE 49	OF 52



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○P3.3V

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○P3.3V
○P3.3V
○P3.3V
○P3.3V
○P5.0V
○P5.0V
○P5.0V
○P5.0V
○P5.0V
○P5.0V
○PLLVD018

○VCC_CRT

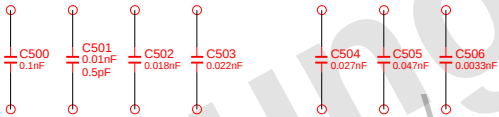
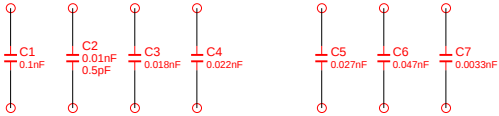
○VCC_CORE
○VCC_CORE
○VCC_CORE
○VCC_CORE
○VCC_CORE

○PRTC_BAT
○P1.2V_ALW

○P1.8V_AUX
○P1.8V_AUX
○P1.8V_AUX
○P1.8V_AUX
○P1.8V_AUX
○P2.5V_LAN
○P2.5V_LAN
○P2.5V_LAN
○P2.5V_LAN
○P2.5V_LAN
○P3.3V_AUX
○P3.3V_AUX
○P3.3V_AUX
○P3.3V_AUX
○P3.3V_AUX
○P5.0V_ALW
○P5.0V_ALW
○P5.0V_ALW
○P5.0V_ALW
○P5.0V_ALW
○P5.0V_AUX
○P5.0V_AUX
○P5.0V_AUX
○P5.0V_AUX
○P5.0V_AUX

○PCIE_VDDR

○P12.0V_ALW
○P12.0V_ALW
○P12.0V_ALW
○P12.0V_ALW
○P12.0V_ALW
○VDC
○VDC
○VDC
○VDC
○VDC
○VDC
○VCCP
○VCCP
○VCCP
○VCCP
○VCCP



DRAW	TERMI KWON	DATE	1/11/2007	TITLE	FIRENZE2-R	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			PART NO. BA41-00714A
MODULE CODE		LAST EDIT	January 11, 2007 8:27:44 PM	PAGE	52 OF 52	