

GENEVA

CPU : MEROM
Chip Set : SANTAROSA CHIPSET
Remarks : Mobility Platform

Model Name : GENEVA
PBA Name : MAIN
PCB Code : BA41-XXXXX
Dev. Step : PV2
Revision : 1.0
T.R. Date :

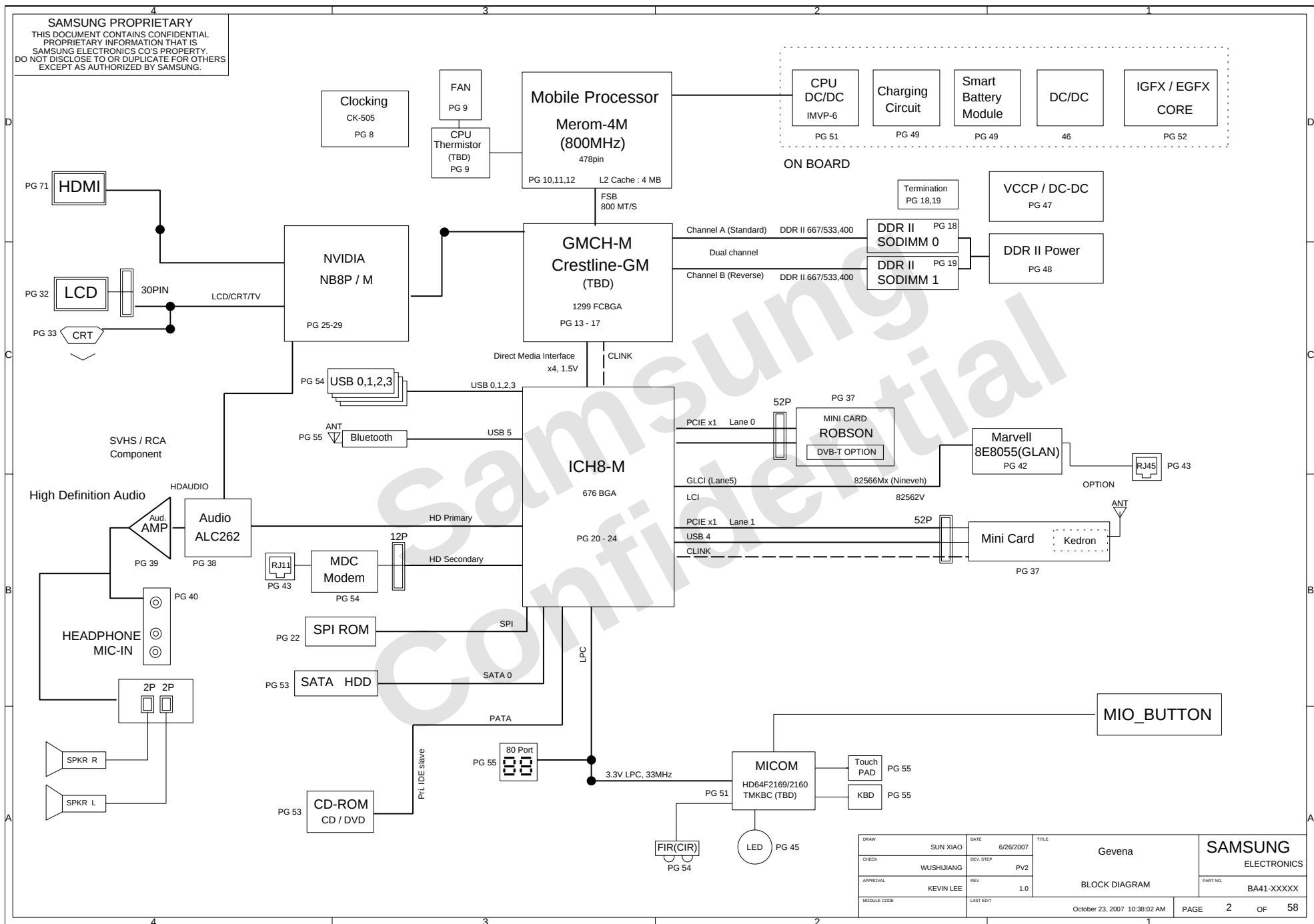
DRAW	CHECK	APPROVAL

Table of Contents

Sheet 1	Cover
Sheet 2	Diagram (Block/Power) & Annotations
Sheet 8	Clock Generator
Sheet 9	Thermal Sensor & FAN
Sheet 10-12	Merom-4M CPU
Sheet 13-17	Crestline-GMCH
Sheet 18	DDR2 SODIMM A
Sheet 19	DDR2 SODIMM B
Sheet 20-23	ICH8-M
Sheet 24	ICH8-M STRAP
Sheet 25-28	NVIDIA NB8P
Sheet 29	NVIDIA NB8P STRAP
Sheet 30	Video Memory Channel A
Sheet 31	Video Memory Channel B
Sheet 32	LCD and Camera Connector
Sheet 33	CRT PORT
Sheet 34	SIO CHIP and Connector
Sheet 35	7 IN 1 Card Reader
Sheet 36	MINI CARD AND ROBSON DVB-T
Sheet 37	Express card
Sheet 38	AUDIO - ALC262
Sheet 39	AUDIO - AMP
Sheet 40	AUDIO - HEADPHONE & MIC JACK
Sheet 41	AUDIO - POWER
Sheet 42-43	LAN AND CONNECTOR
Sheet 44-45	MICOM AND MICOM POWER LOGIC
Sheet 46	POWER - SWITCH POWER
Sheet 47	POWER - VCCP P1.25V and P1.2V
Sheet 48	POWER - DDR2 POWER
Sheet 49	POWER - CHARGE & POWER MANAGEMENT
Sheet 50	POWER - P3.3V_ALW & P5V_AUX
Sheet 51	POWER - CPU VRM
Sheet 52	POWER - GFX CORE P1.5V
Sheet 53	HDD & ODD Connector
Sheet 54	USB/MDC/BLUETOOTH/TOUCHPAD
Sheet 55	KBD/LID SWITCH/80H/ICT/LED IF/USB /IF
Sheet 56	OTHERS
Sheet 57	TOUCHPAD AND LED B'D
Sheet 58	SIO AND USB B'D
Sheet 59	TEST POINT
Sheet 60	TEST POINT

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva	SAMSUNG ELECTRONICS
CHECK	WUSHIJIANG	DEV. STEP	PV2	MILAN		
APPROVAL	KEVIN LEE	REV	1.0	COVER	PART NO. BA41-XXXXX	
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	1	OF 58

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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	B,C,D
DT PCI SLOT	AD22	1	B,C,D,C
MiniPCI SLOT	AD23	2	A,B
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHC1) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
MCH_CORE	Core Voltage for CPU
ICH_CORE	Core Voltage for CPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH8-M
P1.05V_M	1.05V switched power rail for ME (on in M0/M1)
P1.25V_M	1.25V switched power rail for ME (on in M0/M1)
P3.3V_M	3.3V switched power rail for ME (on in M0/M1)
P3.3V_A	3.3V always power rail (by KBC3_ALWS_ON)
MICOM_P3V	3.3V always power rail (for Micom)
LAN_3.3V	3.3V always power rail (for LAN)
P1.5V	1.5V switched off power rail (off in S3-S5)
P1.5V_AUX	1.5V switched on power rail
P2.5V	2.5V switched off power rail (off in S3-S5)
P1.8V	1.8V switched off power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR
P0.9V	0.9V power rail for DDR
P3.3V	3.3V switched off power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail
PSV	5.0V switched off power rail (off in S3-S5)
PSV_AUX	5.0V switched on power rail

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	DMB
3	Expresas Card
4	DOCKING PORT 0
5	Bluetooth
6	Mini PCI Express
7	Aux Display
8	Test Port (RSVD)
9	WWAN/WIBRO (TBD)

PCI Express Assign

PORT #	ASSIGNED TO
0	PCIe x1 Slot
1	Mini Card (Golan)
2	Mini Card (WIBRO : RSVD)
3	Expresas Card
4	DOCKING PORT 0
5	GLAN

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH8-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	24.576MHz	Cardbus Controller	1394
Crystal	25MHz	LAN	Intel LAN
Crystal	27MHz (TBD)	VIDEO	PEG
Crystal	24.576MHz (TBD)	HD Audio	Audio

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

I²C / SMB Address

Devices	Address	Hex	Bus
ICH8-m	Master	-	SMBUS Master
CPU Thermal Sensor	1001 110x	9Ch	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
DB400 (PCI Express Clocks)	1101 110x	DCh	Clock Buffer for PCI Express
TBD	0100 1100	4Ch	Thermal Sensor
TBD : (LVDS BackLight Inverter)	0101 1000	58h	-
TBD : (ALS)	0111 0010	72h	Ambient Light Sensor
TBD : (AUX DISPLAY)	0011 110x	3Ch	EMA
LAN	1100 1000	C8h	82566
PCI Express Docking	TBD	TBD	TBD
TPM	TBD	TBD	TBD

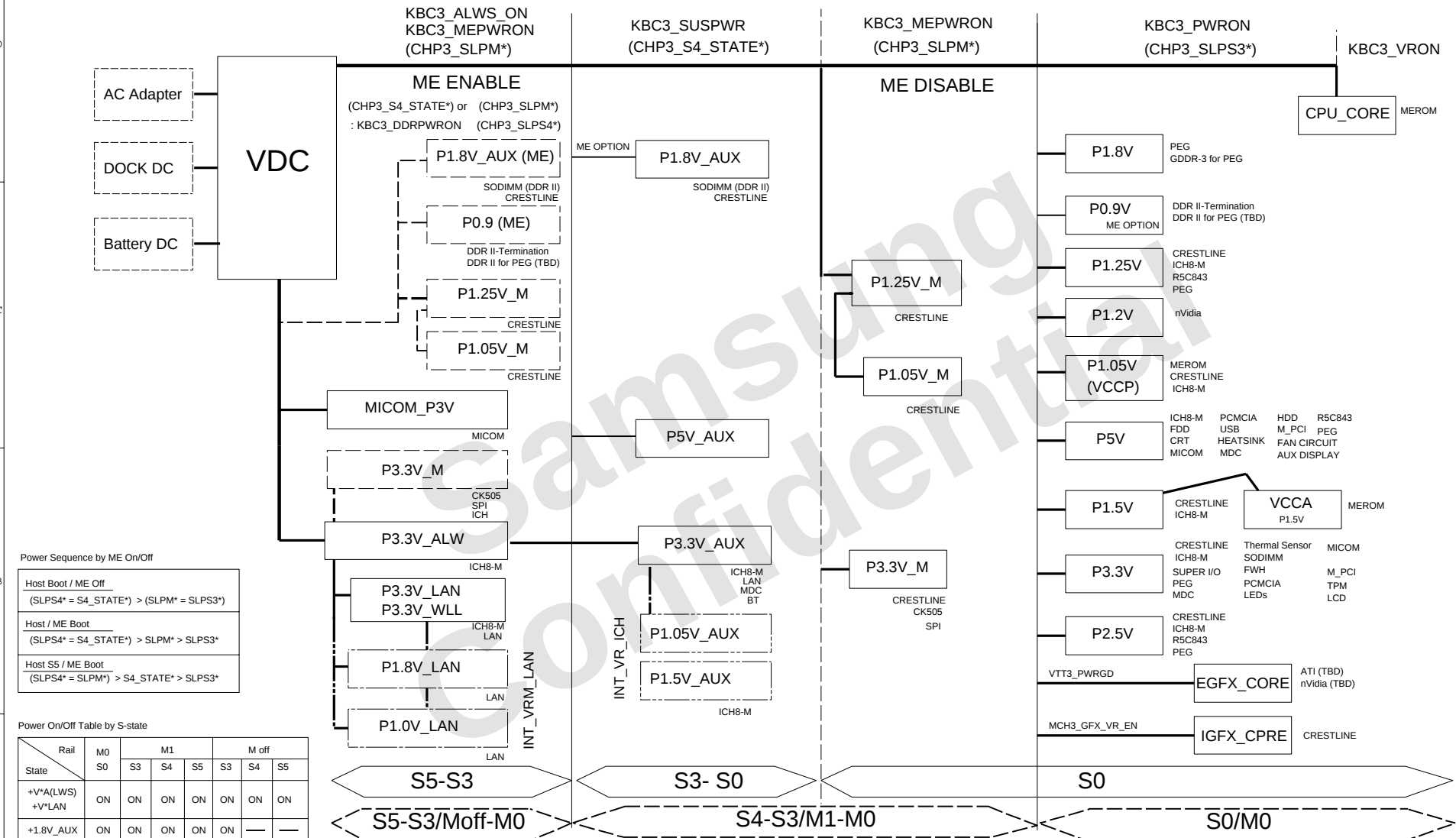
REVISION HISTORY

See rev notes for more information.

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHIJIANG	DEV. STEP	PV2			ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0	BOARD INFO		PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	3	OF 58

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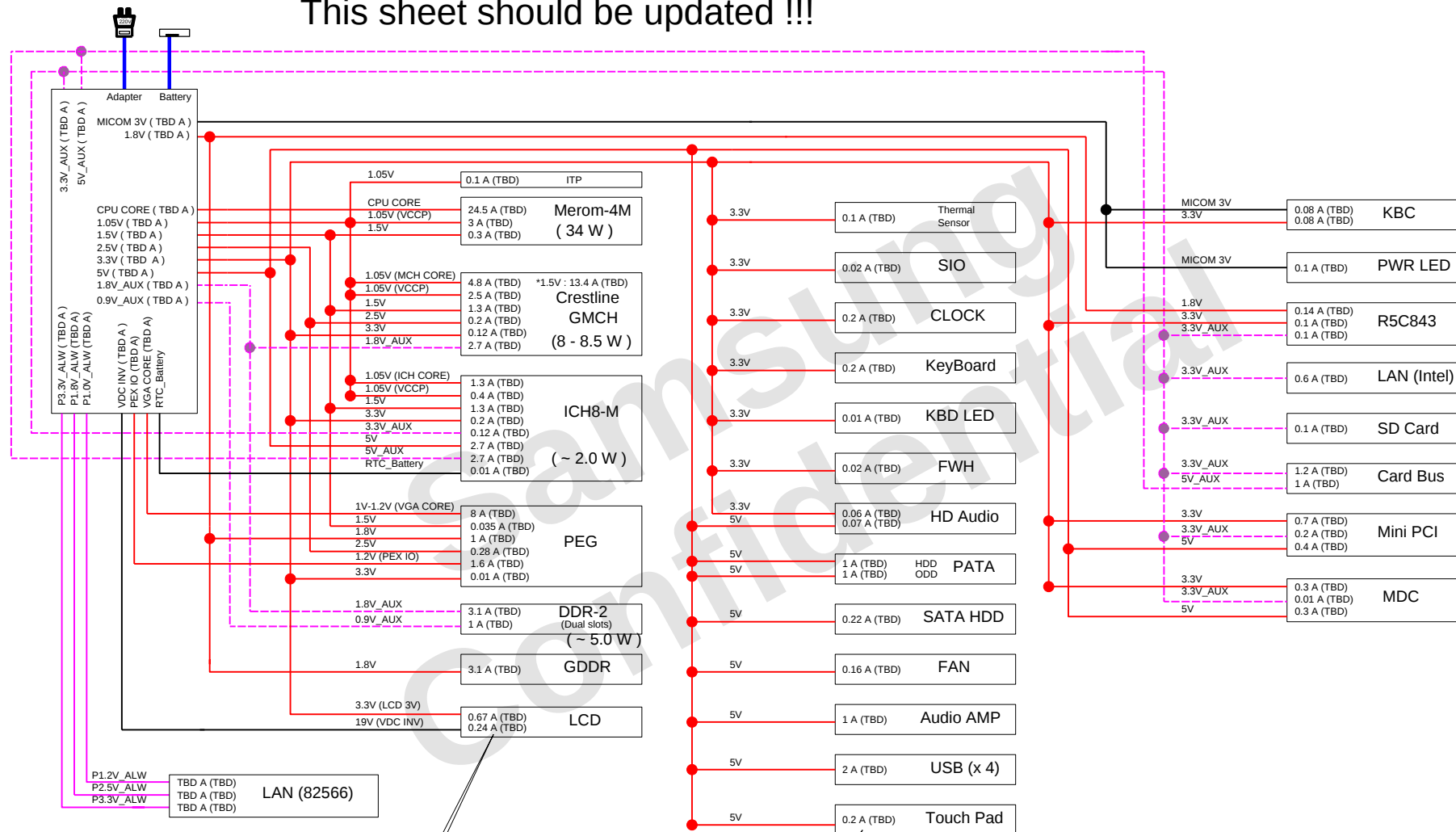
POWER DIAGRAM



POWER RAILS ANALYSIS

Rev. 0.5

This sheet should be updated !!!



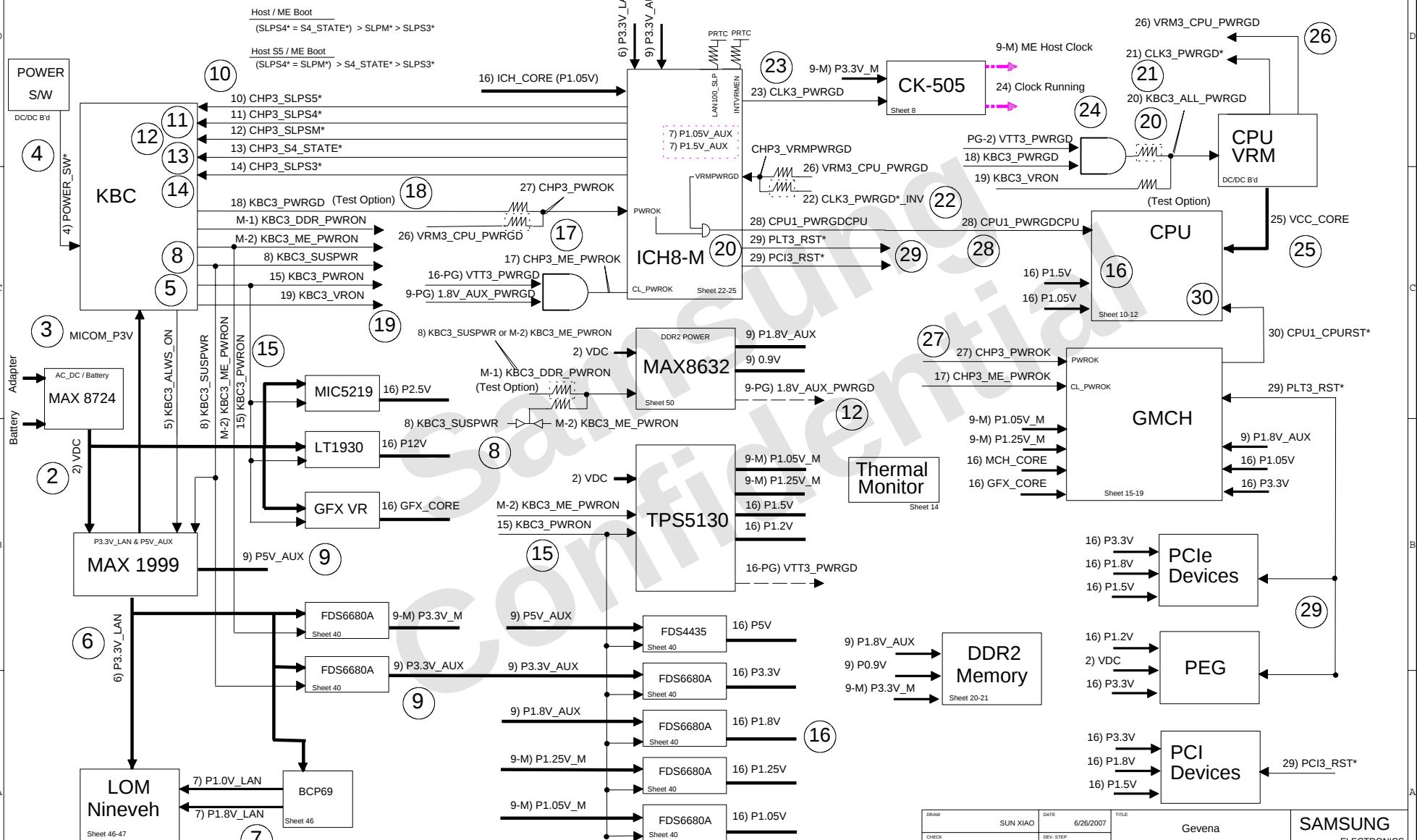
Value by Datasheet/Application notes (Value by measurement)

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva	SAMSUNG
CHECK	WUSHIJIANG	DEV. STEP	PV2			ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0	POWER RAILS	PART NO.	BA41-XXXXX
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	5 OF 58

[illegible]RTC
Battery

1) VCC_RTC (1)
CHP3_RTCRST

Rev. 0.5

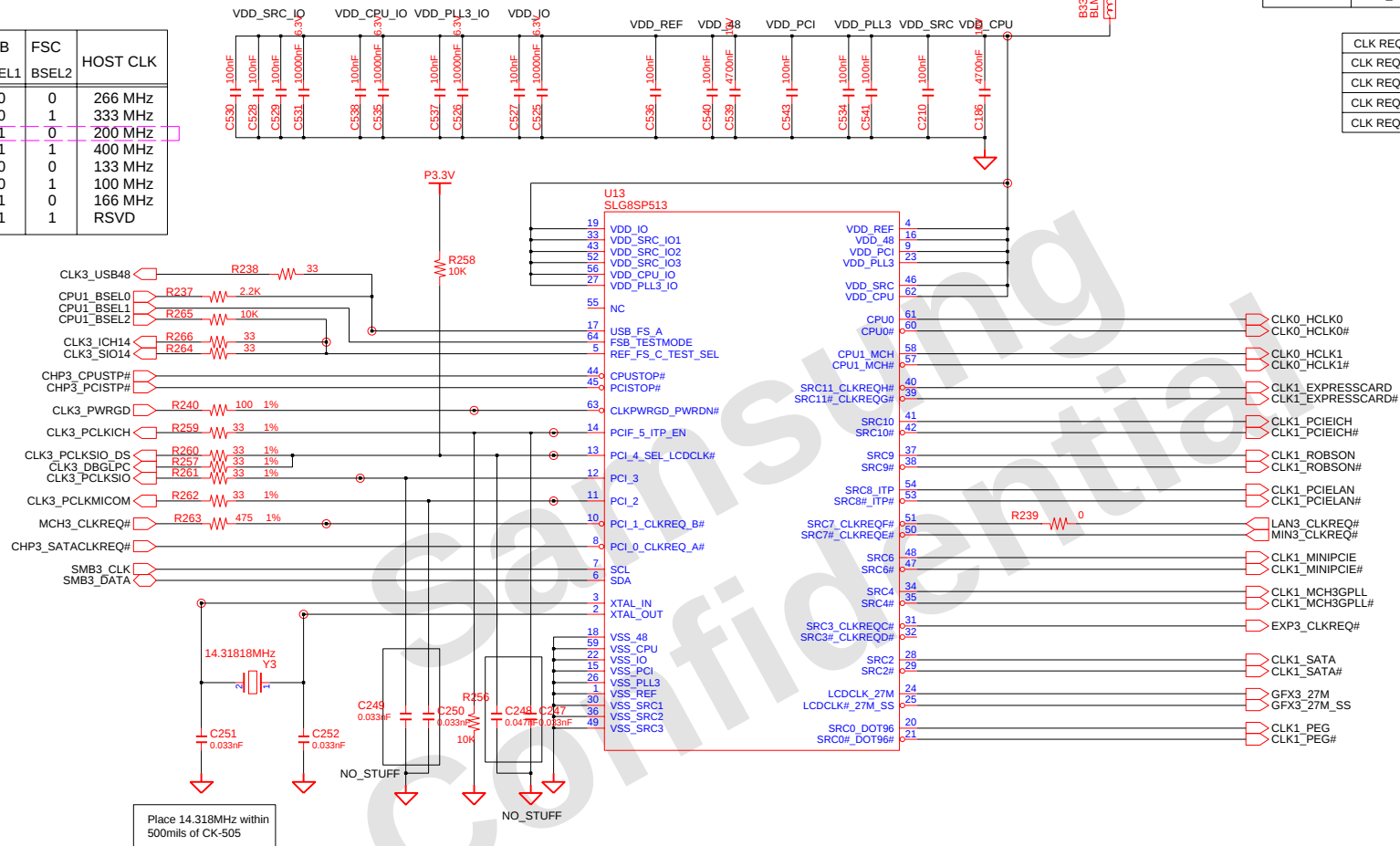


DRAW	SUN XIAO	DATE	6/26/2007	Gevena POWER SEQUENCE October 23, 2007 10:38:02 AM		SAMSUNG ELECTRONICS BA41-XXXXX	
CHECK	WUSHIJIANG	REV-STEP	PV2				
APPROVAL	KEVIN LEE	REV	1.0				
MODULE CODE		LAST EDIT		PAGE 6 OF 58			

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FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

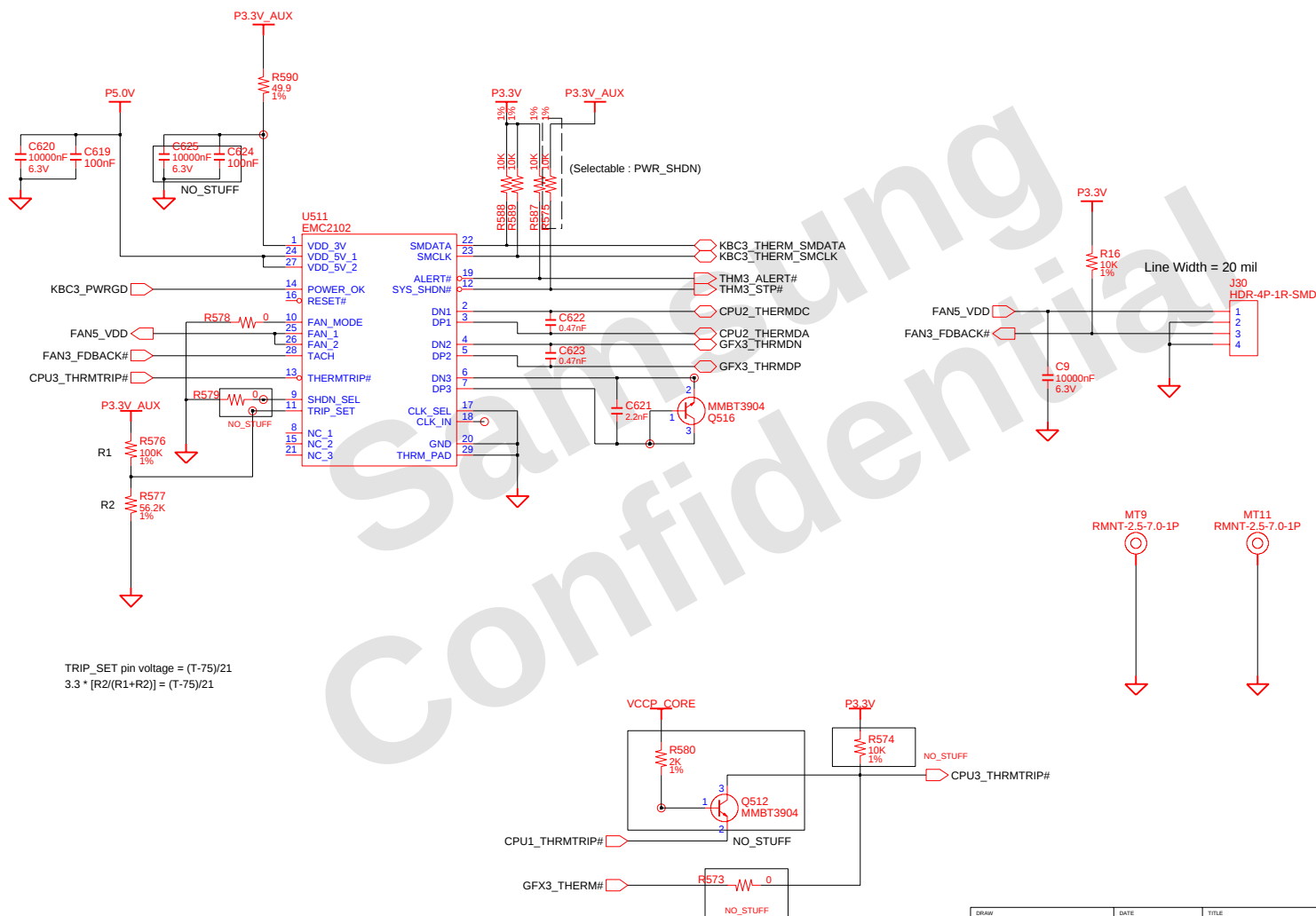


SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	LCDCLK/LCDCLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

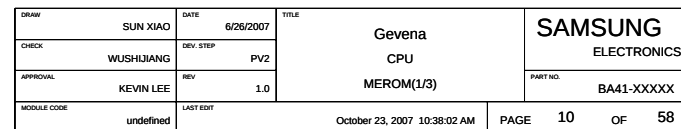
CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXPRESS CARD	SRC8

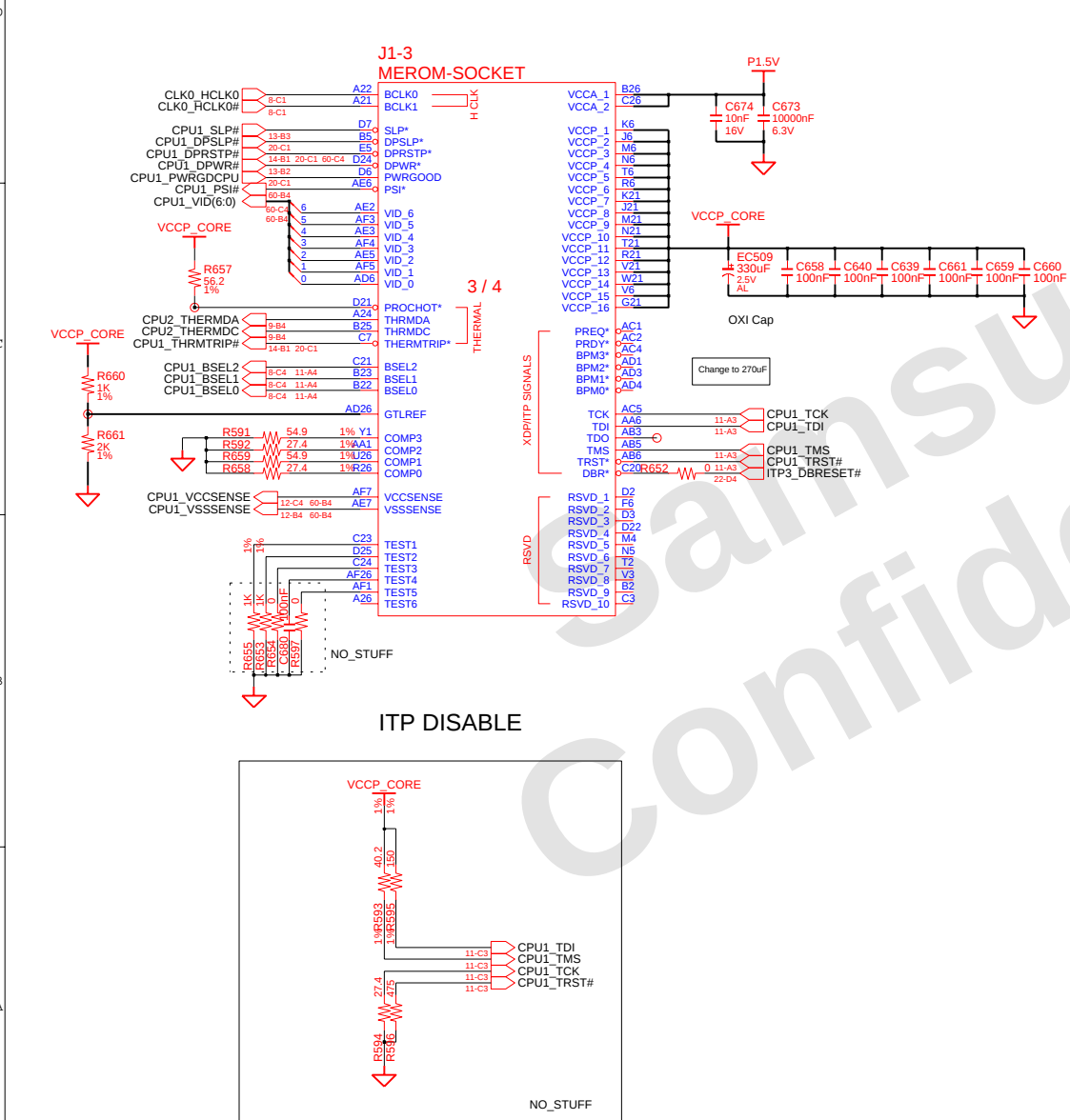
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CHECK	WUSHIJIANG	DEV. STEP	PV2	CLOCK GENERATOR		
APPROVAL	KEVIN LEE	REV	1.0	CK-505		
MODULE CODE		LAST EDIT				
October 23, 2007 10:38:02 AM						PAGE 8 OF 58

THERMAL SENSOR & FAN CONTROL



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APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	9	OF 58





CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6.0)	Voltage	VID(6.0)	Voltage	VID(6.0)	Voltage
0 0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0 0	1.0000 V	1 0 1 0 0 0 0 1	0.4875 V
0 0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 0 1	0.9875 V	1 0 1 0 0 0 1 0	0.4750 V
0 0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 0 1 0	0.9750 V	1 0 1 0 0 0 1 1	0.4625 V
0 0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 0 0	0.9625 V	1 0 1 0 0 1 0 0	0.4500 V
0 0 0 0 0 1 0 0	1.4500 V	0 1 0 1 0 1 0 1	0.9500 V	1 0 1 0 0 1 0 1	0.4375 V
0 0 0 0 0 1 0 1	1.4375 V	0 1 0 1 0 1 1 0	0.9375 V	1 0 1 0 0 1 1 0	0.4250 V
0 0 0 0 0 1 1 0	1.4250 V	0 1 0 1 0 1 1 1	0.9250 V	1 0 1 0 0 1 1 1	0.4125 V
0 0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 0 0 0	0.9125 V	1 0 1 0 1 0 0 0	0.4000 V
0 0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0 0	0.9000 V	1 0 1 0 1 0 0 1	0.3875 V
0 0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 0 1	0.8875 V	1 0 1 0 1 0 1 0	0.3750 V
0 0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 0 1 0	0.8750 V	1 0 1 0 1 0 1 1	0.3625 V
0 0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 0 1 1	0.8625 V	1 0 1 0 1 1 0 0	0.3500 V
0 0 0 0 1 1 0 0	1.3500 V	0 1 1 0 0 1 0 0	0.8500 V	1 0 1 0 1 1 0 1	0.3375 V
0 0 0 0 1 1 0 1	1.3375 V	0 1 1 0 0 1 0 1	0.8375 V	1 0 1 0 1 1 1 0	0.3250 V
0 0 0 0 1 1 1 0	1.3250 V	0 1 1 0 0 1 1 0	0.8250 V	1 0 1 0 1 1 1 1	0.3125 V
0 0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 0 0 0	0.8125 V	1 1 0 0 0 0 0 0	0.3000 V
0 0 0 1 0 0 0 0	1.3000 V	0 1 1 0 1 0 0 1	0.8000 V	1 1 0 0 0 0 0 1	0.2875 V
0 0 0 1 0 0 0 1	1.2875 V	0 1 1 0 1 0 1 0	0.7875 V	1 1 0 0 0 0 1 0	0.2750 V
0 0 0 1 0 0 1 0	1.2750 V	0 1 1 0 1 0 1 1	0.7750 V	1 1 0 0 0 0 1 1	0.2625 V
0 0 0 1 0 0 1 1	1.2625 V	0 1 1 0 1 1 0 0	0.7625 V	1 1 0 0 0 1 0 0	0.2500 V
0 0 0 1 0 1 0 0	1.2500 V	0 1 1 0 1 1 0 1	0.7500 V	1 1 0 0 0 1 0 1	0.2375 V
0 0 0 1 0 1 0 1	1.2375 V	0 1 1 0 1 1 1 0	0.7375 V	1 1 0 0 0 1 1 0	0.2250 V
0 0 0 1 0 1 1 0	1.2250 V	0 1 1 0 1 1 1 1	0.7250 V	1 1 0 0 0 1 1 1	0.2125 V
0 0 0 1 0 1 1 1	1.2125 V	0 1 1 1 0 0 0 0	0.7125 V	1 1 0 0 1 0 0 0	0.2000 V
0 0 0 1 1 0 0 0	1.2000 V	0 1 1 1 0 0 0 1	0.7000 V	1 1 0 0 1 0 0 1	0.1875 V
0 0 0 1 1 0 0 1	1.1875 V	0 1 1 1 0 0 1 0	0.6875 V	1 1 0 0 1 0 1 0	0.1750 V
0 0 0 1 1 0 1 0	1.1750 V	0 1 1 1 0 0 1 1	0.6750 V	1 1 0 0 1 0 1 1	0.1625 V
0 0 0 1 1 0 1 1	1.1625 V	0 1 1 1 0 1 0 0	0.6625 V	1 1 0 0 1 1 0 0	0.1500 V
0 0 0 1 1 1 0 0	1.1500 V	0 1 1 1 0 1 0 1	0.6500 V	1 1 0 0 1 1 0 1	0.1375 V
0 0 0 1 1 1 0 1	1.1375 V	0 1 1 1 0 1 1 0	0.6375 V	1 1 0 0 1 1 1 0	0.1250 V
0 0 0 1 1 1 1 0	1.1250 V	0 1 1 1 0 1 1 1	0.6250 V	1 1 0 0 1 1 1 1	0.1125 V
0 0 0 1 1 1 1 1	1.1125 V	0 1 1 1 1 0 0 0	0.6125 V	1 1 0 1 0 0 0 0	0.1000 V
0 0 1 0 0 0 0 0	1.1000 V	0 1 1 1 1 0 0 1	0.6000 V	1 1 0 1 0 0 0 1	0.0875 V
0 0 1 0 0 0 0 1	1.0875 V	0 1 1 1 1 0 1 0	0.5875 V	1 1 0 1 0 0 0 1	0.0750 V
0 0 1 0 0 0 1 0	1.0750 V	0 1 1 1 1 0 1 1	0.5750 V	1 1 0 1 0 0 1 0	0.0625 V
0 0 1 0 0 0 1 1	1.0625 V	0 1 1 1 1 1 0 0	0.5625 V	1 1 0 1 0 0 1 1	0.0500 V
0 0 1 0 0 1 0 0	1.0500 V	0 1 1 1 1 1 0 1	0.5500 V	1 1 0 1 0 1 0 0	0.0375 V
0 0 1 0 0 1 0 1	1.0375 V	0 1 1 1 1 1 1 0	0.5375 V	1 1 0 1 0 1 0 1	0.0250 V
0 0 1 0 0 1 1 0	1.0250 V	0 1 1 1 1 1 1 1	0.5250 V	1 1 0 1 0 1 1 0	0.0125 V
0 0 1 0 0 1 1 1	1.0125 V	0 1 1 1 1 1 1 1	0.5125 V	1 1 1 1 0 0 0 0	0.0000 V
		1 1 1 1 1 1 1 1	0.5000 V	1 1 1 1 0 0 0 1	0.0000 V
				1 1 1 1 0 0 1 0	0.0000 V
				1 1 1 1 0 0 1 1	0.0000 V
				1 1 1 1 0 1 0 0	0.0000 V
				1 1 1 1 0 1 0 1	0.0000 V
				1 1 1 1 0 1 1 0	0.0000 V
				1 1 1 1 0 1 1 1	0.0000 V
				1 1 1 1 1 0 0 0	0.0000 V
				1 1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1 1	0.0000 V

Active
DPRSLPVR 0
DPRSTP* 1
PSI2* 0 or 1

Deeper Slp
DPRSLPVR 1
DPRSTP* 0
PSI2* 0 or 1

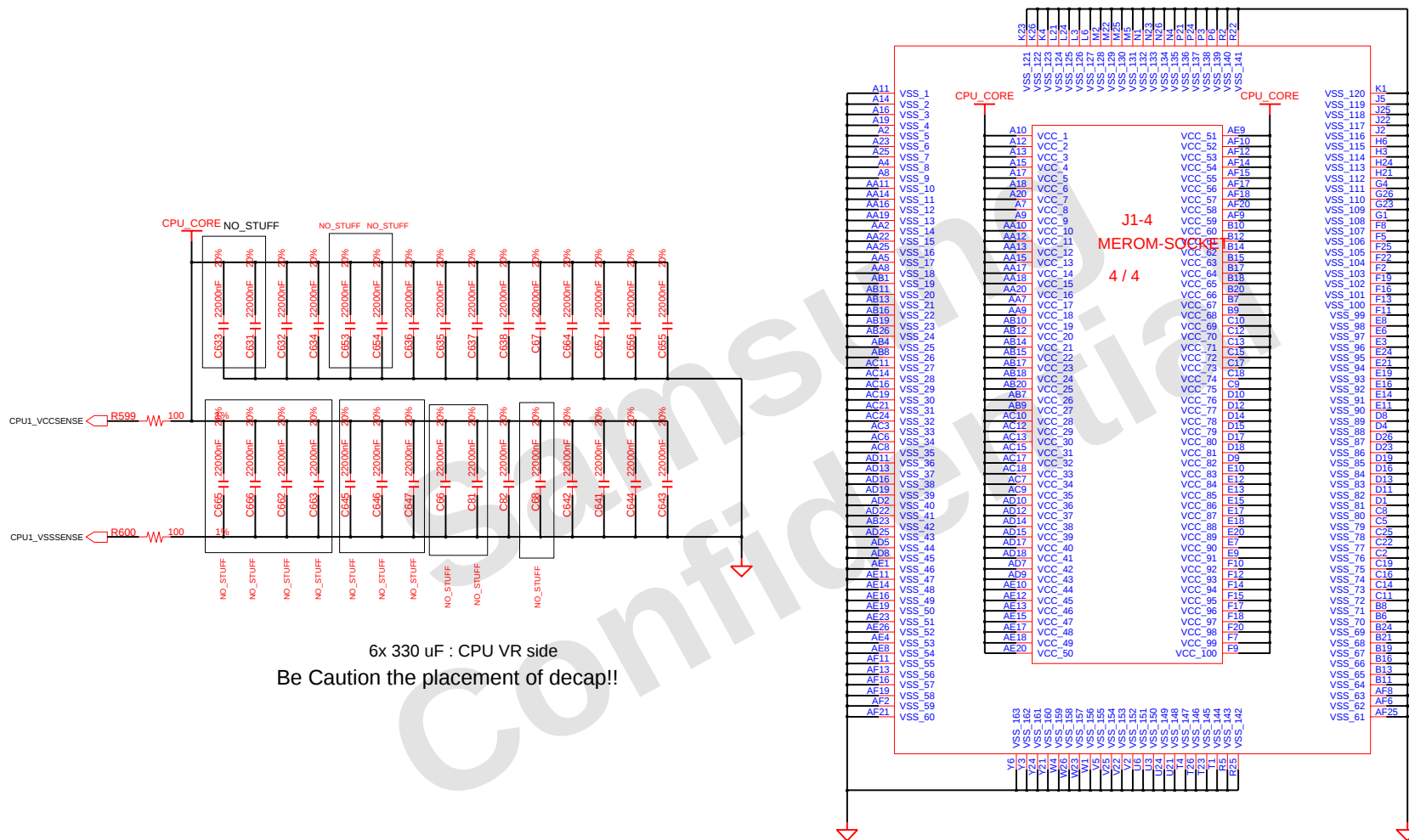
**"1111111": 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

GTREF : Keep the Voltage divider within 0.5" of the first GTREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.



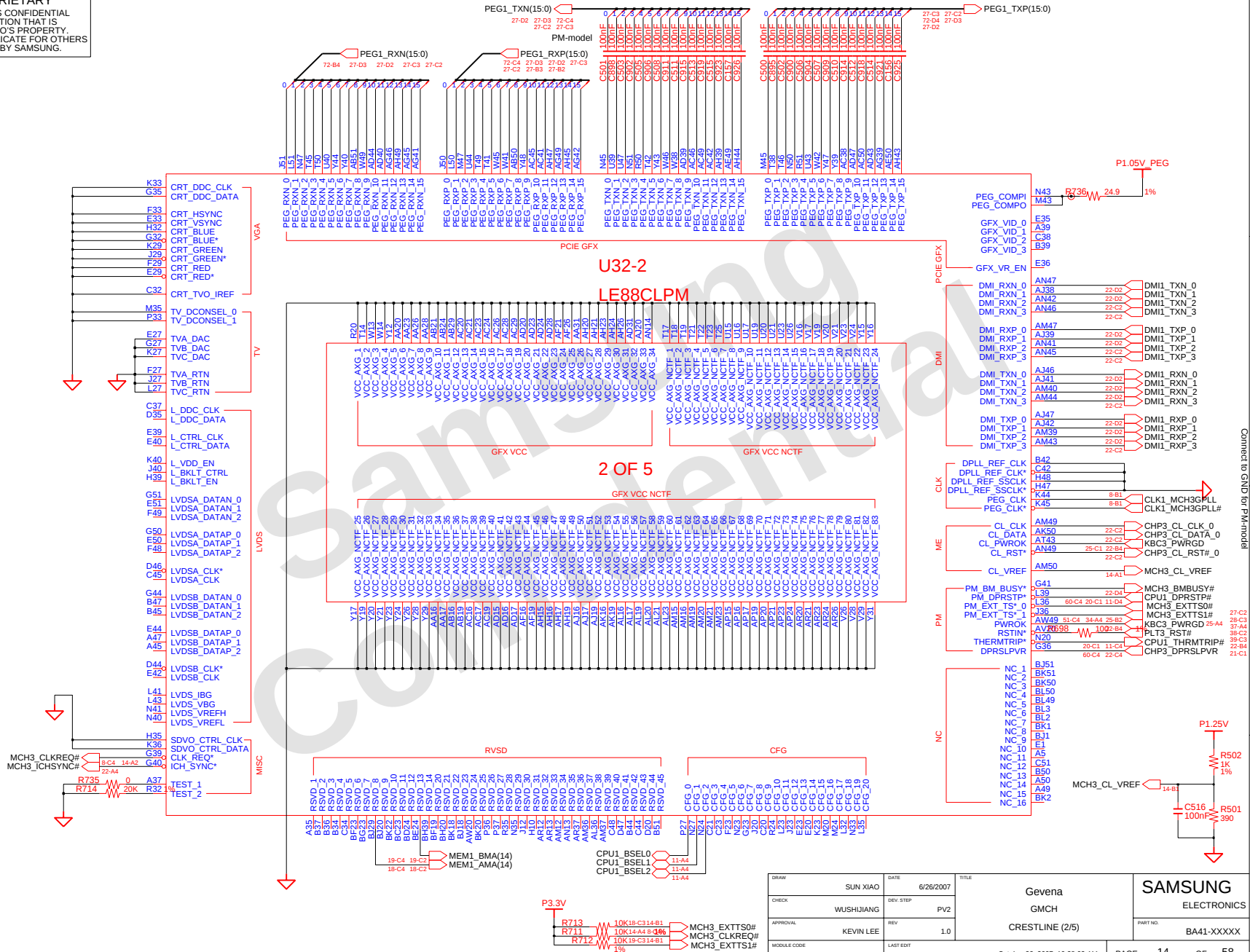
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CHECK	WUSHIJIANG	DEV. STEP	PV2		CPU
APPROVAL	KEVIN LEE	REV	1.0		MEROM(3/3)
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	12 OF 58

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ELECTRONICS

PART NO.
BA41-XXXXX



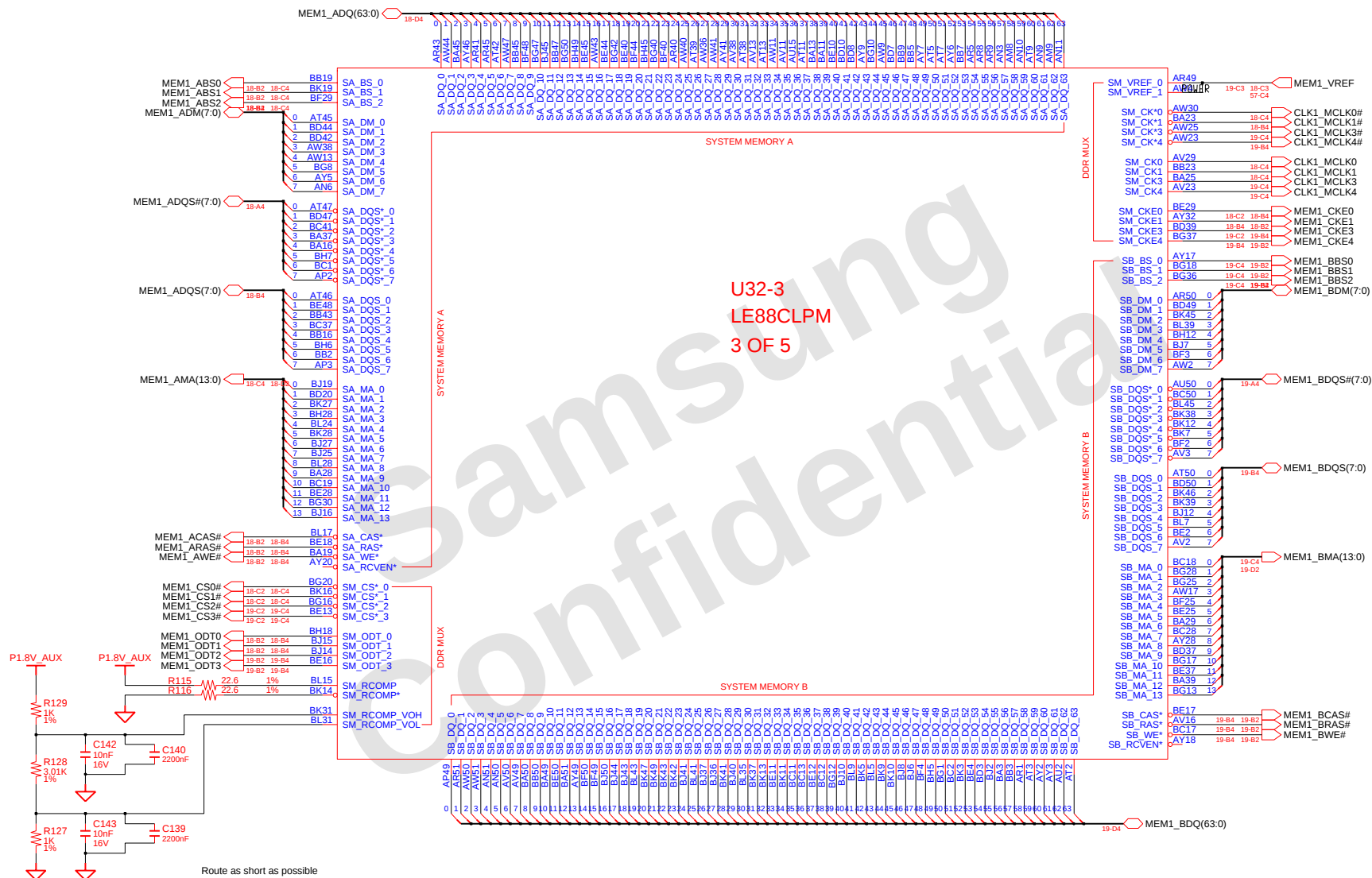
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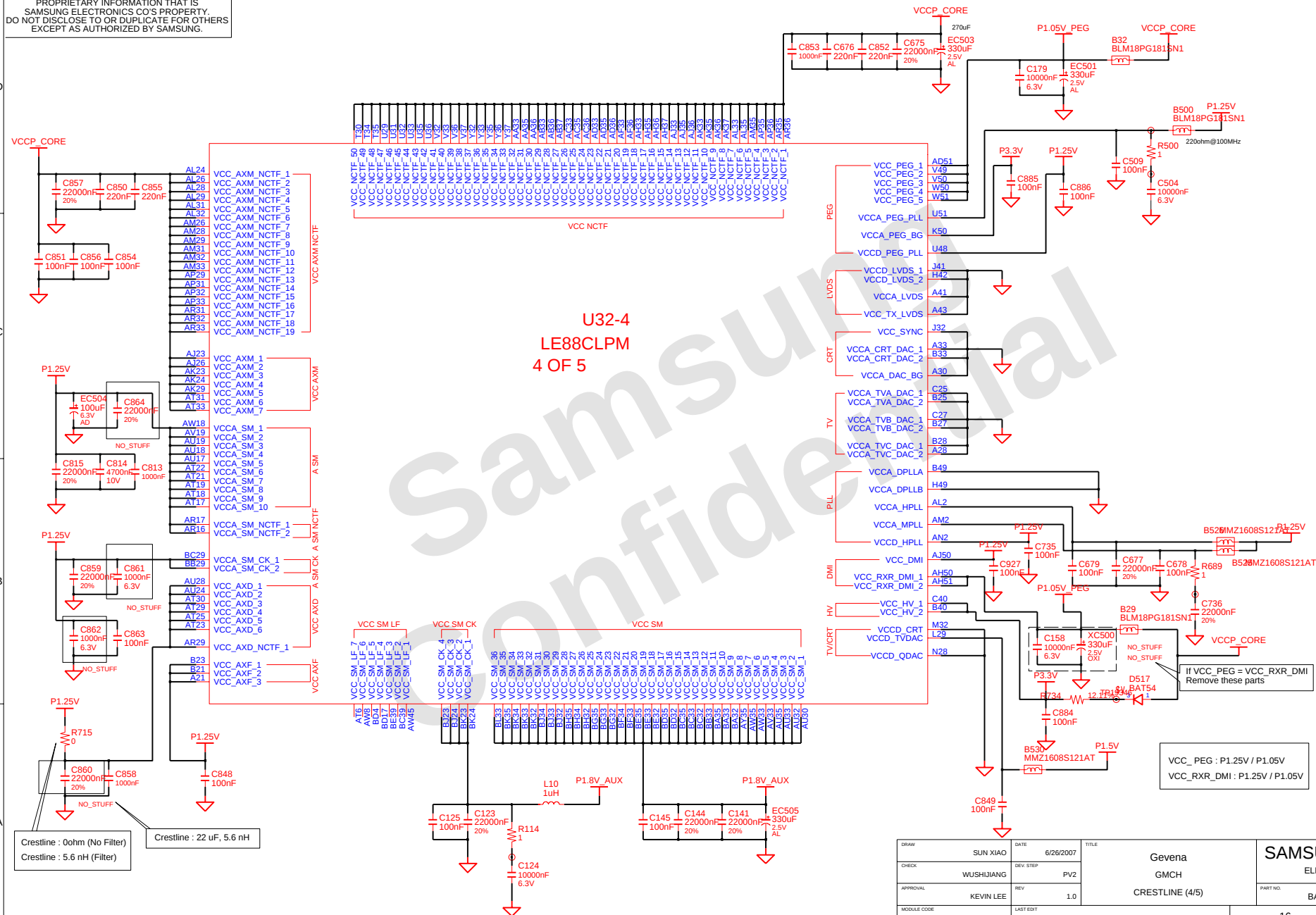
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DRAW	SUN XIAO	DATE	6/26/2007	Gevena GMCH CRESTLINE (3/5)	SAMSUNG ELECTRONICS	
CHECK	WUSHIJIANG	DEV. STEP	PV2			
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MODULE CODE	LAST EDIT				October 23, 2007 10:38:02 AM	PAGE 15 OF 58

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MODULE CODE	LAST EDIT				October 23, 2007 10:38:02 AM	PAGE 16 OF 58

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Array resistors & Single resistors used to improve layout & routing.

ME POWER RAIL UNDER ME ENABLE

P1.8V_AUX

DDR1-1
DDR2-SODIMM-200P-RVS
1/2

P3.3V

MCH3_EXTTSD#
MEM1_VREF

P3.3V

P1.8V_AUX

ME POWER RAIL UNDER ME ENABLE

P1.8V_AUX

NO_STUFF

P0.9V

Place one cap close to every 2 pull-up resistors terminated to P0.9V

NO_STUFF

MEM1_AMA(13:0)

0 RA517-2 1 56
1 RA510-1 1 56
2 RA516-1 1 56
3 RA510-2 1 56
4 RA516-2 1 56
5 RA511-2 1 56
6 RA514-1 1 56
7 RA514-2 1 56
8 RA511-1 1 56
9 RA513-2 1 56
10 RA509-2 1 56
11 RA515-1 1 56
12 RA513-1 1 56
13 RA502-1 1 56

MEM1_AMA(14)

R690 56.2 1%

P0.9V

P0.9V

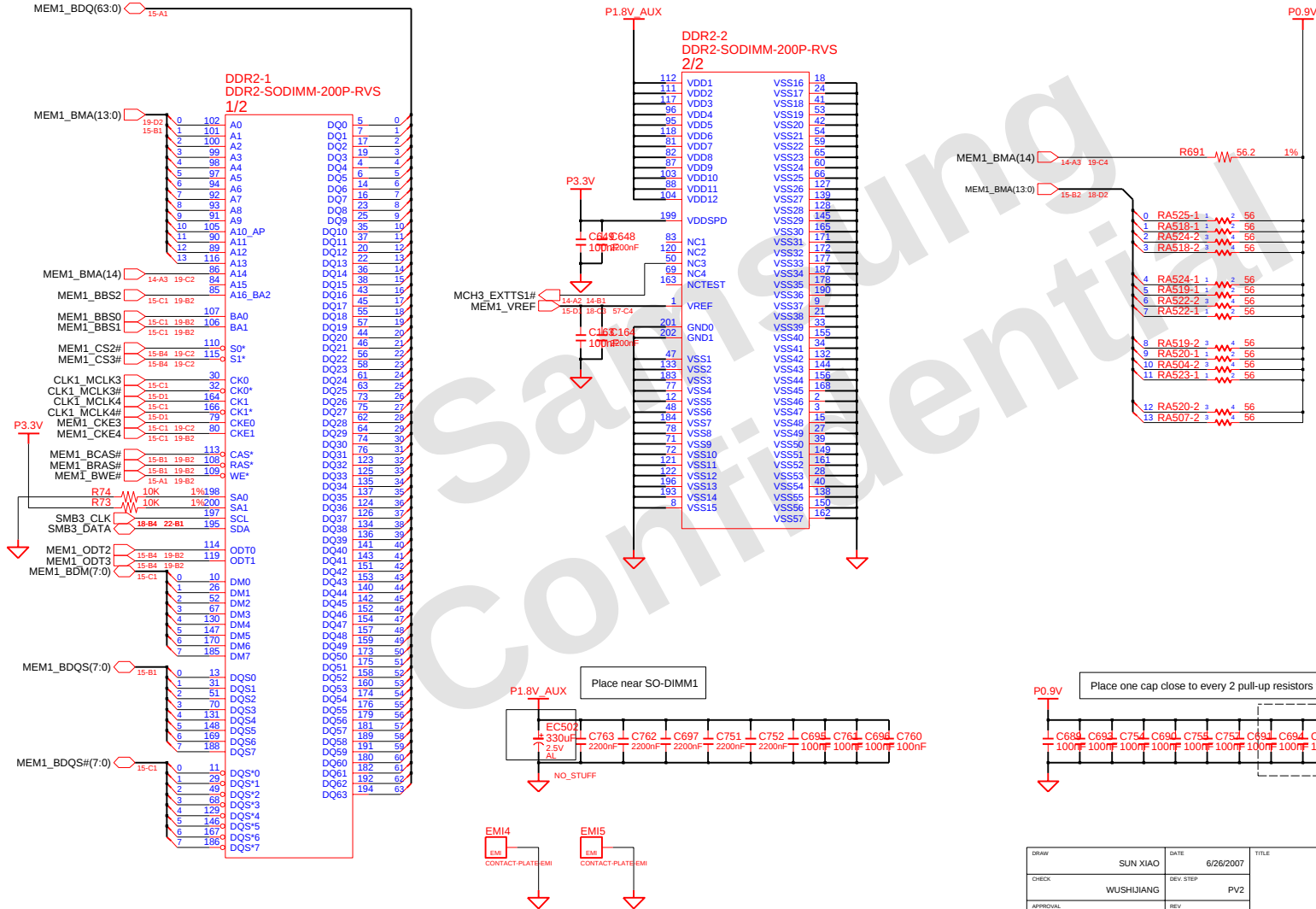
MEM1_CS0# 14-B1 18-C4 RA503-1 1 56
MEM1_CS1# 14-B1 18-C2 RA508-2 3 56
MEM1_CS2# 14-B1 18-C2 RA505-2 3 56
MEM1_CS3# 14-B1 18-C2 RA512-1 1 56
MEM1_CKE0 14-B1 18-C4 RA515-2 3 56
MEM1_CKE1 14-B1 18-C2 RA521-2 3 56
MEM1_CKE2 14-B1 18-C2 RA523-2 3 56
MEM1_ODT0 14-B1 18-B4 RA502-2 3 56
MEM1_ODT1 14-B1 18-B4 RA500-2 3 56
MEM1_ODT2 14-B1 18-B2 RA507-1 1 56
MEM1_ODT3 14-B1 18-B2 RA505-1 1 56
MEM1_ABS0 15-D4 18-C4 RA509-1 1 56
MEM1_ABS1 15-C4 18-C4 RA517-1 1 56
MEM1_ABS2 15-C4 18-C4 RA512-2 3 56
MEM1_ACAS# 15-B4 18-C4 RA501-1 1 56
MEM1_ARAS# 15-B4 18-B4 RA503-2 3 56
MEM1_AWE# 15-B4 18-B4 RA501-2 3 56
MEM1_BBS0 15-D2 18-C2 RA504-1 1 56
MEM1_BBS1 15-C2 18-C2 RA525-2 3 56
MEM1_BBS2 15-C2 18-C2 RA521-1 1 56
MEM1_BCAS# 15-B2 18-C2 RA506-1 1 56
MEM1_BRAS# 15-B2 18-B2 RA508-1 1 56
MEM1_BWE# 15-B2 18-B2 RA506-2 3 56

B

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena SODIMM DDR2 CH A	SAMSUNG ELECTRONICS PART NO. BA41-XXXXX
CHECK	WUSHUJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT				
October 23, 2007 10:38:02 AM						PAGE 18 OF 58

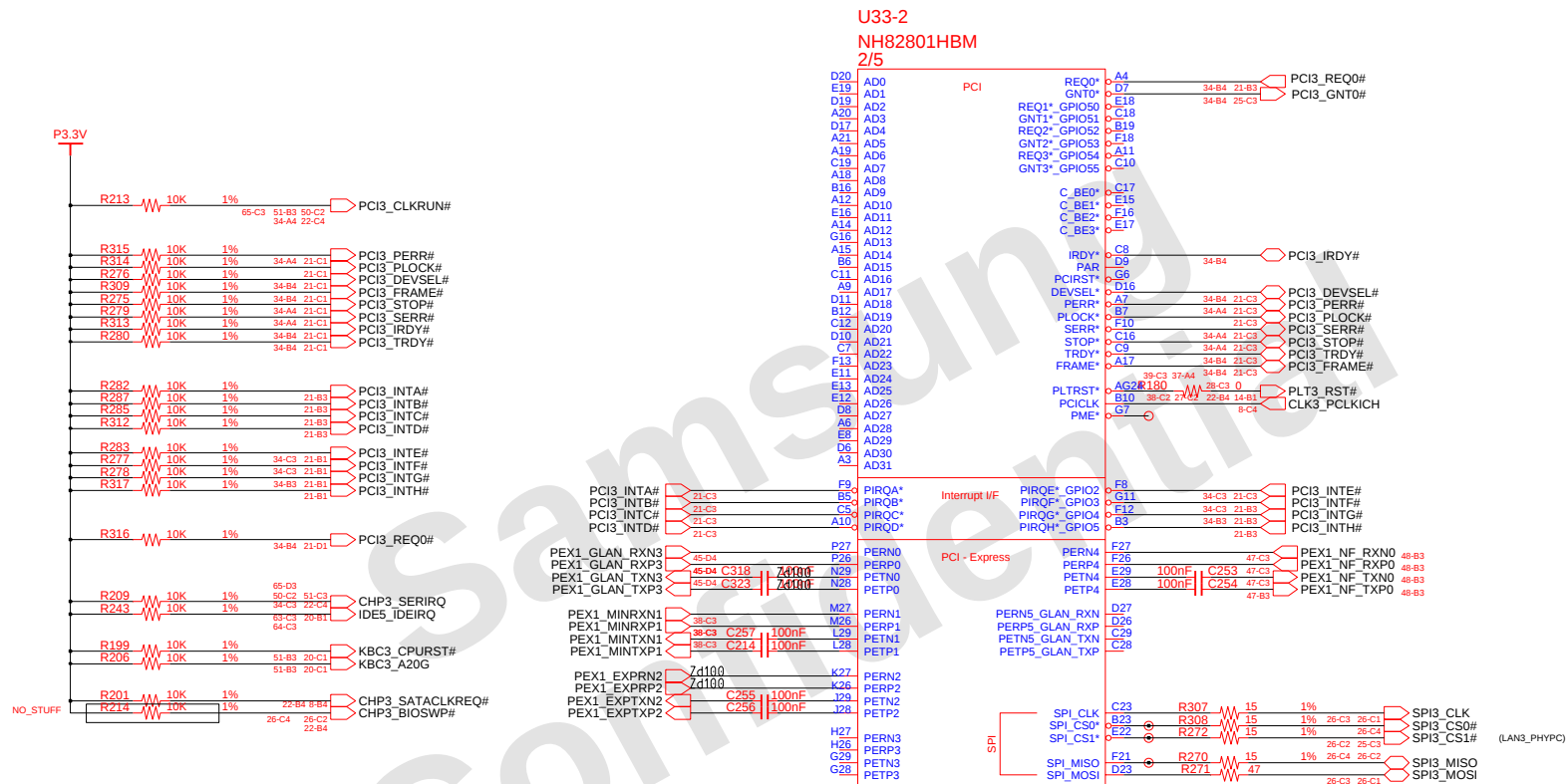
DDR SO-DIMM #1

Array resistors & Single resistors used to improve layout & routing.



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena SODIMM DDR2 CH B	SAMSUNG ELECTRONICS PART NO. BA41-XXXXX
CHECK	WUSHUJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT				
October 23, 2007 10:38:02 AM						PAGE 19 OF 58

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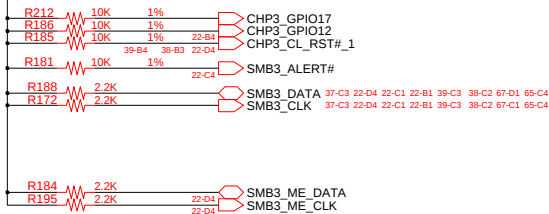


AC caps : PCIE need to be within 250mils of the driver
Resistor for Test : Place Stuffed Option to minimize stubs

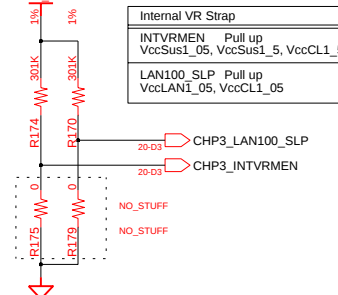
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUJIANG	DEV STEP	PV2		ICH8-M	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0		ICH8-M (2/5)	PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE 21	OF 58

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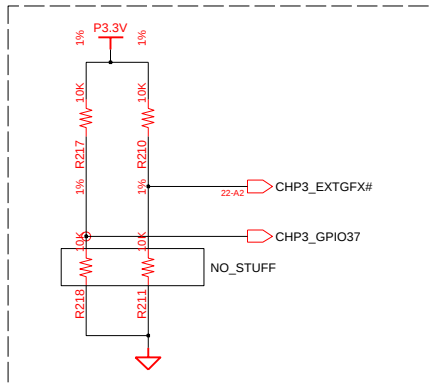
P3.3V_AUX



PRTC_BAT

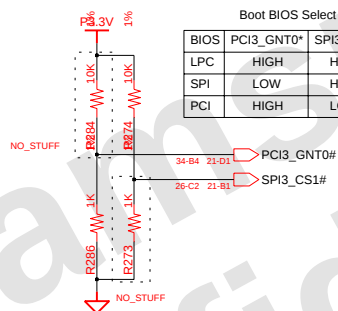


Model Dependent

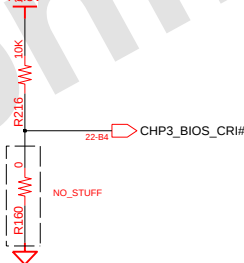


Boot BIOS Select

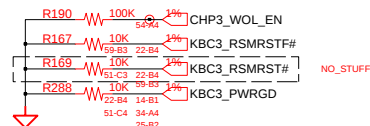
BIOS	PCI3_GNT0*	SPI3_CS1*
LPC	HIGH	HIGH
SPI	LOW	HIGH
PCI	HIGH	LOW



P3.3V

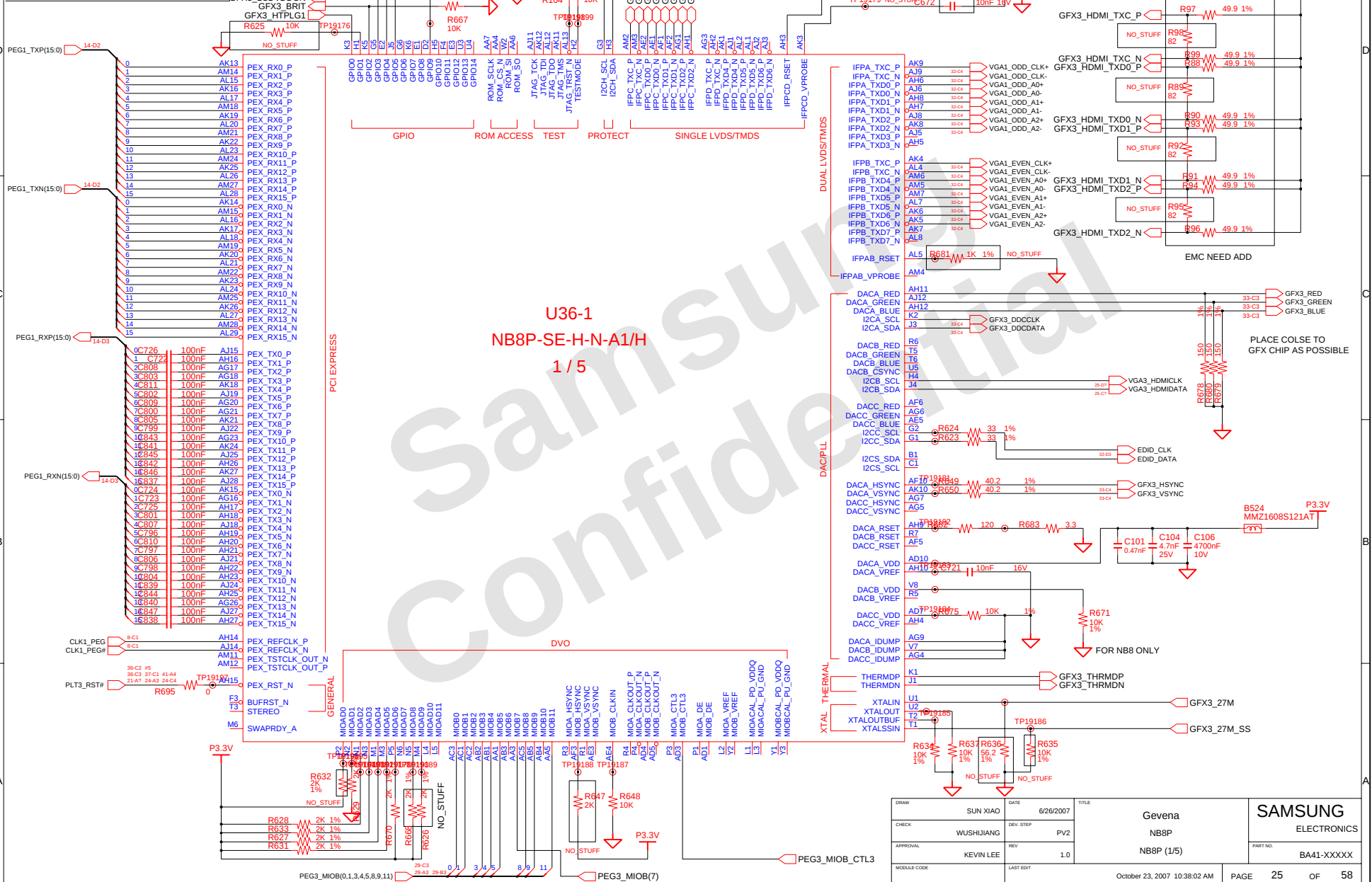


BIOS CRISIS RECOVER STRAP
PLACE NEAR KEYBOARD



DRAW	SUN XIAO	DATE	6/26/2007	TITLE Gevena ICH8-M ICH8-M STAP	SAMSUNG ELECTRONICS
CHECK	WUSHIJIANG	DEV STEP	PV2		
APPROVAL	KEVIN LEE	REV	1.0		
MODULE CODE	LAST EDIT				
				October 23, 2007 10:38:02 AM	PAGE 24 OF 58

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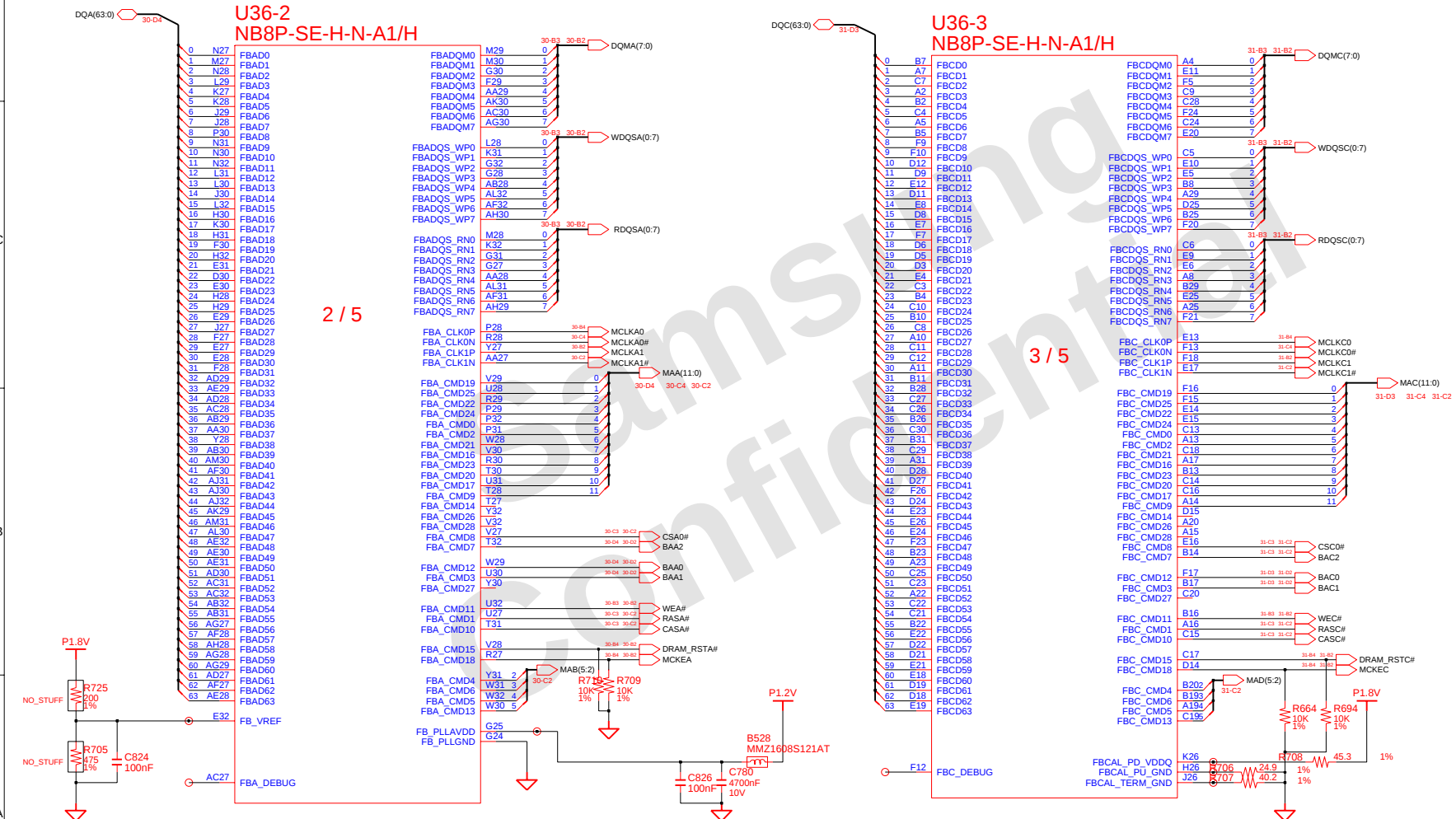


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva
CHECK	WUSHUJIANG	DEV. STEP	PV2		NB8P
APPROVAL	KEVIN LEE	REV	1.0		NB8P (1/5)
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	25 OF 58

SAMSUNG	PART NO.	BA41-XXXXX
ELECTRONICS		

Graphic Memory I/F (Using FBA Channel)

Graphic Memory I/F (Using FBC Channel)



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUJIANG	DEV STEP	PV2		NB8P	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0		NB8P (2/5 3/5)	PART NO.
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM			BA41-XXXXX
				PAGE	26	OF 58

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U36-4
NB8P-SE-H-N-A1/H
4 / 5

Pin List:

Pin	Description	ACTIVATE
GPIO(0)	HDMI DETECT	HIGH
GPIO(1)	TV DETECT	NC
GPIO(2)	PWM BRIGHTNESS CONTROL	HIGH
GPIO(3)	LCD VDD On ENABLE	HIGH
GPIO(4)	LCD Backlight On/OFF	HIGH
GPIO(5)	GPU Voltage ID0	HIGH=1.0V, LOW=1.1V
GPIO(6)	GPU Voltage ID1	NC
GPIO(7)	GPU Voltage ID2	NC
GPIO(8)	Thermal diode Alert	LOW
GPIO(9)	Fan Control	NC
GPIO(10)	TBD	NC
GPIO(11)	HDTV enable	HIGH
GPIO(12)	HDTV DET	NC

Component Values:

- EC511: 3300uF, 2.5V, AL
- C698: 10000nF, 10V
- C882: 10000nF, 10V
- C770: 4700nF, 6.3V
- C880: 4700nF, 6.3V
- C699: 100nF
- C771: 100nF
- C831: 100nF
- C700: 22nF, 25V
- C820: 22nF, 25V
- C825: 22nF, 25V
- C822: 22nF, 25V
- C821: 4.7nF, 25V
- C823: 4.7nF, 25V
- C828: 4.7nF, 25V
- C829: 4.7nF, 25V
- C834: 4.7nF, 25V
- C836: 4.7nF, 25V

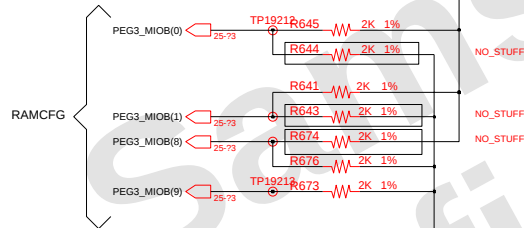
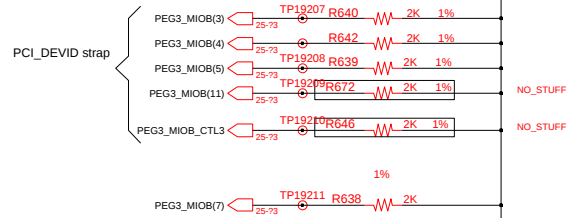
Pin Connections:

- FBVDD_1 to FBVDD_15
- FBVDD_17 to FBVDD_20
- FBVDDQ_1 to FBVDDQ_24
- FBVTT_1 to FBVTT_18
- FBVTT_19 to FBVTT_24
- FBVTT_25 to FBVTT_30
- FBVTT_31 to FBVTT_36
- FBVTT_37 to FBVTT_42
- FBVTT_43 to FBVTT_48
- FBVTT_49 to FBVTT_54
- FBVTT_55 to FBVTT_60
- FBVTT_61 to FBVTT_66
- FBVTT_67 to FBVTT_72
- FBVTT_73 to FBVTT_78
- FBVTT_79 to FBVTT_84
- FBVTT_85 to FBVTT_90
- FBVTT_91 to FBVTT_96
- FBVTT_97 to FBVTT_102
- FBVTT_103 to FBVTT_108
- FBVTT_109 to FBVTT_114
- FBVTT_115 to FBVTT_120
- FBVTT_121 to FBVTT_126
- FBVTT_127 to FBVTT_132
- FBVTT_133 to FBVTT_138
- FBVTT_139 to FBVTT_144
- FBVTT_145 to FBVTT_150
- FBVTT_151 to FBVTT_156
- FBVTT_157 to FBVTT_162
- FBVTT_163 to FBVTT_168
- FBVTT_169 to FBVTT_174
- FBVTT_175 to FBVTT_180
- FBVTT_181 to FBVTT_186
- FBVTT_187 to FBVTT_192
- FBVTT_193 to FBVTT_198
- FBVTT_199 to FBVTT_204
- FBVTT_205 to FBVTT_210
- FBVTT_211 to FBVTT_216
- FBVTT_217 to FBVTT_222
- FBVTT_223 to FBVTT_228
- FBVTT_229 to FBVTT_234
- FBVTT_235 to FBVTT_240
- FBVTT_241 to FBVTT_246
- FBVTT_247 to FBVTT_252
- FBVTT_253 to FBVTT_258
- FBVTT_259 to FBVTT_264
- FBVTT_265 to FBVTT_270
- FBVTT_271 to FBVTT_276
- FBVTT_277 to FBVTT_282
- FBVTT_283 to FBVTT_288
- FBVTT_289 to FBVTT_294
- FBVTT_295 to FBVTT_300
- FBVTT_301 to FBVTT_306
- FBVTT_307 to FBVTT_312
- FBVTT_313 to FBVTT_318
- FBVTT_319 to FBVTT_324
- FBVTT_325 to FBVTT_330
- FBVTT_331 to FBVTT_336
- FBVTT_337 to FBVTT_342
- FBVTT_343 to FBVTT_348
- FBVTT_349 to FBVTT_354
- FBVTT_355 to FBVTT_360
- FBVTT_361 to FBVTT_366
- FBVTT_367 to FBVTT_372
- FBVTT_373 to FBVTT_378
- FBVTT_379 to FBVTT_384
- FBVTT_385 to FBVTT_390
- FBVTT_391 to FBVTT_396
- FBVTT_397 to FBVTT_402
- FBVTT_403 to FBVTT_408
- FBVTT_409 to FBVTT_414
- FBVTT_415 to FBVTT_420
- FBVTT_421 to FBVTT_426
- FBVTT_427 to FBVTT_432
- FBVTT_433 to FBVTT_438
- FBVTT_439 to FBVTT_444
- FBVTT_445 to FBVTT_450
- FBVTT_451 to FBVTT_456
- FBVTT_457 to FBVTT_462
- FBVTT_463 to FBVTT_468
- FBVTT_469 to FBVTT_474
- FBVTT_475 to FBVTT_480
- FBVTT_481 to FBVTT_486
- FBVTT_487 to FBVTT_492
- FBVTT_493 to FBVTT_498
- FBVTT_499 to FBVTT_504
- FBVTT_505 to FBVTT_510
- FBVTT_511 to FBVTT_516
- FBVTT_517 to FBVTT_522
- FBVTT_523 to FBVTT_528
- FBVTT_529 to FBVTT_534
- FBVTT_535 to FBVTT_540
- FBVTT_541 to FBVTT_546
- FBVTT_547 to FBVTT_552
- FBVTT_553 to FBVTT_558
- FBVTT_559 to FBVTT_564
- FBVTT_565 to FBVTT_570
- FBVTT_571 to FBVTT_576
- FBVTT_577 to FBVTT_582
- FBVTT_583 to FBVTT_588
- FBVTT_589 to FBVTT_594
- FBVTT_595 to FBVTT_600
- FBVTT_601 to FBVTT_606
- FBVTT_607 to FBVTT_612
- FBVTT_613 to FBVTT_618
- FBVTT_619 to FBVTT_624
- FBVTT_625 to FBVTT_630
- FBVTT_631 to FBVTT_636
- FBVTT_637 to FBVTT_642
- FBVTT_643 to FBVTT_648
- FBVTT_649 to FBVTT_654
- FBVTT_655 to FBVTT_660
- FBVTT_661 to FBVTT_666
- FBVTT_667 to FBVTT_672
- FBVTT_673 to FBVTT_678
- FBVTT_679 to FBVTT_684
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- FBVTT_691 to FBVTT_696
- FBVTT_697 to FBVTT_702
- FBVTT_703 to FBVTT_708
- FBVTT_709 to FBVTT_714
- FBVTT_715 to FBVTT_720
- FBVTT_721 to FBVTT_726
- FBVTT_727 to FBVTT_732
- FBVTT_733 to FBVTT_738
- FBVTT_739 to FBVTT_744
- FBVTT_745 to FBVTT_750
- FBVTT_751 to FBVTT_756
- FBVTT_757 to FBVTT_762
- FBVTT_763 to FBVTT_768
- FBVTT_769 to FBVTT_774
- FBVTT_775 to FBVTT_780
- FBVTT_781 to FBVTT_786
- FBVTT_787 to FBVTT_792
- FBVTT_793 to FBVTT_798
- FBVTT_799 to FBVTT_804
- FBVTT_805 to FBVTT_810
- FBVTT_811 to FBVTT_816
- FBVTT_817 to FBVTT_822
- FBVTT_823 to FBVTT_828
- FBVTT_829 to FBVTT_834
- FBVTT_835 to FBVTT_840
- FBVTT_841 to FBVTT_846
- FBVTT_847 to FBVTT_852
- FBVTT_853 to FBVTT_858
- FBVTT_859 to FBVTT_864
- FBVTT_865 to FBVTT_870
- FBVTT_871 to FBVTT_876
- FBVTT_877 to FBVTT_882
- FBVTT_883 to FBVTT_888
- FBVTT_889 to FBVTT_894
- FBVTT_895 to FBVTT_900
- FBVTT_901 to FBVTT_906
- FBVTT_907 to FBVTT_912
- FBVTT_913 to FBVTT_918
- FBVTT_919 to FBVTT_924
- FBVTT_925 to FBVTT_930
- FBVTT_931 to FBVTT_936
- FBVTT_937 to FBVTT_942
- FBVTT_943 to FBVTT_948
- FBVTT_949 to FBVTT_954
- FBVTT

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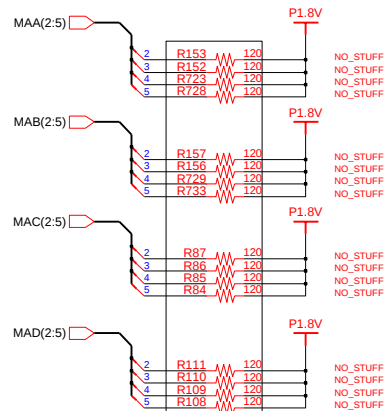
PCI_DEVID strap

	R646	R672	R640	R639	R642
NB8P-SE	NO_STUFF	NO_STUFF	STUFF	NO_STUFF	STUFF
NB8M-GS	0	0	1	1	1
	NO_STUFF	NO_STUFF	STUFF	STUFF	STUFF
	0	0	1	1	1



RAMCFG

	R674	R676	R641	R643
SS 256Mbit	STUFF	NO_STUFF	STUFF	NO_STUFF
IF 256Mbit	STUFF	NO_STUFF	NO_STUFF	STUFF
SS 512Mbit	NO_STUFF	STUFF	STUFF	NO_STUFF
IF 512Mbit	NO_STUFF	STUFF	NO_STUFF	STUFF



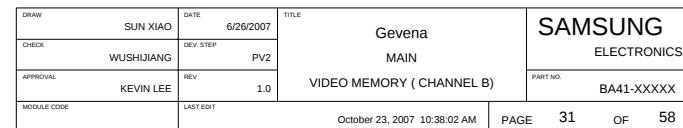
Straps	Pin # (Rev.A02)	Descriptions
SUB_VENDOR	MIOAD(1)	0 : No BIOS 1 : Read from BIOS
RAMCFG(3:0) [9,8,1,0]	MIOB(9) MIOB(8) MIOB(1) MIOB(0)	0111 : SAMSUNG GDDR3 256Mbit 0101 : INFINEON GDDR3 256Mbit 0011 : SAMSUNG GDDR3 512Mbit 0001 : INFINEON GDDR3 512Mbit
CRYSTAL(1:0)	MIOB(2) MIOB(6)	01 : 14.318 MHz 10 : 27 MHz 11 : Unknown 00 : 13.5 MHz
TV_MODE(1:0)	MIOAD(7) MIOAD(10)	00 : SECAM 01 : NTSC 10 : PAL 11 : CRT
PCI_DEVID(4:0) [CTL3,11,3,5,4]	MIOB_CTL(3) MIOB(11) MIOB(3) MIOB(5) MIOB(4)	NB8M-GS: 00111 NB8M-SE: 01000 NB8M-GT: 00110 NB8P-GS: 00111 NB8P-SE: 00101 NB8P-GT: 01000
ROM_TYPE(1:0)	MIOB(10) MIOBVSYN	NO ROM(NC)
USER STRAP	MIOAD(2:5)	EDID
GPIO(12:0)	Sheet 25	Refer to Sheet 25

Test Options for GPIO should be updated..

Samsung		Infineon	
256Mbit	512Mbit	256Mbit	512Mbit
K4J55323QG (1.2/1.4/1.6/2.0) K4J55323QF (1.4/1.6/2.0)	K4J52324QC (1.2/1.4/1.6/2.0)	HYB18H256321AF120(2.0) HYB18H256321AF16(1.6) HYB18H256324AF-20(2.0) HYB18H256321AF-14(1.4) HYB18H256321AF-12(1.2)	HYB18H512321AF120(2.0) HYB18H512321AF16(1.6) HYB18H512324AF-20(1.6) HYB18H512321AF-14(1.4) HYB18H512321AF-12(1.2)
8M*32BIT	16M*32BIT	8M*32BIT	16M*32BIT

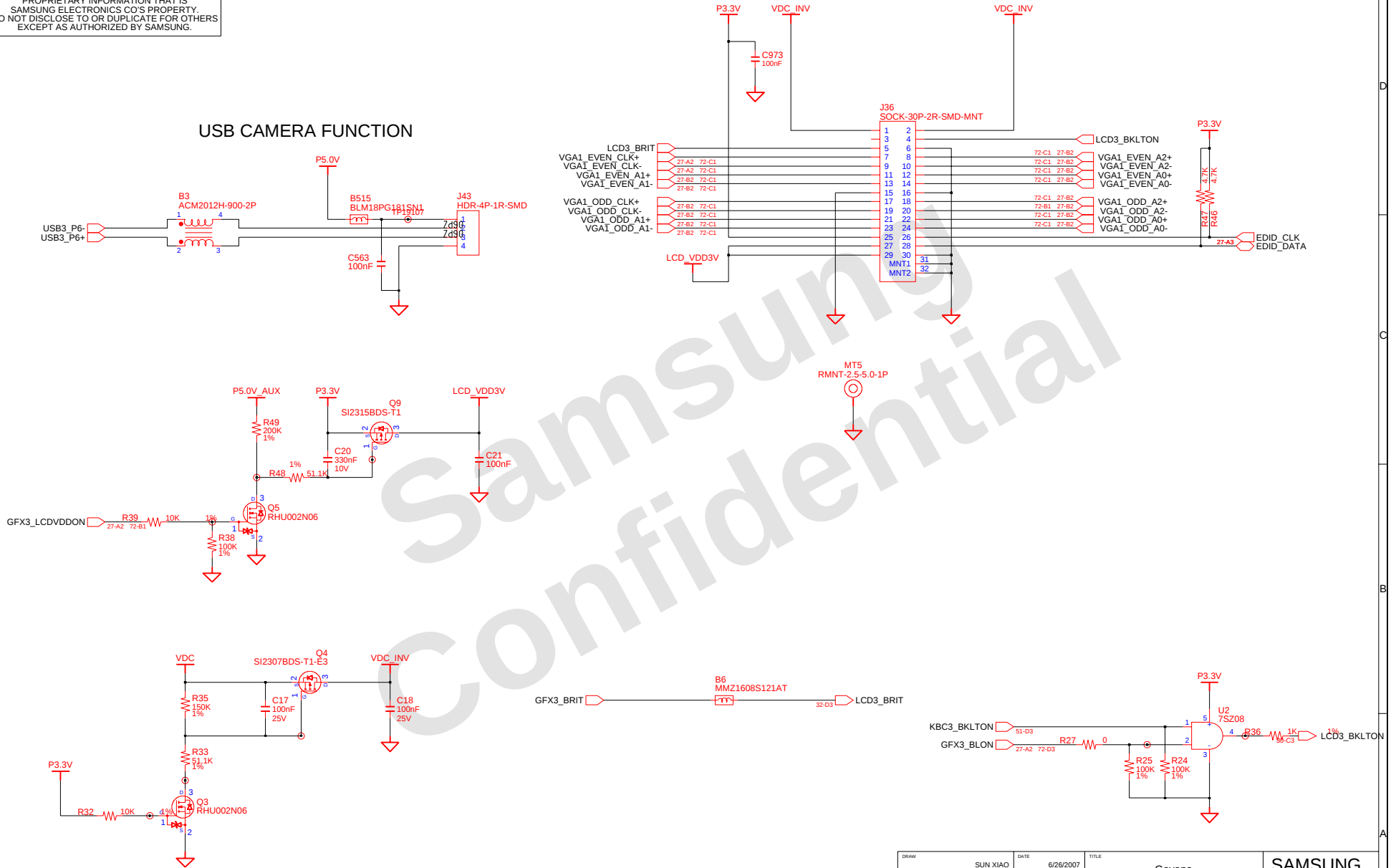
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2		NB8P	
APPROVAL	KEVIN LEE	REV	1.0		NB8P STRAP	
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM			
PAGE 29 OF 58						PART NO. BA41-XXXXX

Video Memory (C Channel)



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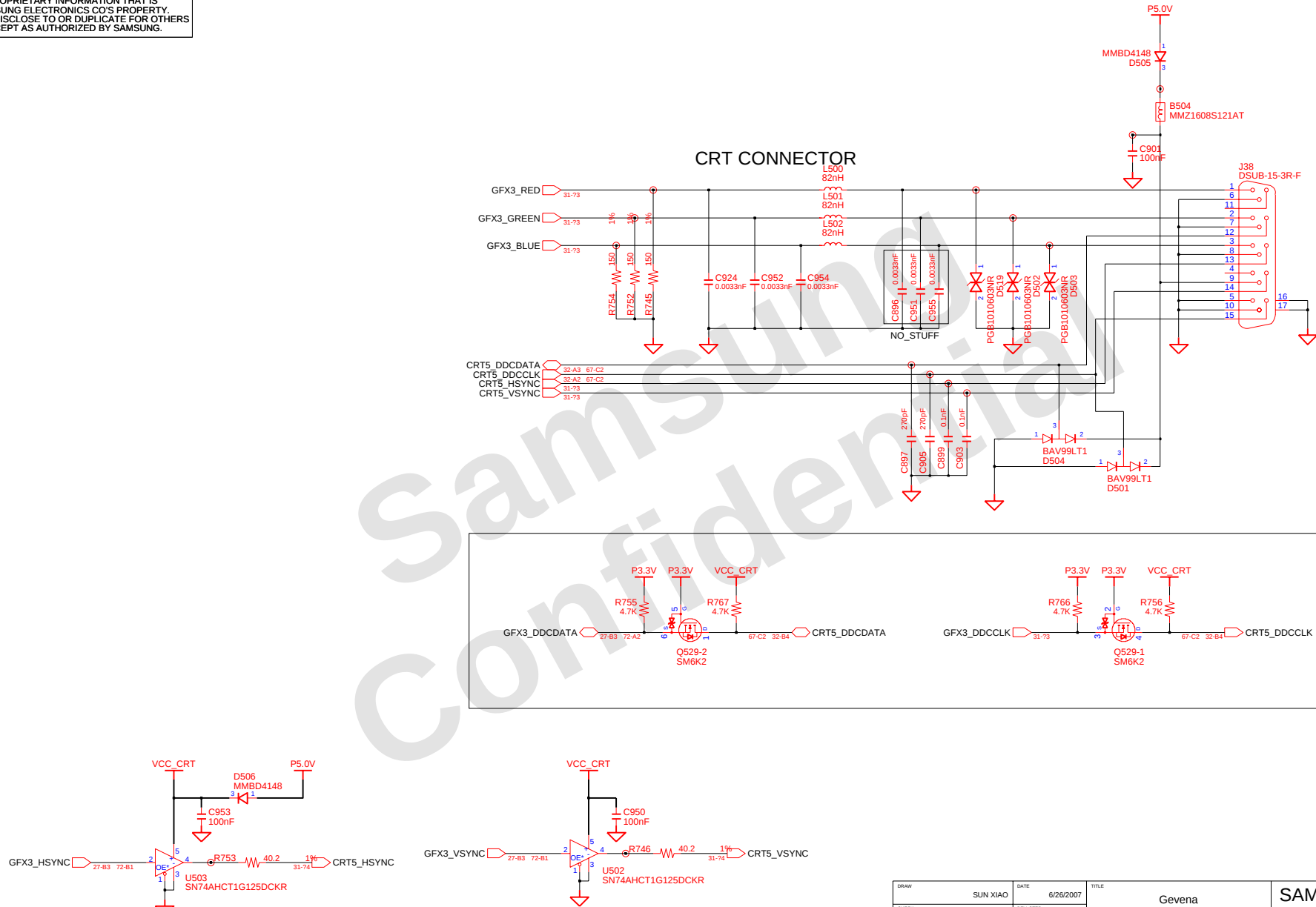
USB CAMERA FUNCTION



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS PART NO. BA41-XXXXX
CHECK	WUSHUJIANG	DEV STEP	PV2		LCD CONNECTER & SPEED SPECTRUM	
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT				
October 23, 2007 10:38:02 AM						PAGE 32 OF 58

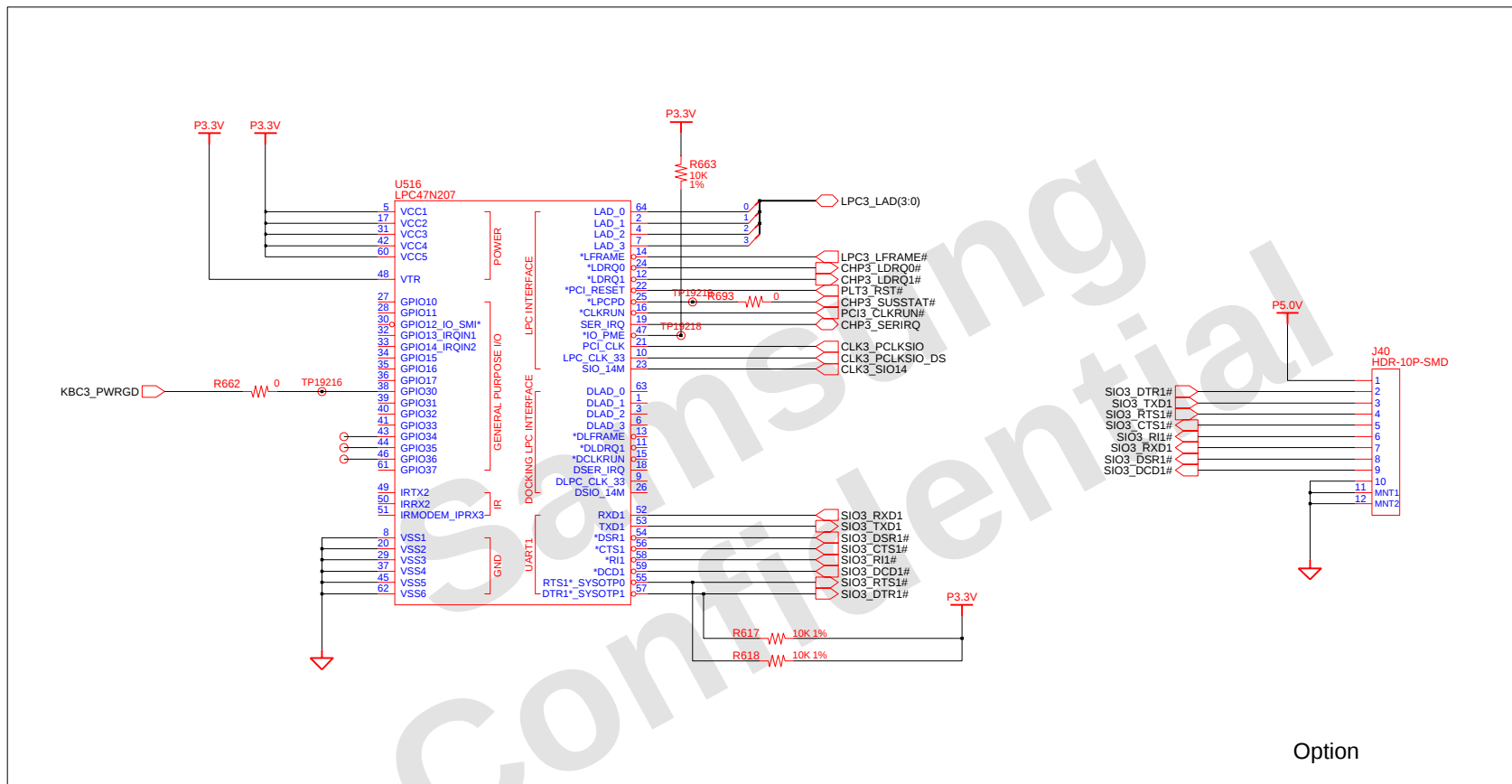
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CRT CONNECTOR



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena MIAN CRT PORT	SAMSUNG ELECTRONICS PART NO. BA41-XXXXX
CHECK	WUSHIJIANG	DEV STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT				
October 23, 2007 10:38:02 AM						PAGE 33 OF 58

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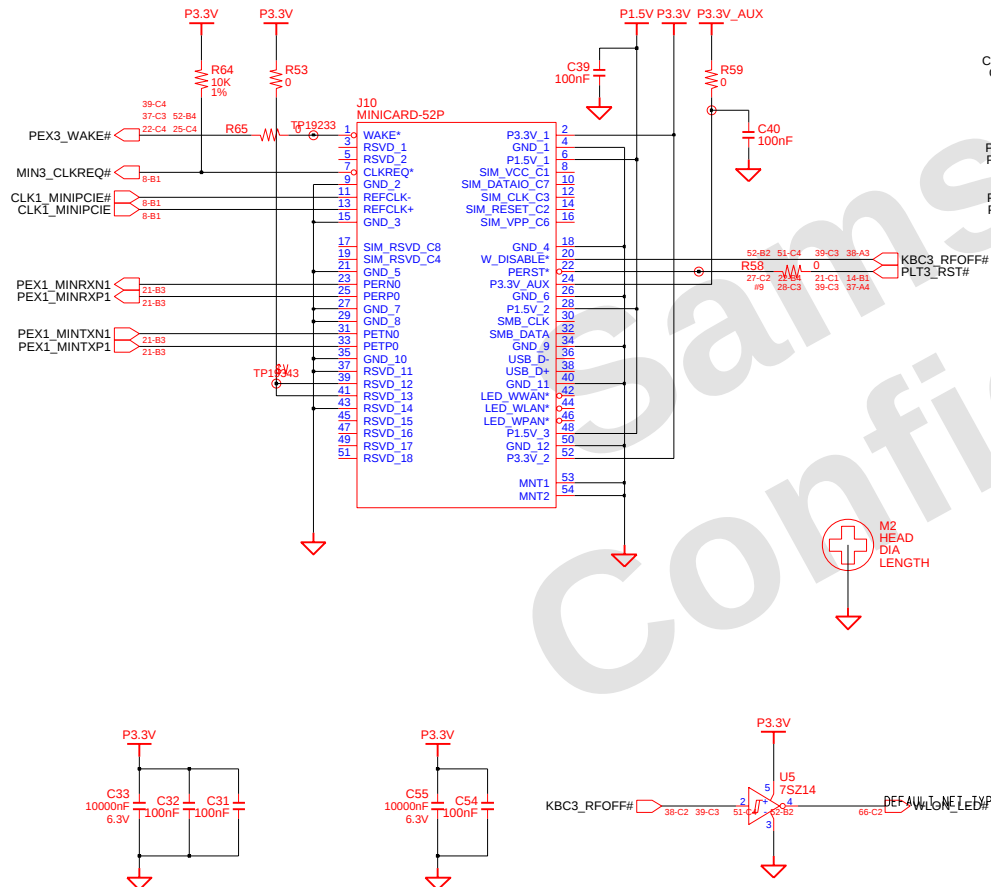
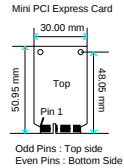


Option

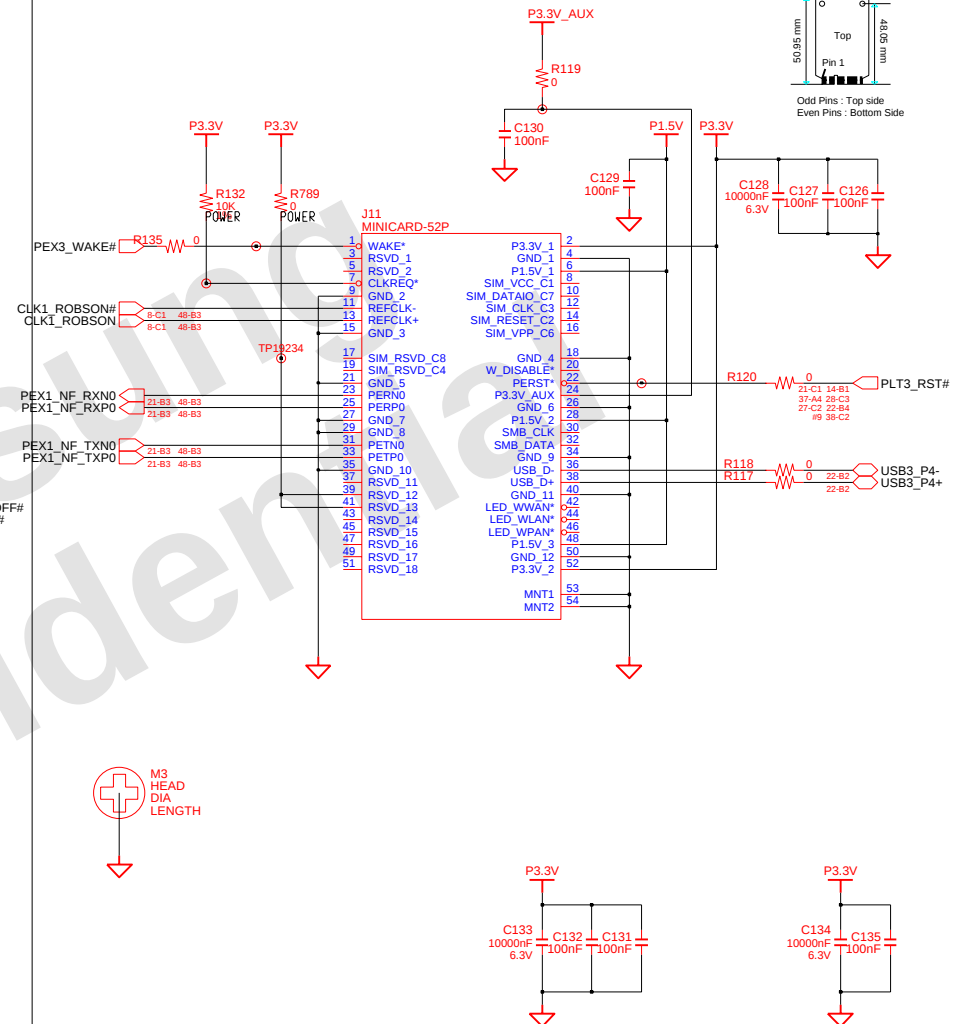
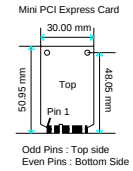
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUJIANG	DEV. STEP	PV2		SIO CHIPSET	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0			PART NO. BA41-
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	34	OF 68

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Mini Card



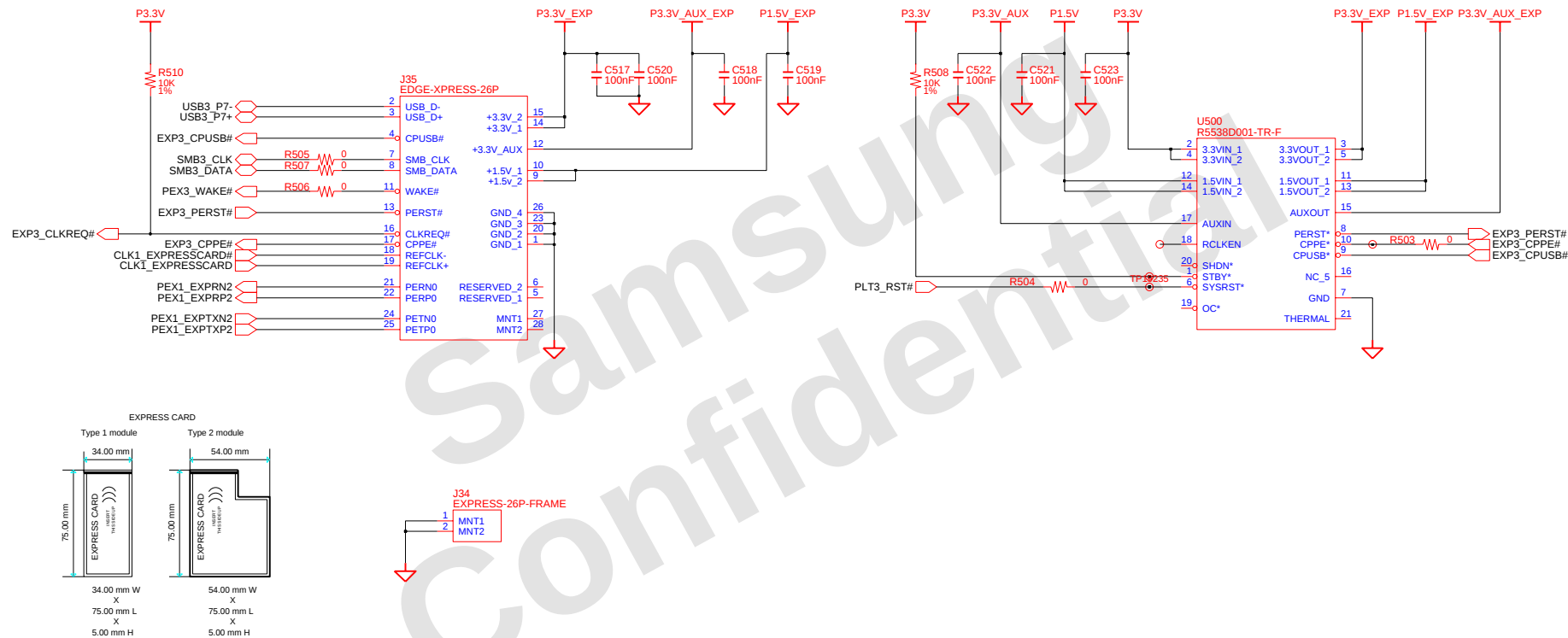
MINI CARD FOR ROBSON



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUJIANG	DEV. STEP	PV2		MINI CARD	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0		FRO BOBSON AND DVB-T	PART NO.
MODULE CODE		LAST EDIT				BA41-XXXX
				October 23, 2007 10:38:02 AM	PAGE	36 OF 58

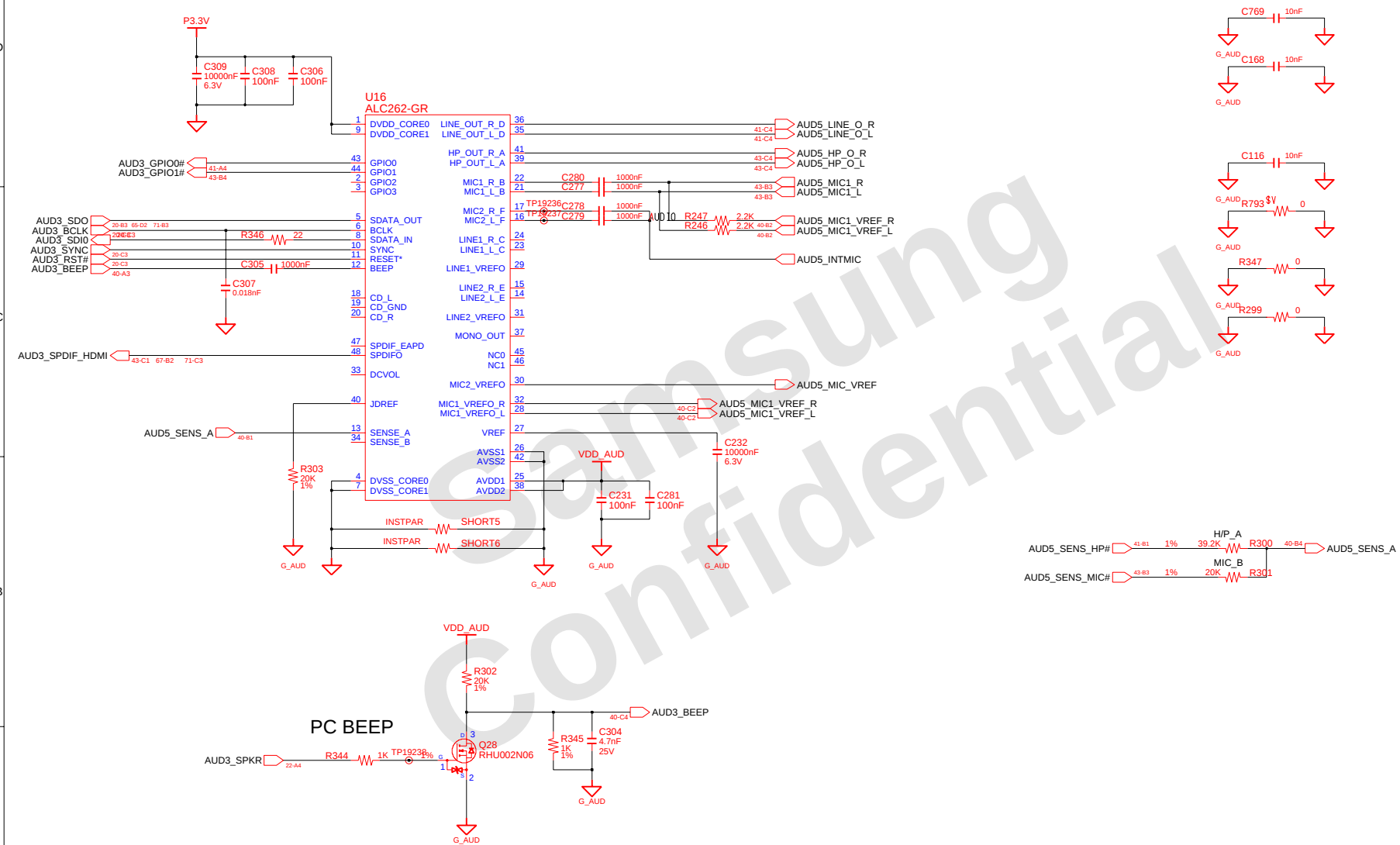
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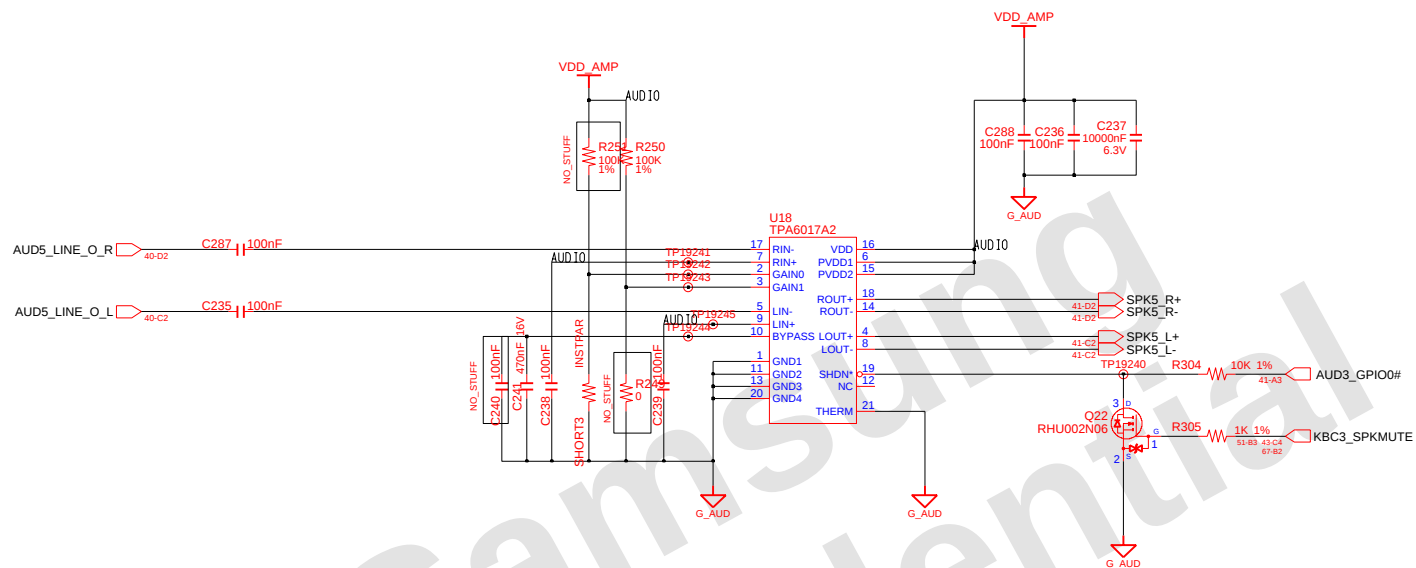
DRAW	SUN XIAO	DATE	6/27/2007	TITLE	Geneva MIO BOARD EXPRESS CARD	SAMSUNG ELECTRONICS
CHECK	WUSHIJIANG	DEV. STEP	PV2			PART NO. BA41-XXXX
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	37	OF 60

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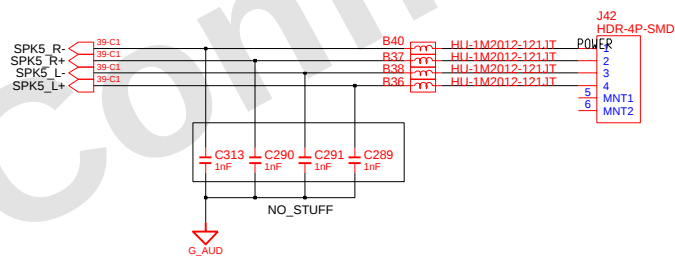


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHIJIANG	DEV. STEP	PV2	AUDIO CODEC	ELECTRONICS	
APPROVAL	KEVIN LEE	REV	1.0	FRO HDMI	PART NO.	BA41-XXXXX
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	38	OF 58

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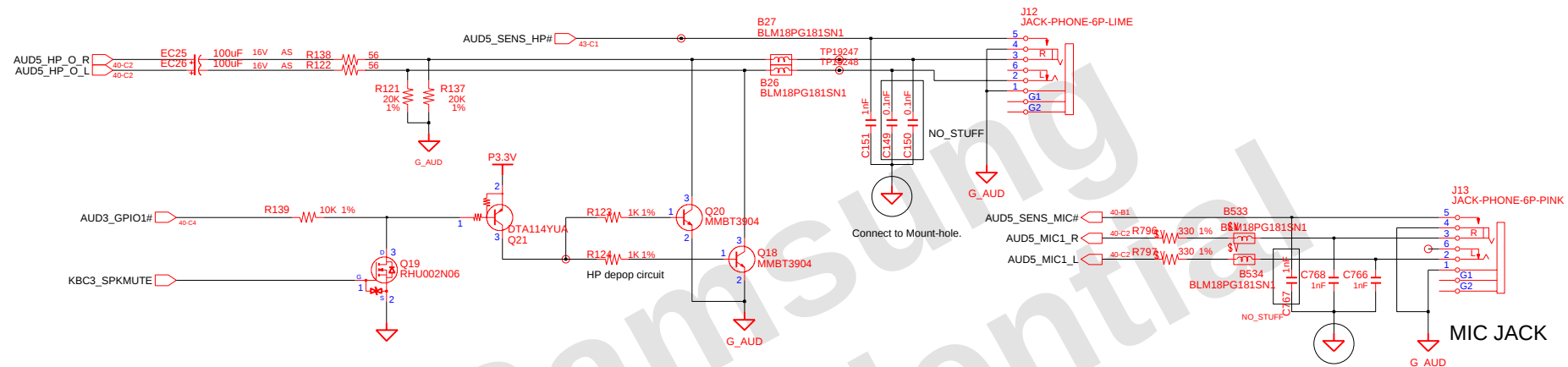
INTERNAL STEREO SPEAKERS



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena AUDIO AMP	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2			PART NO. BA41-XXXXX
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	39	OF 58

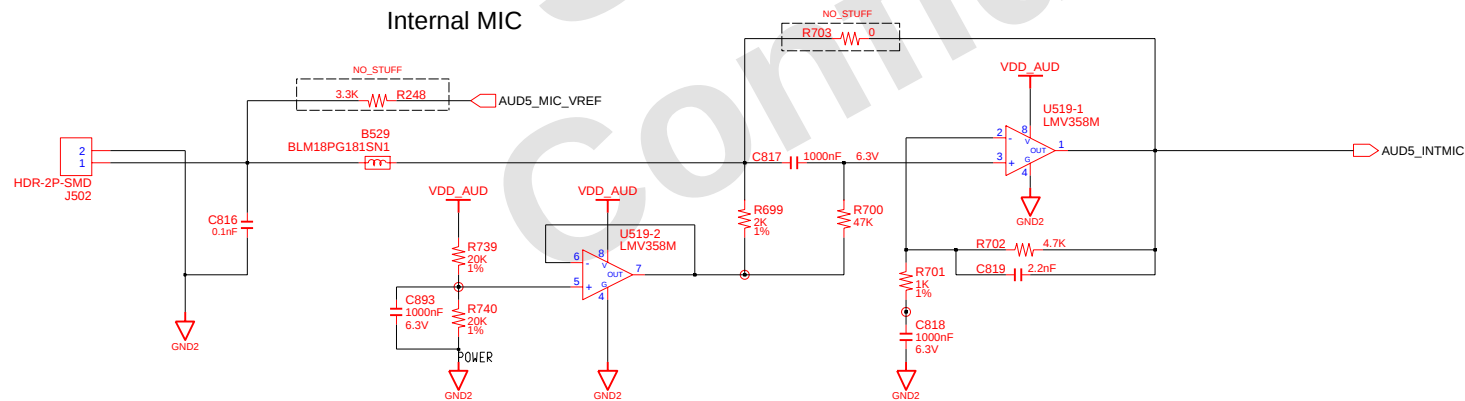
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HEADPHONE



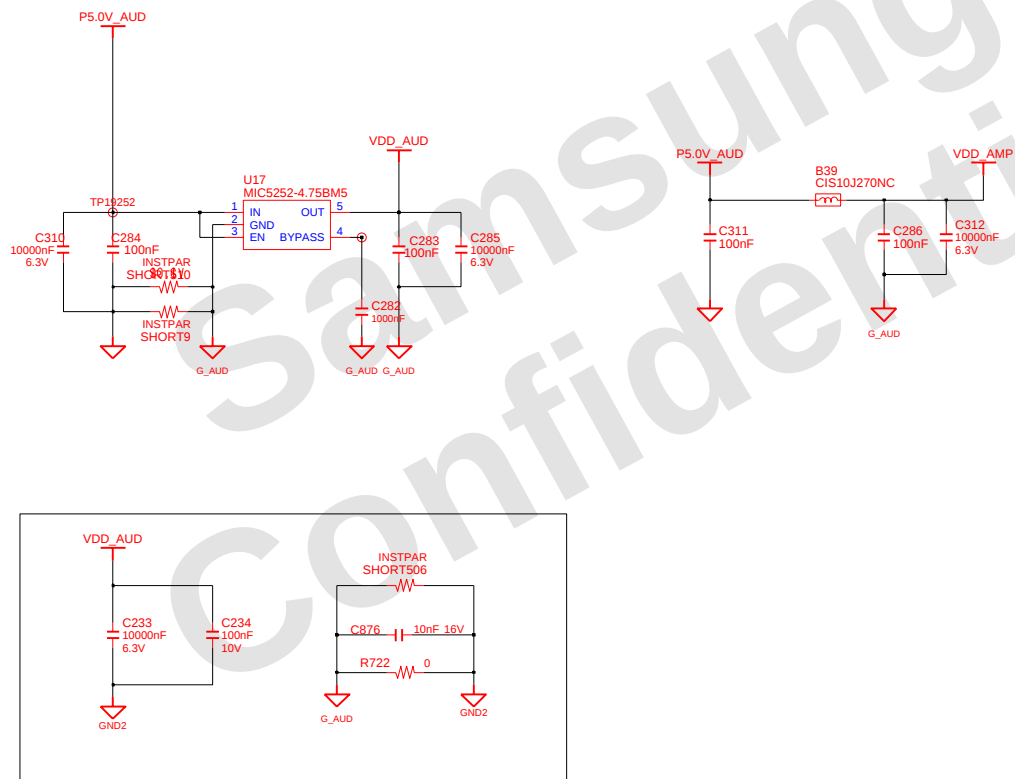
The traces led to Audio Jacks have the width over 10mil

Internal MIC



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2		HEAD PHONE JACK	
APPROVAL	KEVIN LEE	REV	1.0		AND MIC JACK	
MODULE CODE		LAST EDIT				
					October 23, 2007 10:38:02 AM	PAGE 40 OF 58

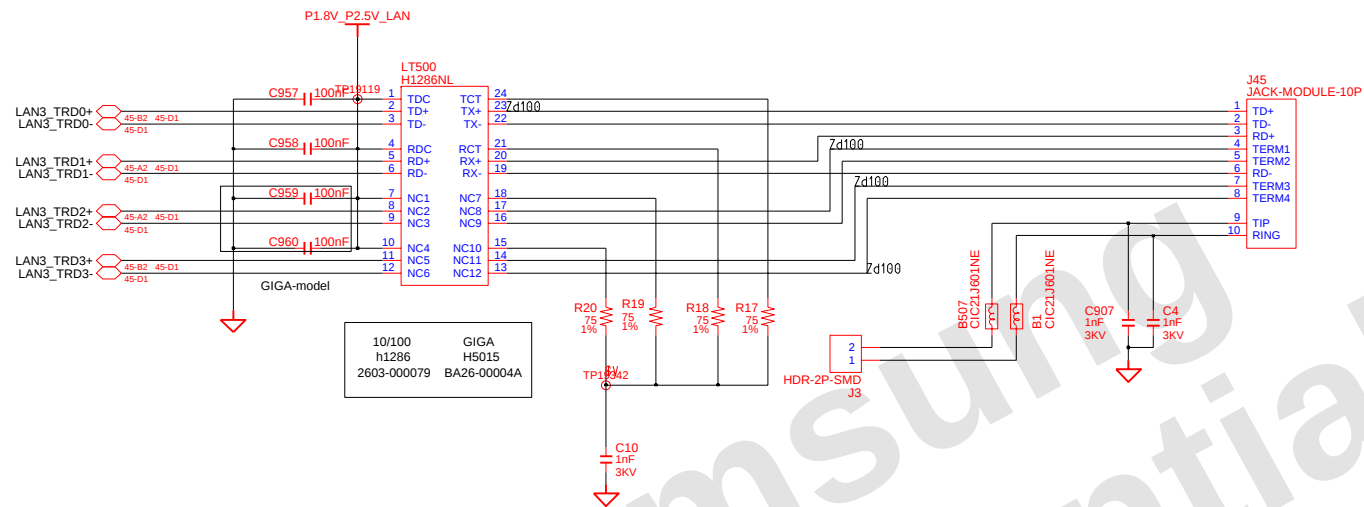
AUDIO POWER



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena AUDIO AUDIO POWER	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2			PART NO. BA41-XXXXX
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	41	OF 58

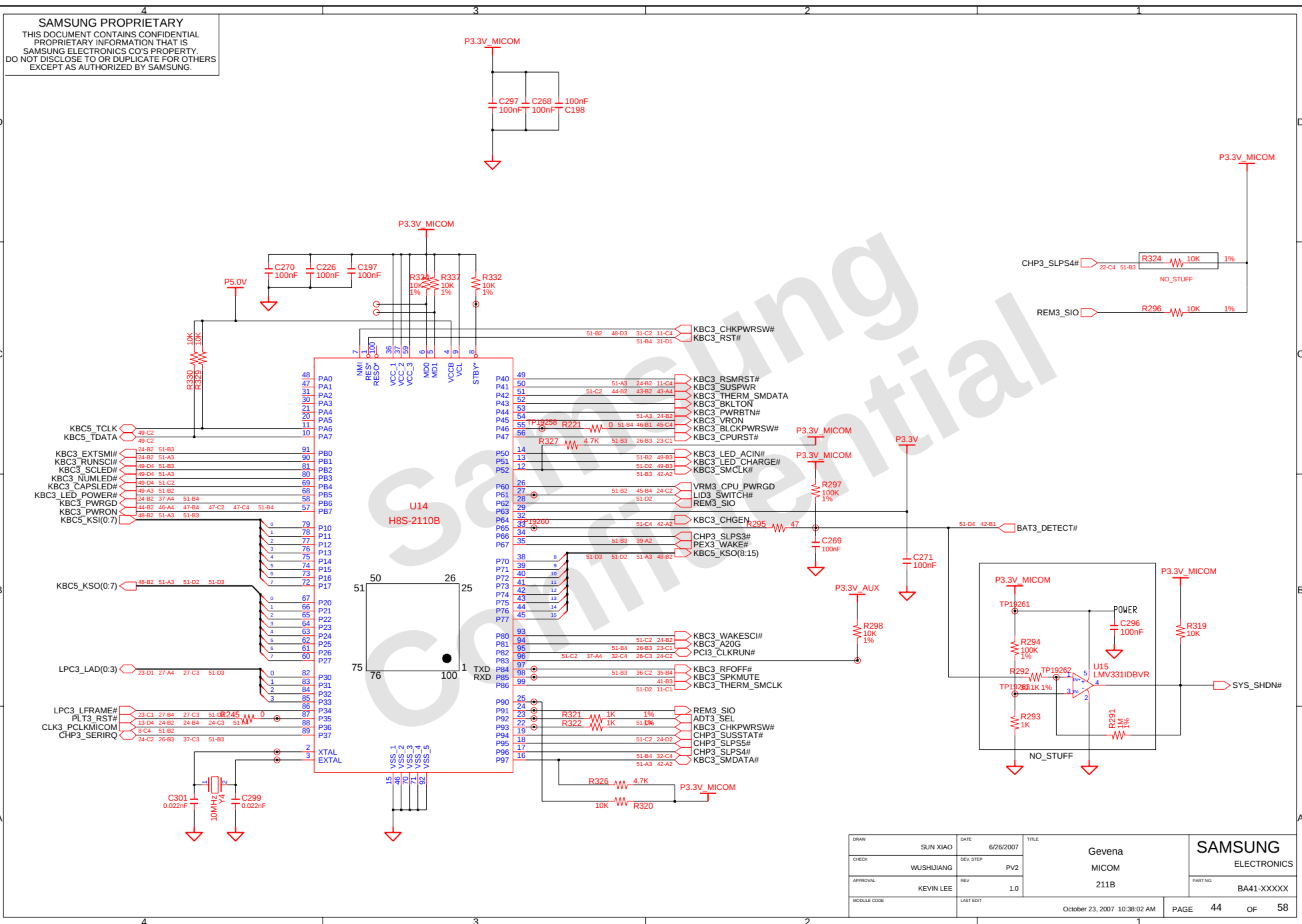
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The distance between LAN controller
and transformer is designed to extend less than two inches.



DRAW	SUN XIAO	DATE	6/26/2007	Gevena LAN LAN JACK RJ45		SAMSUNG			
CHECK	WUSHIJIANG	DEV. STEP	PV2			ELECTRONICS			
APPROVAL	KEVIN LEE	REV	1.0			PART NO.	BA41-XXXXXX		
MODULE CODE	LAST EDIT		October 23, 2007 10:38:02 AM			PAGE	43	OF	58

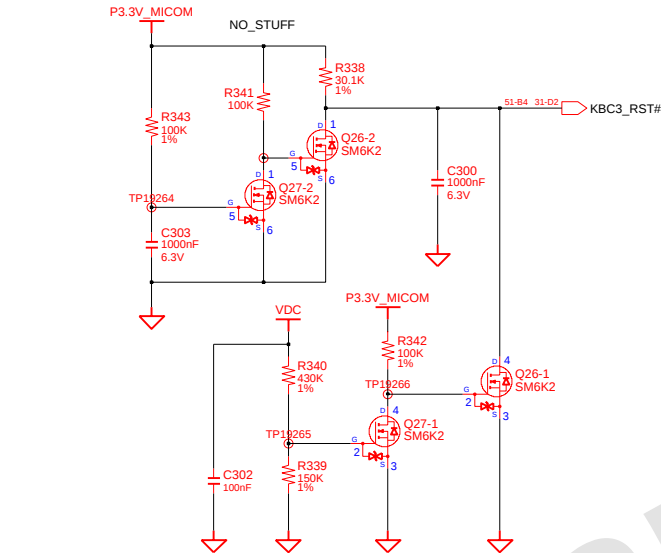
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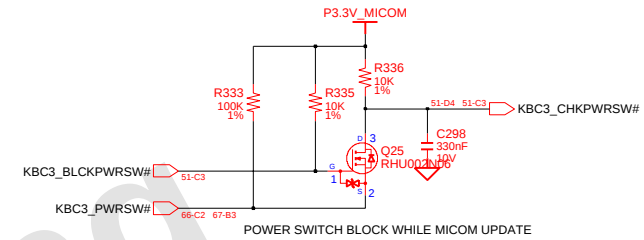
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUJIANG	DEV. STEP	PV2		MICOM	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0		211B	PART NO.
MODULE CODE		LAST EDIT				BA41-XXXXX
				October 23, 2007 10:38:02 AM	PAGE	44 OF 58

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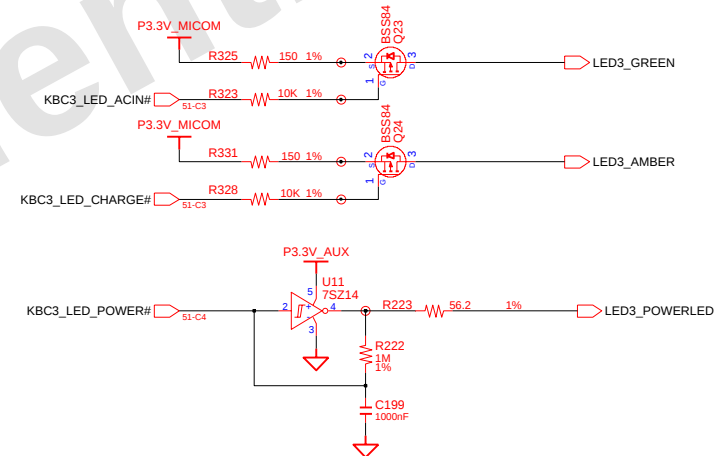
MICOM RESET



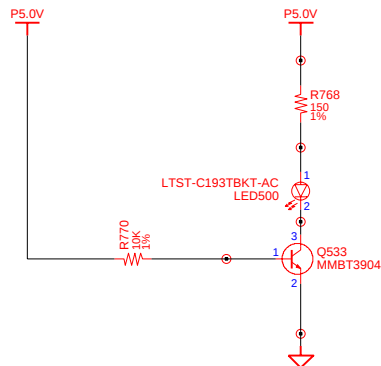
FOR MICOM UPDATE



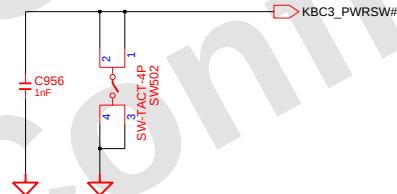
ADAPTERIN/CHARGING LED



POWER ON LED



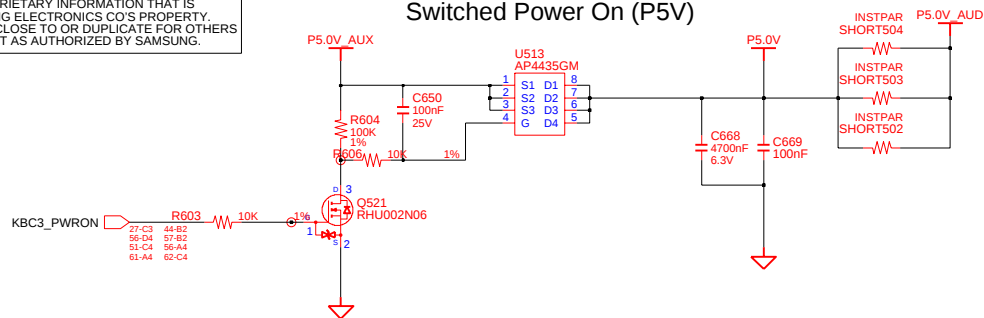
POWER ON SW BUTTON



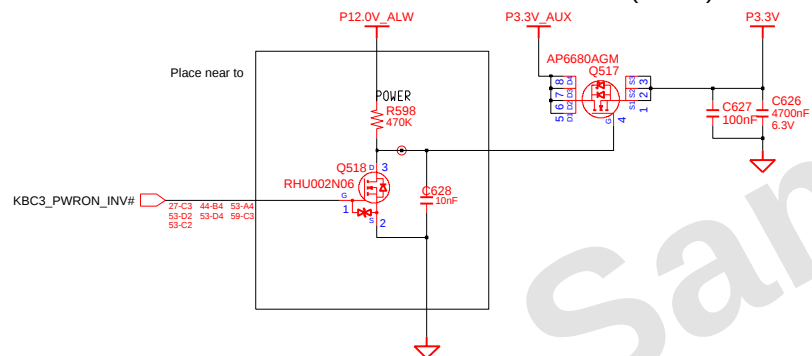
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHIJIANG	DEV. STEP	PV2		MICOM	
APPROVAL	KEVIN LEE	REV	1.0		MICOM LOGIC SCH	
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	45 OF 58

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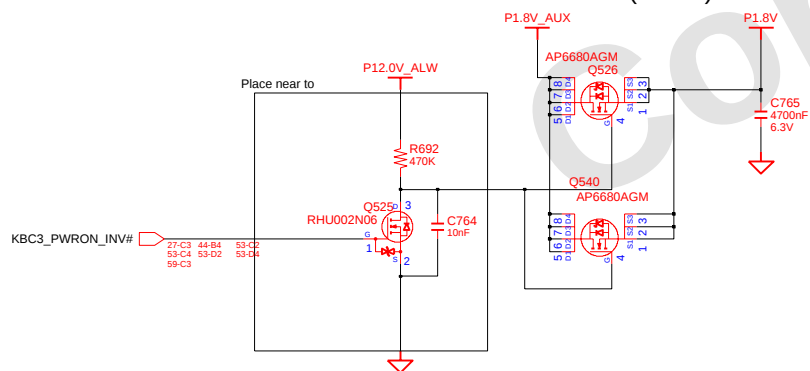
Switched Power On (P5V)



Switched Power On (P3.3V)

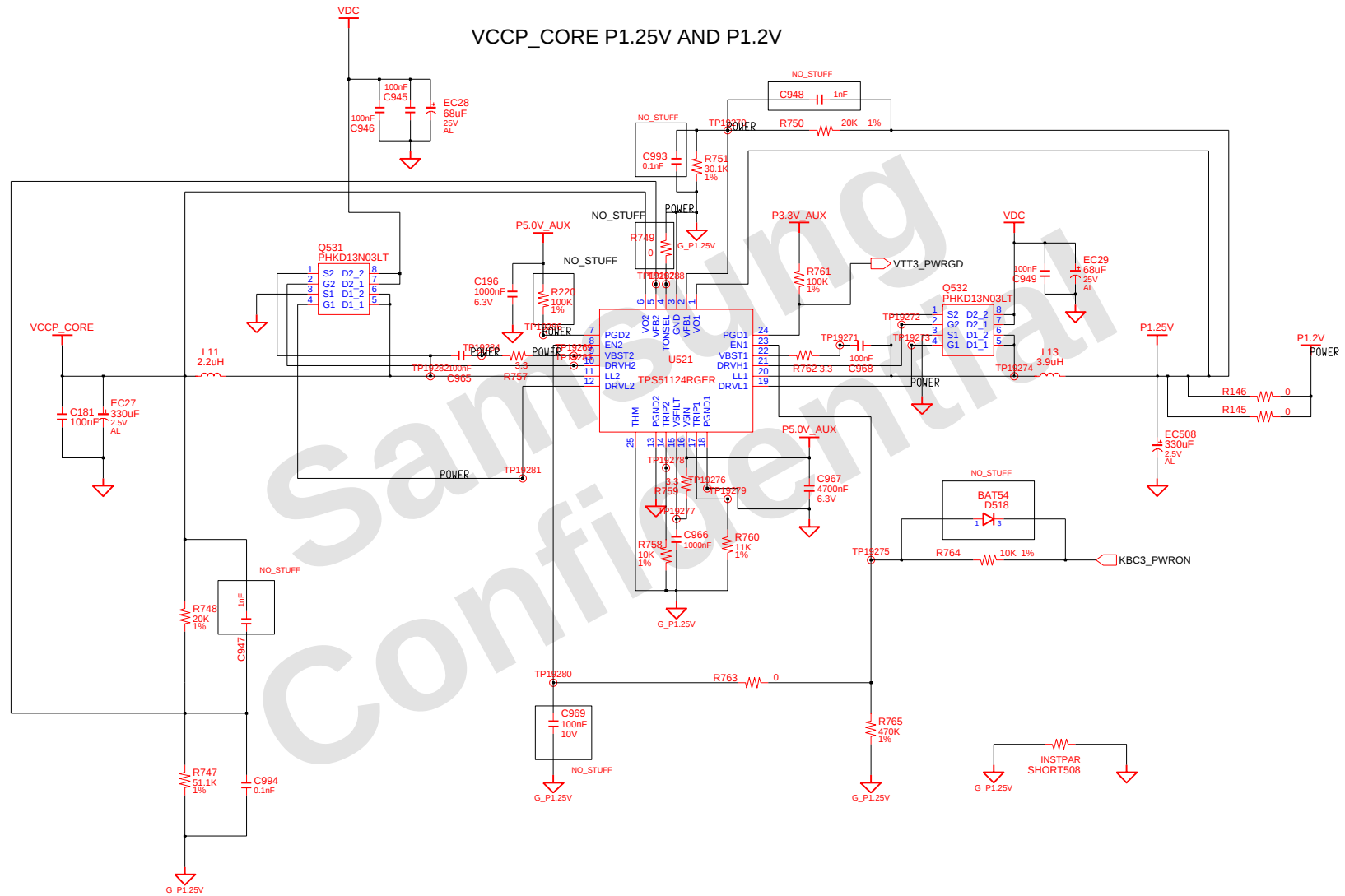


Switched Power On (P1.8V)



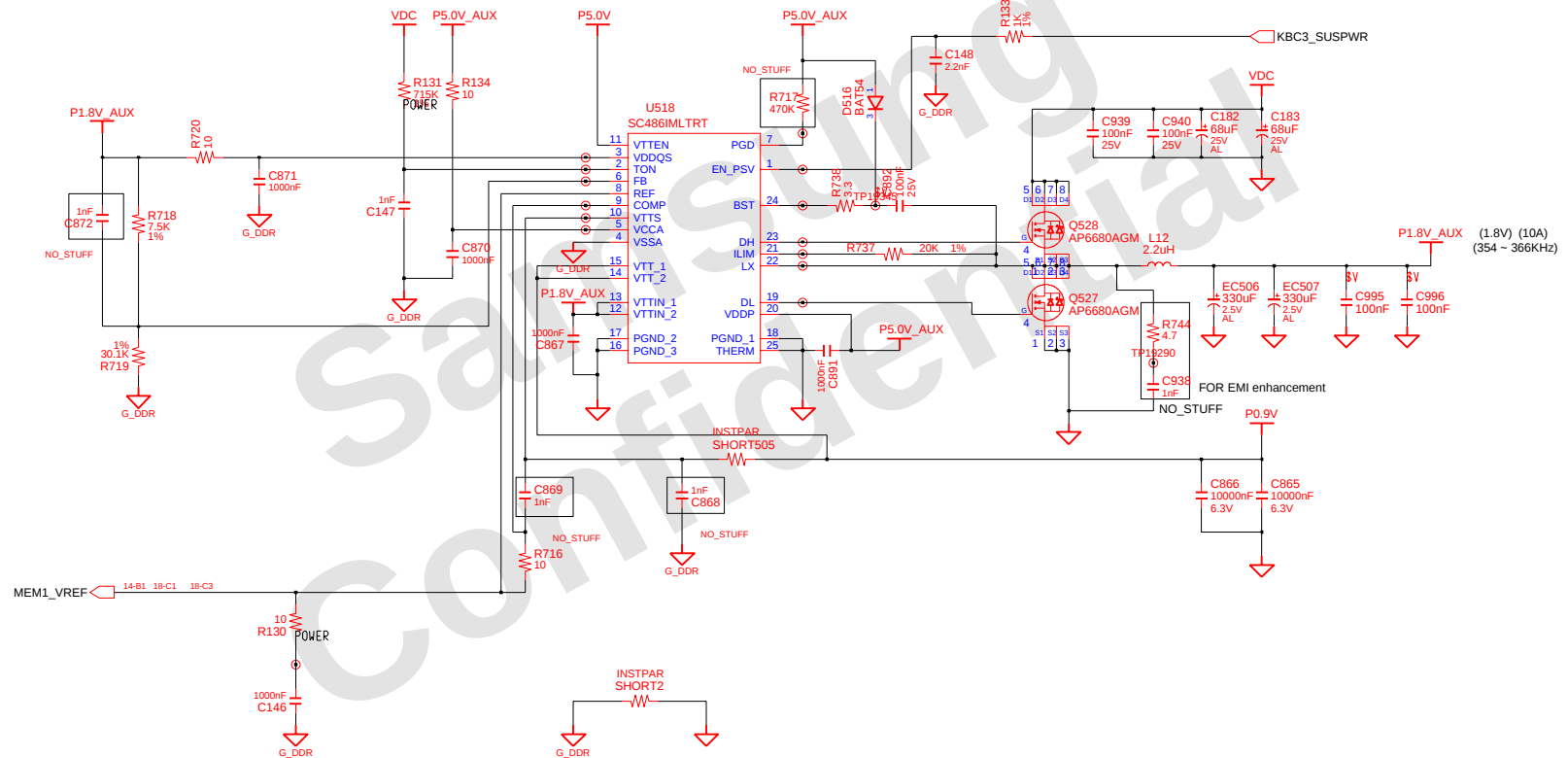
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHIJIANG	DEV. STEP	PV2	MAIN	MAIN	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0	SWITCH POWER P1.5V	PART NO.	BA41-XXXXX
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	46	OF 58

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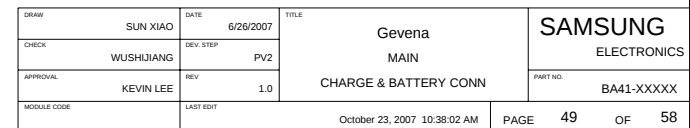
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena MAIN VCCP P1.25V AND P1.2V	SAMSUNG ELECTRONICS PART NO. BA41-XXXXX
CHECK	WUSHUJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	47 OF 58	

DDR2 Power

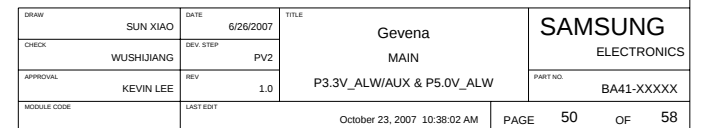


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena MAIN	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0	DDR2 POWER		PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT				
				October 23, 2007 10:38:02 AM	PAGE 48	OF 58

CHARGER & POWER MANAGEMENT

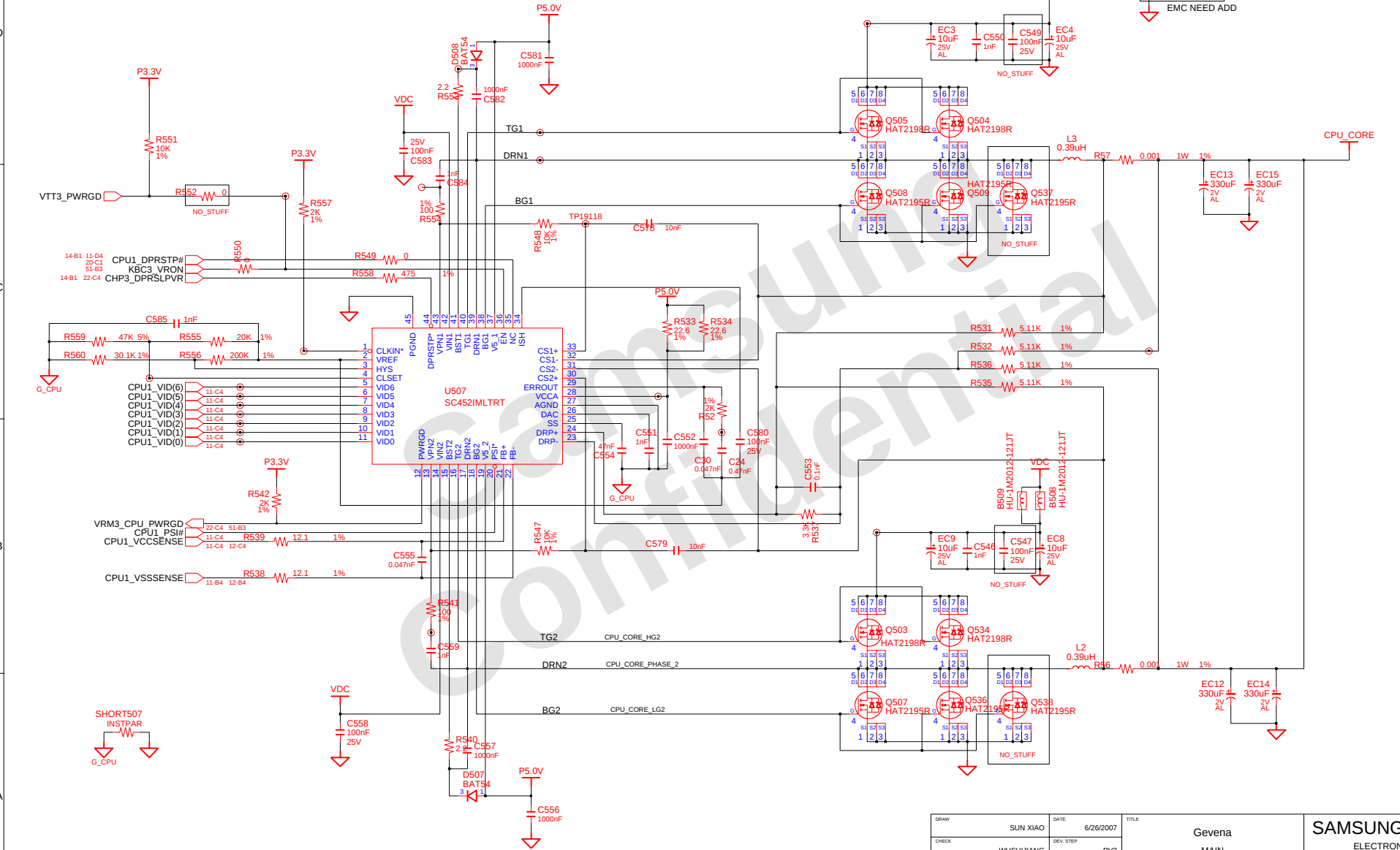


P3.3V_ALW/AUX & P5V_AUX



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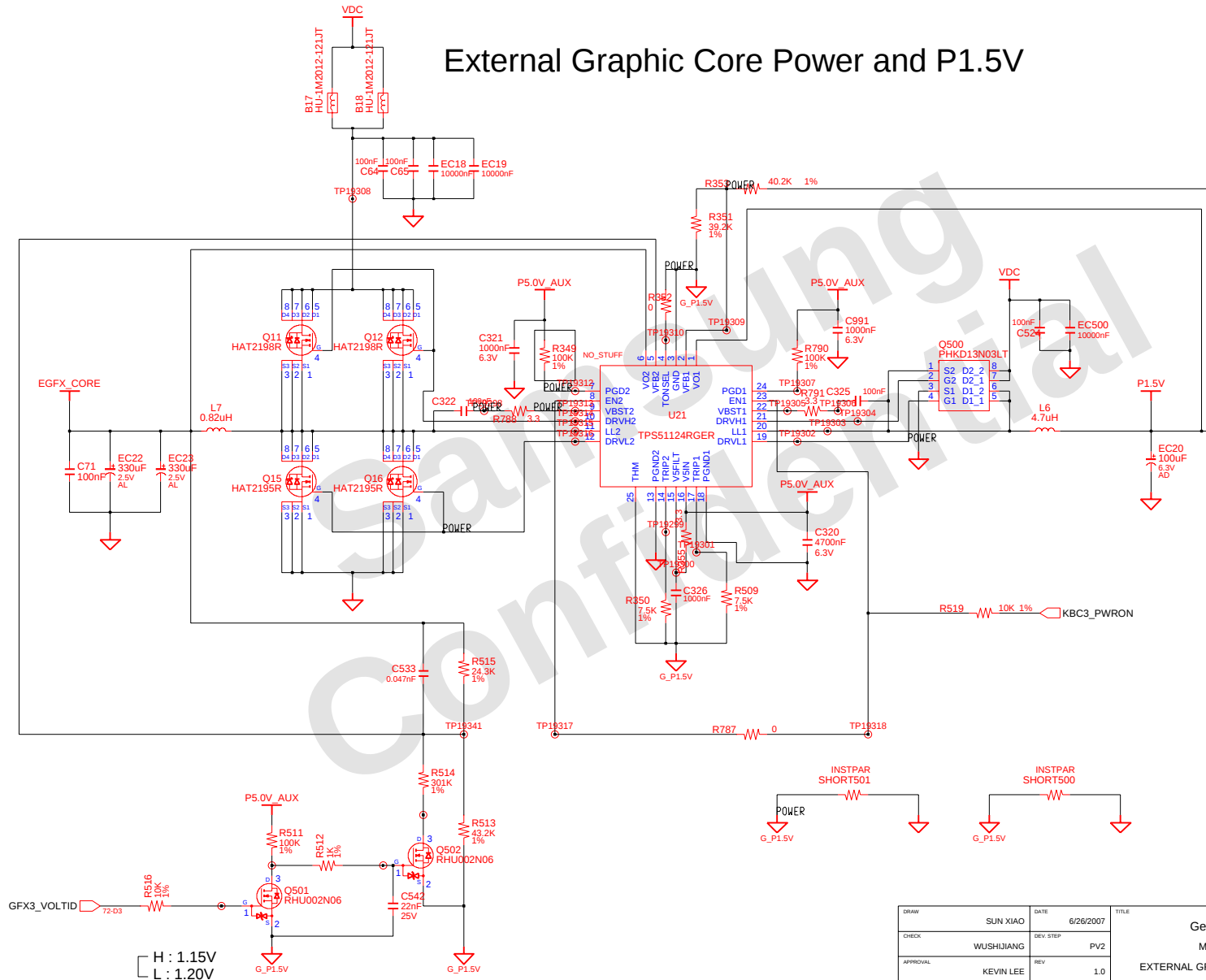
CPU VRM [SEMTECH]



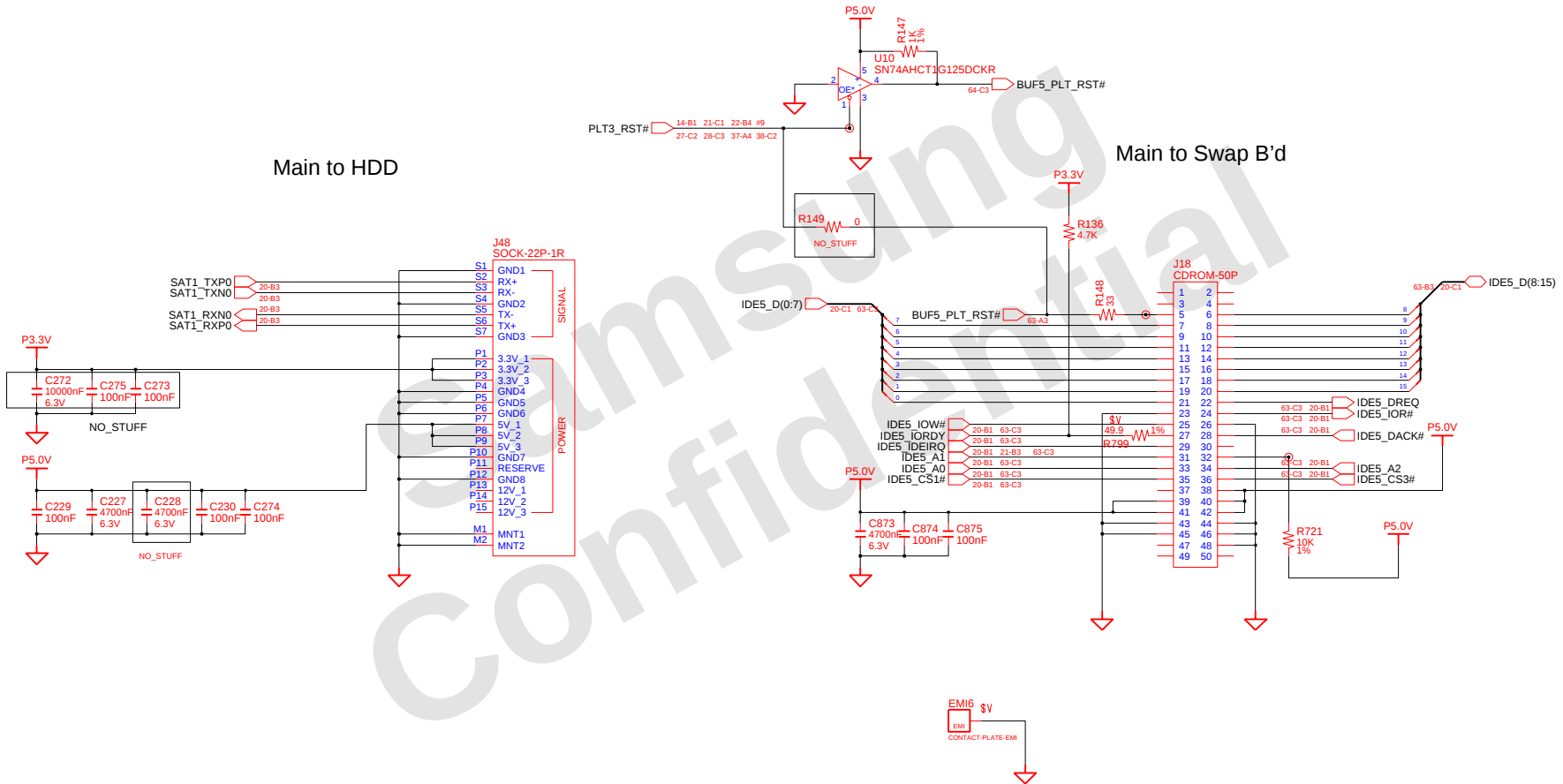
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena MAIN CPU VRM	SAMSUNG ELECTRONICS
CHECK	WUSHIJIANG	DEV STEP	PV2			PART NO. BA41-XXXXX
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT				
October 23, 2007 10:38:02 AM						PAGE 51 OF 58

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External Graphic Core Power and P1.5V

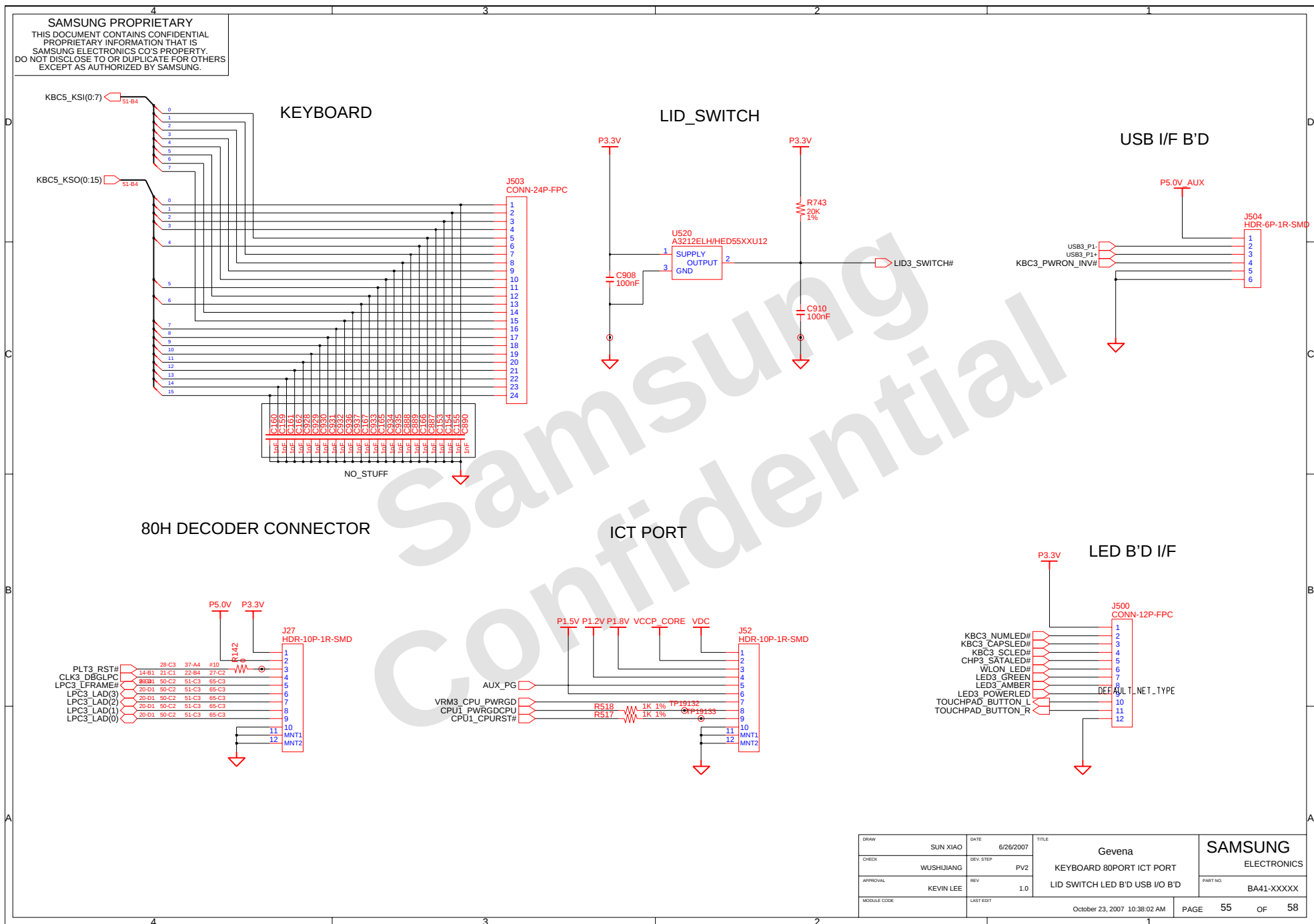


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena MAIN	SAMSUNG ELECTRONICS
CHECK	WUSHIJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0	EXTERNAL GFX POWER VRM		PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT				
				October 23, 2007 10:38:02 AM	PAGE	52 OF 58

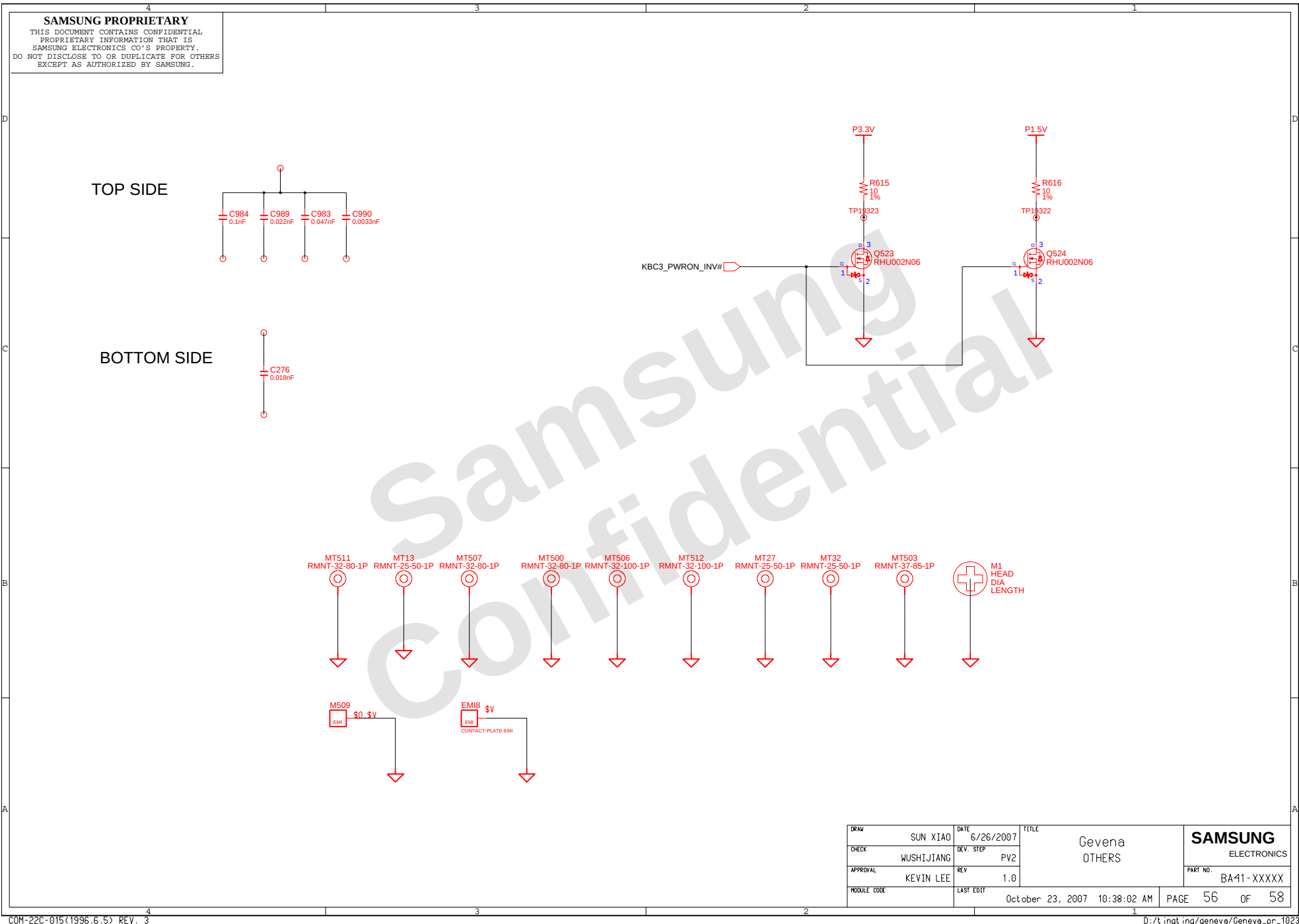


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHIJIANG	DEV STEP	PV2	CONNECTOR		
APPROVAL	KEVIN LEE	REV	1.0	HDD & ODD CONNECTOR		
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM			
October 23, 2007 10:38:02 AM						PAGE 53 OF 58

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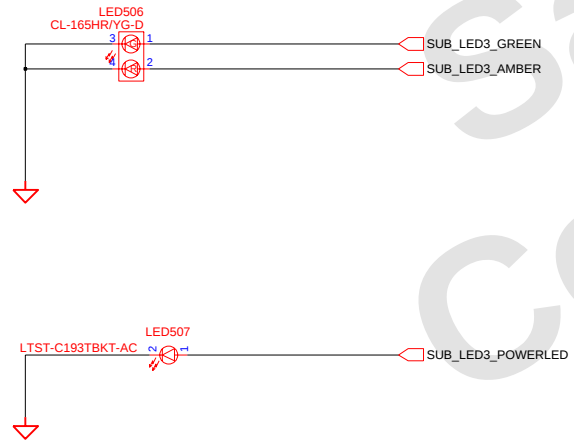
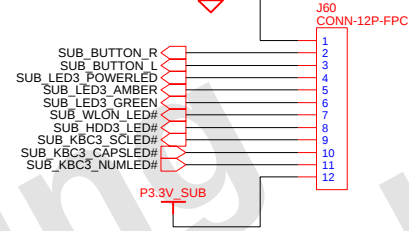
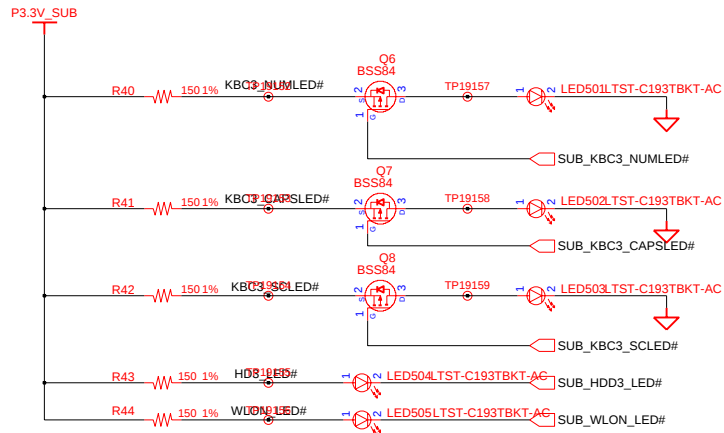
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUJIANG	DEV STEP	PV2	KEYBOARD 80PORT ICT PORT		ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0	LID SWITCH LED B'D USB I/O B'D	PART NO.	BA41-XXXXX
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	55	OF 58



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena OTHERS	SAMSUNG ELECTRONICS PART NO. BA41-XXXXX
CHECK	WUSHIJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	56 OF 58	

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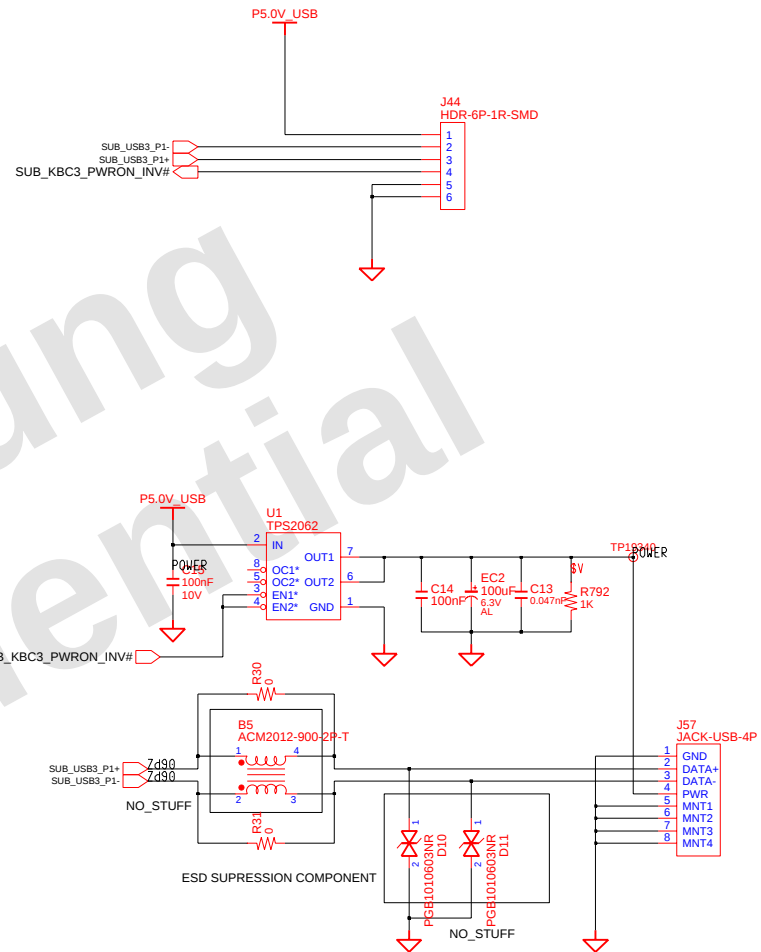
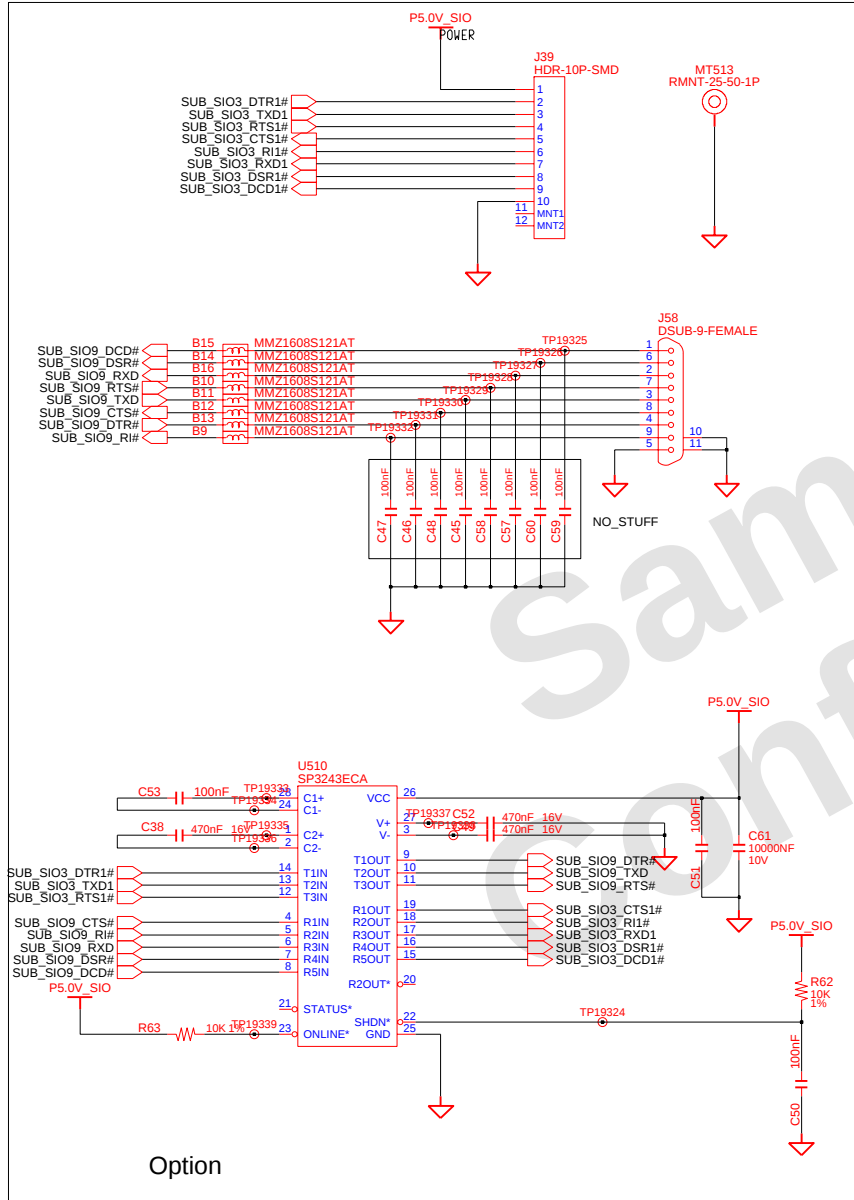
TOUCHPAD AND LED B'D



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva	SAMSUNG ELECTRONICS PART NO. BA41-
CHECK	WUSHIJIANG	DEV. STEP	PV2	TOUCHPAD AND LED B'D		
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE	LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	57 OF 60	

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SIO AND USB SUB B'D



DRAW	SUN XIAO	DATE	6/30/2007	TITLE	Geneva	SAMSUNG ELECTRONICS
CHECK	WUSHIJIANG	DEV. STEP	PV2		MIO BOARD	
APPROVAL	KEVIN LEE	REV	1.0		USB AND SIO SUB B'D	
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM		PAGE 58 OF 60	

TP18380OAU3_SEL
TP18381OAU3_BCLK
TP18382OAU3_BEEP
TP18383OAU3_BEEP_CU
TP18384OAU3_GP100#
TP18385OAU3_GP101#
TP18386OAU3_GP101#_L
TP18387OAU3_RST#
TP18388OAU3_SDIO
TP18389OAU3_SDIO_RU
TP18390OAU3_SDO
TP18391OAU3_SPKR

TP18393OAU3_SYNC
TP18394OAU5_HP_0_L
TP18395OAU5_HP_0_L_CR
TP18396OAU5_HP_0_L_RB
TP18397OAU5_HP_0_B
TP18398OAU5_HP_0_B_CR
TP18399OAU5_HP_0_B_RB
TP18400OAU5_INTMIC
TP18401OAU5_L1NE_0_L
TP18402OAU5_L1NE_0_L_CU
TP18403OAU5_L1NE_0_R
TP18404OAU5_L1NE_0_R_CU
TP18405OAU5_M1C1_L
TP18406OAU5_M1C1_L_BCON
TP18407OAU5_M1C1_L_CU
TP18408OAU5_M1C1_R
TP18409OAU5_M1C1_R_BCON
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TP18351OAU5_SENS_MIC#
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TP18353OAU5_JDREF
TP18354OAU5_PG

TP18361OBA13_SMCLK#
TP18362OBA13_SMDATA#
TP18363OBA13_CONN_TP_BB
TP18364OBU5_PLT_RST#

TP18367OCHP1_5_DMICOMP_R
TP18368OCHP3_BIOSWP#
TP18369OCHP3_BIOS_CR1#
TP18370OCHP3_CL_CLK_0
TP18371OCHP3_CL_DATA_0
TP18372OCHP3_CL_RST#_0
TP18373OCHP3_CL_RST#_1
TP18374OCHP3_CPUSTP#
TP18375OCHP3_CPUSTP#_R_1CH
TP18376OCHP3_DPRSLPVR
TP18377OCHP3_DPRSLPVR_R_1CH
TP18378OCHP3_EXTGFX#
TP18379OCHP3_GP1012
TP18328OCHP3_GP1017
TP18329OCHP3_INTRUDER#
TP18330OCHP3_INTVEMEN
TP18331OCHP3_LANT100_SLP
TP18332OCHP3_LLDR00#
TP18333OCHP3_LLDR01#
TP18334OCHP3_PC1STP#
TP18335OCHP3_R1#_R
TP18336OCHP3_R1CRST#
TP18337OCHP3_SATACLKREQ#
TP18338OCHP3_SATALED#
TP18339OCHP3_SERIRQ
TP18340OCHP3_SLP3#
TP18341OCHP3_SLP5#
TP18342OCHP3_SLP5#
TP18343OCHP3_SUSSTAT#

TP18344OCHP3_TPT_R
TP18345OCHP3_USBRRIAS_R
TP18346OCHP3_USBRROC9#_R
TP18347OCHP3_SDATAOUT0_R
TP18319OCLK3_DBG1PC
TP18320OCLK3_TCH14
TP18321OCLK3_PCLK1CH
TP18322OCLK3_PCLKMICOM
TP18323OCLK3_PCLKSIO
TP18324OCLK3_PCLKSIO_DS
TP18325OCLK3_PWRGD
TP18326OCLK3_S1014
TP18327OCLK3_USB48
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TP18316OCPU1_AD5#
TP18317OCPU1_BNR#
TP18318OCPU1_BPR1#
TP18306OCPU1_DREQ#
TP18307OCPU1_BSEL0
TP18308OCPU1_BSEL1
TP18309OCPU1_BSEL2
TP18310OCPU1_COMP0_R
TP18311OCPU1_COMP1_R
TP18312OCPU1_COMP2_R
TP18313OCPU1_COMP3_R
TP18314OCPU1_CPURST#

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TP18297OCPU1_DPSTP#
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TP18300OCPU1_DRDY#
TP18301OCPU1_FERR#
TP18302OCPU1_HIT#
TP18303OCPU1_HITM#
TP18304OCPU1_IERR#
TP18305OCPU1_IGNNE#
TP18259OCPU1_INT#
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TP18261OCPU1_LOCK#
TP18262OCPU1_NM1
TP18263OCPU1_PS1#
TP18264OCPU1_PWRGDGPU
TP18270OCPU1_RS0#
TP18271OCPU1_RS1#
TP18272OCPU1_RS2#
TP18273OCPU1_SLP#
TP18274OCPU1_SMI#
TP18275OCPU1_STPCLK#
TP18276OCPU1_TCK
TP18277OCPU1_TDI
TP18278OCPU1_TEST1_R
TP18279OCPU1_TEST2_R
TP18280OCPU1_TEST3_R
TP18281OCPU1_TEST4_R
TP18282OCPU1_TEST5_R
TP18283OCPU1_THRMTRIP#
TP18284OCPU1_THRMTRIP_R#
TP18285OCPU1_TMS
TP18286OCPU1_TRDY#
TP18287OCPU1_TRST#
TP18288OCPU1_VCCSENSE
TP18289OCPU1_VSSSENSE
TP18290OCPU2_THERMDA
TP18251OCPU2_THERMDC
TP18252OCPU3_THRMTRIP#
TP18253OCPU_CORE_HG2
TP18254OCPU_CORE_LG1
TP18255OCPU_CORE_LG2
TP18256OCPU_CORE_PHASE_2

TP17811ODRAM_RSTA#
TP17812ODRAM_RSTC#
TP17813OEDID_CLK
TP17814OEDID_DATA
TP17815OEXP3_CLKREQ#
TP17816OEXP3_CPPE#
TP17817OEXP3_CPUSB#
TP17818OEXP3_FERR1#
TP17819OEXP3_FDBACK#
TP17820OFAN5_VDD
TP17821OGFX3_B1ON
TP17822OGFX3_BRIT

TP17799OGFX3_HSYNC
TP17800OGFX3_LCVD00N
TP17801OGFX3_THERM#
TP17802OGFX3_THRMDN
TP17803OGFX3_THRMOP
TP17804OGFX3_VOL1D
TP17805OGFX3_VSYNC

TP17808OIDE5_CS1#
TP17809OIDE5_CS2#
TP17810OIDE5_DACK#
TP17767OIDE5_DREQ
TP17768OIDE5_IDEQ
TP17769OIDE5_IOW#
TP17770OIDE5_IORDY
TP17771OIDE5_IOW#
TP17772OILIM3
TP17773OITP3_DBRESET#
TP17774OITP3_DBRESET#_R
TP17775OITP3_DBRESET#_R
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TP17789OKBC3_PWRCD
TP17790OKBC3_PWRON
TP17791OKBC3_PWRON_INV#
TP17792OKBC3_PWRON_INV#_P1.8V
TP17793OKBC3_PWRON_P1.5V
TP17794OKBC3_PWRSW#
TP17795OKBC3_RSMRST#
TP17796OKBC3_RSMRST#_R_1CH
TP17797OKBC3_RSMRST#
TP17798OKBC3_RST#
TP17735OKBC3_RUNSCI#
TP17736OKBC3_SCLEDE#
TP17737OKBC3_SMCLK#
TP17738OKBC3_SMDATA#
TP17739OKBC3_SPKMUTE_R
TP17740OKBC3_SPKMUTE_RQ_L
TP17741OKBC3_SPKMUTE_RQ_R
TP17742OKBC3_SUSPWR
TP17743OKBC3_THERM_SMCLK
TP17744OKBC3_THERM_SMDATA
TP17745OKBC3_VRON
TP17746OKBC3_WAKESCI#
TP17747OKBC5_KSI(0)
TP17748OKBC5_KSI(1)
TP17749OKBC5_KSI(2)
TP17750OKBC5_KSI(3)

TP17751OKBC5_KSI(4)
TP17752OKBC5_KSI(5)
TP17753OKBC5_KSI(6)
TP17754OKBC5_KSI(7)
TP17755OKBC5_KSI(8)
TP17756OKBC5_KSI(9)
TP17757OKBC5_KSI(10)
TP17758OKBC5_KSI(11)
TP17759OKBC5_KSI(12)
TP17760OKBC5_KSI(13)
TP17761OKBC5_KSI(14)
TP17762OKBC5_KSI(15)
TP17763OKBC5_KSI(2)
TP17764OKBC5_KSI(3)
TP17765OKBC5_KSI(4)
TP17766OKBC5_KSI(5)
TP17767OKBC5_KSI(6)
TP17768OKBC5_KSI(7)
TP17769OKBC5_KSI(8)
TP17770OKBC5_KSI(9)
TP17723OKBC5_TCLK
TP17724OKBC5_TDATA
TP17725OCD3_BKLTON
TP17726OCD3_BRIT
TP17727OCD3_AMBER
TP17728OCD3_GREEN
TP17729OCD3_POWERLED
TP17730OCD3_LAD(0)
TP17731OCD3_LAD(1)
TP17732OCD3_LAD(2)
TP17733OCD3_LAD(3)
TP17734OCD3_LFRAME#
TP17735MAX8734_BST3
TP17736MAX8734_BST5
TP17737MAX8734_FB3
TP17738MAX8734_SKIP#
TP17739MAX8734_THM3_STP#_00
TP17740MAX8734_VCC

DRAW	SUNXIAO	DATE	9/10/2007	TITLE	Gevena TEST POINT	SAMSUNG ELECTRONICS PART NO. BA41 - undef ined
CHECK	WUSHIJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	59 OF 59	

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