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8. Block diagram and Schematic

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CANNES-L

CPU : Intel Penryn
Chip Set : Intel Cantiga & ICH9M
Remarks : Montevina Platform

Model Name : R719
PBA Name : MAIN
PCB Code : GCE :
 NAN :
 HAN :
Dev. Step : PV
Revision : 1.0
T.R. Date : 2009.06.04

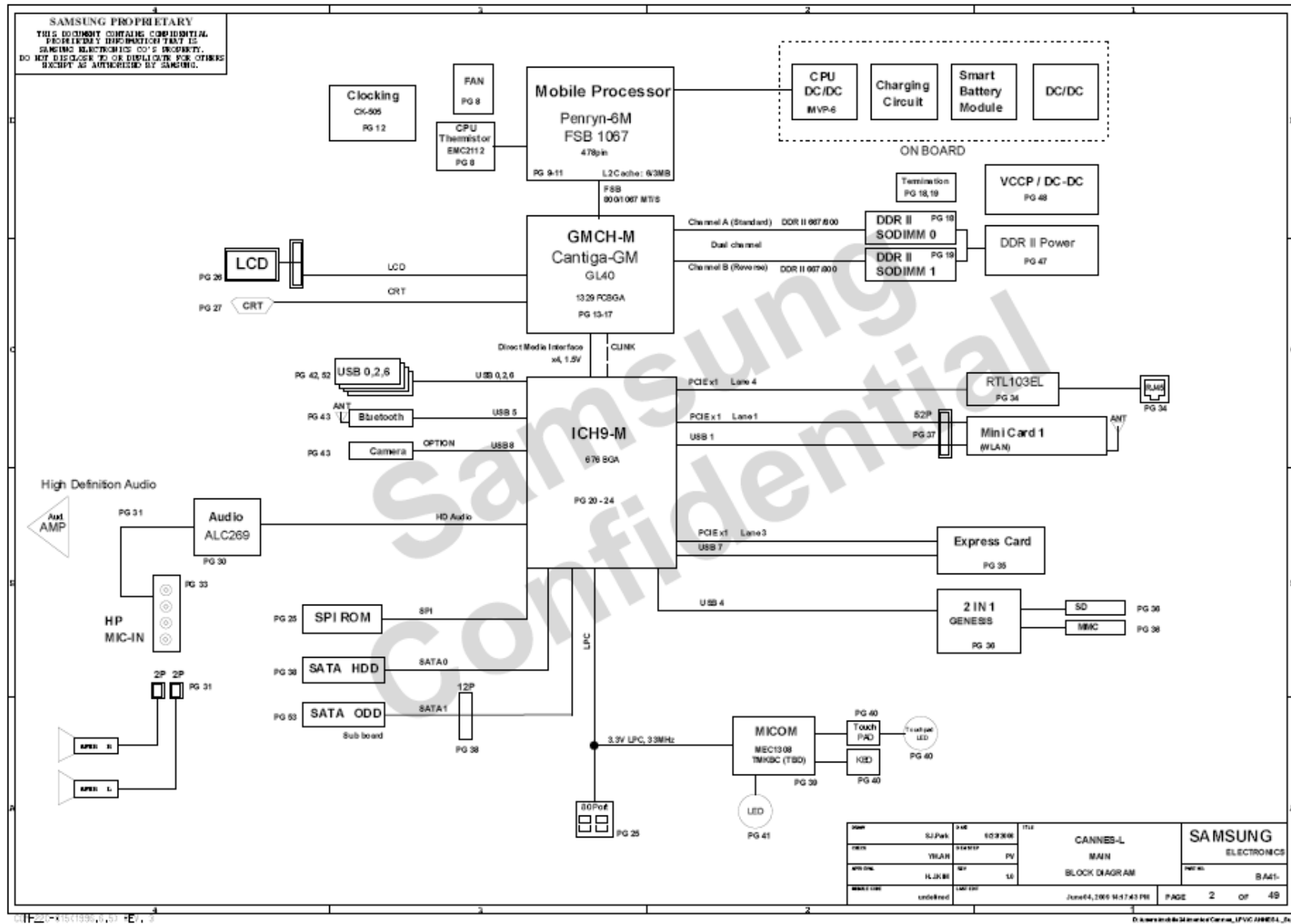
Design	CHECK	APPROVAL

■ Owner : SEC Mobile R & D Signature : X

DATE	BY	REVISION	TITLE	SAMSUNG ELECTRONICS
2009.06.04	YJLH	PV	CANNES-L MAIN COVER	
2009.06.04	YJLH	SP		
2009.06.04	YJLH	SP		

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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ#INT#	Interrupts
Cardbus	AC25	3	A,B,C
USB	AC29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI LPCbridge/IDE/AC97/SMBUS	AC30(internal) AC31(internal)	- -	B B
Internal MAC AC Link GLAN	AC24(internal) - -	- - -	TRGM - -

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	IC46-M	Real Time Clock
Crystal	10MHz	MCOM	HD4471692100
Crystal	14.318MHz	CLOCK-Generator	CK-905
Crystal	25MHz	LAN	RealTek 88E8057

LCD Panel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

Voltage Rails

VDD CORE Primary DC system power supply (0 to 20V)
VDD CORE Core Voltage for CPU
P10SV (VDDCP) VTT for CPU, Coreline & IC49-M
P33V_MCOM 3.3V always power rail (for Mcom)
P15V 1.5V switched power rail (off in S3-S5)
P18V 1.8V switched power rail (off in S3-S5)
P18V_AUX 1.8V power rail for DDR (off in S4-S5)
P09V 0.9V power rail for DDR (off in S3-S5)
P33V 3.3V switched power rail (off in S3-S5)
P33V_AUX 3.3V switched on power rail (off in S4-S5)
P50V 5.0V switched power rail (off in S3-S5)
P50V_AUX 5.0V switched on power rail (off in S4-S5)
P50V_ALW 5.0V always power rail

FC / SMB Address

Devices	Address	Hex	Bus
IC49-M	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
300MM0	1010 000x	A0h	-
300MM1	1010 010x	A4h	-
Thermal Sensor on 300MM0	0011 000x	30h	-
Thermal Sensor on 300MM1	0011 010x	34h	-
CK50SM (Clock Generator)	1101 001x	D0h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	SYSTEM PORT 2
3	NC
4	NC
5	Bluetooth
6	Mini PCI Express 2
7	Camera
8	NC
9	NC

PCI Express Assign

PORT #	ASSIGNED TO
0	NC
1	Mini Card 1 (WLAN)
2	NC
3	NC
4	Mini Card 2 (ROBSON or DVB-T)
5	NC

REVISION HISTORY

See rev notes for more information.

REV	DESCRIPTION	DATE	BY
1.0	Initial Release	2009.06.04	BA11

CANES-L

MAIN

BOARD INFO

SAMSUNG

ELECTRONICS

BA11-

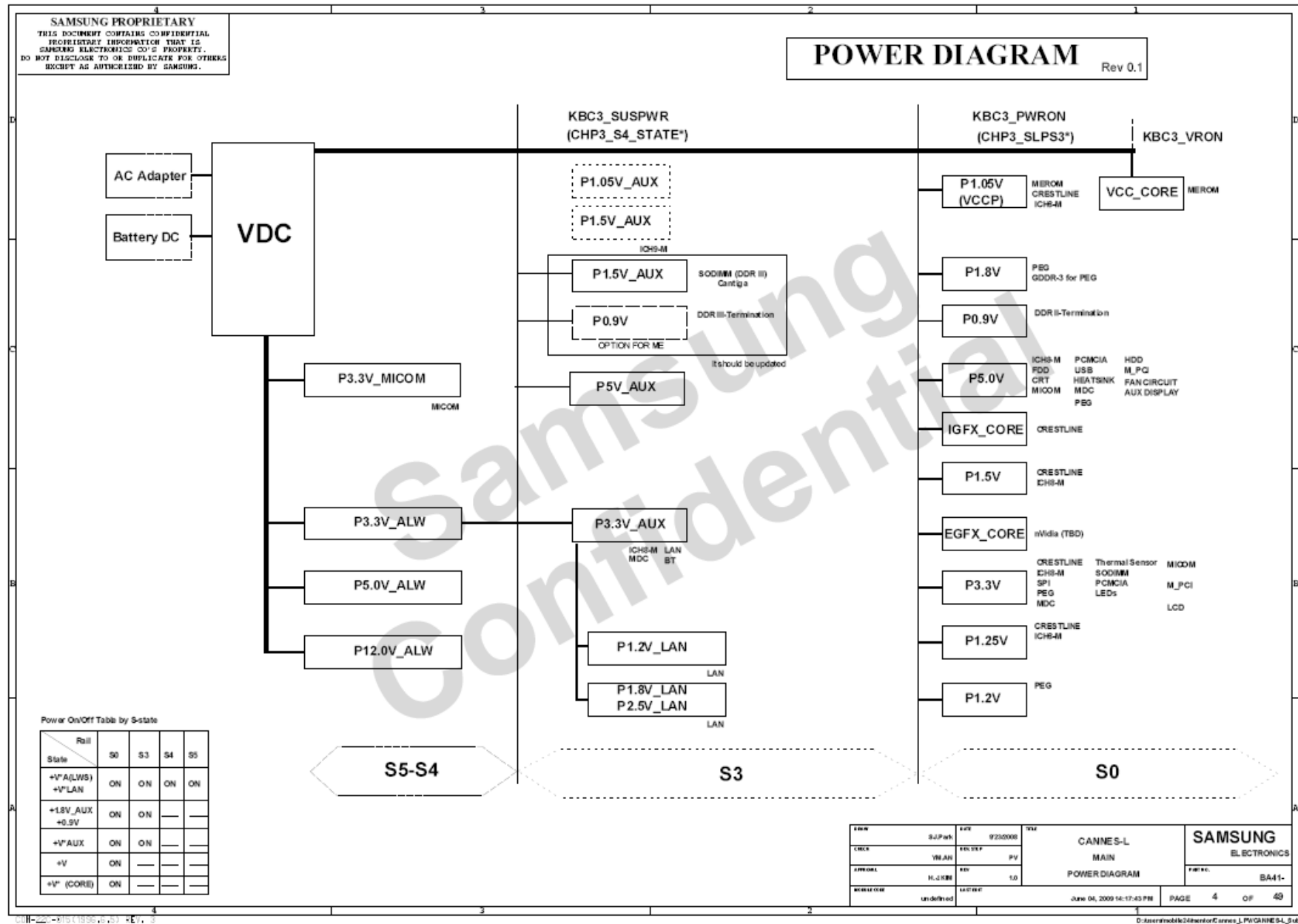
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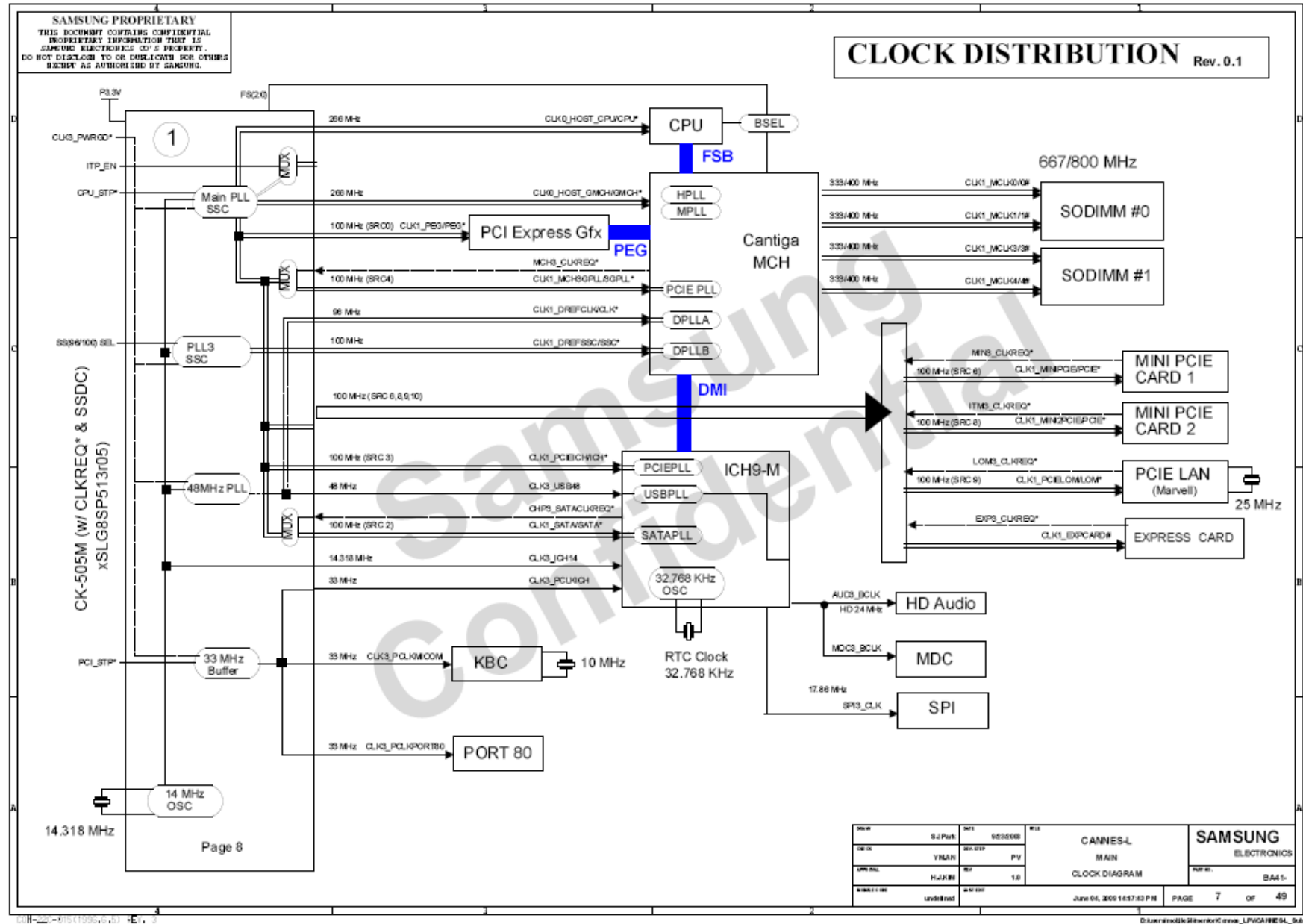
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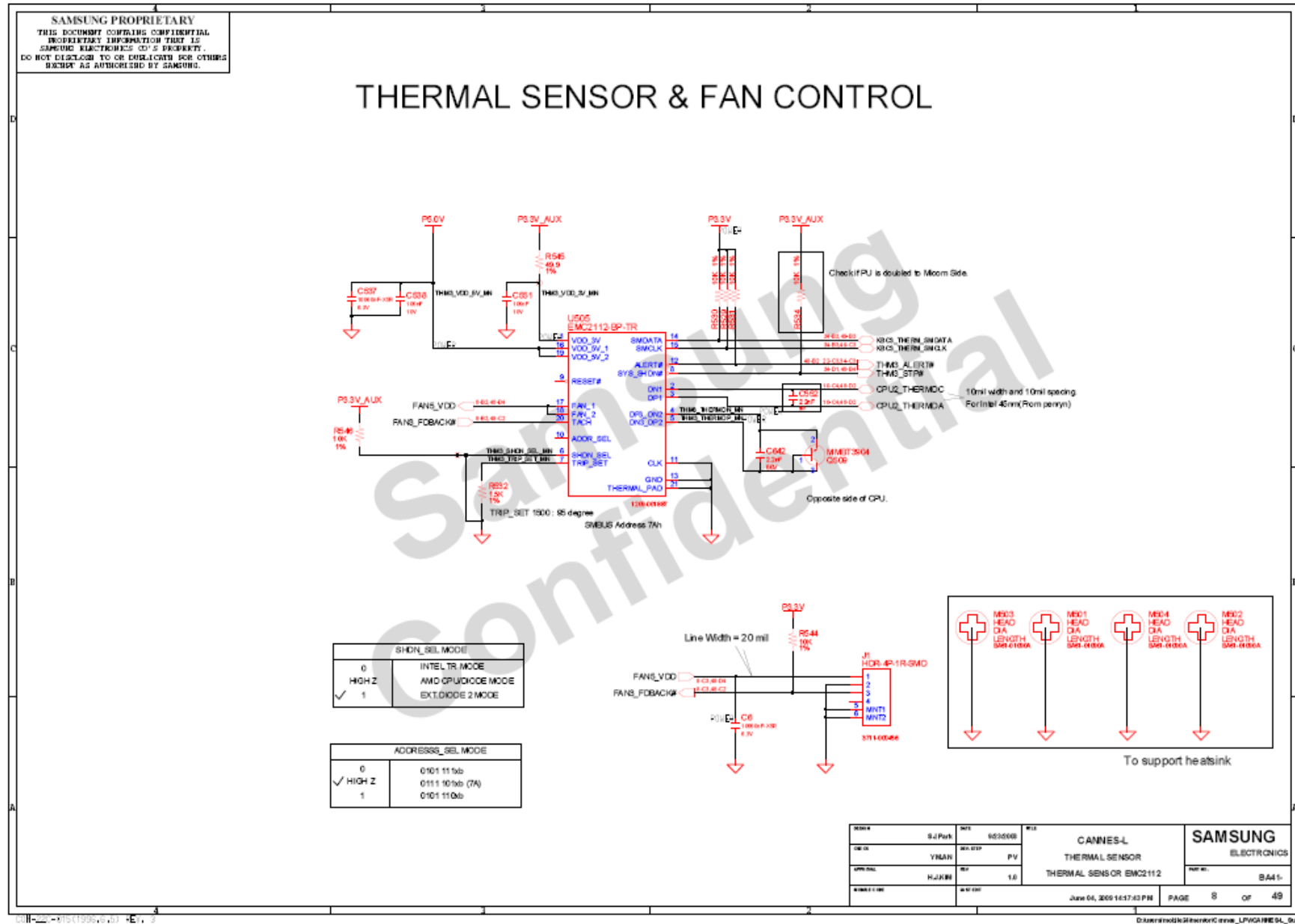
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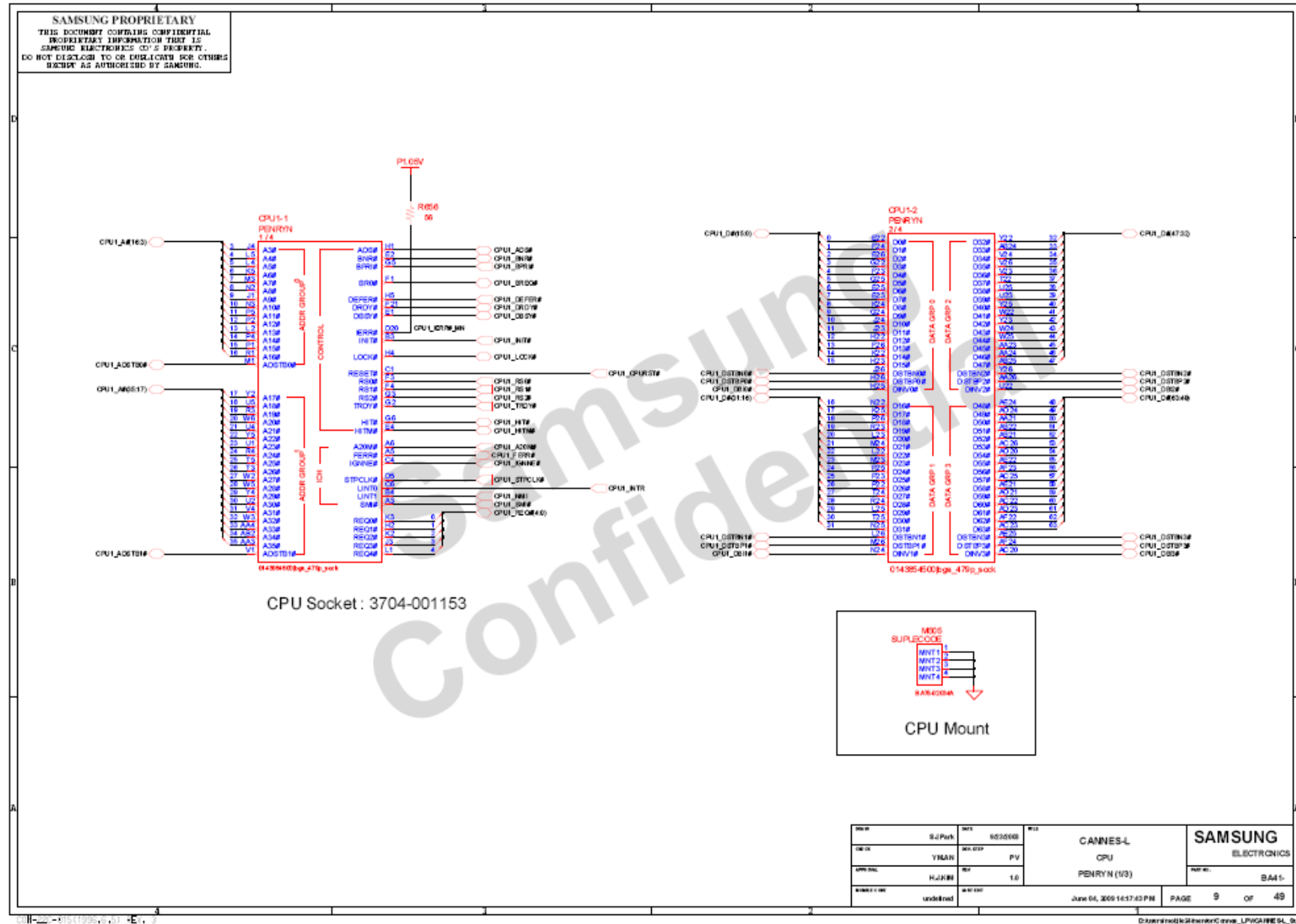
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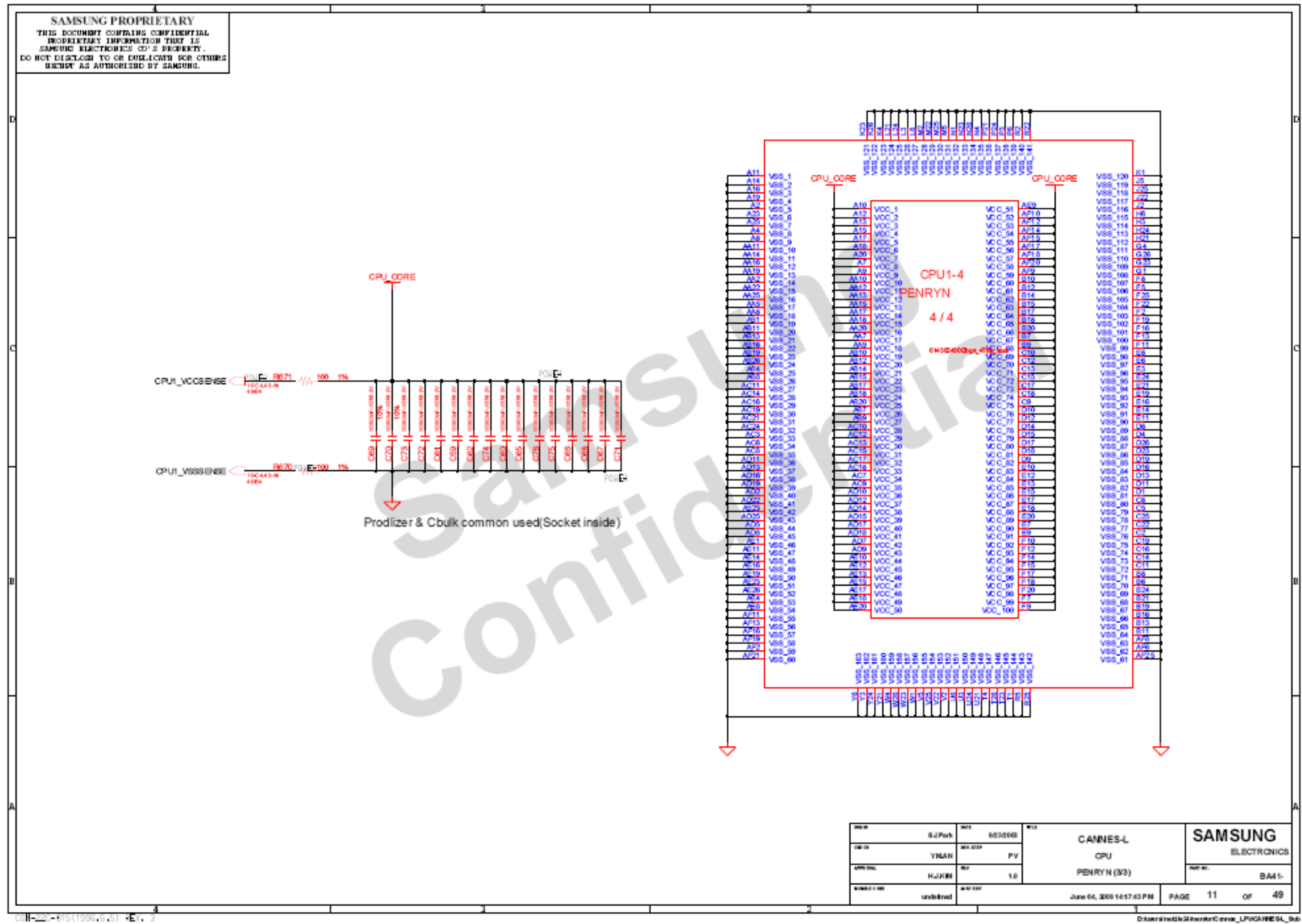
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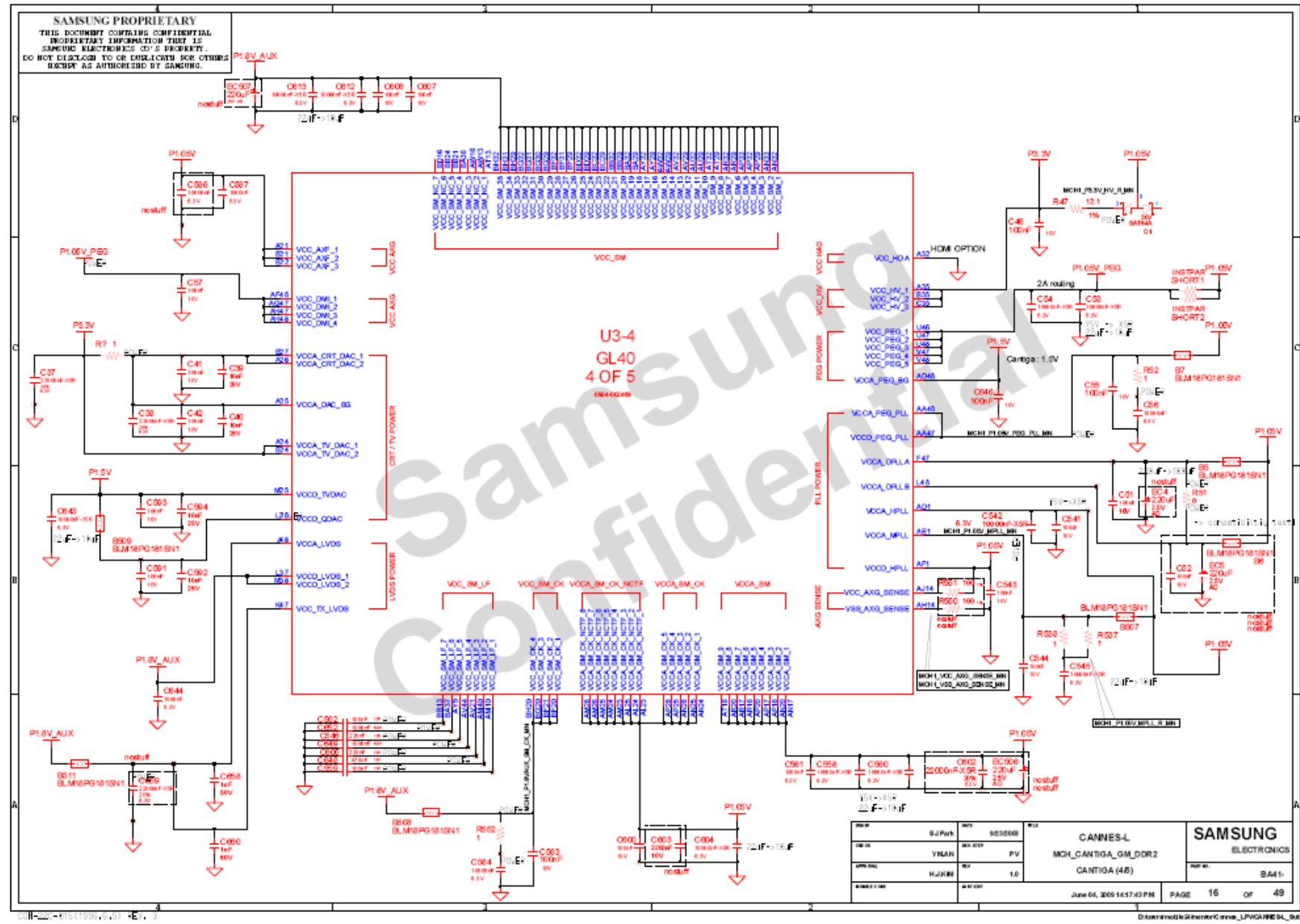
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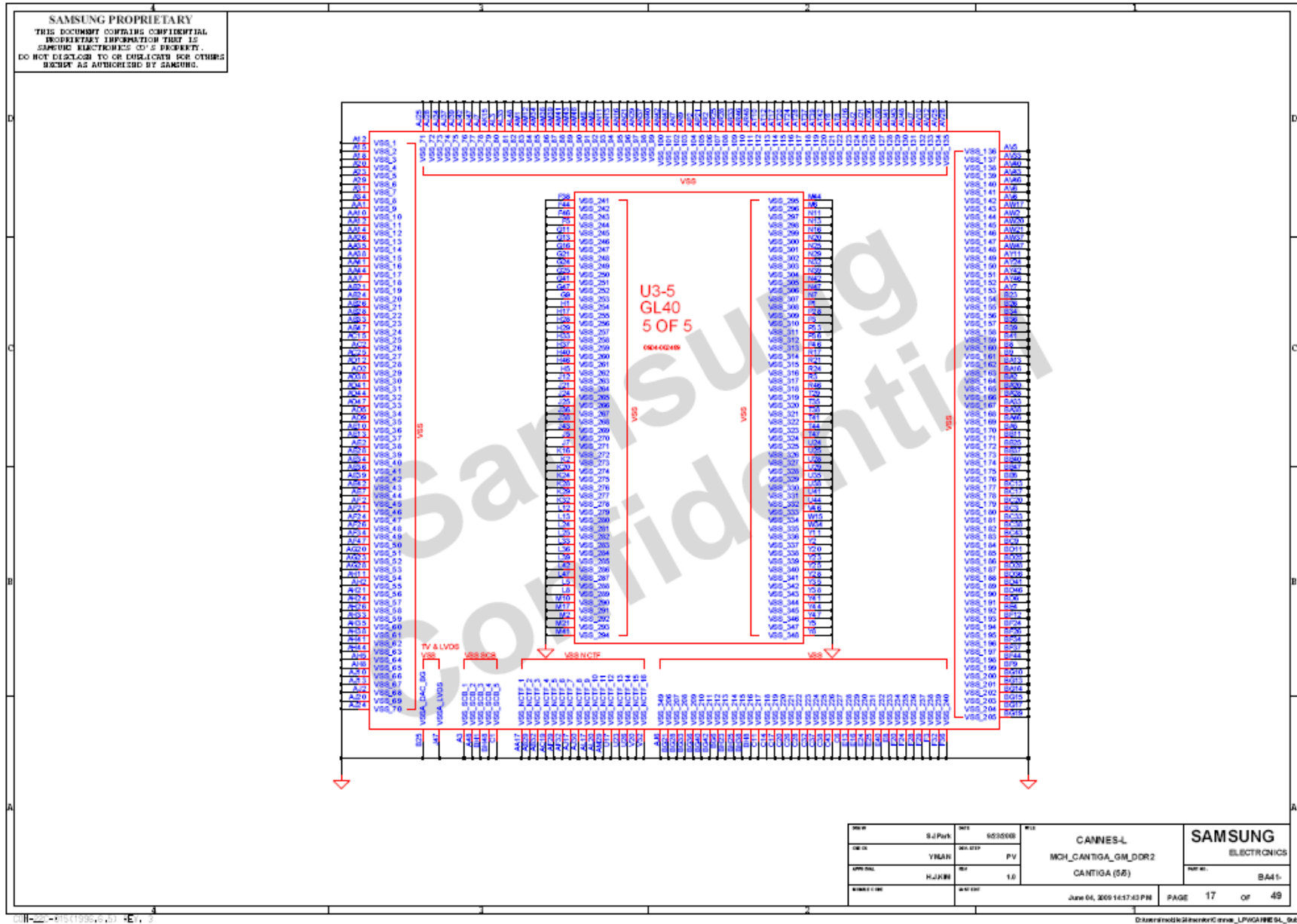


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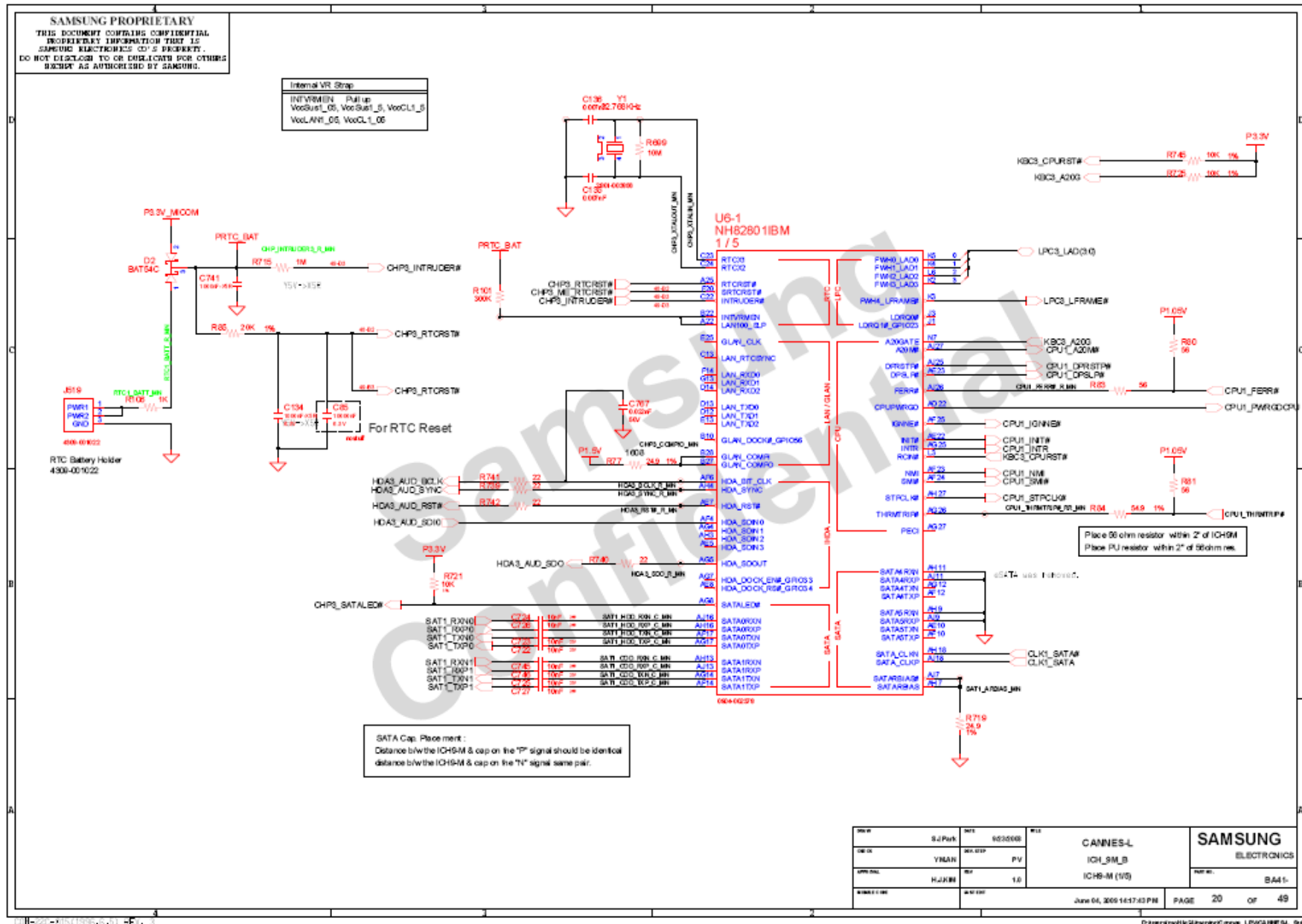
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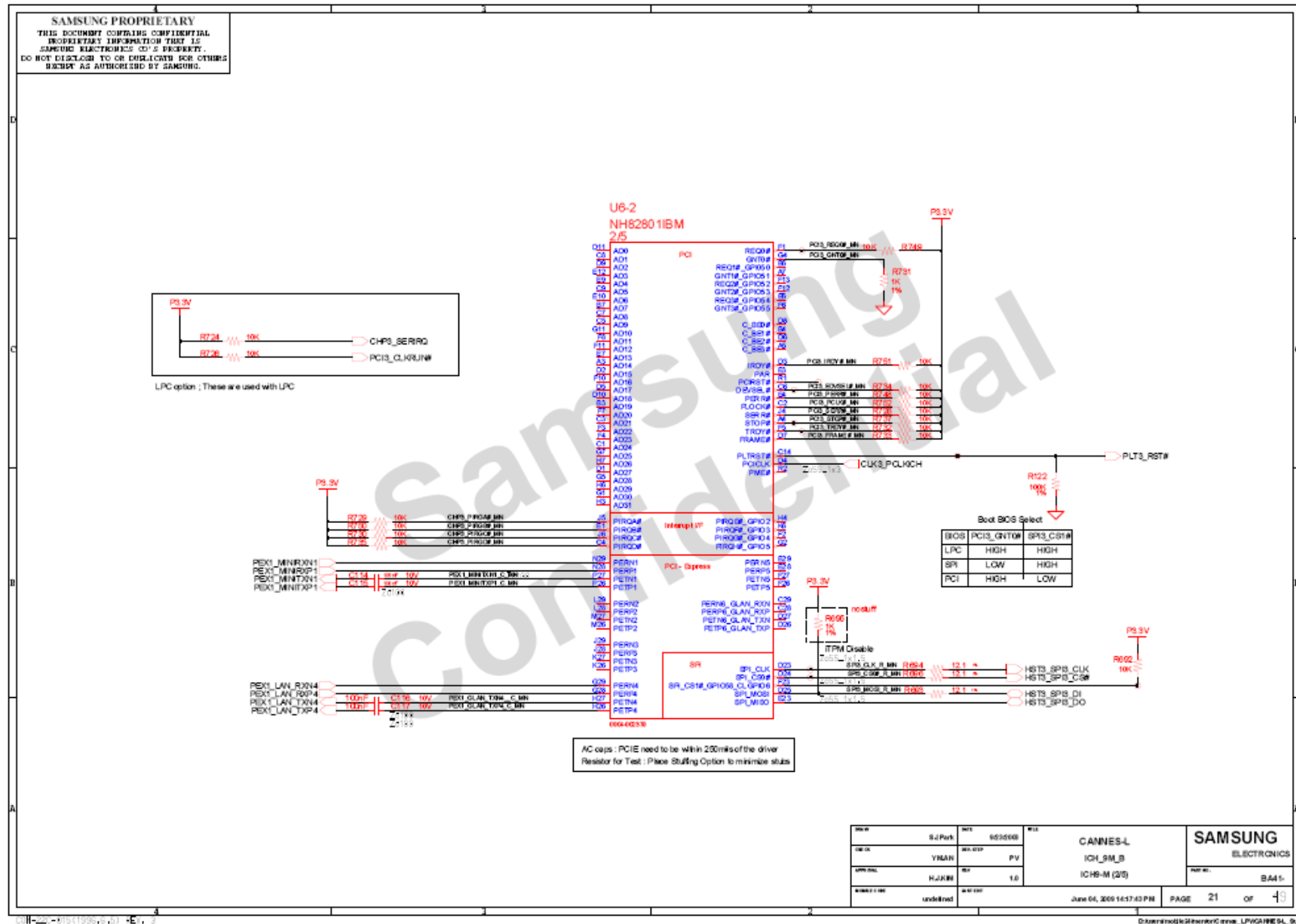
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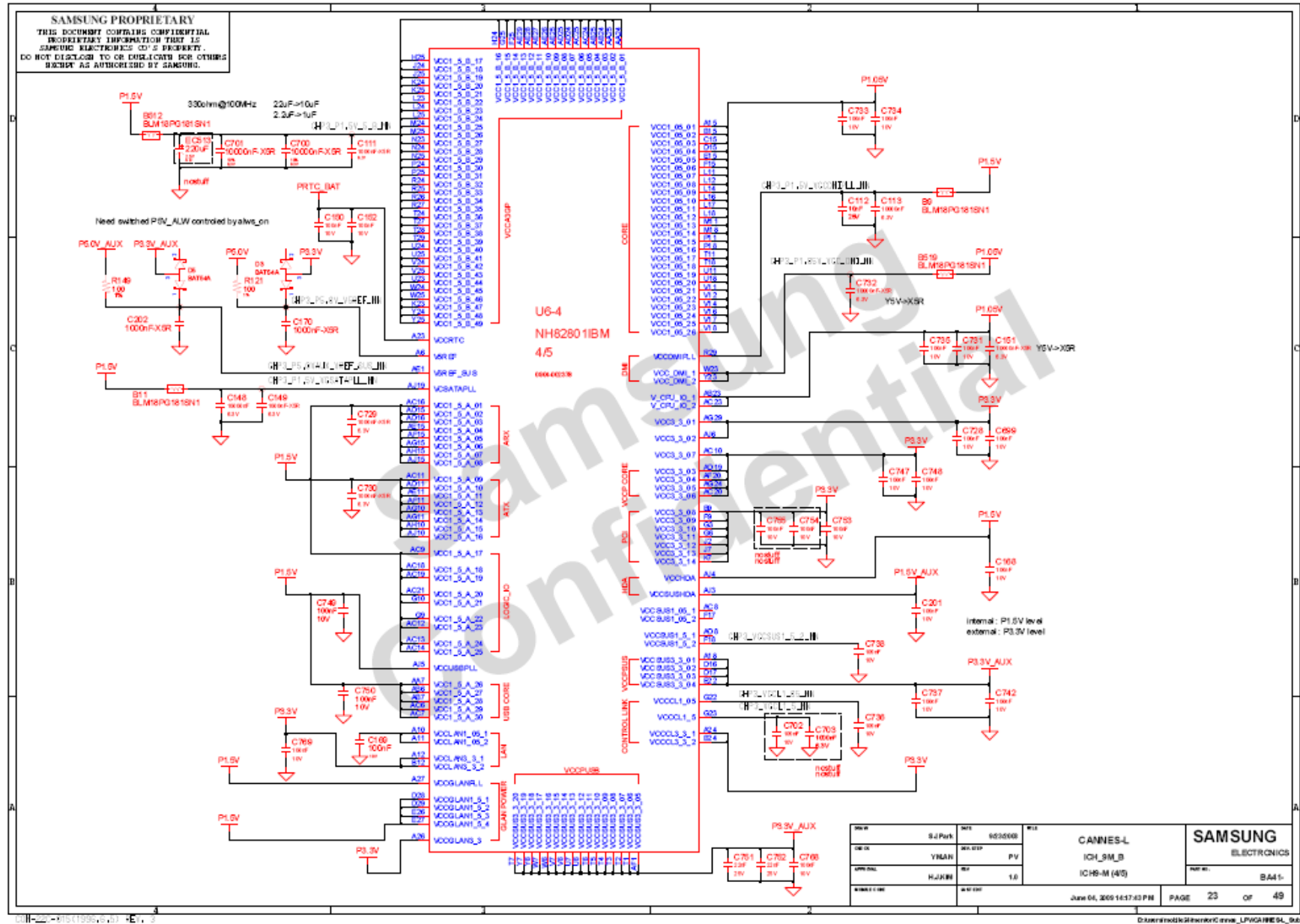
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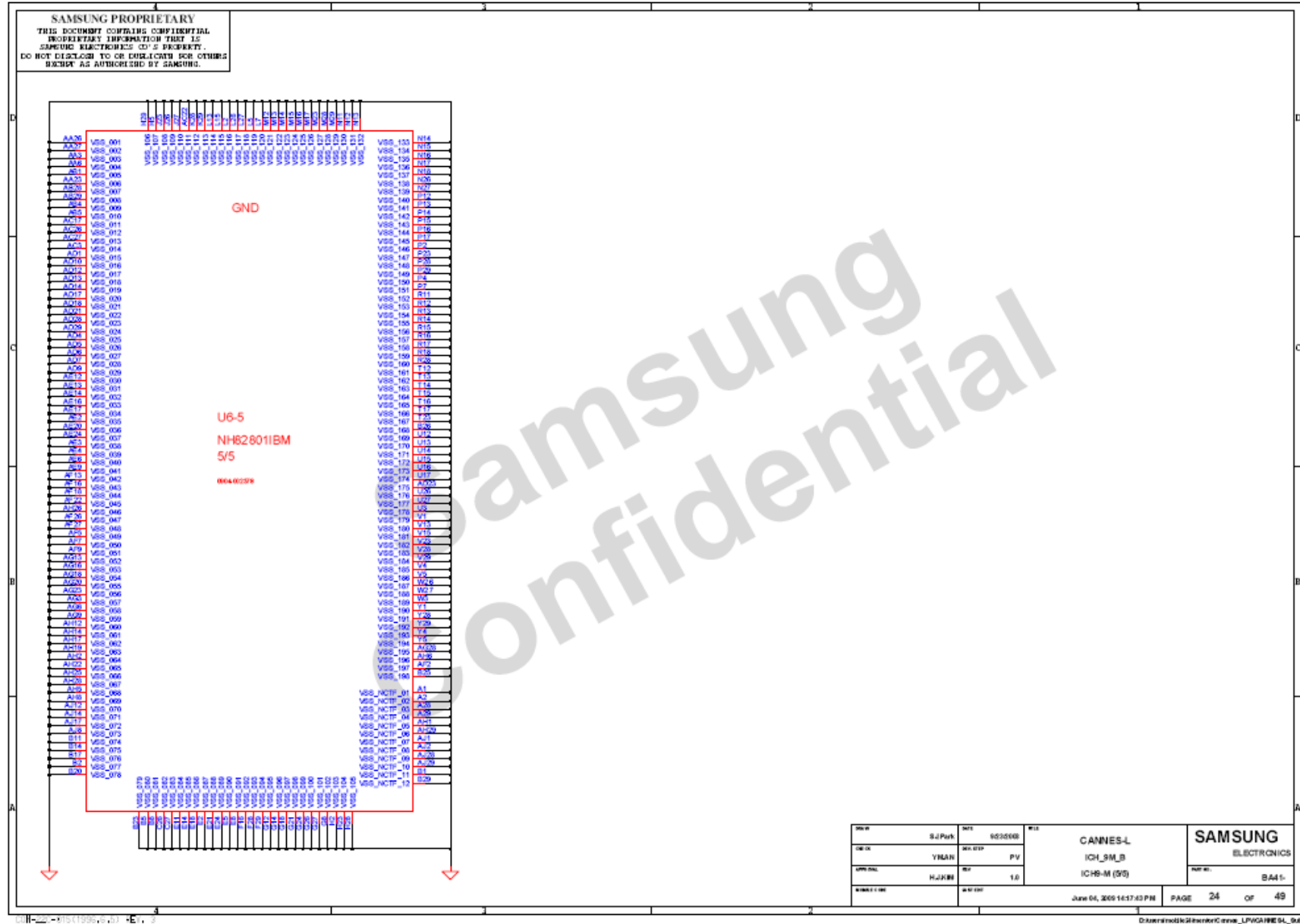
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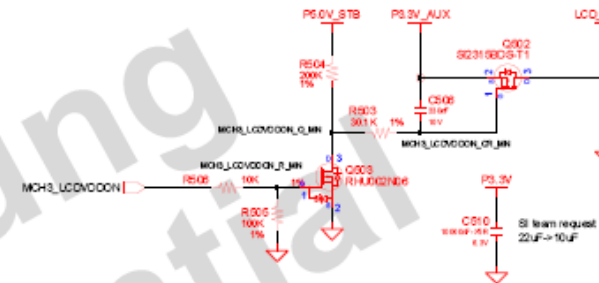


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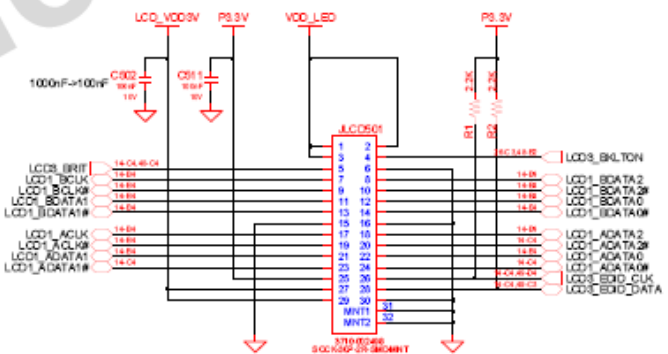


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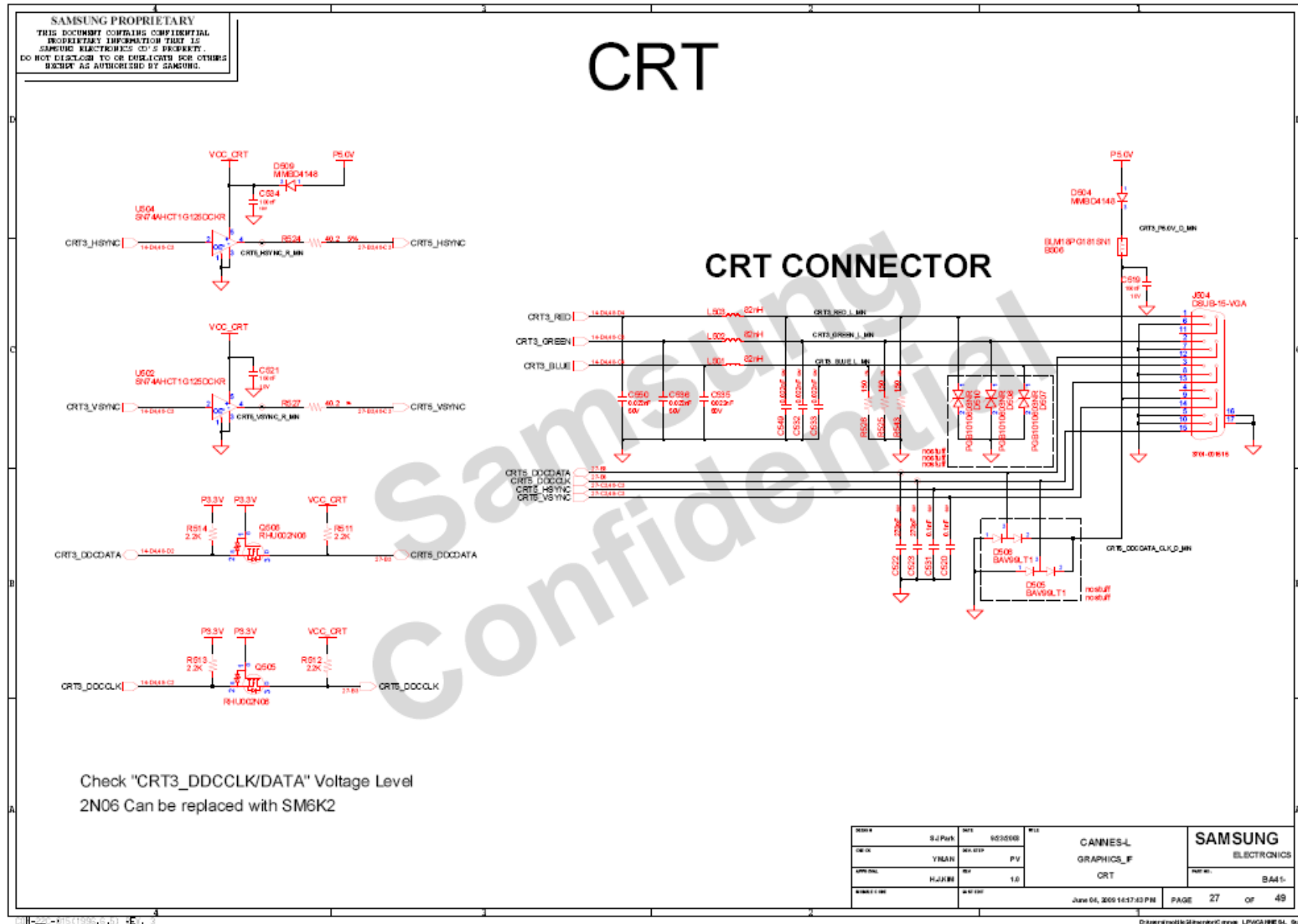


2Ch. LCD Connector

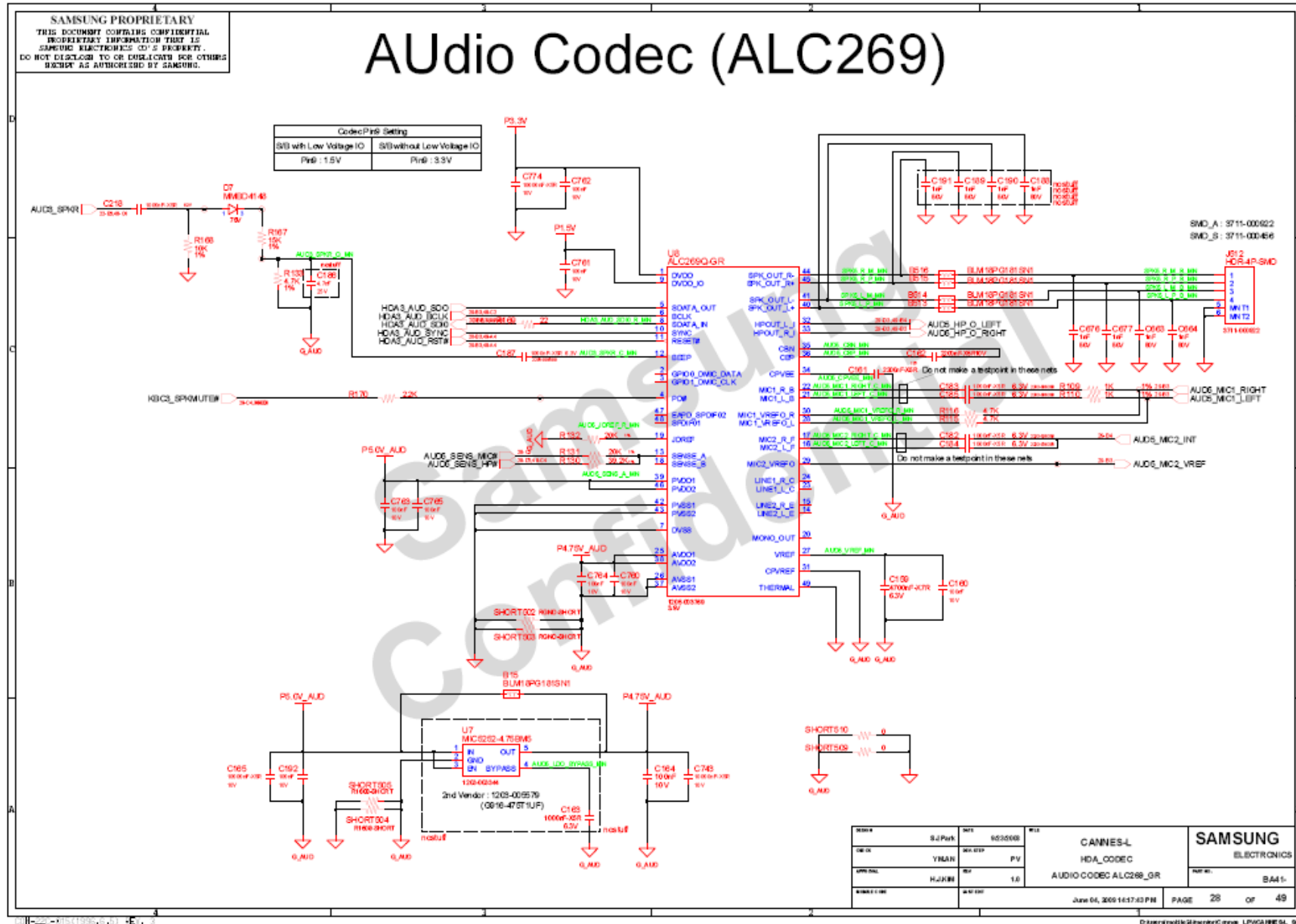


ISSUE #	DATE	ISSUED	CANNES_F GRAPHICS_L LVDS	SAMSUNG ELECTRONICS
DATE	ISSUED			
DATE	ISSUED			
DATE	ISSUED			
DATE	ISSUED			

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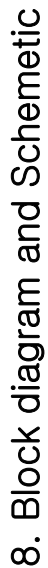
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8. Block diagram and Schematic



8. Block diagram and Schematic



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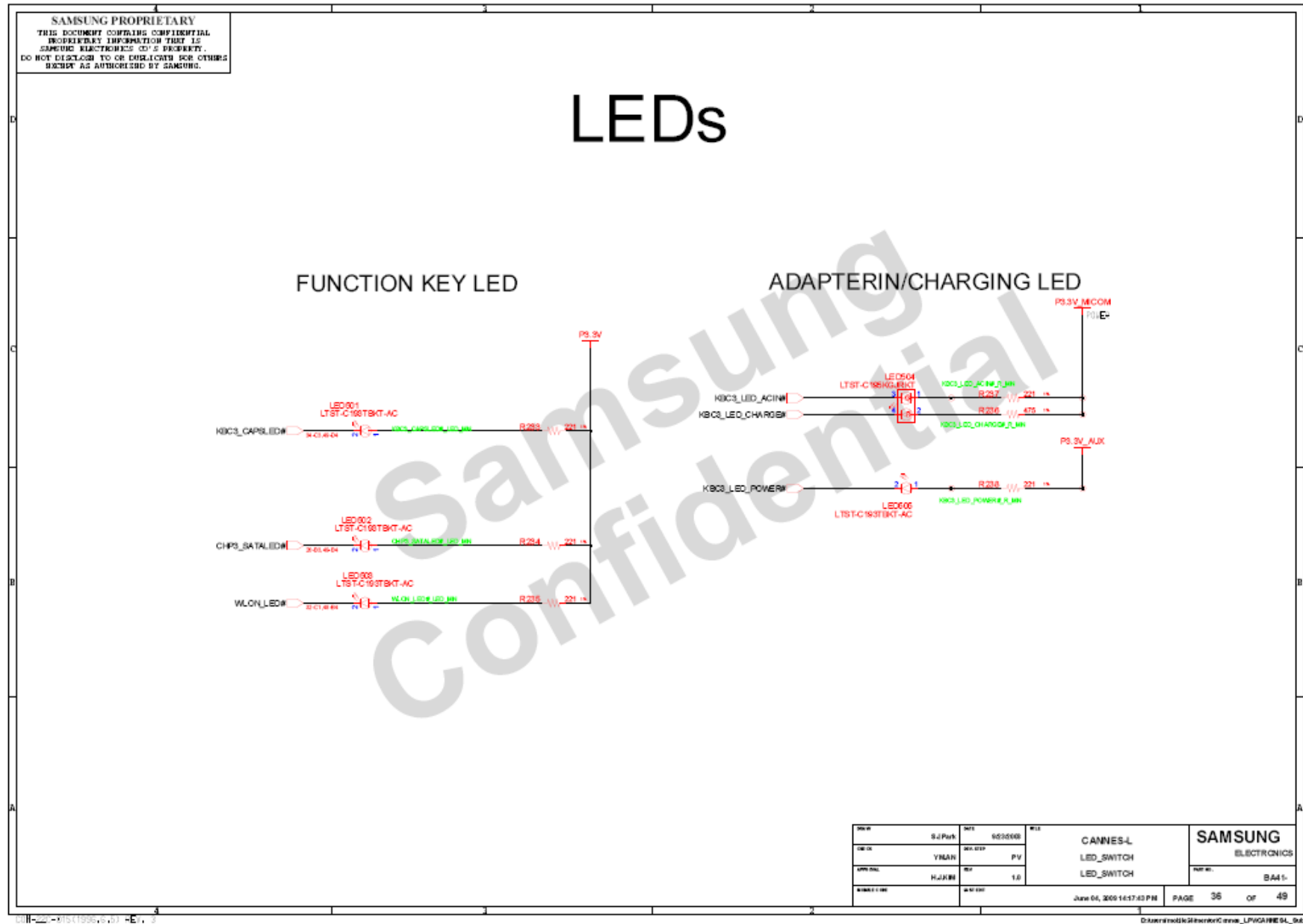
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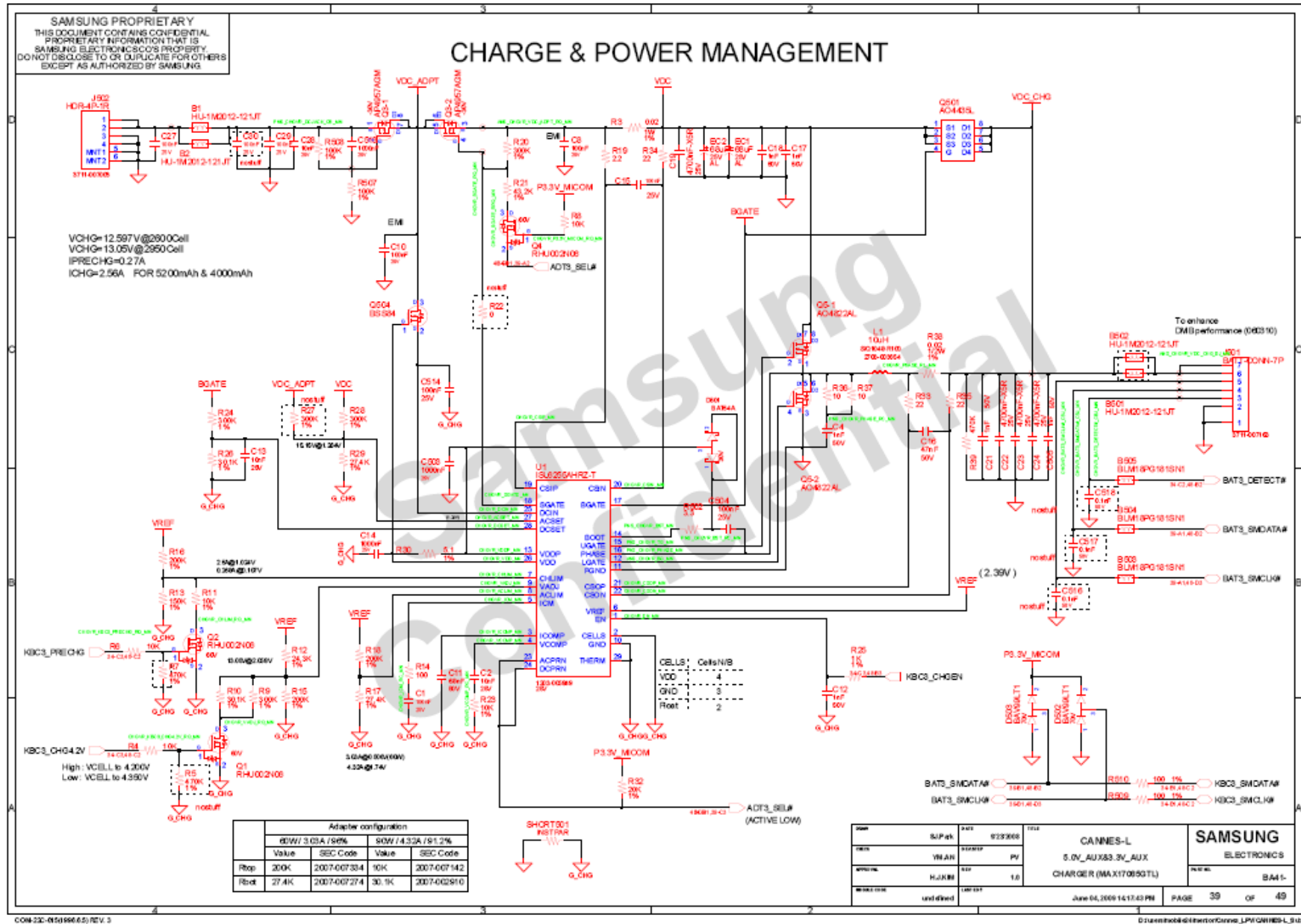
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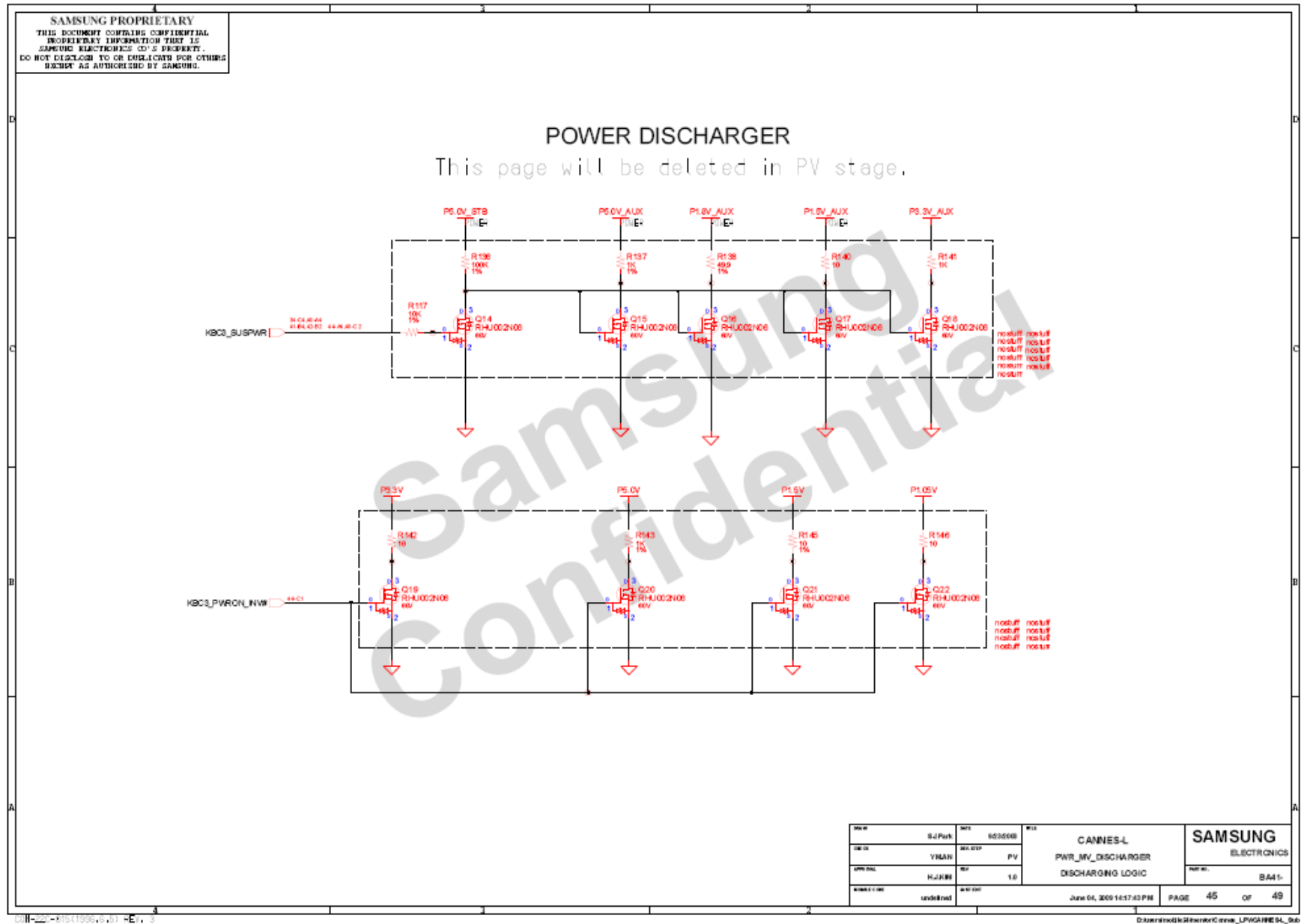
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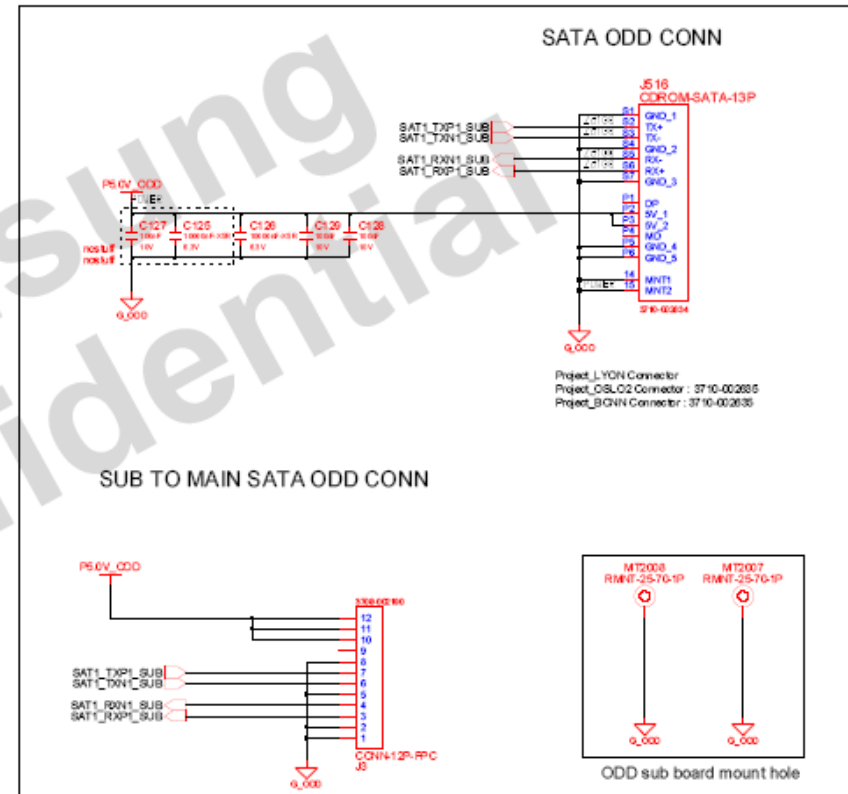
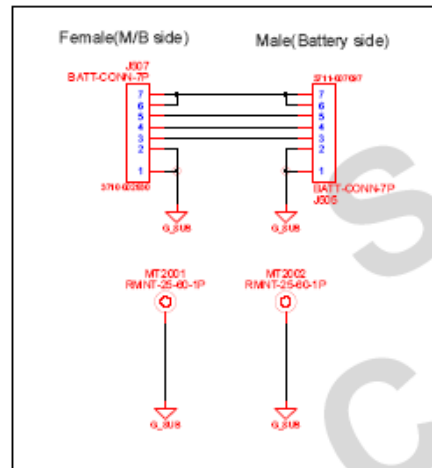


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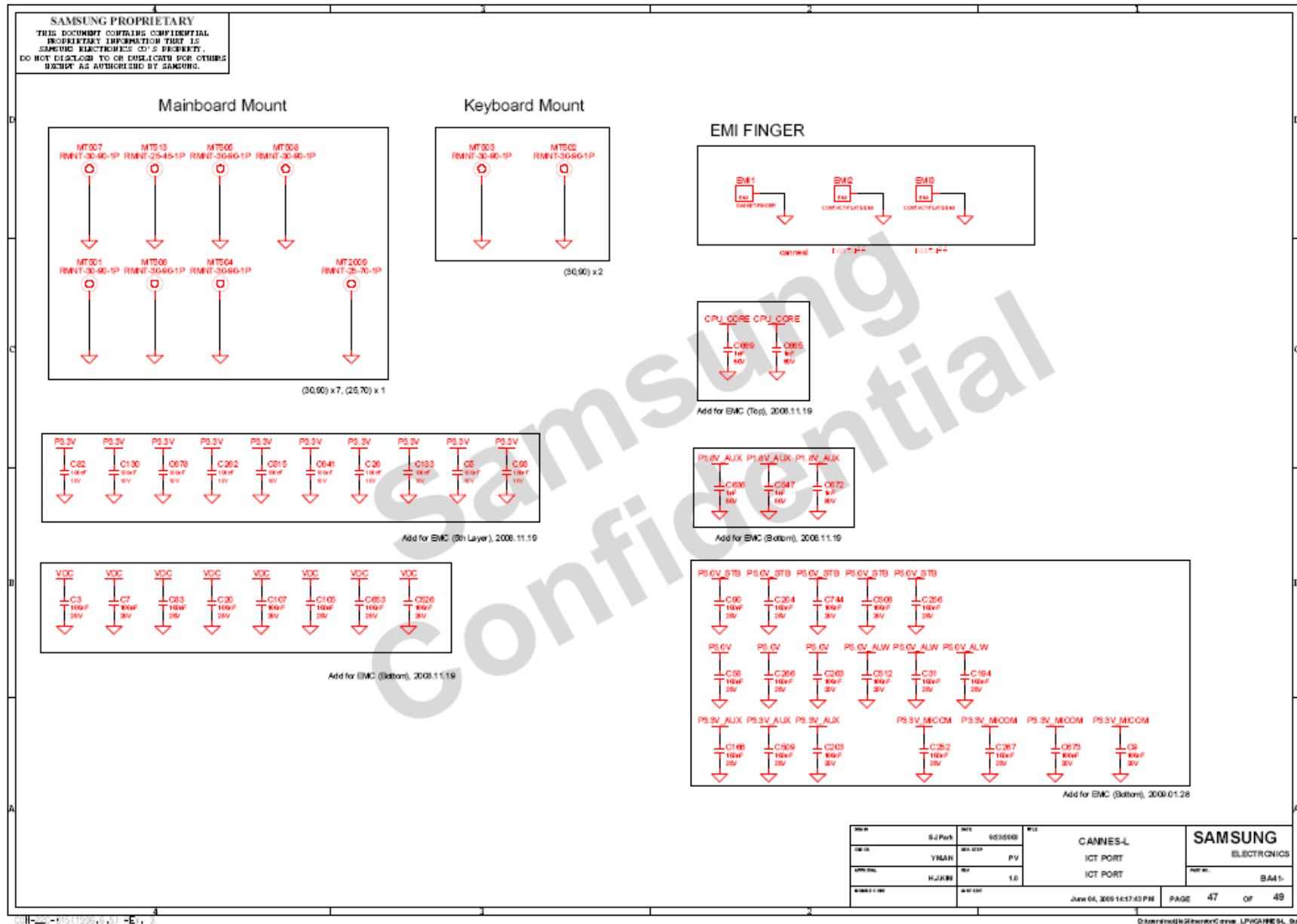
Battery & SATA ODD SUBBOARD

SATA ODD SUB BOARD



Rev. 01	S.J. Park	DATE	05/05/08	W.D.		CANNES-L	SAMSUNG
DR. 01	Y.N.A.R.	REV. 01	P.V.			SUB BOARD	ELECTRONICS
APPR. 01	H.J.H.B.	REV.	1.0			SATA ODD SUB BOARD	BA41-
DESIGNED BY	undrld	DATE	June 04, 2008 14:17:43 PM	PAGE	46	OF	49

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