8. Block Diagram and Schematic

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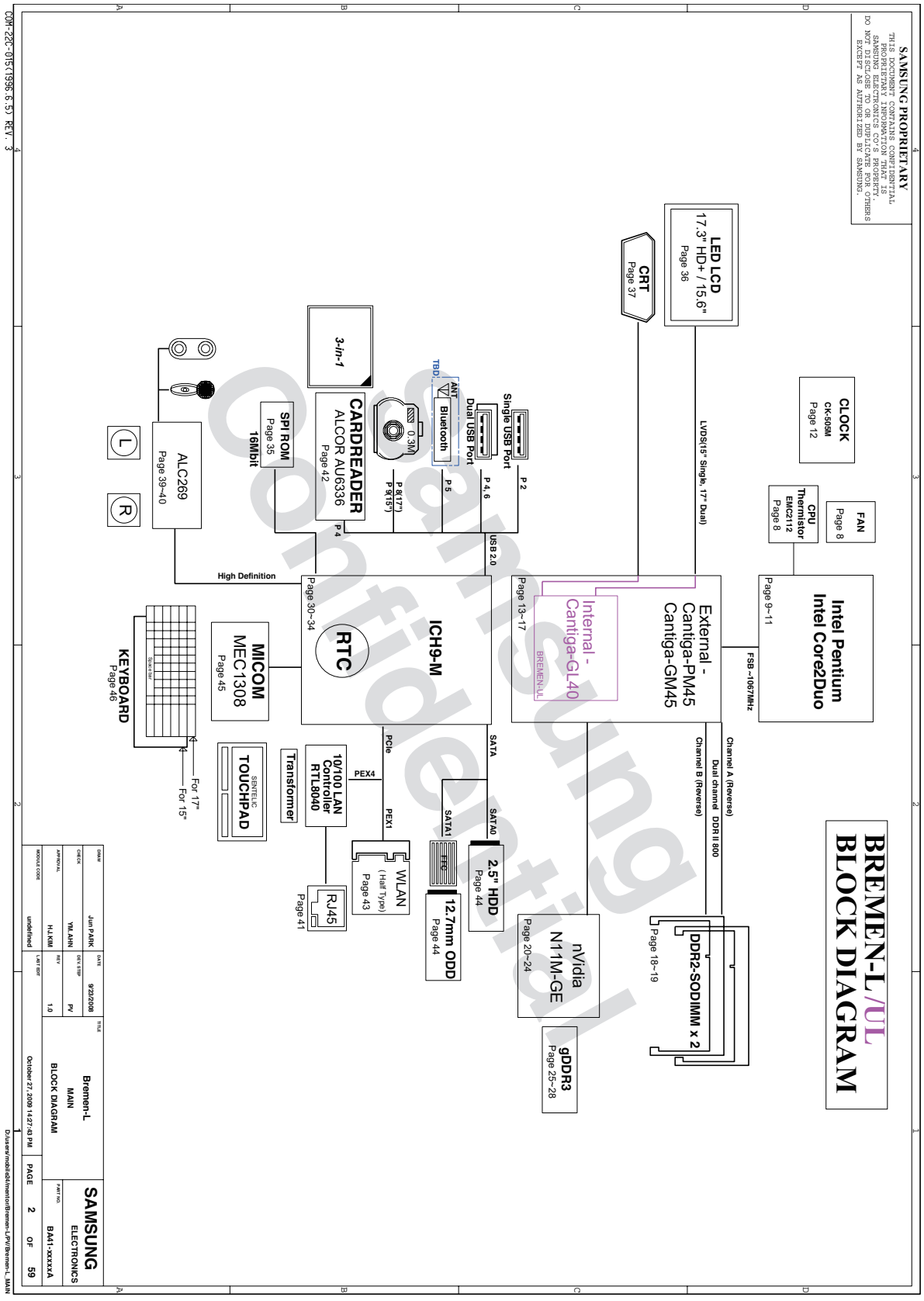


BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9M	**Master**		**SMBUS Master**
CK-505M (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000X	A0h	-
SODIMM1	1010 001X	A4h	
MICOM	**Master**		
BATTERY	0001 011X	16h	
EMC2102	0111 101X	7Ah	

USB PORT Assignation

Port Number		ASSIGNED TO	Port Number		ASSIGNED TO
UHCI_0	0	USB PORT (RIGHT, SUB)	UHCI_3	6	USB PORT (RIGHT, SUB)
	1			7	
UHCI_1	2	USB PORT (LEFT)	UHCI_4	8	CAMERA(17")
	3			9	CAMERA(15")
UHCI_2	4	CARD READER(AU6336)	UHCI_5	10	
	5	BLUETOOTH(TBD)		11	

SATA Assignation

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
SATA0	HDD	SATA1	ODD
SATA2	-	SATA3	-

PCI EXPRESS Assignation

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
PCIe1	WLAN	PCIe2	Wired LAN
PCIe3	-	PCIe4	-

Crystal / Oscillator

TYPE	PREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	
Crystal	10MHz	MICOM	
Crystal	14.318MHz	CLOCK-Generator	
Crystal	25MHz	LAN	

Voltage Rails

Power Rail	Descriptions	Power Rail	Descriptions
VDC_ADPT	Primary DC system power supply (9 to 19V)	***P1.05V_PEG***	P1.05V (Direct Media Interface Compensation)
VDC		***P5.0V***	5.0V Power Rail (off in S3-S5)
VDC_CHG	Charger Reference Voltage Source	***P3.3V***	3.3V Power Rail (off in S3-S5)
PRTC_BAT	3.3V supply for the RTC well.	***P1.05***	1.05V Power Rail (off in S3-S5)
P5.0V_ALW	5.0V always power well	***P0.9V***	DDR2 Termination
P12.0V_ALW	12.0V always power well	***P5.0V_AUX***	5.0V Power Rail (off in S4-S5)
P1.7V_VREF	Power Chip Reference	***P3.3V_AUX***	3.3V Power Rail (off in S4-S5)
P2.0V_VREF	Power Chip Reference	***P1.8_AUX***	1.8V Power Rail (off in S4-S5)
P5.0V_VREF_FILT	Power Chip Reference	***CPU_CORE***	Core Voltage for CPU
P3.3V_MICOM	Output voltage of RT8205AGQW (if VDC is removed, it will be off)	***AUD_P5V***	5.0V supply for Audio
LCD_VDD3V	3.3V (LED LCD)	***P4.75V_AUD***	Auido Analog Voltage
KBC3_CHG4.2V	To charge battery	***P5.0V_STB***	To charge USB device at sleep status
		P5.0V_ODD	5.0V supply at SUB_ODD Board
P1.2V_LAN	Internal Regulator's Power of LAN Controller	***EGFX_CORE***	nVidia Graphic Chip power
P2.5V_LAN		***P1.5V***	1.5V Power Rail (off in S3-S5)
		P1.5_AUX	1.5V Power Rail (off in S4-S5)
P3.3V_MCD	3.3V (3-in-1 Socket)	***P1.8V***	1.8V Power Rail (off in S3-S5)

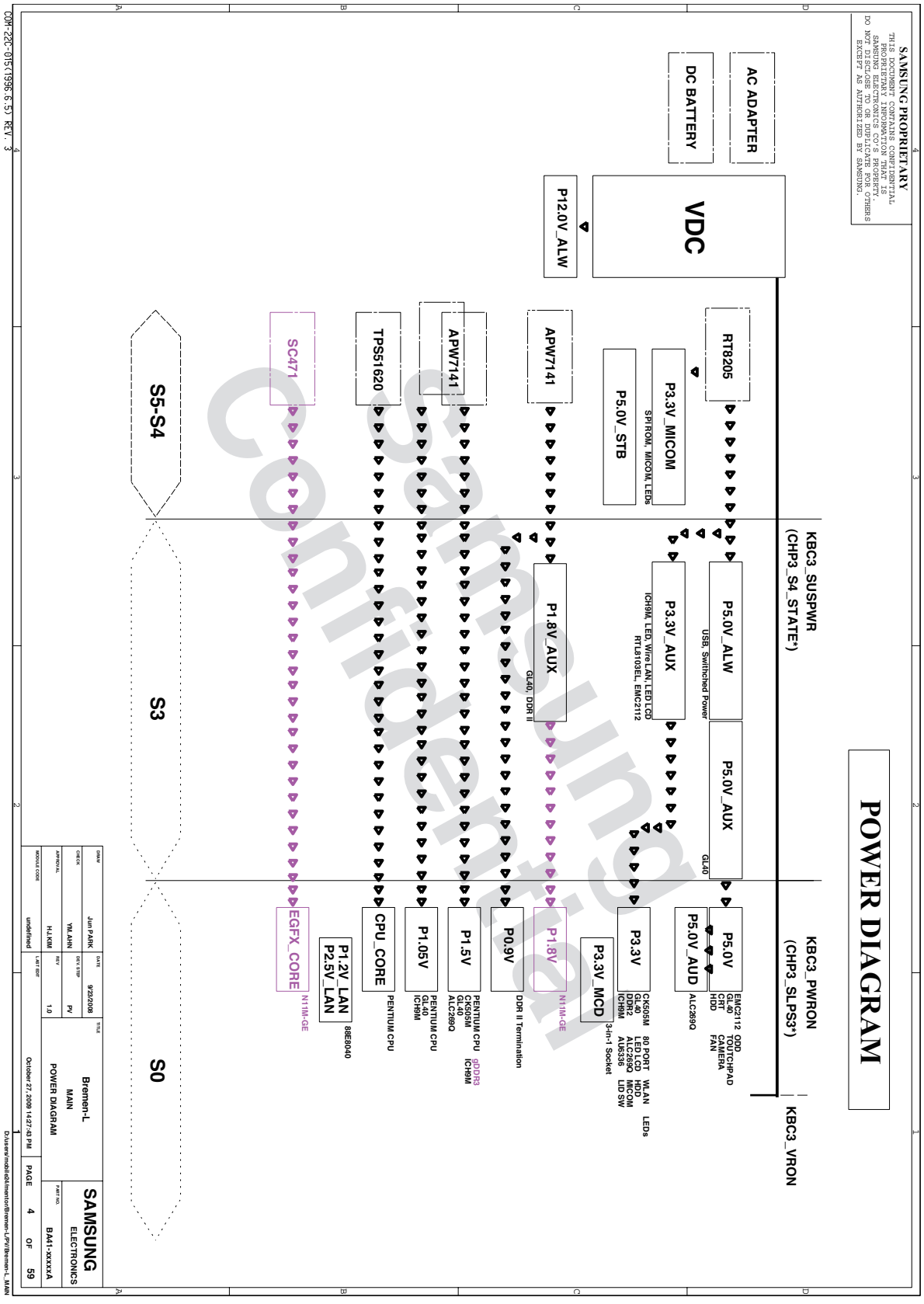
Power source of External

REVISION HISTORY

See rev notes for more information.

DRAW: Jun PARK	DATE: 9/23/2008	TITLE: Bremen-L / MAIN / BOARD INFO	SAMSUNG ELECTRONICS
CHECK: YM.AHN	DEV. ST'EP: PV		
APPROVAL: HJ.KIM	REV: 1.0		PART NO.: BA41-xxxxxA
MODULE CODE: undefined	LASTEDIT: October 27, 2009 14:27:43 PM	PAGE 3 OF 59	

8. Block Diagram and Schematic



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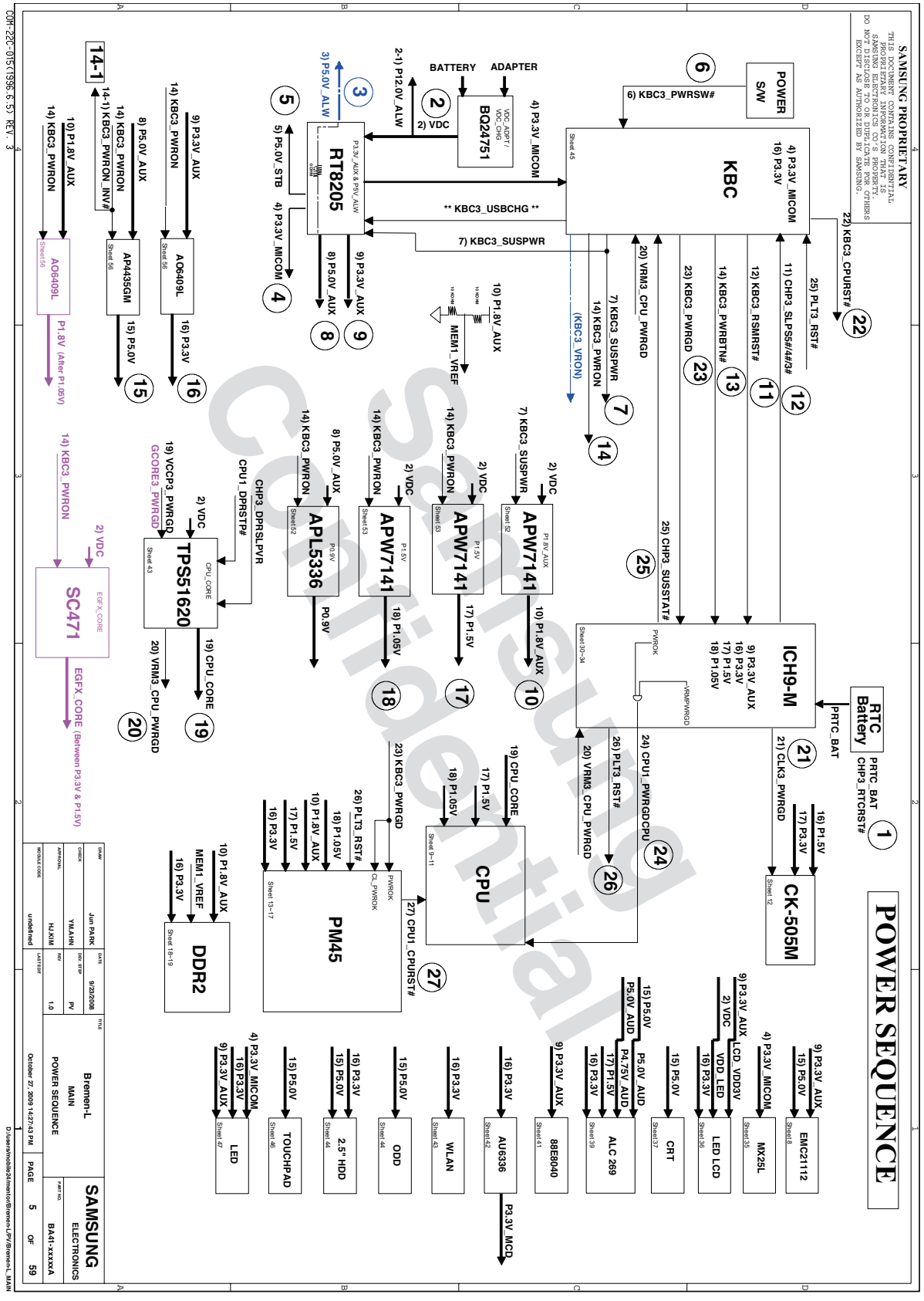

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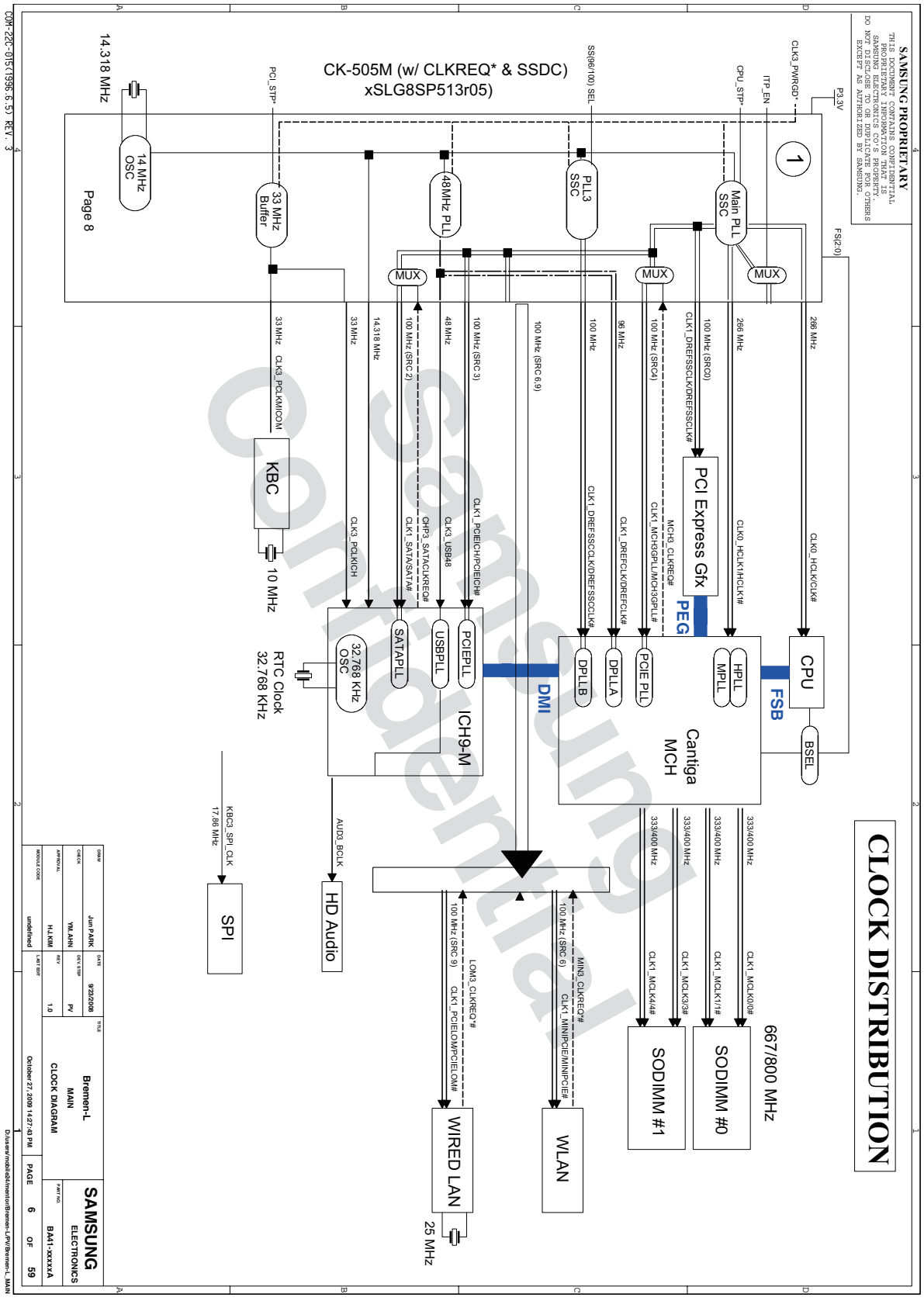

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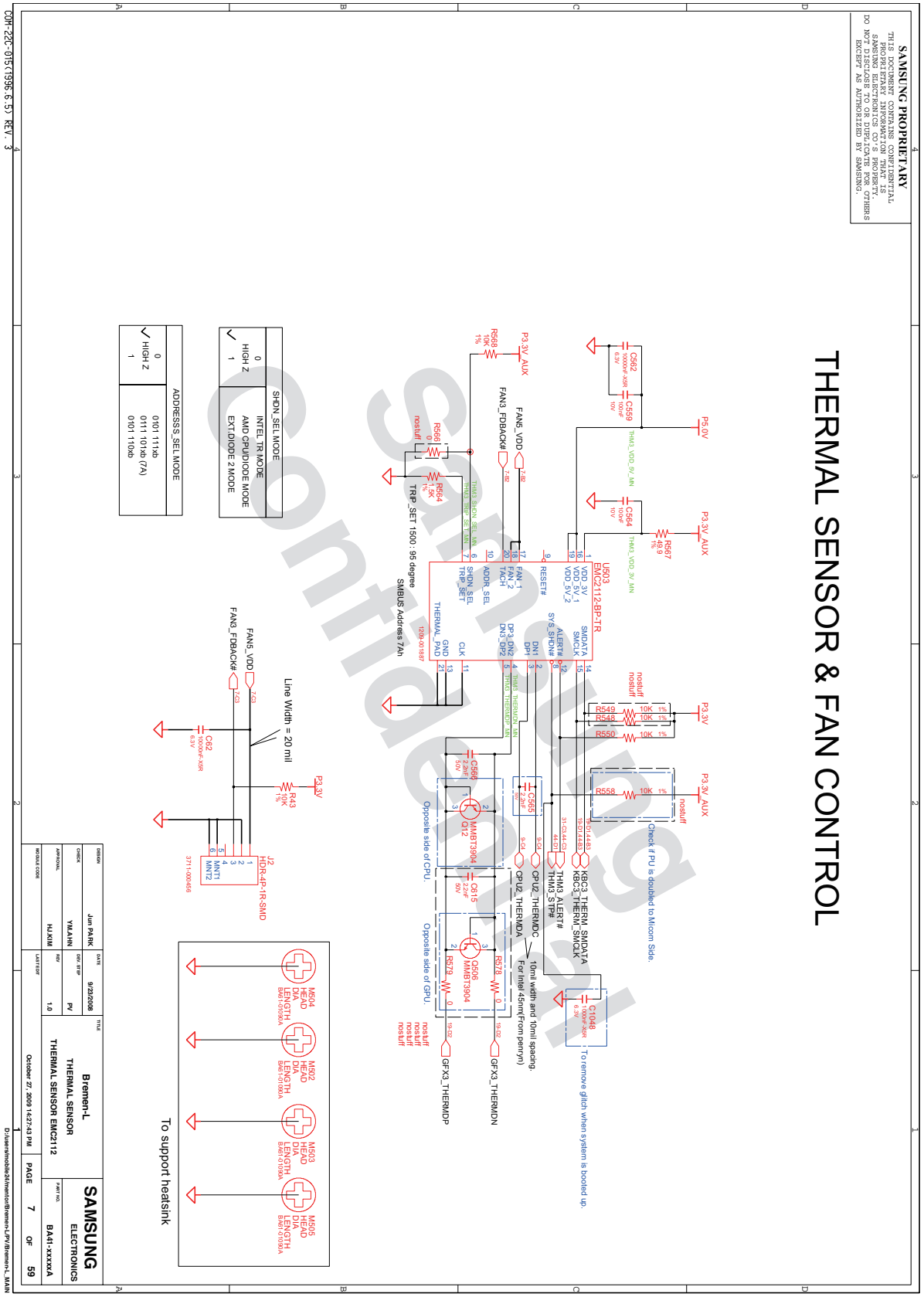

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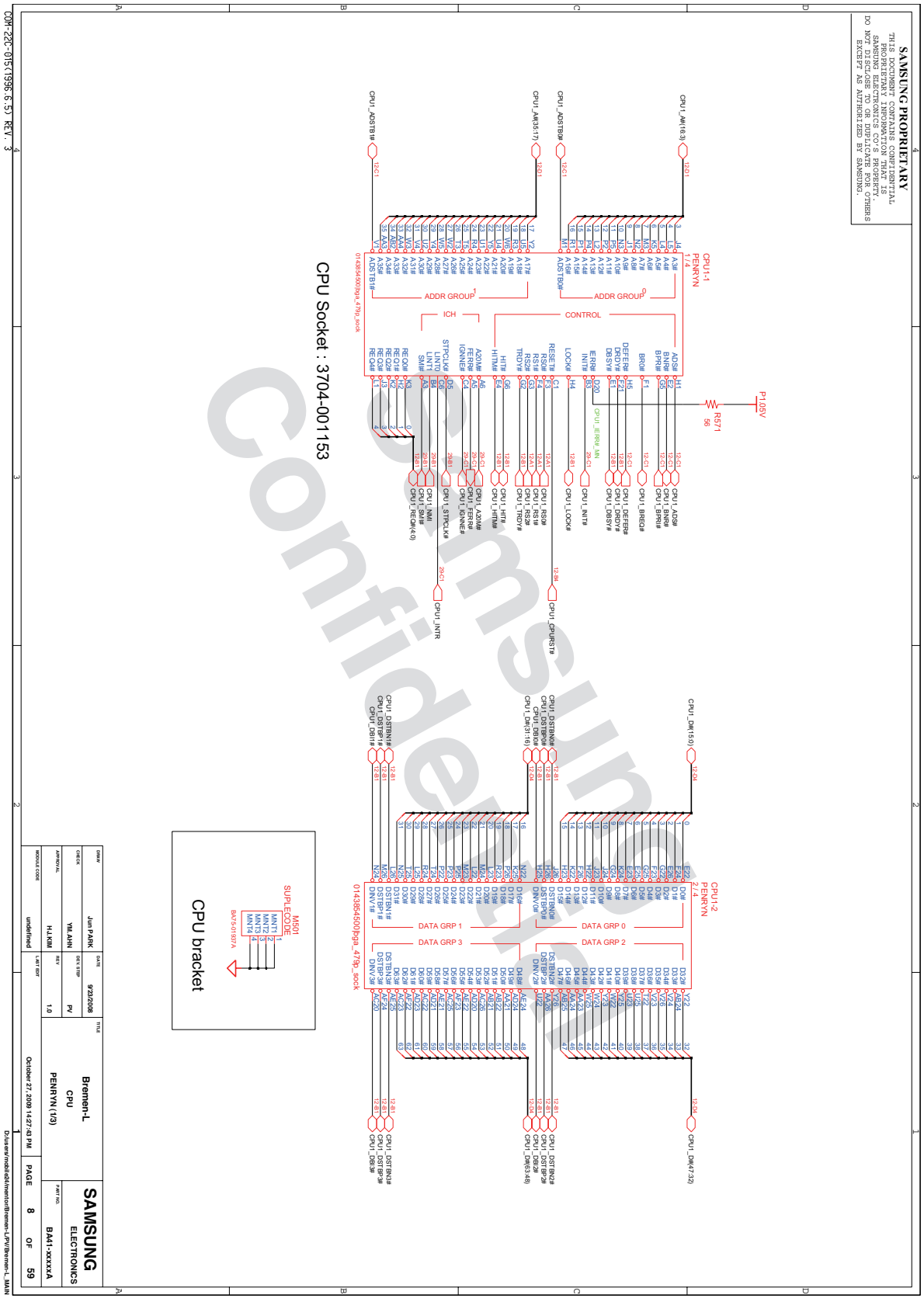

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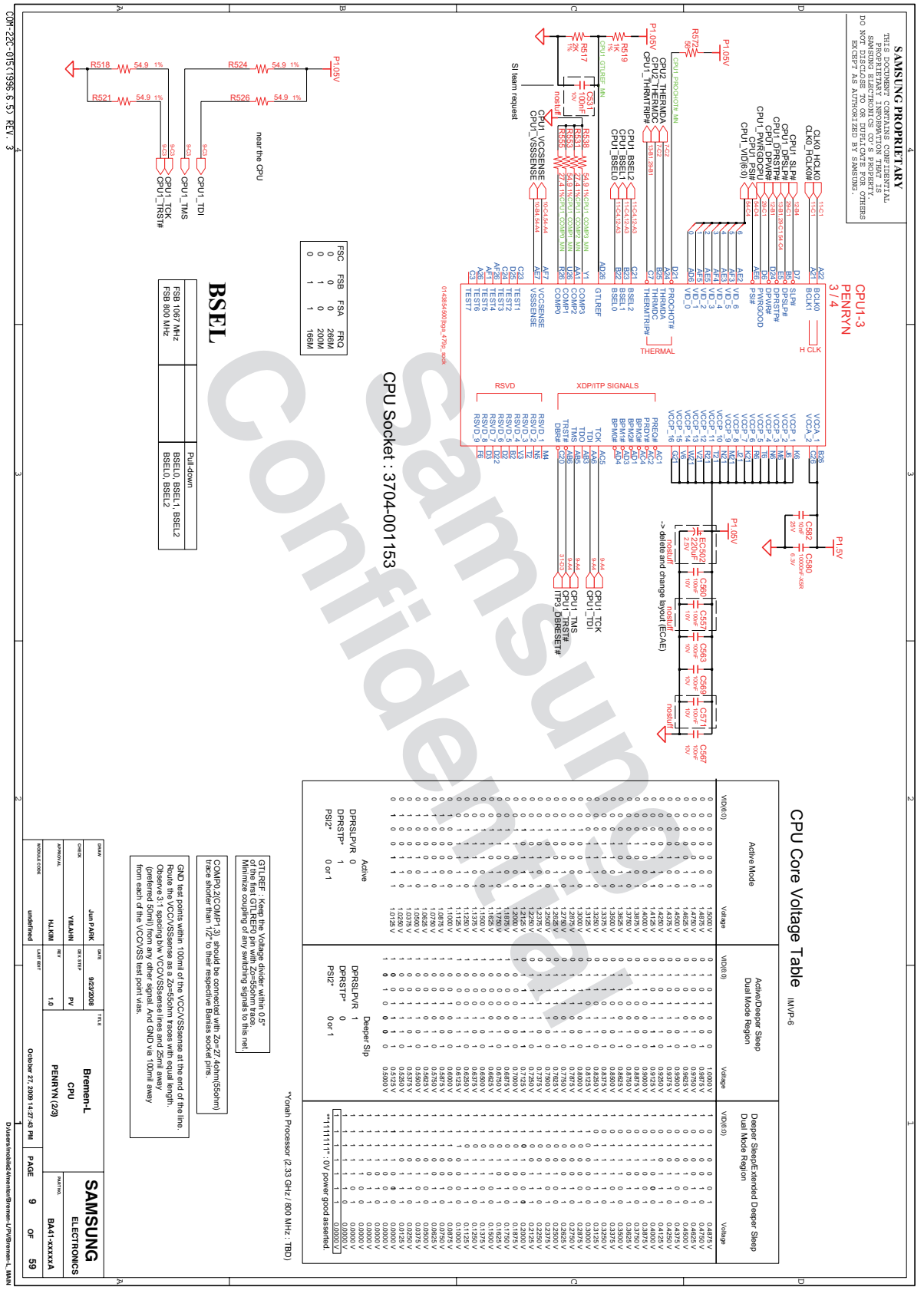

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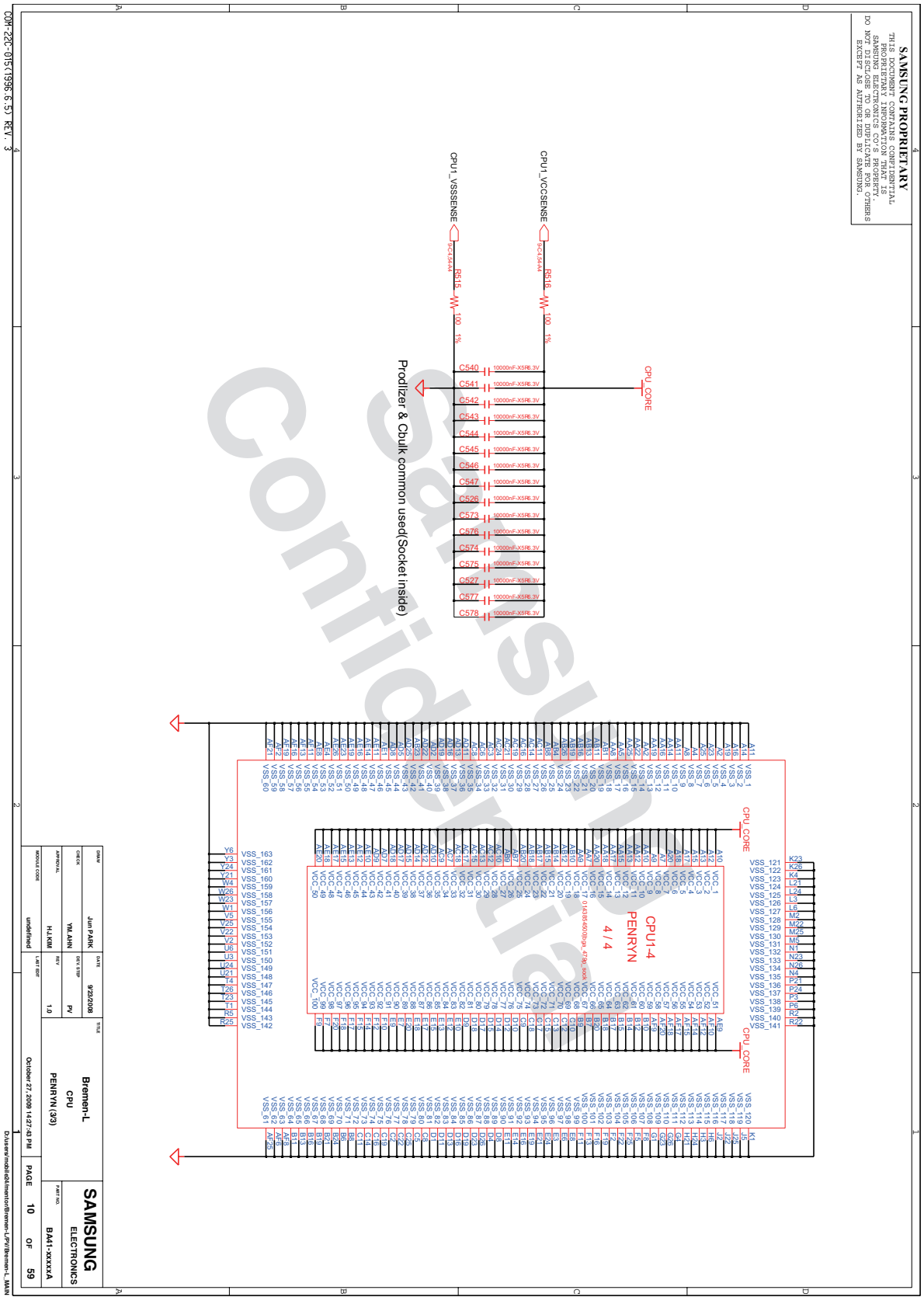

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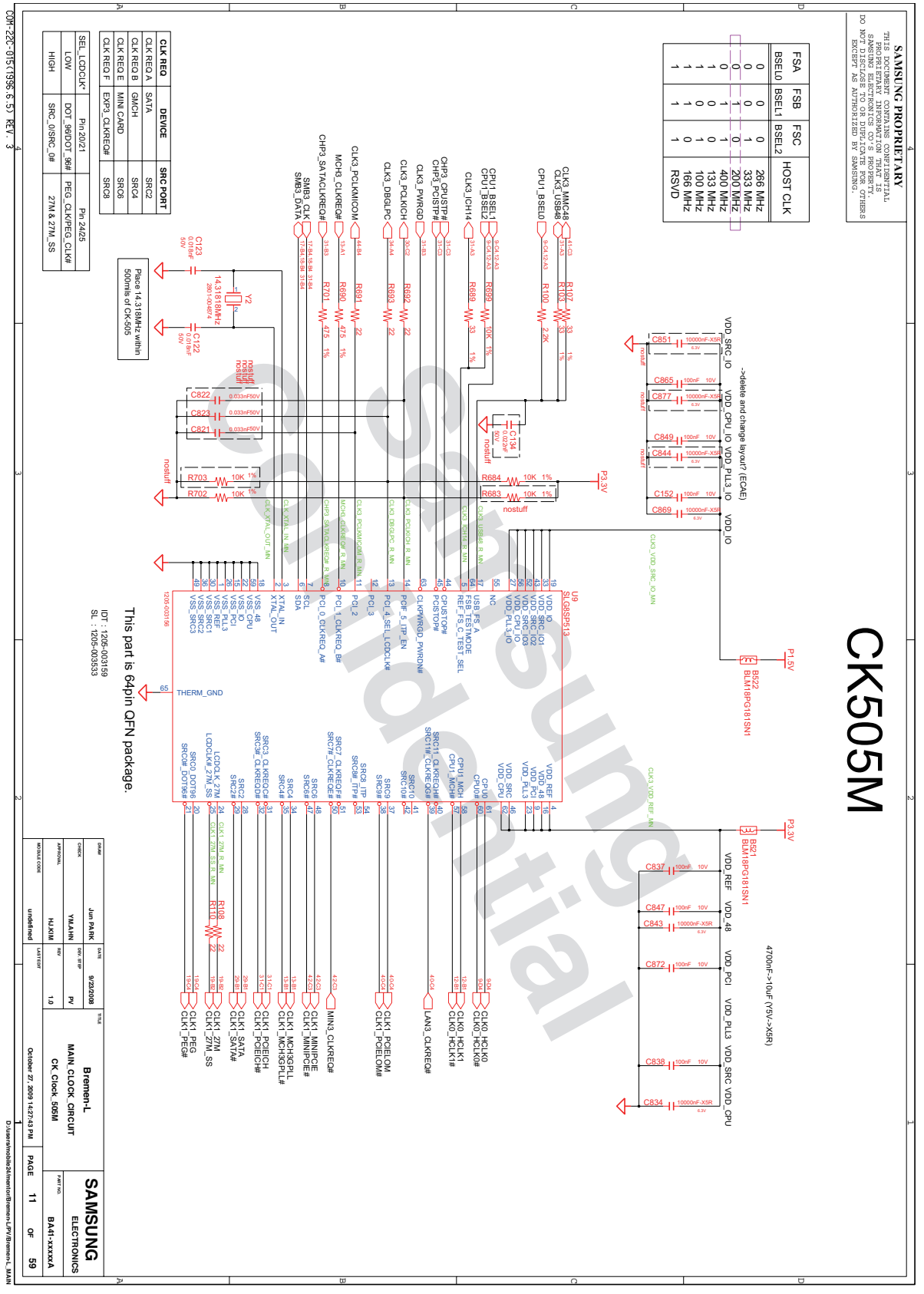

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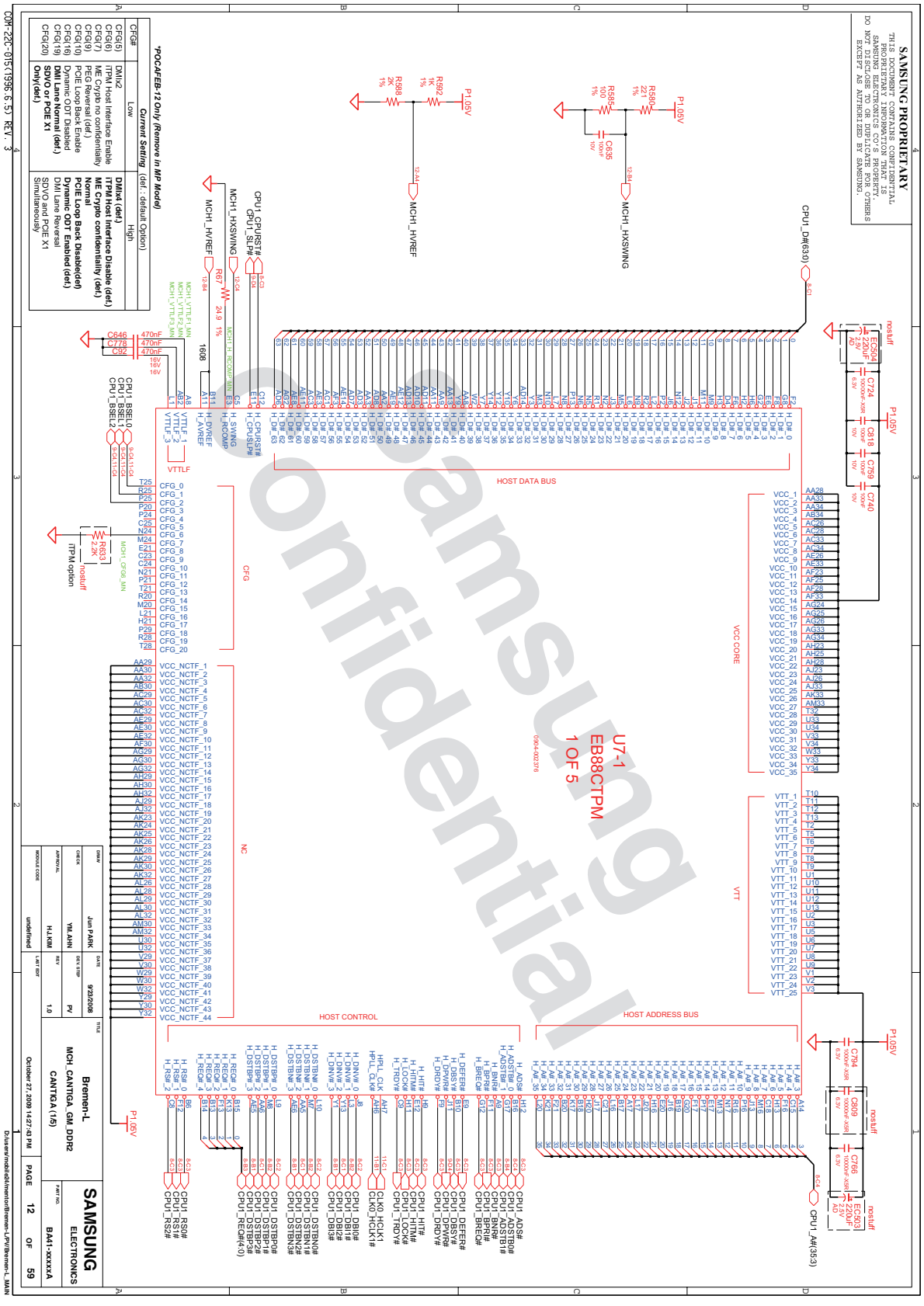

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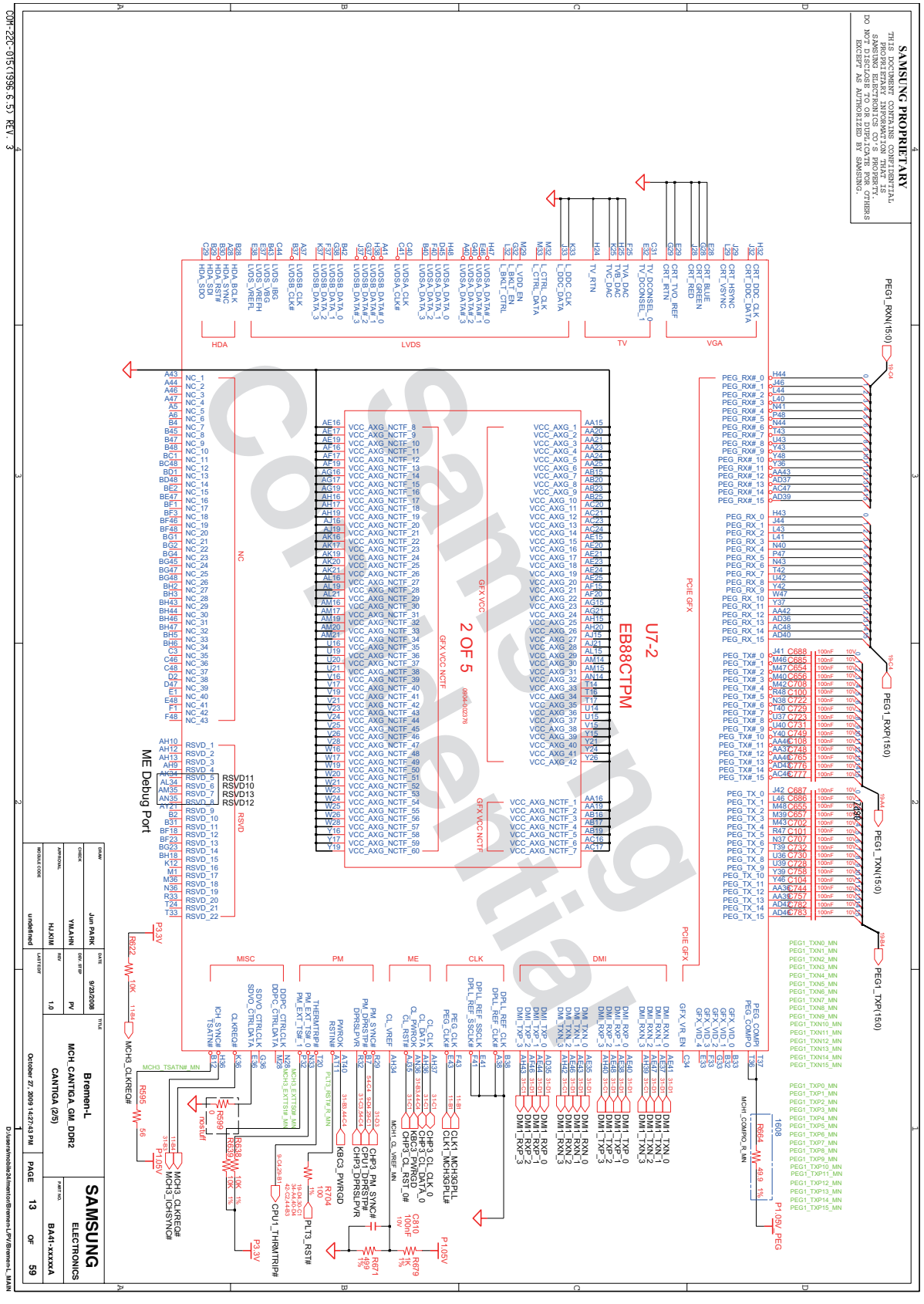

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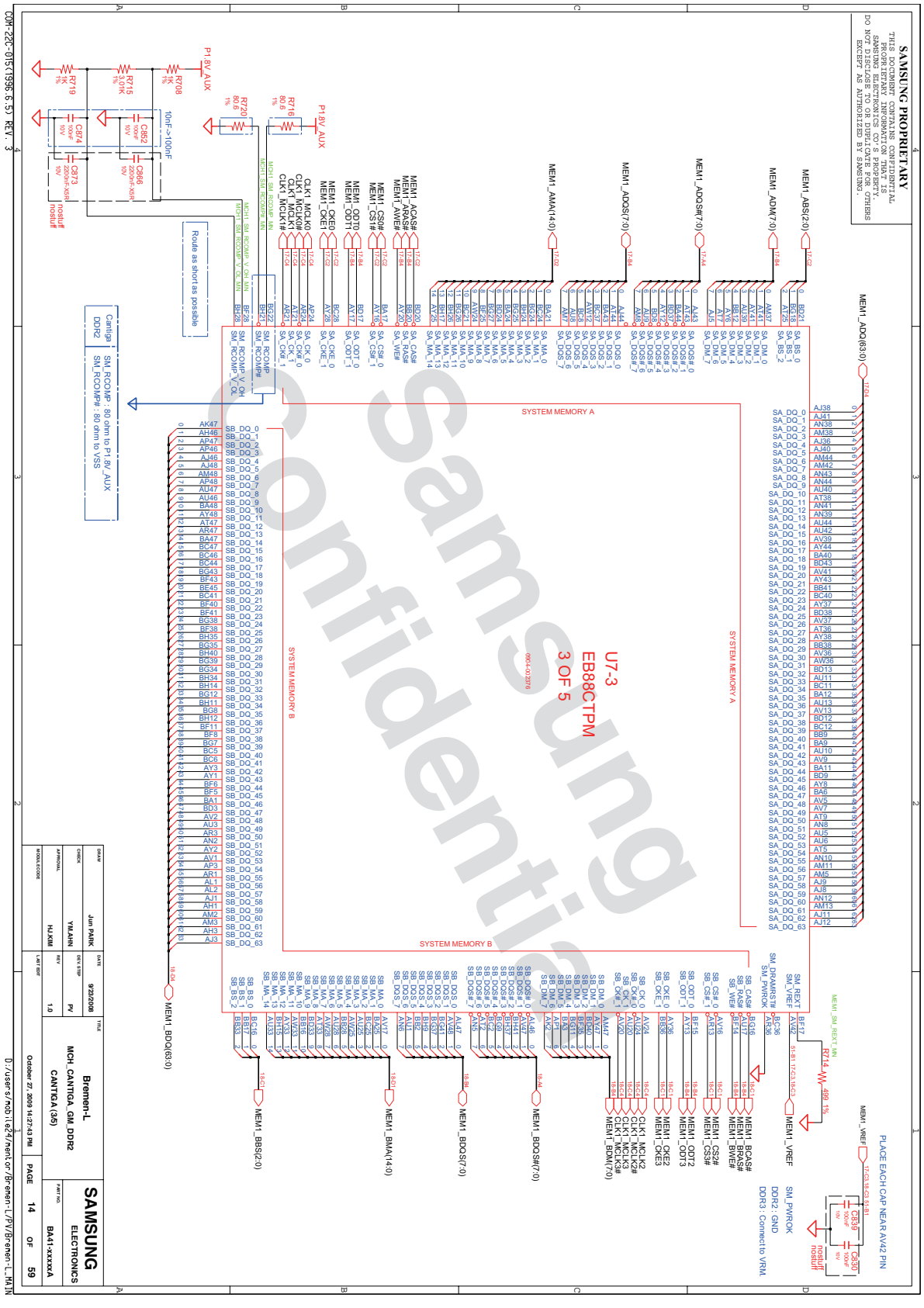

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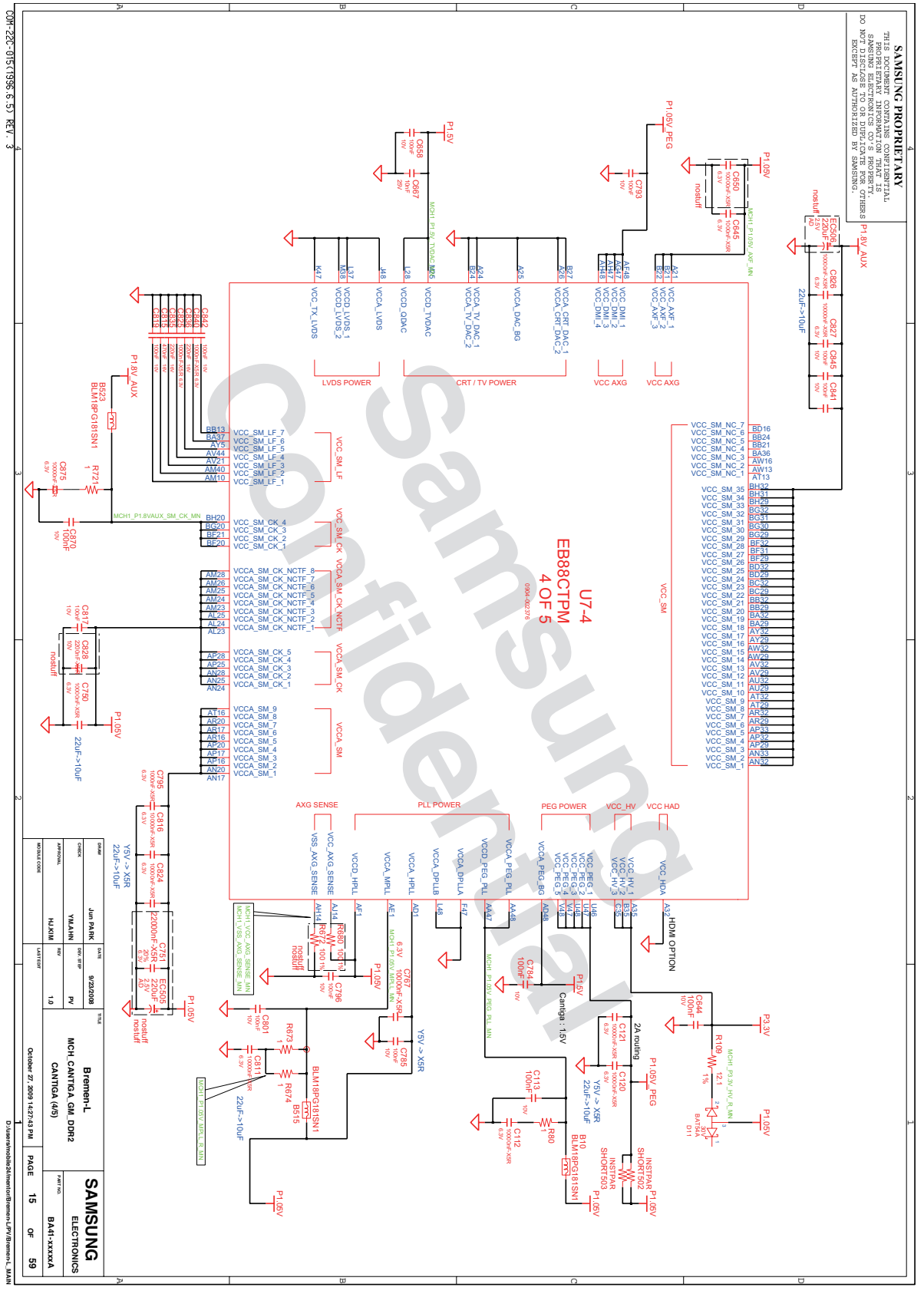

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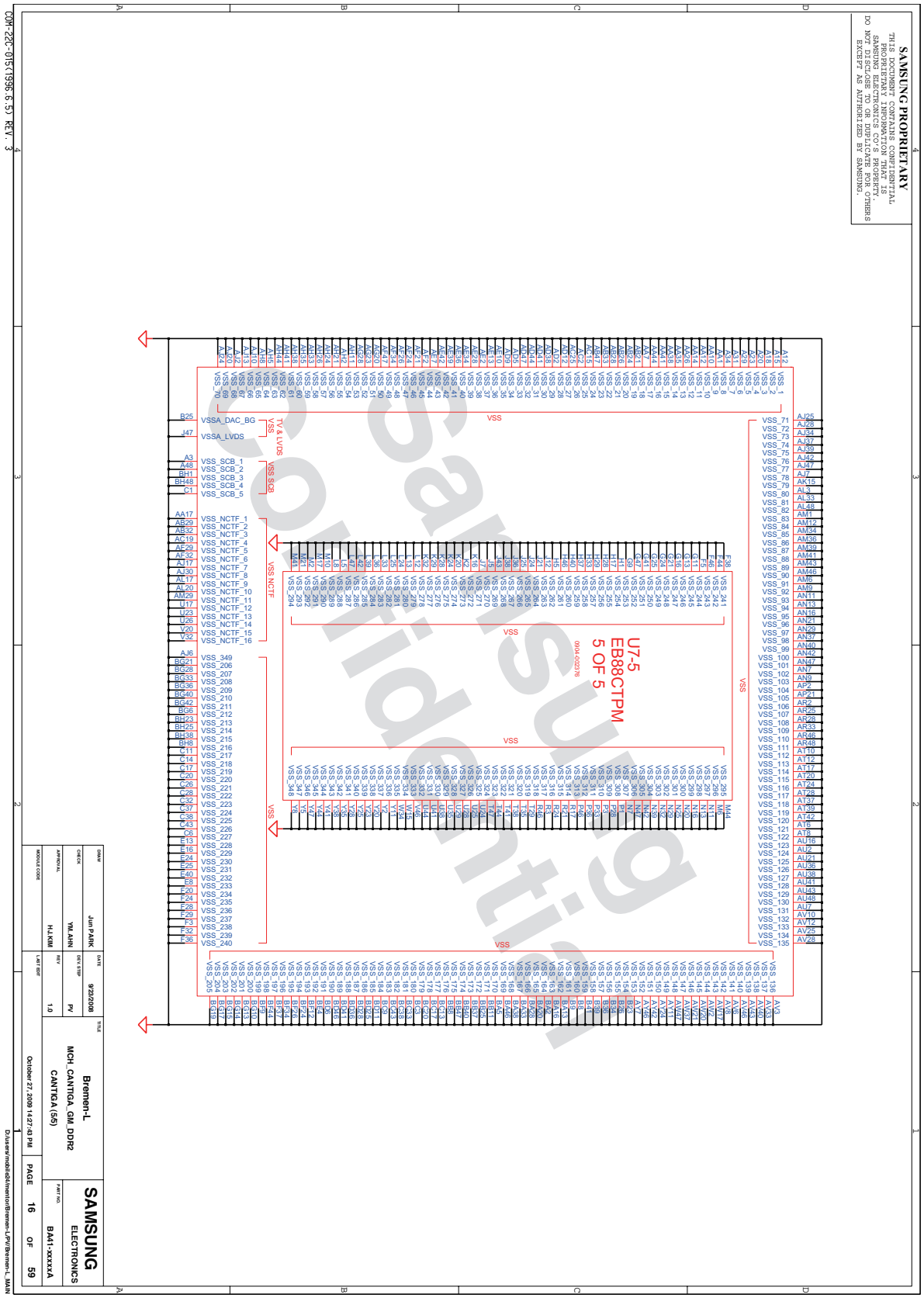

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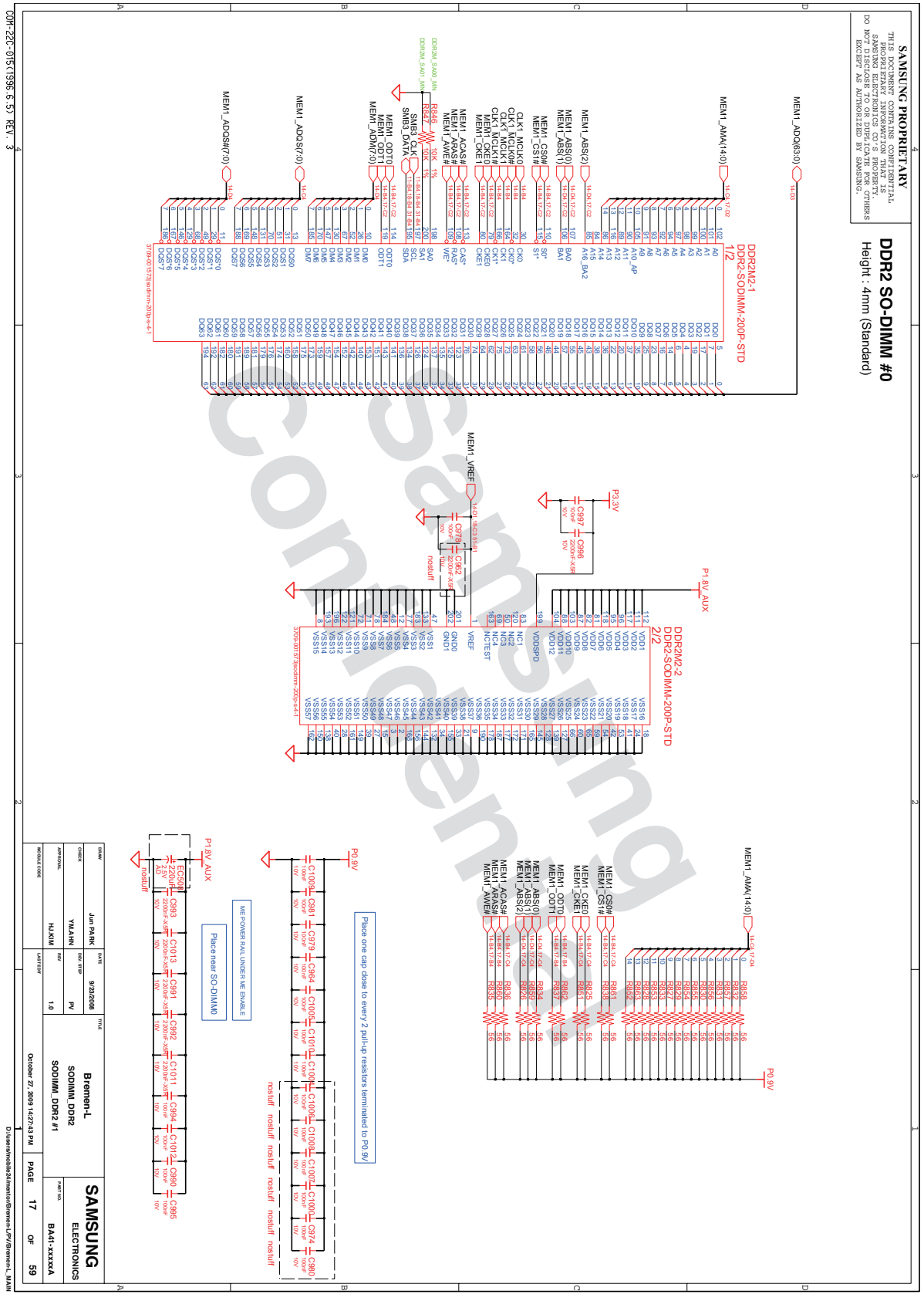

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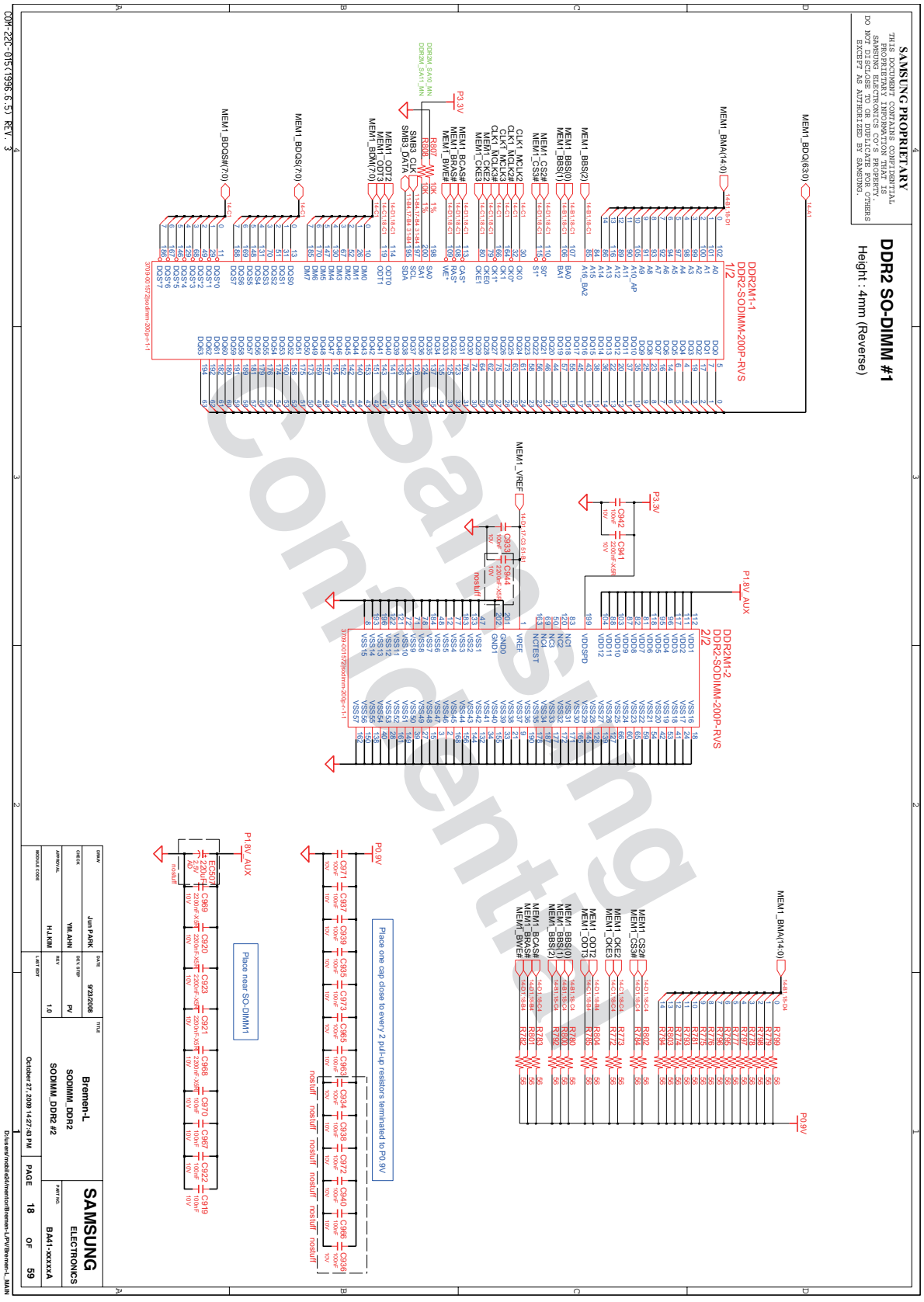

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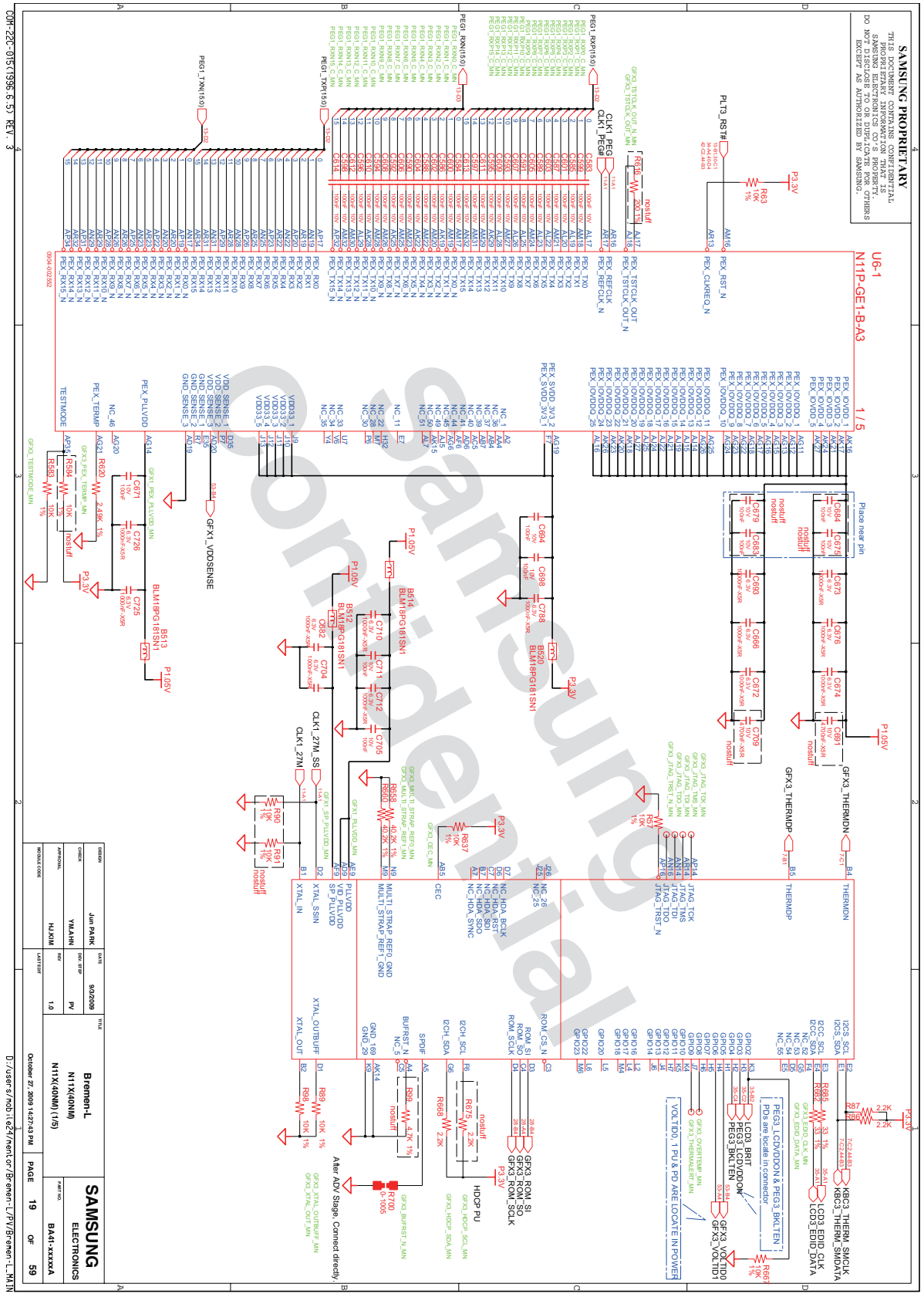

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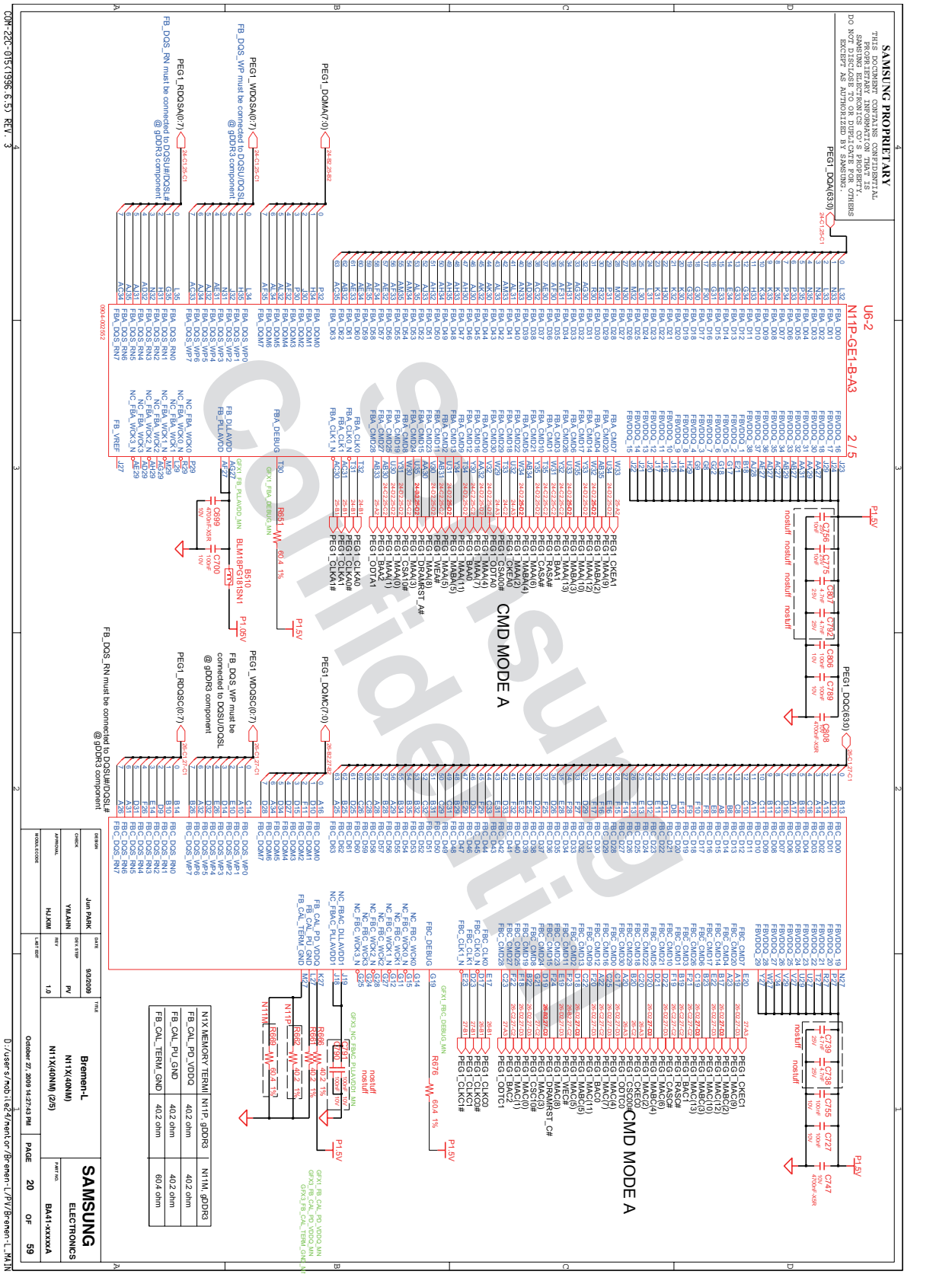

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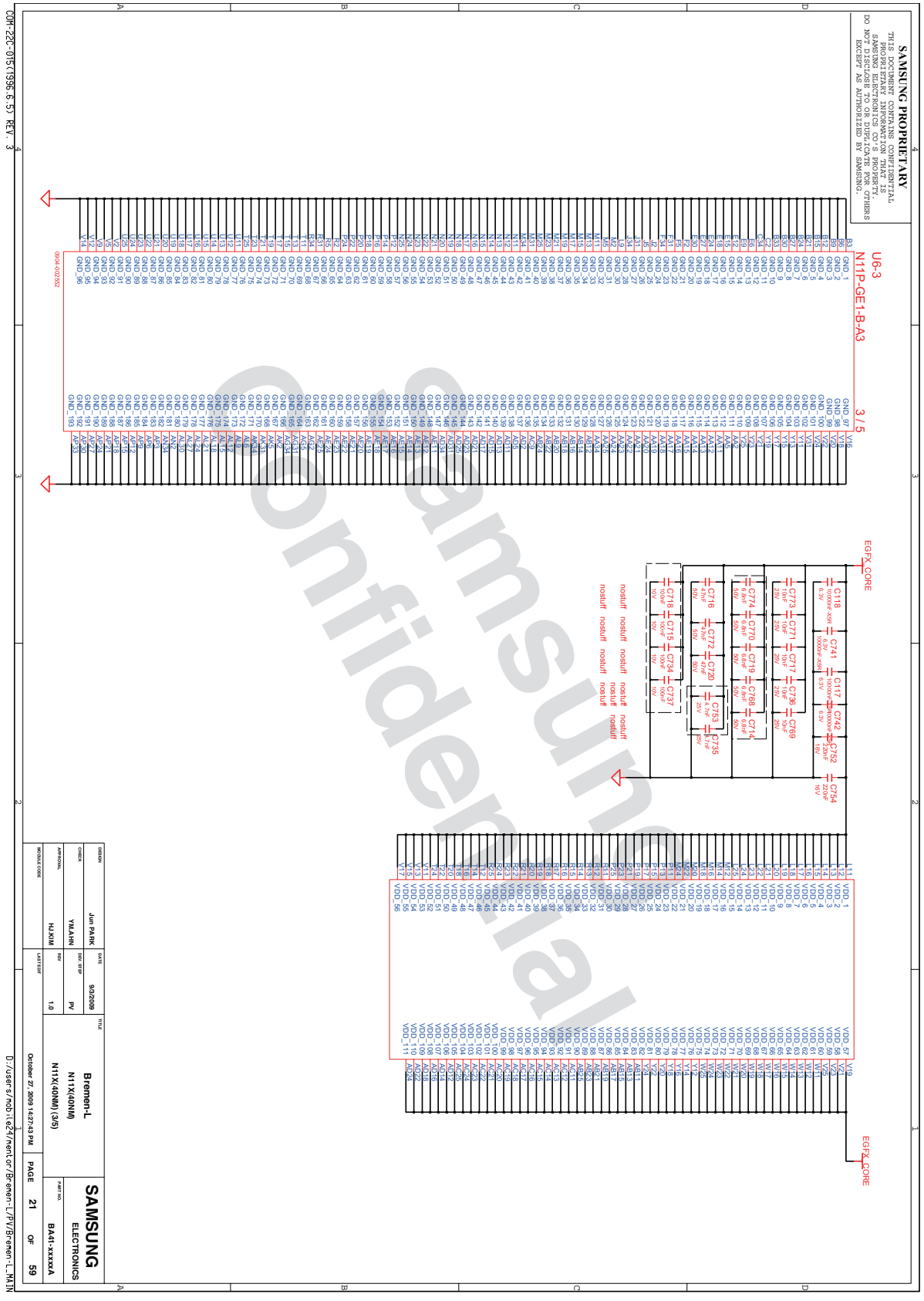

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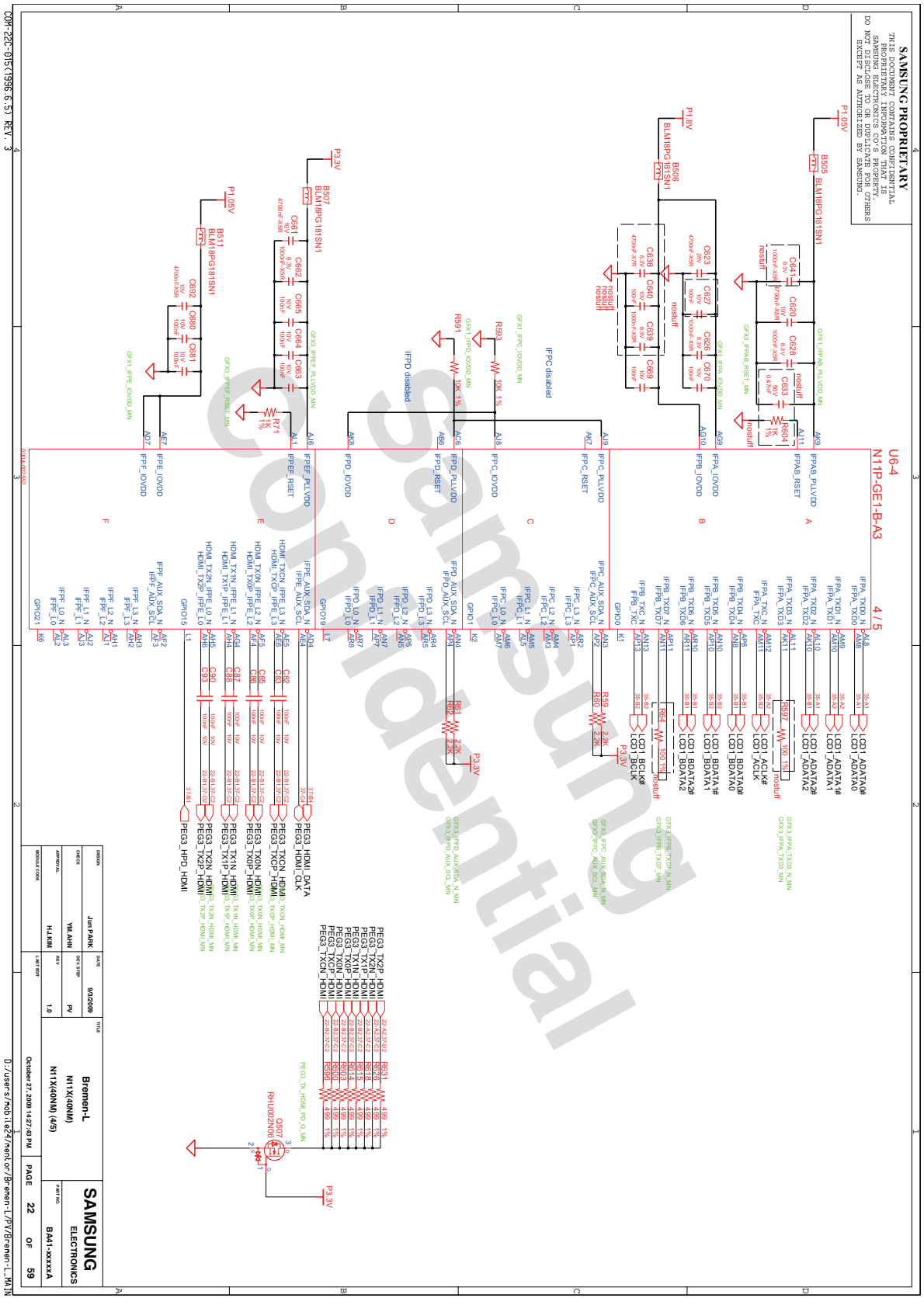

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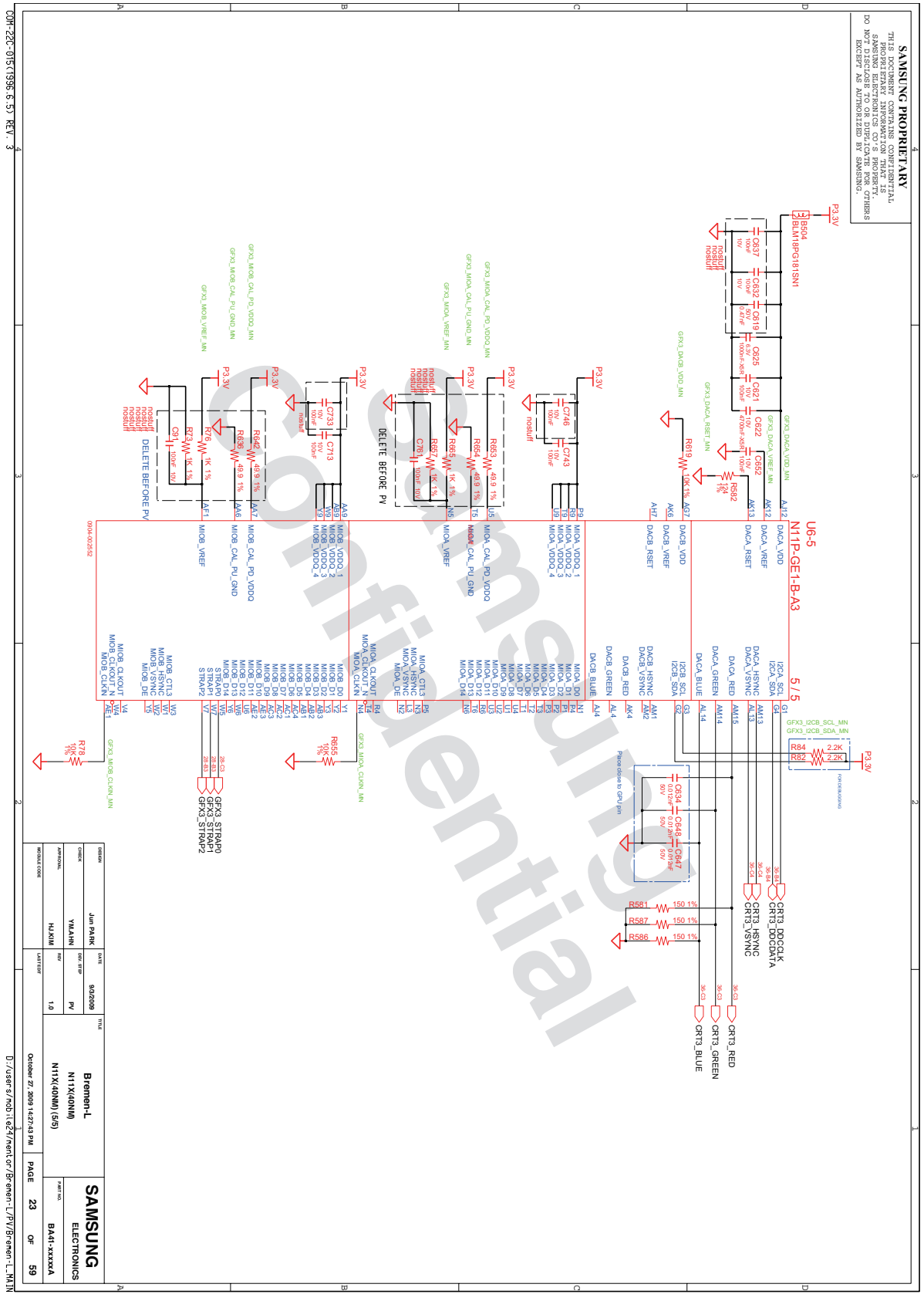

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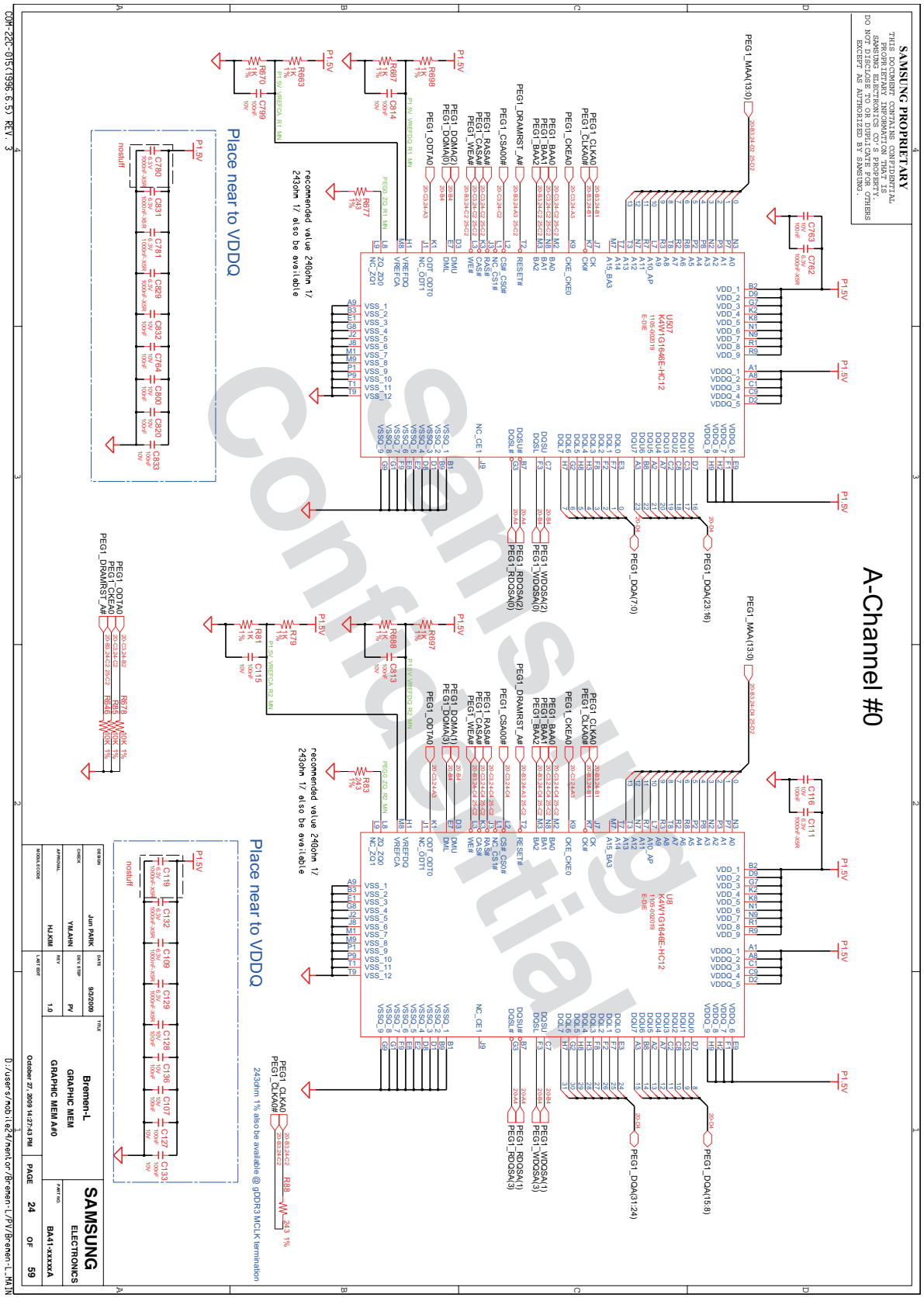

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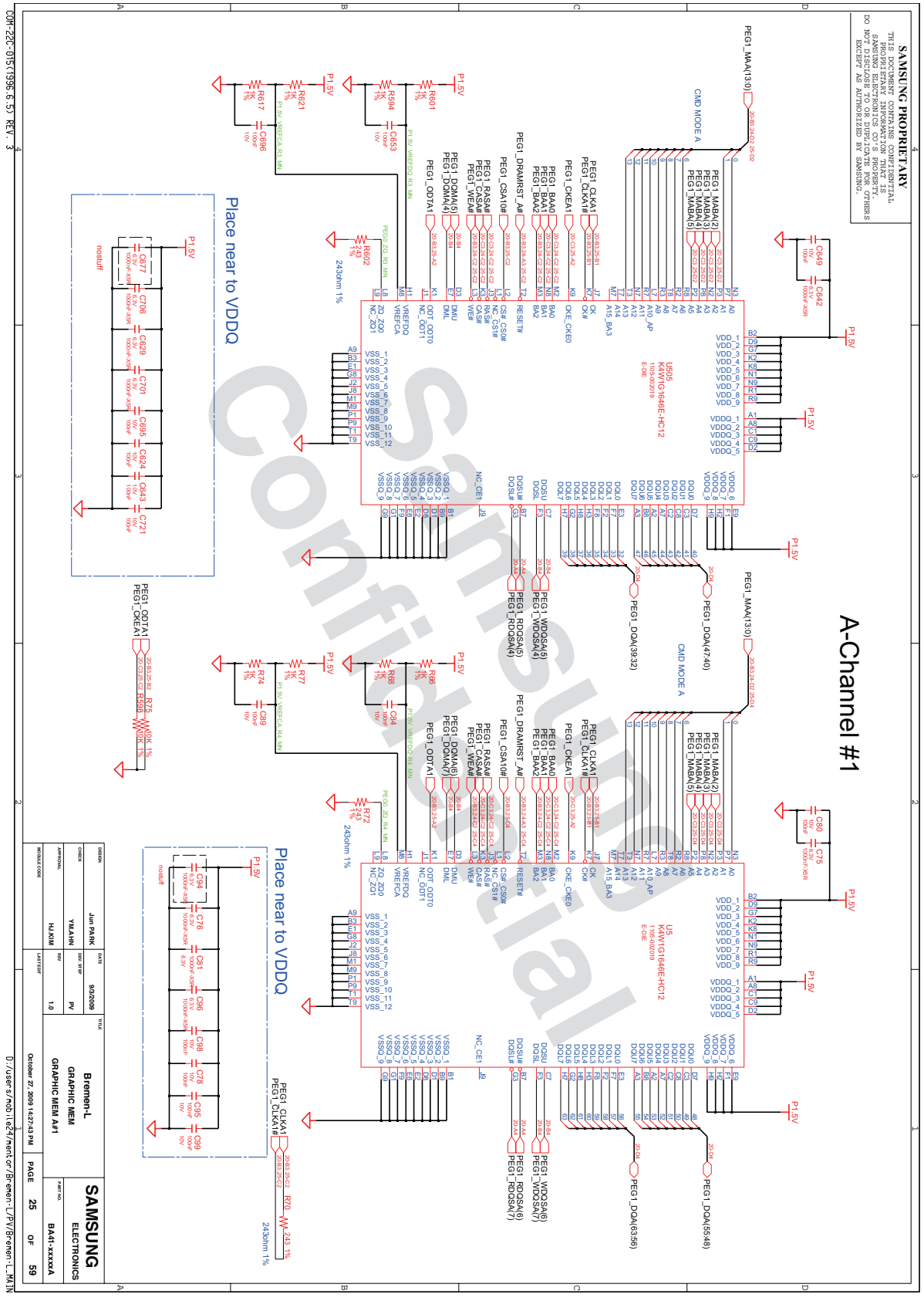

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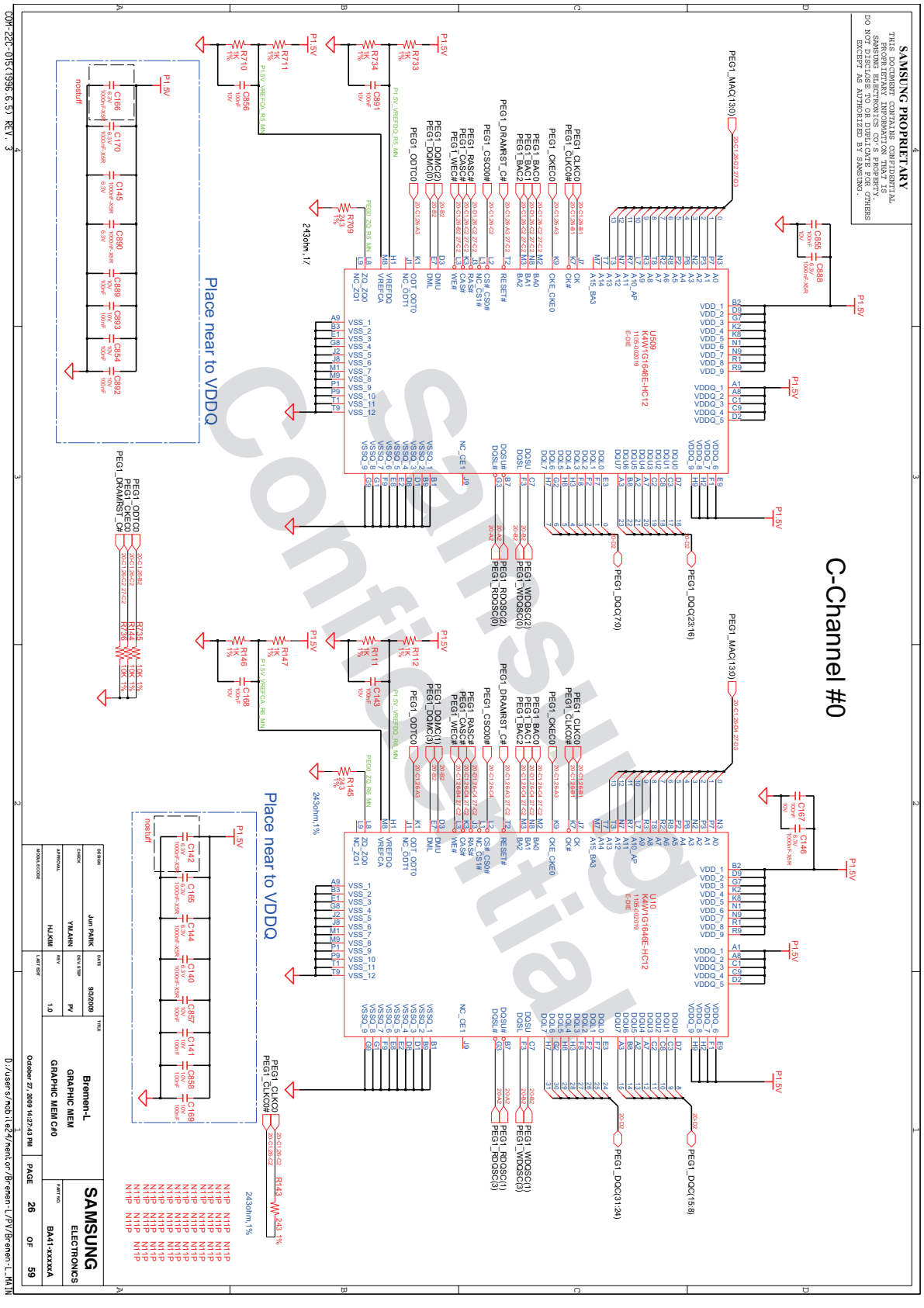

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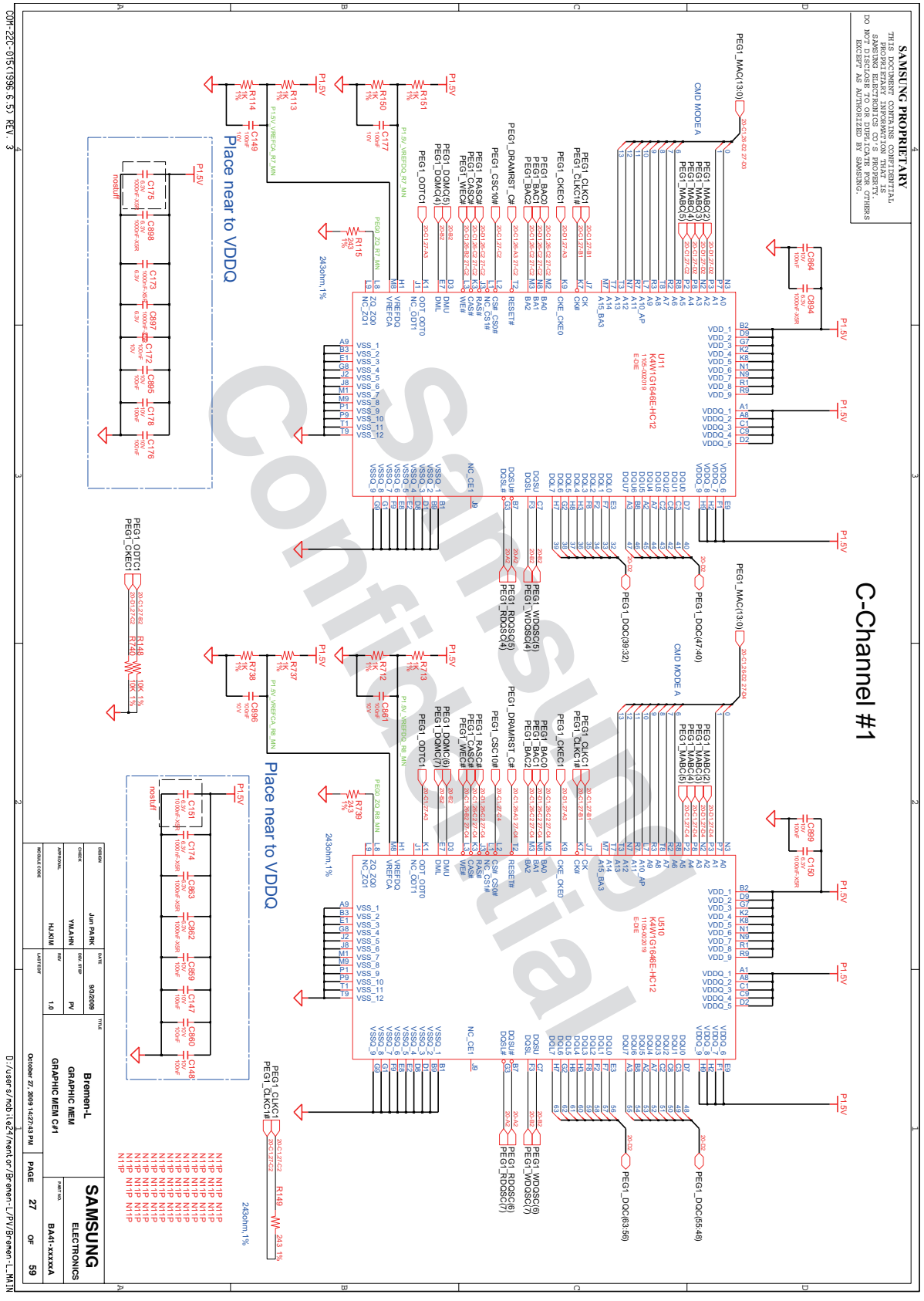

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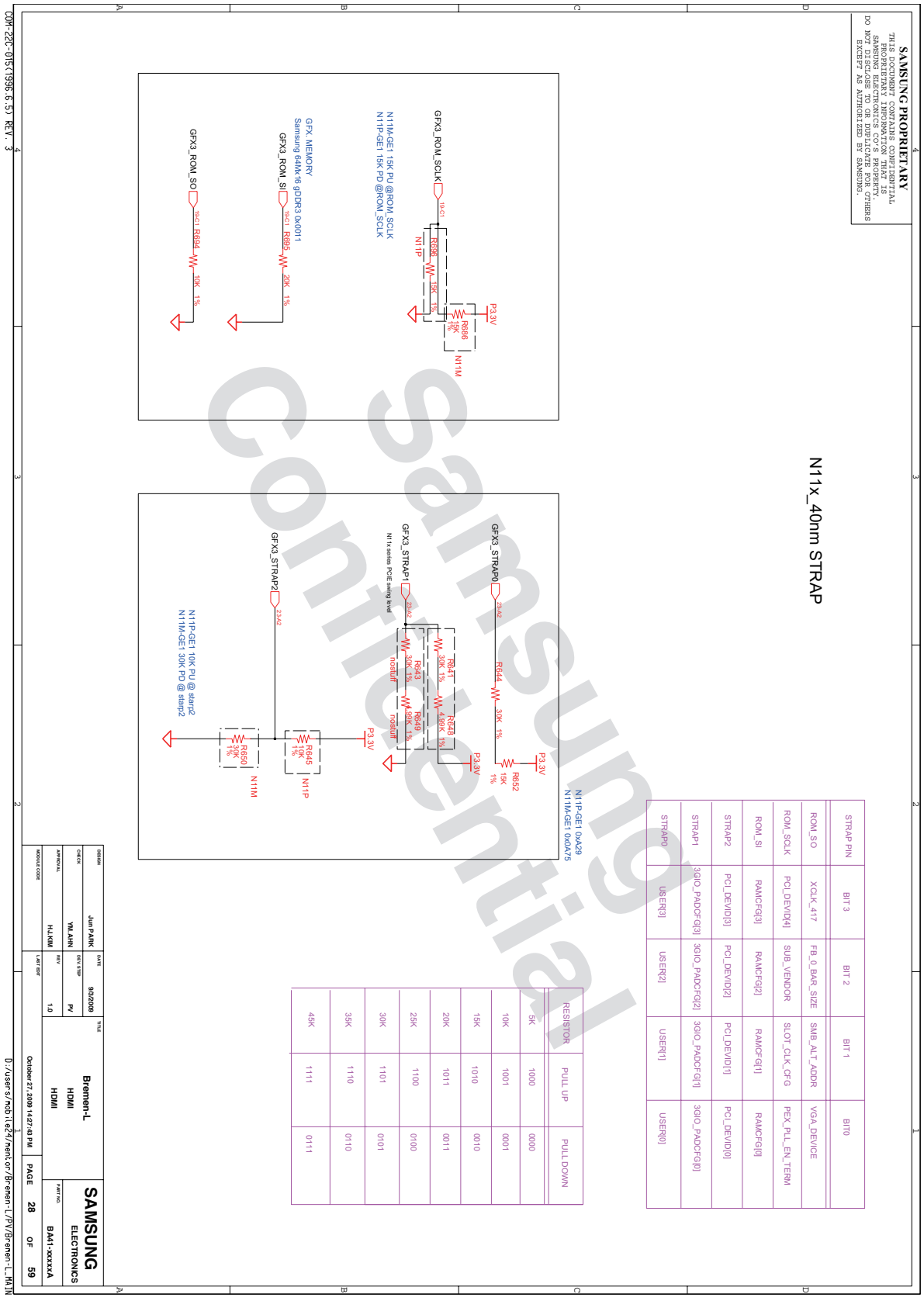

STRAP PIN	BIT 3	BIT 2	BIT 1	BIT0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

RESISTOR	PULL UP	PULLDOWN
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

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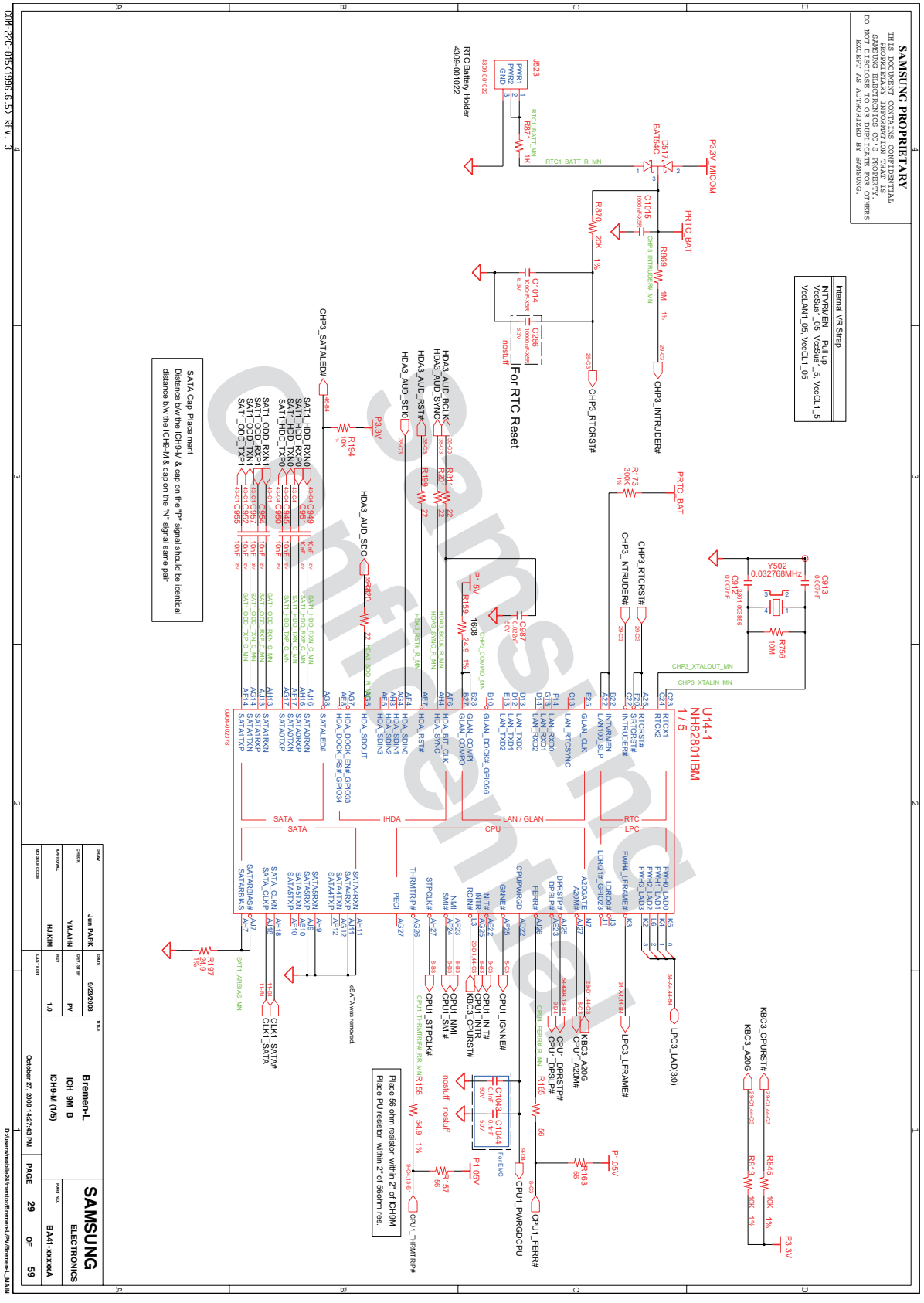

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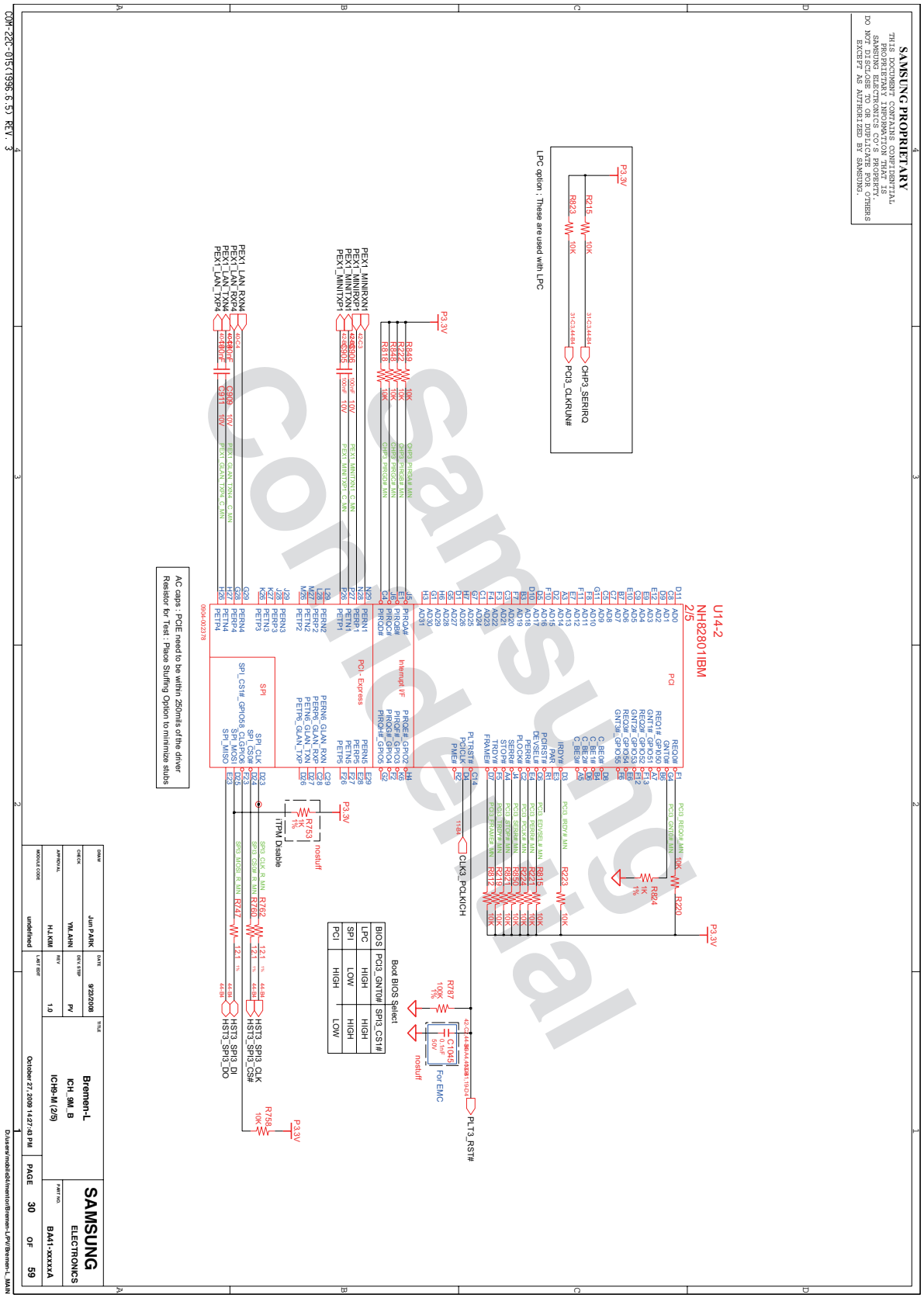

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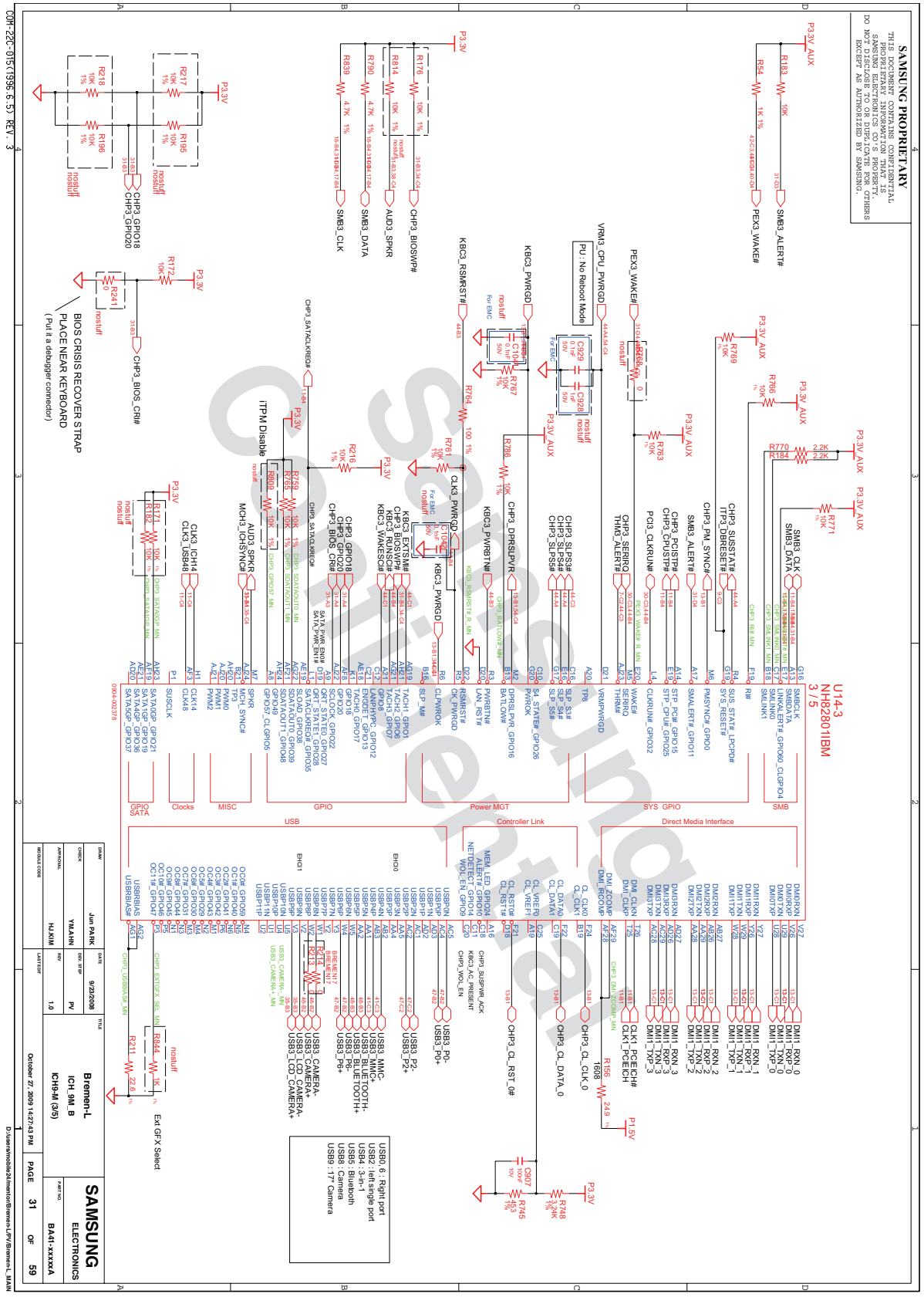

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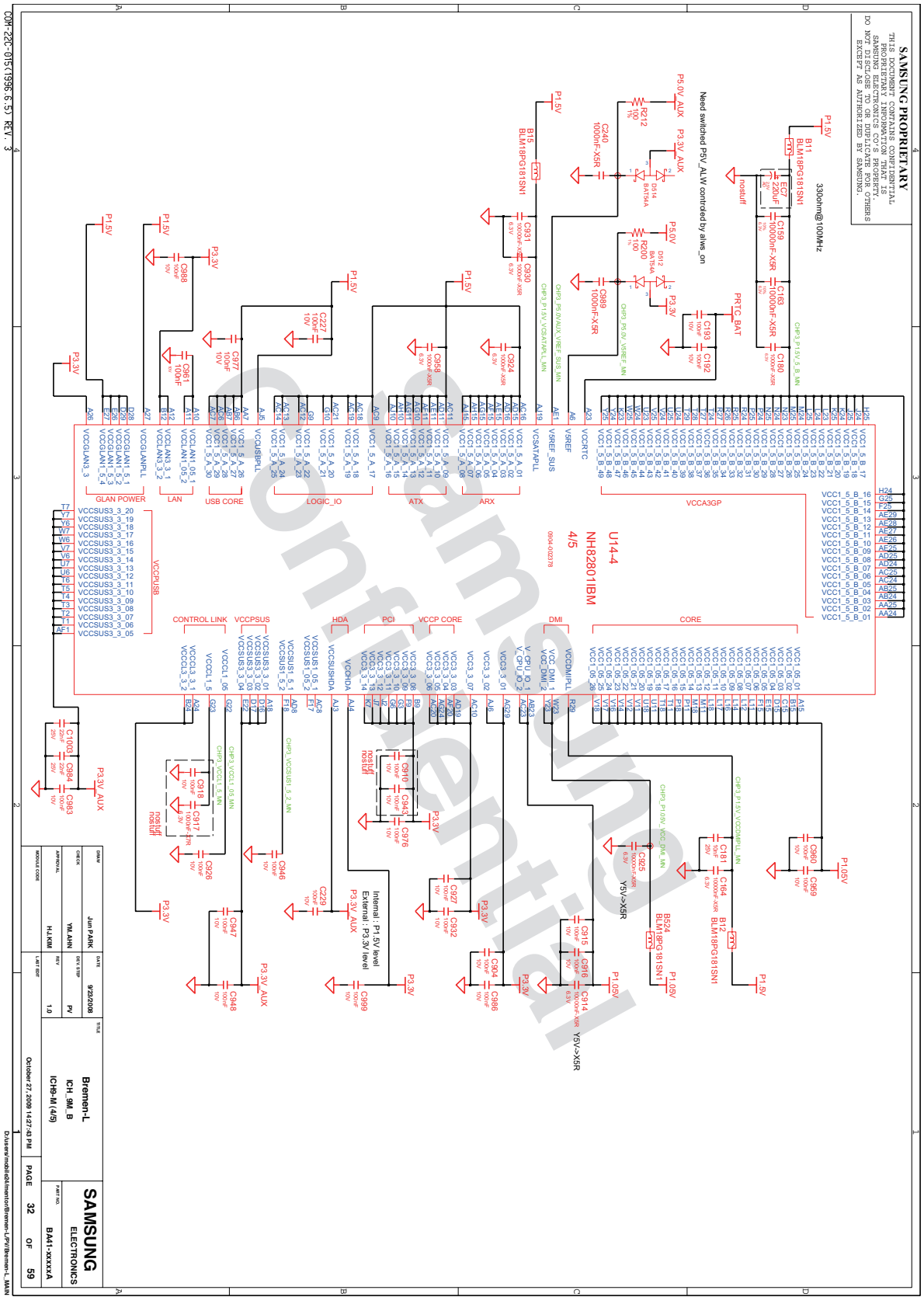

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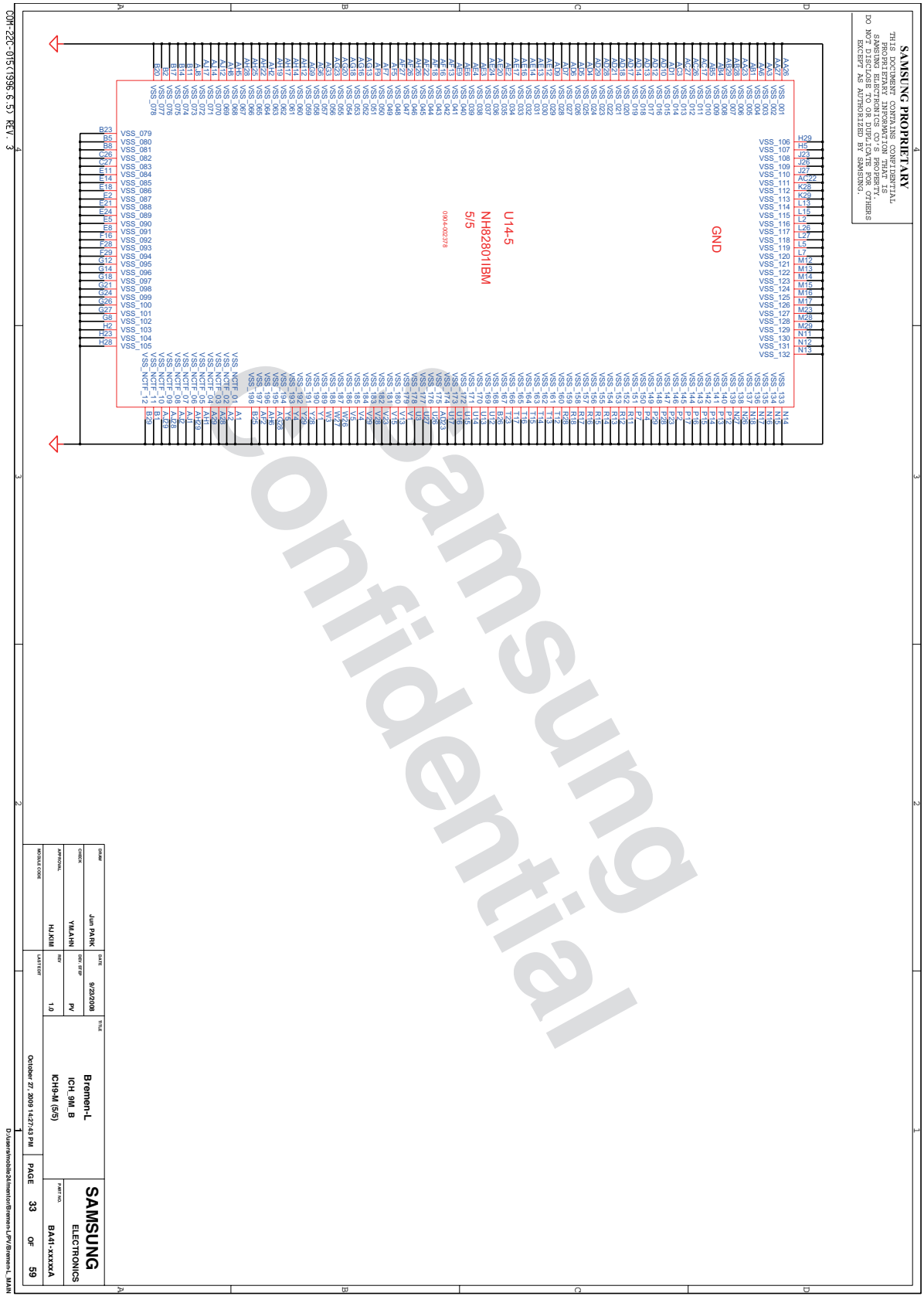

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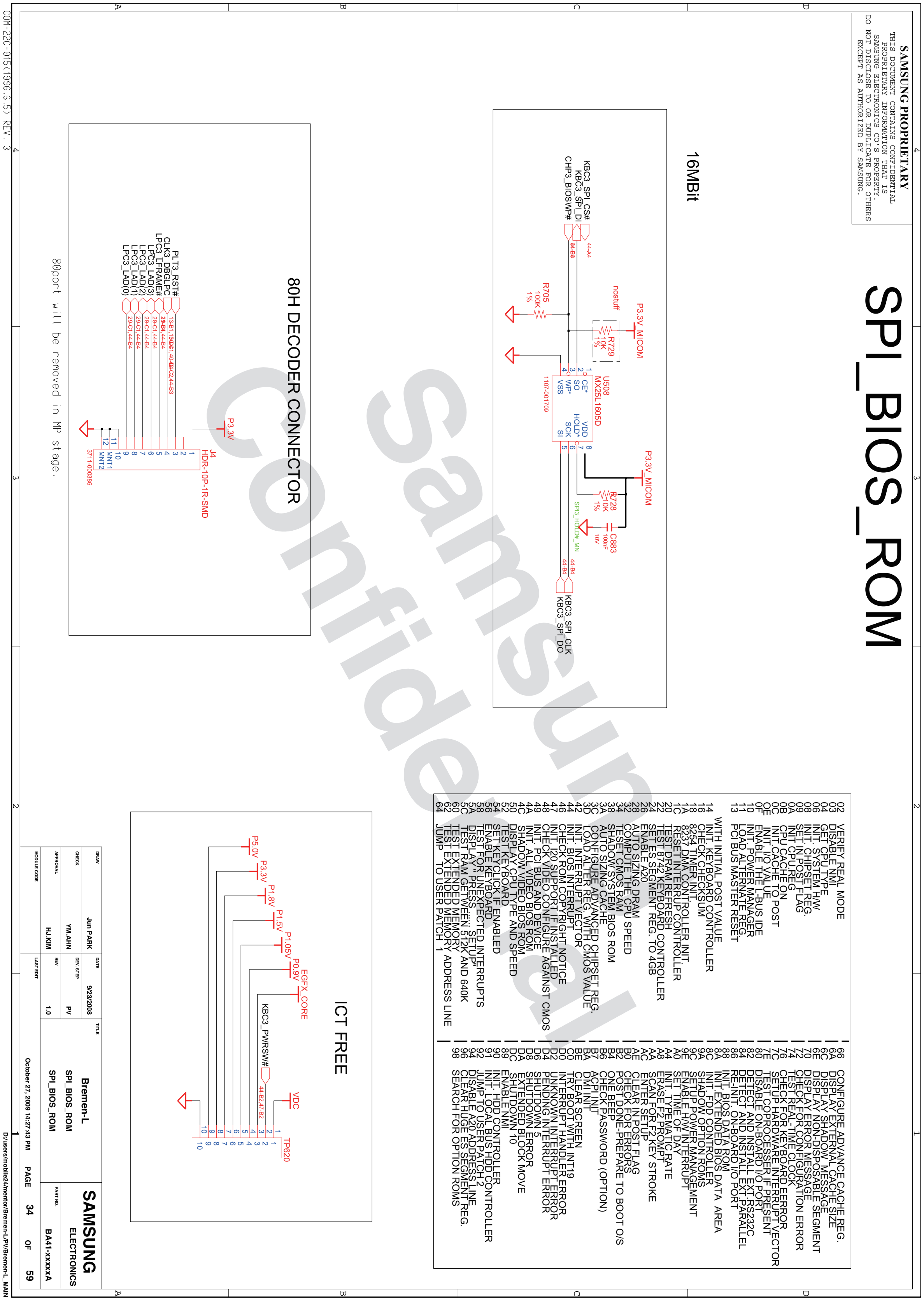

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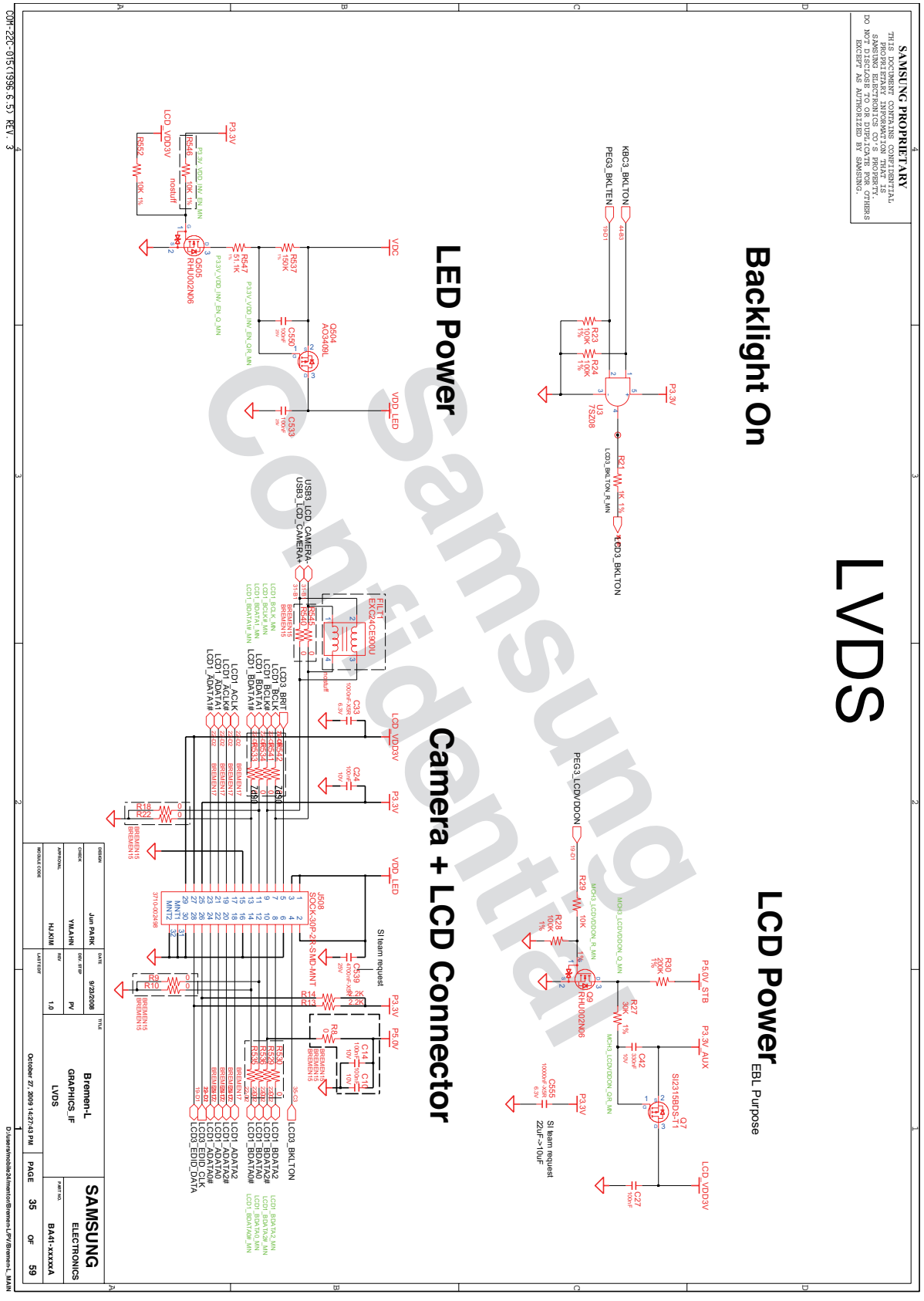

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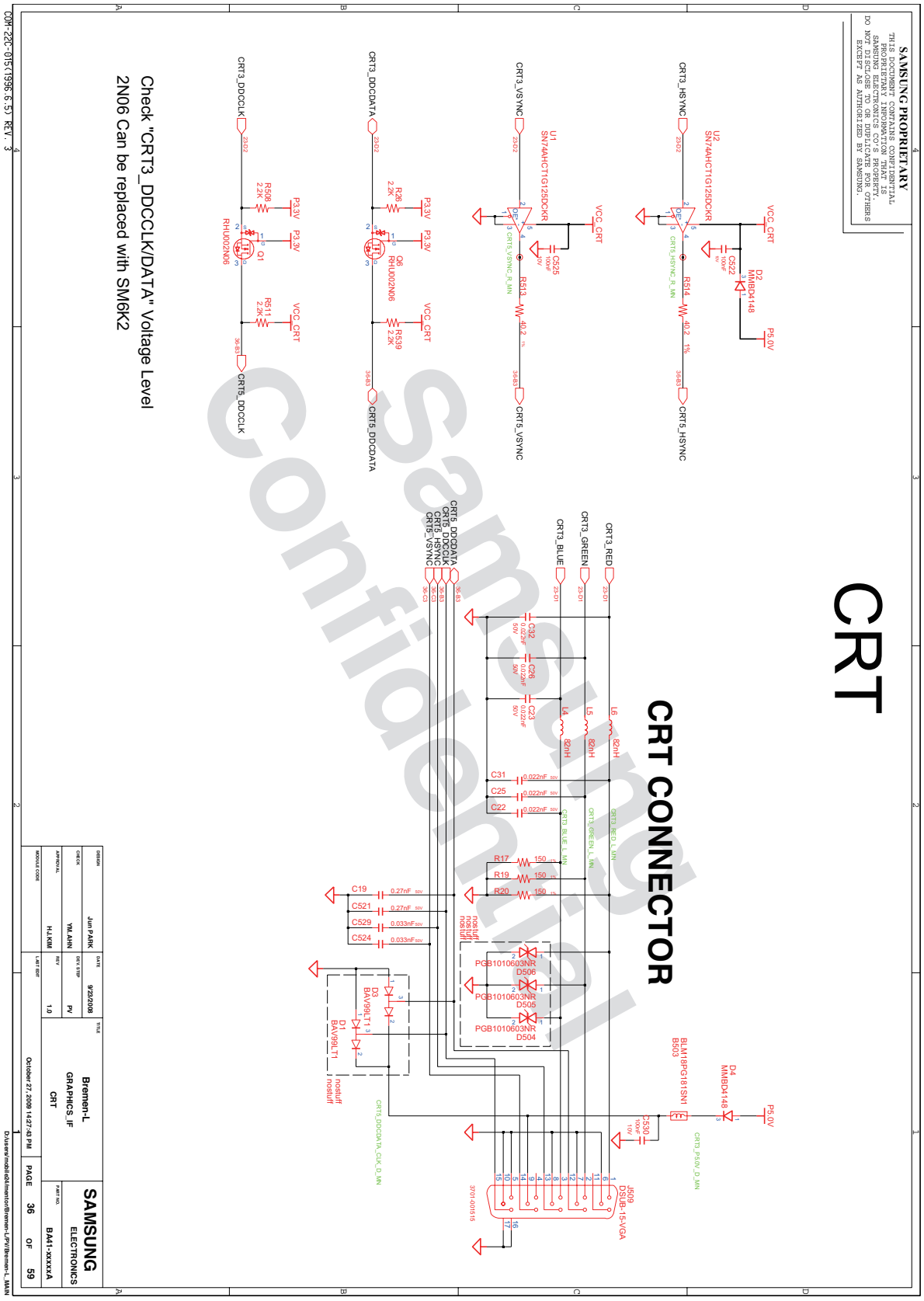

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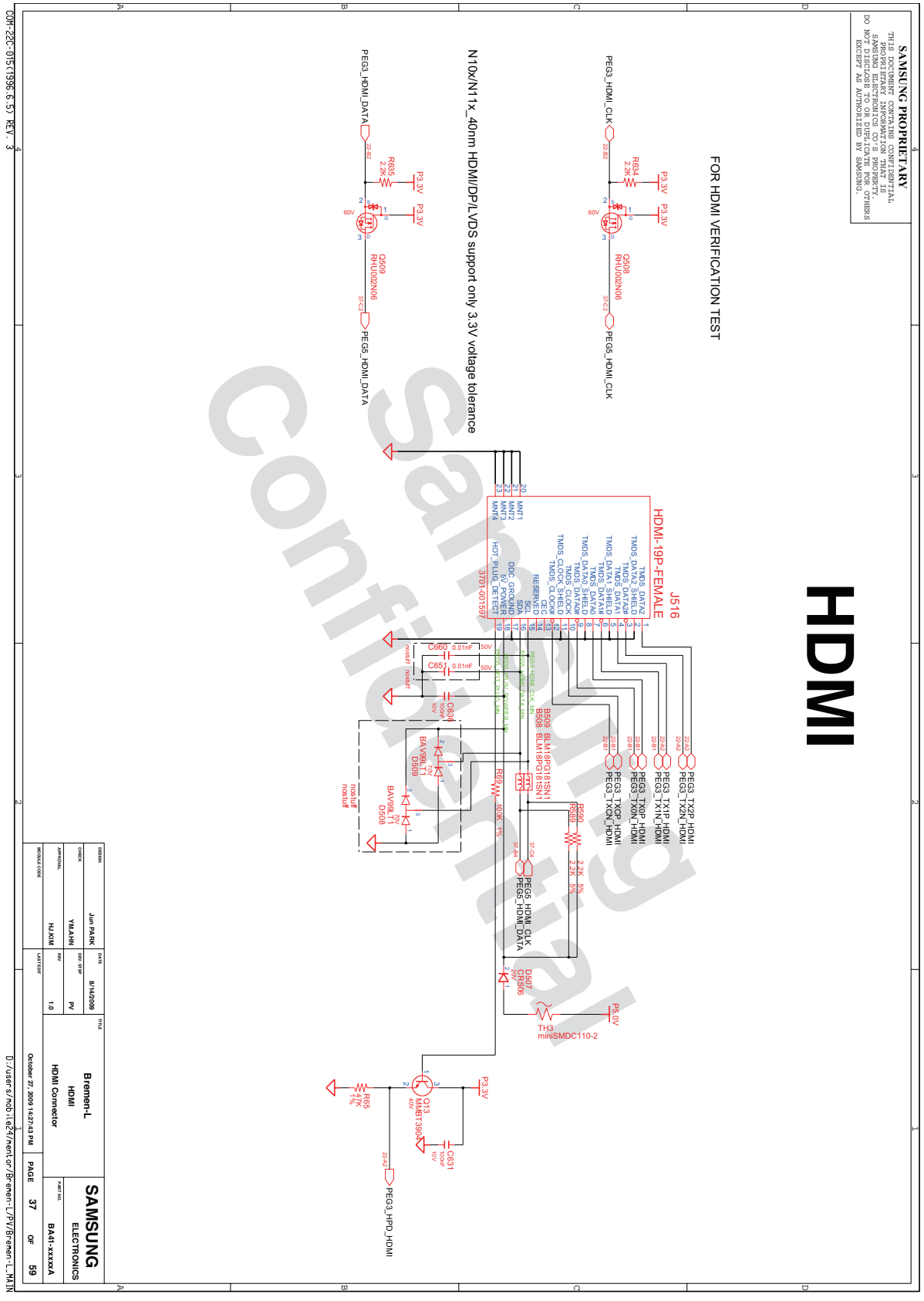

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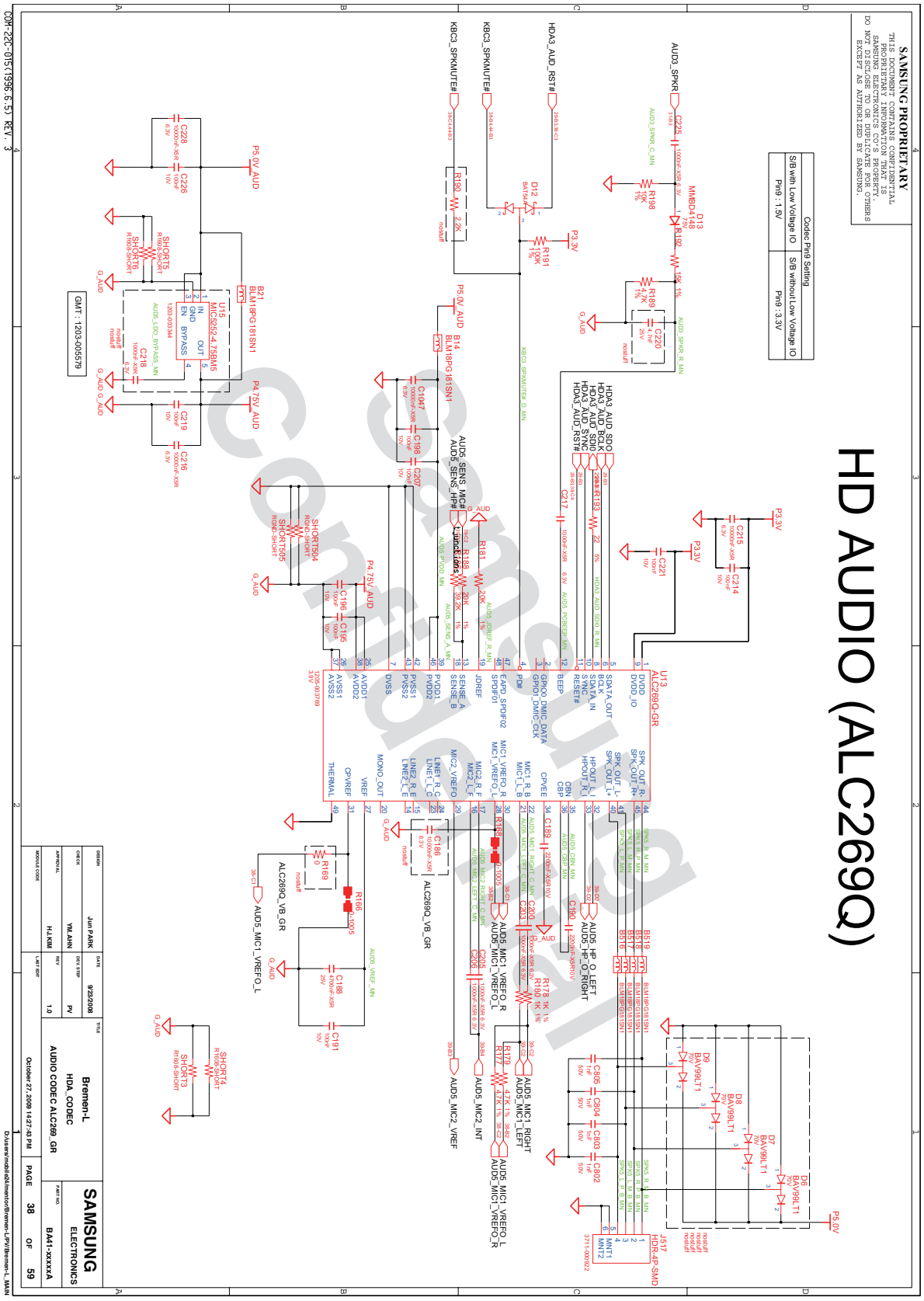

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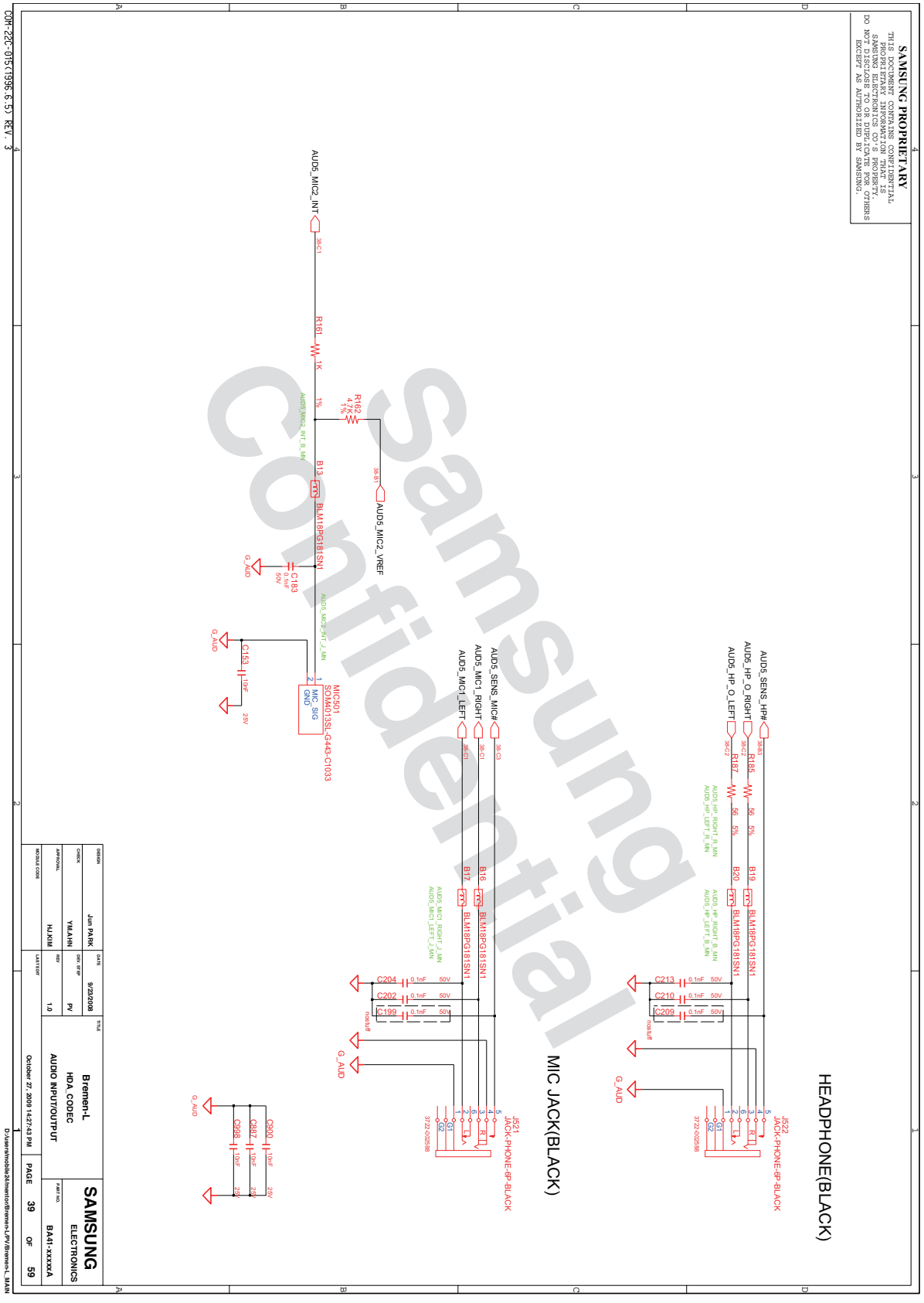

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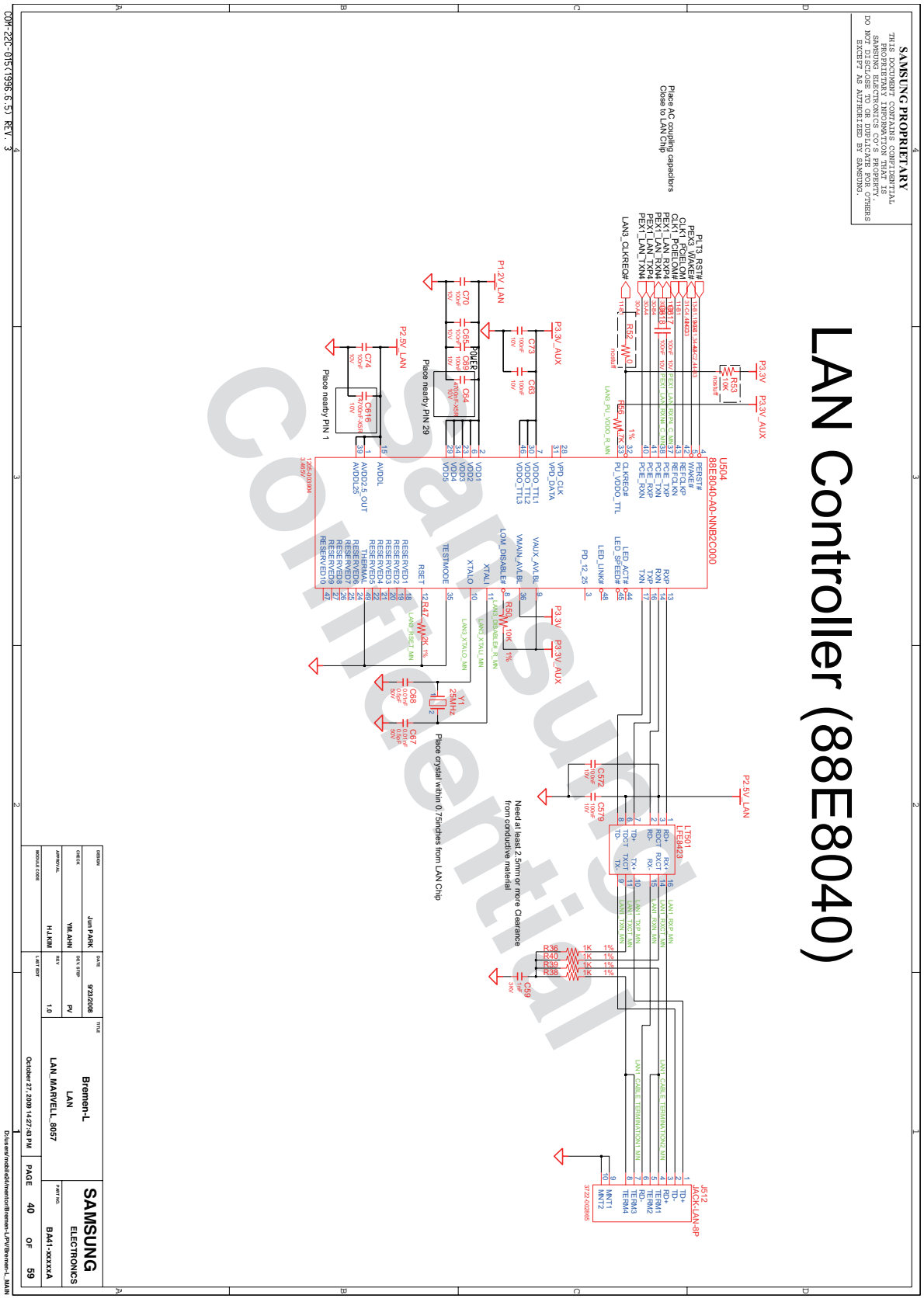

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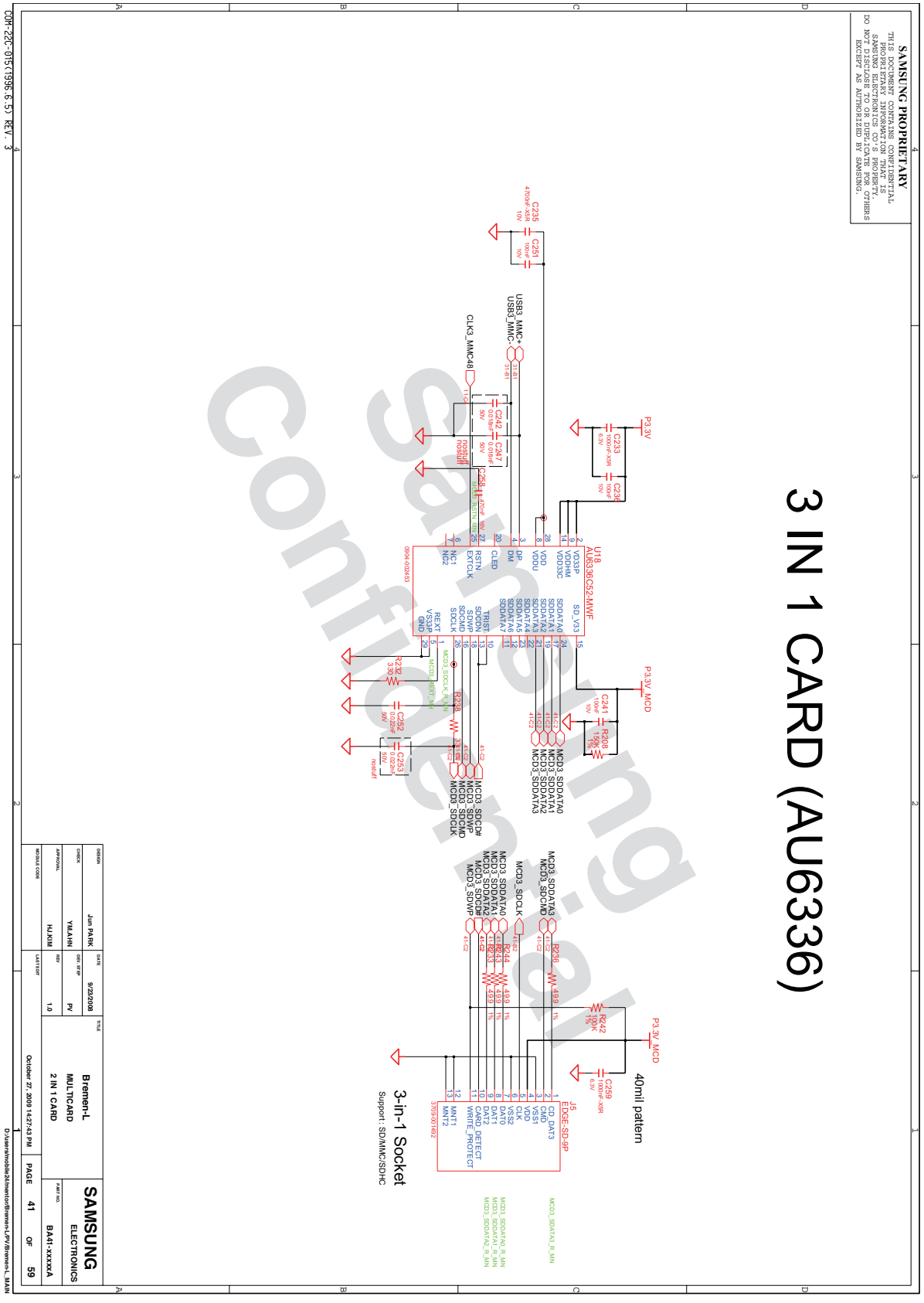

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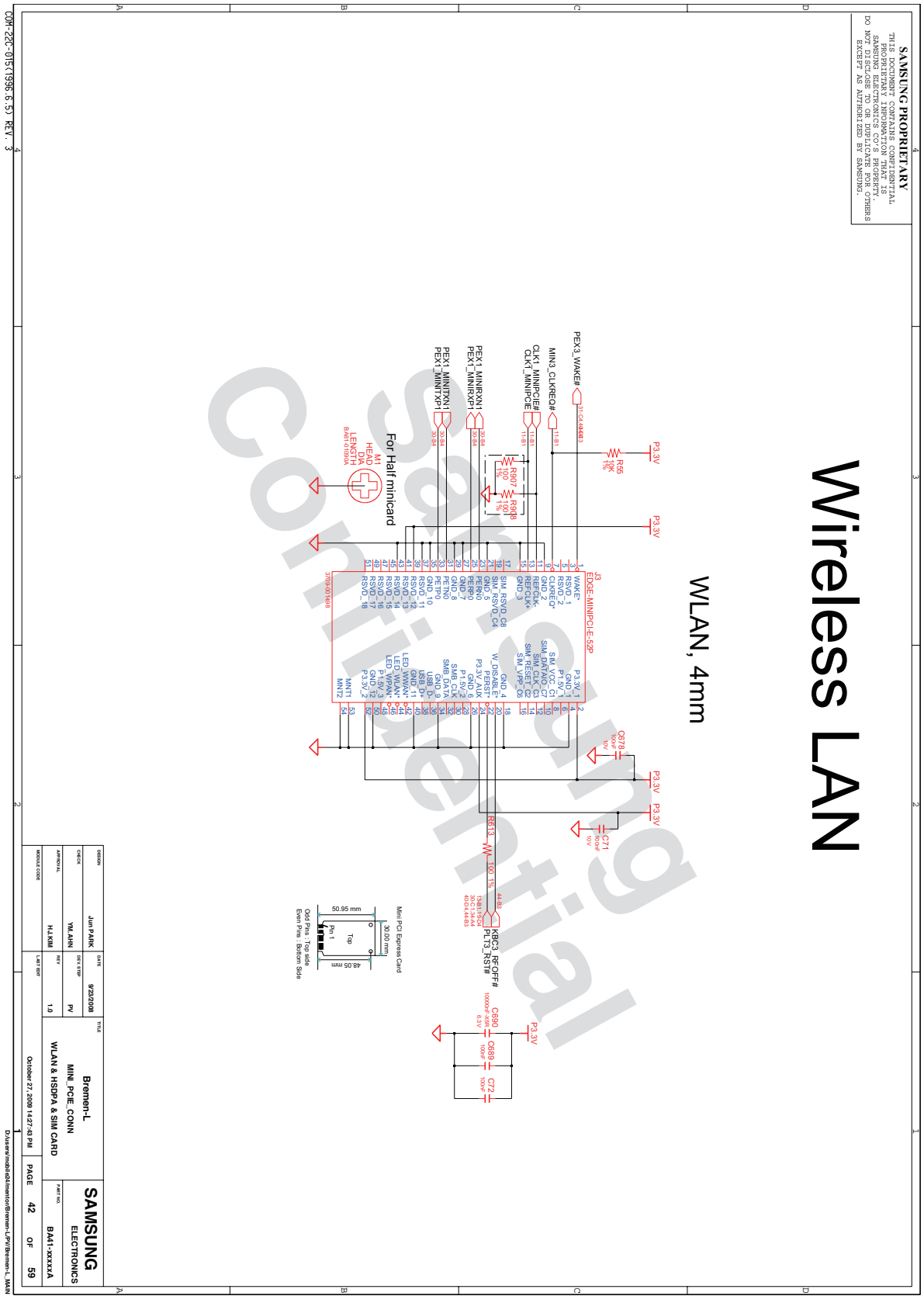

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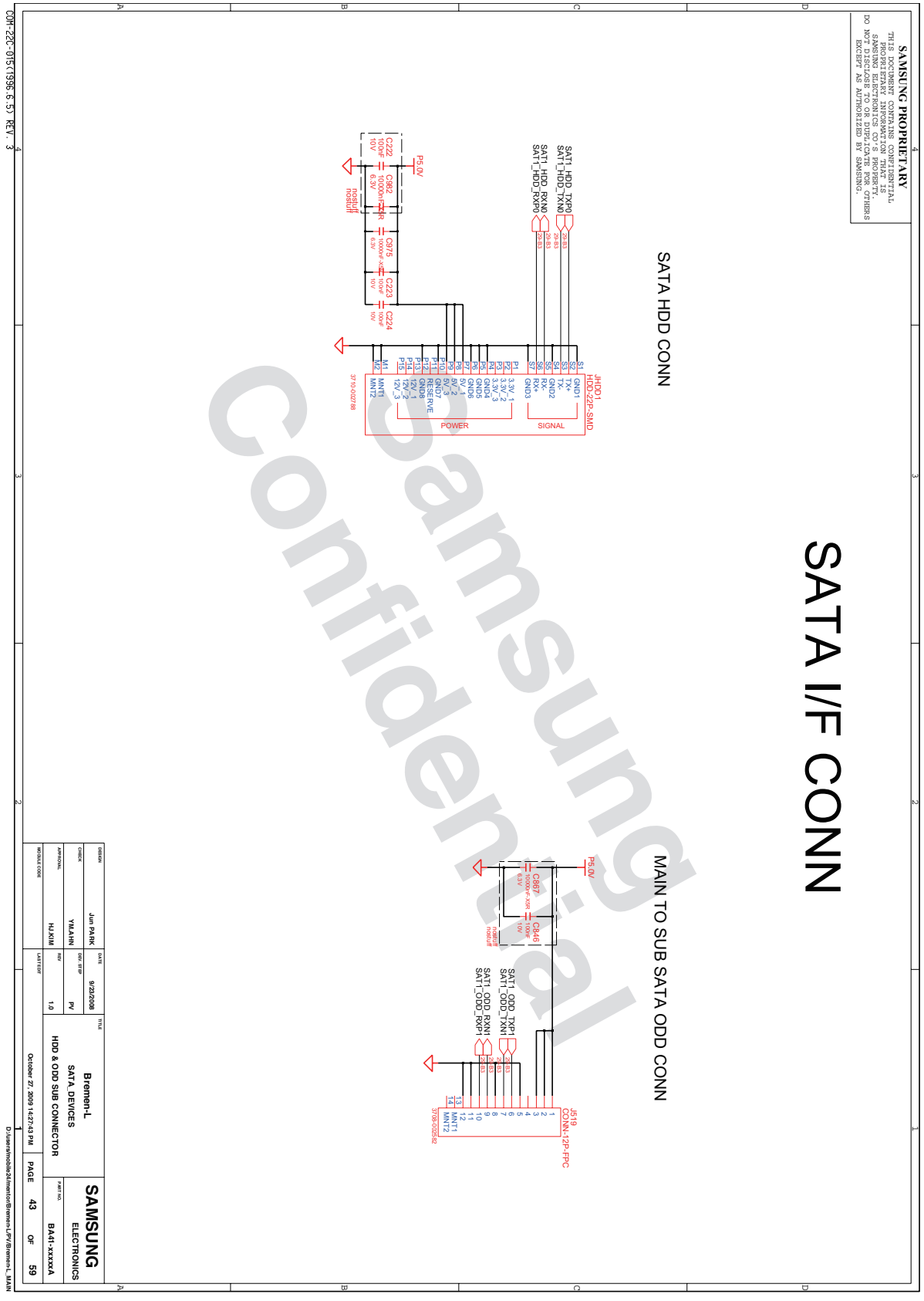

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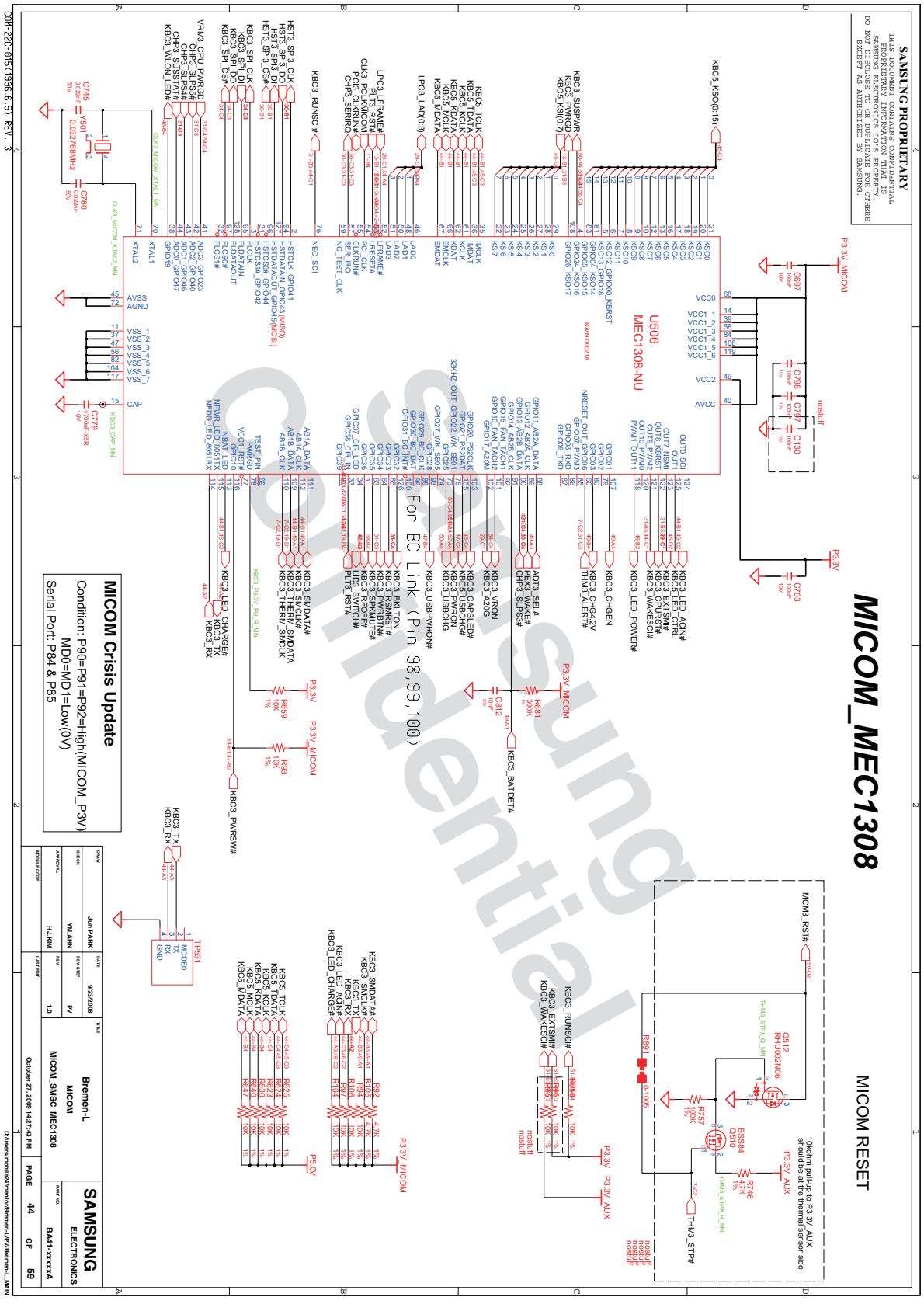

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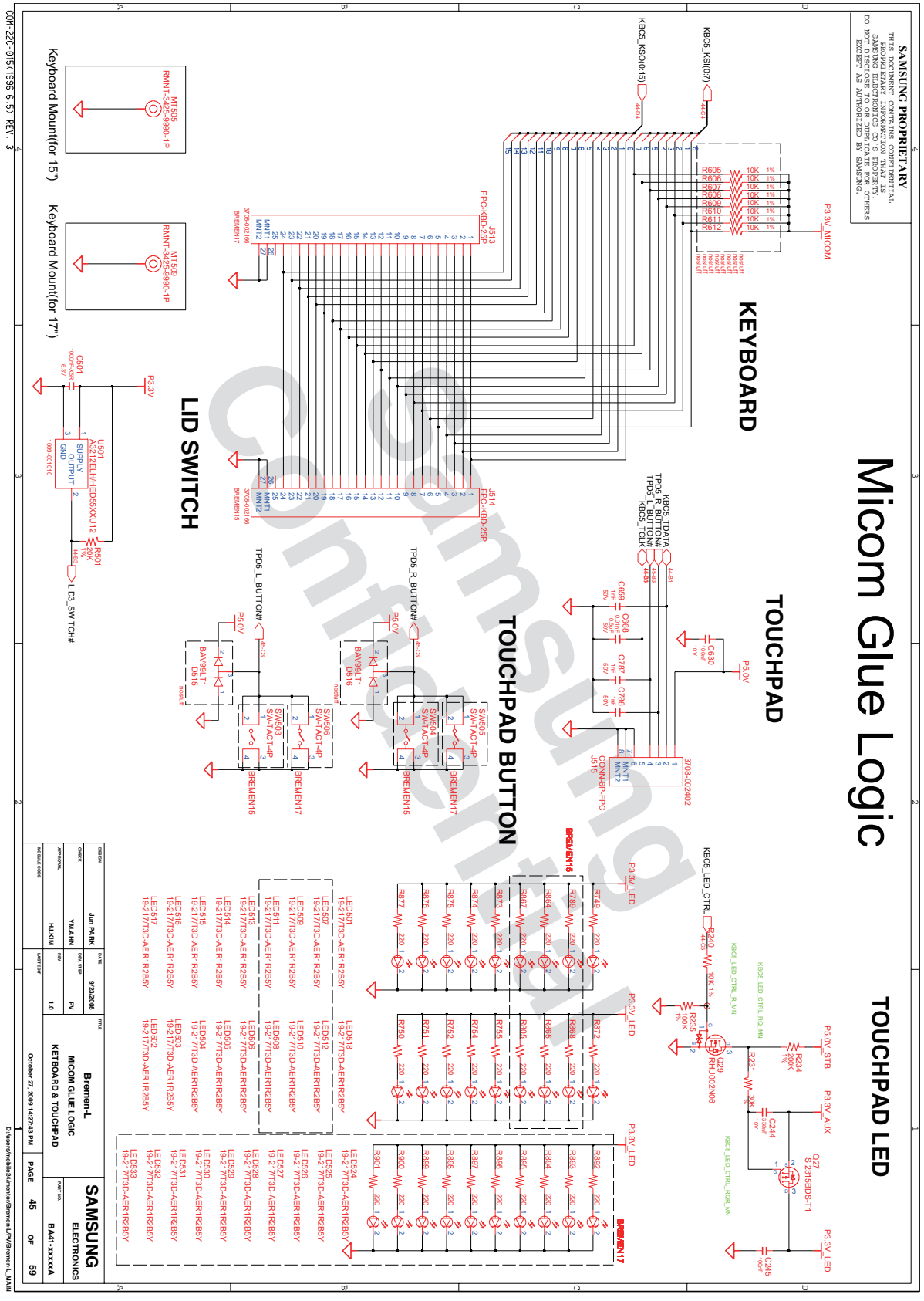

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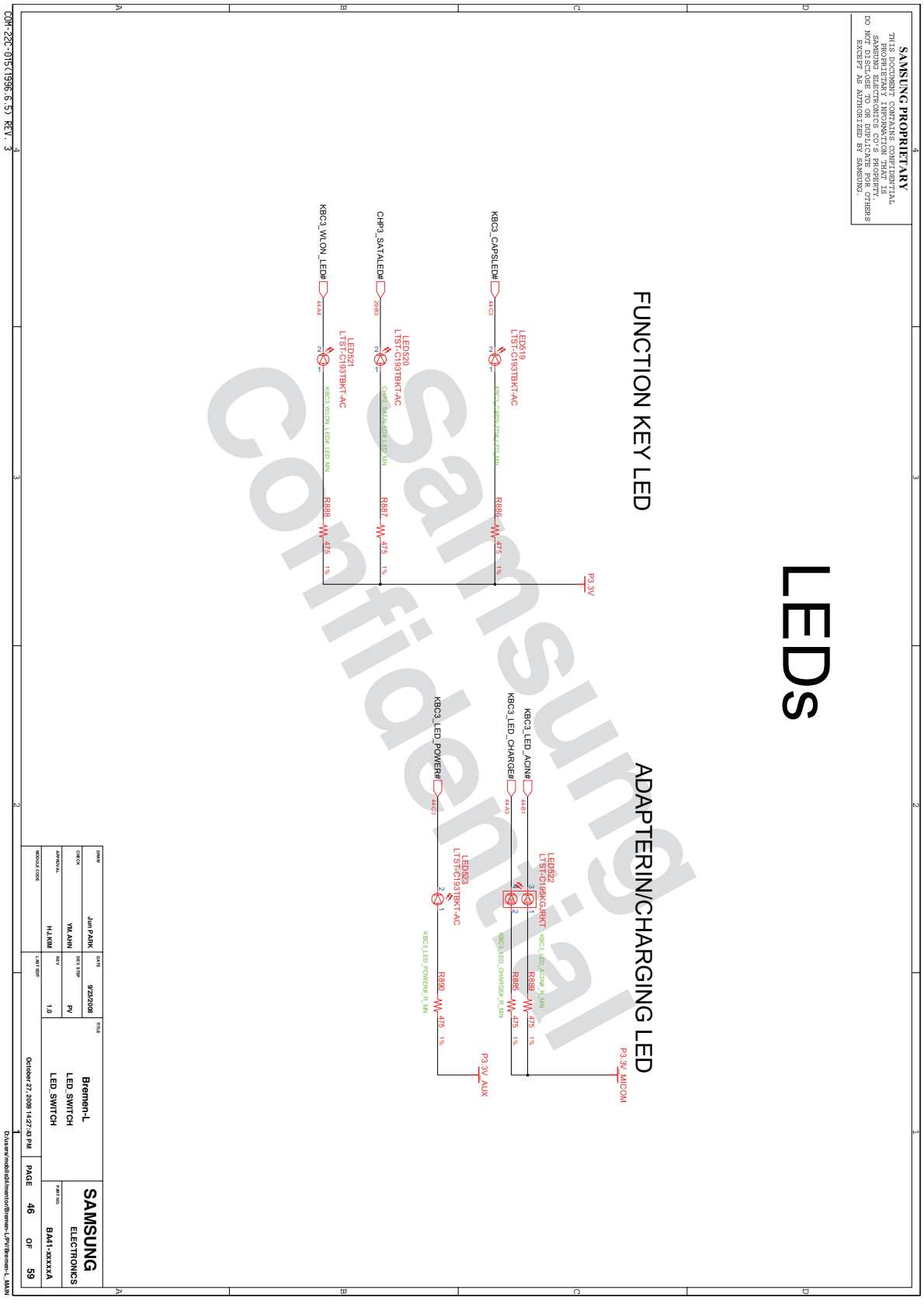

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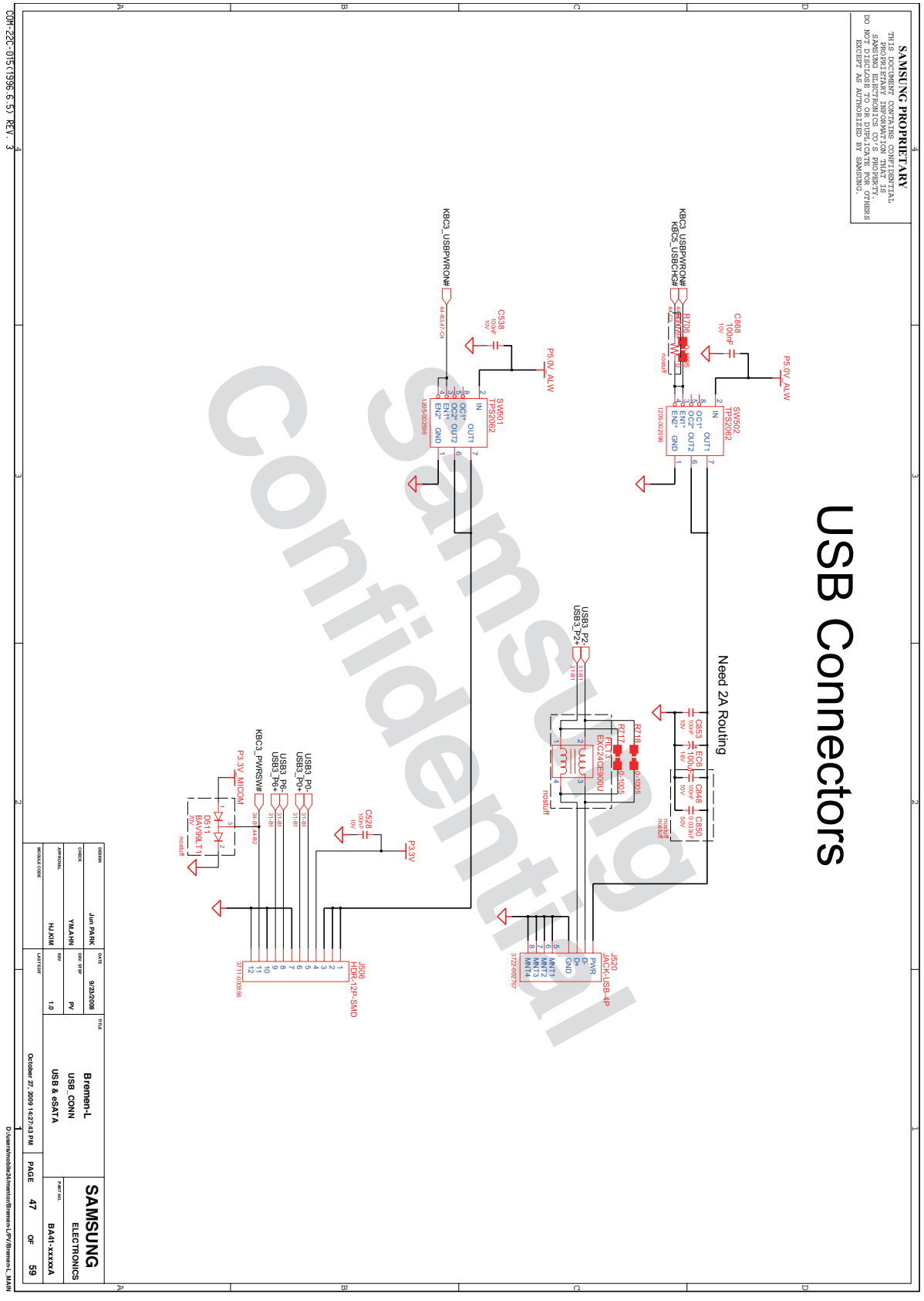

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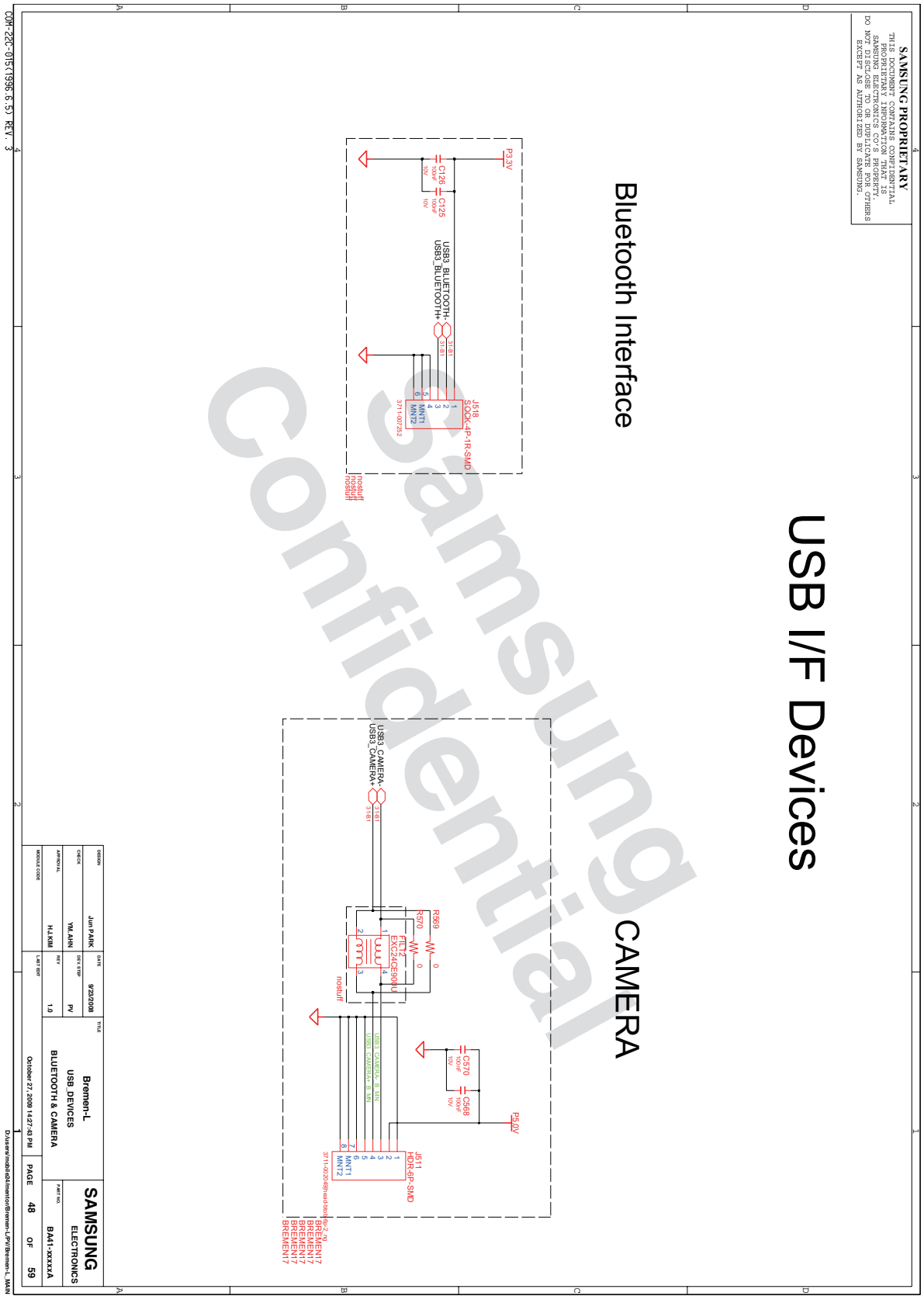

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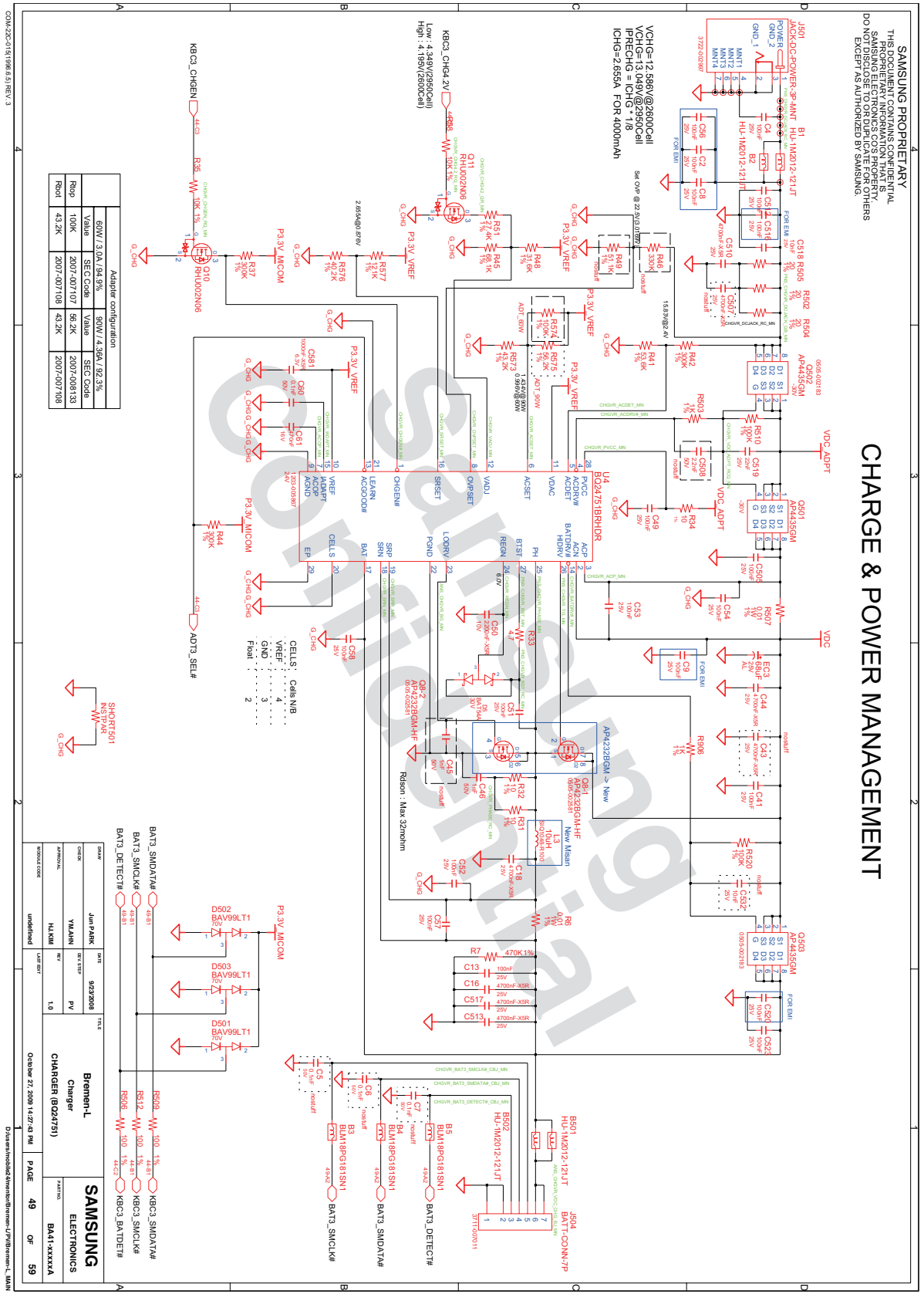

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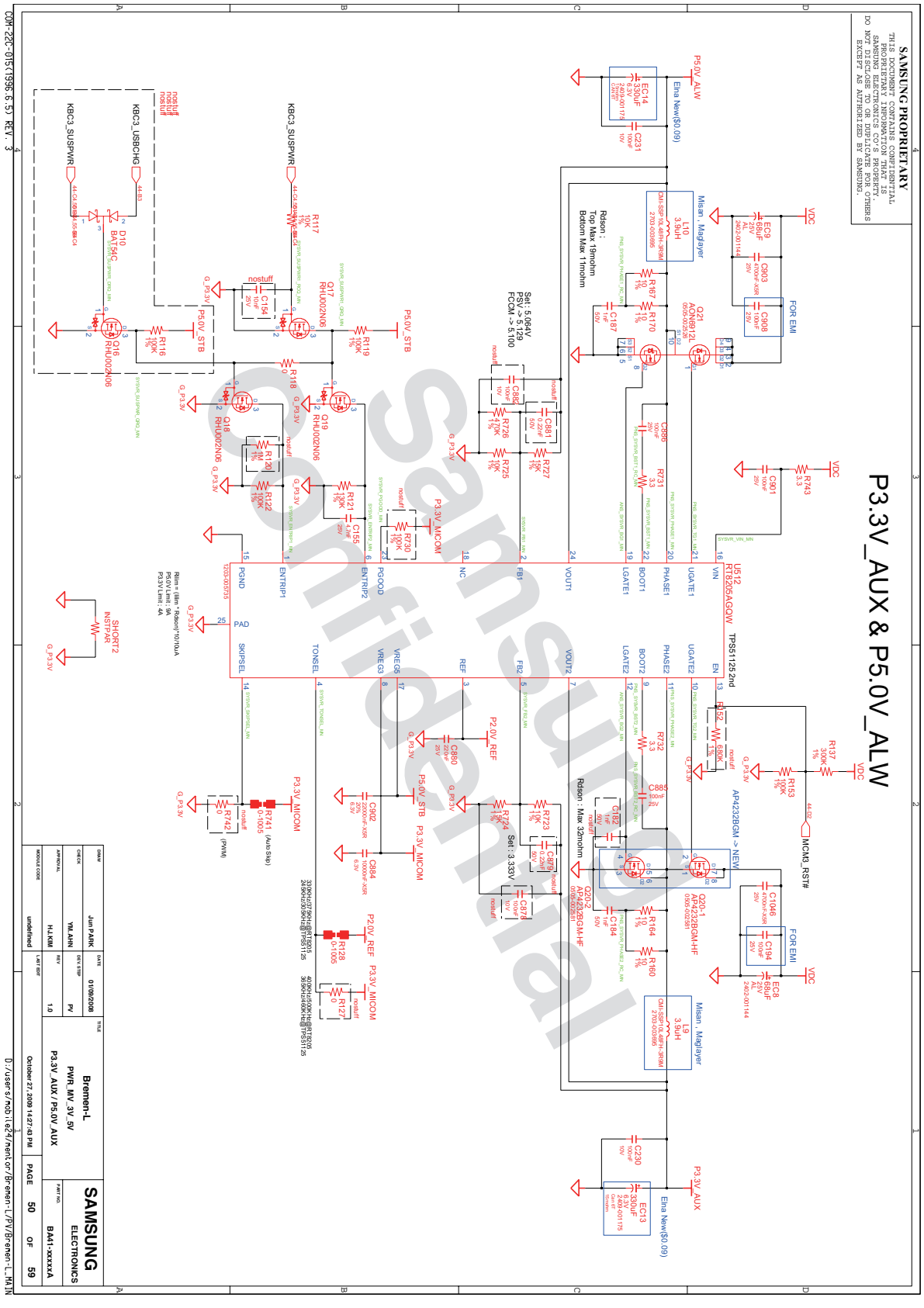

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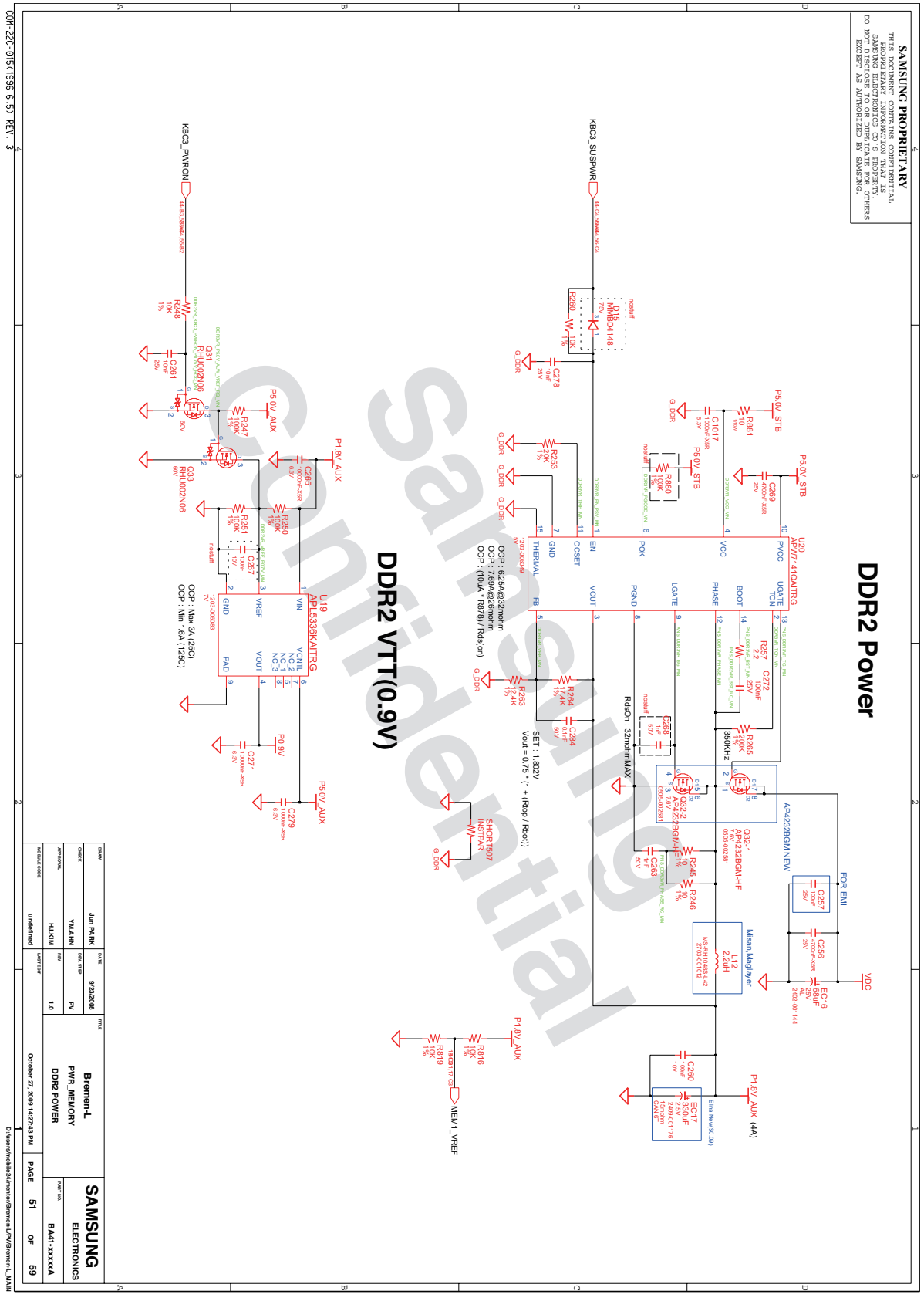

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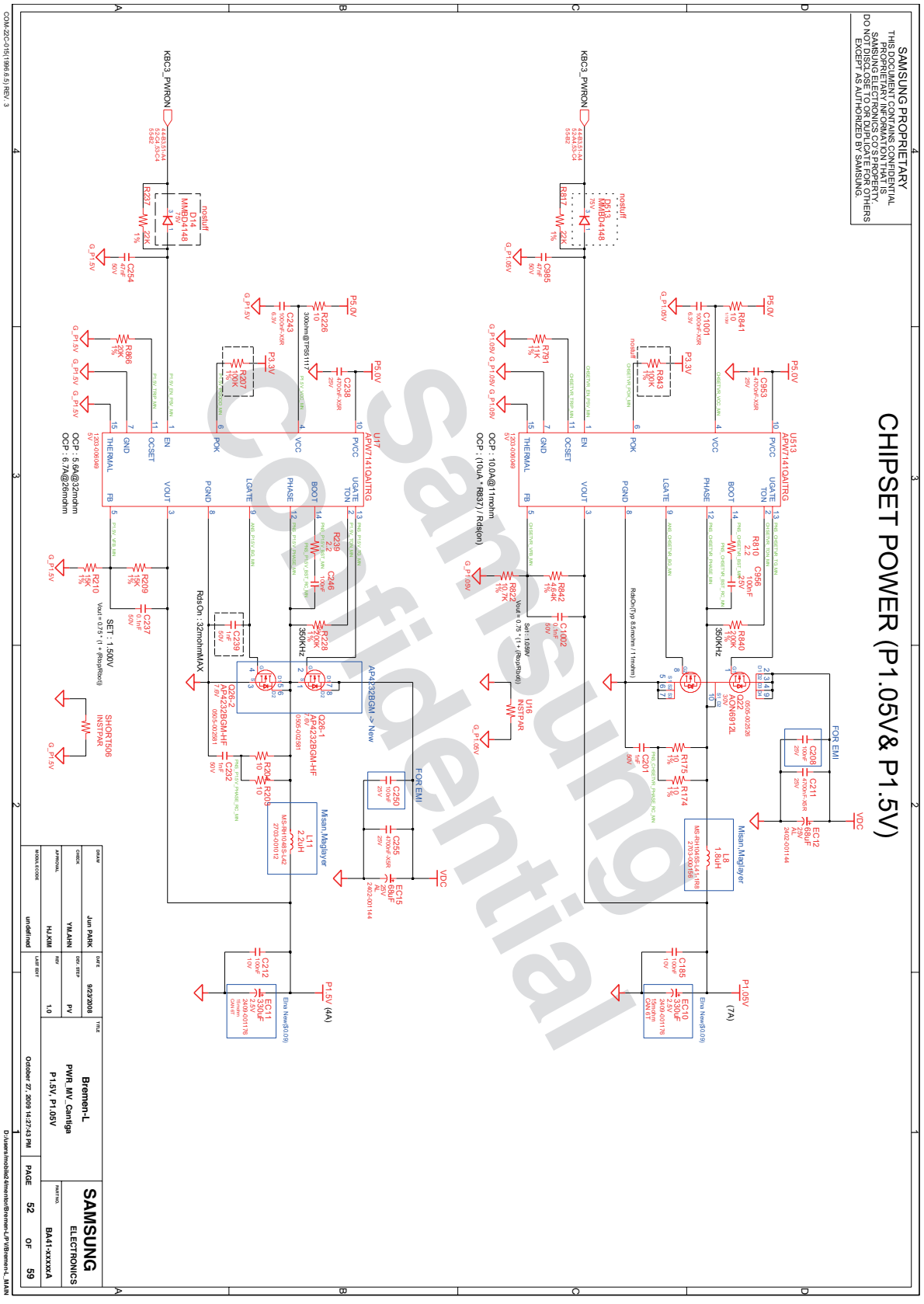

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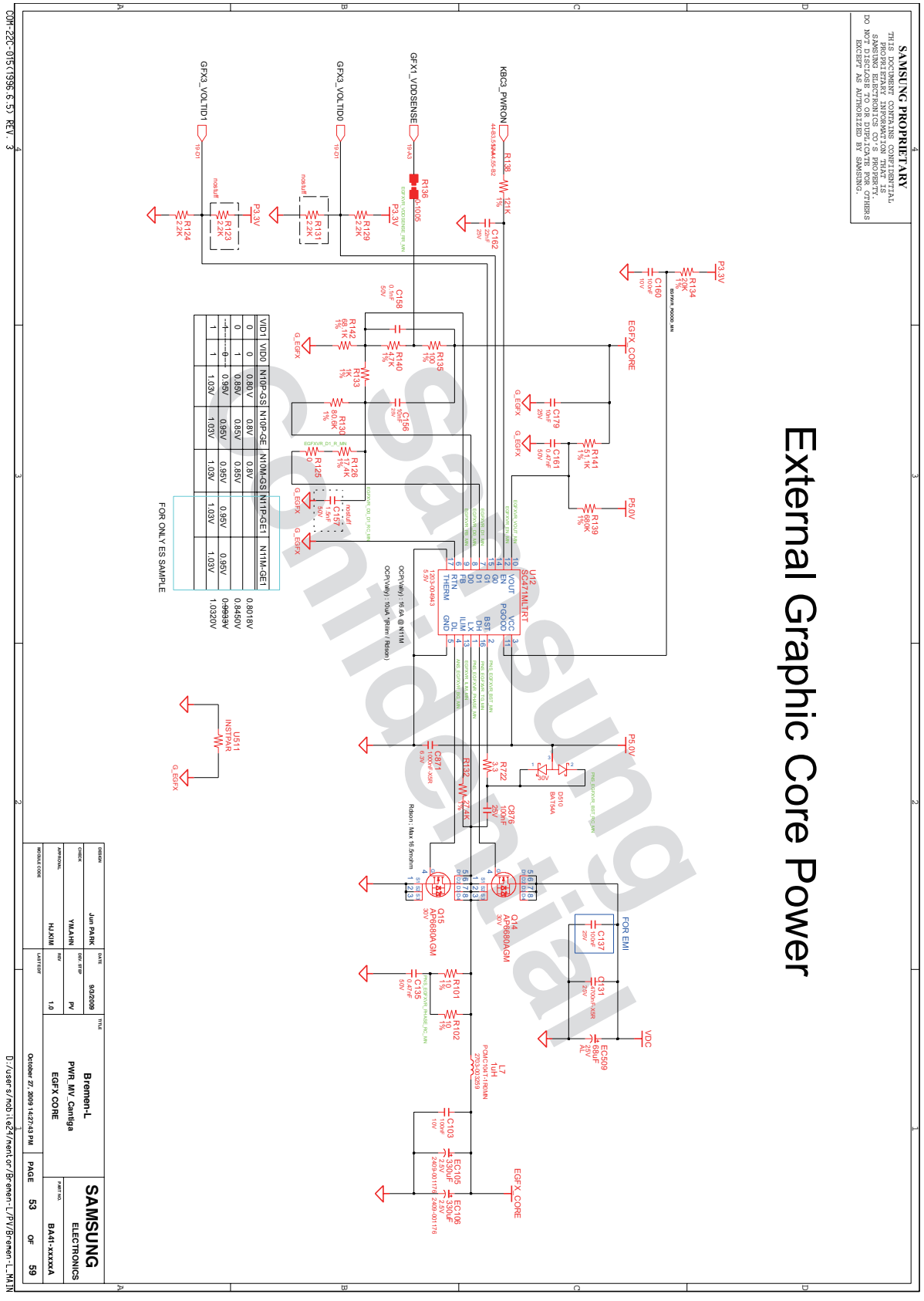

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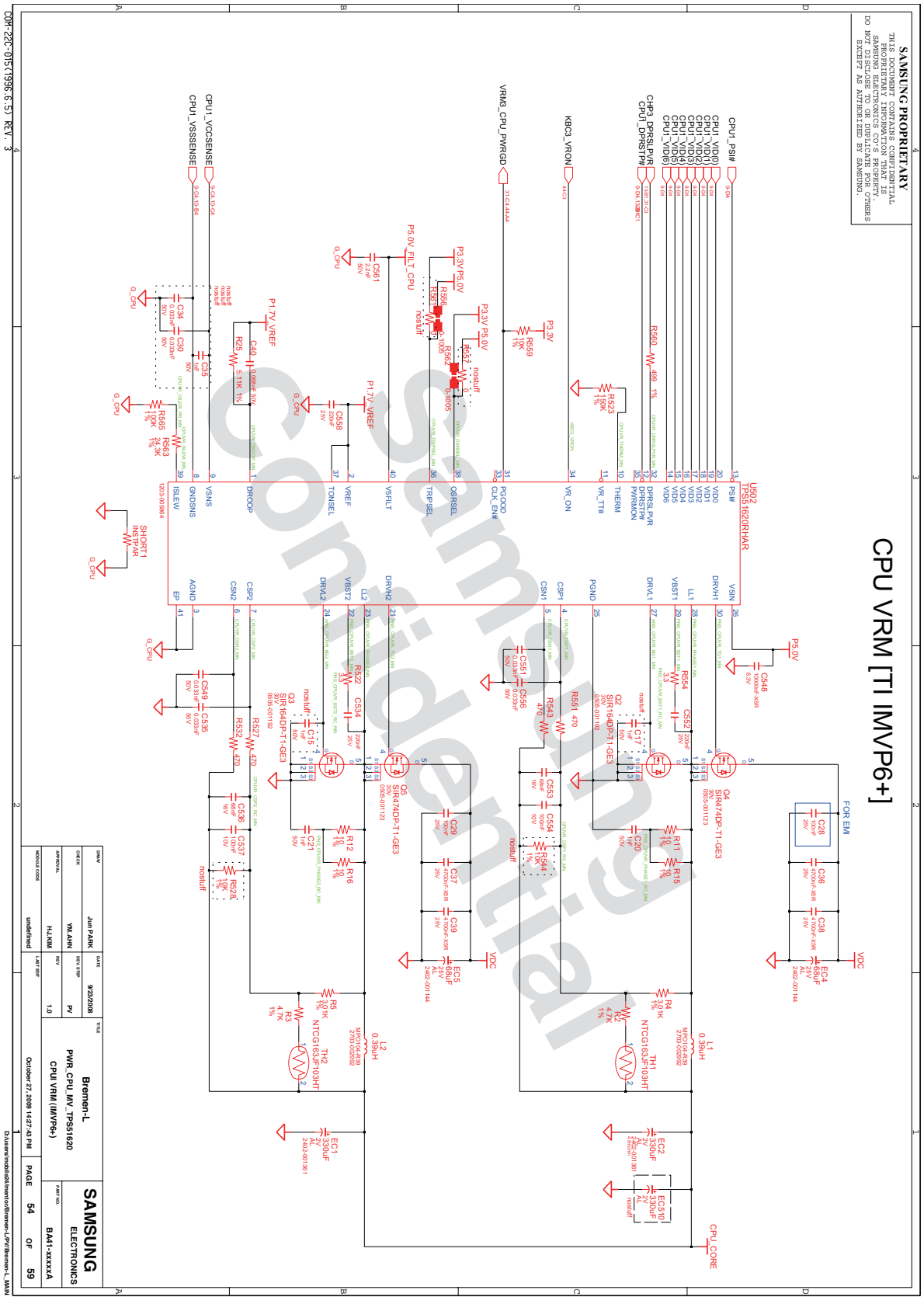

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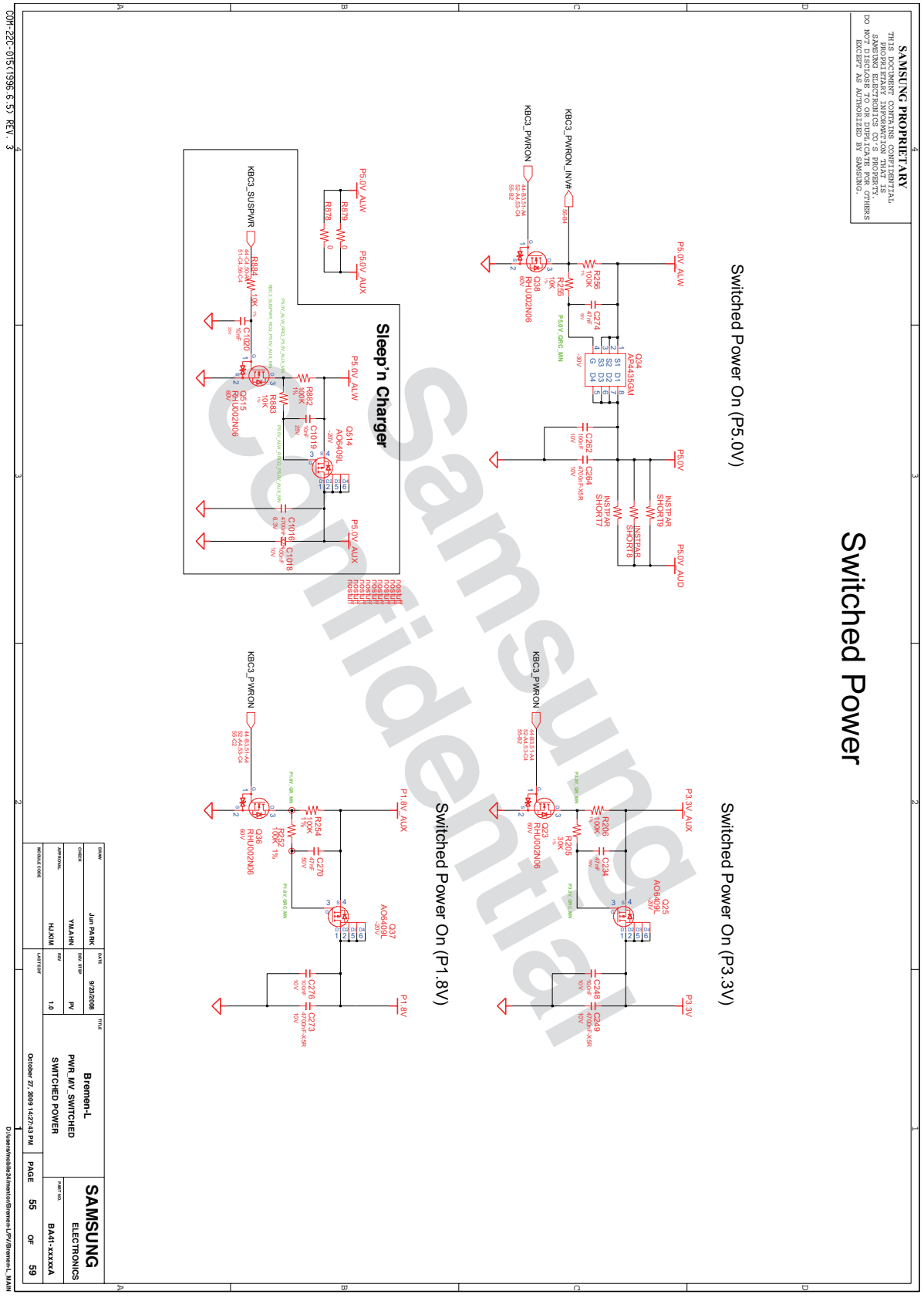

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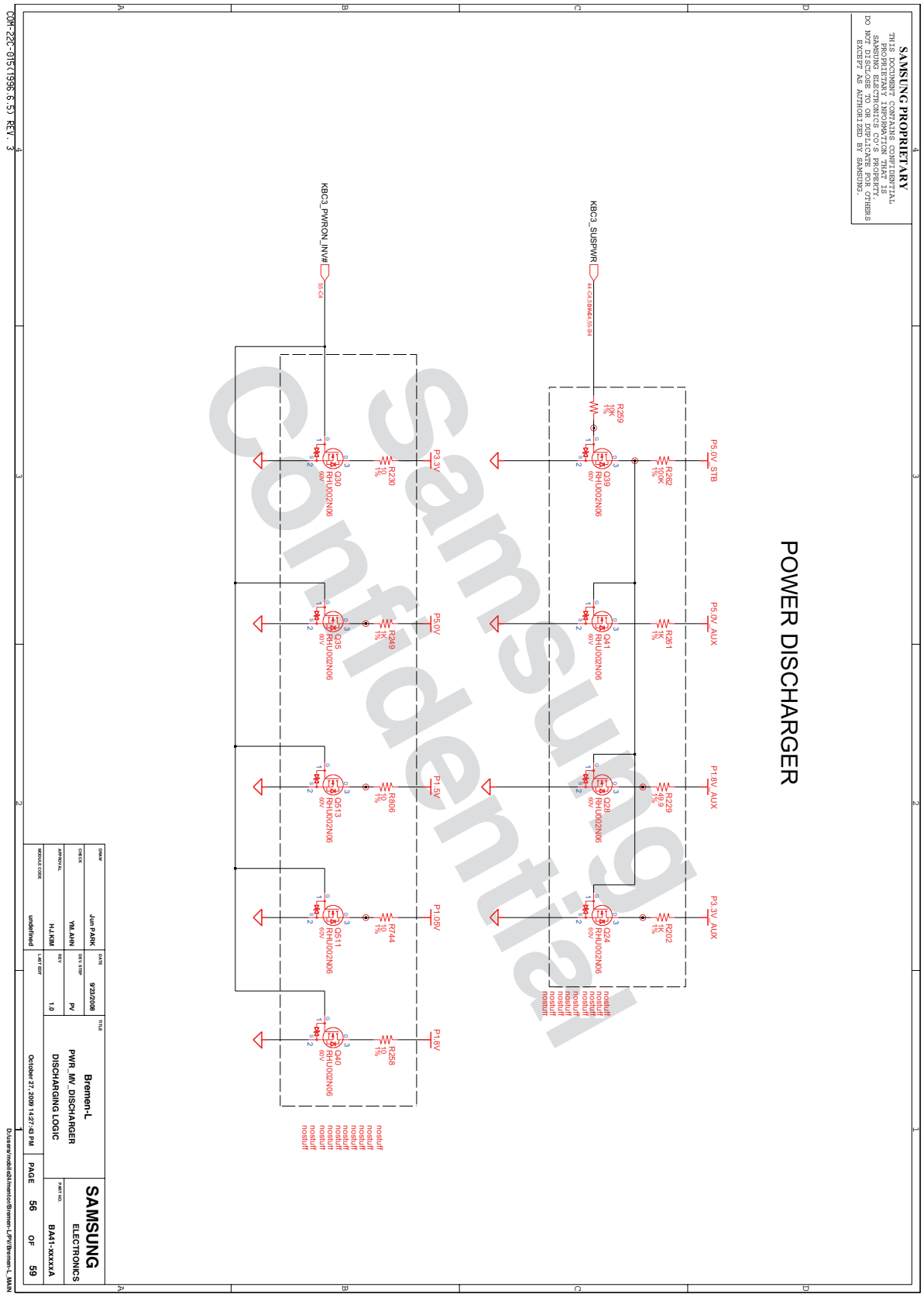

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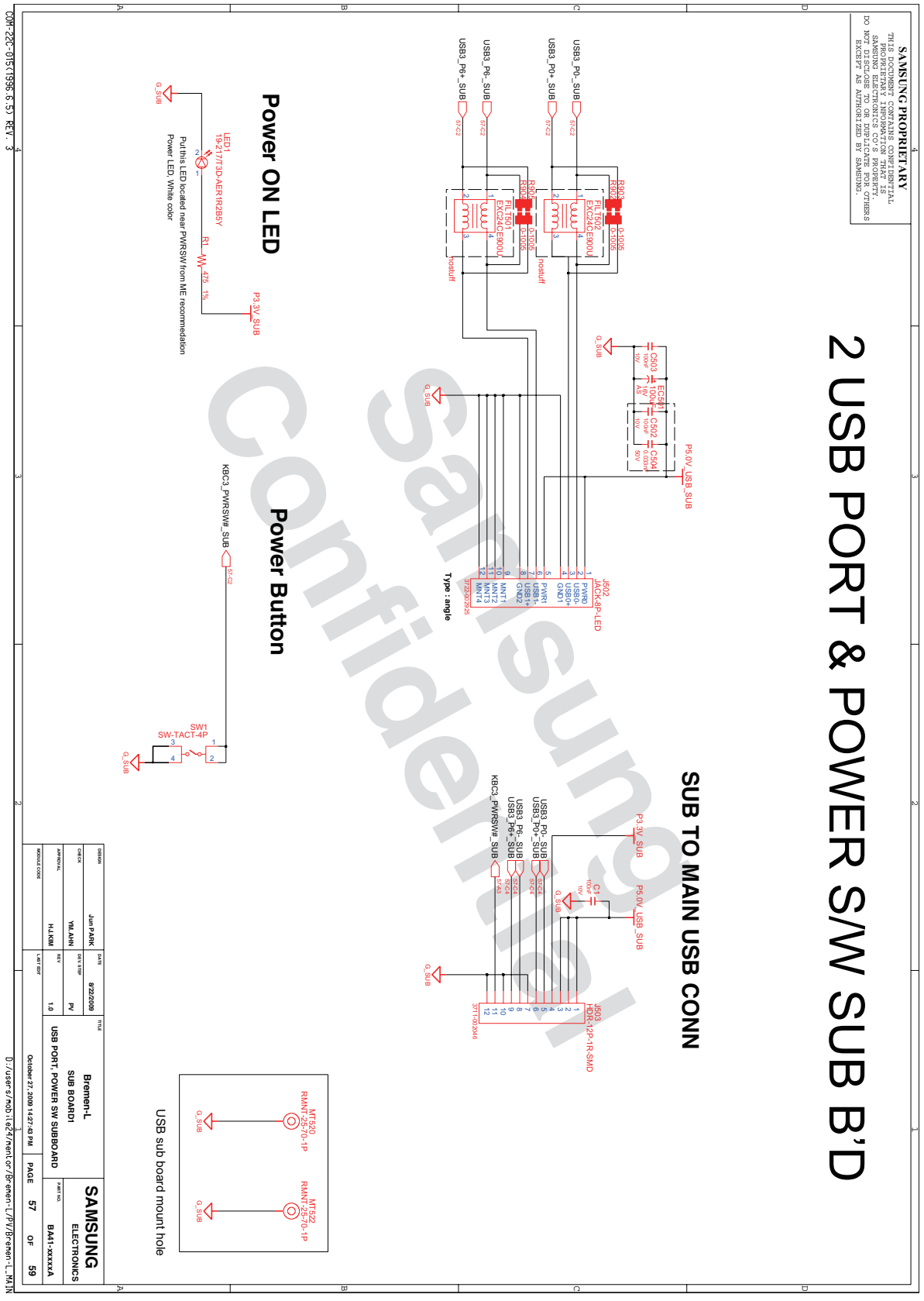

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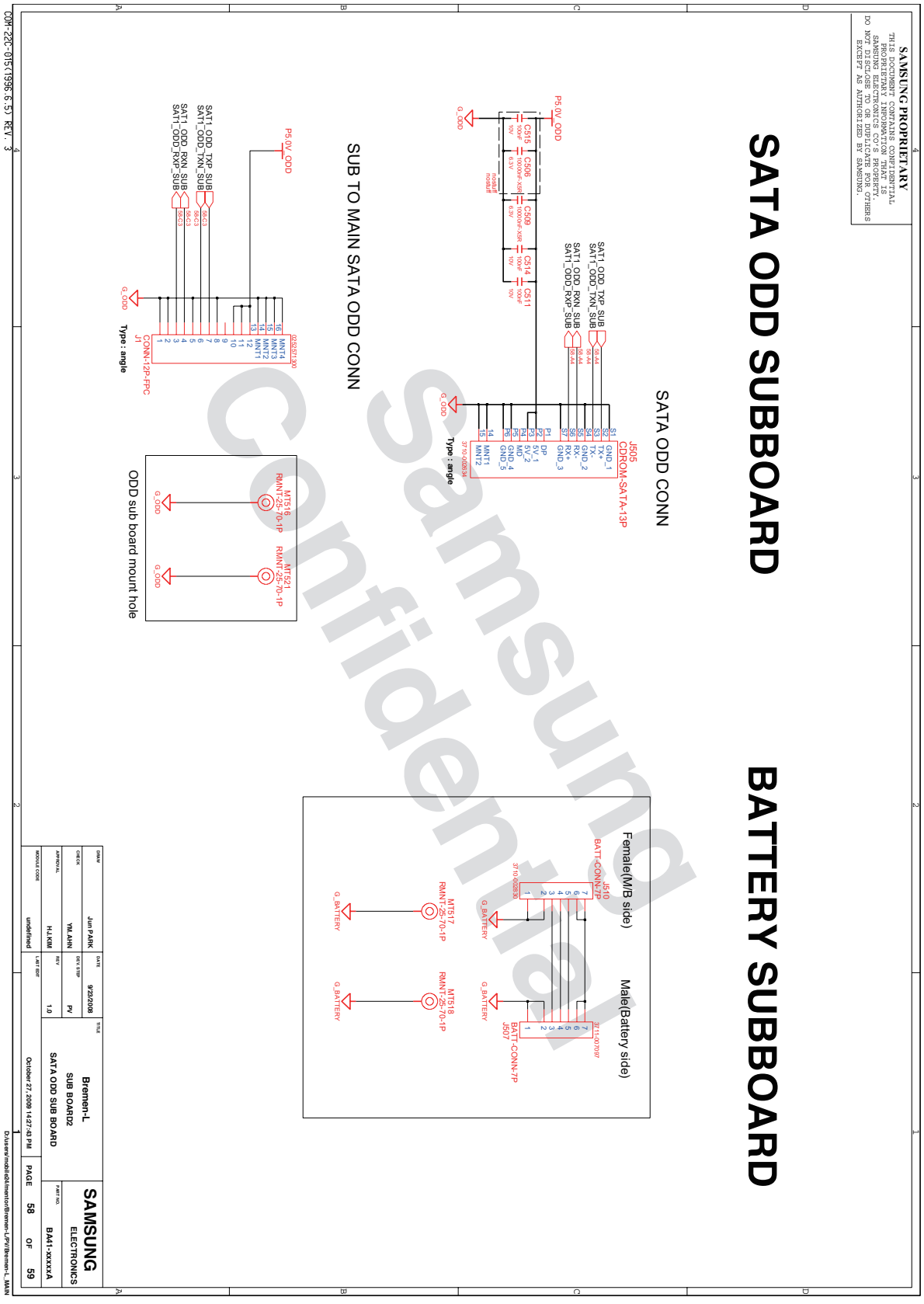

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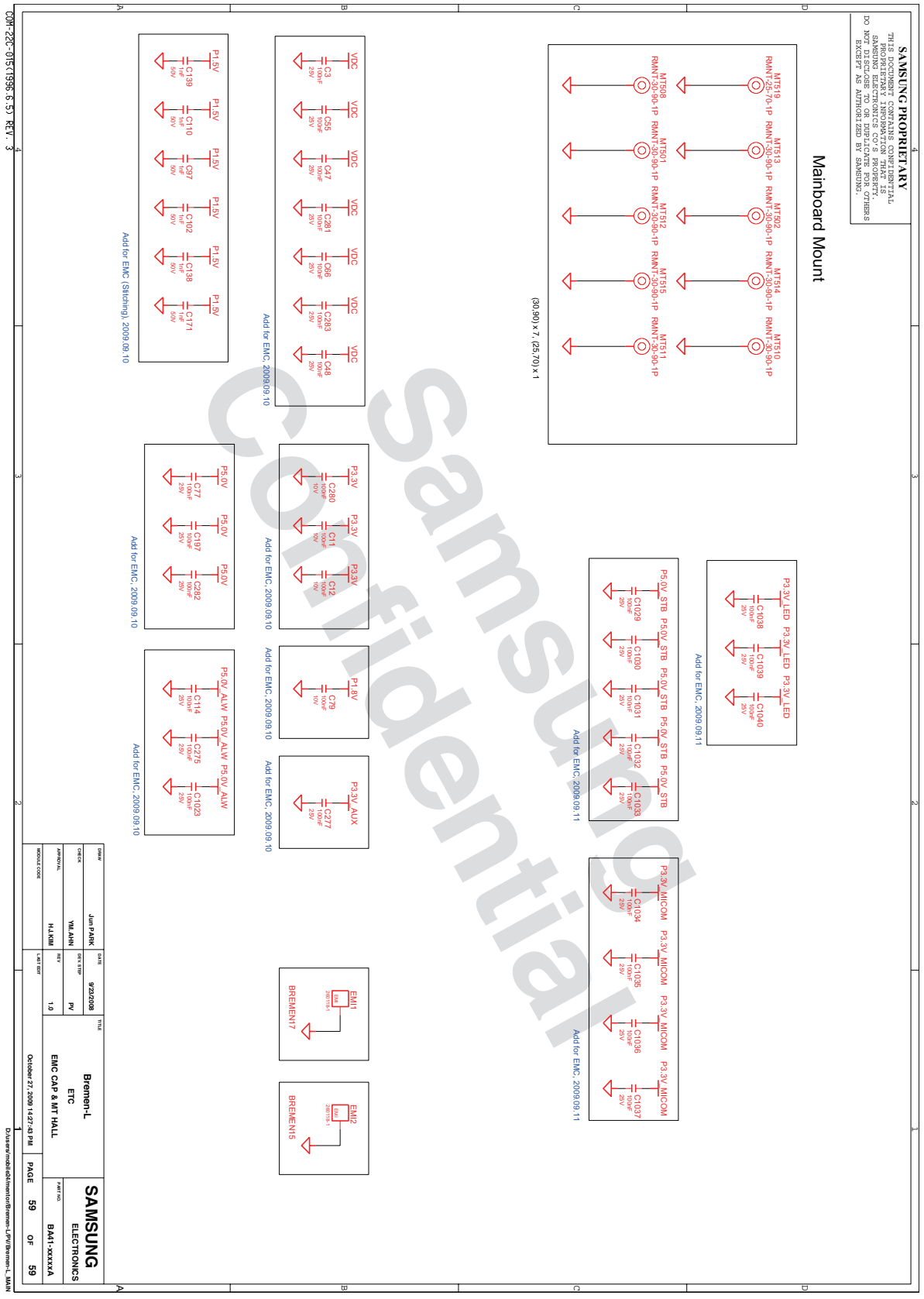

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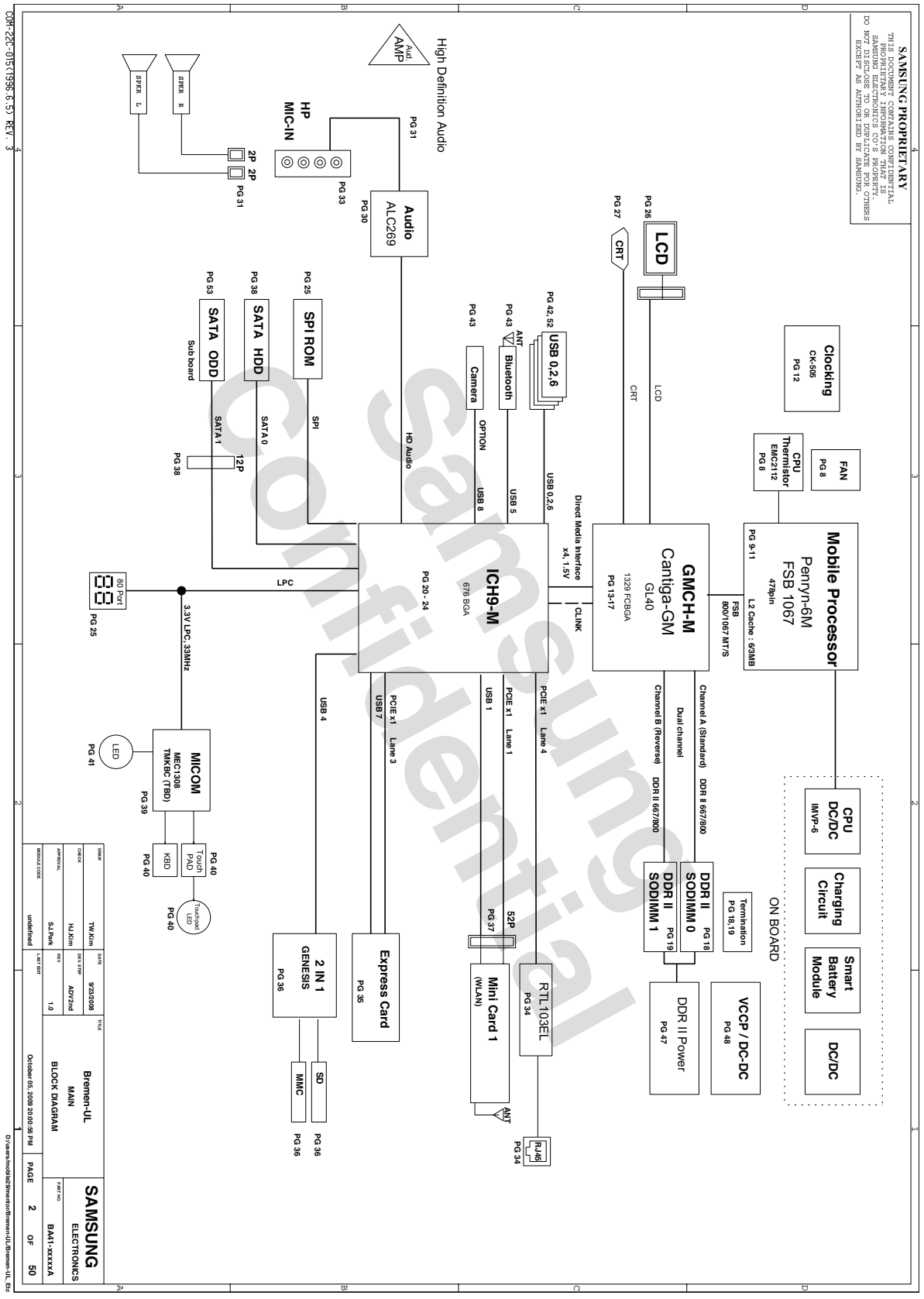


BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A,B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	RealTek 88E8057

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

Voltage Rails

VDC	Primary DC system power supply (9 to 20V)
VCC_CORE	Core Voltage for CPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH9-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

I^2C / SMB Address

Devices	Address	Hex	Bus
ICH9-M	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	SYSTEM PORT 2
3	NC
4	NC
5	Bluetooth
6	Mini PCI Express 2
7	Camera
8	NC
9	NC

PCI Express Assign

PORT #	ASSIGNED TO
0	NC
1	Mini Card 1 (WLAN)
2	NC
3	LOM
4	Mini Card 2 (ROBSON or DVB-T)
5	NC

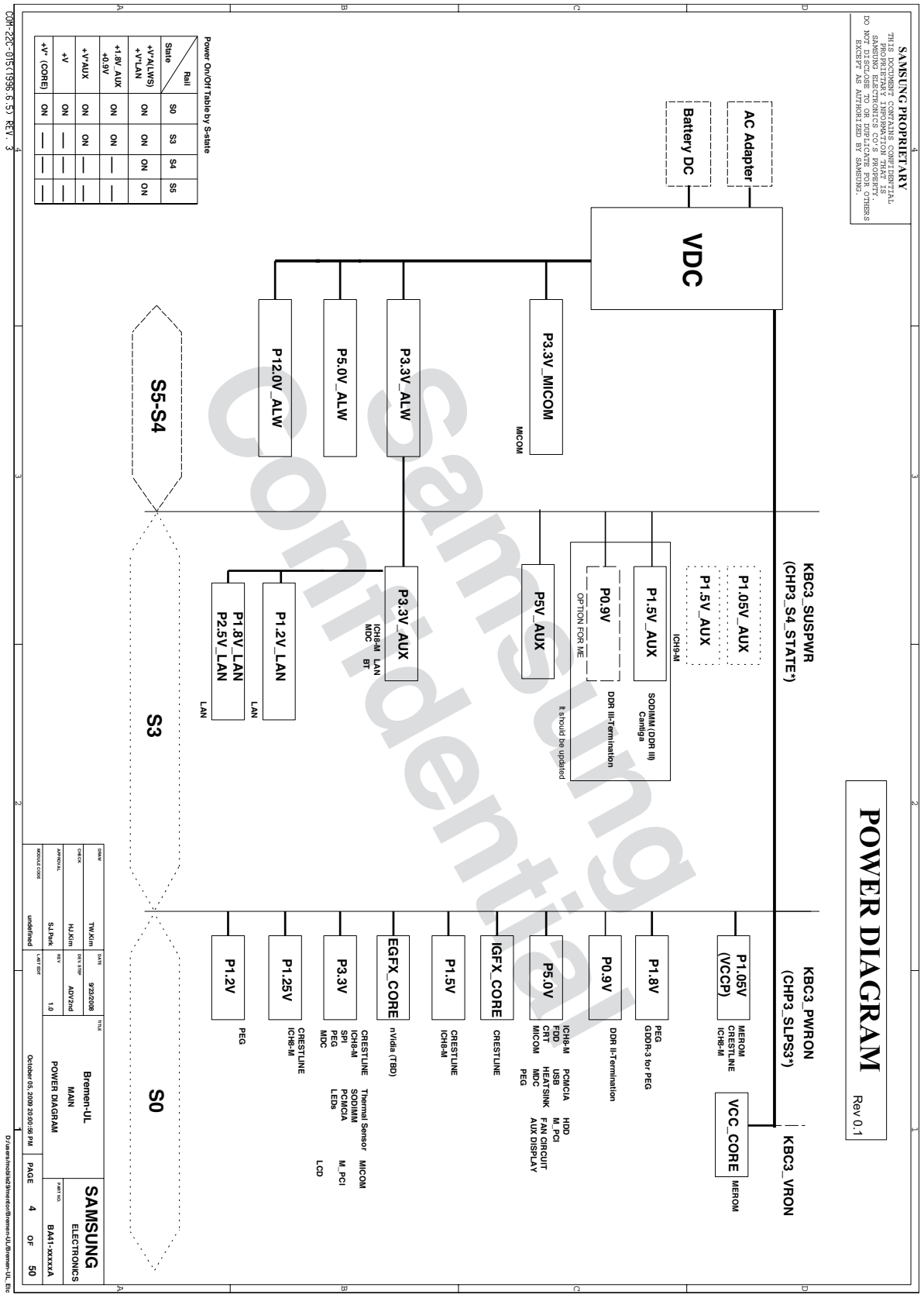
(This table will be update.)

REVISION HISTORY

See rev notes for more information.

DRAW: TW.Kim	DATE: 9/23/2008	TITLE: Bremen-UL	SAMSUNG ELECTRONICS
CHECK: HJ.Kim	DEV. STEP: ADV2nd	MAIN	
APPROVAL: SJ.Park	REV: 1.0	BOARD INFO	PART NO.: BA41-XXXXXA
MODULE CODE: undefined	LAST EDIT: October 05, 2009 20:00:56 PM	PAGE 3 OF 50	

8. Block Diagram and Schematic



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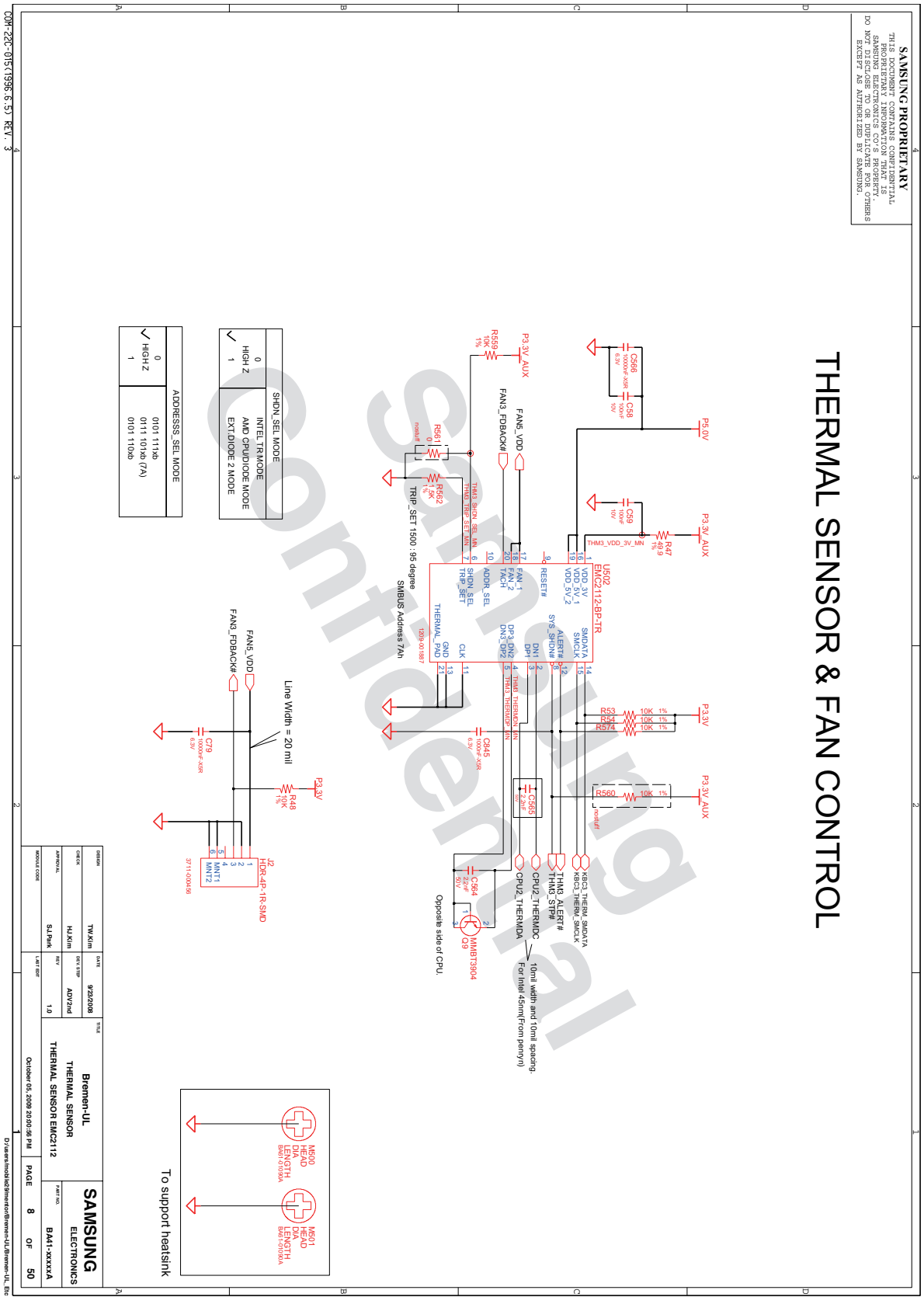

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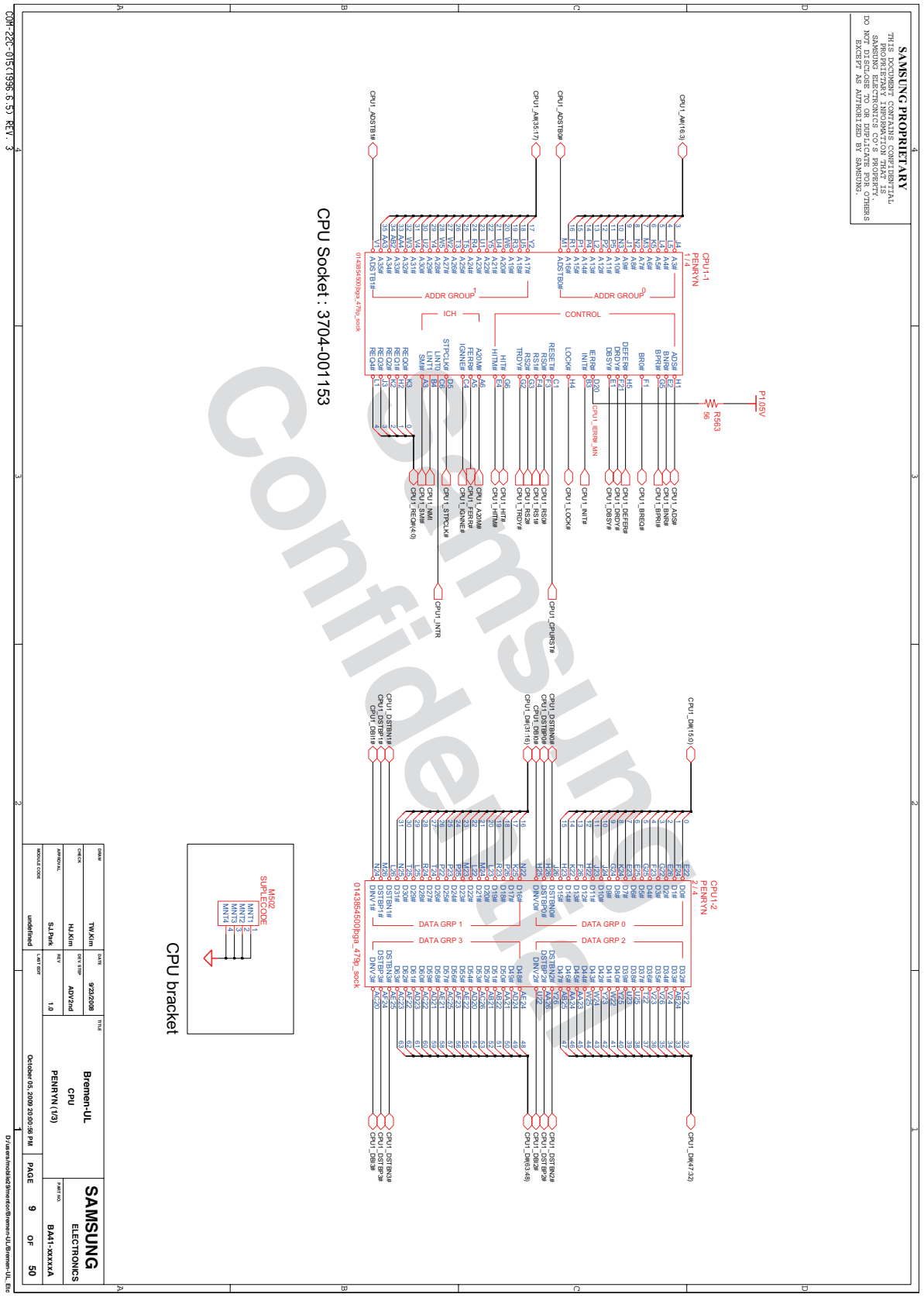

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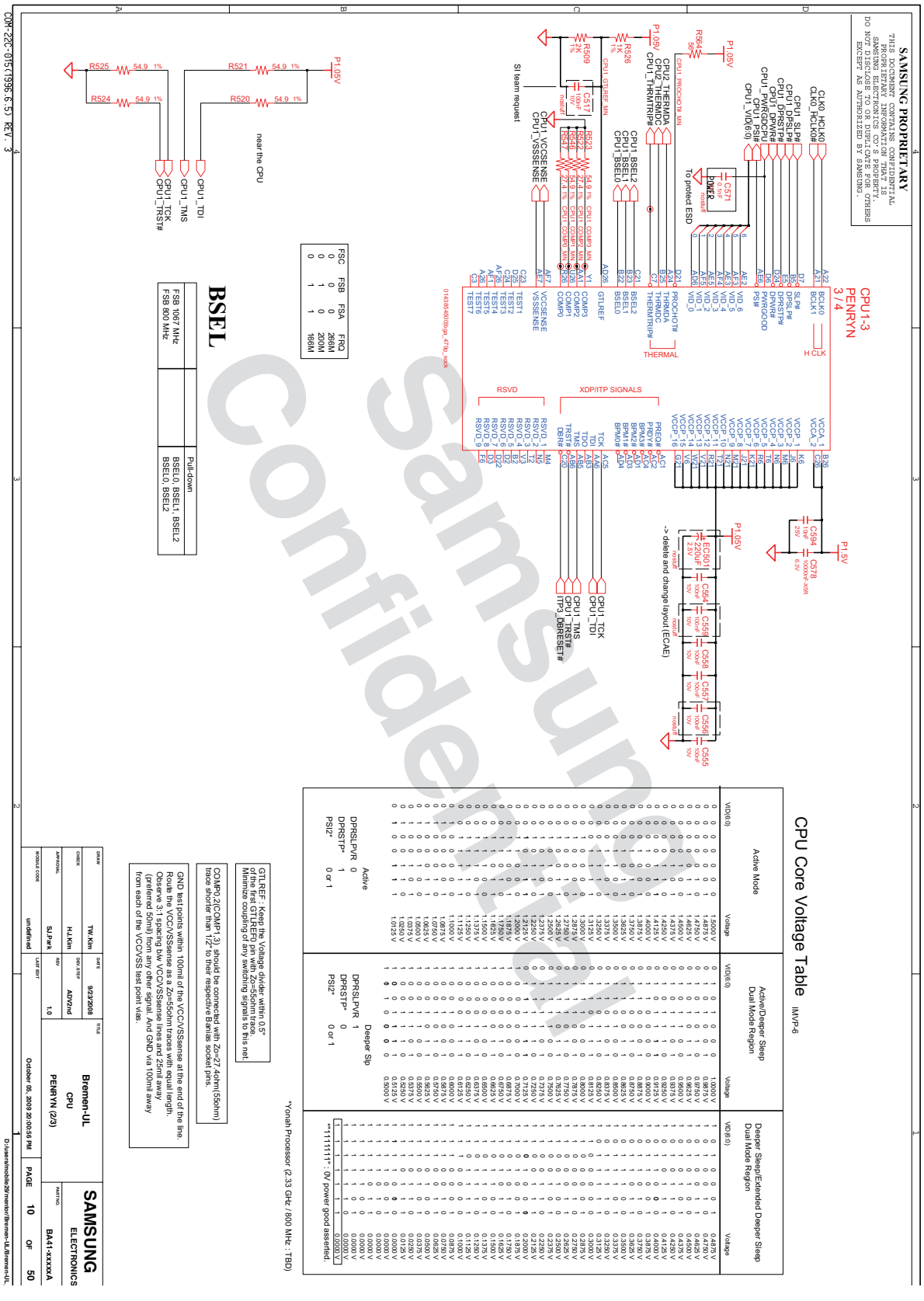

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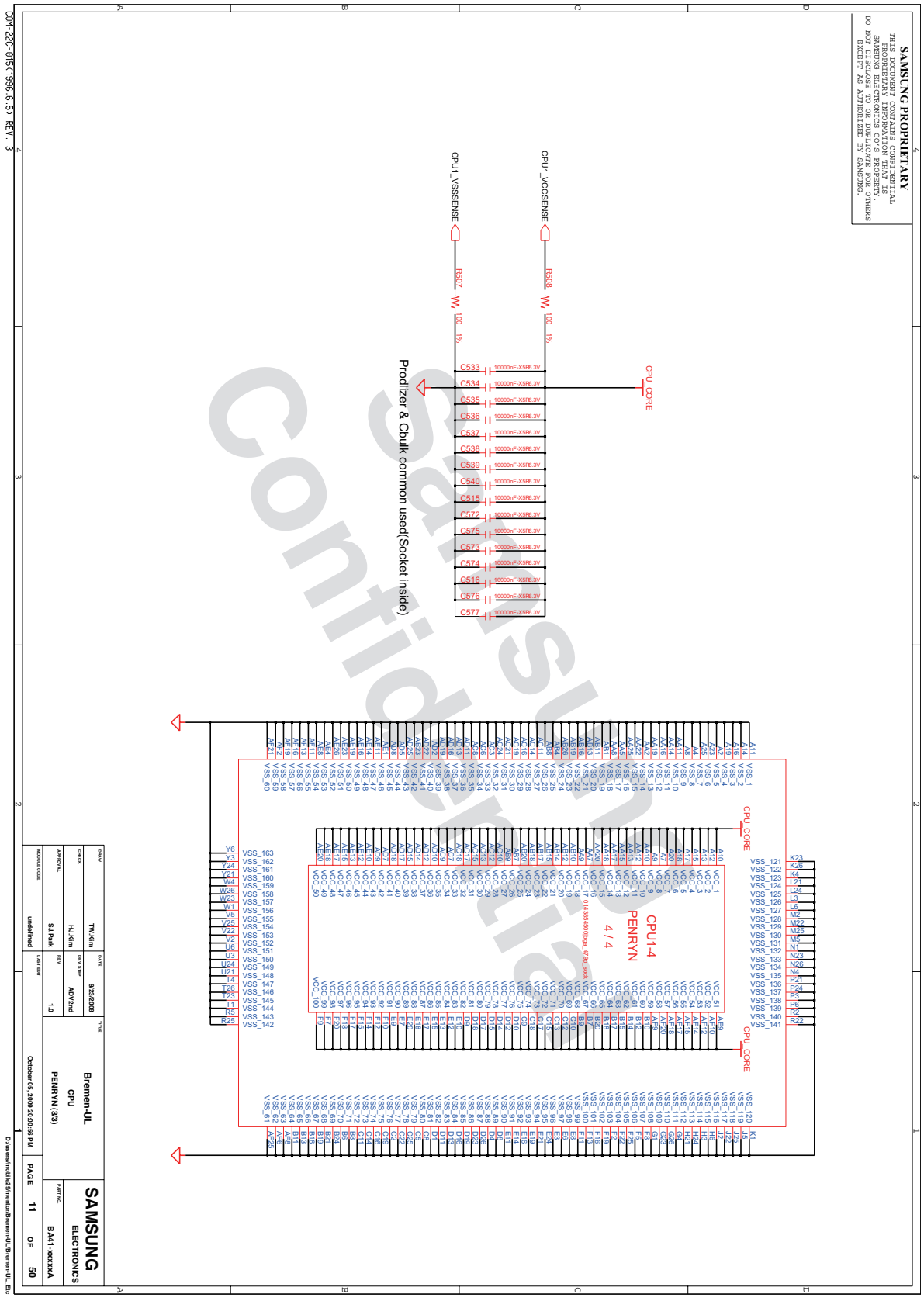

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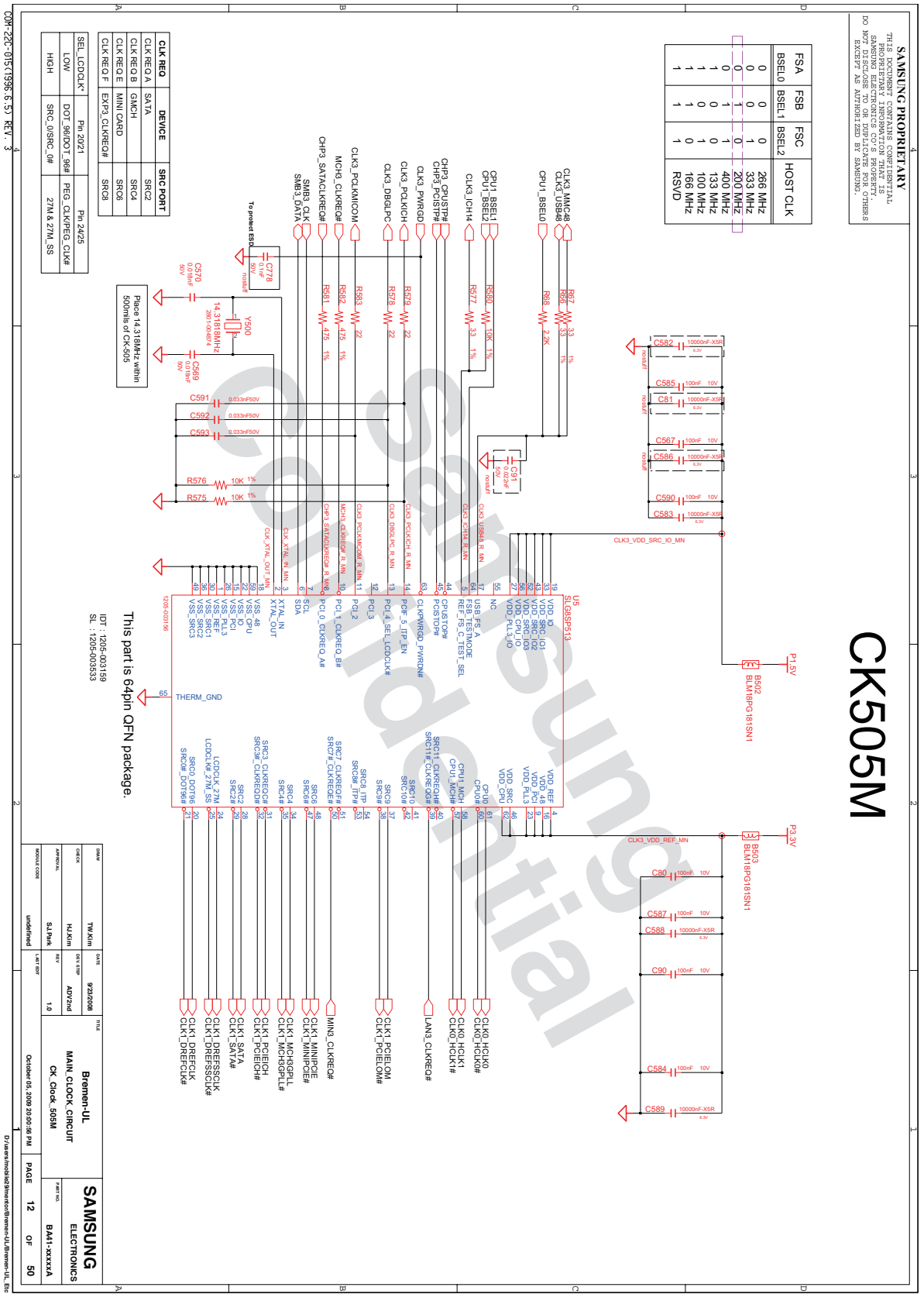

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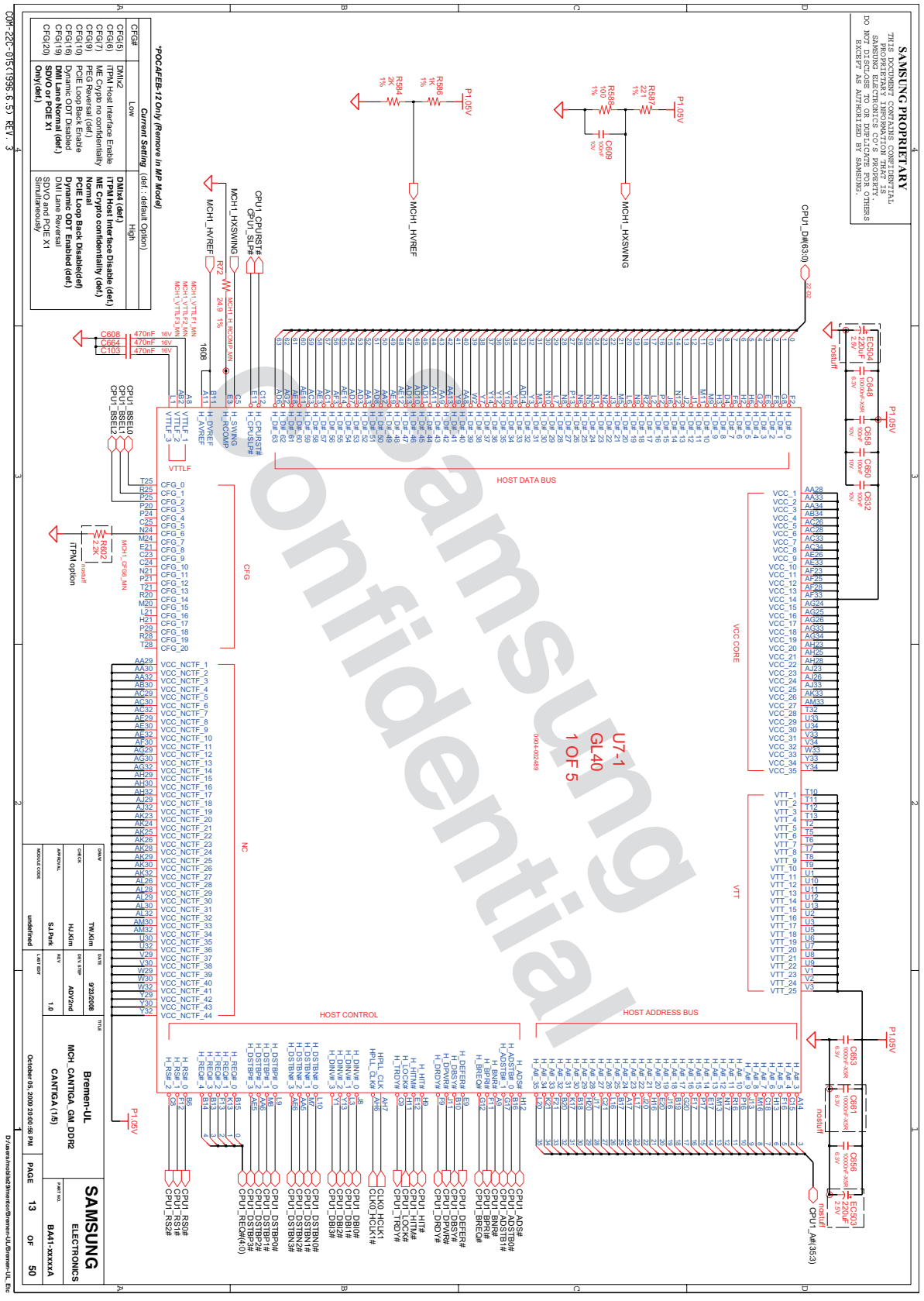

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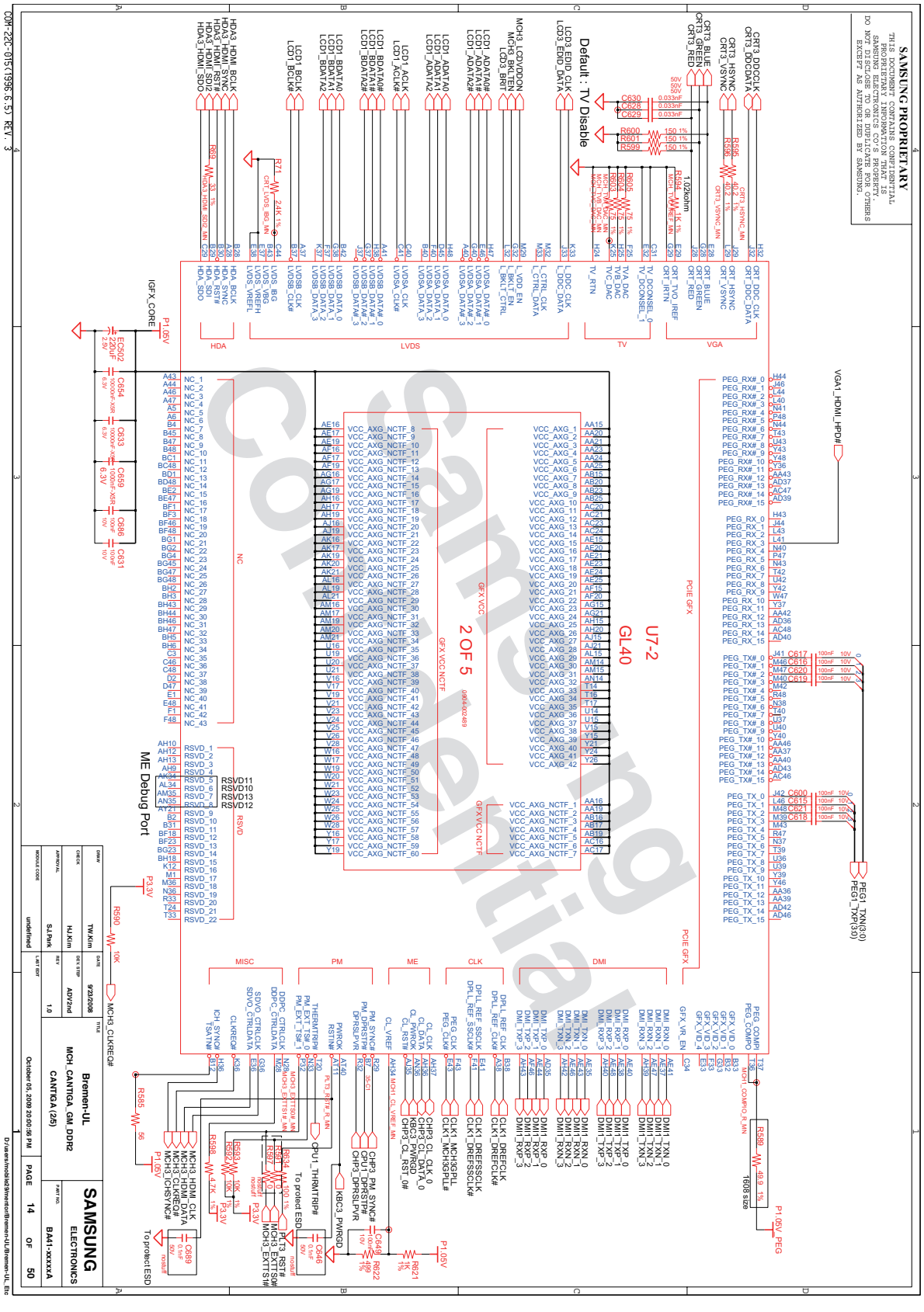

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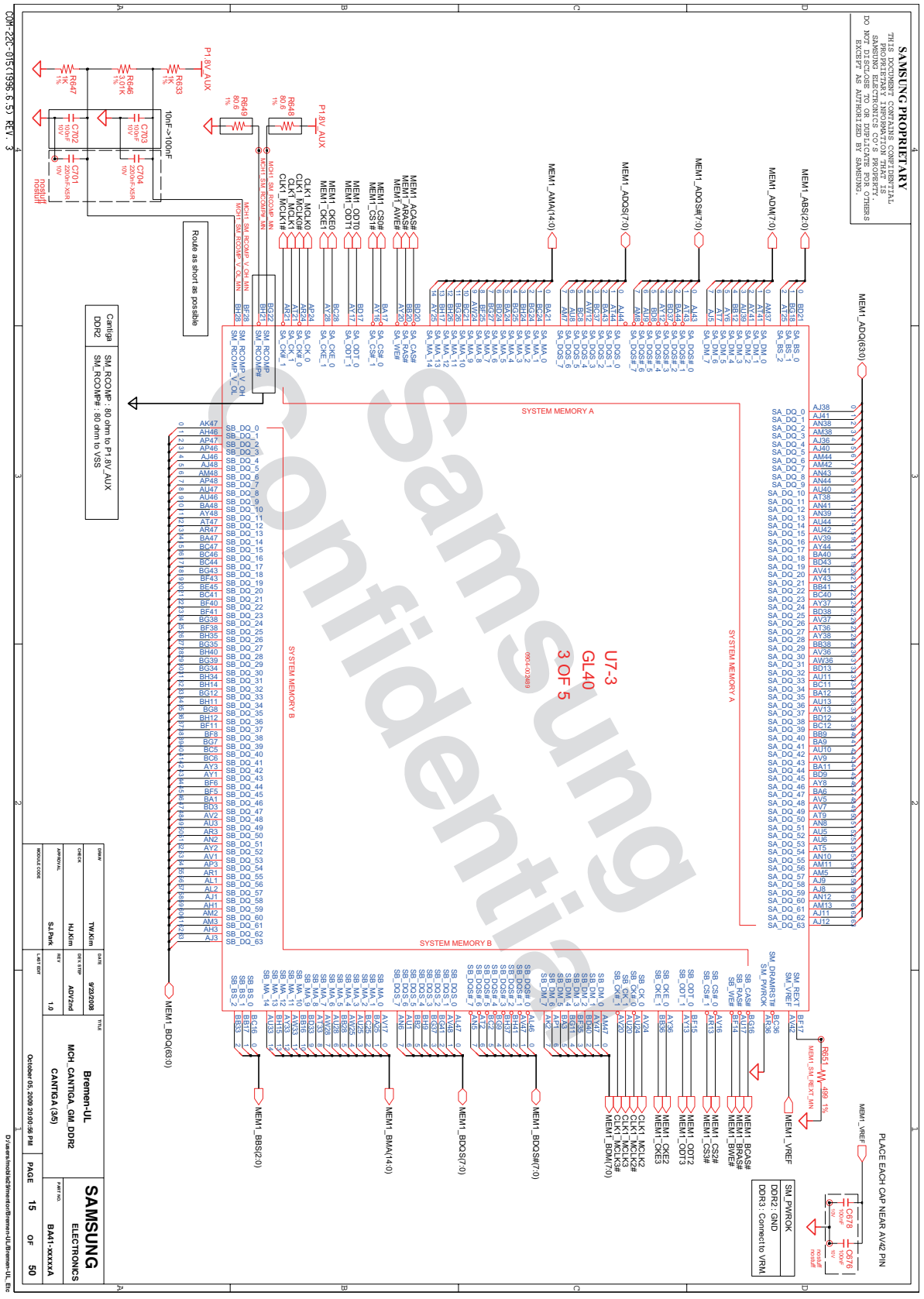

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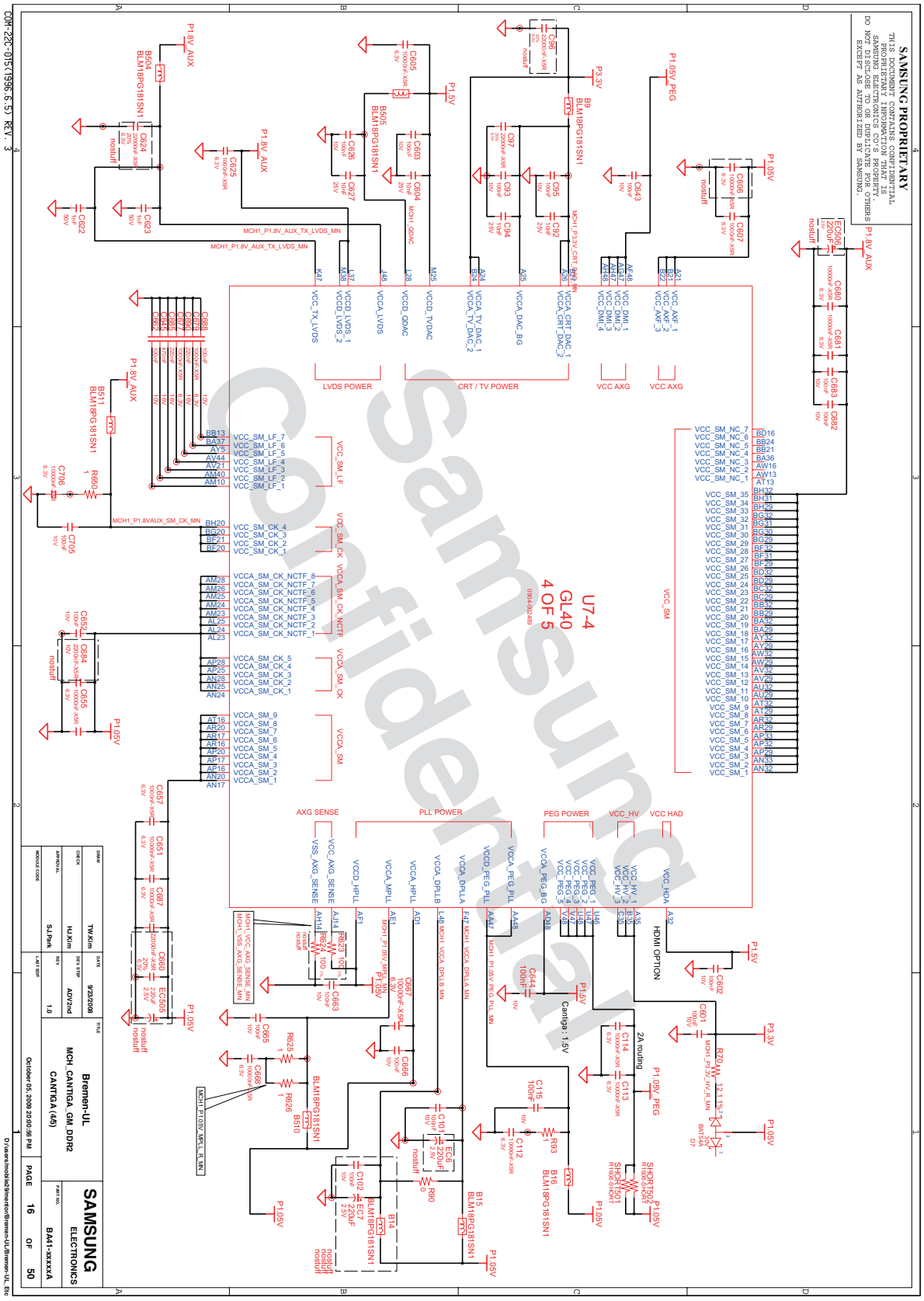

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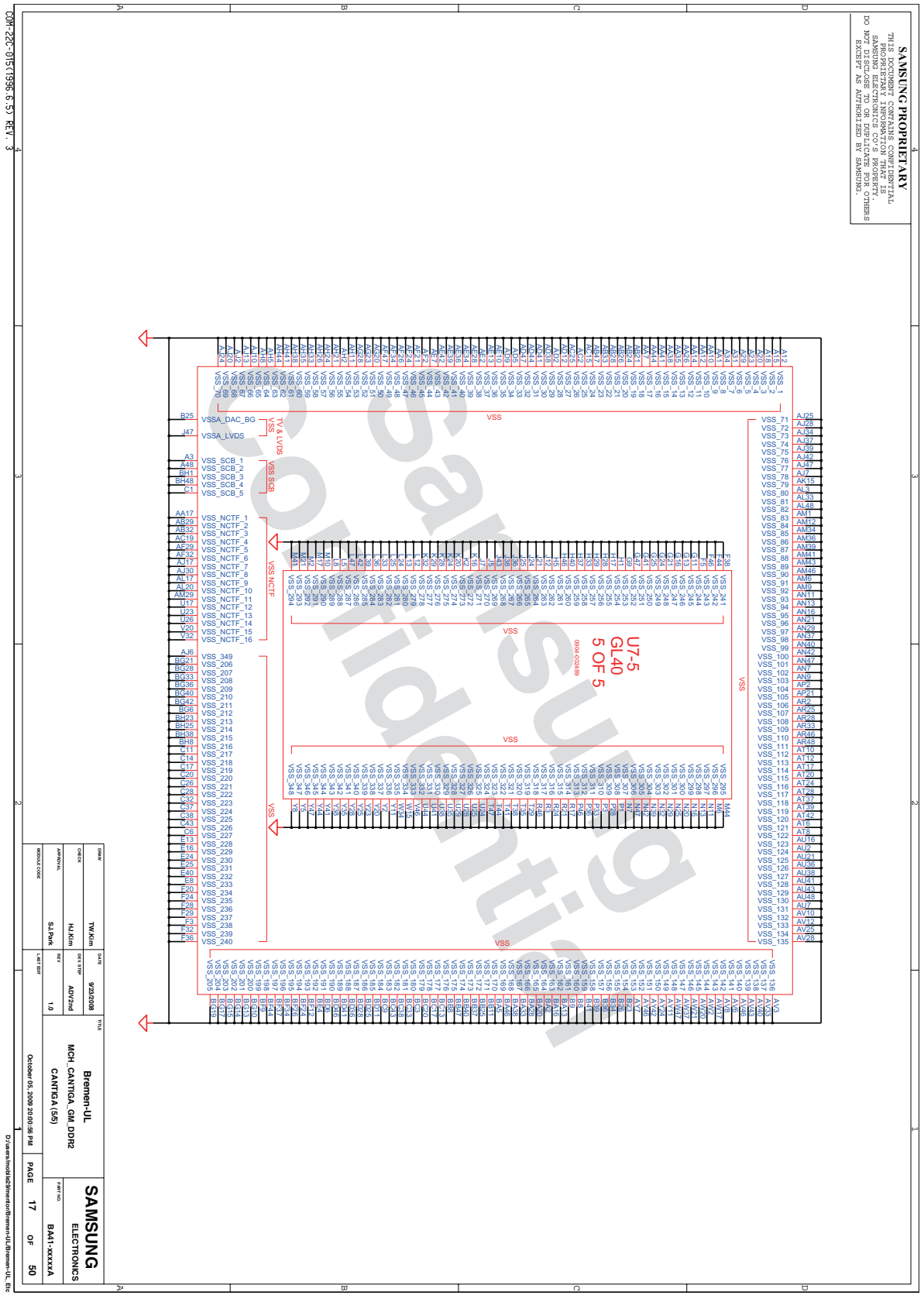

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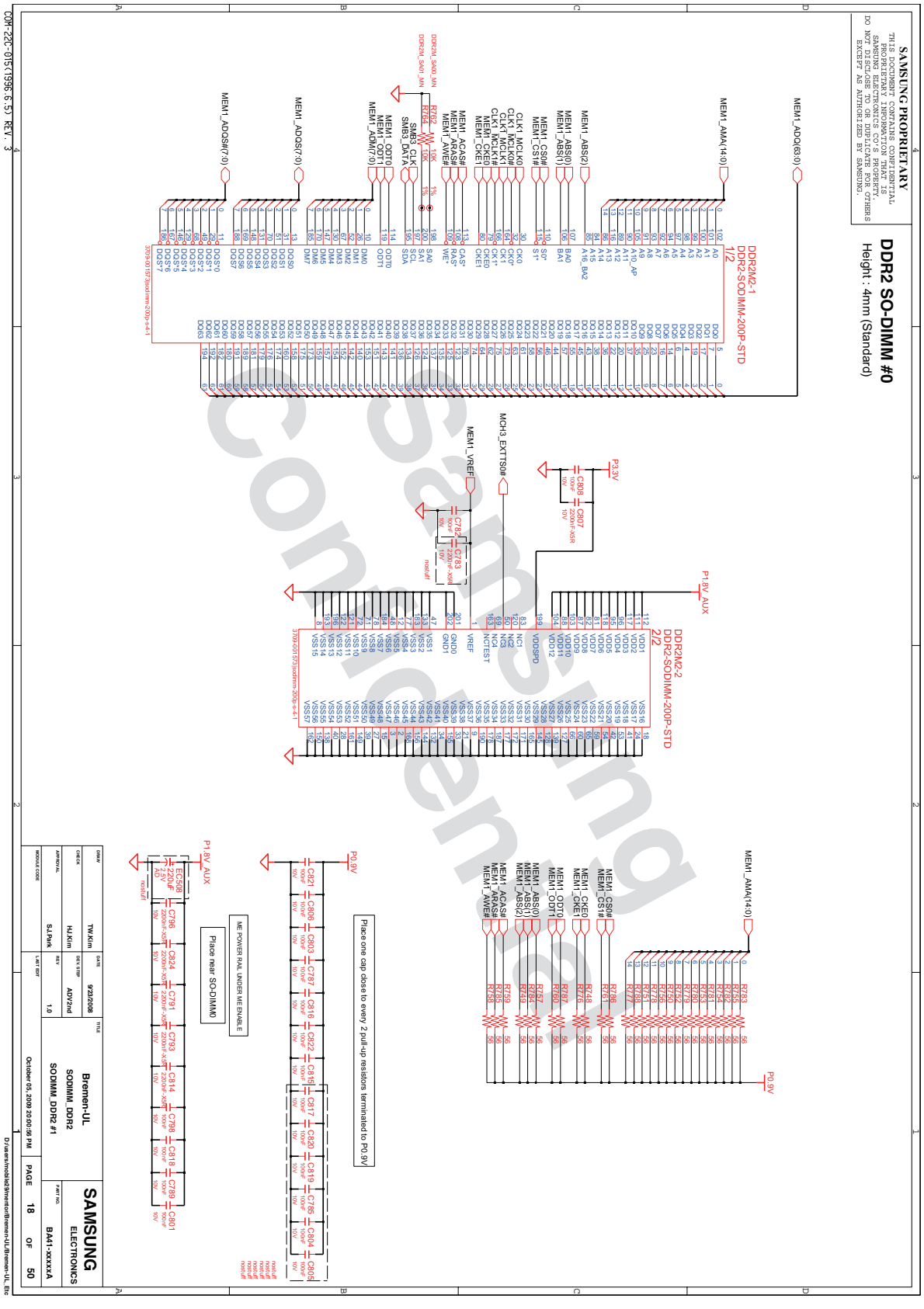

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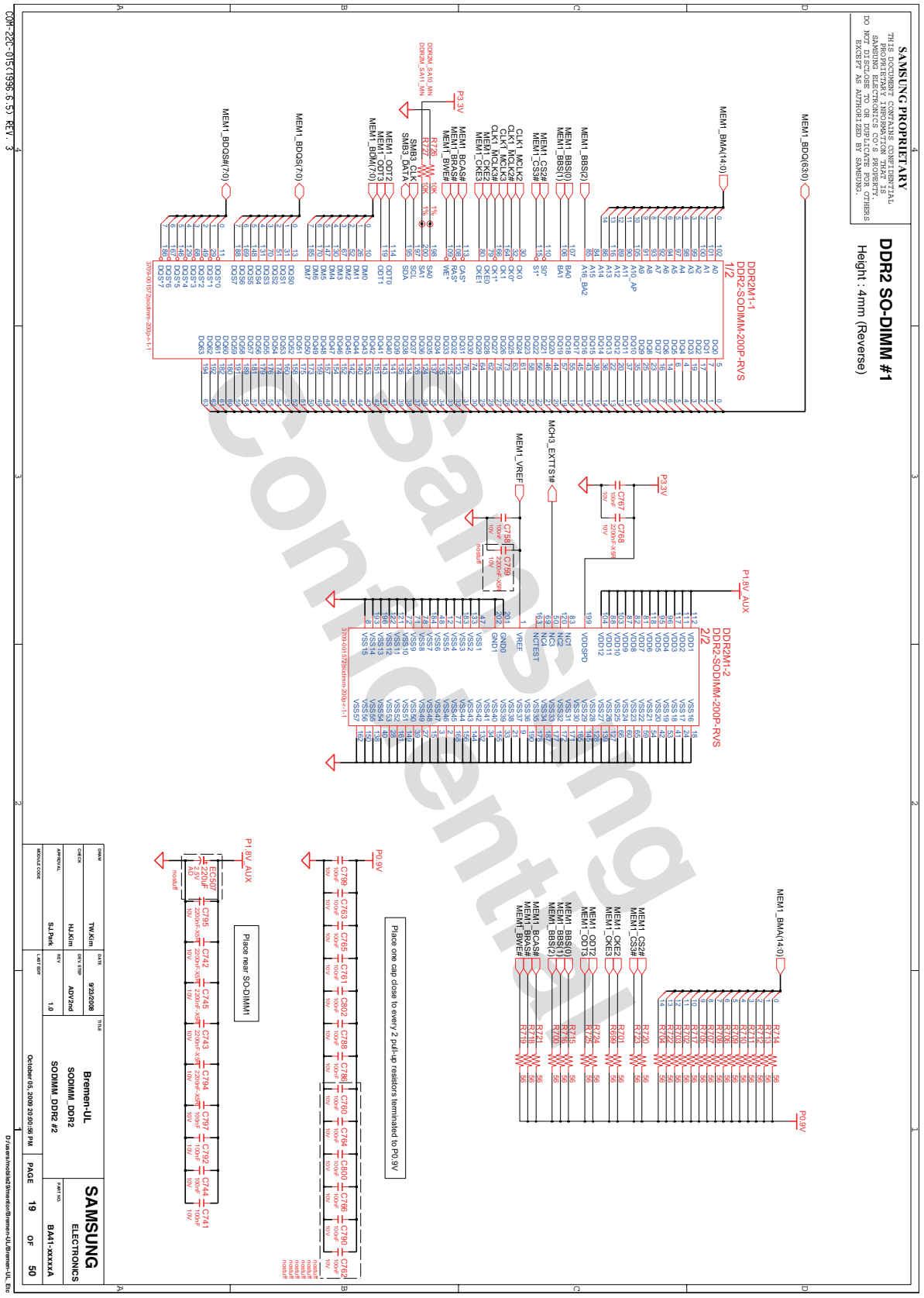

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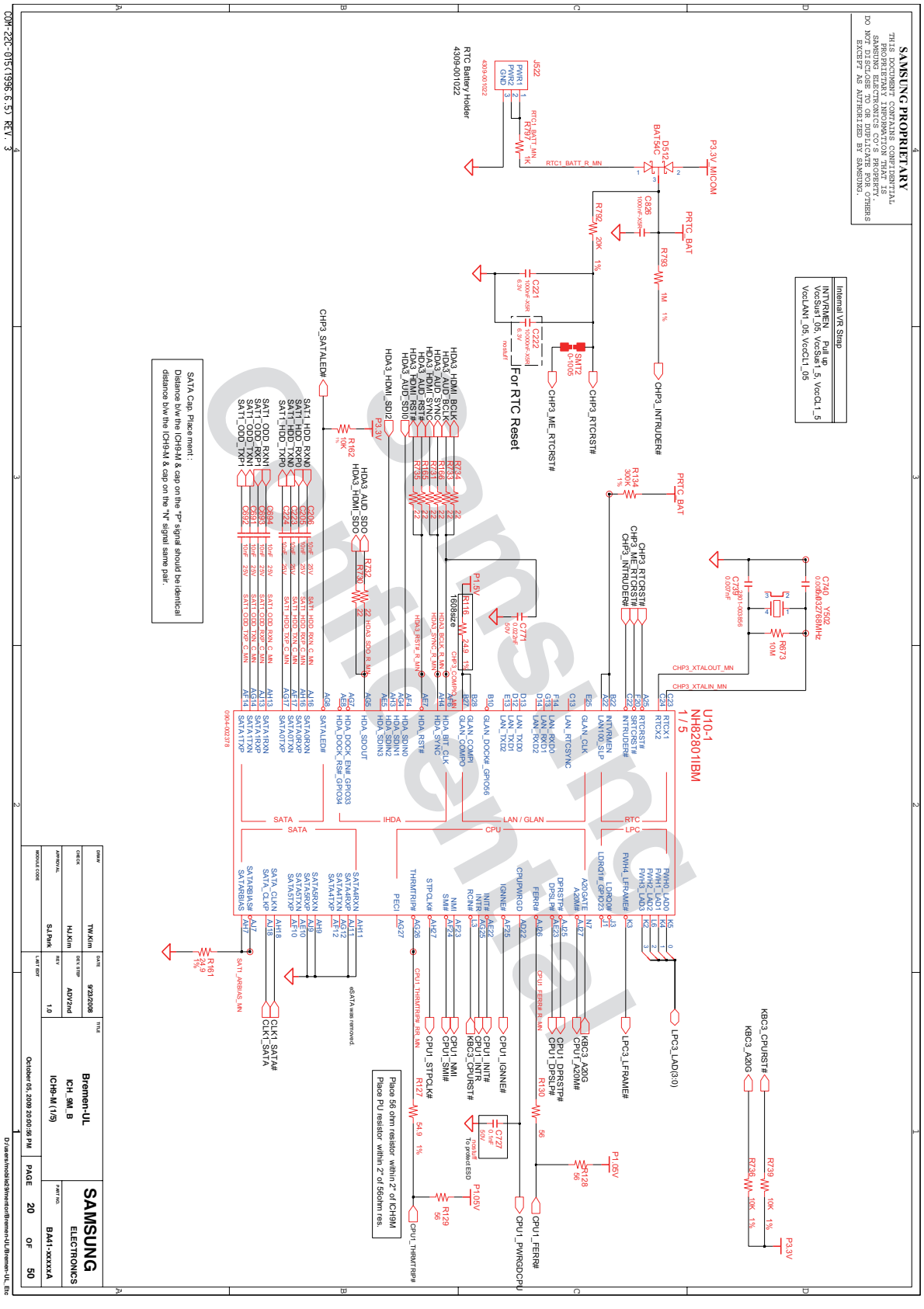

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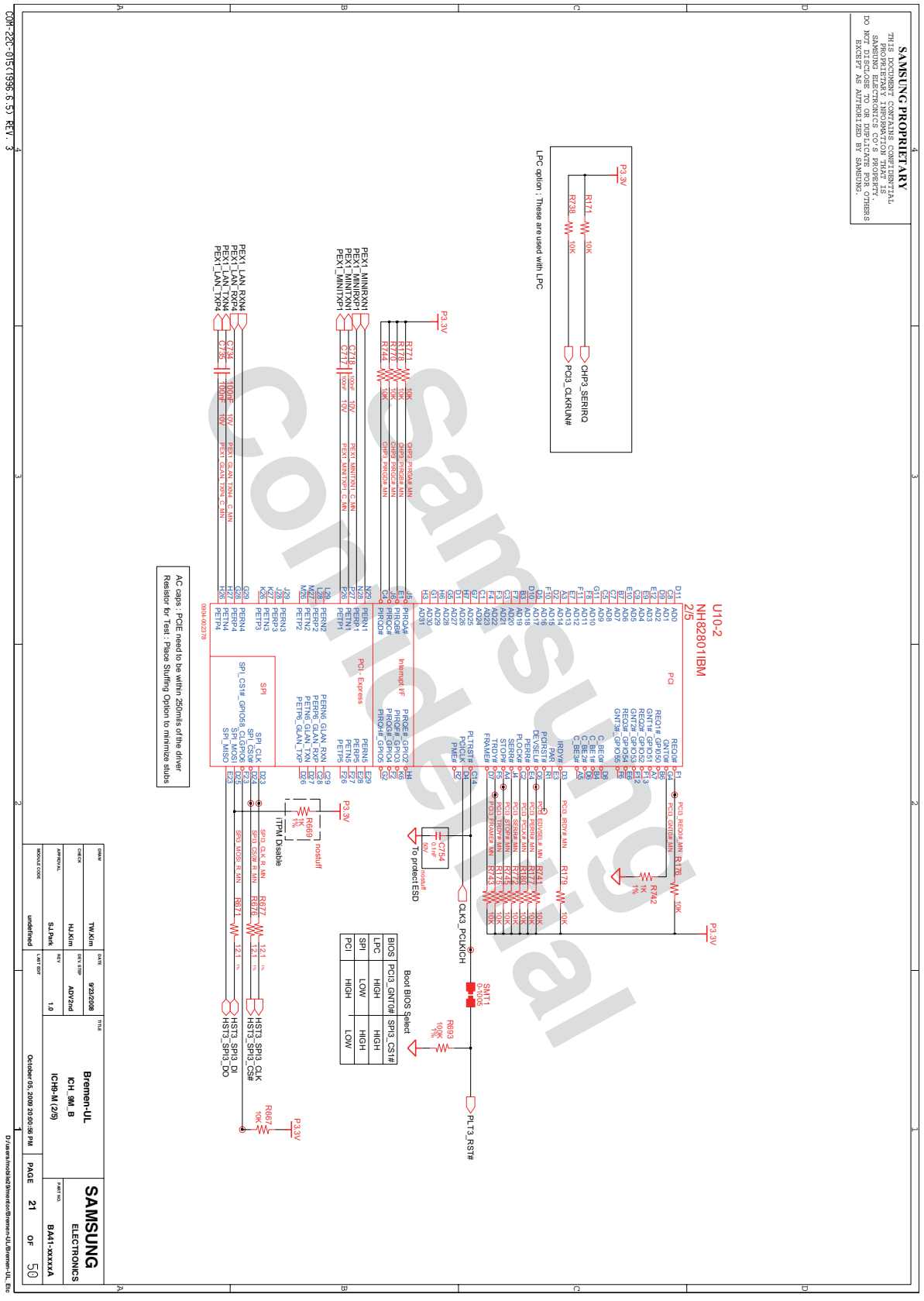

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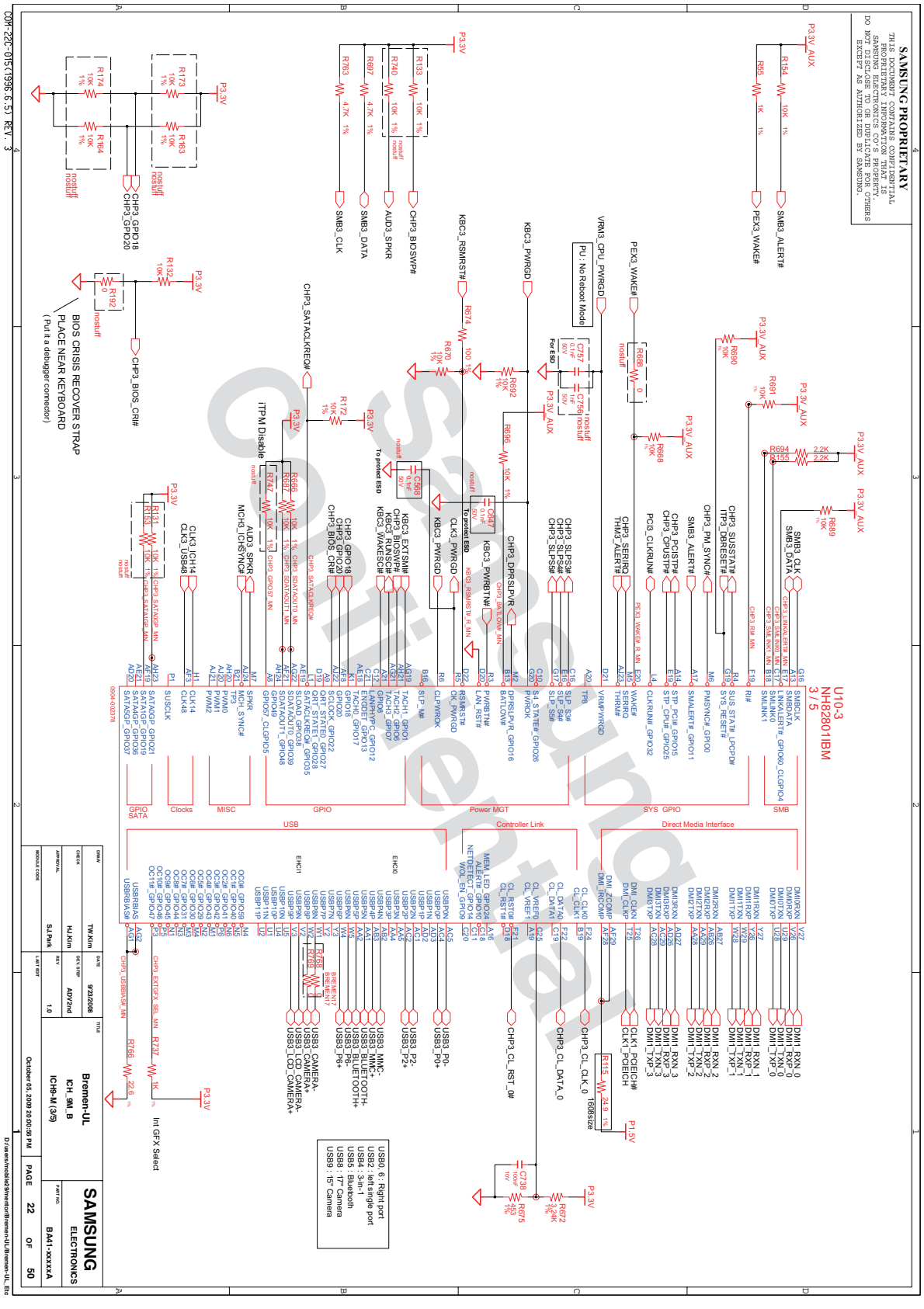

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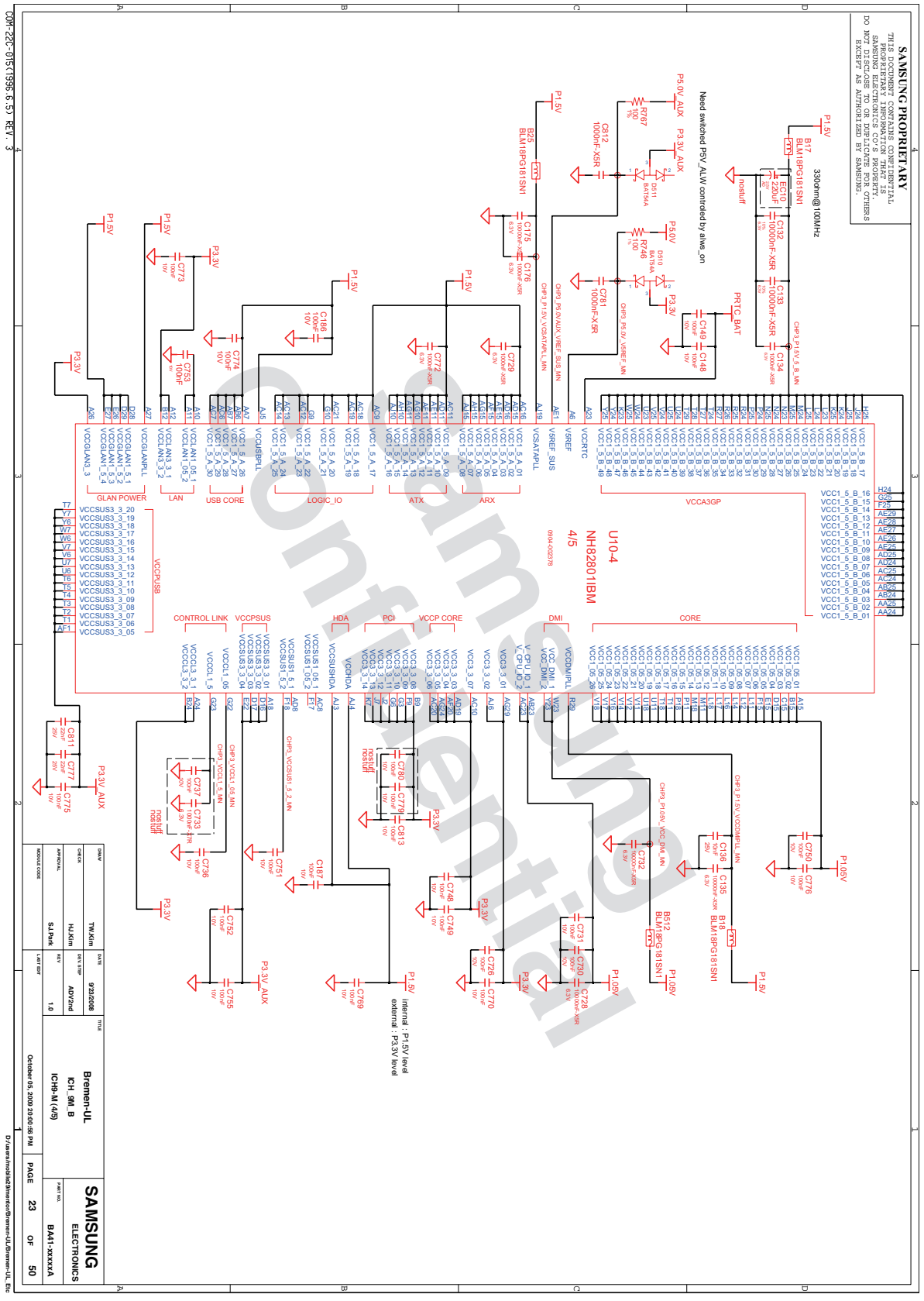

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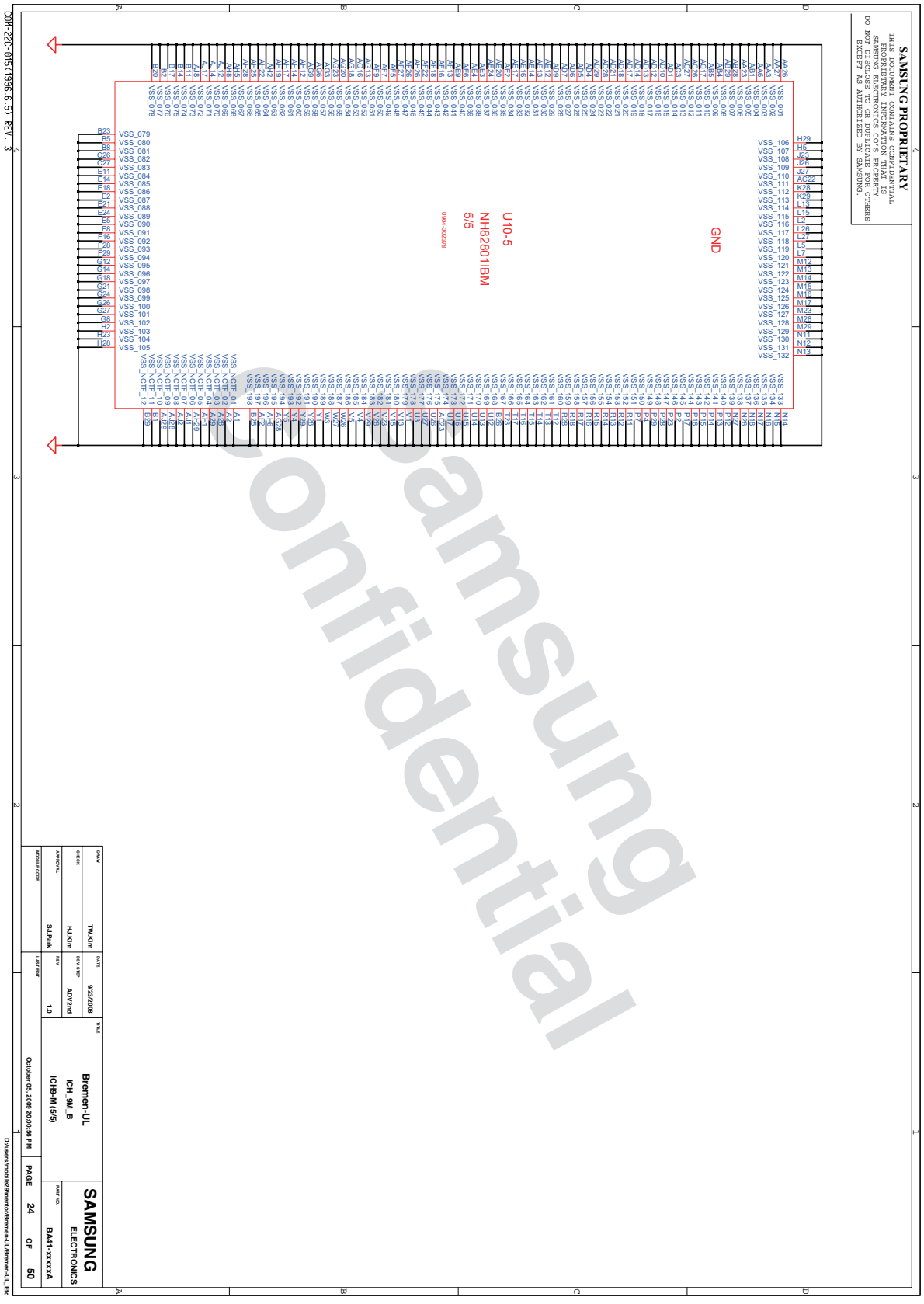

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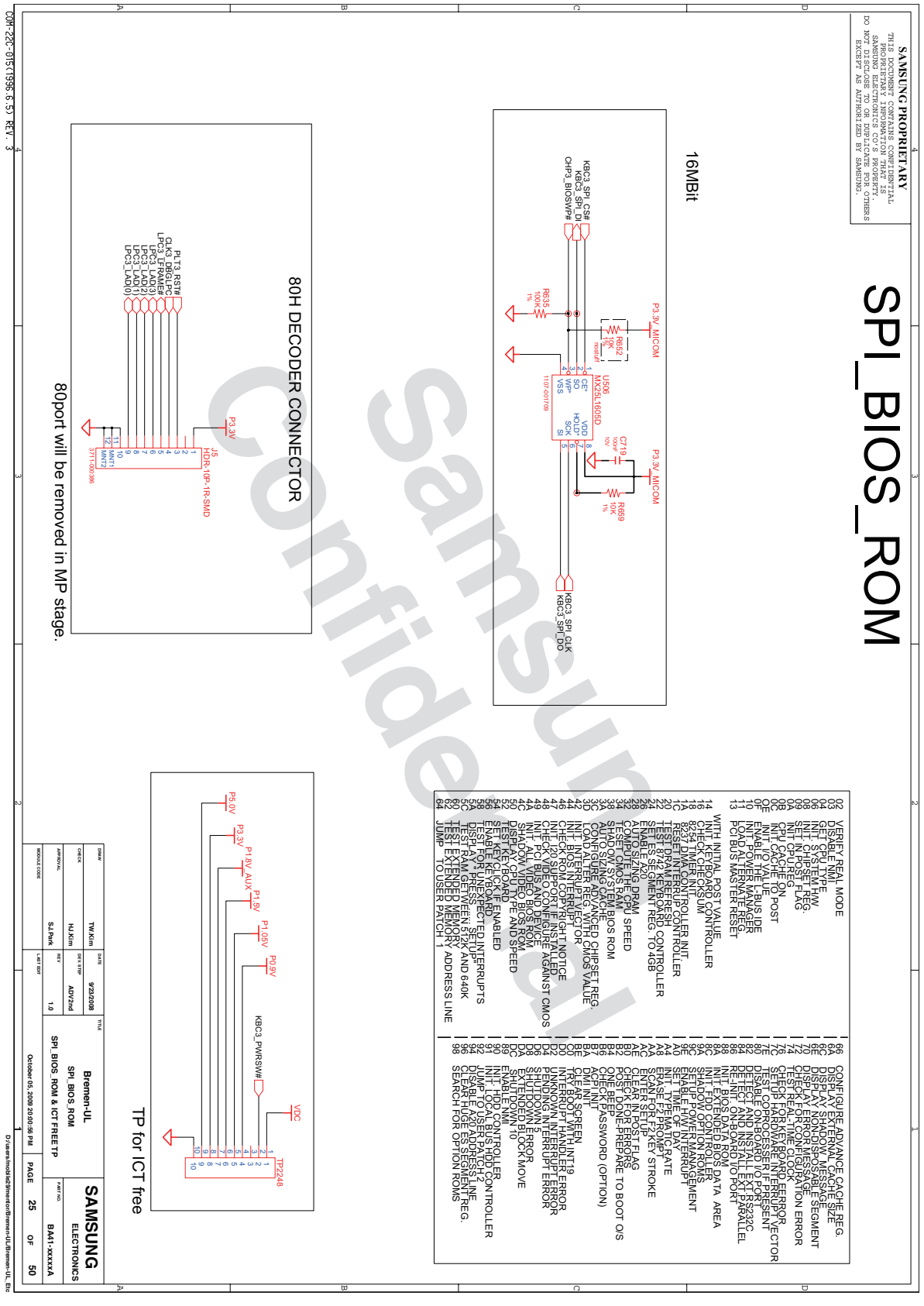

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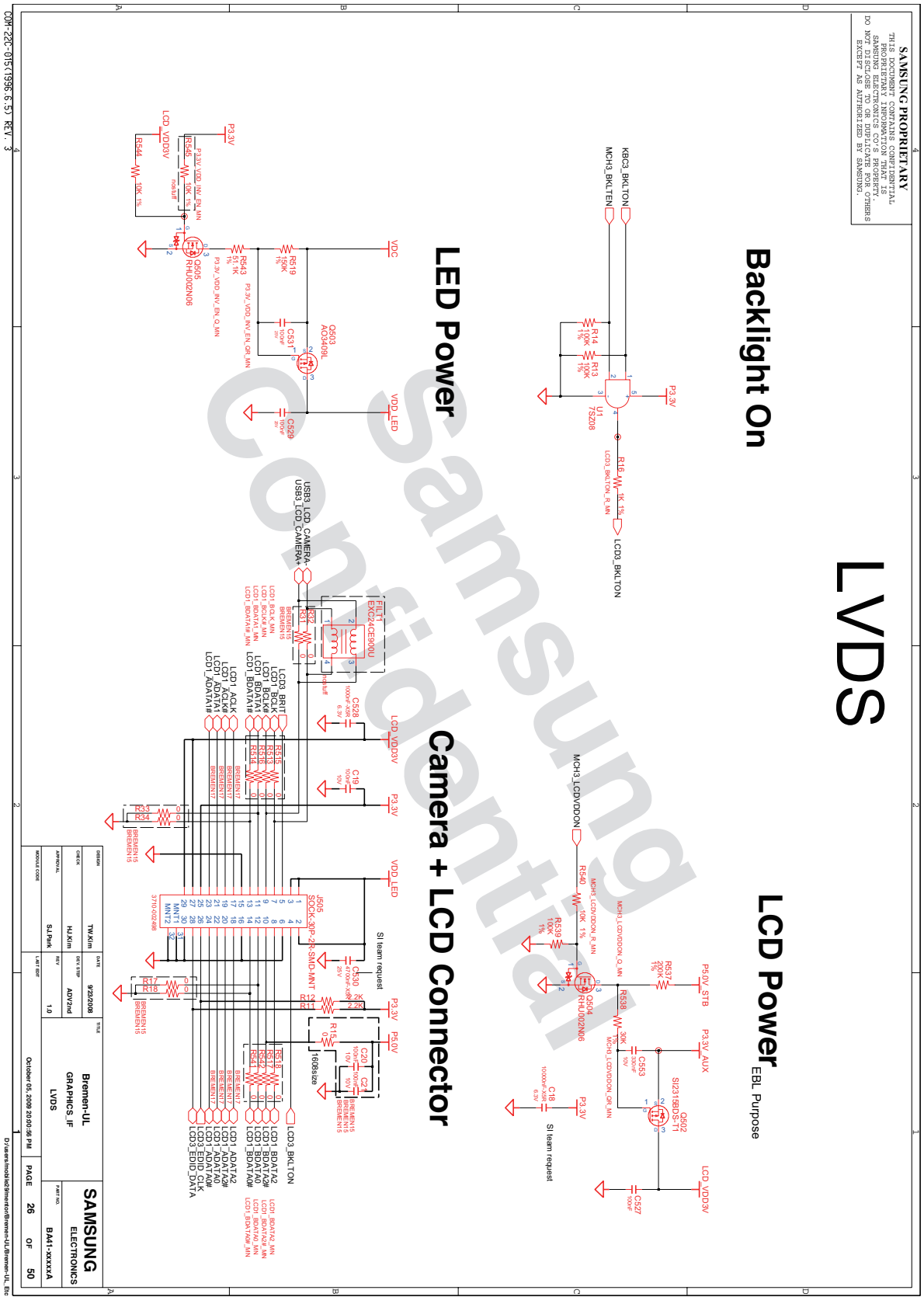

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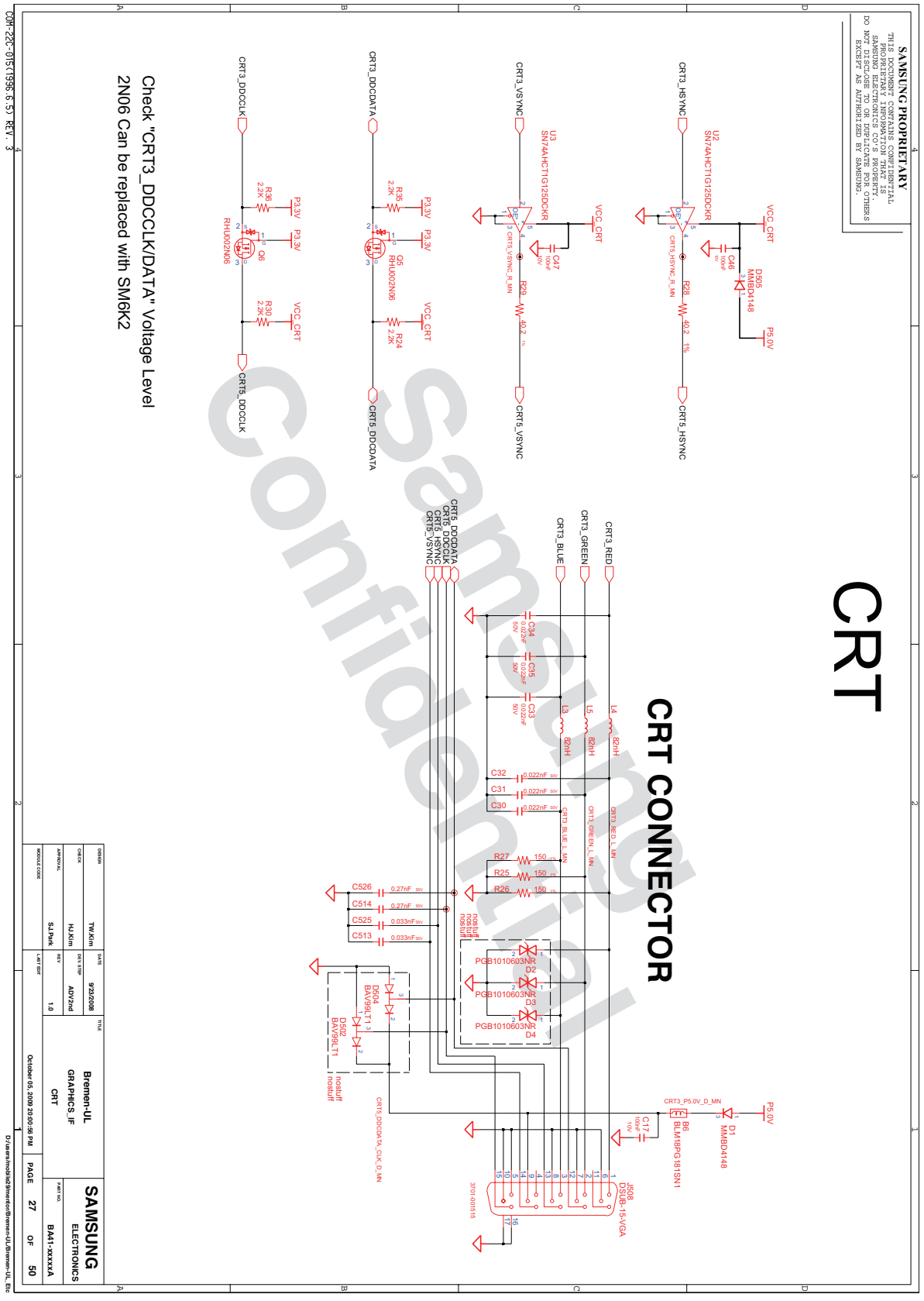

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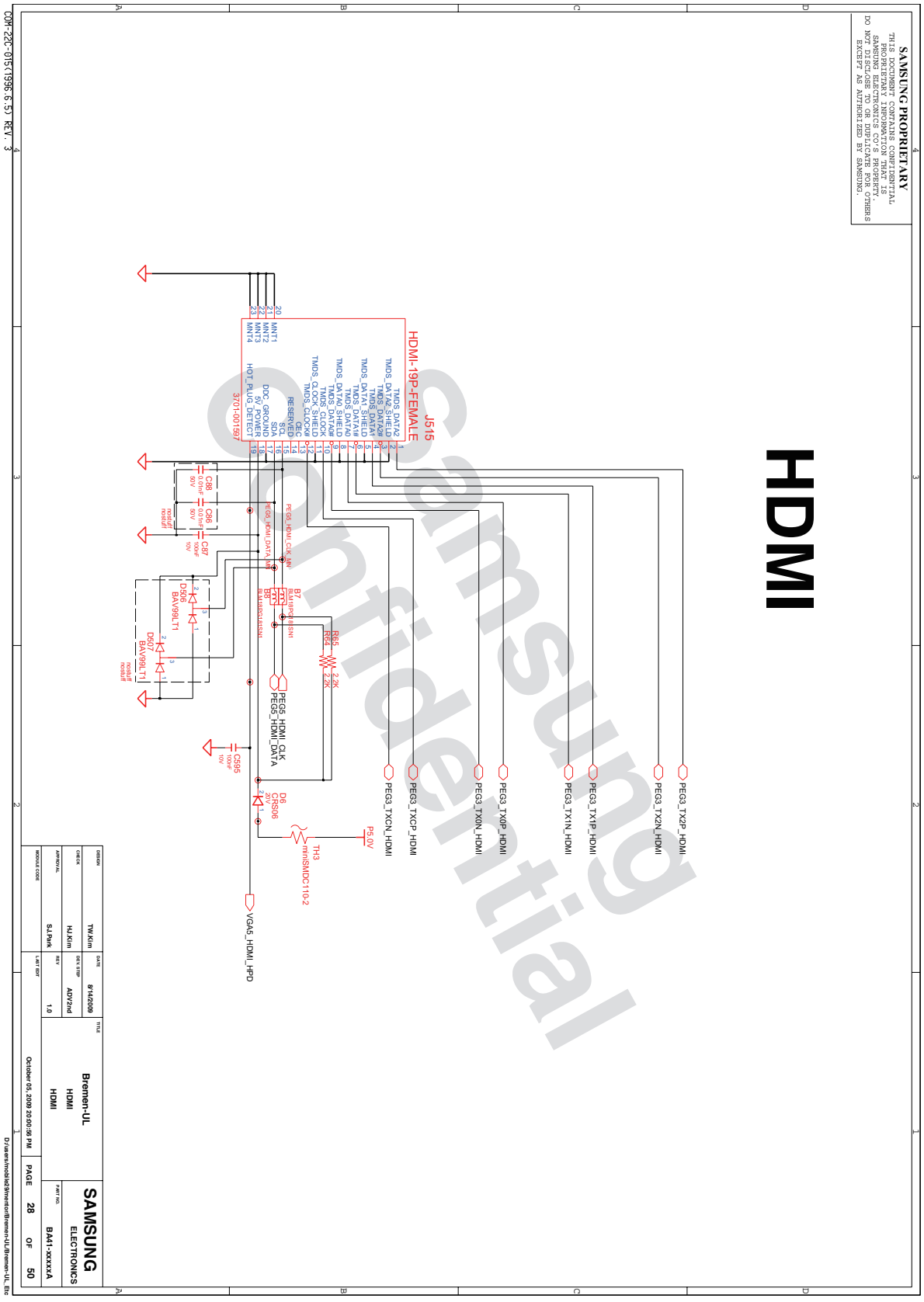

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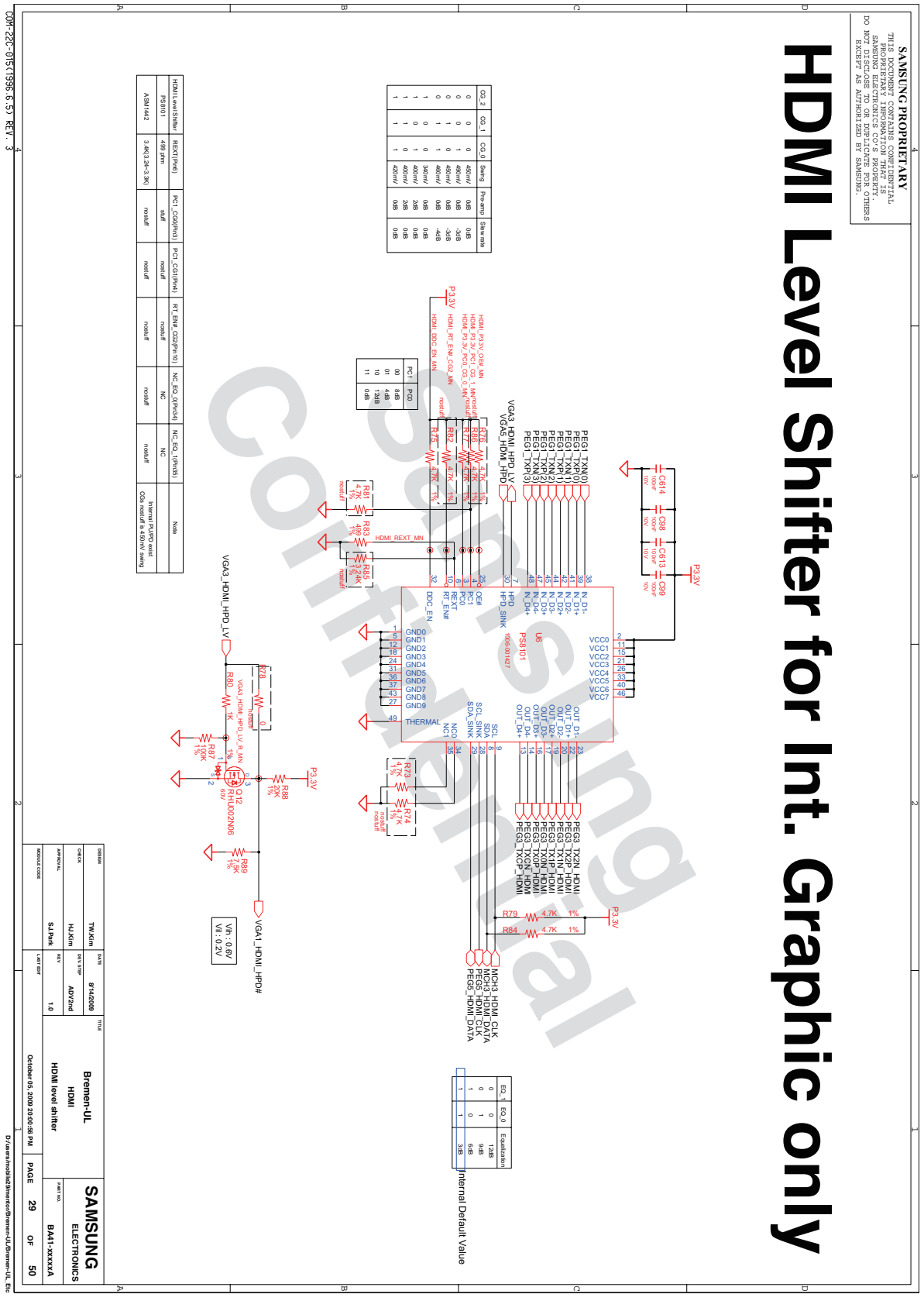

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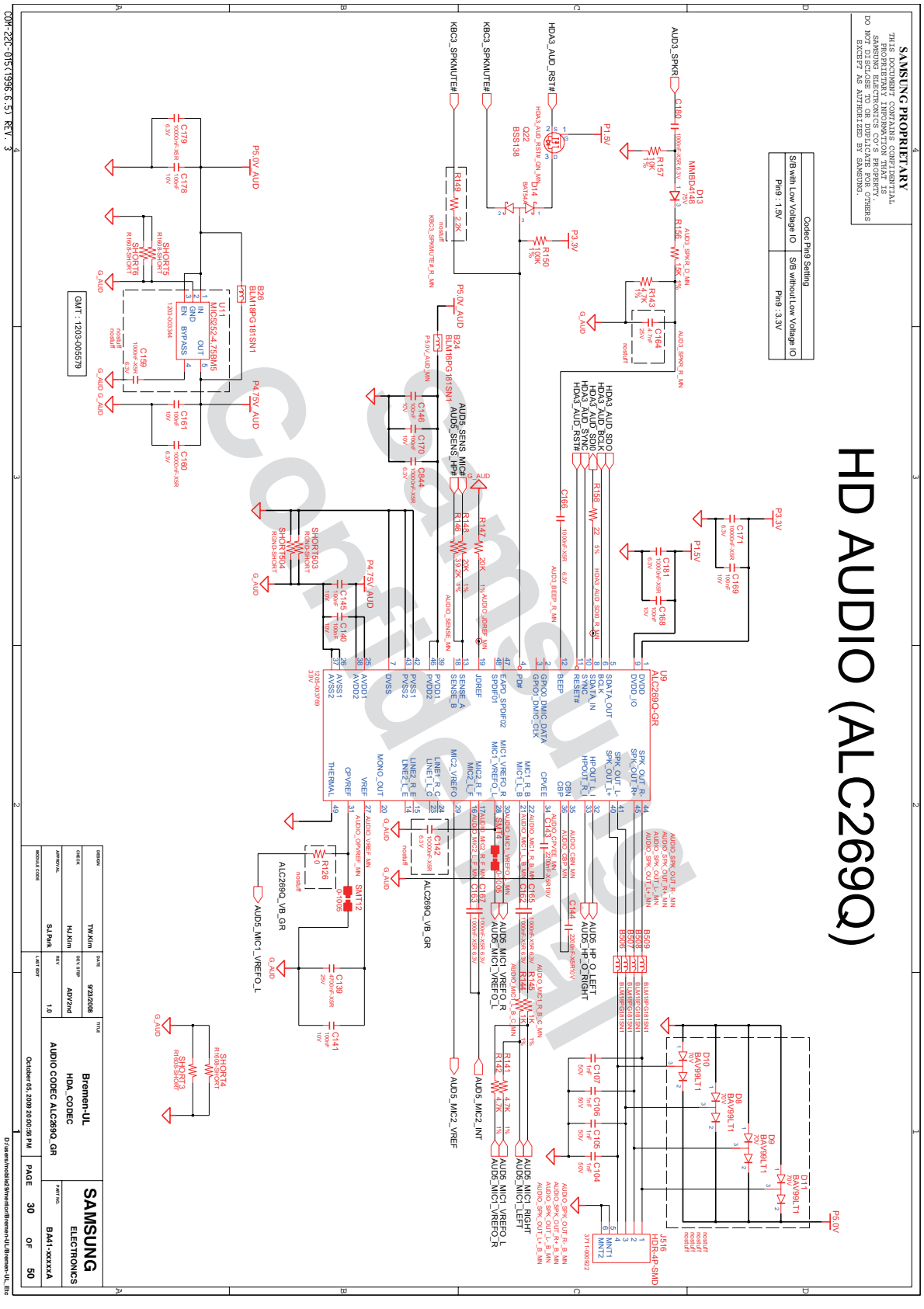

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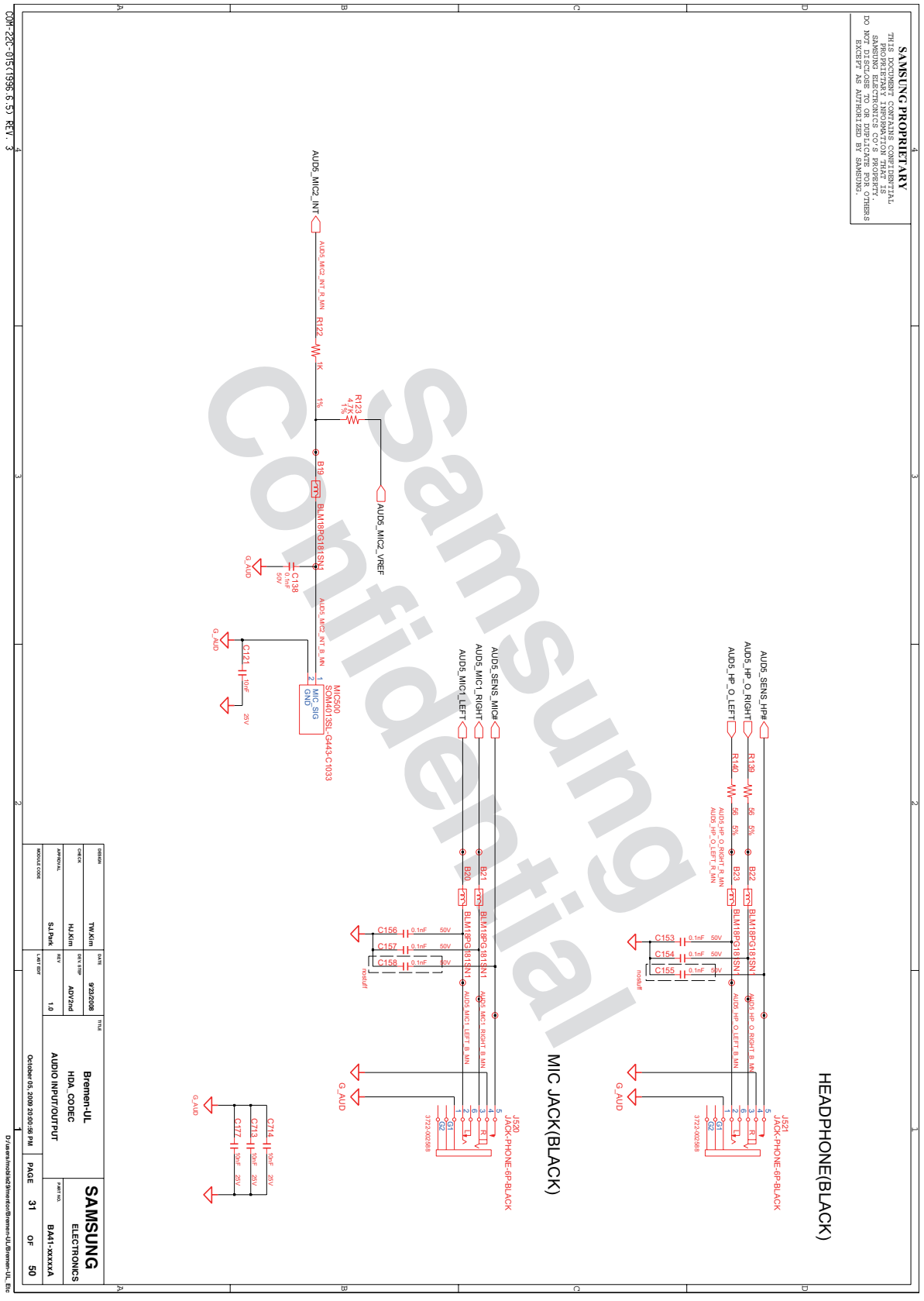

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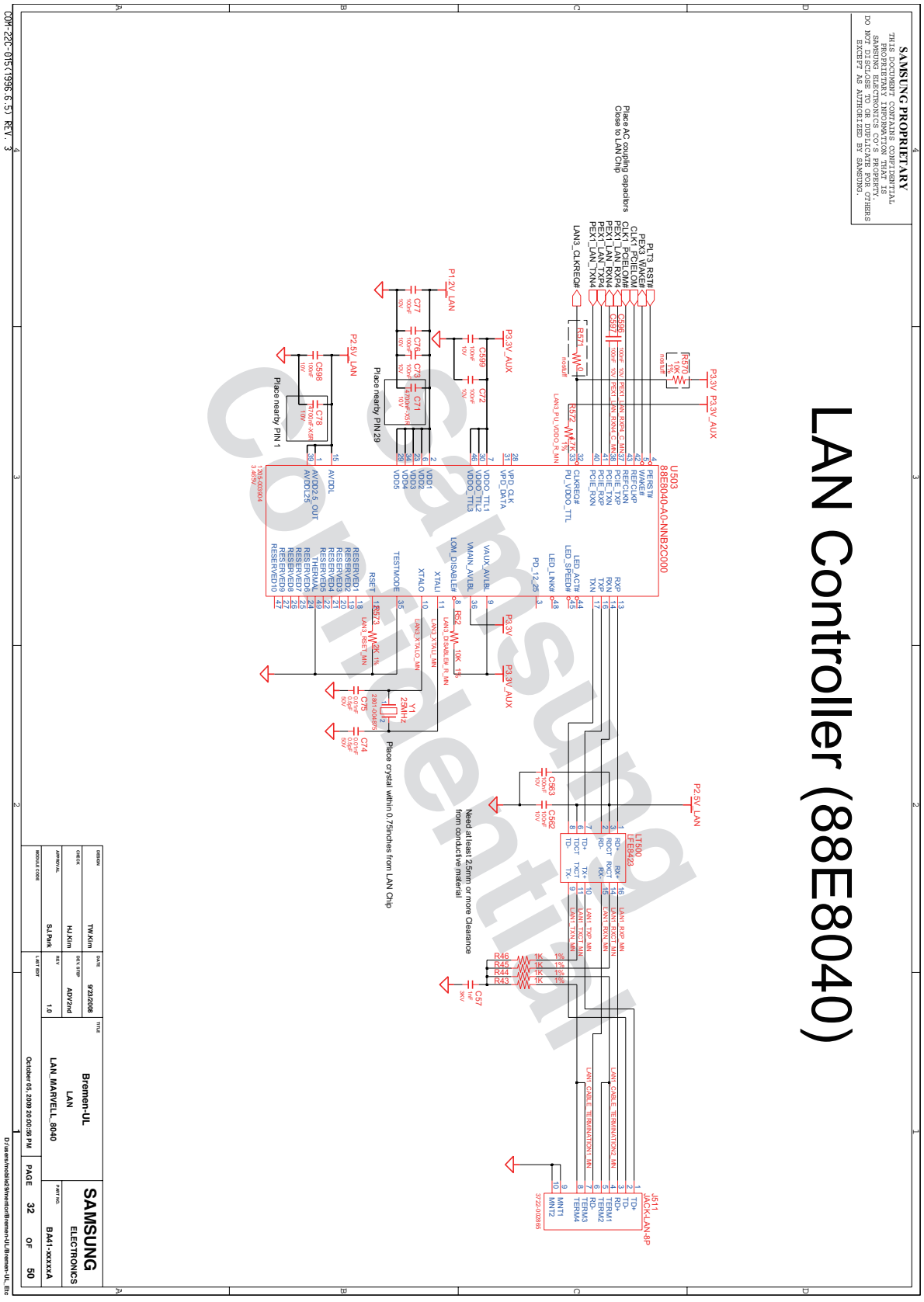

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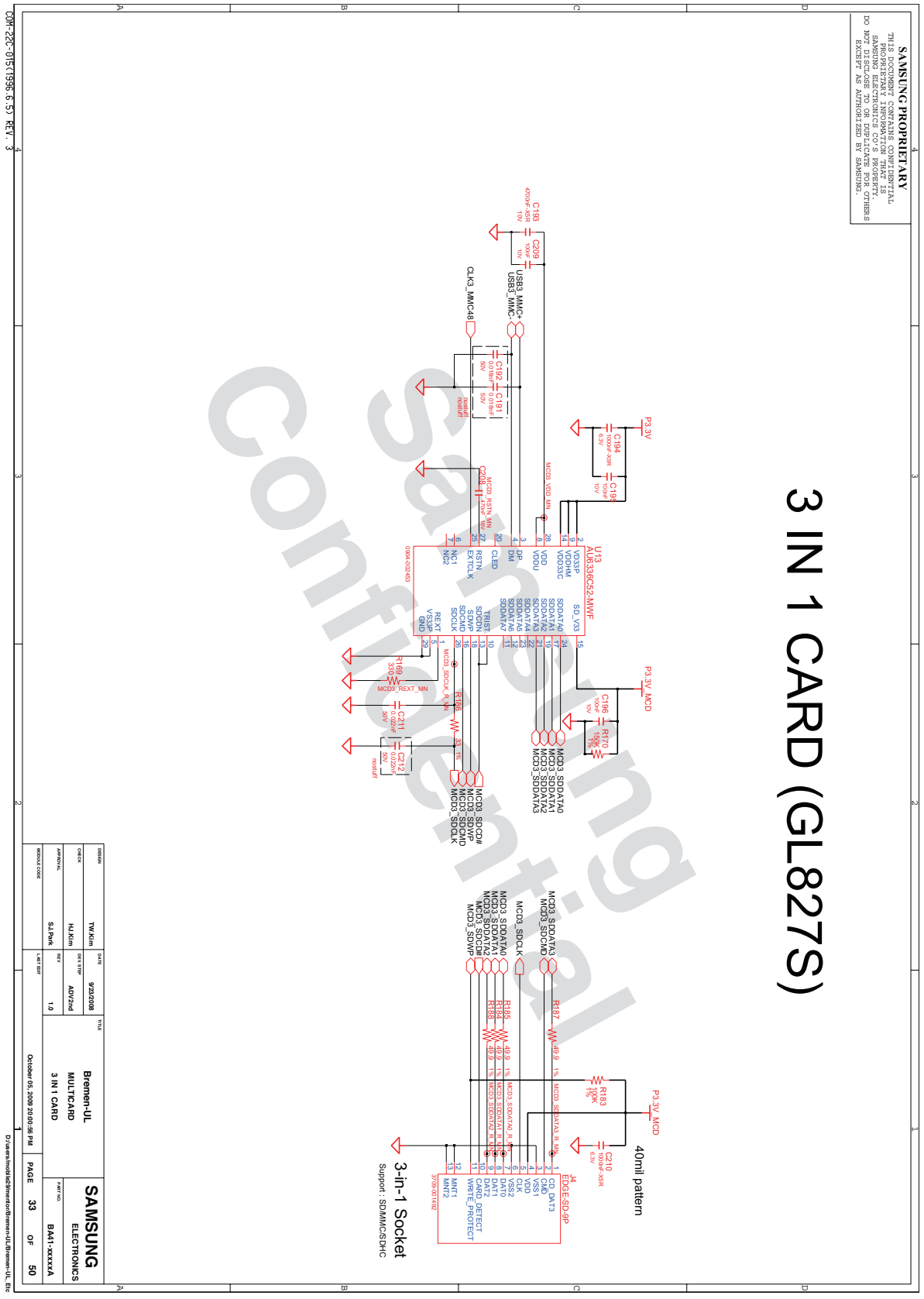

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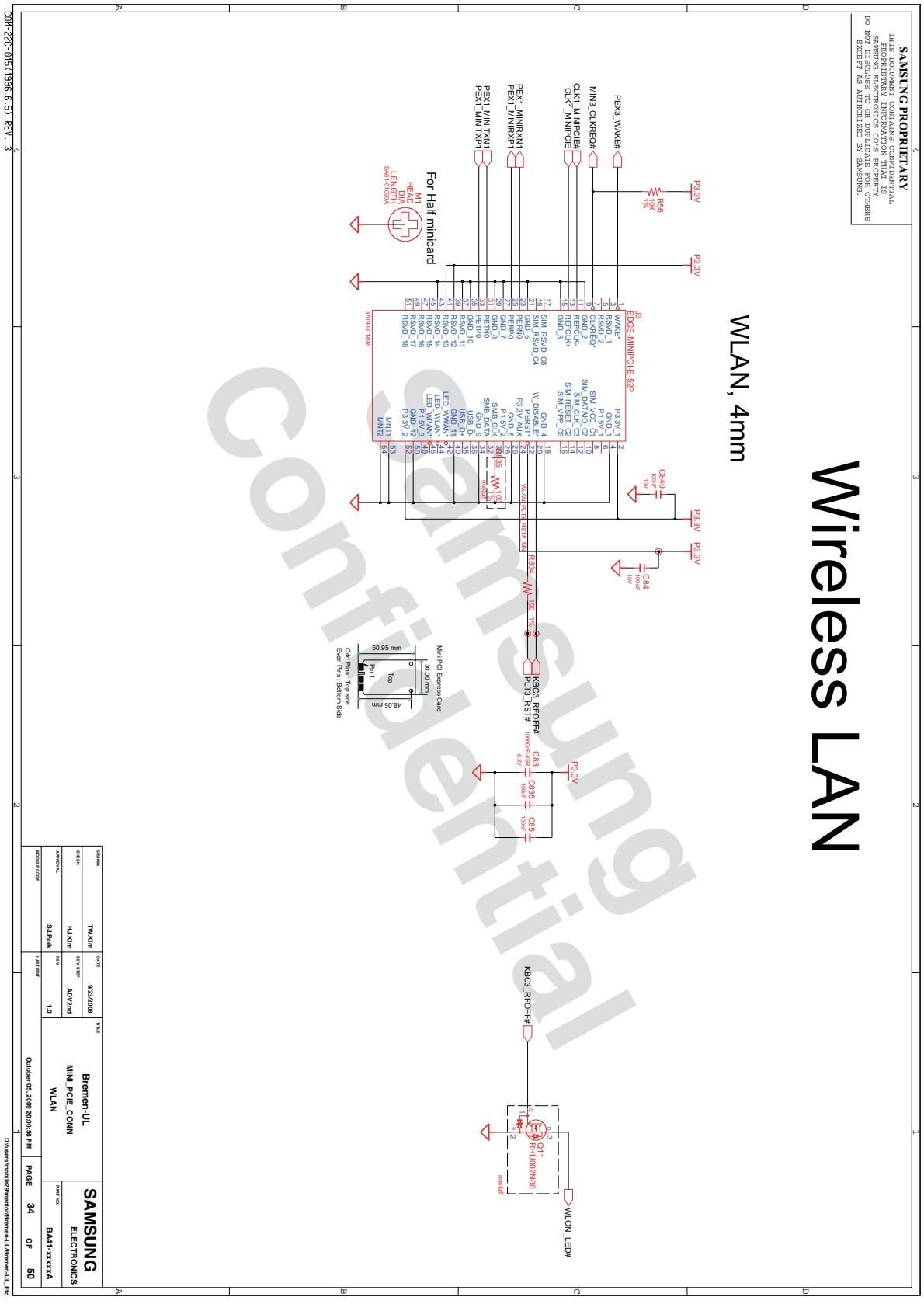

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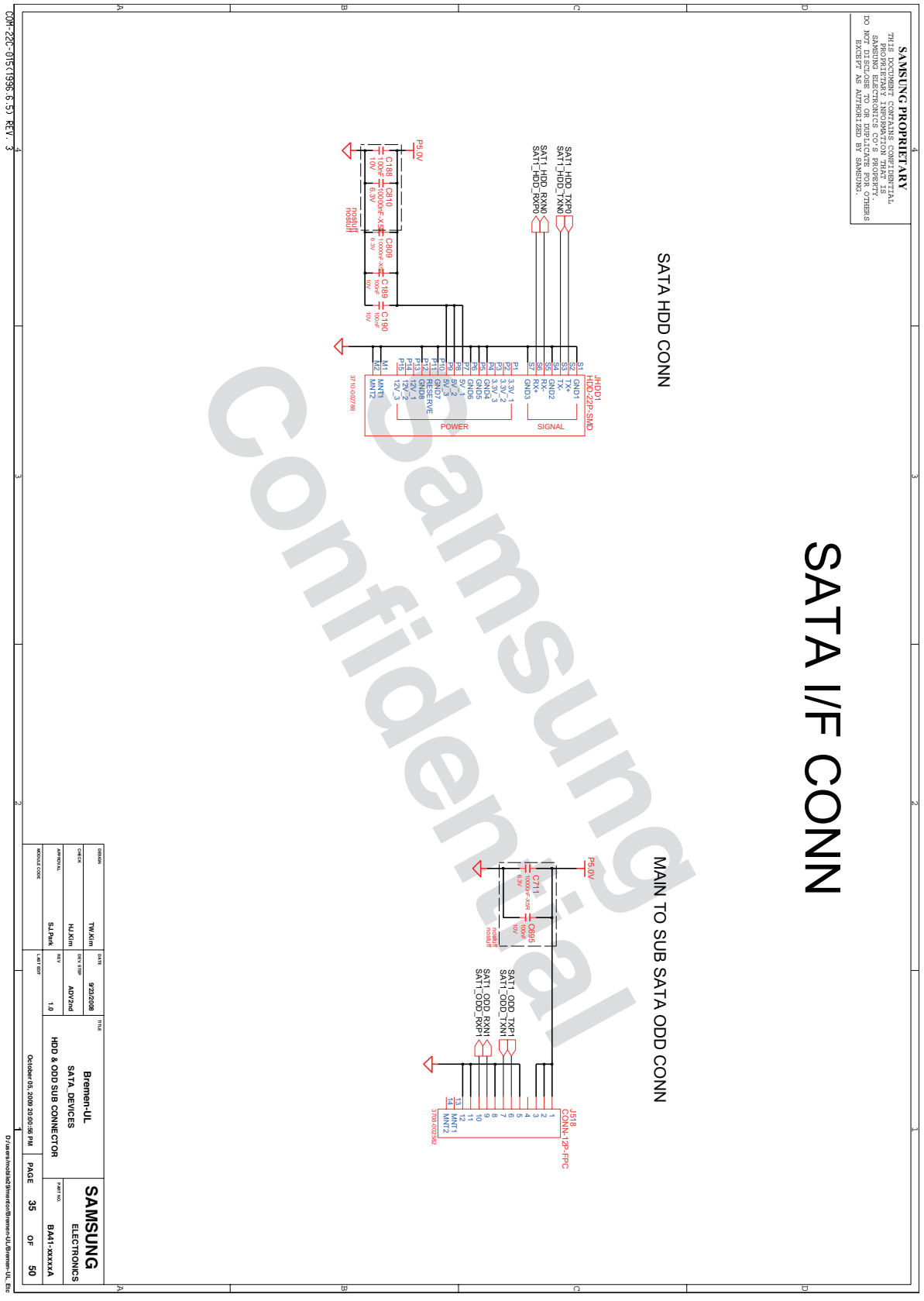

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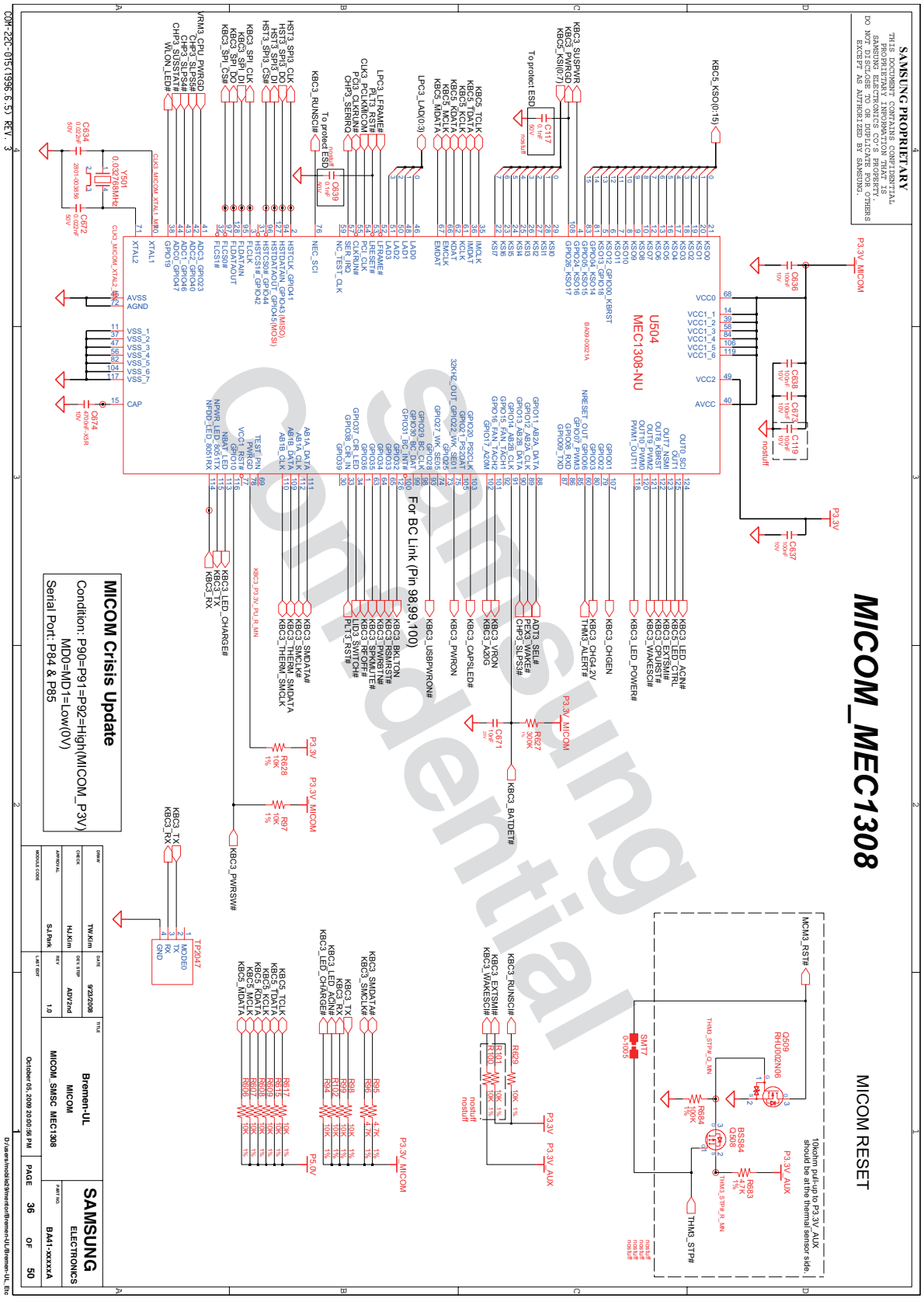

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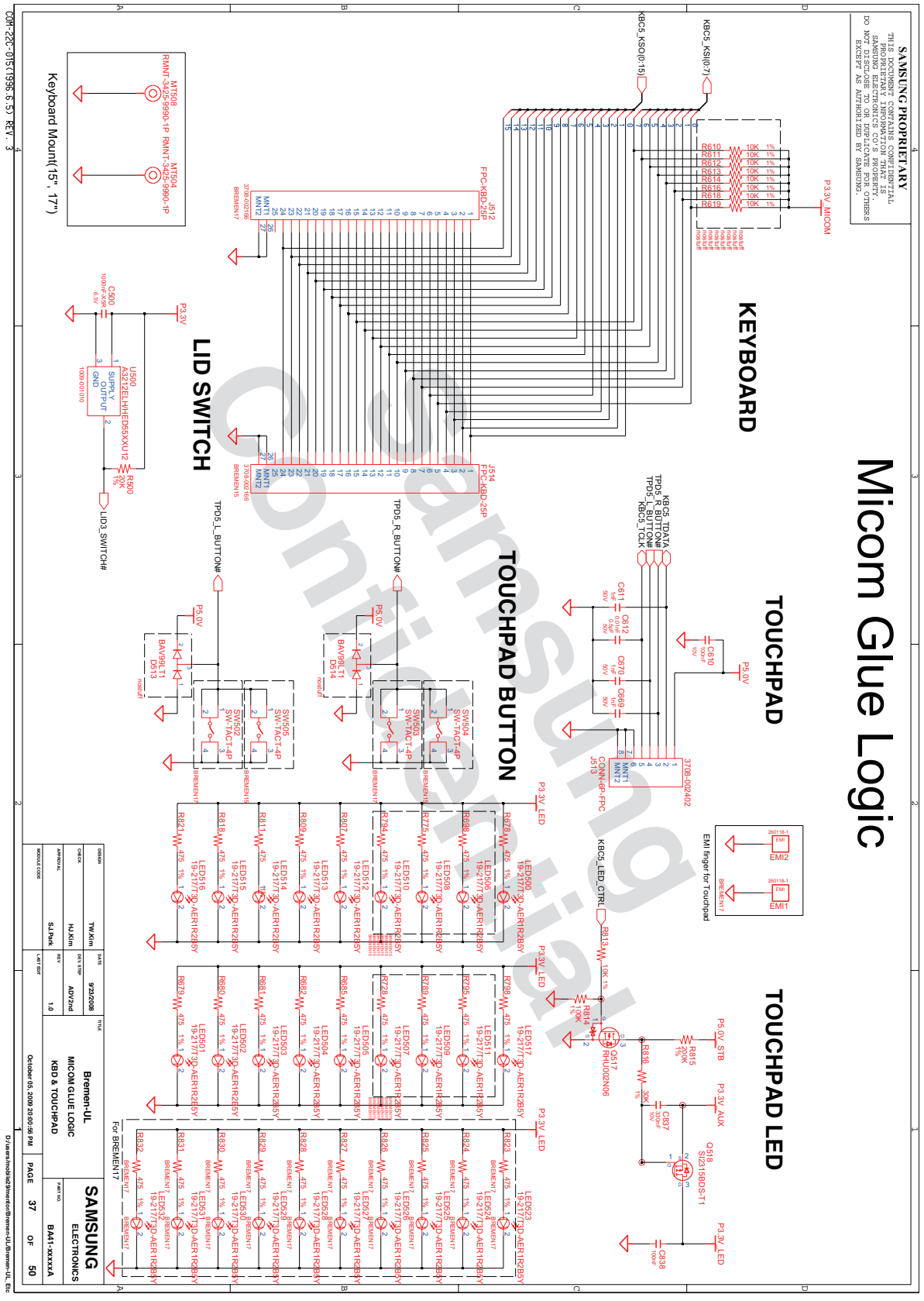

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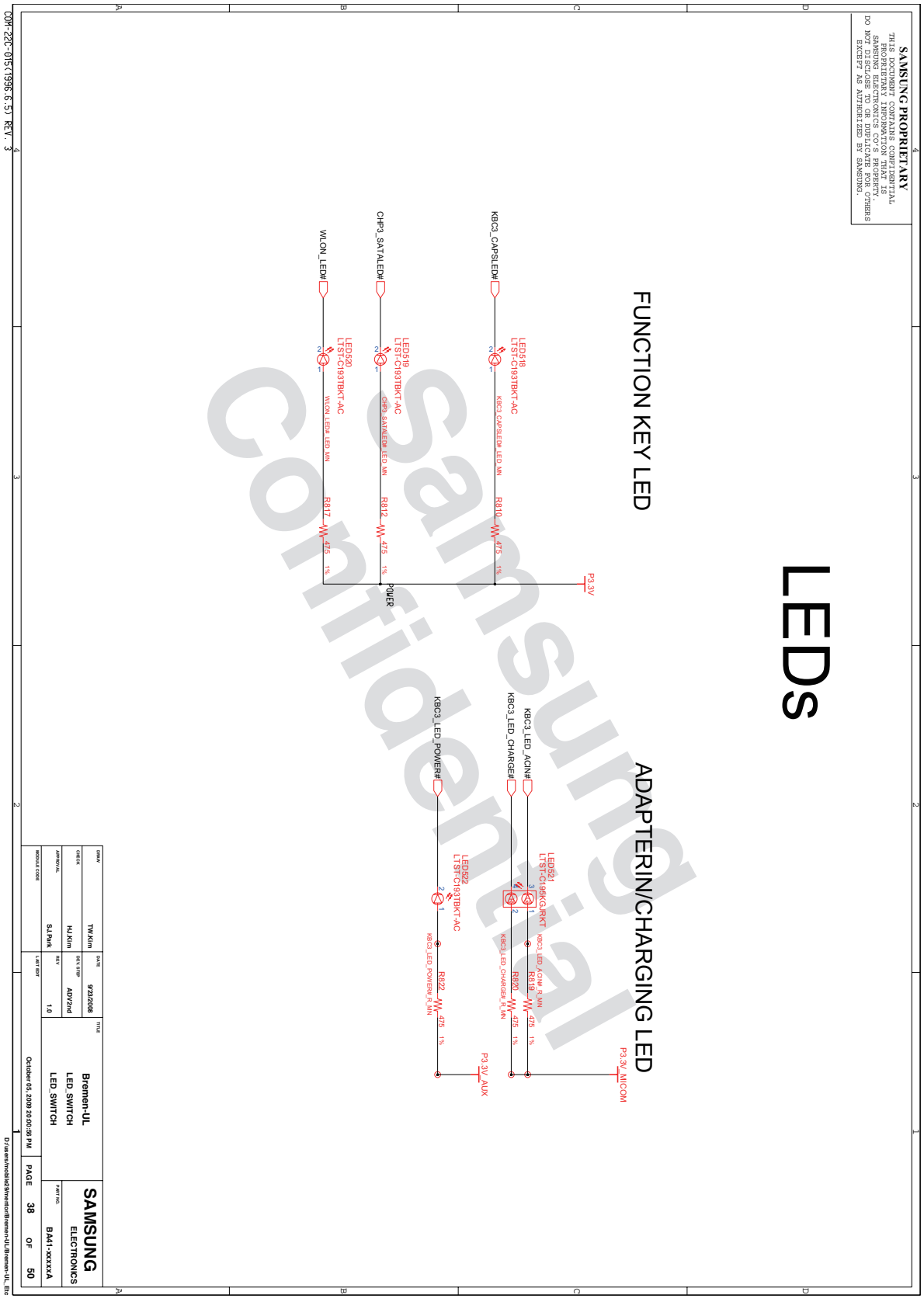

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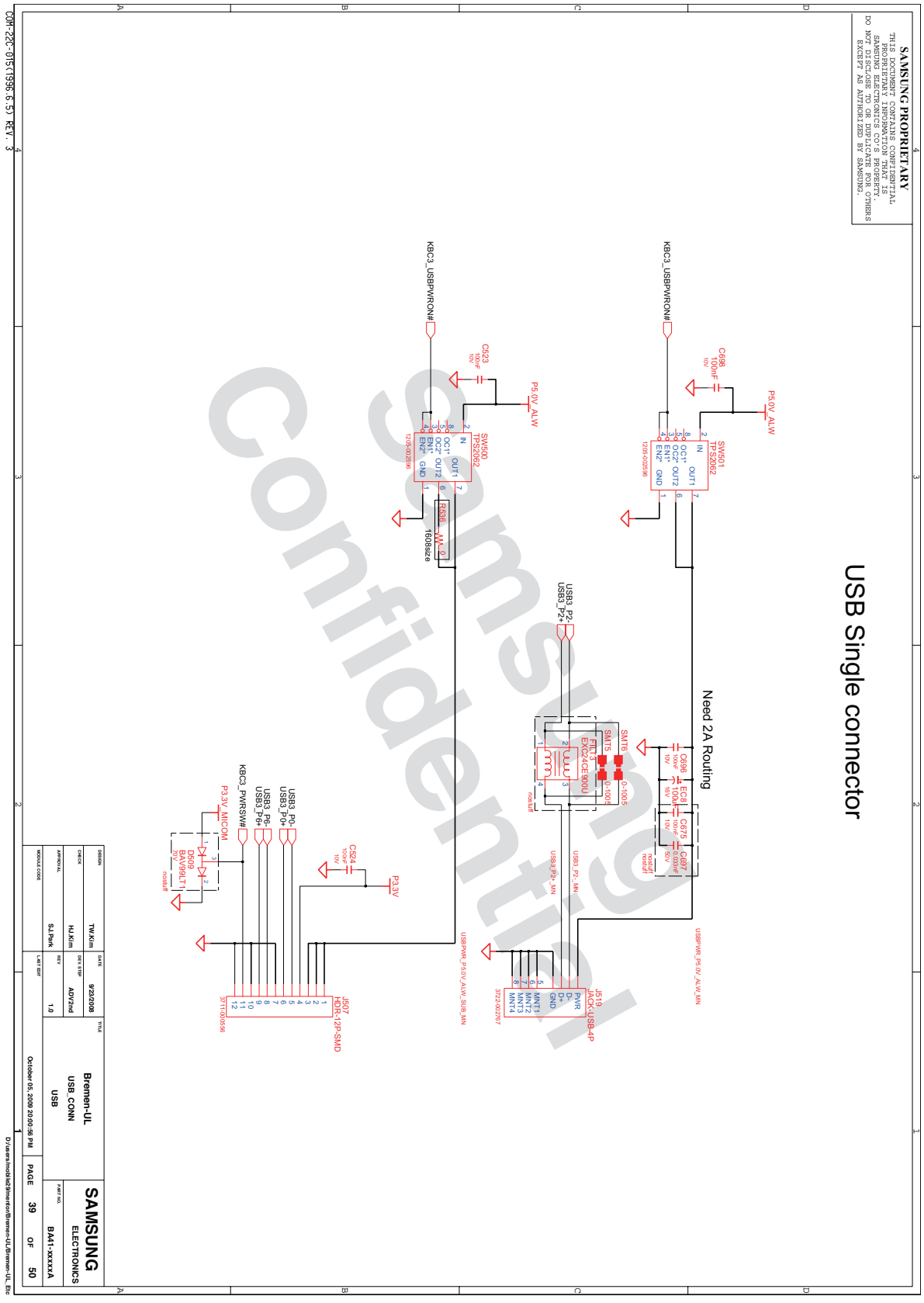

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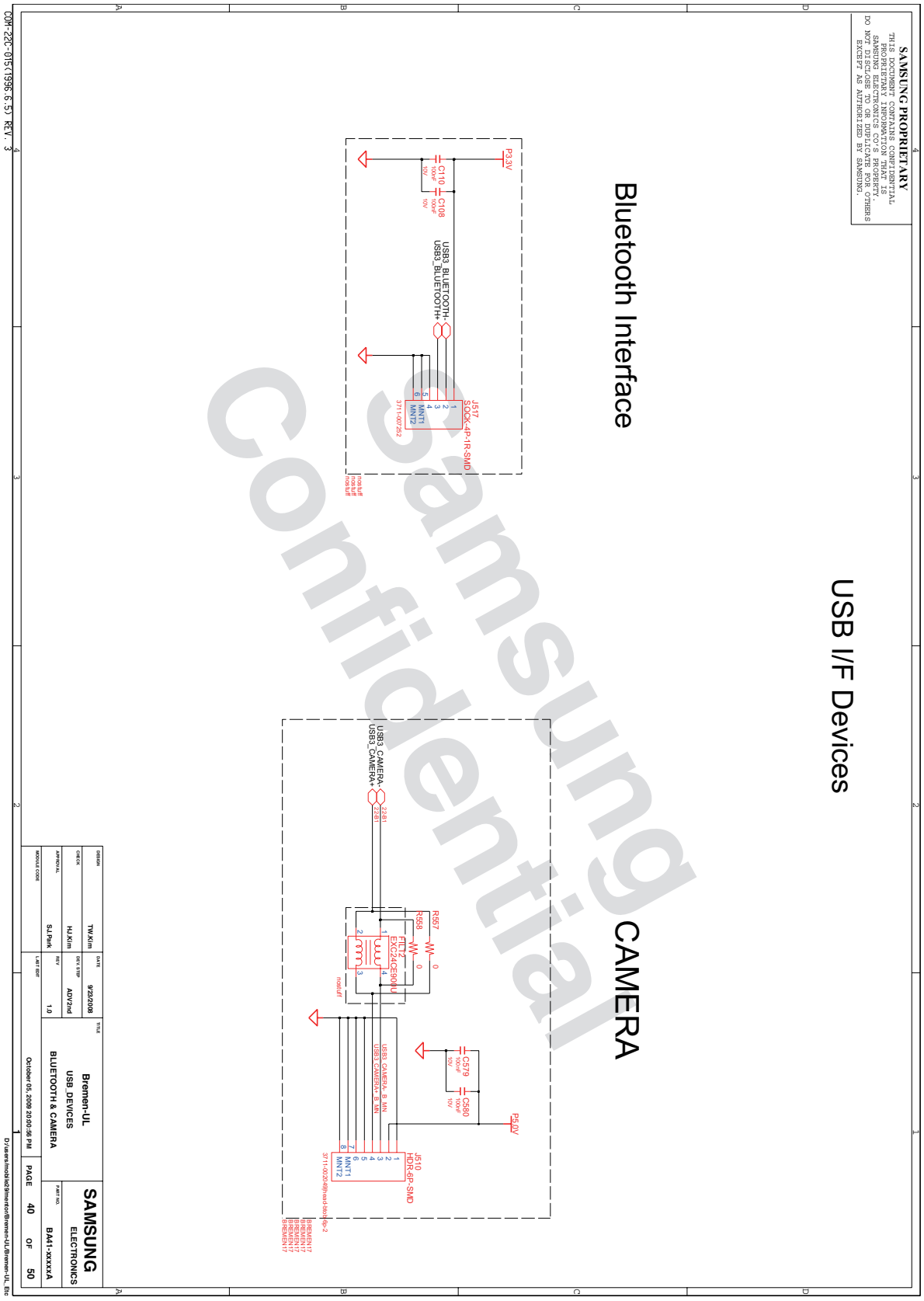

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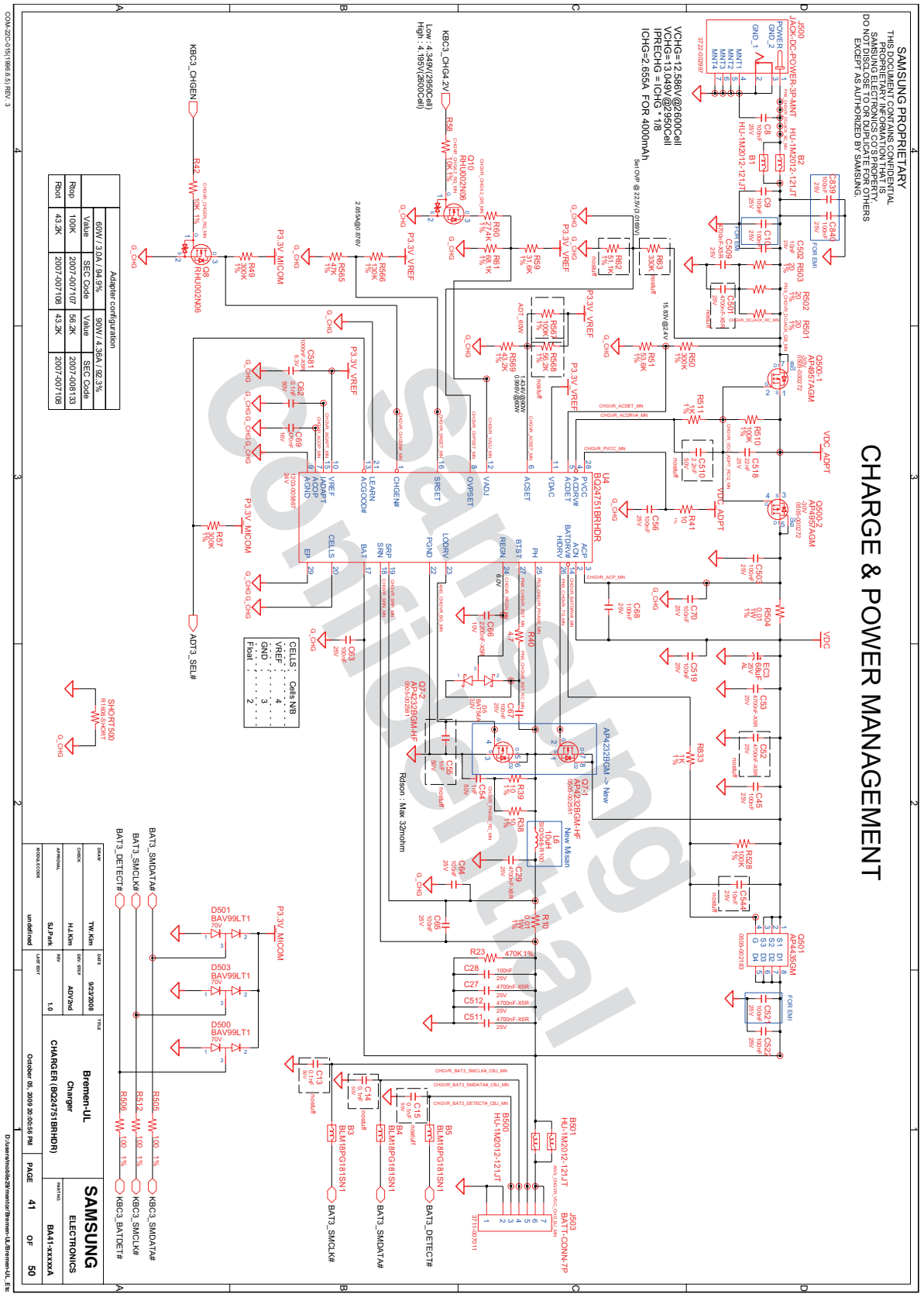

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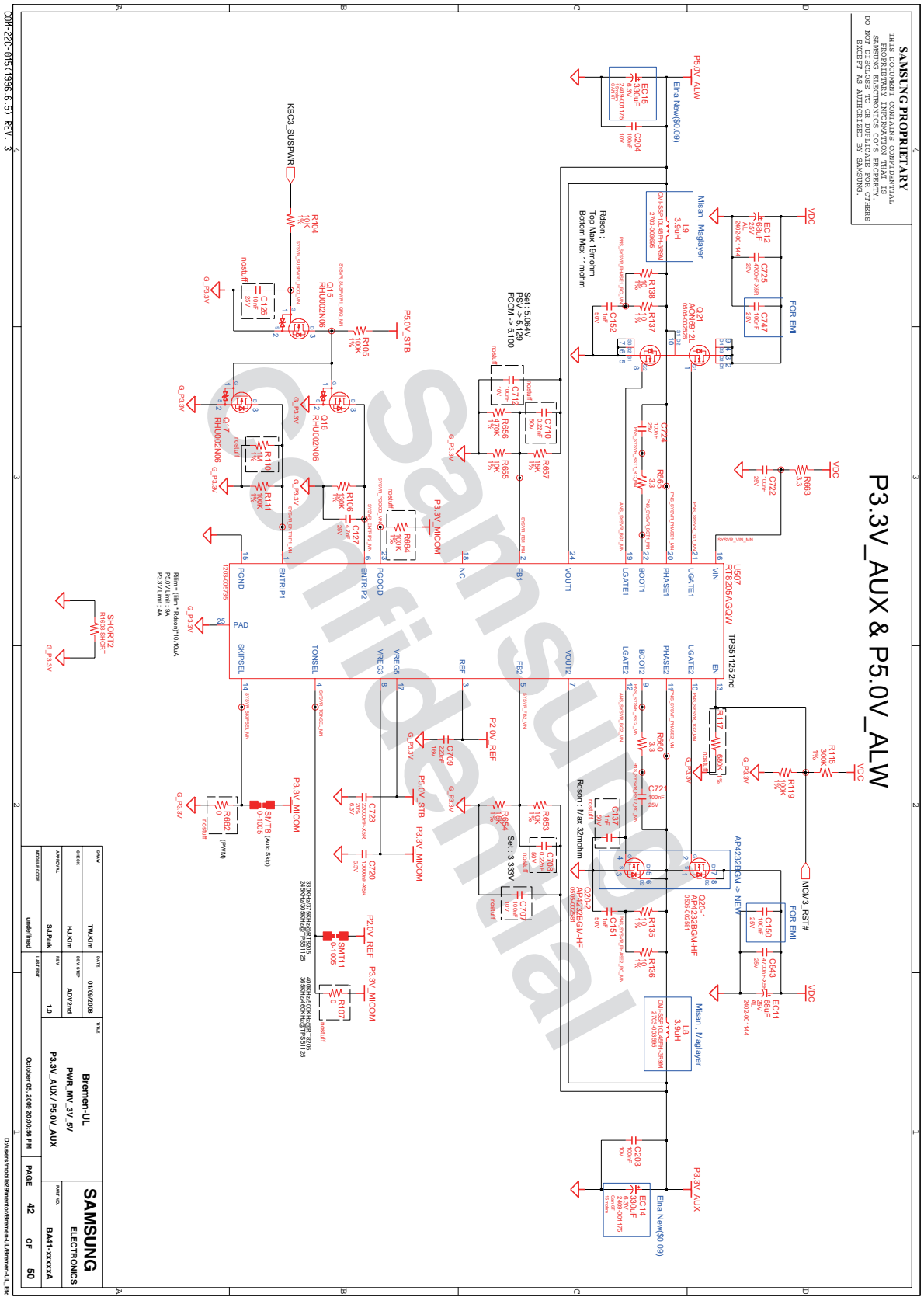

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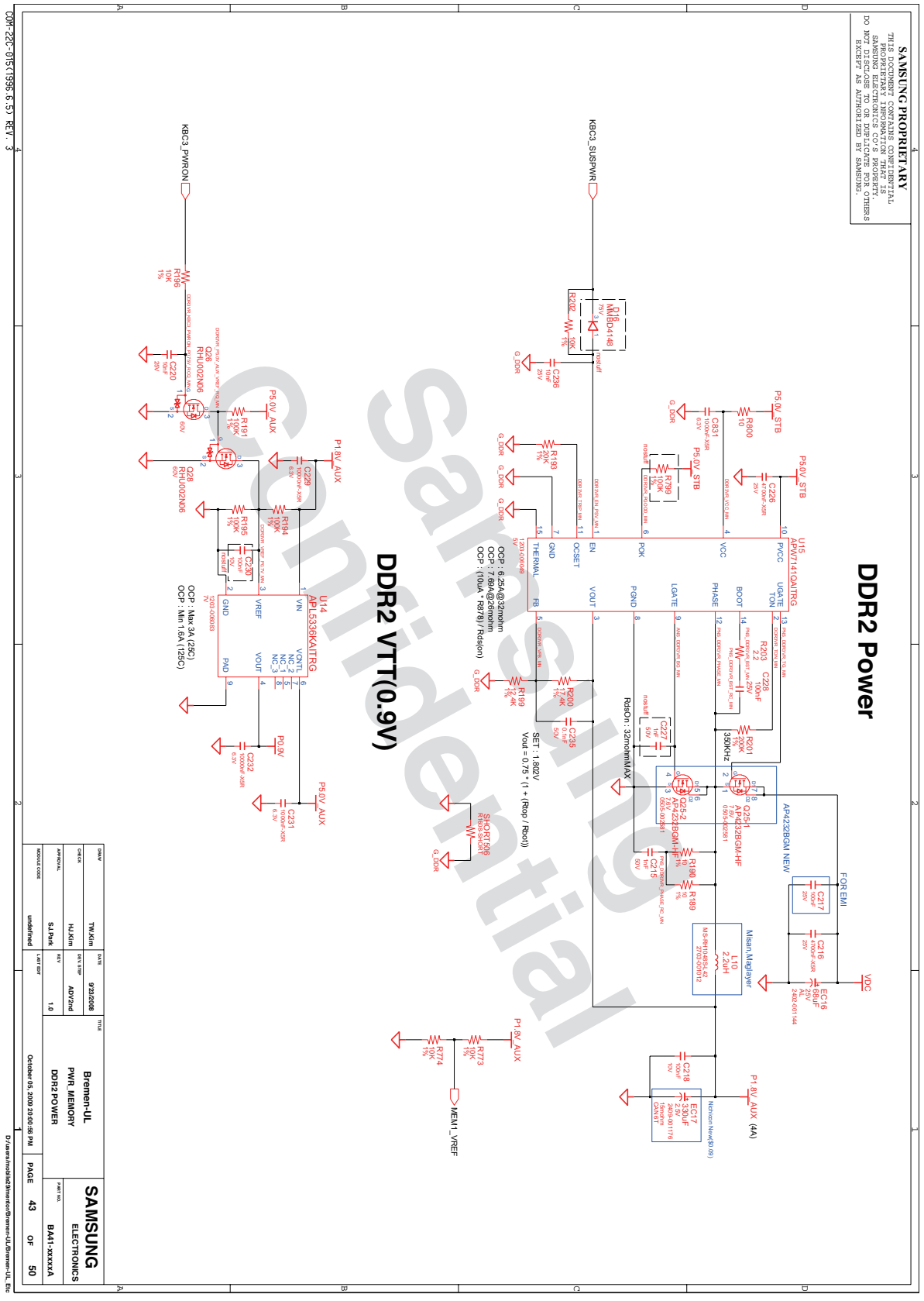

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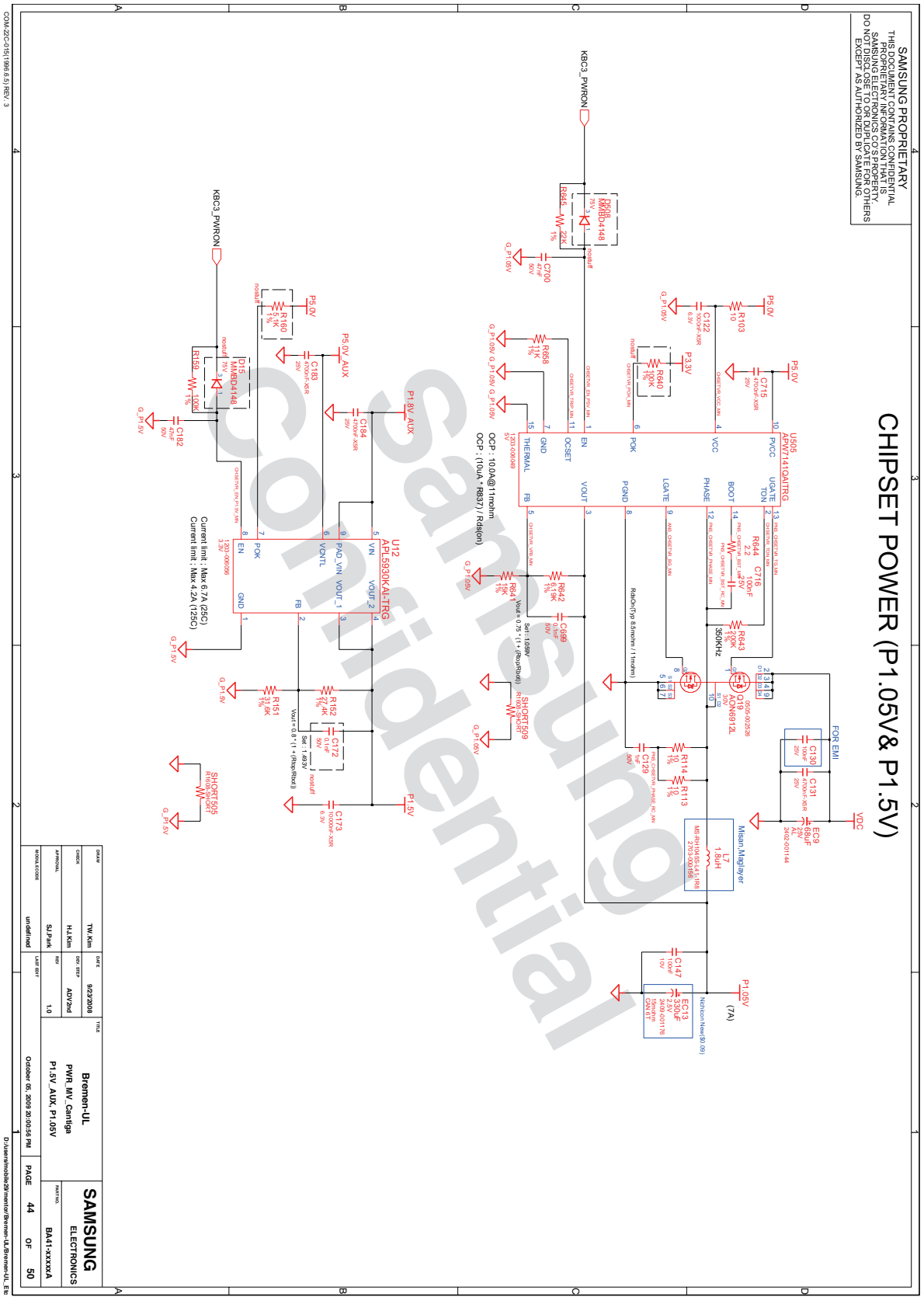

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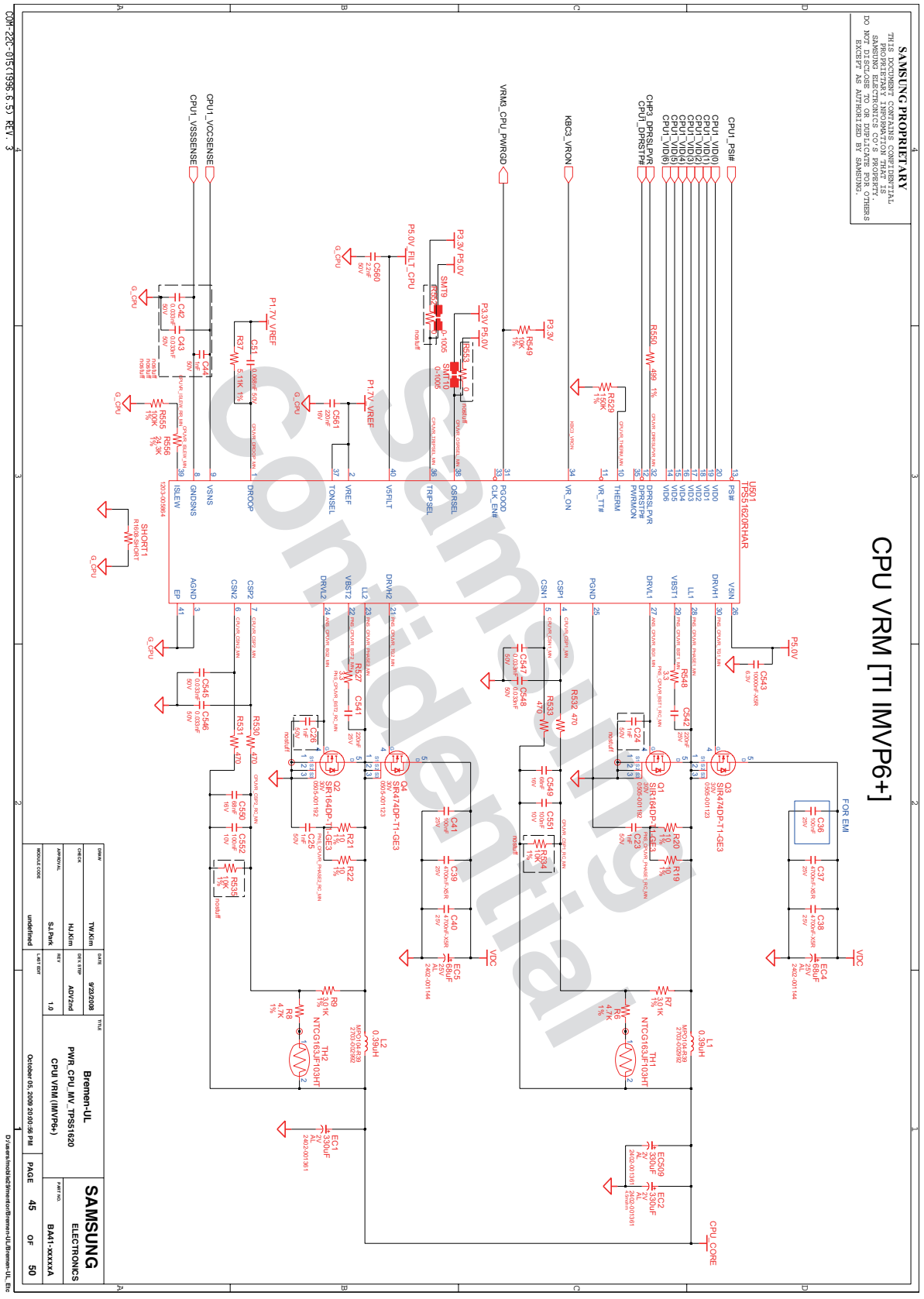
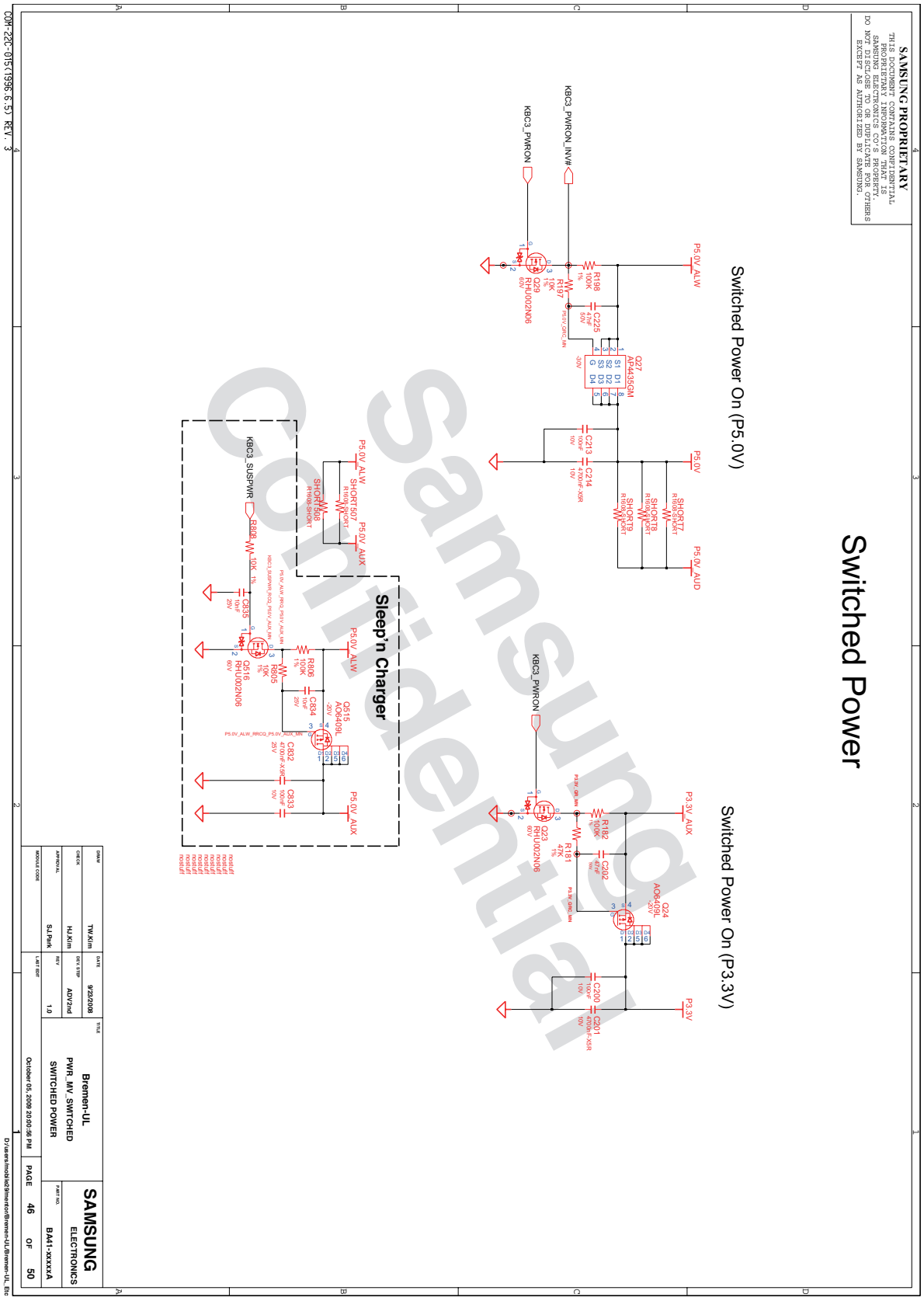
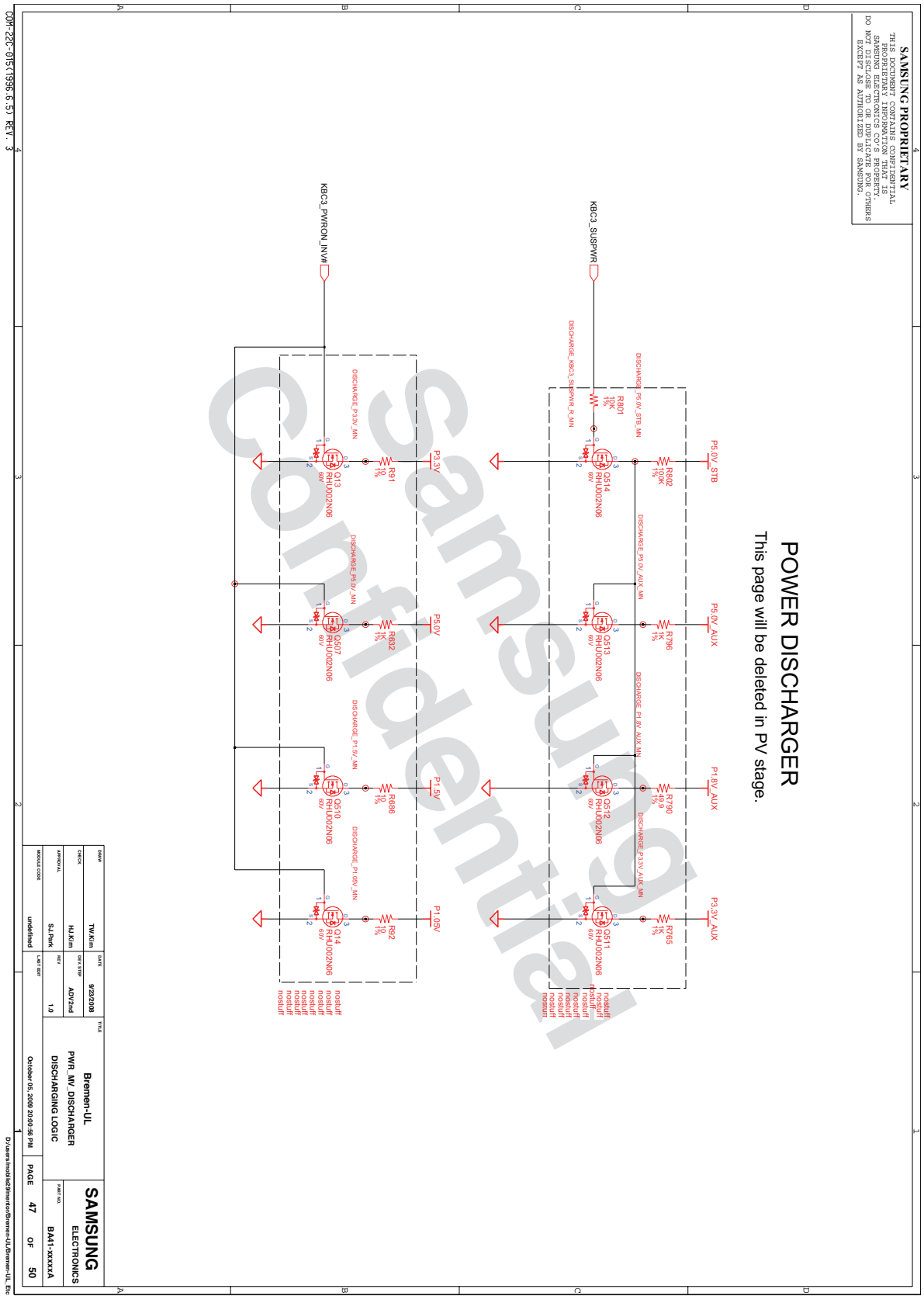


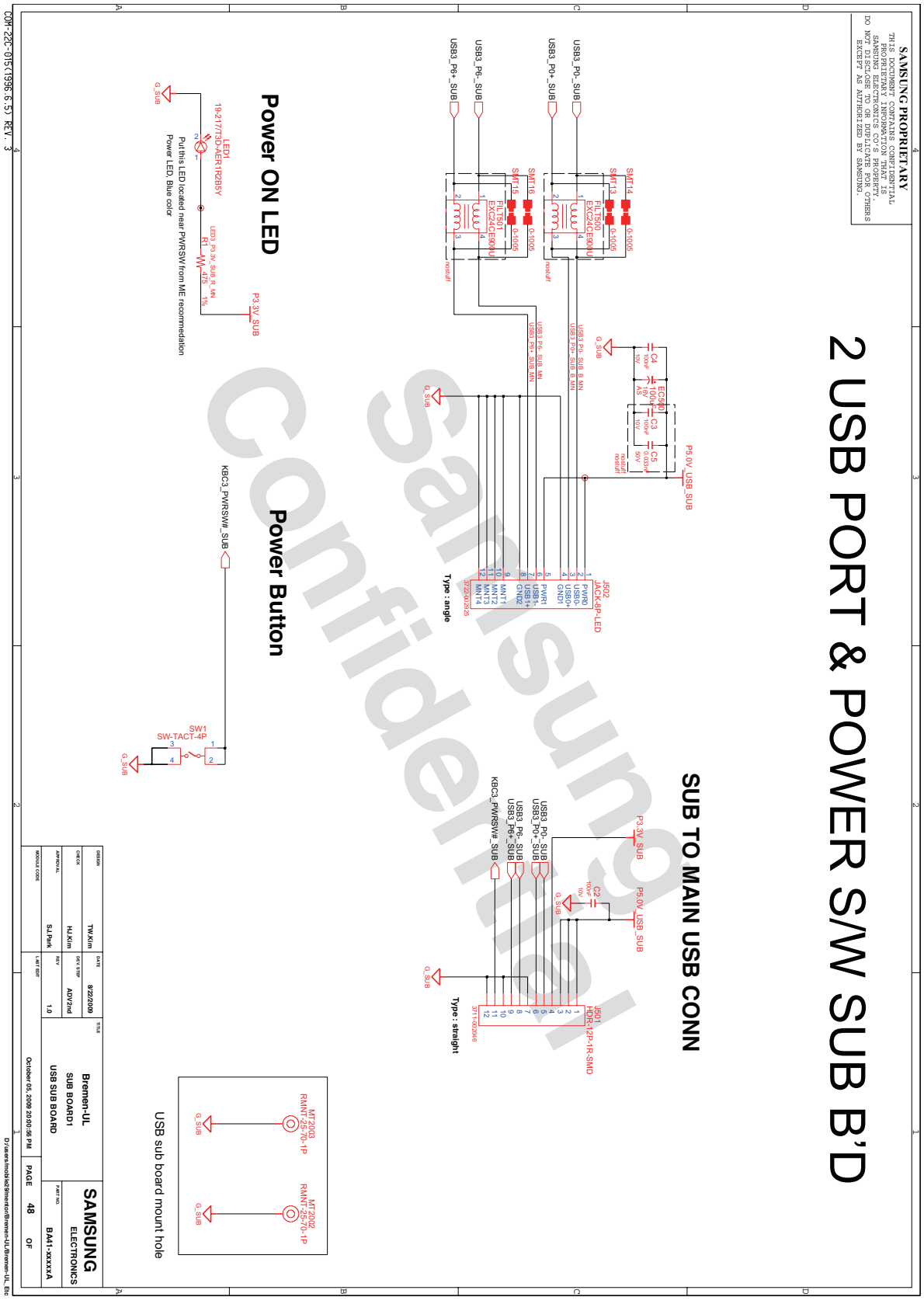
8. Block Diagram and Schematic



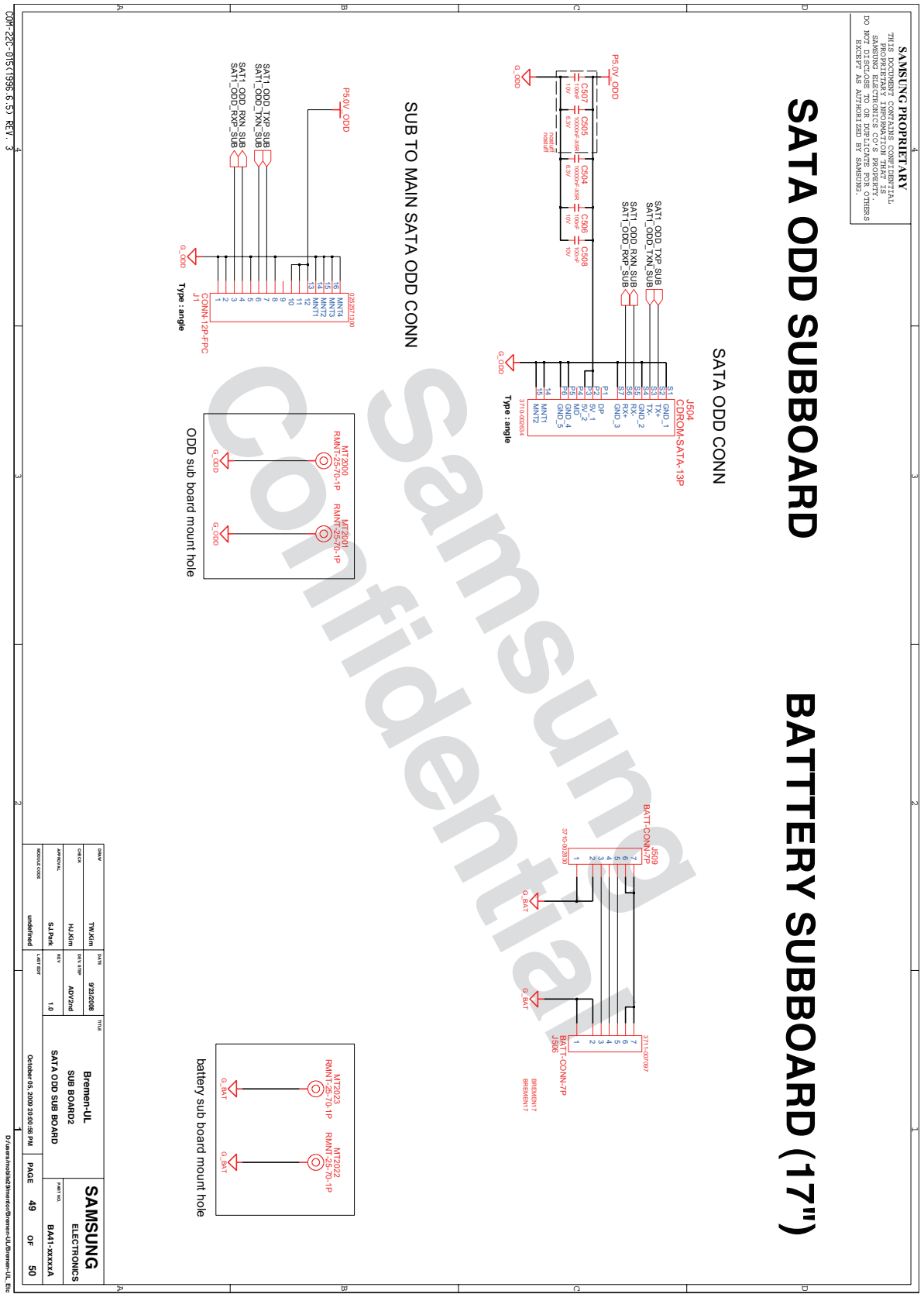
8. Block Diagram and Schematic



8. Block Diagram and Schematic



8. Block Diagram and Schematic



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