

OSLO2

CPU : Intel Penryn-6M (1067/800) MHz
 Chip Set : Intel Cantiga & ICH9M
 Remarks : Montevina Platform

Model Name : Oslo2_DDR3
 PBA Name : MAIN
 PCB Code : BA41-00866A
 BA41-00867A
 Dev. Step : MP
 Revision : 1.1
 T.R. Date : 2008. 05.15

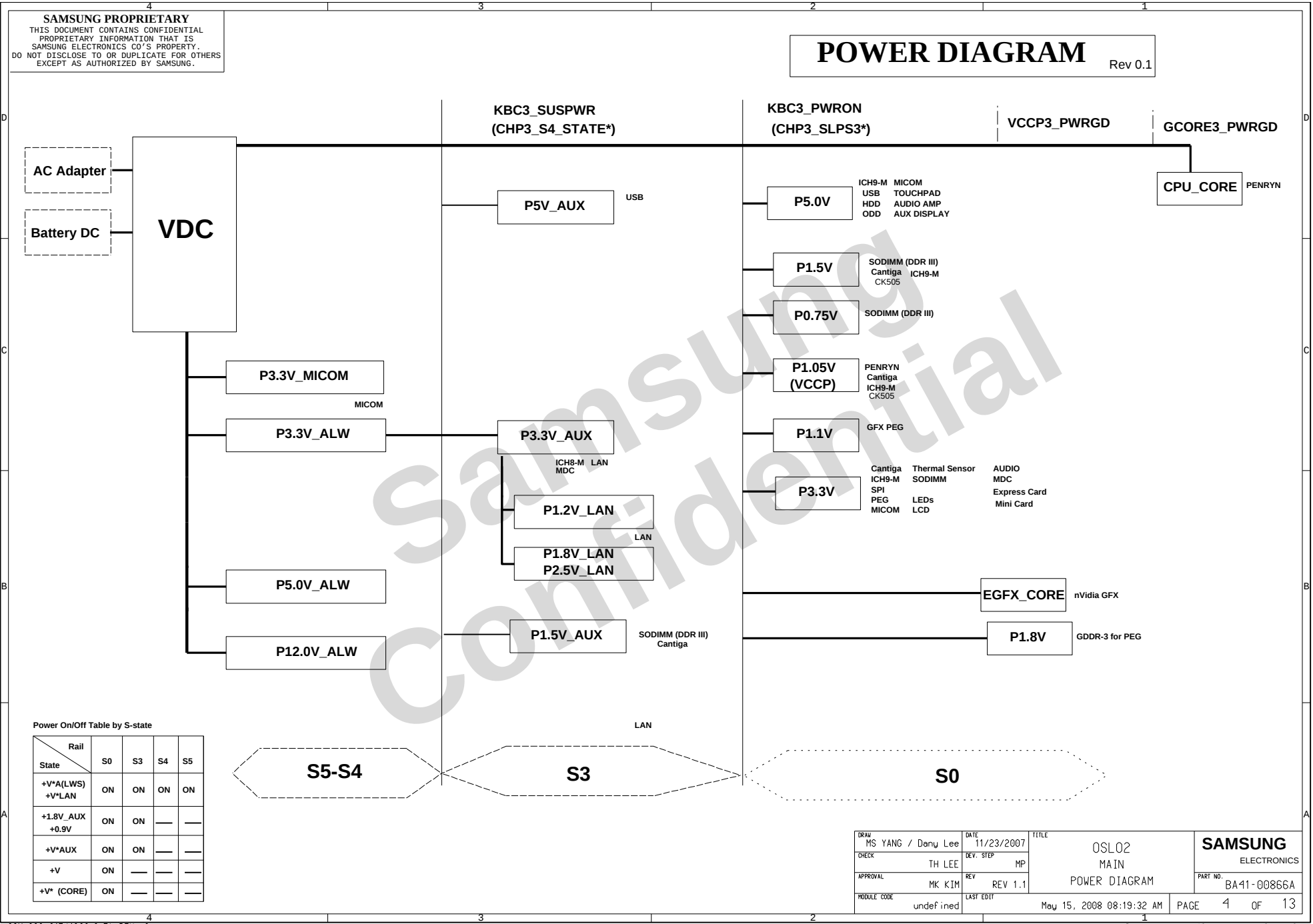
DRAW	CHECK	APPROVAL
MS YANG TH LEE	TH LEE	MK KIM

■ Owner : SEC Mobile R & D Signature : X

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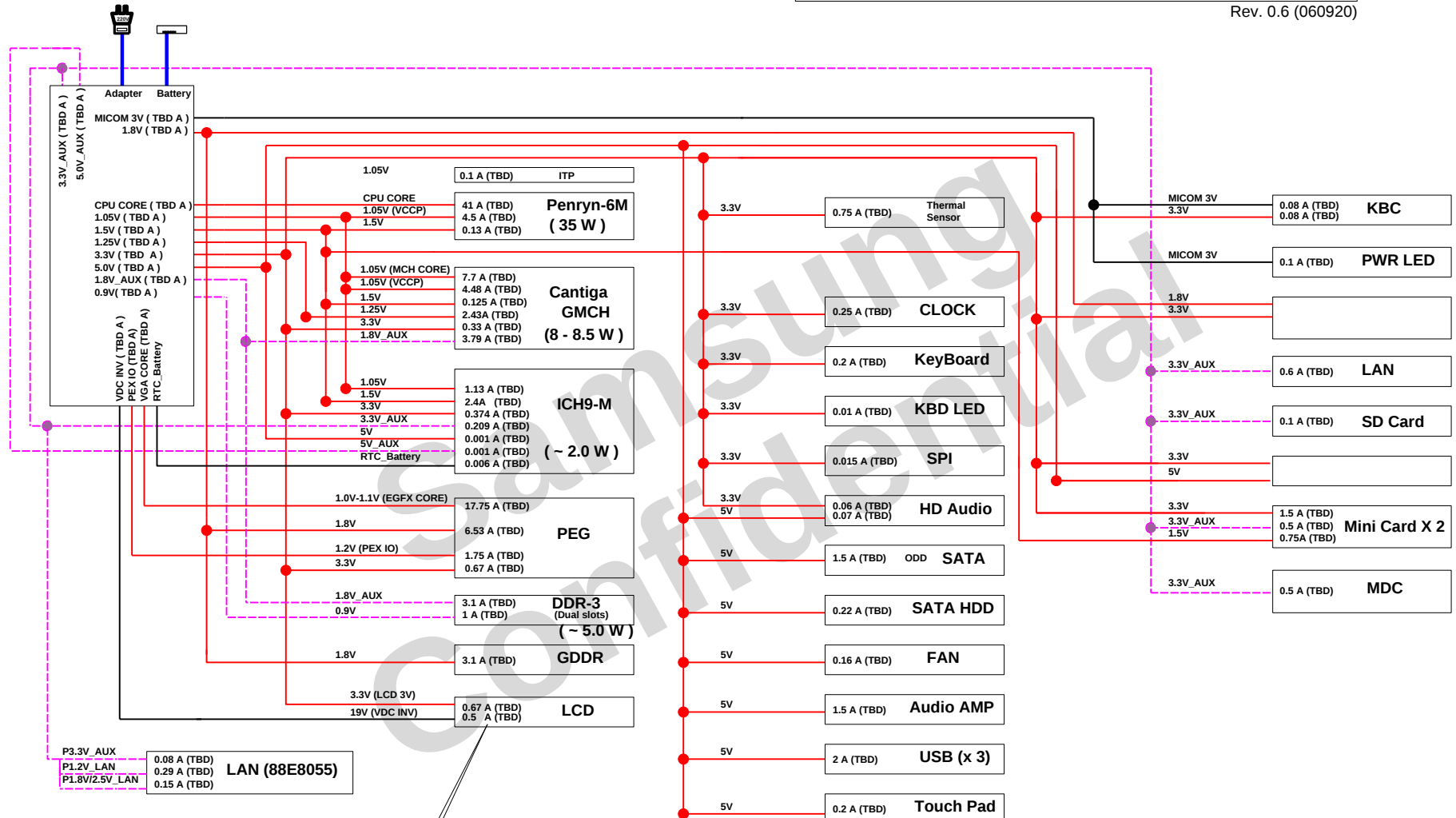
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APPROVAL	MK KIM	REV	REV 1.1		COVER	
MODULE CODE		LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	1	PART NO. BA41-00866A
				OF	13	

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POWER RAILS ANALYSIS

Rev. 0.6 (060920)

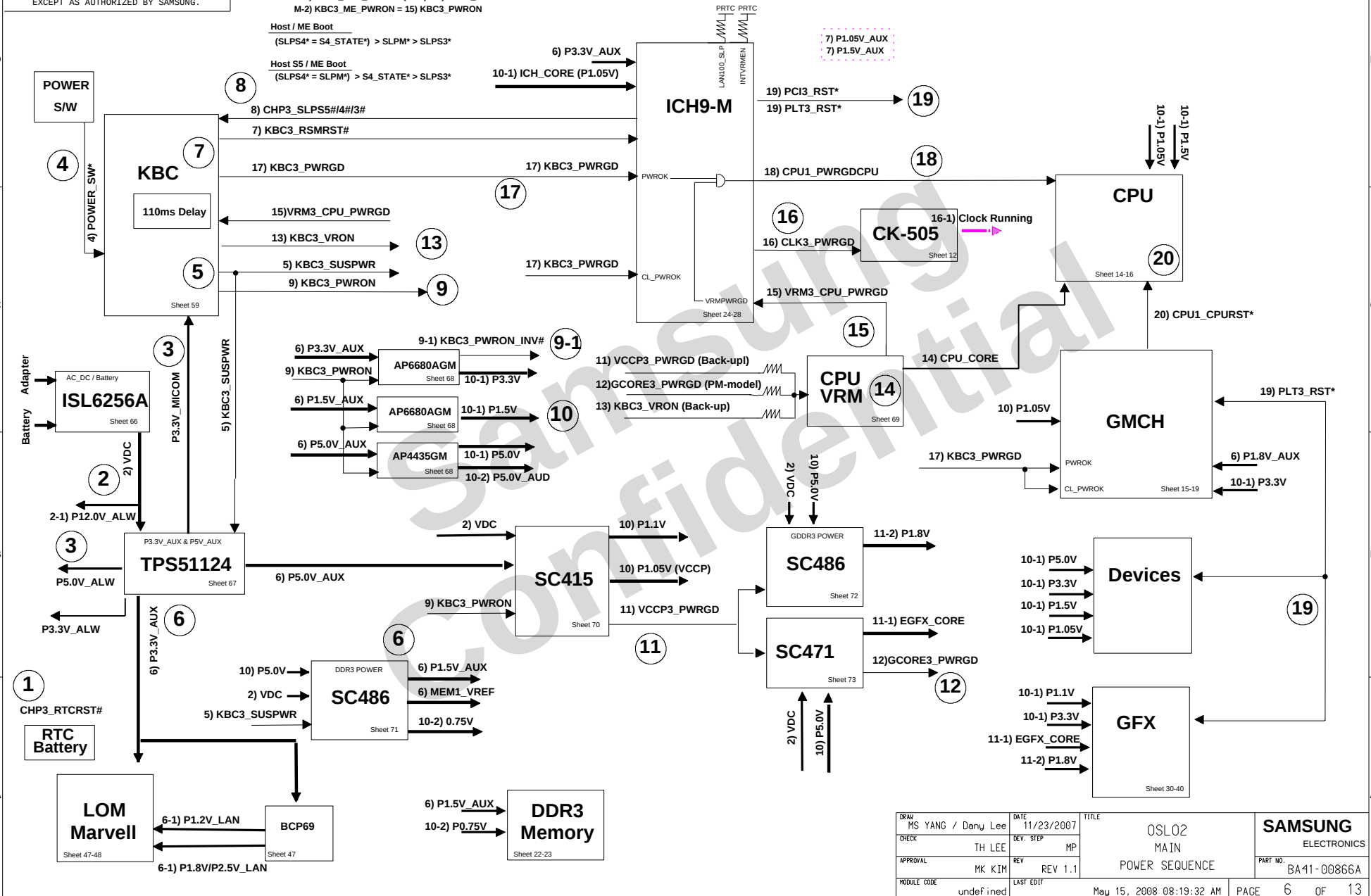


Value by Datasheet/Application notes (Value by measurement)

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APPROVAL	MK KIM	REV	REV 1.1			PART NO. BA41-00866A
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POWER SEQUENCE

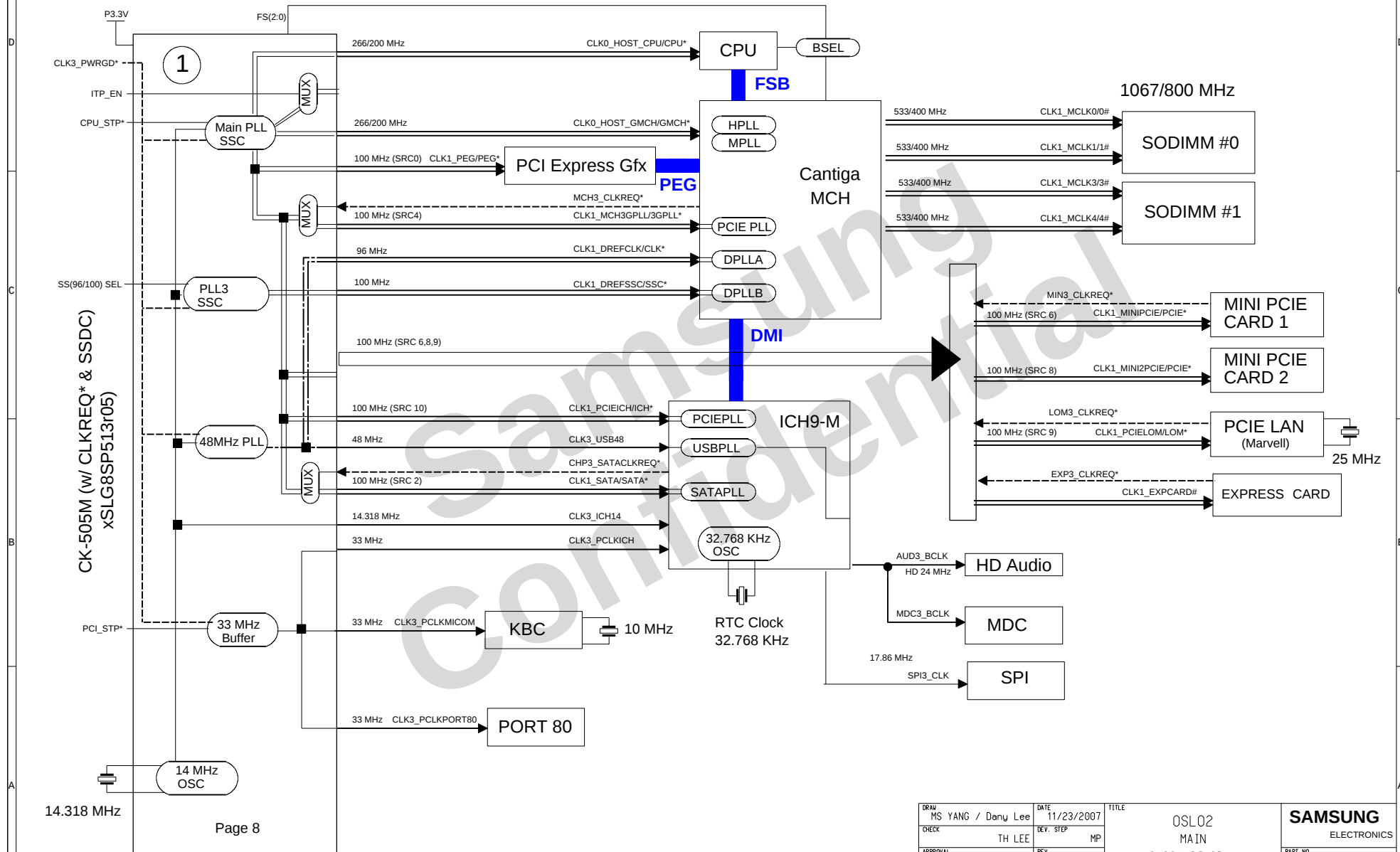
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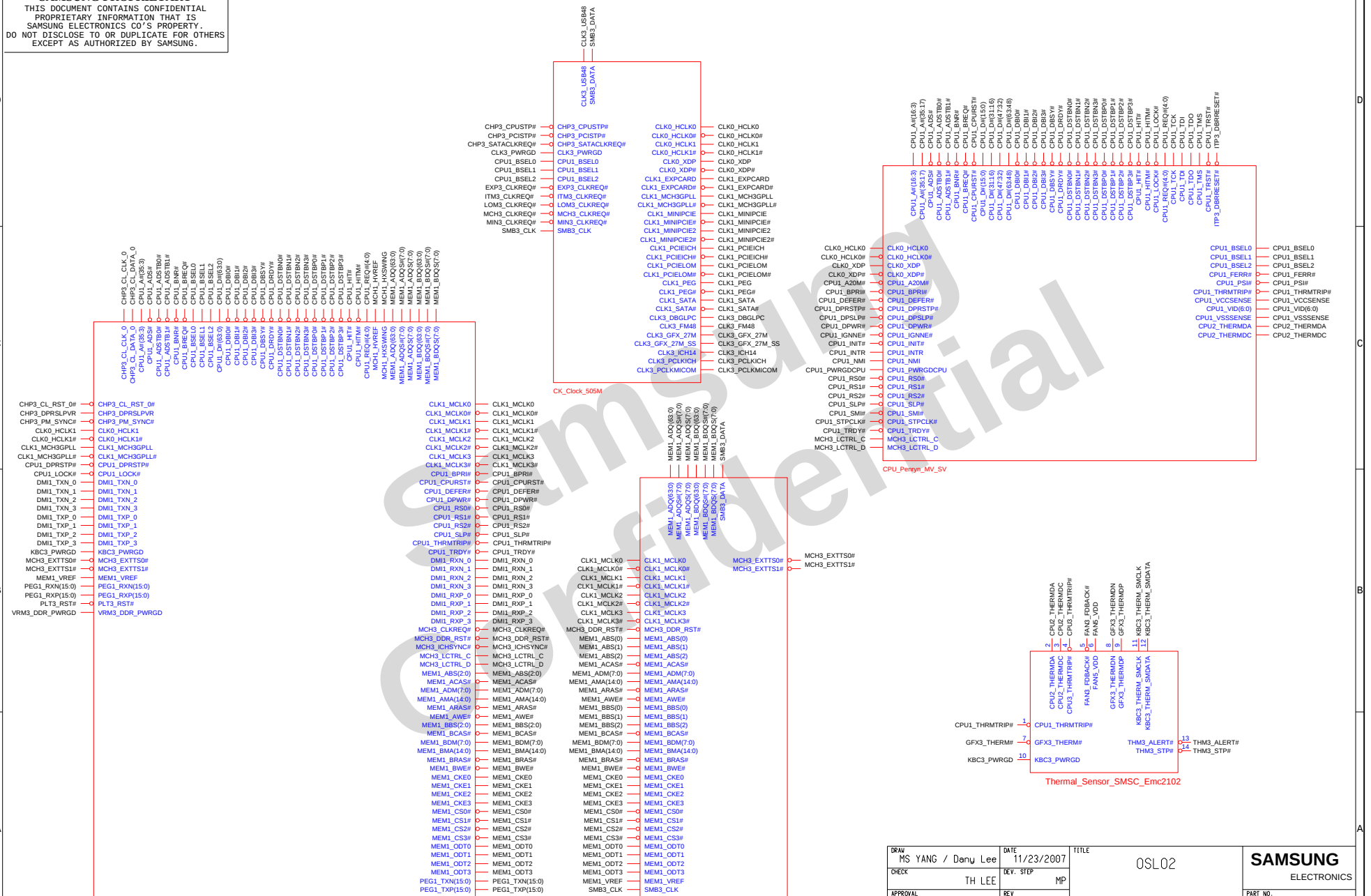
CLOCK DISTRIBUTION Rev. 0.1



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APPROVAL	MK KIM	REV	REV 1.1	CLOCK DIAGRAM		
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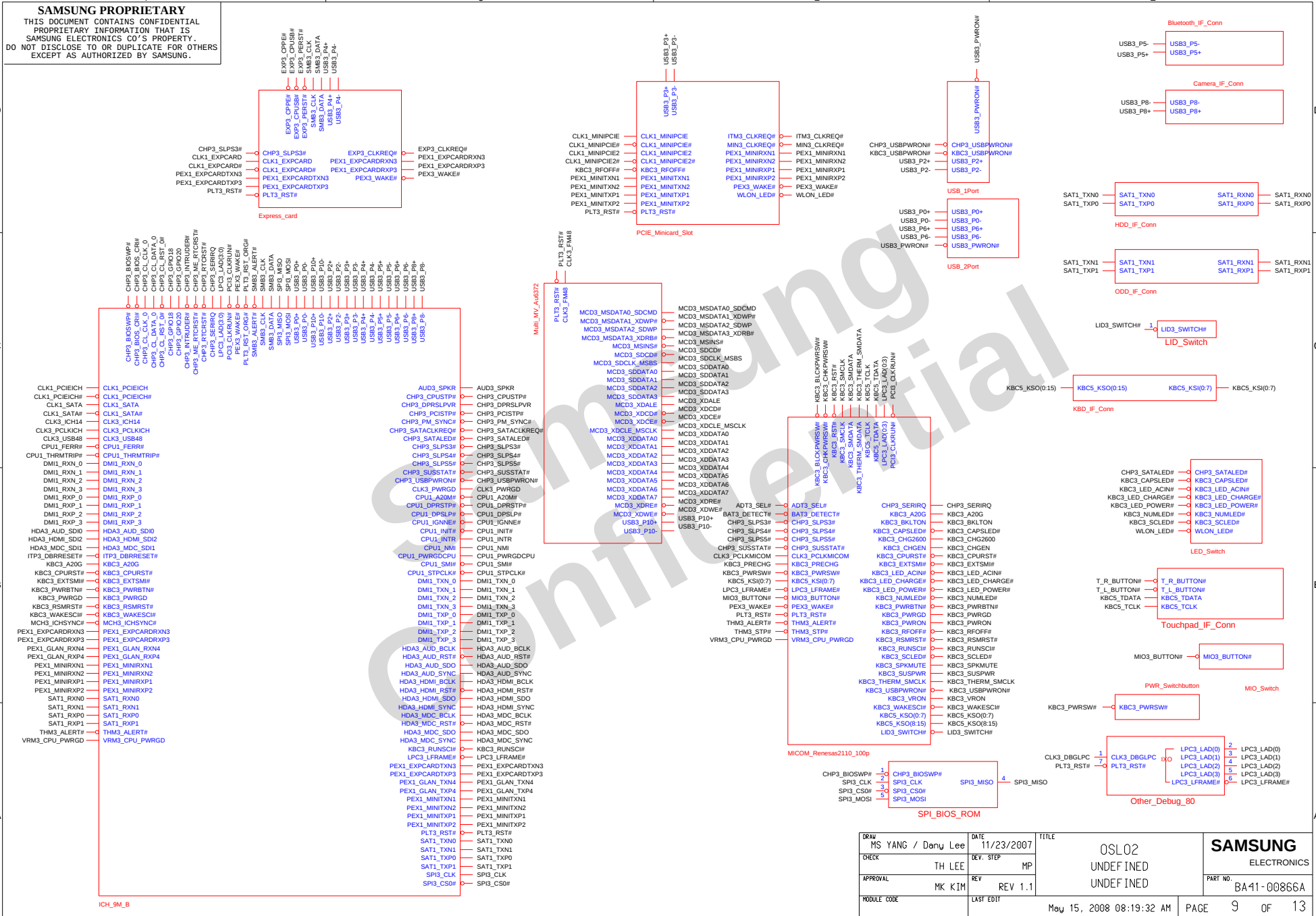
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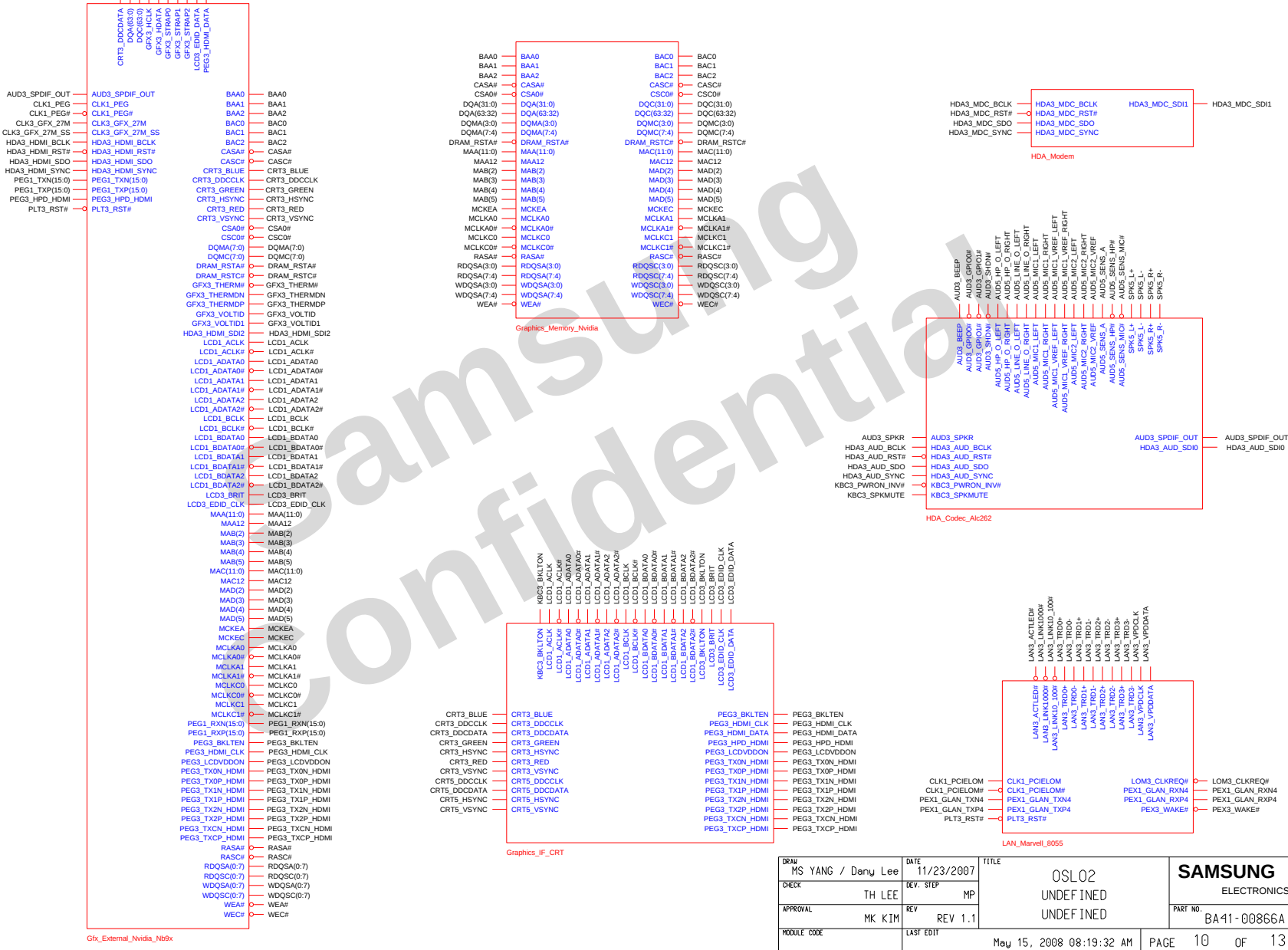
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TH LEE	MP	UNDEFINED	ELECTRONICS
MK KIM	REV 1.1	UNDEFINED	PART NO. BA11-00866A
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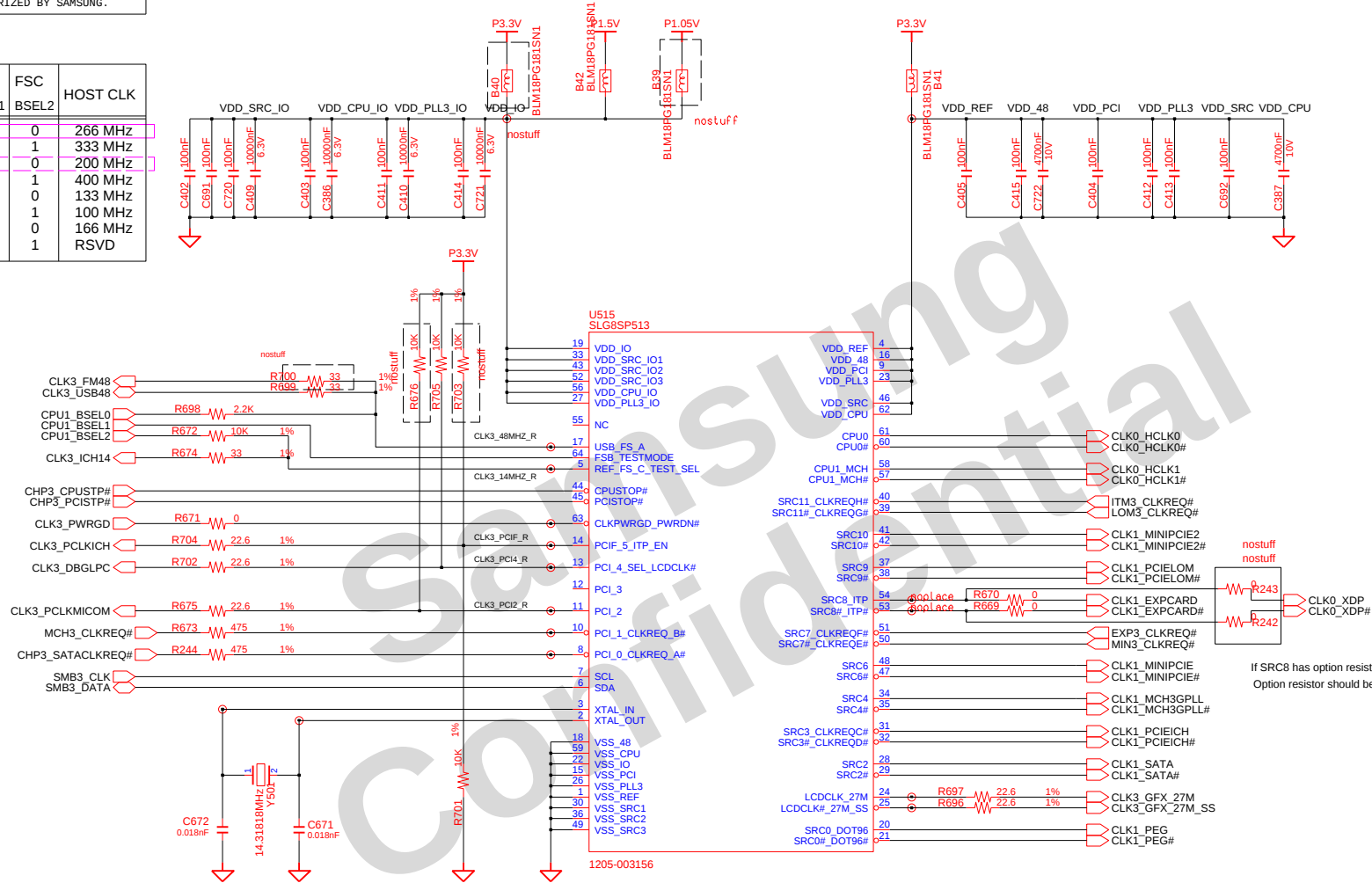
SRP Sheet Number: 9 of 76



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FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATACLKREQ#	SRC2
CLK REQ B	MCH3_CLKREQ#	SRC4
CLK REQ E	MIN3_CLKREQ#	SRC6
CLK REQ F	EXP3_CLKREQ#	SRC8
CLK REQ G	LOM3_CLKREQ#	SRC9

SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

Place 14.318MHz within
 500mils of CK-505

2nd source IDT, 1205-003159

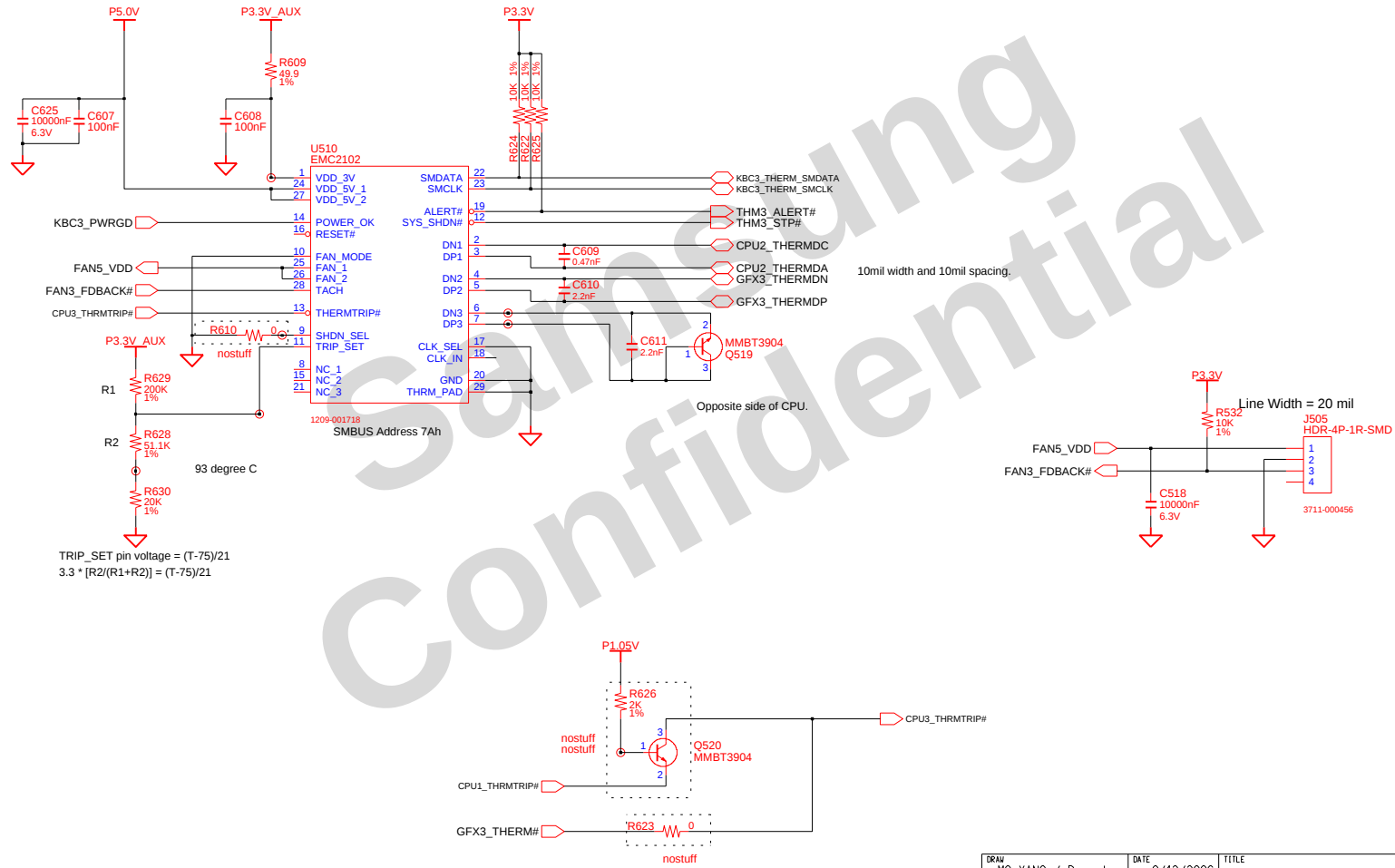
This part is 64pin QFN package.

DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 Main_Clock_Circuit CK-Clock_505M	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP	REV 1.1	
APPROVAL MK KIM	REV 1.1	LAST EDIT May 15, 2008 08:19:32 AM	PAGE 1 OF 1
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THERMAL SENSOR & FAN CONTROL

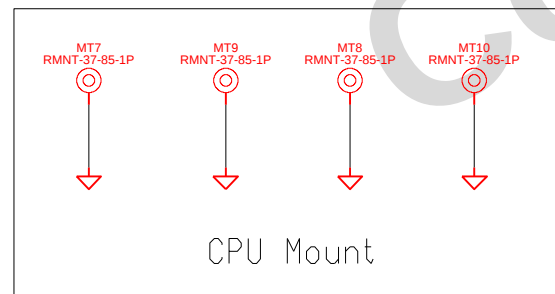
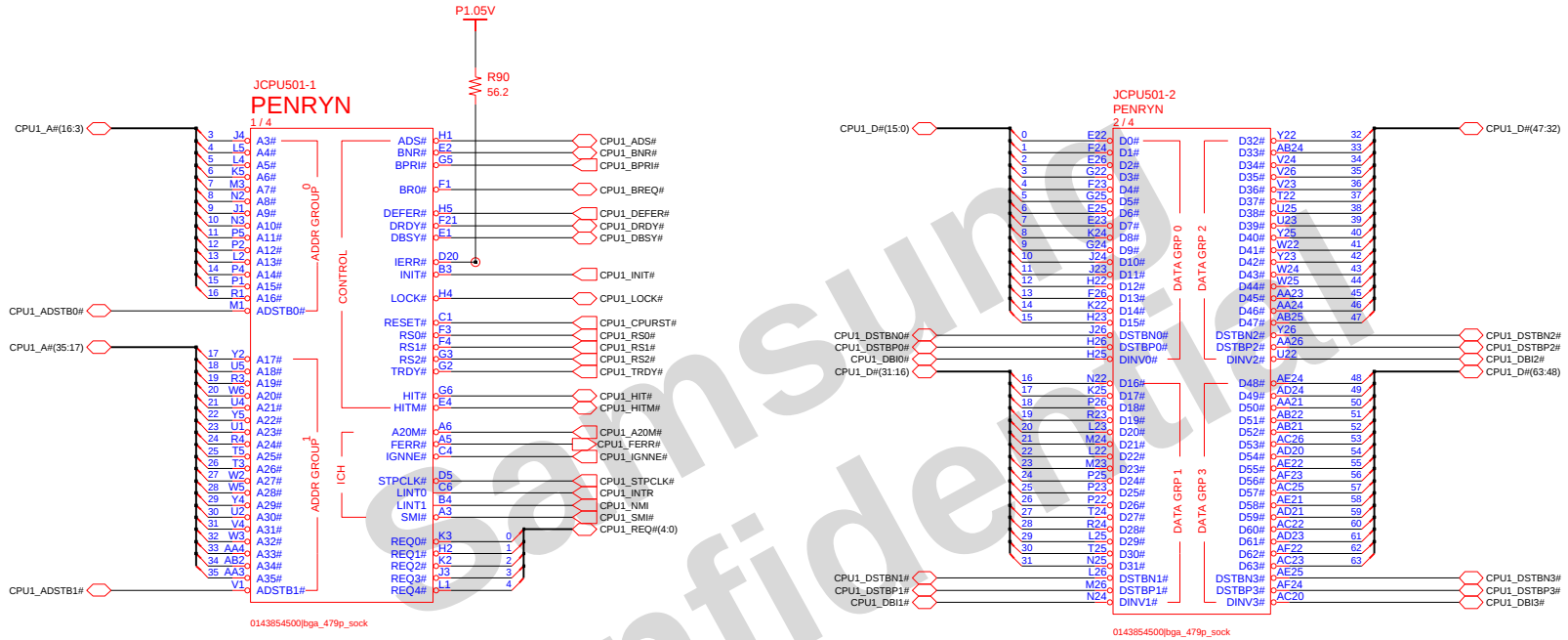


DRAW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
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APPROVAL	MK KIM	REV	REV 1.1	thermal_Sensor_SMSC_Emc2102	BA41-00866A	
MODULE CODE		LAST EDIT				

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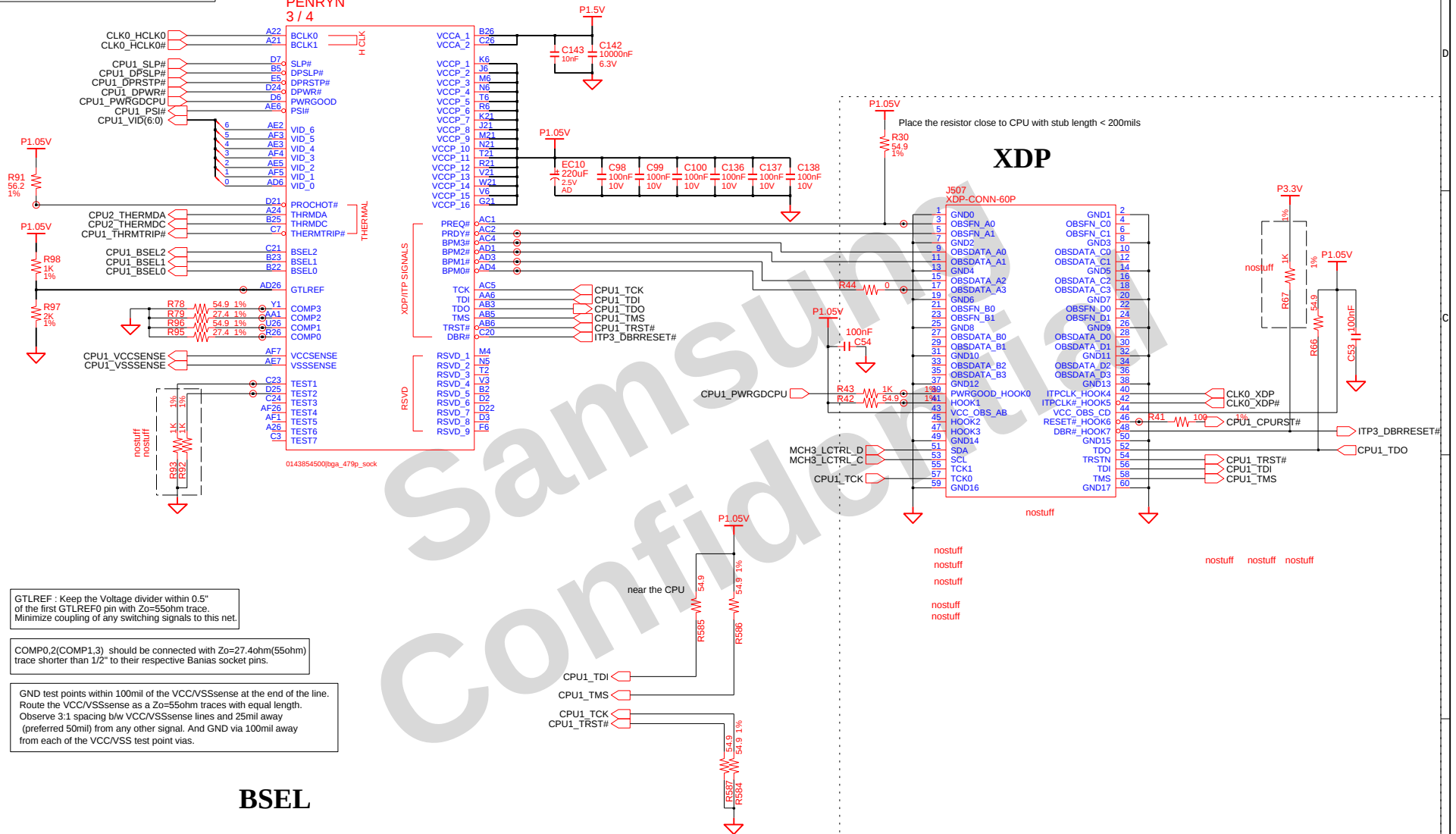
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479P CPU socket is 3704-001153



DRW MS YANG / Dany Lee	DATE 11/8/2006	TITLE OSL02 CPU PENRYN (1/3)	SAMSUNG ELECTRONICS PART NO. BA11-00866A
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APPROVAL MK KIM	REV REV 1.1		
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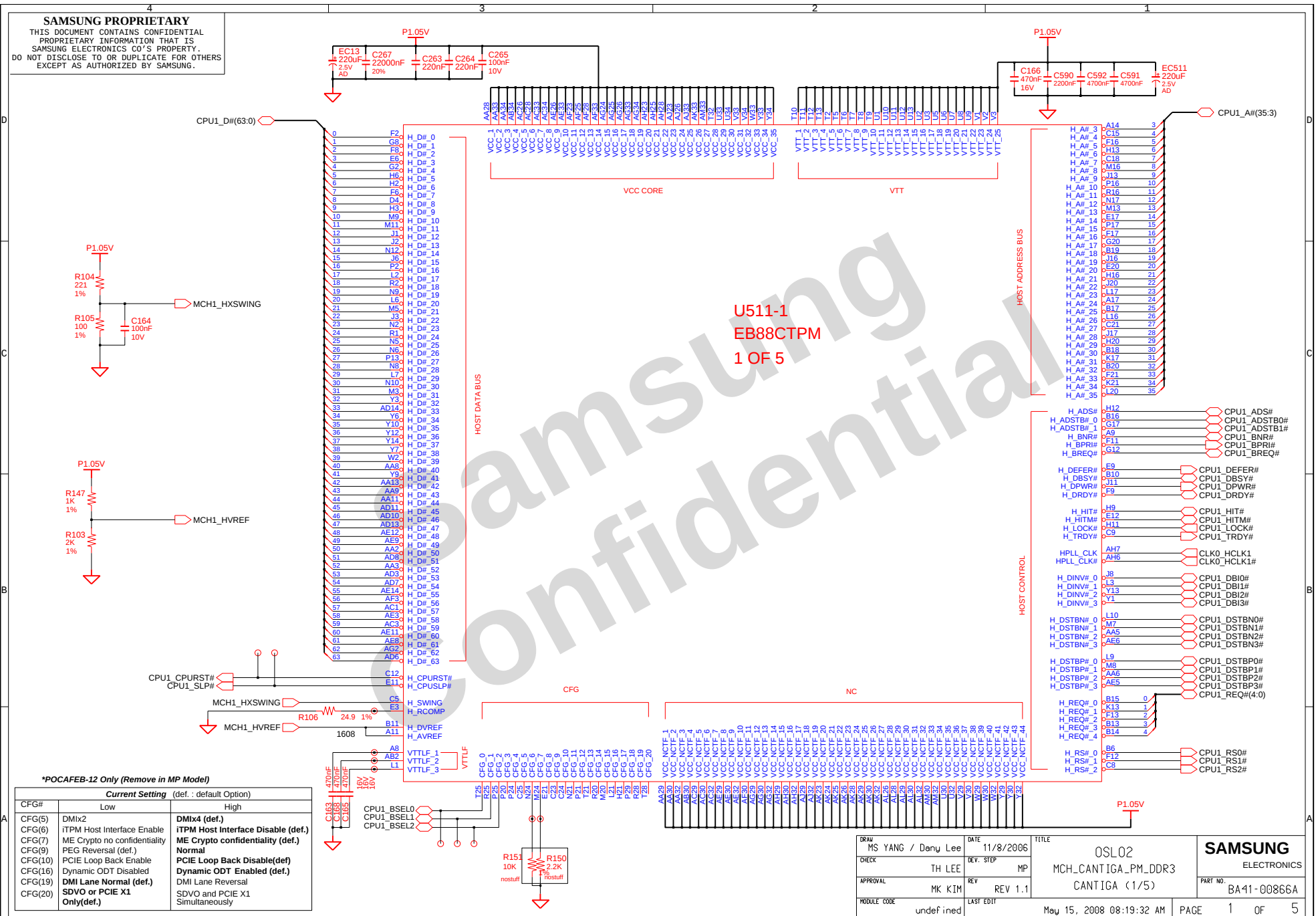
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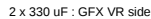


GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a $Z_0=55\text{ohm}$ traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

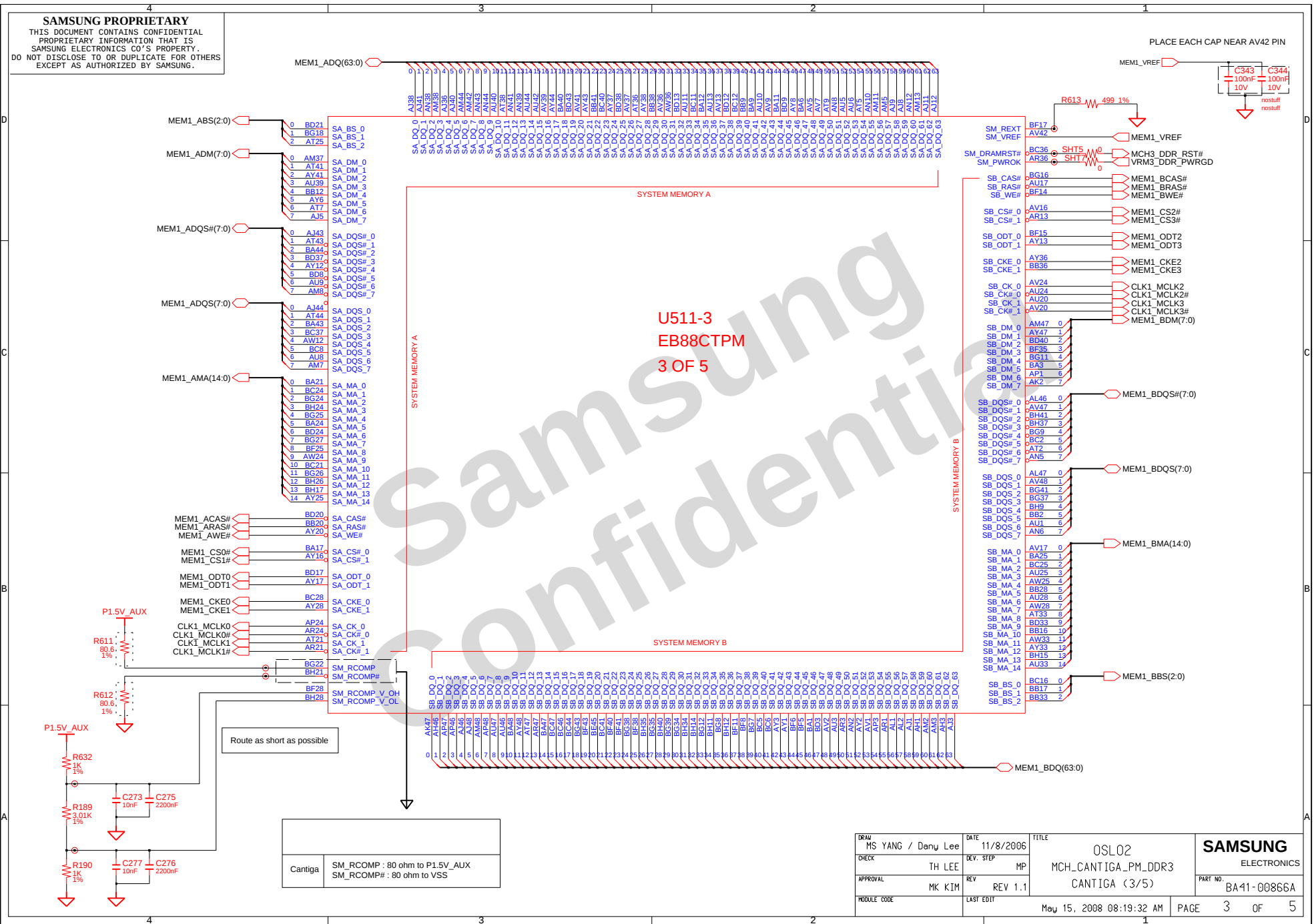
	Pull-up	Pull-down
FSB 1067 MHz FSB 800 MHz	BSEL1	BSEL0, BSEL1, BSEL2 BSEL0, BSEL2

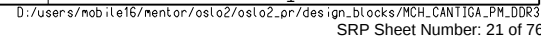
	Pull-up	Pull-down
FSB 1067 MHz FSB 800 MHz	BSEL1	BSEL0, BSEL1, BSEL2 BSEL0, BSEL2





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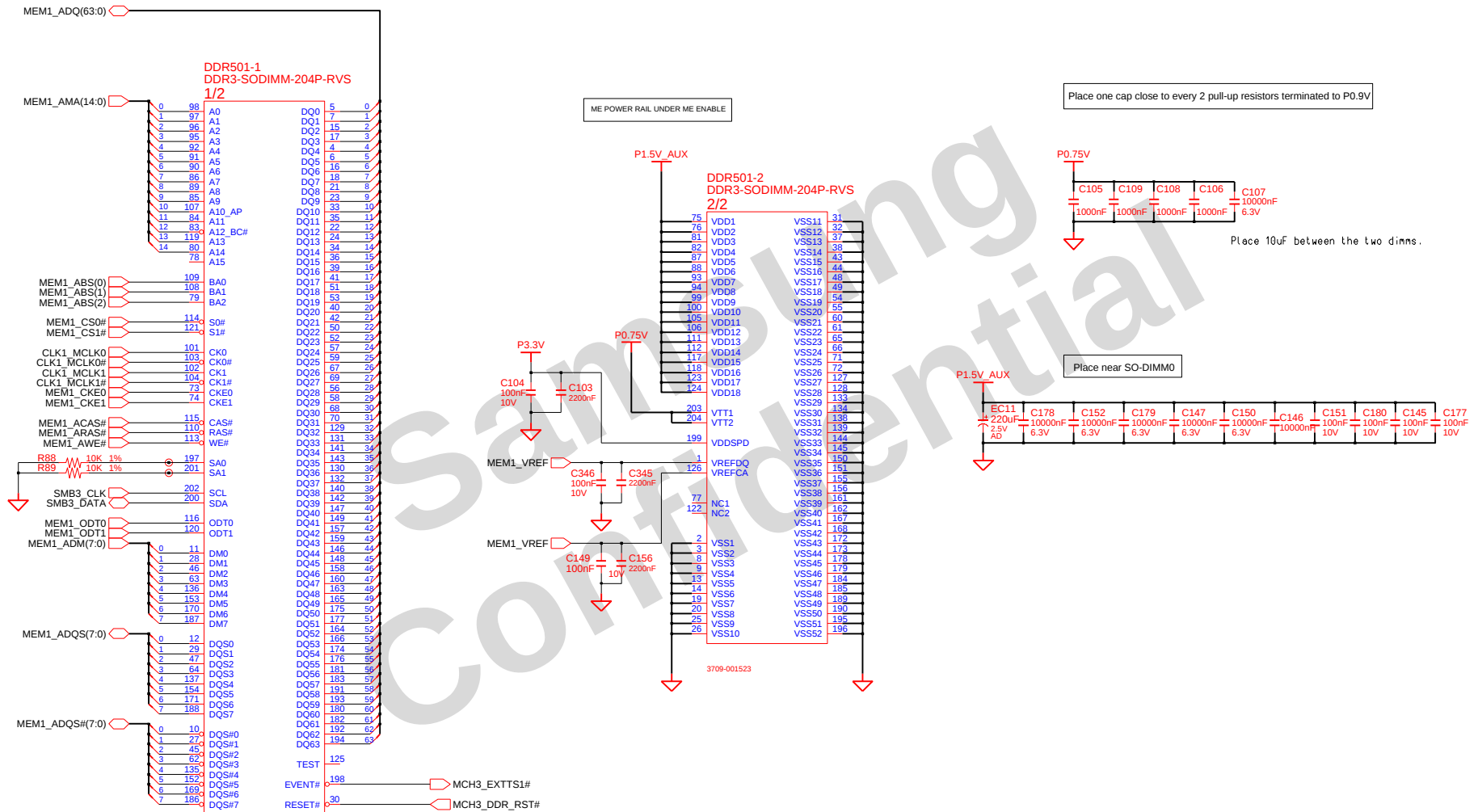


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PART NO. BA41-00866A

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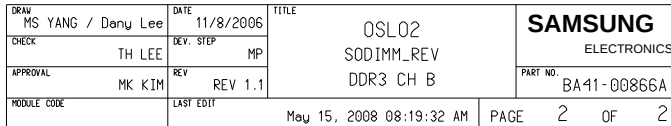
DDR SO-DIMM #0

Height : 5.2mm (Reverse)



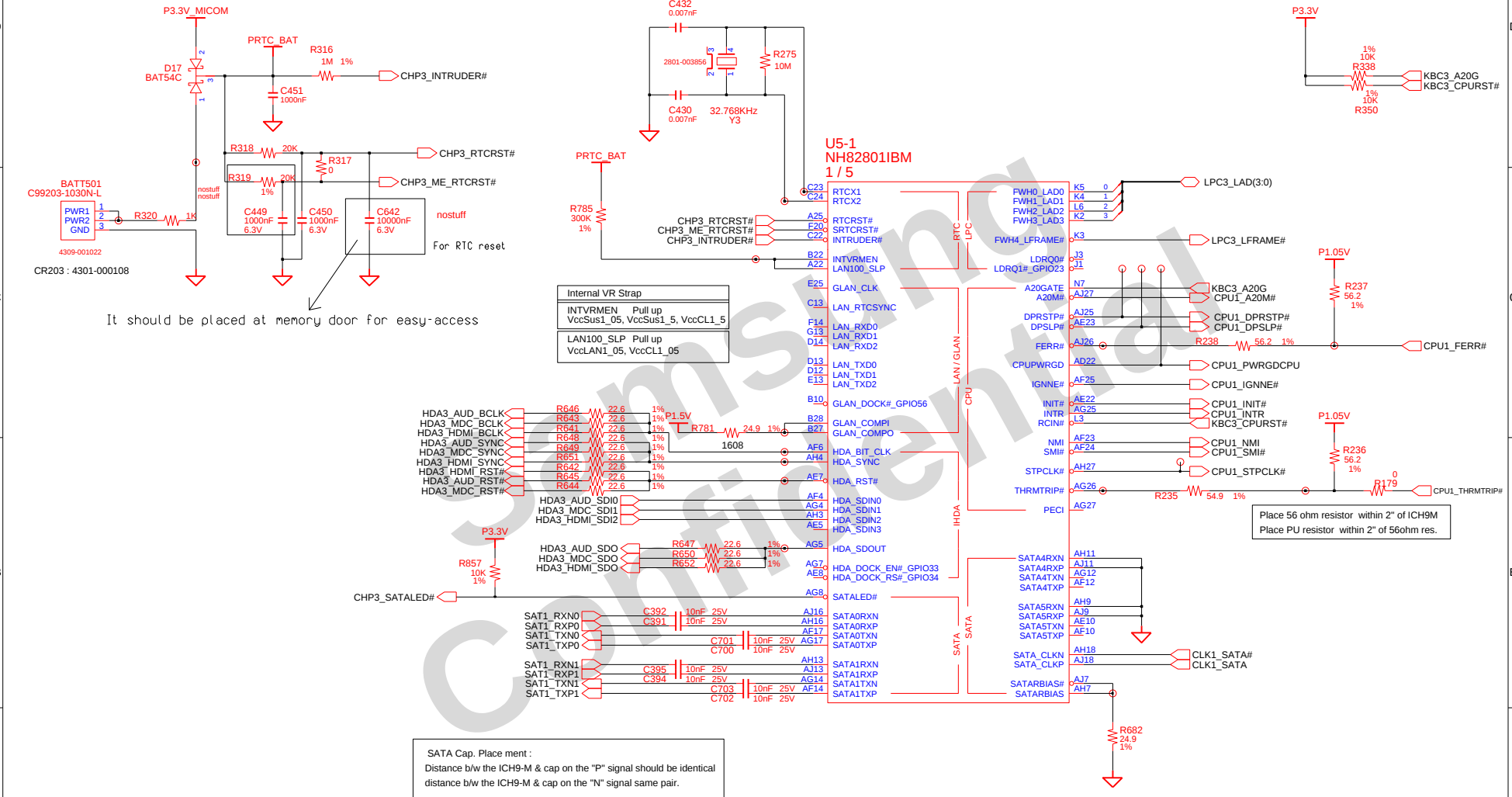
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CHECK TH LEE	DEV. STEP MP		
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT		
May 15, 2008 08:19:32 AM			PAGE 1 OF 2

DDR SO-DIMM #1
Height : 9.2mm (Reverse)



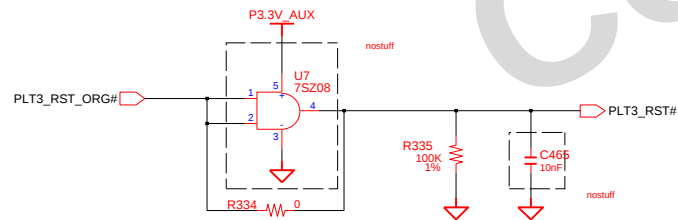
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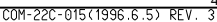


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MODULE CODE		LAST EDIT				

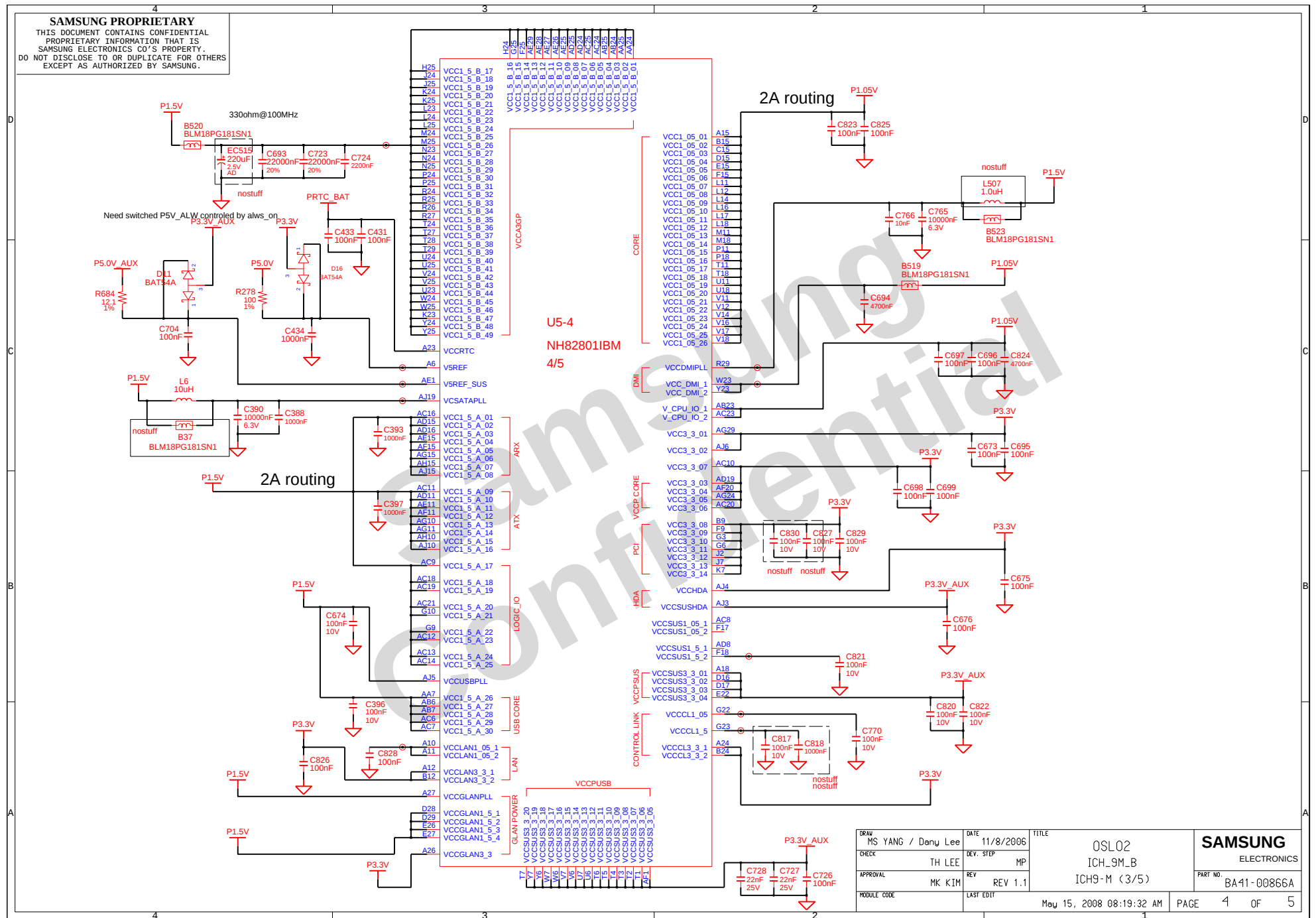
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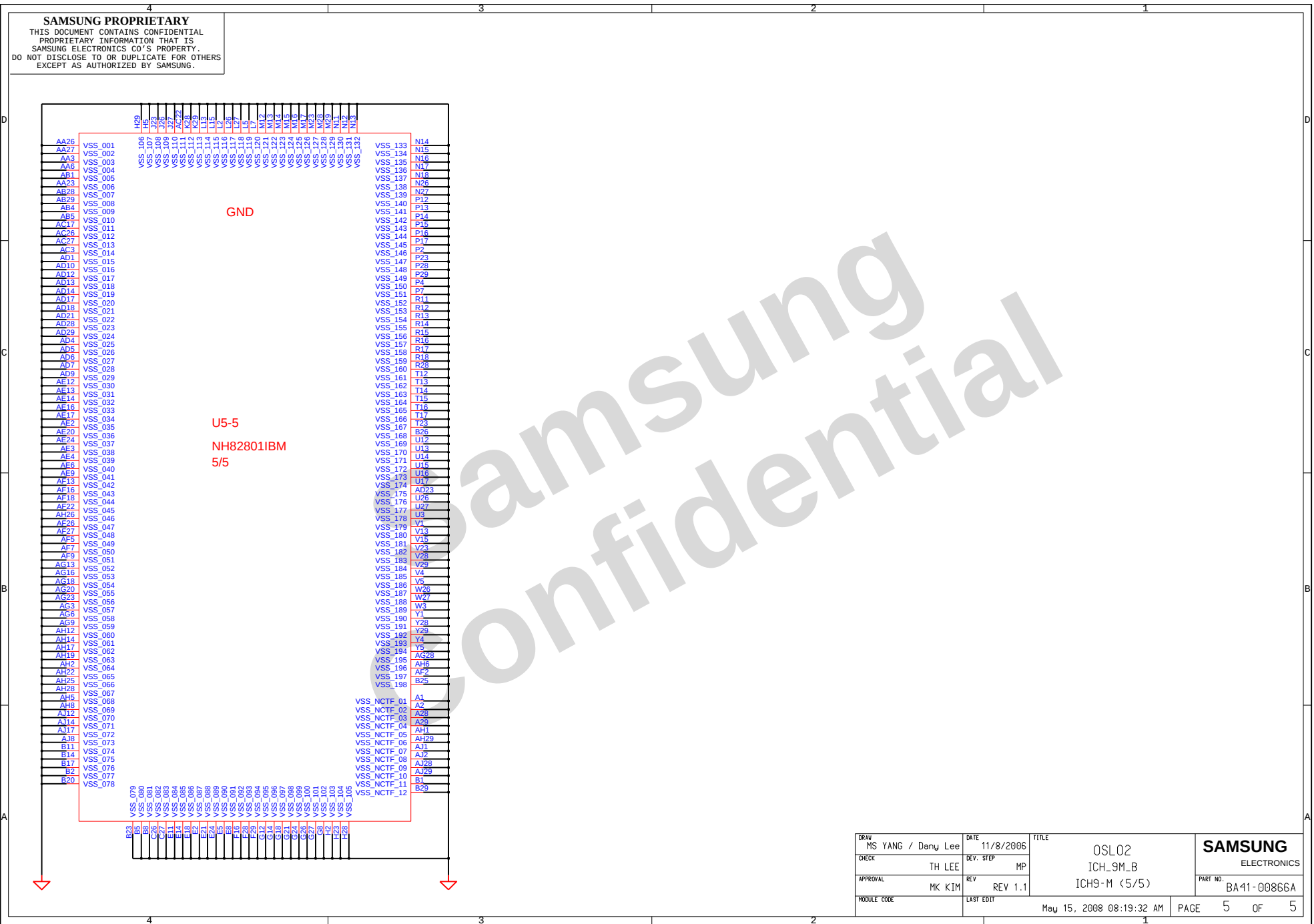


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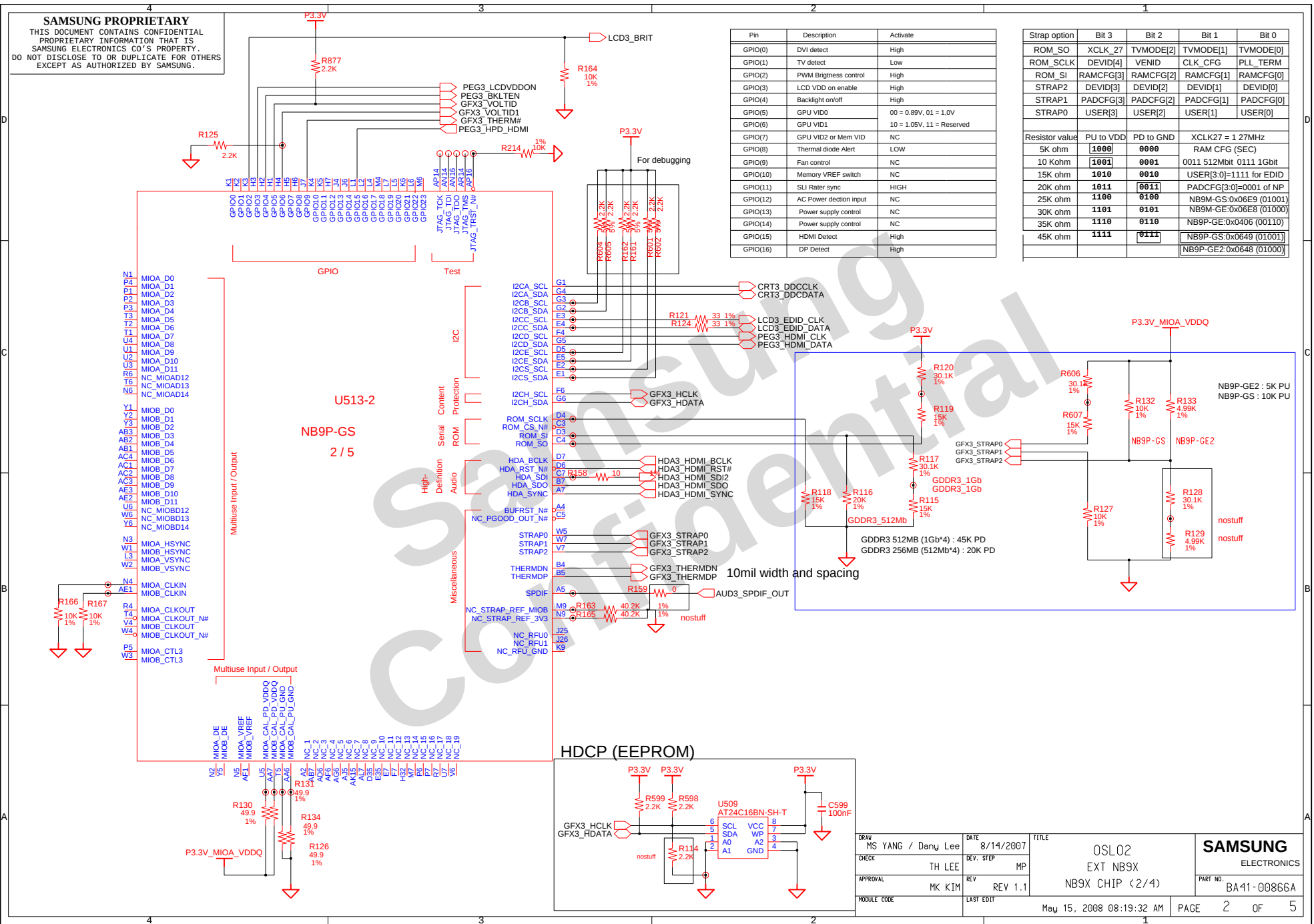


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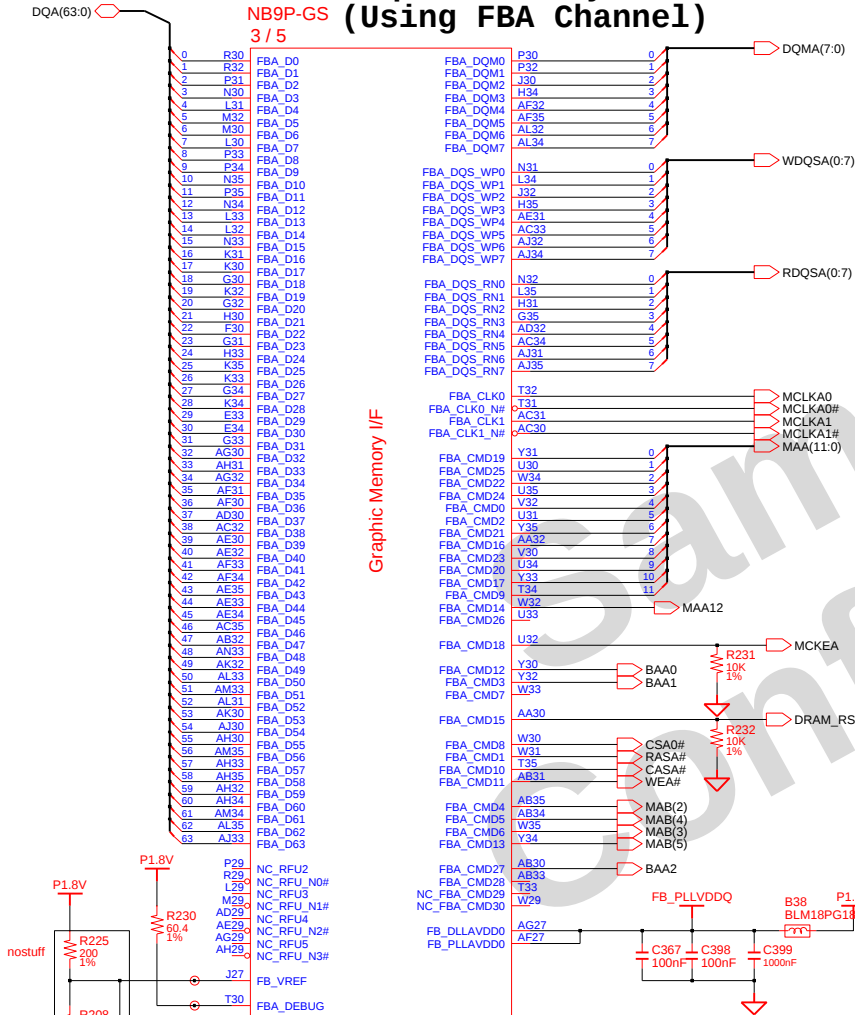




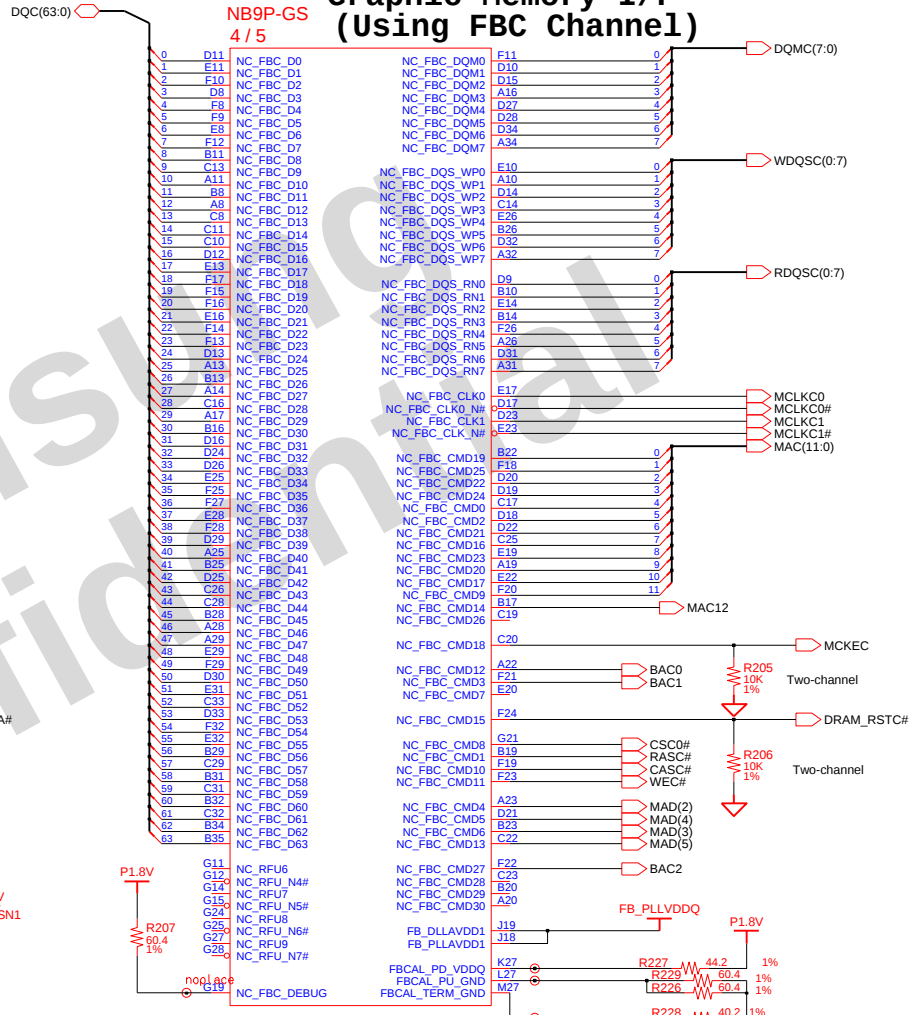
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MODULE CODE		LAST EDIT				
				May 15, 2008 08:19:32 AM	PAGE	5 OF 5



U513-3 Graphic Memory I/F
NB9P-GS (Using FBA Channel)
3/5

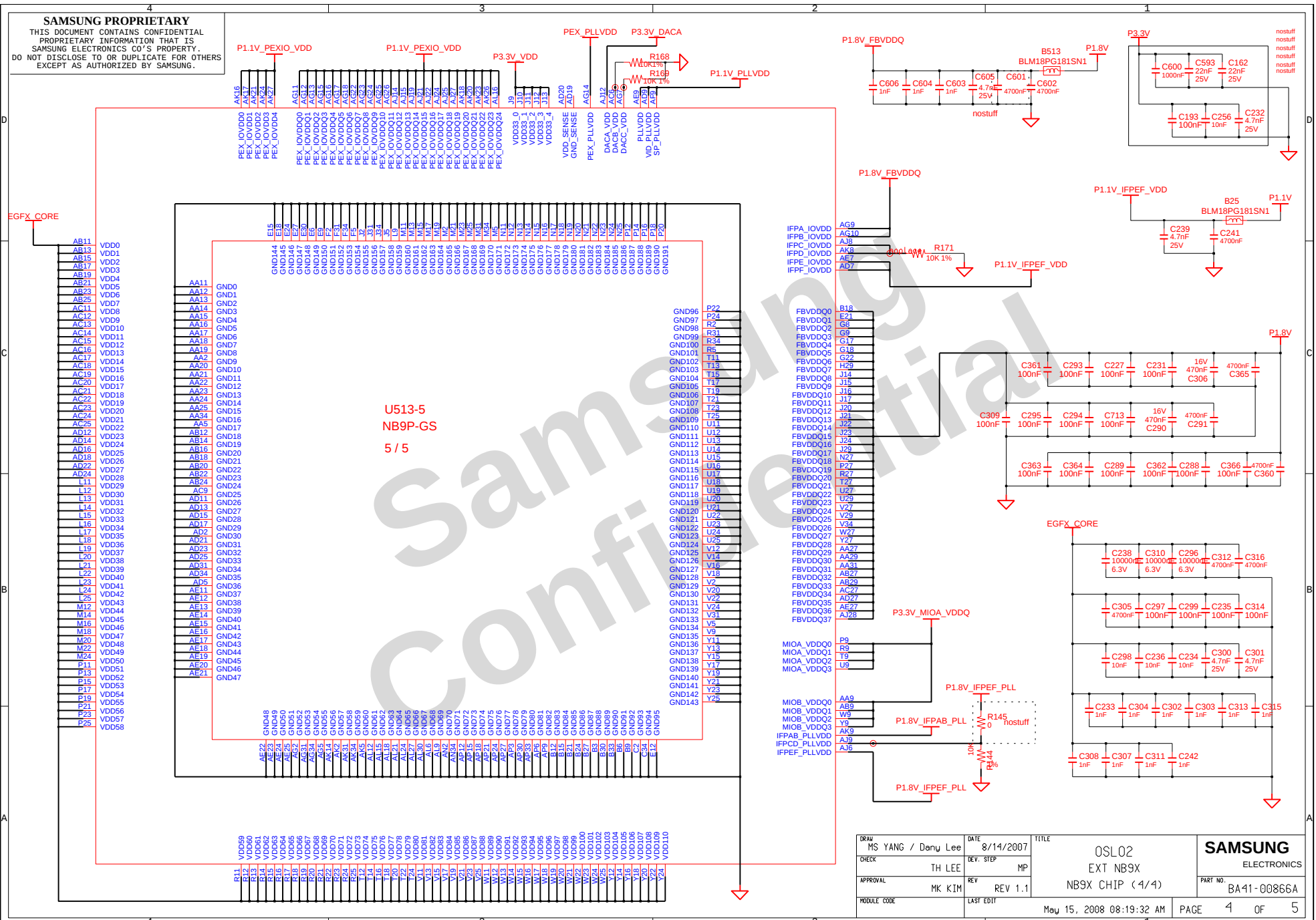


U513-4 Graphic Memory I/F
NB9P-GS (Using FBC Channel)
4/5



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APPROVAL	TH LEE	REV	1.1		NB9X CHIP (3/4)	
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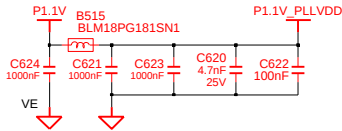
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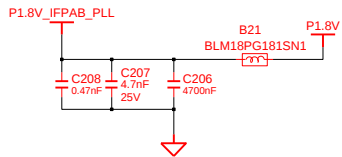
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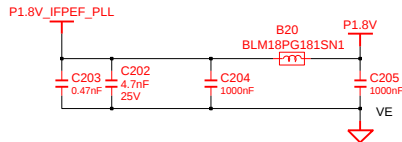
PLL_VDD



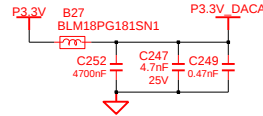
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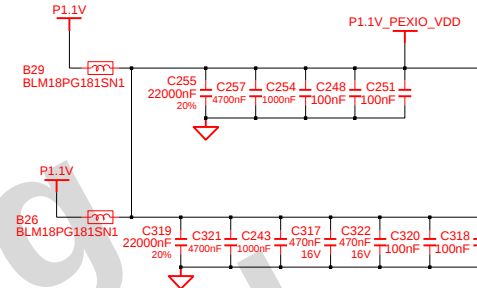
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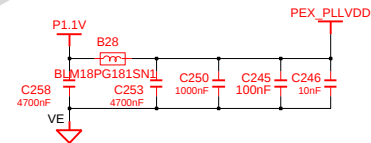
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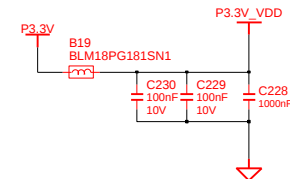
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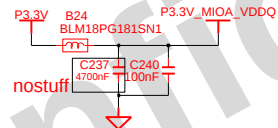
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3.3V_VDD



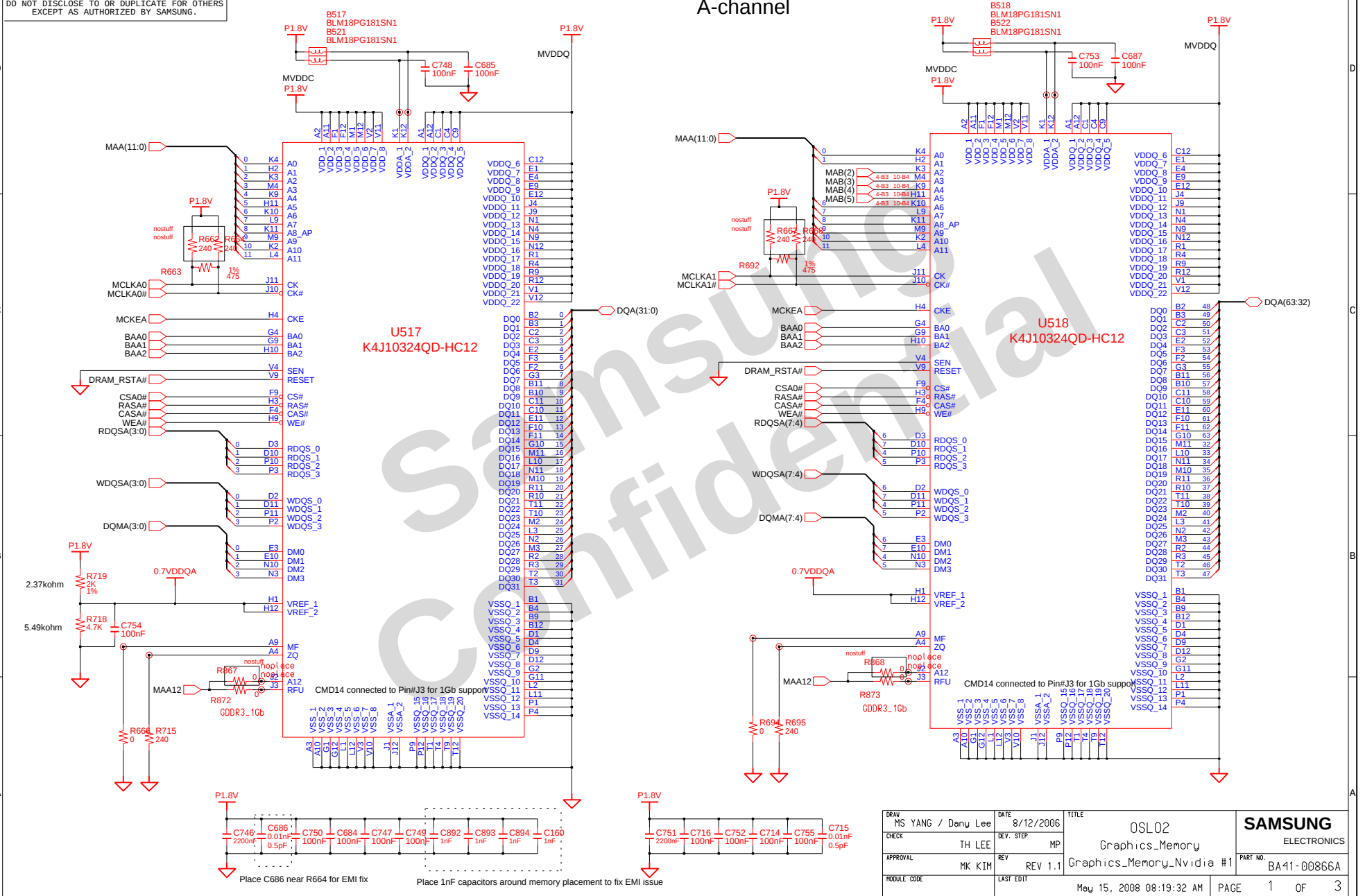
MIOA/B_VDDQ



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APPROVAL	MK KIM	REV	REV 1.1		NB9X POWER RAIL	
MODULE CODE		LAST EDIT				
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A-channel

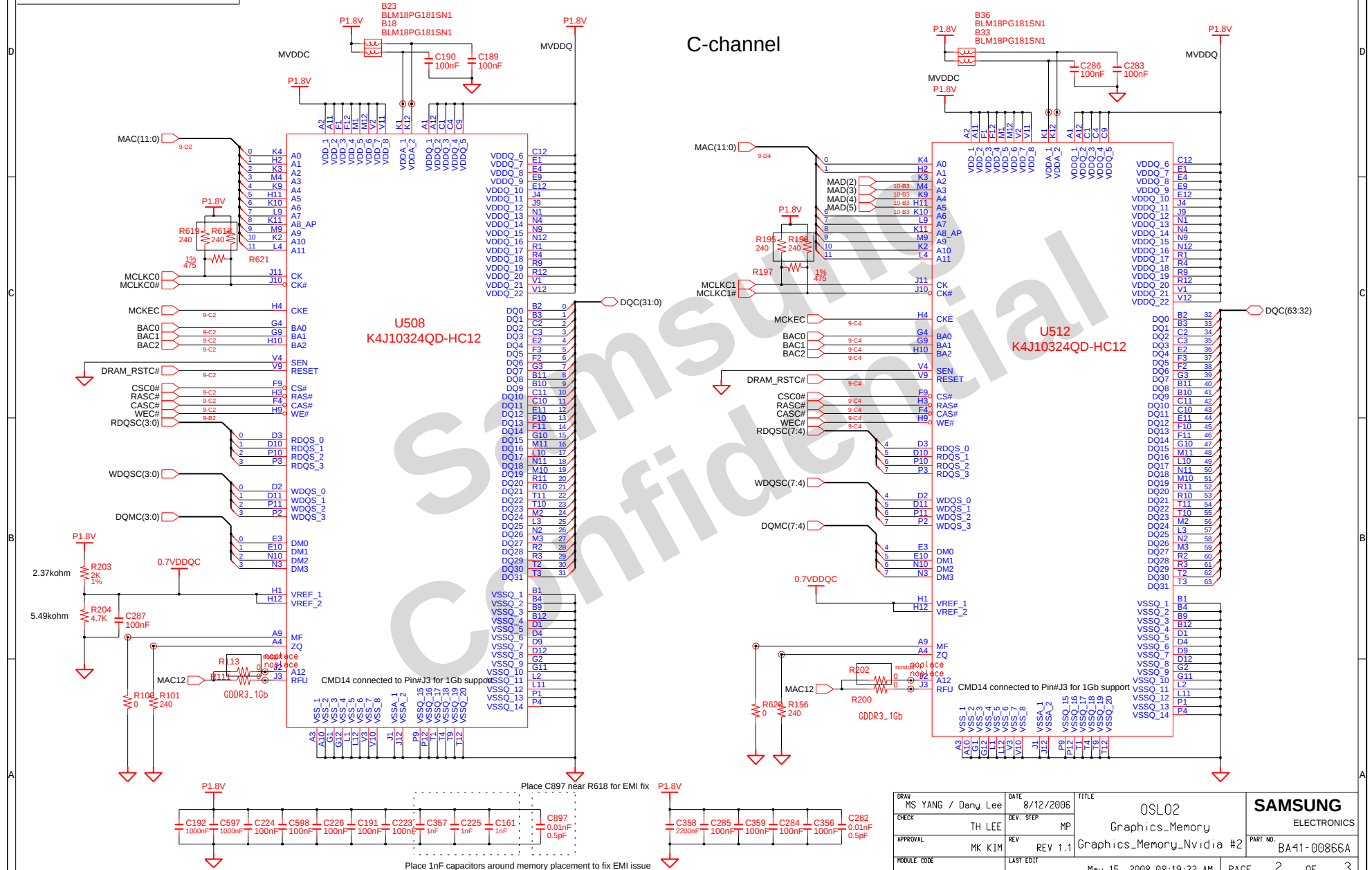


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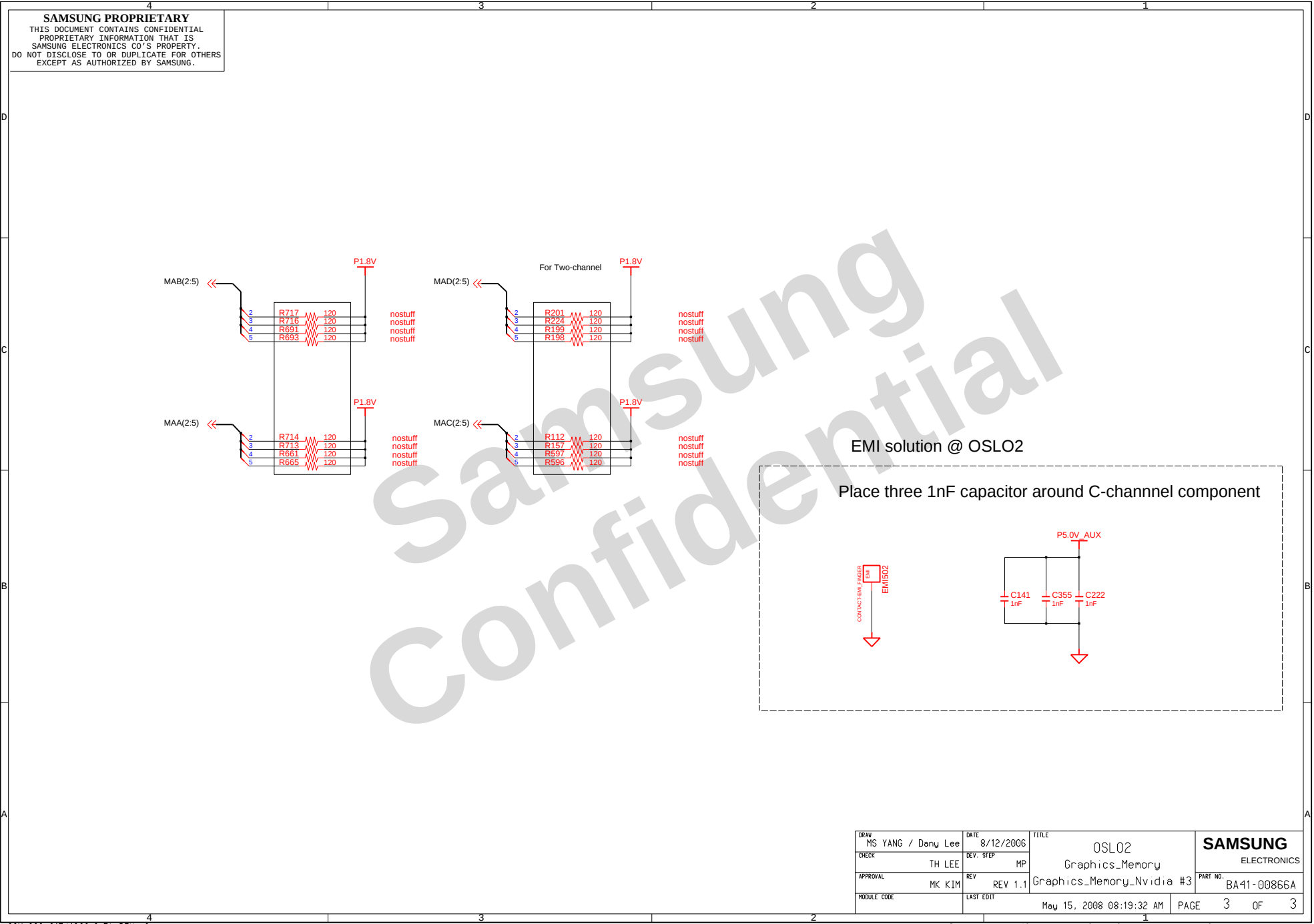
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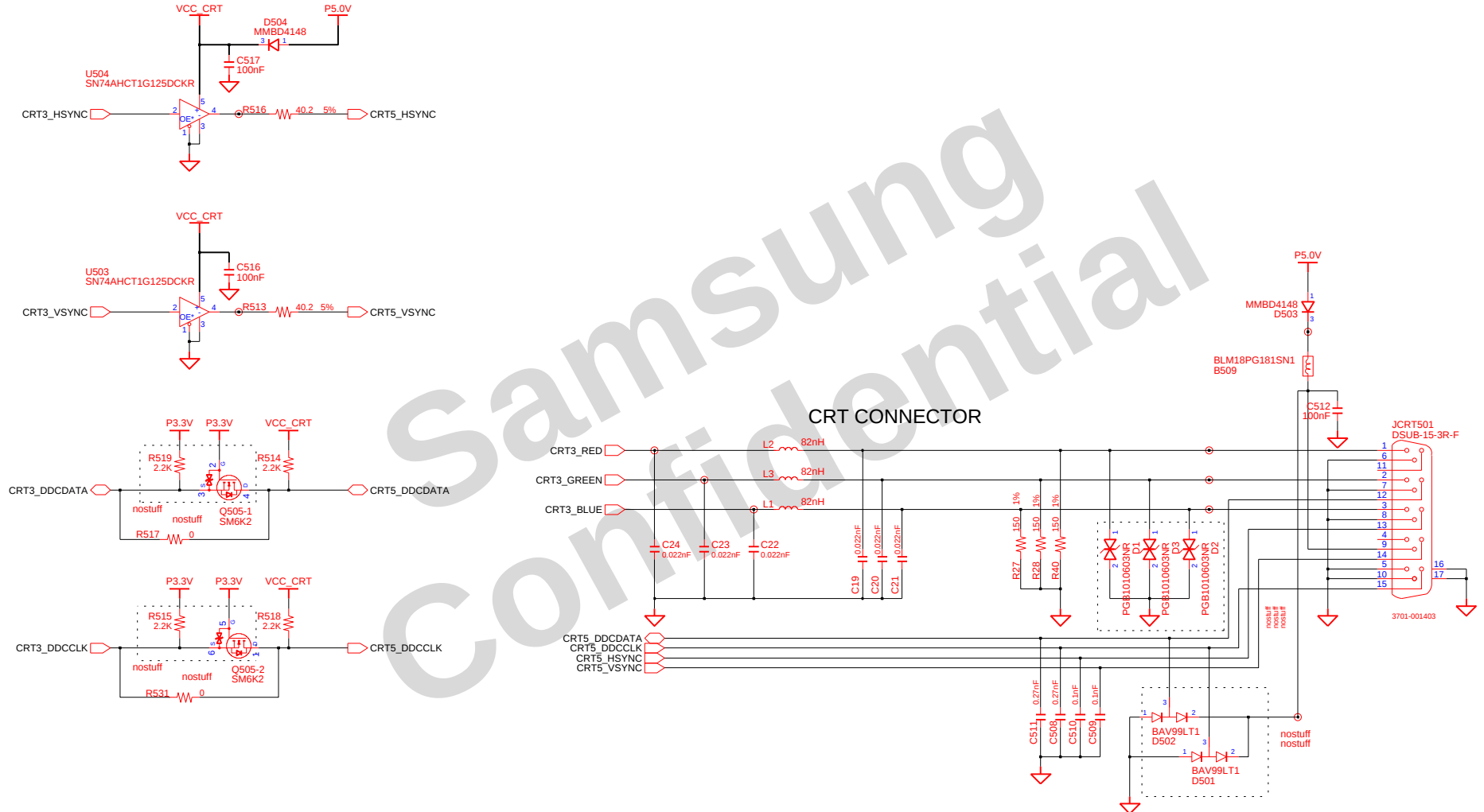


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DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 Interface_Circuit Graphics_IF_CRT	SAMSUNG ELECTRONICS PART NO. BA11-00866A
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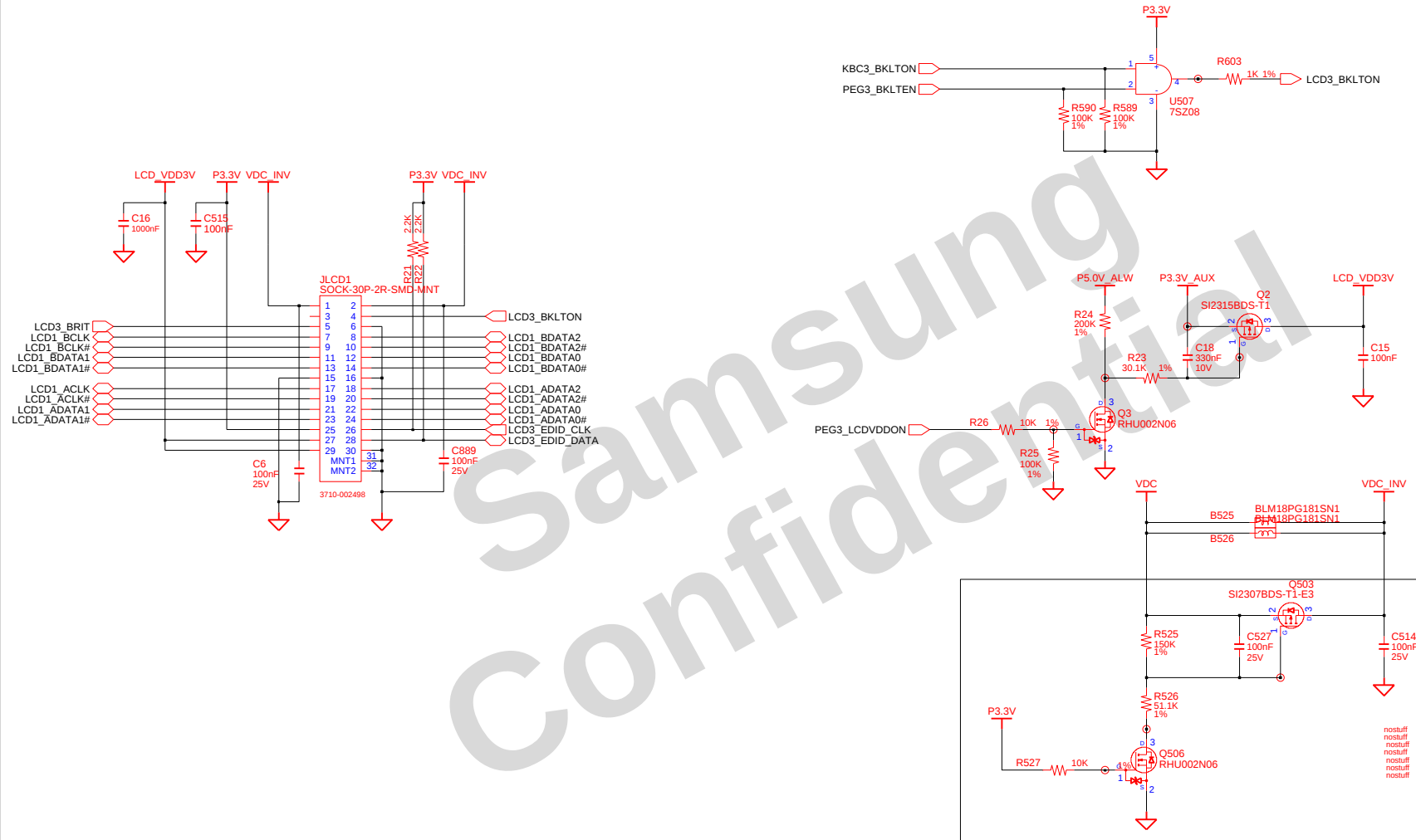
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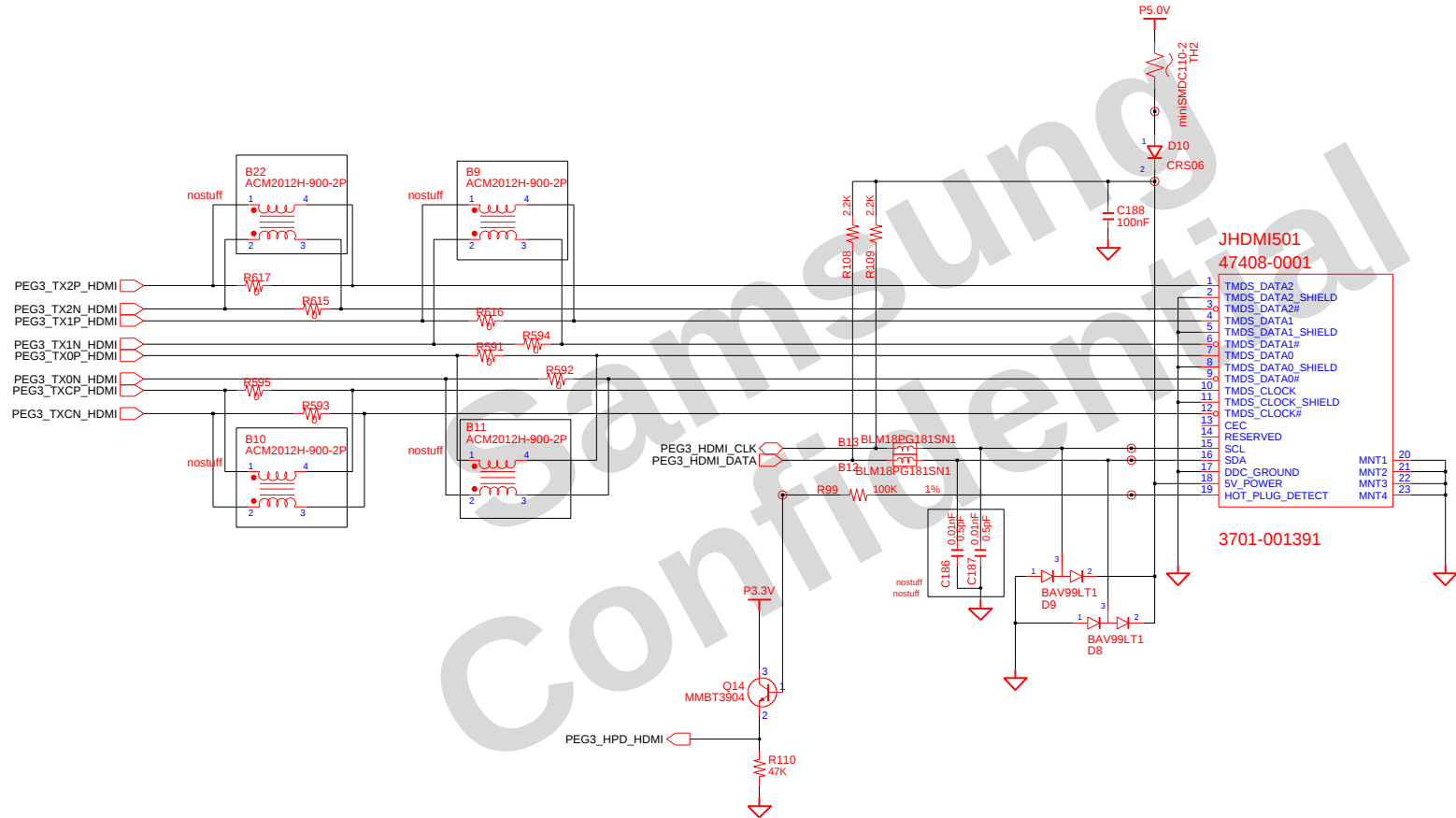


DRAW MS YANG / Dany Lee	DATE 8/17/2007	TITLE OSL02 UNDEF INED	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP		
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT		

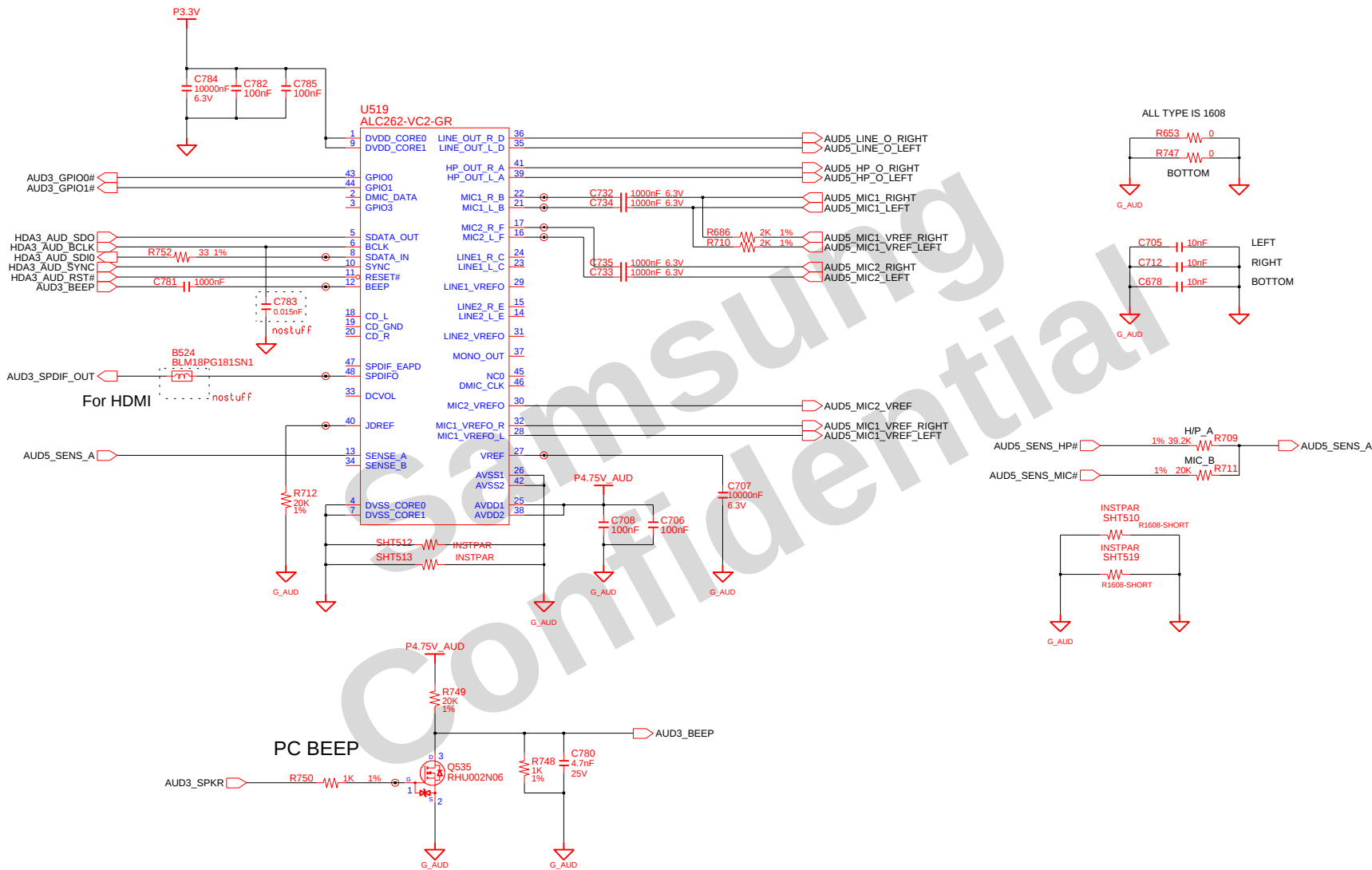
May 15, 2008 08:19:32 AM PAGE 12 of 12

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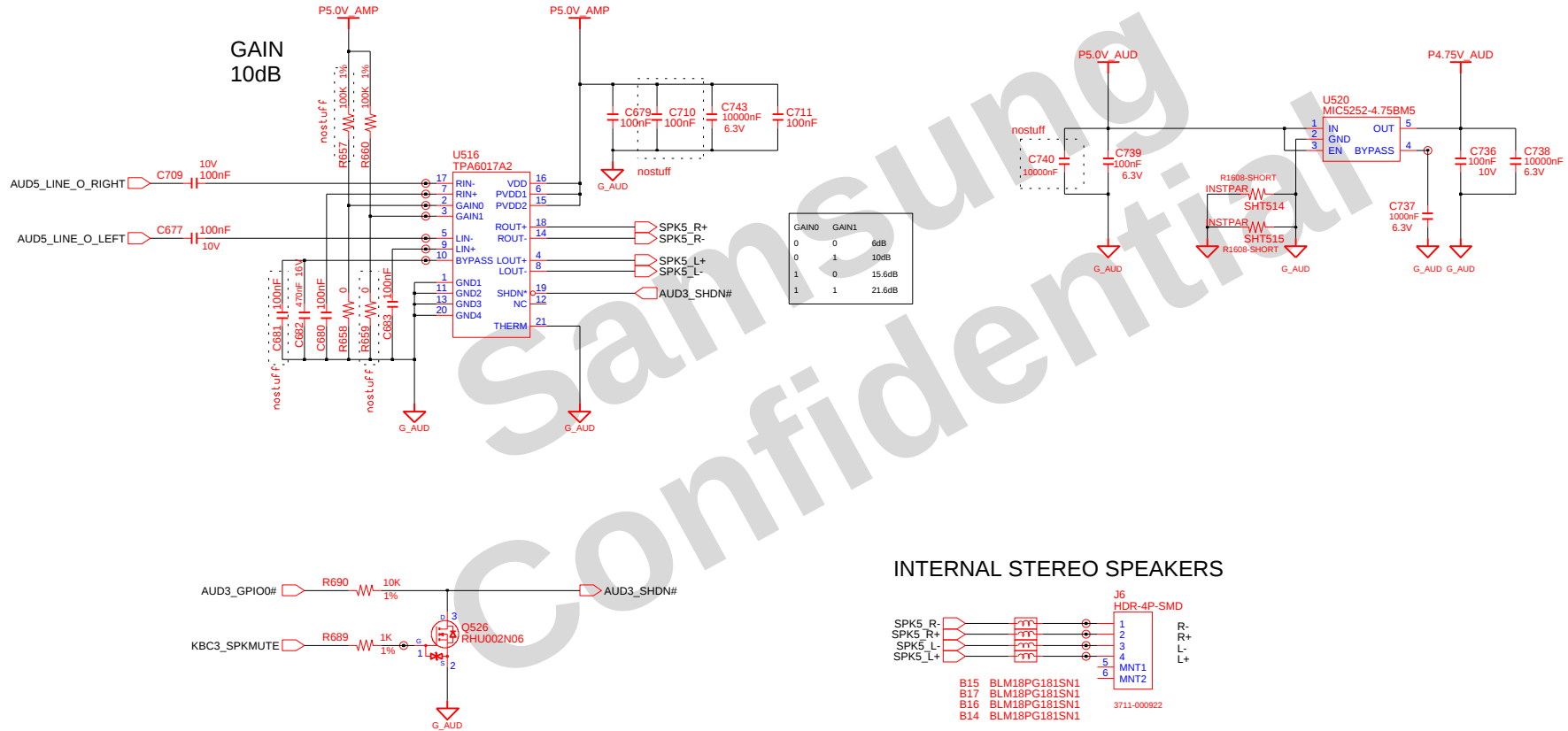
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APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT		
May 15, 2008 08:19:32 AM			PAGE 13 of 13



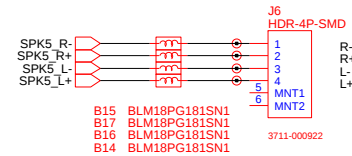
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CHECK TH LEE	DEV. STEP MP	HDA_Codec_Alc262	
APPROVAL MK KIM	REV REV 1.1	HDA_Codec_Alc262 #1	
MODULE CODE undefined	LAST EDIT		
May 15, 2008 08:19:32 AM		PAGE 1 OF 5	

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INTERNAL STEREO SPEAKERS

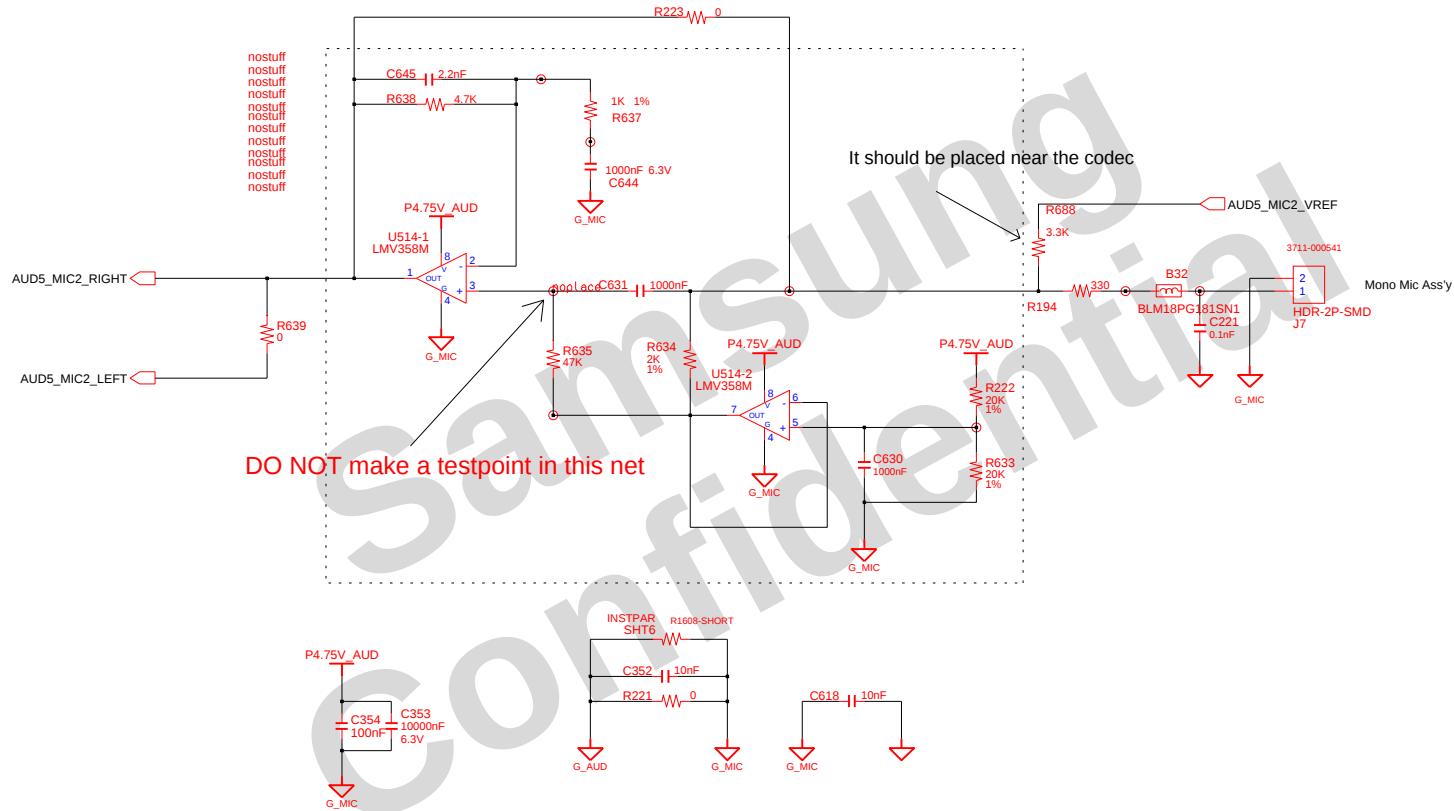


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APPROVAL MK KIM	REV 1.1	HDA_Codec_Alc262 #2	
MODULE CODE	LAST EDIT		

May 15, 2008 08:19:32 AM PAGE 2 OF 5

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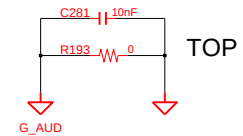
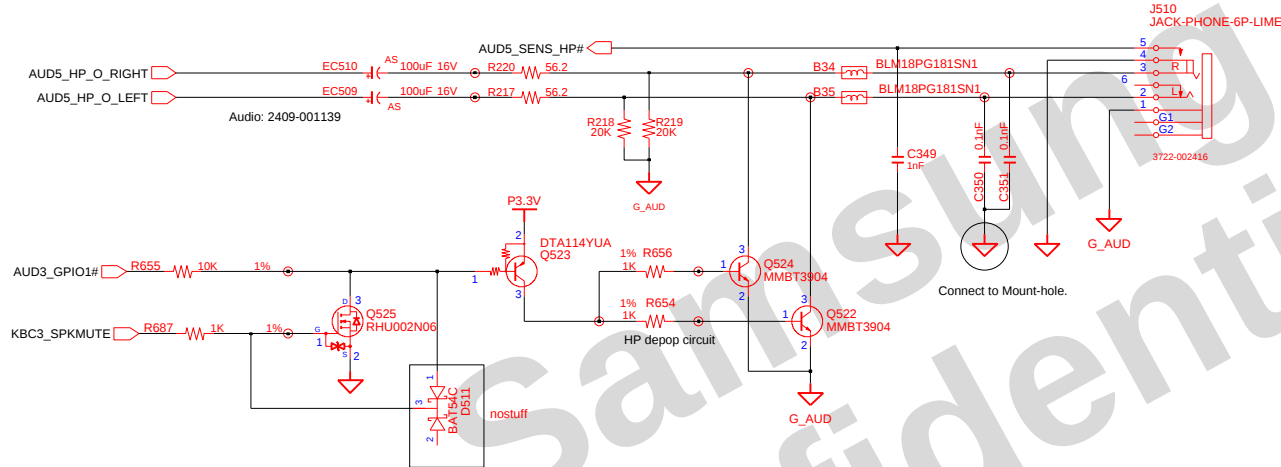
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CHECK TH LEE	DEV. STEP MP	HDA_Codec_Alc262	
APPROVAL MK KIM	REV 1.1	HDA_Codec_Alc262 #3	
MODULE CODE undefined	LAST EDIT		

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HEADPHONE



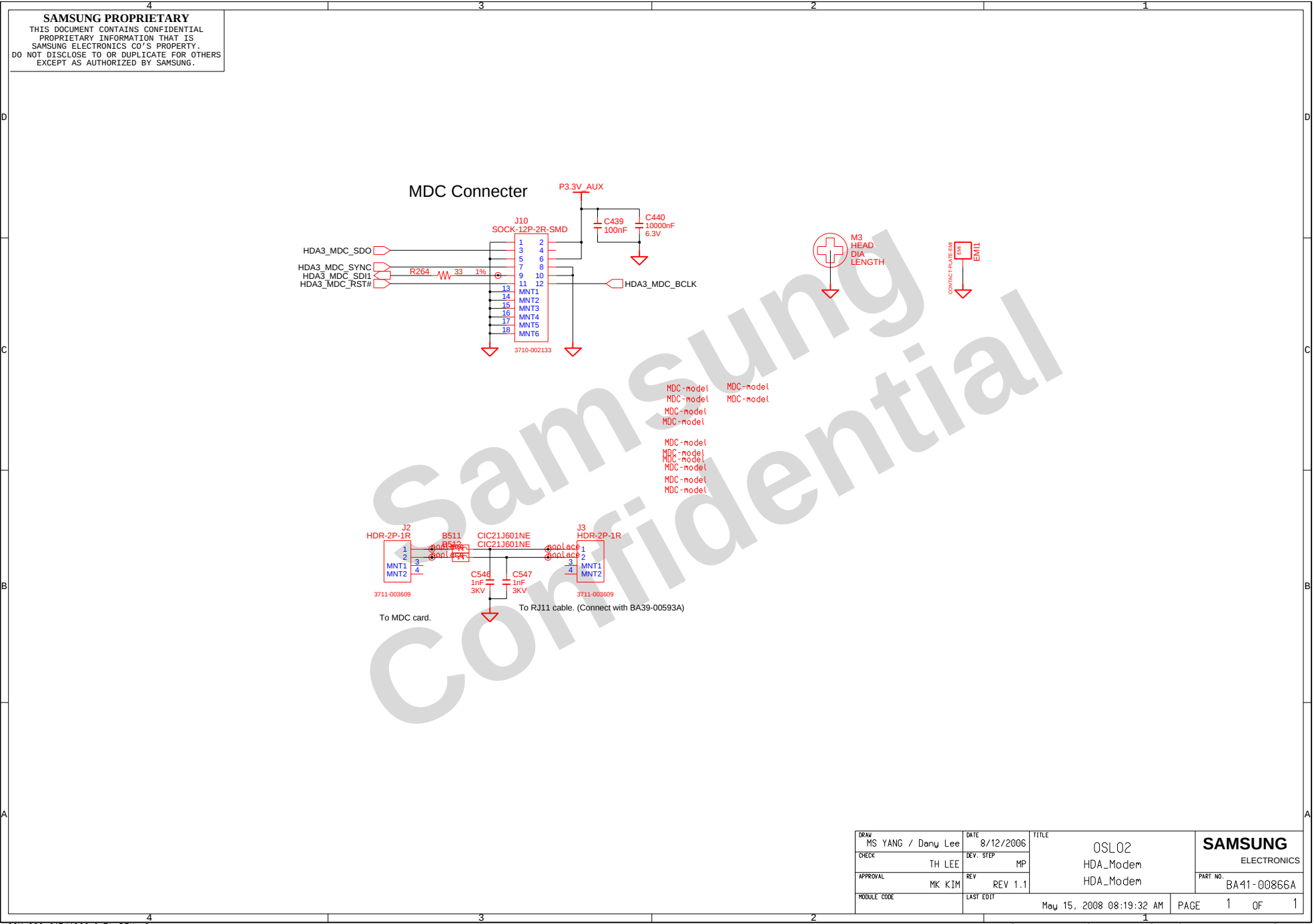
The traces led to Audio Jacks have the width over 10mil

DRW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP	HDA_Codec_Alc262	
APPROVAL MK KIM	REV REV 1.1	HDA_Codec_Alc262 #4	
MODULE CODE	LAST EDIT		
May 15, 2008 08:19:32 AM			PAGE 4 OF 5

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The schematic shows the power management circuitry for the KBC3_PWRON_INV# signal. It includes a dashed box containing the EDC653N Q637, which is connected to various power rails (P12.0V_ALW, P5.0V_AUX, P5.0V_AUD) and ground. The circuit also features several capacitors (C786, C787, C741, C742, C744, C742) and resistors (R753, INSTPAR SHT516, INSTPAR SHT517). The output of the circuit is connected to the KBC3_PWRON_INV# pin.

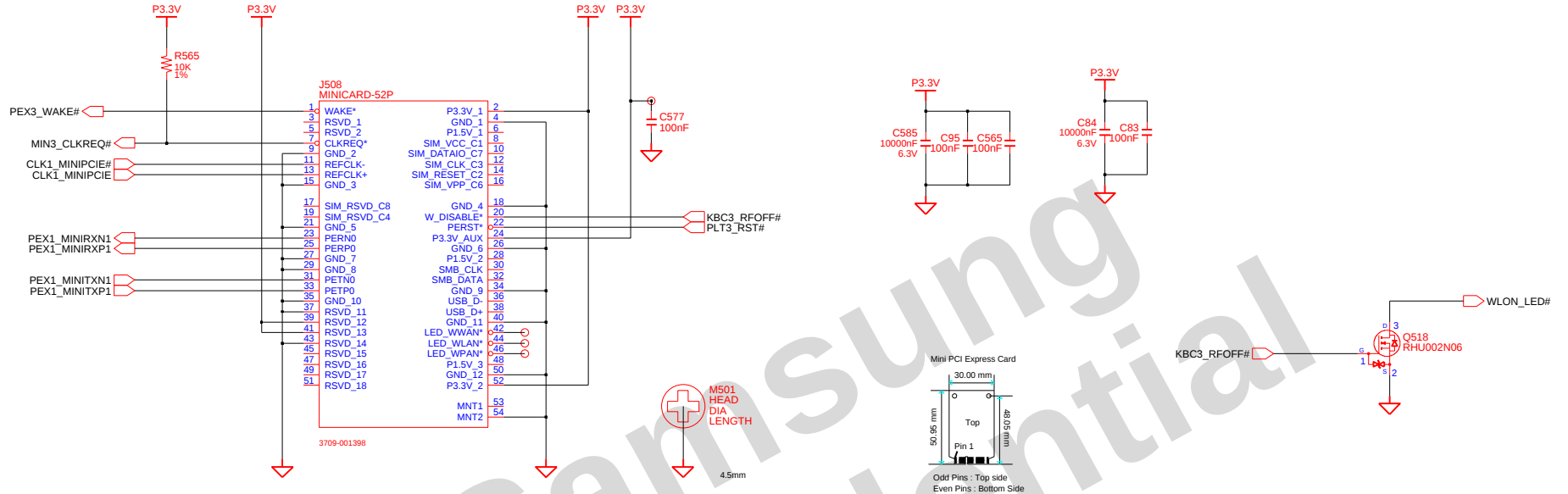
DSN MS YANG / Dany Lee		DATE 8/12/2006		TITLE OSLO2 HDA_Codec_A1c262 HDA_Codec_A1c262 #5			
CHECK TH LEE		DEV. STEP MP					
APPROVAL MK KIM		REV REV 1.1		PART NO.		BA41-00866A	
MODULE CODE undef ined		LAST EDIT May 15, 2008 08:19:32 AM		PAGE		5 OF 5	



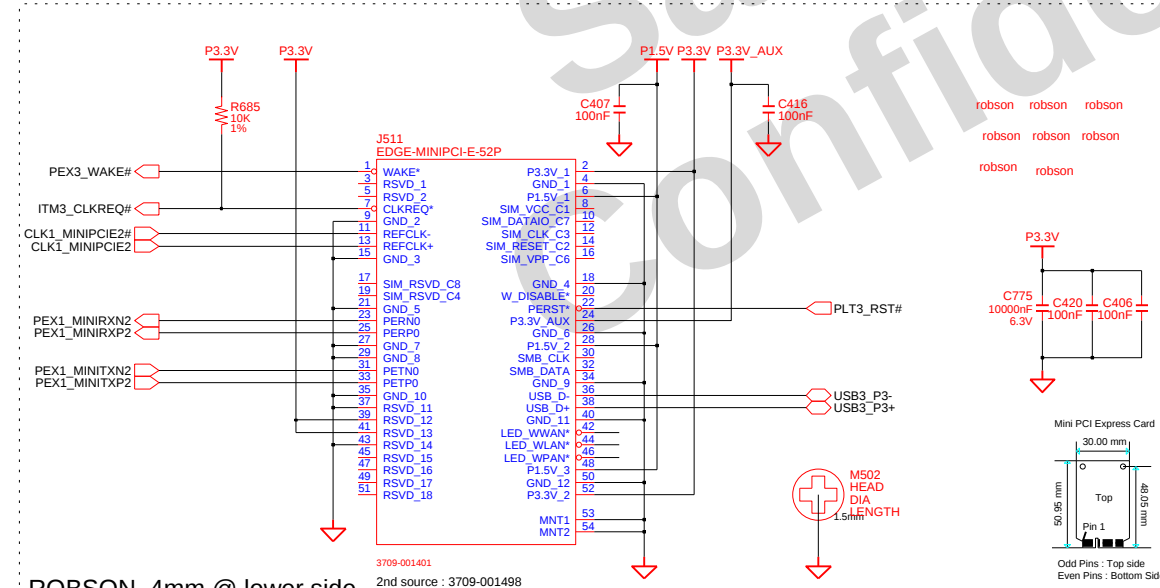
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WLAN, 7mm @ Upper side



To fix Shirley Peak EMI issue
 Place it at the old rubber area



ROBSON, 4mm @ lower side

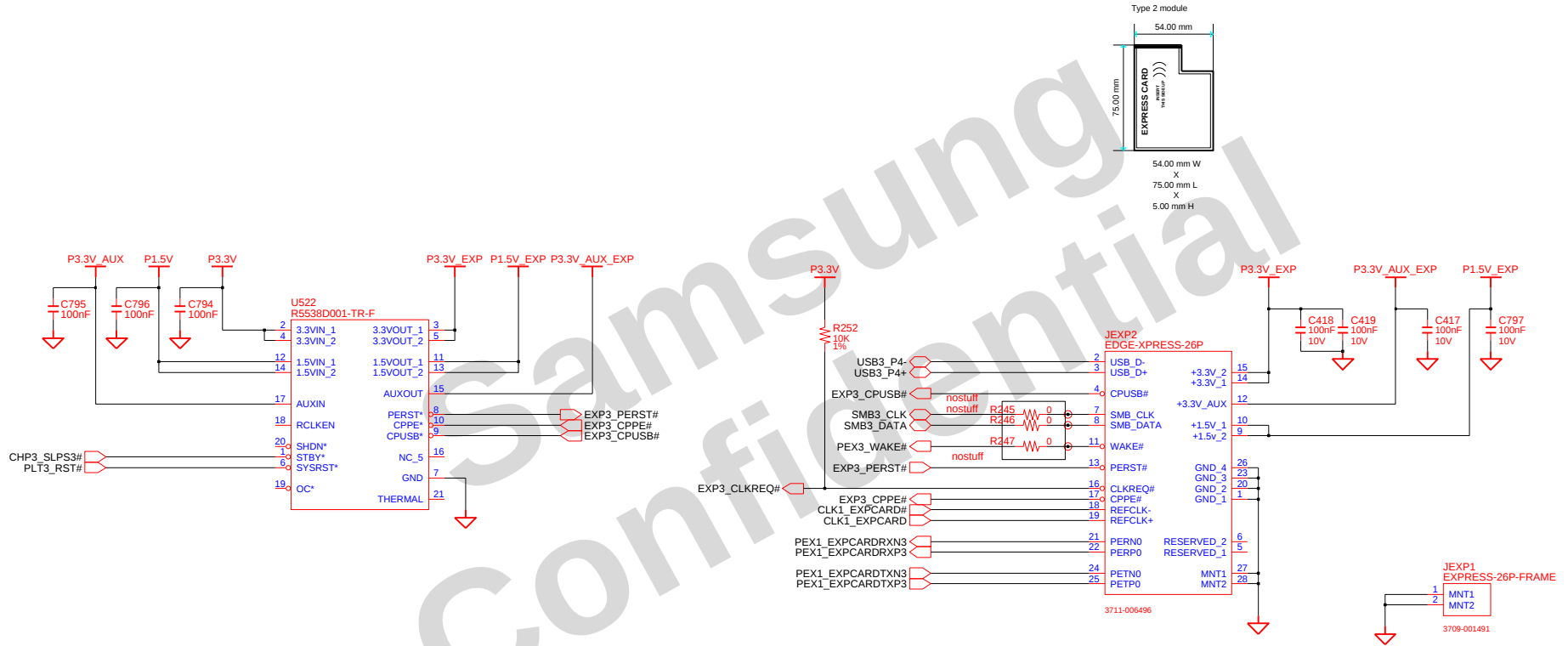
2nd source : 3709-001498

DRAW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP		PCIE_Minicard_Slot	
APPROVAL	MK KIM	REV	REV 1.1		PCIE_Minicard_Slot	PART NO. BA41-00866A
MODULE CODE	undefined	LAST EDIT				

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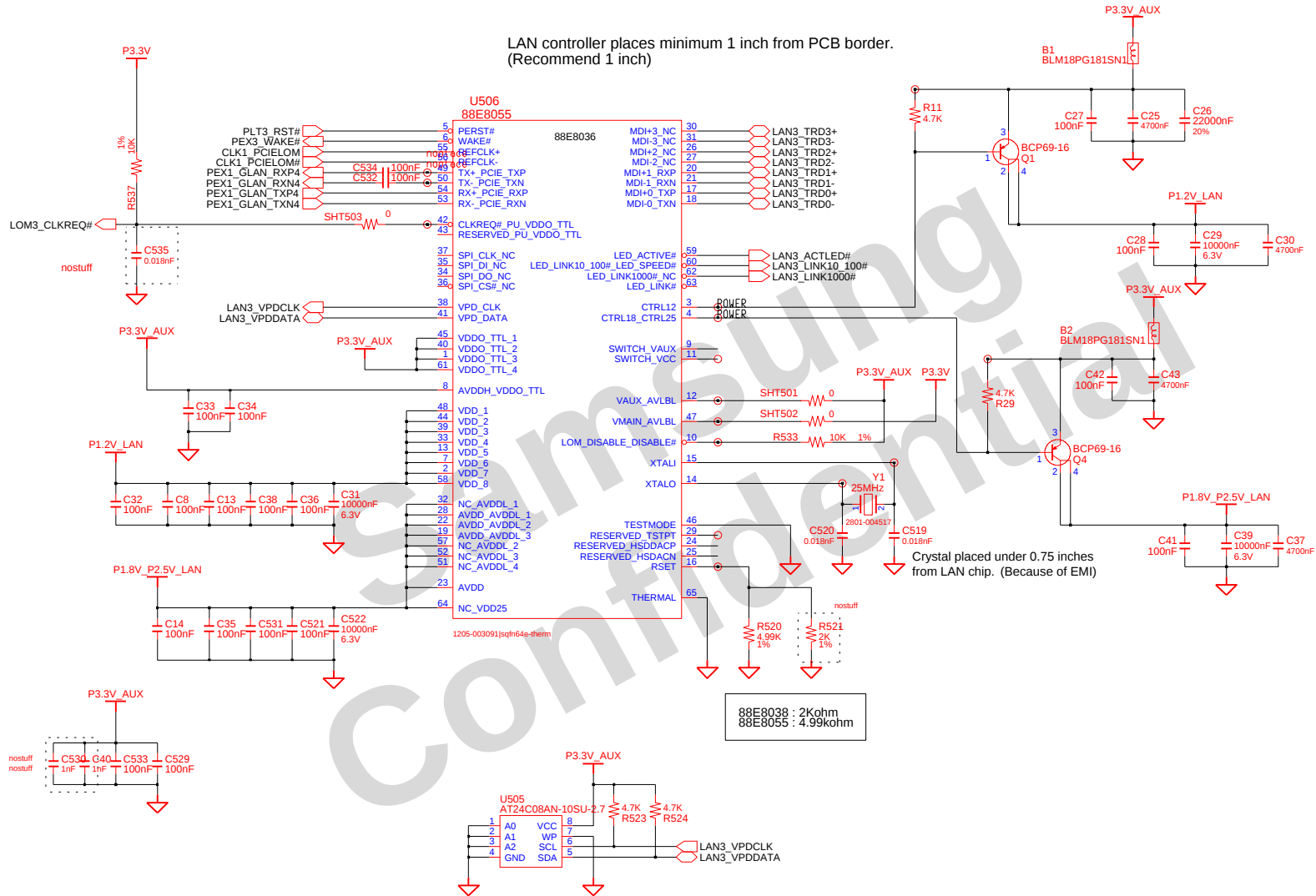


DRW MS YANG / Dany Lee	DATE	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP			
APPROVAL MK KIM	REV REV 1.1			PART NO. BA11-00866A
MODULE CODE undefined	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	OF

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LAN controller places minimum 1 inch from PCB border.
 (Recommend 1 inch)

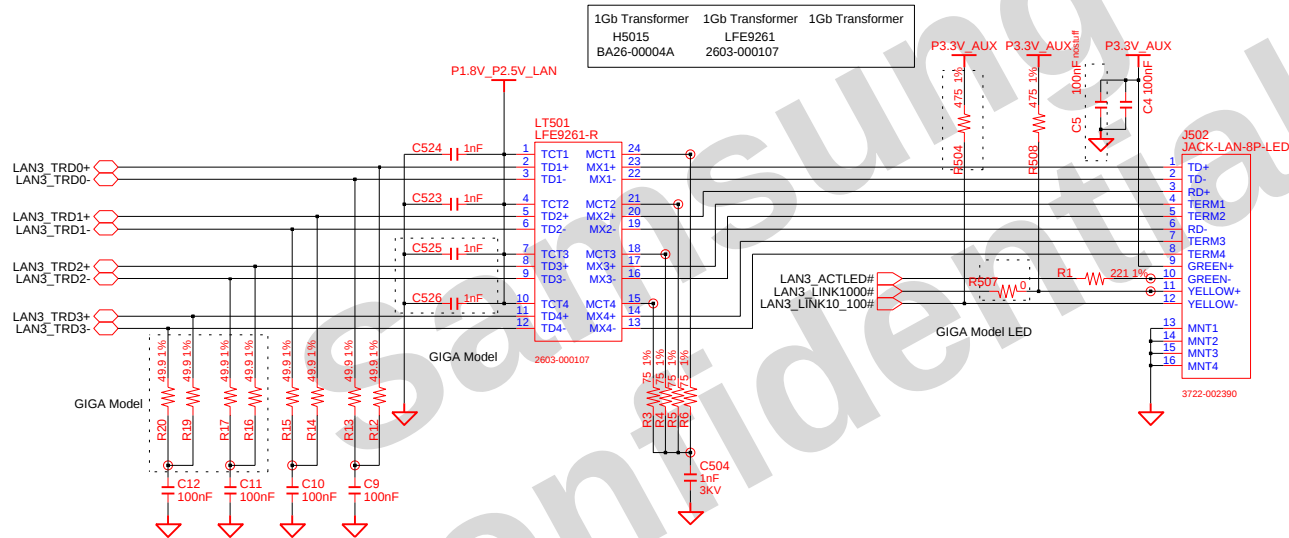


DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	SAMSUNG ELECTRONICS PART NO. BA41-00866A
CHECK TH LEE	DEV. STEP MP	LAN_Marvell_8055	
APPROVAL MK KIM	REV REV 1.1	LAN_Marvell_8055	
MODULE CODE	LAST EDIT		
May 15, 2008 08:19:32 AM			PAGE 1 OF 2

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The distance between LAN controller
and transformer is designed to extend less than two inches.



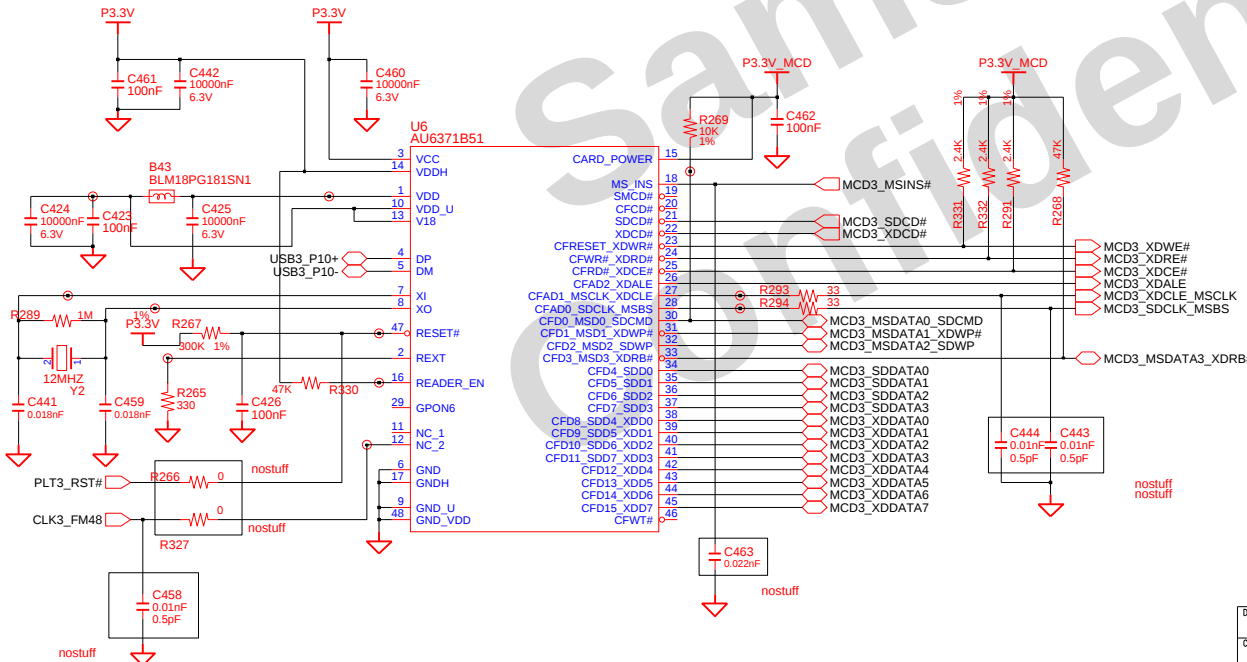
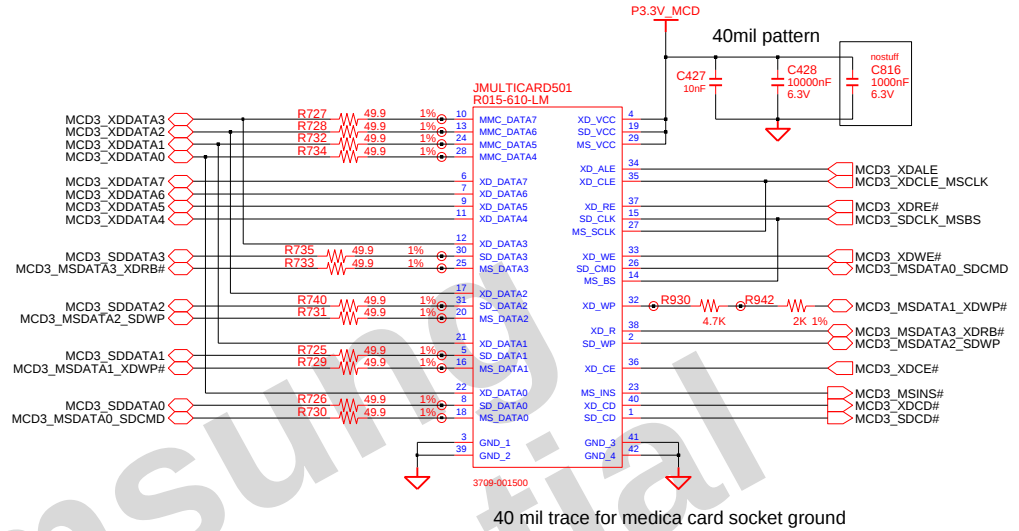
Place near to the Marvell chip.

DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP	LAN_Marvell_8055	
APPROVAL MK KIM	REV REV 1.1	LAN_Marvell_8055	
MODULE CODE	LAST EDIT		
May 15, 2008 08:19:32 AM			PAGE 2 OF 2

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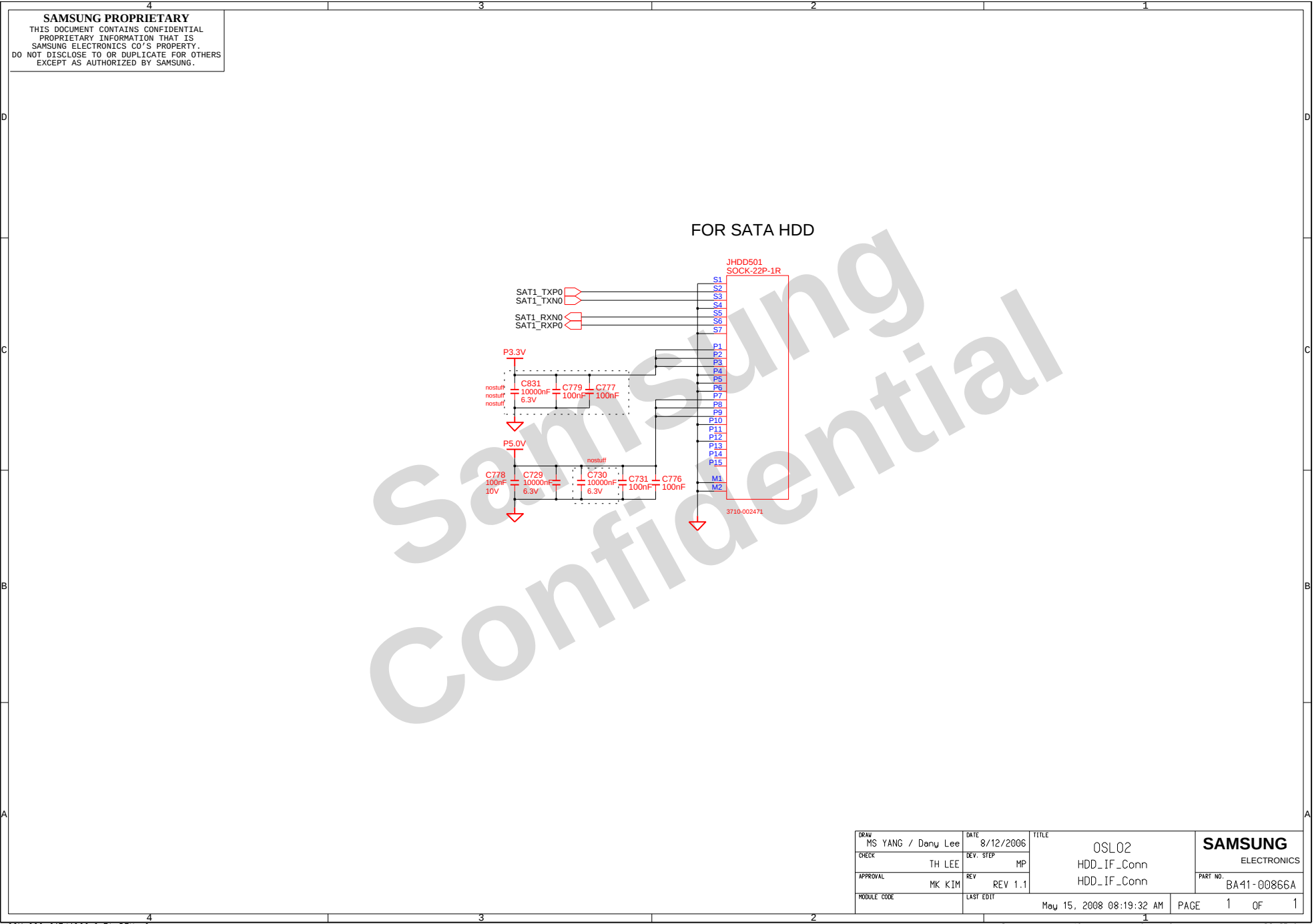
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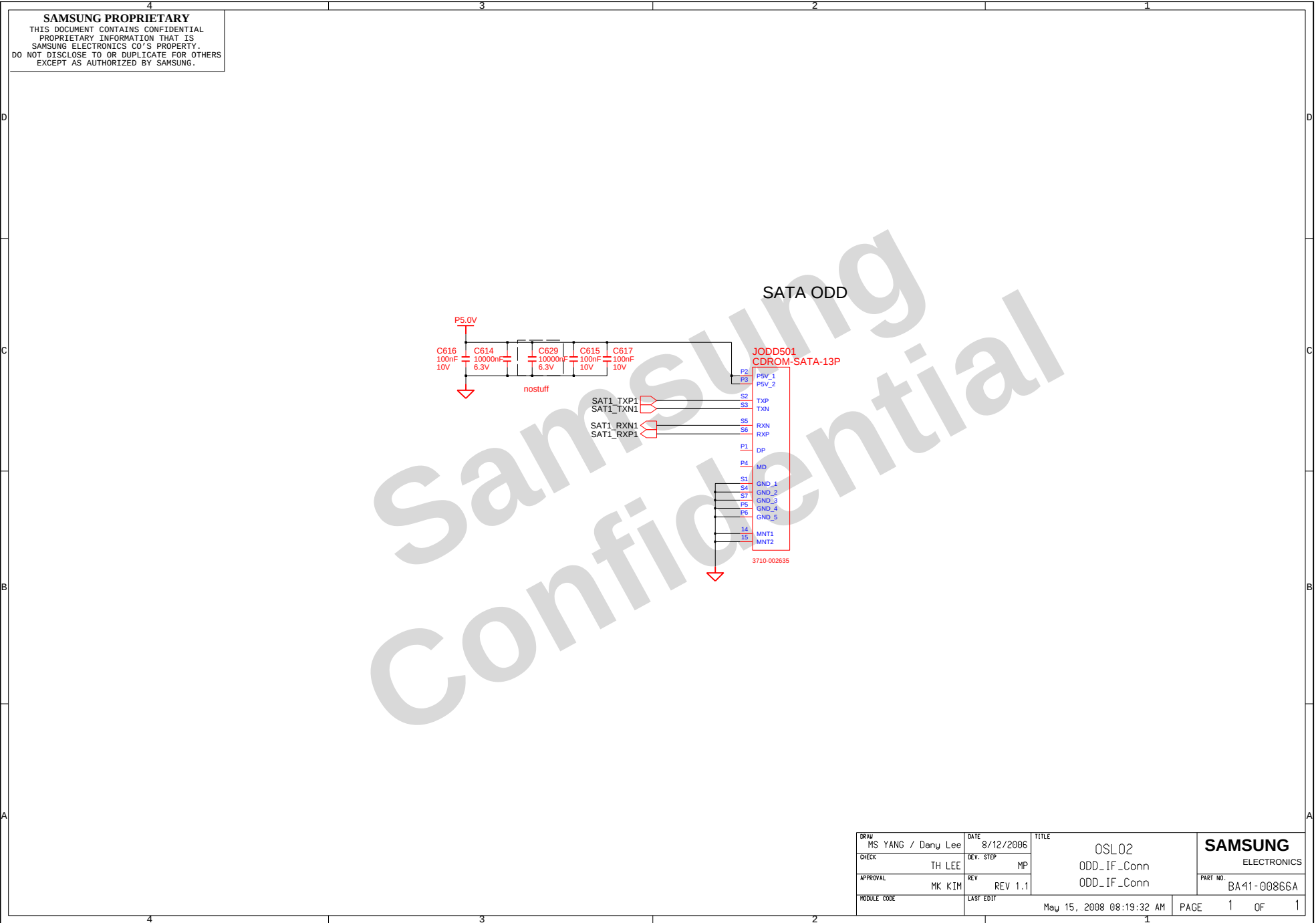
P3.3V_MCD distance between Controller and socket should be less than 2 inches



DRAW	MS YANG / Dany Lee	DATE	8/17/2007	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP		UNDEF INED	
APPROVAL	MK KIM	REV	REV 1.1			PART NO. BA11-00866A
MODULE CODE		LAST EDIT				

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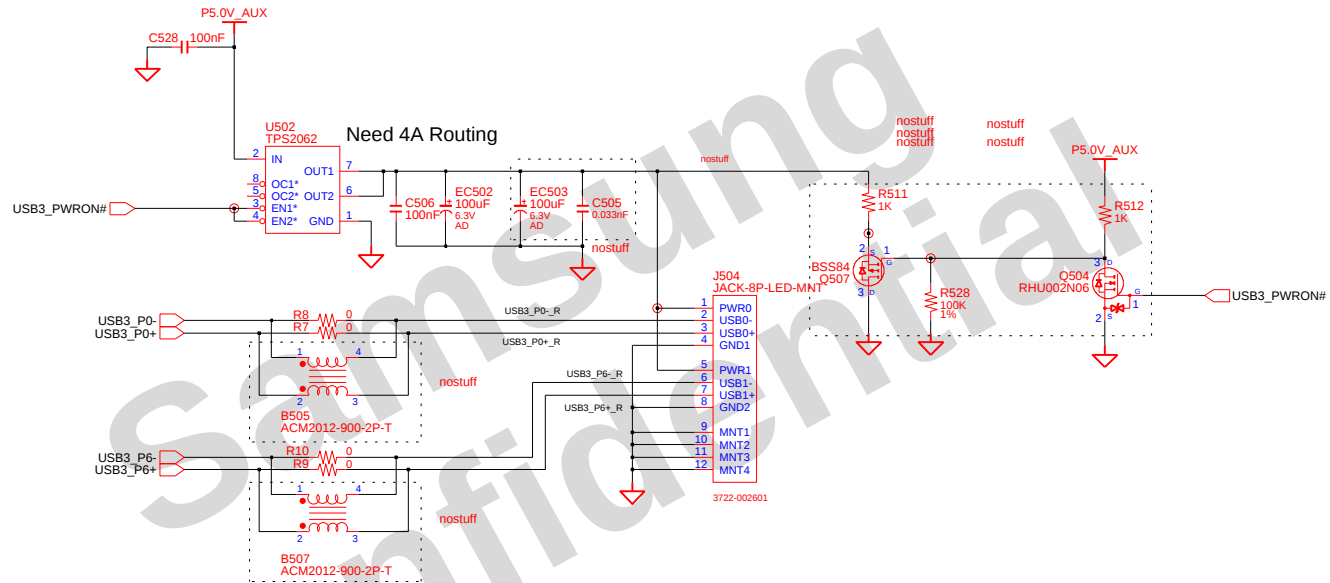




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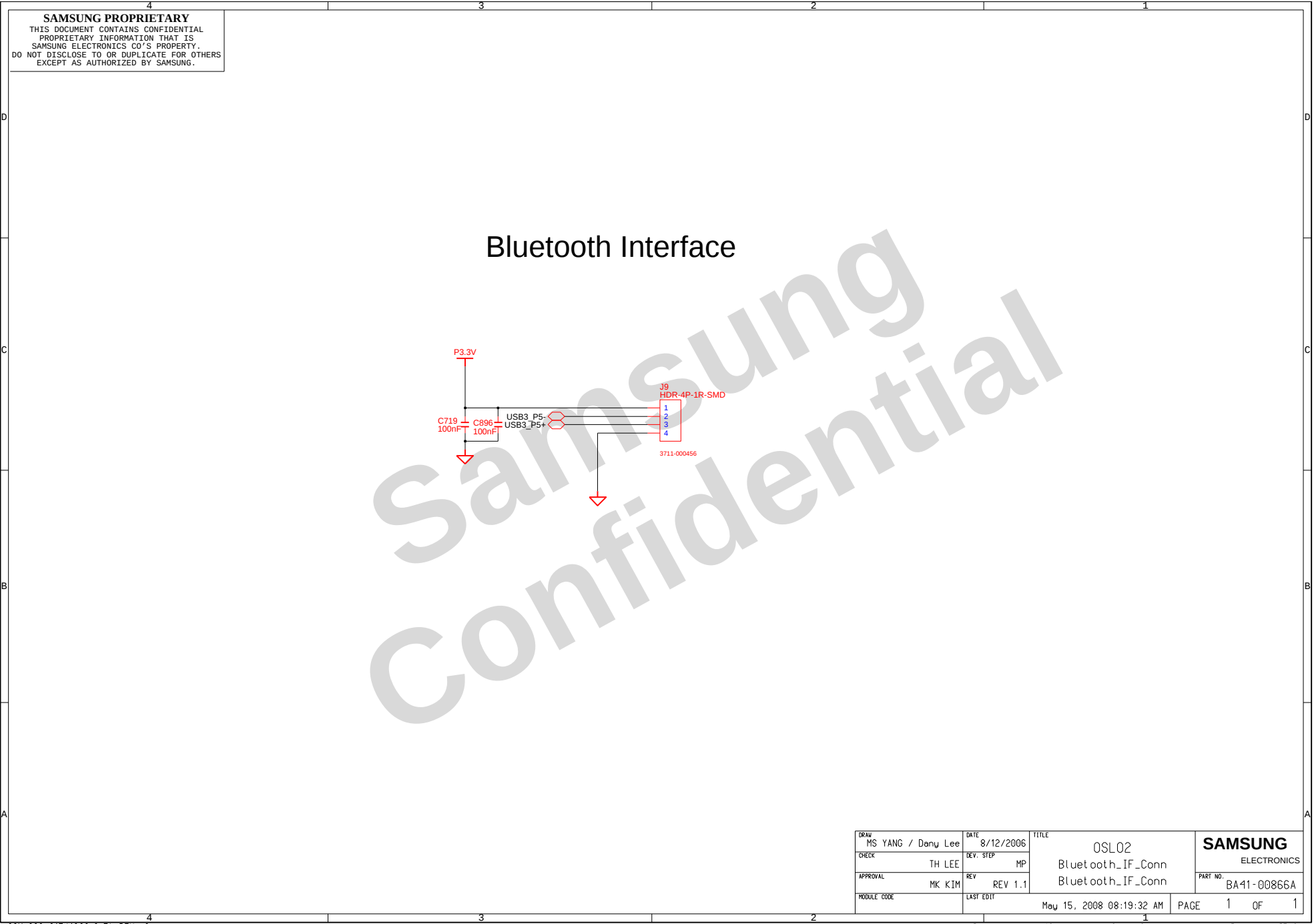
DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	SAMSUNG ELECTRONICS
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APPROVAL MK KIM	REV REV 1.1	ODD_IF_Conn	PART NO. BA41-00866A
MODULE CODE	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 1 OF 1

2 PORT USB CONNECTOR



DRAW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP		USB_2Port	
APPROVAL	MK KIM	REV	REV 1.1		USB_2Port	PART NO. BA11-00866A
MODULE CODE		LAST EDIT				

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USB3_P8
USB2_P8+

R530
R529

0
0

1
2
3
4

1
2
3
4

PS10V

C17 100nF
C7 100nF

J1 HDR-4P-1R-SMD

3711-000456

B510
ACM2012-900-2P-T

DRW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02		
CHECK	TH LEE	REV. STEP	MP		Camera_IF_Conn		
APPROVAL	MK KIM	REV	REV 1.1		Camera_IF_Conn	PART NO.	BA41-00866A
MODULE CODE		LAST EDIT		May 15, 2008 08:19:32 AM	PAGE	1	OF 1

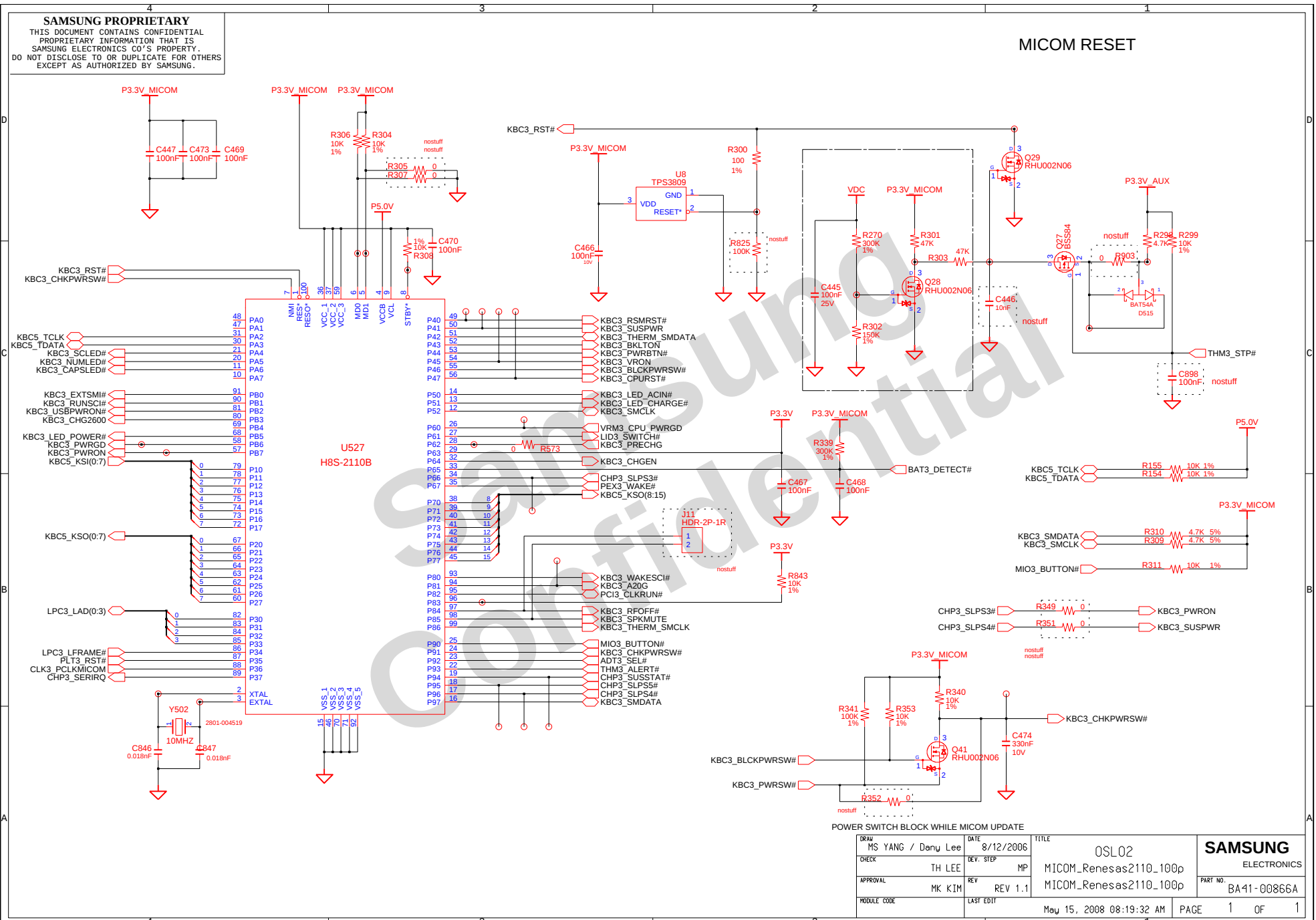


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MICOM RESET

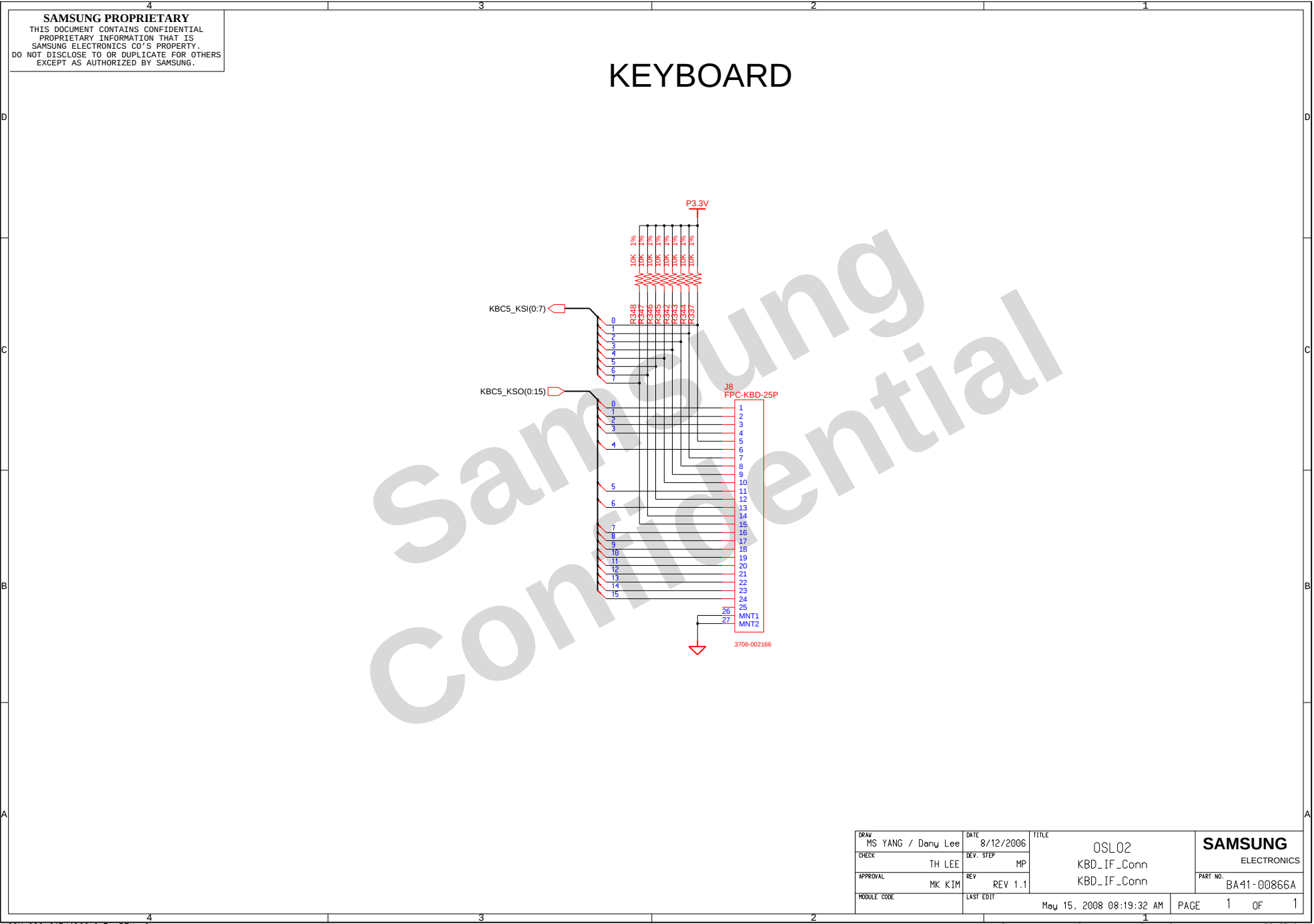
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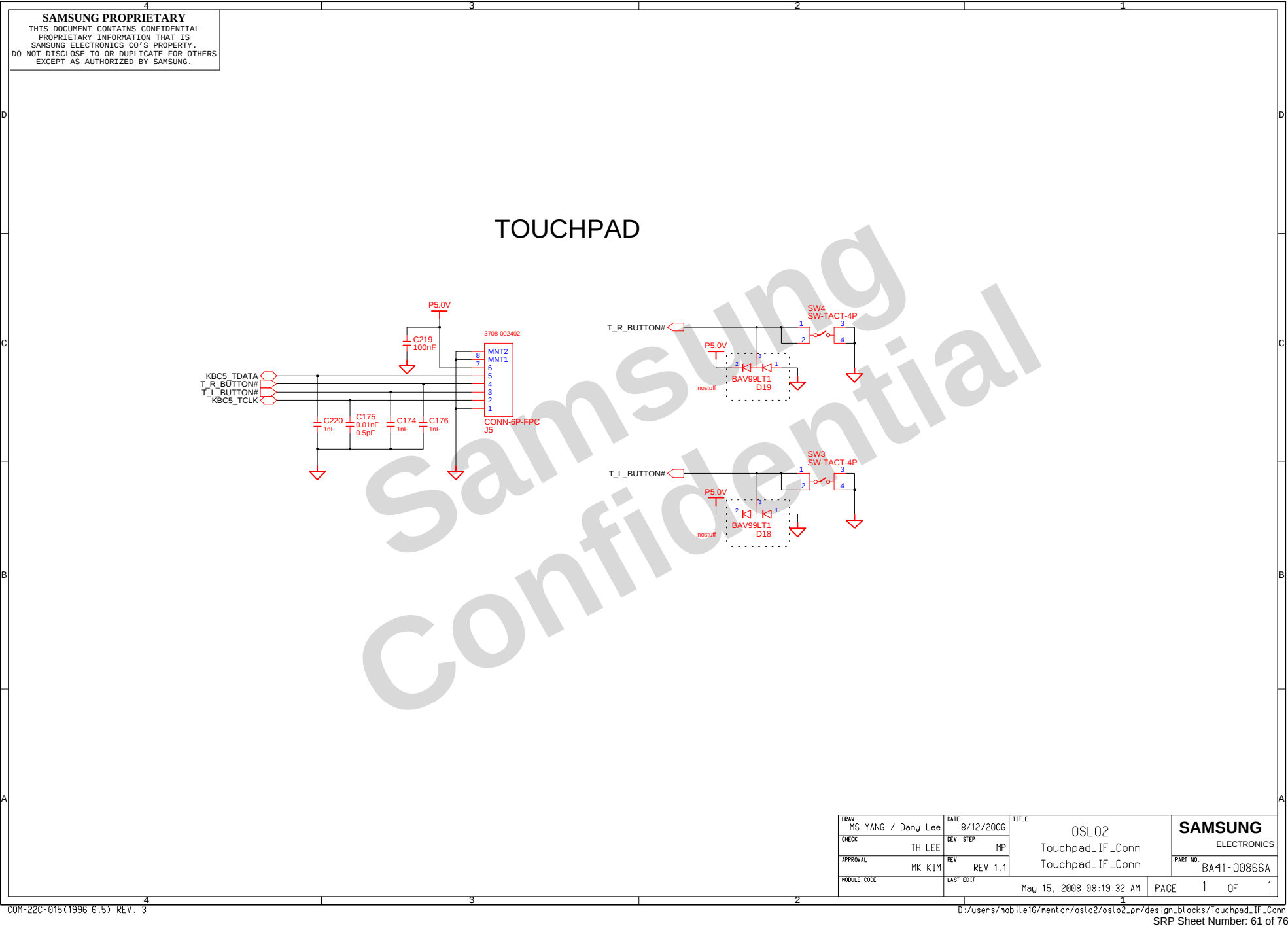
MICOM RESET



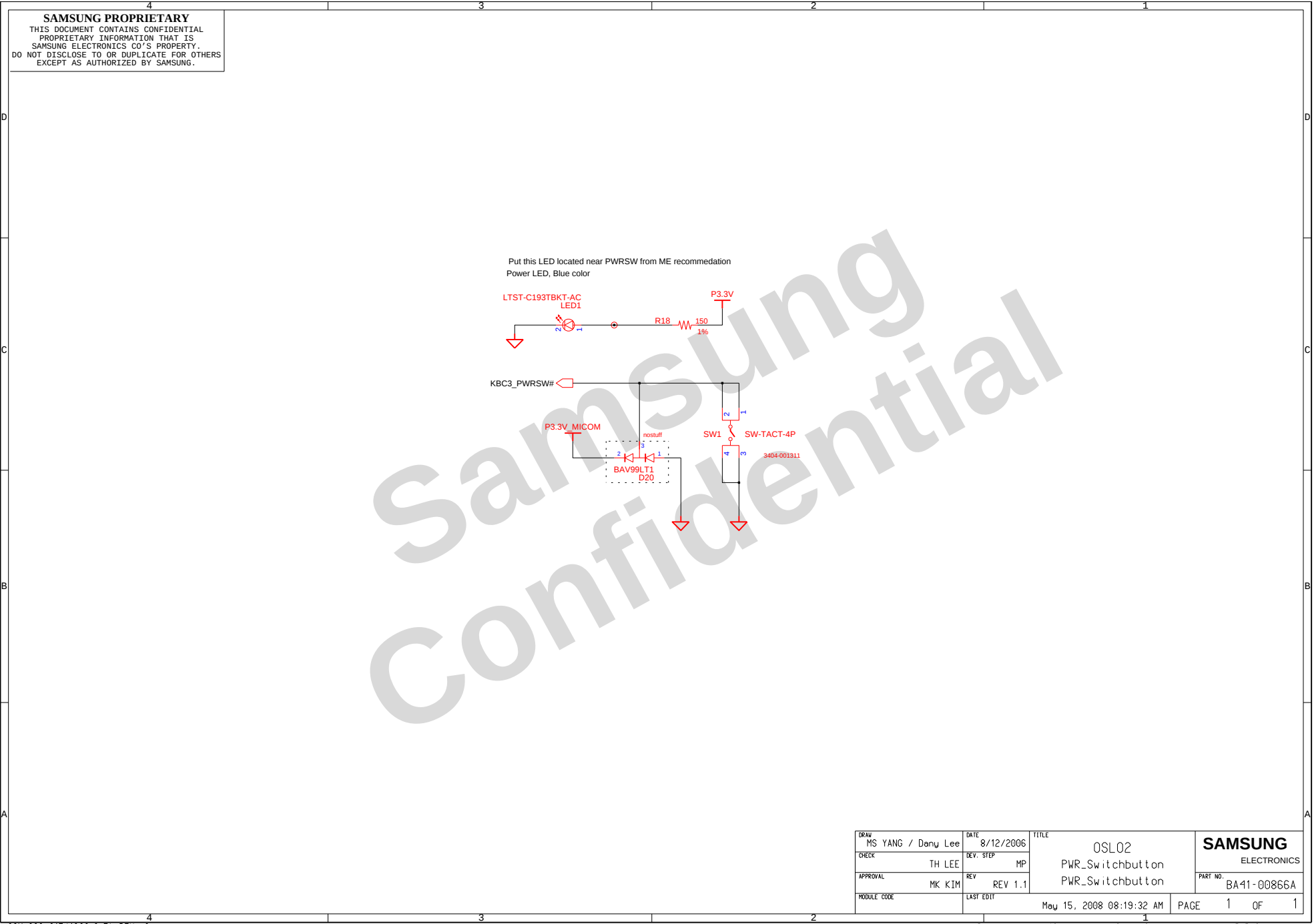
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MICOM RESET





DRAW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS PART NO. BA41-00866A
CHECK	TH LEE	DEV. STEP	MP	Touchpad_IF_Conn		
APPROVAL	MK KIM	REV	REV 1.1	Touchpad_IF_Conn		
MODULE CODE		LAST EDIT				
				May 15, 2008 08:19:32 AM	PAGE	1 OF 1



DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 PWR_Switchbutton PWR_Switchbutton	SAMSUNG ELECTRONICS PART NO. BA41-00866A
CHECK TH LEE	DEV. STEP MP		
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

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The circuit diagram illustrates the internal wiring of the MIO_Switch component. It features several key elements:

- MIO3_BUTTON#**: A push-button switch connected to a common terminal.
- P3.3V_MICOM**: A power supply input connected to one terminal of the diode.
- BAV99LT1 D13**: A diode used for signal conditioning or protection.
- SW2**: A mechanical switch component.
- SW-TACT-4P**: A tactile switch component.

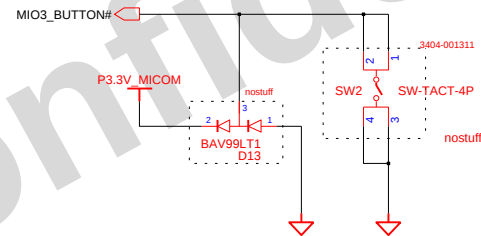
The diagram shows how these components are interconnected through various terminals and ground points, with labels like 'nostuff' indicating areas without physical components.

DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 MIO_Switch	PART NO. BA41-00866A
CHECK TH LEE	DEV. STEP MP	MIO_Switch	
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT May 15, 2008 08:19:32 AM		
		PAGE 1	OF 1

COM-22C-015(1996.6.5) REV. 3

D:/users/nobile16/nentor/oslo2/oslo2_pr/design_blocks/MIO_Switch
SRP Sheet Number: 63 of 76

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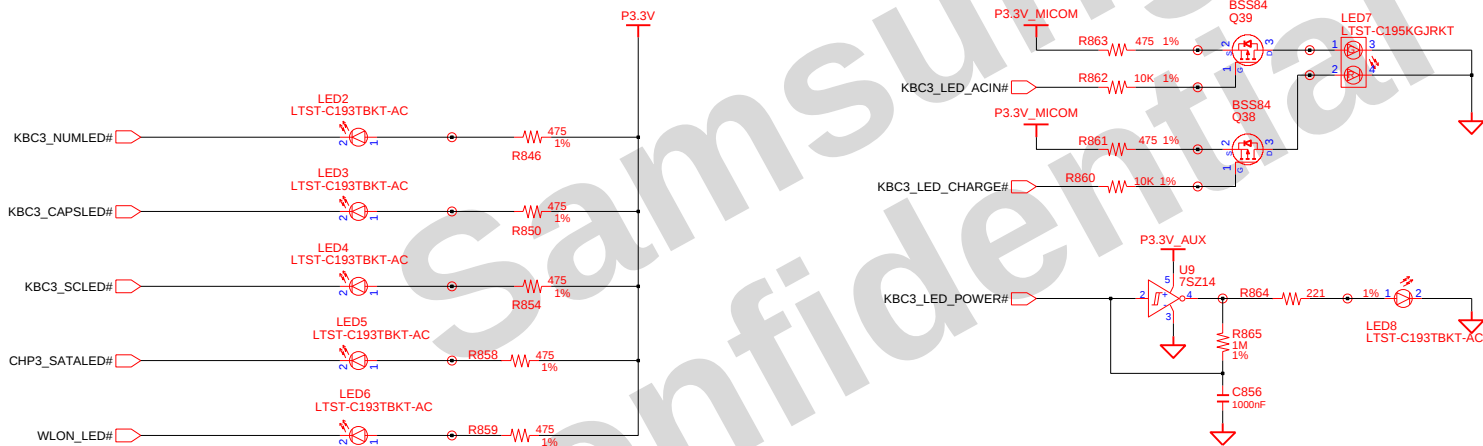


MS YANG / Dany Lee		DATE	8/12/2006		TITLE		OSLO2 MIO_Switch MIO_Switch		SAMSUNG ELECTRONICS	
CHECK	TH LEE	REV. STEP	MP							
APPROVAL	MK KIM	REV	REV 1.1						PART NO. BA41-00866A	
MODULE CODE		LAST EDIT		May 15, 2008 08:19:32 AM			PAGE	1	OF	1

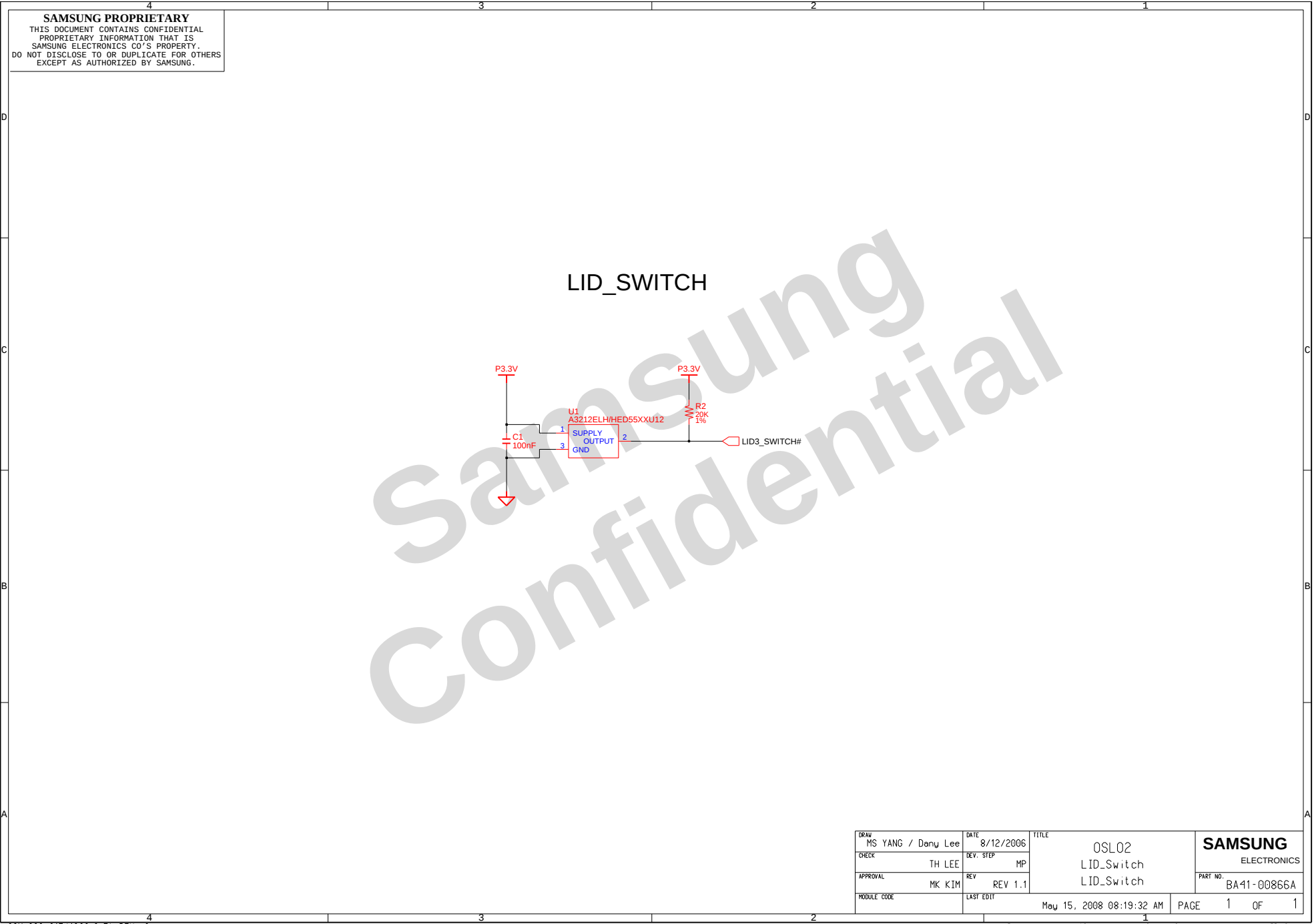
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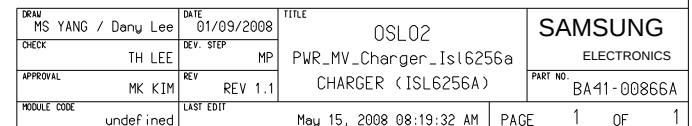
ADAPTERIN/CHARGING LED



DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 LED_Switch LED_Switch	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP		PART NO. BA41-00866A
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 1 OF 1



CHARGER & POWER MANAGEMENT

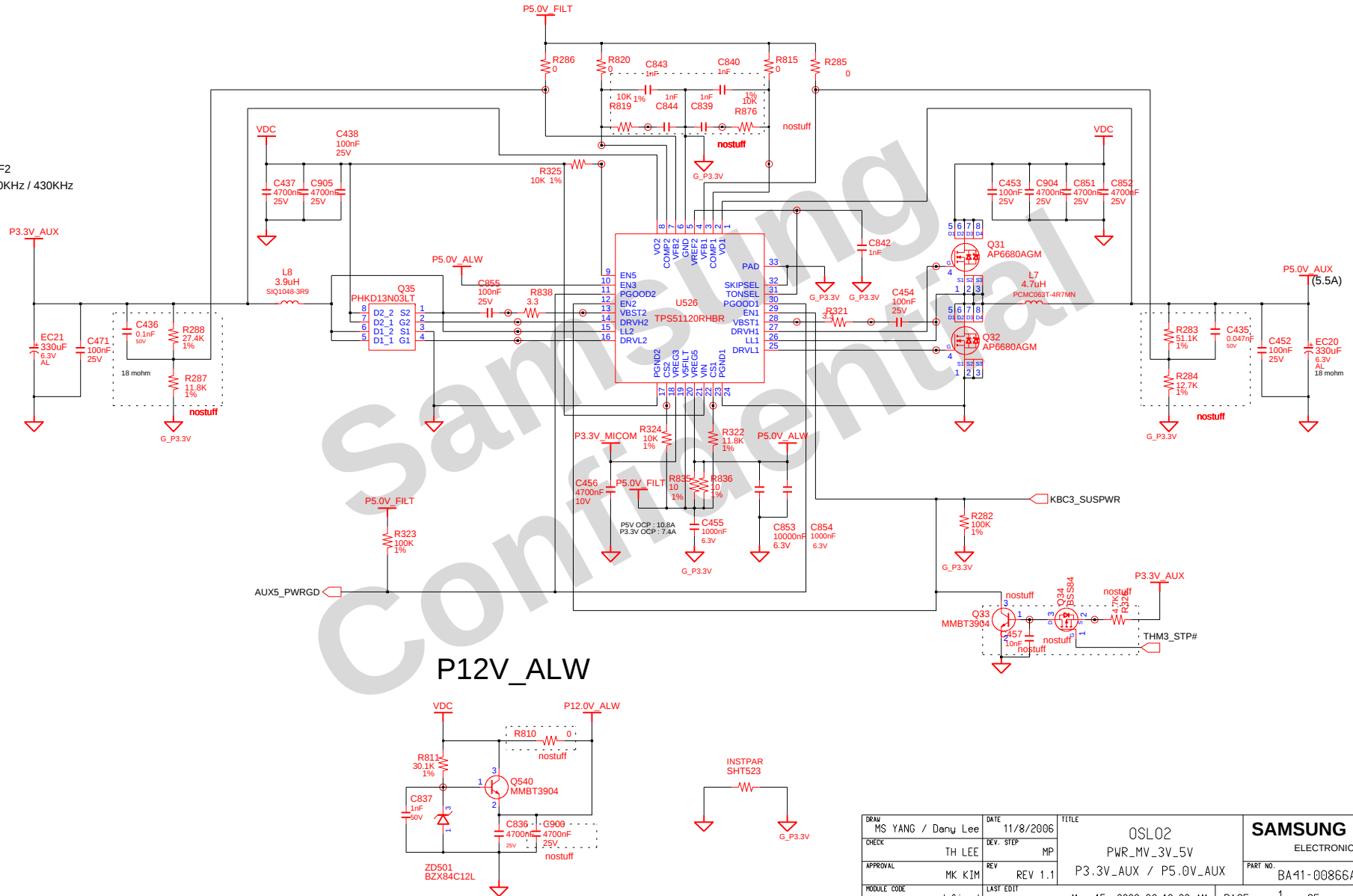


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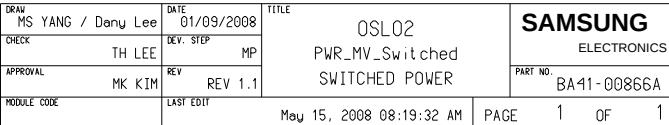
P3.3V_AUX & P5.0V_AUX

TONSEL VREF2
5V / 3.3V : 280KHz / 430KHz
(4.5A)

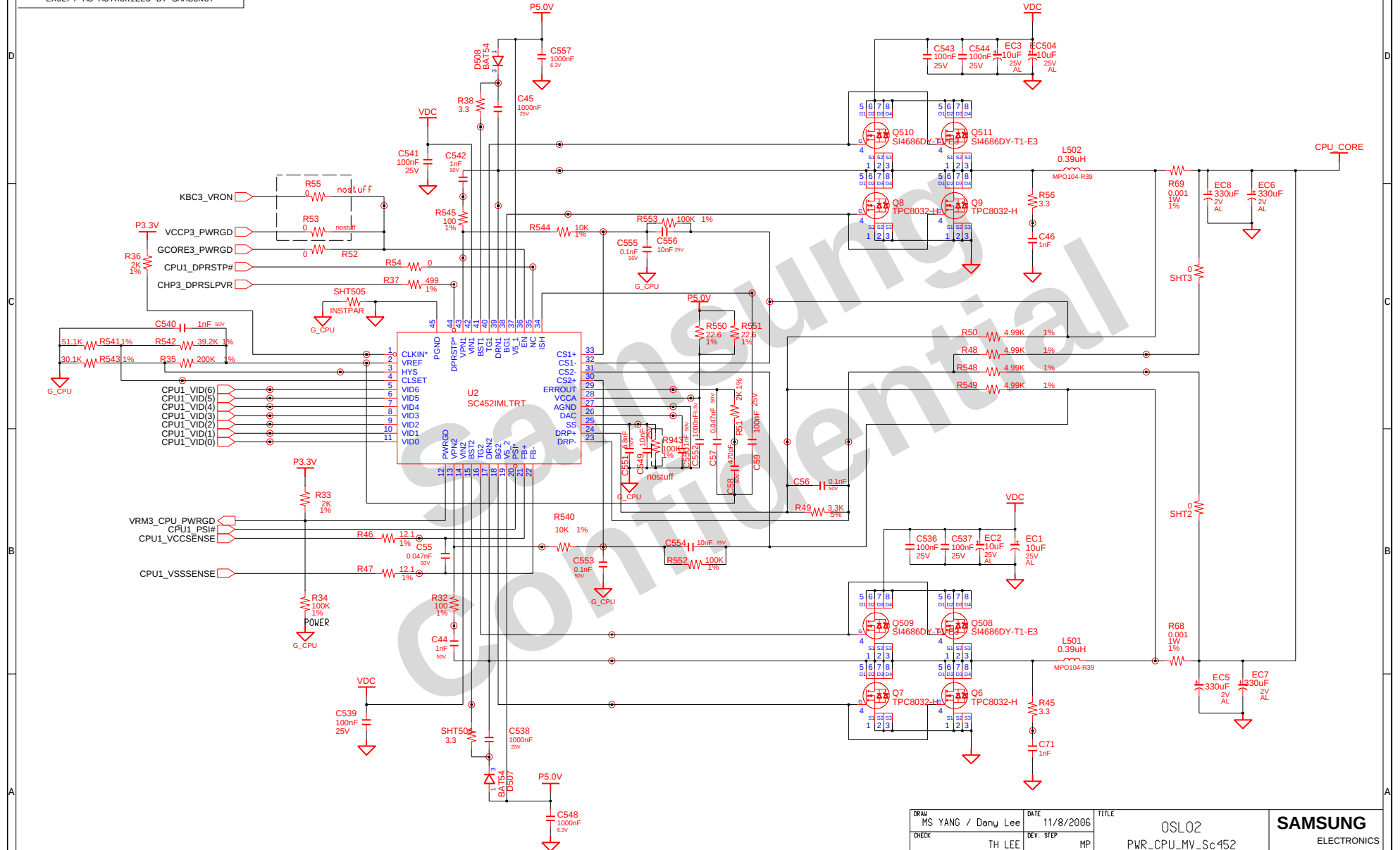


P12V_ALW

DRAW	MS YANG / Dany Lee	DATE	11/8/2006	TITLE	OSL02	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK	TH LEE	DEV. STEP	MP		PWR_MV_3V_5V	
APPROVAL	MK KIM	REV	1.1		P3.3V_AUX / P5.0V_AUX	
MODULE CODE	undefined	LAST EDIT				
May 15, 2008 08:19:32 AM						PAGE 1 OF 1

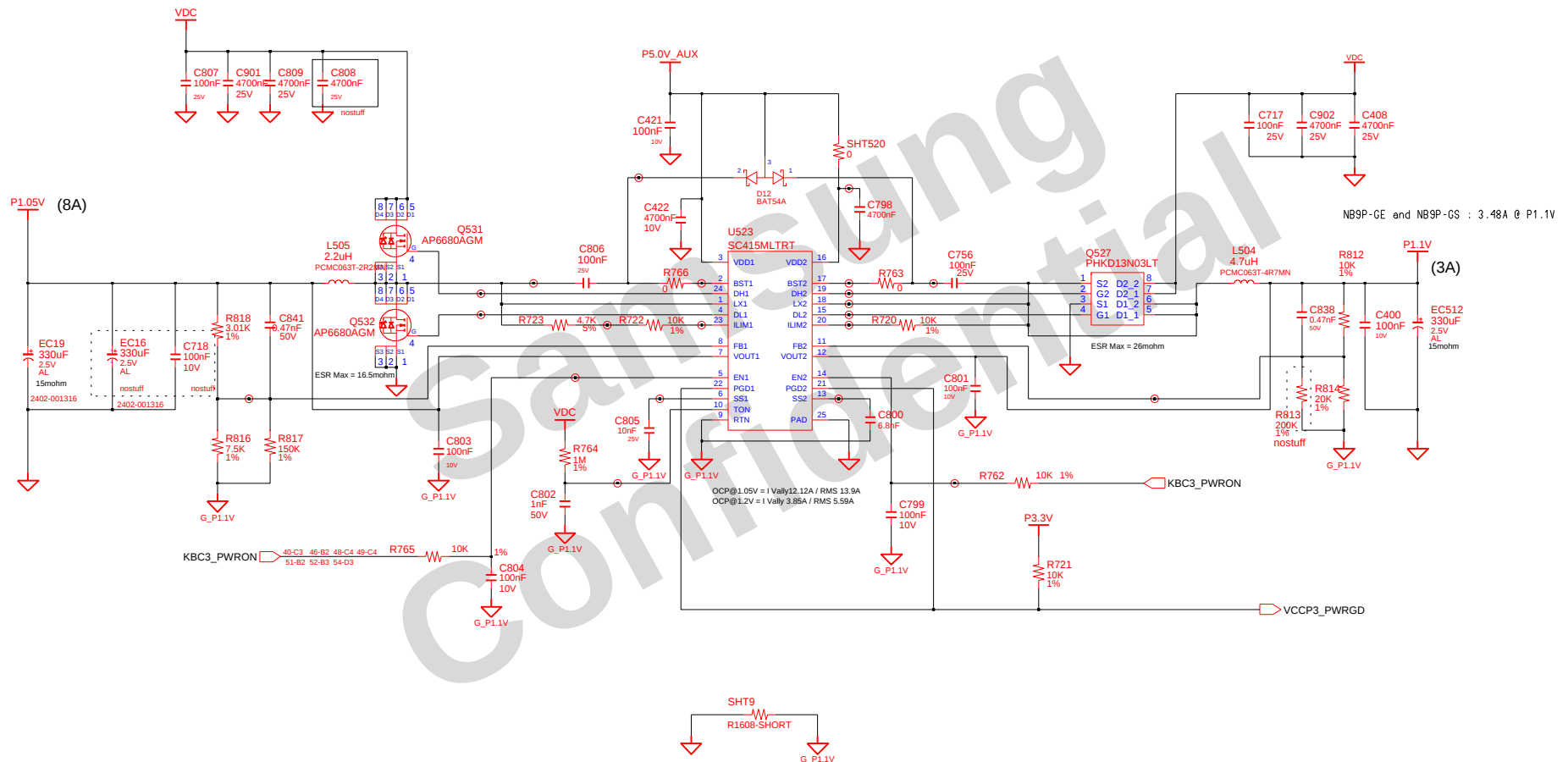


CPU VRM [SEMTECH]



DRAW	MS YANG / Dany Lee	DATE	11/8/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP	PWR_CPU_MV_Sc452		
APPROVAL	MK KIM	REV	1.1	CPU VRM (IMVP6+)	PART NO.	BA11-00866A
MODULE CODE	undefined	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	1	OF 1

CHIPSET POWER(P1.05V & P1.1V)

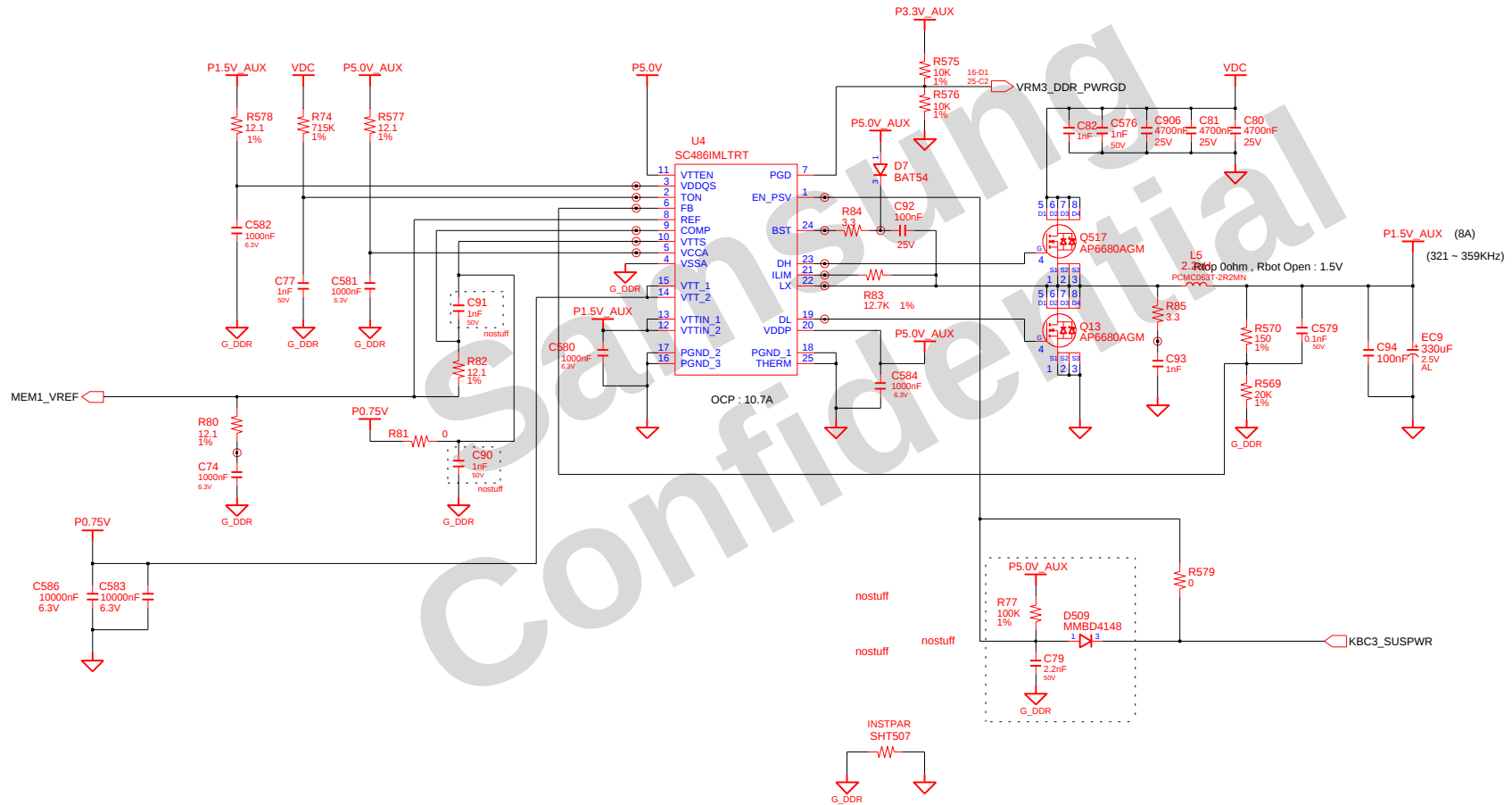


DRAW	MS YANG / Dany Lee	DATE	8/14/2007	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	REV. STEP	MP	PWR_MV_Cantiga	PART NO.	
APPROVAL	MK KIM	REV	1	Chipset Power (P1.05V-M, P1.1V)	BA41-00866A	
MODULE CODE	undefined	LAST EDIT		May 15, 2008 08:19:32 AM	PAGE	1 OF 1

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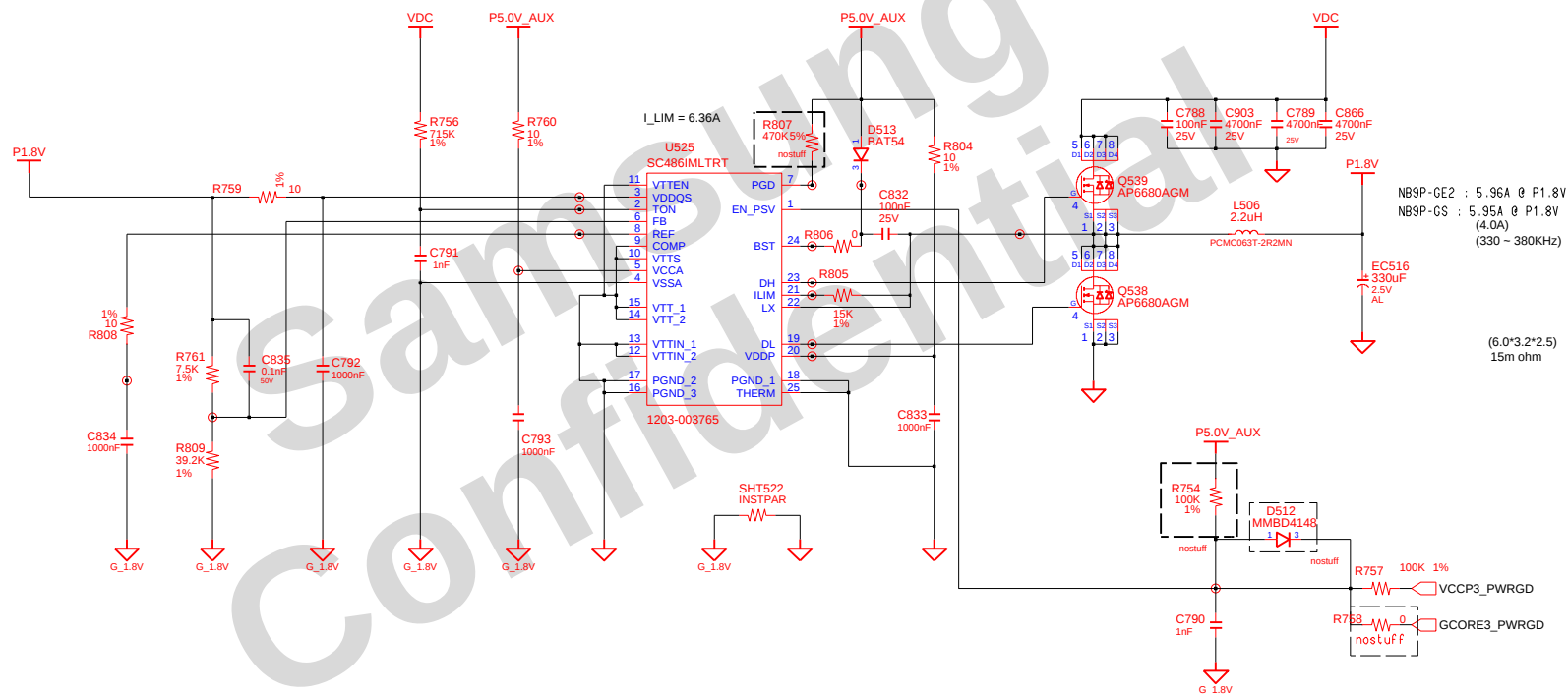
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DDR3 Power



DRAW	MS YANG / Dany Lee	DATE	11/8/2006	TITLE	OSL02	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK	TH LEE	DEV. STEP	MP		PWR_MV_Memory	
APPROVAL	MK KIM	REV	1.1		DDR3 POWER (P1.5V_AUX)	
MODULE CODE	undefined	LAST EDIT				
May 15, 2008 08:19:32 AM						PAGE 1 OF 1

P1.8V (External Gfx Memory)



DRN	MS YANG / Dany Lee	DATE	8/14/2007	TITLE	OSL02	SAMSUNG	
CHECK	TH LEE	DEV. STEP	MP	PWR_Gfx_MV_Ext		ELECTRONICS	
APPROVAL	MK KTM	REV	REV 1.1	Ext Gfx Memory(SC486)		PART NO.	BA41-00866A
MODULE CODE	LAST EDIT			Mon 15, 2008 08:19:32 AM	PAGE	1	OF 2

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Graphic Core Power

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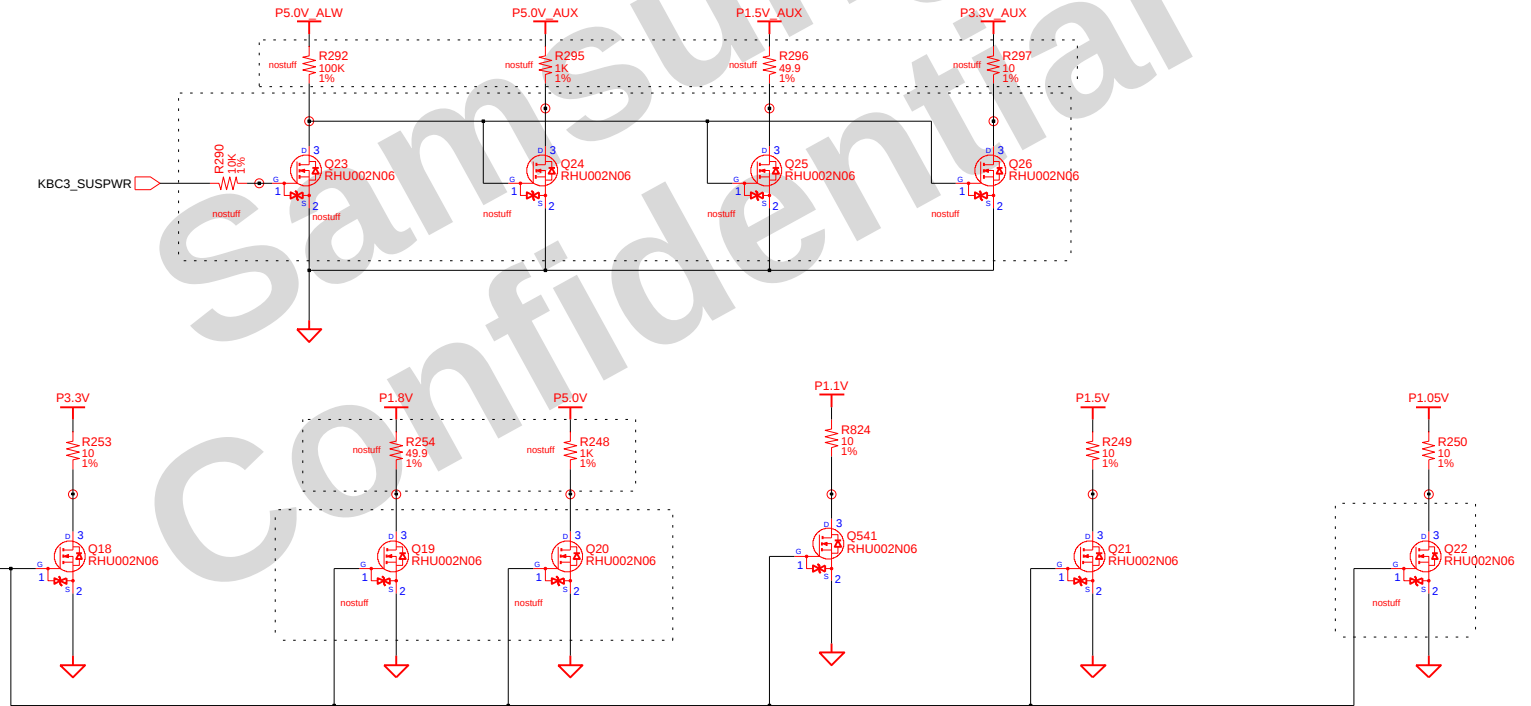
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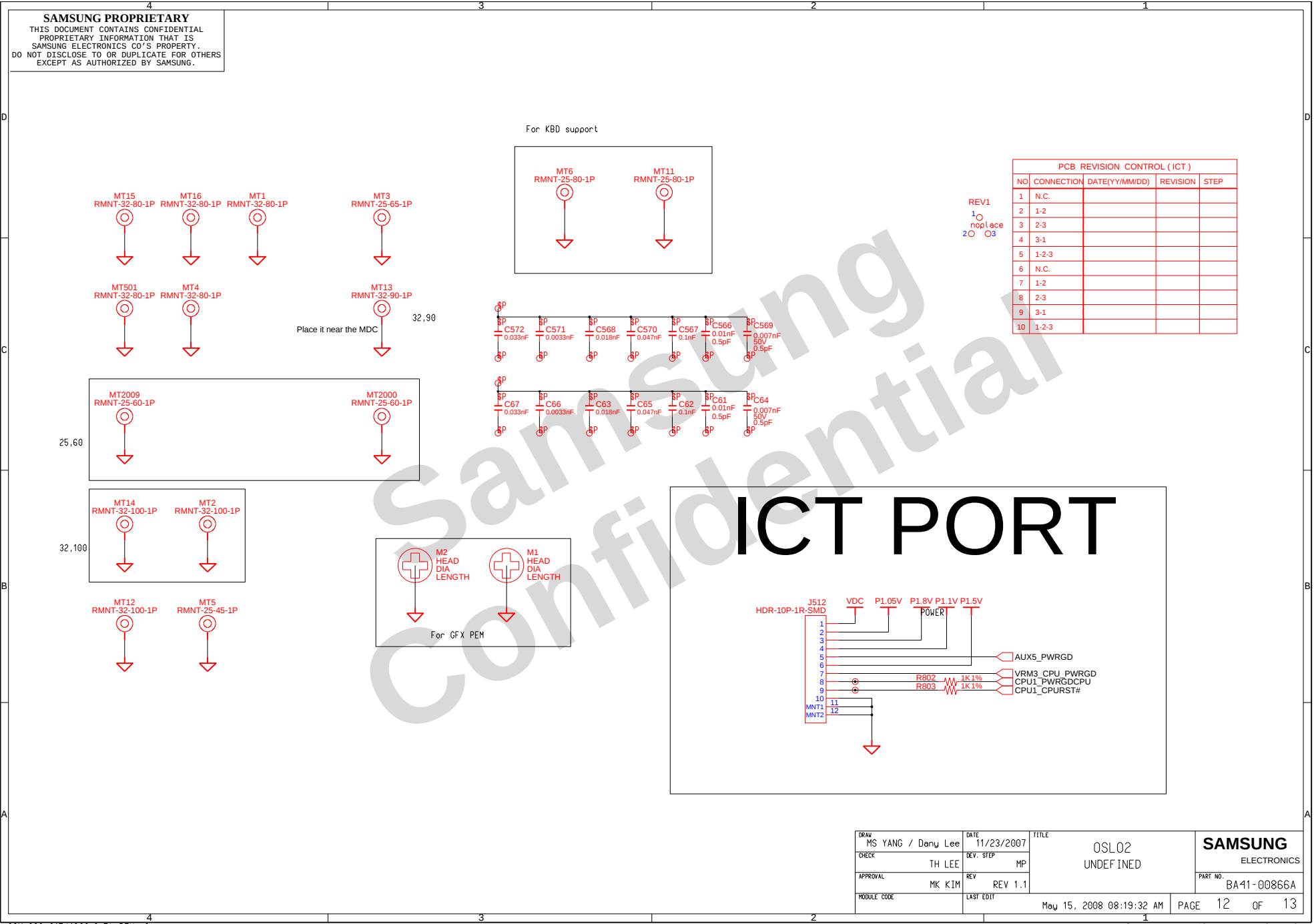
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POWER DISCHARGER



DRAW MS YANG / Dany Lee	DATE 8/14/2007	TITLE OSL02	SAMSUNG ELECTRONICS PART NO. BA41-00866A
CHECK TH LEE	DEV. STEP MP	PWR_MV_DisCharger	
APPROVAL MK KIM	REV REV 1.1	DISCHARGING LOGIC	
MODULE CODE undefined	LAST EDIT	May 15, 2008 08:19:32 AM	
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[illegible]

```

KBK65_K50(8)
KBK65_K50(9)
KBK65_TCLK
KBK65_TCLK#
KBK65_TCLKD#
KBK65_TCLKD#_1
LAN3_L1_LNK100#
LAN3_L1_LNK100_100#
LAN3_VPDCLK
LAN3_VPDDATA

QLDQ3_BKL1ON
QLDQ3_BR1T
QLDQ3_CQDIO_CLK
QLDQ3_EDIT_DATA
QLDQ3_SWITCH#
QLM03_CLKREQ#
QPC3_LAD(0)
QPC3_LAD(1)
QPC3_LAD(2)
QPC3_LAD(3)
QPC3_LFRAME#

MCMH1_HVREF
MCMH1_HXSUSG
MCMH1_HXSUSG#
MCMH1_DDR_RST#
MCMH3_EXT1TS10#
MCMH3_EXT1TS15#
MCMH3_TCHSNC#
MCMH3_LCTRL_C
MCMH3_LCTRL_D

SMB3_ALERT#
SMB3_CLK
SMB3_CLK#
SMB3_DATA
SP13_CLK
SP13_CSN
SP13_CS#
SP13_MOSI
SPK5_L+
SPK5_L-
SPK5_L+L+
SPK5_R+
SPK5_R-
THM3_ALERT#
THM3_STP#
T1_BUTTON
T1R_BUTTON#

MEM1_VREF
MIN3_CLKREQ#
MI03_BUTTON#

PEPG3_BKL1EN
PEPG3_HDM1_CLK
PEPG3_HDM1_DATA
PEPG3_HPD_HDM1
PEPG3_LCDVDION

PEP3_WAKE#
PL13_RST#
PL13_RST_ORG#

W1LON_LED#

VCCP3_PWRGD
VRN3_DDR_PWRGD

PCP13_CLKRUN#

```

☐ VDC
☐ VDC
☐ VDC
☐ VDC
☐ VDC

☒ VDC_INV
☐ VDC_INV
☐ VCC_CRT
☐ VCC_CRT

☒ P12V0_ALW
☐ P12V0_ALW

☐ P5V0_ALW
☐ P5V0_ALW
☐ P5V0_ALW

☐ P5V0_AMP
☐ P5V0_AMP

☐ P5V0
☐ P5V0
☐ P5V0
☐ P5V0
☐ P5V0

☒ P5V0_AUD
☐ P5V0_AUD

☒ P5V0_AUX
☐ P5V0_AUX
☐ P5V0_AUX
☐ P5V0_AUX
☐ P5V0_AUX
☐ P5V0_AUX

☐ P5V0_FILTER

☒ P475V_AUD
☐ P475V_AUD

☒ P33V_VDD

☐ P33V_EXP
☐ P33V_EXP

☒ P33V_MCD

☒ P33V_MICOM
☐ P33V_MICOM
☐ P33V_MICOM
☐ P33V_MICOM
☐ P33V_MICOM
☐ P33V_MICOM_VDDQ
☐ P33V_MICOM_VDDQ

☒ PRRTC_BAT
☐ PRRTC_BAT

☐ P33V
☐ P33V
☐ P33V
☐ P33V
☐ P33V
☐ P33V_AUX_EXP

☒ P33V_DACA

☐ G_P33V

☐ LCD_VDD3V
☐ LCD_VDD3V

☐ G_1.8V

☒ P1B8
☐ P1B8
☐ P1B8
☐ P1B8
☐ P1B8
☐ P1B8_FBDQDQ
☐ P1B8_FBDQDQ

[illegible]

TP21801 ○ **P0.75V**
TP21802 ○ **VDD_5.0V**

TP21803 ○ **ADT3_SEL#**
TP21804 ○ **CHP3_USBPWRON#**
TP21798 ○ **ITM3_CLKREQ#**
TP21799 ○ **KBC3_PRECHG**
TP21800 ○ **KBC3_USBPWRON#**

○KBC3_CHG2600
 ○MCD3_SDDATA0
 ○MCD3_SDDATA1
 ○MCD3_SDDATA2
 ○MCD3_SDDATA3
 ○MCD3_XDDATA0
 ○MCD3_XDDATA1
 ○MCD3_XDDATA2
 ○MCD3_XDDATA3
 ○MCD3_XDDATA4
 ○MCD3_XDDATA5
 ○MCD3_XDDATA6
 ○MCD3_XDDATA7
 ○MCD3_MSDATA2_S
 ○MCD3_MSDATA1_X
 ○MCD3_MSDATA3_X
 ○MCD3_SDCLK_MSB
 ○MCD3_XDCLK_MSC
 ○MCD3_MSINS#
 ○MCD3_SDCD#
 ○MCD3_XDALE
 ○MCD3_XDCD#
 ○MCD3_XDCE#

- ☐ 0.7VDDQDQ
- ☐ 0.7VDDQDQ
- ☐ CPU_CORE
- ☐ CPU_CORE
- ☐ AD_DC
- ☐ AD_DC
- ☐ AD_DC
- ☐ AD_DC
- ☐ AD_CHG_REF
- ☐ FB_PLLVDDQ
- ☐ EGFX_CORE
- ☐ EGFX_CORE
- ☐ PEX_PLLVDD
- ☐ G_AUD
- ☐ G_AUD
- ☐ G_AUD
- ☐ G_AUD
- ☐ G_AUD
- ☐ G_CHG
- ☐ G_CHG
- ☐ G_DDR
- ☐ G_DDR
- ☐ G_EGFX
- ☐ G_MIC
- ☐ G_MIC
- ☐ G_P11V

GROUND
GROUND
GROUND
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GROUND

○KBC3_CHG2600
 ○MCD3_SDDATA0
 ○MCD3_SDDATA1
 ○MCD3_SDDATA2
 ○MCD3_SDDATA3
 ○MCD3_XDDATA0
 ○MCD3_XDDATA1
 ○MCD3_XDDATA2
 ○MCD3_XDDATA3
 ○MCD3_XDDATA4
 ○MCD3_XDDATA5
 ○MCD3_XDDATA6
 ○MCD3_XDDATA7
 ○MCD3_MSDATA2_S
 ○MCD3_MSDATA1_X
 ○MCD3_MSDATA3_X
 ○MCD3_SDCLK_MSB
 ○MCD3_XDCLK_MSC
 ○MCD3_MSINS#
 ○MCD3_SDCD#
 ○MCD3_XDALE
 ○MCD3_XDCD#
 ○MCD3_XDCE#

any Lee	DATE 11/23/2
TH LEE	DEV. STEP
	PCN

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