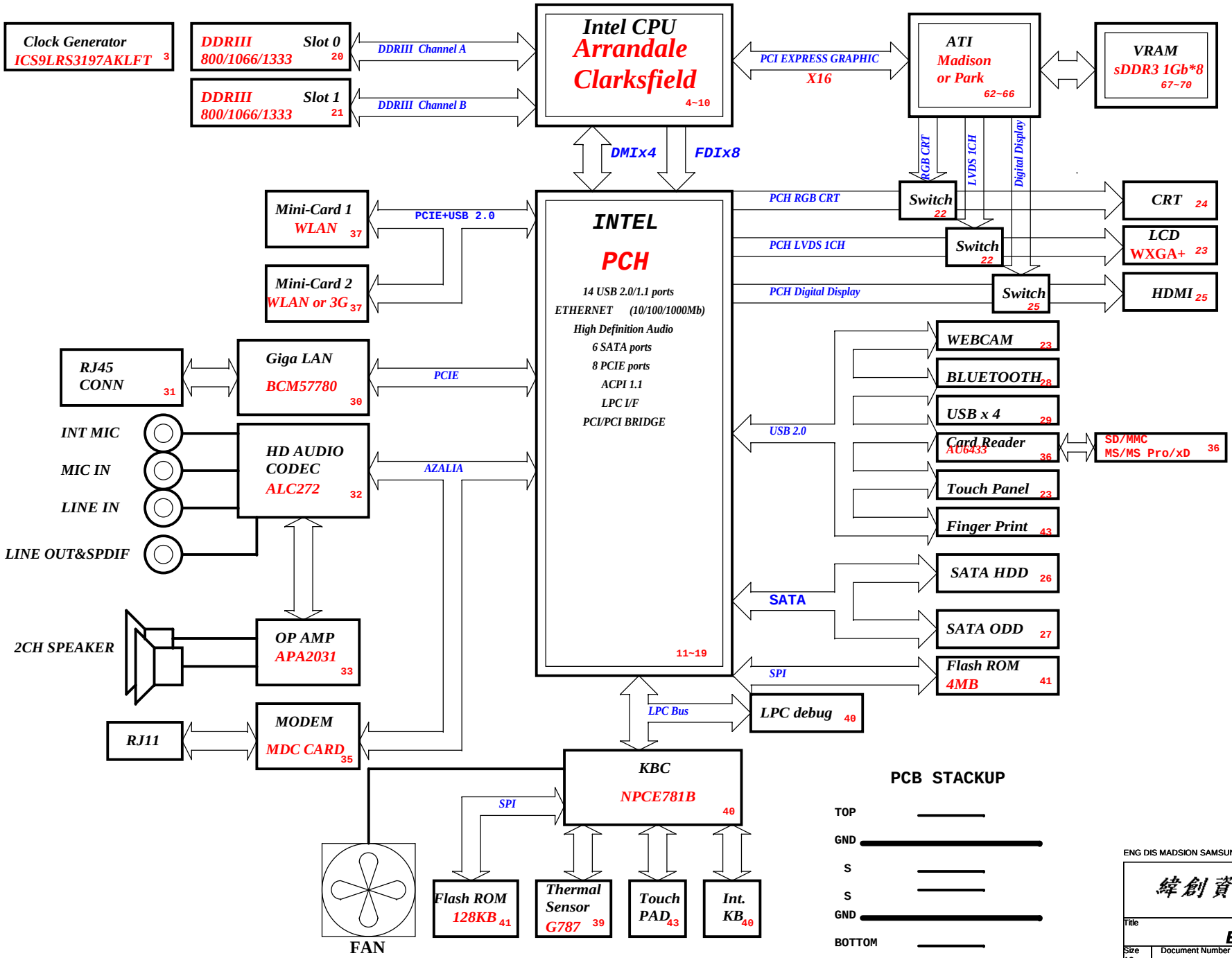
JV50-CP Block Diagram

Project code: 91.4GD01.001
PCB P/N : 48.4GD01.0SB
REVISION : SB 09285



PCB STACKUP

TOP
GND
S
S
GND
BOTTOM

CPU DC/DC ISL62882	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 47,48

SYSTEM DC/DC TPS51123	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 49

SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 50

SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 50

SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 51

RT9025	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0 50

G2997	
INPUTS	OUTPUTS
1D5V_S3	0D75_S0 52

SYSTEM DC/DC ISL62881	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 54

SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	+VGA_CORE 55

CHARGER ISL88731A	
INPUTS	OUTPUTS
DCBATOUT	BT+ 53

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緯創資通 Wistron Corporation
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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

PCIE Routing

LANE1	**LAN**
LANE2	**MiniCard1**
LANE3	**MiniCard2**

USB Table

Pair	*Device*
0	*USB3*
1	*USB2*
2	*USB4*
3	*MINICARD1*
4	*WECAM*
5	*Touch Panel*
6	*NC*
7	*NC*
8	*NC*
9	*USB1(HS)*
10	*Finger Print*
11	*Blue Tooth*
12	*MINIC2*
13	*Cardreader*

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Title: *Table of Content*

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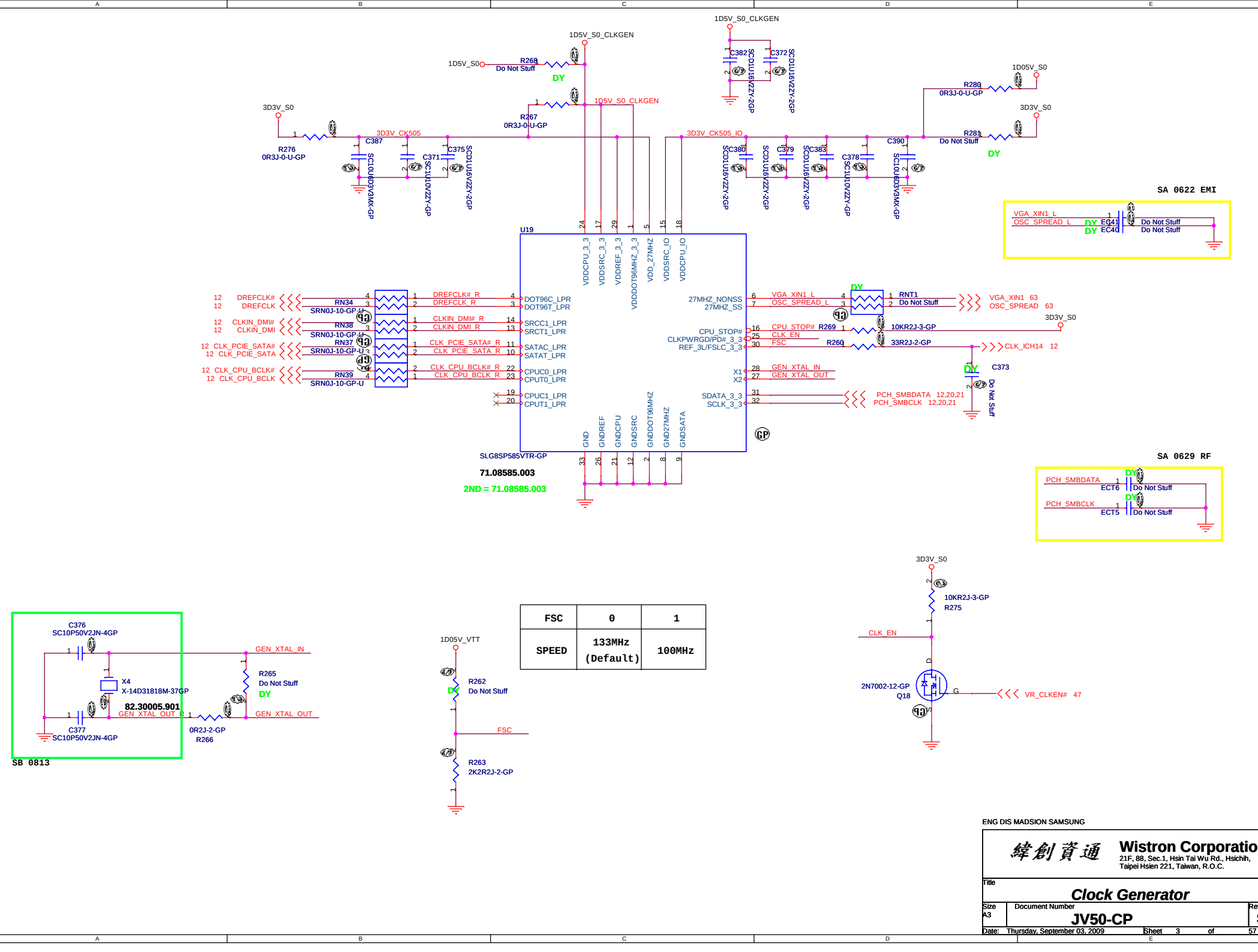

FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title: **Clock Generator**

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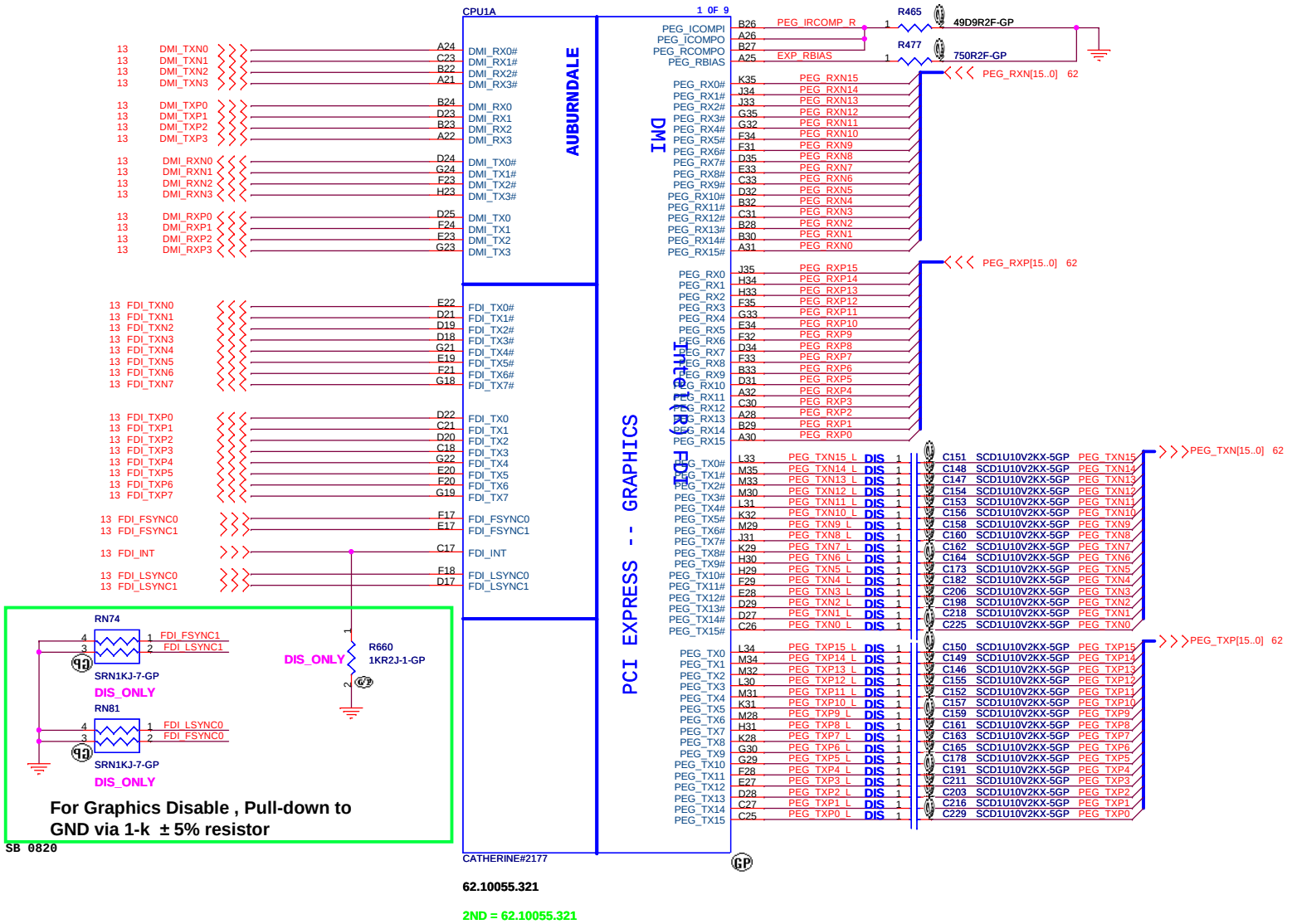

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Title: CPU (1/7)		
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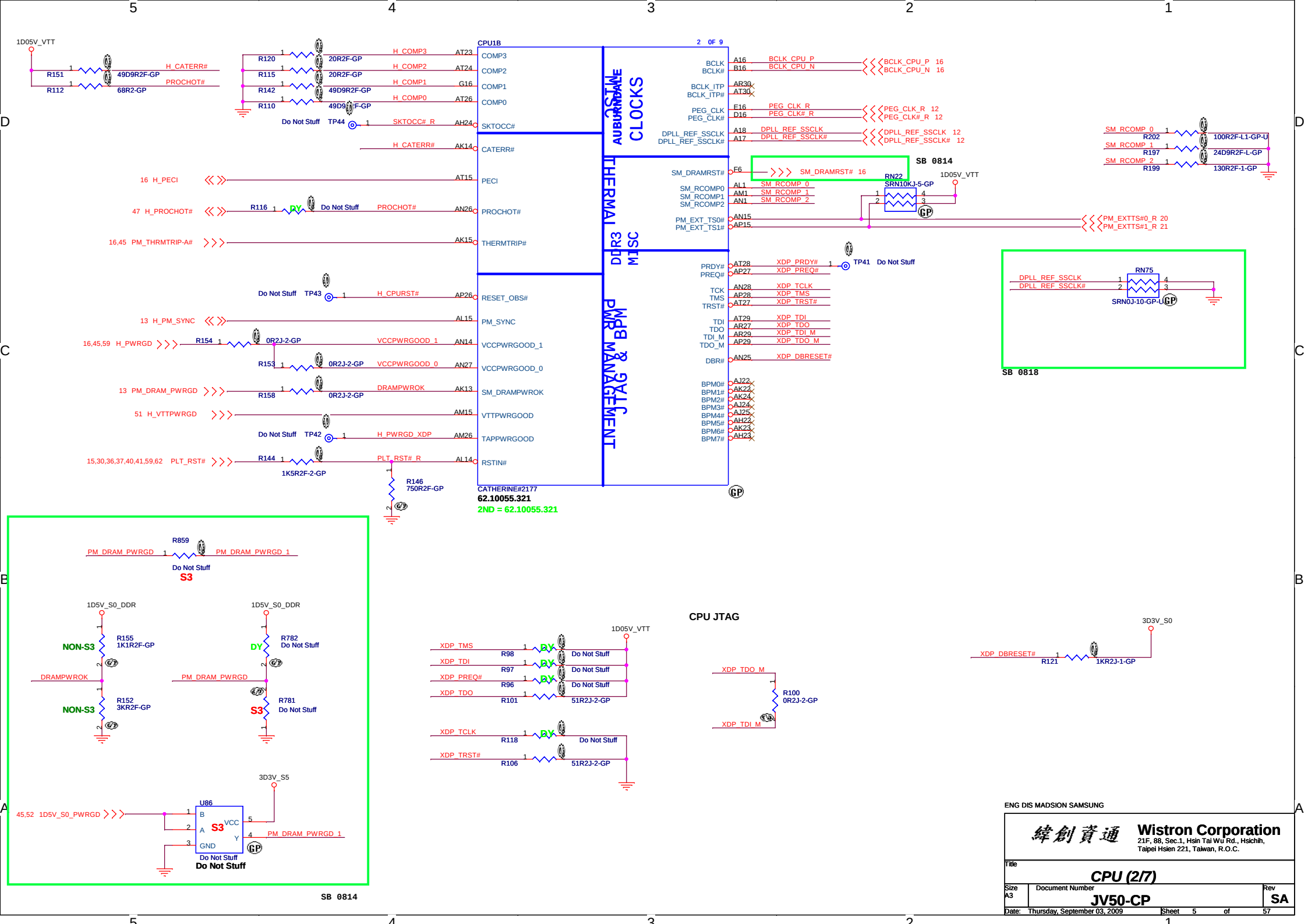
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2 OF 9
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THERMAL
DDR3
MISC
PWR MANAGEMENT
JTAG
1D05V_VTT
R151 49D9R2F-GP
R112 68R2-GP
H_CATERR#
PROCHOT#
R120 20R2F-GP
R115 20R2F-GP
R142 49D9R2F-GP
R110 49D9R2F-GP
H_COMP3
H_COMP2
H_COMP1
H_COMP0
Do Not Stuff
TP44
SKTOCC# R
COMP3
COMP2
COMP1
COMP0
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
RESET_OBS#
PM_SYNC
VCCPWRGOOD_1
VCCPWRGOOD_0
SM_DRAMPWROK
VTTPWRGOOD
TAPPWRGOOD
RSTIN#
16 H_PECI
47 H_PROCHOT#
16,45 PM_THRMTRIP#
R116
DY
Do Not Stuff
13 H_PM_SYNC
16,45,59 H_PWRGD
R154 0R2J-2-GP
R153 0R2J-2-GP
VCCPWRGOOD_1
VCCPWRGOOD_0
13 PM_DRAM_PWRGD
R158 0R2J-2-GP
DRAMPWROK
51 H_VTTPWRGD
TP43
H_CPURST#
TP42
H_PWRGD_XDP
15,30,36,37,40,41,59,62 PLT_RST#
R144 1K5R2F-2-GP
PLT_RST# R
R146 750R2F-GP
CATHERINE#2177
62.10055.321
2ND = 62.10055.321
BCLK
BCLK#
BCLK_ITP
BCLK_ITP#
PEG_CLK
PEG_CLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
BCLK_CPU_P
BCLK_CPU_N
PEG_CLK_R
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SM_DRAMRST# 16
SB 0814
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
SM_RCOMP_0
SM_RCOMP_1
SM_RCOMP_2
RN22 SRN10KJ-5-GP
1D05V_VTT
PM_EXT_TS0#
PM_EXT_TS1#
PM_EXTTS#0_R 20
PM_EXTTS#1_R 21
PRDY#
PREQ#
XDP_PRDY#
XDP_PREQ#
TP41 Do Not Stuff
TCK
TMS
TRST#
XDP_TCLK
XDP_TMS
XDP_TRST#
TDI
TDO
TDI_M
TDO_M
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DBR#
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BPM0#
BPM1#
BPM2#
BPM3#
BPM4#
BPM5#
BPM6#
BPM7#
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SM_RCOMP_2 R199 130R2F-1-GP
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SB 0818
PM_DRAM_PWRGD
R859
PM_DRAM_PWRGD_1
Do Not Stuff
S3
1D5V_S0_DDR
NON-S3
R155 1K1R2F-GP
R152 3KR2F-GP
DRAMPWROK
R782 Do Not Stuff
R781 Do Not Stuff
PM_DRAM_PWRGD
3D3V_S5
U86
45,52 1D5V_S0_PWRGD
VCC
GND
PM_DRAM_PWRGD_1
Do Not Stuff
SB 0814
CPU JTAG
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XDP_TDI
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XDP_TCLK
XDP_TRST#
R98
R97
R96
R101
R118
R106
51R2J-2-GP
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XDP_TDI_M
R100 0R2J-2-GP
3D3V_S0
XDP_DBRESET#
R121 1KR2J-1-GP
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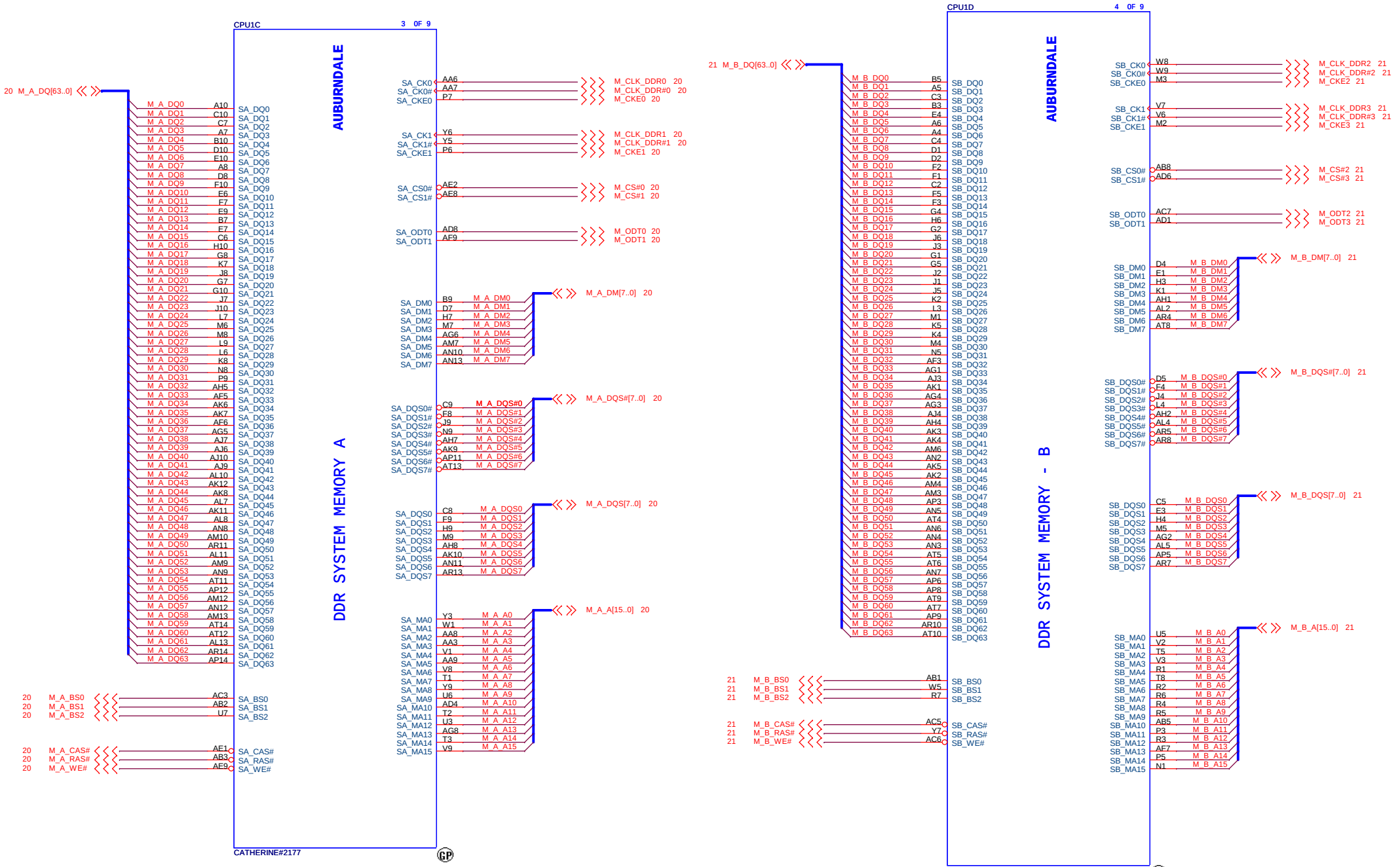
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SA_MA8 Y9 M_A_A8
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SA_MA10 AD4 M_A_A10
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SB_DQS4# AH2 M_B_DQS#4
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SB_DQS7# AR8 M_B_DQS#7
M_B_DQS#[7..0] 21
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SB_DQS3 M5 M_B_DQS3
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SB_DQS7 AR7 M_B_DQS7
M_B_DQS[7..0] 21
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SB_MA1 V2 M_B_A1
SB_MA2 T5 M_B_A2
SB_MA3 V3 M_B_A3
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SB_MA5 T8 M_B_A5
SB_MA6 R2 M_B_A6
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SB_MA8 R4 M_B_A8
SB_MA9 R5 M_B_A9
SB_MA10 AB5 M_B_A10
SB_MA11 P3 M_B_A11
SB_MA12 R3 M_B_A12
SB_MA13 AE7 M_B_A13
SB_MA14 P5 M_B_A14
SB_MA15 N1 M_B_A15
M_B_A[15..0] 21
CATHERINE#2177
2ND = 62.10055.321
62.10055.321
ENG DIS MAD
SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
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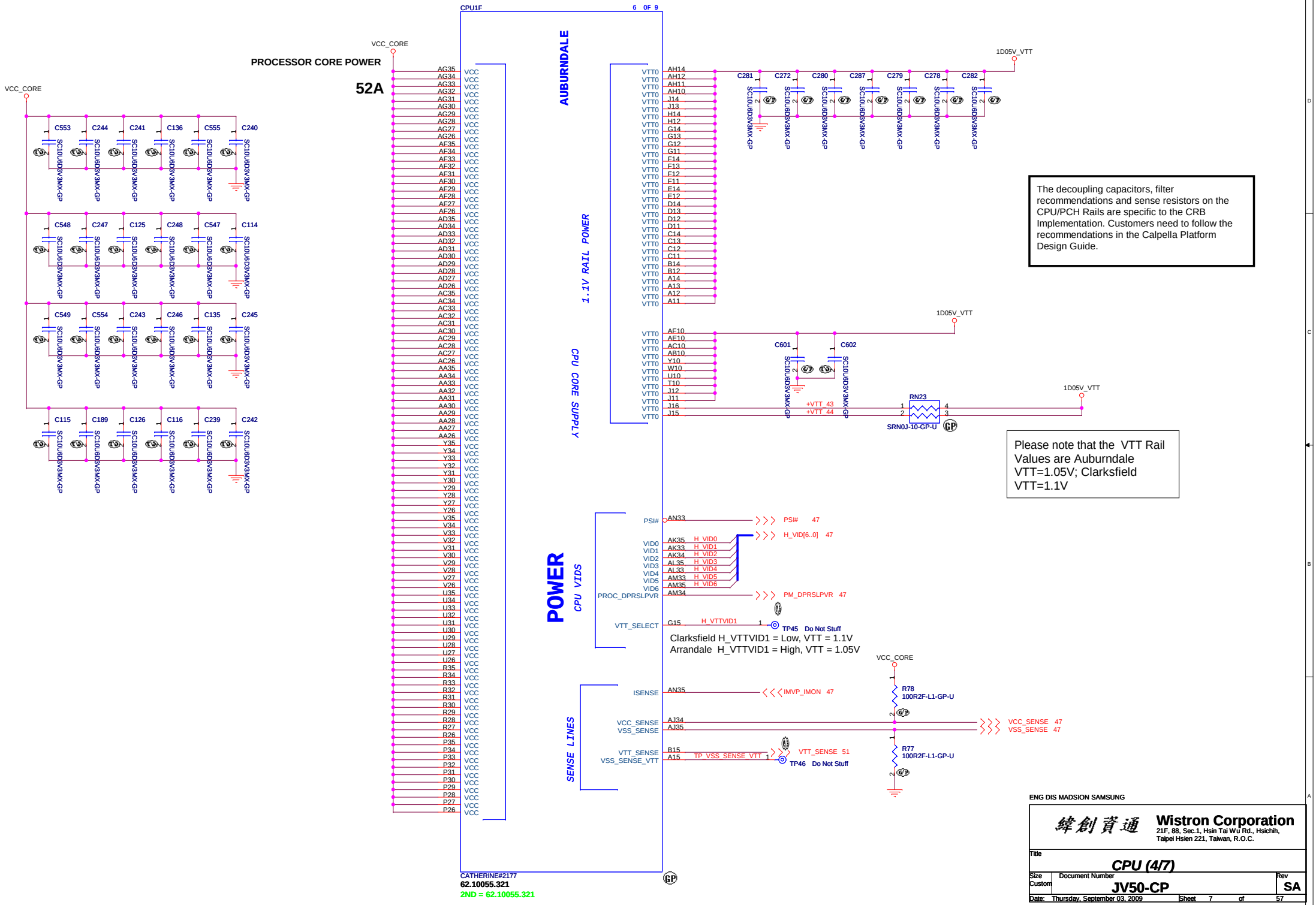
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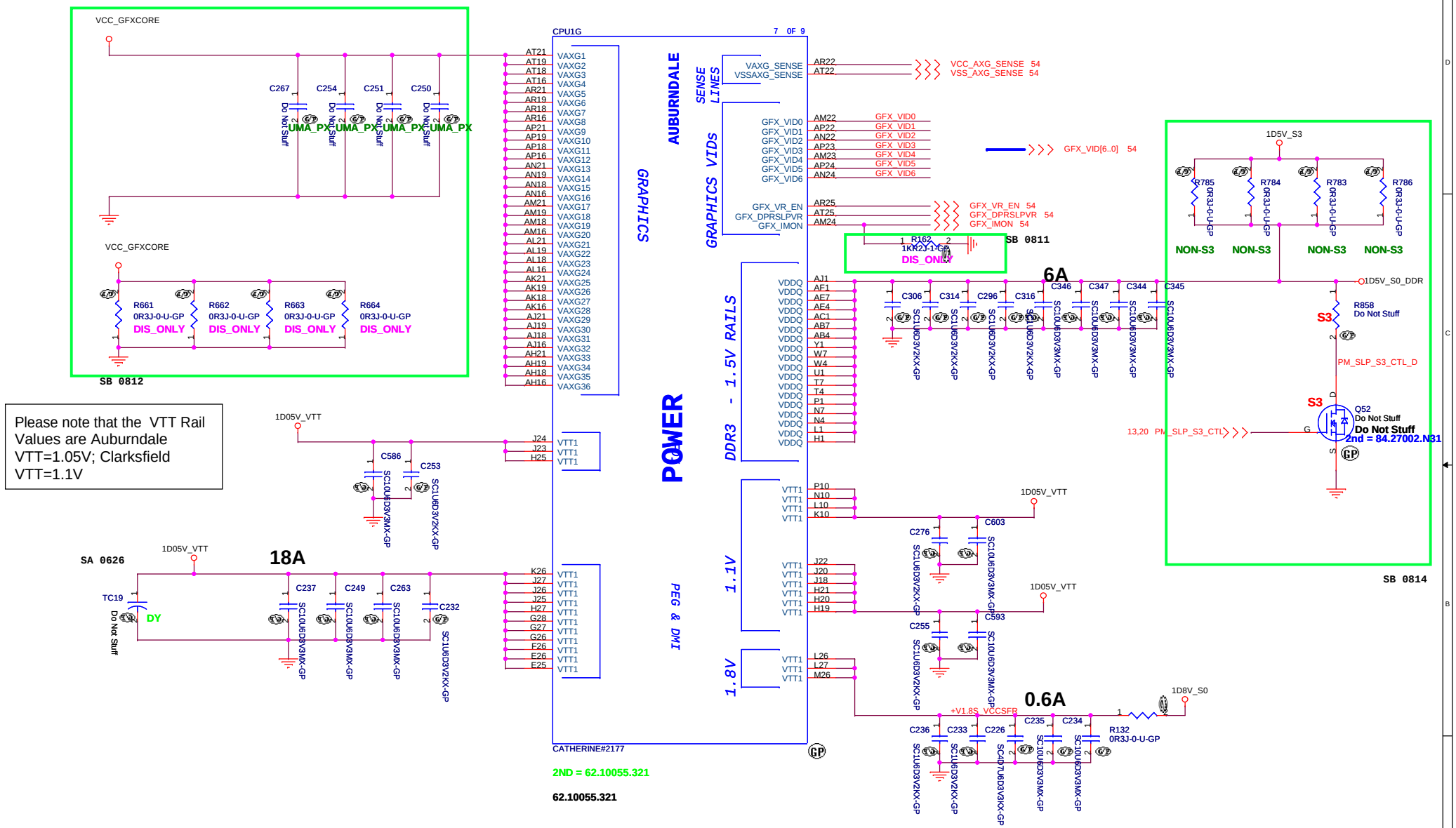
52A
VCC_CORE
CPU1F
6 0F 9
AUBURNDALE
1.1V RAIL POWER
CPU CORE SUPPLY
POWER
CPU VIDS
SENSE LINES
1D05V_VTT
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V
Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V
TP45 Do Not Stuff
TP46 Do Not Stuff
CATHERINE#2177
62.10055.321
2ND = 62.10055.321
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU (4/7)
JV50-CP
SA
Thursday, September 03, 2009
Sheet 7 of 57



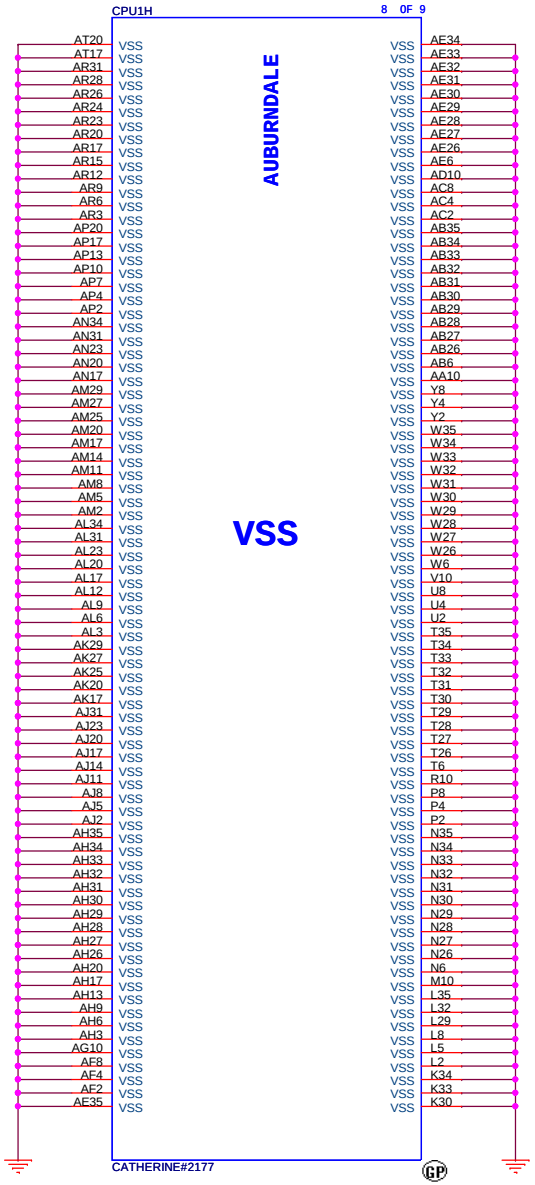
ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (5/7)

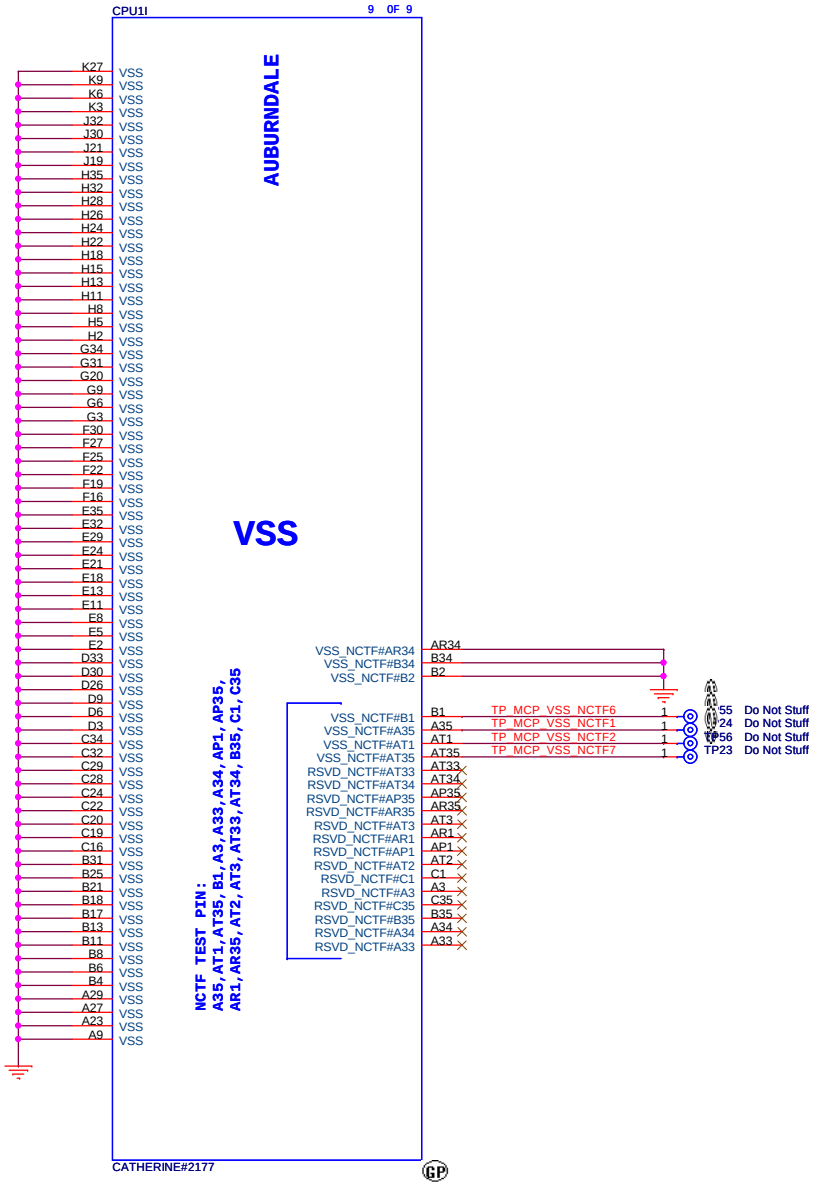
Size: A3 | Document Number: JV50-CP | Rev: SA

Date: Thursday, September 03, 2009 | Sheet 8 of 57



2ND = 62.10055.321

62.10055.321



2ND = 62.10055.321

62.10055.321

ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (6/7)

Size	Document Number	Rev
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Date: Wednesday, August 26, 2009 Sheet 9 of 57

SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor

SB 0817

20 M_VREF_DQ_DIMM0
21 M_VREF_DQ_DIMM1

RN28 DY
H_RSVD9_R
H_RSVD10_R
Do Not Stuff

CPU1E 5 OF 9

AUBURNDALE

RESERVED

SA_DIMM_VREF#
SB_DIMM_VREF#

CATHERINE#2177

2ND = 62.10055.321

62.10055.321

RN17
H_RSVD17_R
H_RSVD18_R
SRN0J-10-GP-U

RN20
RSVD64_R
RSVD65_R
SRN0J-10-GP-U

R73
0R2J-2-GP
RSVD_VSS

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

R74 Do Not Stuff
R76 3KR2F-GP
R119 Do Not Stuff
R75 Do Not Stuff

SA 0623

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (7/7)
Size: A3 | Document Number: JV50-CP | Rev: SA
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integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

PCH1A — 1 OF 10

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN
LPC: FWH0/LAD0, FWH1/LAD1, FWH2/LAD2, FWH3/LAD3, FWH4/LFRAME#, LDRQ0#, LDRQ1#/GPIO23, SERIRQ
IHDA: HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO
SATA: HDA_DOCK_EN#/GPIO33, HDA_DOCK_RST#/GPIO13, SATA0RXN/RXP/TXN/TXP, SATA1RXN/RXP/TXN/TXP, SATA2RXN/RXP/TXN/TXP, SATA3RXN/RXP/TXN/TXP, SATA4RXN/RXP/TXN/TXP, SATA5RXN/RXP/TXN/TXP, SATAICOMPO, SATAICOMPI, SATALED#, SATA0GP/GPIO21, SATA1GP/GPIO19
JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO, TRST#
SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO

IBEXPEAK-M-GP-NF

HDD: SATA0 — SATA_RXN0 26, SATA_RXP0 26, SATA_TXN0 26, SATA_TXP0 26
ODD: SATA4 — SATA_RXN4 27, SATA_RXP4 27, SATA_TXN4 27, SATA_TXP4 27

SA 0629 RF
SB 0825
SA 0709

NO REBOOT STRAP
3D3V_S0 — R557 DY Do Not Stuff — ACZ_SPKR

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"

SPI_MOSI — Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required

When unused all JTAG pins may be NC

ENG DIS MADSION SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (1/9)
Size: A3 | Document Number: JV50-CP | Rev: SA
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LAN

MINICARD1

MINICARD2

PCH1B

2 OF 10

PCI-E*

SMBus

Controller Link

PEG

From CLK BUFFER

Clock Flex

IBEXPEAK-M-GP-NF

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).

SB 0812

SB 0812

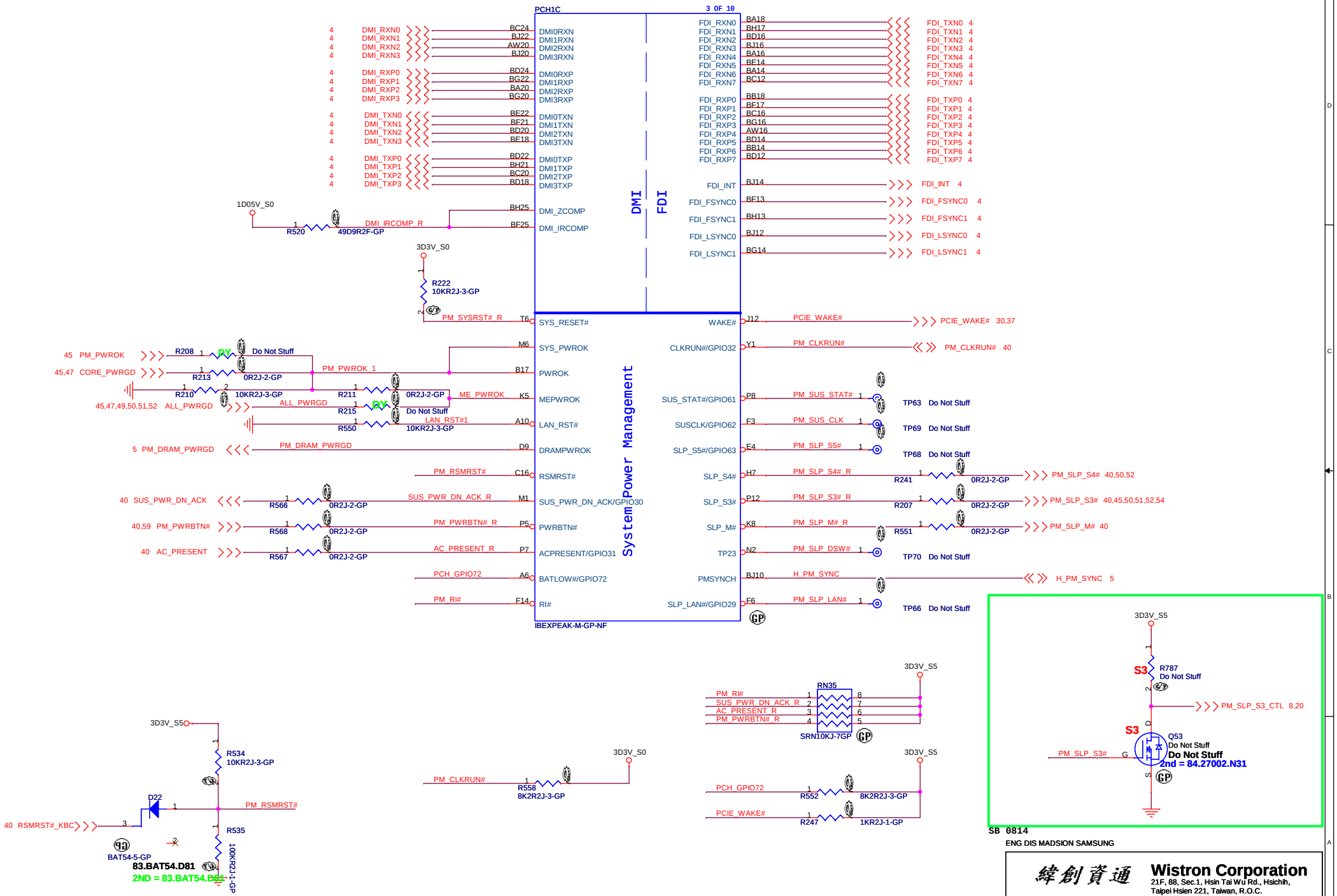
ENG DIS MADSION SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (2/9)

Size: A3 | Document Number: JV50-CP | Rev: SA

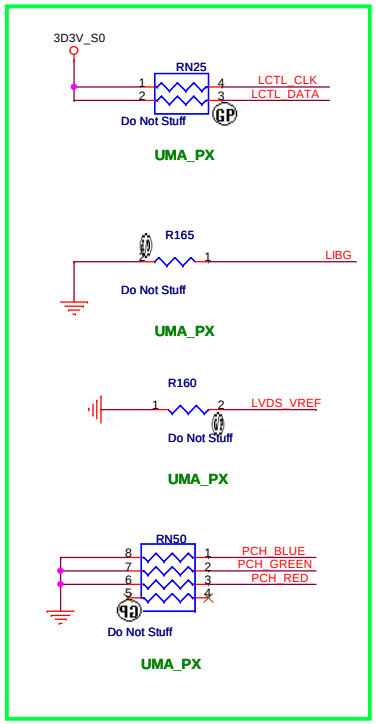
Date: Thursday, September 03, 2009 | Sheet 12 of 57



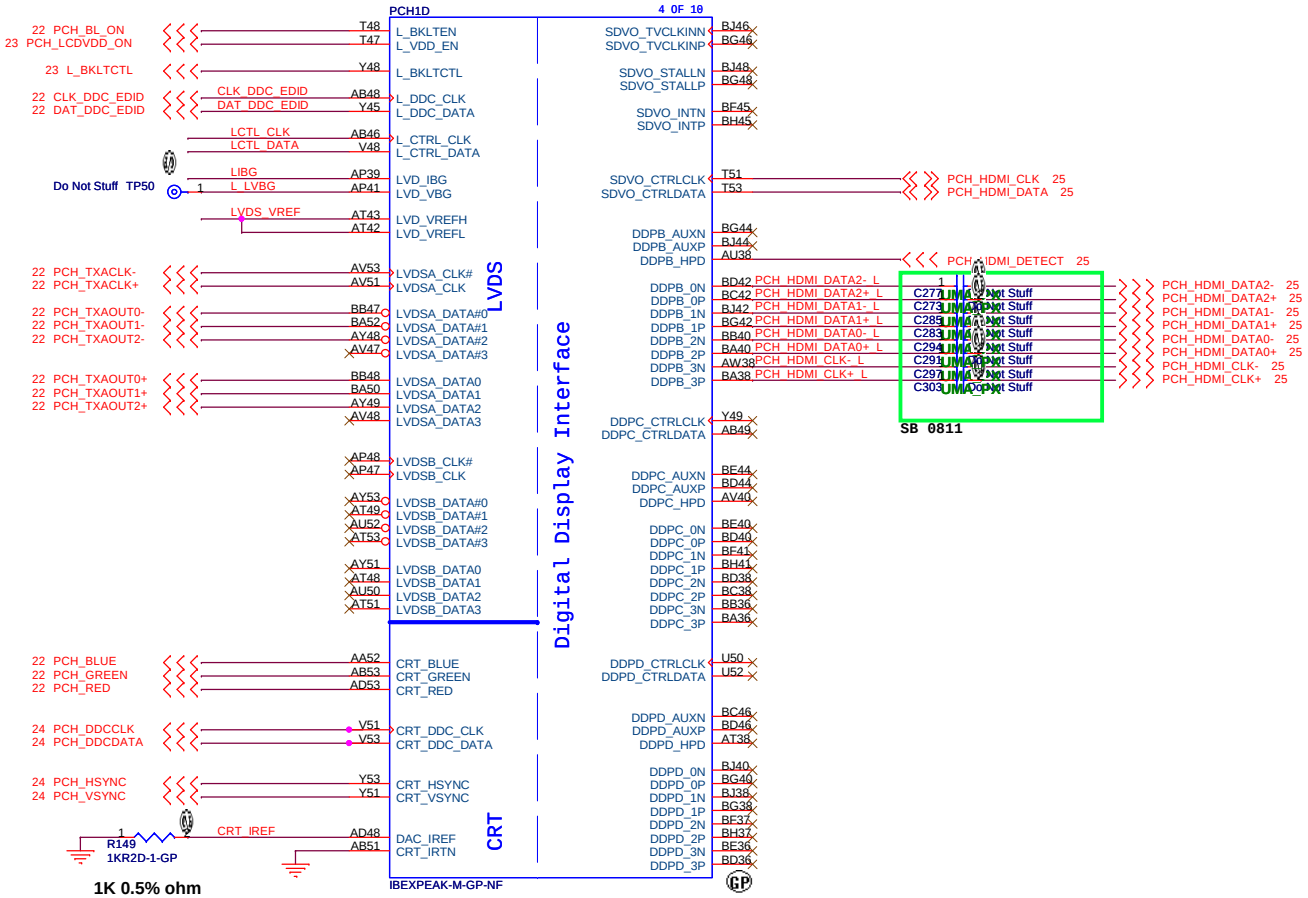
SB 0814

ENG DIS MADSION SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **PCH (3/9)**		
Size: A3	Document Number: **JV50-CP**	Rev: **SA**
Date: Thursday, September 03, 2009	Sheet 13 of 57	



SB 0811



ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCH (4/9)		
Size: A3	Document Number: JV50-CP	Rev: SA
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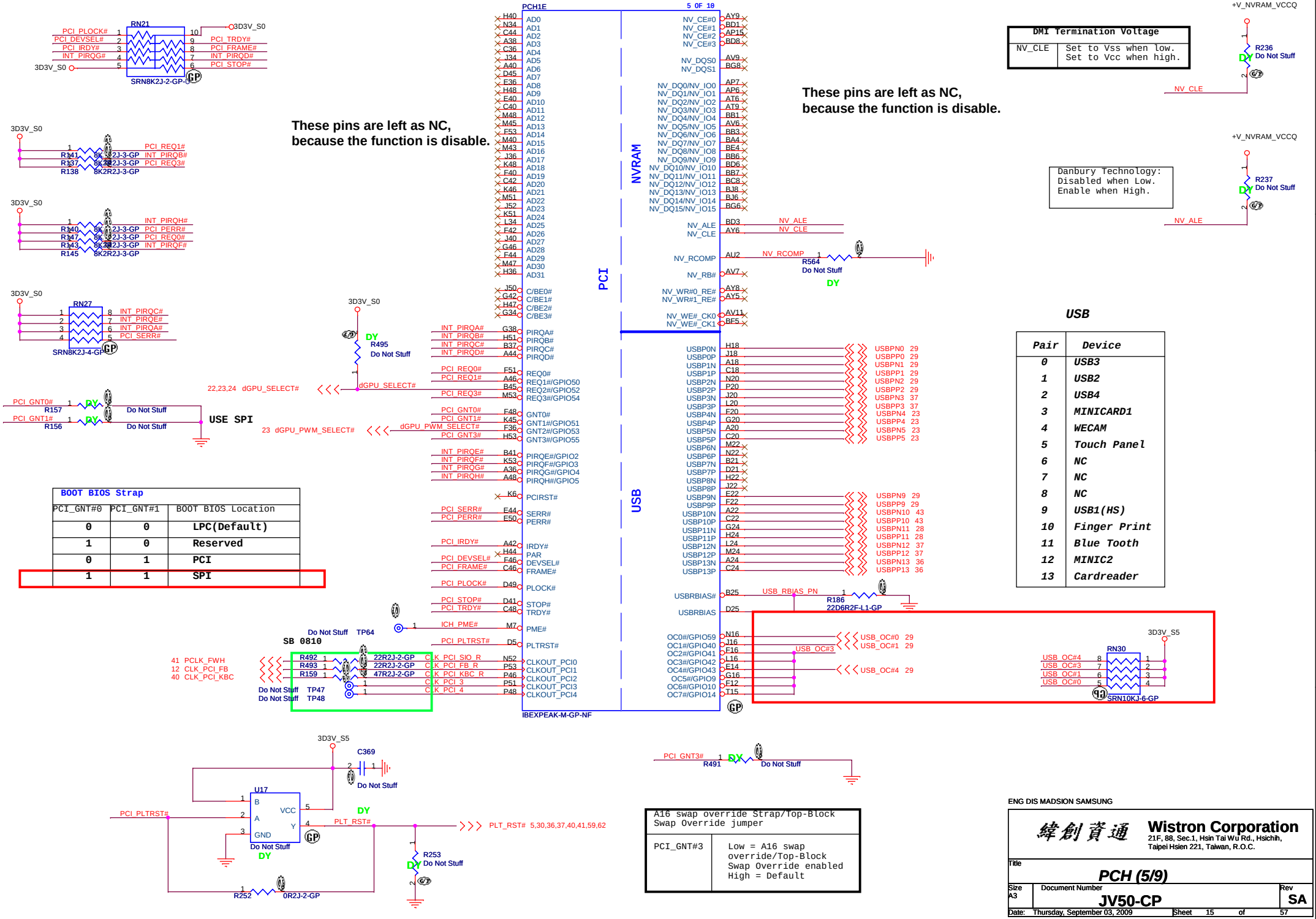
PCH1E
5 OF 10
PCI
NVRAM
USB
IBEXPEAK-M-GP-NF
These pins are left as NC, because the function is disable.
These pins are left as NC, because the function is disable.
USE SPI
SB 0810
Do Not Stuff TP64
Do Not Stuff TP47
Do Not Stuff TP48
Do Not Stuff
DY
Danbury Technology:
Disabled when Low.
Enable when High.
USB
Pair | Device
0 USB3
1 USB2
2 USB4
3 MINICARD1
4 WECAM
5 Touch Panel
6 NC
7 NC
8 NC
9 USB1(HS)
10 Finger Print
11 Blue Tooth
12 MINIC2
13 Cardreader
DMI Termination Voltage
NV_CLE | Set to Vss when low. Set to Vcc when high.
BOOT BIOS Strap
PCI_GNT#0 | PCI_GNT#1 | BOOT BIOS Location
0 | 0 | LPC(Default)
1 | 0 | Reserved
0 | 1 | PCI
1 | 1 | SPI
A16 swap override Strap/Top-Block Swap Override jumper
PCI_GNT#3 | Low = A16 swap override/Top-Block Swap Override enabled
High = Default
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (5/9)
Size A3
Document Number
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SA
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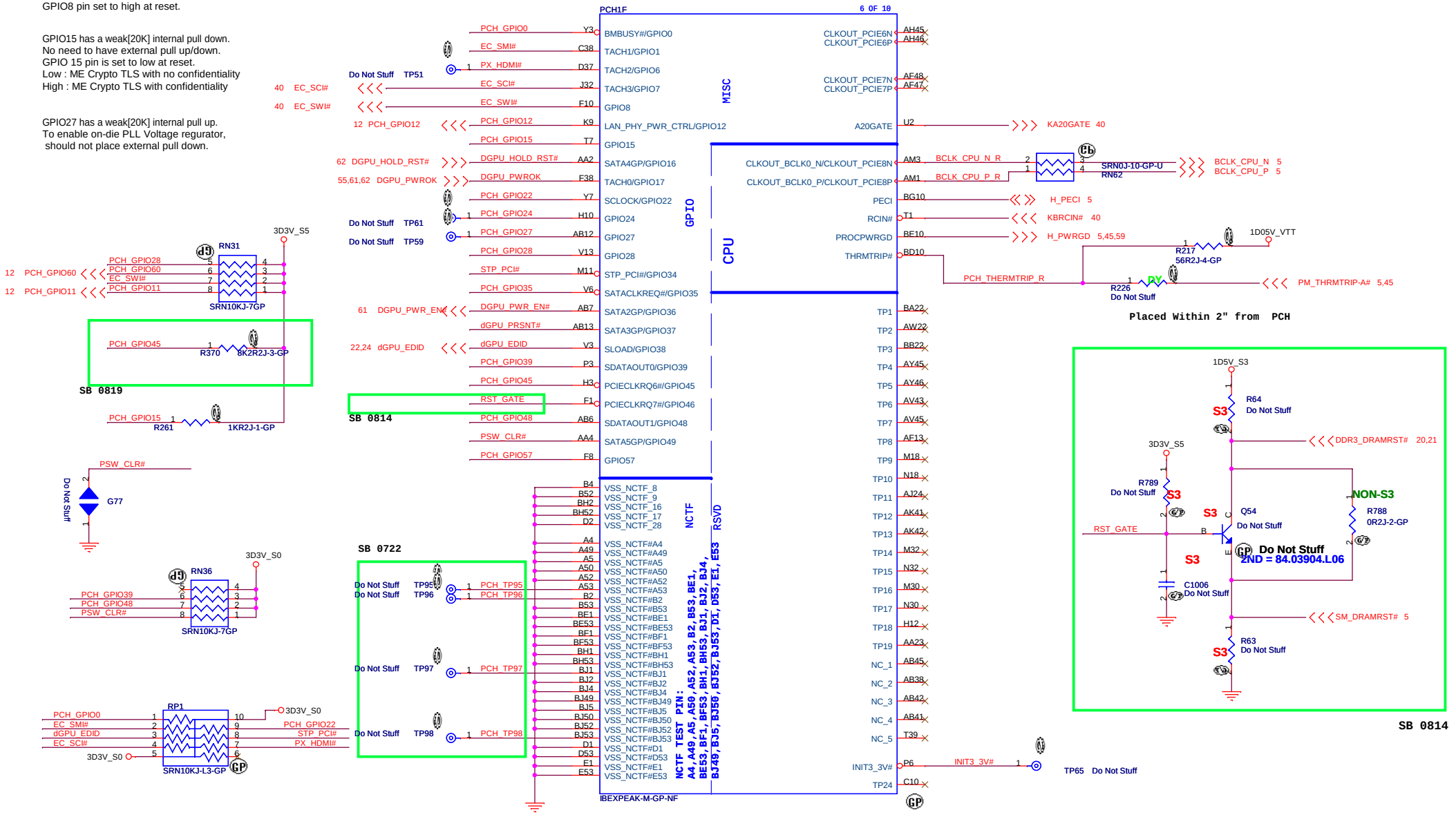
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.



ENG DIS MADSION SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (6/9)

Size	Document Number	Rev
A3	JV50-CP	SA

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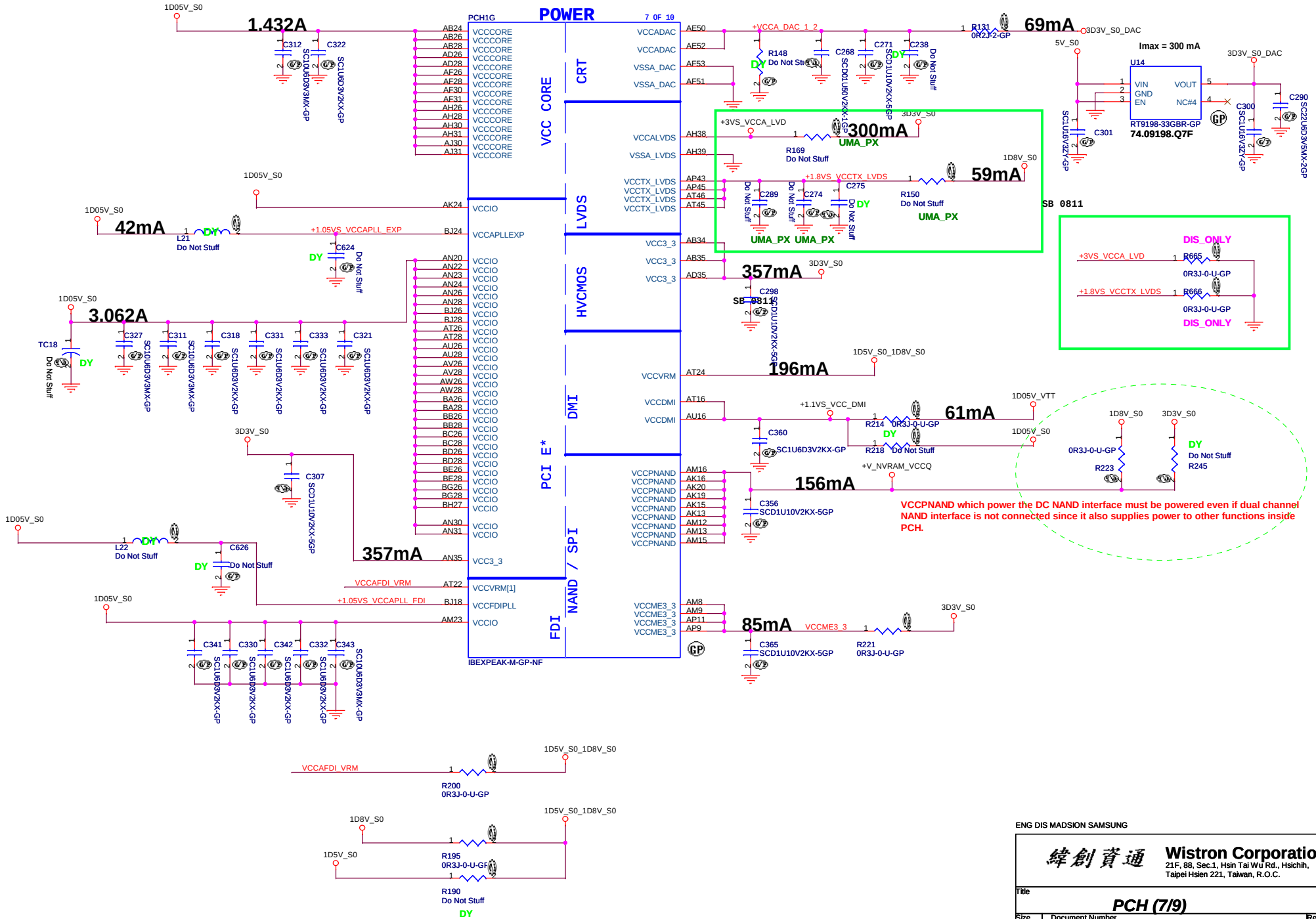
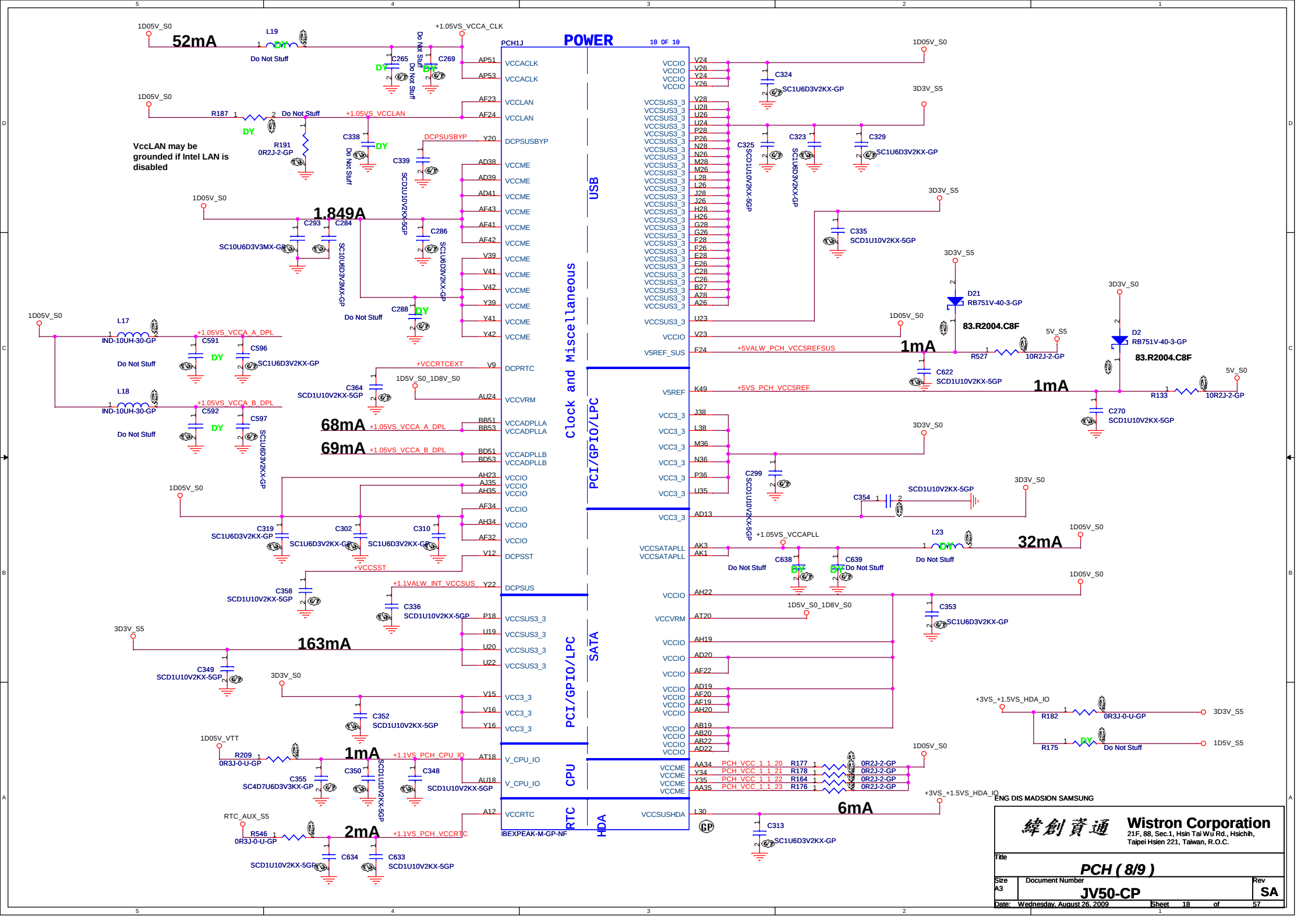

POWER
PCH1G
7 OF 10
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
1.432A
3.062A
42mA
357mA
357mA
196mA
61mA
156mA
85mA
69mA
300mA
59mA
Imax = 300 mA
VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.
DIS_ONLY
SB 0811
UMA_PX
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH (7/9)
JV50-CP
SA
Wednesday, August 26, 2009
17
57


POWER
10 OF 10
PCH1J
IBEXPEAK-M-GP-NF
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
52mA
1.849A
163mA
68mA
69mA
1mA
2mA
6mA
32mA
1mA
1mA
1D05V_S0
3D3V_S5
3D3V_S0
5V_S5
5V_S0
1D05V_VTT
RTC_AUX_S5
+1.05VS_VCCA_CLK
+1.05VS_VCCLAN
+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL
+VCCRTCEXT
+VCCSST
+1.1VALW_INT_VCCSUS
+1.05VS_VCCAPLL
+1.1VS_PCH_CPU_IO
+1.1VS_PCH_VCCRTC
+5VALW_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
1D05V_S0_1D8V_S0
+3VS_+1.5VS_HDA_IO
L19
L17
L18
L23
IND-10UH-30-GP
Do Not Stuff
DY
VccLAN may be grounded if Intel LAN is disabled
D21
RB751V-40-3-GP
83.R2004.C8F
D2
RB751V-40-3-GP
83.R2004.C8F
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (8/9)
Size
A3
Document Number
JV50-CP
Rev
SA
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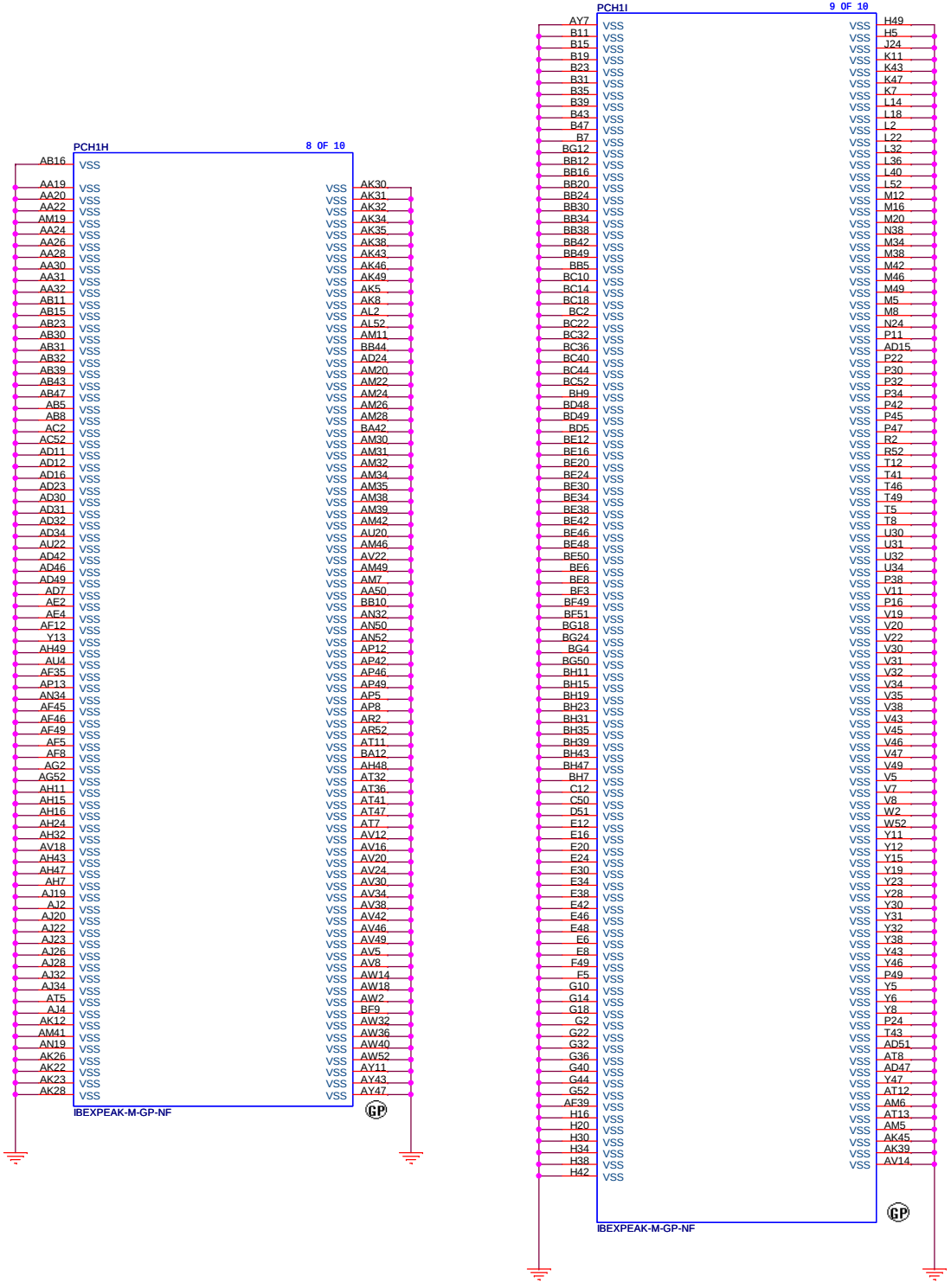

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (9/9)***

Size	Document Number	Rev
A3	JV50-CP	SA

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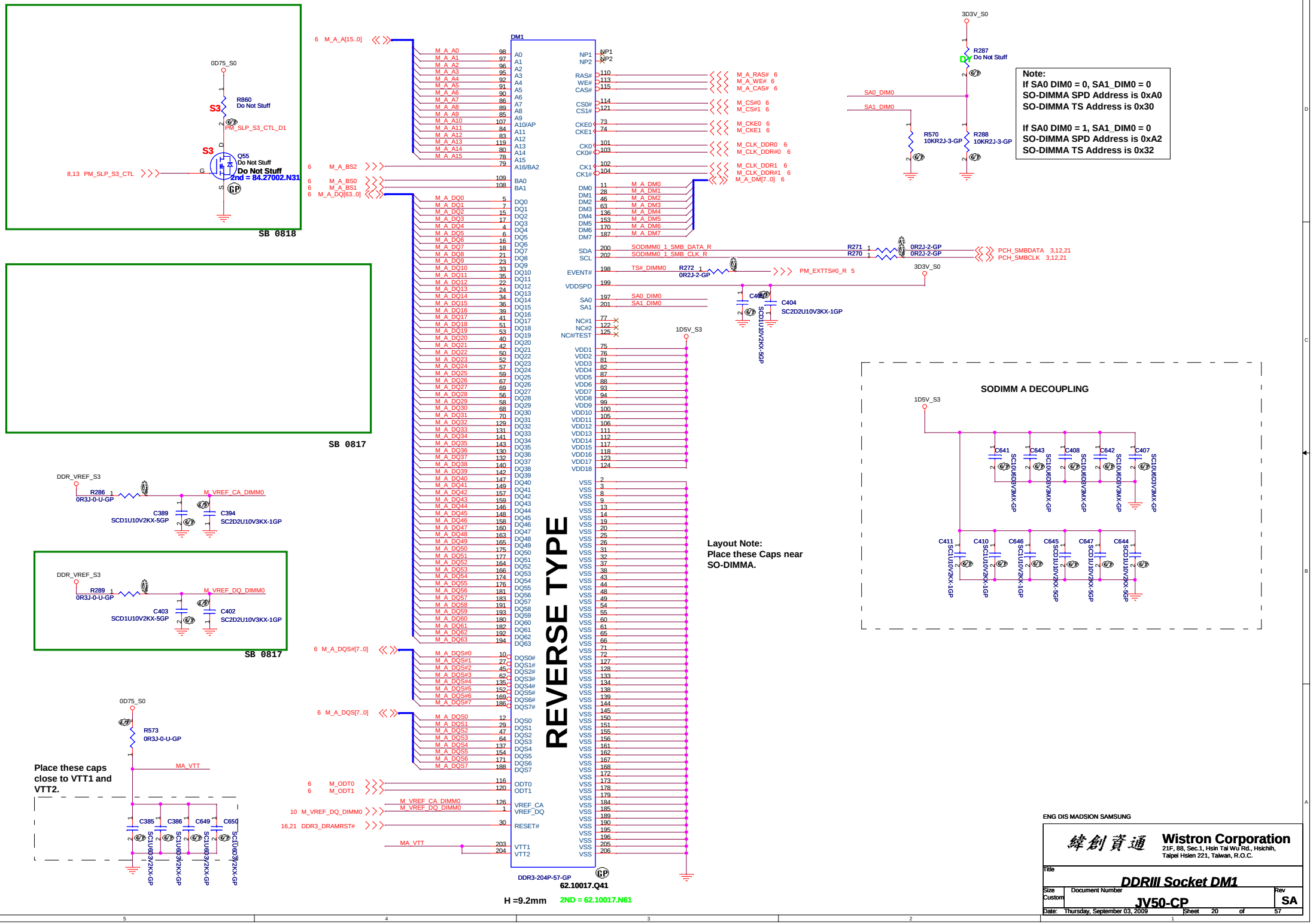
DM1
REVERSE TYPE
DDR3-204P-57-GP
62.10017.Q41
H =9.2mm
2ND = 62.10017.N61
SB 0818
SB 0817
SB 0817
SODIMM A DECOUPLING
Layout Note:
Place these Caps near
SO-DIMMA.
Place these caps
close to VTT1 and
VTT2.
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDRIII Socket DM1
JV50-CP
SA
Thursday, September 03, 2009
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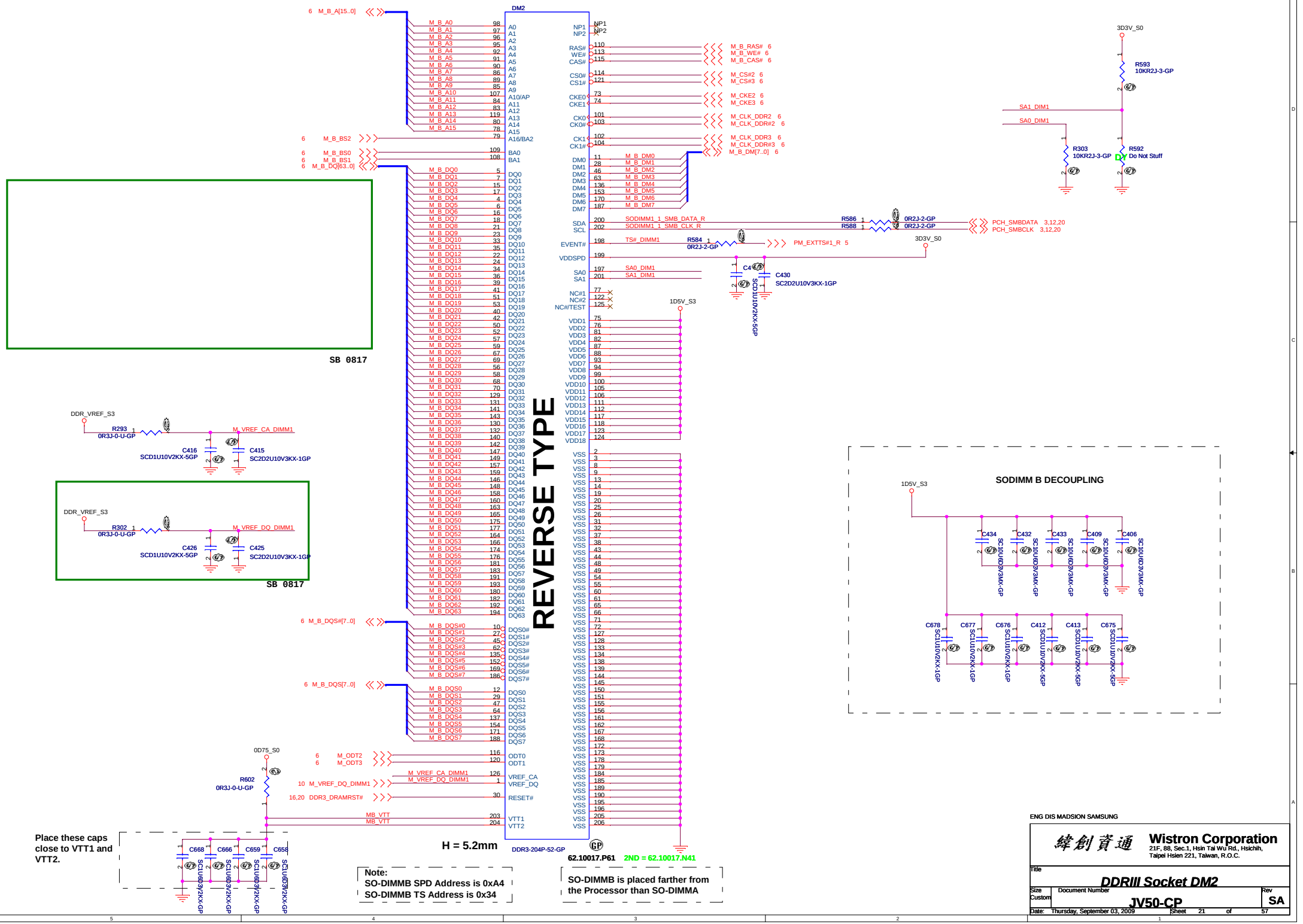
57


DM2
REVERSE TYPE
SB 0817
SB 0817
SODIMM B DECOUPLING
Place these caps close to VTT1 and VTT2.
H = 5.2mm
DDR3-204P-52-GP
62.10017.P61
2ND = 62.10017.N41
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SO-DIMMB is placed farther from the Processor than SO-DIMMA
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRIII Socket DM2
Size
Custom
Document Number
JV50-CP
Rev
SA
Date: Thursday, September 03, 2009
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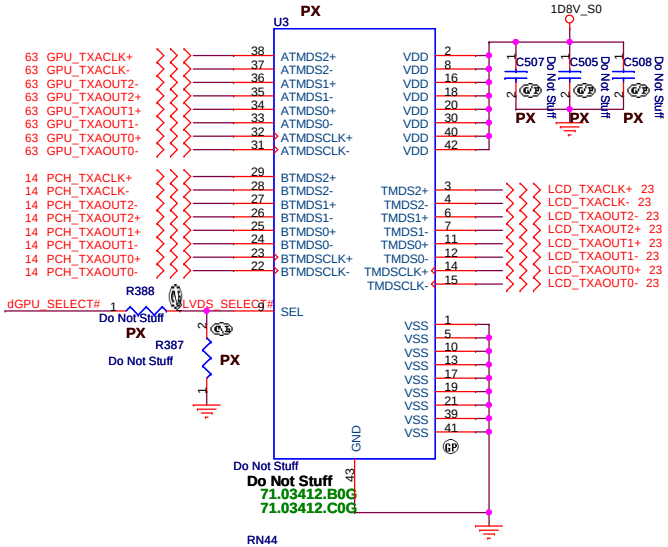
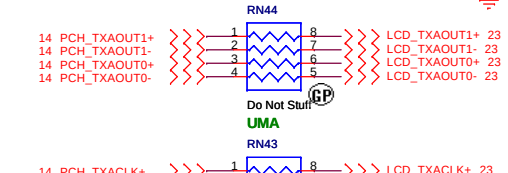
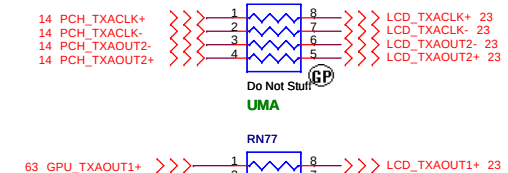
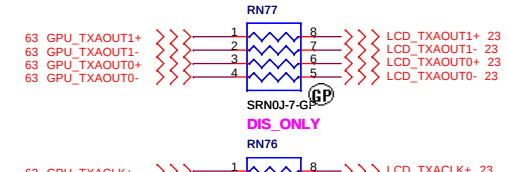
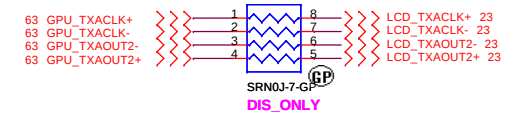
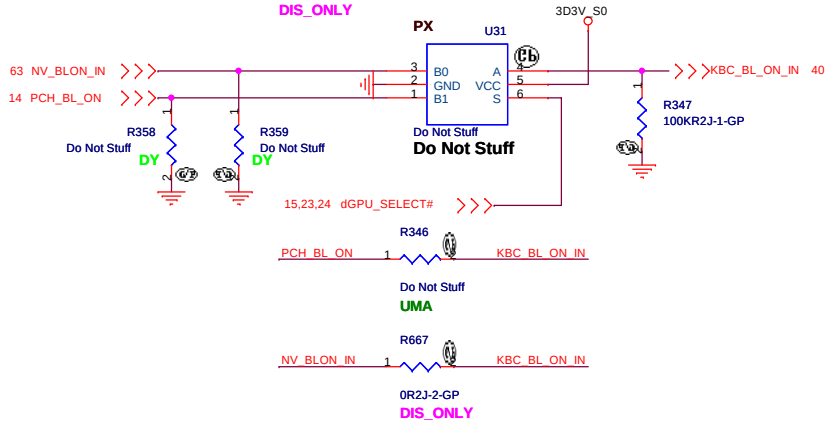






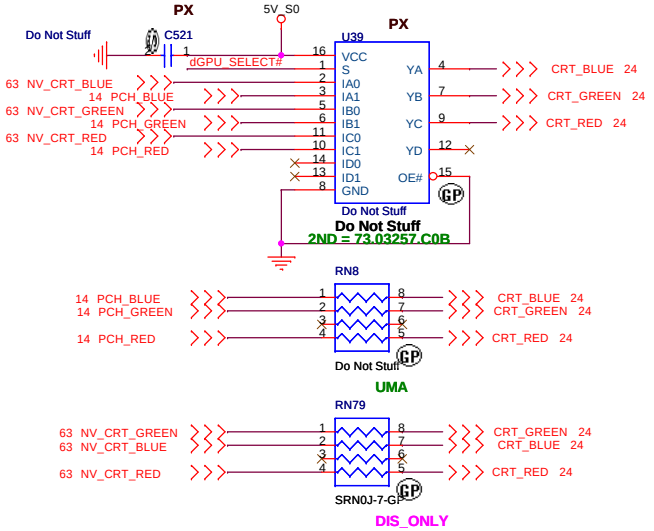


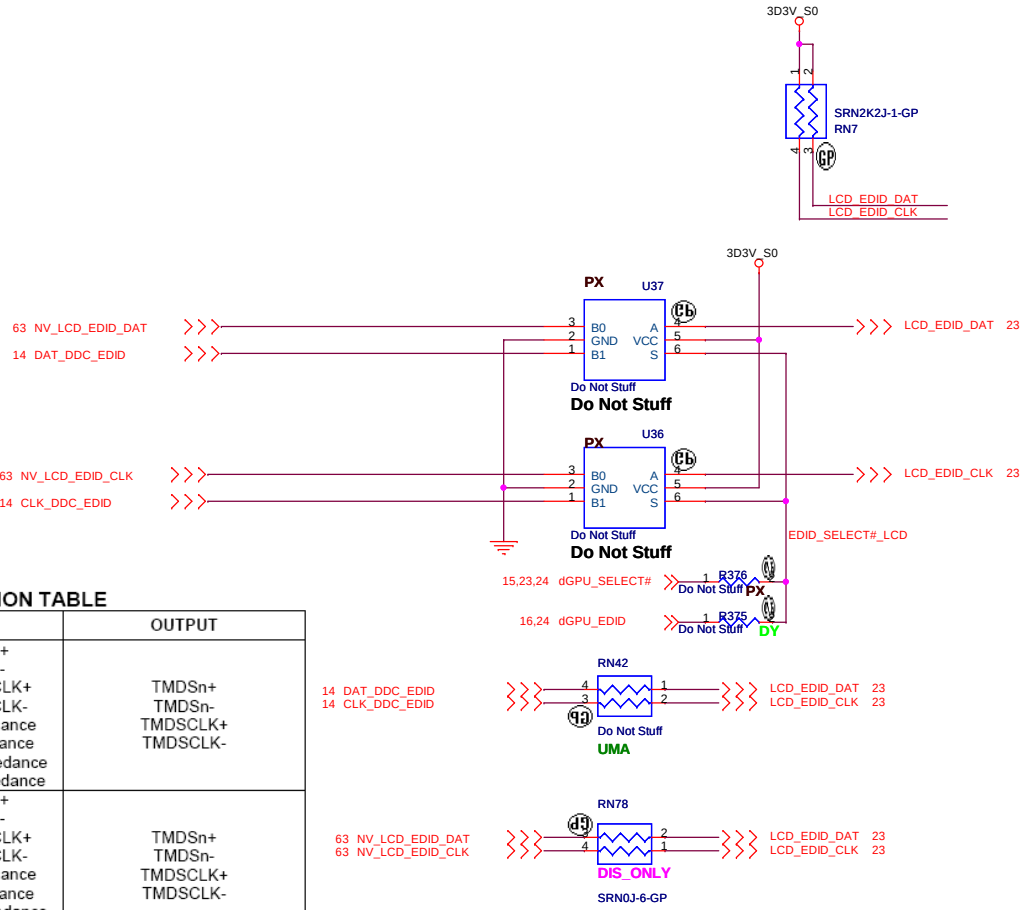




FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-





$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PX SWITCH

Size: A3 | Document Number: JV50-CP | Rev: SA

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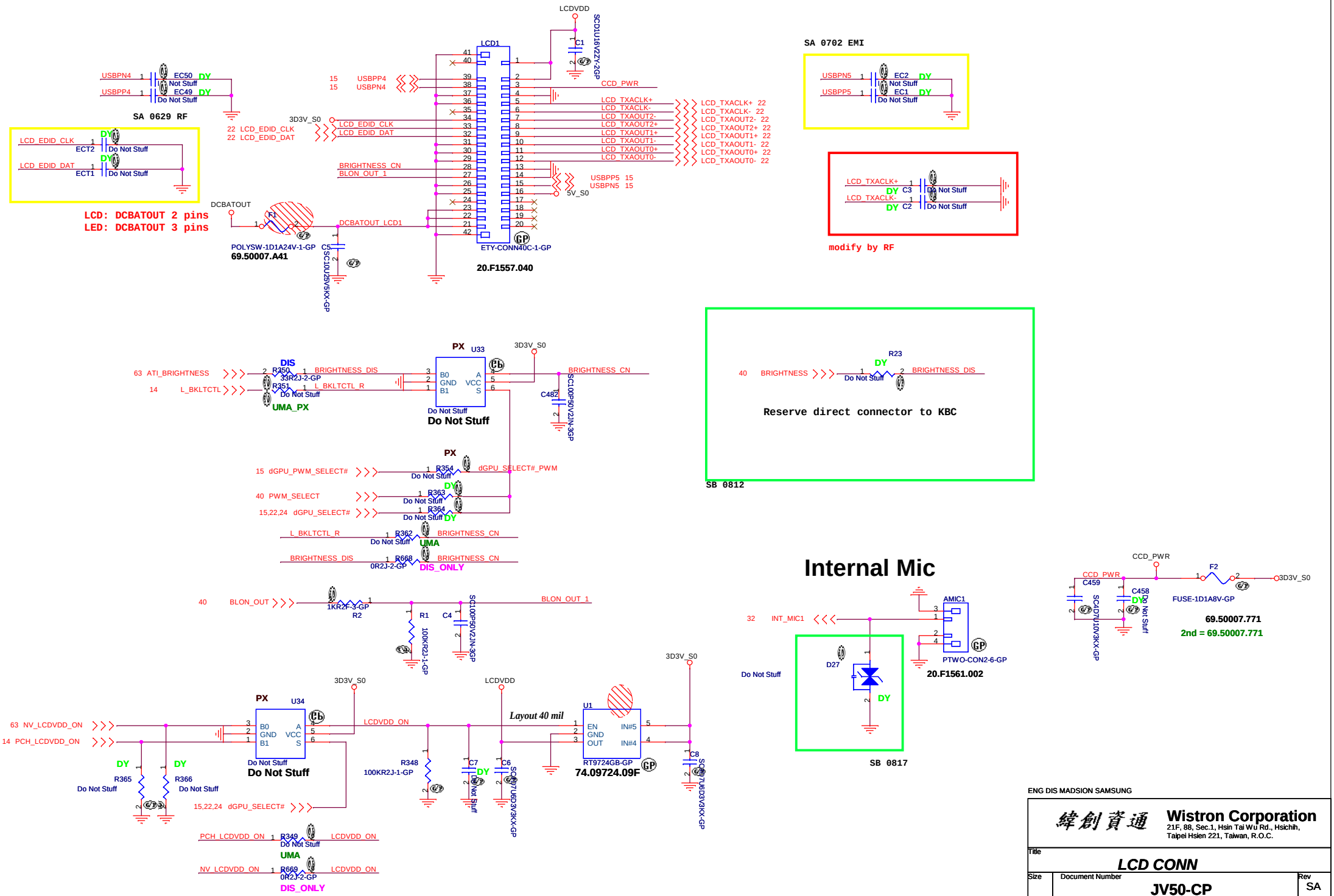
LCD/INVERTER/CCD CONN



ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD CONN		
Size	Document Number: JV50-CP	Rev: SA
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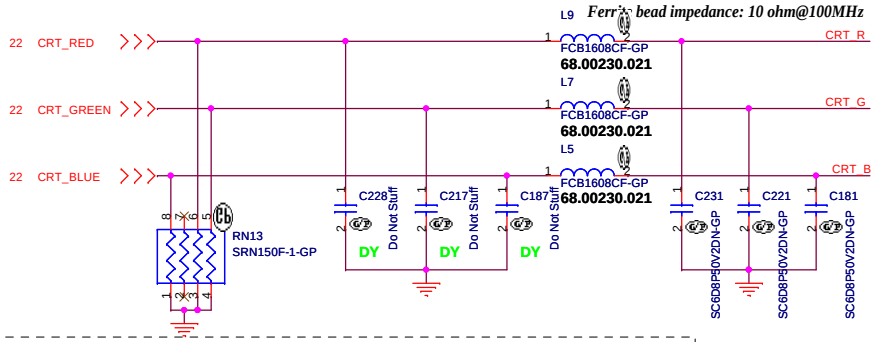
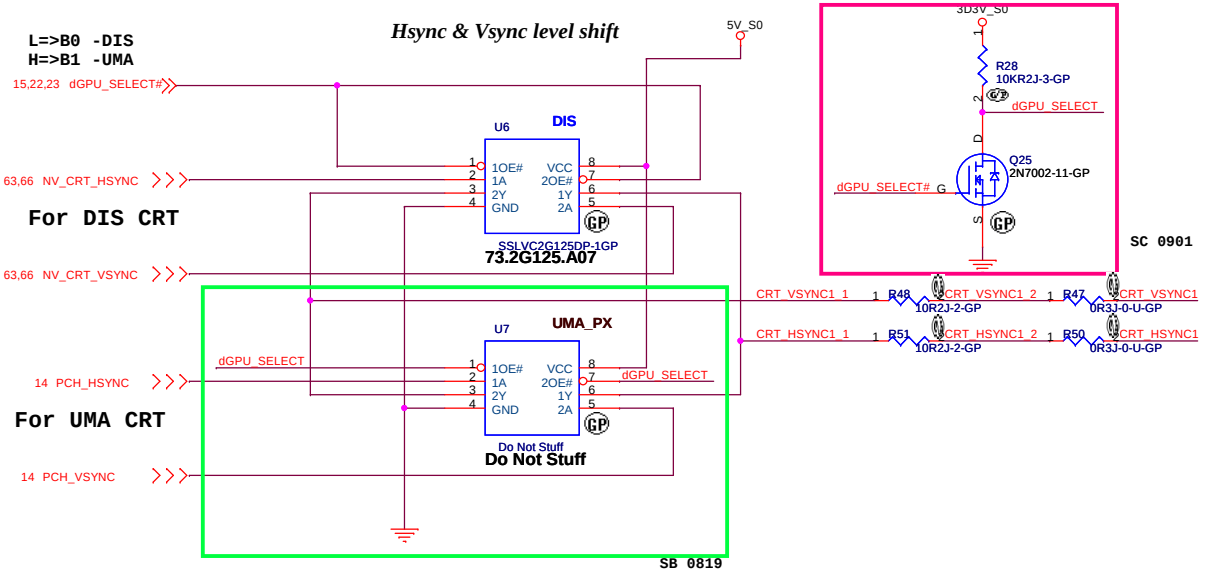
Layout Note:
Place these resistors close to the CRT-out connector

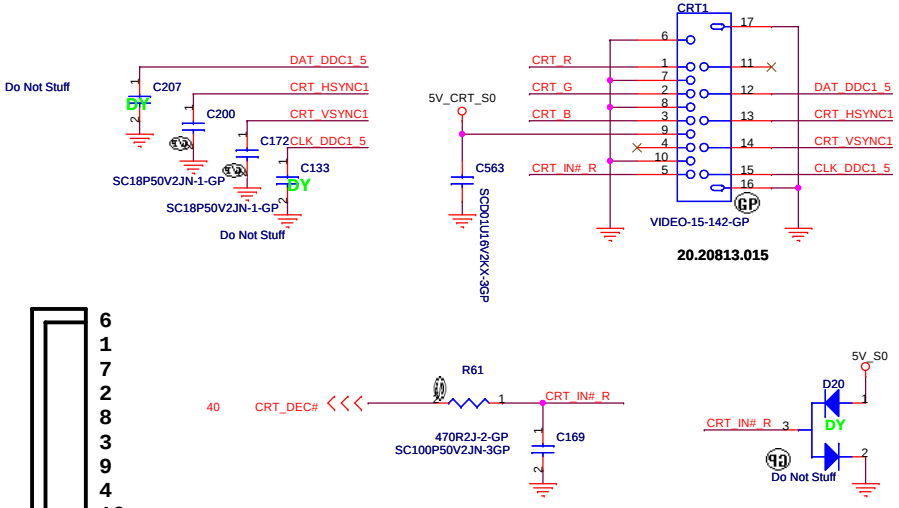


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

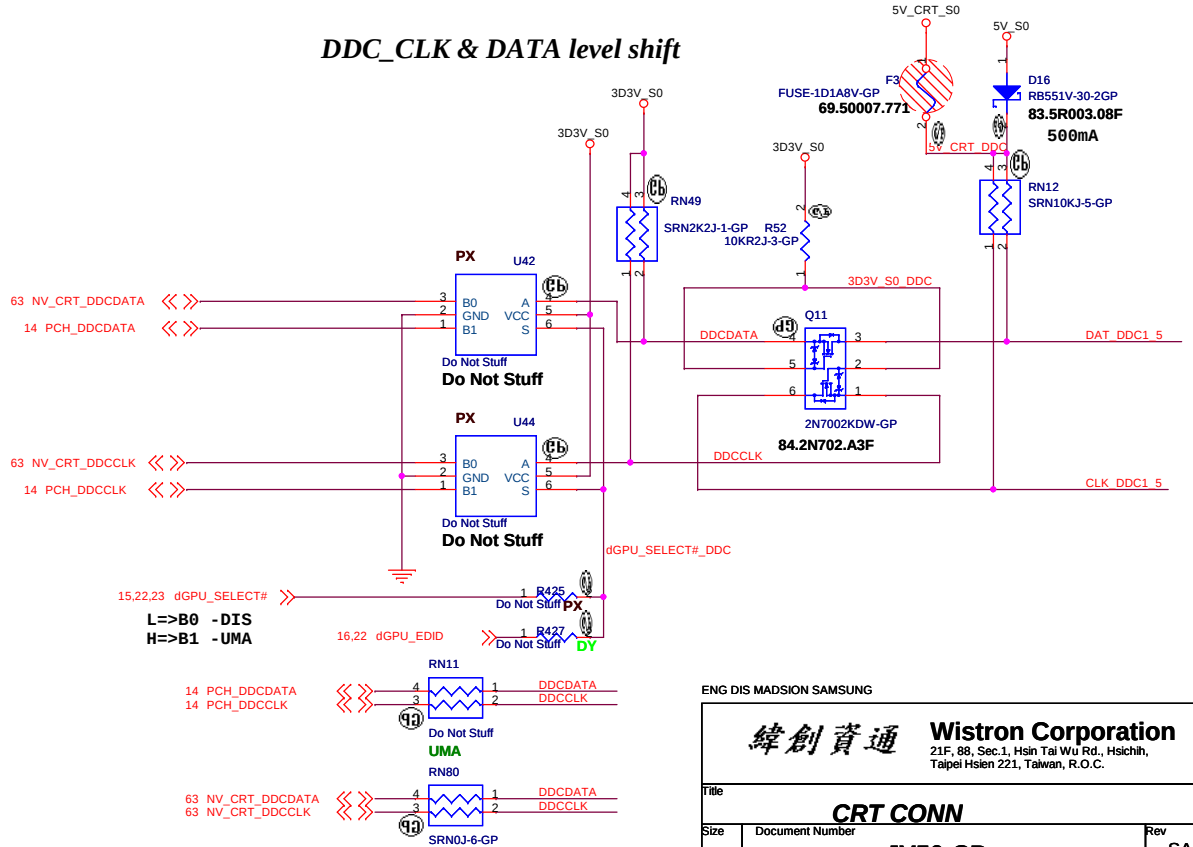
Hsync & Vsync level shift



CRT I/F & CONNECTOR



DDC_CLK & DATA level shift



ENG DIS MADSION SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	***CRT CONN***	
Size	Document Number: **JV50-CP**	Rev: SA
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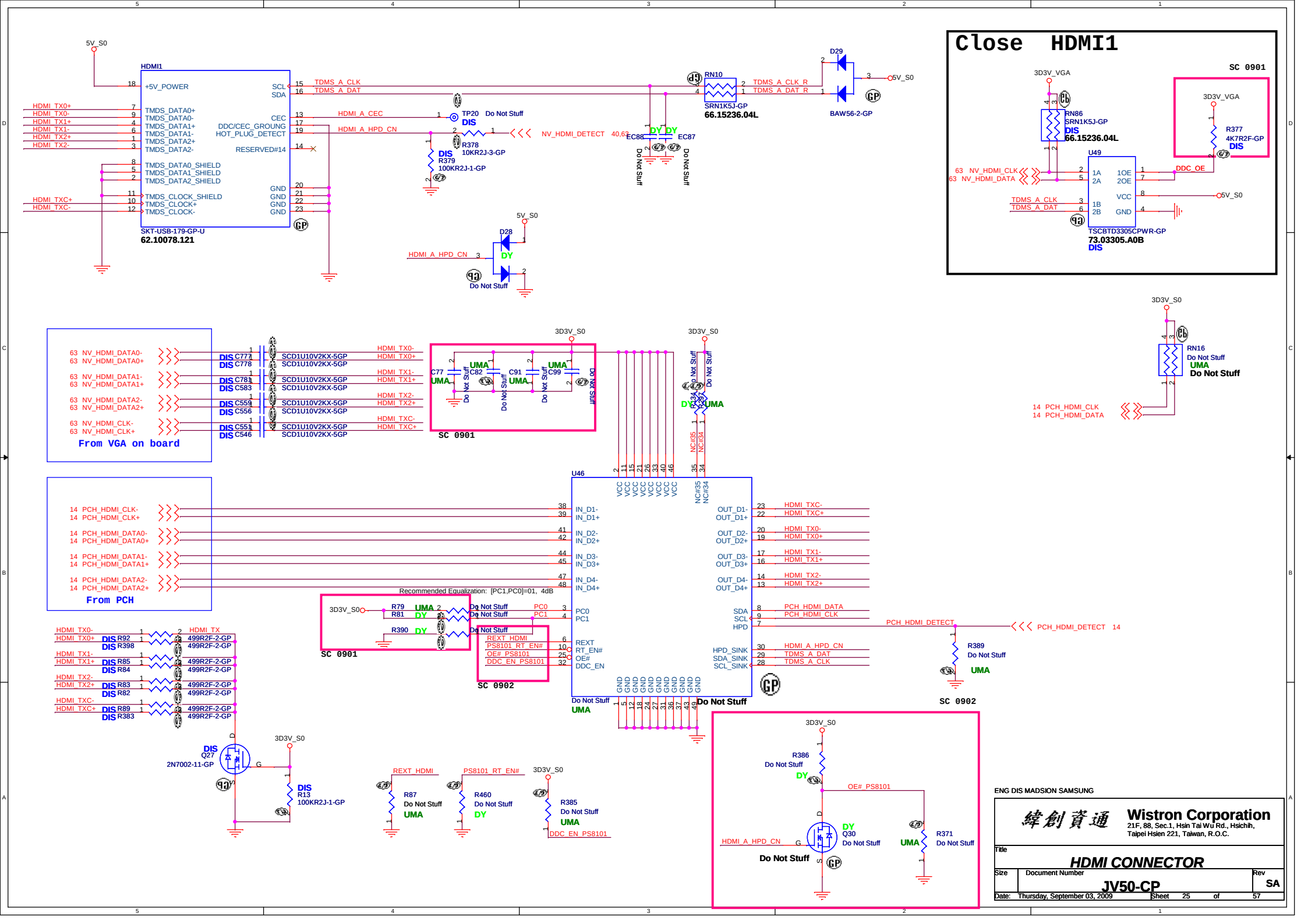
Close HDMI1
SC 0901
HDMI1
SKT-USB-179-GP-U
62.10078.121
+5V_POWER
TMDS_DATA0+
TMDS_DATA0-
TMDS_DATA1+
TMDS_DATA1-
TMDS_DATA2+
TMDS_DATA2-
TMDS_DATA0_SHIELD
TMDS_DATA1_SHIELD
TMDS_DATA2_SHIELD
TMDS_CLOCK_SHIELD
TMDS_CLOCK+
TMDS_CLOCK-
SCL
SDA
CEC
DDC/CEC_GROUNG
HOT_PLUG_DETECT
RESERVED#14
GND
TDMS_A_CLK
TDMS_A_DAT
HDMI_A_CEC
HDMI_A_HPD_CN
TP20 Do Not Stuff
DIS
R378 10KR2J-3-GP
R379 100KR2J-1-GP
NV_HDMI_DETECT 40,63
EC88
EC87
RN10
SRN1K5J-GP
66.15236.04L
TDMS_A_CLK_R
TDMS_A_DAT_R
D29
BAW56-2-GP
D28
3D3V_VGA
RN86
R377 4K7R2F-GP
U49
TSCBTD3305CPWR-GP
73.03305.A0B
DDC_OE
63 NV_HDMI_CLK
63 NV_HDMI_DATA
From VGA on board
SCD1U10V2KX-5GP
C777
C778
C781
C583
C559
C556
C551
C546
C77
C82
C91
C99
RN16
14 PCH_HDMI_CLK
14 PCH_HDMI_DATA
From PCH
U46
IN_D1-
IN_D1+
IN_D2-
IN_D2+
IN_D3-
IN_D3+
IN_D4-
IN_D4+
OUT_D1-
OUT_D1+
OUT_D2-
OUT_D2+
OUT_D3-
OUT_D3+
OUT_D4-
OUT_D4+
SDA
SCL
HPD
HPD_SINK
SDA_SINK
SCL_SINK
PC0
PC1
REXT
RT_EN#
OE#
DDC_EN
Recommended Equalization: [PC1,PC0]=01, 4dB
R79 UMA
R81 DY
R390 DY
REXT_HDMI
PS8101_RT_EN#
OE#_PS8101
DDC_EN_PS8101
SC 0902
PCH_HDMI_DETECT
R389 Do Not Stuff UMA
R92 R398
R85 R84
R83 R82
R89 R383
499R2F-2-GP
Q27 2N7002-11-GP
R13 100KR2J-1-GP
R87 Do Not Stuff UMA
R460 Do Not Stuff DY
R385 Do Not Stuff UMA
R386 Do Not Stuff DY
Q30 Do Not Stuff
R371 Do Not Stuff UMA
ENG DIS MADSION SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI CONNECTOR
Size
Document Number
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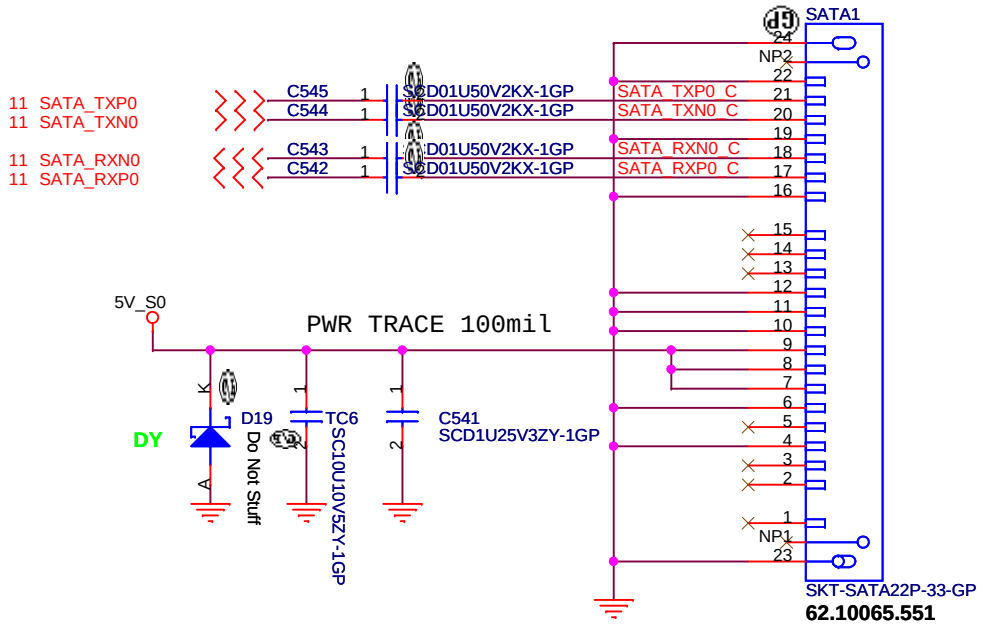
SATA Connector



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Title	***HDD CONN***	
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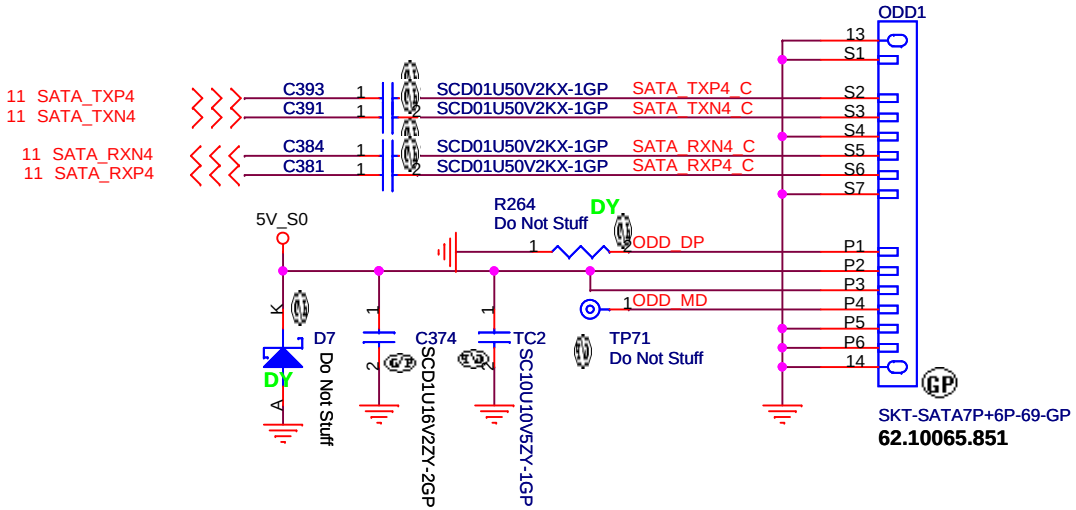
ODD Connector



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Title: ODD		
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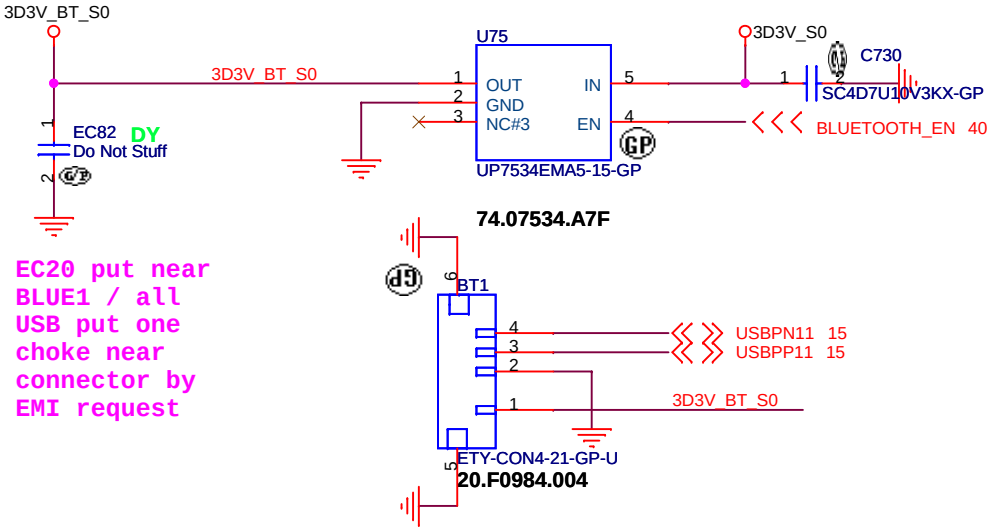
BLUETOOTH MODULE



EC20 put near BLUE1 / all USB put one choke near connector by EMI request

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Title: BLUETOOTH		
Size	Document Number: JV50-CP	Rev: SA
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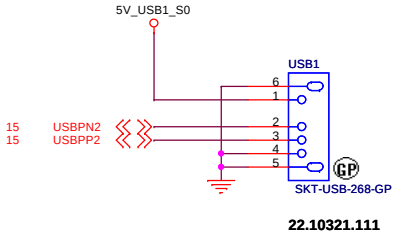

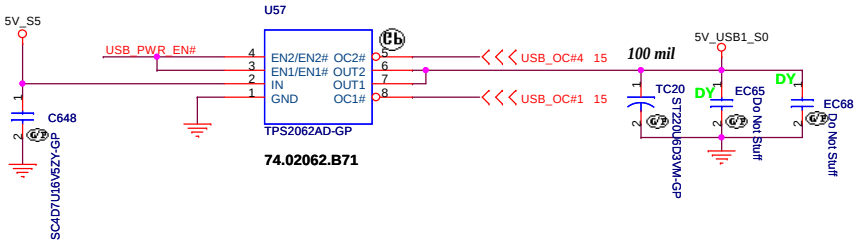

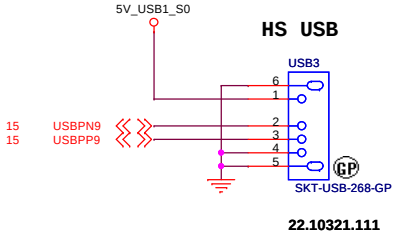

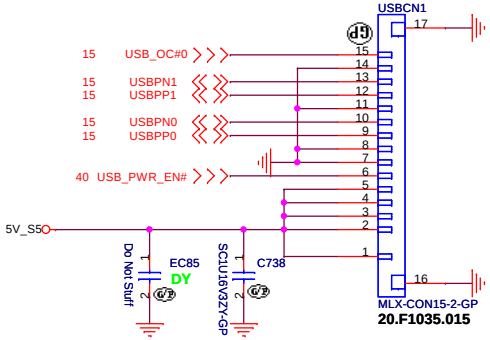

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Taipei Hsien 221, Taiwan, R.O.C.

Title	USB CONN	
Size	Document Number JV50-CP	Rev SA
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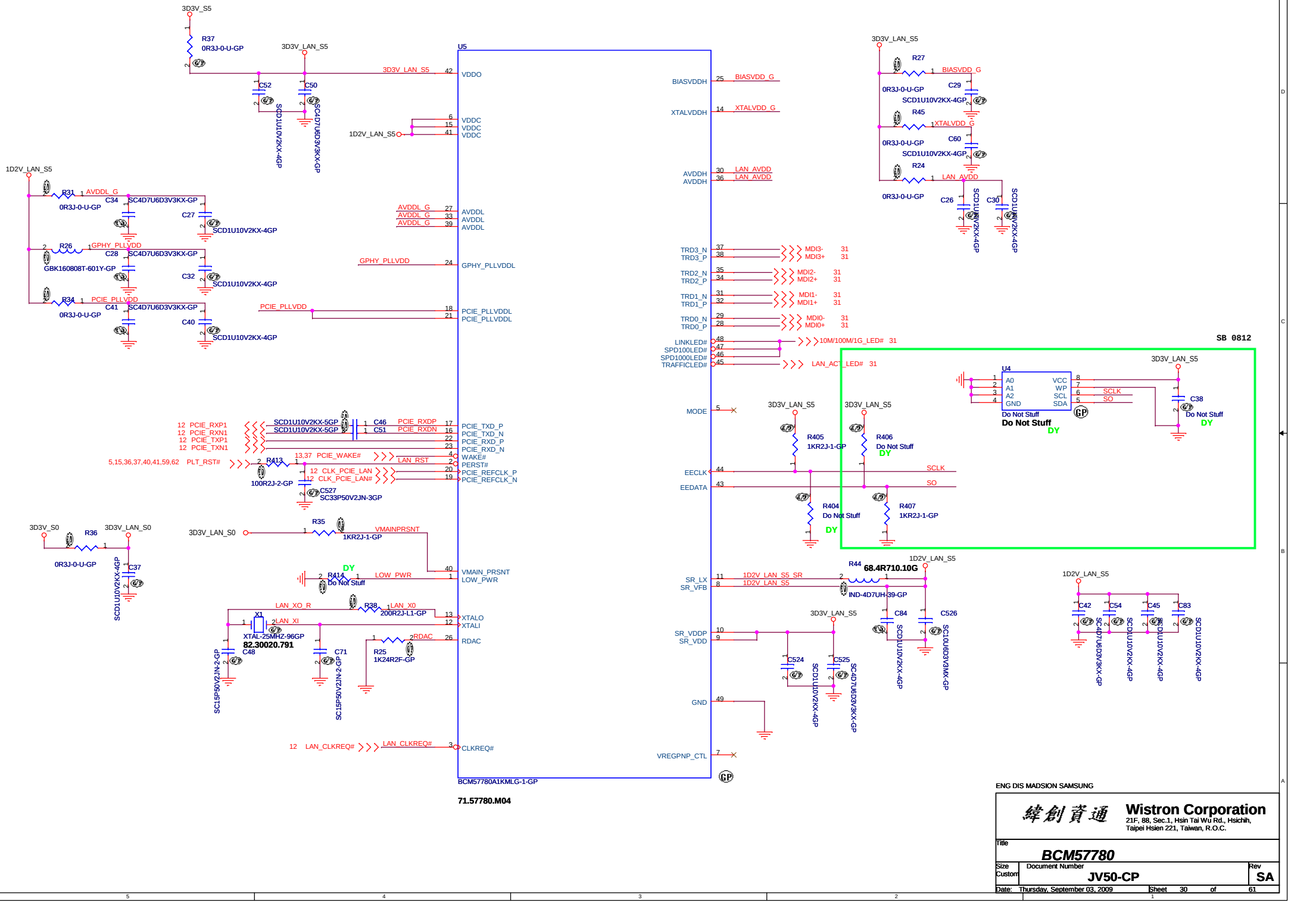
U5
BCM57780A1KMLG-1-GP
71.57780.M04
SB 0812
Do Not Stuff
DY
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM57780
Size
Custom
Document Number
JV50-CP
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SA
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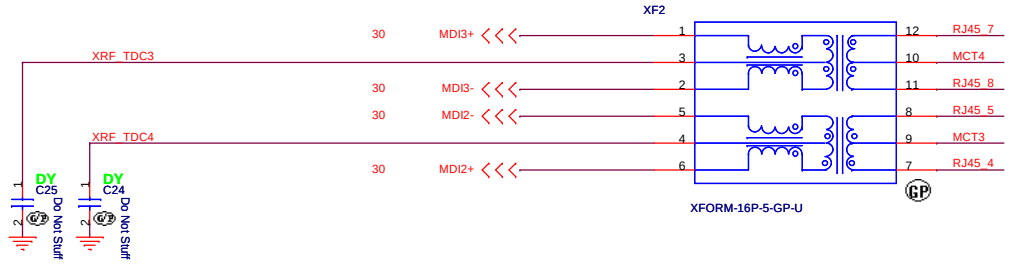
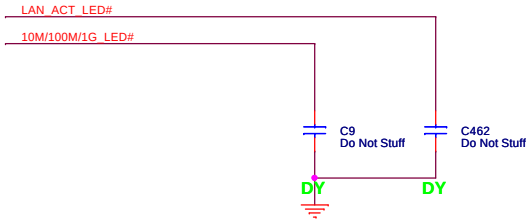
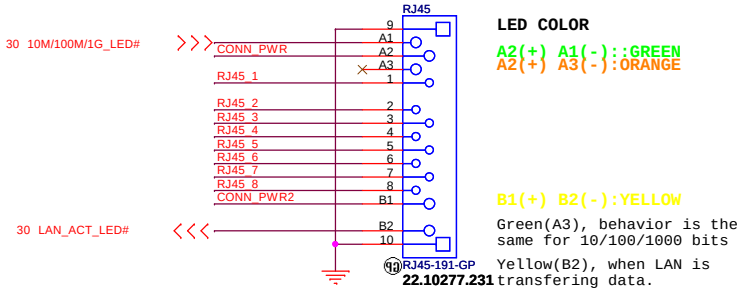
LAN Connector

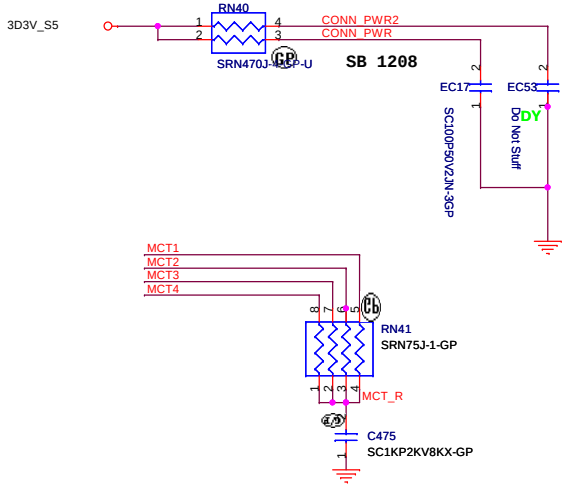
LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.









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Title			
LAN CONN			
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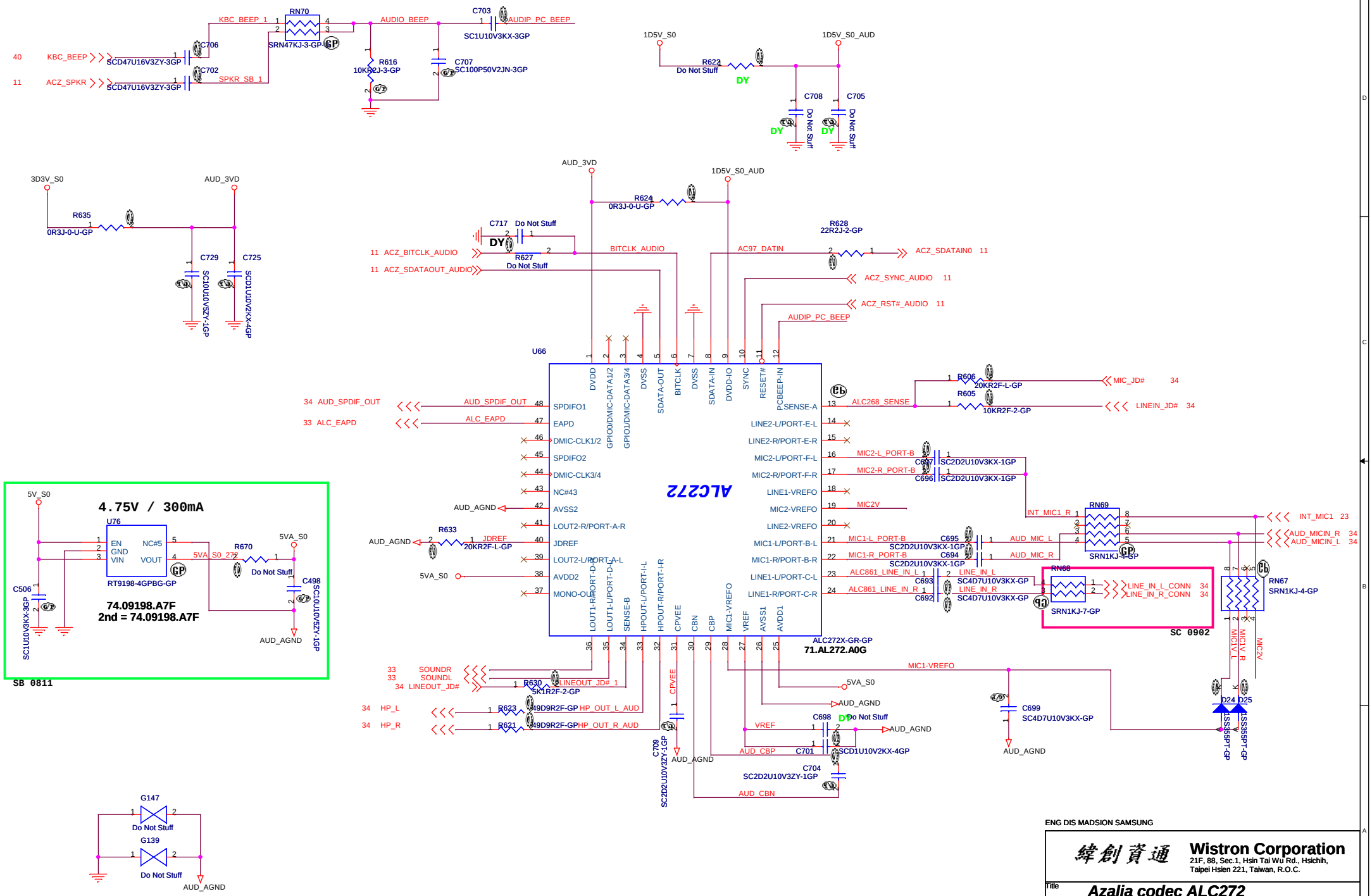

ENG DIS MADSION SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Azalia codec ALC272***	
Size A3	Document Number **JV50-CP**	Rev **SA**
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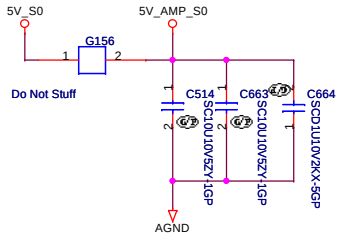
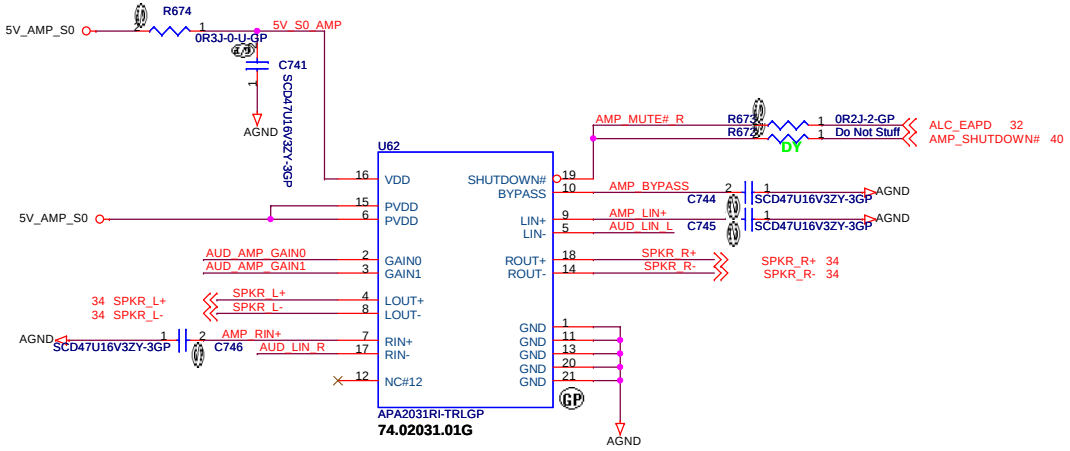
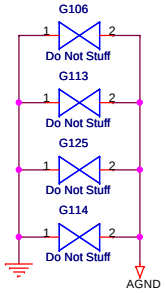
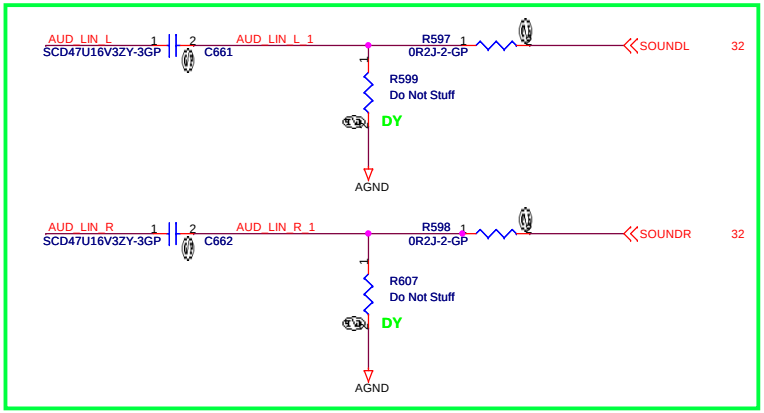


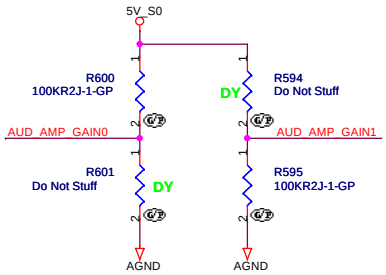






SB 0814

GAIN SETTING



GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

ENG DIS MADSION SAMSUNG

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Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP

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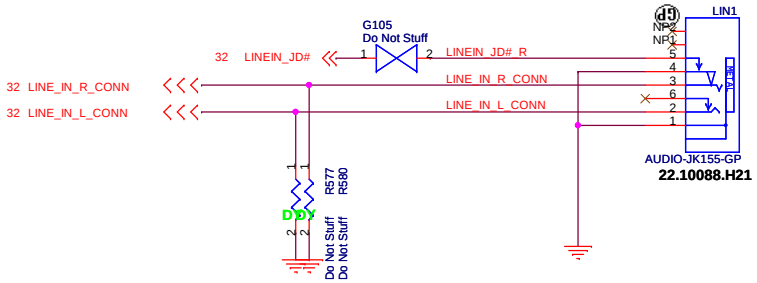
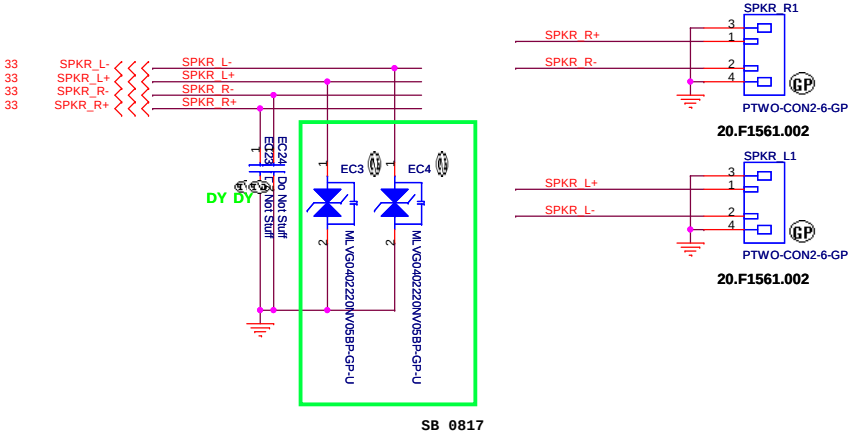
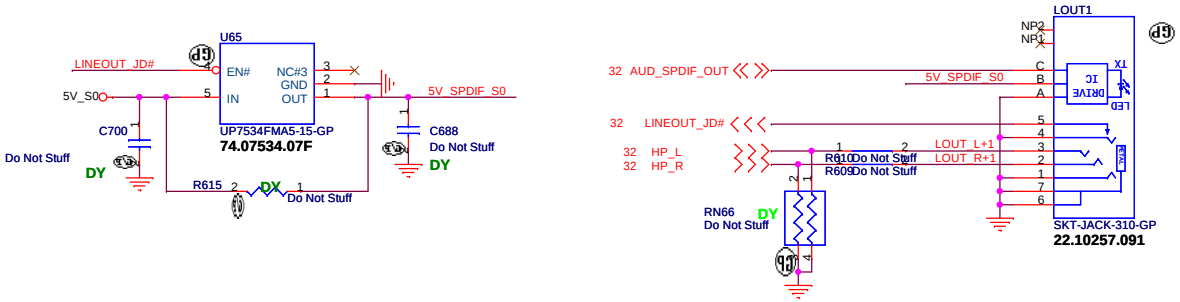
LINE IN

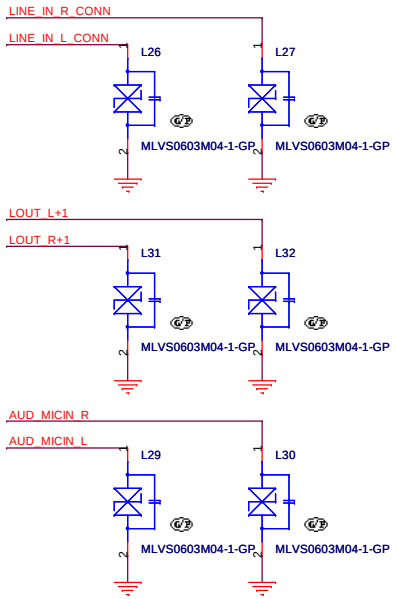


Internal Speaker

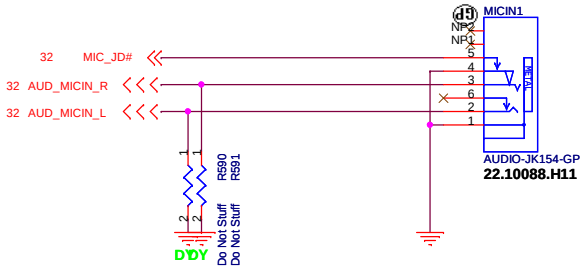


LINE OUT





MIC IN



ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	*AUDIO jack*	
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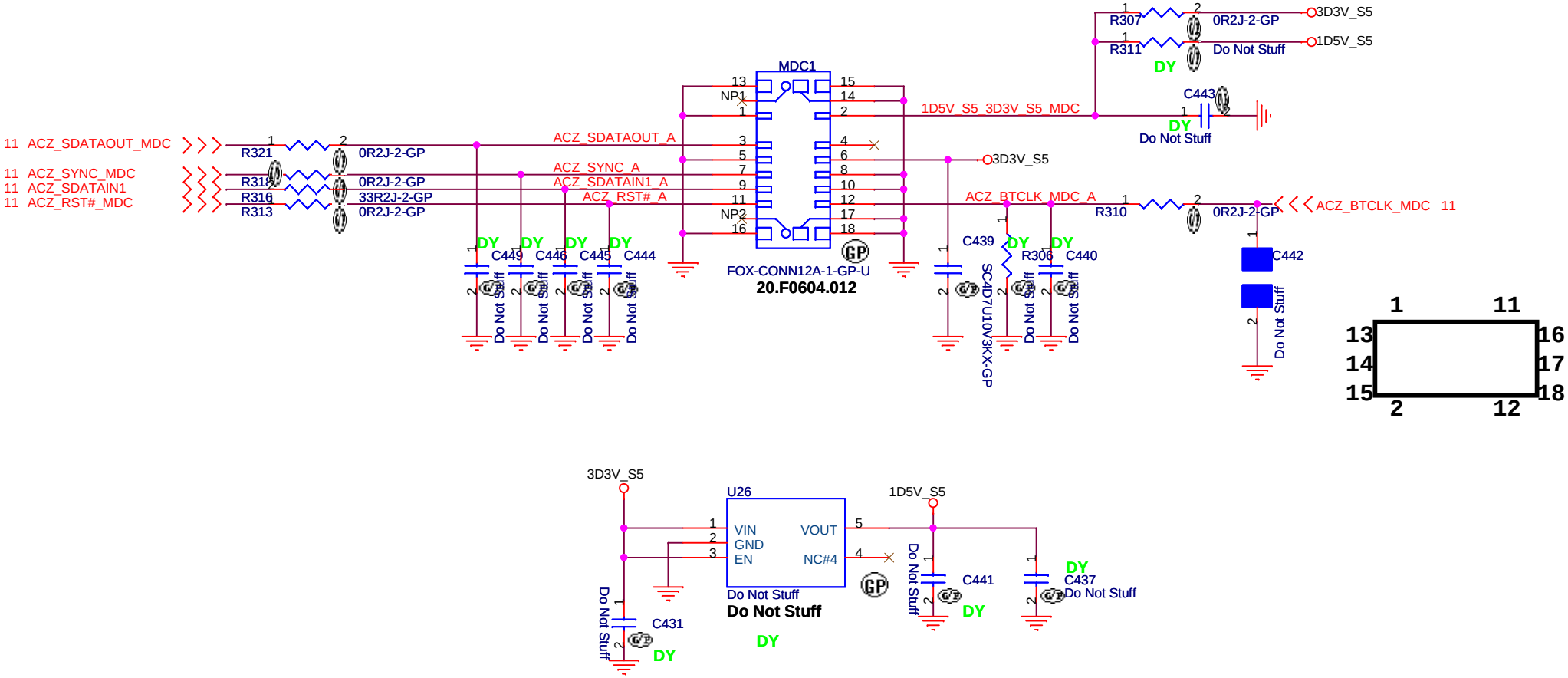
MDC 1.5 CONN



ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MDC	
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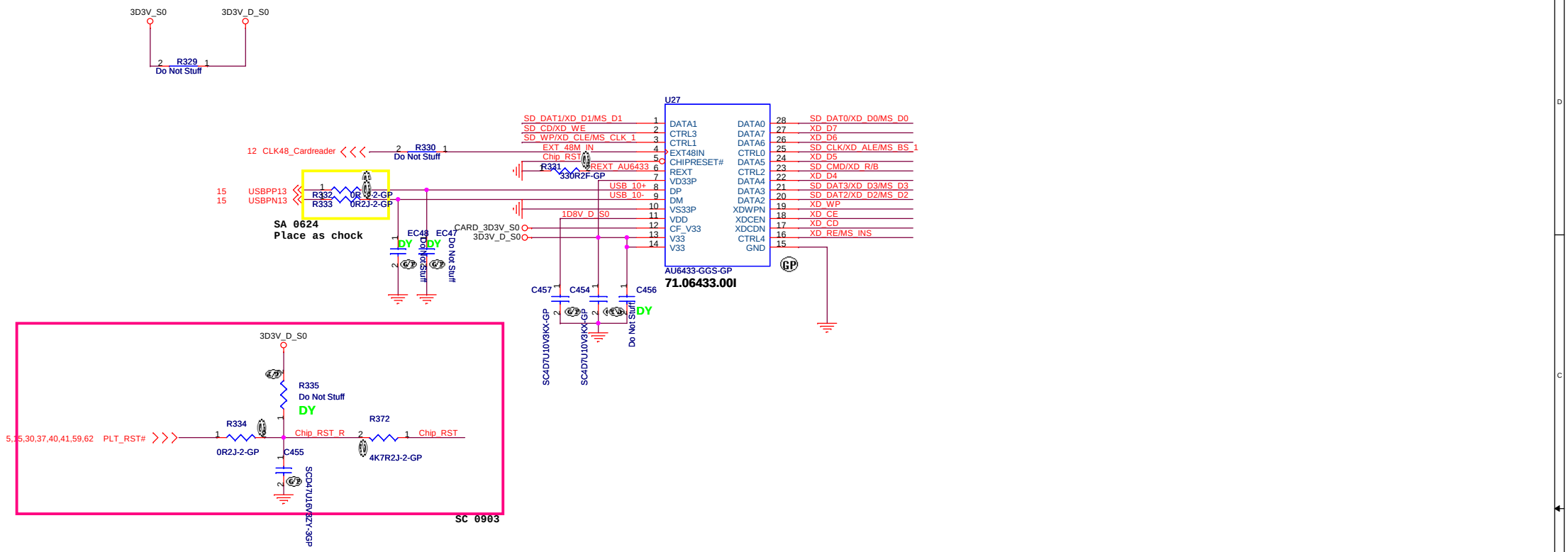
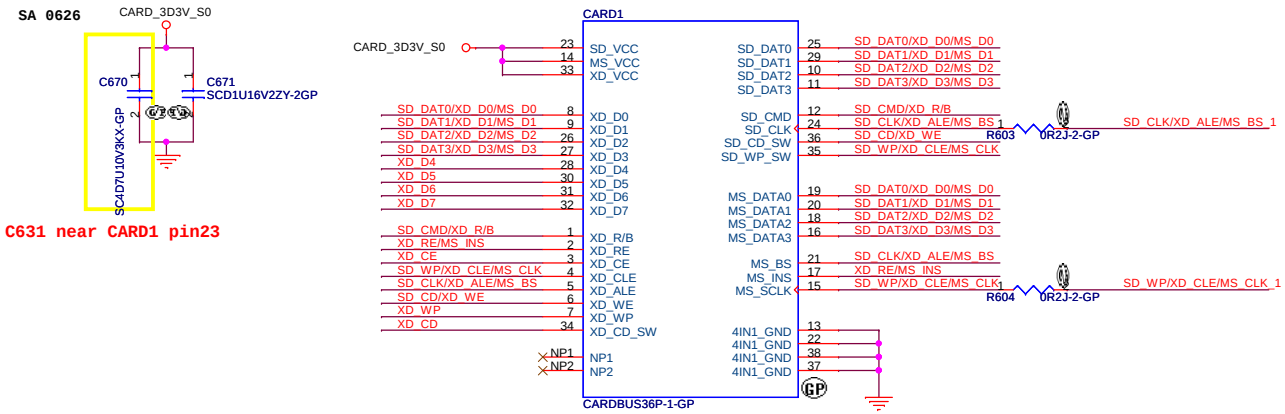
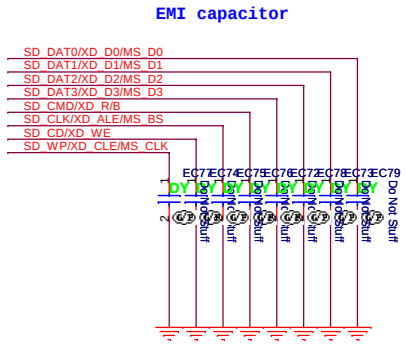


5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)





ENG DIS MADSION SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: *Cardreader*		
Size	Document Number: JV50-CP	Rev: SA
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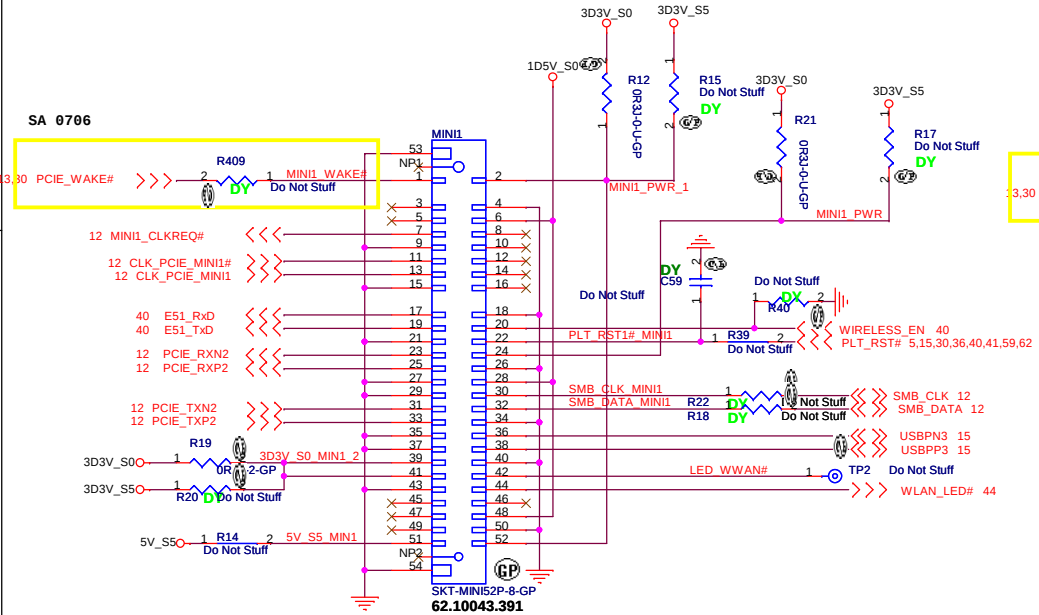
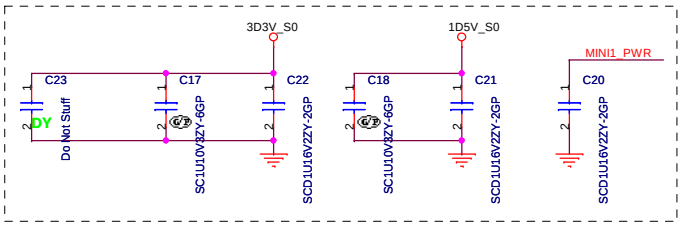
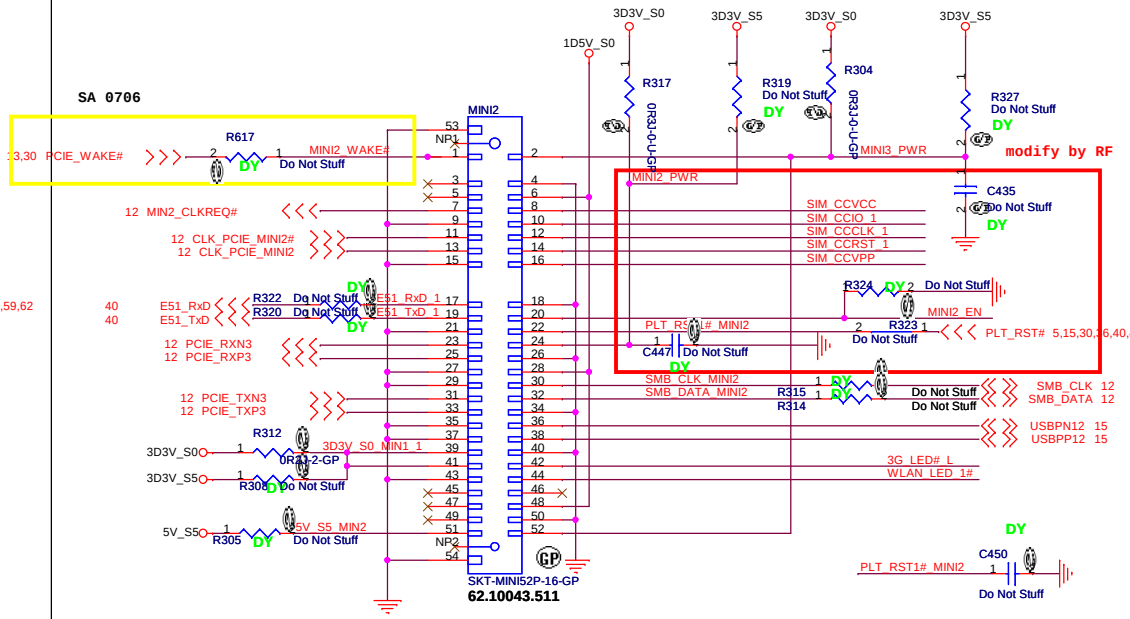
Mini Card Connector(WLAN)
Support debug-card

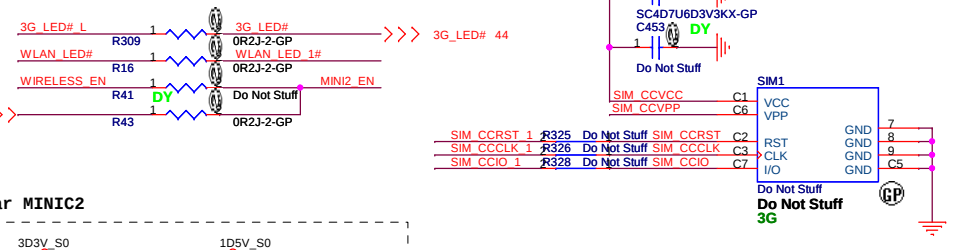


Place near MINI1

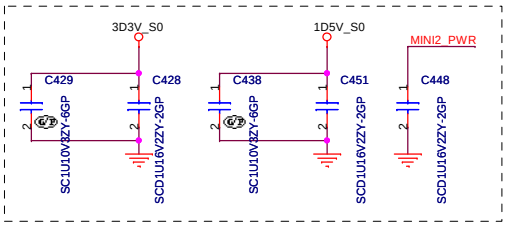


Mini Card Connector(Robson2 and 3G)





Place near MINIC2



ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD

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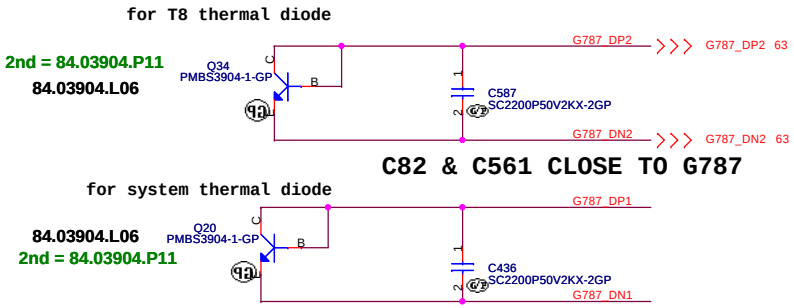
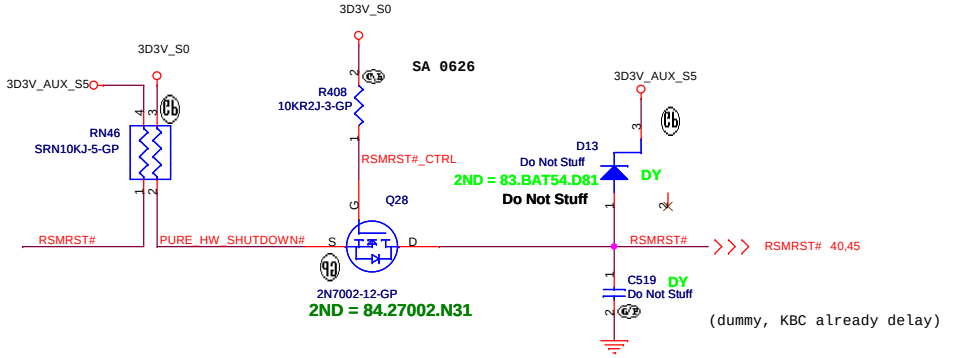
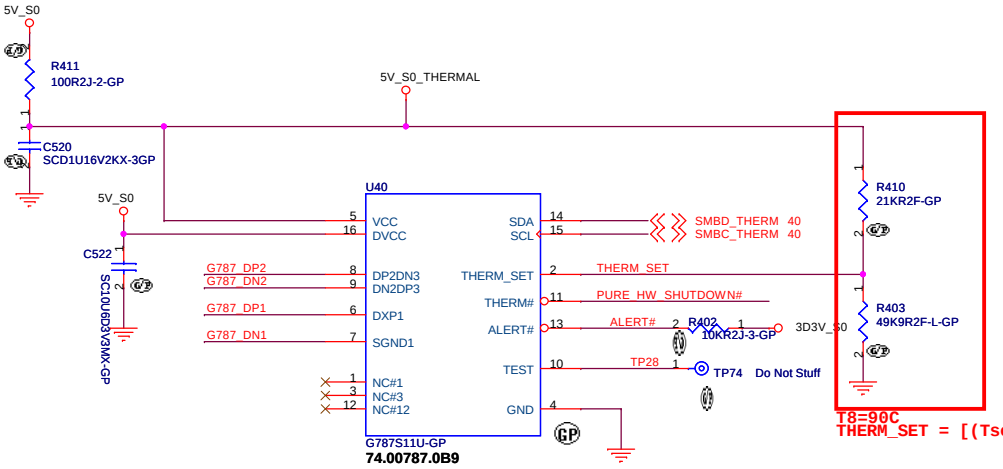
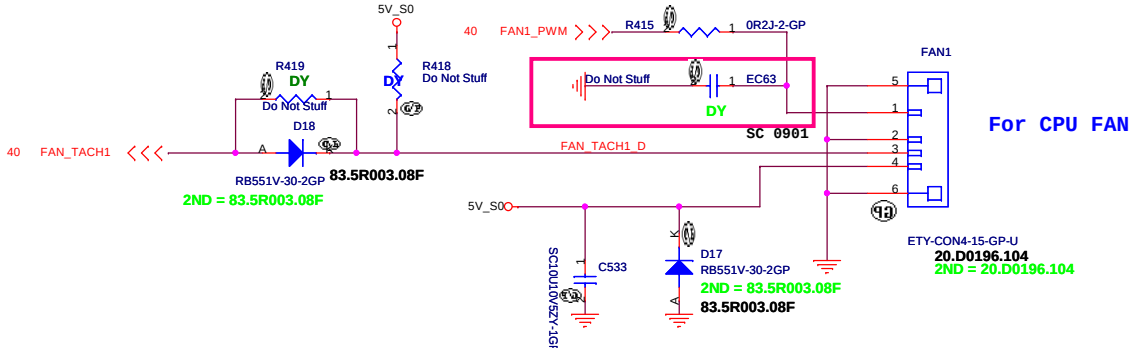


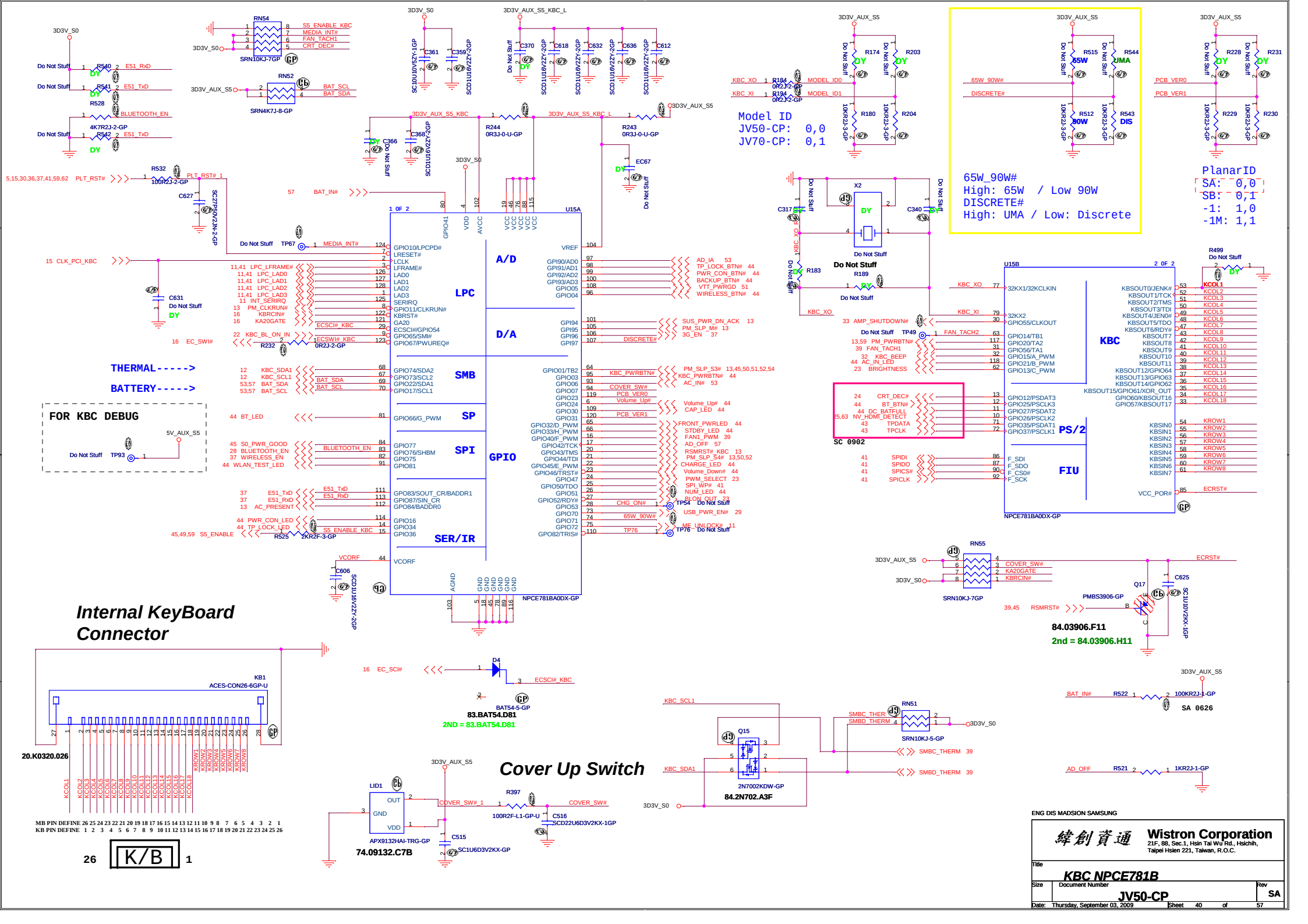




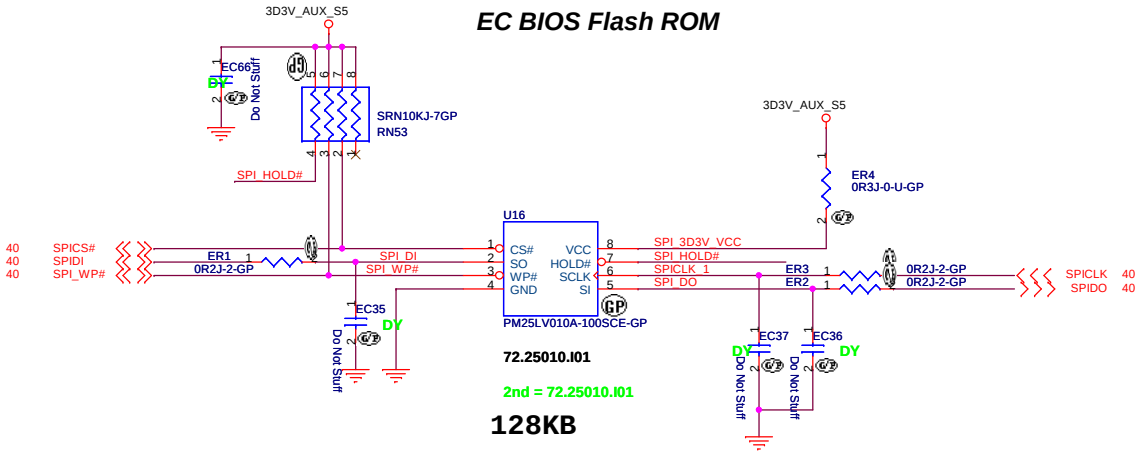


ENG DIS MADSION SAMSUNG

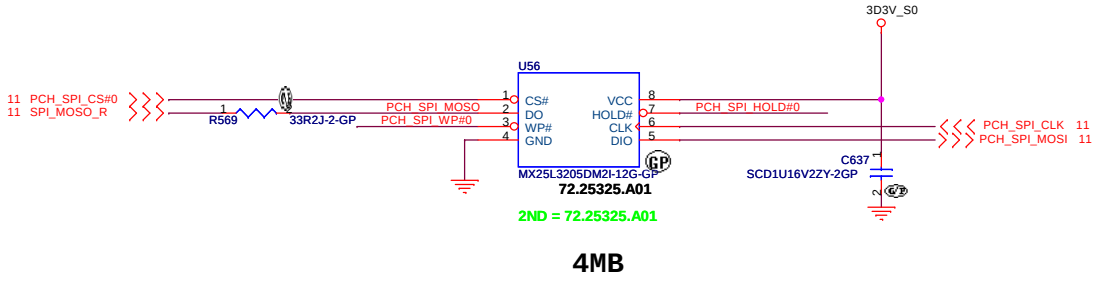
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Thermal/Fan Connector*		
Size	Document Number: JV50-CP	Rev: SA
Date: Thursday, September 03, 2009	Sheet 39 of 57	

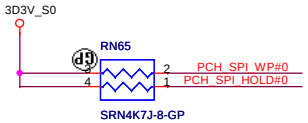

Model ID
JV50-CP: 0,0
JV70-CP: 0,1
65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete
PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
-1M: 1,1
THERMAL----->
BATTERY----->
FOR KBC DEBUG
Internal KeyBoard Connector
Cover Up Switch
SC 0902
84.03906.F11
2nd = 84.03906.H11
83.BAT54.D81
2ND = 83.BAT54.D81
84.2N702.A3F
74.09132.C7B
20.K0320.026
SA 0626
U15A
U15B
KBC
PS/2
FIU
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
NPCE781BA0DX-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC NPCE781B
JV50-CP
Rev SA
Thursday, September 03, 2009
Sheet 40 of 57

EC BIOS Flash ROM

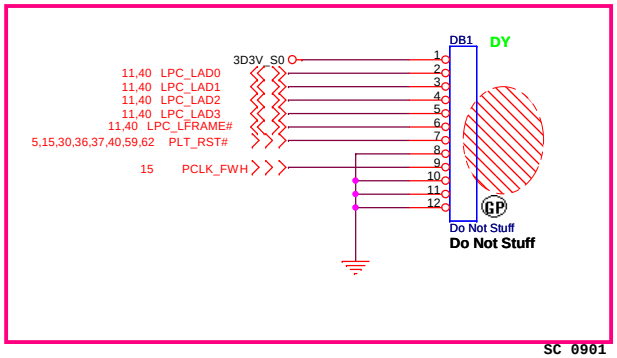


System BIOS Flash ROM





GOLDEN FINGER FOR DEBUG BOARD



ENG DIS MADSION SAMSUNG

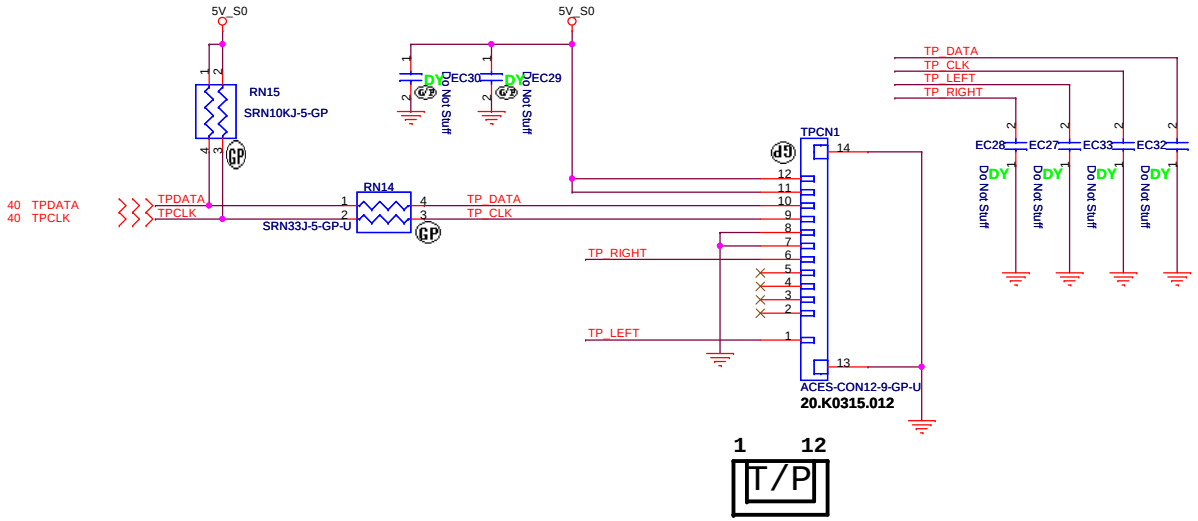
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS**

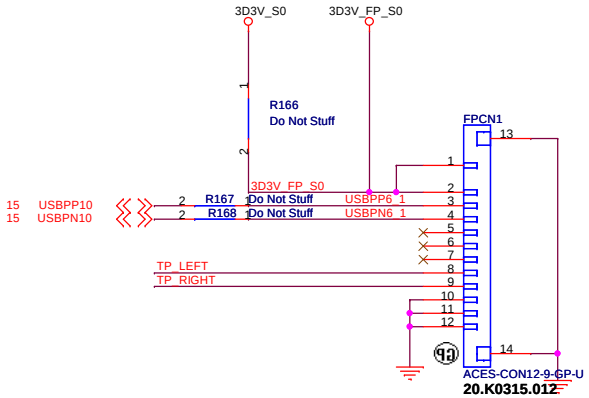
Size	Document Number	Rev
	JV50-CP	SA

Date: Thursday, September 03, 2009 Sheet 41 of 57

TOUCH PAD



Finger printer



ENG DIS MADSION SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: *Touch PAD and FP*		
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Date: Thursday, September 03, 2009	Sheet 43 of 61	

LED

Power LED

Charger LED

WLAN LED

3G/BT LED

SB 1202

SA 0622 EMI

SA 0622 EMI

SA 0622 EMI

BT Button

WLAN Button

BK Button

TP Button

Power Button

PWR_CON_BTN# 1	EC59	DY	Do Not Stuff
PWR_CON_LED#	EC57	DY	Do Not Stuff
Volume_Up# 1	EC60	DY	Do Not Stuff
Volume_Down# 1	EC58	DY	Do Not Stuff

ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED&POWERBD CONN

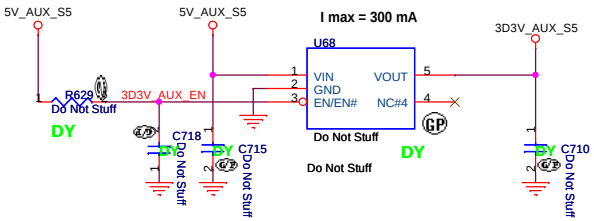
Size | Document Number: JV50-CP | Rev: SA

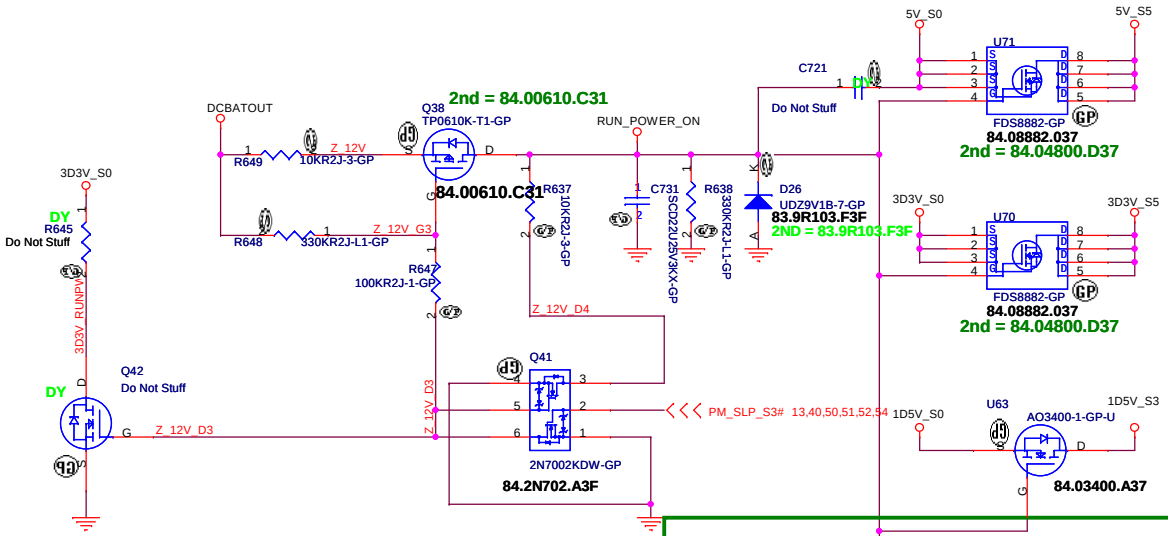
Date: Thursday, September 03, 2009 | Sheet 44 of 61

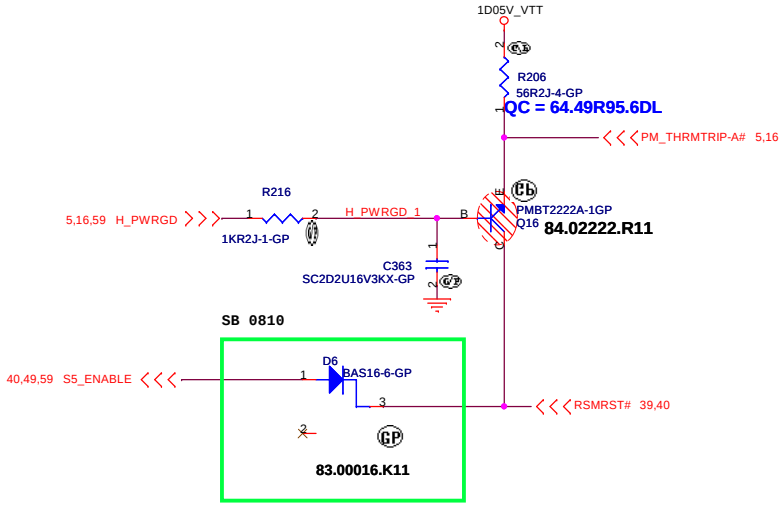
Run Power

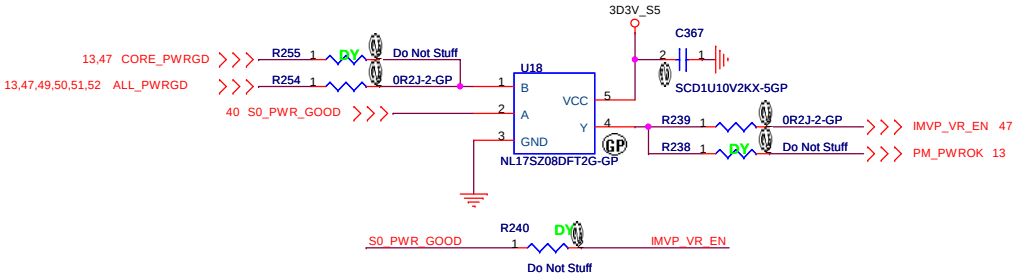
Aux Power

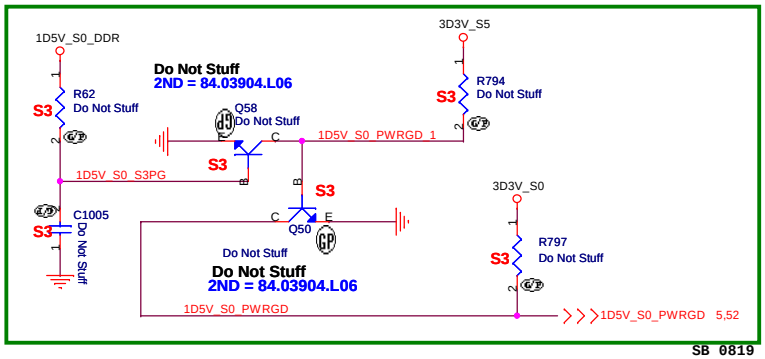
3D3V_AUX_S5











ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

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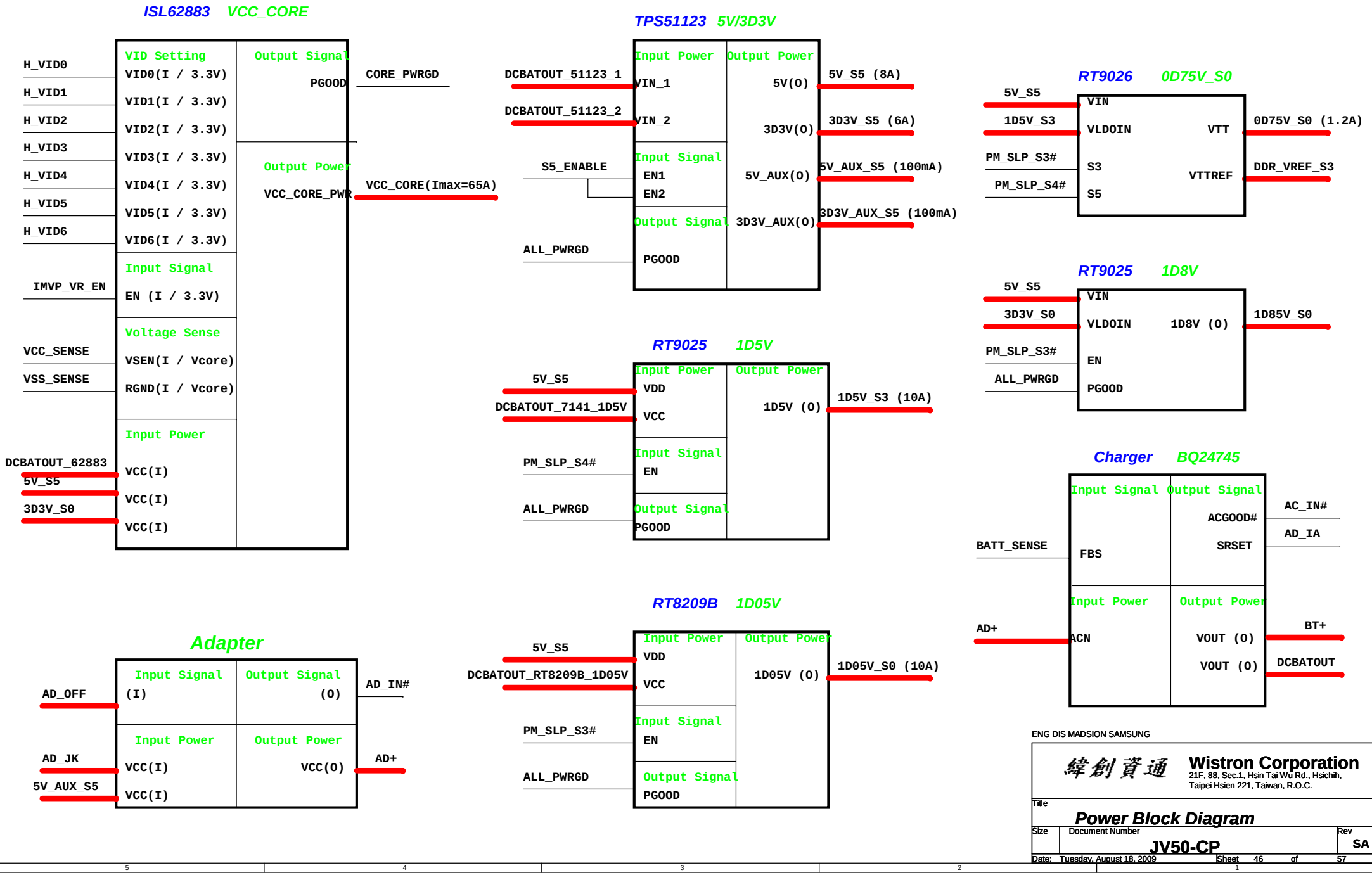


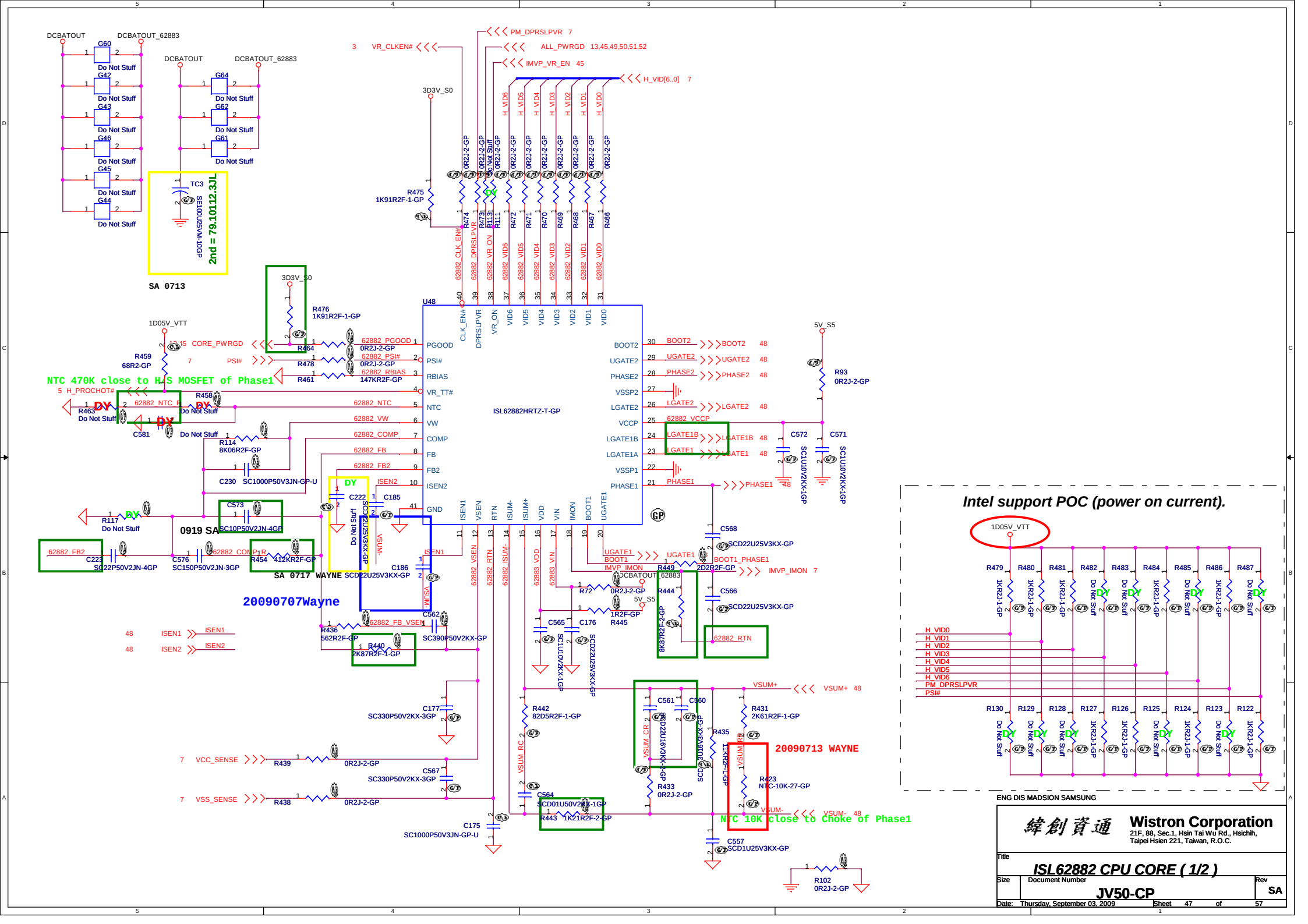
ENG DIS MADSION SAMSUNG

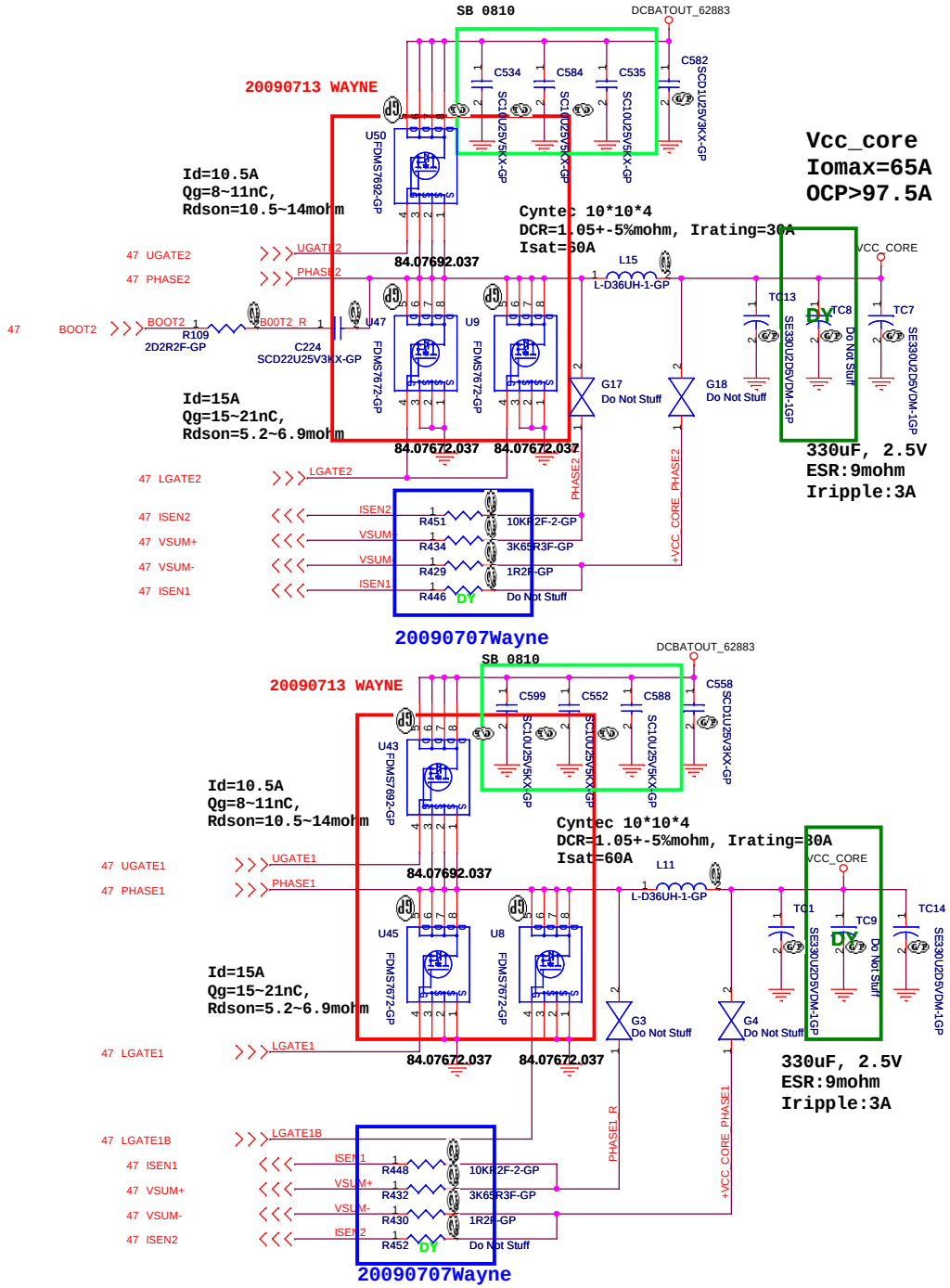
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size	Document Number	Rev
	JV50-CP	SA

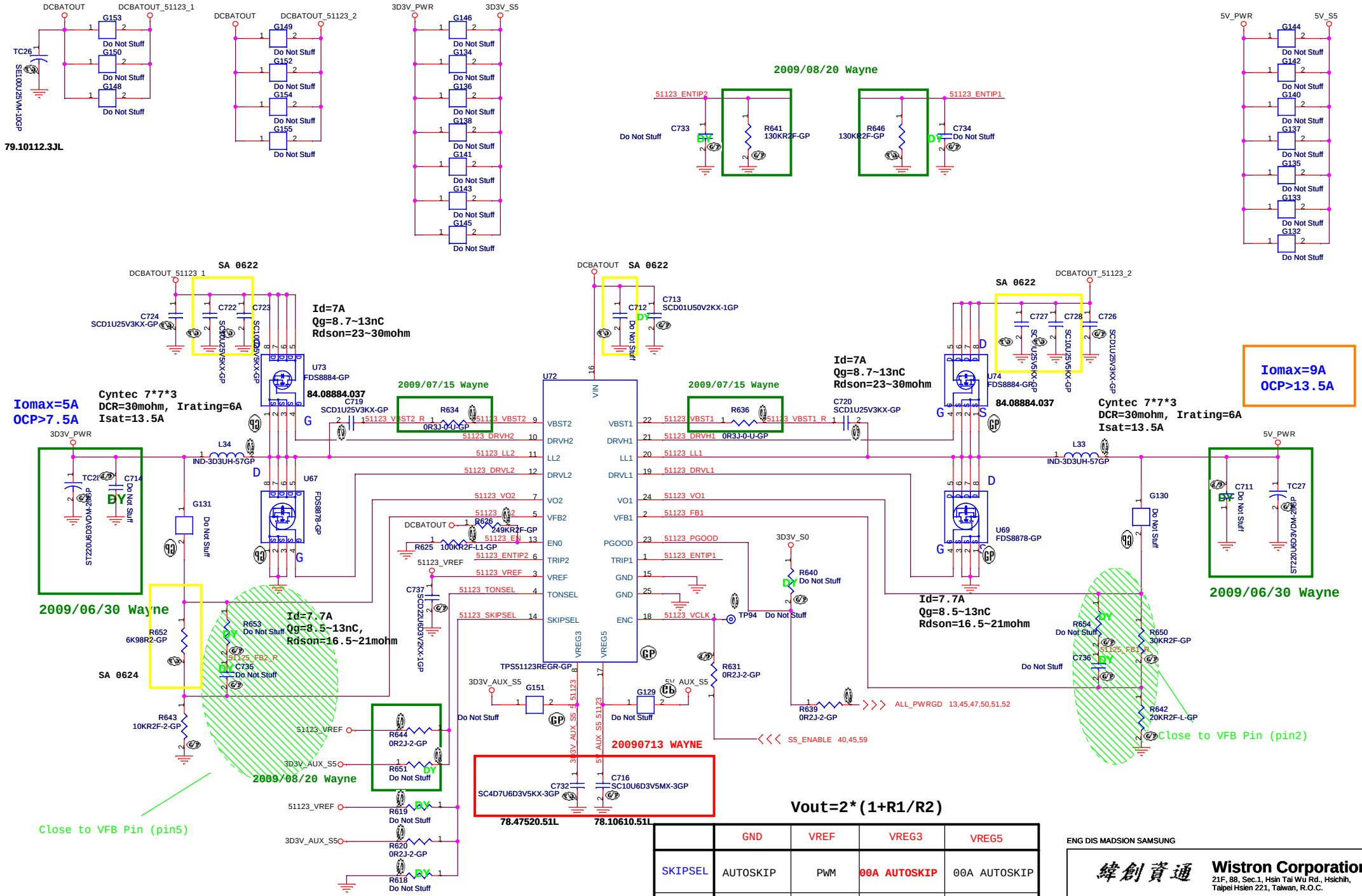
Date: Tuesday, August 18, 2009 Sheet 46 of 57


DCBATOUT
DCBATOUT_62883
G60
G42
G43
G46
G45
G44
G64
G62
G61
Do Not Stuff
TC3
SE100U2VM-10GP
2nd = 79.10112.33L
SA 0713
3D3V_S0
R476
1K91R2F-1-GP
1D05V_VTT
R459
68R2-GP
R464
R478
R461
62882_PGOOD
62882_PSI#
62882_RBIAS
0R2J-2-GP
147KR2F-GP
CORE_PWRGD
PSI#
H_PROCHOT#
NTC 470K close to H/S MOSFET of Phase1
R458
R463
62882_NTC_R
C581
R114
8K06R2F-GP
C230
SC1000P50V3JN-GP-U
62882_NTC
62882_VW
62882_COMP
62882_FB
62882_FB2
ISEN2
U48
ISL62882HRTZ-T-GP
PGOOD
PSI#
RBIAS
VR_TT#
NTC
VW
COMP
FB
FB2
ISEN2
GND
CLK_EN#
DPRSLPVR
VR_ON
VID6
VID5
VID4
VID3
VID2
VID1
VID0
BOOT2
UGATE2
PHASE2
VSSP2
LGATE2
VCCP
LGATE1B
LGATE1A
VSSP1
PHASE1
ISEN1
VSEN
RTN
ISUM-
ISUM+
VDD
VIN
IMON
BOOT1
UGATE1
62882_VCCP
5V_S5
R93
0R2J-2-GP
C572
C571
SC1U10V2KX-1GP
C573
SC10P50V2JN-4GP
R117
0919 SA
C222
C185
SCD22U25V3KX-GP
C223
SC22P50V2JN-4GP
C576
SC150P50V2JN-3GP
R454
412KR2F-GP
SA 0717 WAYNE
C186
20090707Wayne
R436
562R2F-GP
R440
2K87R2F-1-GP
C562
SC390P50V2KX-GP
C568
R449
2D2R2F-GP
IMVP_IMON
R72
1R2F-GP
R445
C565
C176
C566
R444
8K87R2F-2-GP
62882_RTN
C177
SC330P50V2KX-3GP
R442
82D5R2F-1-GP
VSUM+
VSUM-
C561
C560
R431
2K61R2F-1-GP
R435
R433
0R2J-2-GP
R423
NTC-10K-27-GP
20090713 WAYNE
NTC 10K close to Choke of Phase1
C564
SCD01U50V2KX-1GP
R443
1K21R2F-2-GP
C175
SC1000P50V3JN-GP-U
C557
SCD1U25V3KX-GP
R102
0R2J-2-GP
VCC_SENSE
VSS_SENSE
R439
R438
C567
SC330P50V2KX-3GP
Intel support POC (power on current).
R479
R480
R481
R482
R483
R484
R485
R486
R487
R130
R129
R128
R127
R126
R125
R124
R123
R122
1KR2J-1-GP
Do Not Stuff
DY
ENG DIS MADSION SAMSUN
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62882 CPU CORE (1/2)
Size
Document Number
JV50-CP
Rev
SA
Date: Thursday, September 03, 2009
Sheet 47 of 57



ENG DIS MADSION SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***ISL62882 CPU CORE (1/2)***	
Size	Document Number **JV50-CP**	Rev **SA**
Date: Thursday, September 03, 2009	Sheet 48 of 57	



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	**00A AUTOSKIP**	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	**300k/CH1 375k/CH2**	365k/CH1 460k/CH2

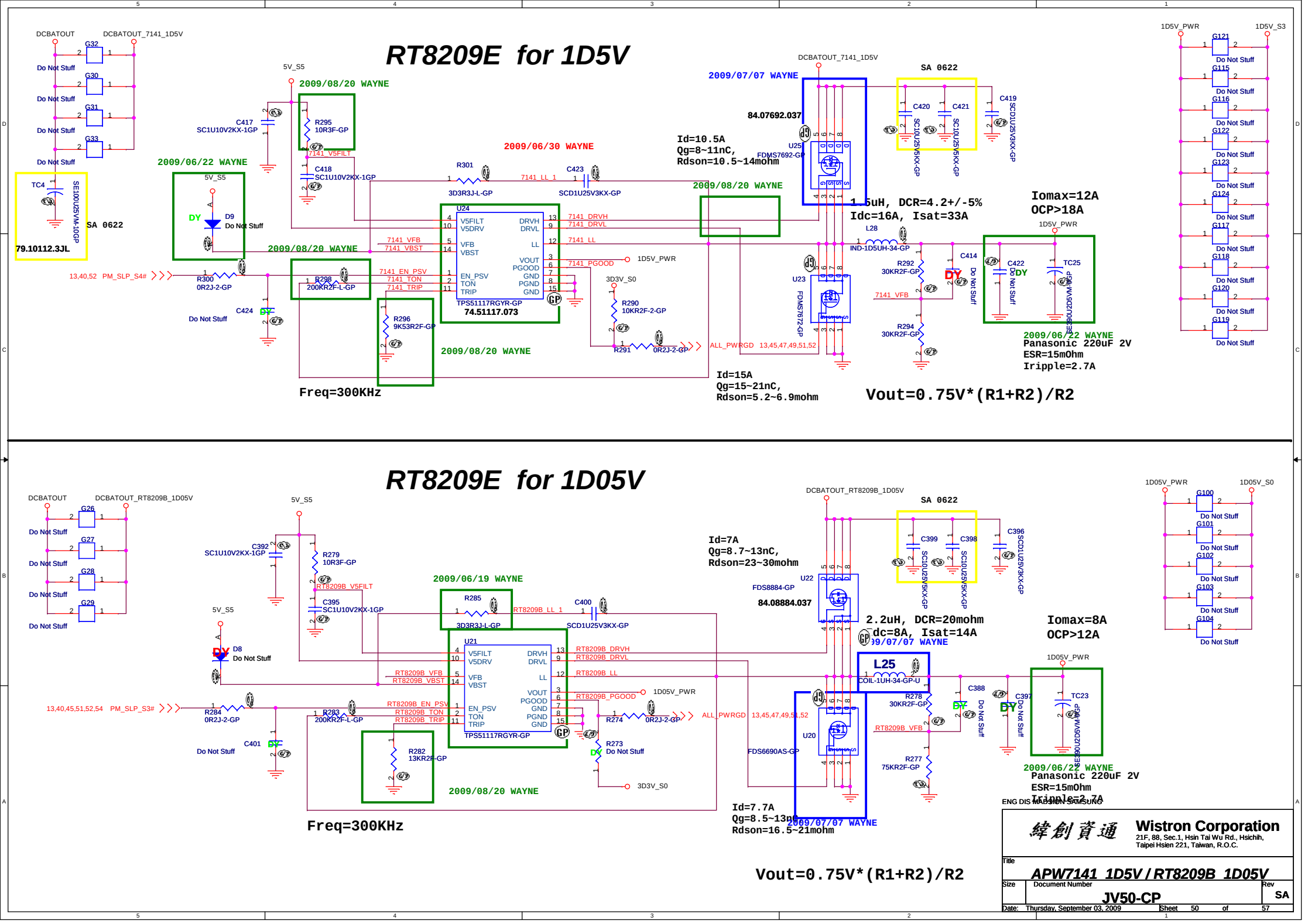
ENG DIS MADSION SAMSUNG

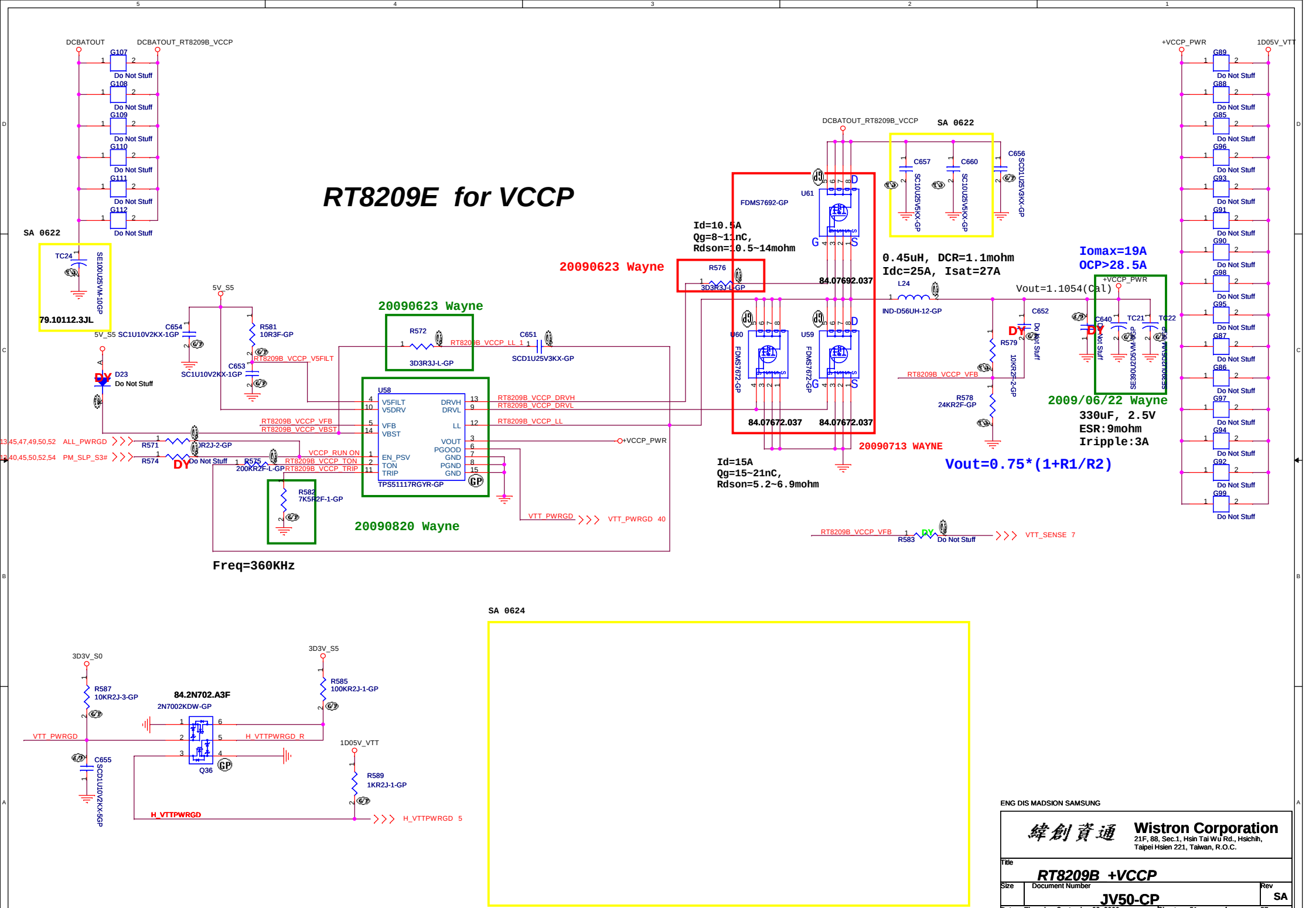
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51123 5V/3D3V**

Size | Document Number: **JV50-CP** | Rev: **SA**

Date: Thursday, September 03, 2009 | Sheet 49 of 57


RT8209E for 1D5V
DCBATOUT
DCBATOUT_7141_1D5V
Do Not Stuff
SA 0622
79.10112.3JL
5V_S5
2009/08/20 WAYNE
2009/06/22 WAYNE
2009/06/30 WAYNE
2009/07/07 WAYNE
C417
SC1U10V2KX-1GP
R295
10R3F-GP
C418
R301
3D3R3J-L-GP
C423
SCD1U25V3KX-GP
U24
TPS51117RGYR-GP
74.51117.073
7141_VFB
7141_VBST
7141_EN_PSV
7141_TON
7141_TRIP
7141_DRVH
7141_DRVL
7141_LL
7141_PGOOD
R300
0R2J-2-GP
R298
200KR2F-L-GP
R296
9K53R2F-GP
R290
10KR2F-2-GP
R291
0R2J-2-GP
C424
D9
DY
1D5V_PWR
3D3V_S0
ALL_PWRGD
13,45,47,49,51,52
13,40,52 PM_SLP_S4#
Freq=300KHz
Id=10.5A
Qg=8~11nC,
Rdson=10.5~14mohm
84.07692.037
U25
FDMS7692-GP
C420
C421
C419
SC10U25V5KX-GP
SCD1U25V3KX-GP
1.5uH, DCR=4.2+/-5%
Idc=16A, Isat=33A
L28
IND-1D5UH-34-GP
Iomax=12A
OCP>18A
R292
30KR2F-GP
R294
30KR2F-GP
C414
C422
TC25
SE330U2D5VM-1DGP
Panasonic 220uF 2V
ESR=15mOhm
Iripple=2.7A
U23
FDMS7672-GP
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm
Vout=0.75V*(R1+R2)/R2
TC4
SE100U25VM-1DGP
G32
G30
G31
G33
G121
G115
G116
G122
G123
G124
G117
G118
G120
G119
RT8209E for 1D05V
DCBATOUT_RT8209B_1D05V
1D05V_PWR
1D05V_S0
2009/06/19 WAYNE
2009/07/07 WAYNE
C392
R279
10R3F-GP
RT8209B_V5FILT
C395
R285
C400
U21
RT8209B_VFB
RT8209B_VBST
RT8209B_EN_PSV
RT8209B_TON
RT8209B_TRIP
RT8209B_DRVH
RT8209B_DRVL
RT8209B_LL
RT8209B_PGOOD
R284
0R2J-2-GP
R283
200KR2F-L-GP
R282
13KR2F-GP
R274
0R2J-2-GP
R273
D8
C401
13,40,45,51,52,54 PM_SLP_S3#
Freq=300KHz
Id=7A
Qg=8.7~13nC,
Rdson=23~30mohm
U22
FDS8884-GP
84.08884.037
C399
C398
C396
2.2uH, DCR=20mohm
Idc=8A, Isat=14A
L25
COIL-1UH-34-GP-U
Iomax=8A
OCP>12A
R278
30KR2F-GP
R277
75KR2F-GP
C388
C397
TC23
Panasonic 220uF 2V
ESR=15mOhm
Iripple=2.7A
U20
FDS6690AS-GP
Id=7.7A
Qg=8.5~13nC,
Rdson=16.5~21mohm
Vout=0.75V*(R1+R2)/R2
G26
G27
G28
G29
G100
G101
G102
G103
G104
ENG DIS MA3 ON SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
APW7141_1D5V / RT8209B_1D05V
Size
Document Number
JV50-CP
Rev
SA
Date: Thursday, September 03, 2009
Sheet 50 of 57


RT8209E for VCCP
DCBATOUT
DCBATOUT_RT8209B_VCCP
SA 0622
Do Not Stuff
79.10112.3JL
20090623 Wayne
Id=10.5A
Qg=8~11nC,
Rdson=10.5~14mohm
FDMS7692-GP
84.07692.037
0.45uH, DCR=1.1mohm
Idc=25A, Isat=27A
Iomax=19A
OCP>28.5A
Vout=1.1054(Cal)
2009/06/22 Wayne
330uF, 2.5V
ESR:9mohm
Iripple:3A
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm
84.07672.037
20090713 WAYNE
Vout=0.75*(1+R1/R2)
20090820 Wayne
Freq=360KHz
TPS51117RGYR-GP
SA 0624
84.2N702.A3F
2N7002KDW-GP
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
RT8209B +VCCP
JV50-CP
Thursday, September 03, 2009
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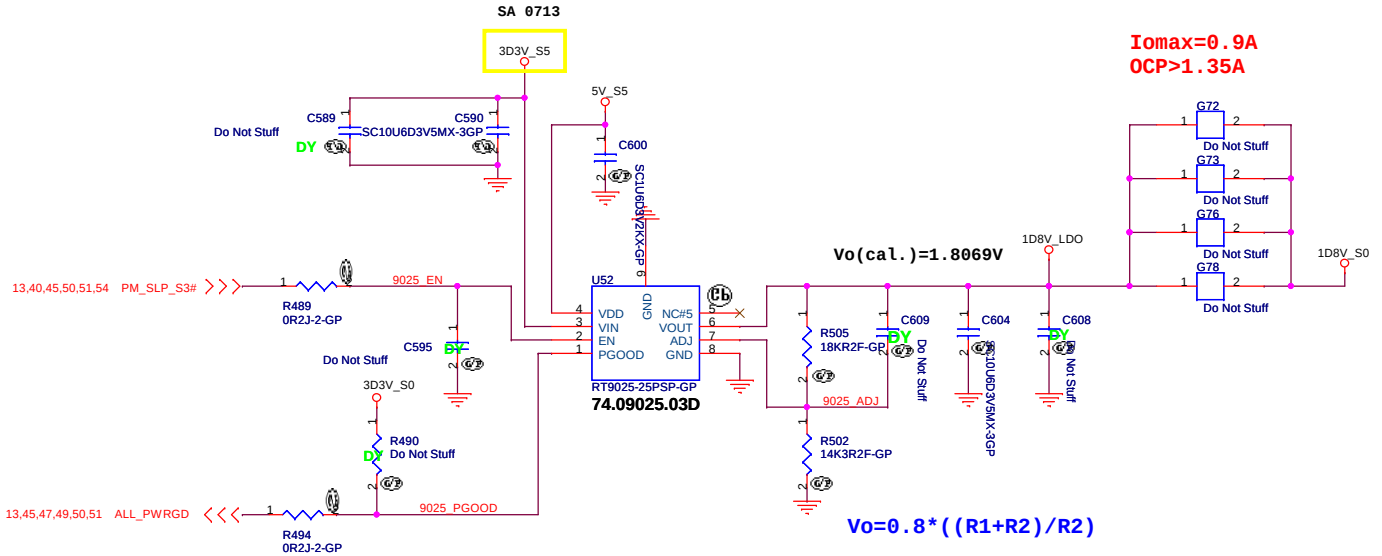
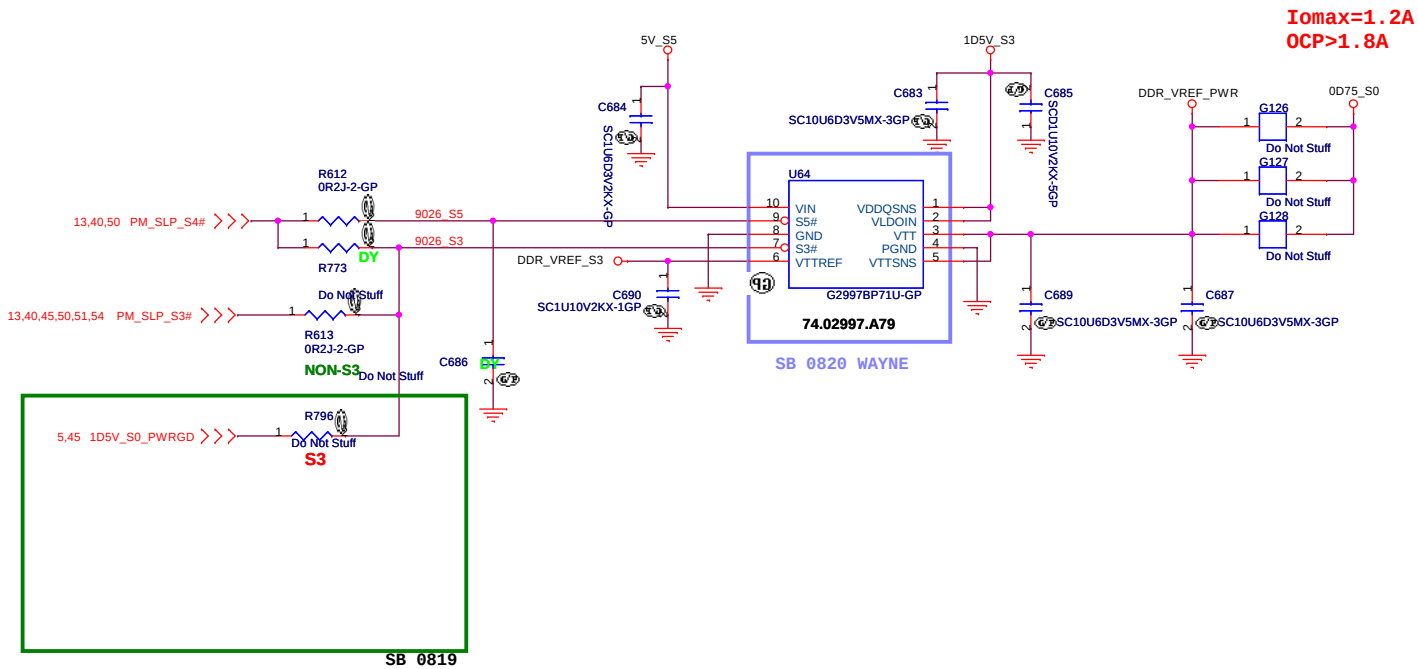
RT9025 for 1D8V_S0



RT9026 for 0D75V_S3



ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RT9025_1D8V/RT9026_0D75***

Size	Document Number	Rev
	JV50-CP	SA

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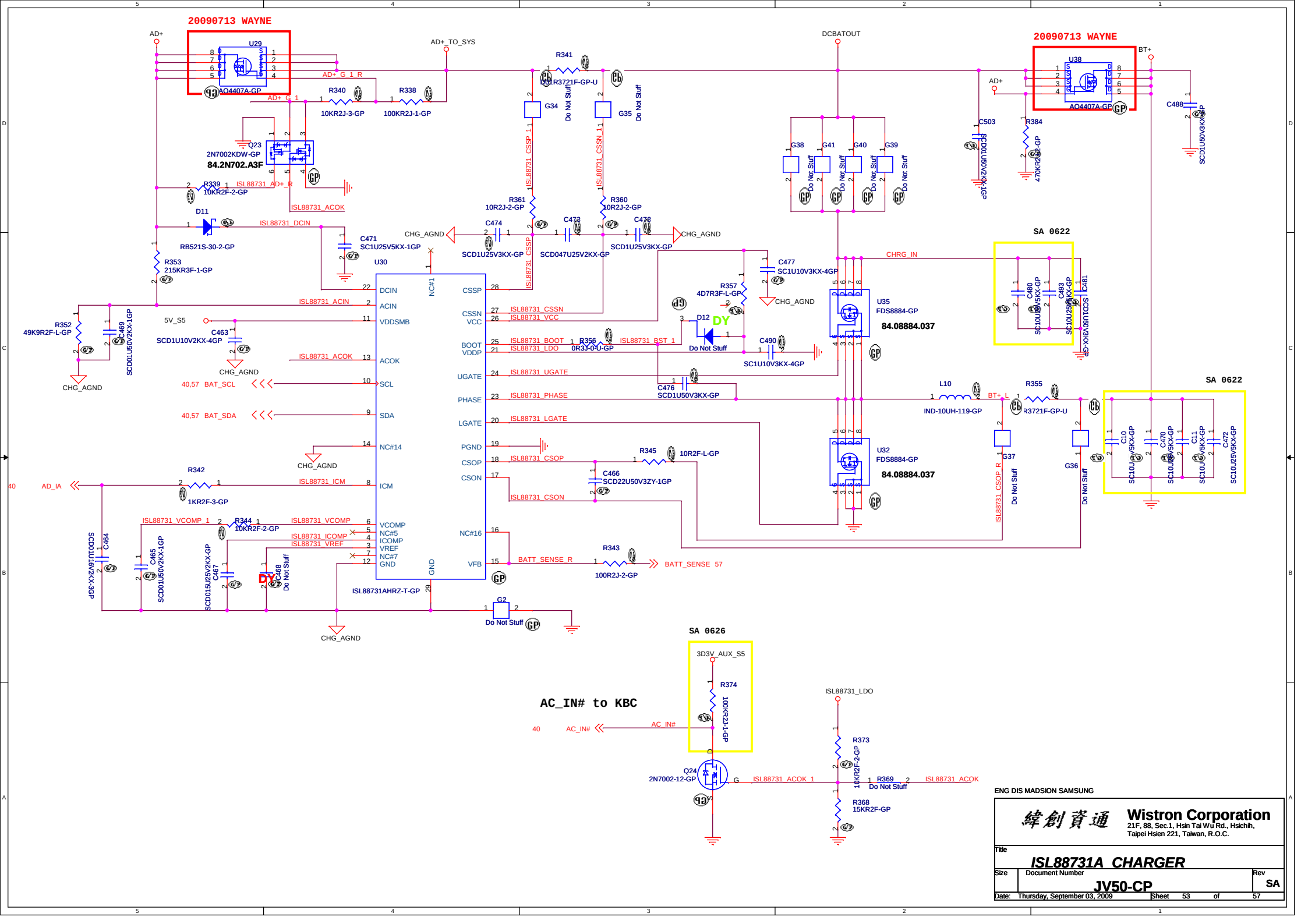
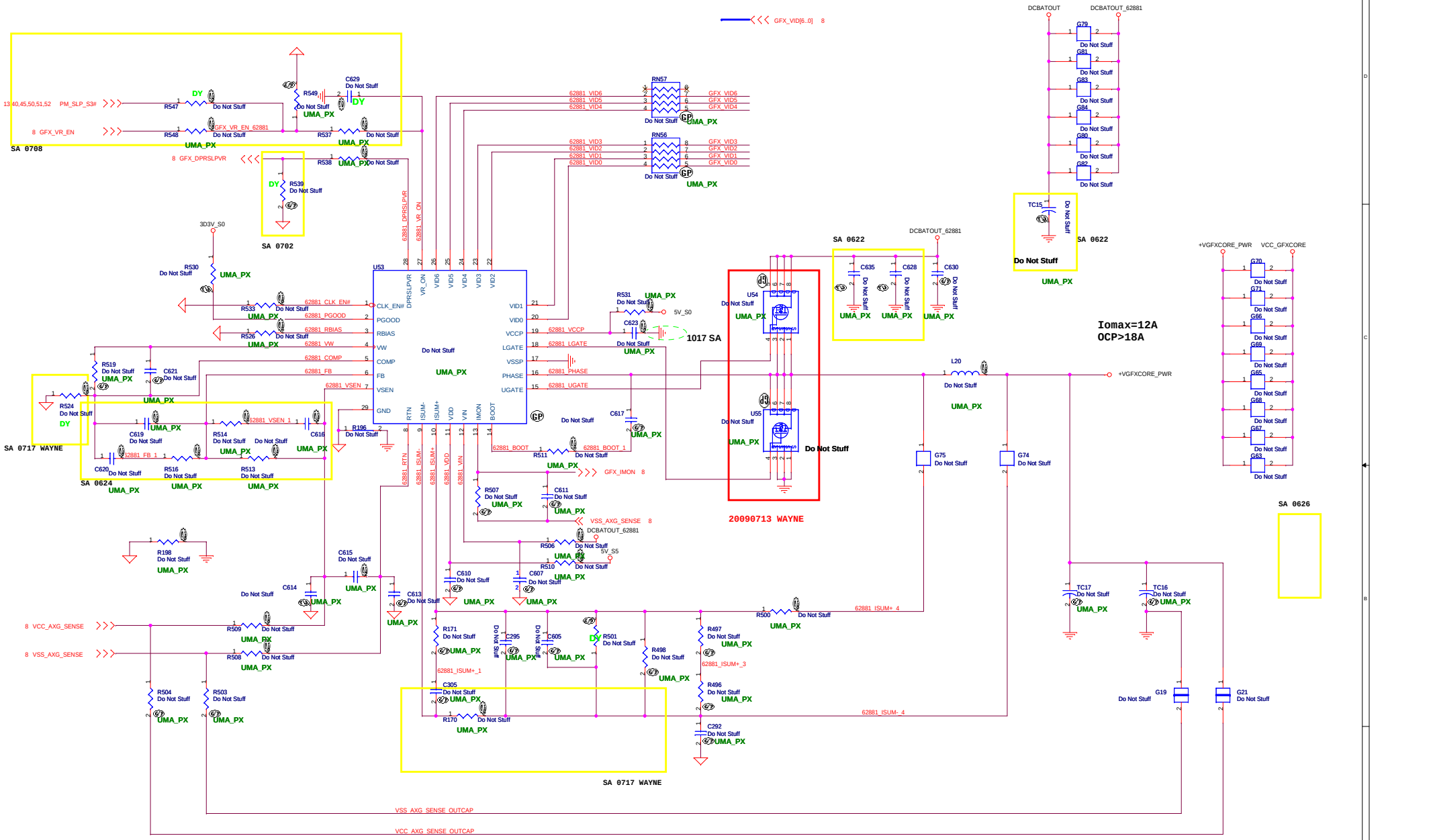

20090713 WAYNE
U29
AO4407A-GP
AD+
AD+_TO_SYS
AD+_G_1_R
AD+_G_1
R340
10KR2J-3-GP
R338
100KR2J-1-GP
Q23
2N7002KDW-GP
84.2N702.A3F
R339
10KR2F-2-GP
ISL88731_AD+_R
ISL88731_ACOK
D11
RB521S-30-2-GP
ISL88731_DCIN
R353
215KR3F-1-GP
C471
SC1U25V5KX-1GP
U30
ISL88731AHRZ-T-GP
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
NC#1
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
R352
49K9R2F-L-GP
C469
SCD01U50V2KX-1GP
5V_S5
C463
SCD1U10V2KX-4GP
CHG_AGND
40,57 BAT_SCL
40,57 BAT_SDA
R342
1KR2F-3-GP
40 AD_IA
ISL88731_VCOMP_1
R344
10KR2F-2-GP
ISL88731_VCOMP
ISL88731_ICOMP
ISL88731_VREF
C464
SCD01U16V2KX-3GP
C465
SCD01U50V2KX-1GP
C467
SCD015U25V2KX-GP
C468
Do Not Stuff
DY
G2
Do Not Stuff
R341
0UR3721F-GP-U
G34
Do Not Stuff
G35
Do Not Stuff
ISL88731_CSSP_1
ISL88731_CSSN_1
R361
10R2J-2-GP
R360
10R2J-2-GP
C474
SCD1U25V3KX-GP
C473
SCD047U25V2KX-GP
C472
SCD1U25V3KX-GP
CHG_AGND
ISL88731_CSSP
ISL88731_CSSN
ISL88731_VCC
ISL88731_BOOT
ISL88731_LDO
ISL88731_BST_1
R356
0R3J-0-U-GP
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
ISL88731_CSOP
ISL88731_CSON
C476
SCD1U50V3KX-GP
R357
4D7R3F-L-GP
D12
Do Not Stuff
DY
C490
SC1U10V3KX-4GP
C477
SC1U10V3KX-4GP
R345
10R2F-L-GP
C466
SCD22U50V3ZY-1GP
R343
100R2J-2-GP
BATT_SENSE_R
BATT_SENSE 57
DCBATOUT
G38
Do Not Stuff
G41
Do Not Stuff
G40
Do Not Stuff
G39
Do Not Stuff
CHRG_IN
U35
FDS8884-GP
84.08884.037
U32
FDS8884-GP
84.08884.037
ISL88731_CSOP_R
G37
Do Not Stuff
G36
Do Not Stuff
L10
IND-10UH-119-GP
BT+_L
R355
R3721F-GP-U
SA 0622
C480
SC10U25V5KX-GP
C493
SC10U25V5KX-GP
C481
SC1U50V3KX-GP
C10
SC10U25V5KX-GP
C470
SC10U25V5KX-GP
C11
SC10U25V5KX-GP
C472
SC10U25V5KX-GP
20090713 WAYNE
U38
AO4407A-GP
AD+
BT+
C503
SCD1U50V2KX-1GP
R384
470KR2F-GP
C488
SCD1U50V3KX-GP
SA 0626
AC_IN# to KBC
3D3V_AUX_S5
R374
100KR2J-1-GP
40 AC_IN#
AC_IN#
Q24
2N7002-12-GP
ISL88731_ACOK_1
ISL88731_LDO
R373
10KR2F-2-GP
R369
Do Not Stuff
ISL88731_ACOK
R368
15KR2F-GP
ENG DIS MADSION SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A CHARGER
Size
Document Number
JV50-CP
Rev
SA
Date: Thursday, September 03, 2009
Sheet 53 of 57



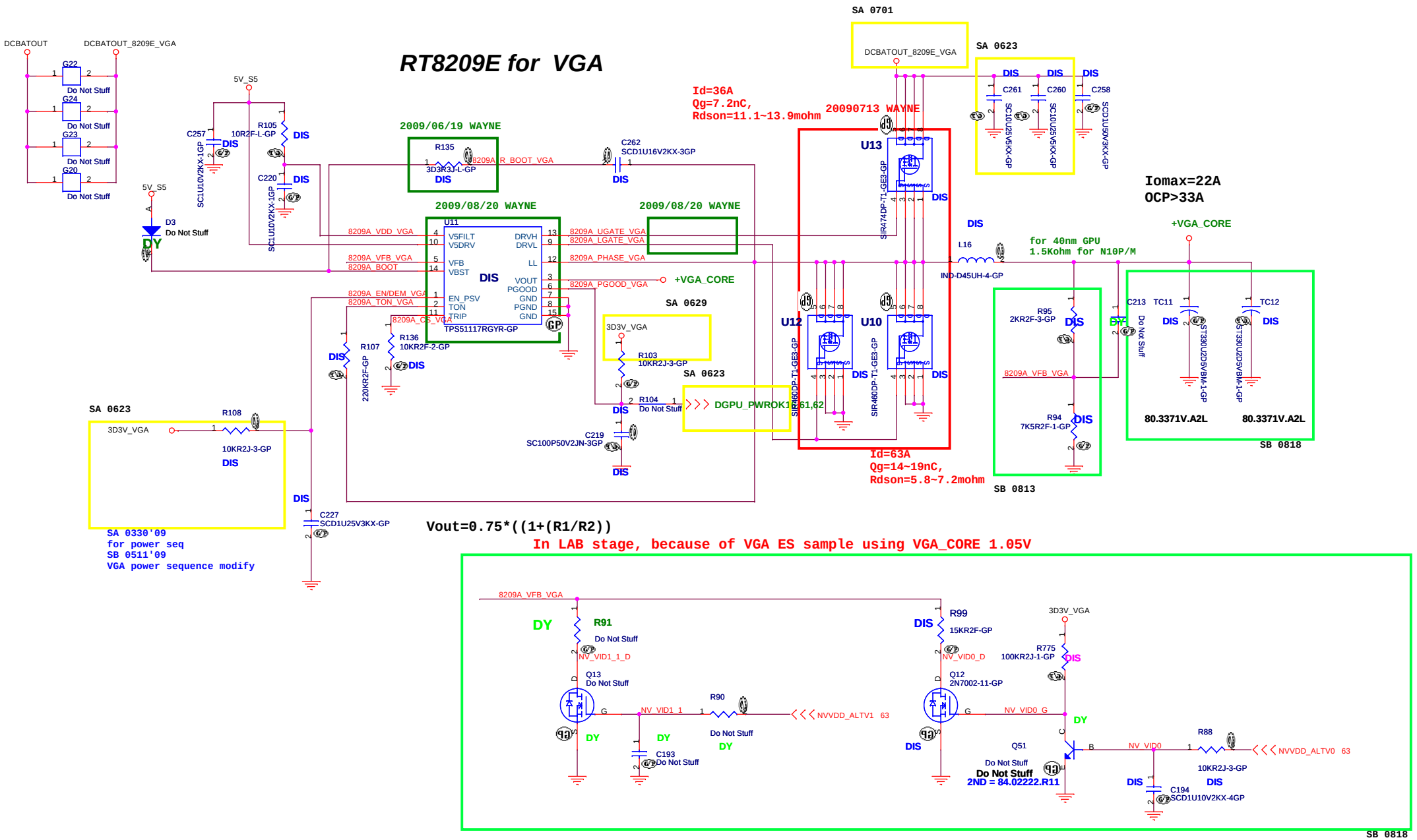
ENG DIS MADSION SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62881_+VCC_GFXCORE

Size	Document Number	Rev
C	JV50-CP	SB

Date: Thursday, September 03, 2009 Sheet 54 of 45



	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.05V GPU VOLTAGE H: 0.95V

ENG DIS MADSION SAMSUNG

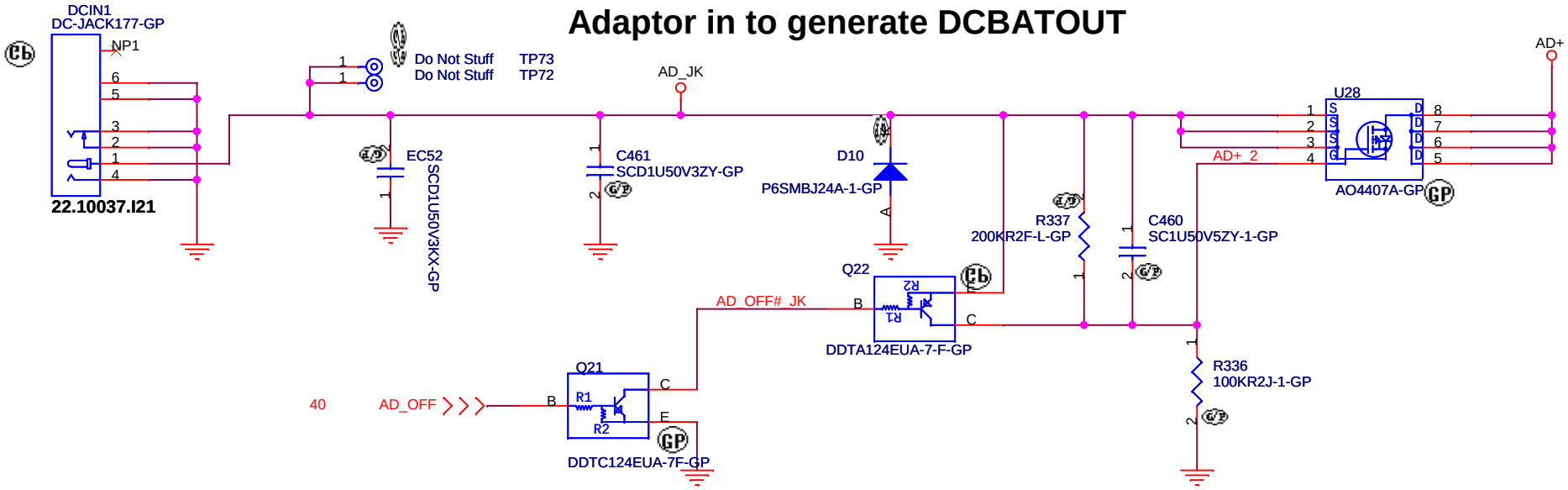
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RT8209E VGA CORE***

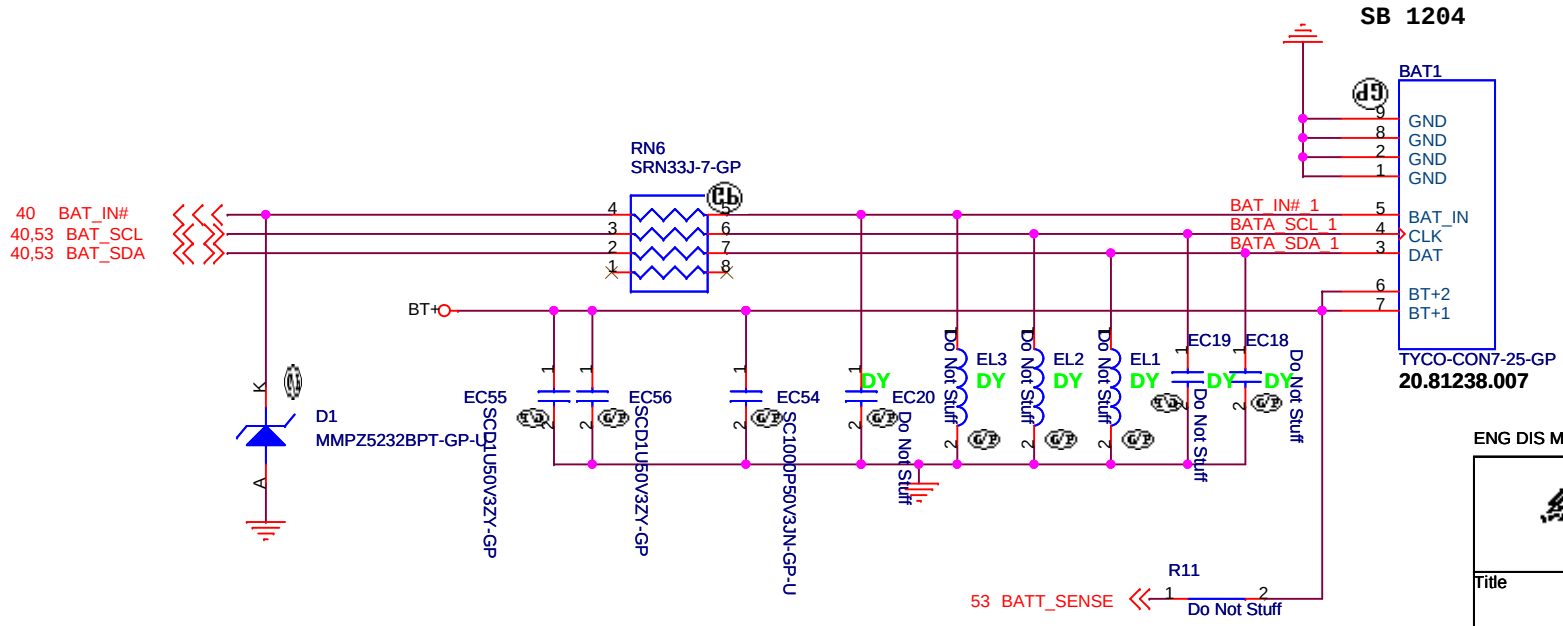
Size: A3 | Document Number: **JV50-CP** | Rev:

Date: Thursday, September 03, 2009 | Sheet 55 of 52

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



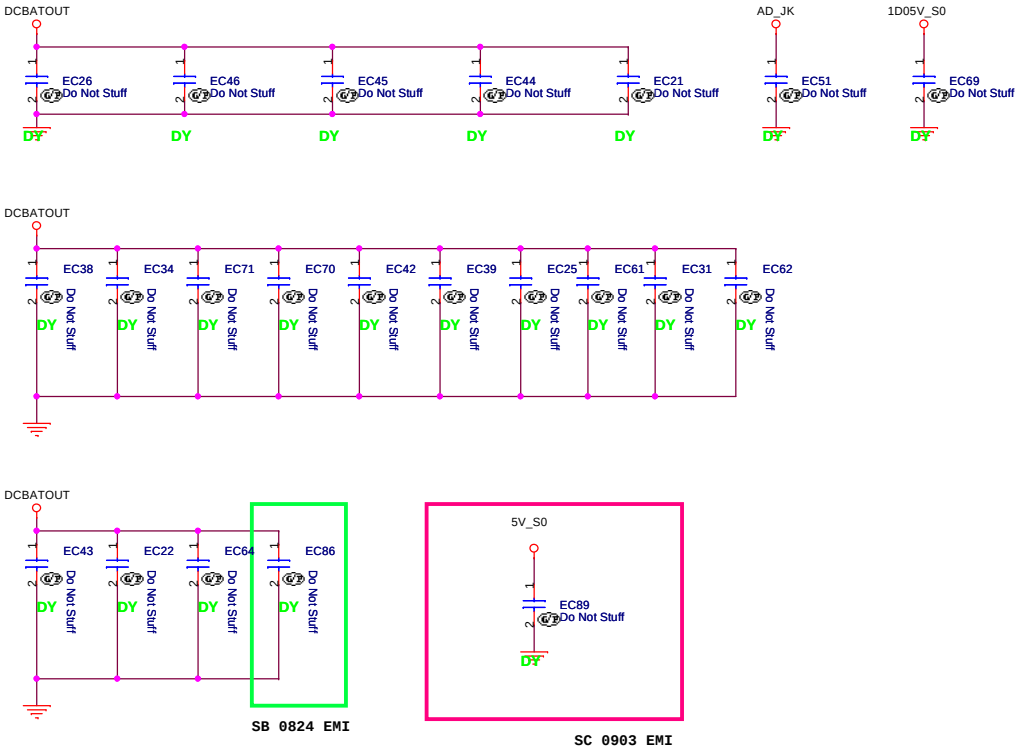
ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size	Document Number	Rev
	JV50-CP	SA

Date: Thursday, September 03, 2009 Sheet 57 of 61



CPU

H1 H2 H3 — STF237R125H42-GP

34.4GD01.001 34.4GD01.001 34.4GD01.001

PCH

H4 — STF237R125H42-GP

34.4GD01.001

VGA

H5 DIS H6 DIS H11 DIS — STF237R125H42-GP

34.4GD01.001 34.4GD01.001 34.4GD01.001

MDC

H7 HOLE — ZZ.0HOLE.XXX

34.42Y01.011

MINICARD

H8 HOLE — ZZ.0HOLE.XXX

34.4P901.001

H9 Do Not Stuff H10 Do Not Stuff

GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND9 GND10 GND11 GND12 — Do Not Stuff

SPRING_GND16 SPRING_GND17 SPRING_GND18 SPRING_GND19 — Do Not Stuff

SPRING_GND14 SPRING_GND15 SPRING_GND21 SPRING_GND22 — Do Not Stuff

SPRING_GND23 SPRING_GND24 SPRING_GND25 SPRING_GND26 — Do Not Stuff

ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
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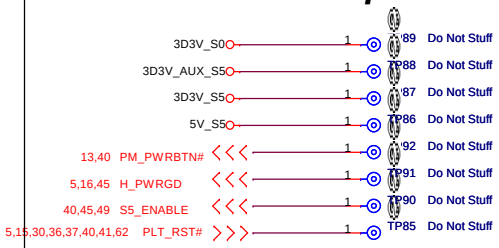
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

Size | Document Number: JV50-CP | Rev: SA

Date: Thursday, September 03, 2009 | Sheet 58 of 61

Check test point



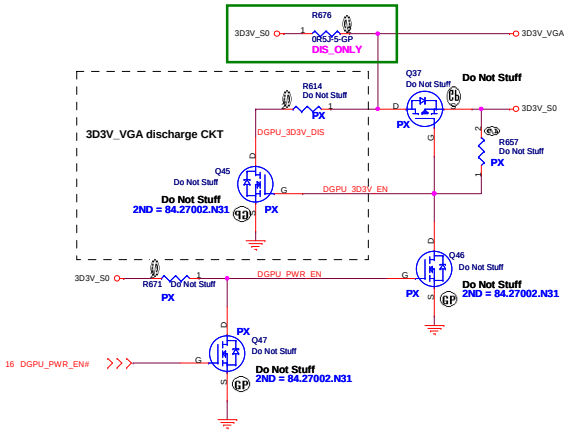
Test Point放在Dimm Door打開可量測處

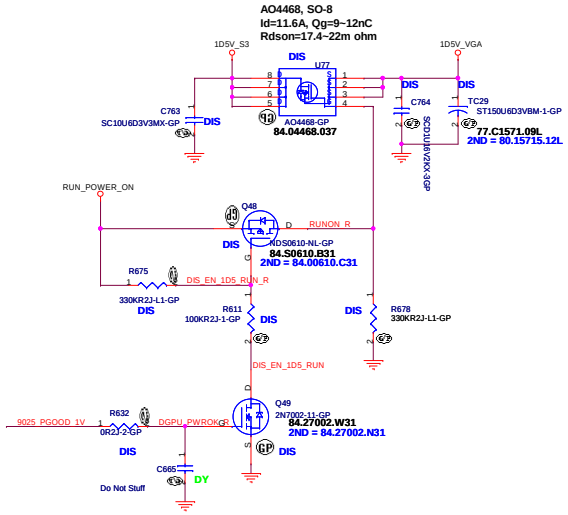
ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

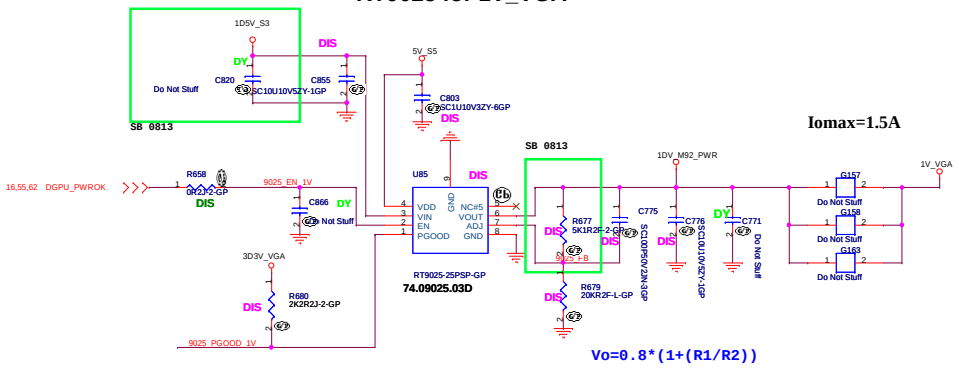
Title: ***AFTE_TP***		
Size	Document Number: **JV50-CP**	Rev: **SA**
Date: Thursday, September 03, 2009	Sheet 59 of 57	

+3VS to 3.3V_DELAY Transfer

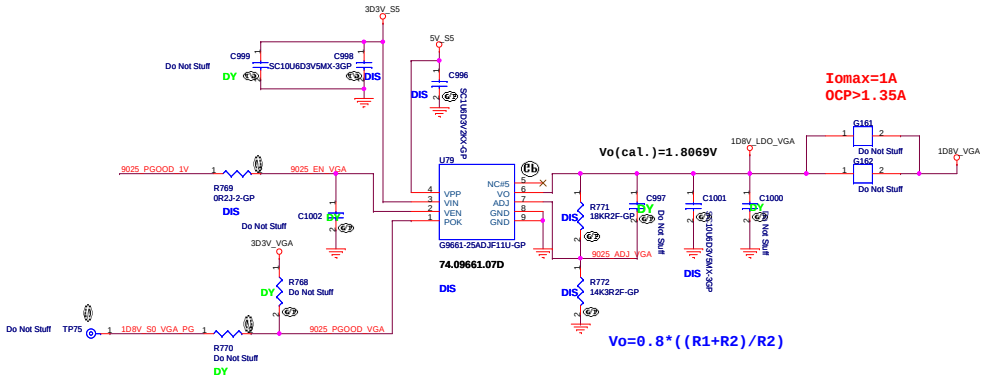




RT9025 for 1V_VGA



G9661 for 1D8V_VGA



ENG DIS MADSION SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI POWER**

Size	Document Number	Rev
A2	JV50-CP	SB

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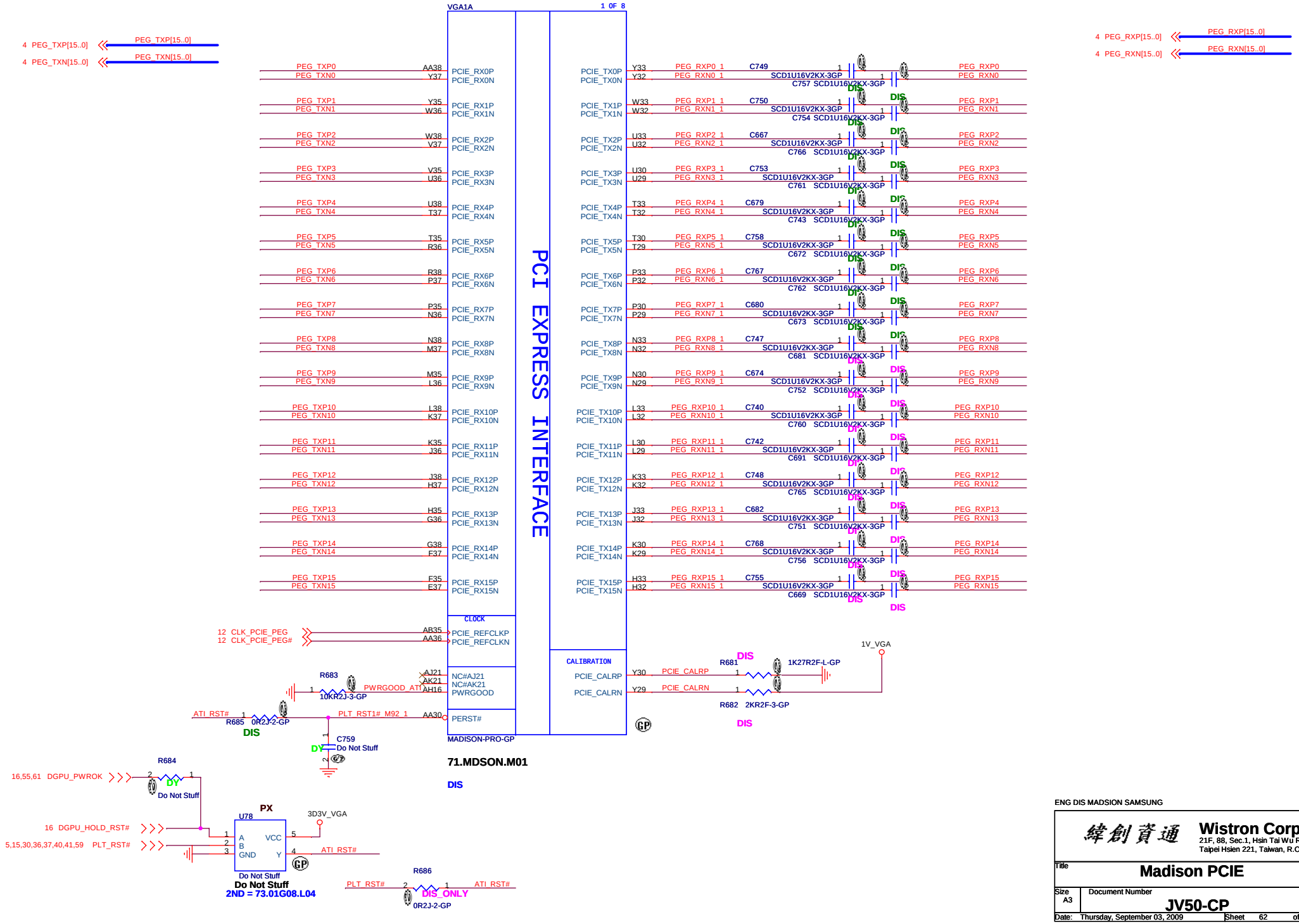

ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Madison PCIE		
Size: A3	Document Number: JV50-CP	Rev: SB
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Layout notice:
It should be pleace near HDMI connector

DVPDATA [3:2:1:0] for VRAM type
selection H/W strap
Should provide VRAM Table for VBios
request

DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)

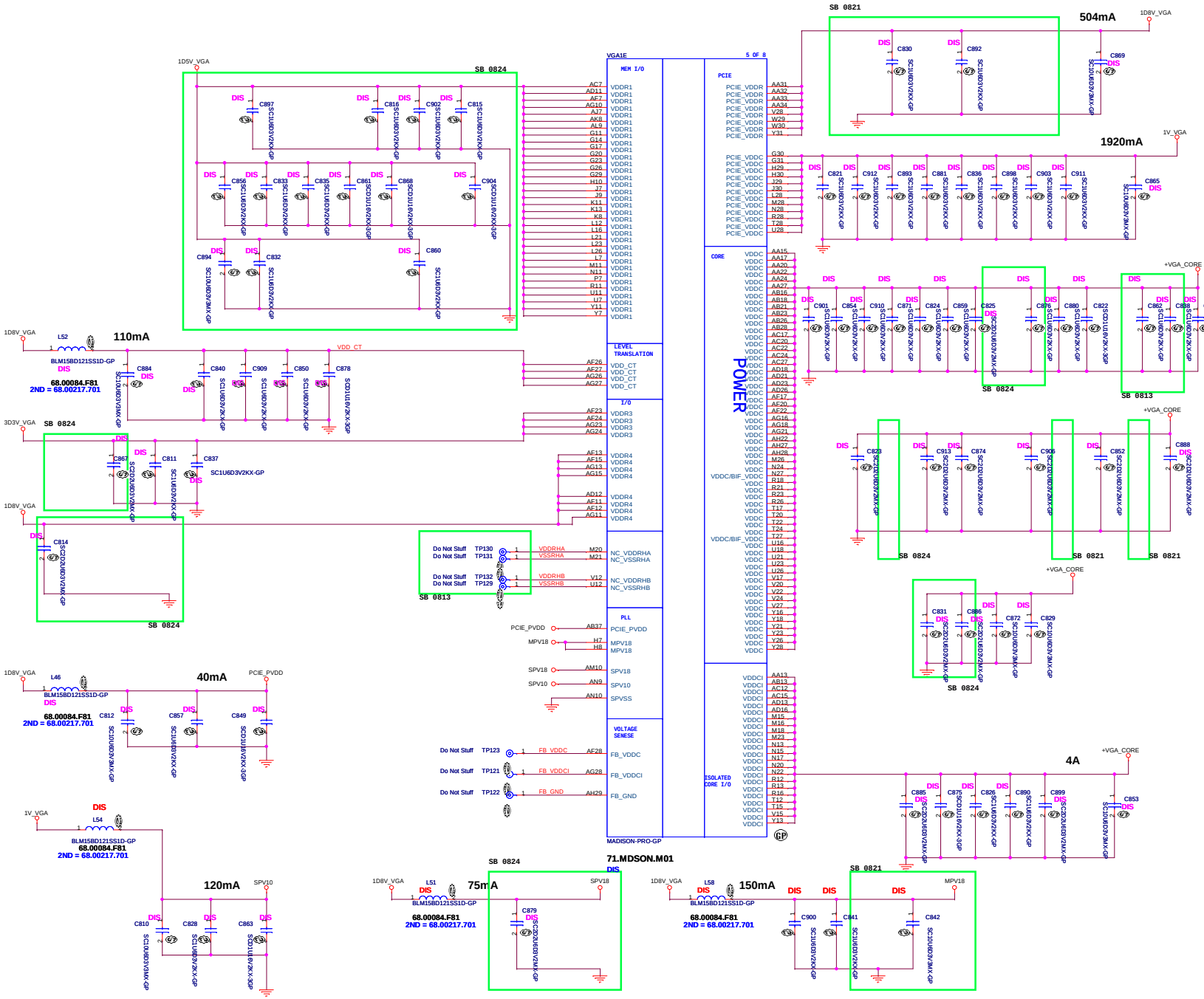
It's strap for GDDR3-136ball
Need to Clarify

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

For Thermal sensor

ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Madison IO		
Size: A2	Document Number: JV50-CP	Rev: SB
Date: Thursday, September 03, 2009	Sheet 63 of 68	


SB 0821
504mA
1D8V_VGA
1920mA
1V_VGA
+VGA_CORE
SB 0824
SB 0813
110mA
3D3V_VGA
40mA
PCIE_PVDD
4A
120mA
SPV10
75mA
SPV18
150mA
MPV18
VGA1E
MEM I/O
PCIE
CORE
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENESE
ISOLATED CORE I/O
POWER
MADISON-PRO-GP
71.MDSON.M01
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Madison POWER
Size
A2
Document Number
JV50-CP
Rev
SB
Date: Wednesday, August 26, 2009
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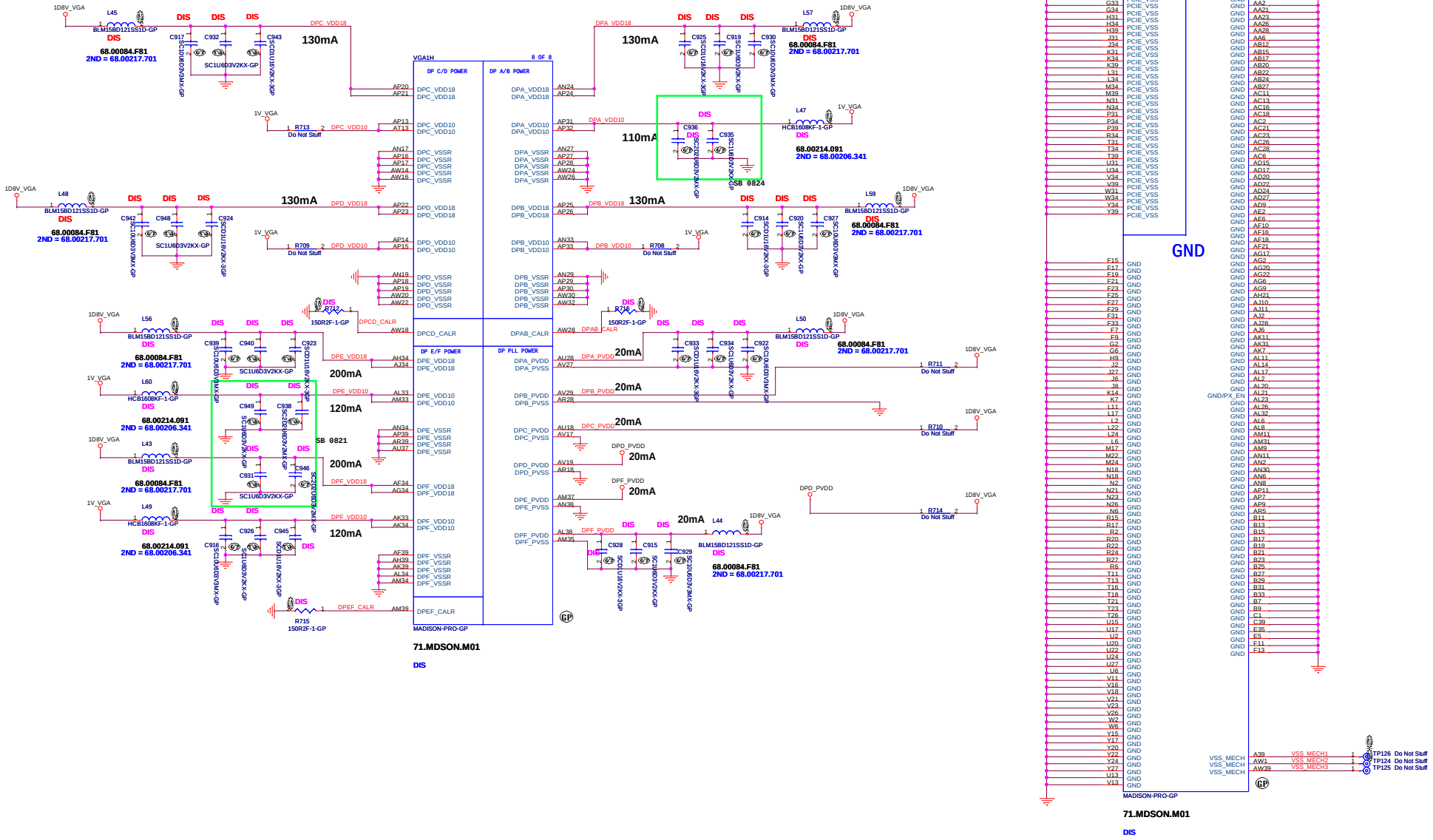
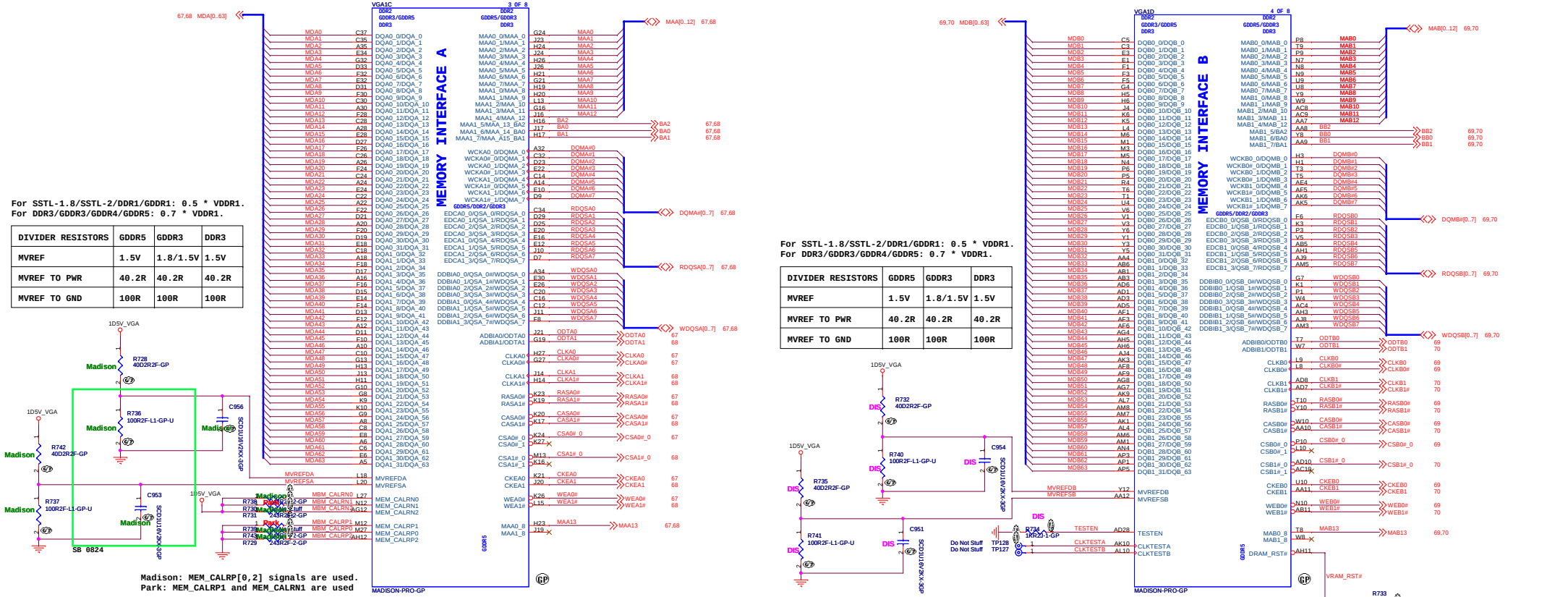


ENG DIS MADSION SAMSUNG

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DP POWER_GND	
Size: A2	Document Number: JV50-CP	Rev: SB
Date: Wednesday, August 26, 2009	Sheet 65 of 68	



DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

ENG DIS MADSION SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Madison Memory / Straps**

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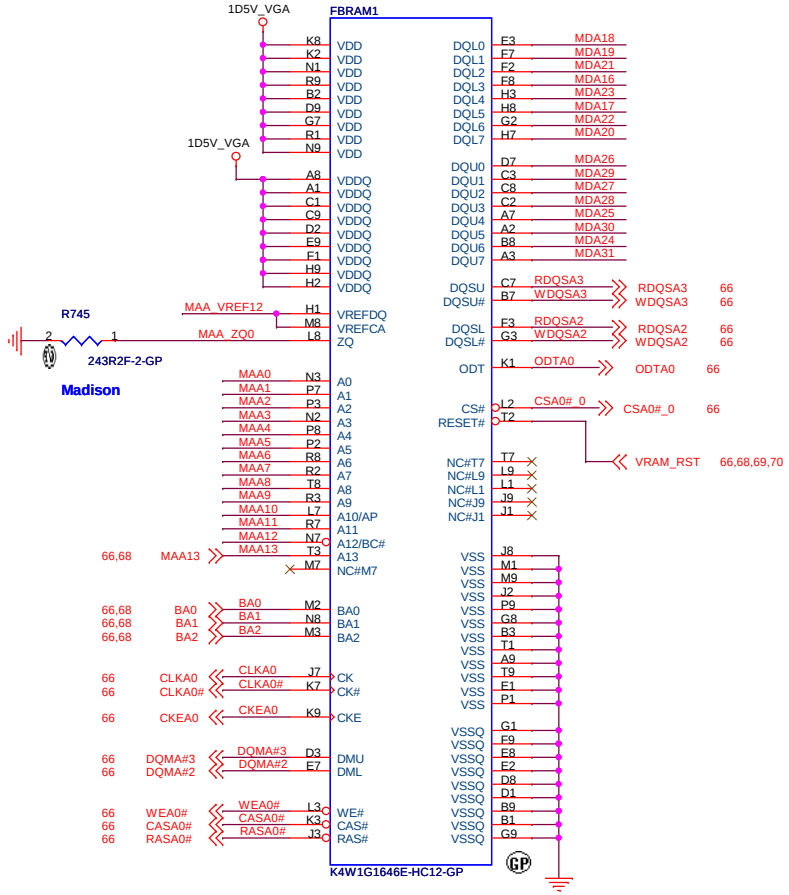
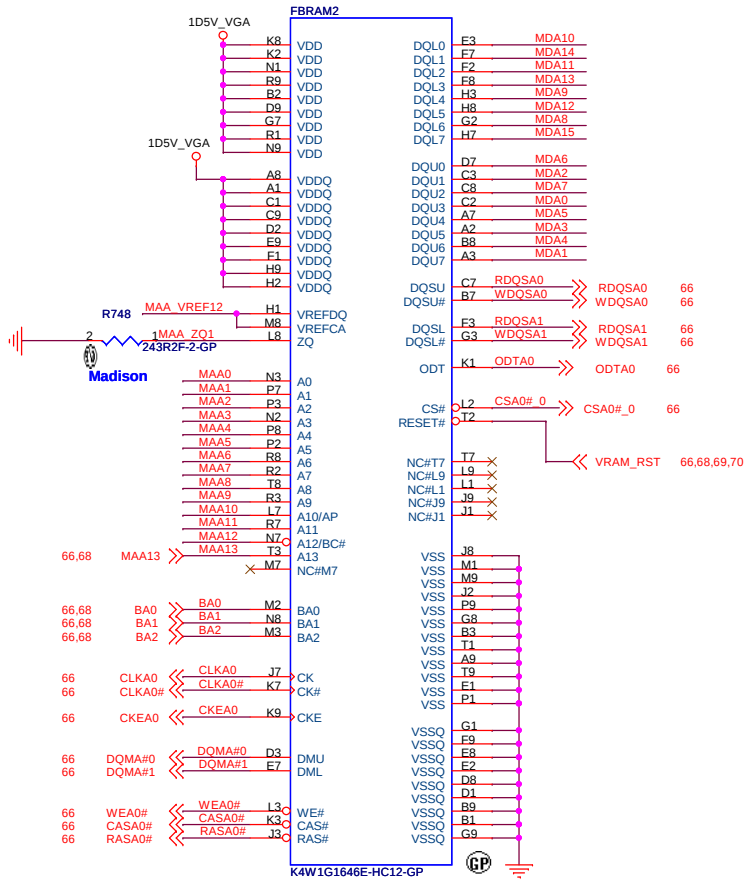
Date: Thursday, September 03, 2009 | Sheet 66 of 68

DDR3





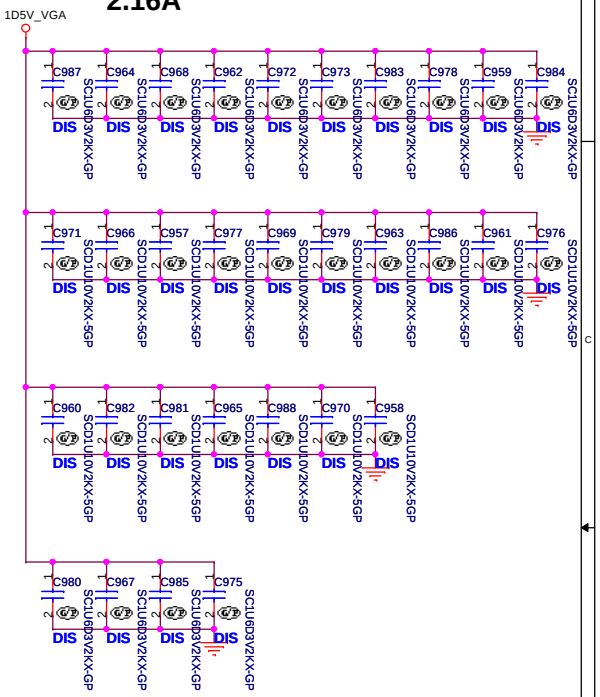
Madison

72.41164.H0U

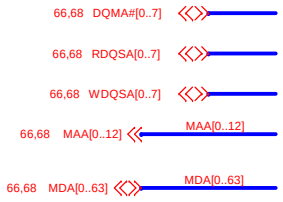
Madison

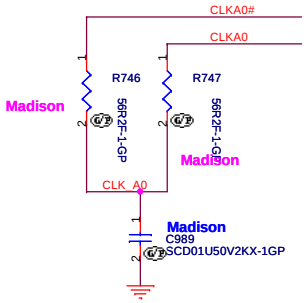
72.41164.H0U

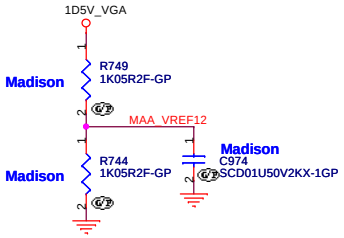
2.16A



SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U







ENG DIS MADSION SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***VRAM(1/4)***		
Size: A3	Document Number: **JV50-CP**	Rev: SB
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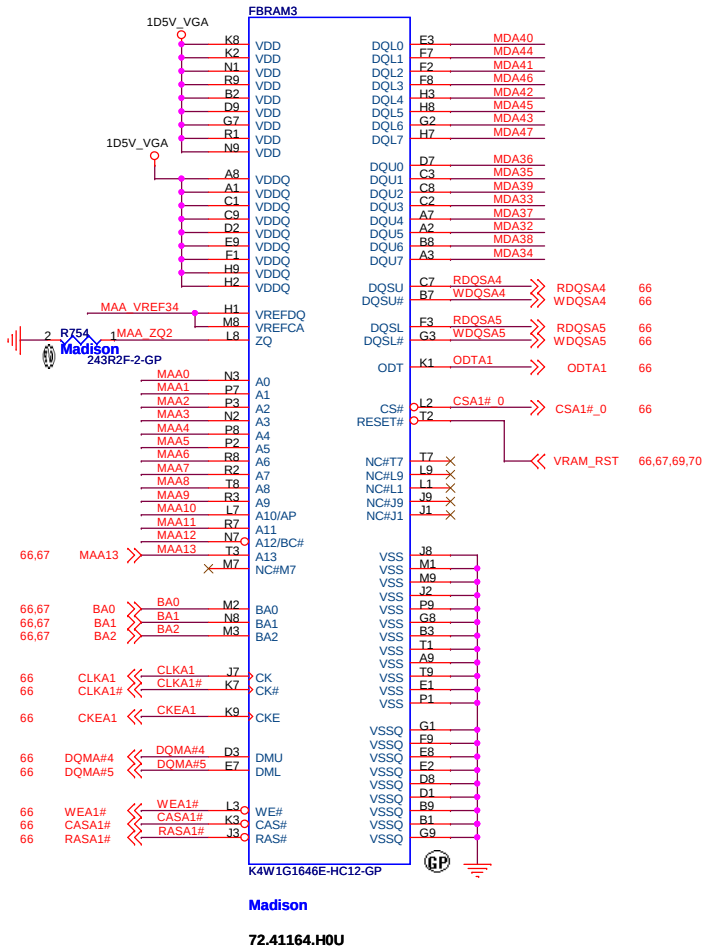
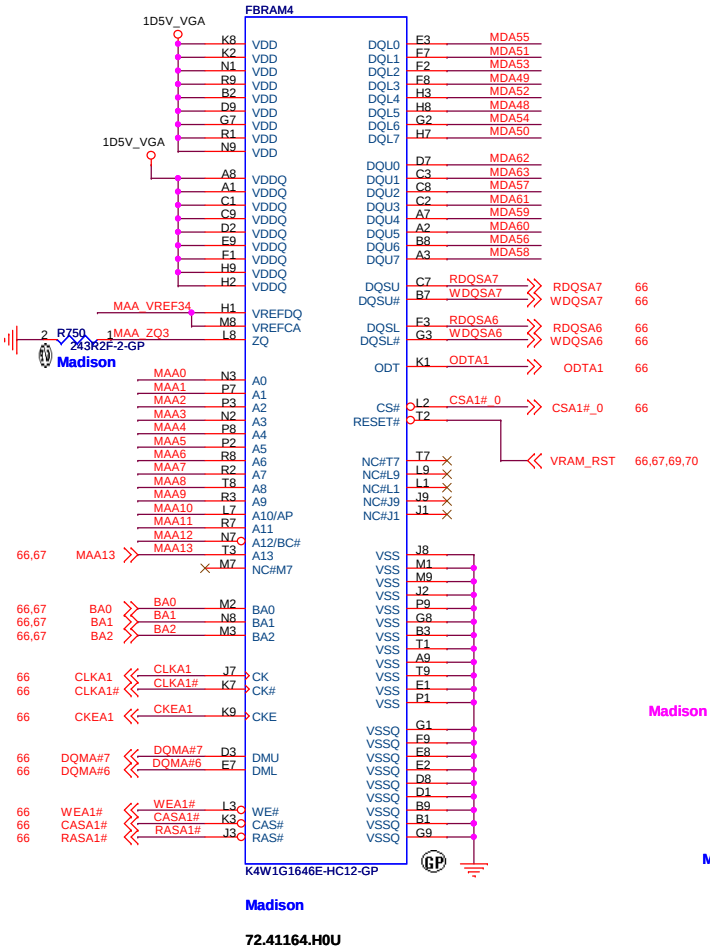
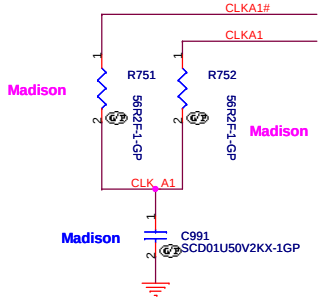
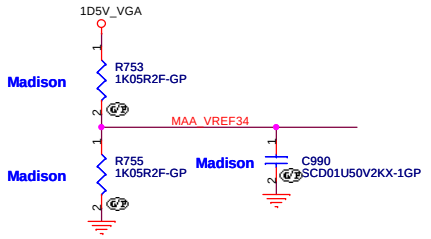
DDR3







SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

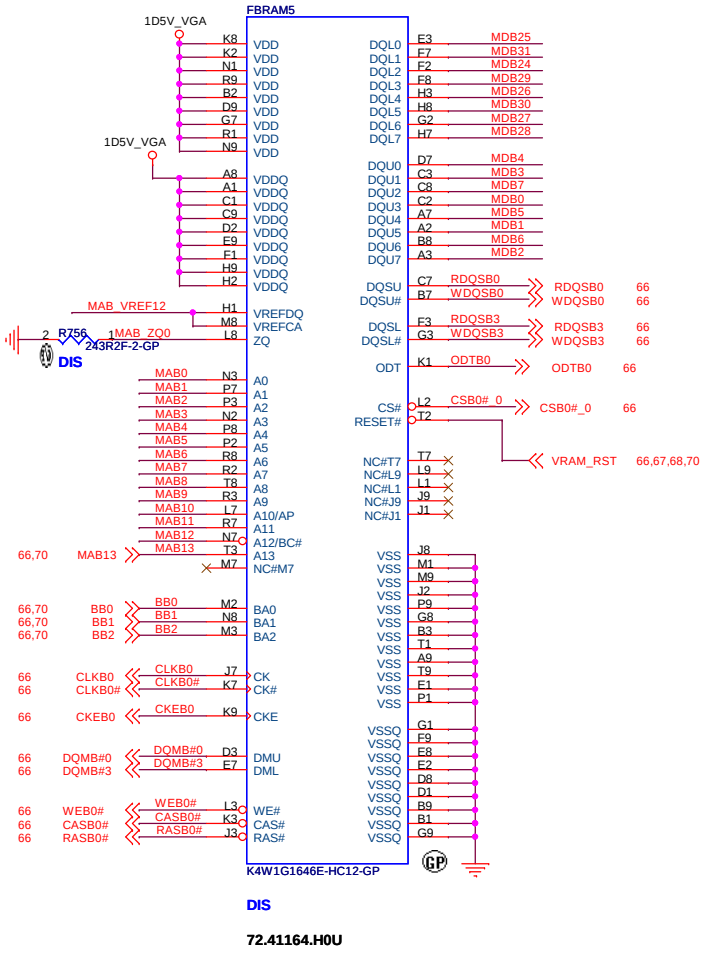


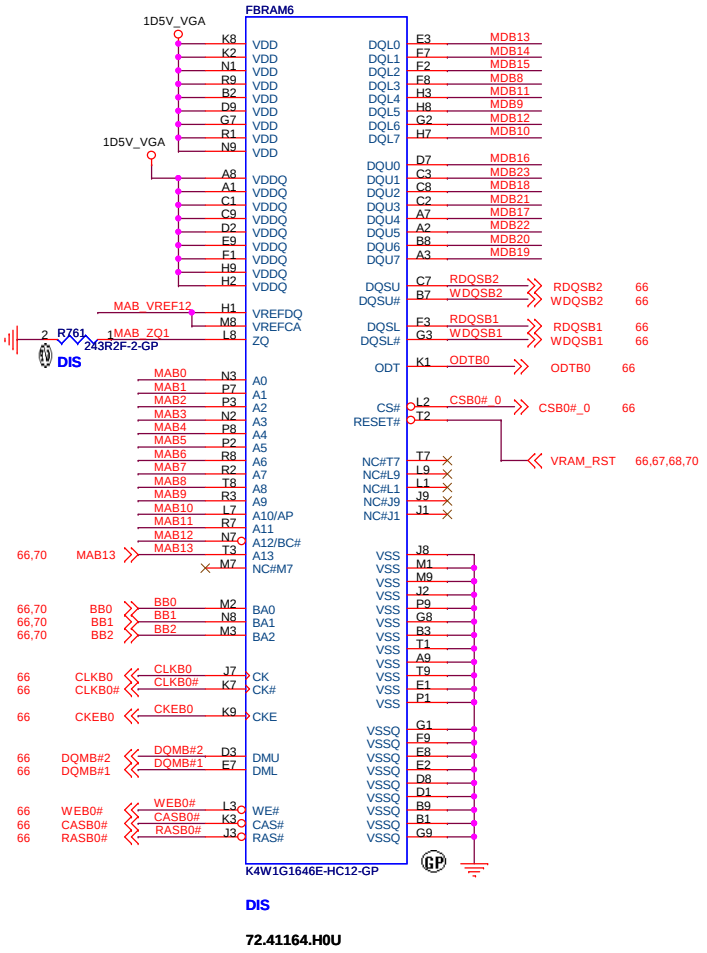
66,67 DQMA#[0..7]
66,67 RDQSA[0..7]
66,67 WDQSA[0..7]
66,67 MAA[0..12] MAA[0..12]
66,67 MDA[0..63] MDA[0..63]

ENG DIS MADSION SAMSUNG

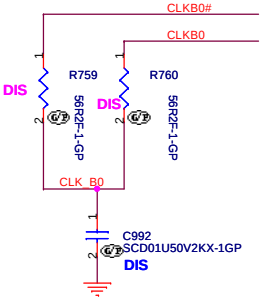
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *VRAM(2/4)*		
Size: A3	Document Number: JV50-CP	Rev: SB
Date: Thursday, September 03, 2009	Sheet 68 of 68	

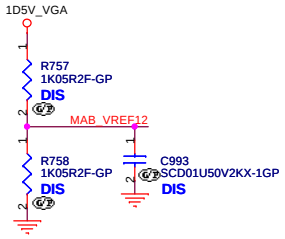
DDR3





SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U





66,70 DQMB#[0..7]
66,70 RDQSB[0..7]
66,70 WDQSB[0..7]
66,70 MAB[0..12] MAB[0..12]
66,70 MDB[0..63] MDB[0..63]

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
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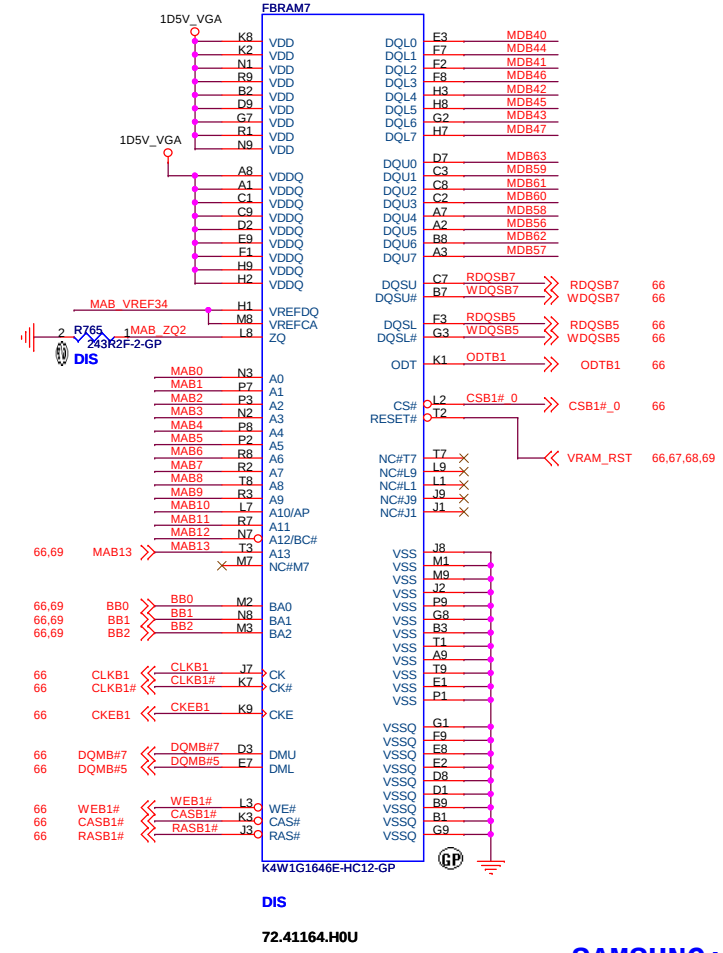

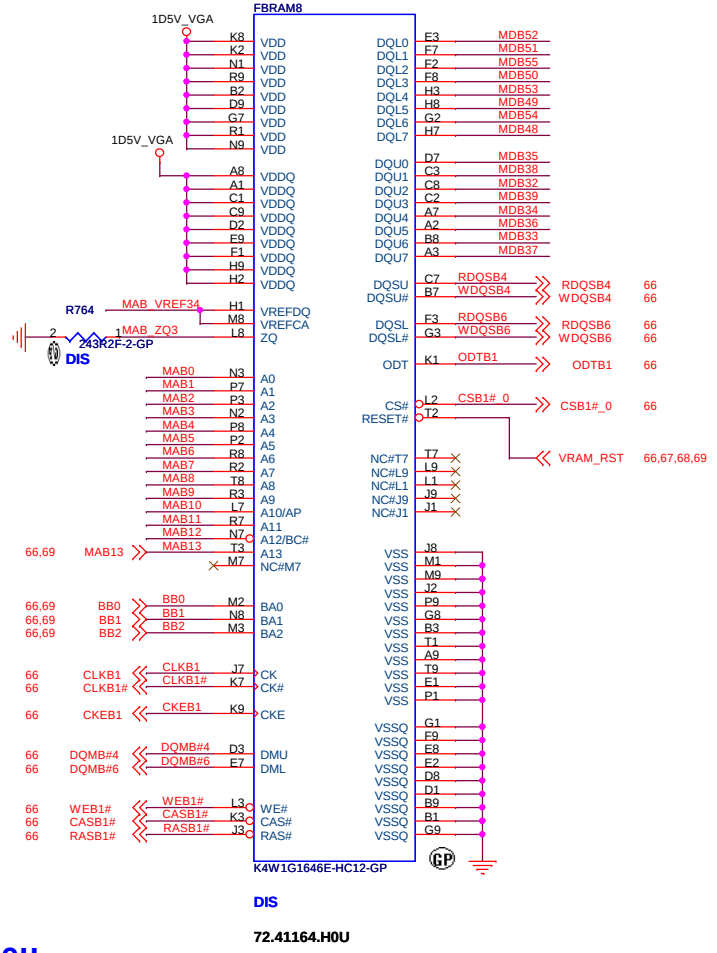

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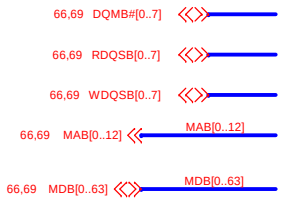

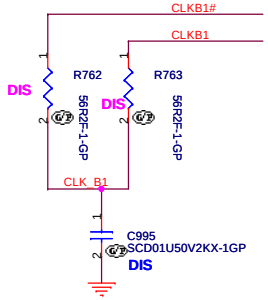

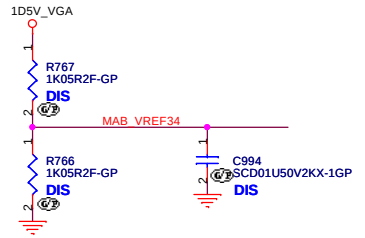

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