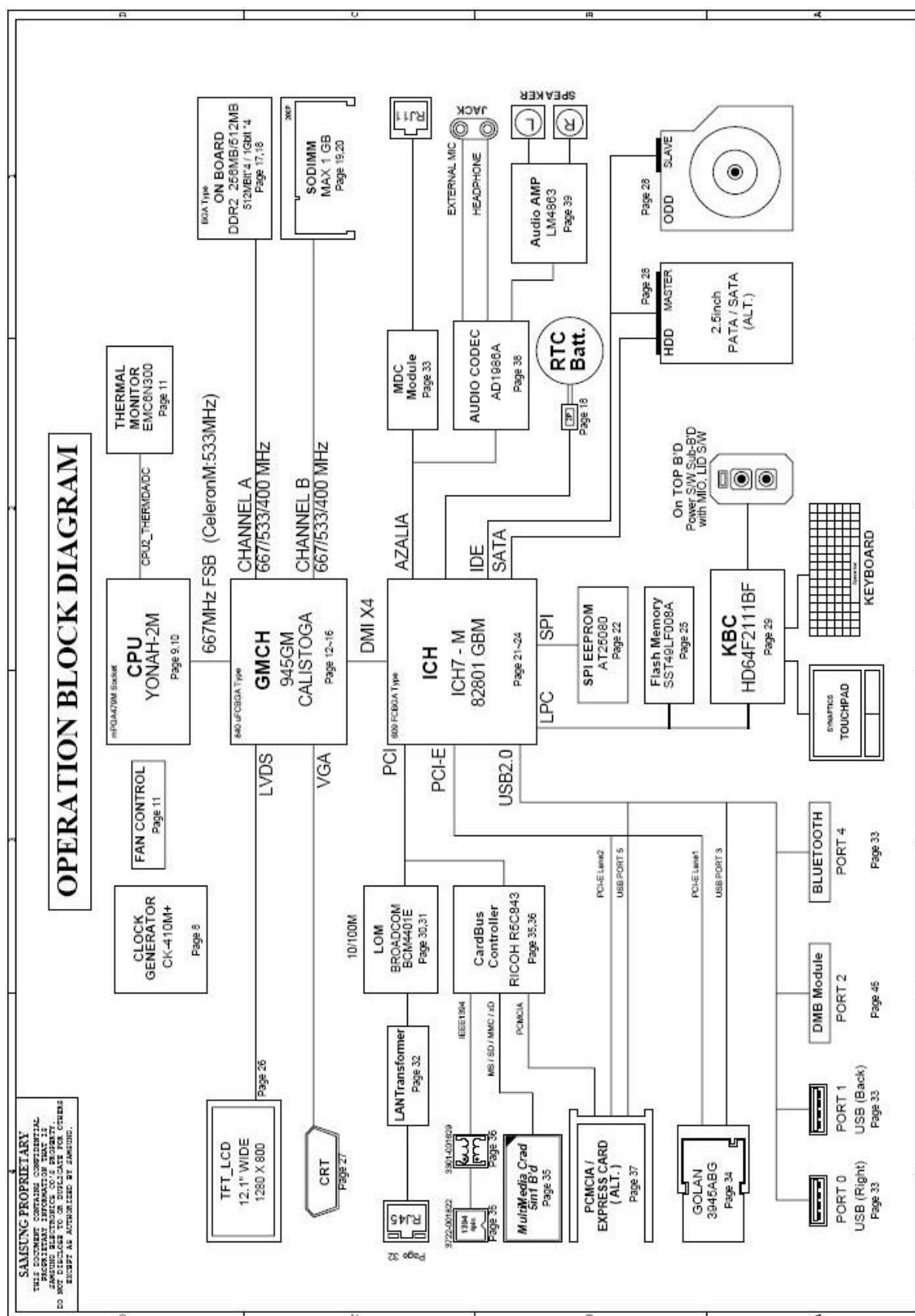


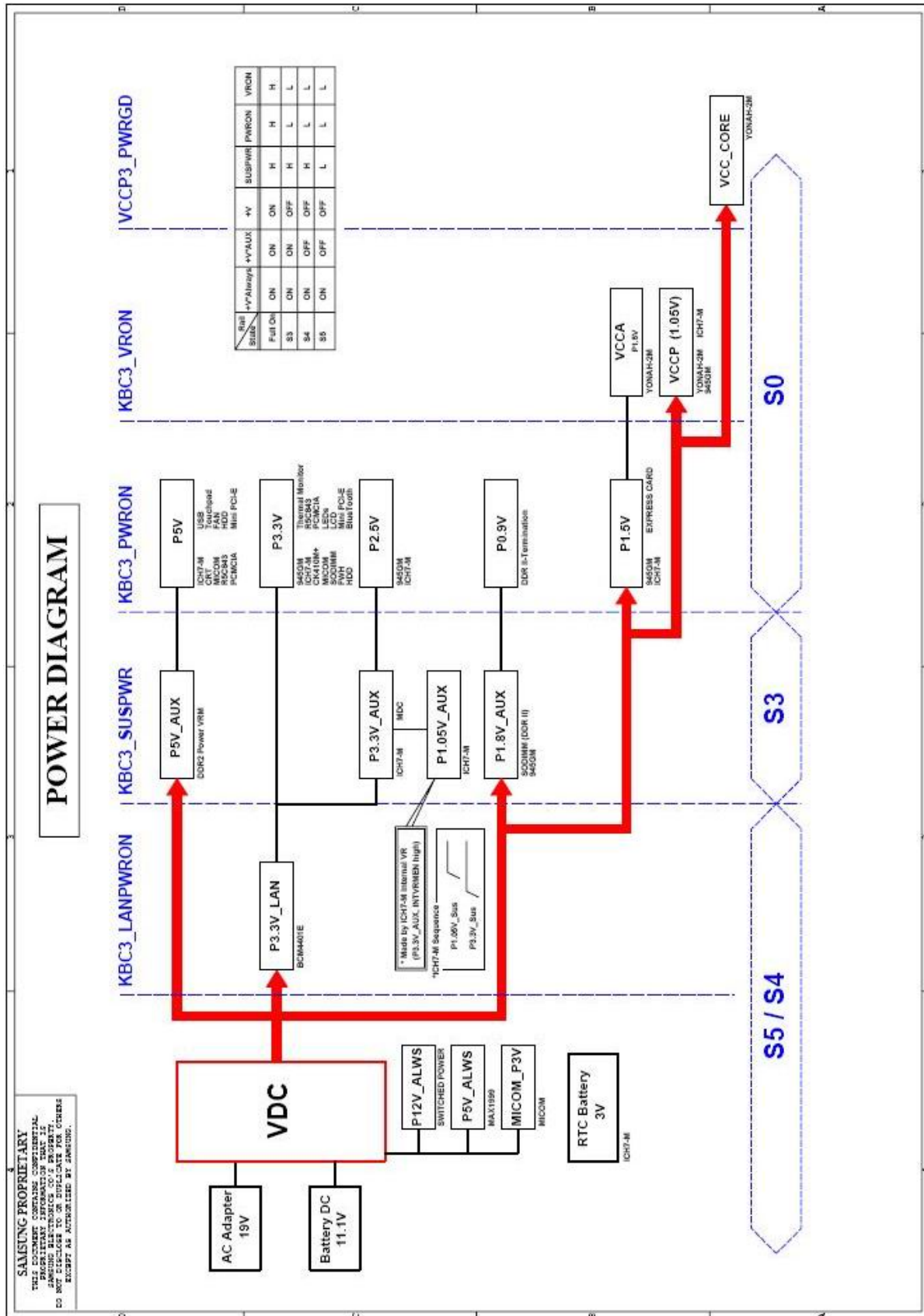
8. System Block Diagram

8-1 Operation Block Diagram



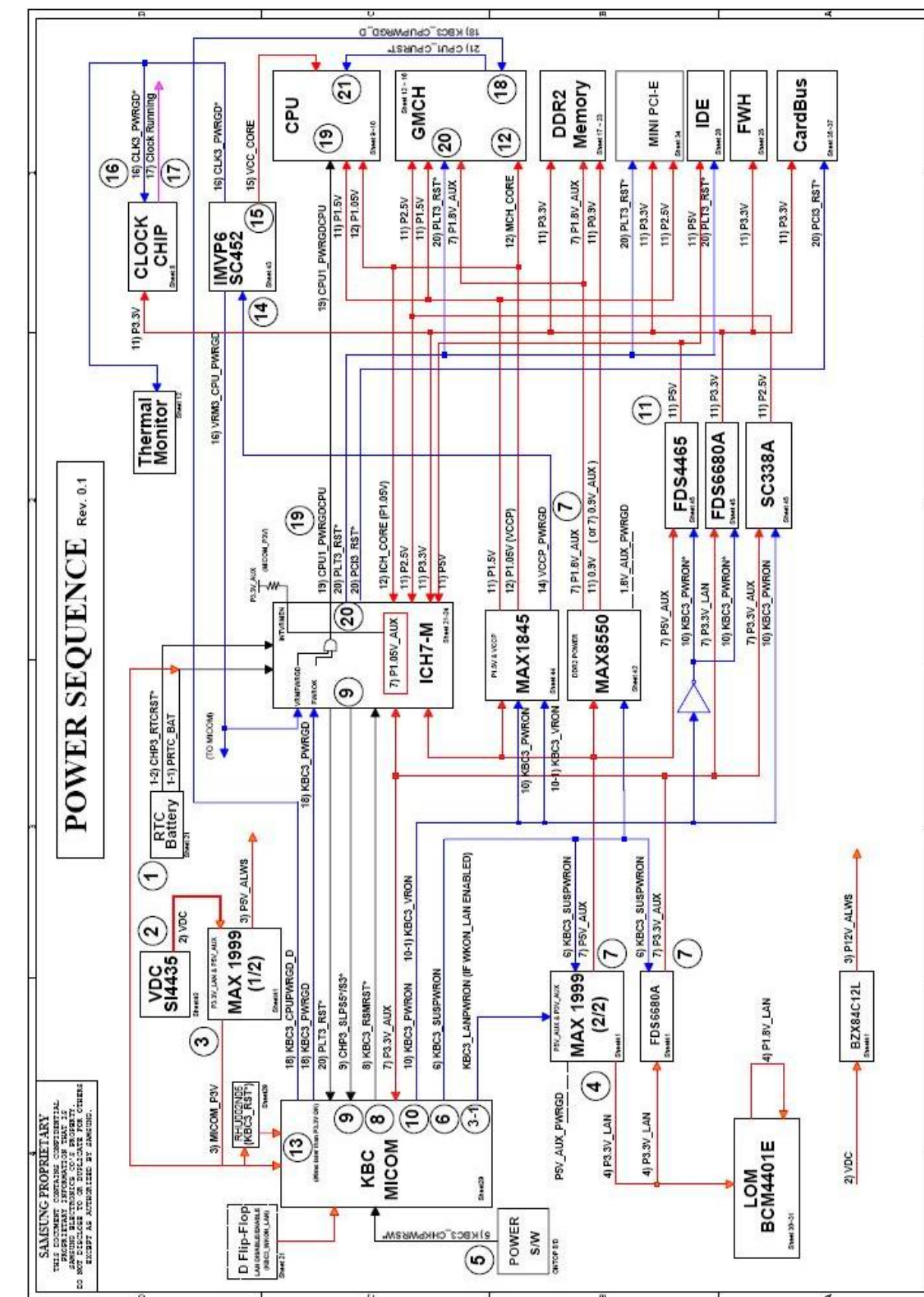
8. System Block Diagram

8-2 Power Diagram



8. System Block Diagram

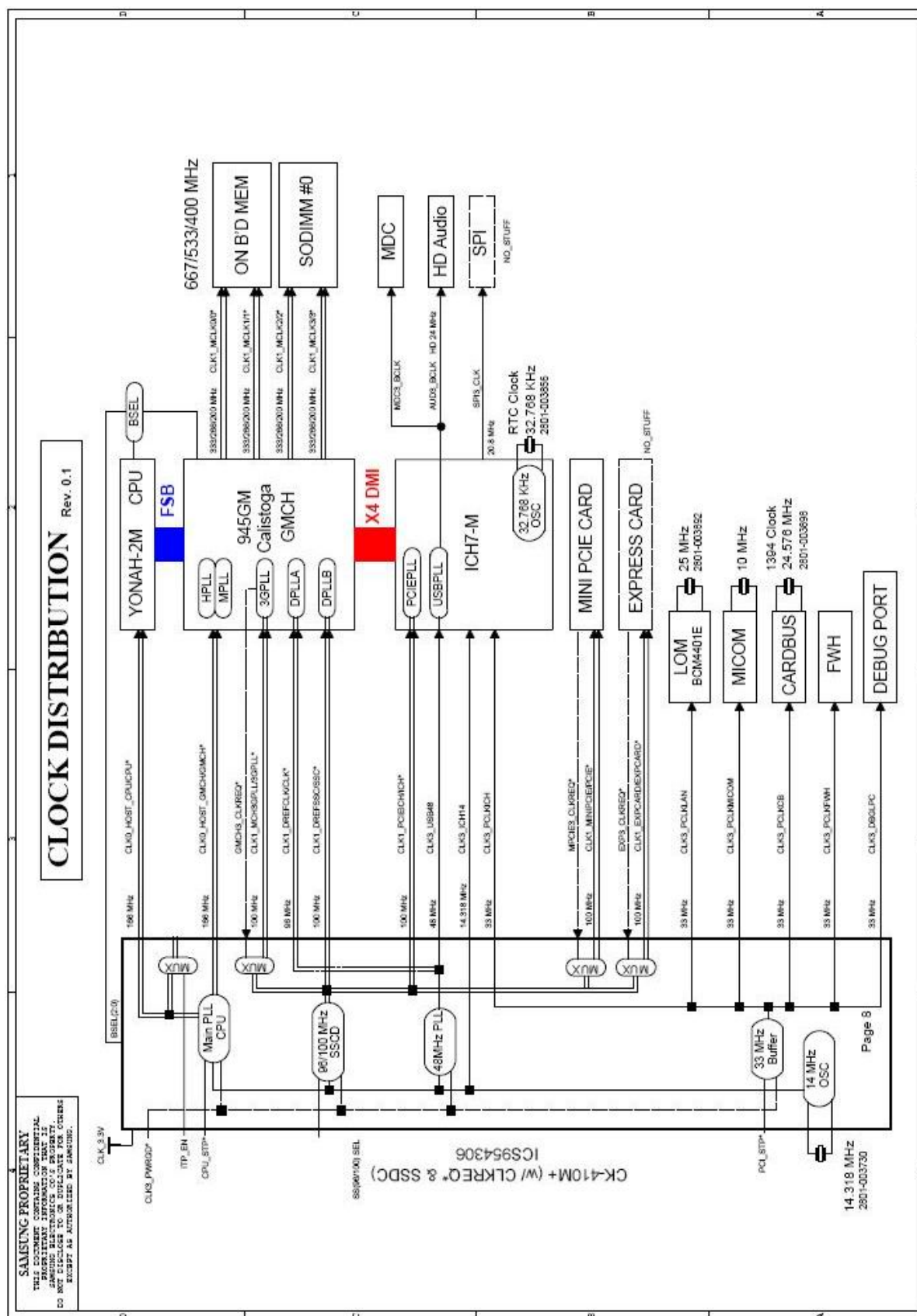
8-3 Power Sequence



[illegible]

8. System Block Diagram

8-5 Clock Distribution



8-6 Board Information

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Services	DSEL#	REGID#	Interrupts
AdBus	AD08 AD27	0	E7, D
USB	AD26(internal)	-	USBD0 #0 A USBD0 #1 B USBD0 #2 C
PCMCIA	AD30(internal) AD31(internal)	- -	B B
Internal MAC	AD34(internal)	-	MAC

Voltage Rails

VCC	Primary DC system power supply (7 to 21V)
VCC2_CORE	Core voltage for Processor P1 (3.06-4.08V)
VTT	Termination (1.05V)
	CMC1.8, C5H7 Core Voltage
P1_5V_AUX	1.5V power rail for DDC2 (off in S4-S8)
P1_5V	1.5V switched power rail (off in S4-S8)
P2_5V	2.5V switched power rail (off in S4-S8)
P3_3V	3.3V switched power rail (off in S4-S8)
P3_5V	3.5V switched power rail (off in S4-S8)
P4_3V_AUX	3.3V power rail (off in S4-S8)
P4_3V	3.3V power rail (off in S4-S8)
P5_3V_AUX	3.3V power rail (Always On)
P5_3V_LAN	3.3V power rail (Always On)
FWT0_BOOT	3.3V power rail (ALWAYS ON)
MC0M_PSV	3.3V power rail (Always On)
PSV_AUX	5V power rail (Always On)
P2V_ALWAYS	1.2V power rail (Always On)

²C / SMB Address

Device	Address	Hex	Bus
CH7	Master	-	SMbus Master
CCGMAN	1010 010x	ACh	
(Clock Generator)	1101 010x	D2h	Clock, Unused Clock Output Disabled
2C40M+	Master	-	SMbus Master
WCOM	0001 011x	18h	
BATTERY	0001 011x	EEh	Thermal Sensor
2B18300(CPU Thermal Sensor)			

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1	SYSTEM PORT B
2	SYSTEM PORT C
3	SYSTEM PORT D
4	MINI-C
5	MINI-D
6	BLUETOOTH
7	ETHERNET
8	ETHERNET
9	ETHERNET
10	ETHERNET
11	ETHERNET
12	ETHERNET
13	ETHERNET
14	ETHERNET
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98	ETHERNET
99	ETHERNET

System Power States

CHRP_SLPST S1: **System-On-Chip-SLPST**: In this state, all disallowed the 7860M chip are disabled.
CHRP_SLPST S2: **Power-On-Supervisor-SLPST**: The system controller is maintained in SLPST, the CPU, memory controller, memory, and all other critical subsystems Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Sleep State or Deep Sleep State.
CHRP_SLPST S3: **Power-On-Supervisor-SLPST**: This state is used to reduce the leakage power.
CHRP_SLPST S4: **Power-On-Supervisor-SLPST**: The system controller is maintained in SLPST, the power is shut off to non-critical circuits.
CHRP_SLPST S5: **Power-On-Supervisor-SLPST**: Memory is retained, and refreshes continue. All clocks are except PFC clock.
CHRP_SLPST S6: **Power-On-Supervisor-SLPST**: The content of the system is maintained on state. All power is then shut off to the system except for the logic required to resume.
CHRP_SLPST S7: **Power-On-Supervisor-SLPST**: System content is not maintained. All power is shut off except for the logic required to resume. A full boot is required when waking.

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICHT-M	Real Time Clock
Crystal	10MHz	CMCM	H34P71692160
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	24.576MHz	Cirrus Controller	1304
Crystal	25MHz	LAN	Intel LAN

CPU Core Voltage Table

[illegible]

*Fourth Processor (2.33 GHz / 1.00 GHz)