CICHLID

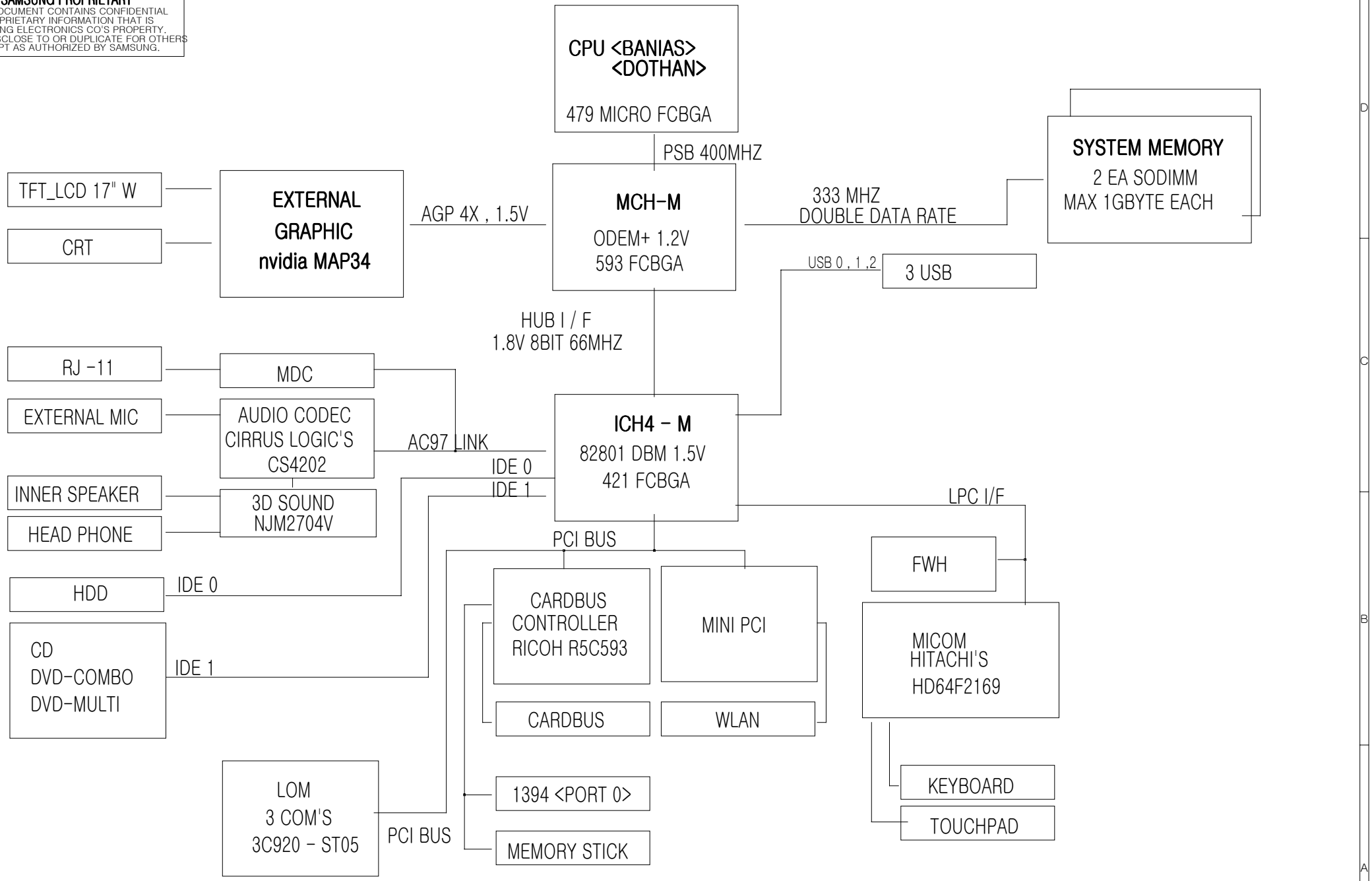
CPU : BANIAS/DOTHAN
Chip Set : MCH-M ODEM+
Remarks : TEMP

Model Name : CICHLID MAIN
PBA Name : BA92-02649A
PCB Code : BA41-00392A
Dev. Step : MP
Revision : 1.0

DRAW	CHECK	APPROVAL

Table of Contents

DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	COVER	PART NO.: BA41-00392A
MODULE CODE:	LAST EDIT: March, 30, 2004 10:12:30 AM	PAGE 1 OF 41	



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CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	BLOCK DIAGRAM	PART NO.: BA41-00392A
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD19	0	A,B,C
LAN	AD21	3	D
MiniPCI SLOT1	AD23	2	E,F
USB	AD29(internal)	-	USB2.0 #0 : A USB2.0 #1 : D USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
AGP	AD17(internal)	-	A,B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
		-	-
PCI SLOT	AD20		A,B,C,D

CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V	
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V	
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V	
0	0	0	0	1	1	1.660 V	1	0	0	0	1	1	1.148 V	
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V	
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V	
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V	
0	0	0	1	1	1	1.596 V	1	0	0	1	1	1	1.084 V	
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V	
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V	
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V	
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V	
0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V	
0	0	1	1	0	1	1.500 V	1	0	1	1	0	1	0.988 V	
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0	0.972 V	
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V	
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V	
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V	
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V	
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V	
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V	
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V	
0	1	0	1	1	0	1.356 V	1	1	0	1	1	0	0.844 V	Lowest Freq.
0	1	0	1	1	1	1.340 V	1	1	0	1	1	1	0.828 V	
0	1	1	0	0	0	1.324 V	1	1	1	0	0	0	0.812 V	
0	1	1	0	0	1	1.308 V	1	1	1	0	0	1	0.796 V	Highest Freq.
0	1	1	0	1	0	1.292 V	1	1	1	0	1	0	0.780 V	
0	1	1	0	1	1	1.276 V	1	1	1	0	1	1	0.764 V	
0	1	1	1	0	0	1.260 V	1	1	1	1	0	0	0.748 V	Deeper Sleep
0	1	1	1	0	1	1.244 V	1	1	1	1	0	1	0.732 V	
0	1	1	1	1	0	1.228 V	1	1	1	1	1	0	0.716 V	
0	1	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V	

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for BANIAS CPU (1.356 ~ 0.844V)
VCCP	BANIAS/ODEM Processor System Bus(PSB) Termination (1.05V)
VCC_MCH	MCH-M Core Voltage (1.2V)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
P2.5V_AUX	2.5V power rail (off in S4-S5)
P1.25V_AUX	1.25V power rail (off in S4-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P3.3V_ALWAYS	3.3V always on Power Rail
P5V	5.0V switched power rail (off in S3-S5)
P5V_ALWAYS	5.0V always on power
P12V	12.0V switched power rail (off in S3-S5)

I²C / SMB Address

Devices	Address	Hex	Bus
ICH4	Master	-	SMBUS Master
ADM1032(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1	SYSTEM PORT B
2	SYSTEM PORT C
3	FINGER PRINT
4	BLUETOOTH

System Power States

CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other criticial subsystems.
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.

CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
Memory is retained, and refreshes continue. All clocks stop except RTC clock.

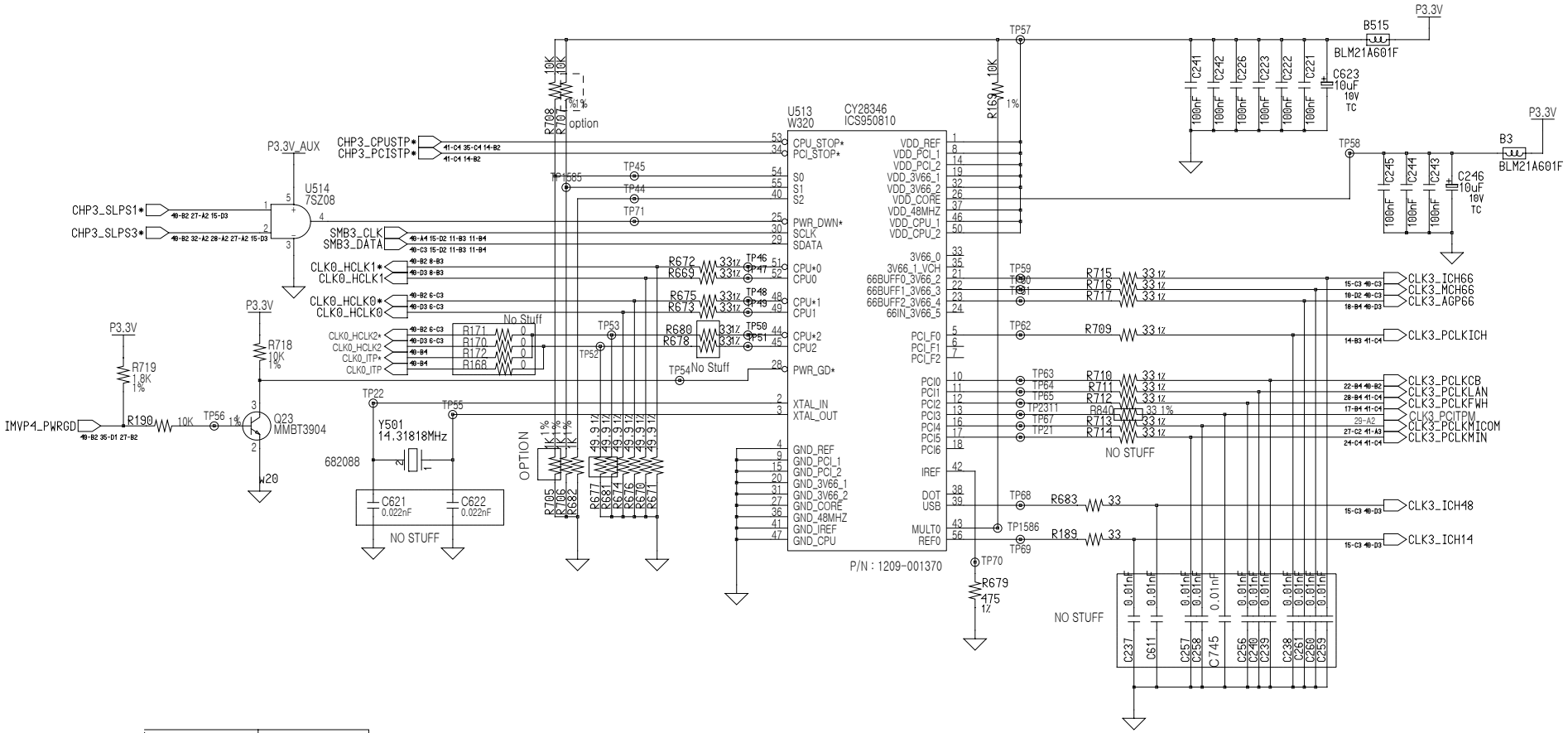
CHP3_SLP4S* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
Externally appears same as S5, but may have different wake events.

CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

REVISION HISTORY

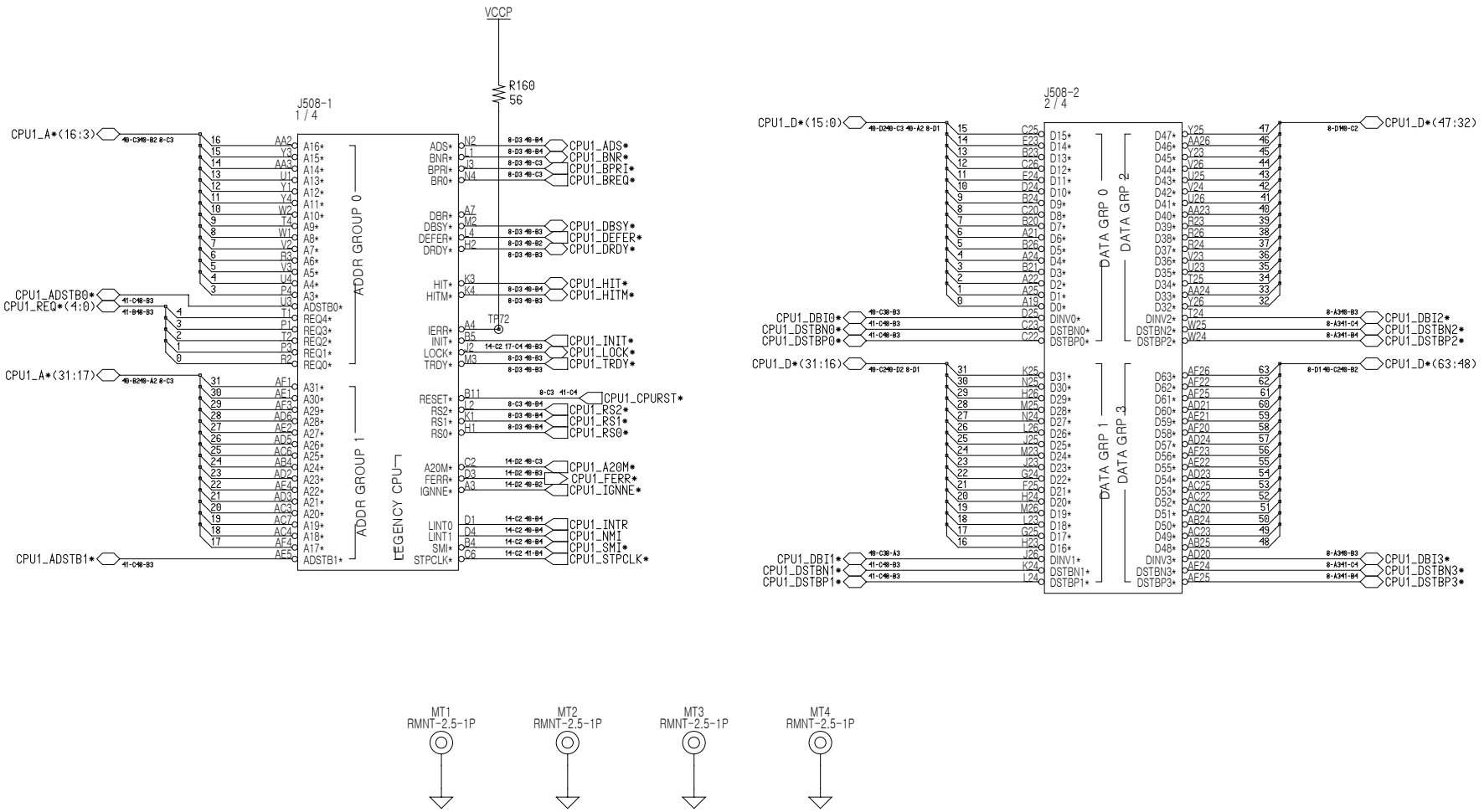
See rev notes in the changes file for more information.

DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	BOARD INFORMATION	PART NO.: BA41-00392A
MODULE CODE	LAST EDIT: March, 30, 2004 10:13:36 AM	PAGE 3 OF 41	



SEL1	SEL0	HOST CLK
0	0	66MHz
0	1	100MHz
1	0	200MHz
1	1	133MHz

DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP	CLOCK GENERATOR	
APPROVAL: H.S, KIM	REV: 1.0		PART NO.: BA41-00392A
MODULE CODE	LAST EDIT: March, 30, 2004 10:14:03 AM	PAGE 4 OF 41	



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CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	BANIAS CPU (1/2)	PART NO.: BA41-00392A
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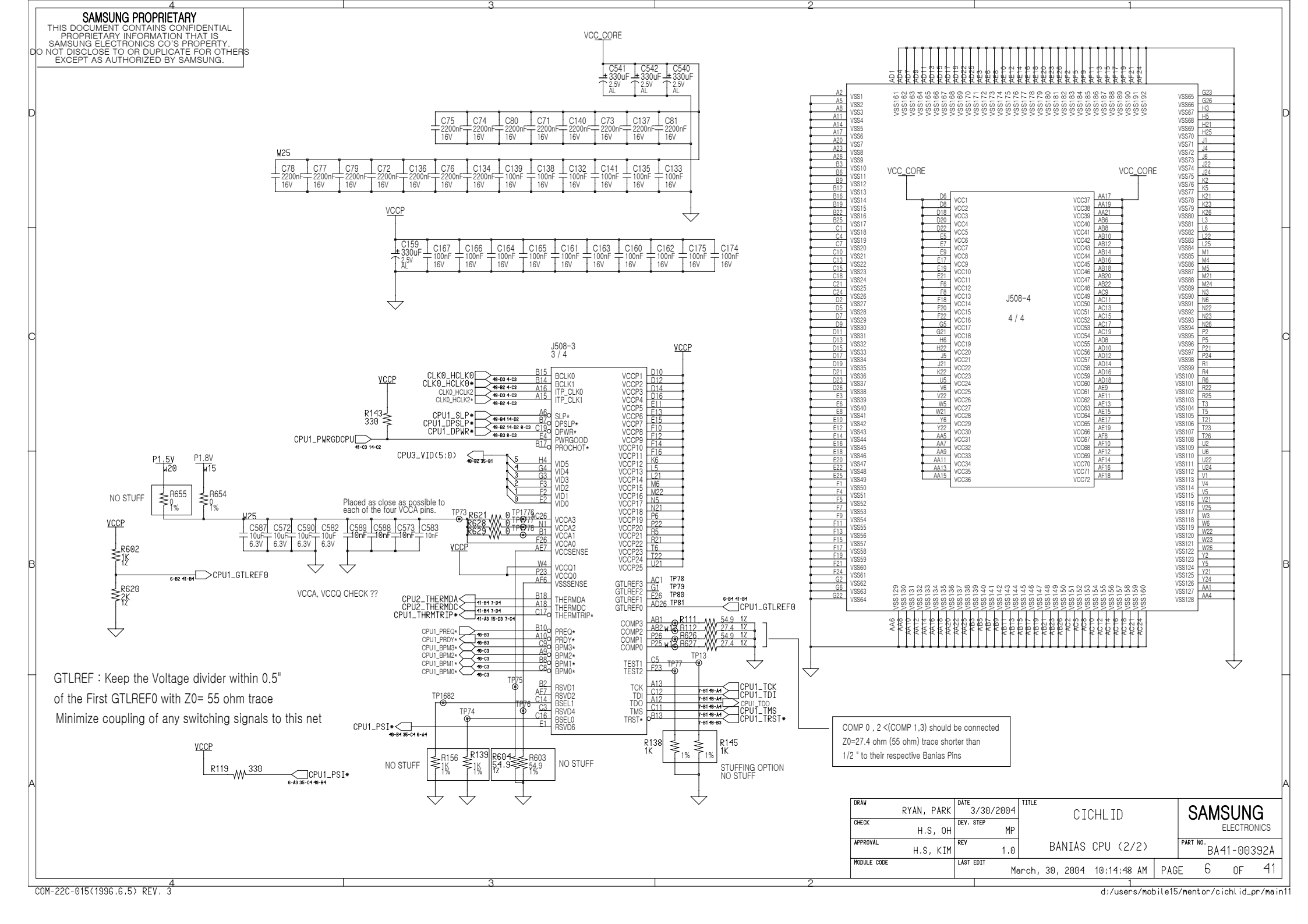

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CHECK: H.S, OH	DEV. STEP: MP	BANIAS CPU (2/2)	
APPROVAL: H.S, KIM	REV: 1.0		PART NO.: BA41-00392A
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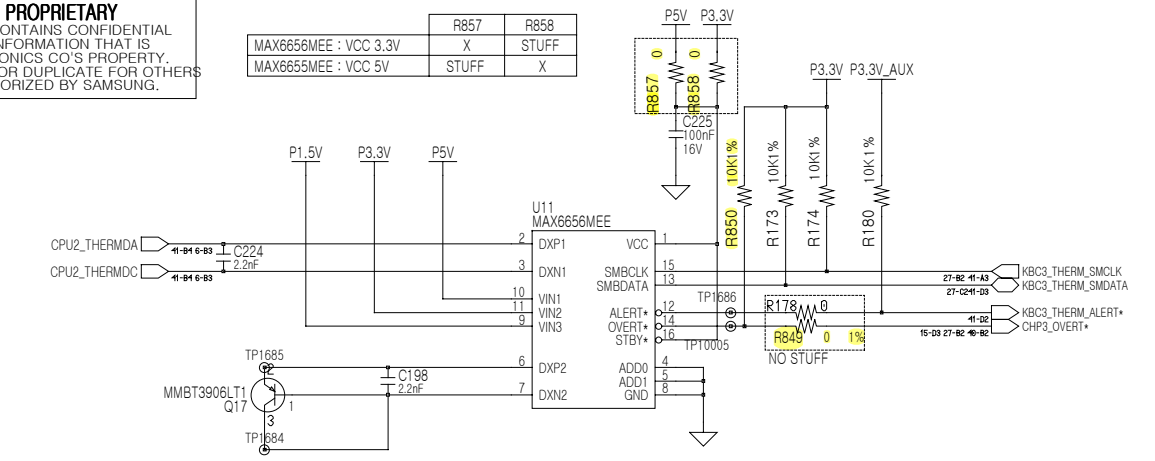
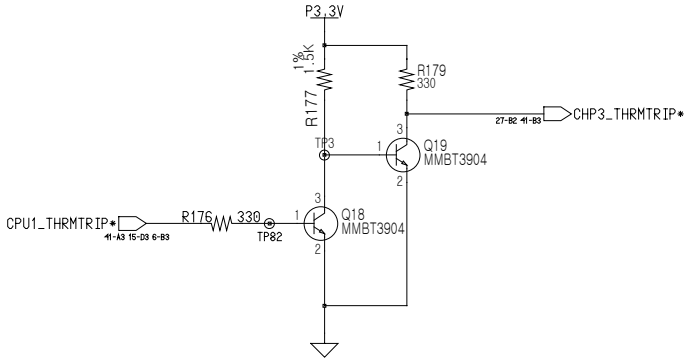
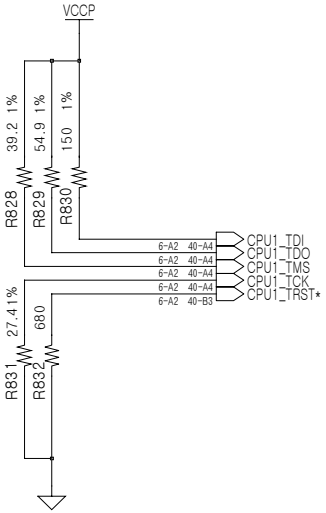
	R857	R858
MAX6656MEE : VCC 3.3V	X	STUFF
MAX6655MEE : VCC 5V	STUFF	X



Refer To Thermal Sensor Layout Guidelines.

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND

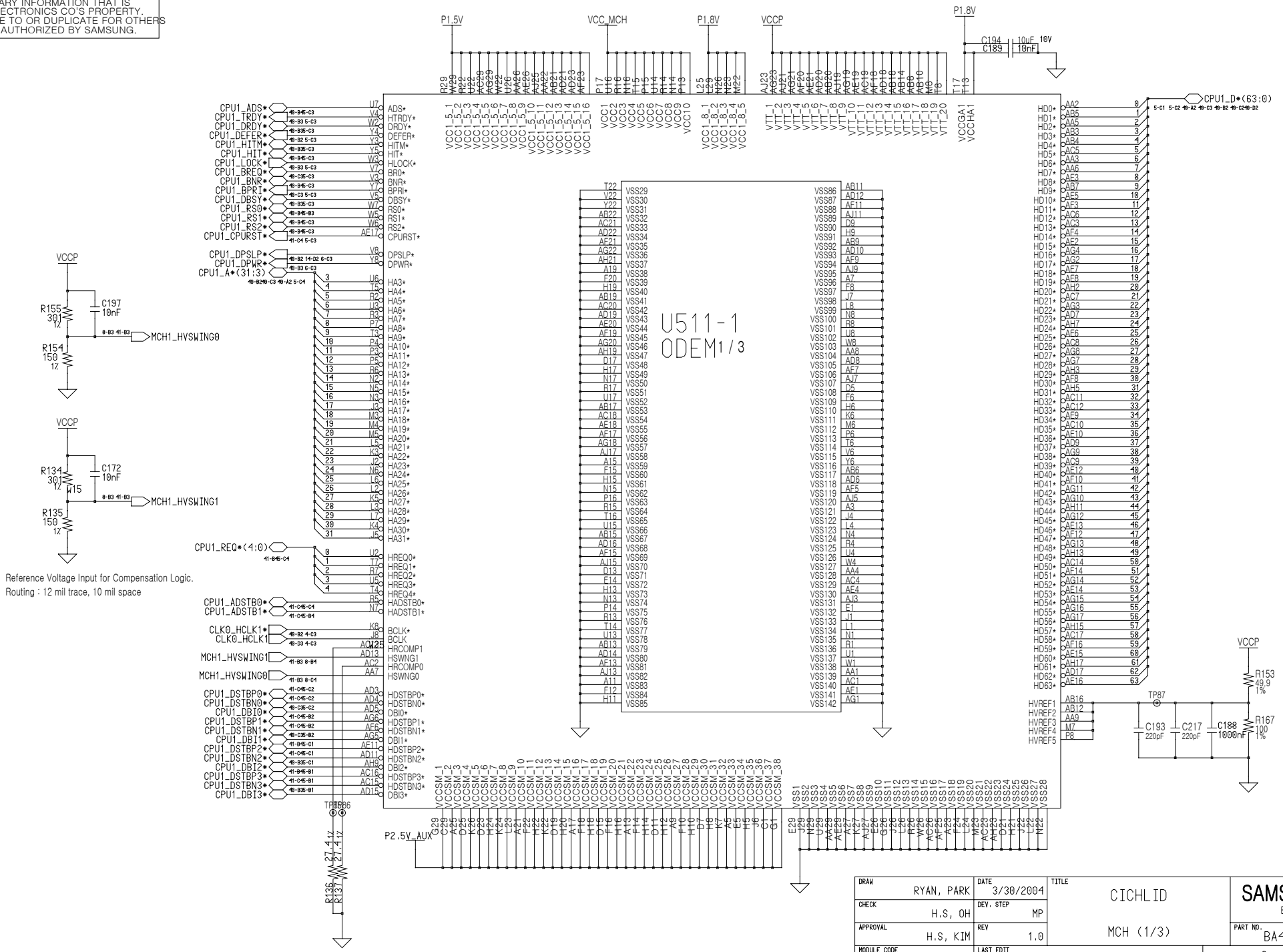




CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V	
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V	
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V	
0	0	0	0	1	1	1.660 V	1	0	0	0	1	1	1.148 V	
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V	
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V	
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V	
0	0	0	1	1	1	1.596 V	1	0	0	1	1	1	1.084 V	
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V	
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V	
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V	
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V	
0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V	
0	0	1	1	0	1	1.500 V	1	0	1	1	0	1	0.988 V	
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0	0.972 V	
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V	
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V	
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V	
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V	
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V	
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V	
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V	Lowest Freq.
0	1	0	1	1	0	1.356 V	1	1	0	1	1	0	0.844 V	
0	1	0	1	1	1	1.340 V	1	1	0	1	1	1	0.828 V	
0	1	1	0	0	0	1.324 V	1	1	1	0	0	0	0.812 V	
Highest Freq. 0	1	1	0	0	1	1.308 V	1	1	1	0	0	1	0.796 V	
0	1	1	0	1	0	1.292 V	1	1	1	0	1	0	0.780 V	
0	1	1	0	1	1	1.276 V	1	1	1	0	1	1	0.764 V	
0	1	1	1	0	0	1.260 V	1	1	1	1	0	0	0.748 V	Deeper Sleep
0	1	1	1	0	1	1.244 V	1	1	1	1	0	1	0.732 V	
0	1	1	1	1	0	1.228 V	1	1	1	1	1	0	0.716 V	
0	1	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V	

DRAW: KI. IM	DATE: 4/7/2003	TITLE: AQUILA W MAIN THERMAL SENSOR & VID	SAMSUNG ELECTRONICS
CHECK: KK.BIN	DEV. STEP: DV		
APPROVAL: DW.KIM	REV: 1.0		PART NO.: BA41-######A
MODULE CODE:	LAST EDIT: April 7, 2003 8:36:31 AM	PAGE 7 OF 42	



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CHECK: H.S, OH	DEV. STEP: MP	MCH (1/3)	
APPROVAL: H.S, KIM	REV: 1.0		PART NO.: BA41-00392A
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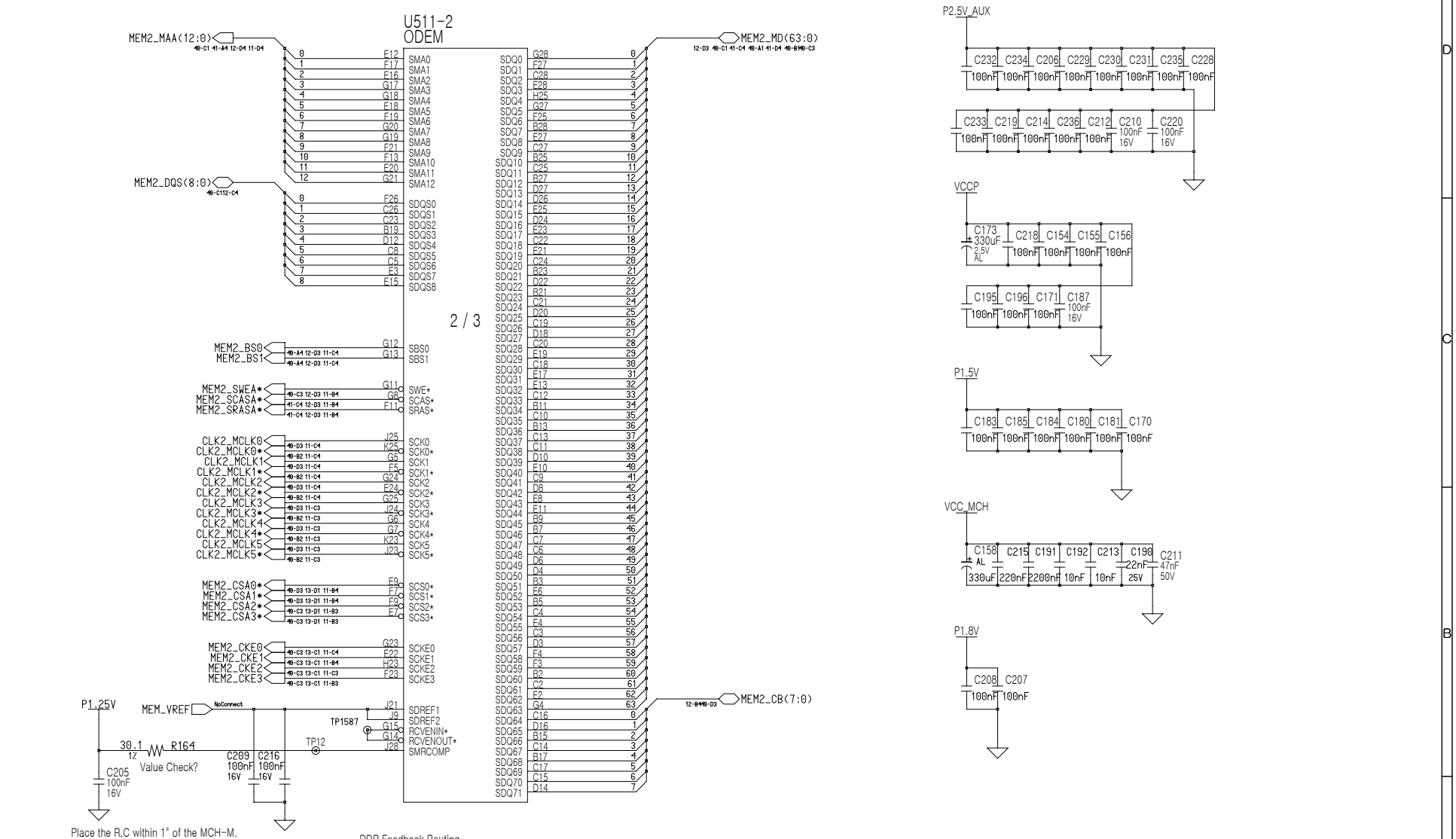

DDR Clocks Routing
> SCK/SCK#[0] = SCK/SCK#[1] = SCK/SCK#[2]
> SCK/SCK#[3] = SCK/SCK#[4] = SCK/SCK#[5]
> Differential clock length must be 1~2" longer than Strobe signals.
> Differential clock length must be 1~3" longer than Control and Command signals.

DDR Feedback Routing
MCH signal ball to signal Via = Max 40 mil
MCH output signal via to input signal via = 95mil ~ 105 mil
RCVEN Sinal must be routed on the same layer as the memory clocks.

DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	MCH (2/3)	PART NO.: BA41-00392A
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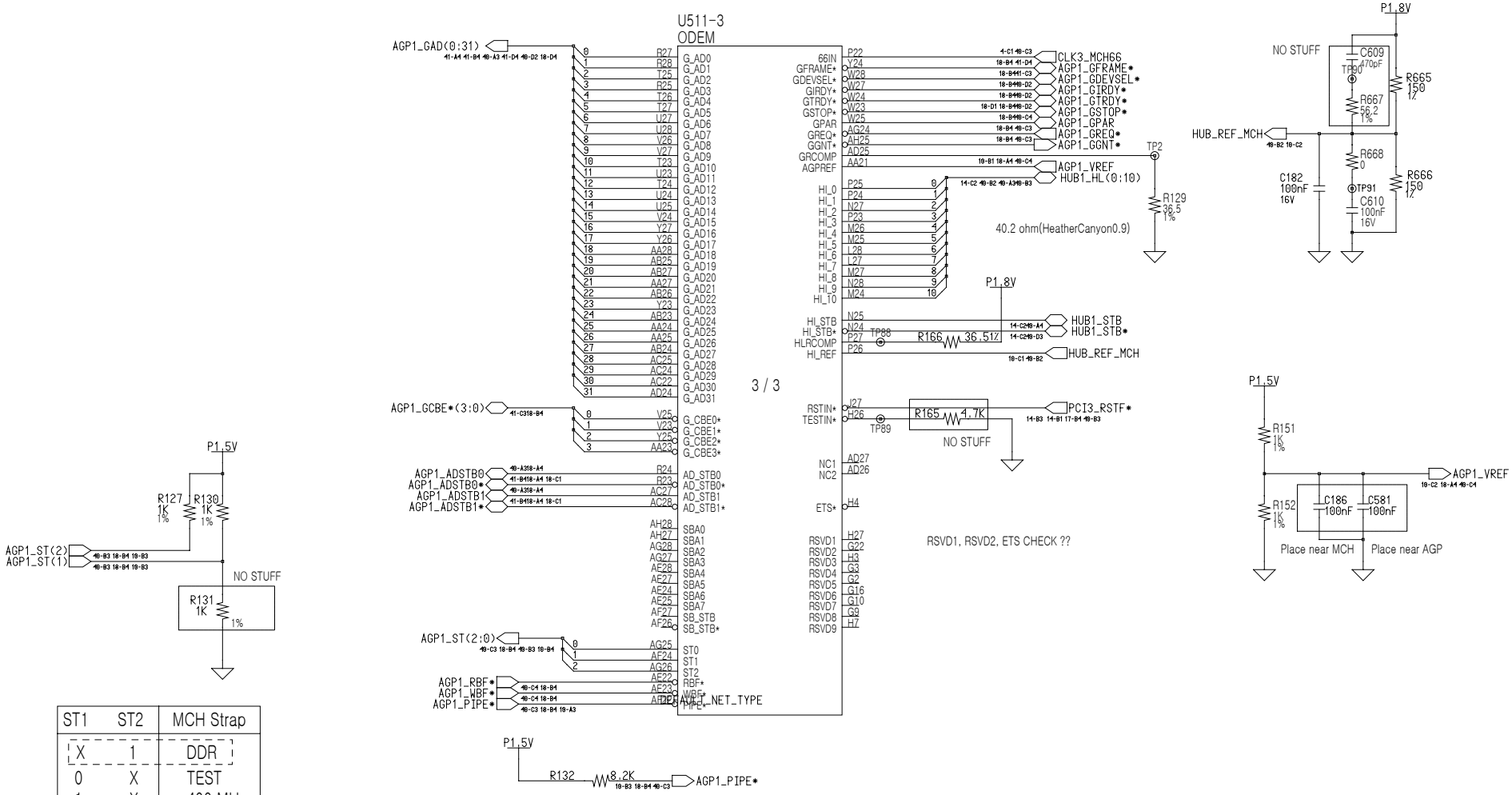

ST1	ST2	MCH Strap
X	1	DDR
0	X	TEST
1	X	400 MHz

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CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	MCH (3/3)	PART NO.: BA41-00392A
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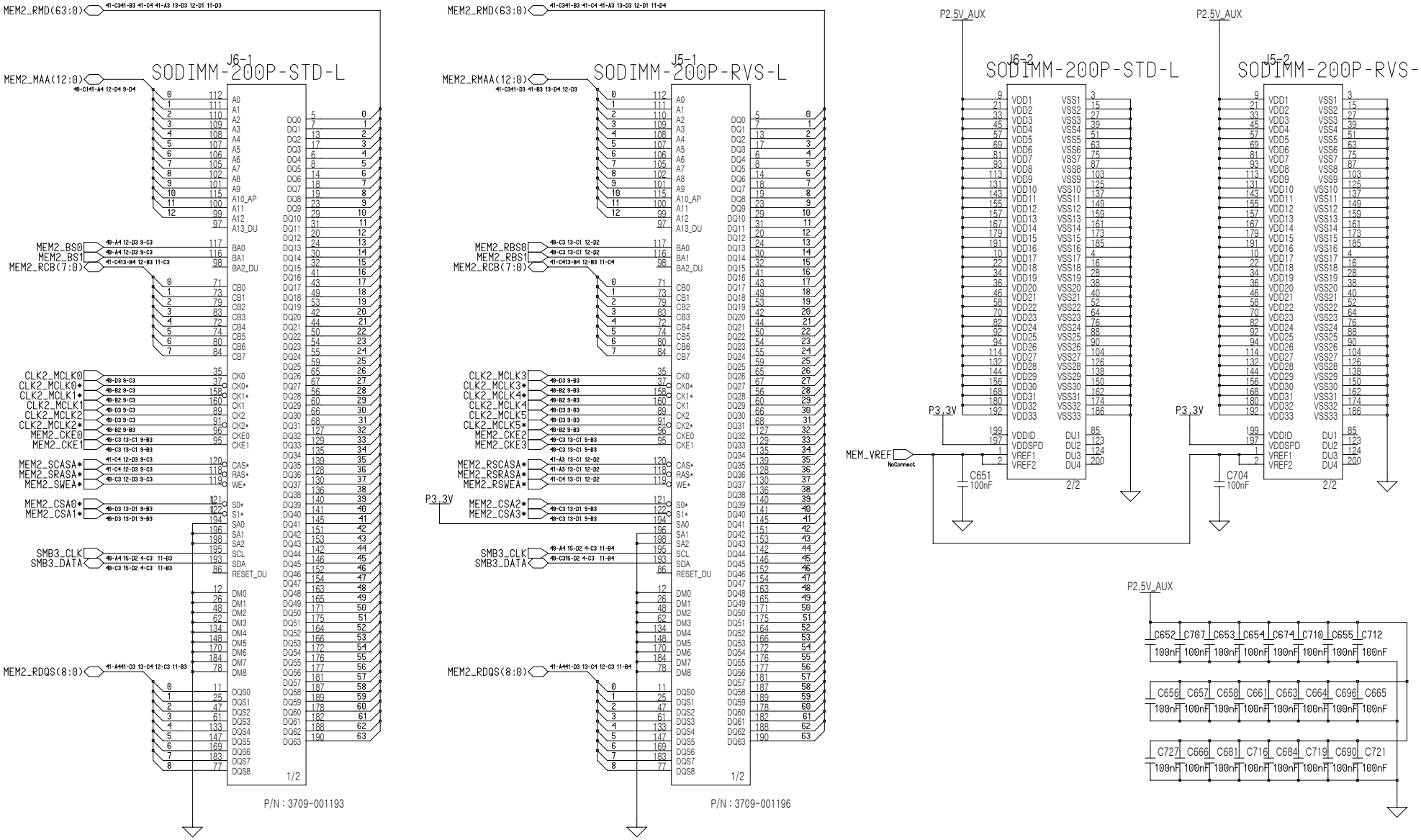

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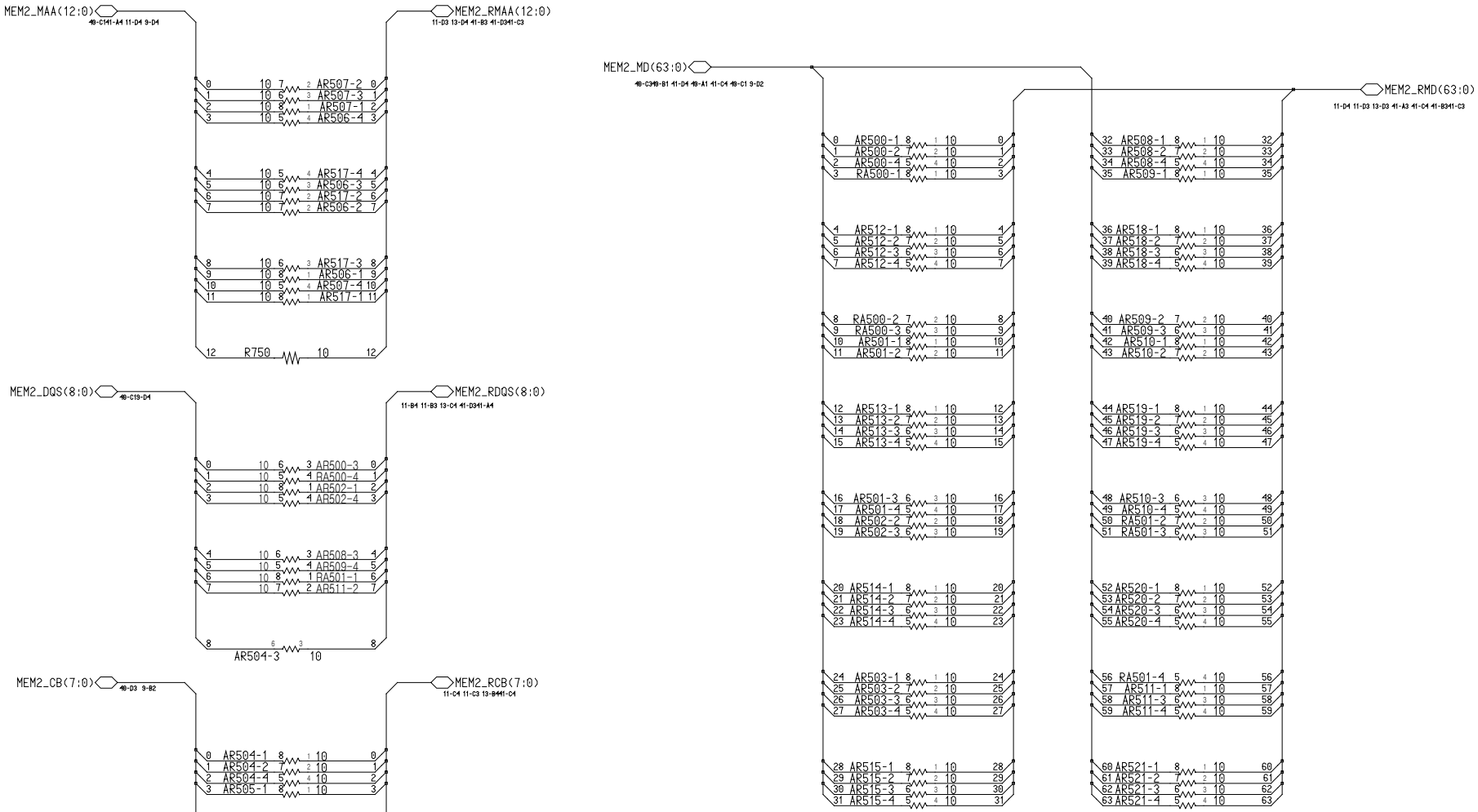
APPROVAL: H.S, KIM	REV: 1.0	MCH (3/3)	PART NO.: BA41-00392A
MODULE CODE:	LAST EDIT: March, 30, 2004 10:21:22 AM	PAGE 11 OF 41	



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APPROVAL: H.S, KIM	REV: 1.0	DDR S-TERMINATION	PART NO.: BA41-00392A
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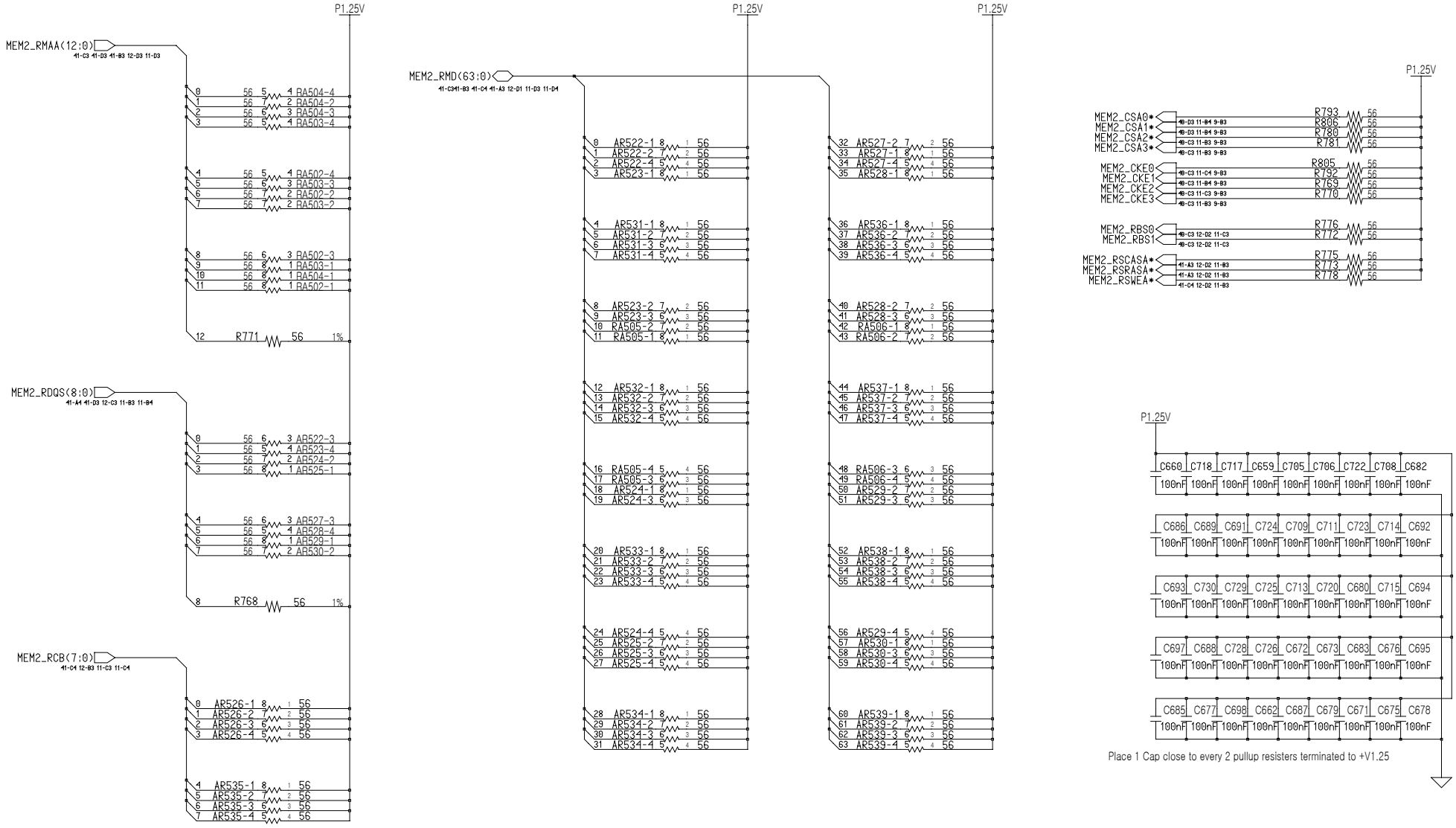

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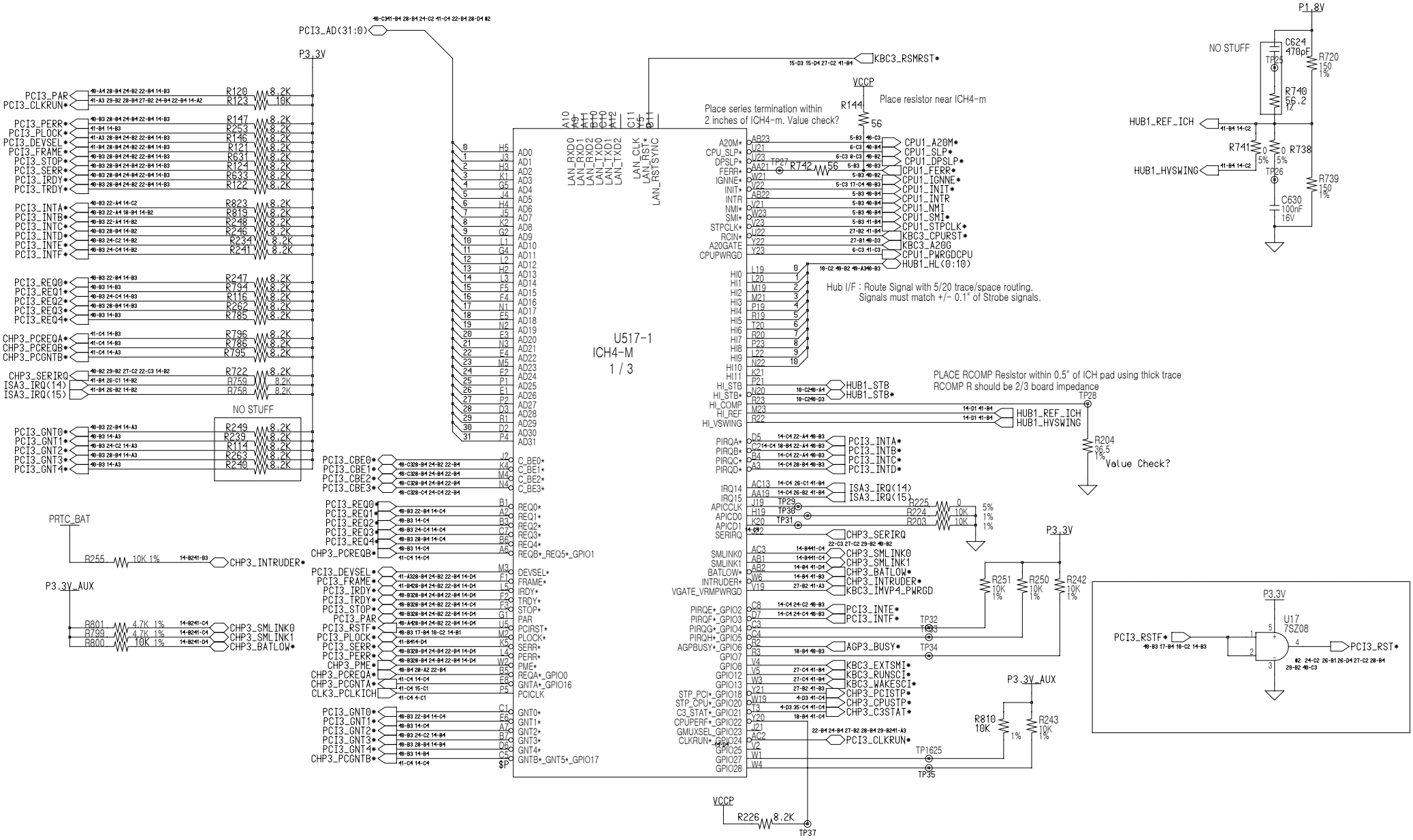

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APPROVAL: H.S, KIM	REV: 1.0	ICH4-M (1/3)	PART NO.: BA41-00392A
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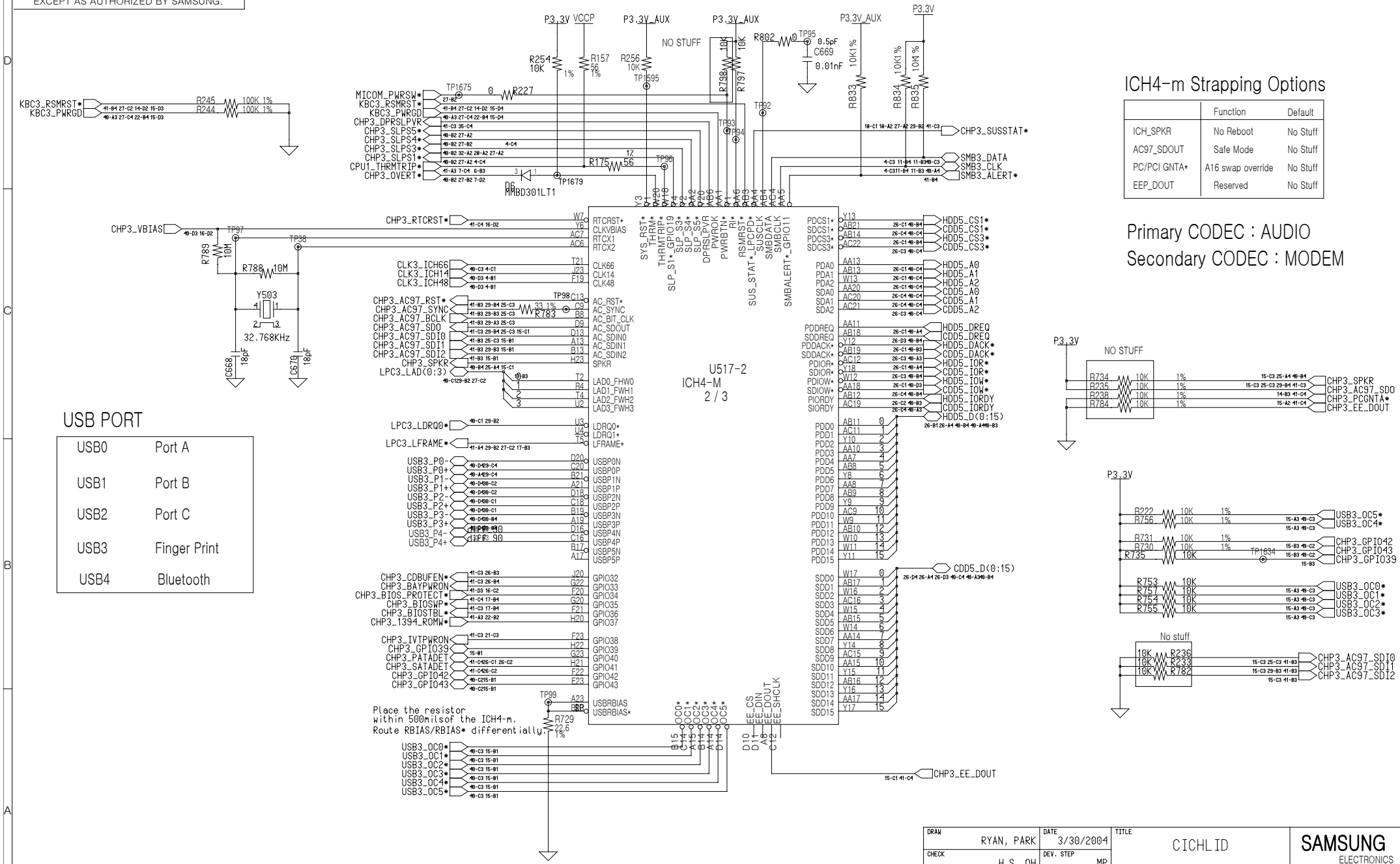


USB PORT

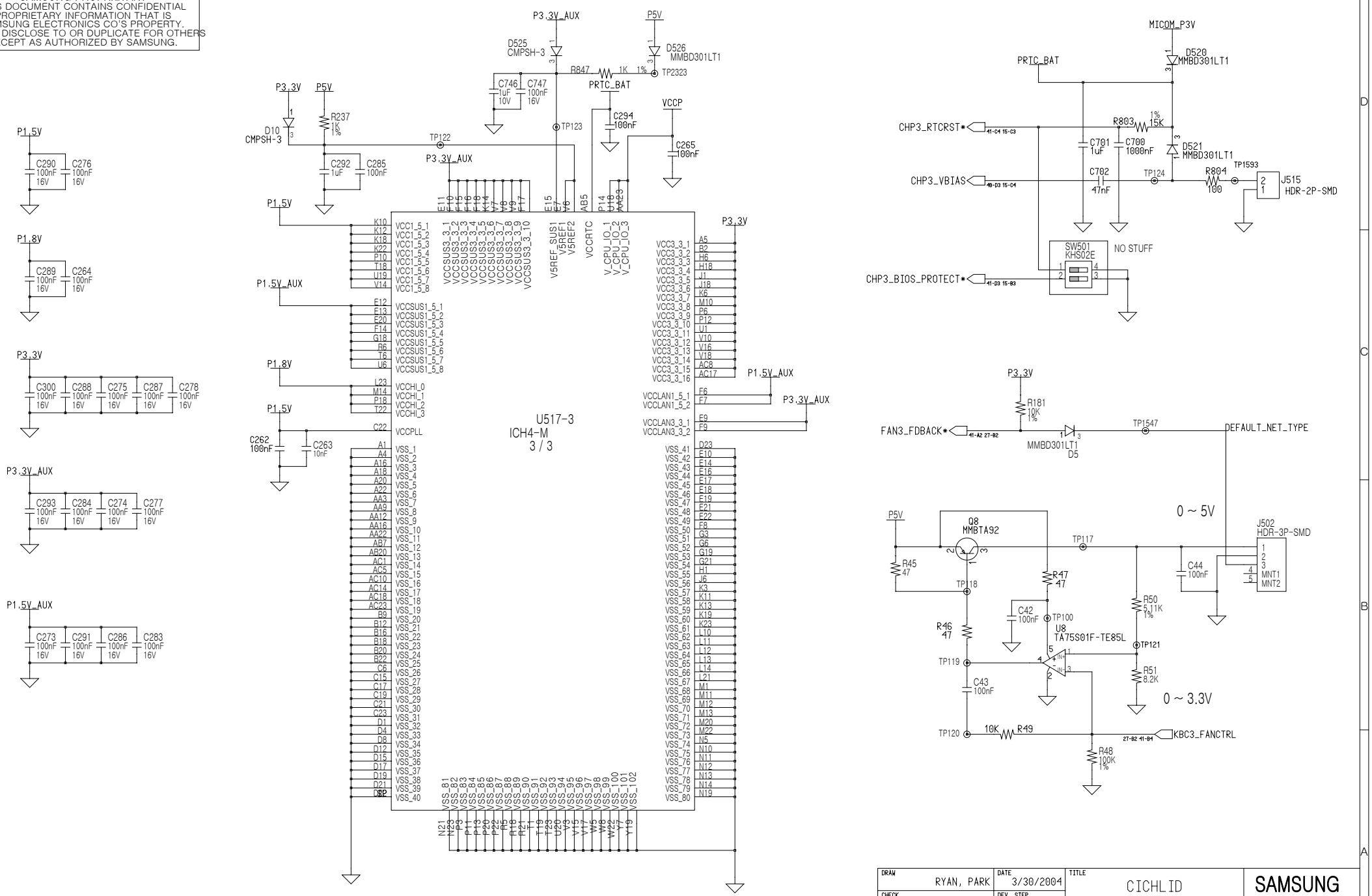
USB0	Port A
USB1	Port B
USB2	Port C
USB3	Finger Print
USB4	Bluetooth

ICH4-m Strapping Options

	Function	Default
ICH_SPKR	No Reboot	No Stuff
AC97_SDOUT	Safe Mode	No Stuff
PC/PCI GNTA*	A16 swap override	No Stuff
EEP_DOUT	Reserved	No Stuff

Primary CODEC : AUDIO
Secondary CODEC : MODEM

DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	ICH4-M (2/3)	PART NO.: BA41-00392A
MODULE CODE:	LAST EDIT: March, 30, 2004 10:25:28 AM	PAGE 15 OF 41	



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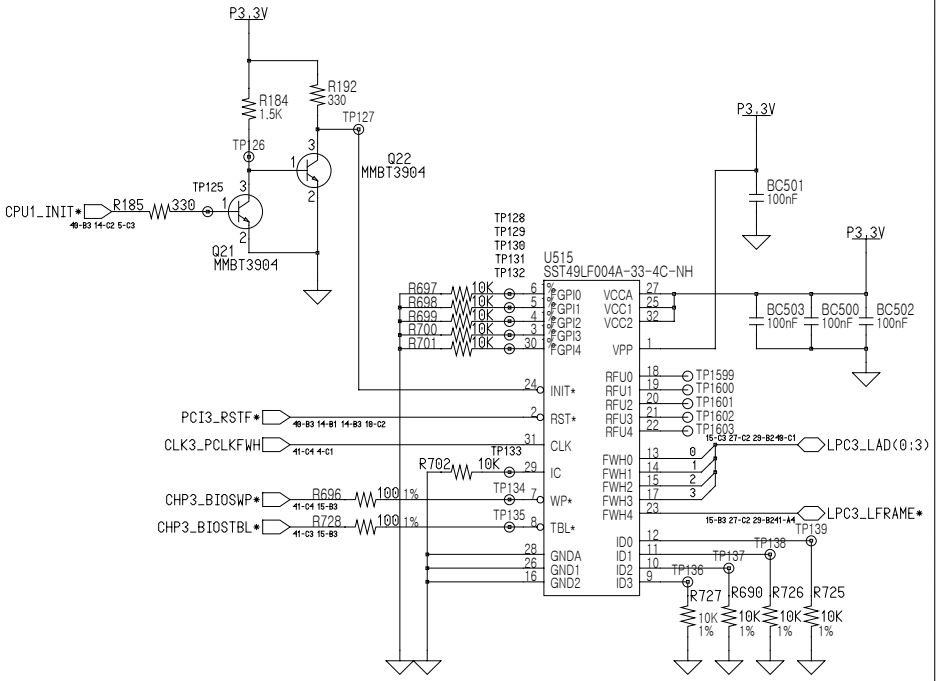
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	ICH4-M (3/3)	PART NO.: BA41-00392A
MODULE CODE:	LAST EDIT: March, 30, 2004 10:25:57 AM	PAGE 16 OF 41	



02	VERIFY REAL MODE
03	DISABLE NMI
04	GET CPU TYPE
06	INIT. SYSTEM H/W
08	INIT. CHIPSET REG.
09	SET IN POST FLAG
0A	INIT CPU.REG
0B	CPU CACHE ON
0C	INIT.CACHE TO POST
0E	INIT. I/O VALUE
0F	ENABLE THE L-BUS IDE
10	INIT. POWER MANAGER
11	LOAD ALTERNATE REG.
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE
14	INIT. KEYBOARD CONTROLLER
16	CHECK CHECKSUM
18	8254 TIMER INIT.
1A	8237 DMA CONTROLLER INIT.
1C	RESET INTERRUP CONTROLLER
20	TEST DRAM REFRESH
22	TEST 8742 KEYBOARD CONTROLLER
24	SET ES SEGMENT REG. TO 4GB
26	ENABLE A20
28	AUTO SIZING DRAM
32	COMPUTE THE CPU SPEED
34	TESET CMOS RAM
38	SHADOW SYSTEM BIOS ROM
3A	AUTO SIZING CACHE
3C	CONFIGURE ADVANCED CHIPSET REG.
3D	LOAD ALTER REG. WITH CMOS VALUE
42	INIT. INTERRUPT VECTOR
44	INIT. BIOS INTERRUPT
46	CHECK ROM COPYRIGHT NOTICE
47	INIT. I20 SUPPORT IF INSTALLED
48	CHECK VIDEO CONFIGURE AGAINST CMOS
49	INIT. PCI BUS AND DEVICE
4A	INIT. ALL VIDEO BIOS ROM
4C	SHADOW VIDEO BIOS ROM
50	DISPLAY CPU TYPE AND SPEED
52	TEST KEYBOARD
54	SET KEYCLICK IF ENABLED
56	ENABLE KEYBOARD
58	TEST FOR UNEXPECTED INTERRUPTS
5A	DISPLAY " PRESS ..... SETUP"
5C	TEST RAM GETWEEN 512K AND 640K
60	TEST EXTENDED MEMORY
62	TEST EXTENDED MEMORY ADDRESS LINE
64	JUMP TO USER PATCH 1
66	CONFIGURE ADVANCE CACHE REG.
6A	DISPLAY EXTERNAL CACHE SIZE
6C	DISPLAY SHADOW MESSAGE
6E	DISPLAY NON-DISPOSABLE SEGMENT
70	DISPLAY ERROR MESSAGE
72	CHECK FOR CONFIGURATION ERROR
74	TEST REAL-TIME CLOCK
76	CHECK FOR KEYBOARD EERROR
7C	SETUP HARDWARE INTERRUPT VECTOR
7E	TEST COPROCESSER IF PRESENT
80	DISABLE ON-BOARD I/O PORT
82	DETECT AND INSTALL EXT.RS232C
84	DETECT AND INSTALL EXT.PARALLEL
86	RE-INIT. ON-BOARD I/O PORT
88	INIT. BIOS DATA ROM
8A	INIT.EXTENDED BIOS DATA AREA
8C	INIT. FDD CONTROLLER
9A	SHADOW OPTION ROMS
9C	SETUP POWER MANAGEMENT
9E	ENABLE H/W INTERRUPT
A0	SET TIME OF DAY
A4	INIT. TYPEMATIC RATE
A8	ERASE F2 PROMPT
AA	SCAN FOR F2 KEY STROKE
AC	ENTER SETUP
AE	CLEAR IN POST FLAG
B0	CHECK FOR ERRORS
B2	POST DONE-PREPARE TO BOOT O/S
B4	ONE BEEP
B6	CHECK PASSWORD (OPTION)
B7	ACPI INIT
BA	DMI INIT
BE	CLEAR SCREEN
C0	TRY BOOT WITH INT19
D0	INTERRUPT HANDLER ERROR
D2	UNKNOWN INTERRUPT ERROR
D4	PENDING INTERRUPT ERROR
D6	SHUTDOWN 5
D8	SHUTDOWN ERROR
DA	EXTENDED BLOCK MOVE
DC	SHUTDOWN 10
89	ENABLE NMI
90	INIT. HDD CONTROLLER
91	INIT. LOCAL BUS HDD CONTROLLER
92	JUMP TO USER PATCH 2
94	DISABLE A20 ADDRESS LINE
96	CLEAR HUGE ES SEGMENT REG.
98	SEARCH FOR OPTION ROMS

DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	FIRMWARE HUB	PART NO.: BA41-00392A
MODULE CODE	LAST EDIT: March, 30, 2004 10:26:13 AM	PAGE 17 OF 41	

	XGA	SXGA+
VGA3_VIPHAD1	1	0
VGA3_VIPHAD0	1	1

U505-1
NV17-MAP
1 / 3

MAP34-64M
GeforceFX Go5200 64M

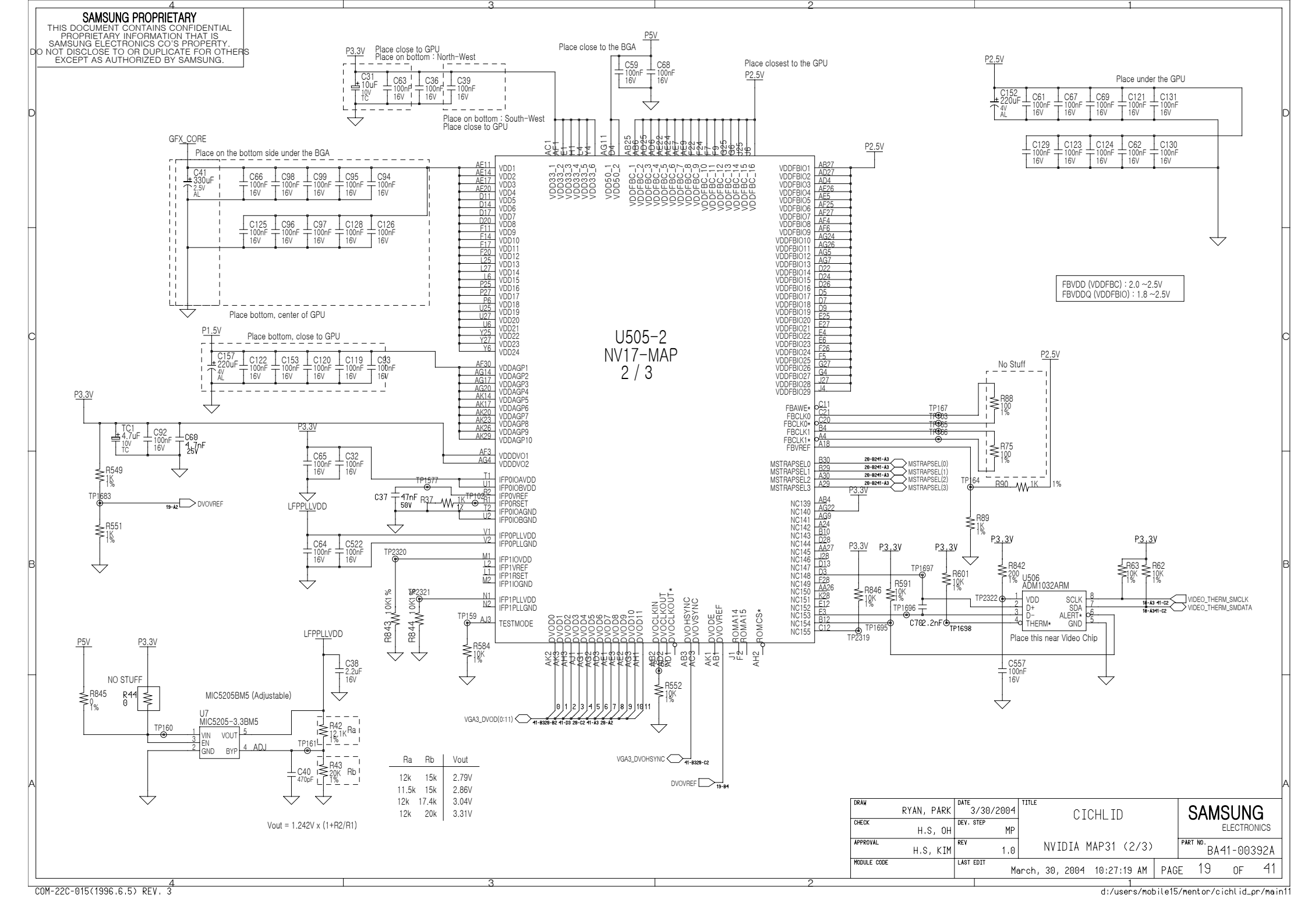
Option
USER(1)
USER(0)
Panel ID Switch
Test Option

GPIO(9)		RESERVED
GPIO(8)		THERMAL_DIODE_SUPPORT
GPIO(7)	-	Gfx Core Voltage Switching
GPIO(6)	0	Hardware suspend
GPIO(5)	-	Spread spectrum support
GPIO(4)	-	RESERVED
GPIO(3)	-	Panel power enable
GPIO(2)	-	Backlight enable
GPIO(1:0)	-	GPIO

DRAW	RYAN, PARK	DATE	3/30/2004
CHECK	H.S, OH	DEV. STEP	MP
APPROVAL	H.S, KIM	REV	1.0
MODULE CODE		LAST EDIT	March, 30, 2004 10:26:37 AM

TITLE: CICHLID
NVIDIA MAP31 (1/3)

SAMSUNG ELECTRONICS
PART NO. BA41-00392A
PAGE 18 OF 41

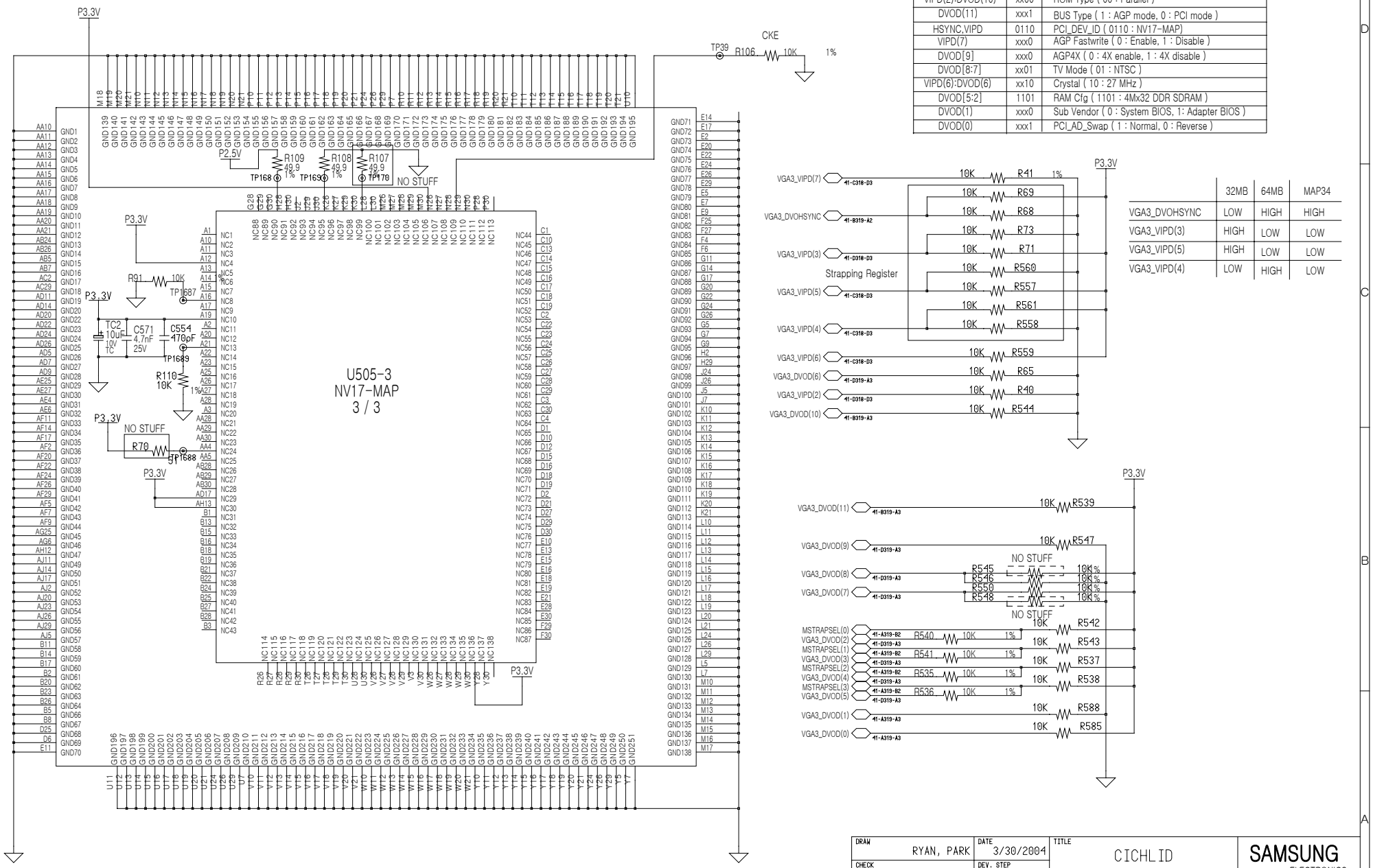


Ra	Rb	Vout
12k	15k	2.79V
11.5k	15k	2.86V
12k	17.4k	3.04V
12k	20k	3.31V

DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	NVIDIA MAP31 (2/3)	PART NO.: BA41-00392A
MODULE CODE	LAST EDIT: March, 30, 2004 10:27:19 AM	PAGE 19 OF 41	

Strapping Option

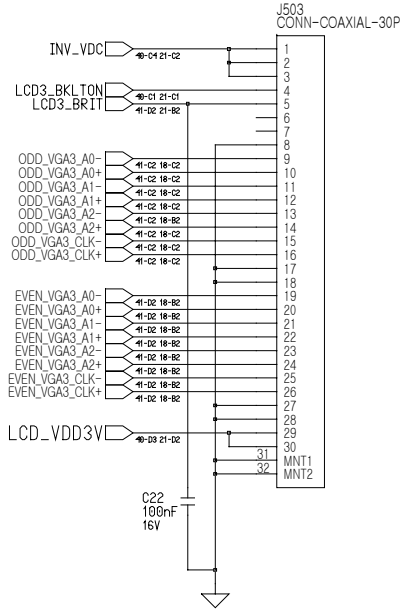
VIPD(2):DVOD(10)	xx00	ROM Type (00 : Parallel)
DVOD(11)	xxx1	BUS Type (1 : AGP mode, 0 : PCI mode)
HSYNC,VIPD	0110	PCI_DEV_ID (0110 : NV17-MAP)
VIPD(7)	xxx0	AGP Fastwrite (0 : Enable, 1 : Disable)
DVOD[9]	xxx0	AGP4X (0 : 4X enable, 1 : 4X disable)
DVOD[8:7]	xx01	TV Mode (01 : NTSC)
VIPD(6):DVOD(6)	xx10	Crystal (10 : 27 MHz)
DVOD[5:2]	1101	RAM Cfg (1101 : 4Mx32 DDR SDRAM)
DVOD(1)	xxx0	Sub Vendor (0 : System BIOS, 1: Adapter BIOS)
DVOD(0)	xxx1	PCI_AD_Swap (1 : Normal, 0 : Reverse)

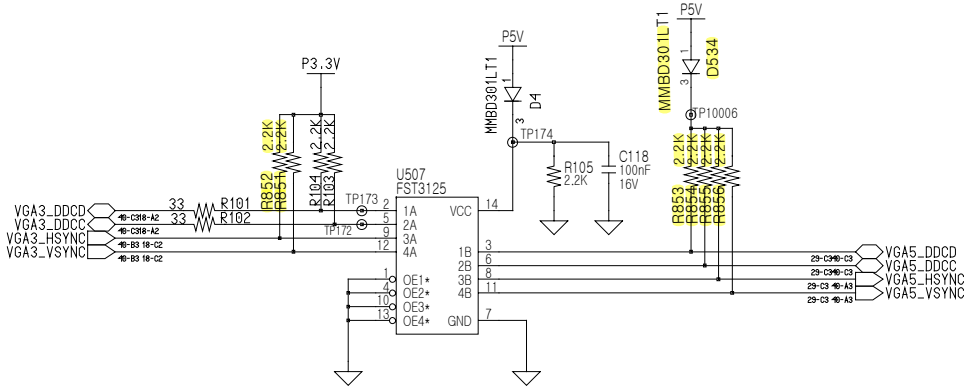


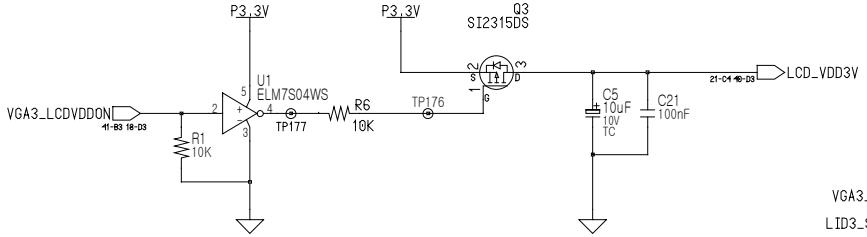
	32MB	64MB	MAP34
VGA3_DVOHSYNC	LOW	HIGH	HIGH
VGA3_VIPD(3)	HIGH	LOW	LOW
VGA3_VIPD(5)	HIGH	LOW	LOW
VGA3_VIPD(4)	LOW	HIGH	LOW

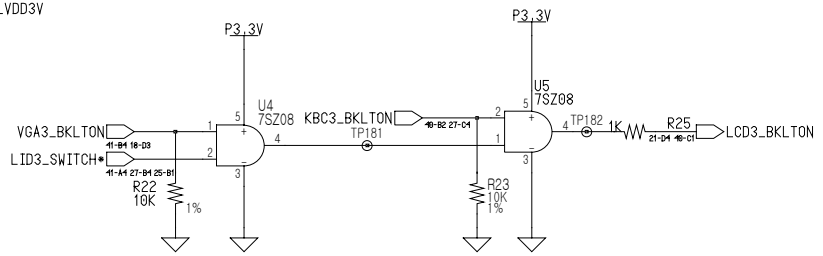
DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	NVIDIA MAP31 (3/3)	PART NO.: BA41-00392A
MODULE CODE	LAST EDIT: March, 30, 2004 10:27:42 AM	PAGE 20 OF 41	

LCD CONNECTOR

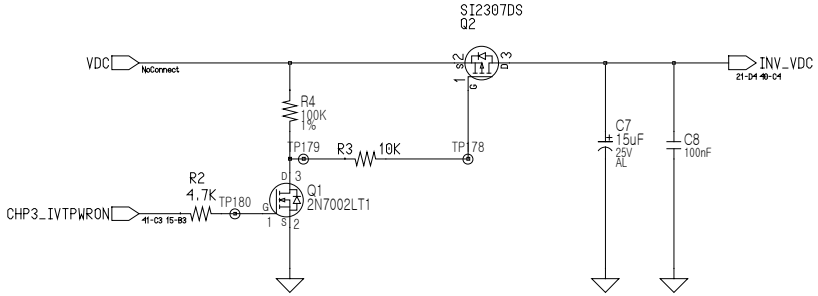


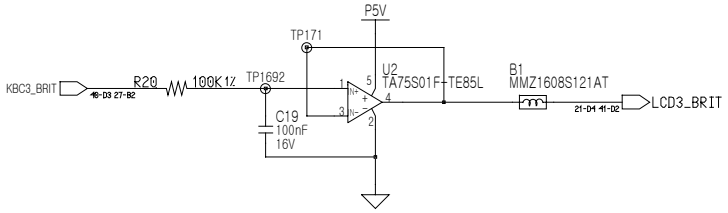




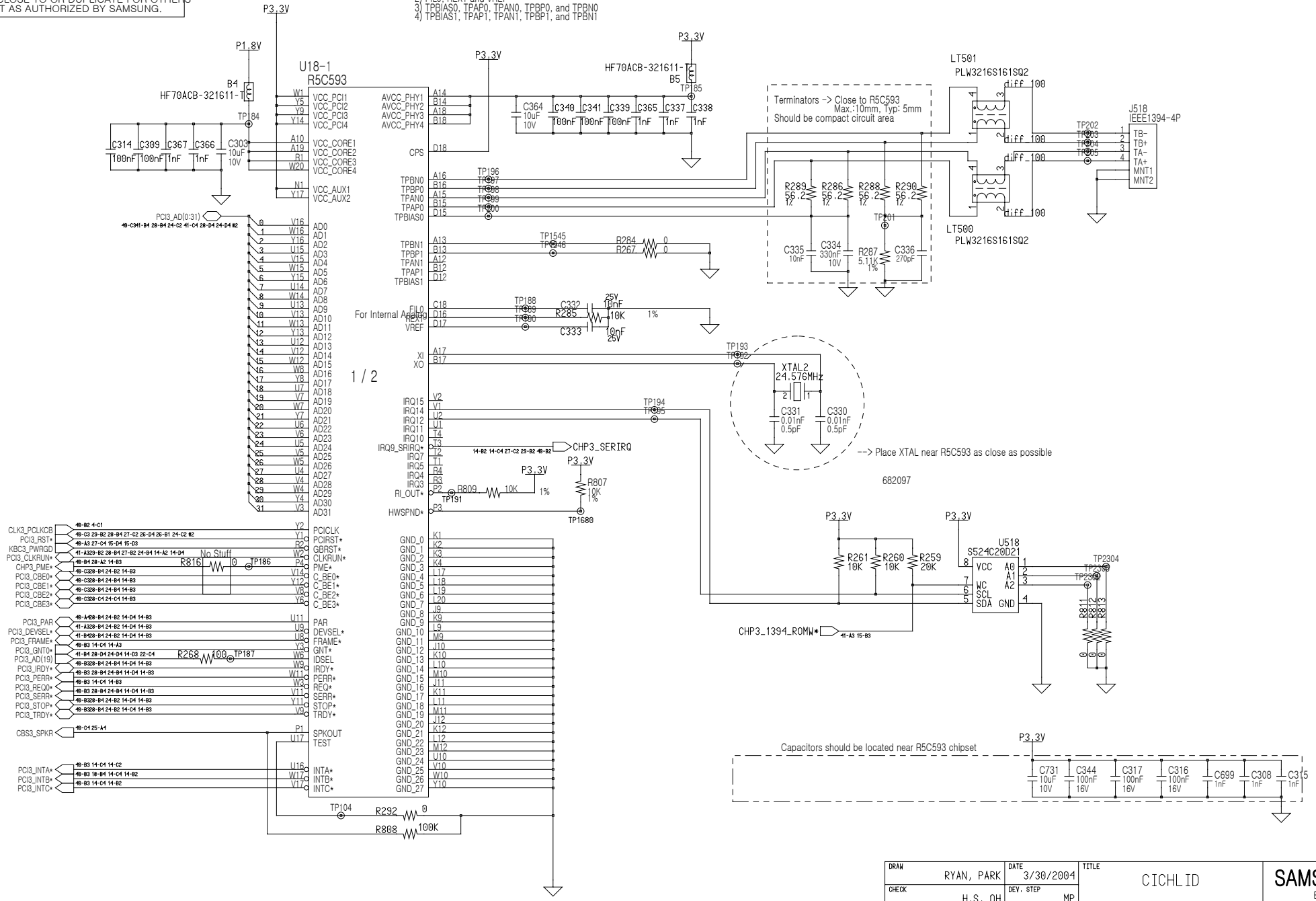


	XGA	SXGA+
VGA3_VIPHAD1	1	0
VGA3_VIPHAD0	1	1



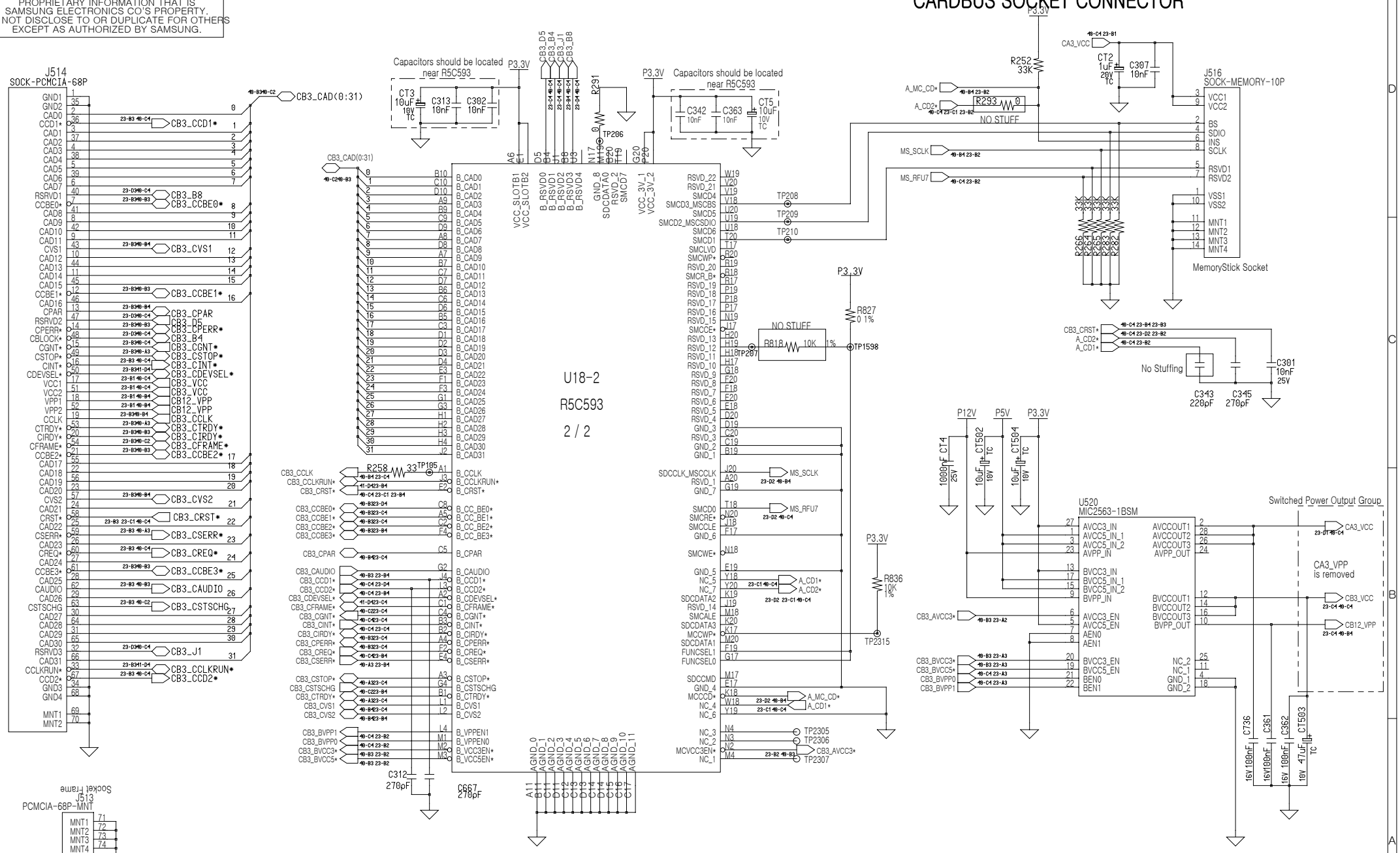


DRAW: KI. IM	DATE: 4/7/2003	TITLE: AQUILA W / MAIN / LCD_CONNECTOR	SAMSUNG ELECTRONICS
CHECK: KK.BIN	DEV. STEP: DV		
APPROVAL: DW.KIM	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE:	LAST EDIT: April 7, 2003 8:36:31 AM	PAGE 21 OF 42	



DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP	CARDBUS & 1394	
APPROVAL: H.S, KIM	REV: 1.0		PART NO.: BA41-00392A
MODULE CODE:	LAST EDIT: March, 30, 2004 10:29:12 AM	PAGE 22 OF 41	

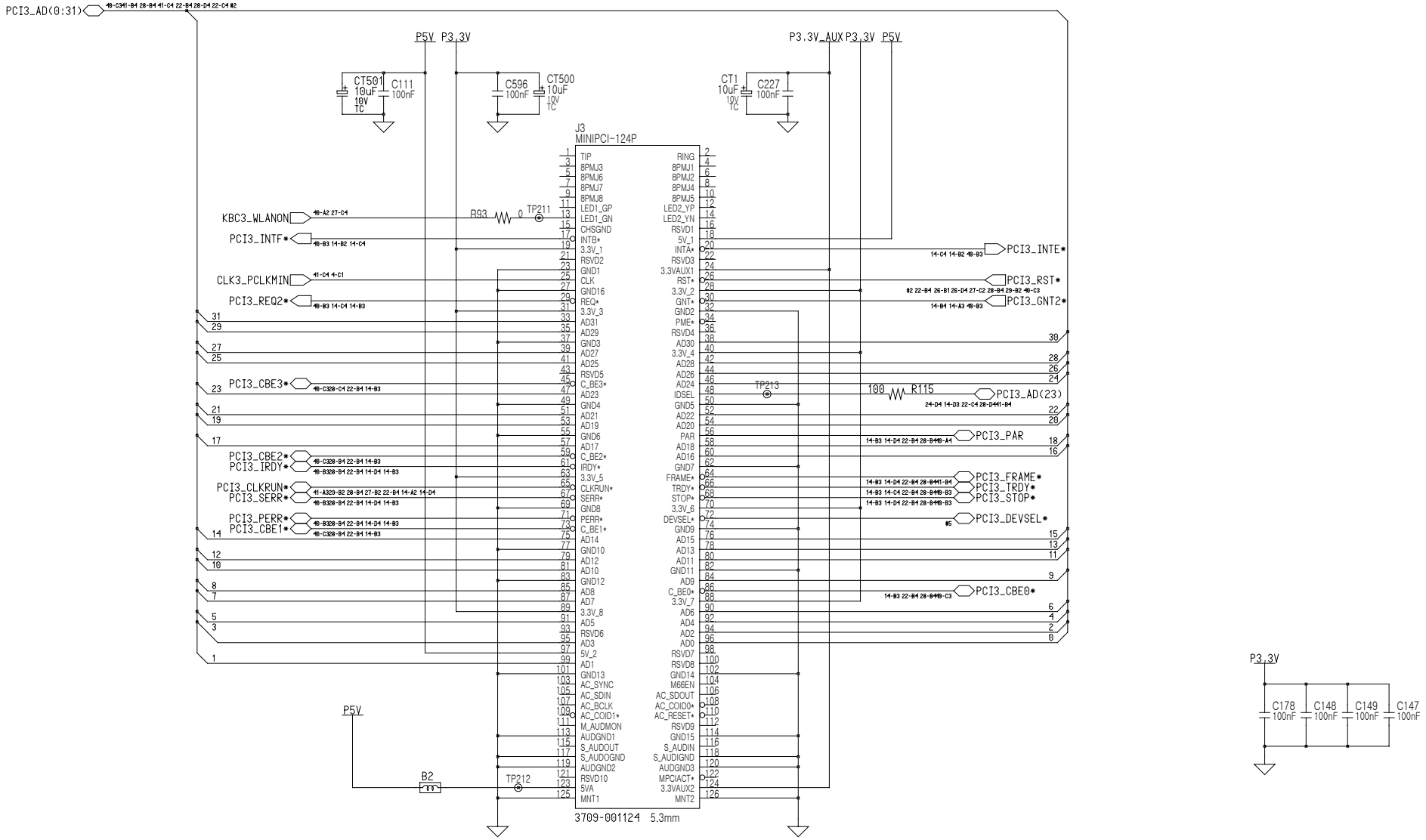
CARDBUS SOCKET CONNECTOR



* SHIELD GROUND *
Apply Shiled Grounding to Following Signals:
1) CB3_CCLK (A1) 2) A_MS_SCLK (J20)

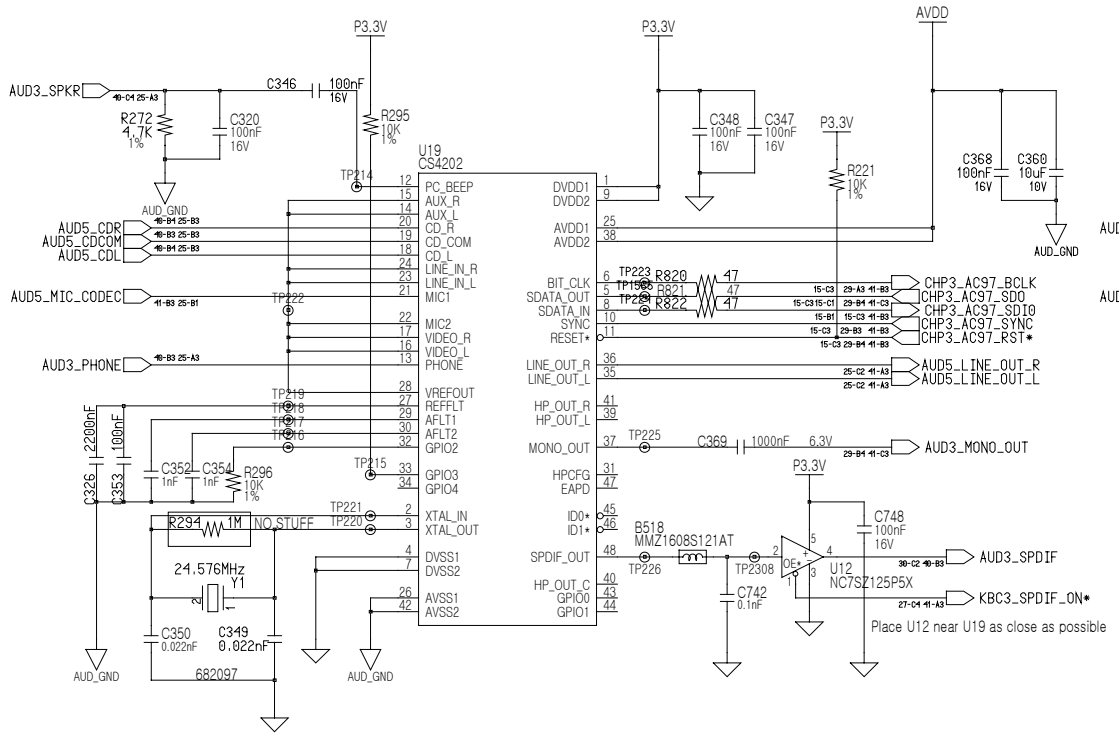
DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	CARDBUS SOCKET	PART NO.: BA41-00392A
MODULE CODE	LAST EDIT: March, 30, 2004 10:29:38 AM	PAGE 23 OF 41	

MINIPCI

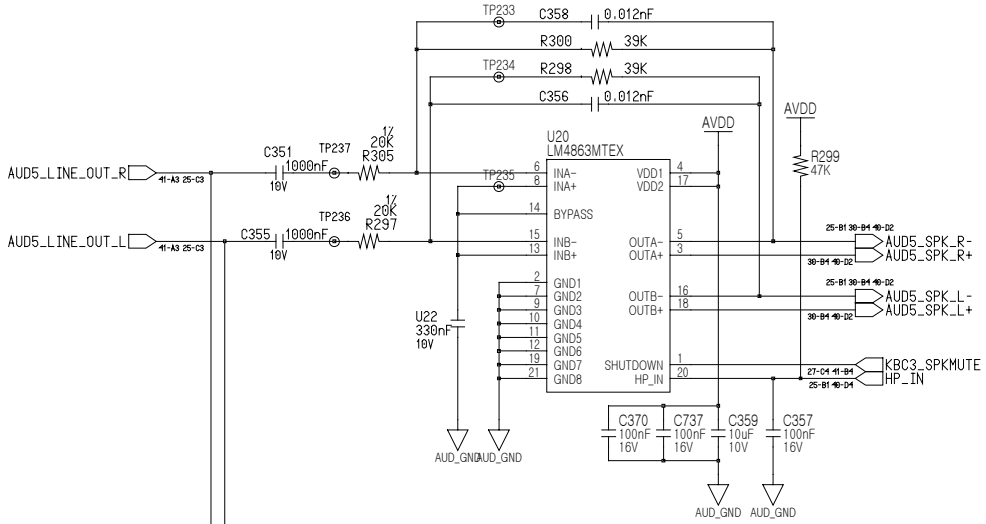


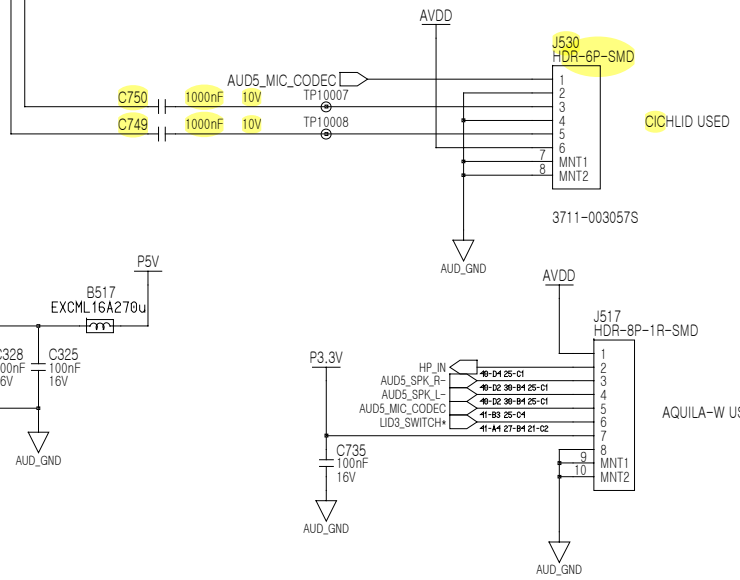
DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	MINI PCI	PART NO.: BA41-00392A
MODULE CODE	LAST EDIT: March, 30, 2004 10:29:54 AM	PAGE 24 OF 41	

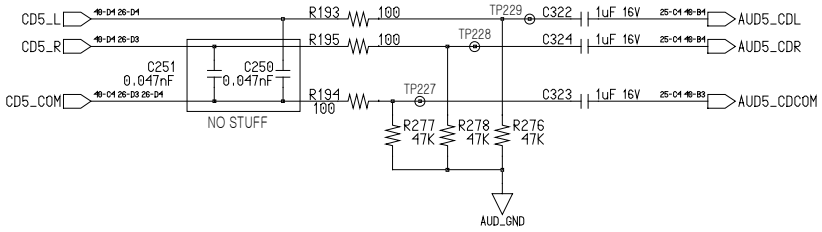
AC97 Audio Codec

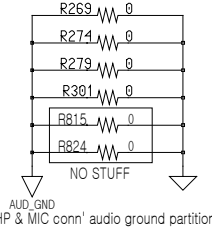


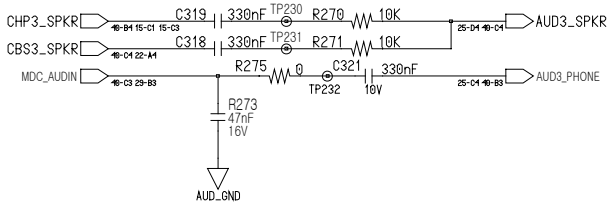
Audio AMP





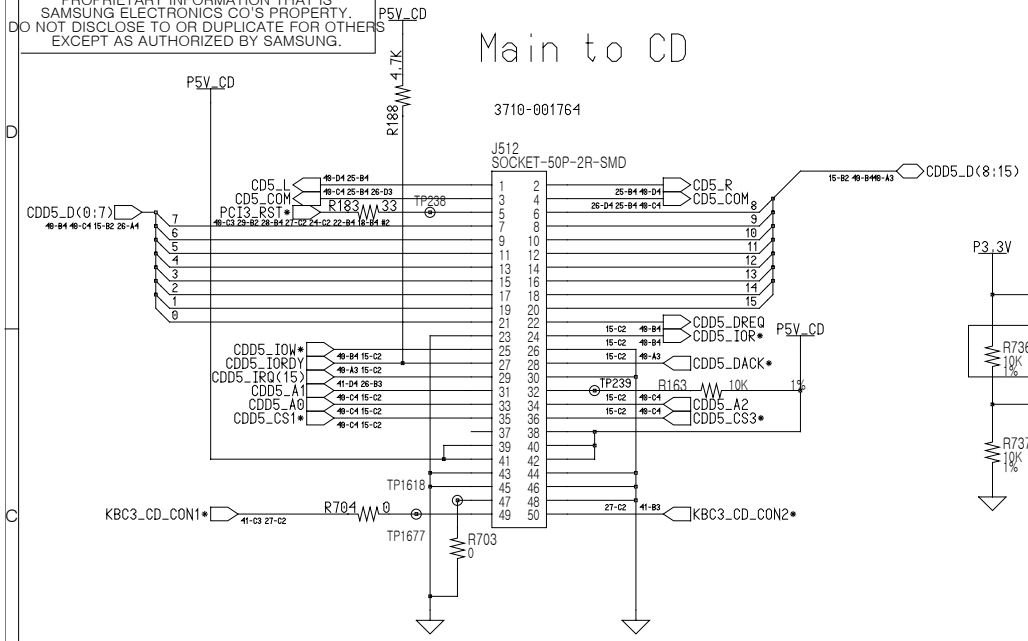


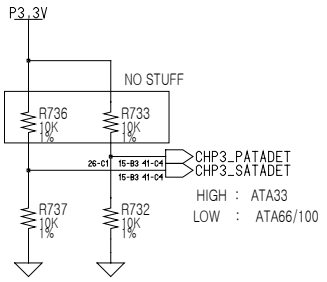


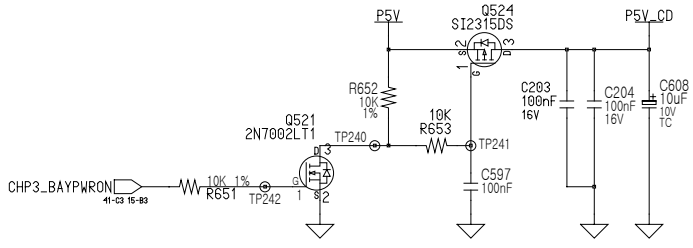


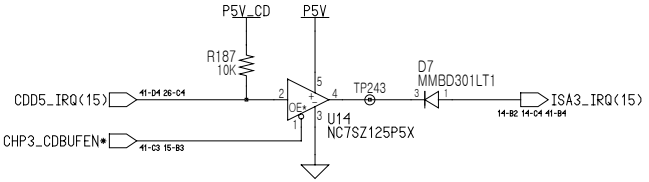
DRAW: KI. IM	DATE: 4/7/2003	TITLE: AQUILA W MAIN AUDIO CODEC & AMP	SAMSUNG ELECTRONICS
CHECK: KK.BIN	DEV. STEP: DV		
APPROVAL: DW.KIM	REV: 1.0		PART NO.: BA41-#####A
MODULE CODE	LAST EDIT: April 7, 2003 8:36:31 AM	PAGE 25 OF 42	

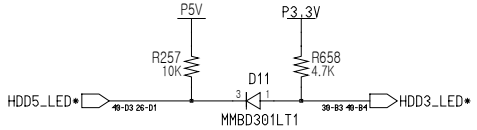
Main to CD

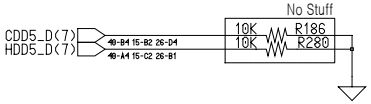




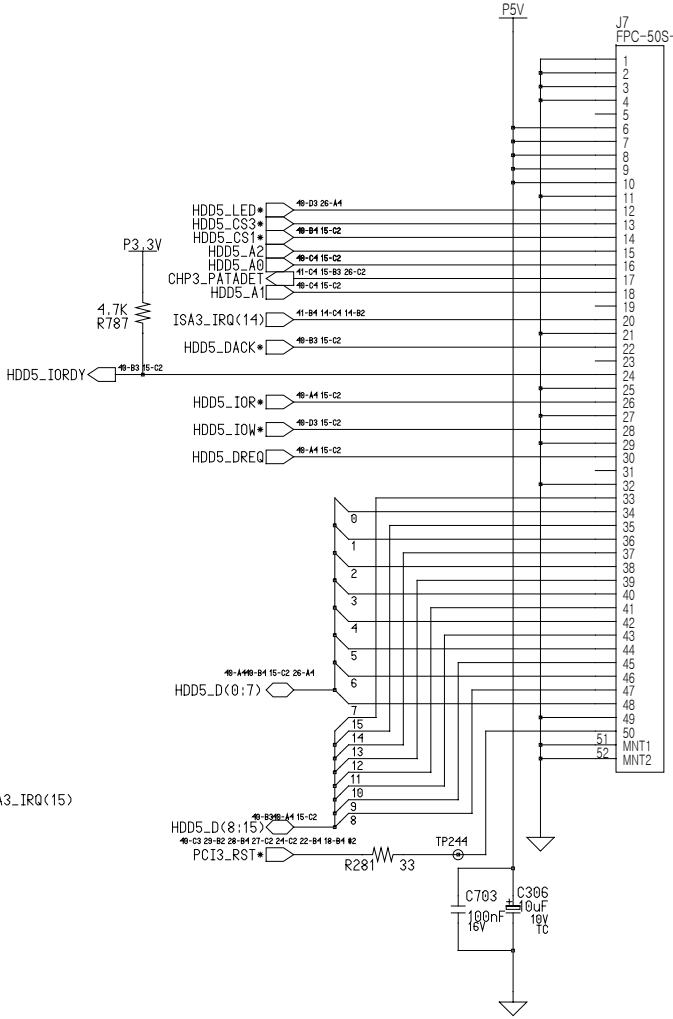




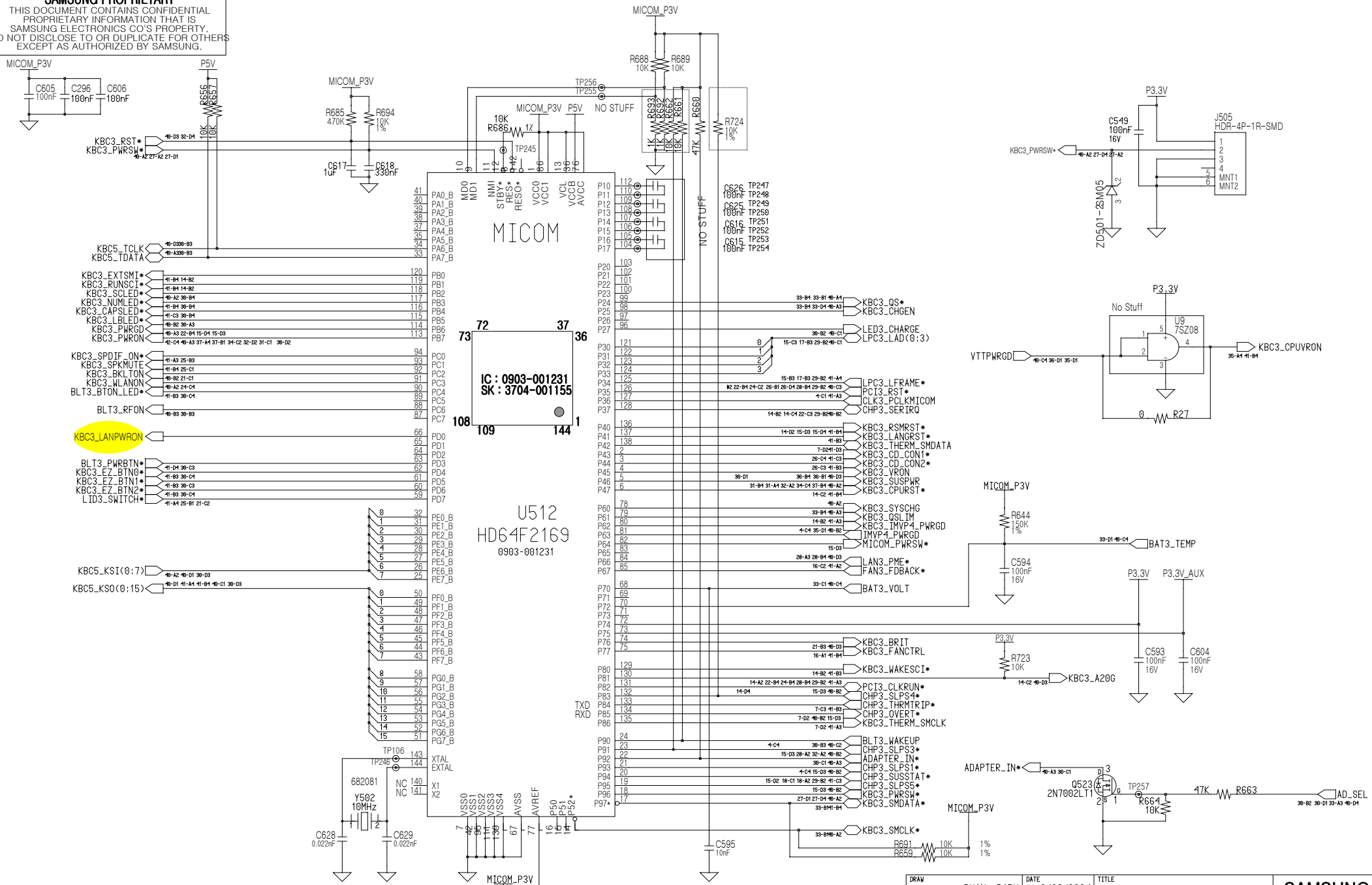




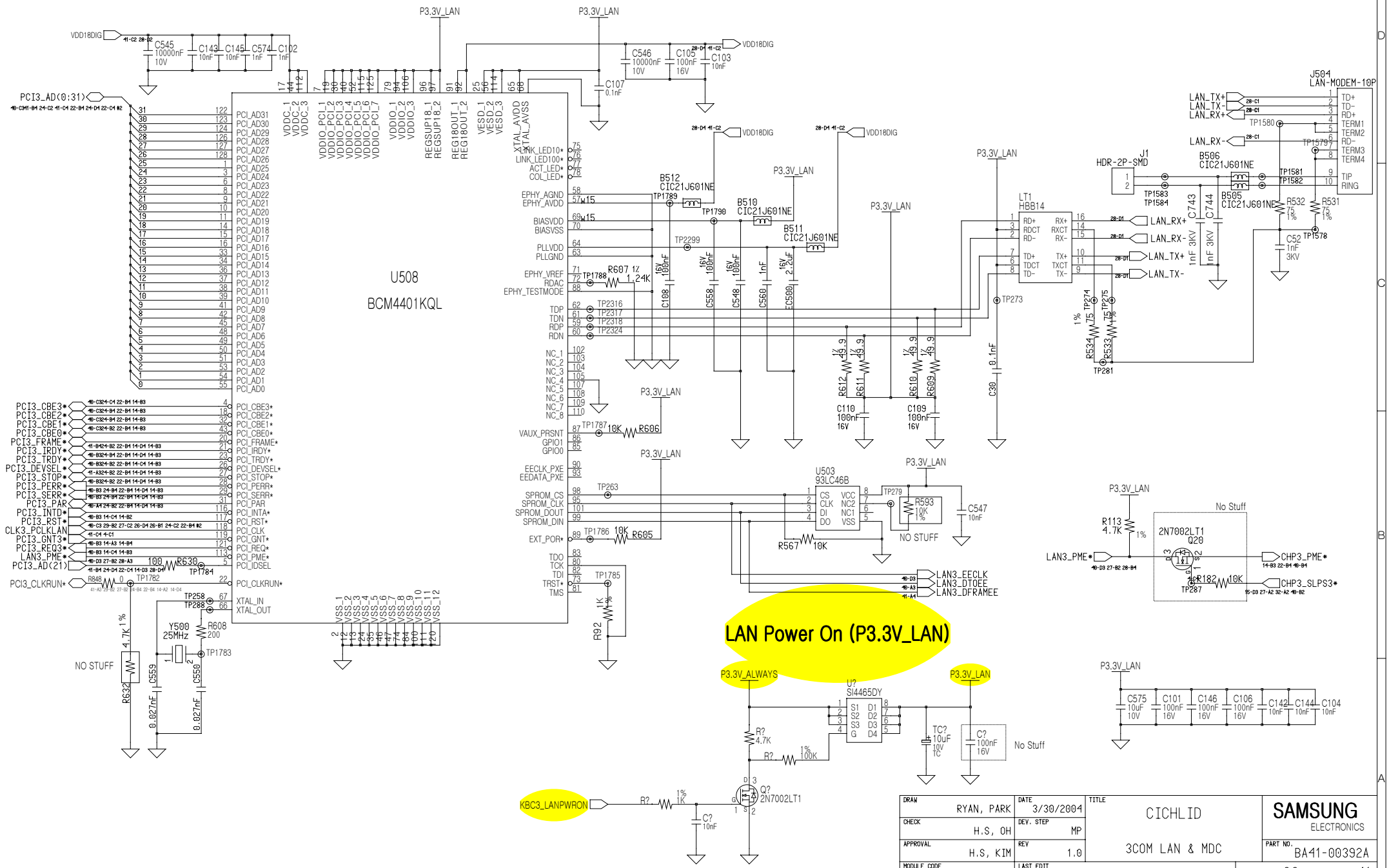
Main to HDD



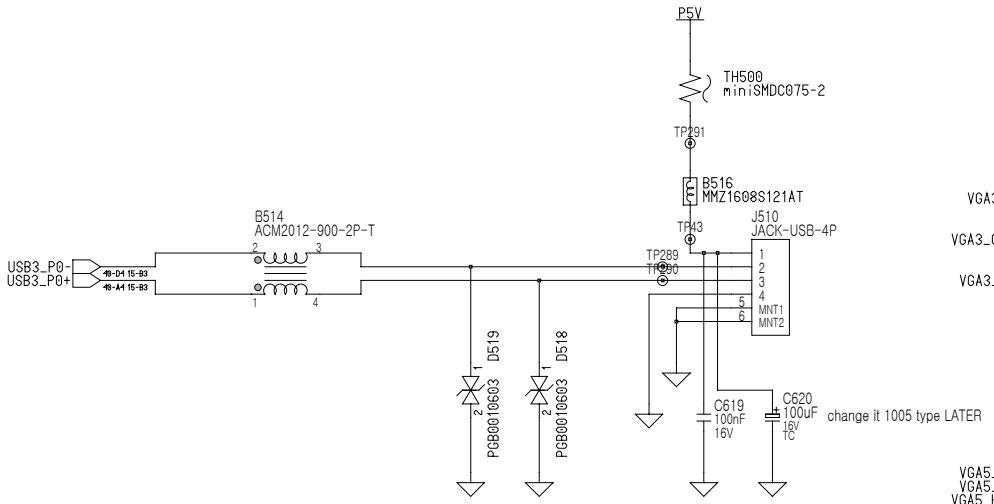
DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	BAY CONNECTOR	PART NO.: BA41-00392A
MODULE CODE:	LAST EDIT: March, 30, 2004 10:53:09 AM	PAGE 26 OF 41	

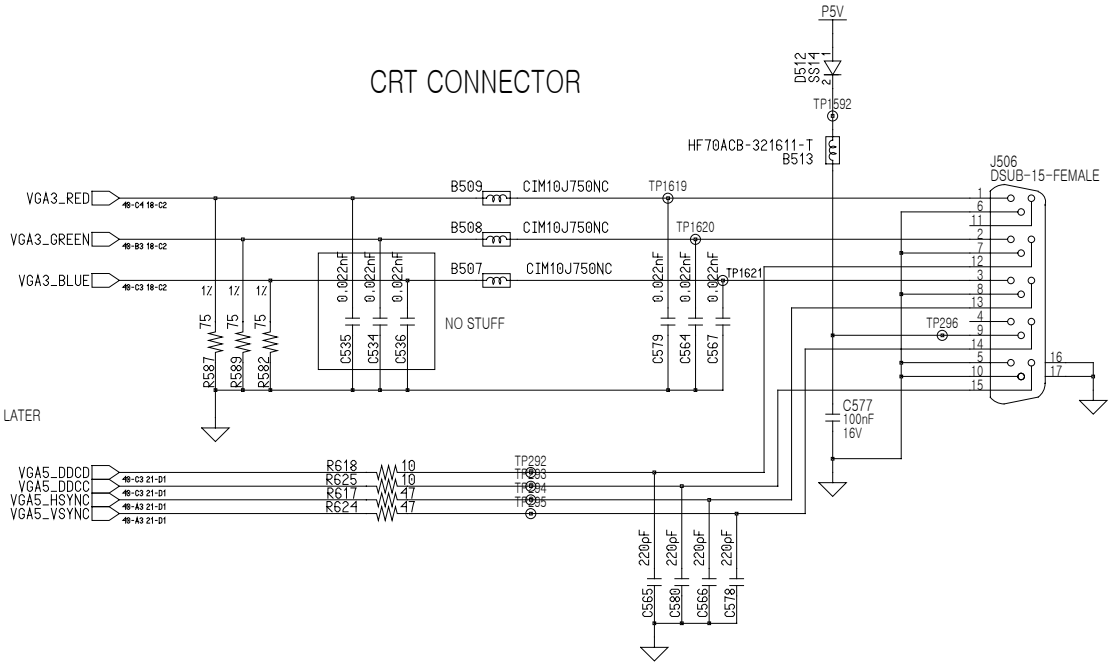


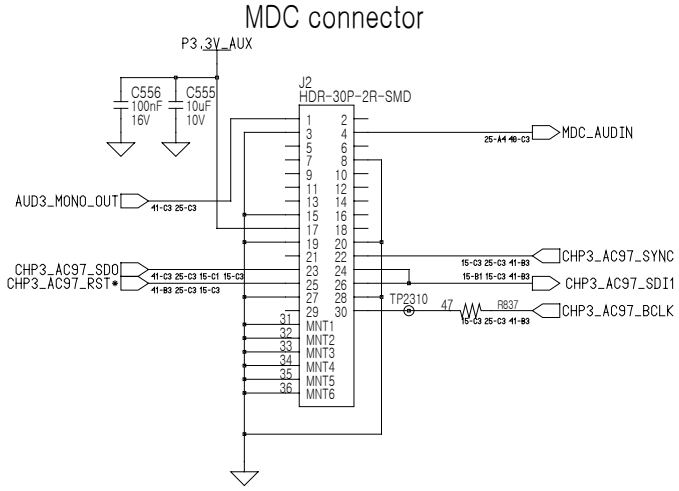
DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP	MICOM	
APPROVAL: H.S, KIM	REV: 1.0		PART NO.: BA41-00392A
MODULE CODE	LAST EDIT: March, 30, 2004 10:53:25 AM	PAGE 27 OF 41	

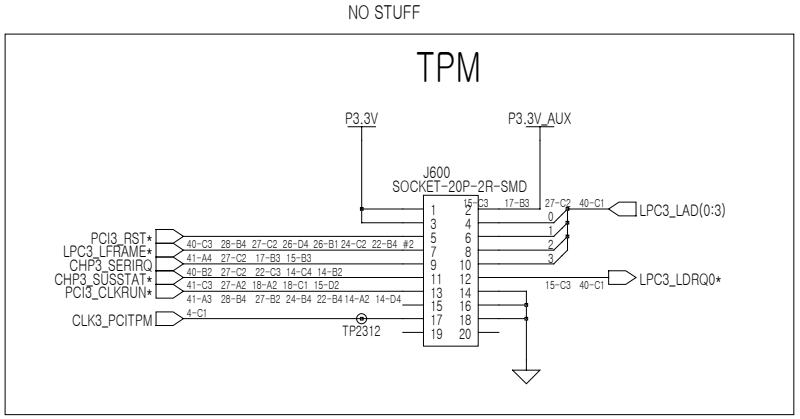


DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	3COM LAN & MDC	PART NO.: BA41-00392A
MODULE CODE:	LAST EDIT: March, 30, 2004 10:53:52 AM	PAGE 28 OF 41	





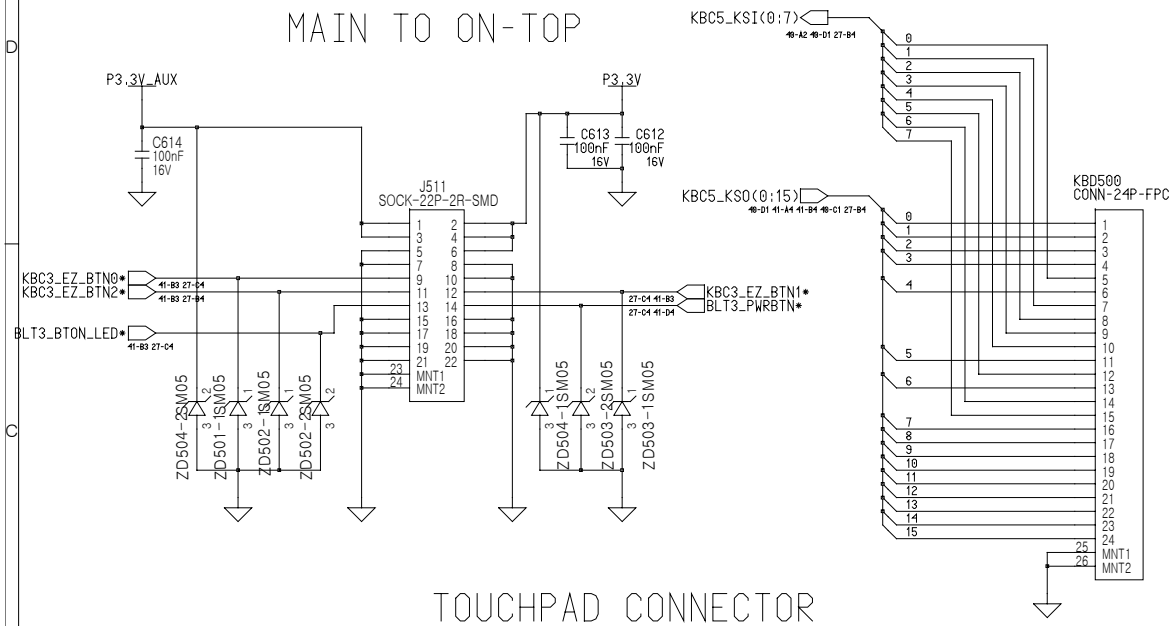




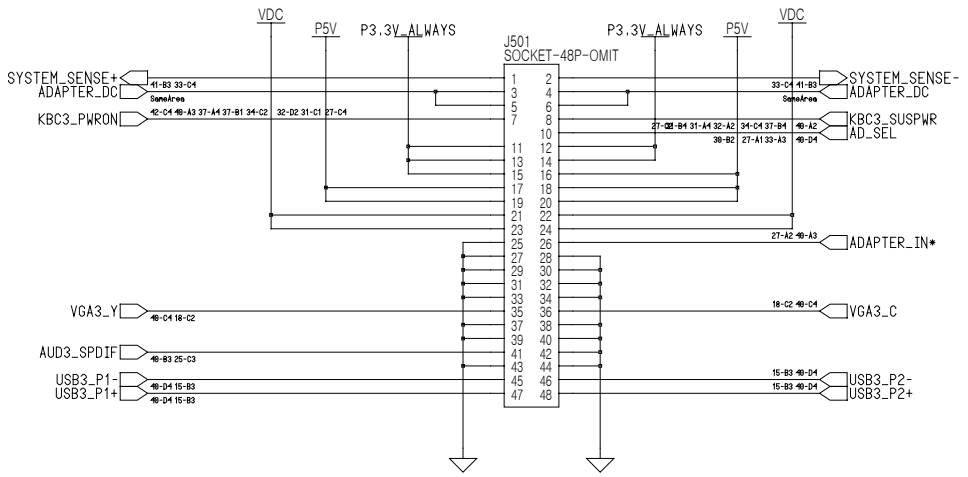
DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	USB CONNECTOR	PART NO.: BA41-00392A
MODULE CODE:	LAST EDIT: March, 30, 2004 10:54:11 AM	PAGE 29 OF 41	

KEYBOARD

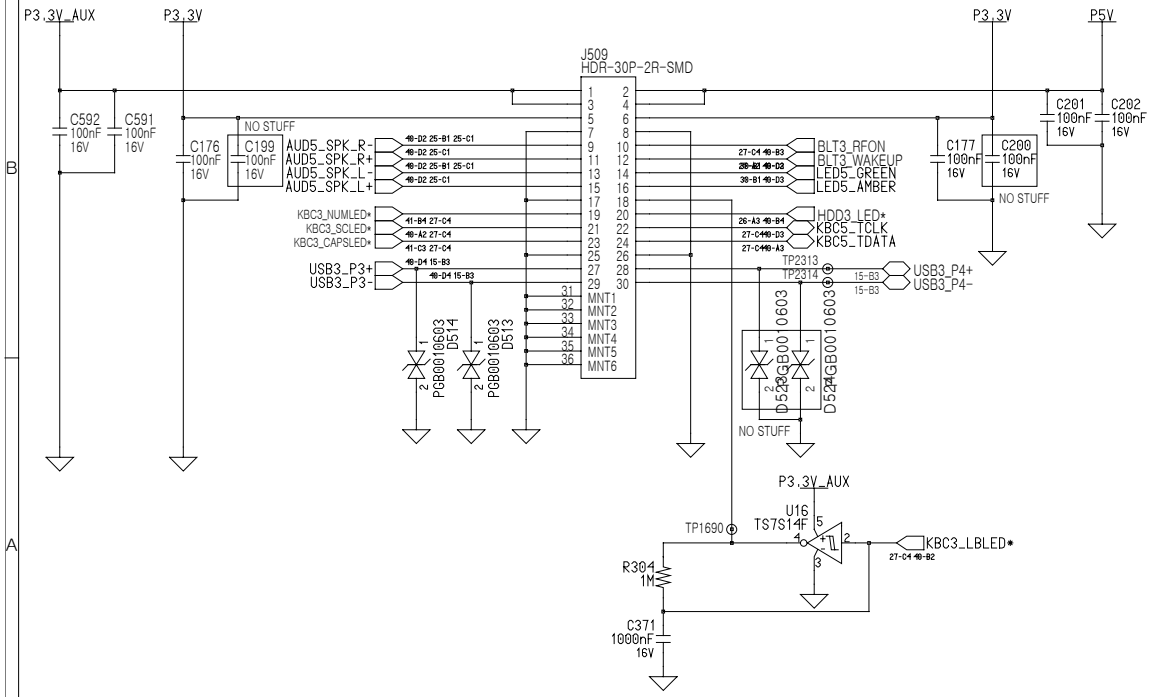
MAIN TO ON-TOP



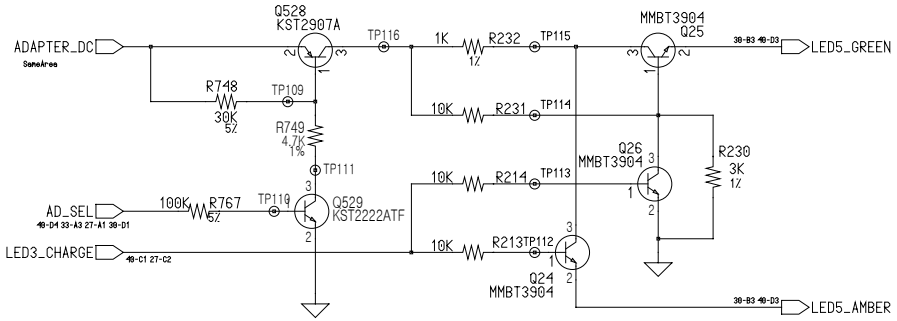
Main to DC/DC BOARD



TOUCHPAD CONNECTOR

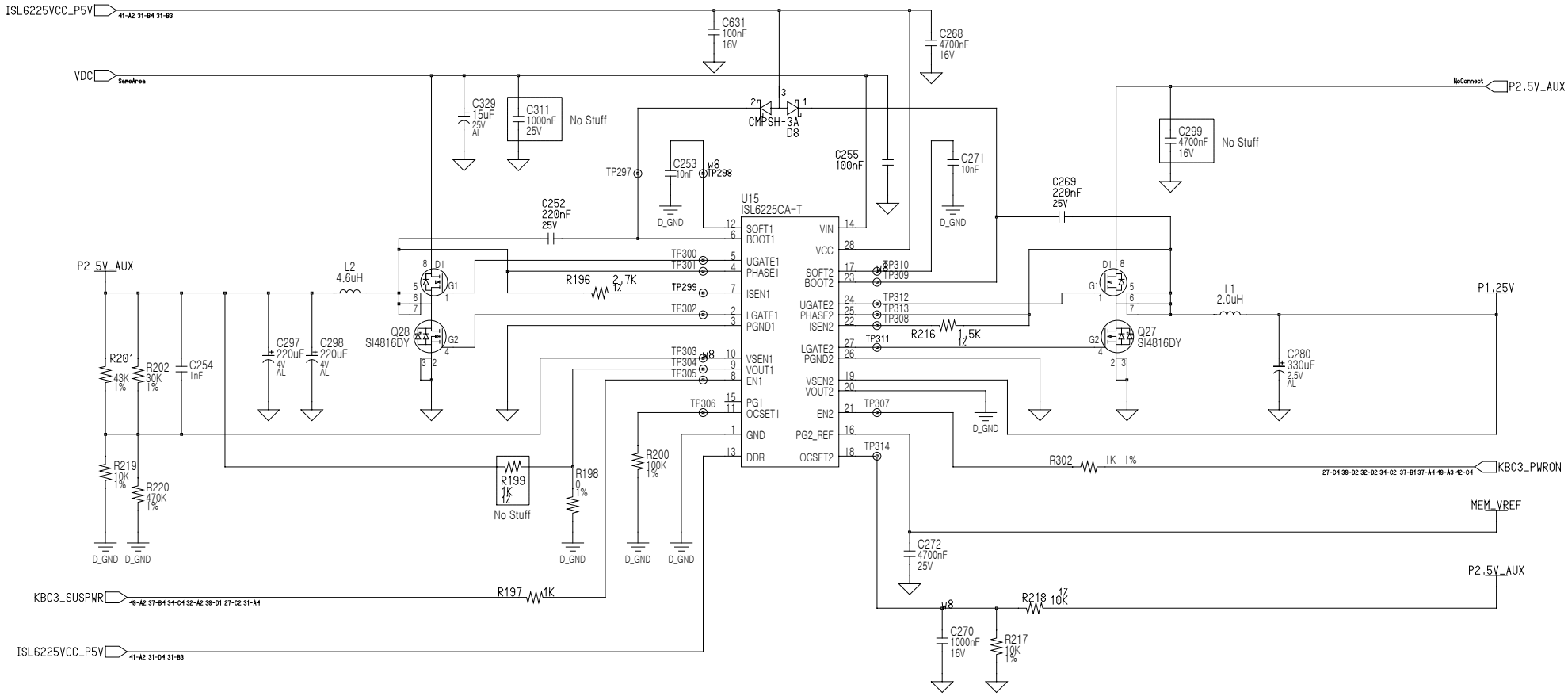


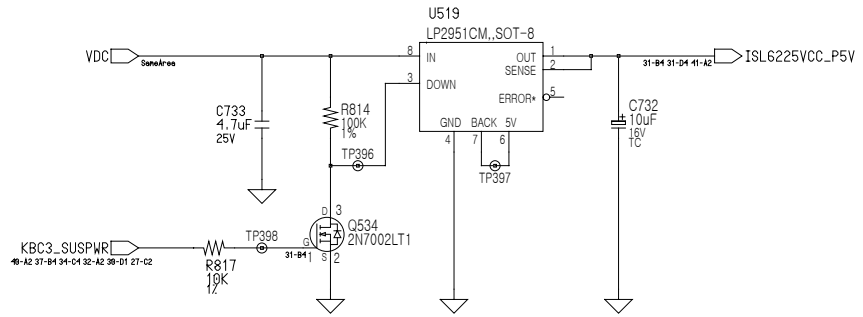
ADAPTERIN/CHARGING LED

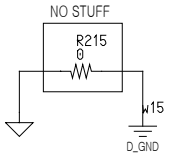


DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	B'D TO B'D CONNECTOR	PART NO.: BA41-00392A
MODULE CODE	LAST EDIT: March, 30, 2004 10:54:33 AM	PAGE 30 OF 41	

Main DDR Power

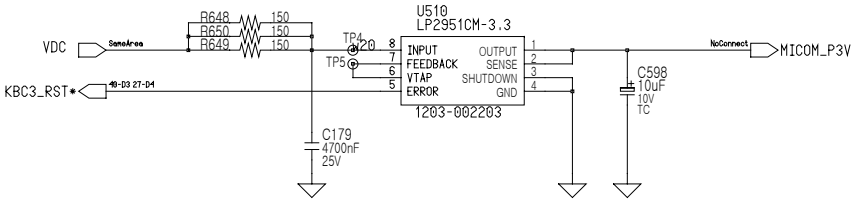




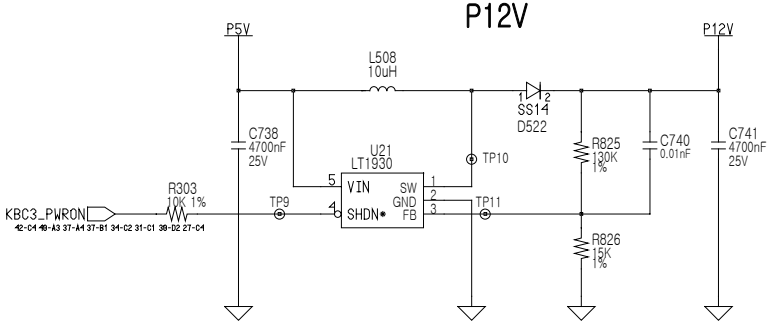


DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	DDR & GRAPHIC POWER	PART NO.: BA41-00392A
MODULE CODE:	LAST EDIT: March, 30, 2004 10:55:56 AM	PAGE 31 OF 41	

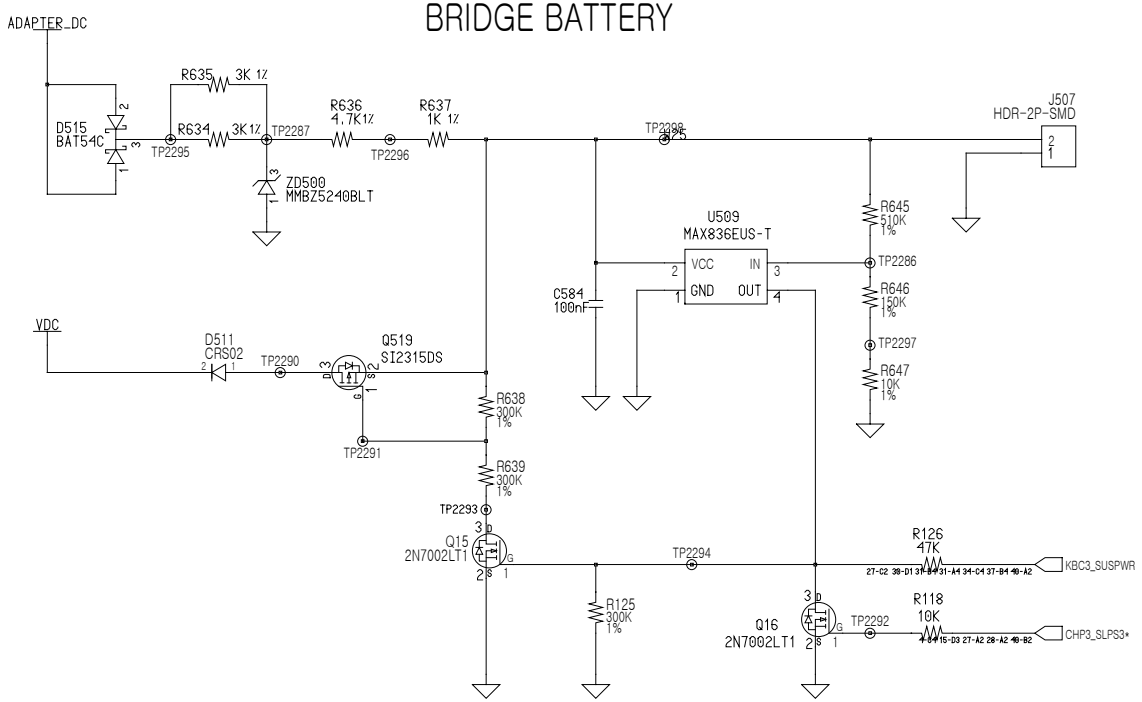
MICOM_P3V Power

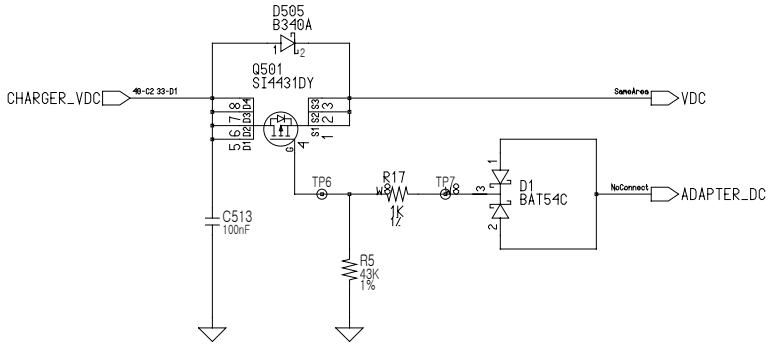


P12V

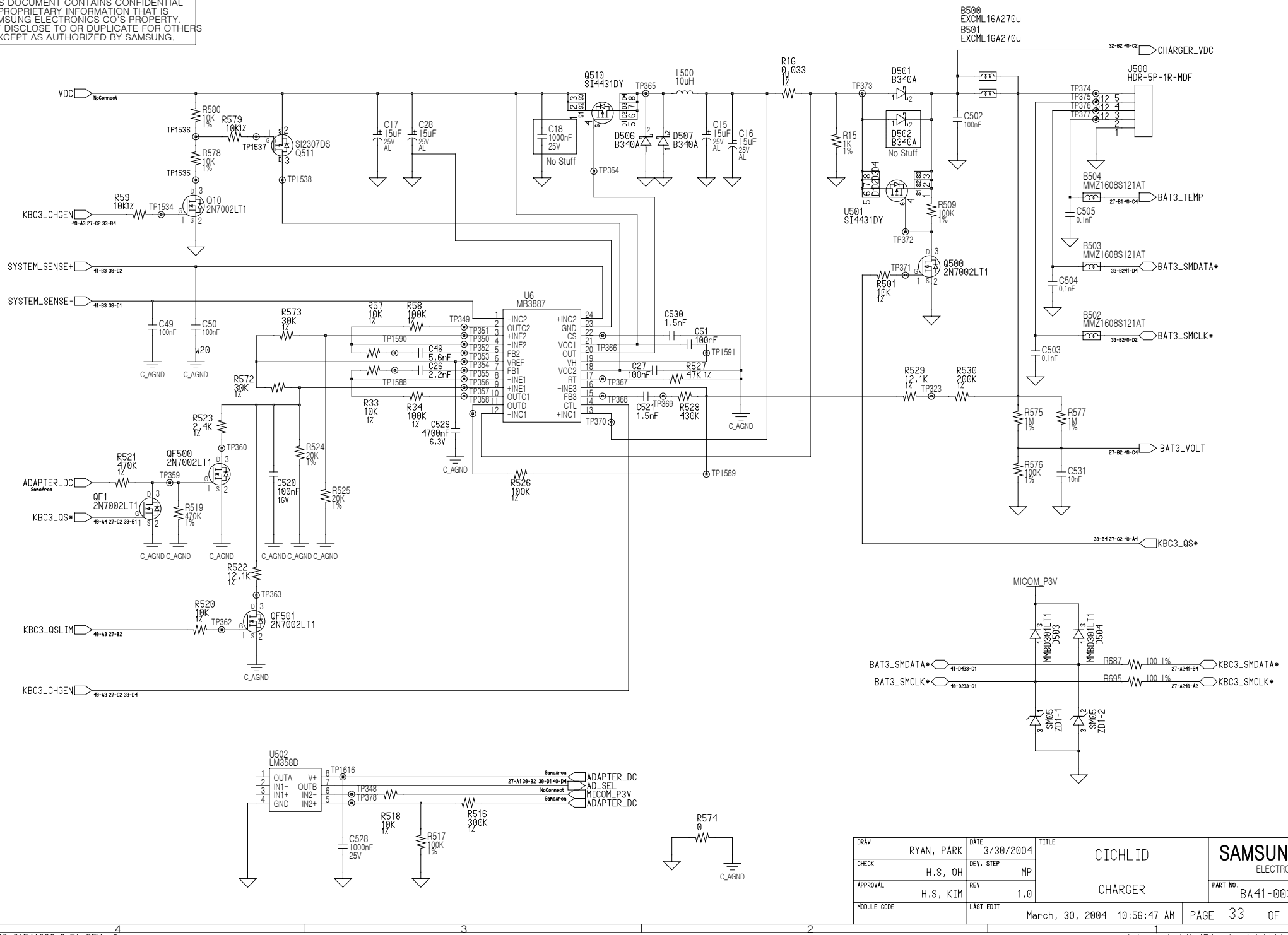


BRIDGE BATTERY



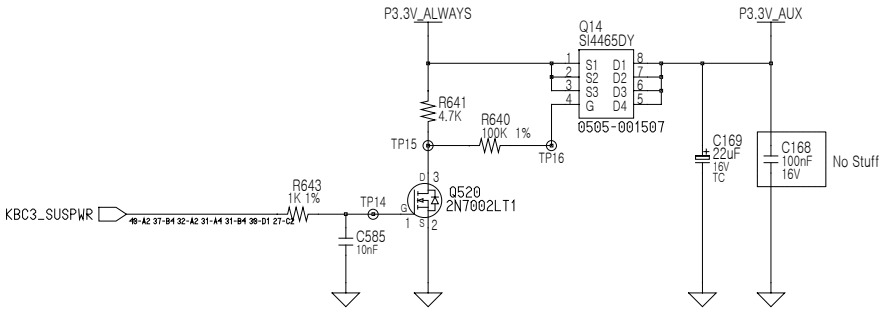


DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	MICOM & P12V & BBVL POWER	PART NO.: BA41-00392A
MODULE CODE:	LAST EDIT: March, 30, 2004 10:56:31 AM	PAGE 32 OF 41	

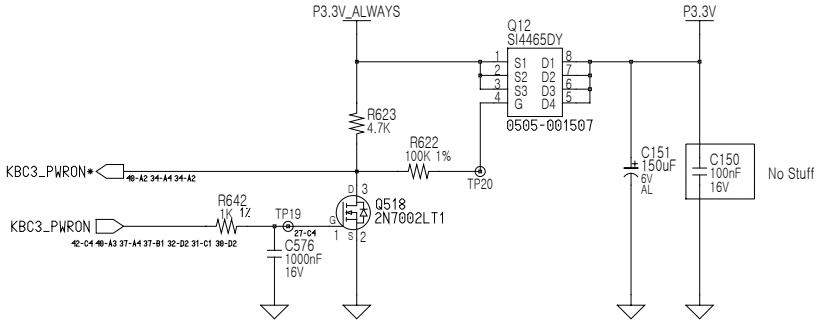


DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	CHARGER	PART NO.: BA41-00392A
MODULE CODE	LAST EDIT: March, 30, 2004 10:56:47 AM	PAGE 33 OF 41	

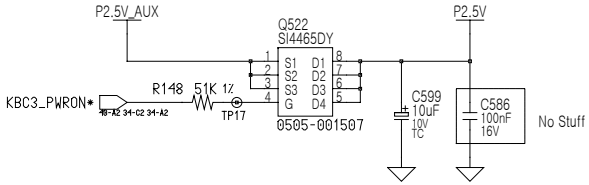
Switched Power On (P3.3V_AUX)

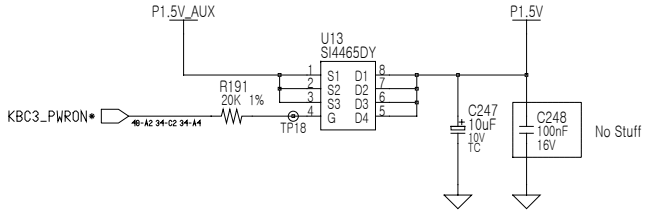


Switched Power On (P3.3V)

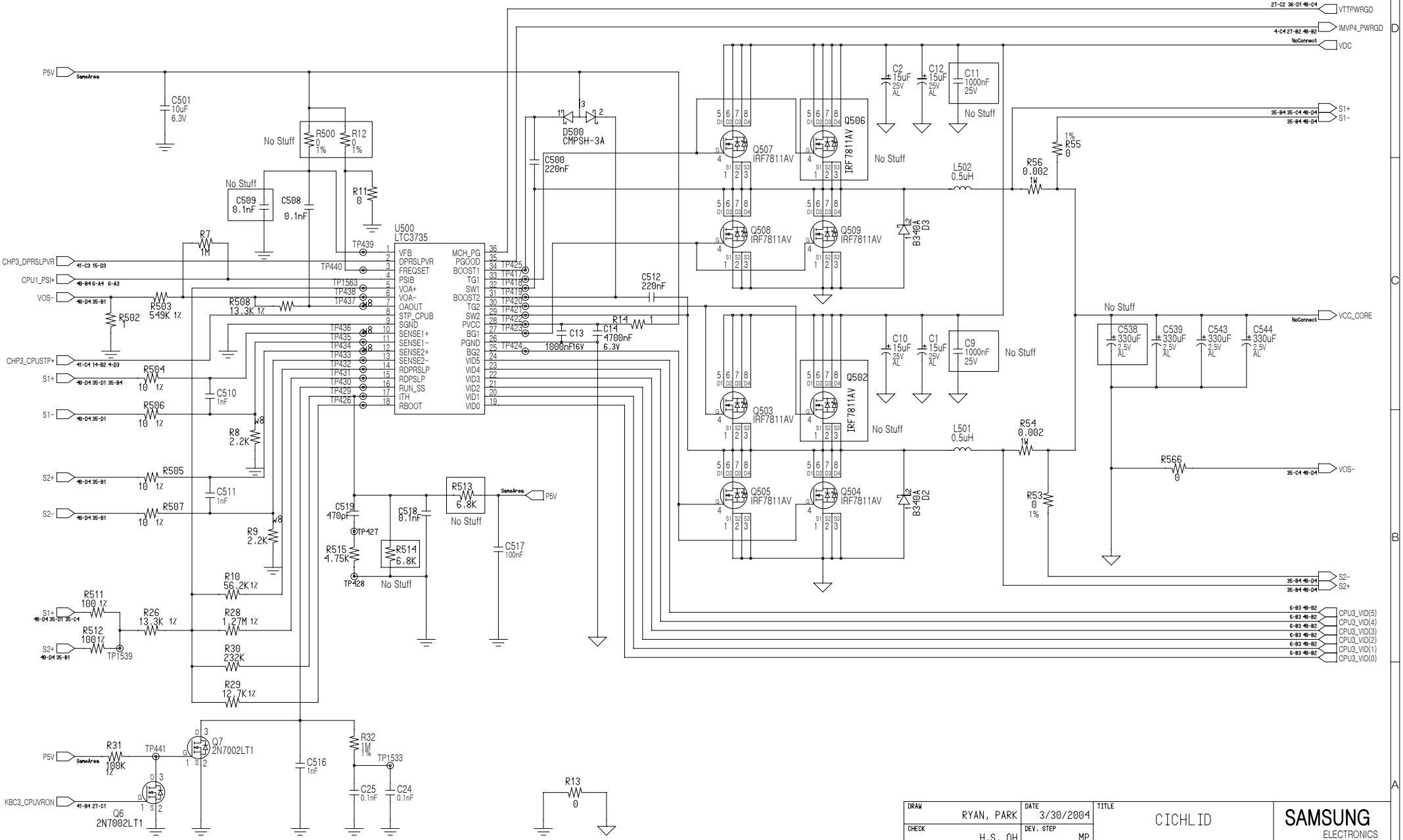


Switched Power On (P2.5V, P1.5V)

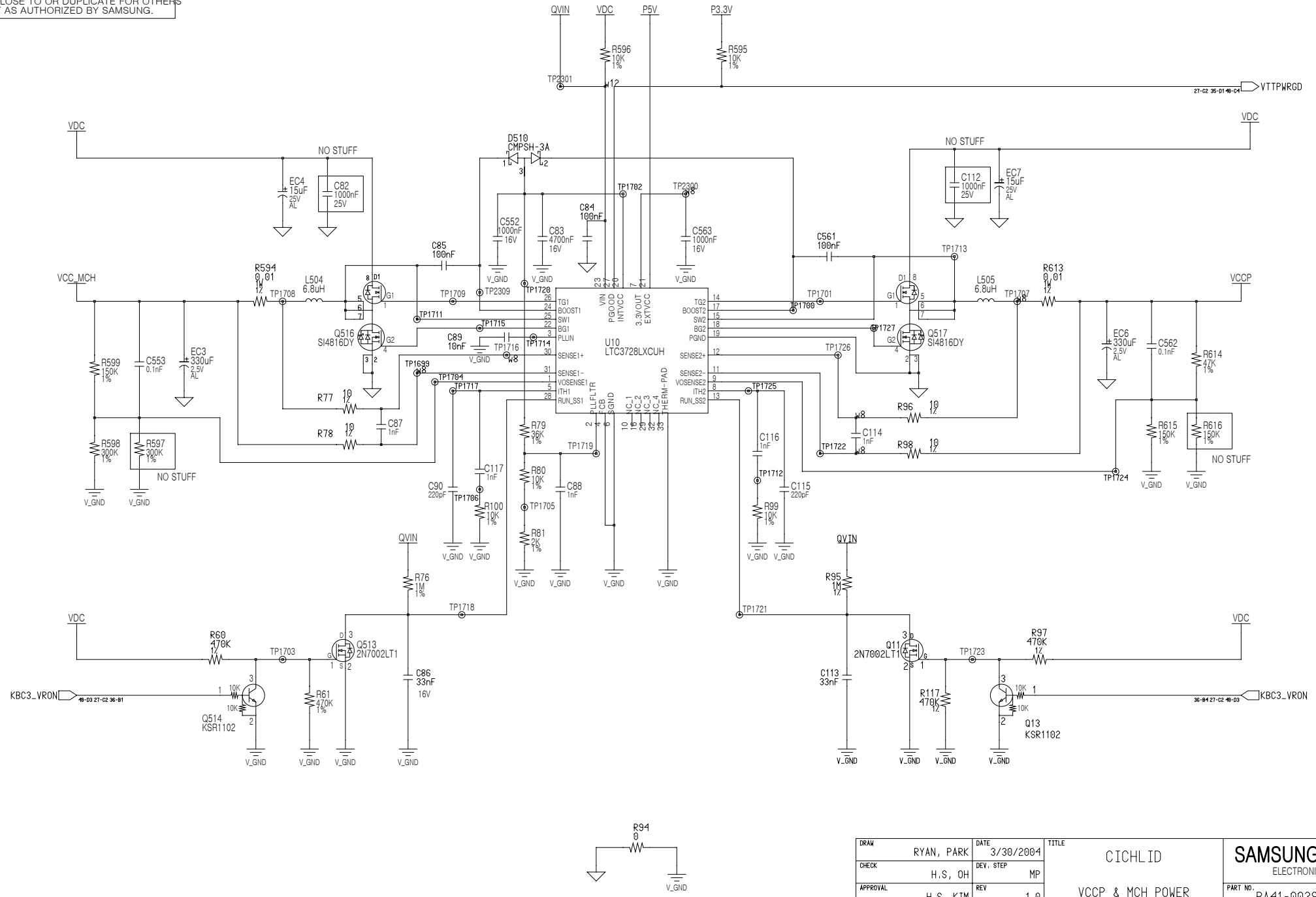




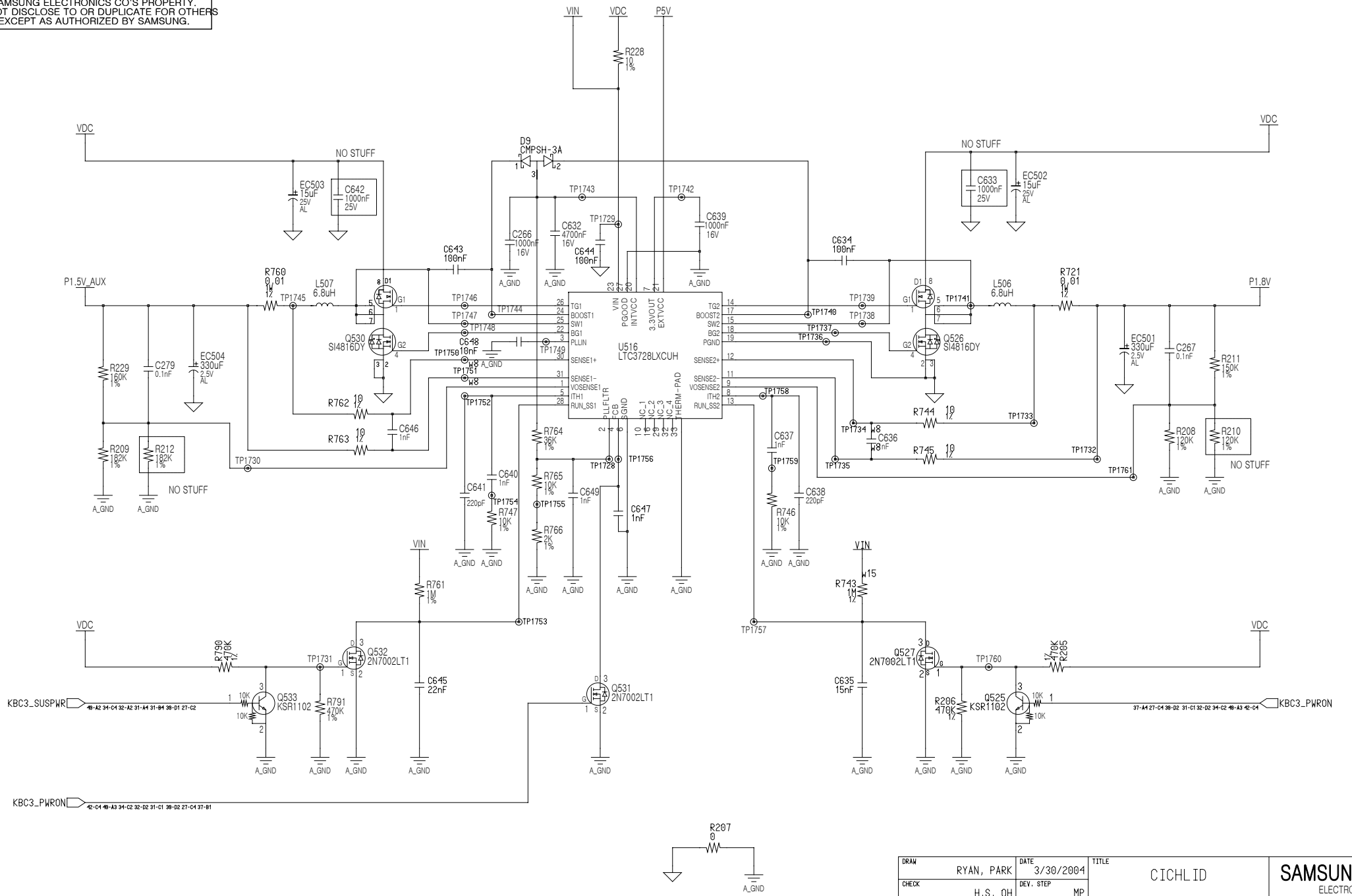
DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	P3.3 & P2.5 & P1.5 POWER	PART NO.: BA41-00392A
MODULE CODE	LAST EDIT: March, 30, 2004 10:57:13 AM	PAGE 34 OF 41	



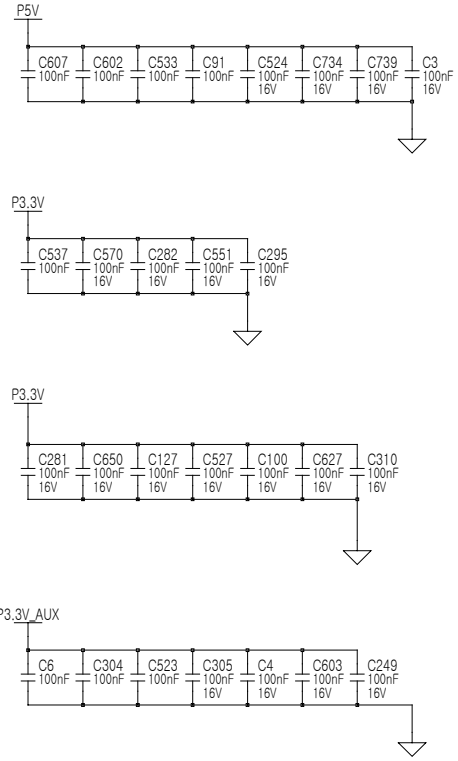
DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	CPU POWER	PART NO.: BA41-00392A
MODULE CODE	LAST EDIT: March, 30, 2004 10:57:28 AM	PAGE 35 OF 41	

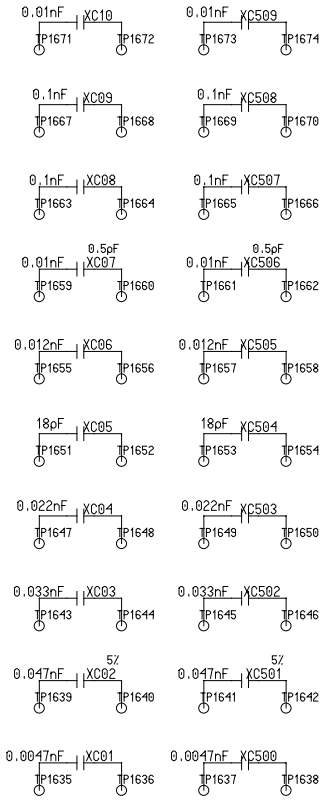


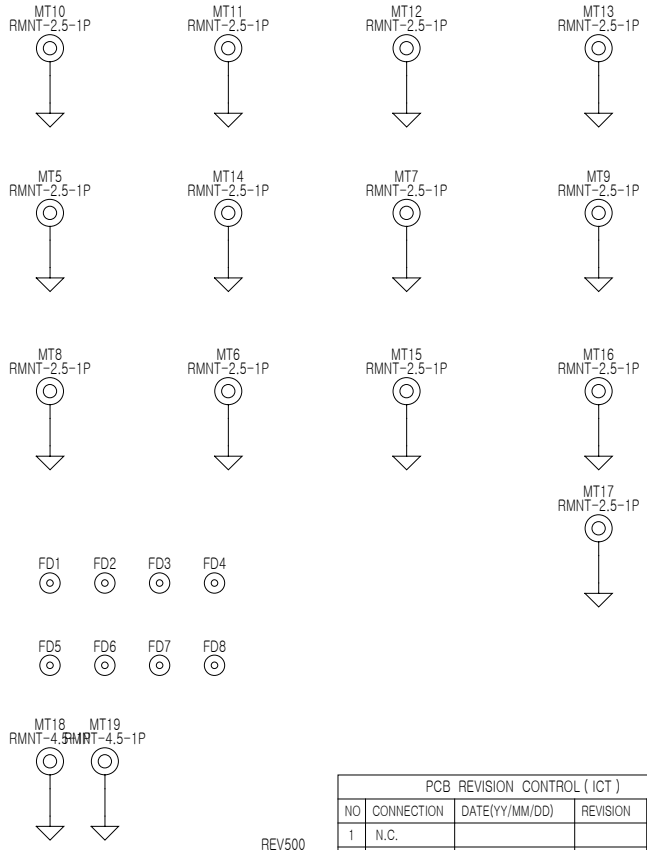
DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	VCCP & MCH POWER	PART NO.: BA41-00392A
MODULE CODE:	LAST EDIT: March, 30, 2004 10:57:47 AM	PAGE 36 OF 41	



DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	P1.5 & P.1.8 POWER	PART NO.: BA41-00392A
MODULE CODE:	LAST EDIT: March, 30, 2004 10:58:18 AM	PAGE 37 OF 41	



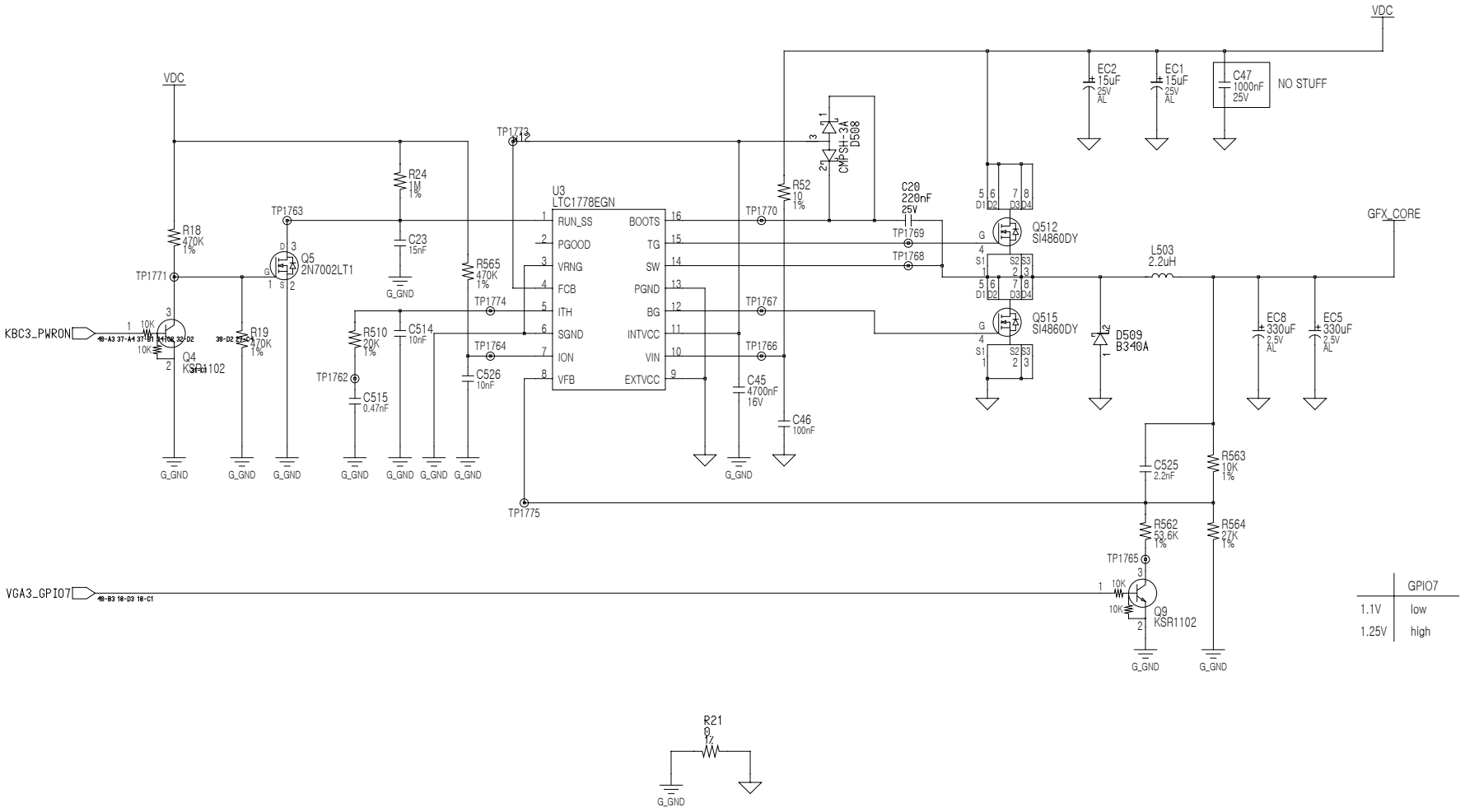




PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	MOUNT HOLE & REV.	PART NO.: BA41-00392A
MODULE CODE	LAST EDIT: March, 30, 2004 10:58:37 AM		PAGE 38 OF 41

Graphic Core Power



DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS
CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	GRAPHIC POWER	PART NO.: BA41-00392A
MODULE CODE	LAST EDIT: March, 30, 2004 11:43:13 AM	PAGE 39 OF 41	

TP1050OS1+
TP1051OS1-
TP1052OS2+
TP1053OS2-

TP1055OVOS-
TP1056OCD5_L
TP1057OCD5_R
TP1058OHP_IN

TP1062OAD_SEL
TP1063OA_CD1*
TP1064OA_CD2*
TP1065OCB3_B4
TP1066OCB3_B8
TP1067OCB3_D5
TP1068OCB3_J1

TP1074OVGA3_C
TP1075OVGA3_Y
TP1076OCA3_VCC
TP1077OCB3_VCC
TP1078OCD5_COM
TP1079OCDD5_A0
TP1080OCDD5_A1
TP1081OCDD5_A2
TP1018OHDD5_A0
TP1019OHDD5_A1
TP1020OHDD5_A2
TP1021OINV_VDC

TP1026OMS_RFU7
TP1027OMS_SCLK

TP1045OAUD5_CDL
TP1046OAUD5_CDR
TP1047OA_MC_CD*
TP1048OCB12_VPP
TP1049OCB3_CCLK
TP986OCB3_CPAR
TP987OCB3_CVS1
TP988OCB3_CVS2
TP989OCLK0_ITP
TP990OCPU1_NMI
TP991OCPU1_TCK
TP992OCPU1_TDI
TP993OCPU1_TDO
TP994OCPU1_TMS
TP995OHUB1_STB
TP996OKBC3_QS*
TP997OMEM2_BS0
TP998OMEM2_BS1
TP999OPCI3_PAR
TP1000OSMB3_CLK
TP1001OUSB3_P0+

TP1002OUSB3_P0-
TP1003OUSB3_P1+
TP1004OUSB3_P1-
TP1005OUSB3_P2+
TP1006OUSB3_P2-
TP1007OUSB3_P3+
TP1008OUSB3_P3-

TP955OVGA3_RED
TP956OVTTPWRGD
TP957OAGP1_GPAR
TP958OAGP1_RBF*
TP959OAGP1_VREF
TP960OAGP1_WBF*
TP961OAUD3_SPKR
TP962OBAT3_TEMP
TP963OBAT3_VOLT

TP966OCB3_BVPP0
TP967OCB3_BVPP1
TP968OCB3_CCD1*
TP969OCB3_CCD2*
TP970OCB3_CGNT*
TP971OCB3_CINT*
TP972OCB3_CREQ*
TP973OCB3_CRST*
TP974OCBS3_SPKR
TP975OCDD5_CS1*
TP976OCDD5_CS3*
TP977OCDD5_D(0)
TP978OCDD5_D(1)
TP979OCDD5_D(2)
TP980OCDD5_D(3)
TP981OCDD5_D(4)
TP982OCDD5_D(5)
TP983OCDD5_D(6)
TP984OCDD5_D(7)
TP985OCDD5_D(8)
TP922OCDD5_D(9)
TP923OCDD5_DREQ
TP924OCDD5_IOR*
TP925OCDD5_IOW*
TP926OCHP3_PME*
TP927OCHP3_SPKR
TP928OCLK0_ITP*
TP929OCPU1_ADS*
TP930OCPU1_BNR*
TP931OCPU1_HIT*
TP932OCPU1_INTR
TP933OCPU1_PSI*
TP934OCPU1_RS0*
TP935OCPU1_RS1*
TP936OCPU1_RS2*
TP937OCPU1_SLP*
TP938OCPU1_SMI*
TP939OHDD3_LED*
TP940OHDD5_CS1*
TP941OHDD5_CS3*
TP942OHDD5_D(0)
TP943OHDD5_D(1)
TP944OHDD5_D(2)
TP945OHDD5_D(3)
TP946OHDD5_D(4)
TP947OHDD5_D(5)
TP948OHDD5_D(6)
TP949OHDD5_D(7)
TP950OHDD5_D(8)
TP951OHDD5_D(9)
TP952OHDD5_DREQ
TP953OHDD5_IOR*

TP890OHDD5_IOW*
TP891OHDD5_LED*
TP892OHUB1_STB*
TP893OKBC3_A20G
TP894OKBC3_BRIT
TP895OKBC3_RST*
TP896OKBC3_VRON

TP899OKBC5_TCLK
TP900OLAN3_PME*

TP902OLCD_VDD3V
TP903OMDC_AUDIN
TP904OMEM2_CKE0
TP905OMEM2_CKE1
TP906OMEM2_CKE2
TP907OMEM2_CKE3
TP908OMEM2_RBS0
TP909OMEM2_RBS1
TP910OPCI3_RST*
TP911OSMB3_DATA
TP912OUSB3_OC0*
TP913OUSB3_OC1*
TP914OUSB3_OC2*
TP915OUSB3_OC3*
TP916OUSB3_OC4*
TP917OUSB3_OC5*
TP918OVGA3_BLUE

TP921OVGA3_DDCC
TP858OVGA3_DDCD
TP859OVGA3_SSON
TP860OVGA5_DDCC
TP861OVGA5_DDCD
TP862OADAPTER_DC
TP863OAGP1_GGNT*
TP864OAGP1_GREQ*
TP865OAGP1_PIPE*
TP866OAGP1_ST(0)
TP867OAGP1_ST(1)
TP868OAGP1_ST(2)
TP869OAGP3_BUSY*
TP870OAUD3_PHONE
TP871OAUD3_SPDIF
TP872OAUD5_CDCOM
TP873OBLT3_RFON
TP874OCB3_AVCC3*

TP876OCB3_BVCC3*
TP877OCB3_BVCC5*
TP878OCB3_CAD(0)
TP879OCB3_CAD(1)
TP880OCB3_CAD(2)
TP881OCB3_CAD(3)
TP882OCB3_CAD(4)
TP883OCB3_CAD(5)
TP884OCB3_CAD(6)
TP885OCB3_CAD(7)
TP886OCB3_CAD(8)
TP887OCB3_CAD(9)
TP888OCB3_CAUDIO
TP889OCB3_CCBE0*
TP826OCB3_CCBE1*
TP827OCB3_CCBE2*
TP828OCB3_CCBE3*
TP829OCB3_CIRDY*
TP830OCB3_CPERR*
TP831OCB3_CSERR*
TP832OCB3_CSTOP*
TP833OCB3_CTRDY*
TP834OCDD5_D(10)
TP835OCDD5_D(11)
TP836OCDD5_D(12)
TP837OCDD5_D(13)
TP838OCDD5_D(14)
TP839OCDD5_D(15)
TP840OCDD5_DACK*
TP841OCDD5_IORDY

TP842OCHP3_VBIAS
TP843OCLK0_HCLK0
TP844OCLK0_HCLK1
TP845OCLK0_HCLK2
TP846OCLK2_MCLK0
TP847OCLK2_MCLK1
TP848OCLK2_MCLK2
TP849OCLK2_MCLK3
TP850OCLK2_MCLK4
TP851OCLK2_MCLK5
TP852OCLK3_AGP66
TP853OCLK3_ICH14
TP854OCLK3_ICH48
TP855OCLK3_ICH66
TP856OCLK3_MCH66
TP857OCPU1_A*(3)
TP794OCPU1_A*(4)
TP795OCPU1_A*(5)
TP796OCPU1_A*(6)
TP797OCPU1_A*(7)
TP798OCPU1_A*(8)
TP799OCPU1_A*(9)
TP800OCPU1_A20M*
TP801OCPU1_BPM0*
TP802OCPU1_BPM1*
TP803OCPU1_BPM2*
TP804OCPU1_BPM3*
TP805OCPU1_BPRI*
TP806OCPU1_BREQ*
TP807OCPU1_D*(0)
TP808OCPU1_D*(1)
TP809OCPU1_D*(2)
TP810OCPU1_D*(3)
TP811OCPU1_D*(4)
TP812OCPU1_D*(5)
TP813OCPU1_D*(6)
TP814OCPU1_D*(7)
TP815OCPU1_D*(8)
TP816OCPU1_D*(9)
TP817OCPU1_DBI0*
TP818OCPU1_DBI1*
TP819OCPU1_DBI2*
TP820OCPU1_DBI3*
TP821OCPU1_DBSY*
TP822OCPU1_DPWR*
TP823OCPU1_DRDY*
TP824OCPU1_FERR*
TP825OCPU1_HITM*
TP762OCPU1_INIT*
TP763OCPU1_LOCK*
TP764OCPU1_PRDY*
TP765OCPU1_PREQ*
TP766OCPU1_TRDY*
TP767OCPU1_TRST*
TP768OHDD5_D(10)
TP769OHDD5_D(11)
TP770OHDD5_D(12)
TP771OHDD5_D(13)
TP772OHDD5_D(14)
TP773OHDD5_D(15)
TP774OHDD5_DACK*
TP775OHDD5_IORDY
TP776OHUB1_HL(0)
TP777OHUB1_HL(1)
TP778OHUB1_HL(2)
TP779OHUB1_HL(3)
TP780OHUB1_HL(4)
TP781OHUB1_HL(5)
TP782OHUB1_HL(6)
TP783OHUB1_HL(7)
TP784OHUB1_HL(8)
TP785OHUB1_HL(9)
TP786OKBC3_CHGEN
TP787OKBC3_PWRGD
TP788OKBC3_PWRON
TP789OKBC3_QSLIM

TP792OKBC5_TDATA
TP793OLAN3_DTOEE

TP730OLAN3_EECLK
TP731OLED5_AMBER
TP732OLED5_GREEN
TP733OMEM2_CB(0)
TP734OMEM2_CB(1)
TP735OMEM2_CB(2)
TP736OMEM2_CB(3)
TP737OMEM2_CB(4)
TP738OMEM2_CB(5)
TP739OMEM2_CB(6)
TP740OMEM2_CB(7)
TP741OMEM2_CSA0*
TP742OMEM2_CSA1*
TP743OMEM2_CSA2*
TP744OMEM2_CSA3*
TP745OMEM2_MD(0)
TP746OMEM2_MD(1)
TP747OMEM2_MD(2)
TP748OMEM2_MD(3)
TP749OMEM2_MD(4)
TP750OMEM2_MD(5)
TP751OMEM2_MD(6)
TP752OMEM2_MD(7)
TP753OMEM2_MD(8)
TP754OMEM2_MD(9)
TP755OMEM2_SWEA*

TP757OPCI3_AD(0)
TP758OPCI3_AD(1)
TP759OPCI3_AD(2)
TP760OPCI3_AD(3)
TP761OPCI3_AD(4)
TP698OPCI3_AD(5)
TP699OPCI3_AD(6)
TP700OPCI3_AD(7)
TP701OPCI3_AD(8)
TP702OPCI3_AD(9)
TP703OPCI3_CBE0*
TP704OPCI3_CBE1*
TP705OPCI3_CBE2*
TP706OPCI3_CBE3*
TP707OPCI3_GNT0*
TP708OPCI3_GNT1*
TP709OPCI3_GNT2*
TP710OPCI3_GNT3*
TP711OPCI3_GNT4*
TP712OPCI3_INTA*
TP713OPCI3_INTB*
TP714OPCI3_INTC*
TP715OPCI3_INTD*
TP716OPCI3_INTE*
TP717OPCI3_INTF*
TP718OPCI3_IRDY*
TP719OPCI3_PERR*
TP720OPCI3_REQ0*
TP721OPCI3_REQ1*
TP722OPCI3_REQ2*
TP723OPCI3_REQ3*
TP724OPCI3_REQ4*
TP725OPCI3_RSTF*
TP726OPCI3_SERR*
TP727OPCI3_STOP*
TP728OPCI3_TRDY*
TP729OVGA3_GPI00
TP666OVGA3_GPI07
TP667OVGA3_GREEN
TP668OVGA3_HSYNC
TP669OVGA3_SSOUT
TP670OVGA3_VSYNC
TP671OVGA5_HSYNC
TP672OVGA5_VSYNC
TP673OADAPTER_IN*
TP674OAGP1_ADSTB0
TP675OAGP1_ADSTB1
TP676OAGP1_GAD(0)
TP677OAGP1_GAD(1)
TP678OAGP1_GAD(2)
TP679OAGP1_GAD(3)
TP680OAGP1_GAD(4)
TP681OAGP1_GAD(5)

TP682OAGP1_GAD(6)
TP683OAGP1_GAD(7)
TP684OAGP1_GAD(8)
TP685OAGP1_GAD(9)
TP686OAGP1_GIRDY*
TP687OAGP1_GSTOP*
TP688OAGP1_GTRDY*
TP689OAUD5_SPK_L+
TP690OAUD5_SPK_L-
TP691OAUD5_SPK_R+
TP692OAUD5_SPK_R-
TP693OBAT3_SMCLK*

TP695OBLT3_WAKEUP
TP696OCB3_CAD(10)
TP697OCB3_CAD(11)
TP634OCB3_CAD(12)
TP635OCB3_CAD(13)
TP636OCB3_CAD(14)
TP637OCB3_CAD(15)
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TP652OCB3_CAD(30)
TP653OCB3_CAD(31)
TP654OCB3_CFRAME*
TP655OCB3_CSTSCHG
TP656OCHARGER_VDC
TP657OCHP3_GPIO42
TP658OCHP3_GPIO43
TP659OCHP3_OVERT*
TP660OCHP3_SERIRQ
TP661OCHP3_SLPS1*
TP662OCHP3_SLPS3*
TP663OCHP3_SLPS4*
TP664OCHP3_SLPS5*
TP665OCLK0_HCLK0*
TP602OCLK0_HCLK1*
TP603OCLK0_HCLK2*
TP604OCLK2_MCLK0*
TP605OCLK2_MCLK1*
TP606OCLK2_MCLK2*
TP607OCLK2_MCLK3*
TP608OCLK2_MCLK4*
TP609OCLK2_MCLK5*
TP610OCLK3_PCLKCB
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TP560OCPU1_DPSLP*
TP561OCPU1_IGNNE*
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TP563OCPU3_VID(1)
TP564OCPU3_VID(2)
TP565OCPU3_VID(3)
TP566OCPU3_VID(4)
TP567OCPU3_VID(5)

TP569OHUB1_HL(10)
TP506OHUB_REF_MCH
TP507OIMVP4_PWRGD

TP509OKBC3_BKLTON
TP510OKBC3_LBLED*
TP511OKBC3_PWRON*
TP512OKBC3_PWRSW*
TP513OKBC3_SCLED*
TP514OKBC3_SMCLK*
TP515OKBC3_SUSPWR
TP516OKBC3_SYSCHG
TP517OKBC3_WLANON
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TP535OKBC5_KSO(9)
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TP537OLED3_CHARGE
TP474OLPC3_LAD(0)
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TP472OMEM2_MD(48)
TP473OMEM2_MD(49)

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CHECK: H.S, OH	DEV. STEP: MP		
APPROVAL: H.S, KIM	REV: 1.0	TP	PART NO.: BA41-00392A
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TP1499 MEM2_MD(51)
TP1500 MEM2_MD(52)
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TP1467 MEM2_SCASA*
TP1468 MEM2_SRASA*
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TP1492 PCI3_PLOCK*
TP1493 SMB3_ALERT*
TP1494 VGA3_BKLTON
TP1495 AGP1_ADSTB0*
TP1496 AGP1_ADSTB1*
TP1497 AGP1_GAD(10)
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TP1455 AGP1_GFRAME*
TP1456 BAT3_SMDATA*
TP1457 BLT3_PWRBTN*
TP1458 CB3_CCLKRUN*
TP1459 CB3_CDEVSEL*
TP1460 CDD5_IRQ(15)
TP1461 CHP3_BATLOW*
TP1462 CHP3_BIOSWP*
TP1463 CHP3_C3STAT*
TP1464 CHP3_CPUSTP*
TP1465 CHP3_EE_DOUT
TP1402 CHP3_PATADET
TP1403 CHP3_PCGNTA*
TP1404 CHP3_PCGNTB*
TP1405 CHP3_PCISTP*
TP1406 CHP3_PCREQA*
TP1407 CHP3_PCREQB*
TP1408 CHP3_RTCRST*
TP1409 CHP3_SATADET
TP1410 CHP3_SMLINK0
TP1411 CHP3_SMLINK1
TP1412 CLK3_PCLKFWH
TP1413 CLK3_PCLKICH
TP1414 CLK3_PCLKLAN
TP1415 CLK3_PCLKMIN

TP1417 CPU1_ADSTB0*
TP1418 CPU1_ADSTB1*
TP1419 CPU1_CPURST*
TP1420 CPU1_DSTBN0*
TP1421 CPU1_DSTBN1*
TP1422 CPU1_DSTBN2*
TP1423 CPU1_DSTBN3*
TP1424 CPU1_DSTBP0*
TP1425 CPU1_DSTBP1*
TP1426 CPU1_DSTBP2*
TP1427 CPU1_DSTBP3*
TP1428 CPU1_GTLREF0
TP1429 CPU1_REQ*(0)
TP1430 CPU1_REQ*(1)
TP1431 CPU1_REQ*(2)
TP1432 CPU1_REQ*(3)
TP1433 CPU1_REQ*(4)
TP1370 CPU1_STPCLK*
TP1371 CPU2_THERMDA
TP1372 CPU2_THERMDC

TP1374 HUB1_HVSWING
TP1375 HUB1_REF_ICH
TP1376 ISA3_IRQ(14)
TP1377 ISA3_IRQ(15)
TP1378 KBC3_CPURST*
TP1379 KBC3_CPUVRON
TP1380 KBC3_EXTSMI*
TP1381 KBC3_FANCTRL
TP1382 KBC3_NUMLED*
TP1383 KBC3_RSMRST*
TP1384 KBC3_RUNSCI*
TP1385 KBC3_SMDATA*
TP1386 KBC3_SPKMUTE
TP1387 KBC5_KSO(10)
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TP1394 LID3_SWITCH*
TP1395 LPC3_LFRAME*
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TP1281 MEM2_RSRASA*
TP1282 MSTRAPSEL(0)
TP1283 MSTRAPSEL(1)
TP1284 MSTRAPSEL(2)
TP1285 MSTRAPSEL(3)
TP1286 PCI3_CLKRUN*
TP1287 PCI3_DEVSEL*
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TP1289 VGA3_DVOD(1)

TP1290 VGA3_DVOD(2)
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TP1294 VGA3_DVOD(6)
TP1295 VGA3_DVOD(7)
TP1296 VGA3_DVOD(8)
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TP1298 VGA3_VIPD(0)
TP1299 VGA3_VIPD(1)
TP1300 VGA3_VIPD(2)
TP1301 VGA3_VIPD(3)
TP1302 VGA3_VIPD(4)
TP1303 VGA3_VIPD(5)
TP1304 VGA3_VIPD(6)
TP1305 VGA3_VIPD(7)
TP1242 VGA3_VIPHAD0
TP1243 VGA3_VIPHAD1
TP1244 AGP1_GCBE*(0)
TP1245 AGP1_GCBE*(1)
TP1246 AGP1_GCBE*(2)
TP1247 AGP1_GCBE*(3)
TP1248 AGP1_GDEVSEL*
TP1249 AUD3_MONO_OUT
TP1250 CHP3_AC97_SDO
TP1251 CHP3_BAYPWRON
TP1252 CHP3_BIOSTBL*
TP1253 CHP3_CDBUFEN*
TP1254 CHP3_DPRSLPVR
TP1255 CHP3_IVTPWRON
TP1256 CHP3_SUSSTAT*
TP1257 CPU1_PWRGDCPU

TP1264 KBC3_CAPSLED*
TP1265 KBC3_CD_CON1*
TP1266 KBC3_CD_CON2*
TP1267 KBC3_EZ_BTN0*
TP1268 KBC3_EZ_BTN1*
TP1269 KBC3_EZ_BTN2*
TP1270 KBC3_LANGRST*
TP1271 KBC3_WAKESCI*
TP1272 MCH1_HVSWING0
TP1273 MCH1_HVSWING1
TP1210 MEM2_RMAA(10)
TP1211 MEM2_RMAA(11)
TP1212 MEM2_RMAA(12)
TP1213 SYSTEM_SENSE+
TP1214 SYSTEM_SENSE-
TP1215 VGA3_DVOD(10)
TP1216 VGA3_DVOD(11)
TP1217 VGA3_DVOHSYNC
TP1218 VGA3_LCDVDDON
TP1219 AUD5_MIC_CODEC
TP1220 A_LID3_SWITCH*
TP1221 BLT3_BTON_LED*
TP1222 CHP3_AC97_BCLK
TP1223 CHP3_AC97_RST*
TP1224 CHP3_AC97_SDI0
TP1225 CHP3_AC97_SDI1
TP1226 CHP3_AC97_SDI2
TP1227 CHP3_AC97_SYNC
TP1228 CHP3_INTRUDER*
TP1229 CHP3_THRMTRIP*
TP1230 CLK3_PCLKMICOM
TP1231 CPU1_THRMTRIP*

TP1233 KBC3_SPDIF_ON*
TP1234 AUD5_LINE_OUT_L
TP1235 AUD5_LINE_OUT_R
TP1236 CHP3_1394_ROMW*

TP1238 A_AUD5_MIC_CODEC
TP1239 KBC3_IMVP4_PWRGD
TP1240 KBC3_THERM_SMCLK
TP1241 A_AUD5_LINE_OUT_L

TP1178 A_AUD5_LINE_OUT_R
TP1179 KBC3_THERM_SMDATA

TP1181 CHP3_BIOS_PROTECT*

TP1182 AVDD
TP1183 AVDD
TP1184 AVDD
TP1185 AVDD
TP1186 A_AVDD
TP1187 A_AVDD
TP1188 A_AVDD
TP1189 A_AVDD
TP1190 AUD_GND
TP1191 AUD_GND
TP1192 AUD_GND
TP1193 AUD_GND
TP1194 C_AGND
TP1195 C_AGND
TP1196 C_AGND
TP1197 C_AGND

TP1681 GROUND
TP10002 GROUND
TP10001 GROUND
TP1202 GROUND
TP1203 GROUND
TP1204 GROUND
TP1205 GROUND
TP1541 GROUND
TP1542 GROUND
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TP1147 GFX_CORE
TP1148 GFX_CORE
TP1149 GFX_CORE
TP1150 LFPPLLVDD
TP1151 LFPPLLVDD

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TP1155 MIC_GND
TP1156 MIC_GND
TP1157 MIC_GND
TP1158 MEM_VREF
TP1159 MEM_VREF
TP1160 MEM_VREF
TP1161 MEM_VREF
TP1162 MICOM_P3V
TP1163 MICOM_P3V
TP1164 MICOM_P3V
TP1165 MICOM_P3V
TP10003 5V

TP1167 5V
TP1168 5V
TP1169 5V
TP1170 P12V
TP1171 P12V
TP1172 P12V
TP1173 P12V
TP1174 P1.5V
TP1175 P1.5V
TP1176 P1.5V
TP1177 P1.5V
TP1114 P1.8V
TP1115 P1.8V
TP1116 P1.8V
TP1117 P1.8V
TP1118 P2.5V
TP1119 P2.5V
TP1120 P2.5V
TP1121 P2.5V
TP1122 P3.3V
TP1123 P3.3V
TP1124 P3.3V
TP1125 P3.3V
TP1543 P3.3V
TP1544 P3.3V
TP1126 P1.25V
TP1127 P1.25V
TP1128 P1.25V
TP1129 P1.25V

TP1130 P5V_CD
TP1131 P5V_CD

TP1134 PRTC_BAT
TP1135 PRTC_BAT

TP1138 P1.5V_AUX
TP1139 P1.5V_AUX
TP1140 P1.5V_AUX
TP1141 P1.5V_AUX
TP1142 P2.5V_AUX
TP1143 P2.5V_AUX
TP1144 P2.5V_AUX
TP1145 P2.5V_AUX
TP1082 P3.3V_AUX
TP1083 P3.3V_AUX
TP1084 P3.3V_AUX
TP1085 P3.3V_AUX
TP1086 P3.3V_ALWAYS
TP1087 P3.3V_ALWAYS
TP1088 P3.3V_ALWAYS
TP1089 P3.3V_ALWAYS

TP1098 VDC
TP10004 VDC
TP1099 VDC
TP1100 VDC
TP1101 VDC
TP1102 VCCP
TP1103 VCCP
TP1104 VCCP
TP1105 VCCP
TP1106 VCC_MCH
TP1107 VCC_MCH
TP1108 VCC_MCH
TP1109 VCC_MCH
TP1110 VCC_CORE
TP1111 VCC_CORE
TP1112 VCC_CORE
TP1113 VCC_CORE

TP1166 P5V

TP1576 ISL6225VCC_P5V

TP1561 FAN3_FDBACK*
TP1676 KBC3_SICEN*

TP2276 EVEN_VGA3_A0+
TP2277 EVEN_VGA3_A0-
TP2278 EVEN_VGA3_A1+
TP2279 EVEN_VGA3_A1-
TP2280 EVEN_VGA3_A2+
TP2281 EVEN_VGA3_A2-
TP2282 EVEN_VGA3_CLK+
TP2283 EVEN_VGA3_CLK-
TP2284 KBC3_THERM_ALERT*
TP2285 LCD3_BRIT

TP1804 ODD_VGA3_A0+
TP1805 ODD_VGA3_A0-
TP1806 ODD_VGA3_A1+
TP1807 ODD_VGA3_A1-
TP1808 ODD_VGA3_A2+
TP1809 ODD_VGA3_A2-
TP1810 ODD_VGA3_CLK+
TP1811 ODD_VGA3_CLK-

TP1814 VDD18DIG
TP1815 VIDEO_THERM_SMCLK
TP1816 VIDEO_THERM_SMDATA
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TP1818 A_GND
TP1819 A_GND
TP1820 A_GND
TP1821 D_GND
TP1822 D_GND
TP1823 D_GND
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TP1792 V_GND
TP1793 V_GND
TP1794 V_GND
TP1795 V_GND

DRAW: RYAN, PARK	DATE: 3/30/2004	TITLE: CICHLID	SAMSUNG ELECTRONICS	
CHECK: H.S, OH	DEV. STEP: MP			
APPROVAL: H.S, KIM	REV: 1.0	TP	PART NO.: BA41-00392A	
MODULE CODE	LAST EDIT: March, 30, 2004 11:53:18 AM	PAGE 41 OF 41		

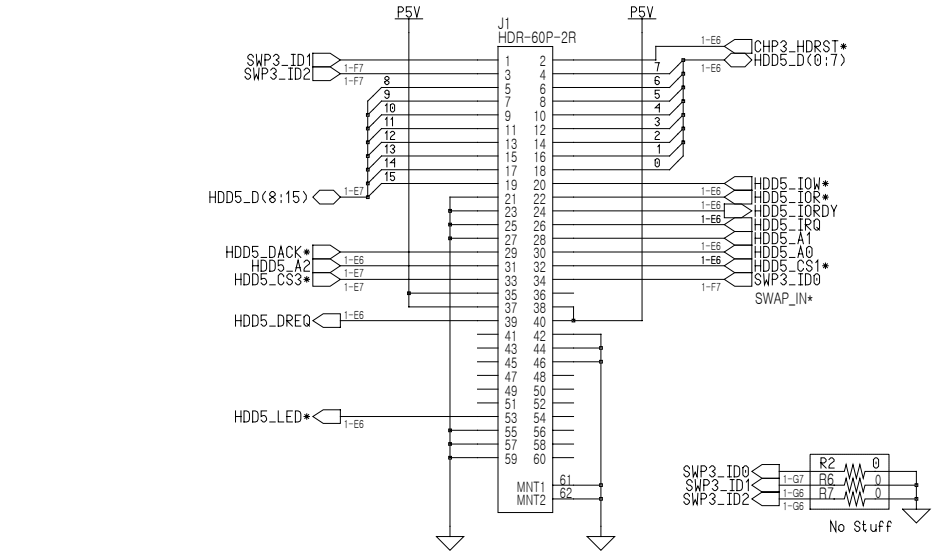
2ndHDD-I/F BOARD

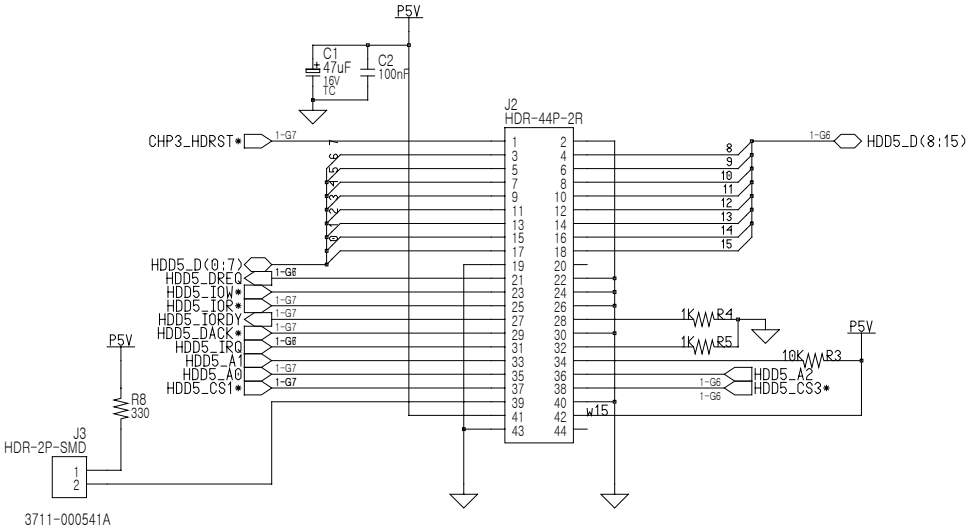
CPU : BANIAS
Chip Set : ODEM+
Remarks : 2ndHDD

Model Name : CICHLID
PBA Name : 2nd HDD Interface
A'ssy Code : BA59-01330A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2004. 1. 17

DRAW	CHECK	APPROVAL

■ *Owner :* *Signature :* X





SWAPBAY ID

Devices	SWAP_IN*
CD-ROM	0
2nd HDD	1 (No Connect)

MT1 RMNT-2.8-1P
MT2 RMNT-2.8-1P

DRAW: RYAN, PARK	DATE: 12/11/2003	TITLE: CICHLID 2ND HDD I/F B'D 2ND HDD I/F B'D	SAMSUNG ELECTRONICS
CHECK: OH, H.S	DEV. STEP: DV		
APPROVAL: LEE, KEVIN	REV: 1.0		PART NO.: BA41-XXXXXX
MODULE CODE	LAST EDIT: December, 11, 2003 5:35:29 PM	PAGE 1 OF 1	

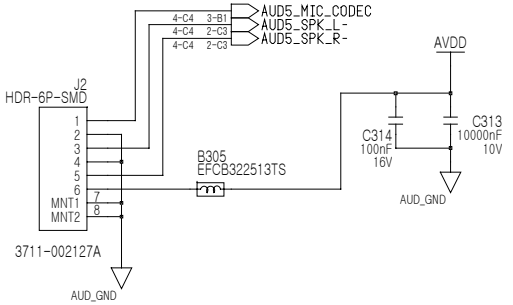
CICHLID

CPU : BANIAS/DOTHAN
Chip Set : ODEM+
Remarks :

Model Name : AUDIO Board
PBA Name :
PCB Code : BA59-01332A
Dev. Step : MP
Revision : 1.3
T.R. Date : 05/07/2004

DRAW	CHECK	APPROVAL

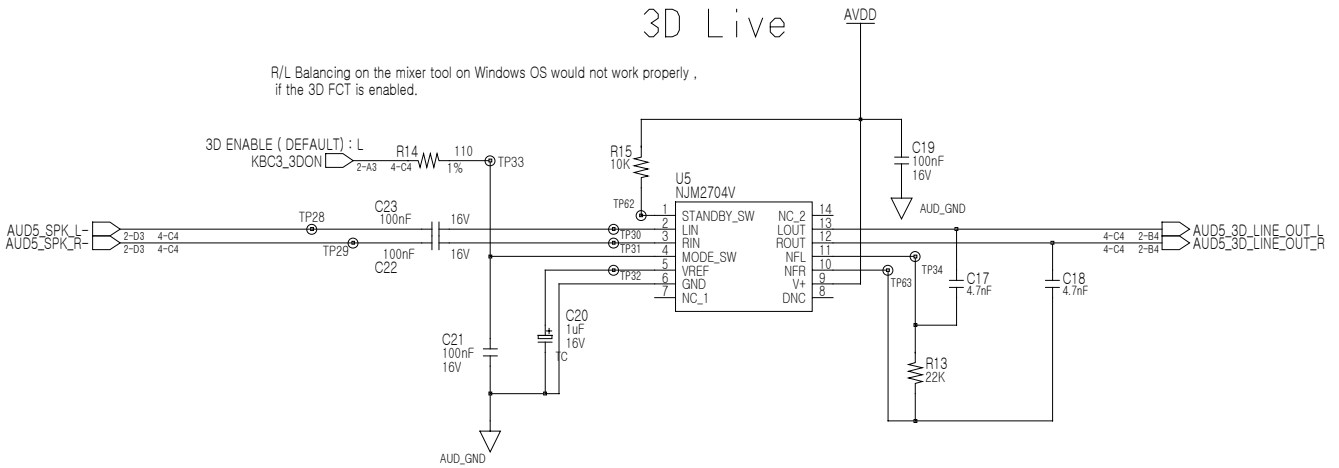
DRAW: PARK, RYAN	DATE: 3/22/2004	TITLE: CICHLID AUDIO BOARD	SAMSUNG ELECTRONICS
CHECK: OH, H.S	DEV. STEP: MP		
APPROVAL: LEE, KEVIN	REV: 1.1		PART NO.: BA59-01332A
MODULE CODE:	LAST EDIT: March 22, 2004 7:52:12 PM	PAGE 1 OF 4	



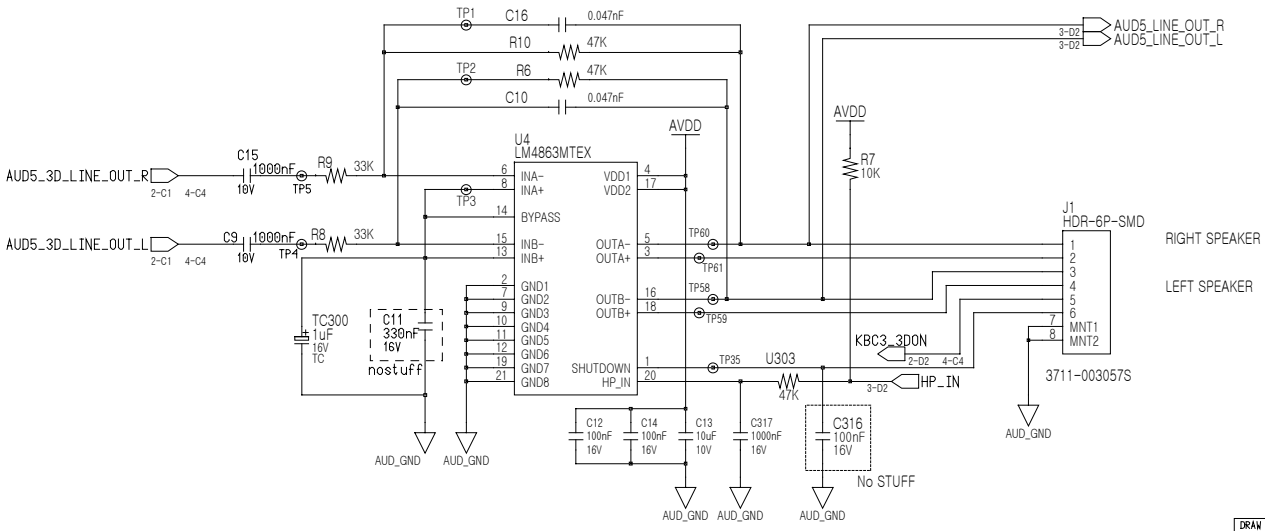
The Ground 'Line between MIC_CODEC and SPK_L-' of the 'Audio BD to Main BD Cable' must be shielded.

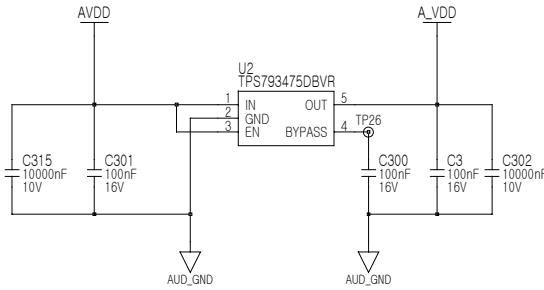
3D Live

R/L Balancing on the mixer tool on Windows OS would not work properly , if the 3D FCT is enabled.



Audio AMP



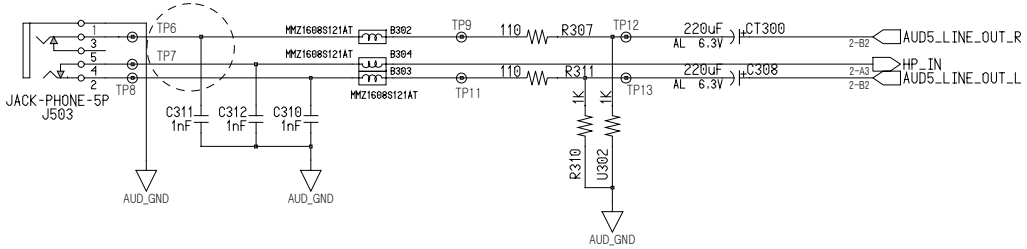


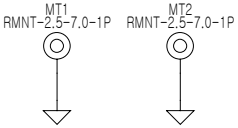
Enough Thermal Ground Area Should be Guaranteed for spreading intense heat of LM4863.

DRAW: PARK, RYAN	DATE: 3/22/2004	TITLE: CICHLID AUDIO BOARD UNDEFINED	SAMSUNG ELECTRONICS
CHECK: OH, H.S	DEV. STEP: MP		
APPROVAL: LEE, KEVIN	REV: 1.1		PART NO.: BA59-01332A
MODULE CODE	LAST EDIT: March 22, 2004 7:52:12 PM	PAGE 2 OF	

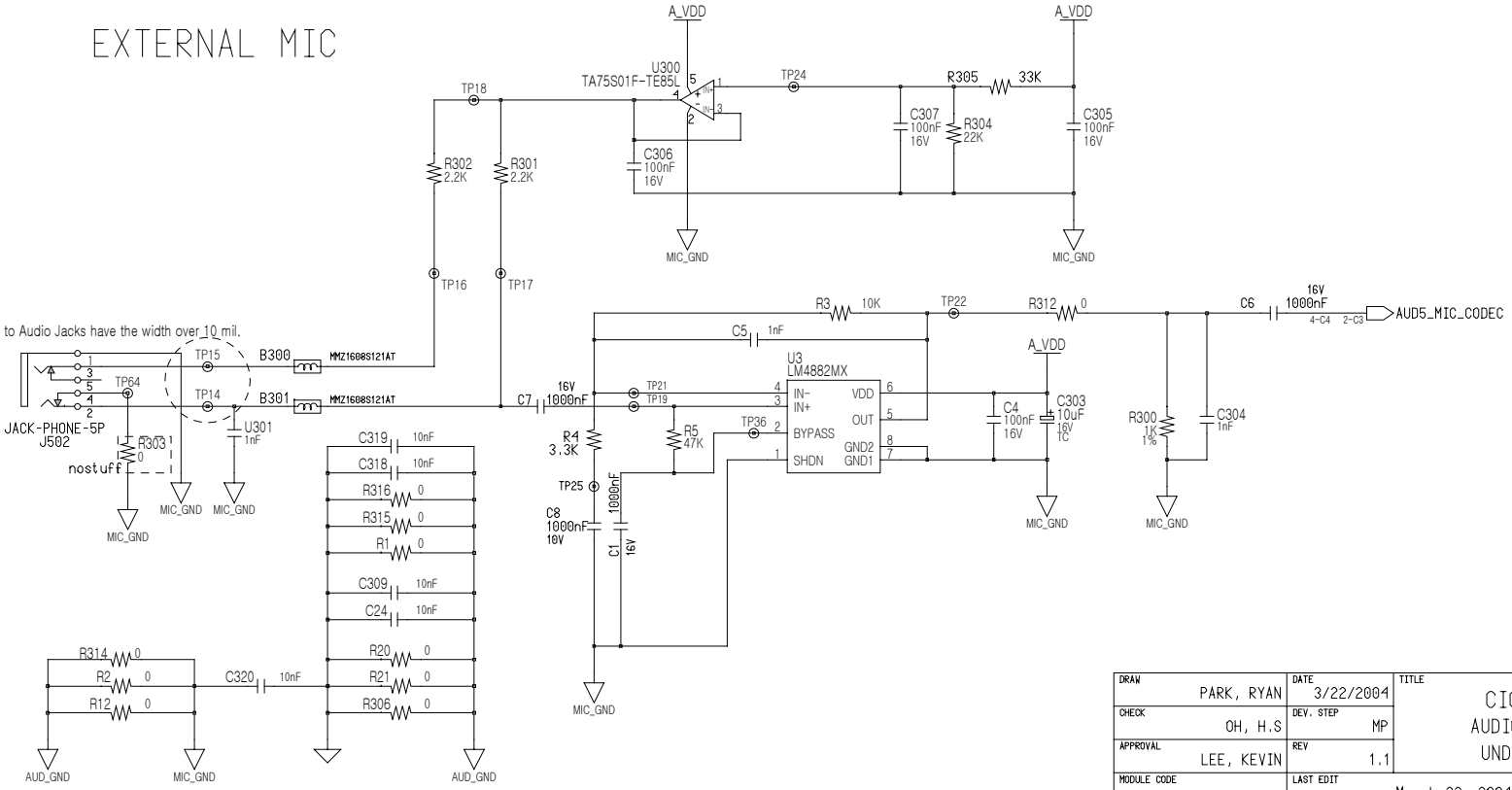
HEADPHONE

Make sure that the traces led to Audio Jacks have the width over 10 mil.





EXTERNAL MIC



DRAW: PARK, RYAN	DATE: 3/22/2004	TITLE: CICHLID AUDIO BOARD UNDEFINED	SAMSUNG ELECTRONICS
CHECK: OH, H.S	DEV. STEP: MP		
APPROVAL: LEE, KEVIN	REV: 1.1		PART NO.: BA59-01332A
MODULE CODE	LAST EDIT: March 22, 2004 7:52:12 PM	PAGE 3 OF 4	

TP37 KBC3_3DON
TP38 AUD5_SPK_L-
TP39 AUD5_SPK_R-
TP40 AUD5_MIC_CODEC

TP41 AUD5_3D_LINE_OUT_L
TP42 AUD5_3D_LINE_OUT_R

TP55 AVDD
TP54 A_VDD

TP43 AUD_GND

TP51 MIC_GND

DRAW: PARK, RYAN	DATE: 3/22/2004	TITLE: CICHLID AUDIO BOARD UNDEFINED	SAMSUNG ELECTRONICS
CHECK: OH, H.S	DEV. STEP: MP		
APPROVAL: LEE, KEVIN	REV: 1.1		PART NO.: BA59-01332A
MODULE CODE:	LAST EDIT: March 22, 2004 7:52:12 PM	PAGE 4 OF 4	

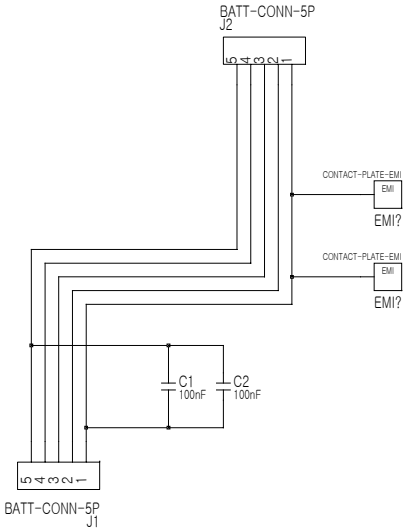
CICHLID

CPU : BANIAS / DOTHAN
Chip Set : ODEM+
Remarks :

Model Name : BATTERY BR. BOARD
PBA Name :
PCB Code : BA59-01331A
Dev. Step : MP
Revision : 1.2
T.R. Date : 2004.04.01

DRAW	CHECK	APPROVAL

To BATTERY



To MAIN

NET LIST NAME

#1 GND
#2 BAT3_TEMP
#3 BAT3_SMDATA*
#4 BAT3_SMCLK*
#5 VDC

DRAW: PARK, RYAN	DATE: 12/5/2003	TITLE: CICHLID BATTERY BRIDGE BOARD	SAMSUNG ELECTRONICS
CHECK: OH, H.S	DEV. STEP: DV		
APPROVAL: LEE, KEVIN	REV: 1.0		PART NO.: BA41-
MODULE CODE:	LAST EDIT: December, 5, 2003 6:00:28 PM	PAGE 1 OF 1	

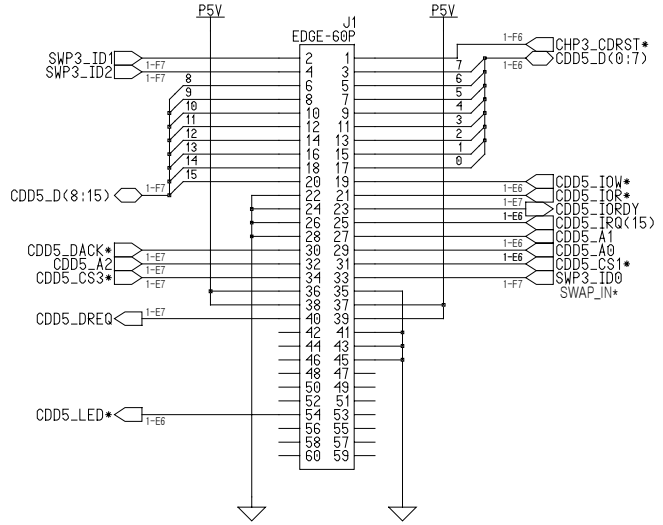
CD-I/F BOARD

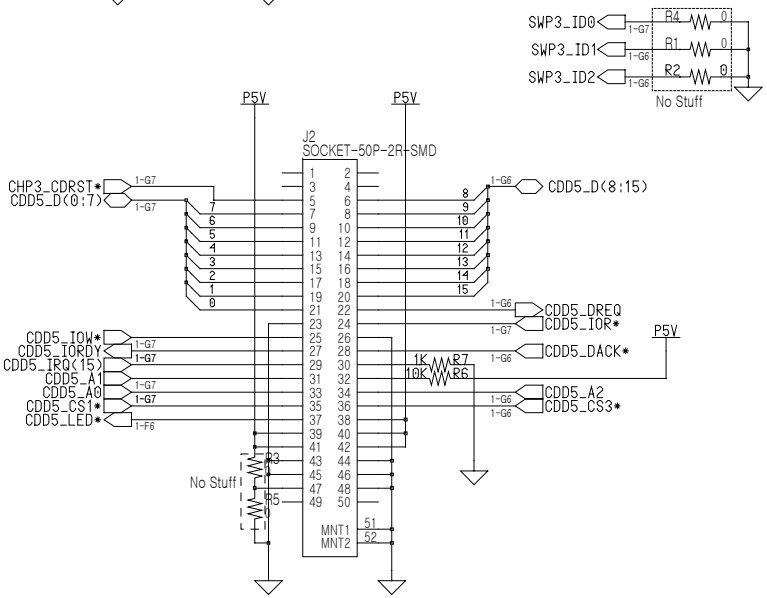
CPU : BANIAS/DOTHAN
Chip Set : ODEM+
Remarks : CD/COMBO/DVD-MULTI

Model Name : CICHLID
PBA Name : CD Interface
A'ssy Code : BA59-01333A
Dev. Step : MP
Revision : 1.1
T.R. Date : 2004.05.06

DRAW	CHECK	APPROVAL

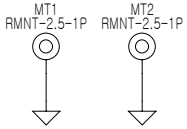
■ *Owner :* *Signature :* X





SWAPBAY ID

Devices	SWAP_IN*
CD-ROM	0
2nd HDD	1



DRAW: PARK, RYAN	DATE: 12/4/2003	TITLE: CICHLID CD I/F B'D CD I/F B'D	SAMSUNG ELECTRONICS
CHECK: OH, H.S	DEV. STEP: DV		
APPROVAL: LEE, KEVIN	REV: 1.0		PART NO.: BA41-XXXXXX
MODULE CODE	LAST EDIT: December, 4, 2003 2:55:12 PM	PAGE 1 OF 1	

ONTOP BOARD

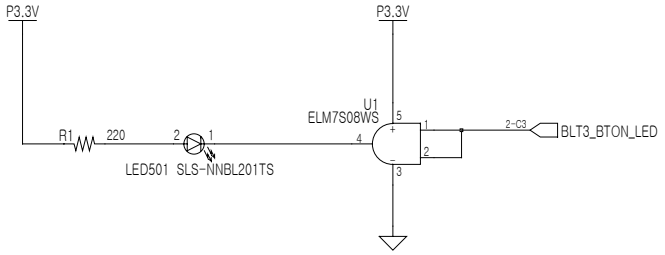
CPU : BANIAS/DOTHAN
Chip Set : ODEM+
Remarks : EASY BUTTON BOARD

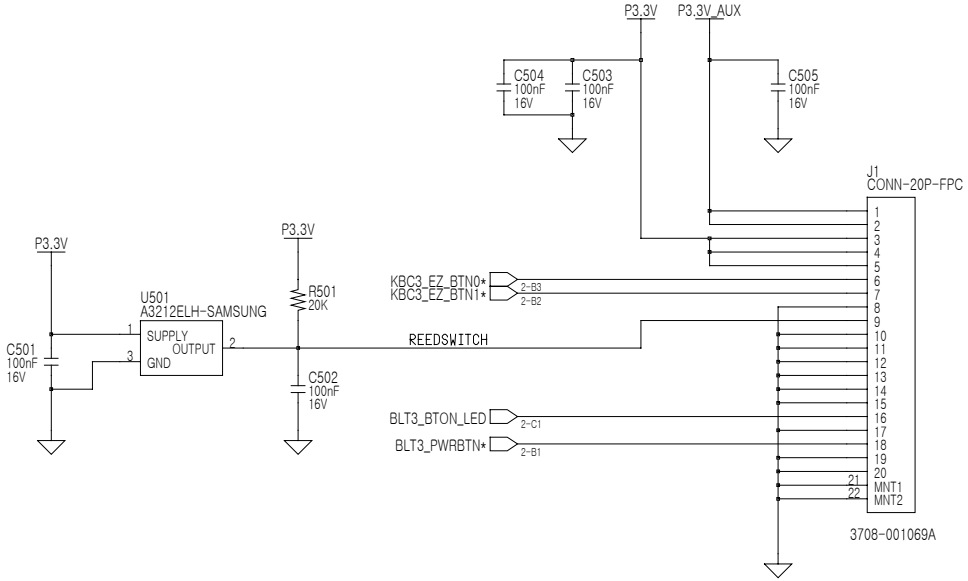
Model Name : ONTOP BOARD
PBA Name :
PCB Code : BA59-01334A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2004.01.28

DRAW	CHECK	APPROVAL

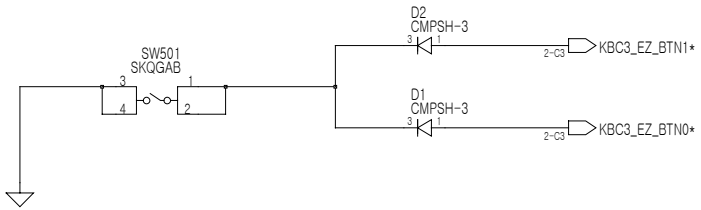
DRAW: PARK, RYAN	DATE: 12/3/2003	TITLE: CICHLID ONTOP BOARD	SAMSUNG ELECTRONICS
CHECK: OH, H.S	DEV. STEP: DV		
APPROVAL: LEE, KEVIN	REV: 1.0		PART NO.: BA41-
MODULE CODE:	LAST EDIT: January, 28, 2004 2:12:38 PM	PAGE 1 OF 2	

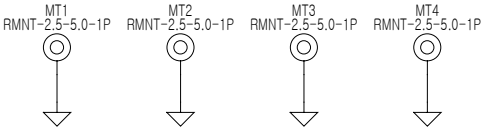
BLUETOOTH BUTTON LED



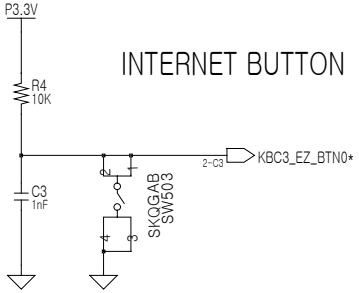


USER BUTTON

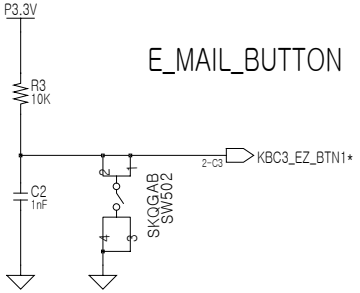




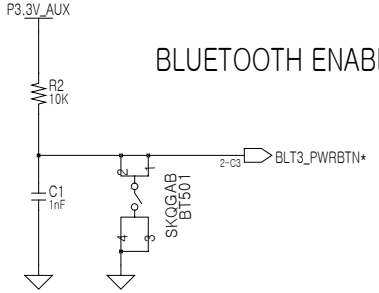
INTERNET BUTTON



E_MAIL_BUTTON



BLUETOOTH ENABLE BUTTON



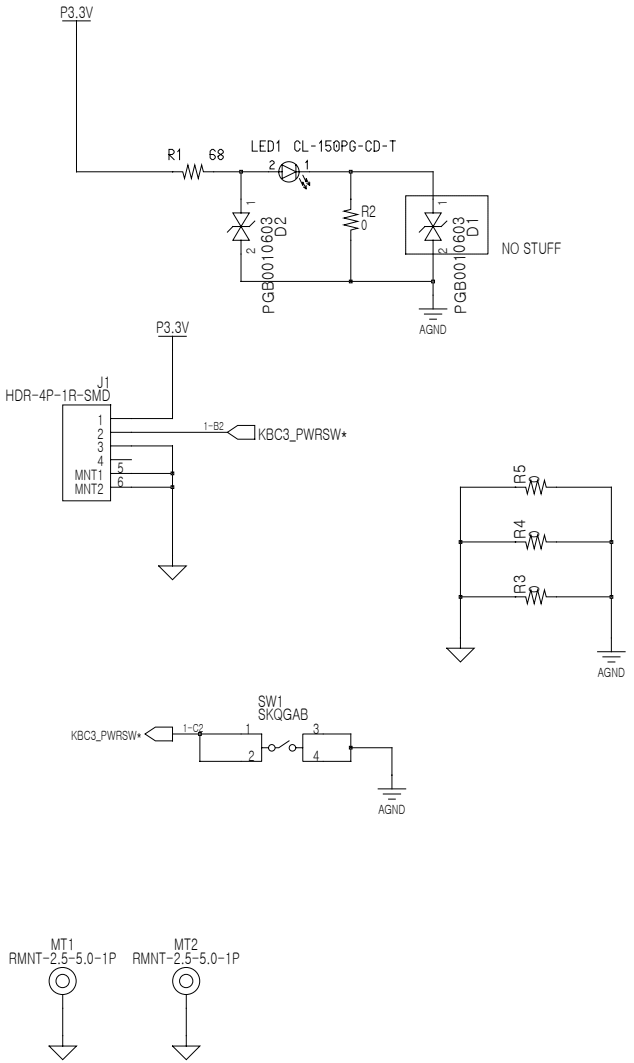
DRAW: PARK, RYAN	DATE: 12/3/2003	TITLE: CICHLID UNDEFINED ONTOP BOARD	SAMSUNG ELECTRONICS
CHECK: OH, H.S	DEV. STEP: DV		
APPROVAL: LEE, KEVIN	REV: 1.0		PART NO.: BA41-undefined
MODULE CODE:	LAST EDIT: December, 3, 2003 2:13:08 PM	PAGE 2 OF 2	

POWER SW BOARD

CPU : BANIAS/DOTHAN
Chip Set : ODEM+
Remarks :

Model Name : Power SW Board
PBA Name :
PCB Code : BA59-01336A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2004.01.28

DRAW	CHECK	APPROVAL



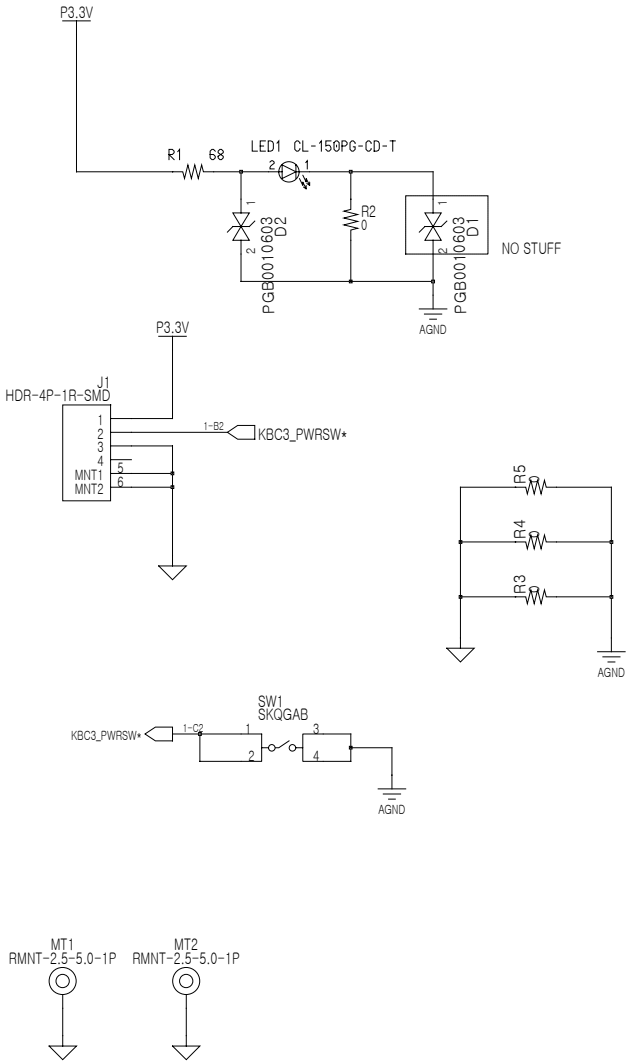
DRAW: PARK, RYAN	DATE: 12/4/2003	TITLE: CICHLID POWER BOARD POWER BOARD	SAMSUNG ELECTRONICS
CHECK: OH, H.S	DEV. STEP: DV		
APPROVAL: LEE, KEVIN	REV: 1.0		PART NO.: BA41-undefined
MODULE CODE:	LAST EDIT: December, 4, 2003 11:57:34 AM	PAGE 1 OF 1	

POWER SW BOARD

CPU : BANIAS/DOTHAN
Chip Set : ODEM+
Remarks :

Model Name : Power SW Board
PBA Name :
PCB Code : BA59-01336A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2004.01.28

DRAW	CHECK	APPROVAL



DRAW: PARK, RYAN	DATE: 12/4/2003	TITLE: CICHLID POWER BOARD POWER BOARD	SAMSUNG ELECTRONICS
CHECK: OH, H.S	DEV. STEP: DV		
APPROVAL: LEE, KEVIN	REV: 1.0		PART NO.: BA41-undefined
MODULE CODE:	LAST EDIT: December, 4, 2003 11:57:34 AM	PAGE 1 OF 1	

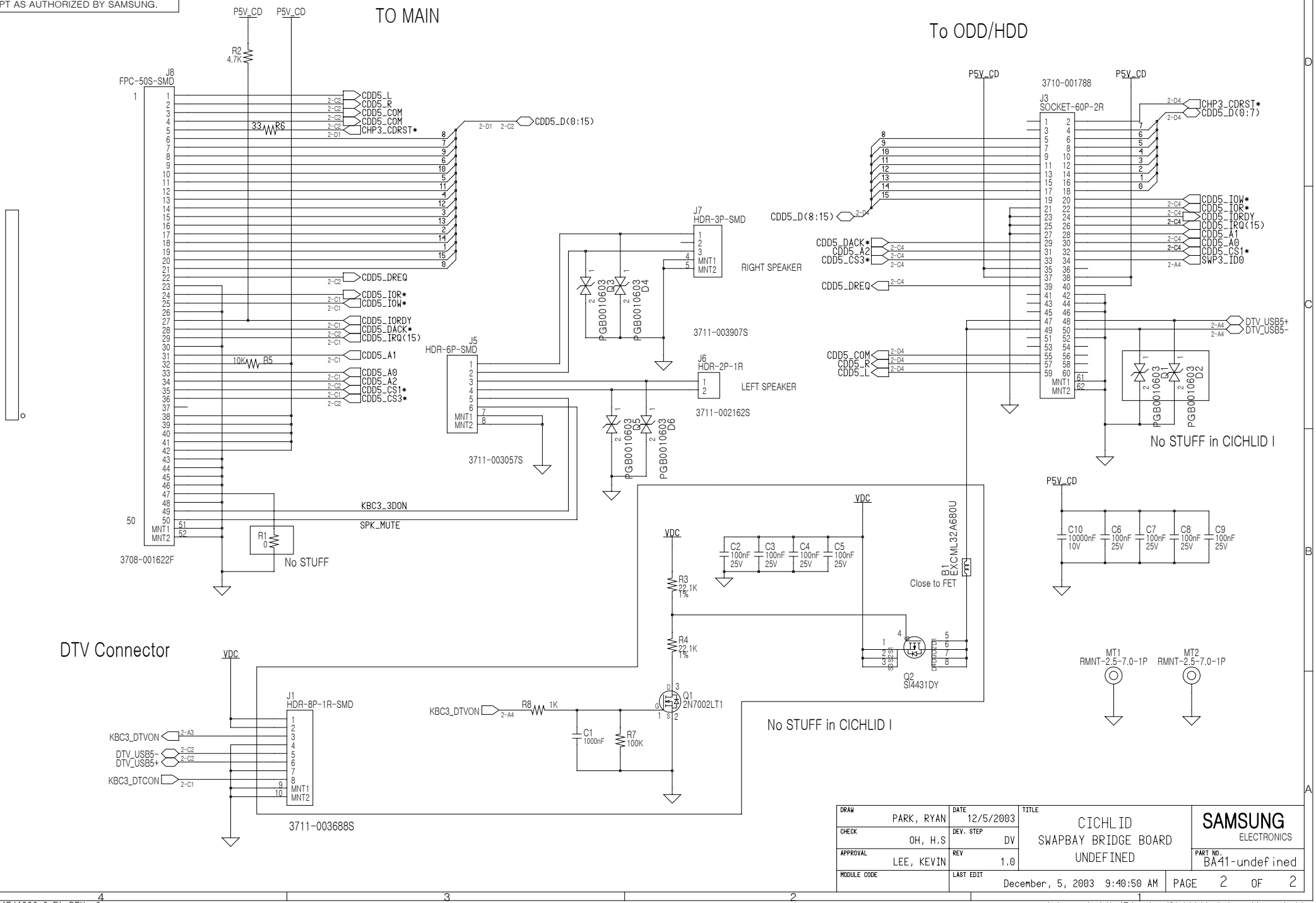
SWAPBAY BR. BOARD

CPU : BANIAS/DOTHAN
Chip Set : ODEM+
Remarks :

Model Name : SWAPBAY BR. BOARD
PBA Name :
PCB Code : BA59-01335A
Dev. Step : MP
Revision : 1.2
T.R. Date : 2004.04.01

DRAW	CHECK	APPROVAL

DRAW: PARK, RYAN	DATE: 12/5/2003	TITLE: CICHLID SWAPBAY BRIDGE BOARD	SAMSUNG ELECTRONICS
CHECK: OH, H.S	DEV. STEP: DV		
APPROVAL: LEE, KEVIN	REV: 1.0		PART NO.: BA41-
MODULE CODE:	LAST EDIT: December, 5, 2003 9:40:29 AM	PAGE 1 OF 2	



DRAW: PARK, RYAN	DATE: 12/5/2003	TITLE: CICHLID SWAPBAY BRIDGE BOARD UNDEFINED	SAMSUNG ELECTRONICS
CHECK: OH, H.S	DEV. STEP: DV		
APPROVAL: LEE, KEVIN	REV: 1.0		PART NO.: BA41-undefined
MODULE CODE:	LAST EDIT: December, 5, 2003 9:40:50 AM		PAGE 2 OF 2

TP19 ON$4406
TP20 ON$4407
TP21 ON$4408
TP22 OCDD5_L
TP23 OCDD5_R
TP24 ON$4411
TP25 ON$4412
TP26 ON$4413
TP27 ON$4414
TP28 ON$4415
TP29 ON$4416
TP30 ON$4417
TP31 ON$4418
TP32 ON$4419
TP33 OCDD5_A0
TP34 OCDD5_A1
TP35 OCDD5_A2
TP36 OCDD5_COM
TP37 OSPK_MUTE
TP38 OCDD5_CS1*
TP39 OCDD5_CS3*
TP40 OCDD5_D(0)
TP41 OCDD5_D(1)
TP42 OCDD5_D(2)
TP43 OCDD5_D(3)
TP44 OCDD5_D(4)
TP45 OCDD5_D(5)
TP46 OCDD5_D(6)
TP47 OCDD5_D(7)
TP48 OCDD5_D(8)
TP49 OCDD5_D(9)
TP50 OCDD5_DREQ
TP3 OCDD5_IOR*
TP4 OCDD5_IOW*
TP5 ODTV_USB5+
TP6 ODTV_USB5-
TP7 OKBC3_3DON
TP8 OCDD5_D(10)
TP9 OCDD5_D(11)
TP10 OCDD5_D(12)
TP11 OCDD5_D(13)
TP12 OCDD5_D(14)
TP13 OCDD5_D(15)
TP14 OCDD5_DACK*
TP15 OCDD5_IORDY
TP16 OKBC3_DTVON
TP17 OCHP3_CDRST*
TP18 OCDD5_IRQ(15)
TP1 OP5V_CD
TP2 OVDC

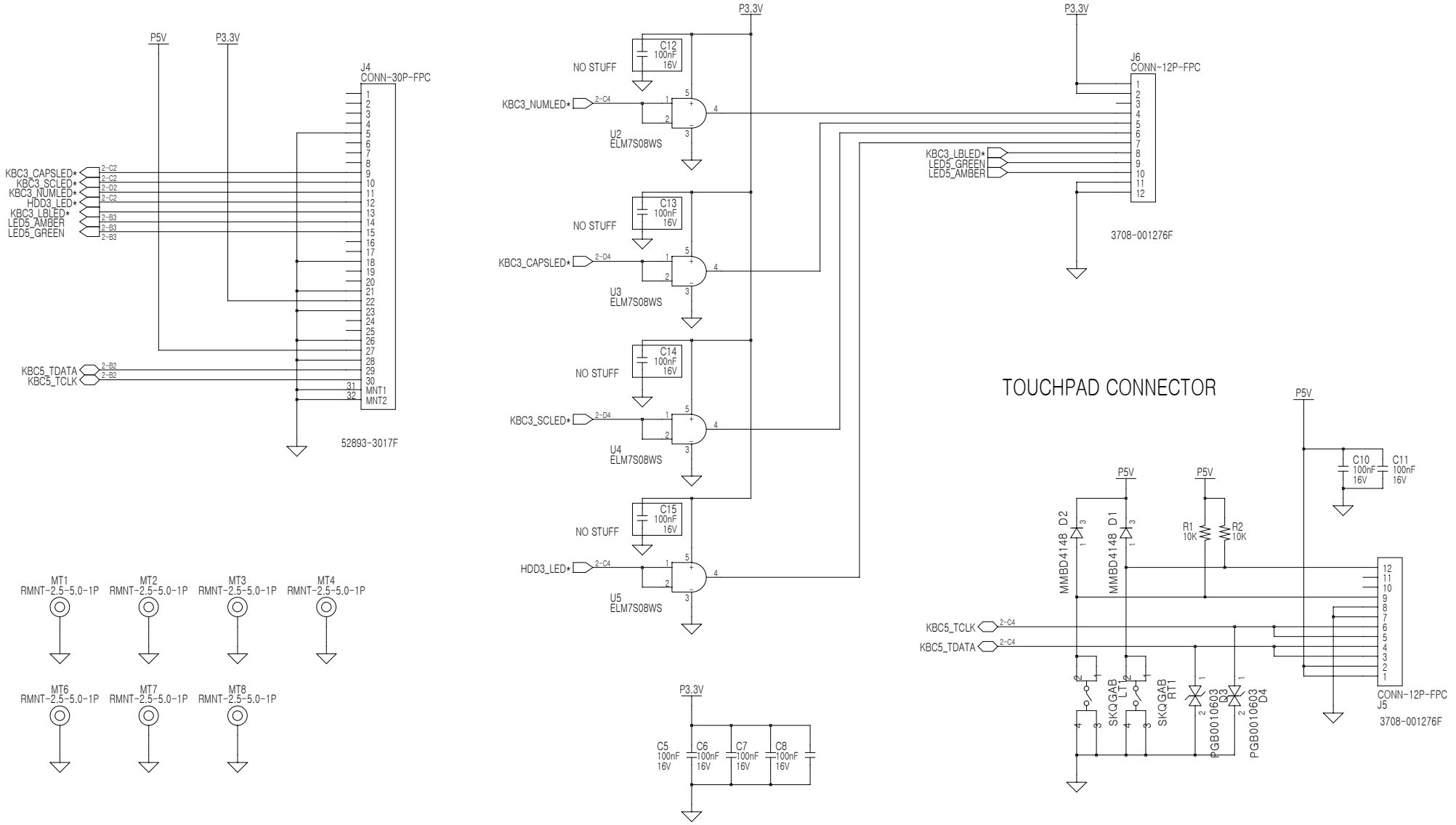
CICHLID

CPU : BANIAS/DOTHAN
Chip Set : ODEM+
Remarks :

Model Name : TOUCHPAD I/F BOARD
PBA Name :
PCB Code : BA59-01329A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2004. 2. 28

DRAW	CHECK	APPROVAL

DRAW: PARK, RYAN	DATE: 12/2/2003	TITLE: CICHLID TOUCHPAD I/F BOARD	SAMSUNG ELECTRONICS
CHECK: OH, H.S	DEV. STEP: DV		
APPROVAL: LEE, KEVIN	REV: 1.0		PART NO.: BA41-
MODULE CODE:	LAST EDIT: December, 2, 2003 1:43:54 PM	PAGE 1 OF 2	



DRAW: PARK, RYAN	DATE: 12/2/2003	TITLE: CICHLID TOUCHPAD I/F BOARD UNDEFINED	SAMSUNG ELECTRONICS
CHECK: OH, H.S	DEV. STEP: DV		
APPROVAL: LEE, KEVIN	REV: 1.0		PART NO.: BA41-undefined
MODULE CODE:	LAST EDIT: December, 2, 2003 1:44:53 PM	PAGE 2 OF 2	