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SAMOA(DDR3)

CPU : PENRYN SFF
Chip Set : CANTIGA GS & ICH9M SFF
Remarks : INTEL MONTEVINA SFF

Model Name : SAMOA
PCB Part No : BA41-00905A(Nanya)
BA41-00906A(GCE)
Dev. Step : PR/MP
Revision : 1.1
T.R. Date :

DRAW	CHECK	APPROVAL
Jun PARK	HJ KIM	JS EUH

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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN COVER	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 1 OF 44	

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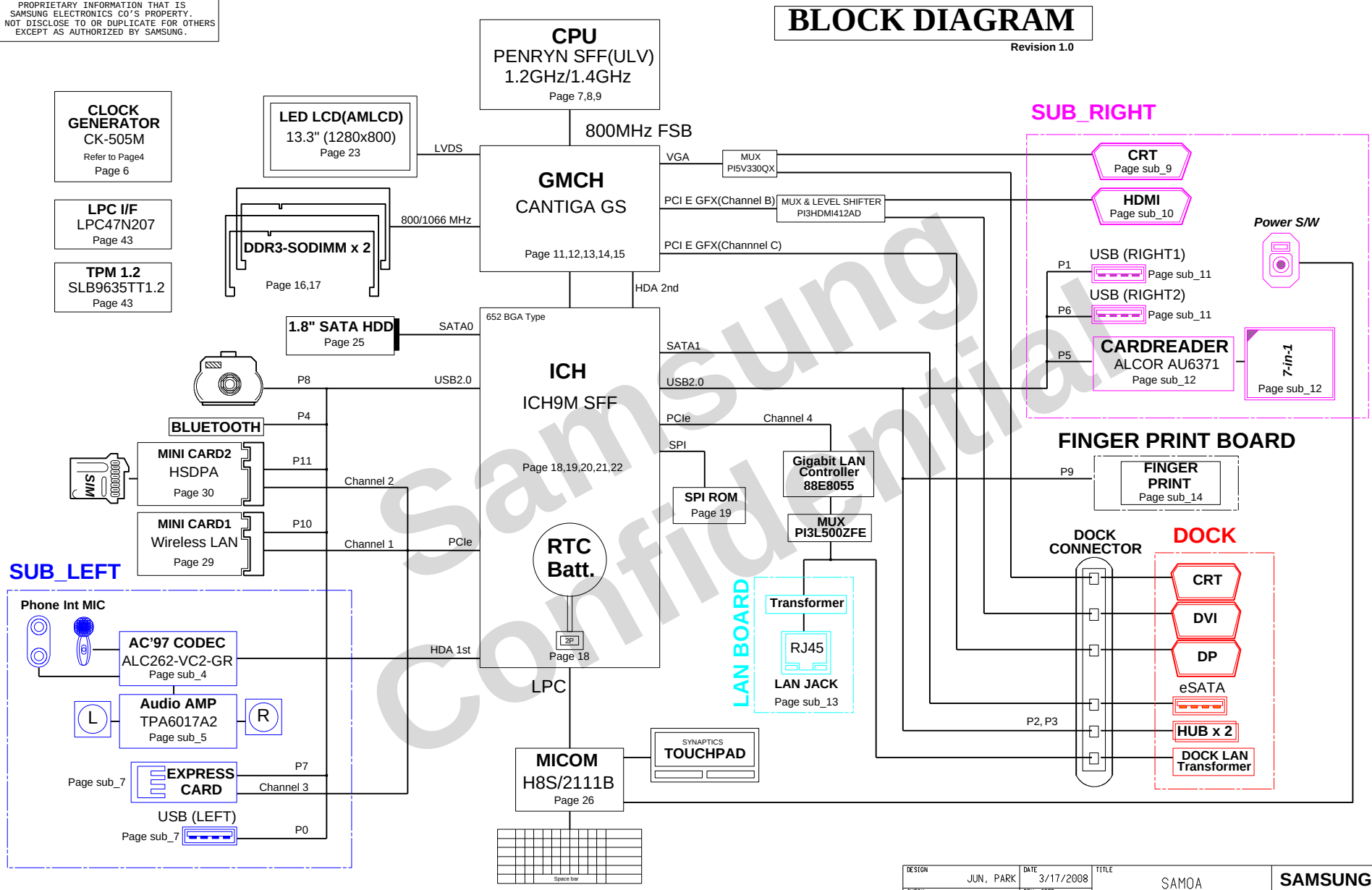
BLOCK DIAGRAM

Revision 1.0



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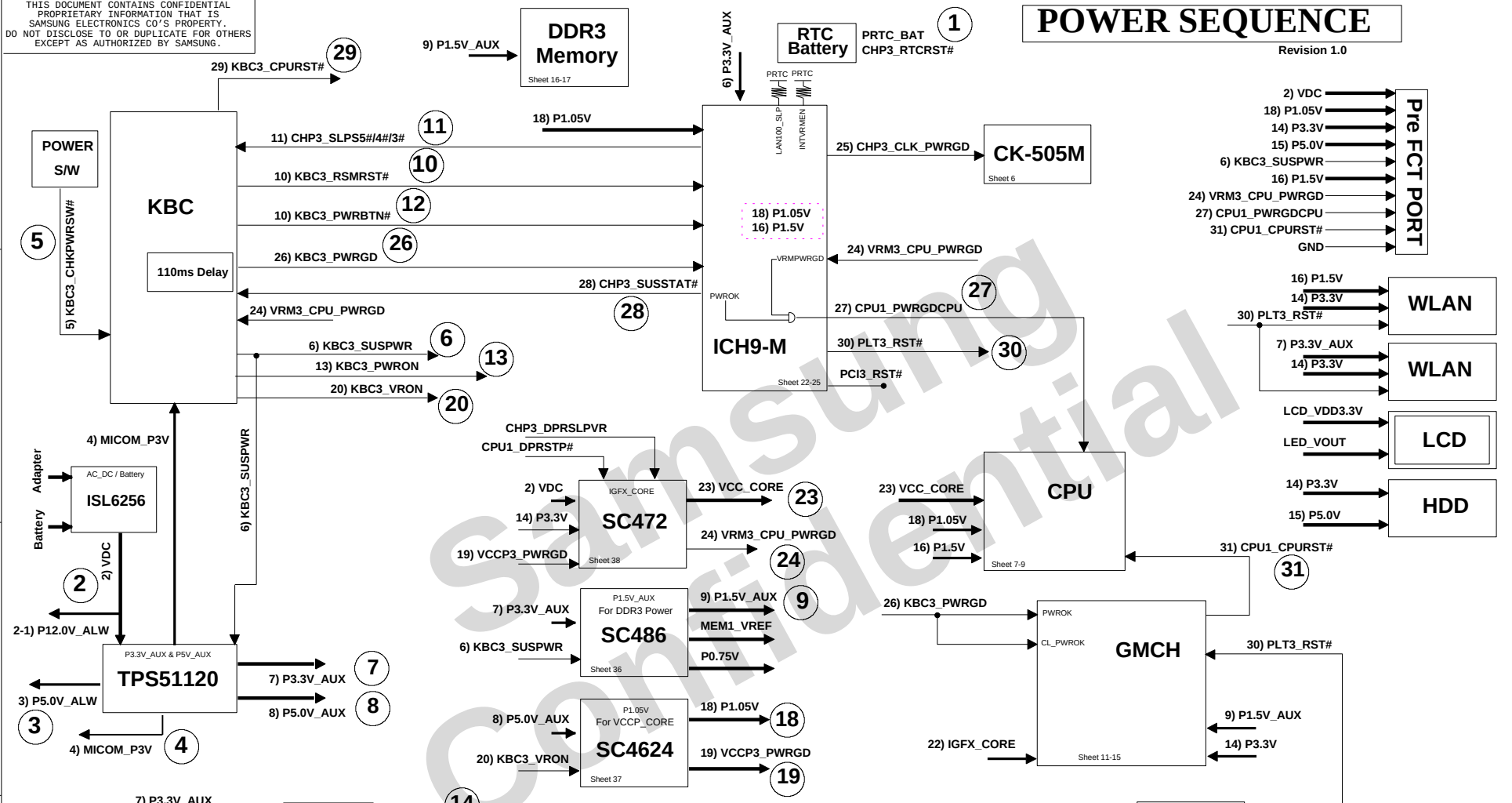
POWER SEQUENCE

Revision 1.0



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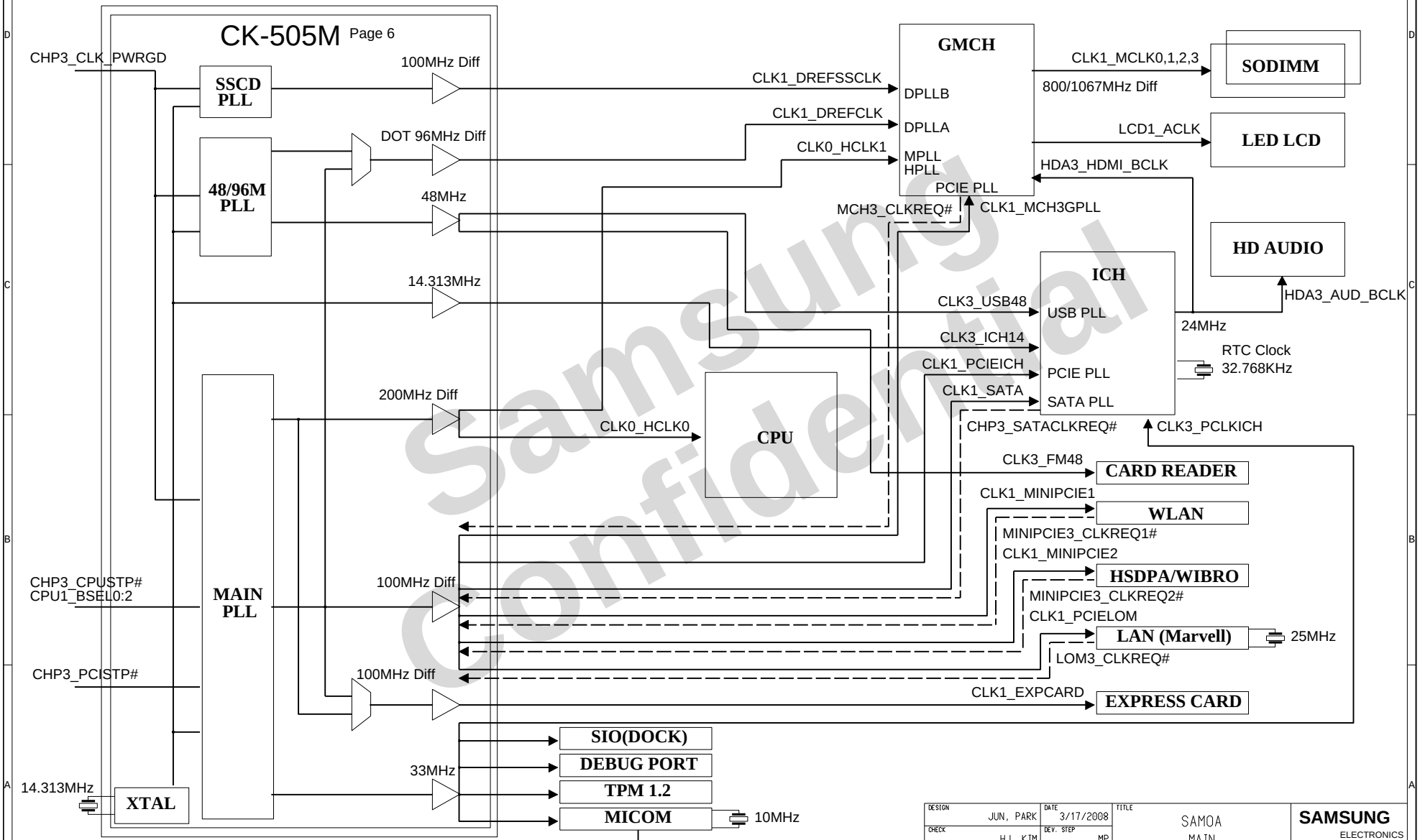
CLOCK DISTRIBUTION

Revision 1.0



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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
USB	AD29(internal)	Programable	
LPC Bridge/IDE/AC97/SMBUS	AD31(internal)		
Internal MAC	AD24(internal)		

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9M	**Master**		**SMBUS Master**
CK-505M (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000X	A0h	-
SODIMM1	1010 001X	A4h	
PI3HDMI412AD	1010 001X	C0h	
MICOM	**Master**		-
			-
BATTERY	0001 011X	16h	
EMC2102	0111 101X	7Ah	

USB PORT Assign

Port Number		ASSIGNED TO	Port Number		ASSIGNED TO
UHCI_0	0	USB PORT (LEFT)	UHCI_3	6	USB PROT (RIGHT2)
	1	USB PORT (RIGHT1)		7	EXPRESS CARD
UHCI_1	2	USB HUB1 (DOCK)	UHCI_4	8	CAMERA
	3	USB HUB2 (DOCK)		9	FINGER PRINT
UHCI_2	4	BLUETOOTH	UHCI_5	10	WLAN for Combo
	5	AU6371		11	HSDPA

System Power States

Power Rail	Devices (Page Number)
P5.0V	EMC2102 (10) ICH9M (21) 1.8" SATA HDD (25) MICOM (26) Pre FCT PORT (32) DISCHARGE, CAMERA, TOUCHPAD (33) SC472 (38) SC454 (39) AP6680 (41) PI5V330QX (24,42) HDMI CONN. (SUB_10) CRT CONN. (SUB_9)
P3.3V	CK505M (6) FAN (10) CANTIGA GS (14) SPI ROM (19) ICH9M (21) LED LCD (23) 1.8" SATA HDD (25) WLAN (29) HSDPA (30) PI3HDMI412AD (31) Pre FCT PORT (32) DEBUG PORT, Pre FCT PORT & WHITE LED (32) DISCHARGE & BLUETOOTH (33) SWITCHED (41) LPC47N207 (43) ALC262-VC2 (SUB_4) R5538 (SUB_7) POWER S/W LED (SUB_11) AU6371 (SUB_12) AES1610 (SUB_14)
P1.8V	CANTIGA GS (14) DISCHARGE (33) SWITCHED (41)
P1.5V	CK505M (6) PENRYN ULV (8) CANTIGA GS (14) ICH9M (21) WLAN (29) HSDPA (30) Pre FCT PORT (32) DISCHARGE (33) SWITCHED (41) ALC262-VC2 (SUB_4) R5538 (SUB_7)
P1.05V	PENRYN ULV (8) CANTIGA GS (11,14) ICH9M (21) Pre FCT PORT (32) DISCHARGE (33) SC4624 (37)
P0.75V	DDR3 (16, 17) SC486 (36)
P5V_AUX	ICH9M (21) TPS51120 (35) SC486 (36) SC4624 (37) SWITCHED (41) USB PORT (7,11)
P3.3V_AUX	EMC2102 (10) ICH9M (21) 88E8055 (27) STMUX1000 (28) WLAN (29) LAN JACK LED (32) TPS51120 (35) SWITCHED (41) SLB9635 (43) R5538 (SUB_7)
P1.5V_AUX	CANTIGA GS (14) DDR3 (16, 17) ICH9M (21) SC486 (36) SWITCHED (41)
VCC_CORE	PENRYN ULV (8,9) SC454 (39)
VCC_CORE	CANTIGA GS (12)

Voltage Rails

Power Rail	Descriptions
AD_DC ***VDC***	Primary DC system power supply (9 to 19V)
CHG_REF	Charger Reference Voltage Source
PRTC_BAT	3.3V supply for the RTC well.
P5.0V_FILT	???
P12.0V_ALW	???
P5.0V_ALW	???
MICOM_P3V	Output voltage of ISL6256(Charger) (if VDC is removed, it will be off)
LCD_VDD3V	3.3V (LED LCD)
LED VOUT	7V-19V (LED LCD)
VDC_LED	VDC (LED LCD)
P5.0V_CRT	5.0V (CRT Conn.)
VCC_CRT	5.0V (CRT)
P1.2V_LAN ***P1.8V_P2.5V_LAN***	Internal Regulator's Power of LAN Controller
P3.3V_MCD	3.3V (7-in-1 Socket)

Power Rail	Descriptions
P1.05V_PEG	P1.05V (Direct Media Interface Compensation)
P5.0V	5.0V Power Rail (off in S3-S5)
P3.3V	3.3V Power Rail (off in S3-S5)
P1.8V	1.8V Power Rail (off in S3-S5)
P1.5V	1.5V Power Rail (off in S3-S5)
P1.05	1.05V Power Rail (off in S3-S5)
P0.75V	DDR3 Termination
P5.0V_AUX	5.0V Power Rail (off in S4-S5)
P3.3V_AUX	3.3V Power Rail (off in S4-S5)
P1.5_AUX	1.5V Power Rail (off in S4-S5)
VCC_CORE	Core Voltage for PENRYN ULV
IGFX_CORE	Core Voltage for CANTIGA GS
AUD_P5V	5.0V switched power rail (off in S3-S5)
AMP_VDD	5.0V (Audio AMP)
AVDD	5.0V (ADI1986)
P1.5V_EXT	1.5V (R5538, EXPRESS CARD)
P3.3V_AUX_EXT ***P3.3V_EXT***	3.3V (R5538, EXPRESS CARD)
3.3V_VDD	3.3V (AES1610, FINGER PRINT)
FP_P3.3V	3.3V (AES1610, FINGER PRINT)

GMCH Core Voltage

	EN	V4	V3	V2	V1	V0	Voltage
Render Performance States	1	0	0	0	0	0	1.250
	1	0	0	0	0	1	1.225
	1	0	0	0	1	0	1.200
	1	0	0	0	1	1	1.175
	1	0	0	1	0	0	1.150
	1	0	0	1	0	1	1.125
	1	0	0	1	1	0	1.100
	1	0	0	1	1	1	1.075
	1	0	1	0	0	0	1.050
	1	0	1	0	0	1	1.025
	1	0	1	0	1	0	1.000
	1	0	1	0	1	1	0.975
	1	0	1	1	0	0	0.950
	1	0	1	1	0	1	0.925
	1	0	1	1	1	0	0.900
	1	0	1	1	1	1	0.875
	1	1	0	0	0	0	0.850
	1	1	0	0	0	1	0.825
Render Suspend States	1	1	0	0	1	0	0.800
	1	1	0	0	1	1	0.775
	1	1	0	1	0	0	0.750
	1	1	0	1	0	1	0.725
	1	1	0	1	1	0	0.700
	1	1	0	1	1	1	0.675
	1	1	1	0	0	0	0.650
	1	1	1	0	0	1	0.625
	1	1	1	0	1	0	0.600
	1	1	1	0	1	1	0.575
	1	1	1	1	0	0	0.550
	1	1	1	1	0	1	0.525
	1	1	1	1	1	0	0.500
	1	1	1	1	1	1	0.400
	0	X	X	X	X	X	0.000

CPU Core Voltage Table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500
0	0	1	0	1	0	1	1.2375
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125

Active Mode

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125

Active / Deeper Sleep Dual Mode

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000

Deeprer Sleep / Deep Power Down Mode

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000

Programmable Deep Power Down

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000

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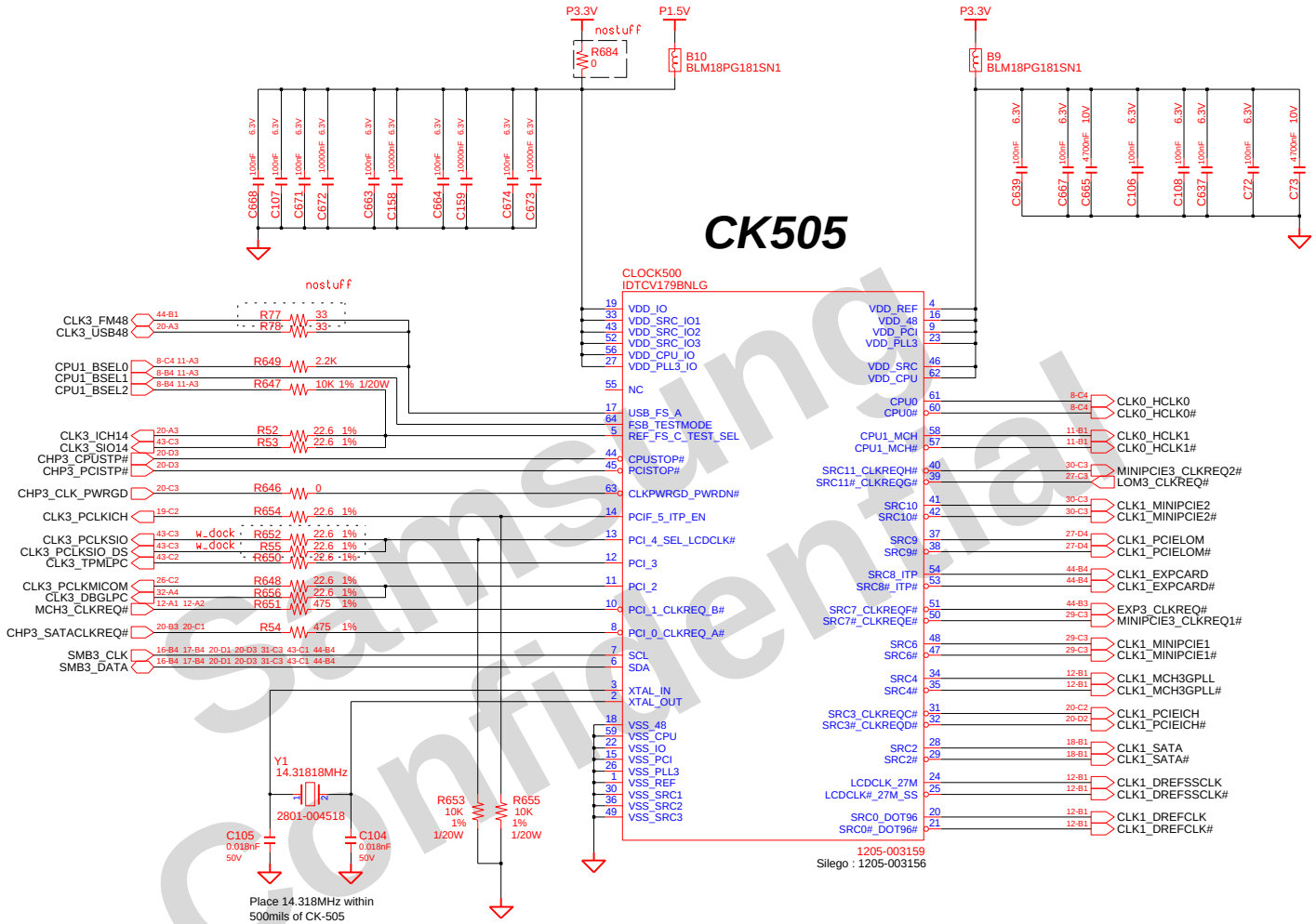
FSC BSEL2	FSB BSEL1	FSA BSEL0	HOST CLK
0	0	0	266 MHz
0	0	1	RSVD
0	1	0	200 MHz
0	1	1	166 MHz
1	0	0	RSVD
1	0	1	RSVD
1	1	0	RSVD
1	1	1	RSVD



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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS
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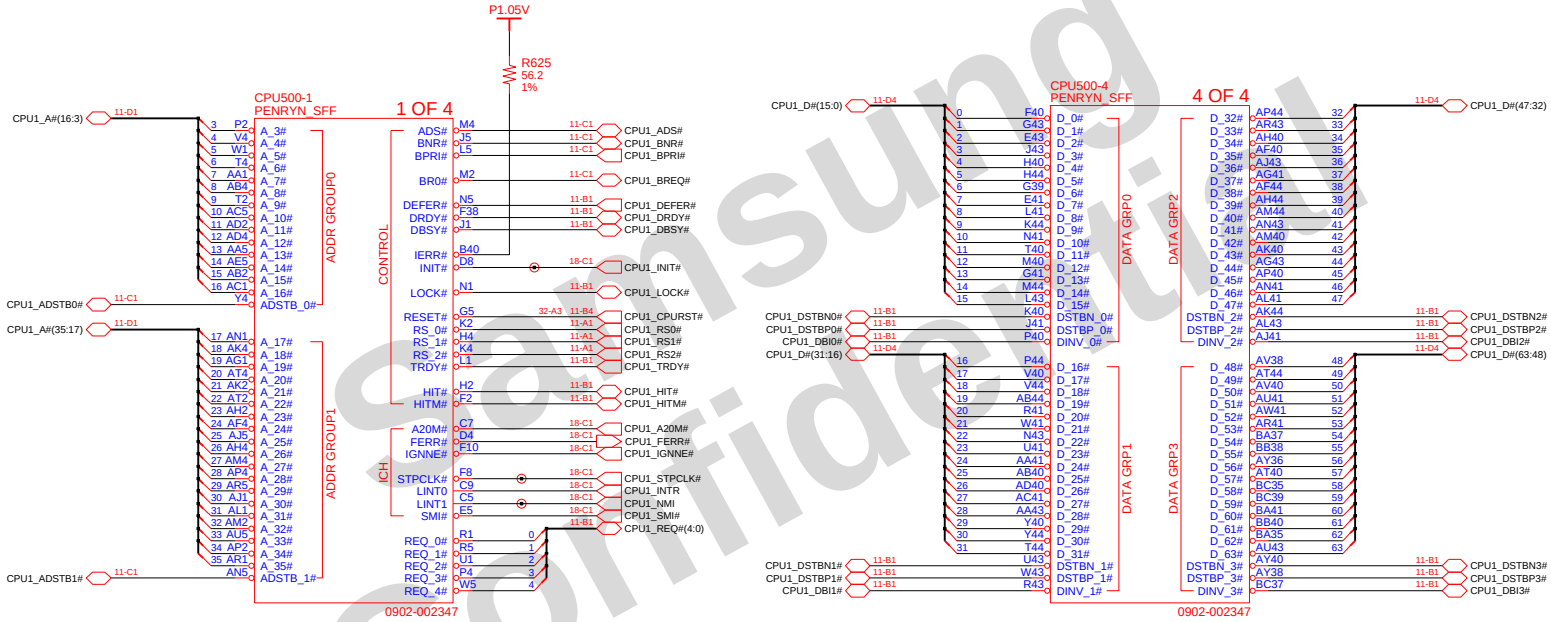
ULV CPU(Penryn SFF)



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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN PENRYN ULV CPU(1/3)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		PART NO. BA41-0XXXXA
APPROVAL: JS , EUH	REV: 1.1		
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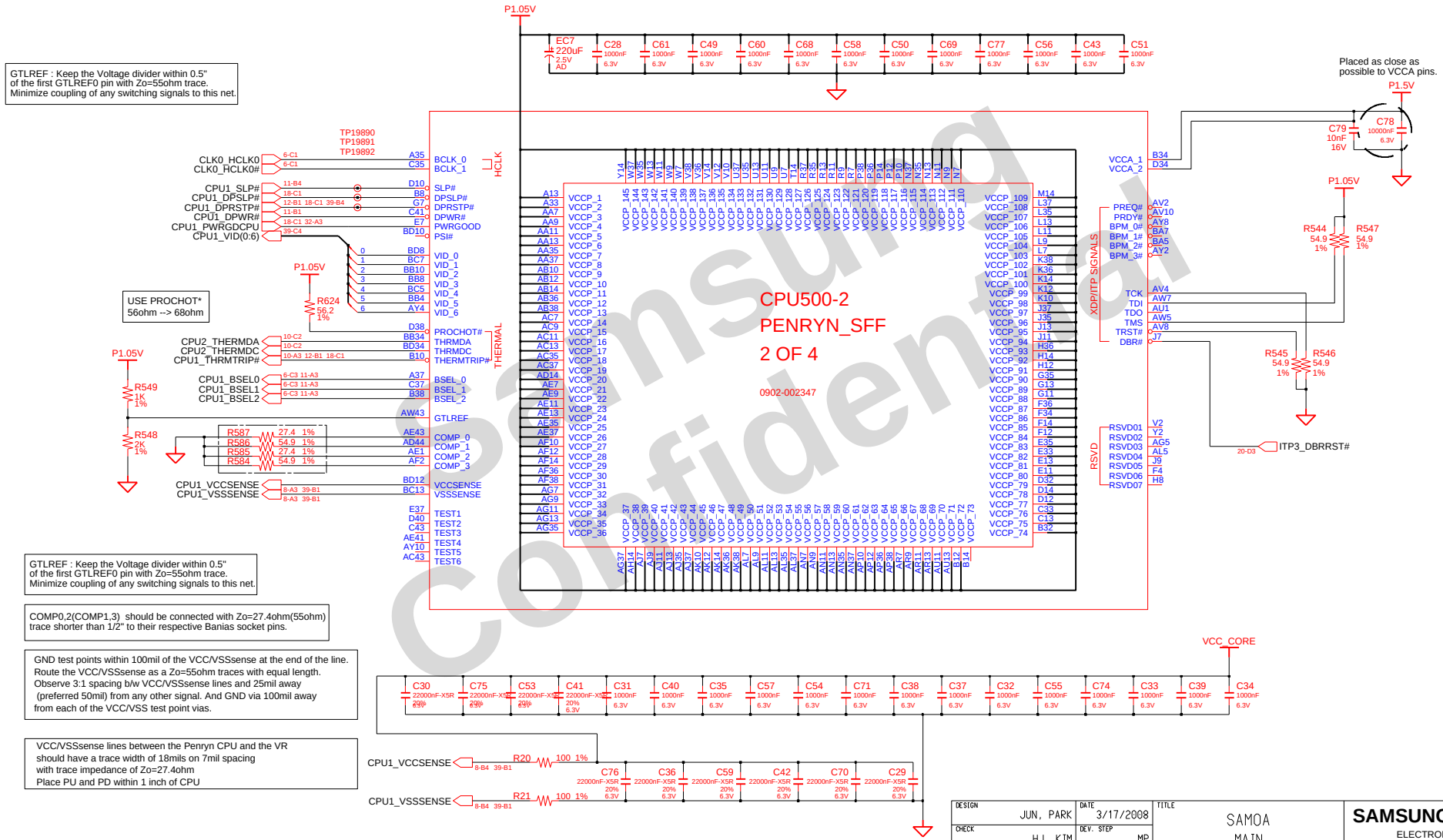
ULV CPU(Penryn SFF)



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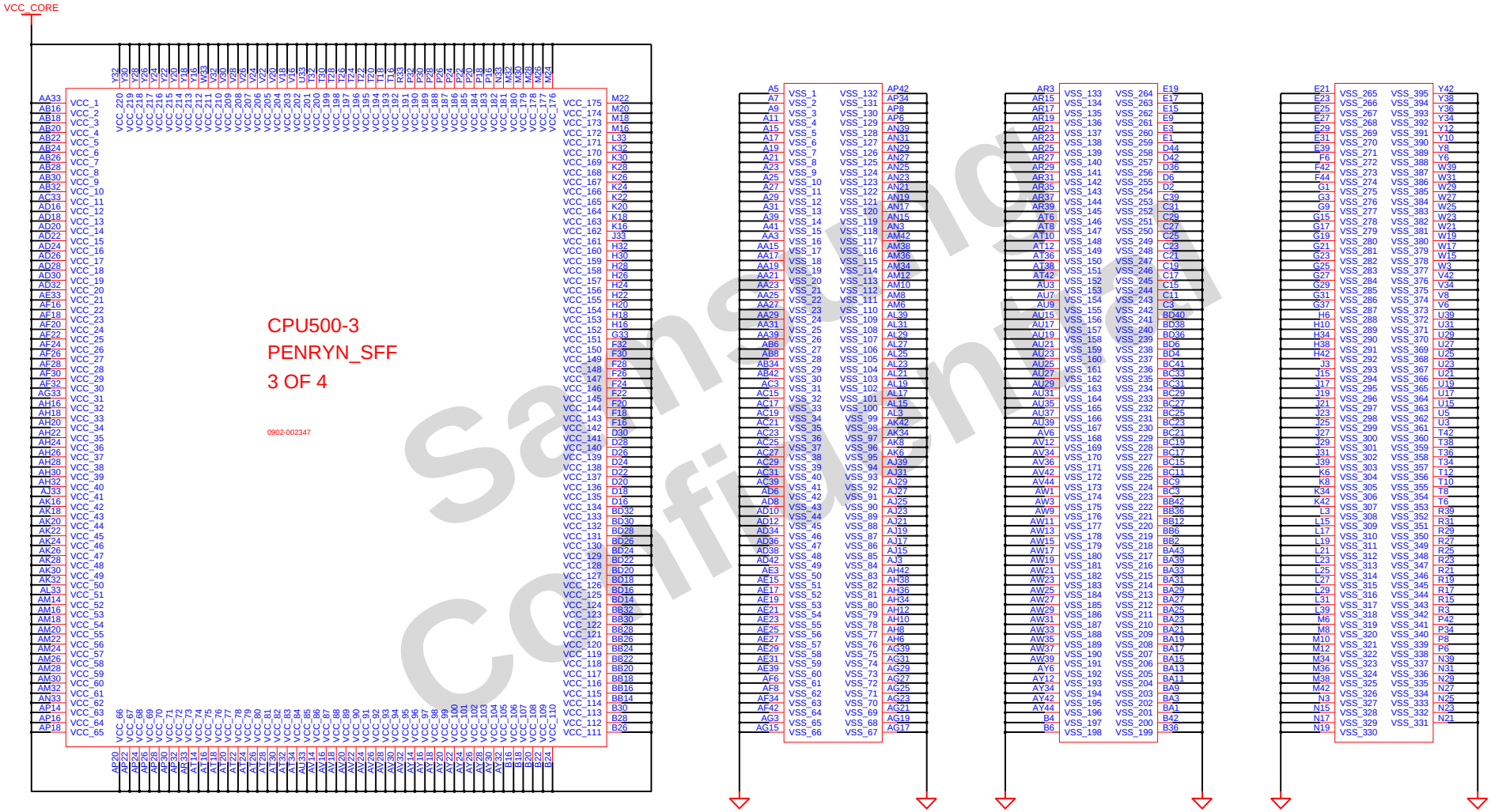
ULV CPU(Penryn SFF)



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CHECK: HJ, KIM	DEV. STEP: MP		
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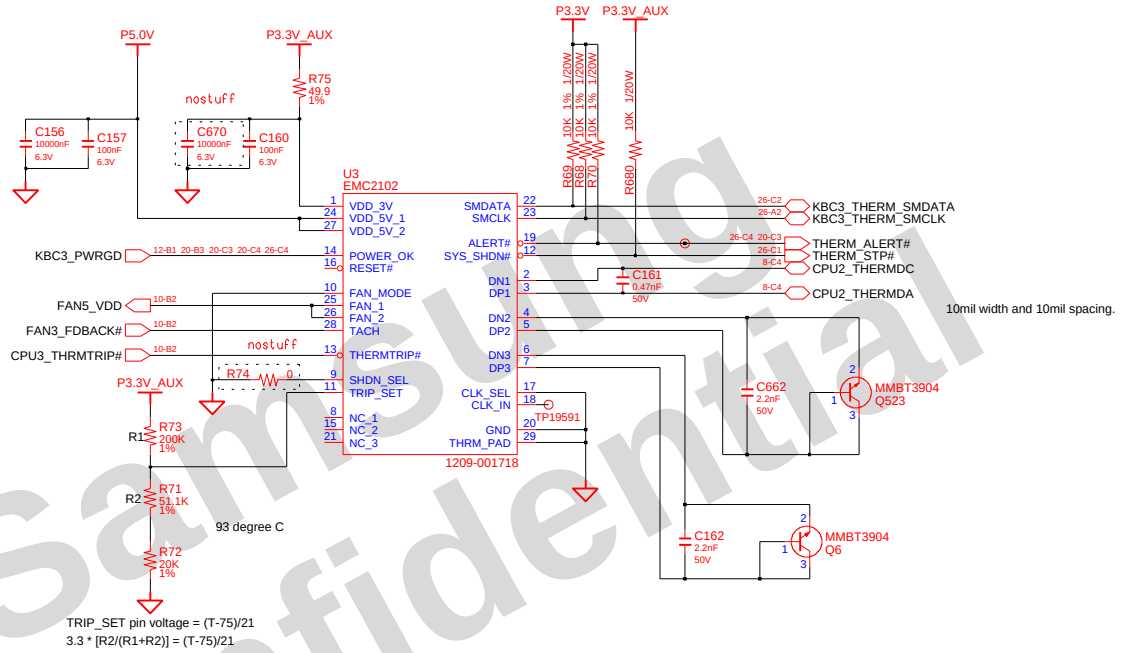
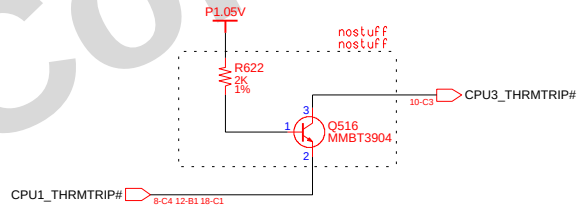
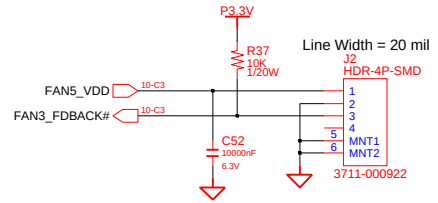
THERMAL MONITOR



FAN MODE	
0	0% Drive
Open	60% drive after spin up routine
1	75% drive after spin up routine

SHDN_SEL	
0	Intel Mode
High-Z	Diode Mode
1	Disabled





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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN THERMAL MONITOR	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM		PAGE 10 OF 44

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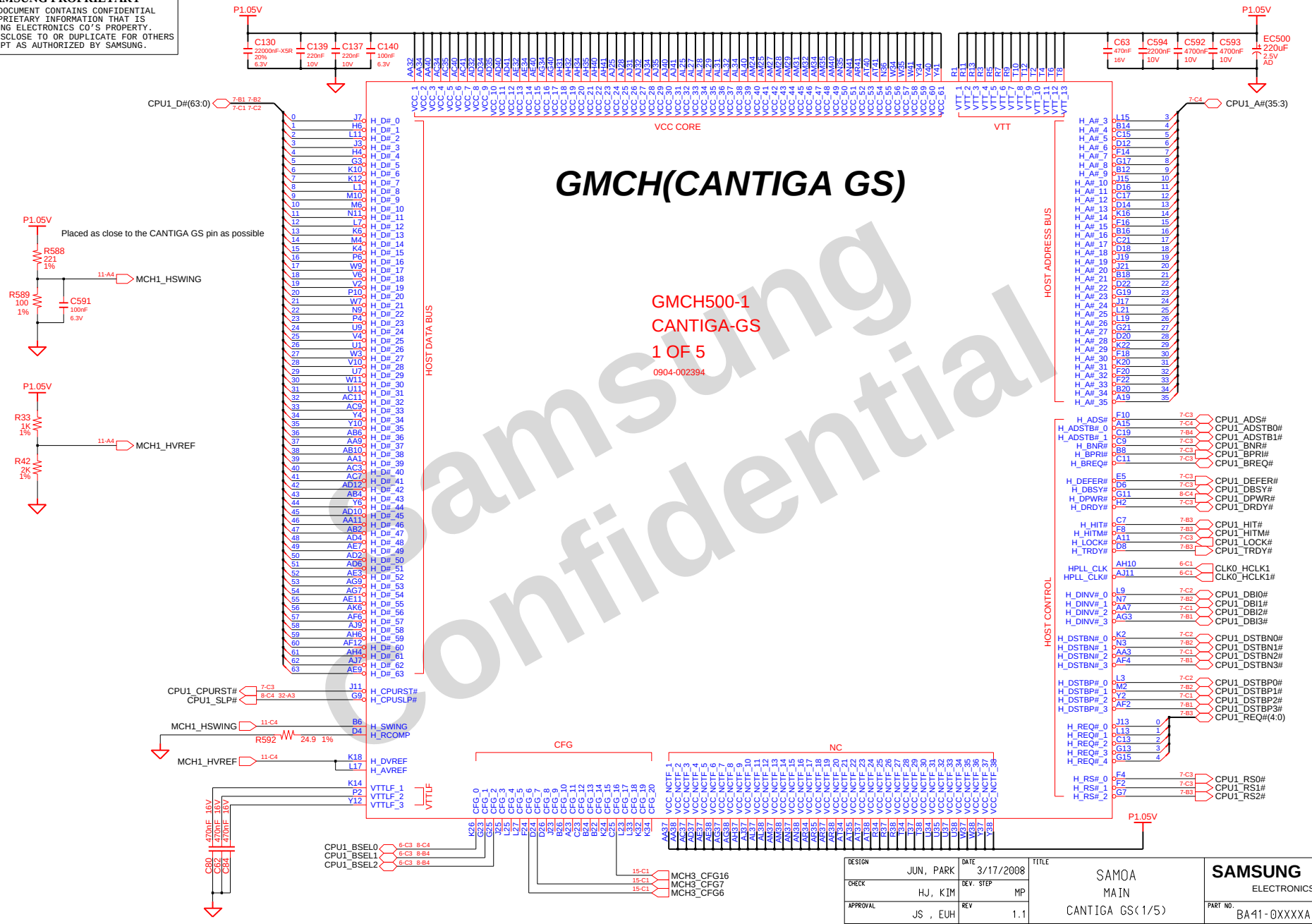
GMCH(CANTIGA GS)

GMCH500-1
CANTIGA-GS
1 OF 5
0904-002394



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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN CANTIGA GS(1/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		PART NO. BA41-0XXXXA
APPROVAL: JS , EUH	REV: 1.1		
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM		PAGE 11 OF 44

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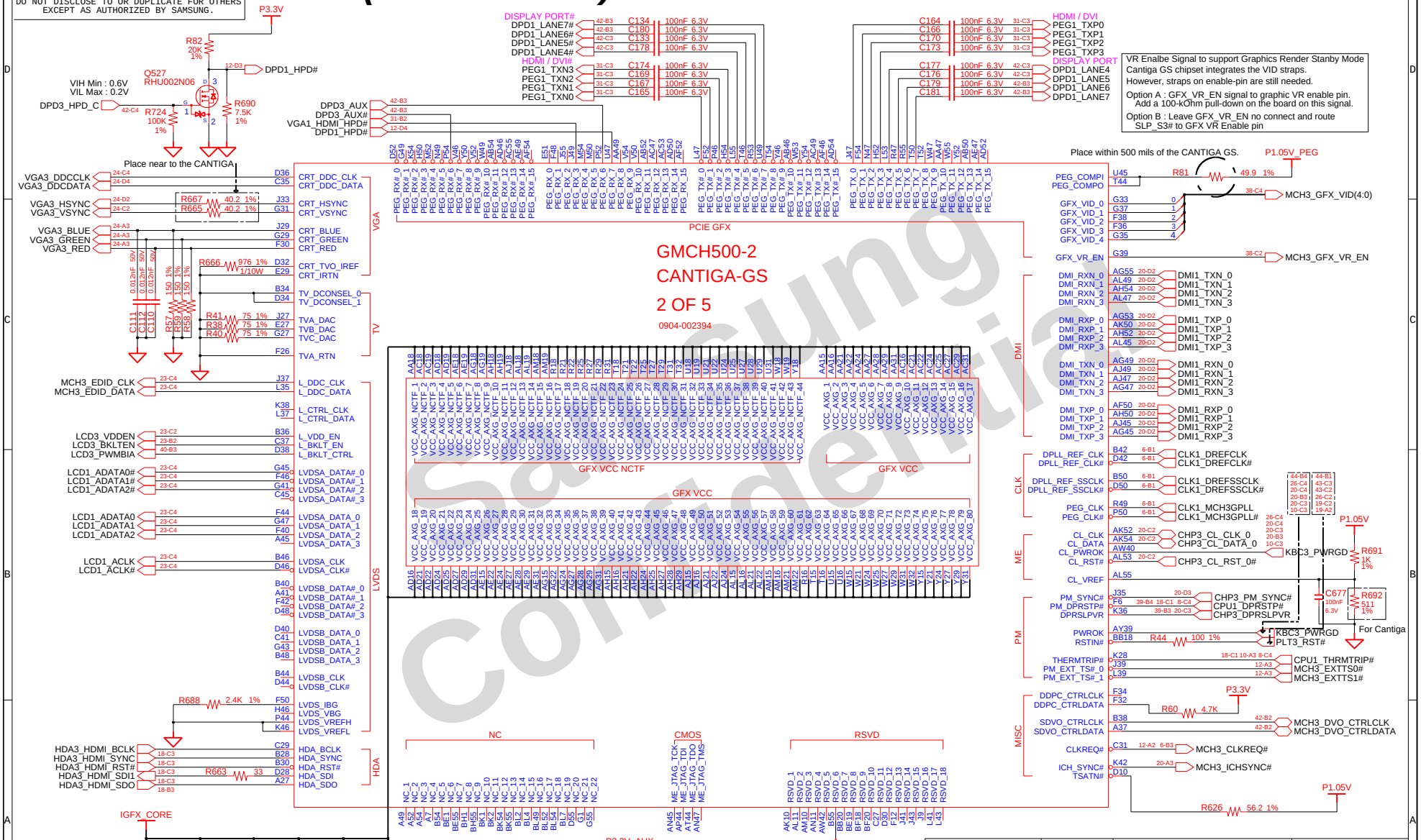
GMCH(CANTIGA GS)



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DESIGN JUN, PARK	DATE 3/17/2008	TITLE SAMOA MAIN CANTIGS GS(2/5)	SAMSUNG ELECTRONICS
CHECK HJ, KIM	DEV. STEP MP		PART NO. BA41-0XXXXA
APPROVAL JS , EUH	REV 1.1		
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GMCH(CANTIGA GS)

GMCH500-3
CANTIGA-GS
3 OF 5
0904-002394

SM_DRAMRST#	Leave as NC in DDR2 mode. Used only in DDR3 mode.
SM_PWROK	Connect to GND in DDR2 mode.

PLACE EACH CAP NEAR BC51 PIN

C184 100nF 6.3V, C183 100nF 6.3V — nostuff

R45 499 1%

MEM1_VREF

MEM1_ADQ(63:0) — SYSTEM MEMORY A

MEM1_ABS(2:0): SA_BS_0, SA_BS_1, SA_BS_2

MEM1_ADM(7:0): SA_DM_0, SA_DM_1, SA_DM_2, SA_DM_3, SA_DM_4, SA_DM_5, SA_DM_6, SA_DM_7

MEM1_ADQS#(7:0): SA_DQS#_0, SA_DQS#_1, SA_DQS#_2, SA_DQS#_3, SA_DQS#_4, SA_DQS#_5, SA_DQS#_6, SA_DQS#_7

MEM1_ADQS(7:0): SA_DQS_0, SA_DQS_1, SA_DQS_2, SA_DQS_3, SA_DQS_4, SA_DQS_5, SA_DQS_6, SA_DQS_7

MEM1_AMA(14:0): SA_MA_0, SA_MA_1, SA_MA_2, SA_MA_3, SA_MA_4, SA_MA_5, SA_MA_6, SA_MA_7, SA_MA_8, SA_MA_9, SA_MA_10, SA_MA_11, SA_MA_12, SA_MA_13, SA_MA_14

MEM1_ACAS# — SA_CAS#
MEM1_ARAS# — SA_RAS#
MEM1_AWE# — SA_WE#
MEM1_CS0# — SA_CS#_0
MEM1_CS1# — SA_CS#_1
MEM1_ODT0 — SA_ODT_0
MEM1_ODT1 — SA_ODT_1
MEM1_CKE0 — SA_CKE_0
MEM1_CKE1 — SA_CKE_1
CLK1_MCLK0 — SA_CK_0
CLK1_MCLK0# — SA_CK#_0
CLK1_MCLK1 — SA_CK_1
CLK1_MCLK1# — SA_CK#_1

SM_RCOMP
SM_RCOMP#
SM_RCOMP_VOH
SM_RCOMP_VOL

SM_REXT — BH20
SM_VREF — BC51
SM_DRAMRST# — BA37 — MCH3_DDR_RST#
SM_PWROK — AY37 — VRM3_DDR_PWRGD

SB_CAS# — BH14 — MEM1_BCAS#
SB_RAS# — BE21 — MEM1_BRAS#
SB_WE# — BK14 — MEM1_BWE#
SB_CS#_0 — BE23 — MEM1_CS2#
SB_CS#_1 — BC19 — MEM1_CS3#
SB_ODT_0 — BC17 — MEM1_ODT2
SB_ODT_1 — BE17 — MEM1_ODT3
SB_CKE_0 — BE37 — MEM1_CKE2
SB_CKE_1 — BC37 — MEM1_CKE3
SB_CK_0 — BA33 — CLK1_MCLK2
SB_CK#_0 — BC33 — CLK1_MCLK2#
SB_CK_1 — BA23 — CLK1_MCLK3
SB_CK#_1 — BB24 — CLK1_MCLK3#

SYSTEM MEMORY B

MEM1_BDM(7:0): SB_DM_0, SB_DM_1, SB_DM_2, SB_DM_3, SB_DM_4, SB_DM_5, SB_DM_6, SB_DM_7

MEM1_BDQS#(7:0): SB_DQS#_0, SB_DQS#_1, SB_DQS#_2, SB_DQS#_3, SB_DQS#_4, SB_DQS#_5, SB_DQS#_6, SB_DQS#_7

MEM1_BDQS(7:0): SB_DQS_0, SB_DQS_1, SB_DQS_2, SB_DQS_3, SB_DQS_4, SB_DQS_5, SB_DQS_6, SB_DQS_7

MEM1_BMA(14:0): SB_MA_0, SB_MA_1, SB_MA_2, SB_MA_3, SB_MA_4, SB_MA_5, SB_MA_6, SB_MA_7, SB_MA_8, SB_MA_9, SB_MA_10, SB_MA_11, SB_MA_12, SB_MA_13, SB_MA_14

MEM1_BBS(2:0): SB_BS_0, SB_BS_1, SB_BS_2

MEM1_BDQ(63:0)

P1.5V_AUX
R628 80.6 1%
R43 80.6 1%
R673 1K 1%
R671 3.01K 1%
R672 1K 1%
C642 10nF 16V
C644 2200nF 10V
C645 10nF 16V
C646 2200nF 10V

Cantiga
SM_RCOMP : 80 ohm to P1.5V_AUX
SM_RCOMP# : 80 ohm to VSS
P1.8V_AUX FOR DDR2

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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN CANTIGS GS(3/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		PART NO. BA41-0XXXXA
APPROVAL: JS , EUH	REV: 1.1		
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM		PAGE 13 OF 44

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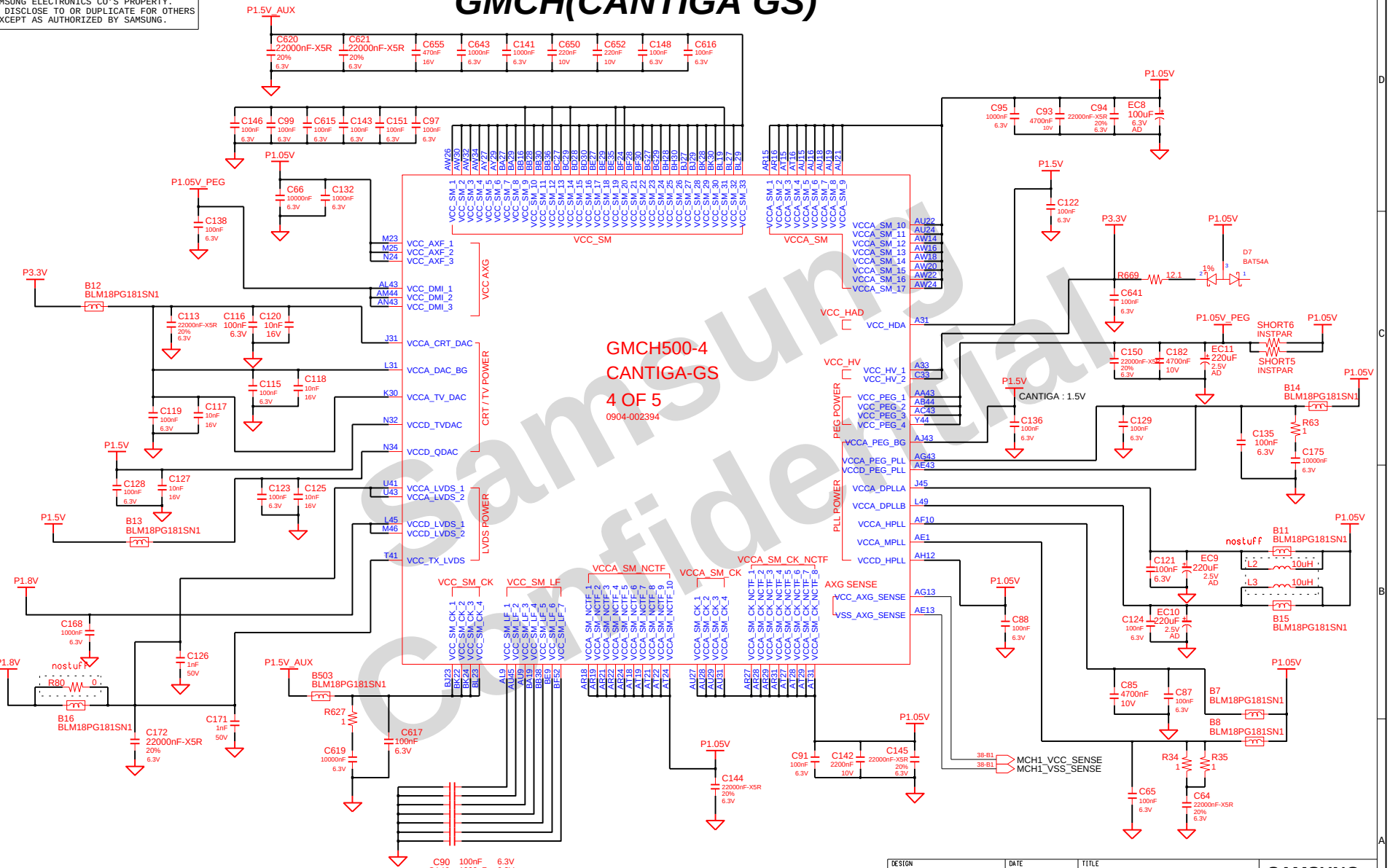
GMCH(CANTIGA GS)



DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN CANTIGA GS(4/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM		PAGE 14 OF 44

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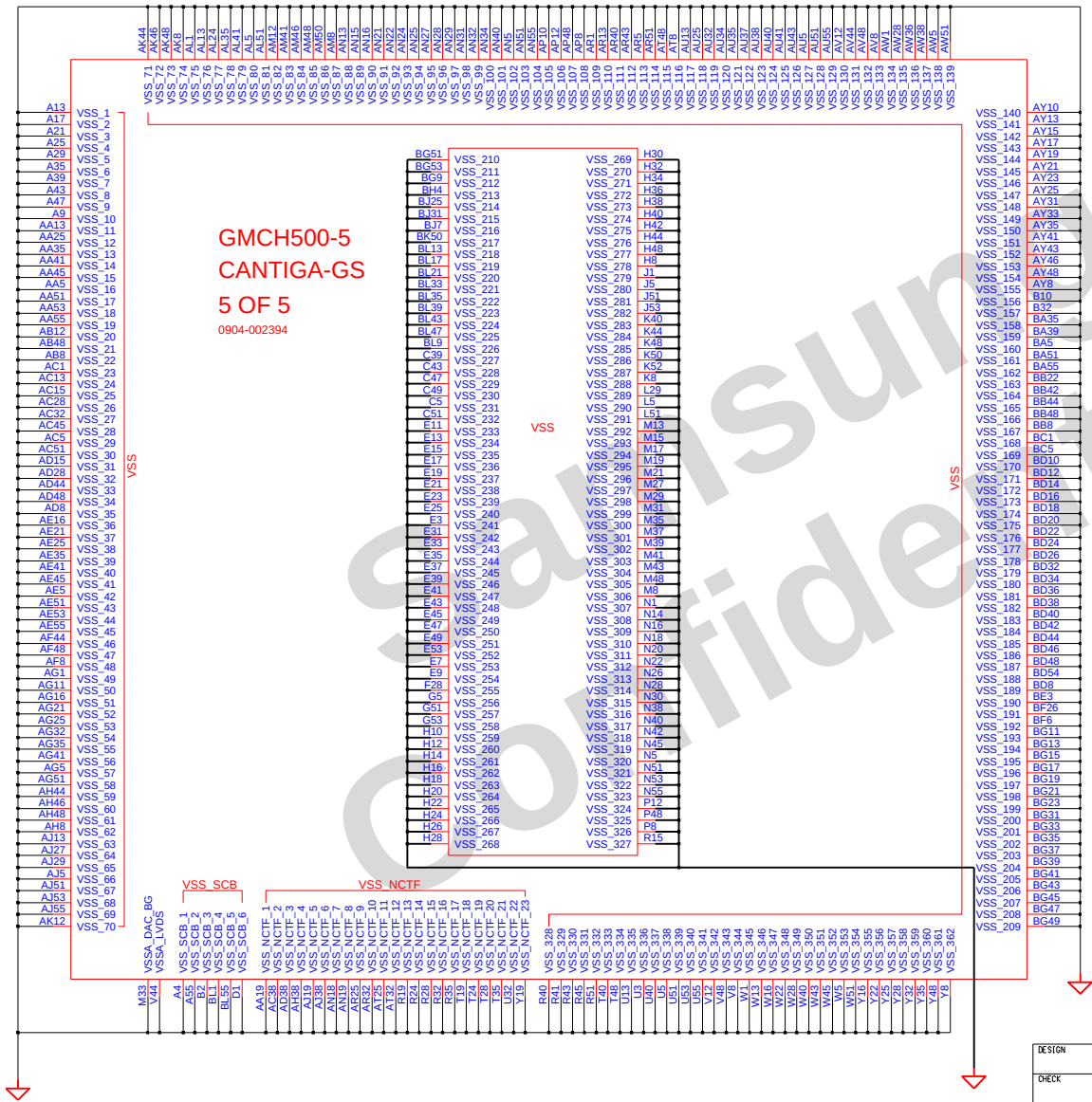
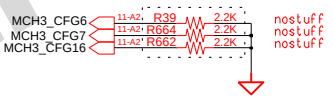
GMCH(CANTIGA GS)



	Current Setting (def. : default Option)	
CFG#	Low	High
CFG(6)	iTPM Host Interface Enable	**iTPM Host Interface Disable (def.)**



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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN CANTIGS GS(5/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		PART NO. BA41-0XXXXA
APPROVAL: JS , EUH	REV: 1.1		
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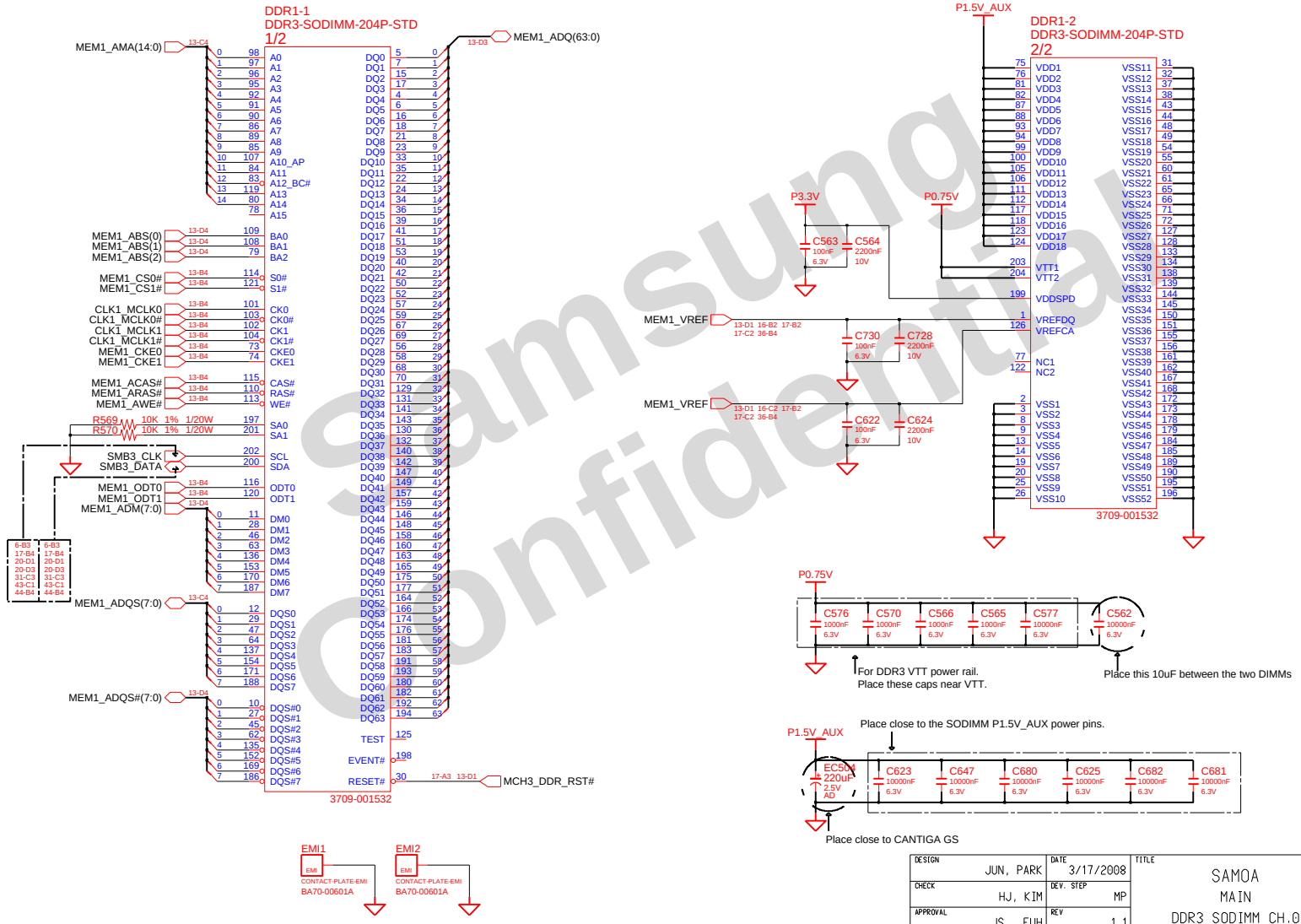
DDR3 SO-DIMM #0

Height : 4.0mm (Standard)



DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN DDR3 SODIMM CH.0	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		PART NO. BA41-0XXXXA
APPROVAL: JS , EUH	REV: 1.1		
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM		PAGE 16 OF 44

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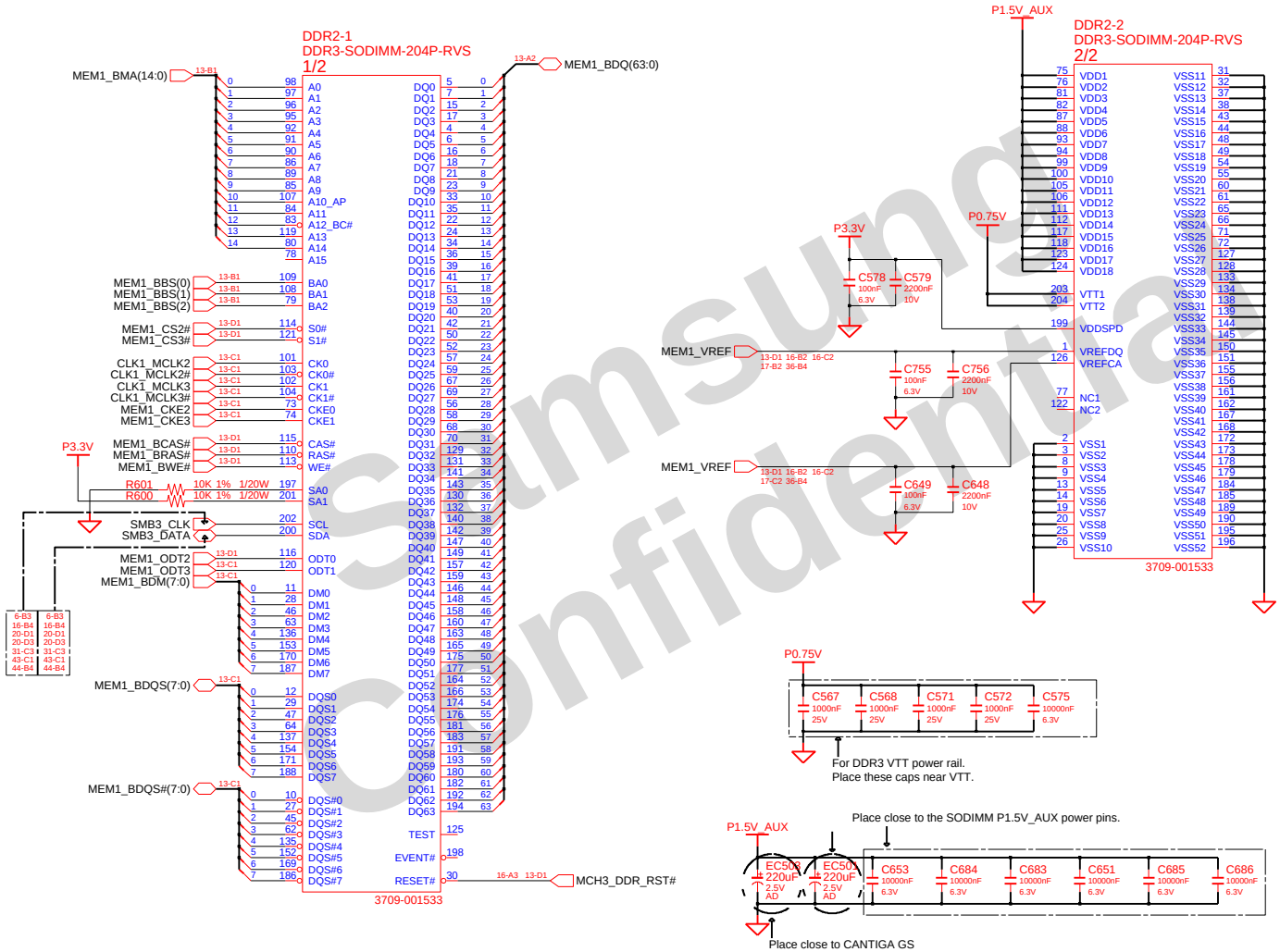
DDR3 SO-DIMM #1

Height : 4.0mm (Reverse)



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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN DDR3 SODIMM CH.1	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM		PAGE 17 OF 44

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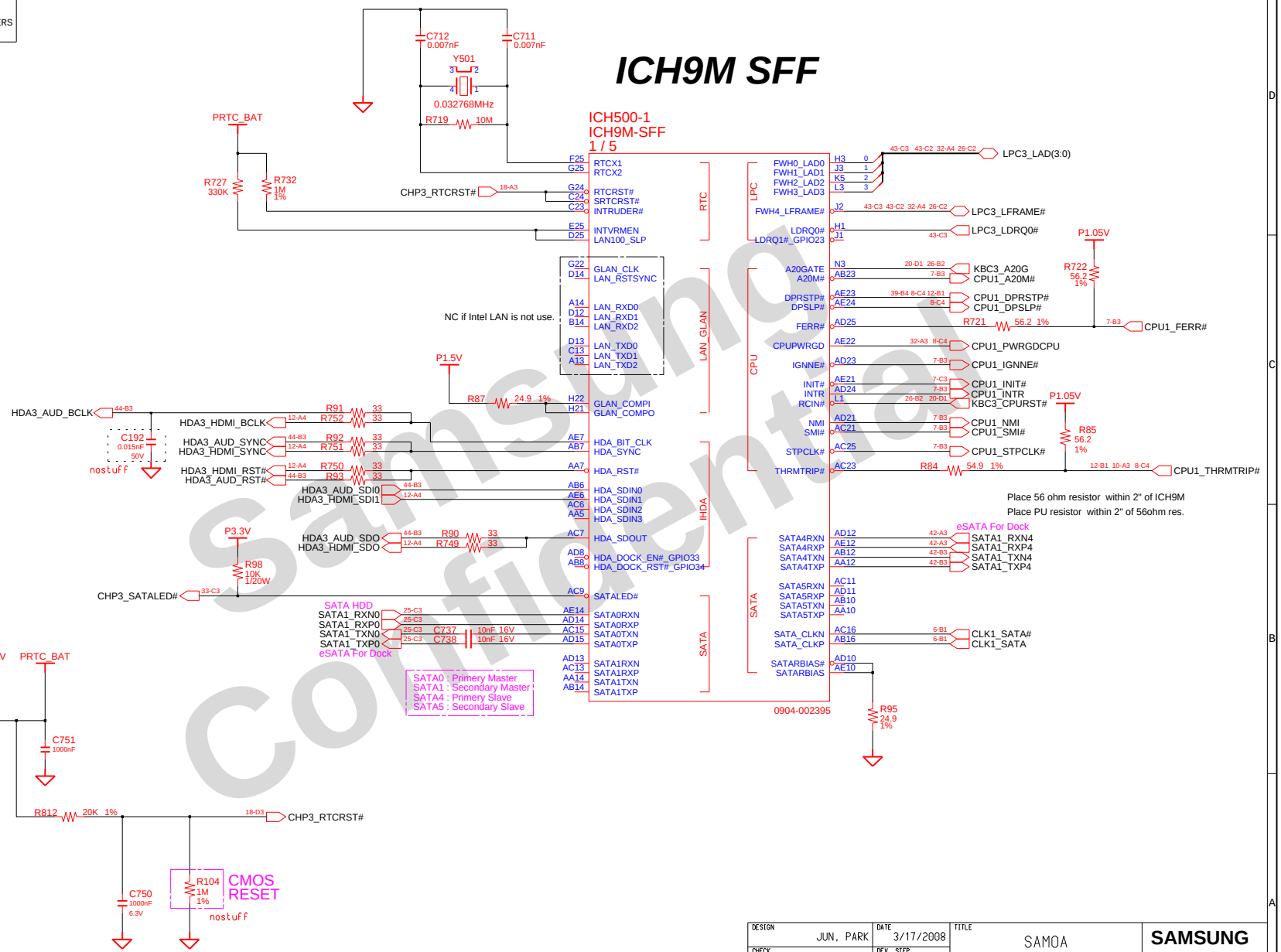
ICH9M SFF



DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN ICH9M SFF(1/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM		PAGE 18 OF 44

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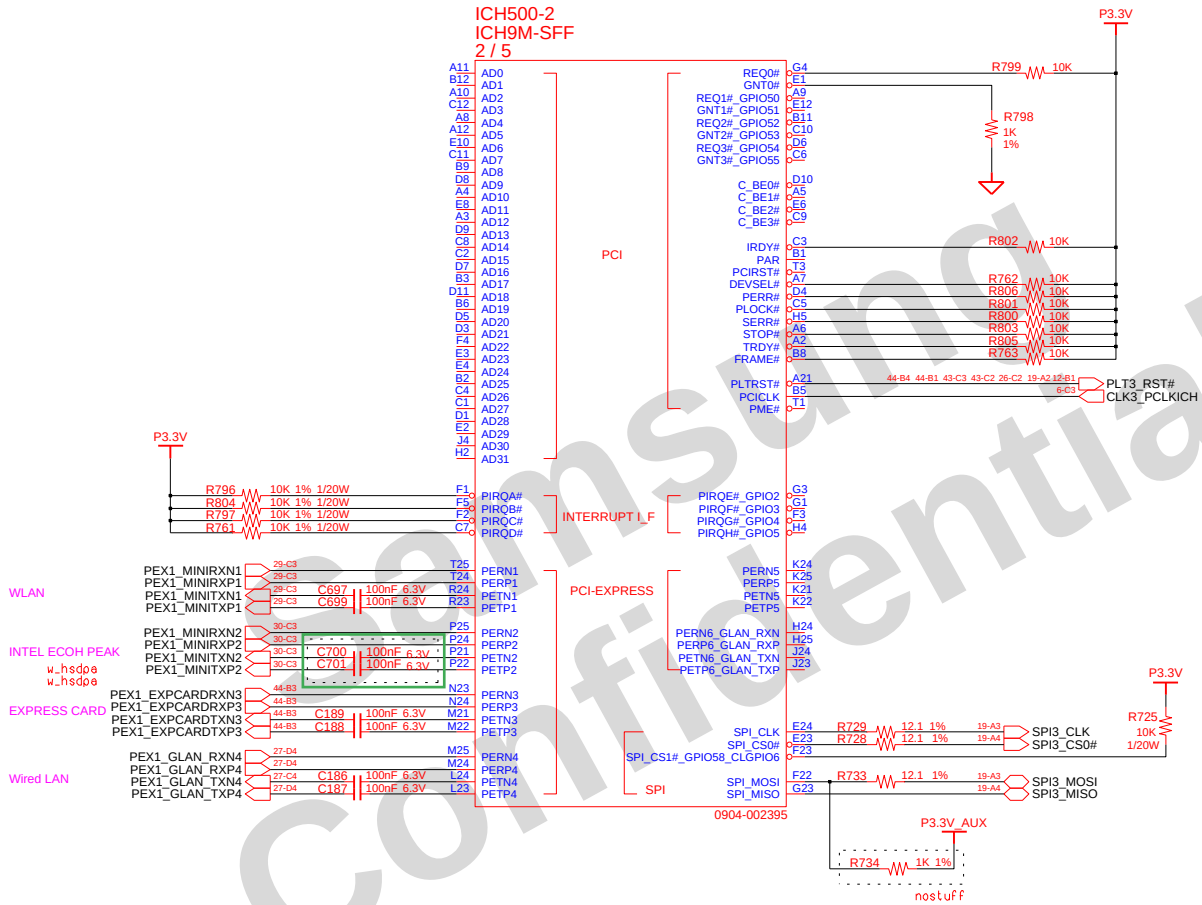
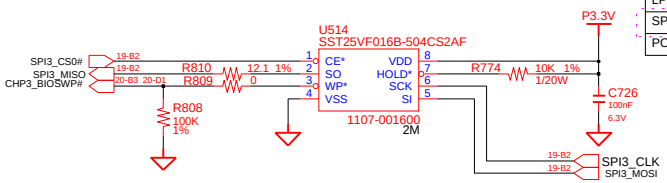
ICH9M SFF

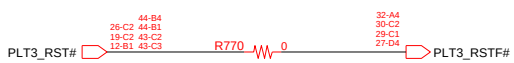


SPI ROM



Boot BIOS Select

BIOS	PCI3_GNT0#	SPI3_CS1#
LPC	HIGH	HIGH
SPI	LOW	HIGH
PCI	HIGH	LOW



DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN ICH9M SFF(2/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		PART NO. BA41-0XXXXA
APPROVAL: JS , EUH	REV: 1.1		
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 19 OF 44	

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ICH9M SFF

ICH500-3
ICH9M-SFF
3 / 5

SYS_RESET# is P3.3V tolerant and should be pulled up to P3.3V_AUX by the front panel header

Place clsely to ICH

When using Cantiga SFF, GPIO49 should be left as NC.

BIOS CRISIS RECOVER STRAP
PLACE NEAR KEYBOARD
(Put it a debugger connector)

Place this registor within 500-mils of the ICH9M
Avoid routing next to clock/high speed signals.

R743 nostuff
R713 nostuff
R716 nostuff
R744 stuff for eSATA Hot Plug Detection Enable

0904-002395

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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN ICH9M SFF(3/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		PART NO. BA41-0XXXXA
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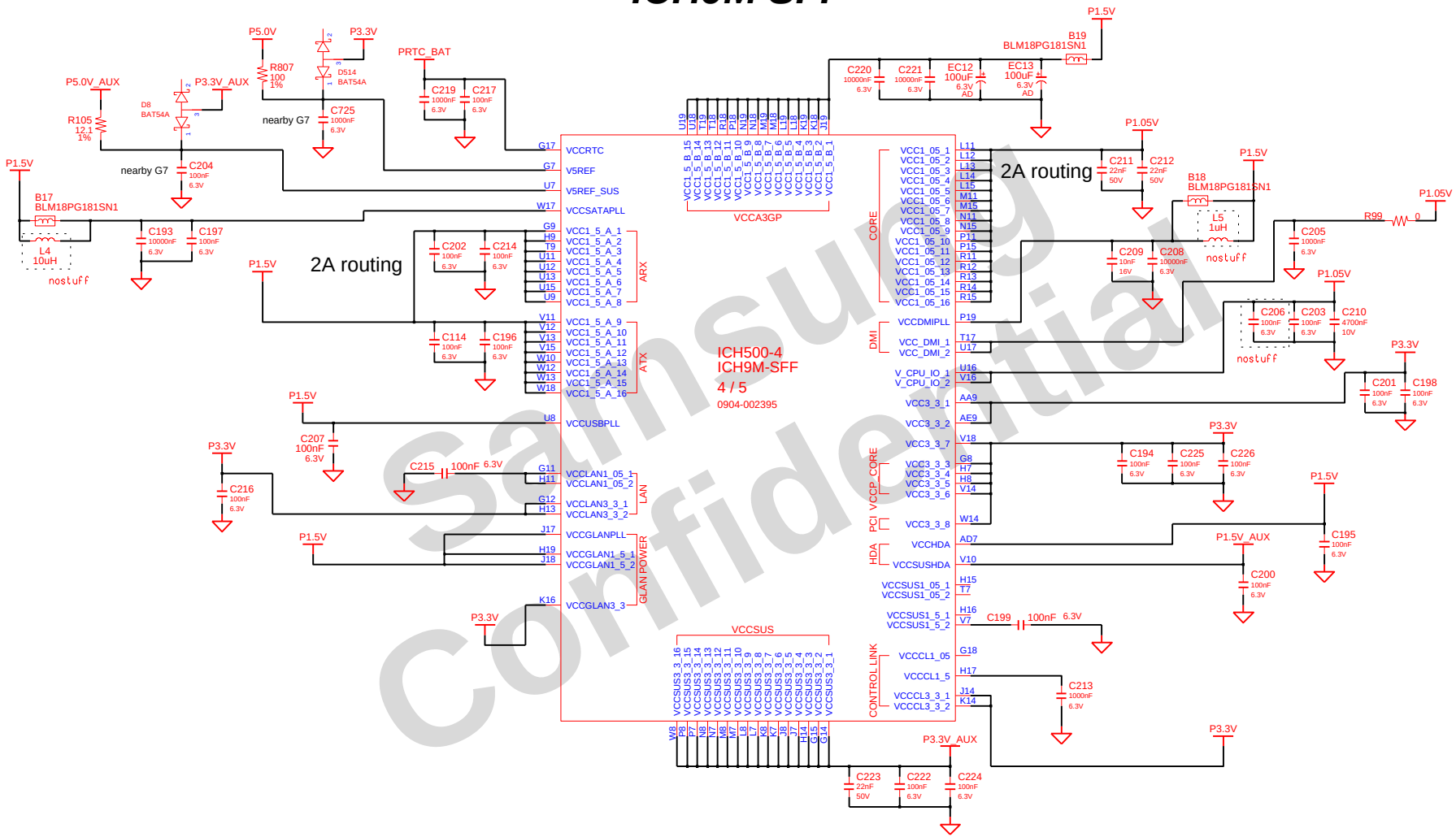
ICH9M SFF



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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN ICH9M SFF(4/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
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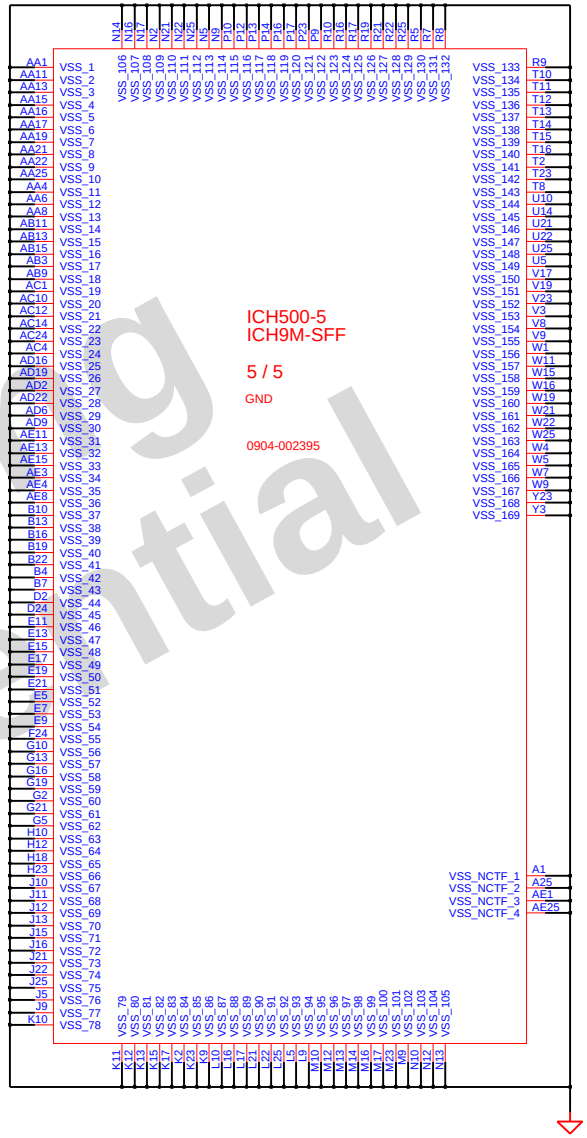
BIOS CODE

ICH9M SFF

02	VERIFY REAL MODE
03	DISABLE NMI
04	GET CPU TYPE
06	INIT. SYSTEM H/W
08	INIT. CHIPSET REG.
09	SET IN POST FLAG
0A	INIT CPU.REG
0B	CPU CACHE ON
0C	INIT.CACHE TO POST
OE	INIT. I/O VALUE
0F	ENABLE THE L-BUS IDE
10	INIT. POWER MANAGER
11	LOAD ALTERNATE REG.
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE
14	INIT. KEYBOARD CONTROLLER
16	CHECK CHECKSUM
18	8254 TIMER INIT.
1A	8237 DMA CONTROLLER INIT.
1C	RESET INTERRUP CONTROLLER
20	TEST DRAM REFRESH
22	TEST 8742 KEYBOARD CONTROLLER
24	SET ES SEGMENT REG. TO 4GB
26	ENABLE A20
28	AUTO SIZING DRAM
32	COMPUTE THE CPU SPEED
34	TESET CMOS RAM
38	SHADOW SYSTEM BIOS ROM
3A	AUTO SIZING CACHE
3C	CONFIGURE ADVANCED CHIPSET REG.
3D	LOAD ALTER REG. WITH CMOS VALUE
42	INIT. INTERRUPT VECTOR
44	INIT. BIOS INTERRUPT
46	CHECK ROM COPYRIGHT NOTICE
47	INIT. I20 SUPPORT IF INSTALLED
48	CHECK VIDEO CONFIGURE AGAINST CMOS
49	INIT. PCI BUS AND DEVICE
4A	INIT. ALL VIDEO BIOS ROM
4C	SHADOW VIDEO BIOS ROM
50	DISPLAY CPU TYPE AND SPEED
52	TEST KEYBOARD
54	SET KEYCLICK IF ENABLED
56	ENABLE KEYBOARD
58	TEST FOR UNEXPECTED INTERRUPTS
5A	DISPLAY " PRESS ..... SETUP"
5C	TEST RAM GETWEEN 512K AND 640K
60	TEST EXTENDED MEMORY
62	TEST EXTENDED MEMORY ADDRESS LINE
64	JUMP TO USER PATCH 1

66	CONFIGURE ADVANCE CACHE REG.
6A	DISPLAY EXTERNAL CACHE SIZE
6C	DISPLAY SHADOW MESSAGE
6E	DISPLAY NON-DISPOSABLE SEGMENT
70	DISPLAY ERROR MESSAGE
72	CHECK FOR CONFIGURATION ERROR
74	TEST REAL-TIME CLOCK
76	CHECK FOR KEYBOARD EERROR
7C	SETUP HARDWARE INTERRUPT VECTOR
7E	TEST COPROCESSER IF PRESENT
80	DISABLE ON-BOARD I/O PORT
82	DETECT AND INSTALL EXT.RS232C
84	DETECT AND INSTALL EXT.PARALLEL
86	RE-INIT. ON-BOARD I/O PORT
88	INIT. BIOS DATA ROM
8A	INIT.EXTENDED BIOS DATA AREA
8C	INIT. FDD CONTROLLER
9A	SHADOW OPTION ROMS
9C	SETUP POWER MANAGEMENT
9E	ENABLE H/W INTERRUPT
A0	SET TIME OF DAY
A4	INIT. TYPEMATIC RATE
A8	ERASE F2 PROMPT
AA	SCAN FOR F2 KEY STROKE
AC	ENTER SETUP
AE	CLEAR IN POST FLAG
B0	CHECK FOR ERRORS
B2	POST DONE-PREPARE TO BOOT O/S
B4	ONE BEEP
B6	CHECK PASSWORD (OPTION)
B7	ACPI INIT
BA	DMI INIT
BE	CLEAR SCREEN
C0	TRY BOOT WITH INT19
D0	INTERRUPT HANDLER ERROR
D2	UNKNOWN INTERRUPT ERROR
D4	PENDING INTERRUPT ERROR
D6	SHUTDOWN 5
D8	SHUTDOWN ERROR
DA	EXTENDED BLOCK MOVE
DC	SHUTDOWN 10
89	ENABLE NMI
90	INIT. HDD CONTROLLER
91	INIT. LOCAL BUS HDD CONTROLLER
92	JUMP TO USER PATCH 2
94	DISABLE A20 ADDRESS LINE
96	CLEAR HUGE ES SEGMENT REG.
98	SEARCH FOR OPTION ROMS



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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN ICH9M SFF(5/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM		PAGE 22 OF 44

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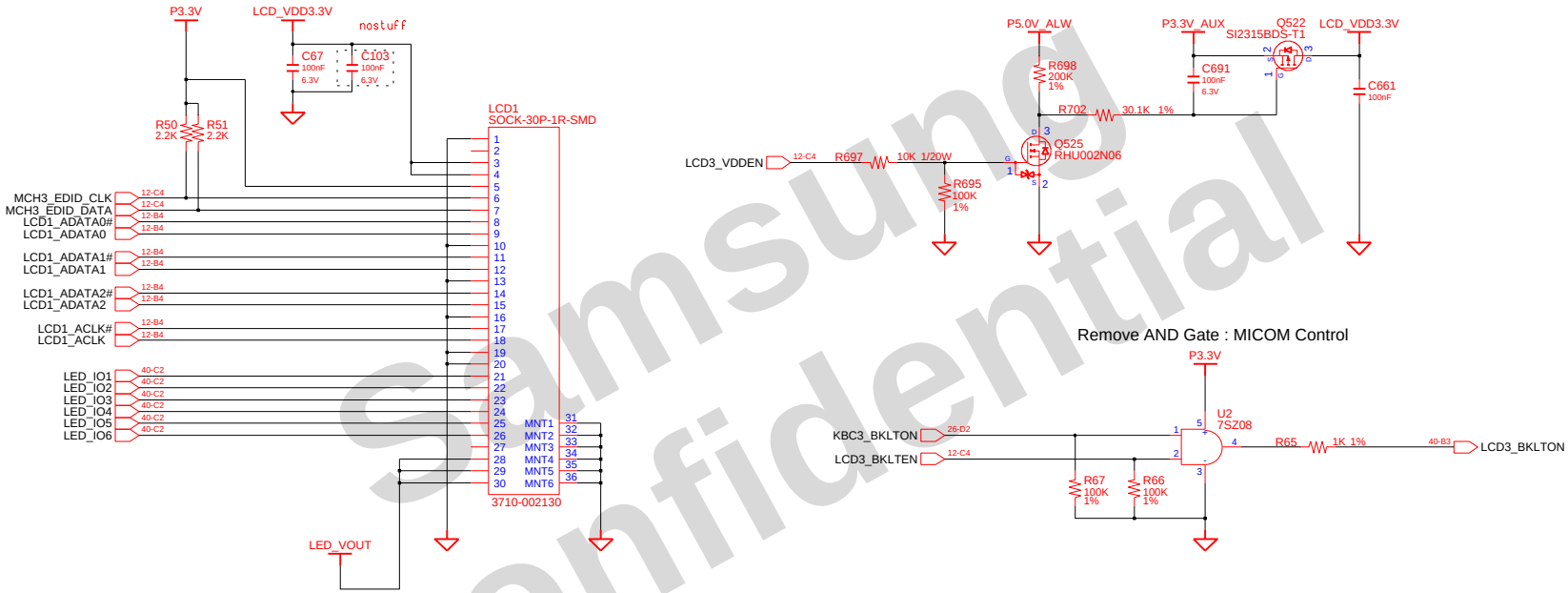
LED LCD CONNECTOR



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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN LED LCD I/F	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM		PAGE 23 OF 44

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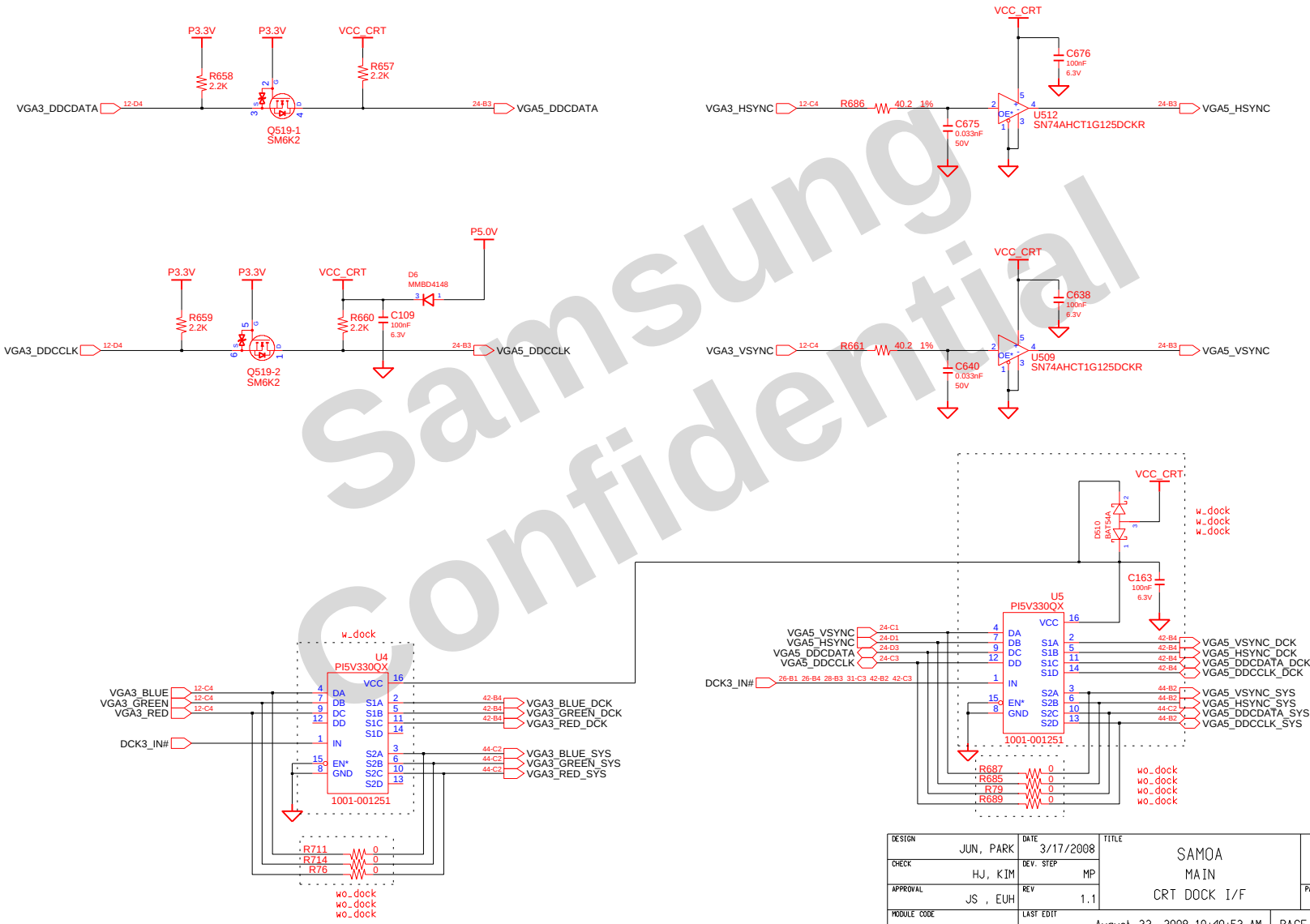
CRT DOCK I/F



DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN CRT DOCK I/F	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		PART NO. BA41-0XXXXA
APPROVAL: JS , EUH	REV: 1.1		
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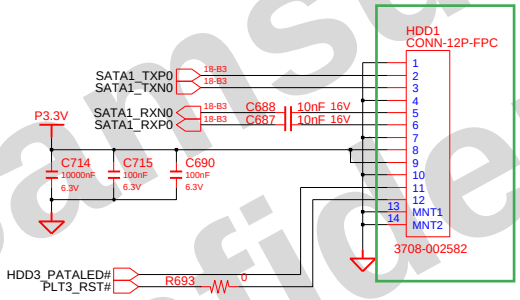
1.8" SATA HDD I/F



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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN 1.8inch SATA HDD I/F	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
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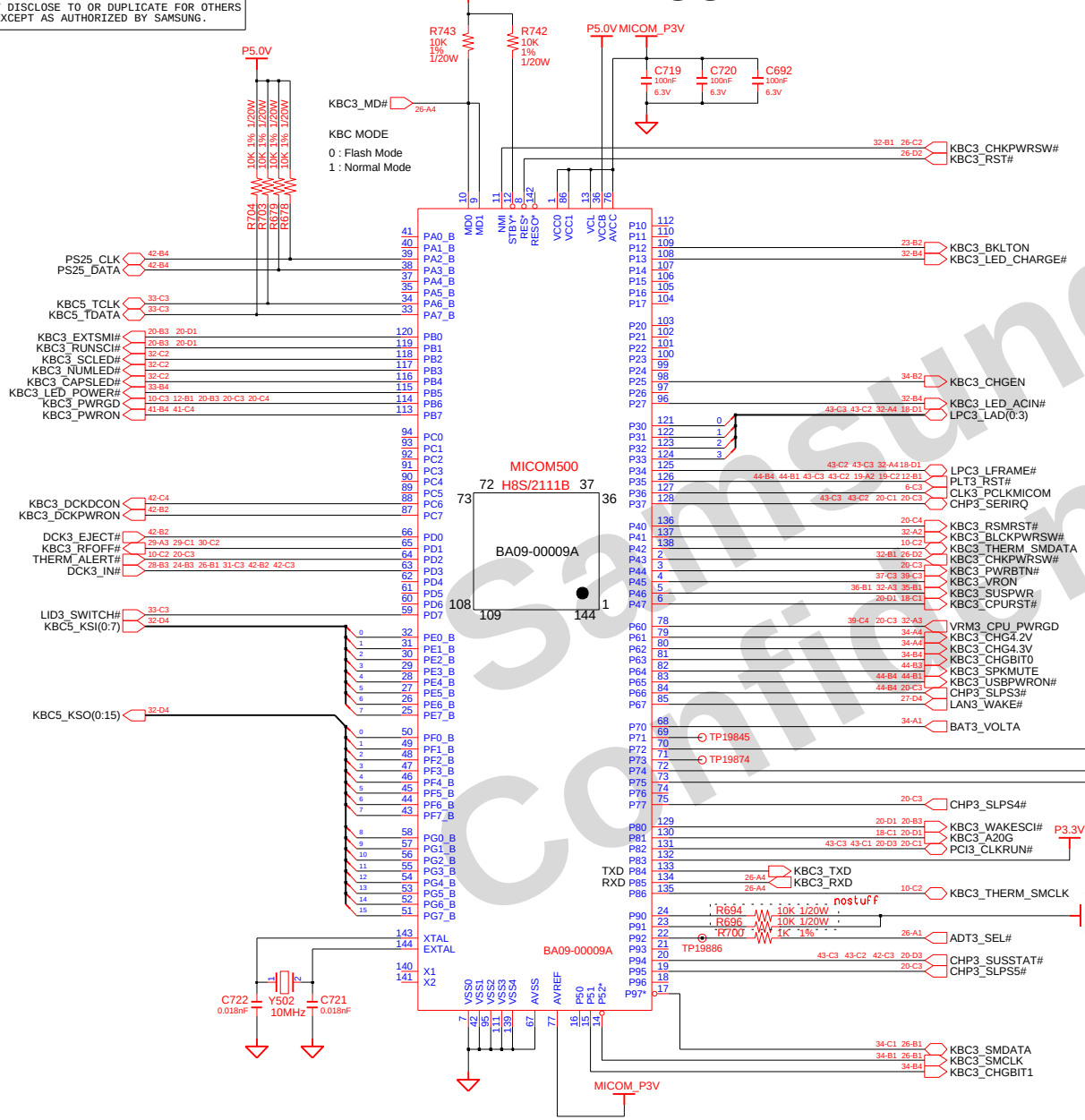
MICOM



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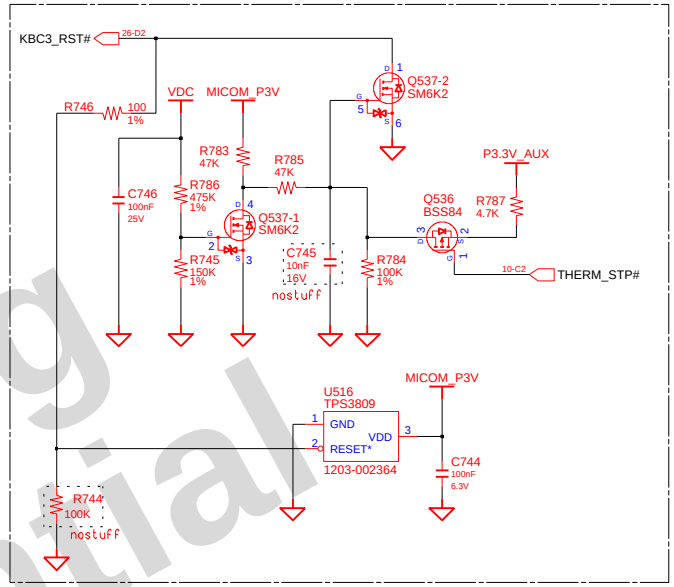

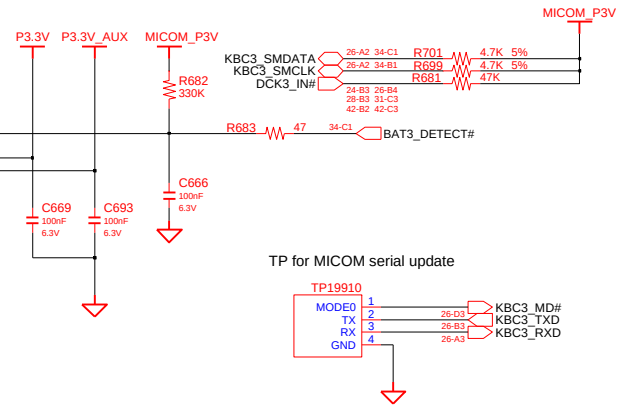

DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN KEYBOARD CONTROLLER	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
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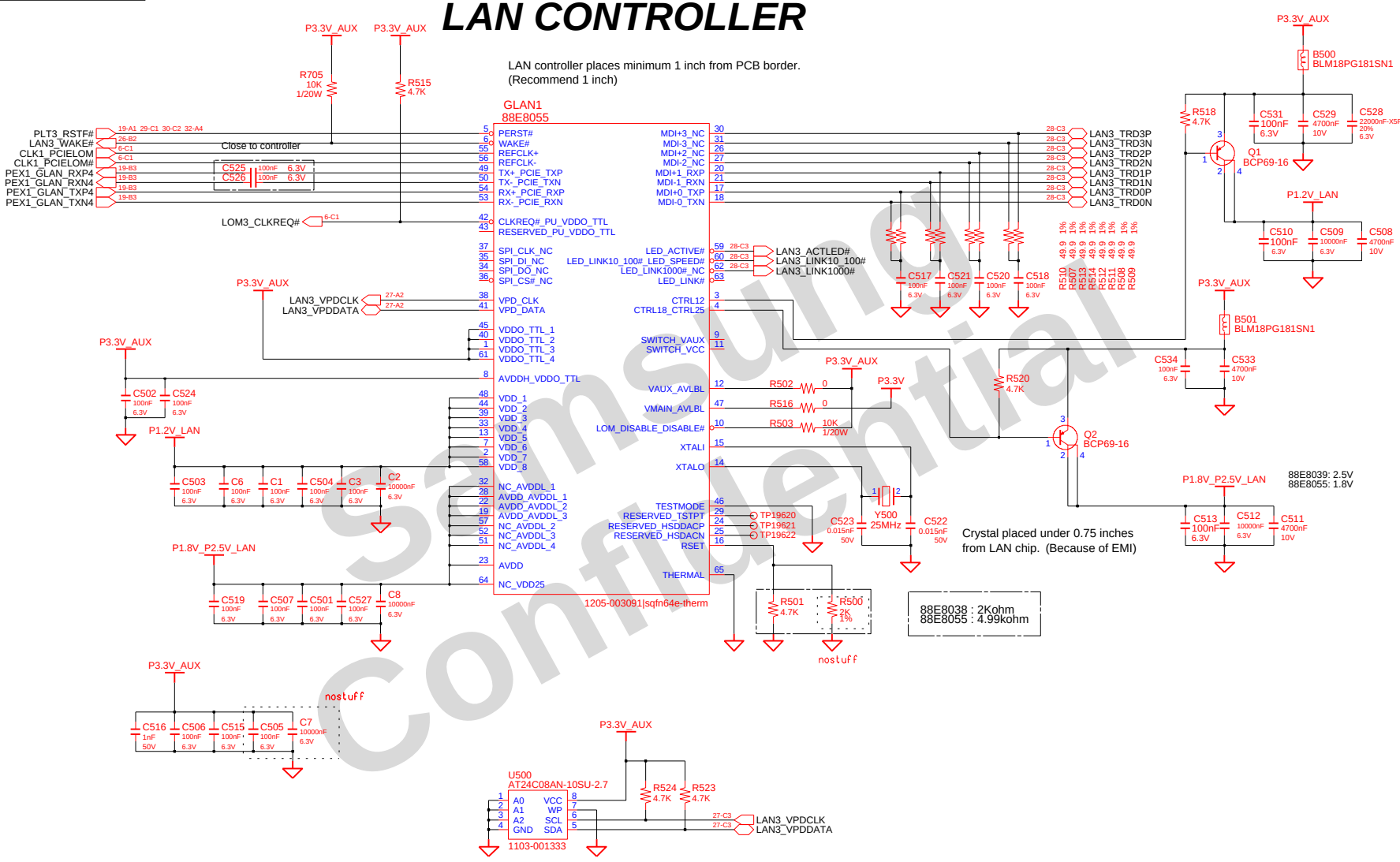
LAN CONTROLLER



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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN LAN CONTROLLER	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
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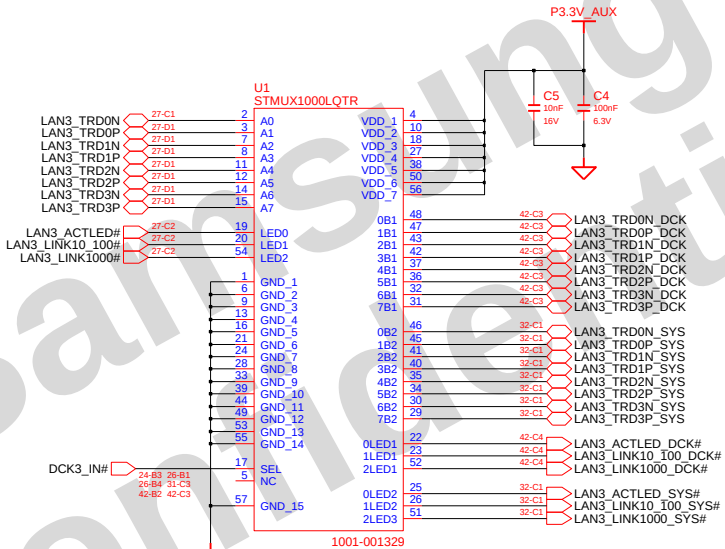
LAN PASSTHRU BRIDGE CHIP



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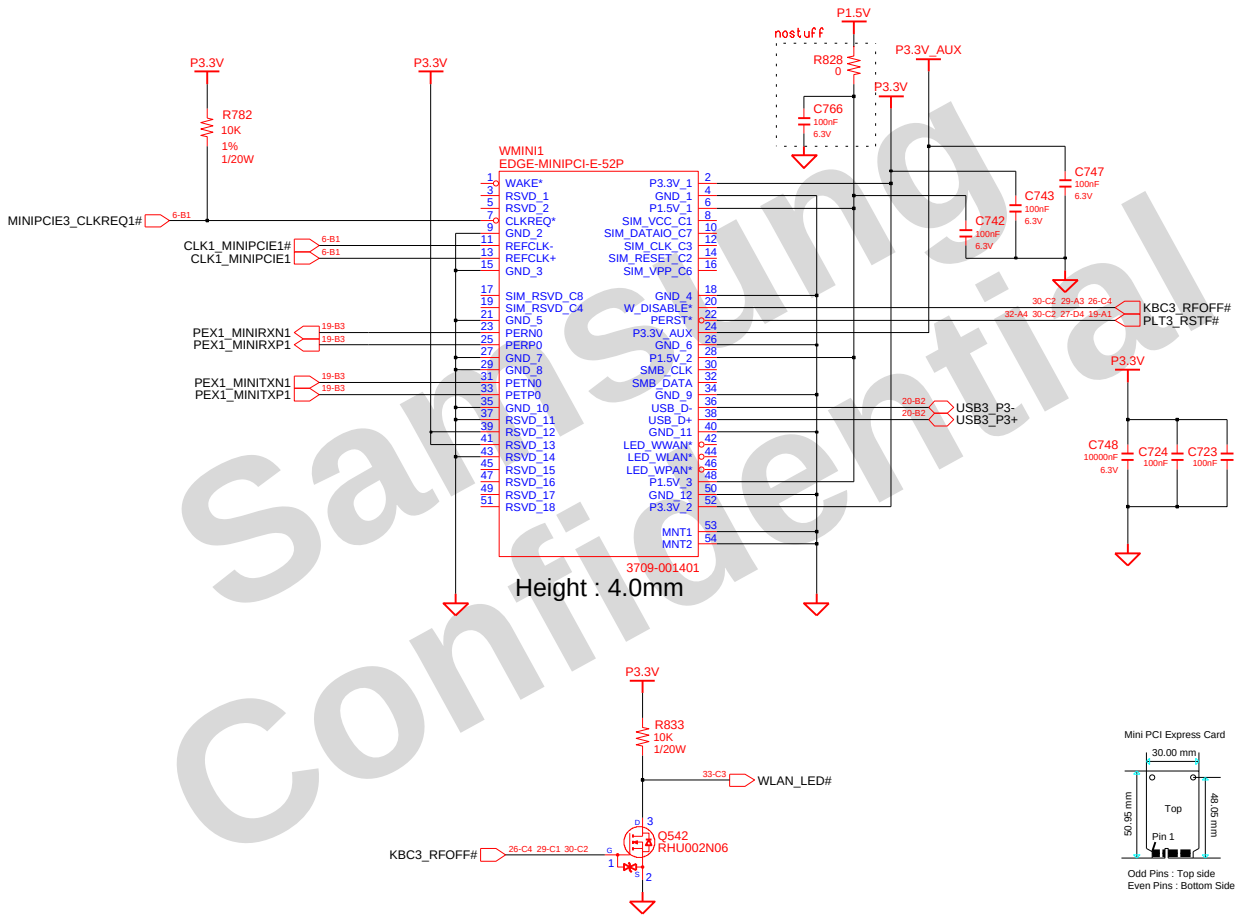
MINICARD(WLAN)



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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN WIRELESS LAN	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		PART NO. BA41-0XXXXA
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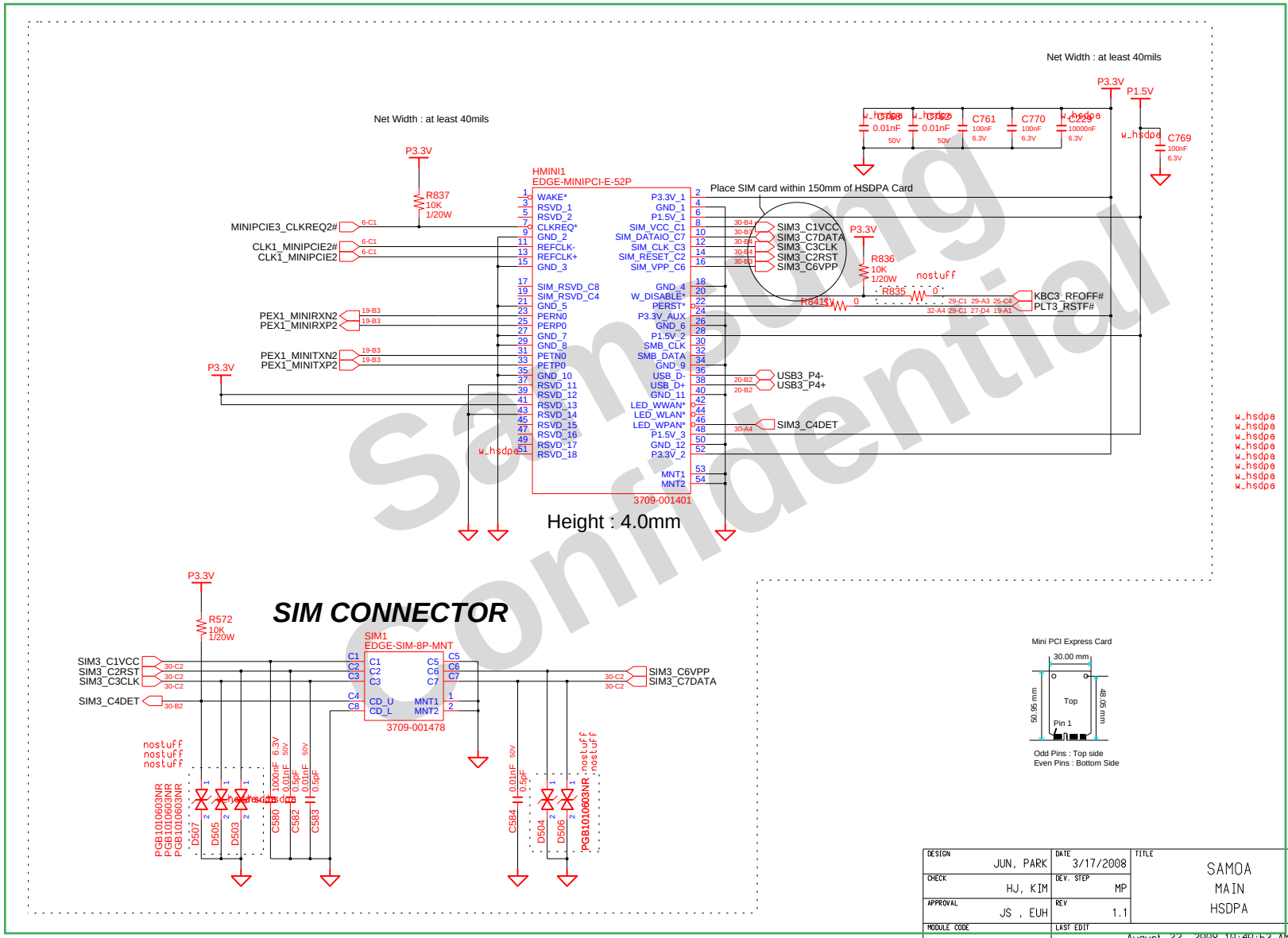
MINICARD(HSDPA)



SIM CONNECTOR

DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN HSDPA	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		PART NO. BA41-0XXXXA
APPROVAL: JS , EUH	REV: 1.1		
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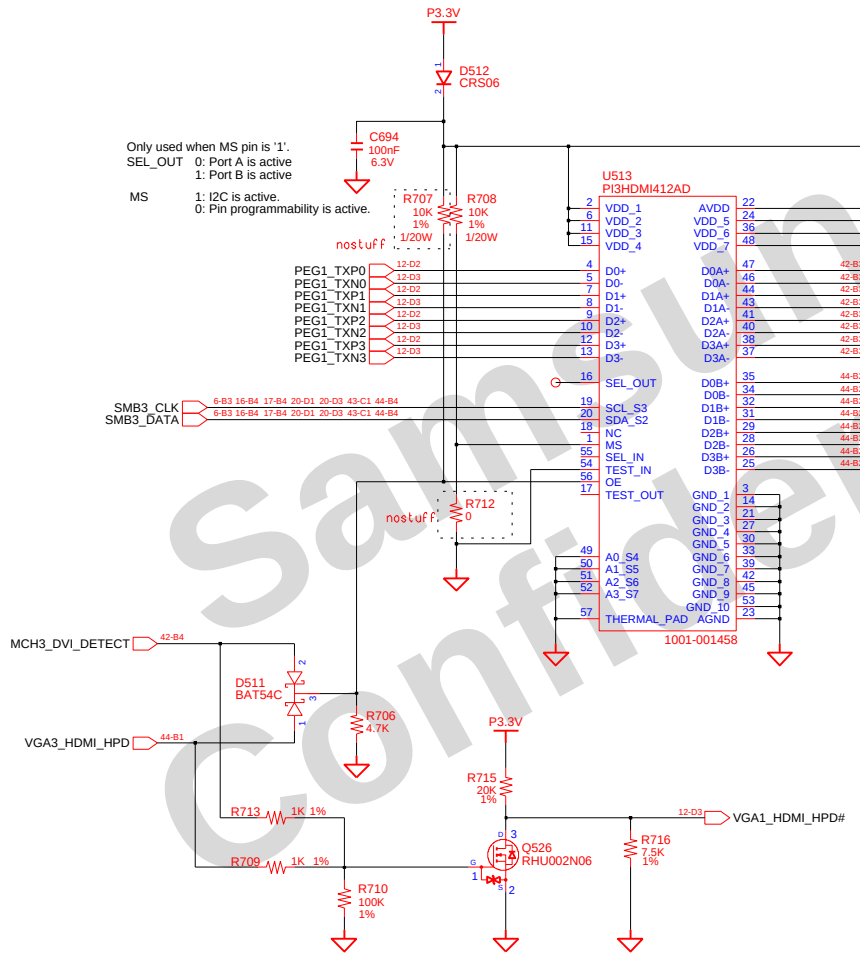
HDMI & DVI I/F



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CHECK: HJ, KIM	DEV. STEP: MP		
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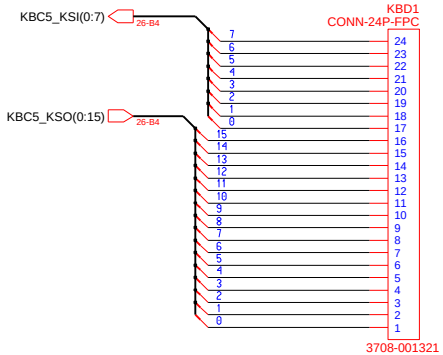
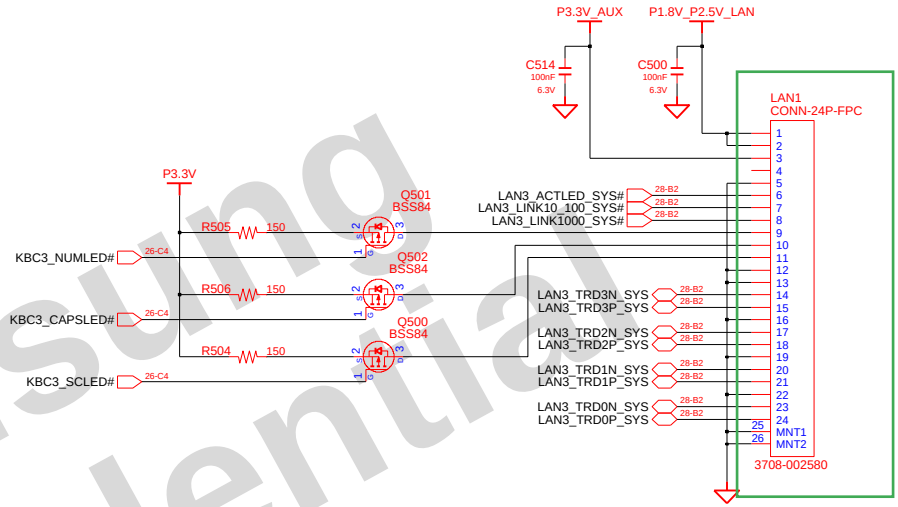
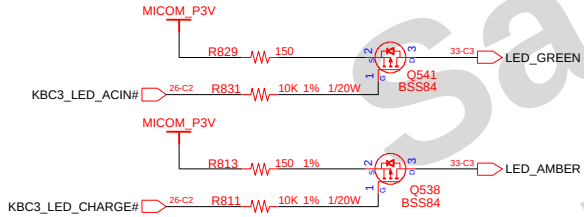
KEYBOARD CONNECTOR



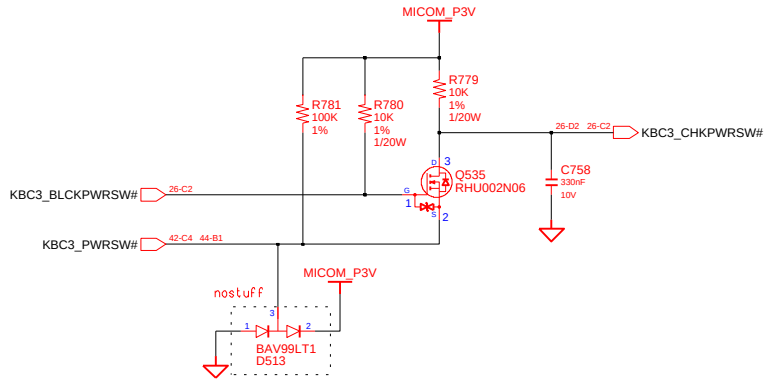
LAN BOARD CONNECTOR



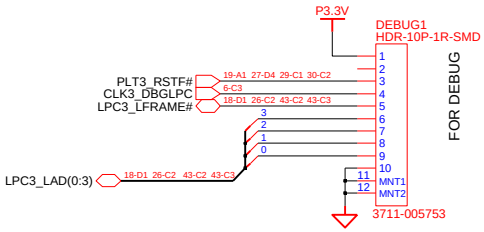
ADAPTERIN / CHARGING LED



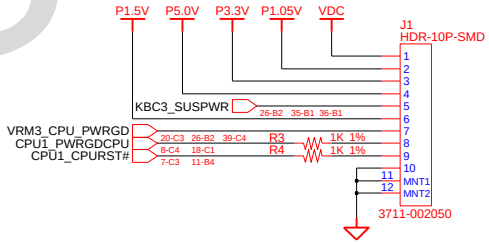
POWER S/W



DEBUG PORT



Pre FCT PORT



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CHECK: HJ, KIM	DEV. STEP: MP		
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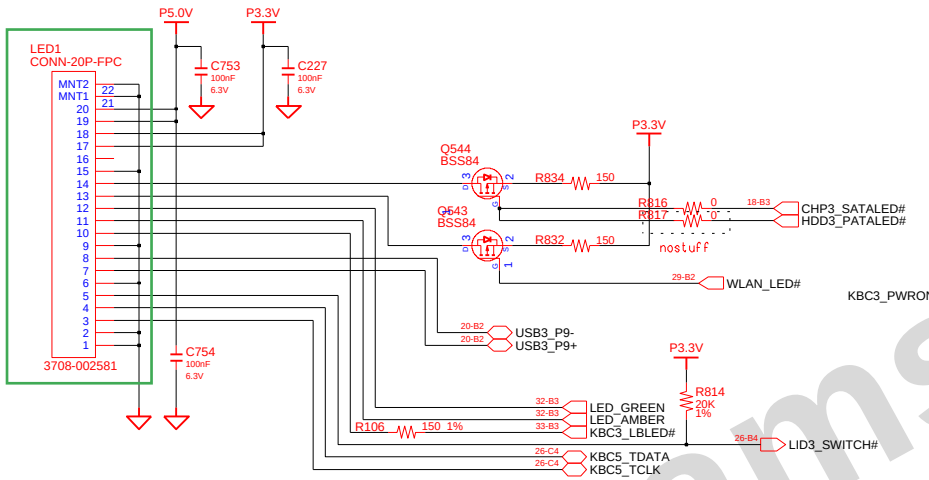
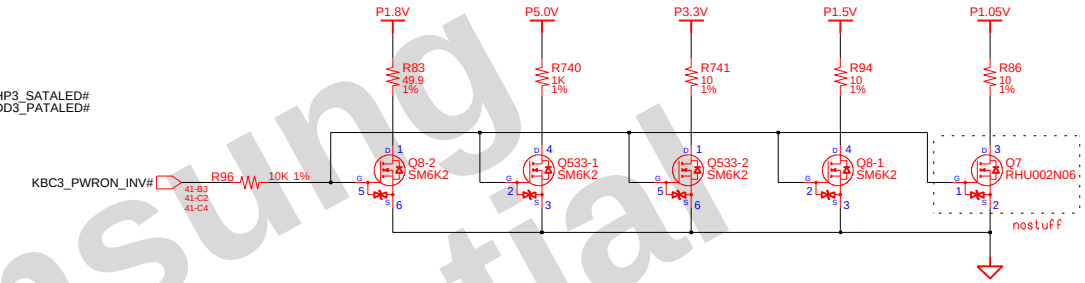
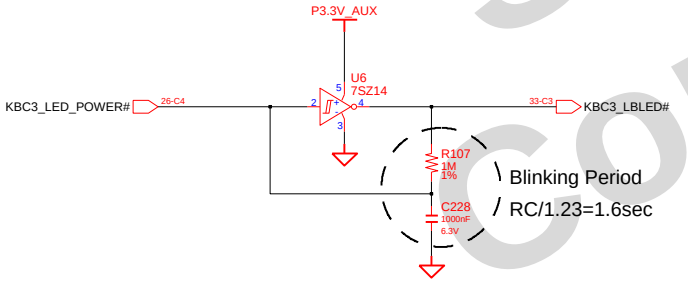
LED & T/P FPC CONNECTOR



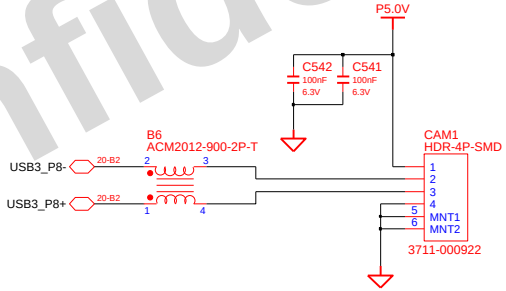
DISCHARGE



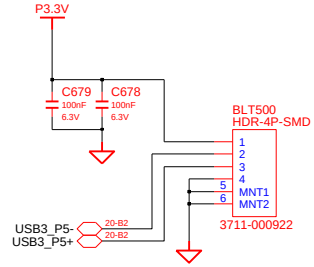
POWR ON / LB LED

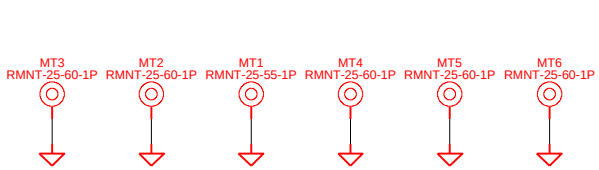


CAMERA



BLUETOOTH





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CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
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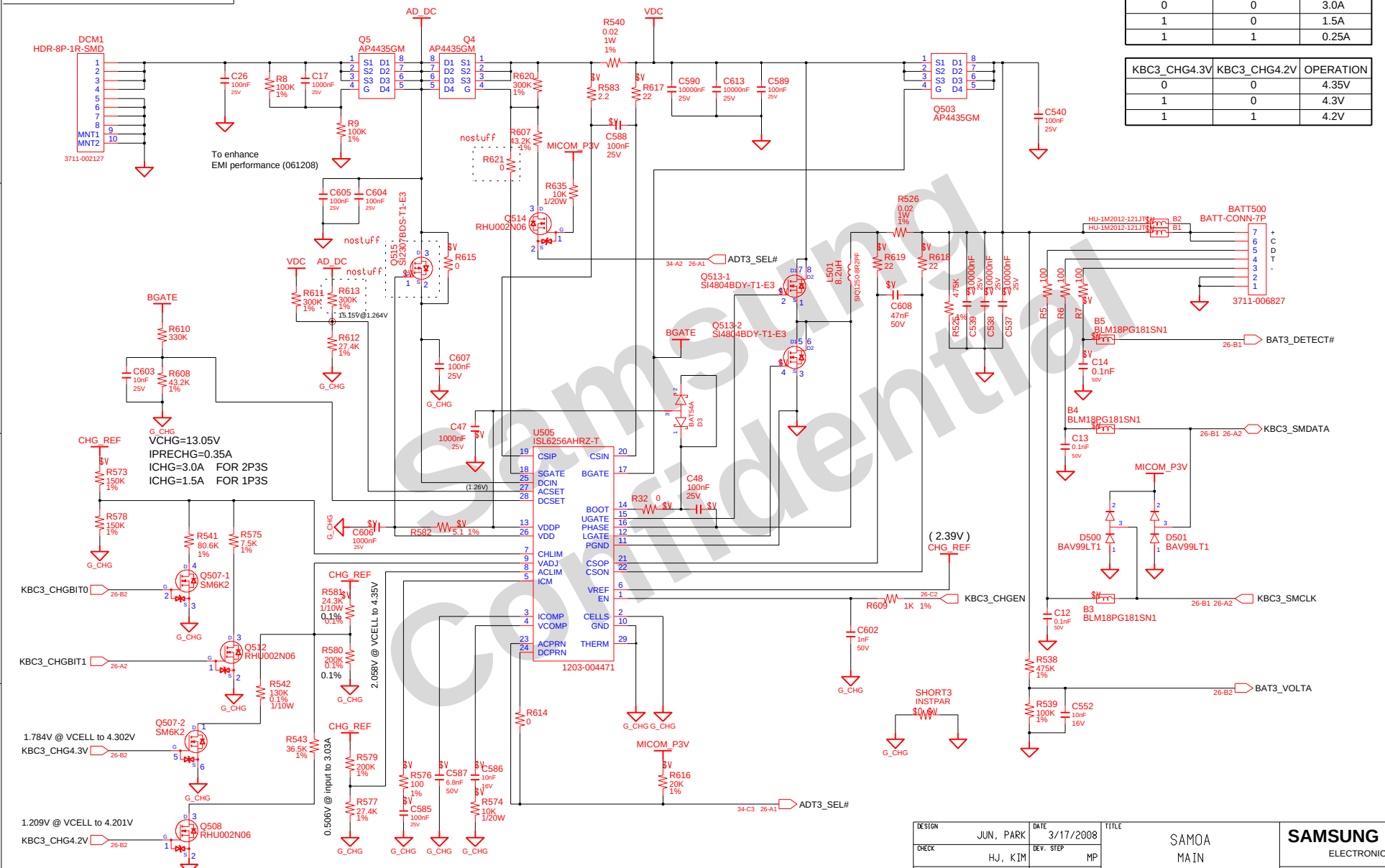
CHARGER & POWER MANAGEMENT

KBC3_CHGBIT0	KBC3_CHGBIT1	OPERATION
0	0	3.0A
1	0	1.5A
1	1	0.25A

KBC3_CHG4.3V	KBC3_CHG4.2V	OPERATION
0	0	4.35V
1	0	4.3V
1	1	4.2V



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN CHARGER	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS , EUH	REV	1.1			PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT	August 22, 2008 10:40:53 AM	PAGE	34 OF 44	

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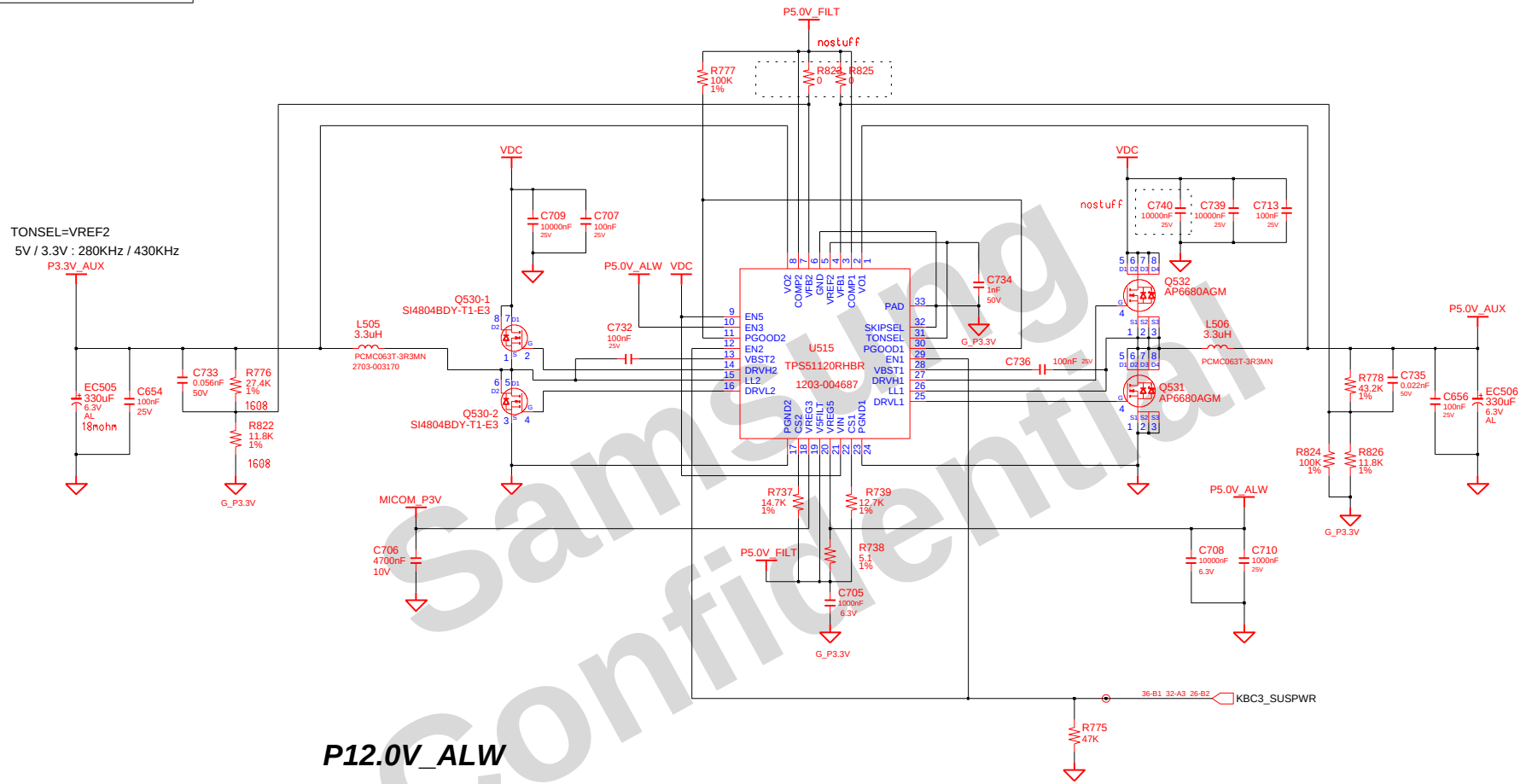
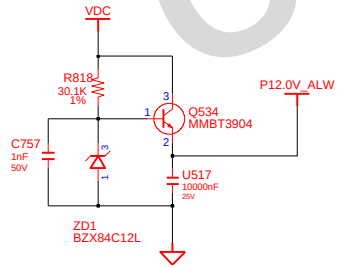
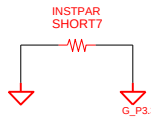
P5.0V_AUX & P3.3V_AUX



P12.0V_ALW





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CHECK: HJ, KIM	DEV. STEP: MP		PART NO. BA41-0XXXXA
APPROVAL: JS , EUH	REV: 1.1		
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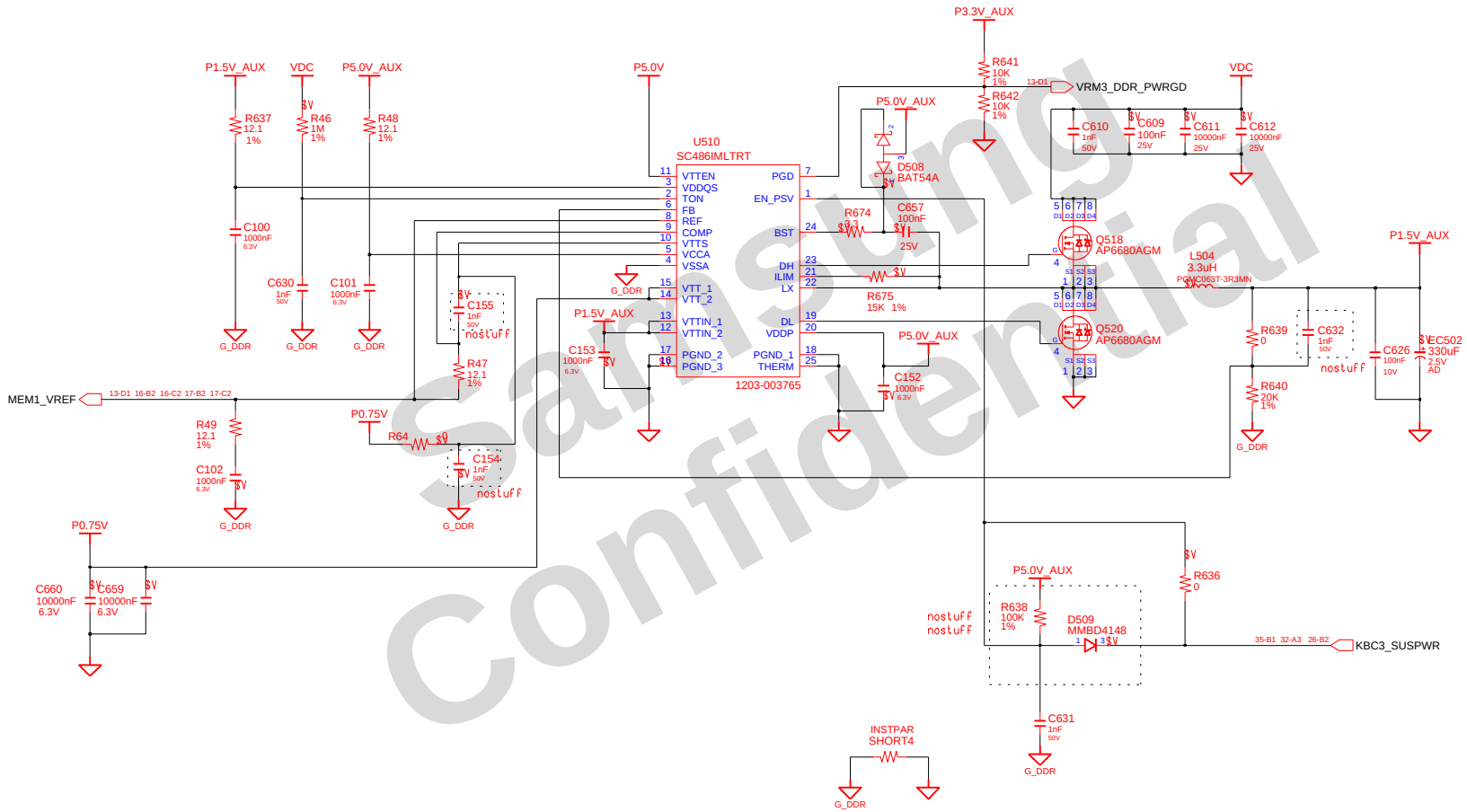
DDR3 Power



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CHECK: HJ, KIM	DEV. STEP: MP		PART NO. BA41-0XXXXA
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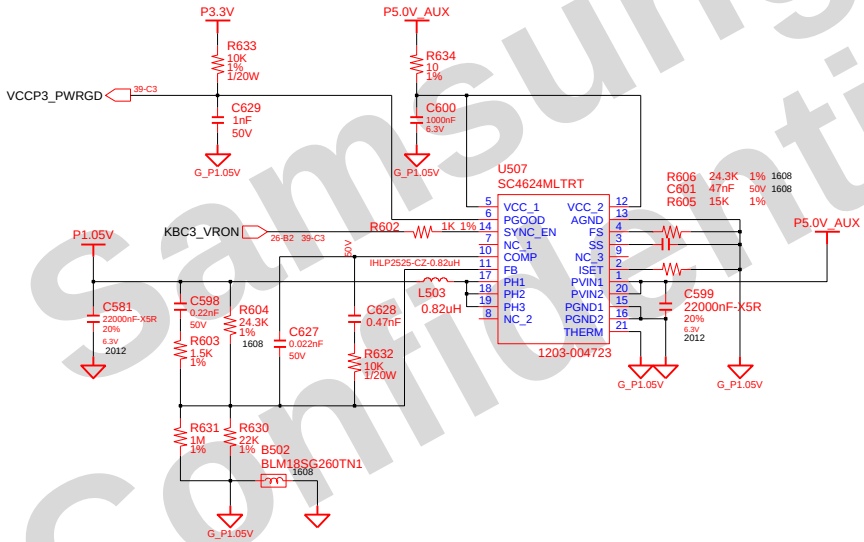
VCCP_CORE



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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN DDR2 POWER	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
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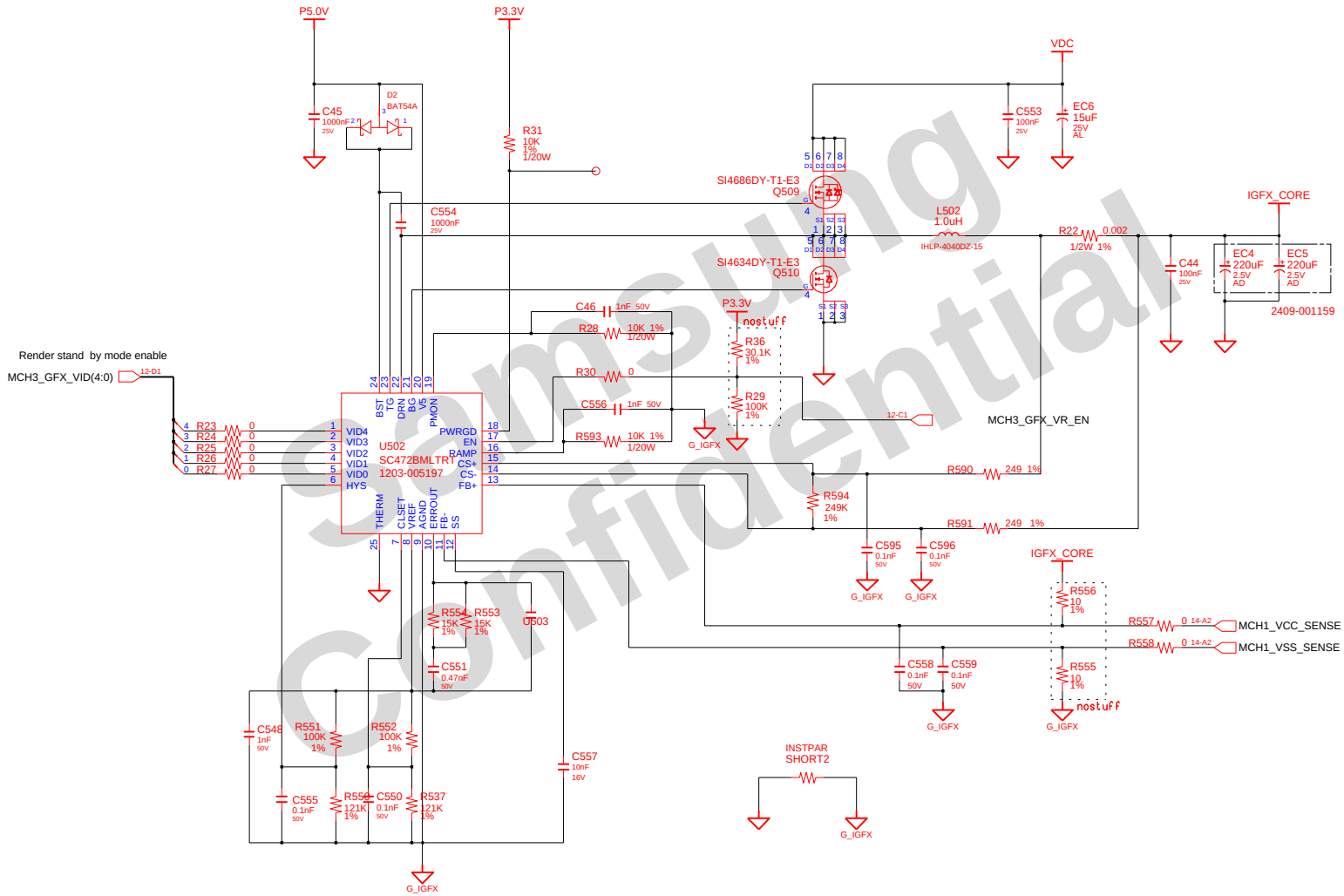
INTERNAL GFX CORE



DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN INTERNAL GFX CORE	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
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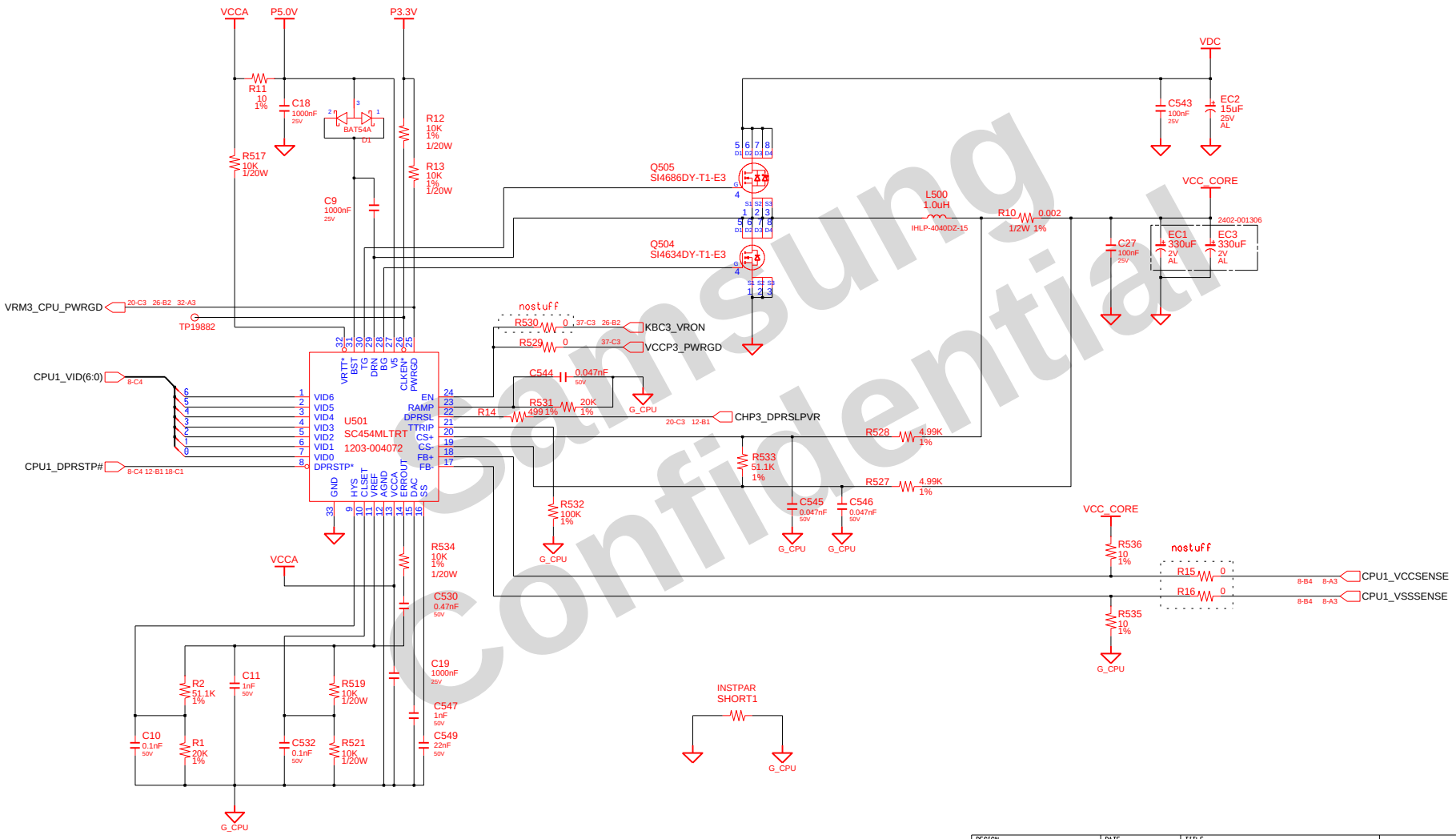
CPU VRM POWER



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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN CPU VRM POWER	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
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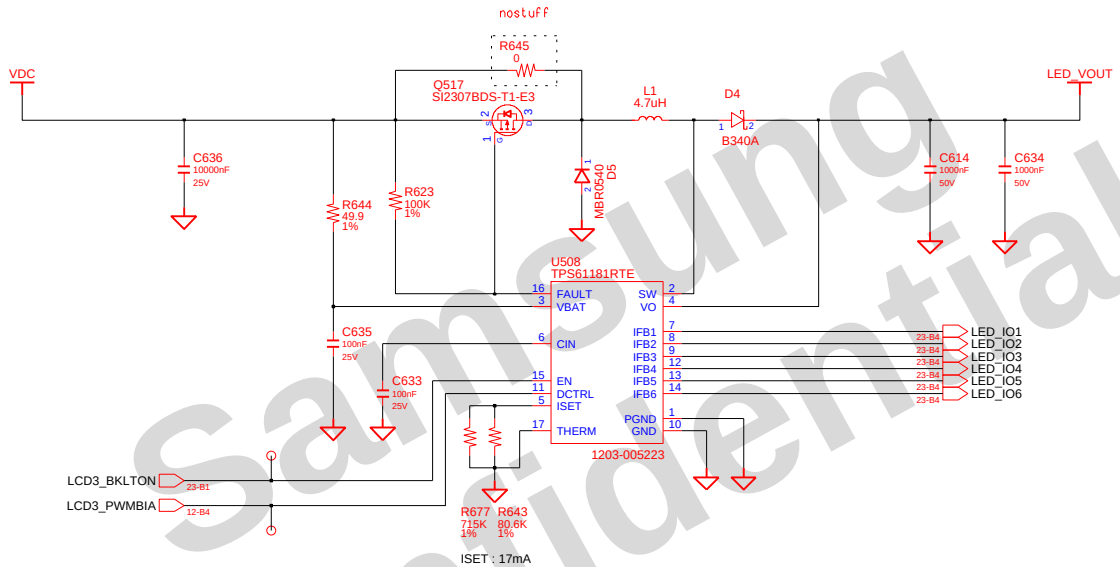
LED DRIVER



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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN LED DRIVER	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
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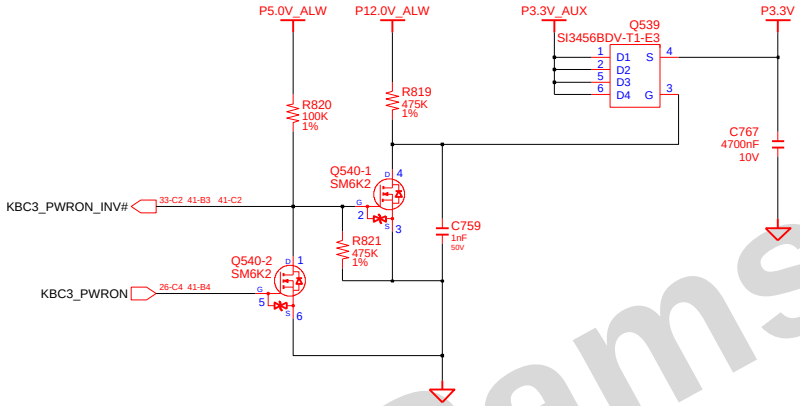
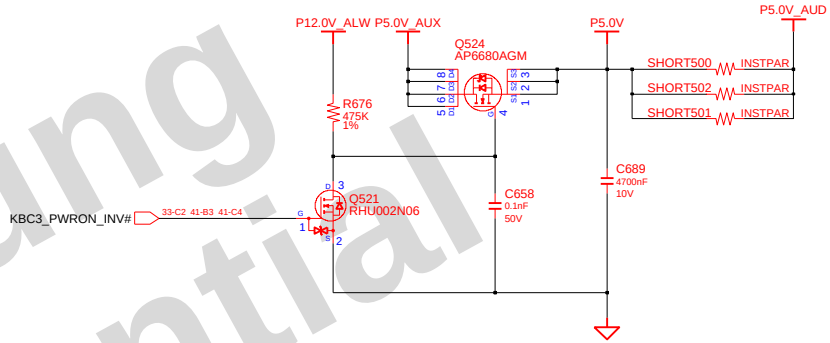
SWITCHED POWER

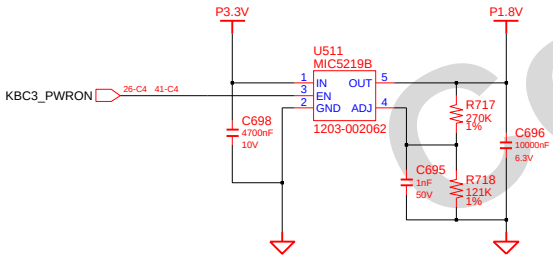
Switched Power On (P3.3V)



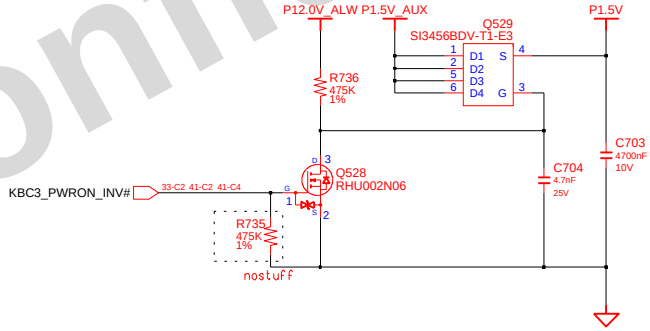
Switched Power On (P5V)



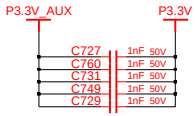
Switched Power On (P1.8V)



Switched Power On (P1.5V)



Stiching caps(For EMC)



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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM		PAGE 41 OF 44

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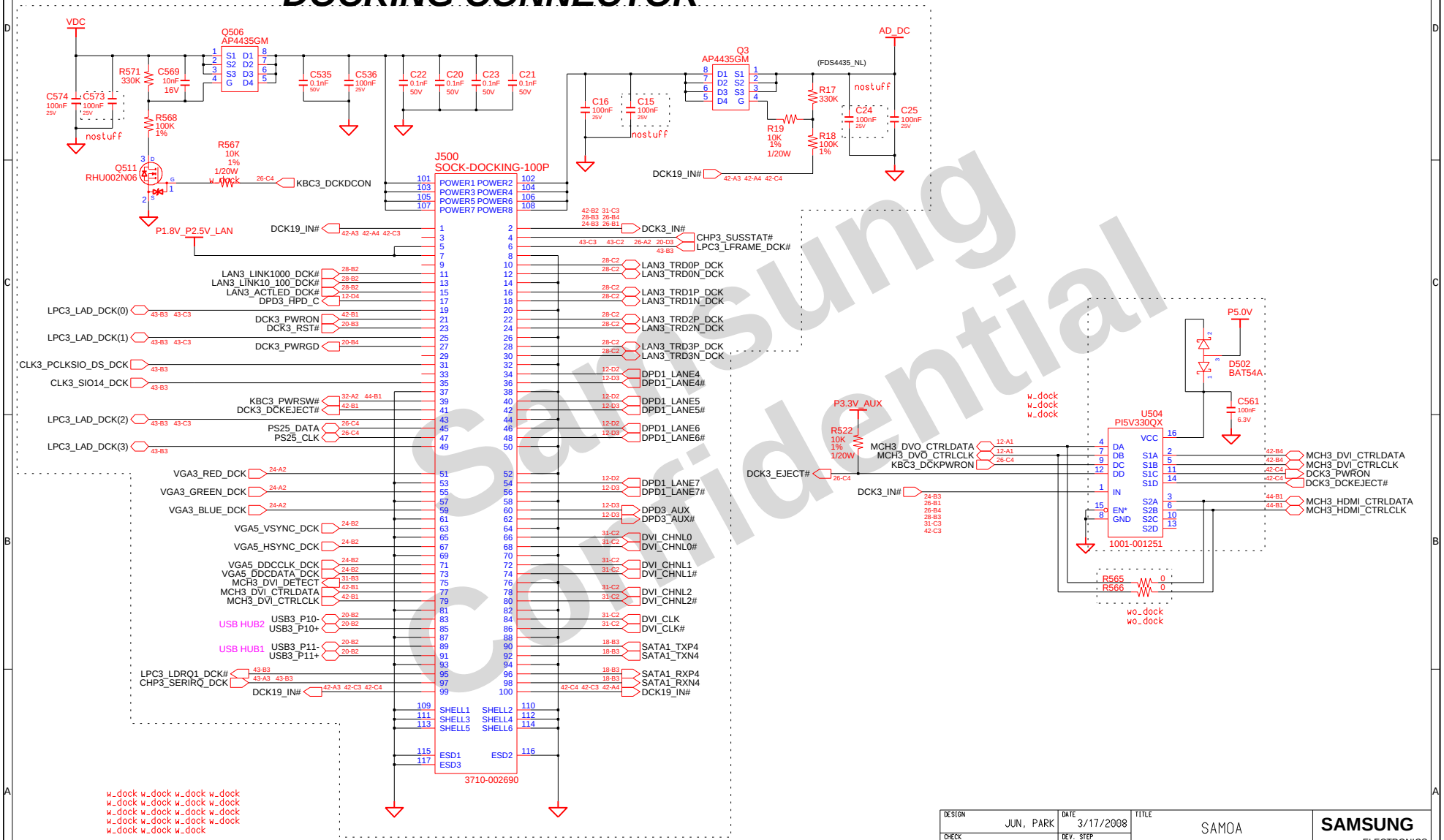
DOCKING CONNECTOR



DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN DOCKING I/F	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
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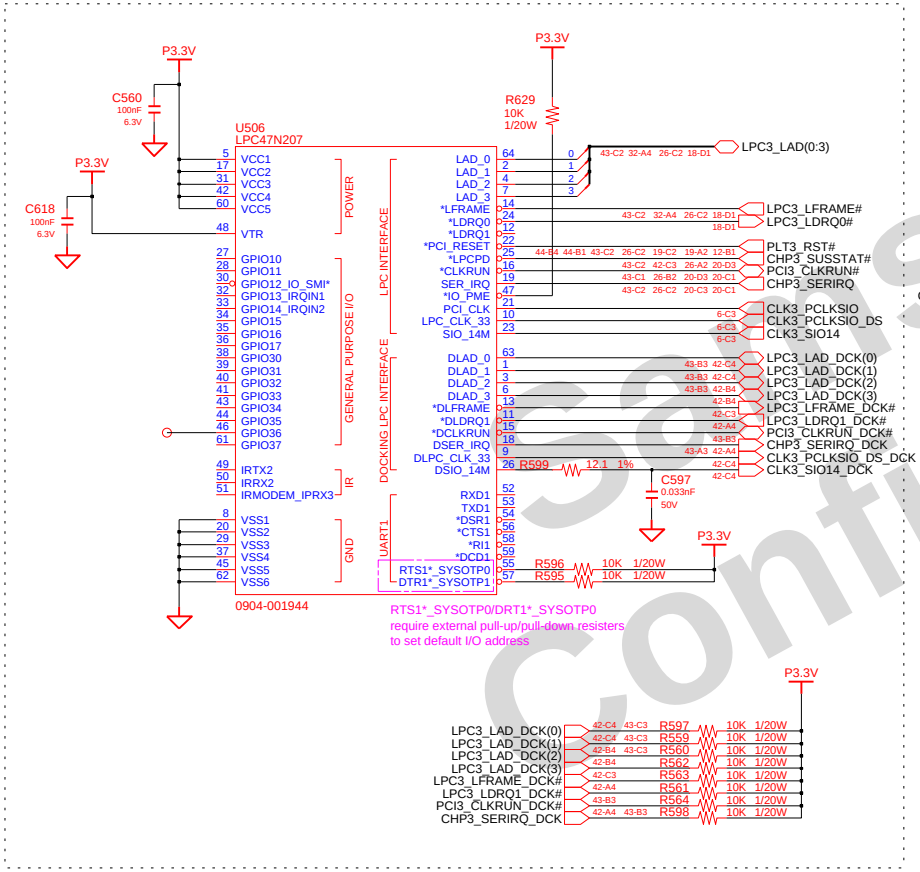
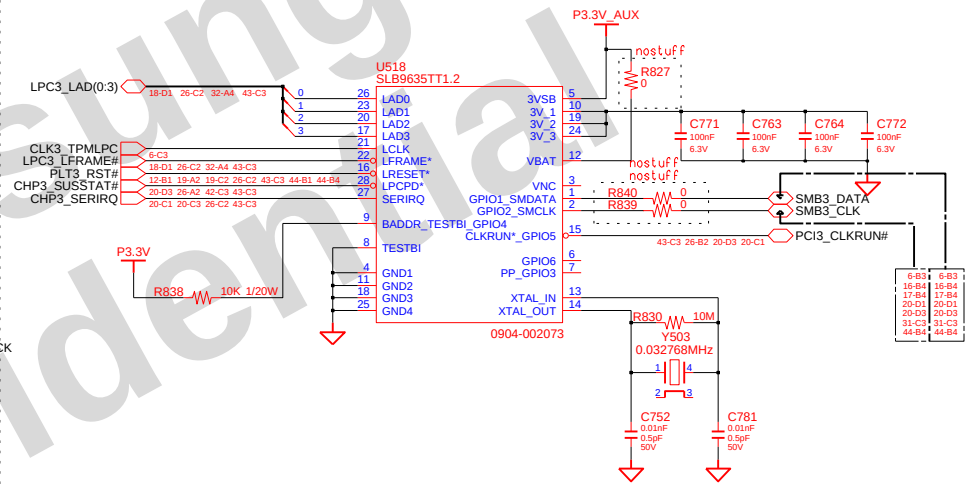
LPC I/F



TPM 1.2



w_dock w_dock
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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN LPC I/F	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
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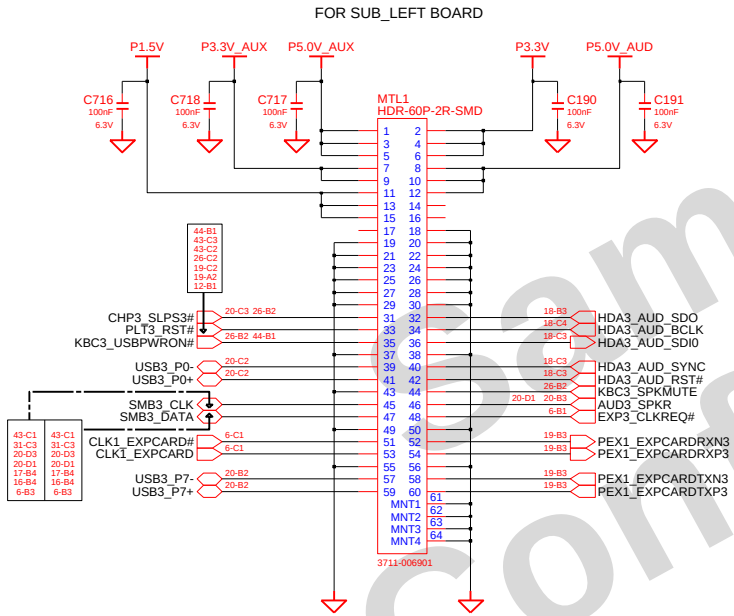
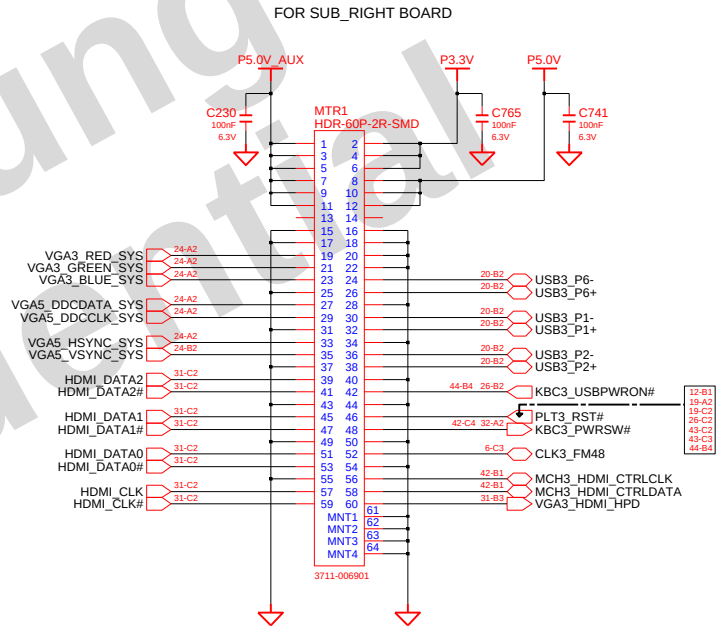
MAIN to SUB CONNECTOR





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DESIGN: JUN, PARK	DATE: 1/4/2008	TITLE: SAMOA MAIN LEFT SUB CONNECTOR	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO. BA41-0XXXXA
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SAMOA SUB

CPU : PENRYN SFF
Chip Set : CANTIGA GS & ICH9M SFF
Remarks : INTEL MONTEVINA SFF

Model Name : SAMOA SUB BOARD
PCB Code : BA41-00903A(Nanya_CHN)
BA41-00904A(GCE_CHN)
Dev. Step : PR/MP
Revision : 1.1
T.R. Date :

DESIGN	CHECK	APPROVAL
Jun PARK	HJ KIM	JS EUH

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CHECK: HJ, KIM	DEV. STEP: MP		PART NO. BA41-#####A
APPROVAL: JS, EUH	REV: 1.1		
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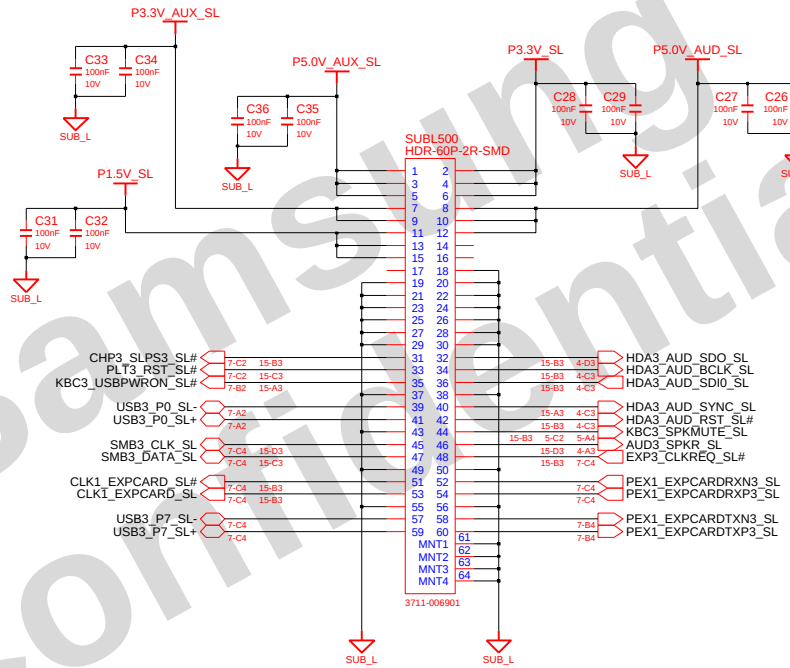
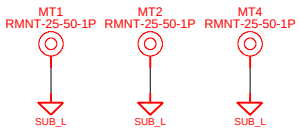
MAIN to SUB CONNECTOR(SUB_L)





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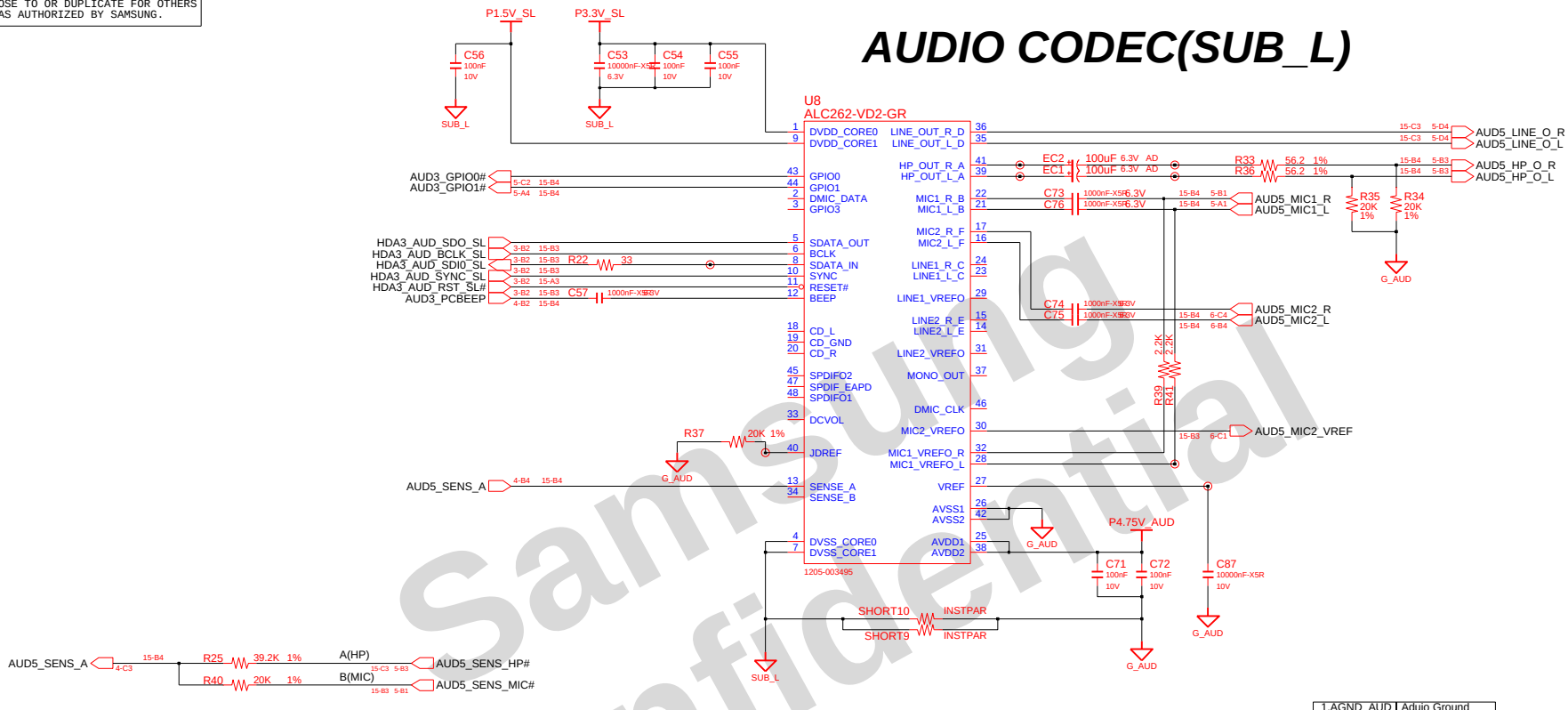
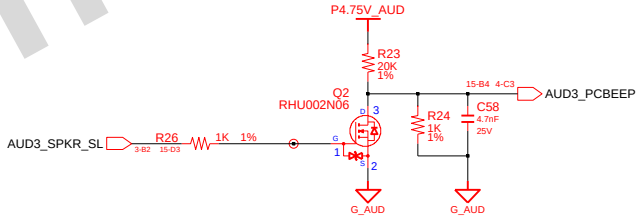
AUDIO CODEC(SUB_L)

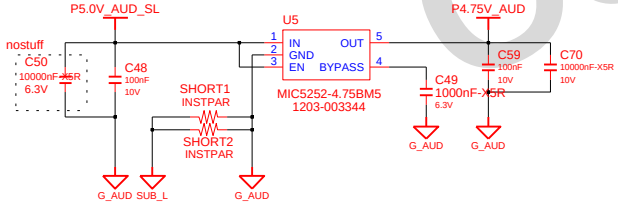


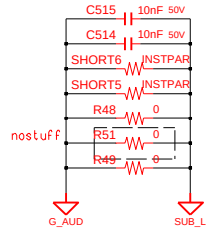
1.AGND_AUD	Aduio Ground
2.GND	Digital Ground

ALL 1608 SIZE

PC BEEP SOUND(SUB_L)







DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB LEFT AUDIO CONDEC	SAMSUNG ELECTRONICS
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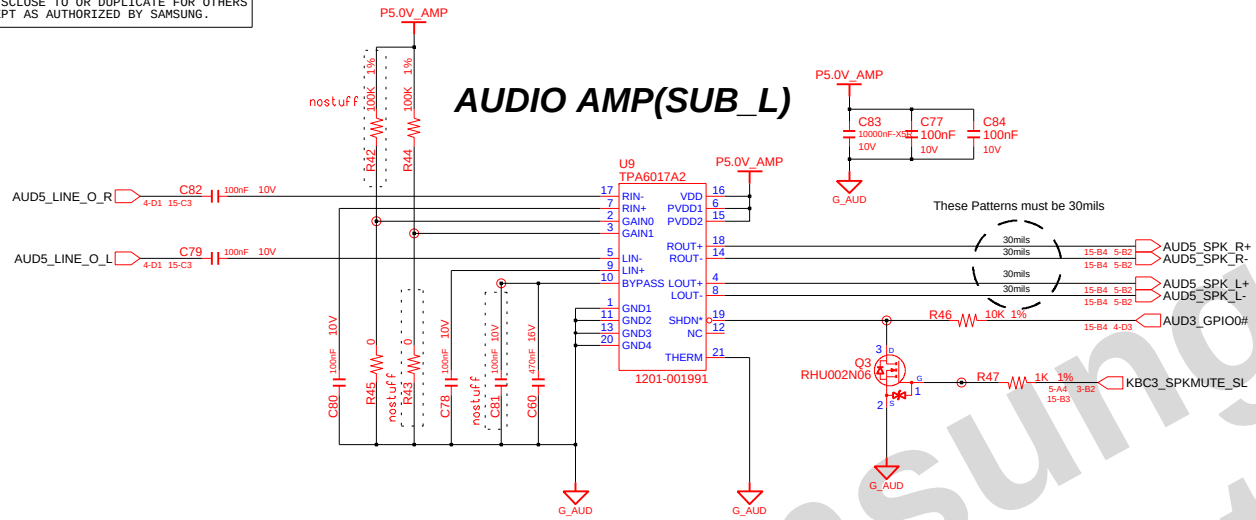

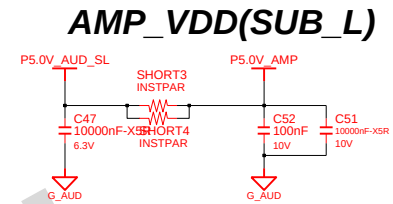

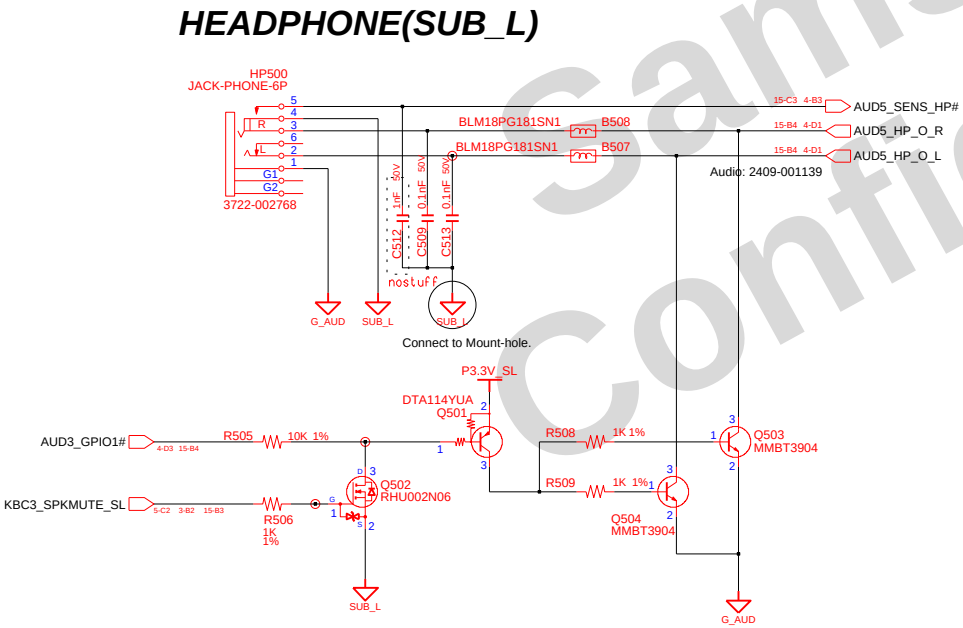

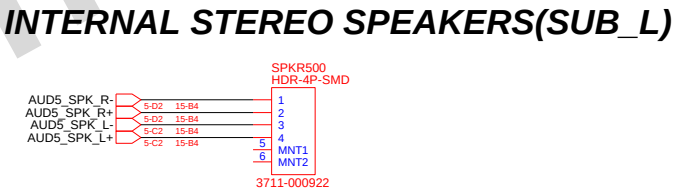

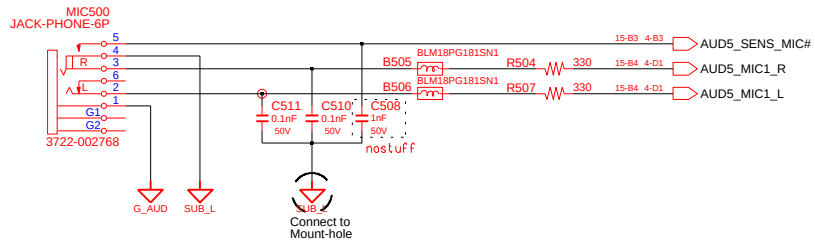

DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB LEFT AUDIO AMP & JACK	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS, EUH	REV: 1.1		PART NO. BA41-#####A
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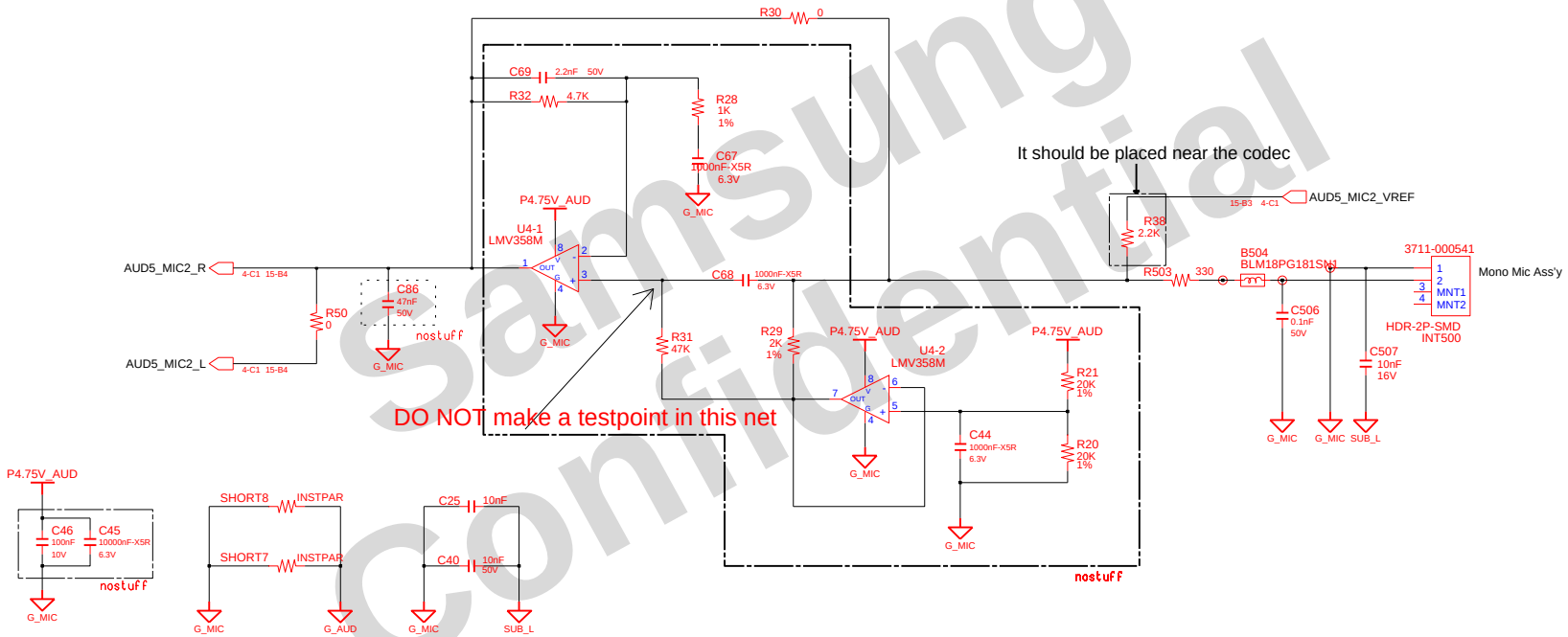
INTERNAL MIC(SUB_L)



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DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB LEFT INTERNAL MIC	SAMSUNG ELECTRONICS
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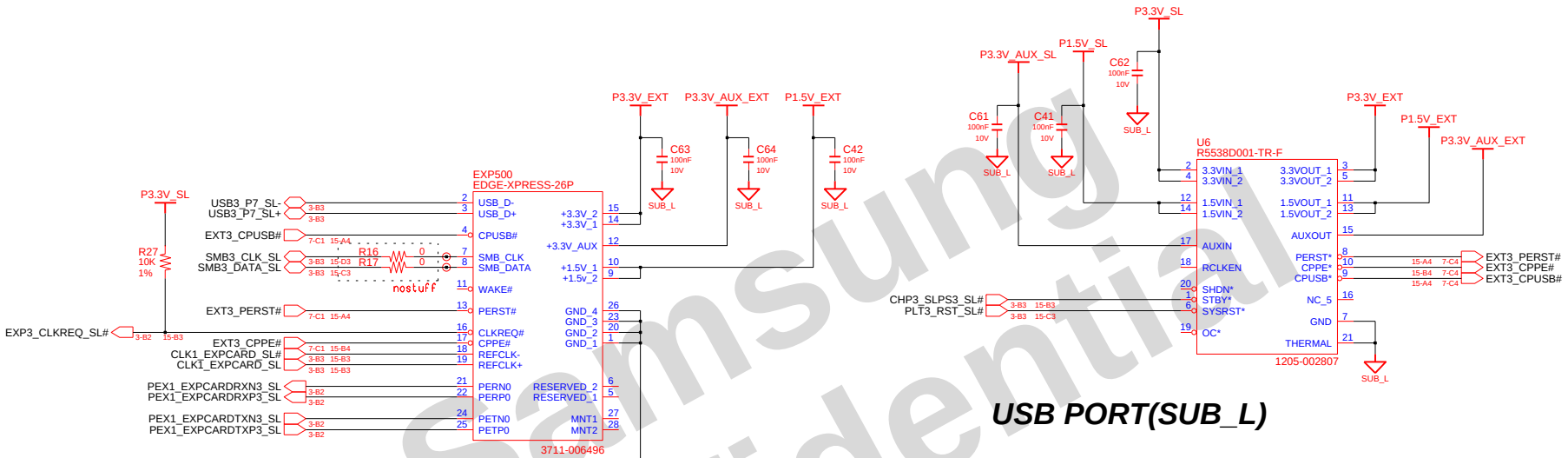
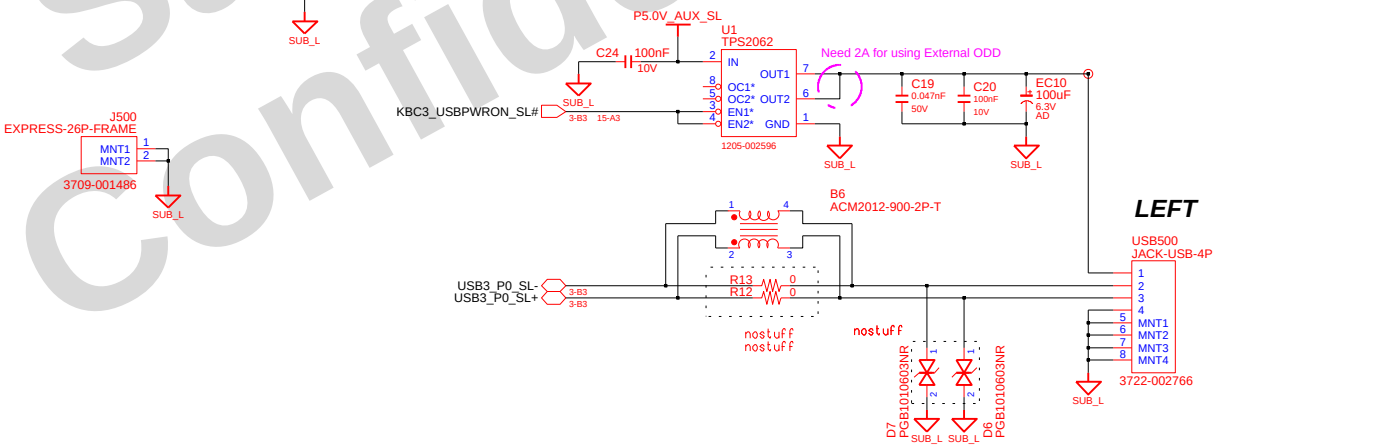
EXPRESS CARD(SUB_L)



USB PORT(SUB_L)



DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB LEFT EXPRESS CARD & USB PORT	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS, EUH	REV: 1.1		PART NO. BA41-#####A
MODULE CODE	LAST EDIT: August 22, 2008 10:42:11 AM		PAGE 7 OF 15

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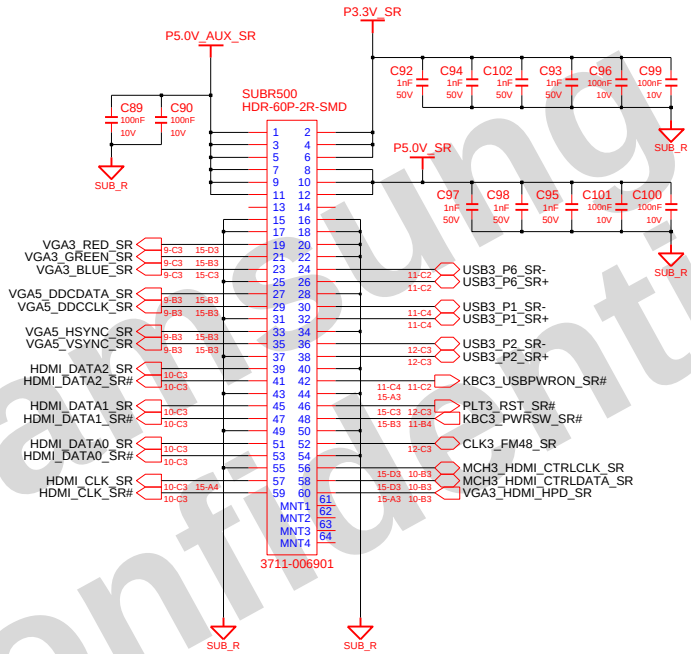
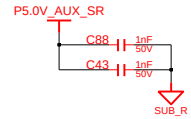
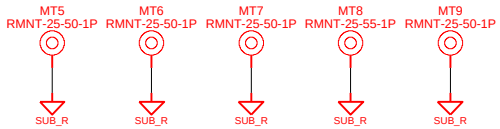
MAIN to SUB CONNECTOR(SUB_R)



Stiching caps(For EMC)





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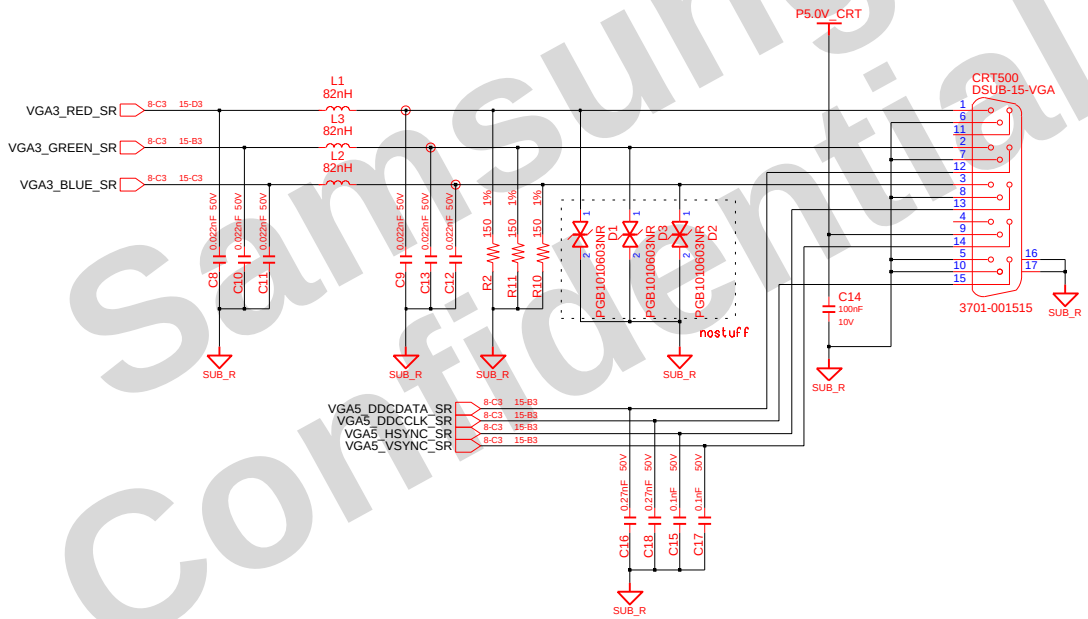
CRT CONNECTOR(SUB_R)



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DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB RIGHT CRT CONNECTOR	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
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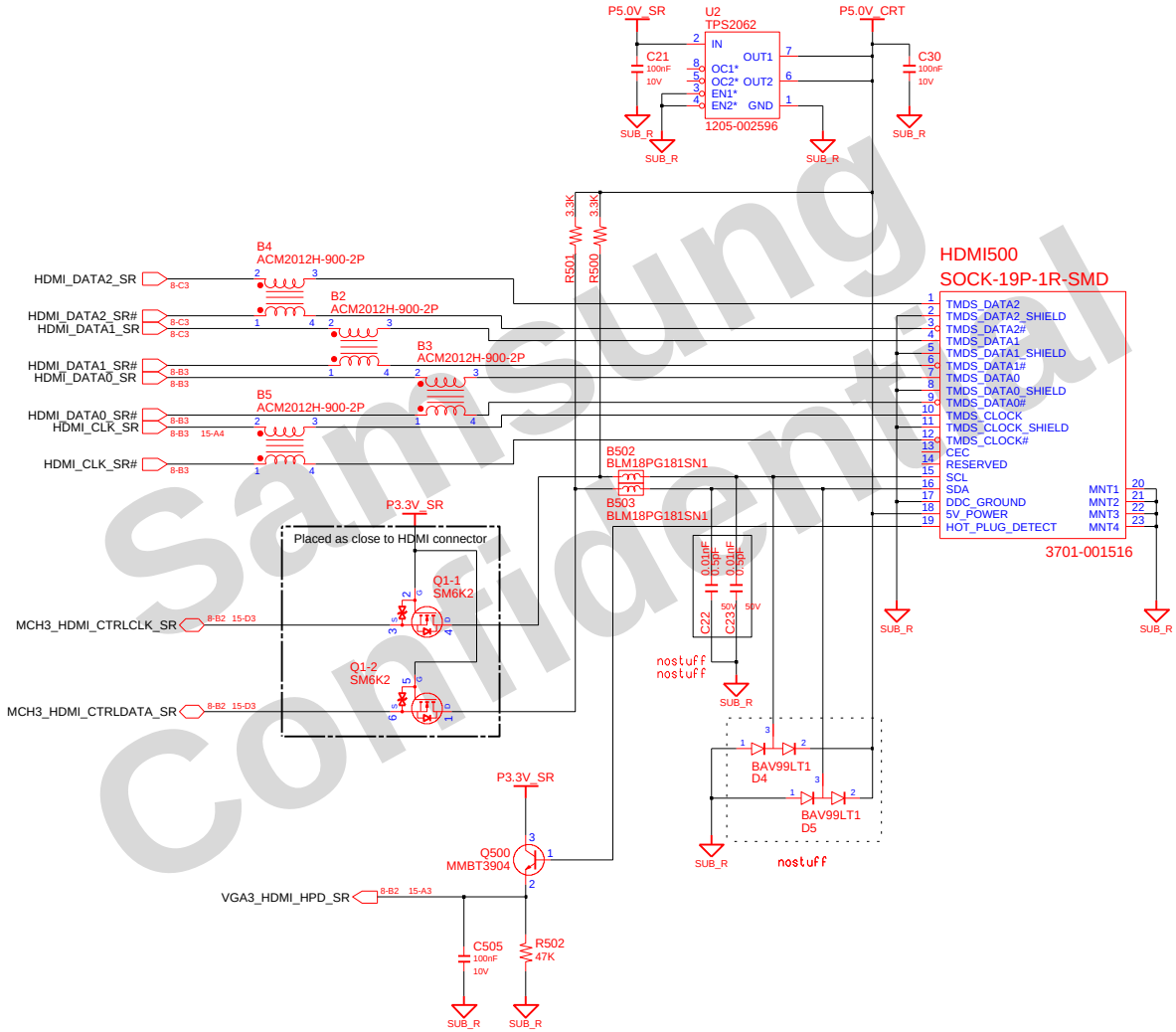
HDMI CONNECTOR(SUB_R)



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DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB RIGHT HDMI CONNECTOR	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS, EUH	REV: 1.1		PART NO. BA41-#####A
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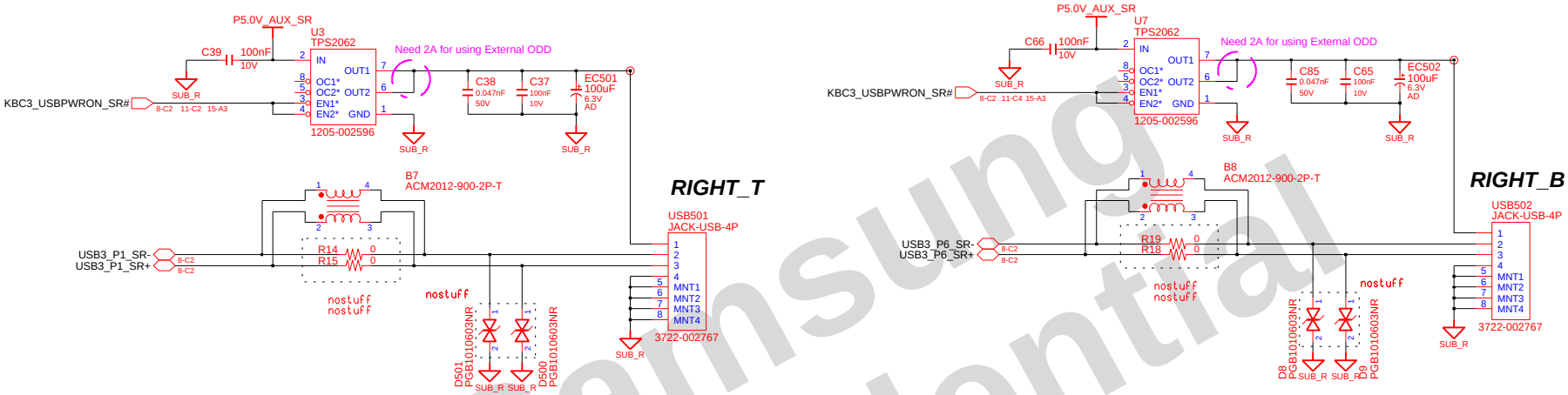
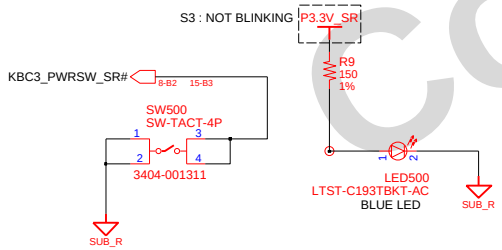
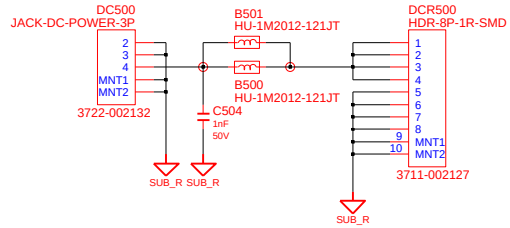
USB PORT(SUB_R)



POWER S/W(SUB_R)



DC JACK(SUB_R)



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DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB RIGHT USB,POWER S/W&DC JACK	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS, EUH	REV: 1.1		PART NO. BA41-#####A
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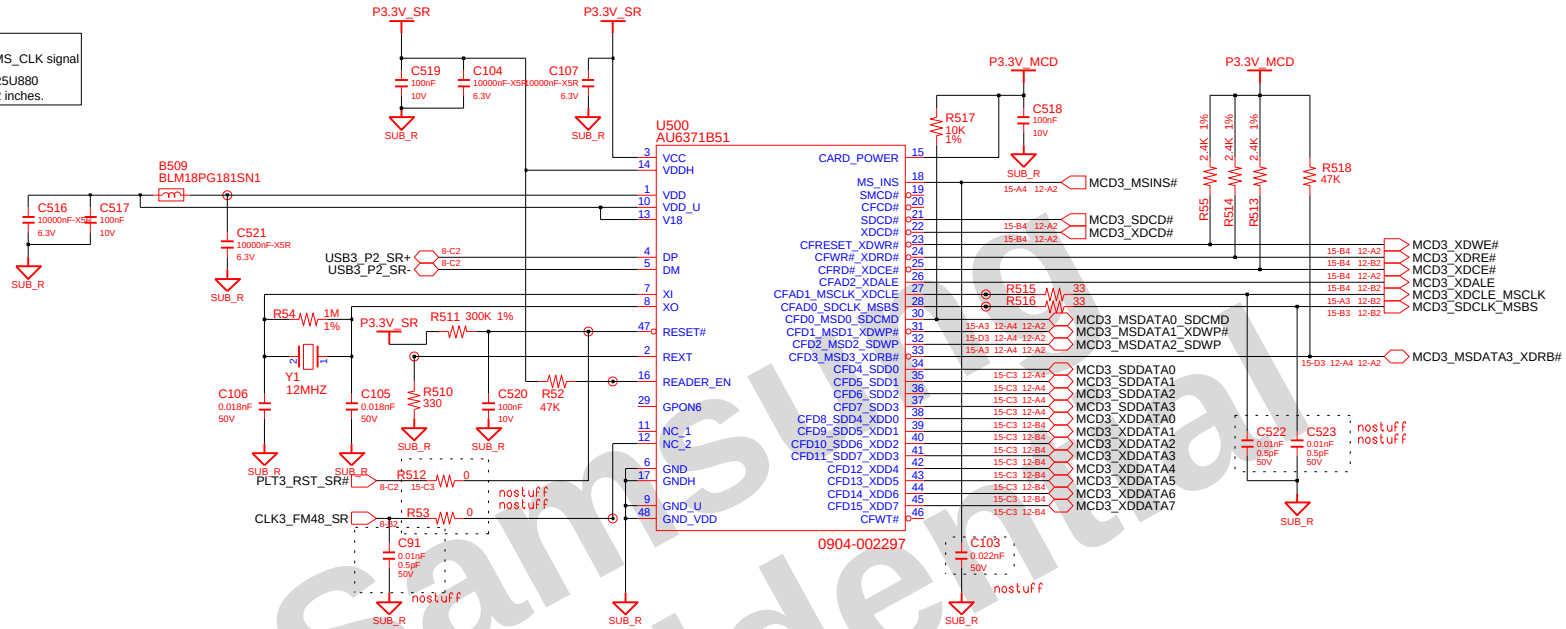
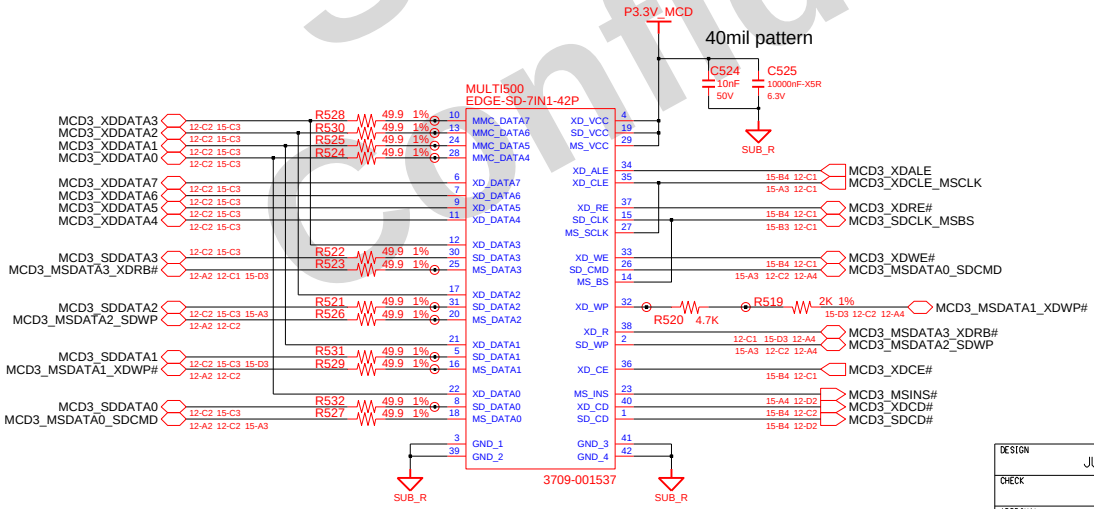
CARD READER(AU6371, SUB_R)

40mil pattern
Apply shield GND for SD/MMC/MS_CLK signal
P3.3V_MCD distance between R5U880 and socket should be less than 2 inches.





40 mil trace for medica card socket ground

DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB RIGHT CARD READER & 7-IN-1	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		PART NO. BA41-#####A
APPROVAL: JS, EUH	REV: 1.1		
MODULE CODE	LAST EDIT: August 22, 2008 10:42:11 AM	PAGE 12 OF 15	

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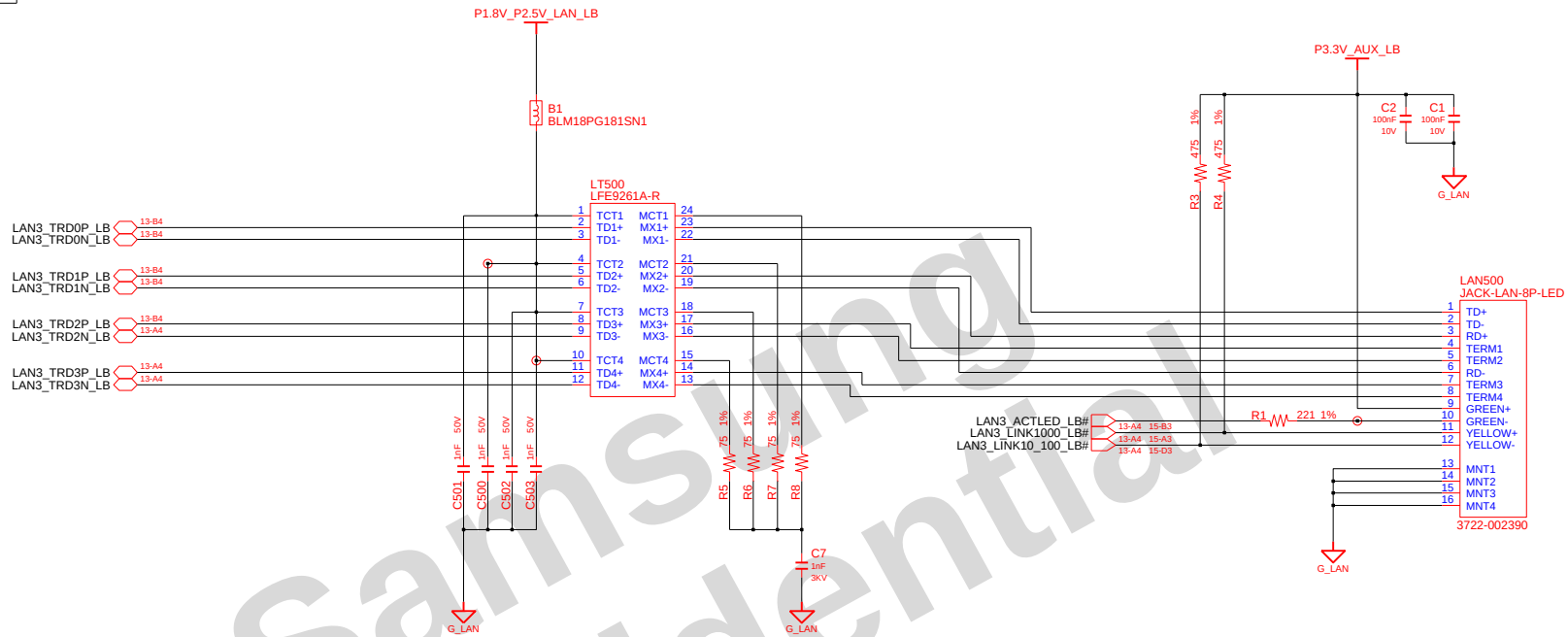
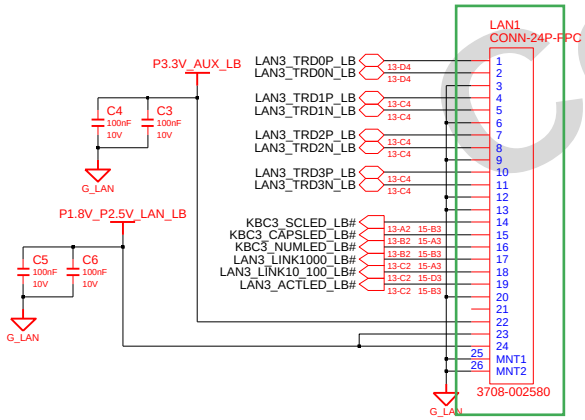
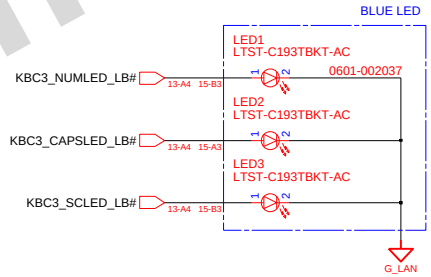
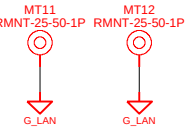
LAN JACK BOARD



LAN SUB BOARD CONNECTOR







DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB LAN LAN I/F	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		PART NO. BA41-#####A
APPROVAL: JS, EUH	REV: 1.1		
MODULE CODE	LAST EDIT: August 22, 2008 10:42:11 AM	PAGE 13 OF 15	

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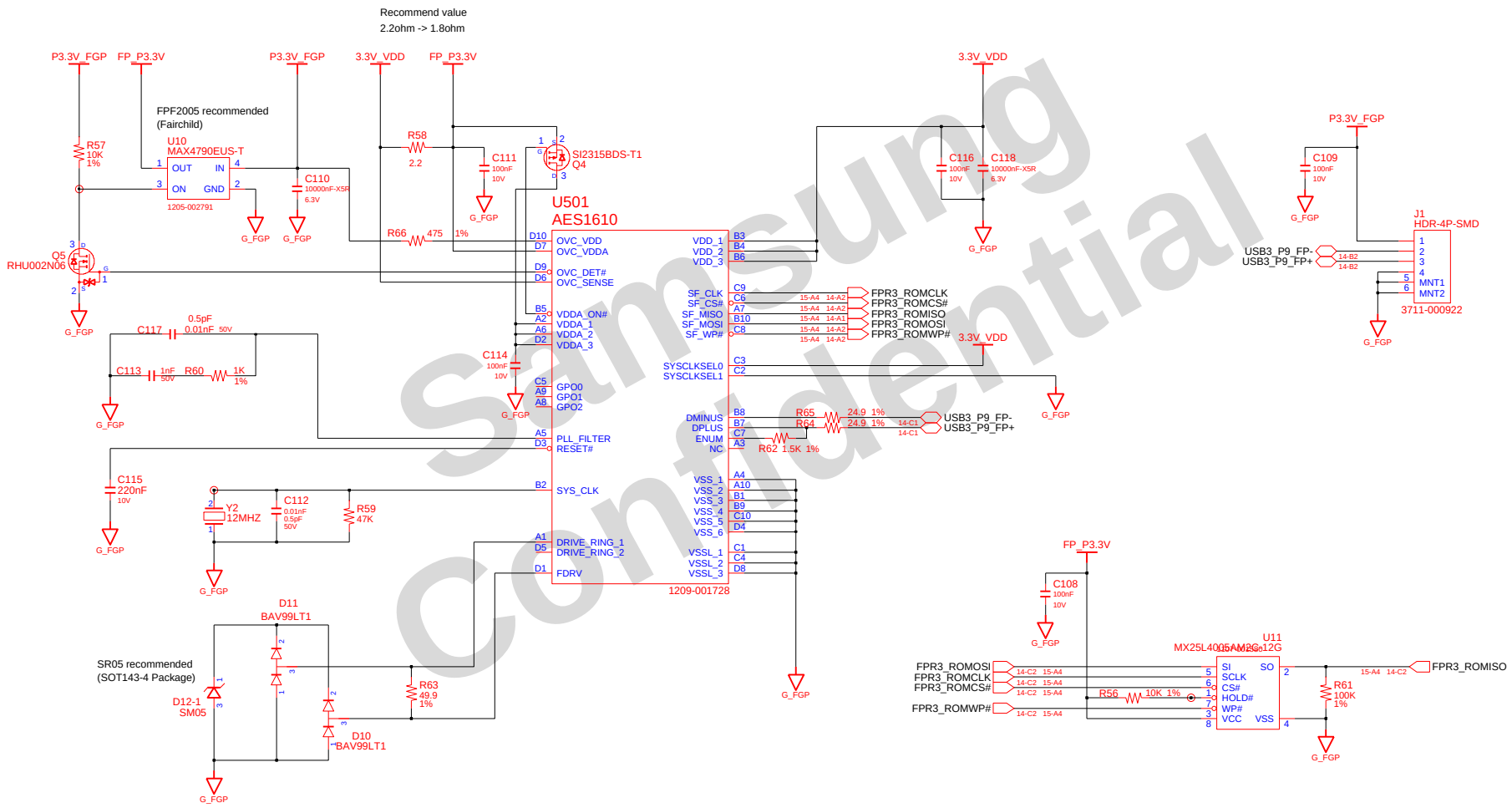
FINGER PRINT BOARD



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DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB FINGER PRINT FINGER PRINT I/F	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		PART NO. BA41-#####A
APPROVAL: JS, EUH	REV: 1.1		
MODULE CODE	LAST EDIT: August 22, 2008 10:42:11 AM		PAGE 14 OF 15