

10.

10-1 MAIN BOARD

10-1-1 Schematic Diagrams

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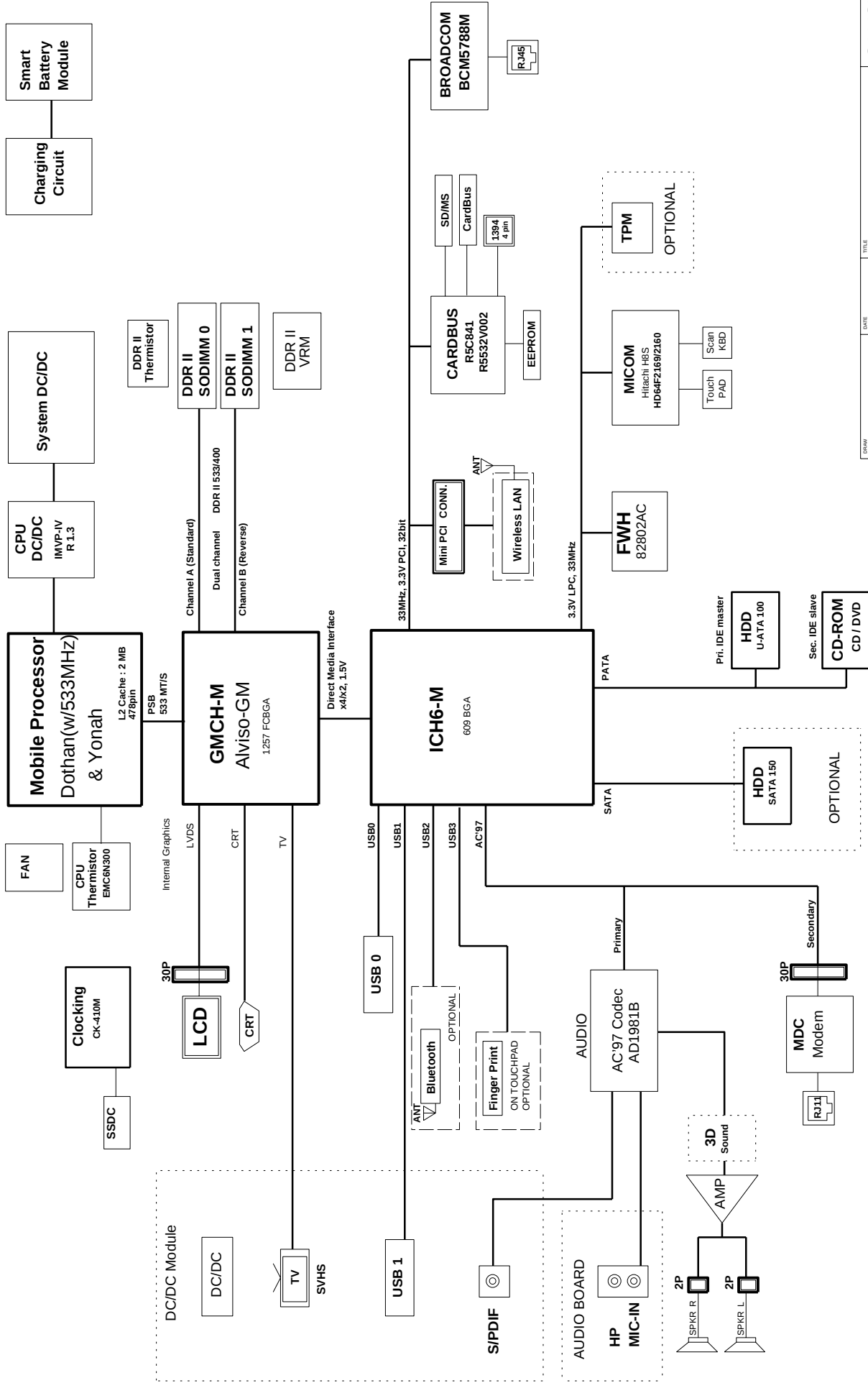
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Aquila-So

CPU : Dothan
Chip Set : Intel Alviso + ICH6-M
Remarks : Internal Gfx.

Model Name : X06
PBA Name : BA92-03859A
PCB Code : BA41-00529A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2005-6-25

DRAW	CHECK	APPROVAL
ZHOU JUN GUO LEI	CHEN TAO	KEVIN LEE



DATE	6/25/2005	TITLE	SAMSUNG ELECTRONICS
CHECK	ANTONIO	CHK. STEP	MP
APPROVAL	KEVIN LEE	REV	1.0
MODULE CODE		LAST EDIT	June 25, 2005 12:21:39 PM
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			OPERATION BLOCK DIAGM
			BA41-00529A
			MAIN
			AQUILA-SONOMA

External PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus MiniPCI SLOT LOM	AD25	0	A B C
	AD23	1	E F
	AD21	2	G

Devices	Address	Hex	Bus
ICH6-M	Master	-	SMbus Master
CK-410 (Clock Generator)	1101 001x	D2h	Clock, Unused
CY2592-3ZC(Spread Spectrum)	1101 010x	D4h	Clock Output
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 010x	A4h	-
MICOM	Master	-	SMbus Master
EMCNS300(Termal Sensor)	0001 011x	5Eh	Thermal Sensor
BATTERY	0001 16h	-	BATTERY INFORMATION

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1	SYSTEM PORT B
2 (OPTION)	BLUETOOTH (OPTION)
3 (OPTION)	FINGER PRINTER (OPTION)

VCC_VCC_CORE	Primary/DC system power supply (7 to 21V)
VTT	Core voltage for DOTHAN CPU (1.356 - 0.844V)
P15V_AUX	Processor System Bus(PSB) Termination (1.05V) MCH-M Core Voltage (1.05V)
P09V	1.5V switched power rail (off in S3-S5)
P18V_AUX	1.5V power rail (off in S4-S5)
MICOM_P3V	0.9V power rail (off in S3-S5)
P33V_P3V_AUX	1.8V power rail(off in S4-S5)
P33V_P3V_ALWAYS	3.3V always on power rail for MICOM
P33V_P3V_ALWAYS	3.3V switched power rail (off in S3-S5)
P33V_P3V_ALWAYS	3.3V power rail (off in S4-S5)
P33V_P3V_ALWAYS	3.3V power rail (Always on!AC-IN mode & off in S4-S5@BATT mode)
P5V_AUX	5.0V switched power rail (off in S3-S5)
P2.5V	5V power rail (off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)

See revision notes in the changes file for more information.

Sleep Stage Progression									
Stage 1 (Light Sleep)					Stage 2 (Moderate Sleep)				
Time	Heart Rate (bpm)	Respiration Rate (breaths/min)	Temperature (°C)	Electrical Activity	Time	Heart Rate (bpm)	Respiration Rate (breaths/min)	Temperature (°C)	Electrical Activity
00:00	78	12	36.5	Alpha waves	00:05	75	10	36.8	Delta waves
00:10	72	10	37.0	Theta waves	00:15	70	8	37.2	Delta waves
00:20	68	8	37.5	Theta waves	00:25	65	6	37.8	Delta waves
00:30	65	6	38.0	Theta waves	00:35	62	4	38.2	Delta waves
00:40	60	4	38.5	Theta waves	00:45	58	3	38.5	Delta waves
00:50	58	3	38.8	Theta waves	00:55	55	2	38.8	Delta waves
01:00	55	2	39.0	Theta waves	01:05	52	1	39.2	Delta waves
01:10	50	1	39.5	Theta waves	01:15	48	1	39.8	Delta waves
01:20	48	1	40.0	Theta waves	01:25	45	0	40.2	Delta waves
01:30	45	0	40.5	Theta waves	01:35	42	0	40.5	Delta waves
01:40	42	0	40.8	Theta waves	01:45	40	0	40.8	Delta waves
01:50	40	0	41.0	Theta waves	01:55	38	0	41.2	Delta waves
02:00	38	0	41.5	Theta waves	02:05	35	0	41.8	Delta waves
02:10	35	0	42.0	Theta waves	02:15	32	0	42.2	Delta waves
02:20	32	0	42.5	Theta waves	02:25	30	0	42.5	Delta waves
02:30	30	0	42.8	Theta waves	02:35	28	0	42.8	Delta waves
02:40	28	0	43.0	Theta waves	02:45	25	0	43.2	Delta waves
02:50	25	0	43.5	Theta waves	02:55	22	0	43.5	Delta waves
03:00	22	0	43.8	Theta waves	03:05	20	0	43.8	Delta waves
03:10	20	0	44.0	Theta waves	03:15	18	0	44.0	Delta waves
03:20	18	0	44.2	Theta waves	03:25	15	0	44.2	Delta waves
03:30	15	0	44.5	Theta waves	03:35	12	0	44.5	Delta waves
03:40	12	0	44.8	Theta waves	03:45	10	0	44.8	Delta waves
03:50	10	0	45.0	Theta waves	03:55	8	0	45.0	Delta waves
04:00	8	0	45.2	Theta waves	04:05	5	0	45.2	Delta waves
04:10	5	0	45.5	Theta waves	04:15	3	0	45.5	Delta waves
04:20	3	0	45.8	Theta waves	04:25	2	0	45.8	Delta waves
04:30	2	0	46.0	Theta waves	04:35	1	0	46.0	Delta waves
04:40	1	0	46.2	Theta waves	04:45	0	0	46.2	Delta waves
04:50	0	0	46.5	Theta waves	04:55	0	0	46.5	Delta waves
05:00	0	0	46.8	Theta waves	05:05	0	0	46.8	Delta waves
05:10	0	0	47.0	Theta waves	05:15	0	0	47.0	Delta waves
05:20	0	0	47.2	Theta waves	05:25	0	0	47.2	Delta waves
05:30	0	0	47.5	Theta waves	05:35	0	0	47.5	Delta waves
05:40	0	0	47.8	Theta waves	05:45	0	0	47.8	Delta waves
05:50	0	0	48.0	Theta waves	05:55	0	0	48.0	Delta waves
06:00	0	0	48.2	Theta waves	06:05	0	0	48.2	Delta waves
06:10	0	0	48.5	Theta waves	06:15	0	0	48.5	Delta waves
06:20	0	0	48.8	Theta waves	06:25	0	0	48.8	Delta waves
06:30	0	0	49.0	Theta waves	06:35	0	0	49.0	Delta waves
06:40	0	0	49.2	Theta waves	06:45	0	0	49.2	Delta waves
06:50	0	0	49.5	Theta waves	06:55	0	0	49.5	Delta waves
07:00	0	0	49.8	Theta waves	07:05	0	0	49.8	Delta waves
07:10	0	0	50.0	Theta waves	07:15	0	0	50.0	Delta waves
07:20	0	0	50.2	Theta waves	07:25	0	0	50.2	Delta waves
07:30	0	0	50.5	Theta waves	07:35	0	0	50.5	Delta waves
07:40	0	0	50.8	Theta waves	07:45	0	0	50.8	Delta waves
07:50	0	0	51.0	Theta waves	07:55	0	0	51.0	Delta waves
08:00	0	0	51.2	Theta waves	08:05	0	0</		

Signal	SLP_S3#	SLP_S4#	SLP_S5#	+V _{ALW}	+V ₊	+V _S	Clocks
S0 (Full On)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3-Hot (STR)	LOW	HIGH	HIGH	ON	ON	ON	LOW
S3-Cold (STR)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (STD)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	ON	OFF	OFF	OFF

DATE		6/25/2005	TITLE		SAMSUNG ELECTRONICS PART NO. BA41-00529A
DRAMA	ZHOU & GUO	DIS. STEP	MP	AQUILA-SONOMA MAIN BOARD INFORMATION	
CHECK	ANTONIO	REV	1.0		
APPROVAL	KEVIN LEE	LAST EDIT			
MODULE CODE	June 25, 2005 12:21:39 PM				
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ADAPTOR
BATTERY

ALWAYS

P3.3V_ALWAYS

BRIDGE
BATTERY

VDC

MICOM_P3V

KBC3_SUSPWR

P1.5V_AUX

ICH6-M

P3.3V_AUX

ICH6-M

MDC

BT

P2.5V

ALVISO-GM

ICH6-M

R5C841

P5V

ICH6-M

ODD

CRT

R5C841

P5V_AUX

DDR Power

P1.8V_AUX

SODIMM (DDR I)

ALVISO-GM

P0.9V

DDR I1-Termination

VTT

CPU VCCP

GMCH VCC_MCH

VCC_CORE
DOTHAN633 / YONAH

KBC3_PWRON

P1.5V

ALVISO-GM

ICH6-M

P3.3V

ALVISO-GM

ICH6-M

CK410-M

LCD

MDC

P2.5V

ALVISO-GM

ICH6-M

R5C841

P5V

ICH6-M

ODD

CRT

R5C841

P5V_AUX

DDR Power

P1.8V_AUX

SODIMM (DDR I)

ALVISO-GM

P0.9V

DDR I1-Termination

VTT

CPU VCCP

GMCH VCC_MCH

KBC3_VRON

P1.5V

ALVISO-GM

ICH6-M

P3.3V

ALVISO-GM

ICH6-M

CK410-M

LCD

MDC

P2.5V

ALVISO-GM

ICH6-M

R5C841

P5V

ICH6-M

ODD

CRT

R5C841

P5V_AUX

DDR Power

P1.8V_AUX

SODIMM (DDR I)

ALVISO-GM

P0.9V

DDR I1-Termination

VTT

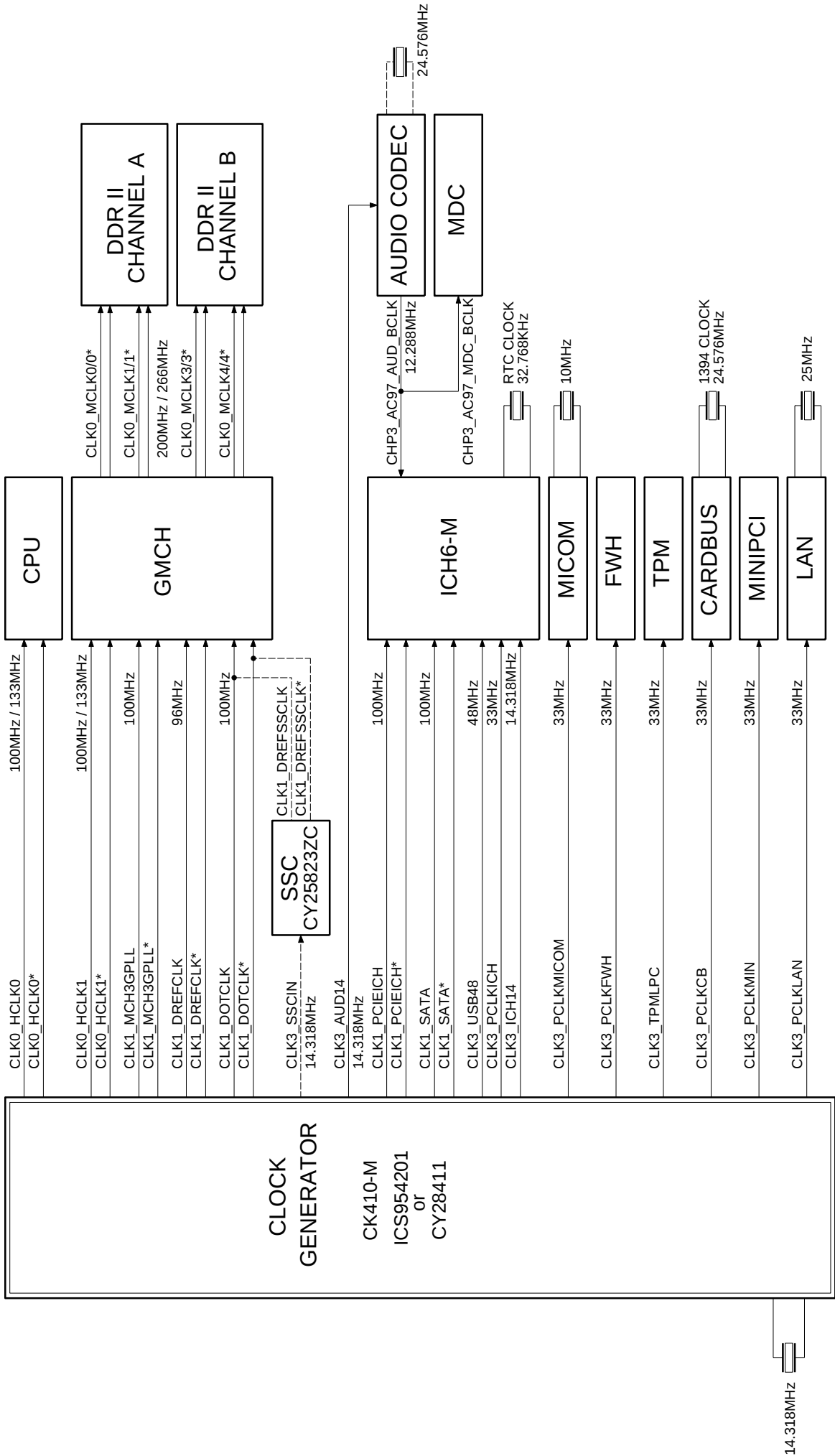
CPU VCCP

GMCH VCC_MCH

DRAWN	DATE		TITLE		SAMSUNG ELECTRONICS	
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	CHECK		DEV. STEP			
	ANTONIO		MP			
APPROVAL	REV		1.0		PART NO. BA41-00529A	
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MODULE CODE		LAST EDIT		POWER DIAGRAM		
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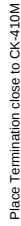


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CHECK		HOW / TIME	MP				PART NO.		
APPROVAL	ANTONIO	REV	1.0		POWER ON SEQUENCE		BA41-00529A		
MODULE CODE	KEVIN LEE	LAST EDIT					PAGE	5	OF 46
							June 25, 2005 12:21:39 PM		



DRAWN	DATE	TITLE	SAMSUNG
CHECK	6/25/2005	AQUILA-SONOMA	ELECTRONICS
APPROVAL	DRW. STOP	MAIN	
MODULE CODE	REV	CLOCK DIAGRAM	PART NO.
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	LAST EDIT		
	June 25, 2005 12:21:39 PM		
	PAGE	6	OF 46

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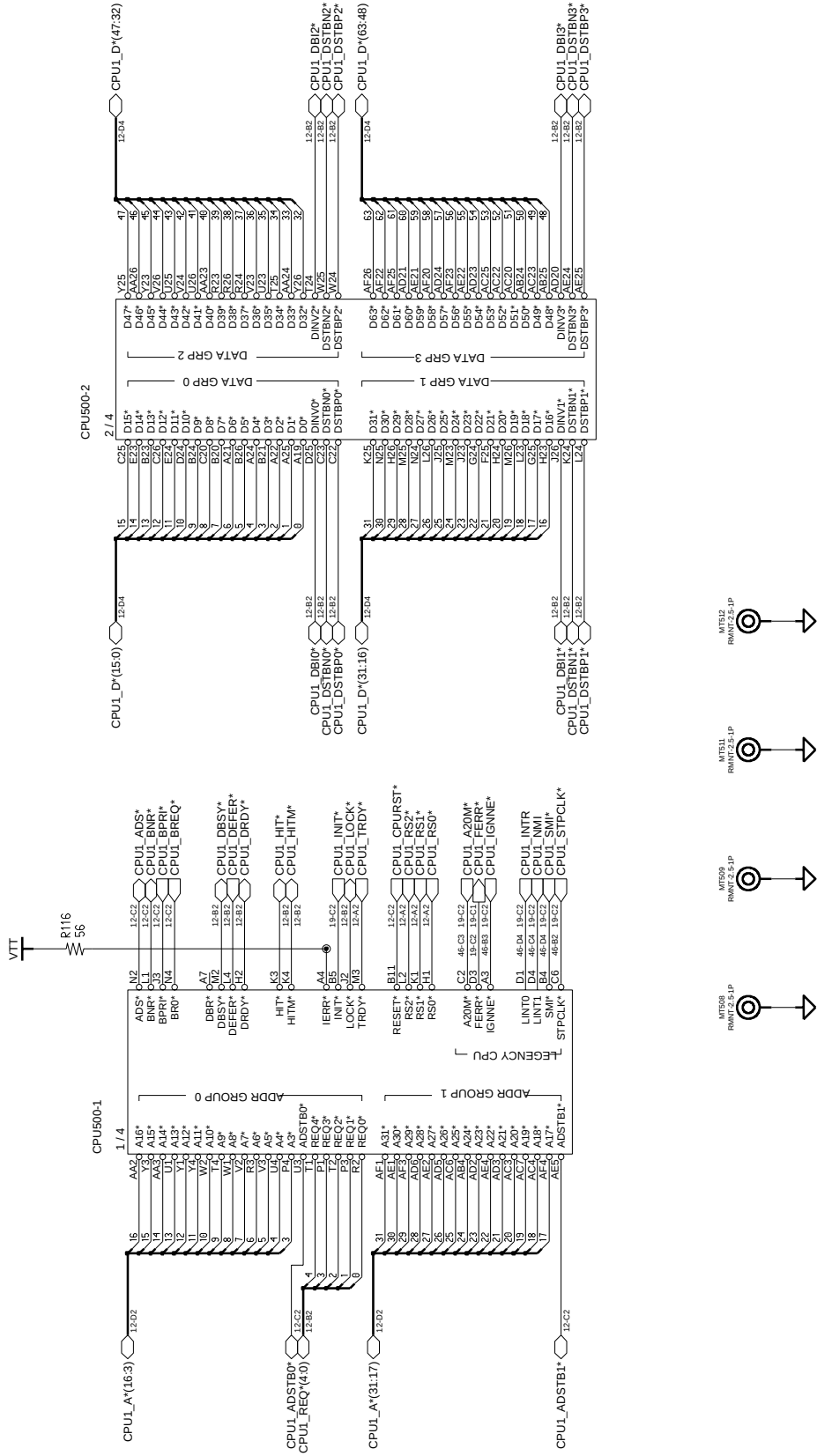


Place 14.318MHz within
500mils of CK-410M

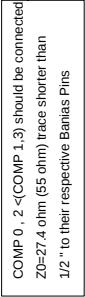
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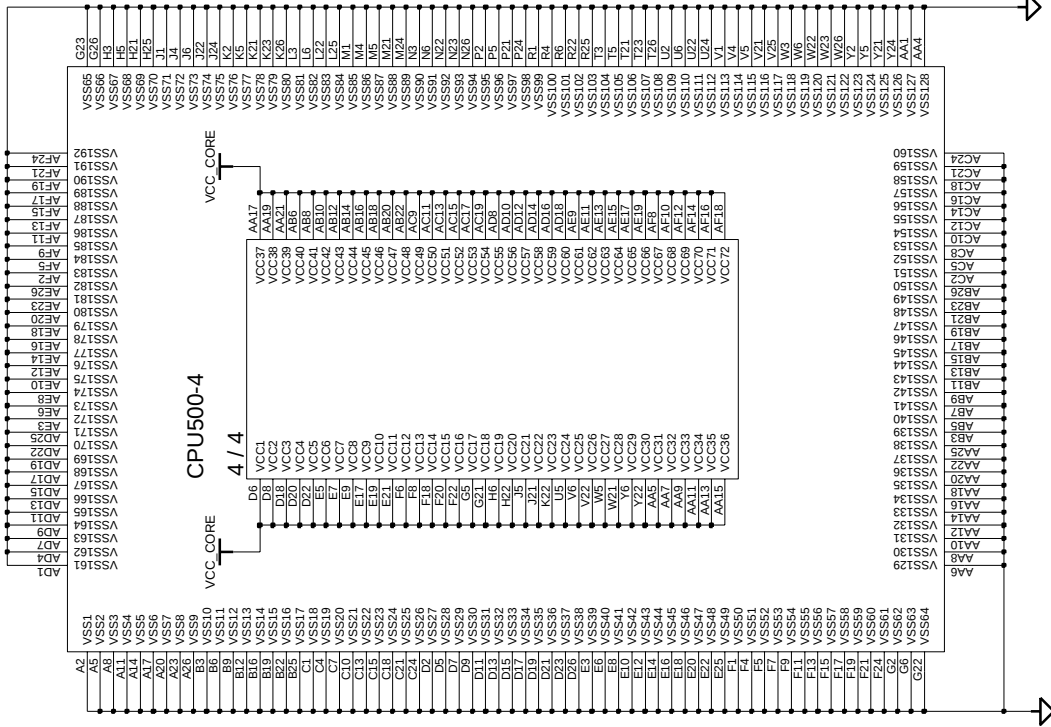
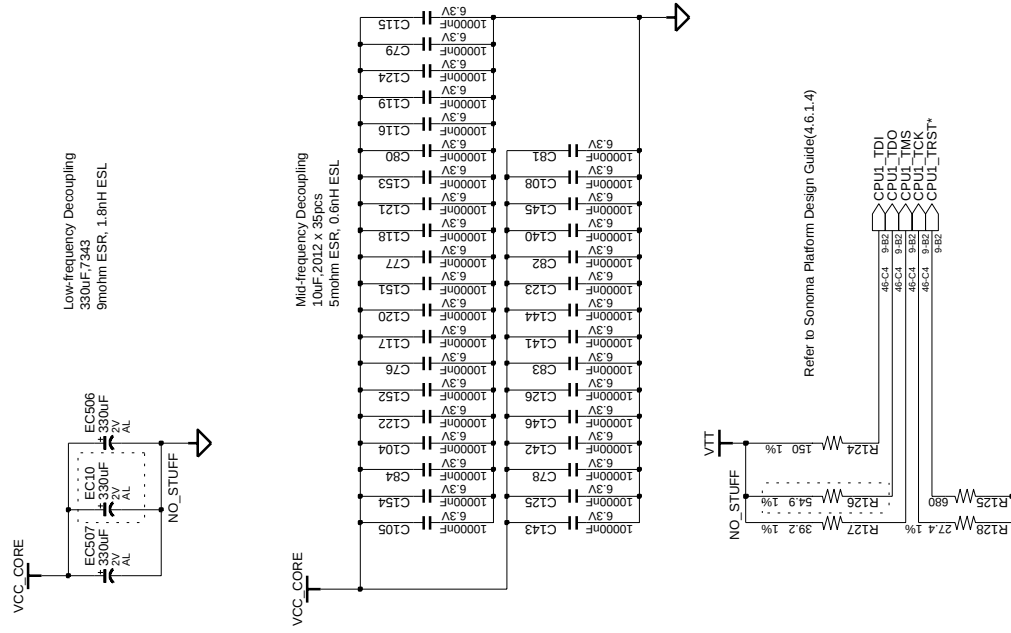
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DRAWN		DATE		TITLE	
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APPROVAL		REV		CPU (113)	
MODULE CODE		LAST EDIT		June 25, 2005 12:21:39 PM	
		PAGE		8 OF 46	

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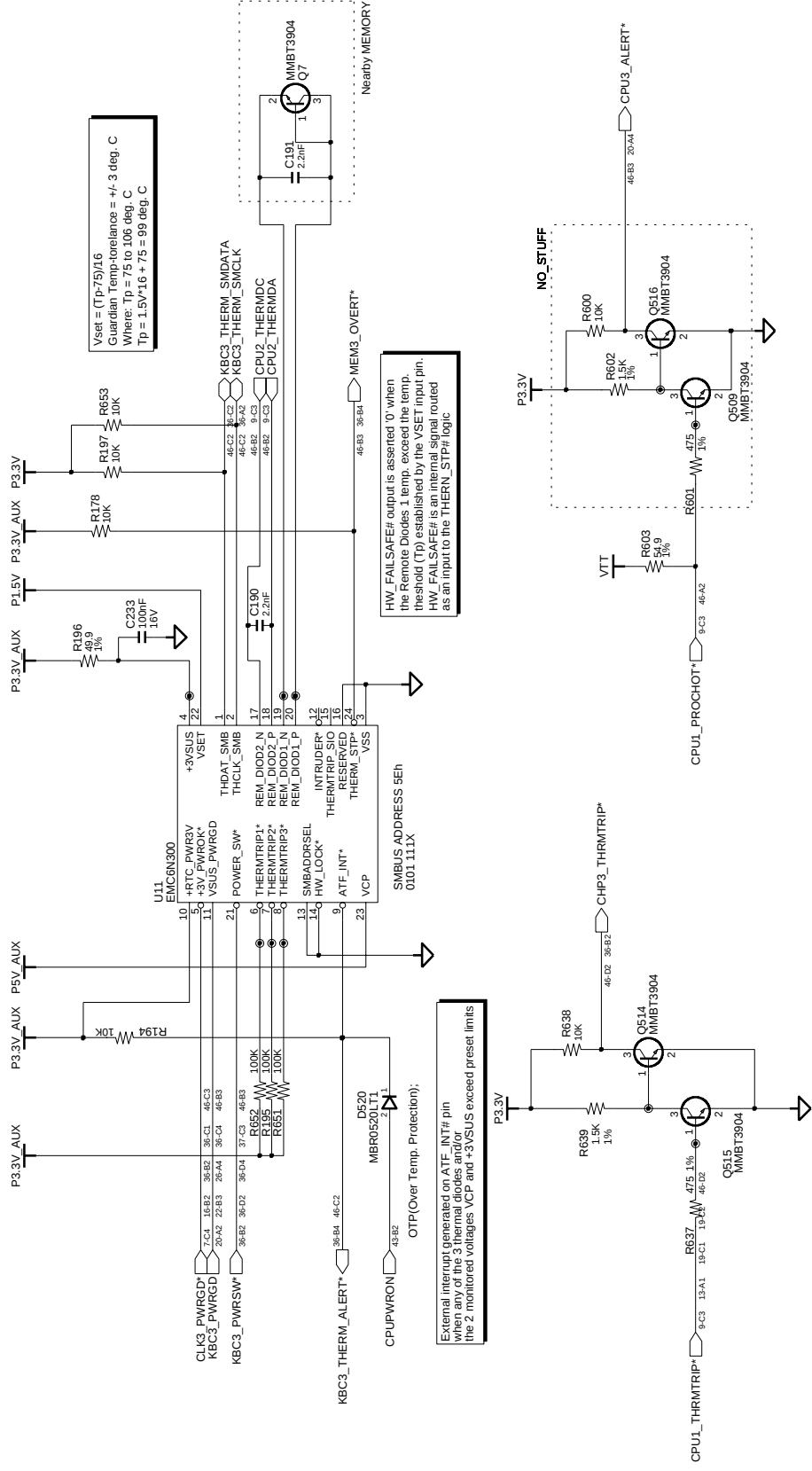
Vcc-core Decoupling (Refer to MVP-IV Option #4)



DRAWN	DATE		TITLE	
	6/25/2005		AQUILA-SONOMA	
CHECK	REV. STOP		MAIN	
	ANTONIO		CPU (3/3)	
APPROVAL	REV		1.0	
	KEVIN LEE		June 25, 2005 12:21:39 PM	
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SAMSUNG		ELECTRONICS	
PART NO.		BA41-00529A	

CPU / DDR Thermal Sensor

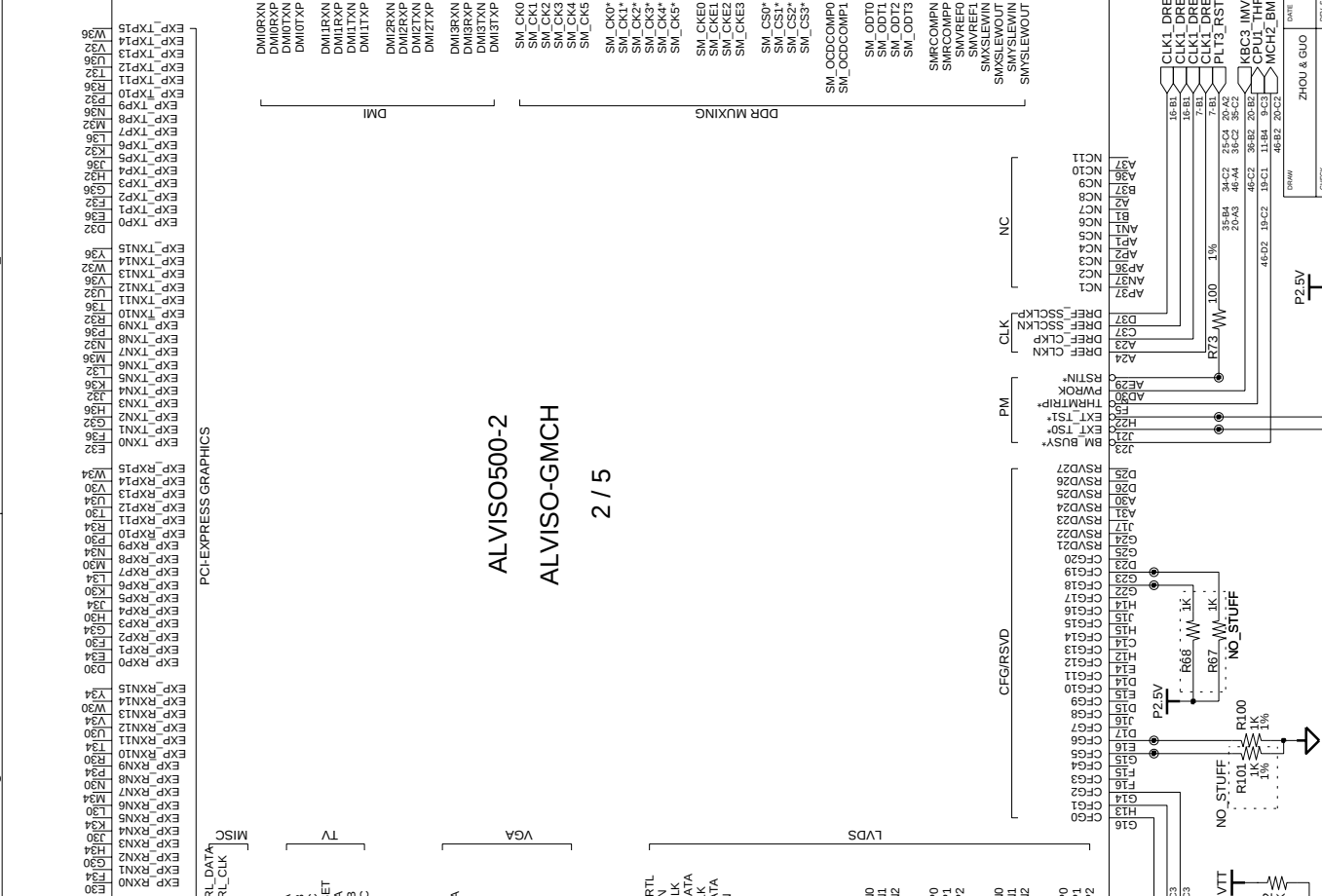
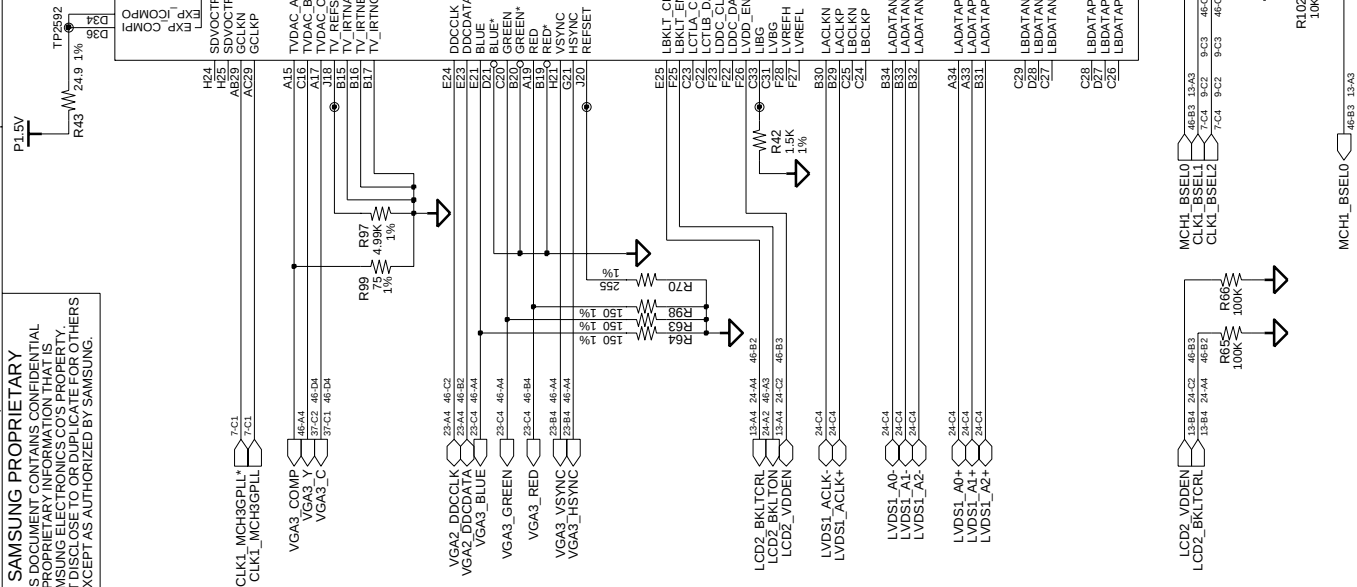


DATE	6/25/2005	TITLE	AQUILA-SONOMA MAIN
CHKD	ANTONIO	MP	CPU/DDR Thermal Sensor
APPRV	KEVIN LEE	REV	1.0
MODULE CODE	undefined	LAST EDIT	June 25, 2005 12:21:39 PM

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PART NO. BA41-00529A	



DATE	6/25/2005	TITLE		AQUILA-SONOMA MAIN ALVISO (1/15)	SAMSUNG ELECTRONICS
DEV. STEP	MP				
REV	1.0				
APPROVAL					
MODULE CODE					
ZHOU & GUO		ANTONIO		KEVIN LEE	PAGE 12 OF 46 June 25, 2005 12:21:39 PM



Feature	Alviso	Iris(Grantsdale)
VCC_GMCH	VCC 1.05V	VCC 1.5V
VCCP	VTT 1.05V	VTT 1.2V
DMI	x2 / x4	x4 only

CFG#	Low	High
CFG(6)	Dmix2	DMix4 (Def.)
CFG(5)	DDR-2	DDR-1 (Def.)
CFG(7)	DDR-2	Mobile CPU (Def.)
CFG(9)	PEG Reversible Test Mode	Normal(Def.)
CFG(13,12)		Normal(Def.)
CFG(16)	FSS Dynamic ODT Disabled	Enabled (def.)
CFG(18)	VCC1.05V (Def.)	VCC 1.5V
CFG(19)	VCCP 1.05V (Def.)	VCCP 1.2V
SDVOCTRL_DATA	No (Def.)	SDVP Present

MEM1_ADQ(63:0) 17:04

MEM1_ABS0*
MEM1_ABS1*
MEM1_ABS2*
MEM1_ADM(7:0)

MEM1_ADS0(7:0) 17:04

MEM1_ADS1(7:0) 17:04

MEM1_AMA(13:0) 17:04 18:03

MEM1_ARAS*
MEM1_AVE*
MEM1_AVE*

DDR SYSTEM MEMORY A

ALVISO500-3

ALVISO-GMCH

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DDR SYSTEM MEMORY B

DDR-II ONLY	DDR-I
SA_DQS(7:0)*	NC
SB_DQS(7:0)*	NC
SM_ODT(3:0)	NC

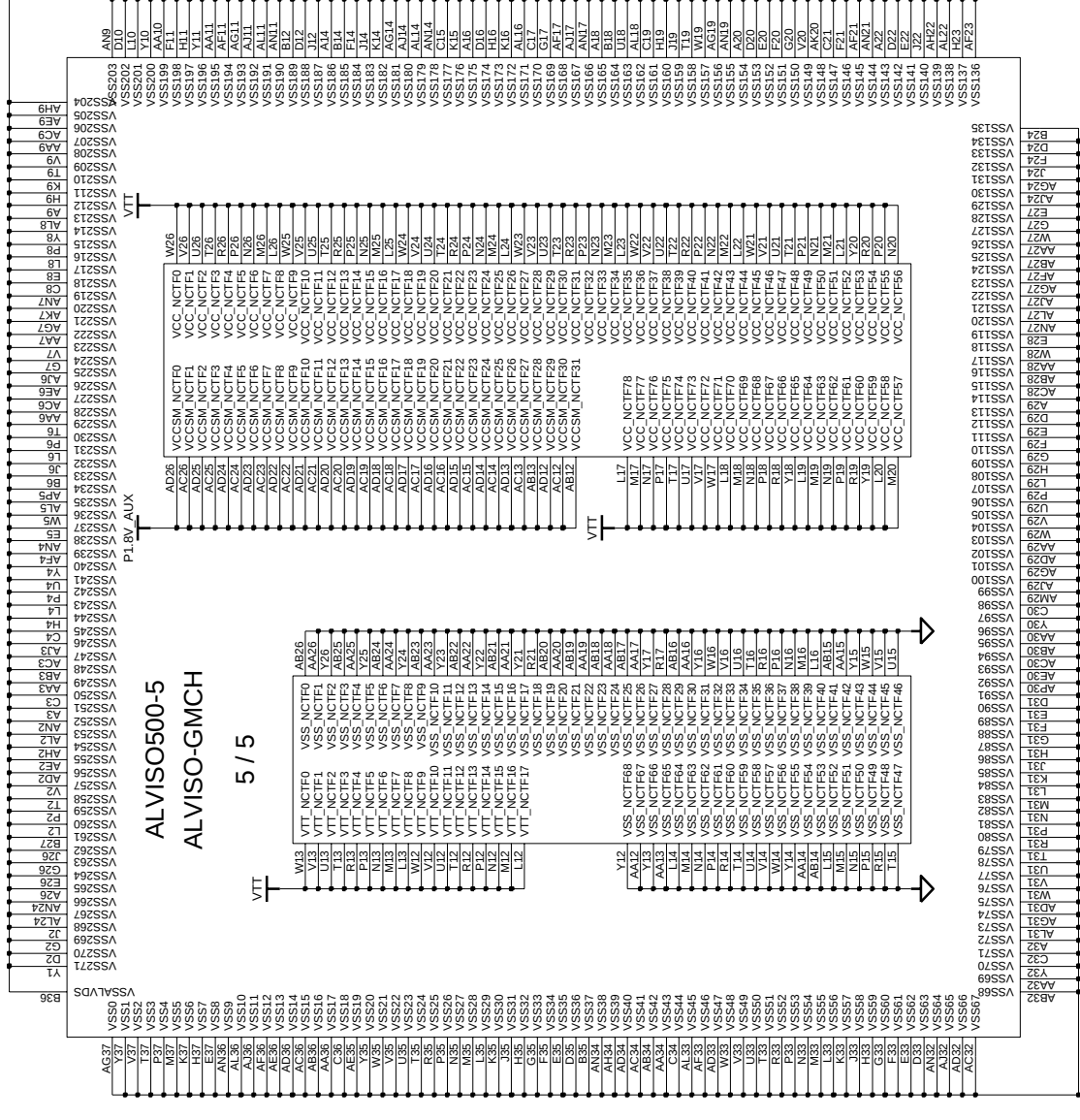
Dual Channel	Ch. A (So-DIMM A)	Ch. B (So-DIMM B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	SB_CK(2:0)
SM_CK(5:3)*	N/A	SB_CK(2:0)*
SM_CS(1:0)*	SA_CS(1:0)*	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_CS(3:2)*	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_SKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

SDVO Mode	PEG (SAGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVOB_RED*	EXP_TXN_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_GREEN*	EXP_TXN_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE*	EXP_TXN_2
SDVOB_CLK*	EXP_TXN_3
SDVOB_CLK*	EXP_TXN_3
SDVOB_ALPHA*	EXP_TXN_4
SDVOB_ALPHA*	EXP_TXN_4
SDVOB_GREEN*	EXP_TXN_5
SDVOB_GREEN*	EXP_TXN_5
SDVOB_BLUE*	EXP_TXN_6
SDVOB_BLUE*	EXP_TXN_6
SDVOB_CLK*	EXP_TXN_7
SDVOB_CLK*	EXP_TXN_7
SDVOB_TVCLKIN*	EXP_RXN_0
SDVOB_TVCLKIN*	EXP_RXN_0
SDVOB_INT*	EXP_RXN_1
SDVOB_INT*	EXP_RXN_1
SDVOB_STALL	EXP_RXN_2
SDVOB_STALL	EXP_RXN_2
SDVOB_INTB	EXP_RXN_5
SDVOB_INTB	EXP_RXN_5

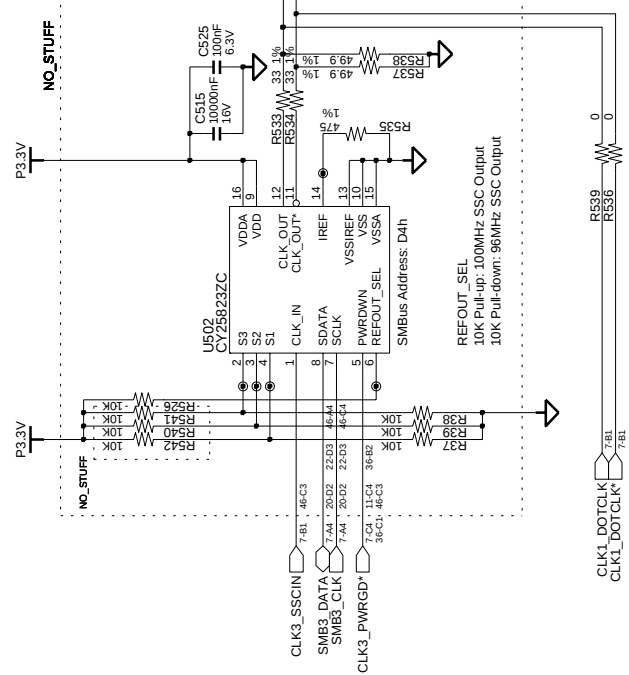


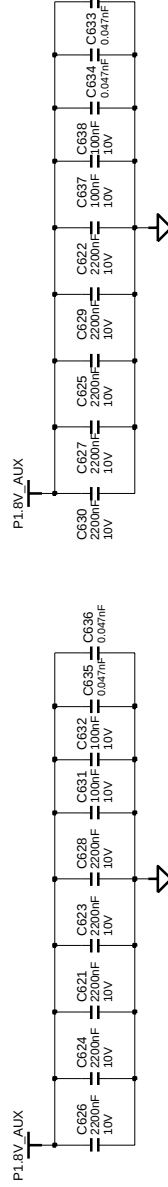
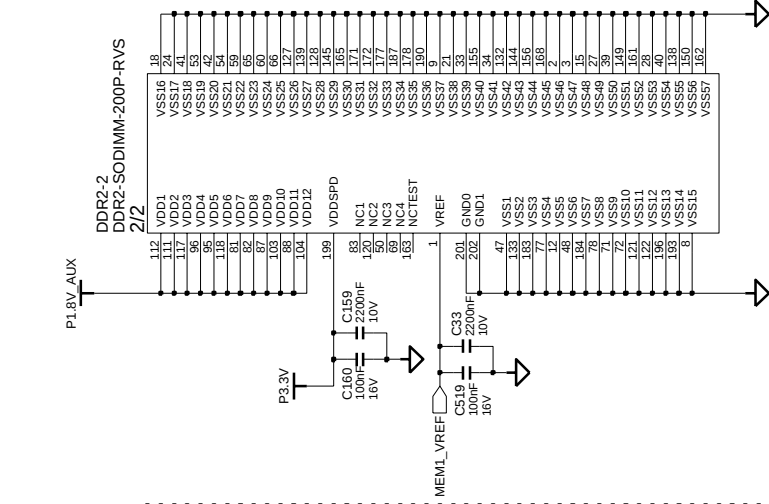
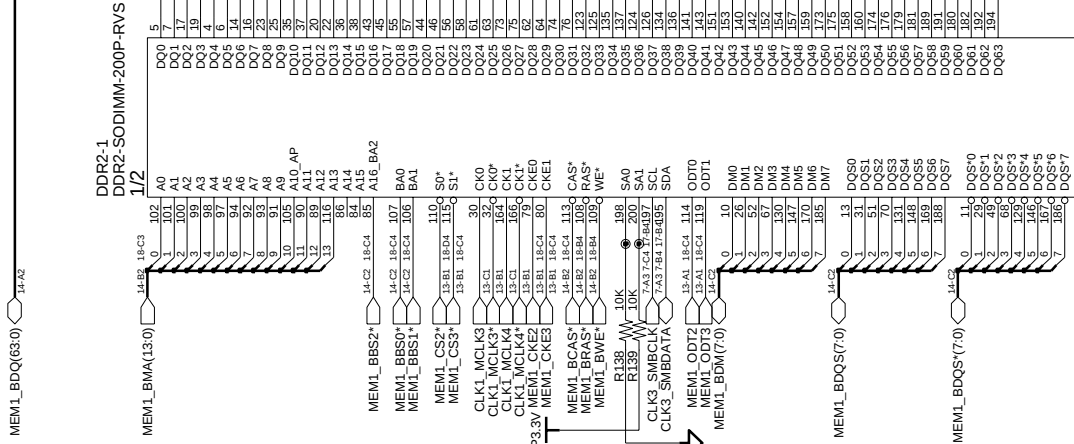
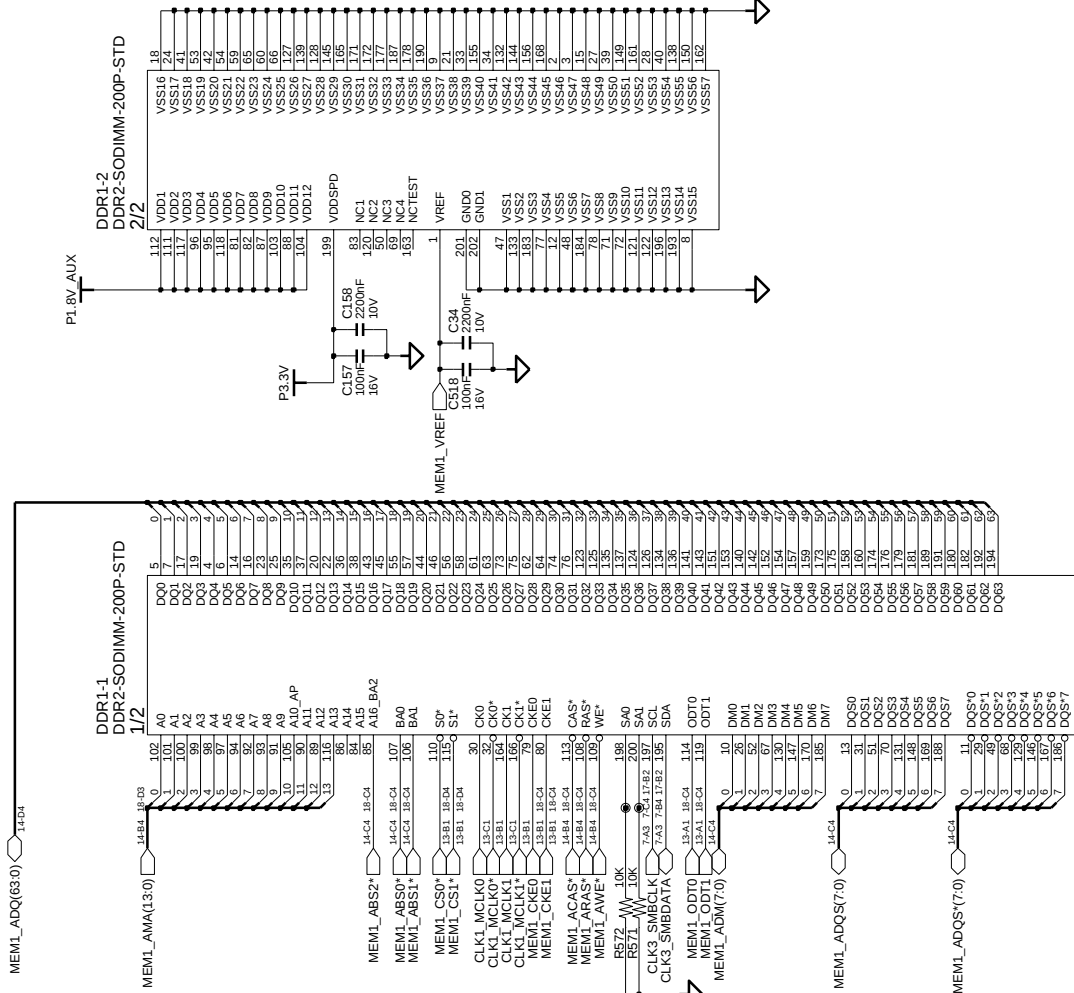
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ALVISO-GMCH

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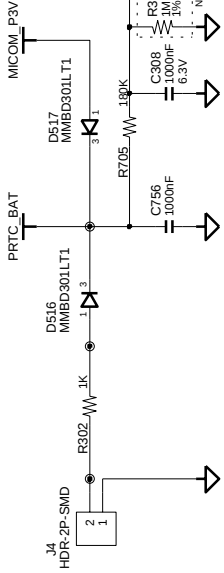


NCTF: Non-Critical to Function
VTT_NCTF: NCTF FSB power supply (1.05V or 1.2V)
VCC_NCTF: NCTF Core Vcc(1.05V or 1.5V)

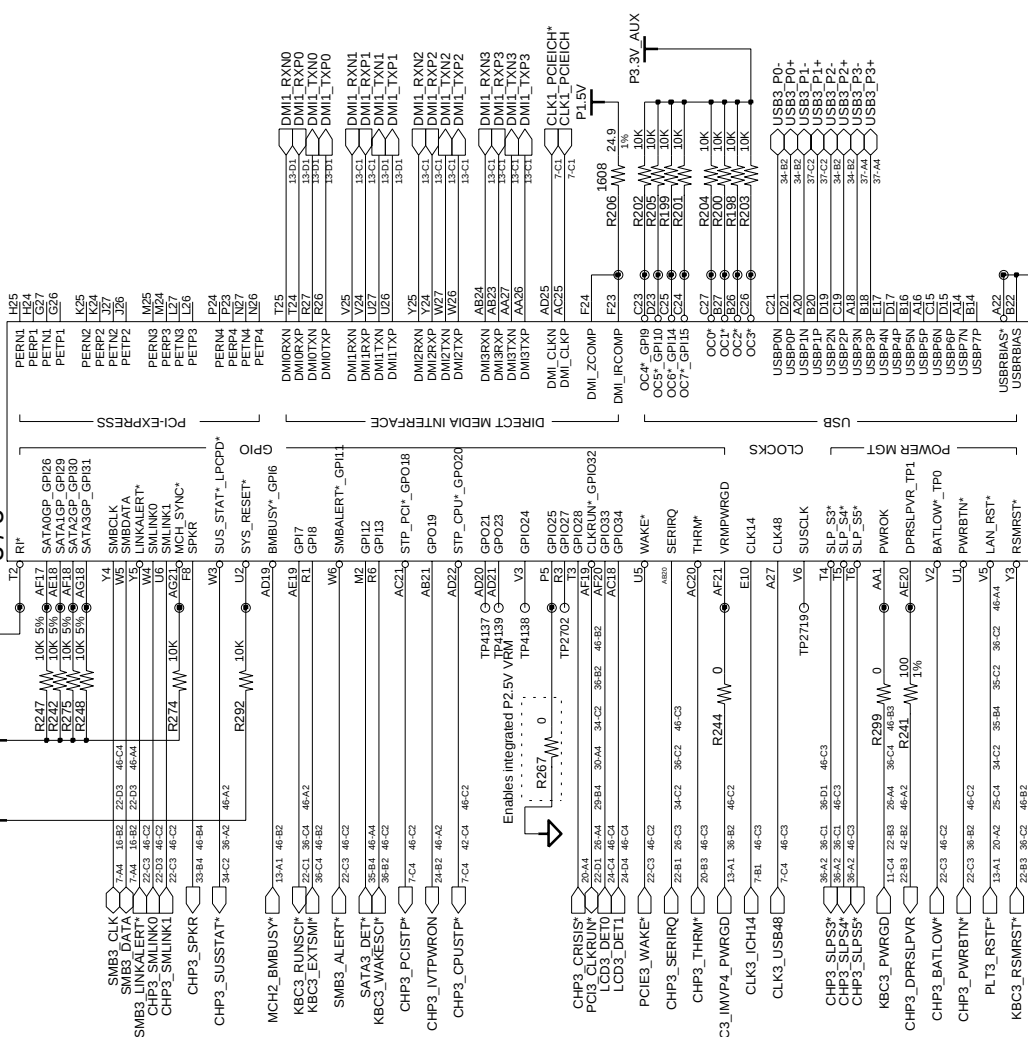
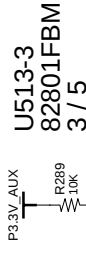
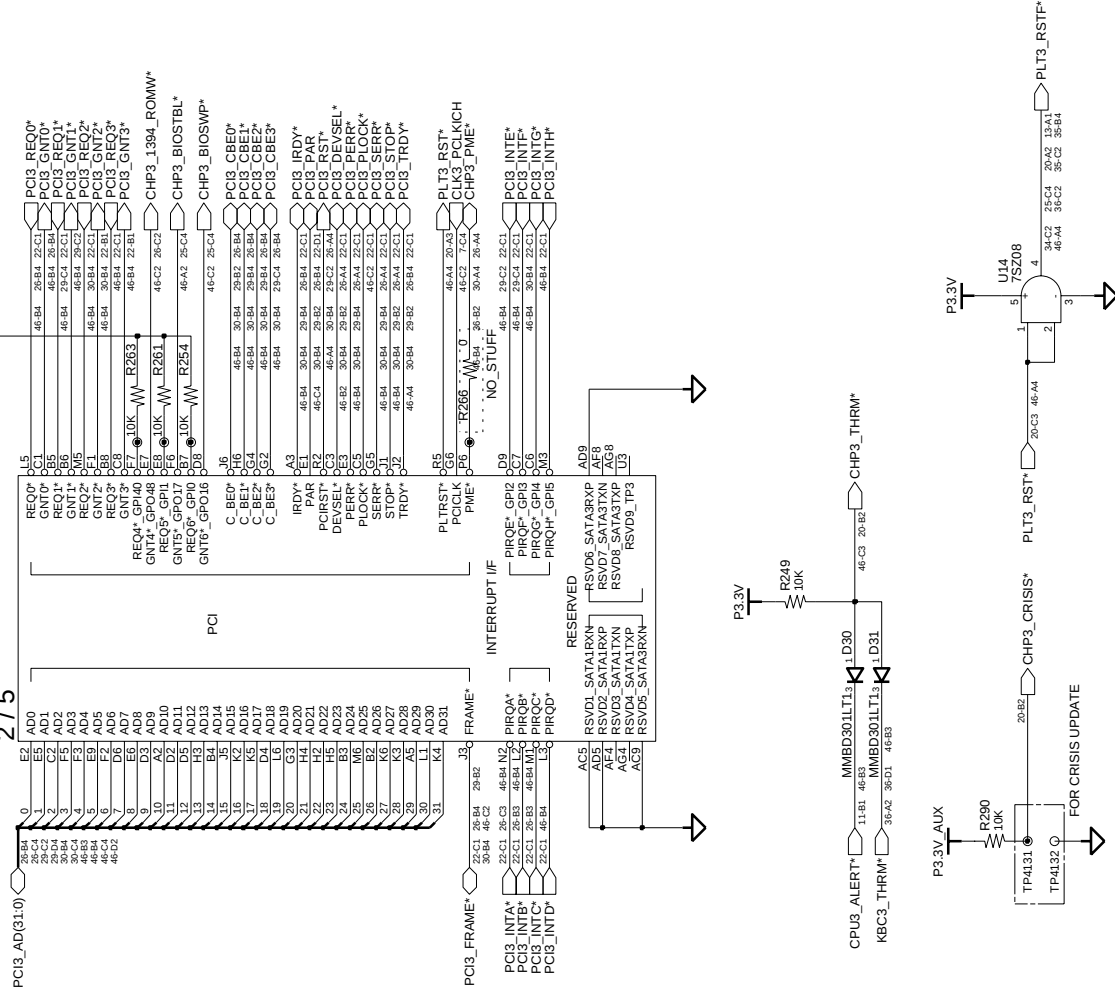
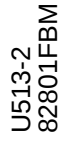




NAME	DATE	TITLE		SAMSUNG ELECTRONICS
CHECK	NO / Y / N	MP	MAIN	
APPROVAL	REV	1.0	DDR II SODIMM	
MODULE CODE	LAST EDIT			
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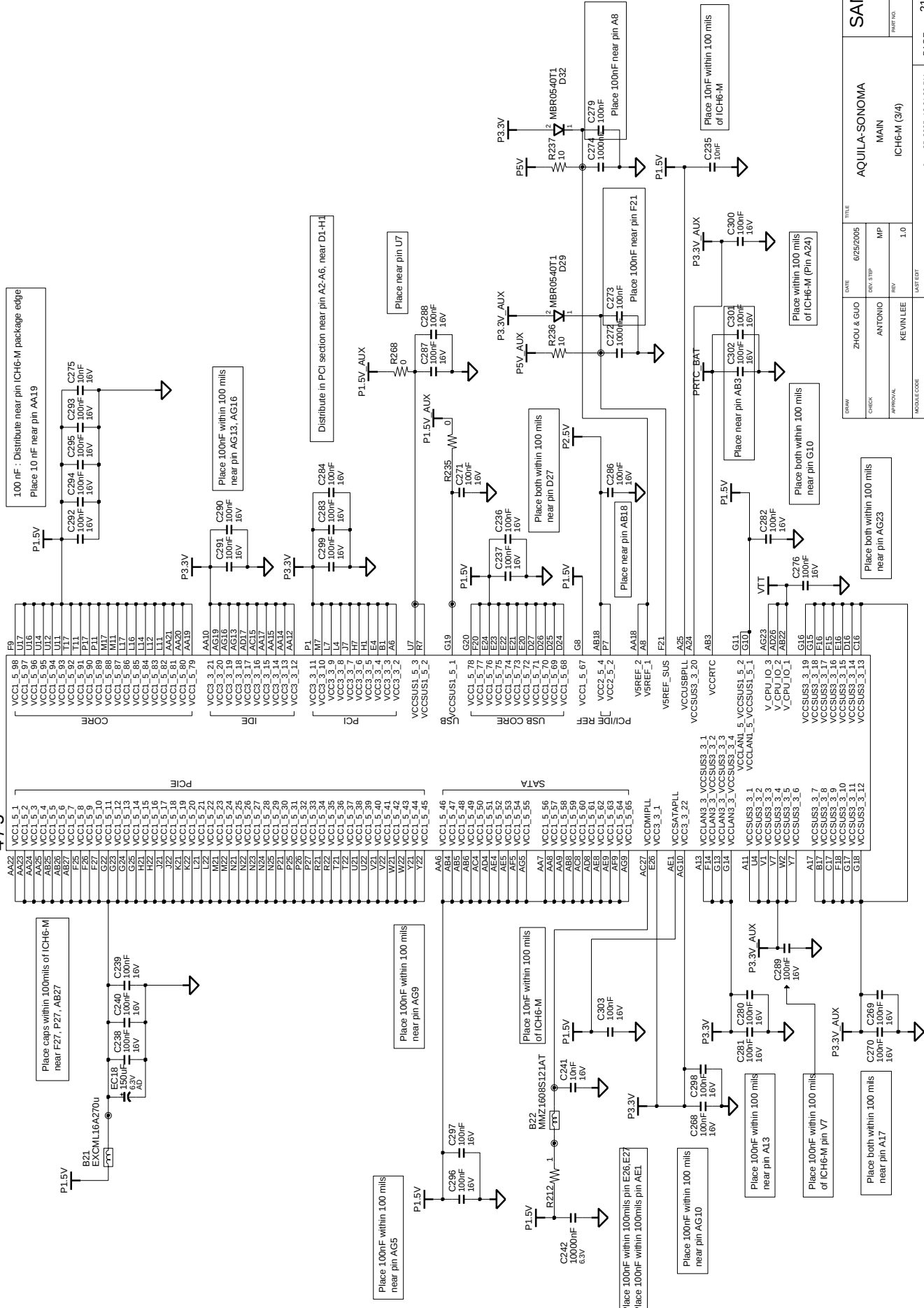
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APPROVAL	KEVIN LEE	REV	1.0		
MODULE CODE			LAST EDIT		
			JUNE 25, 2005 12:21:39 PM PAGE 19 OF 46		



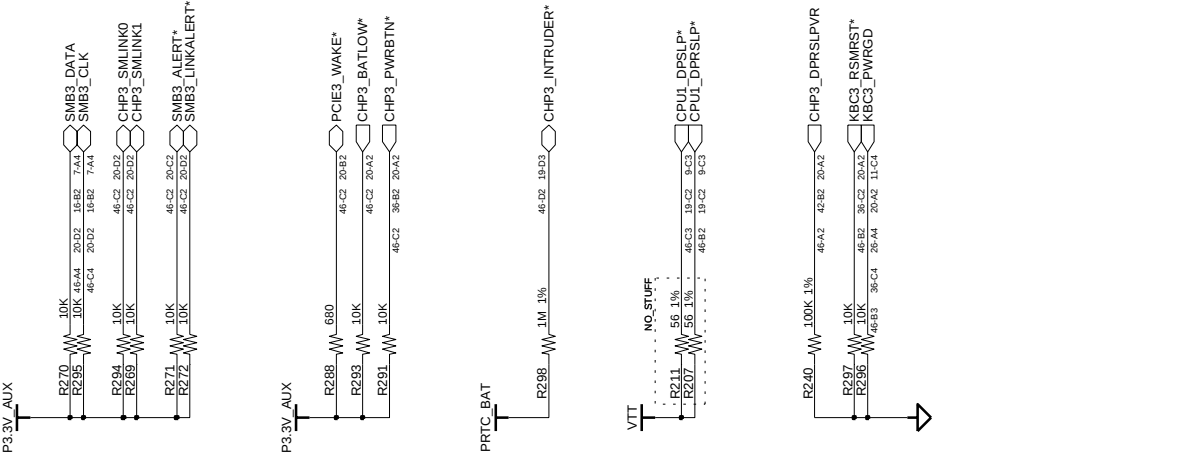
Place within 500 mils of ICH6-M

FORMA	DATE	TITLE		SAMSUNG ELECTRONICS
CHECK	QW / STOP	MP	AQUILA-SONOMA MAIN	
APPROVAL	REV	1.0	ICH6-M (2/4)	
LAST EXP			PART NO	
MODULE CODE				BA41-00529A
3un 25, 2005 12:21:39 PM				PAGE 20 OF 46

U513-4
82801FBM



82801FBM

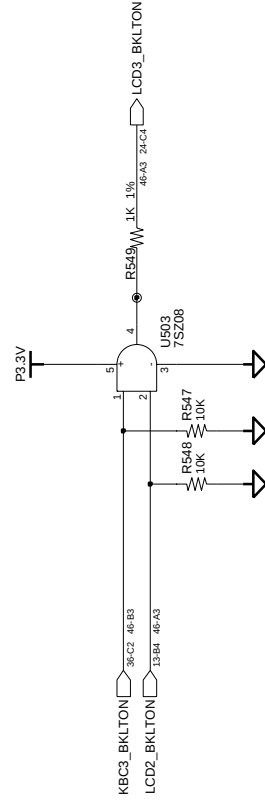
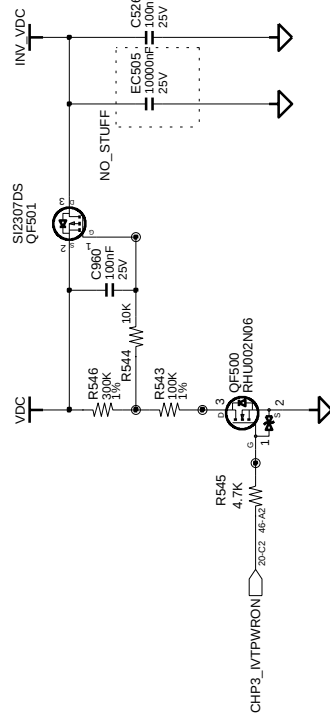
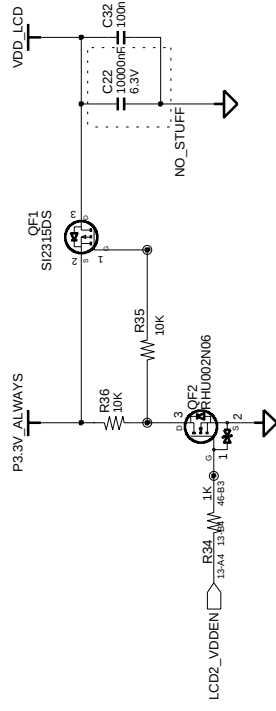
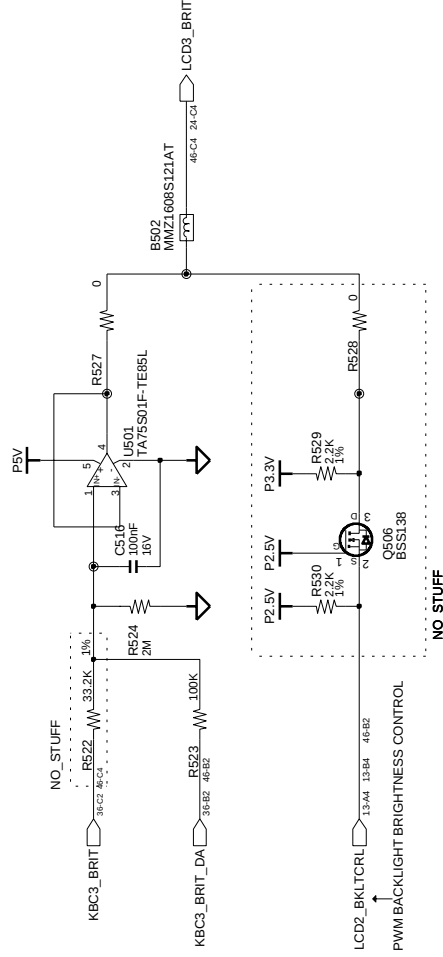


ICH6-M Strapping Options

	Function	Default
CHP3_SPKR	No Reboot	No Stuff
CHP3_BIOSWP*	Boot BIOS	No Stuff
PC/PCI GNTA*	A16 swap override	No Stuff
AC97_SDOUT	Safe Mode	TBD
EEP_DOUT		TBD

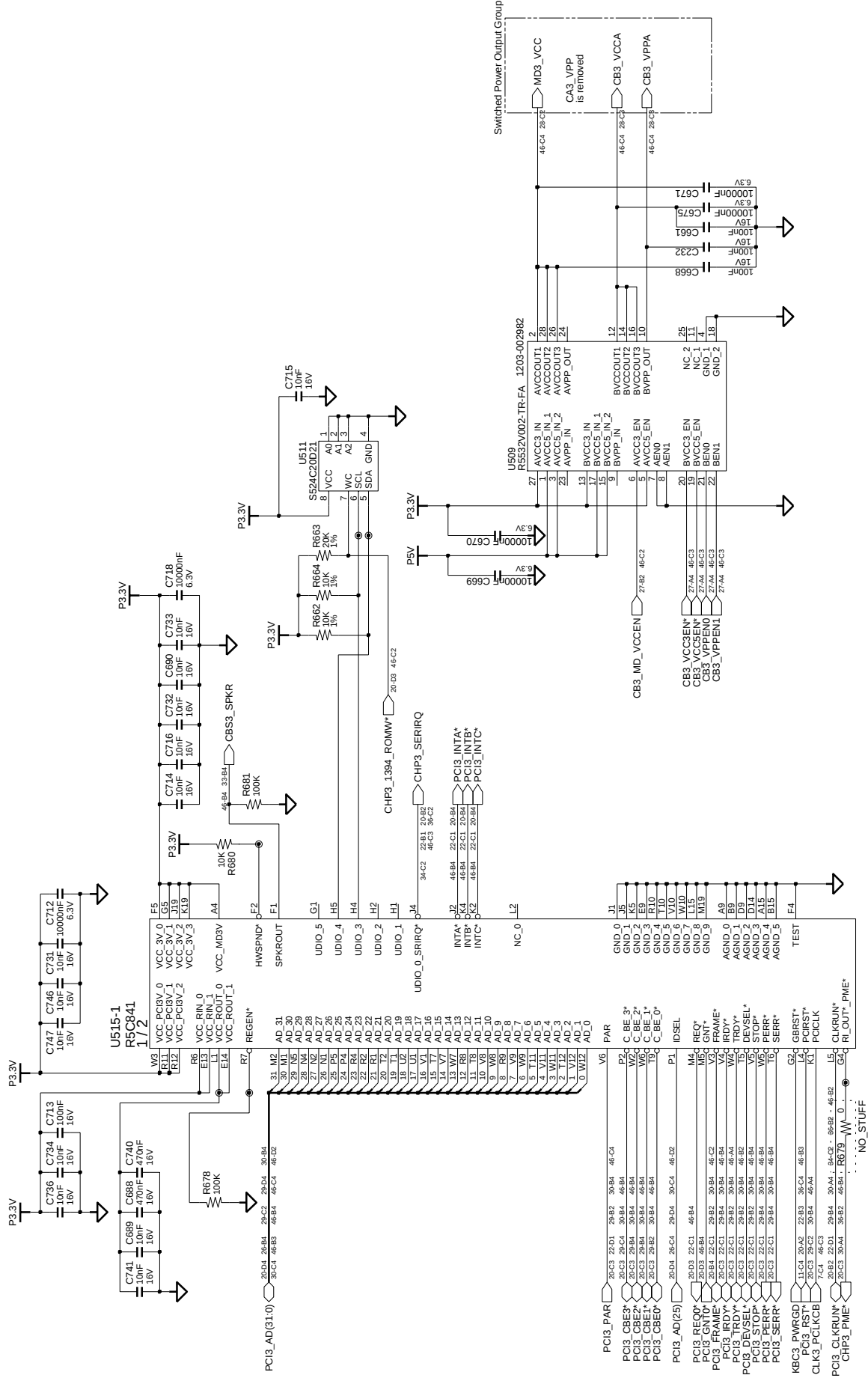
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CHECK	ZHOU & GUO		6/25/2005		ELECTRONICS	
	DPO. 5/10P		MP		PART NO.	
APPROVAL	ANTONIO		MAIN		BA41-00529A	
	KEVIN LEE		ICH6-M (4/4)			
MODULE CODE			LAST EDIT			
			June 25, 2005 12:21:39 PM		PAGE 22 OF 46	

SHAW	DATE	TITLE		SAMSUNG ELECTRONICS
CHUCK	END / STOP	AQUILA-SONOMA		
APPROVAL	REV	MAIN		
		CRT		
MODULE CODE		LAST EDIT		BA41-00529A
		June 25, 2005 12:21:39 PM		PAGE 23 OF 46

[illegible]

SAMSUNG ELECTRONICS	
BA41-00529A	WARRANT NO.
AQUILA-SONOMA MAIN	LCD CONNECTOR
DATE 6/25/2005	REV. MP
ZHOU & GUO	ANTONIO
CHECK	KEVIN LEE
APPROVAL	
MODULE CODE	
PAGE 24 OF 46	June 25, 2005 12:21:38 PM

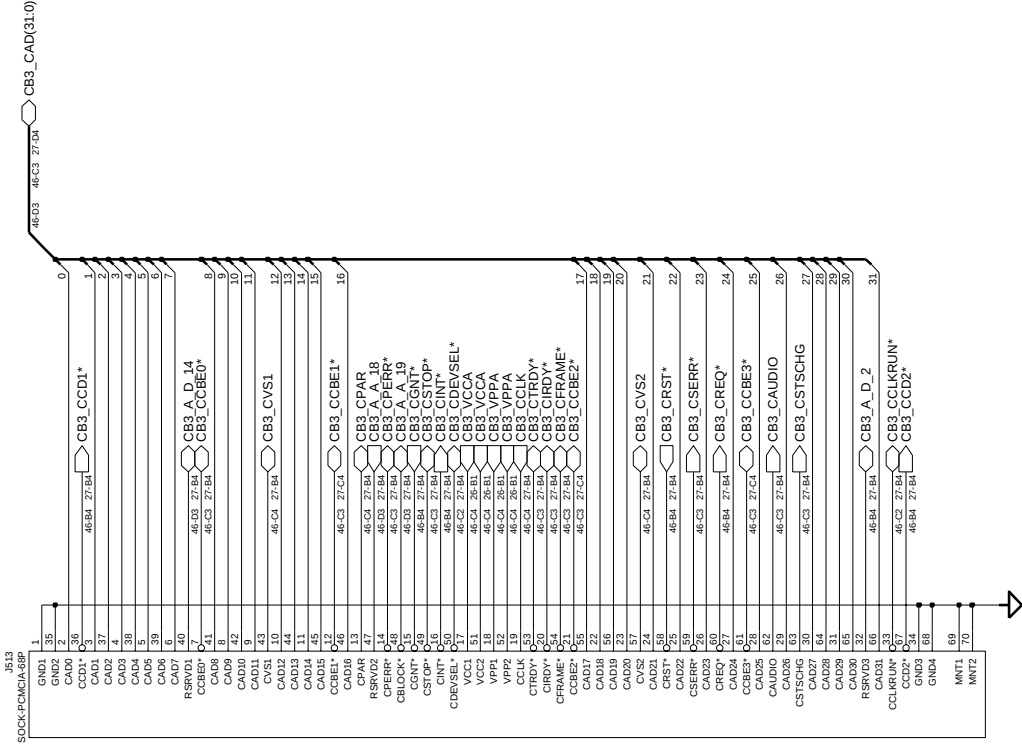
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DRAWN		DATE		TITLE	
ZHOU & GUO		6/25/2005		AQUILA-SONOMA	
CHECK		DRAW STOP		MAIN	
APPROVAL		REV		CARDBUS (1/2) & 1394	
MODULE CODE		LAST EDIT		PART NO.	
		June 25 2005 12:21:39 PM		BA41-00529A	
		PAGE		26	
		OF		46	

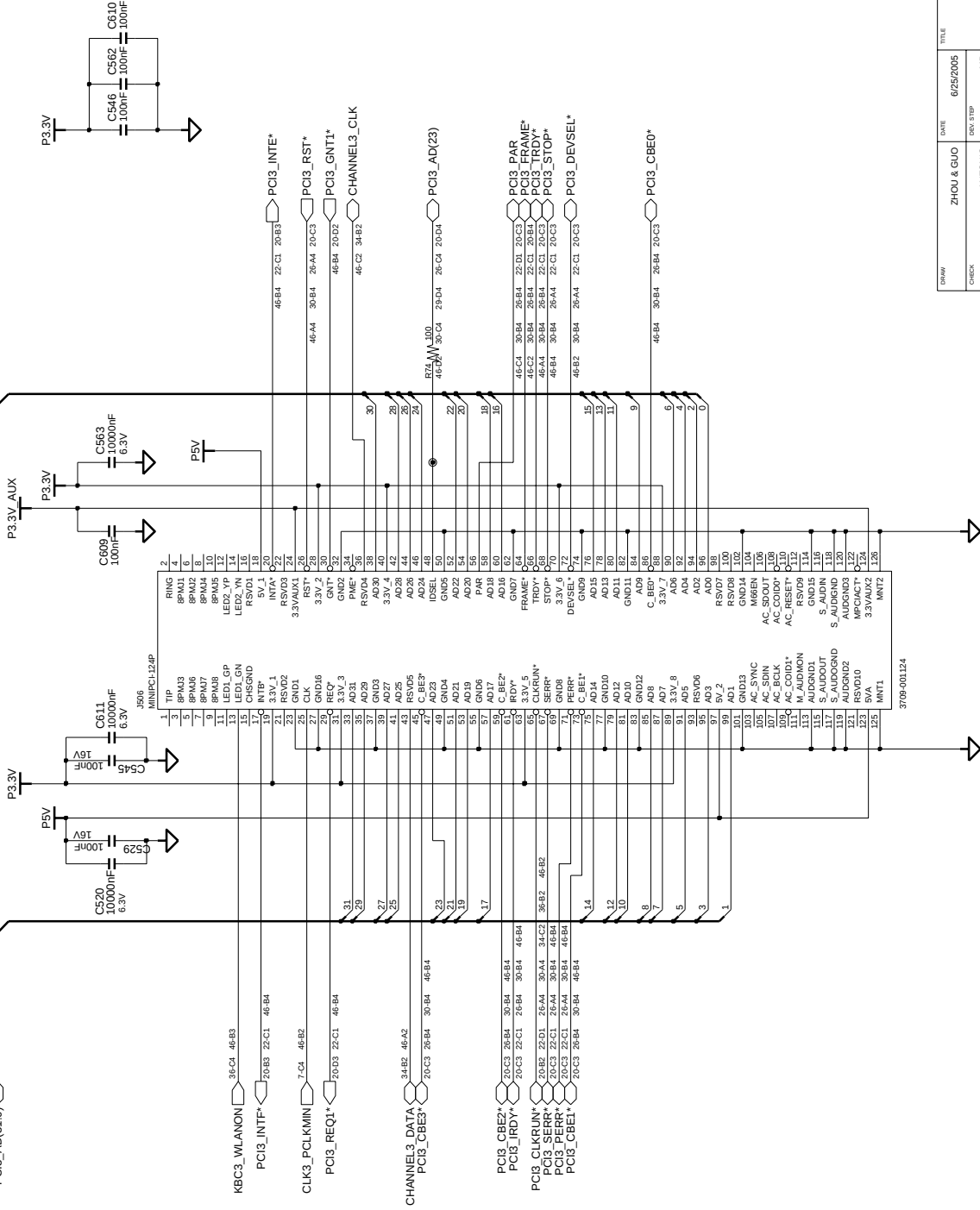


DRAWN	DATE	TITLE	SAMSUNG ELECTRONICS PART NO. BA41-00529A
CHECK	DWG. STP	MP	
APPROVAL	REV	1.0	
ZHOU & GUO ANTONIO KEVIN LEE		AQUILA-SONOMA MAIN CARBIDUS (2/2)	
MODULE CODE		PAGE 27 OF 46 June 25, 2005 12:21:39 PM LAST EDIT	

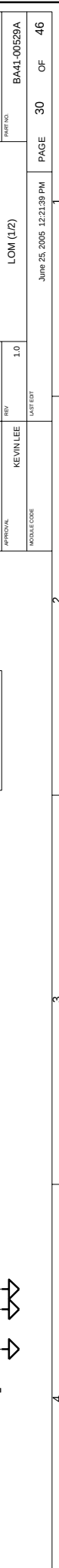


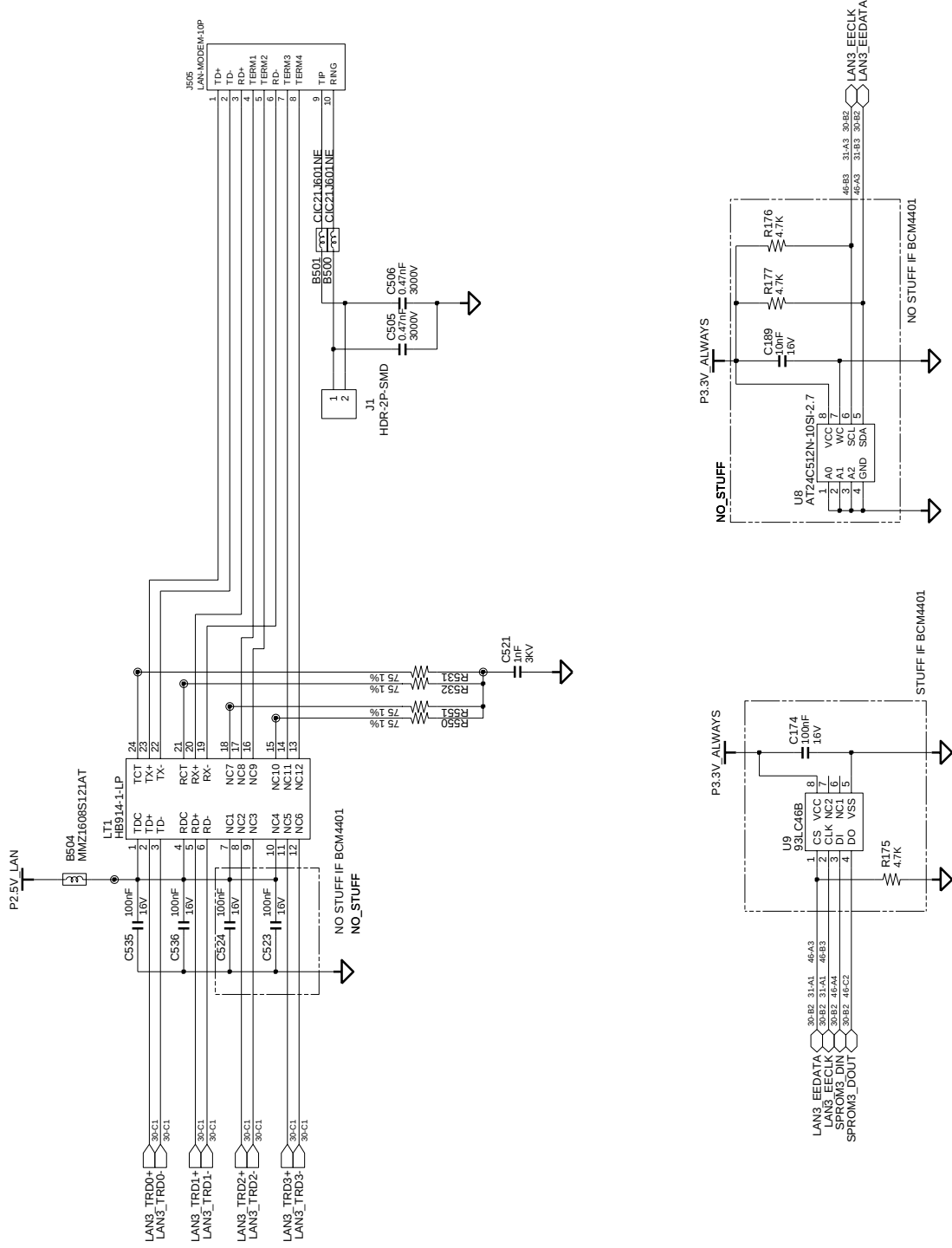
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CHECK	6/25/2005	AQUILA-SONOMA	ELECTRONICS
APPROVAL	DEV. STEP	MAIN	
MODULE CODE	REV	PCMCIA / MEDIA CARD SOCKET	PART NO.
	1.0		BA41-00529A
	LAST EDIT		
	June 25 2005 12:21:39 PM	PAGE	28 OF 46

	20-D4	26-B4	29-C2	30-B4	30-C4	46-B3	46-B4	46-C4	46-D2
PCI3 AD(31'0)									



GRAND	DATE	TITLE		SAMSUNG ELECTRONICS PART NO. BA11-00529A
CHECK	DOV / STOP	MP	AQUILA-SONOMA MAIN	
APPROVAL	REV	1.0	MINI PCI	
MODULE CODE	LAST EDIT			
ZHOU & GUO ANTONIO KEVIN LEE		June 25, 2005 12:21:39 PM PAGE 29 OF 46		



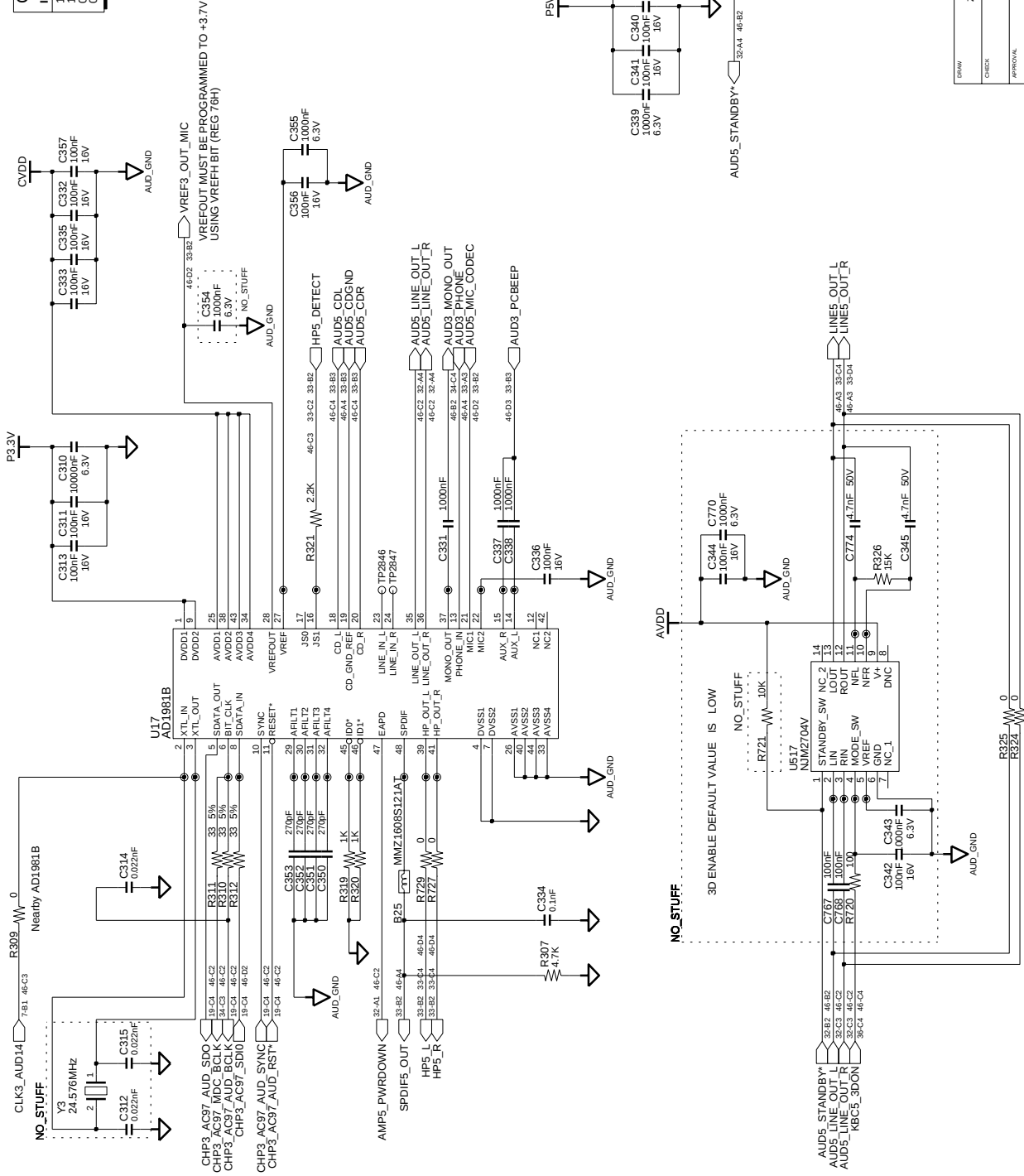
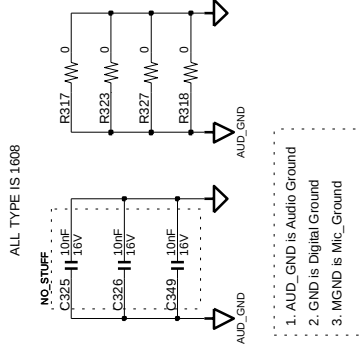


DRAWN		DATE		TITLE	
ZHOU & GUO		6/25/2005		AQUILA-SONOMA	
CHECK		CHK. STOP		MAIN	
APPROVAL		REV		LOM (2/2)	
MODULE CODE		LAST EDIT		BA41-00529A	
		PAGE		31 OF 46	

AC97 2.3 CODEC

CLOCK SELECTION			
ID0*	ID1*	CODEC ID	CLK FREQ.
1	1	PRIMARY	24.576 MHz
0	1	EXT. CLK	24.576 MHz
0	0	PRIMARY	48.000 MHz
0	0	PRIMARY	14.338 MHz

SOURCE	
Local XTAL	
Ext. Clock (into XTAL_IN)	
Ext. Clock (into XTAL_IN)	

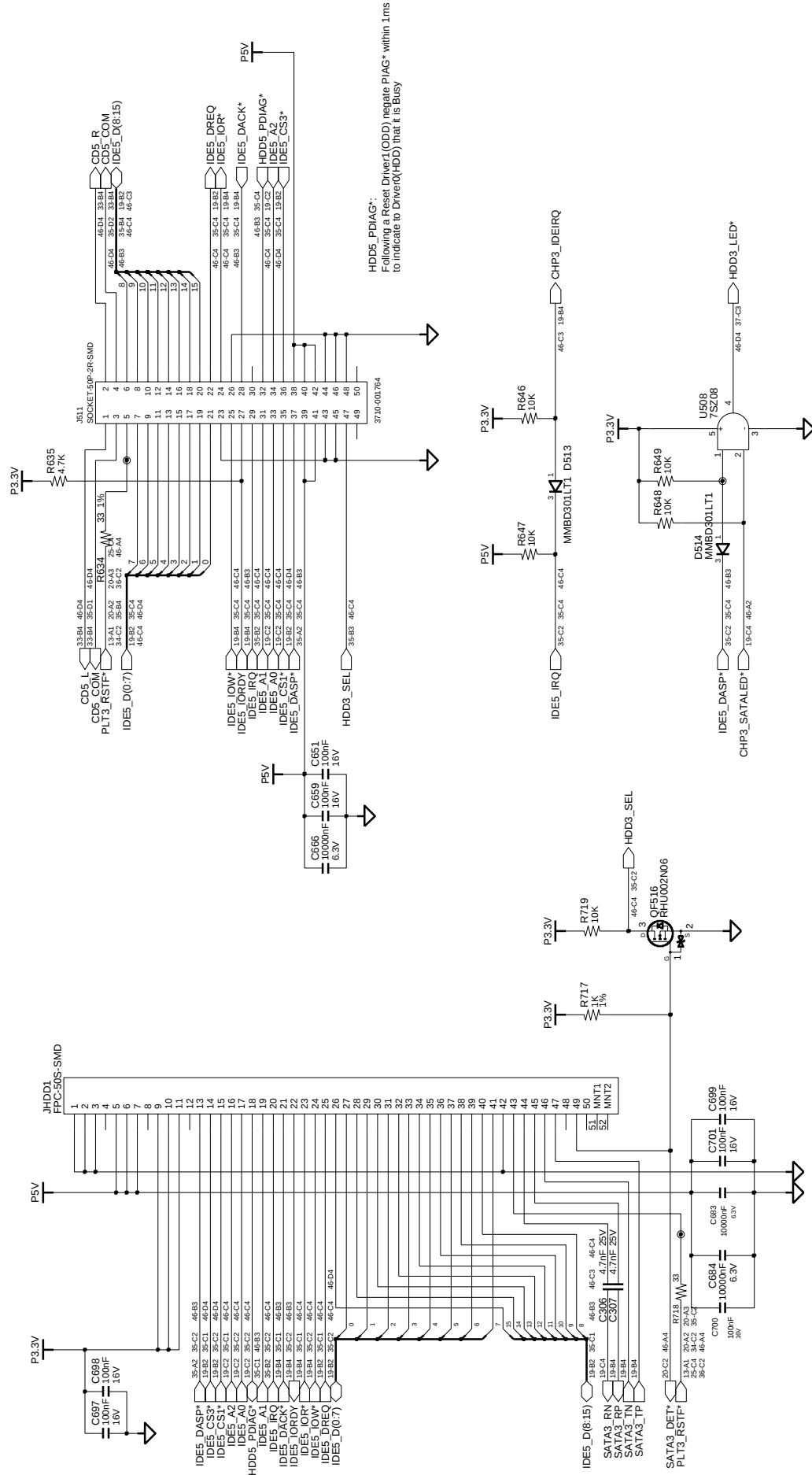




M1 HEAD DIA LENGTH

DRAWN		DATE	TITLE		SAMSUNG ELECTRONICS	
CHECK		6/25/2005	AQUILA-SONOMA MAIN		PART NO.	
APPROVAL		DOV / STIP	MP		BA41-00529A	
		ANTONIO	REV			
		KEVIN LEE	1.0			
MODULE CODE		LAST EDIT		PAGE	OF	46
		JUNE 25, 2005 12:21:39 PM		34		

Main to ODD

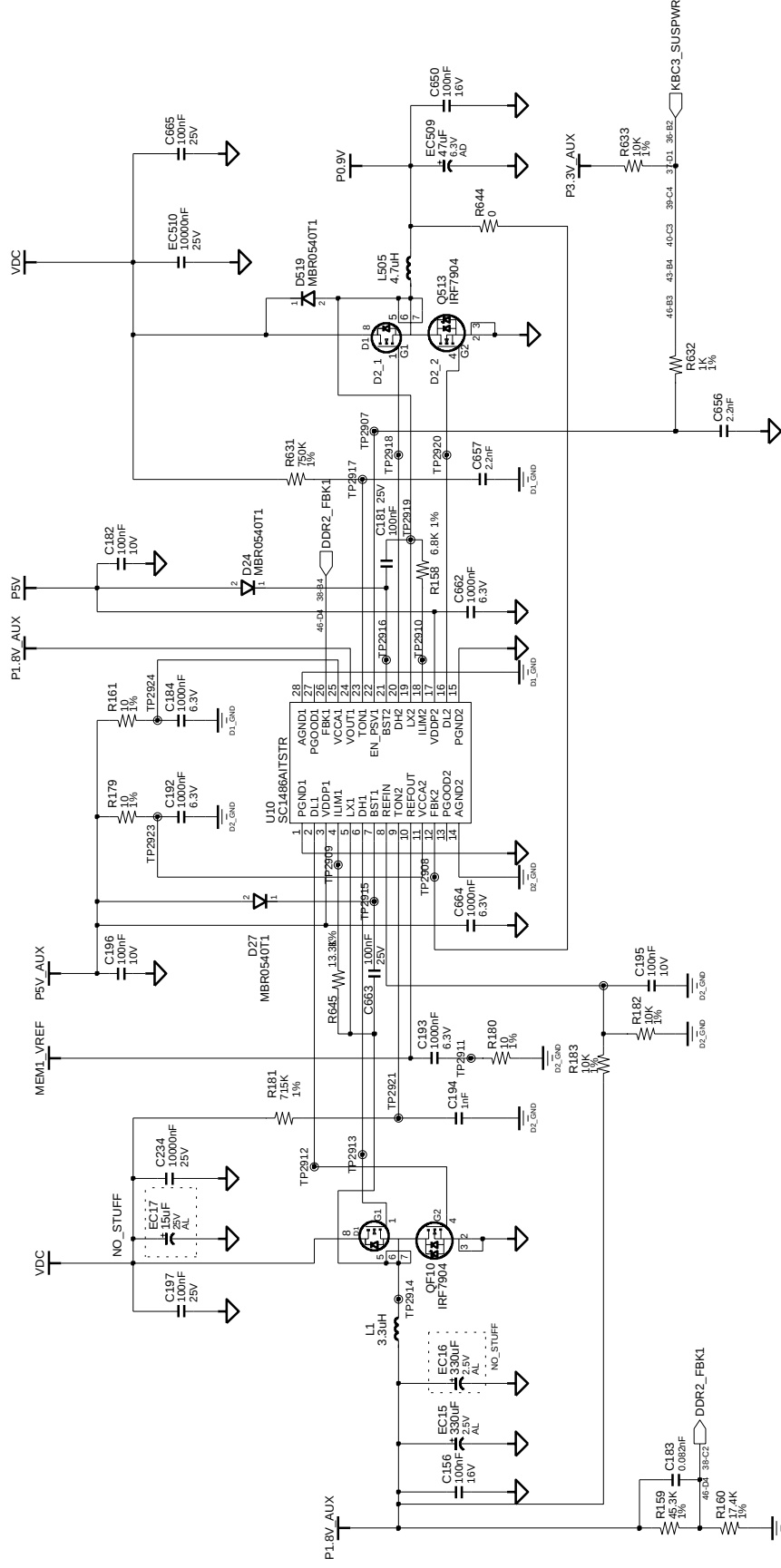


DATE	6/25/2005	TITLE		AQUILA-SONOMA MAIN IDE CONNECTOR	PAGE 35 OF 46
CHECK	END - 3 STEP	MP			
APPROVAL	END	1.0			
ZHOU & GUO		ANTONIO			
KEVIN LEE		BA41-00529A			
MODULE CODE		LAST EDIT		June 25, 2005 12:21:39 PM	

7

DRAWN	ZHU & GUO		DATE	6/25/2005		TITLE		AQUILA-SONOMA	
CHECK	ANTONIO		CHK / STIP	MP		MAIN		SAMSUNG ELECTRONICS	
APPROVAL	KEVIN LEE		REV	1.0		B'd to B'd CONN		PART NO.	
MODULE CODE		LAST EDIT		June 25, 2005 12:21:39 PM		PAGE		37 OF 46	
								BA41-00529A	

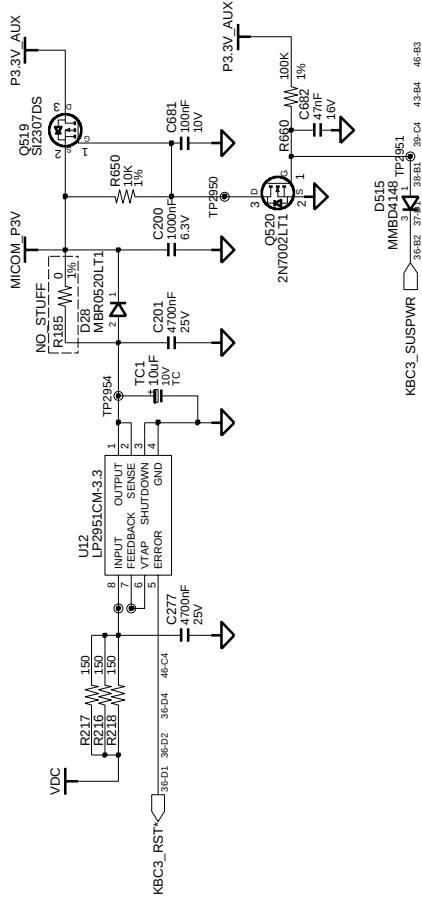
DDR II Power



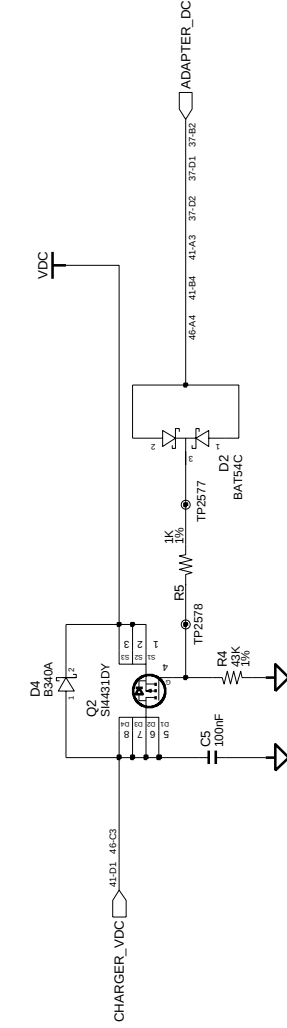
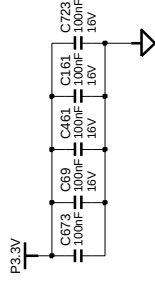
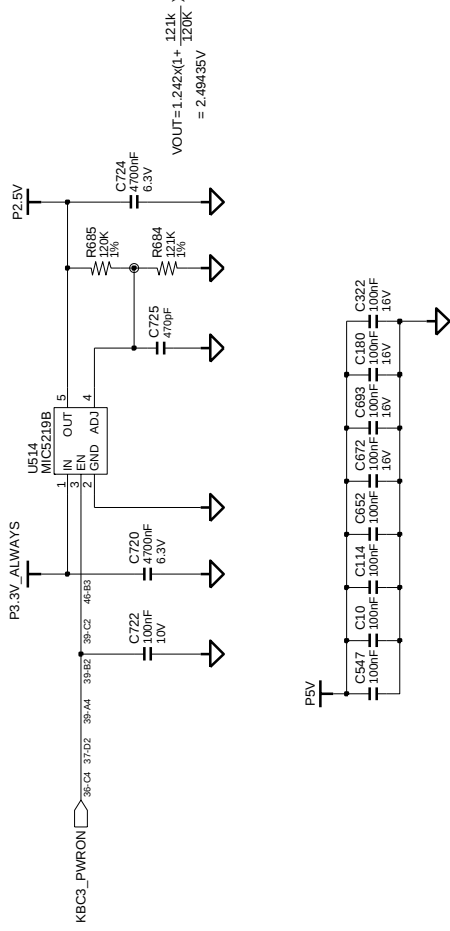
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DRAWN	ZHOU & GUO	DATE	G/25/2005	TITLE	AQUILA-SONOMA MAIN
CHECKED	ANTONIO	DOY / STEP	MP		
APPROVAL	KEVIN LEE	REV	1.0		SWITCHED POWER
MATERIAL CODE		LAST EDIT		PAGE	39 OF 46
					JUNE 25, 2005 12:21:38 PM
					SAMSUNG ELECTRONICS BA41-00529A WARE NO.

MICOM_P3V

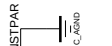


P2.5V



DRAWN	DATE	TITLE	SAMSUNG
CHECK	6/25/2005	AQUILA-SONOMA	ELECTRONICS
APPROVAL	DEV. STEP	MAIN	
MODULE CODE	REV	MICOM_P3V / P2.5V	
	1.0		
	LAST EDIT		
	June 25 2005 12:21:39 PM		
	PAGE	40	OF 46

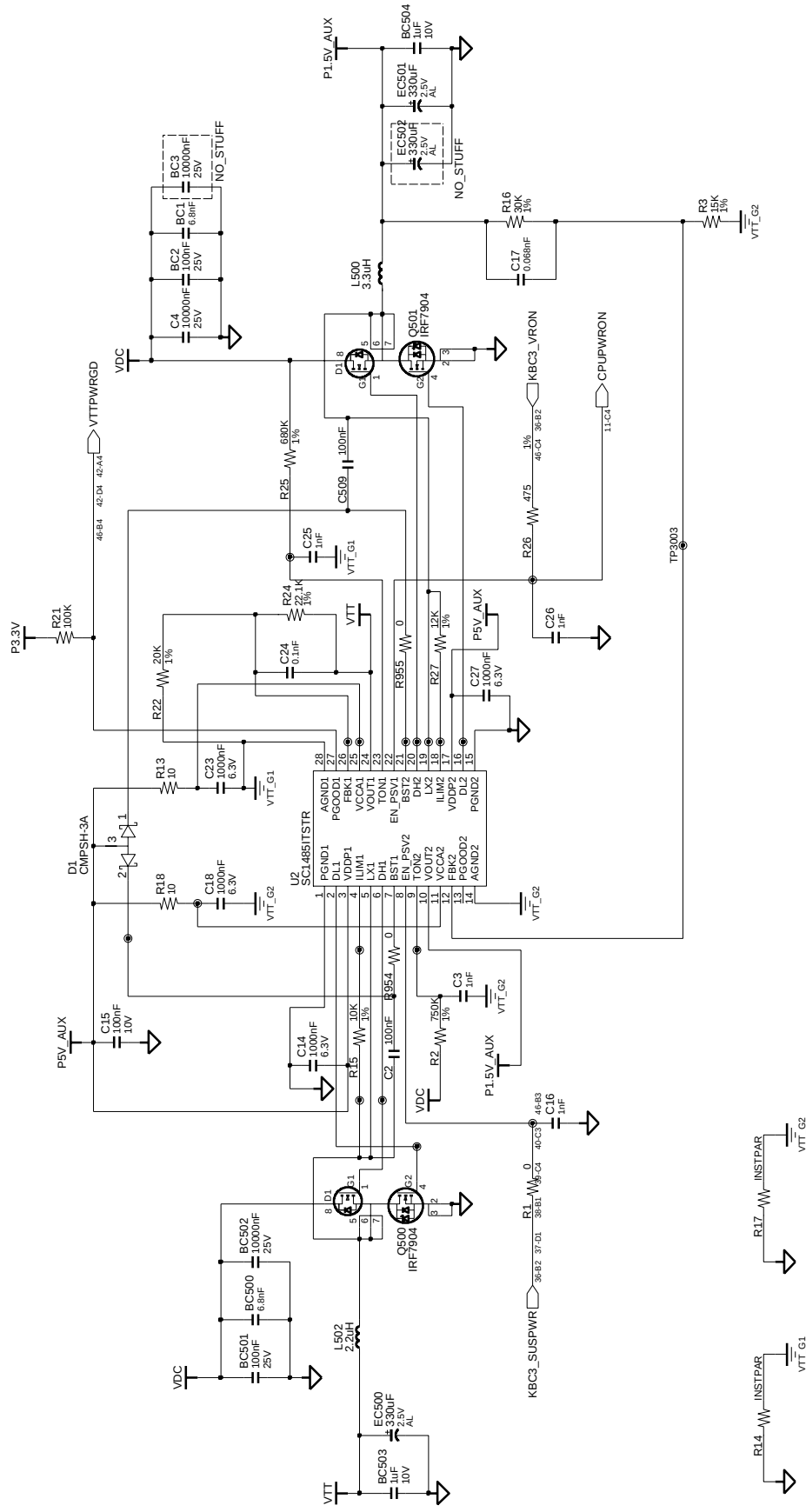
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4	3	2	1	PAGE 41 OF 46	June 25, 2005 12:21:39 PM	REPORT DATA
CONFIDENTIAL SOURCE						
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DRAWN	ZHOU & GUO	TITLE	AQUILA-SONOMA	SAMSUNG ELECTRONICS
CHECK	ANTONIO	DATE	6/25/2005	
APPROVAL	KEVIN LEE	REV	1.0	
MODULE CODE		REV	1.0	
		DATE	June 25, 2005 12:23:39 PM	
		PAGE	43	46
		OF	43	46
		PART NO.	BA41-00529A	

THESE ARE USED FOR INTERNAL CIRCUIT TEST
TO COMPARE CAPACITORS WHICH ARE UNDER 100pF

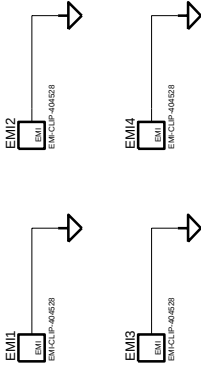
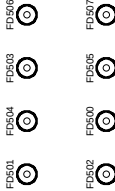
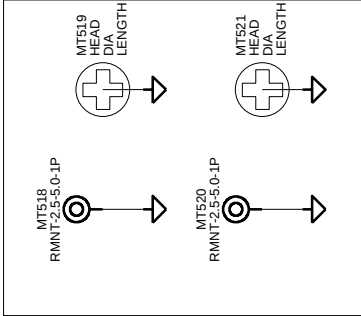
TOP

TP2512 ○ — C950 || 0.1nF — ○ TP2513
TP2466 ○ — C951 || 0.01nF — ○ TP2465
TP2467 ○ — C952 || 0.1nF — ○ TP2468
TP2481 ○ — C953 || 0.01nF 0.5pF — ○ TP2482
TP2485 ○ — C954 || 18pF — ○ TP2486
TP2489 ○ — C955 || 0.022nF — ○ TP2490
TP2497 ○ — C956 || 0.0033nF — ○ TP2498
TP2509 ○ — C957 || 0.0033nF — ○ TP2510
TP2503 ○ — C958 || 47pF — ○ TP2504

BOTTOM

TP2531 ○ — C462 || 0.1nF — ○ TP2532
TP2515 ○ — C463 || 0.01nF — ○ TP2516
TP2517 ○ — C464 || 0.1nF — ○ TP2518
TP2519 ○ — C465 || 0.01nF 0.5pF — ○ TP2520
TP2521 ○ — C466 || 18pF — ○ TP2522
TP2523 ○ — C467 || 0.022nF — ○ TP2524
TP2525 ○ — C468 || 0.0033nF — ○ TP2526
TP2529 ○ — C469 || 0.0033nF — ○ TP2530
TP2527 ○ — C470 || 47pF — ○ TP2528

FOR THERMAL



PCB REVISION CONTROL (ICT)			
NO	CONNECTION DATE(Y/MM/DD)	REVISION	STEP
1	N.C.	2005-6-25	1.0 MP
2	1-2		
3	2-3		
4	3-1		
5	1-2-3		
6	N.C.		
7	1-2		
8	2-3		
9	3-1		
10	1-2-3		

REV500

1 ○

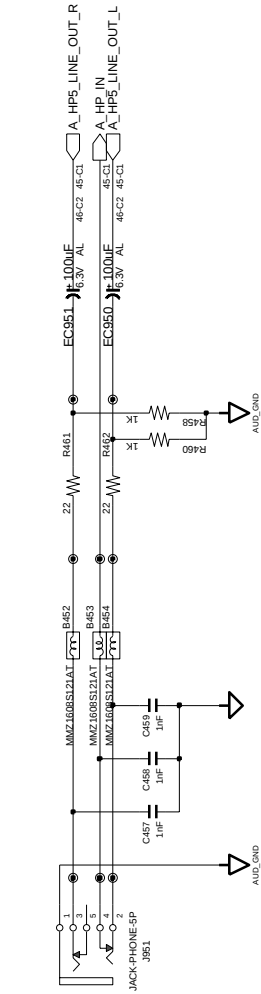
2 ○

3 ○

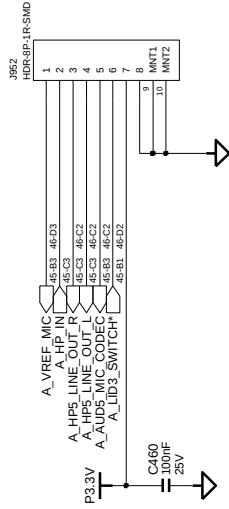
DRAWN	ZHOU & GUO	DATE	6/25/2005	TITLE	AQUILA-SONOMA	SAMSUNG ELECTRONICS
CHECK	ANTONIO	CHK. STEP	MP		MAIN	
APPROVAL	KEVIN LEE	REV	1.0		PCB STUFFS	
MODULE CODE		LAST EDIT	June 25 2005 12:23:39 PM	PAGE	44	OF 46
					BA41-00529A	

AUDIO BOARD

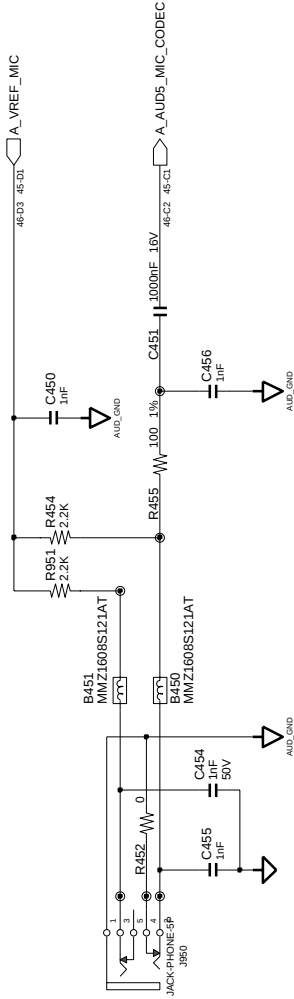
HEADPHONE



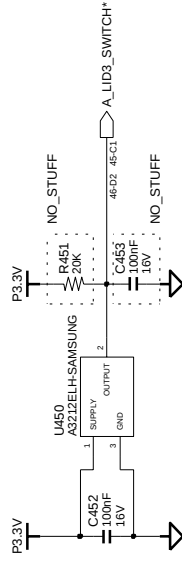
B'D TO B'D CONN



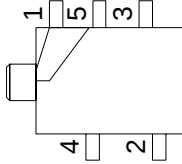
EXTERNAL MIC



LID SWITCH



TOP VIEW



DATE	6/25/2005	TITLE	AQUILA-SONOMA SUB BOARD AUDIO BOARD	SAMSUNG ELECTRONICS
CHECK	ANTONIO	REV	MP	PART NO.
APPROVAL	KEVIN LEE	REV	1.0	BA41-00529A
MODULE CODE		LAST EDIT	June 25 2005 12:21:39 PM	PAGE 45 OF 46

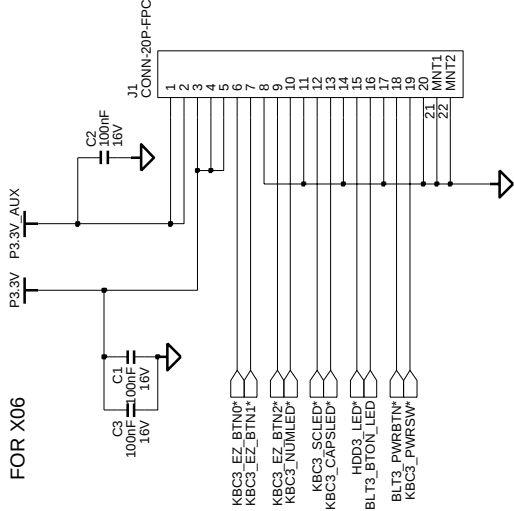
DRAWN		ZHAO, GUO		DATE	6/25/2005		TITLE		AQUILA-SONOMA MAIN		SAMSUNG ELECTRONICS	
CHECKED		ANTONIO,		DESIGN STEP		MP				PART NO.		
APPROVAL		KEVIN, LEE		REV		1.0		TESTPOINT		BA41-00529A		
MODULE CODE				LAST EDIT				June 25, 2005 12:21:39 PM		PAGE	46 OF 46	

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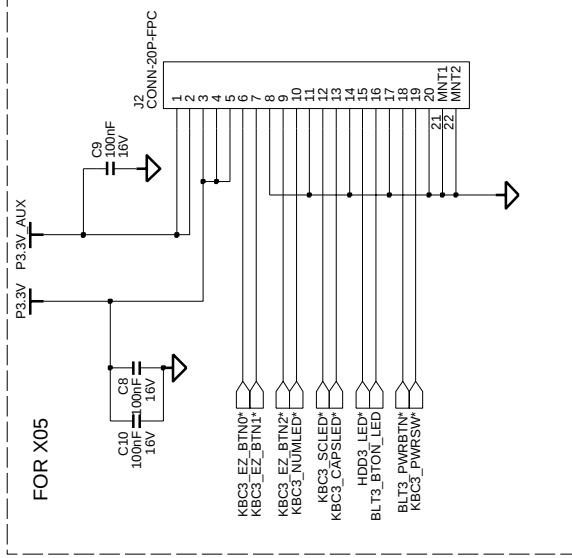
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10-2 ON-TOP BOARD

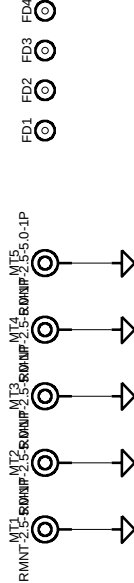
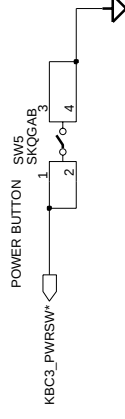
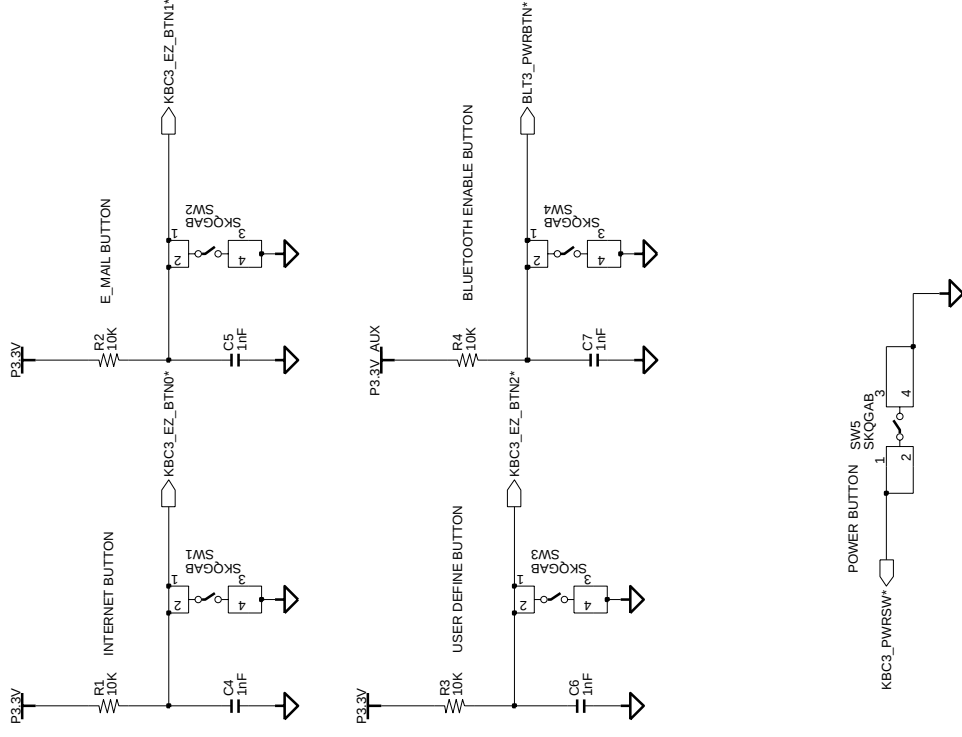
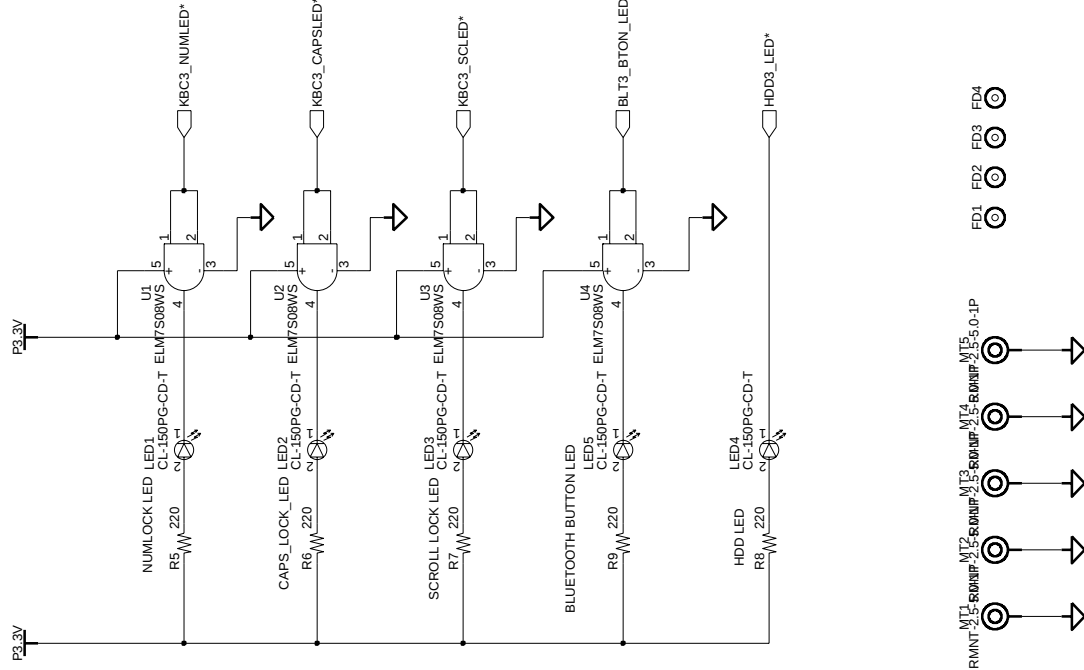
FOR X06



FOR X05



NO_STUFF



DRAW	DATE	TITLE	SAMSUNG
CHECK	DEV/STEP	MP	ELECTRONICS
APPROVAL	REV	1.0	PART NO.
MODULE CODE	LAST EDIT	May, 25, 2005 10:09:07 AM	BA59-01633A
		PAGE	1 OF 1

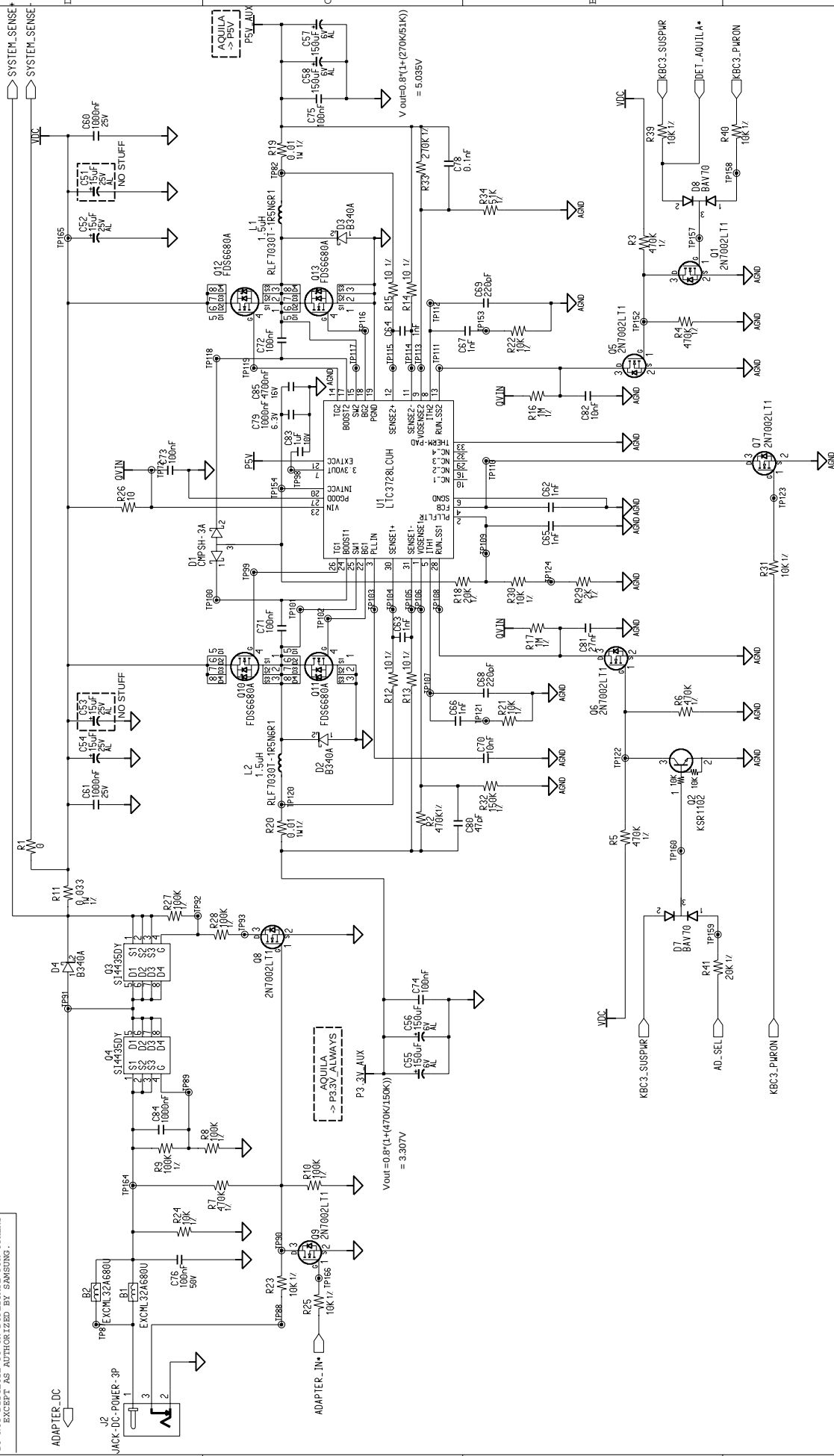
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- This Document can not be used without Samsung's authorization -

10.

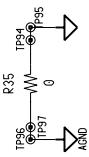
10-3 DCDC BOARD

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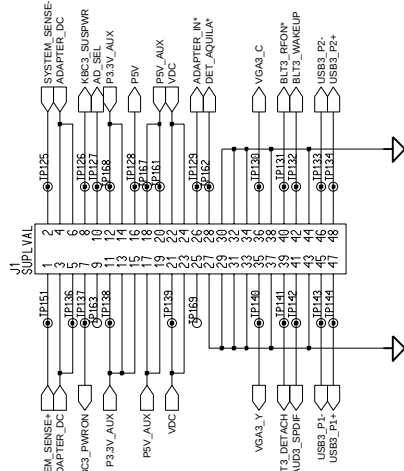
DATE	REV	DESCRIPTION	DATE	REV	DESCRIPTION
02/08/2003	HJ	DC-DC BOARD	02/08/2003	HJ	DC-DC BOARD
HA, JS	PR	3.3V & 5V GENERATION	HA, JS	PR	3.3V & 5V GENERATION
LEE, CH	REV	10	LEE, CH	REV	10
MODULE CODE	LAST EDIT	March, 9, 2002 4:21:54 PM	MODULE CODE	LAST EDIT	March, 9, 2002 4:21:54 PM
PAGE	2	OF	PAGE	2	OF
3			3		



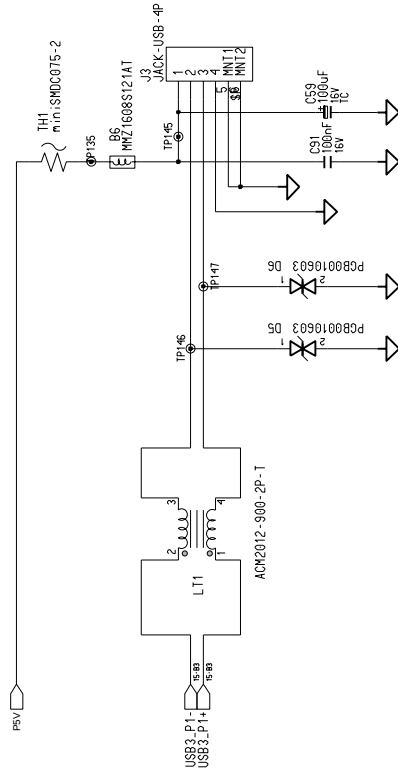
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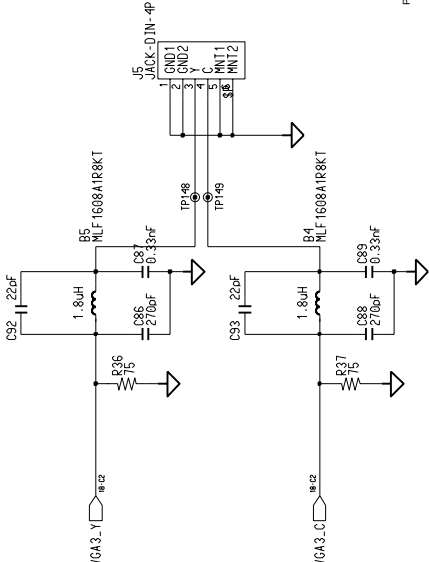
CHANGE THIS CONNECTOR TO HEADER < 12809A-48G5T>
FROM DCDC TO MAIN BOARD



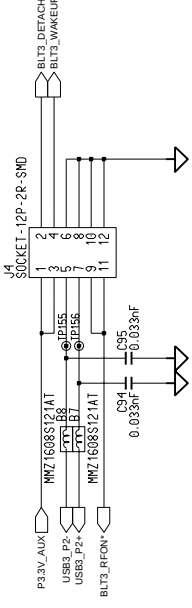
USB
90ohm + - 10%



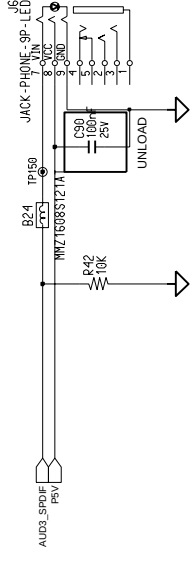
SUPER - VHS TV OUT



bluetooth connector

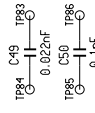


SPDIF OUT



NO	CONNECTION	DATE	REV	REV	REV
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2	1-2				
3	2-3				
4	3-1				
5	1-2-3				
6	N.C.				
7	1-2				
8	2-3				
9	3-1				
10	1-2-3				

REV1
b
20 03



REV	DATE	TITLE	SAMSUNG
SEC, HJ	02/08/2003	AQUILA_C	ELECTRONICS
HA, JS	REV. 31P	DC-DC BOARD	
LEE, CH	REV	CONNECTOR & PORT	
MODULE CODE	LAST EDIT	March, 9, 2002 4:23:55 PM	PAGE 3 OF 3