

 Elitegroup Computer Systems	
Title	
BLOCK DIAGRAM	
Size	Document Number
Custom	400-1-4-01
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Rev	A.0

Voltage Rails	ON S0-S1	ON S3	ON S4	ON S5	Control signal
12VOUT	X	X	X	X	
3V_591	X	X	X	X	
5VPCU	X	X	X	X	
+3V_S5	X	X	X	X	S5_ON
+1.5V_S5	X	X	X	X	S5_ON
+1.8VSUS	X	X			SUS_ON
+3VSUS	X	X			SUS_ON
+5VSUS	X	X			SUS_ON
+0.9VSUS	X	X			SUS_ON
CPU_CORE	X	X			VR_ON
+0.9V	X				MAIN_ON
+VCCP	X				MAIN_ON
+1.5V	X				MAIN_ON
+1.8V	X				MAIN_ON
+2.5V	X				MAIN_ON
+3V	X				MAIN_ON
+5V	X				MAIN_ON
+12V	X				MAIN_ON

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Giga LAN	AD22	0	B
Mini-PCI	AD23	1	C, D
CardBus+1394	AD24	2	E, F, G

EC SM Bus1 address

Device

Smart Battery

THERMAL SENSOR 1001 100X b

SB450MB SM Bus address

Device

SODIMM 1010 000X b

Clock Gen 1101 001x b

Functions with Spread Spectrum Capibility for Clock

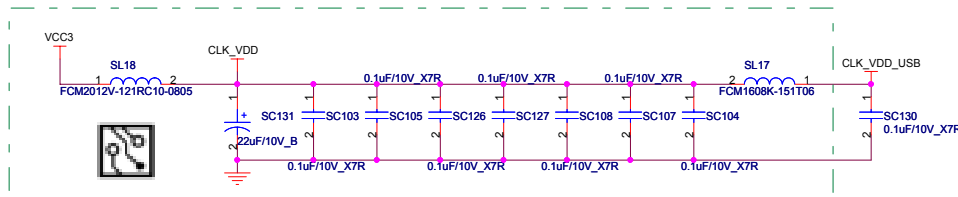
Memory

LVDS

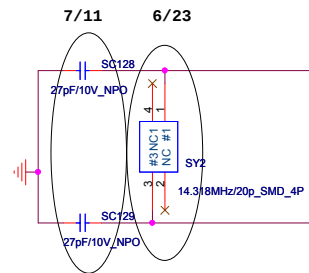
Host Bus

PCIE Interface

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SYSTEM INFO			
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- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS U300 AS POSSIBLE
- 2- ROUTE ALL CPUCCLK/#, NBCLK/# AND ITPLCLK/# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U300 POWER PIN



From uP-->

14 CLKEN#
16,33 CPUSTP#

11,12,17 SCLK
11,12,17 SDATA

$$I_{REF} = VDD / (3 \times R_{RR})$$

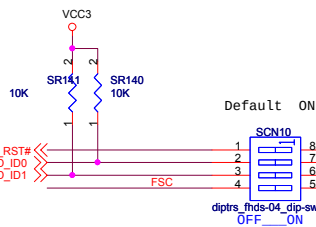
$I_{oh} = 6 \times I_{ref}$
(2.32mA)
 $V_{oh} = 0.7V @ 50 ohm$



ICS951413/RTM8651

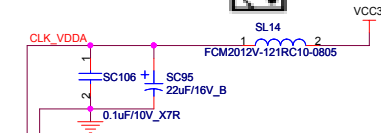
CK410 FREQUENCY SELECT TABLE(MHZ)

FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF
1	0	1	100	100	33	14.31
0	0	1	133	100	33	14.31
0	1	1	166	100	33	14.31
0	1	0	200	100	33	14.31
0	0	0	266	100	33	14.31
1	0	0	333	100	33	14.31
1	1	0	400	100	33	14.31
1	1	1	Resv	100	33	14.31



Check if needed in next version -->

<-- LOW: FSB533(DEFAULT), HIGH: FSB400



>>> NBCLK# 9
>>> NBCLK 9
>>> CPUCLK# 4
>>> CPUCLK 4

SR114 49.9 1%
SR115 49.9 1%
SR116 49.9 1%
SR117 49.9 1%

SR118 49.9 1%
SR119 49.9 1%

SR138 49.9 1%
SR139 49.9 1%

>>> ALINKCLK 8
>>> ALINKCLK# 8
>>> SBSRCLK 16
>>> SBSRCLK# 16

CK410#=LOW CK410 MODE

USB_48

SR134 33

CLK_VDD 17

FSC

SR135 4.7K

FSB533# 8

CLK_VDD

FSA

SR112 1 2 4.7K

SR121 33

SR113 33

>>> SB_OSCIN 17

>>> OSC14M 9



Elitegroup Computer Systems

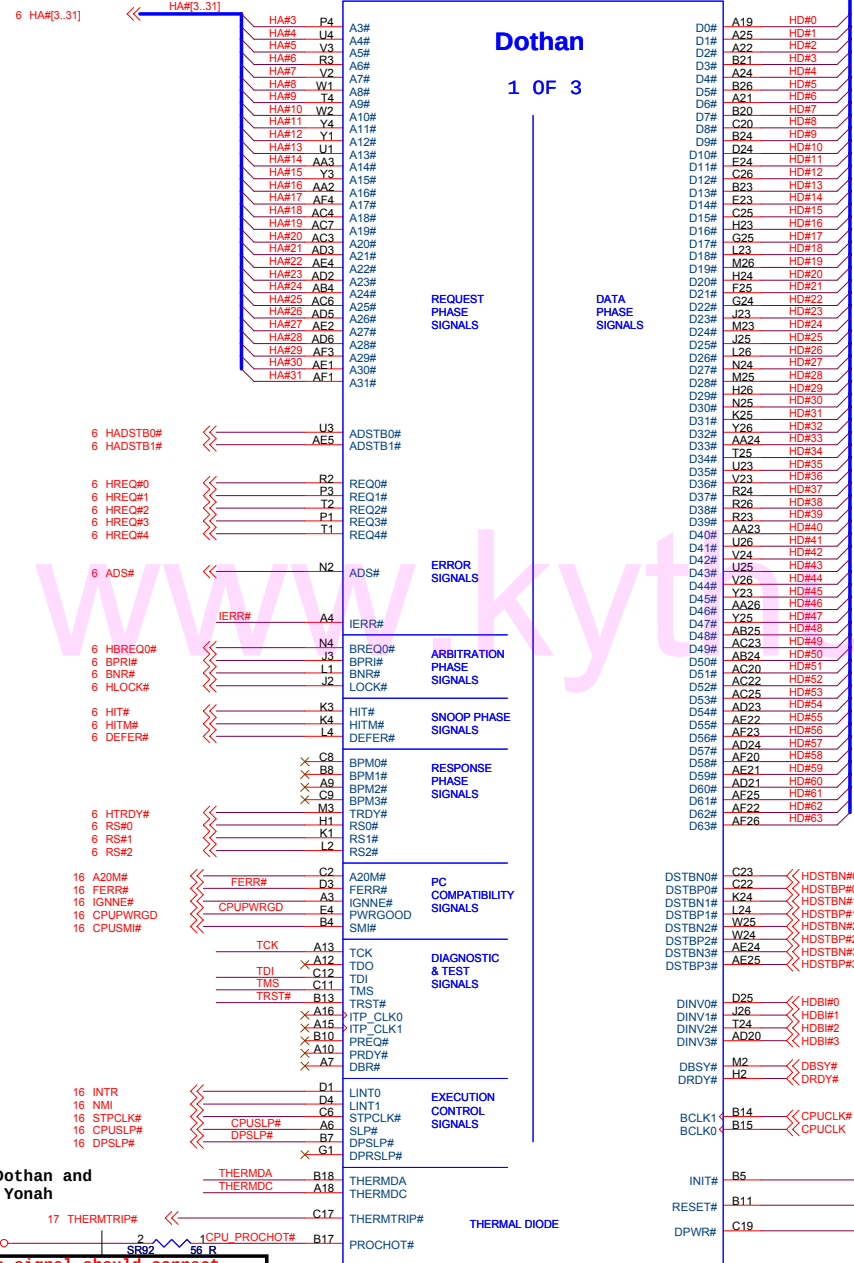
File			
CLK GEN.			
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Dothan

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SUZA

HD#0..63

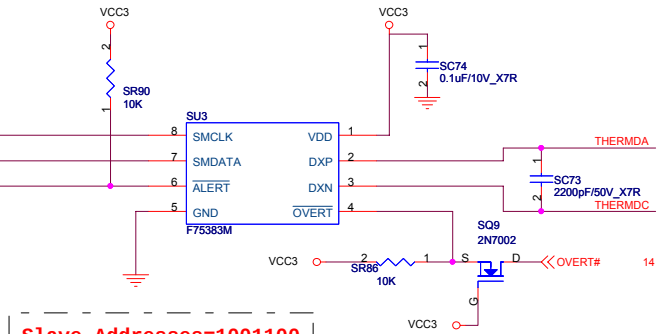


G1: NC for Dothan and
DPRSLP# for Yonah

The signal should connect
to SB and NB w/o T-ing
(No stub)

AMP_1612364-1_BANIAS_SKT

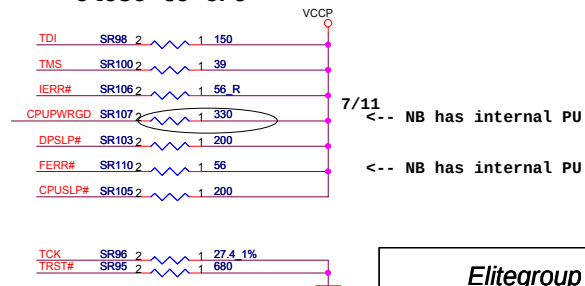
14,15 SMB_CLK3
14,15 SMB_DAT3
14 CPU_ALERT#



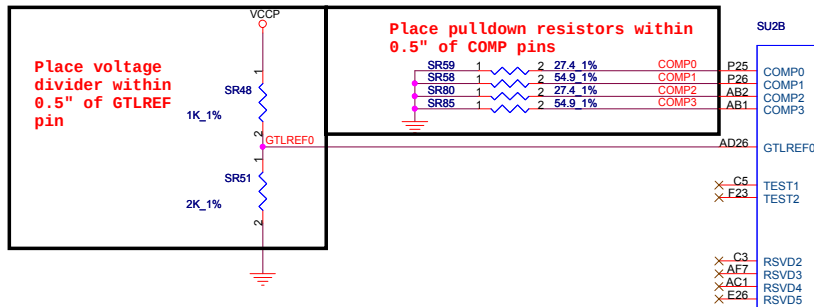
Slave Addresses=1001100

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the CPU
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the CPU
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the CPU
TCK	27 ohm +/- 5%	GND	Within 2.0" of the CPU
TD0	Open	NC	Within 2.0" of the CPU

close to CPU



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POWER, GROUND, RESERVED SIGNALS

POWER, GROUND, RESERVED SIGNALS

POWER, GROUND, RESERVED SIGNALS

POWER, GROUND, RESERVED SIGNALS

POWER, GROUND, RESERVED SIGNALS

POWER, GROUND, RESERVED SIGNALS

POWER, GROUND, RESERVED SIGNALS

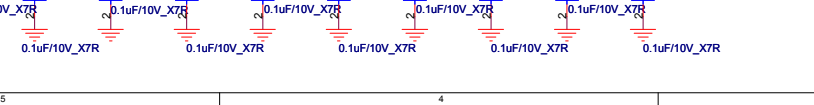
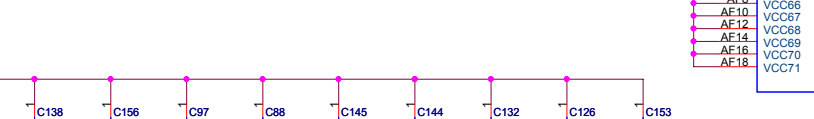
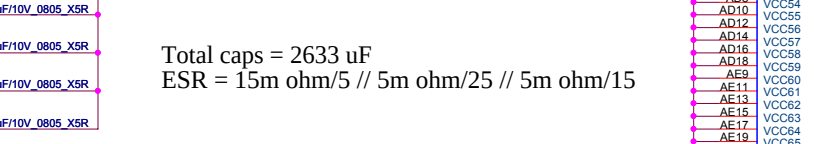
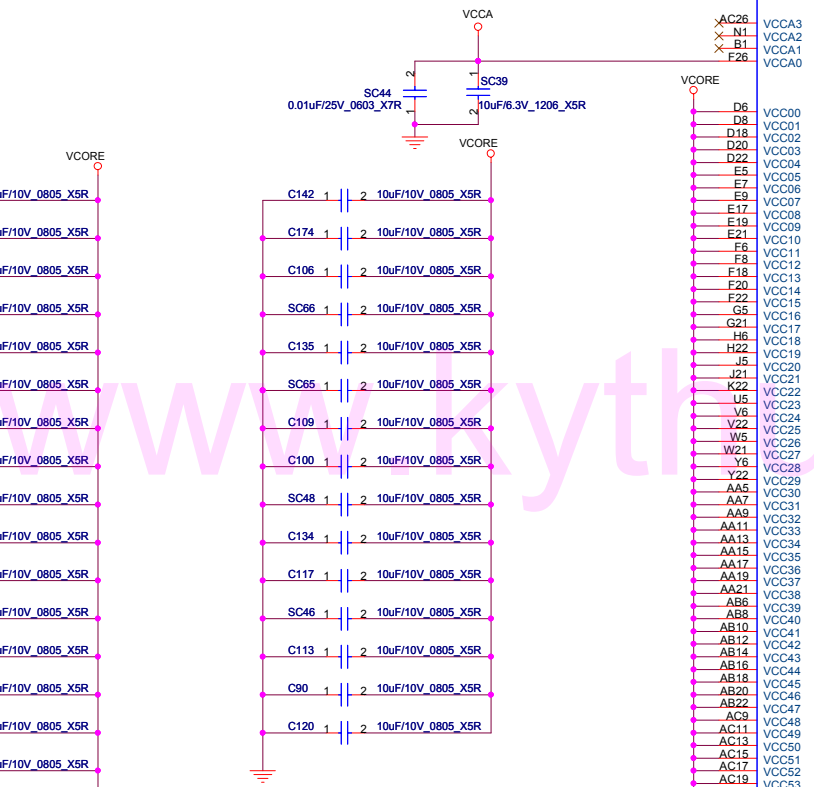
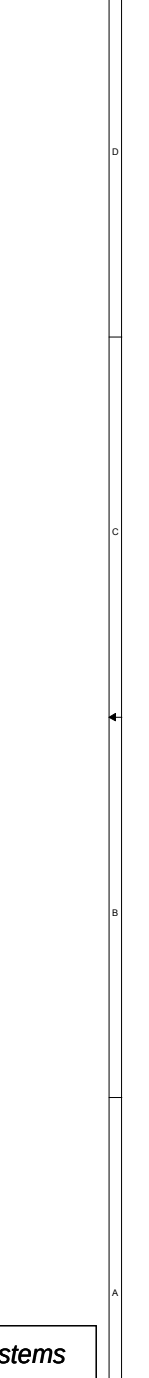
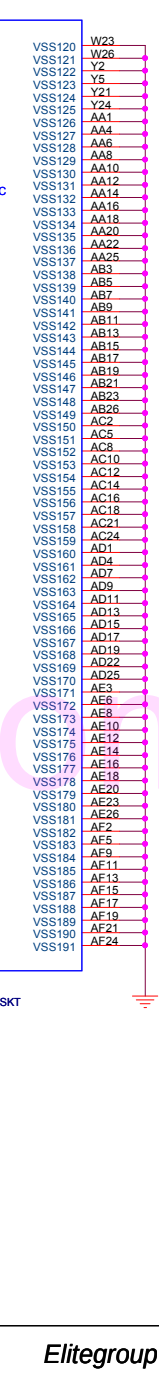
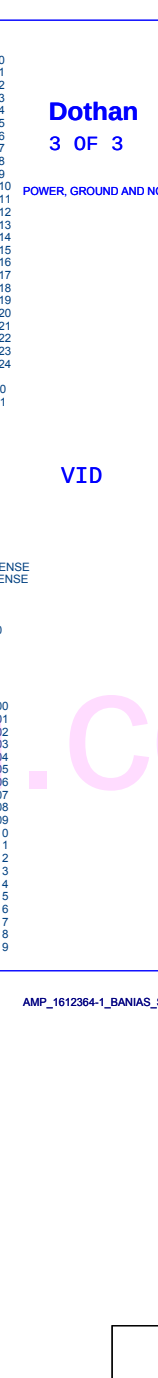
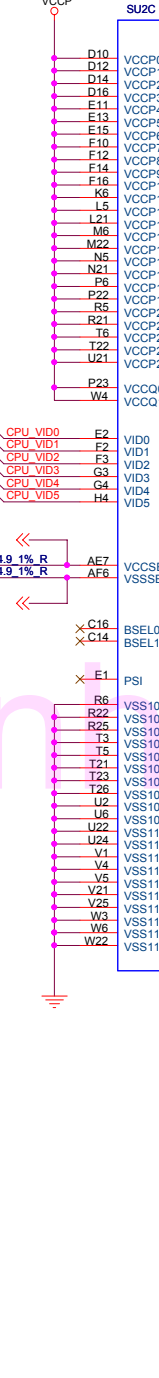
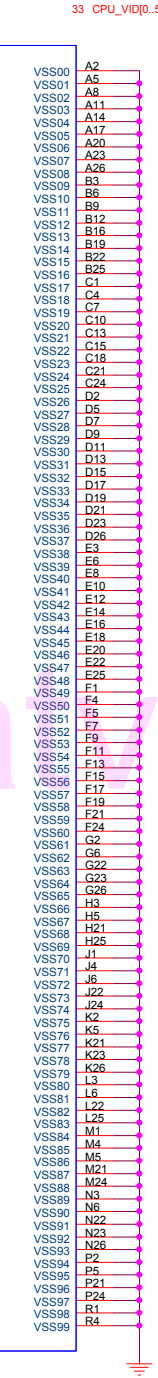
POWER, GROUND, RESERVED SIGNALS

POWER, GROUND, RESERVED SIGNALS

POWER, GROUND, RESERVED SIGNALS

POWER, GROUND, RESERVED SIGNALS

POWER, GROUND, RESERVED SIGNALS



Total caps = 2633 uF
ESR = 15m ohm/5 // 5m ohm/25 // 5m ohm/15

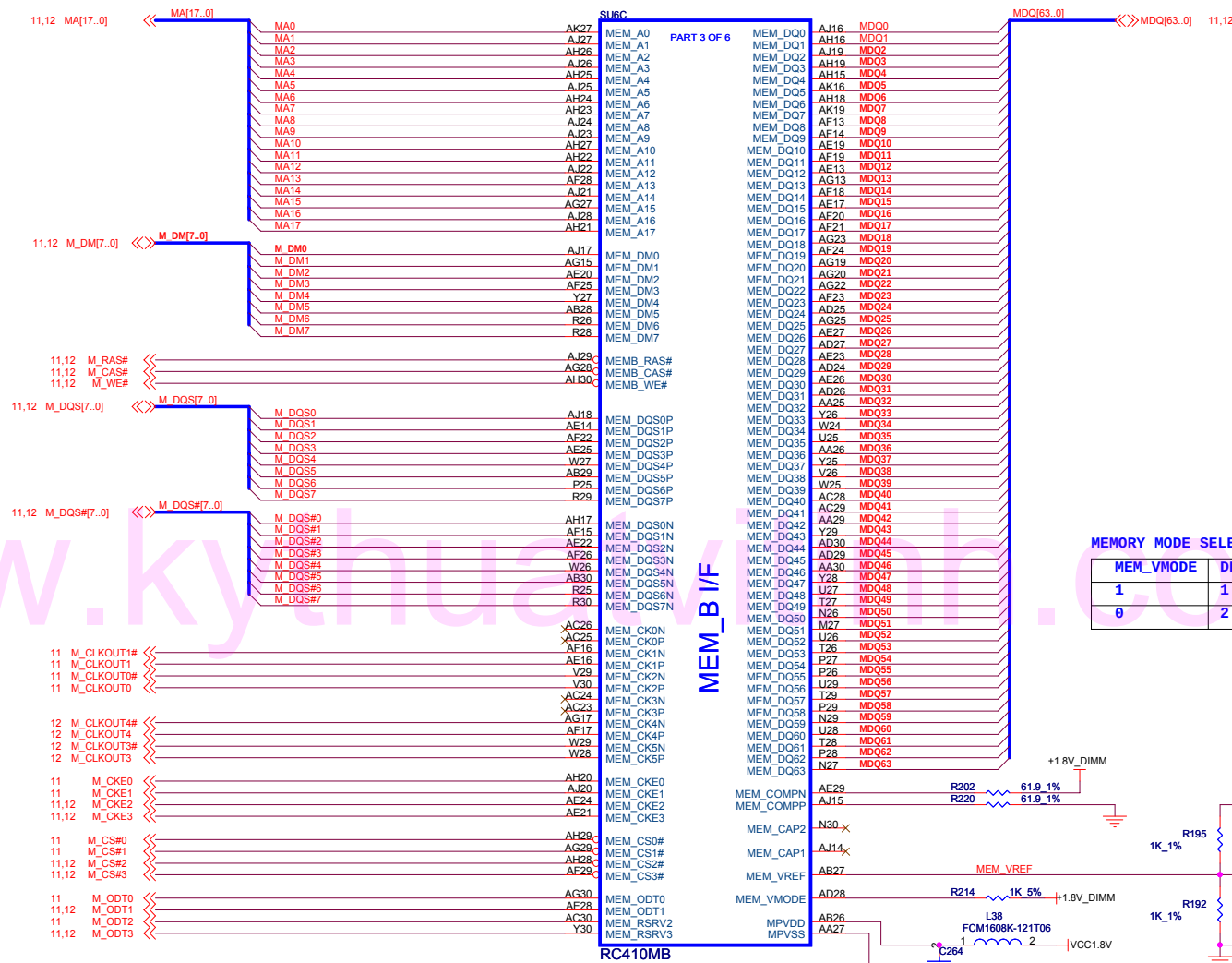
Dothan 3 OF 3

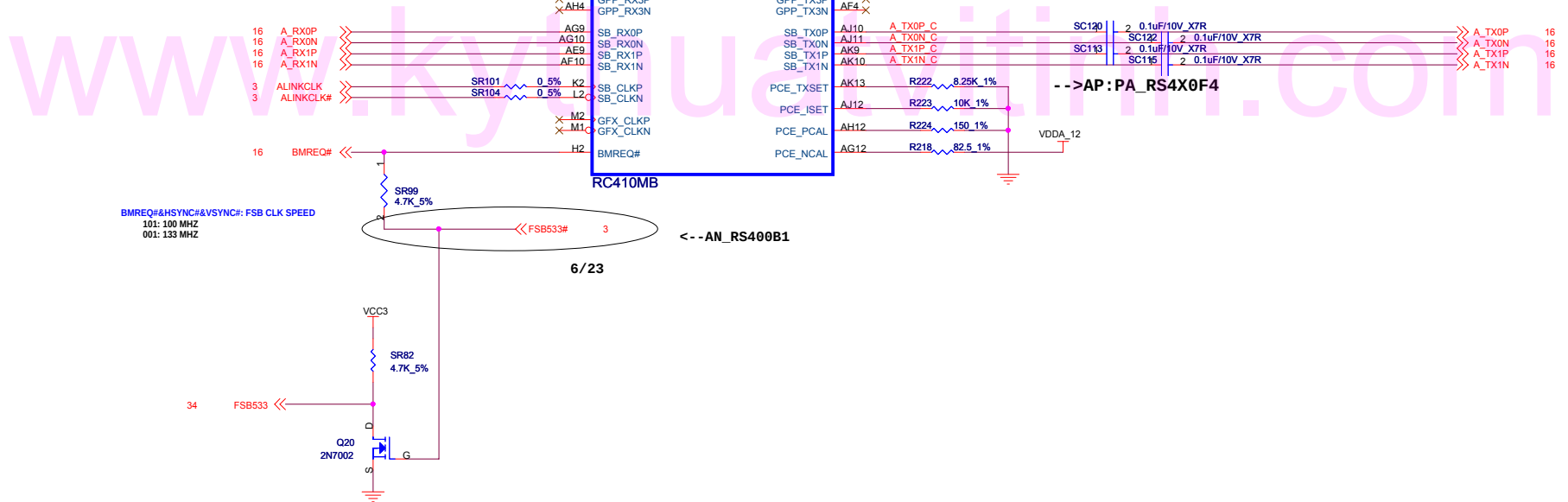
POWER, GROUND AND NC

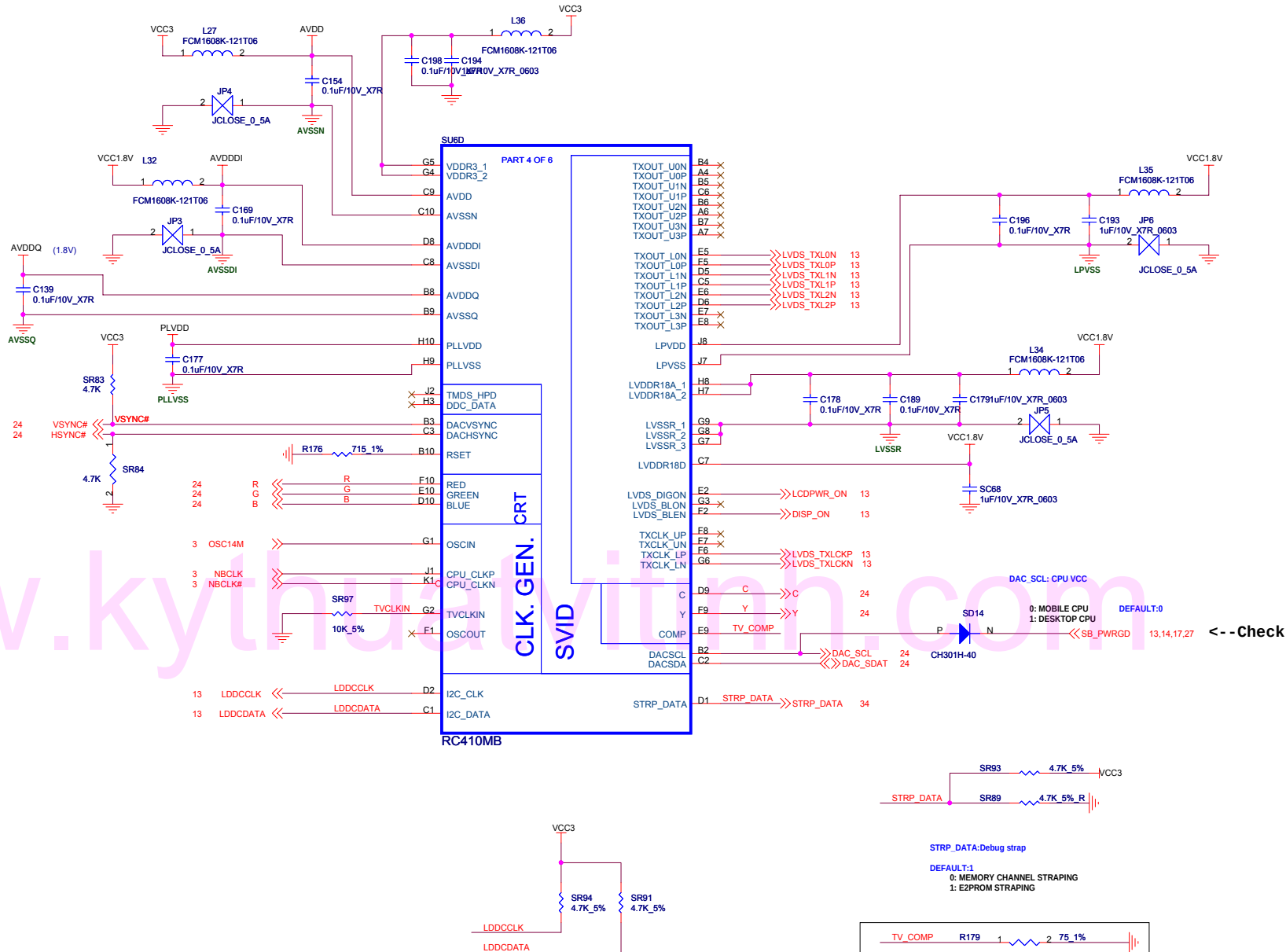
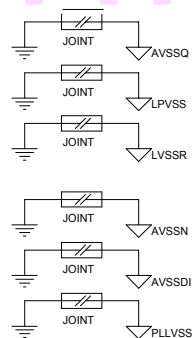
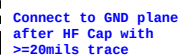
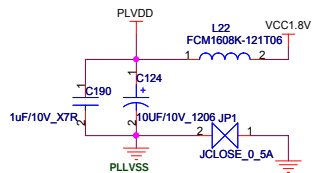
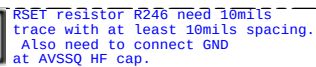
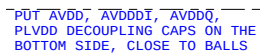
VID

AMP_1612364-1_BANIAS_SKT

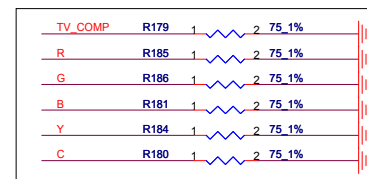
Elitegroup Computer Systems			
Title			
Dothan (POWER/NC)			
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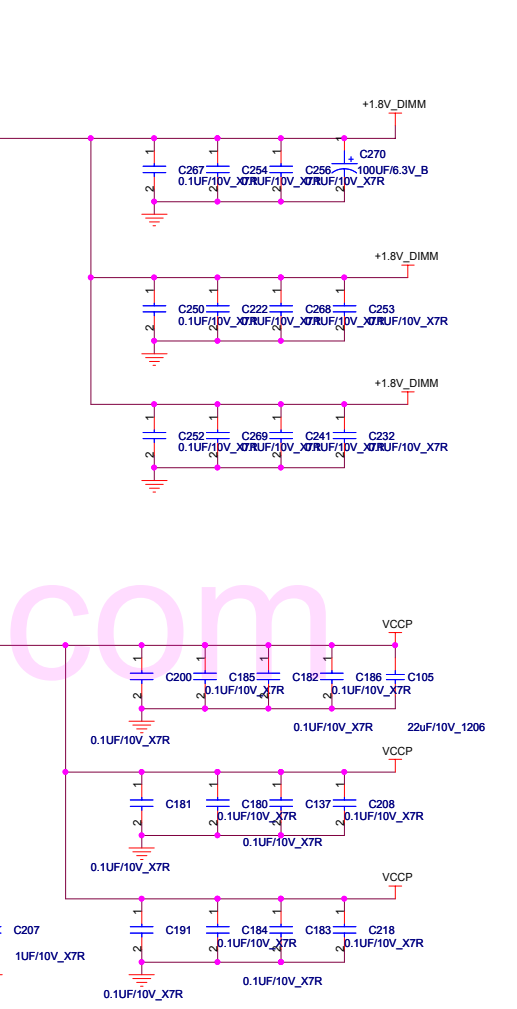
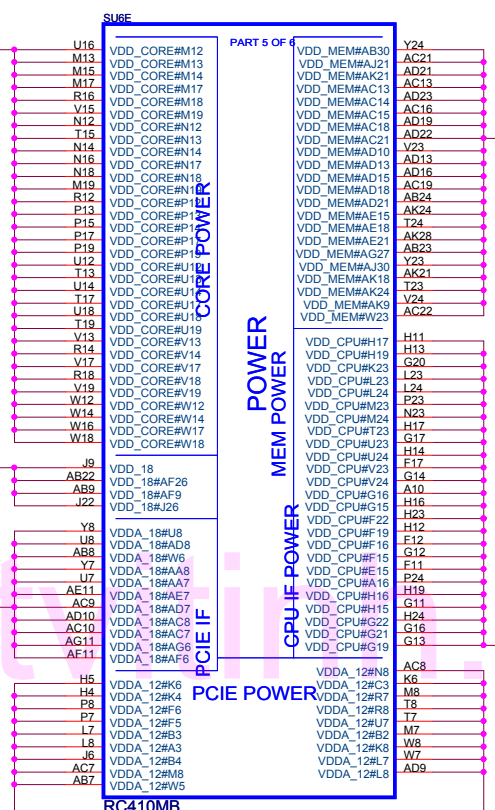
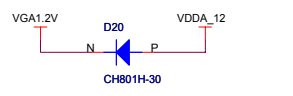
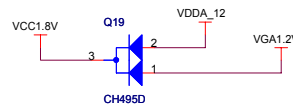
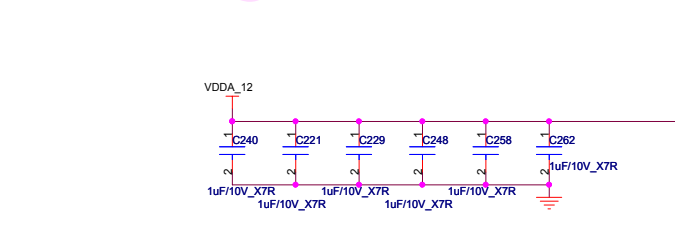
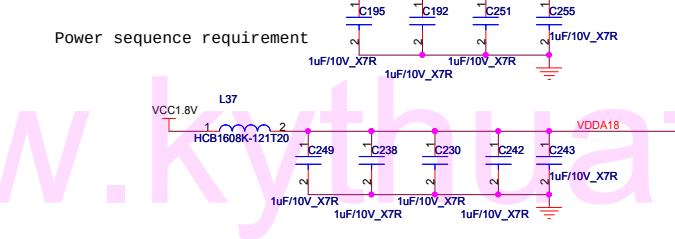
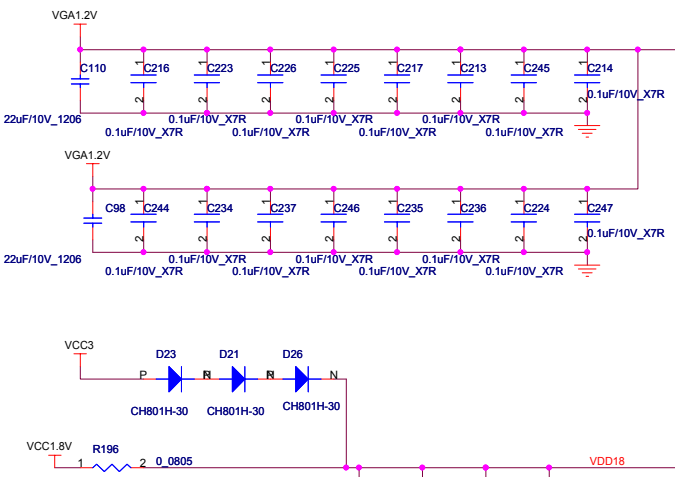
Close to NB-->

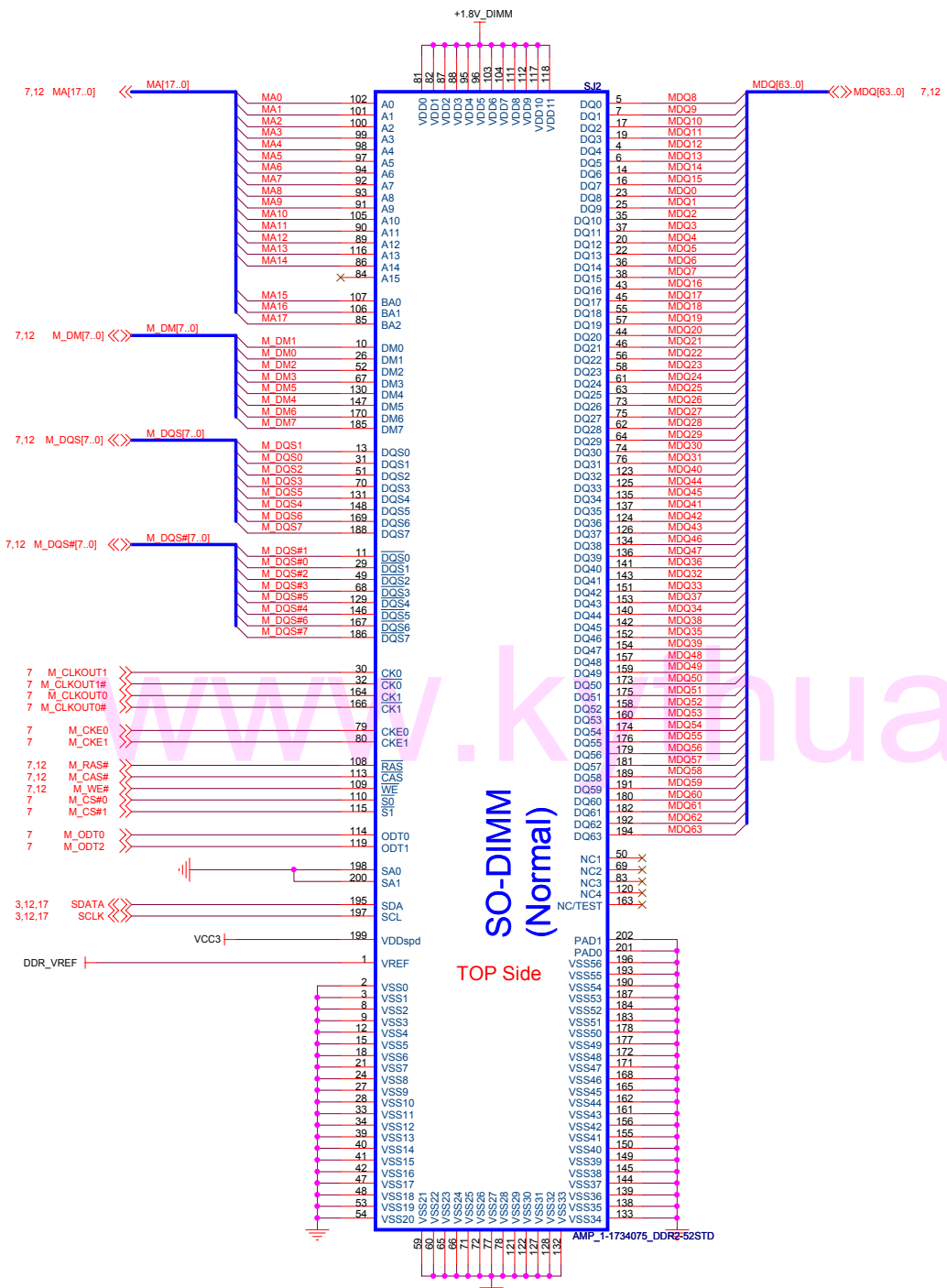


SUBF			
W5	VSSA#U5	VSS#M15	M14
W6	VSSA#U6	VSS#G14	AG16
AB5	VSSA#Y5	VSS#G27	A22
AB6	VSSA#Y6	VSS#G27	A2
V7	VSSA#P8	VSS#G3	D27
AA8	VSSA#P7	VSS#H13	AG26
AA7	VSSA#U8	VSS#H14	H18
AD7	VSSA#Y7	VSS#H23	A16
AD8	VSSA#Y8	VSS#H4	A9
N8	VSSA#L8	VSS#J23	AD17
R7	VSSA#K7	VSS#J24	B27
N7	VSSA#A2	VSS#J30	D24
AE7	VSSA#A5	VSS#K27	T30
AG5	VSSA#A6	VSS#U19	VSS#V30
T6	VSSA#A5	VSS#M16	M16
N5	VSSA#L6	VSS#M11	AD11
AE5	VSSA#H6	VSS#M30	H15
AE6	VSSA#H5	VSS#N15	N15
AE7	VSSA#H6	VSS#N16	N19
AE8	VSSA#H6	VSS#N27	A25
AE9	VSSA#H6	VSS#G5	F3
AE10	VSSA#H6	VSS#P15	R15
AE11	VSSA#H6	VSS#P16	P16
AE12	VSSA#H6	VSS#P23	G10
AE13	VSSA#H6	VSS#P24	M24
AE14	VSSA#H6	VSS#R12	M12
AE15	VSSA#H6	VSS#R13	R13
AE16	VSSA#H6	VSS#R14	P14
AE17	VSSA#H6	VSS#R15	U13
AE18	VSSA#H6	VSS#R16	VSS#R17
AE19	VSSA#H6	VSS#R17	V18
AE20	VSSA#H6	VSS#R18	R19
AE21	VSSA#H6	VSS#R19	R24
AE22	VSSA#H6	VSS#R20	J30
AE23	VSSA#H6	VSS#R21	T12
AE24	VSSA#H6	VSS#R22	N13
AE25	VSSA#H6	VSS#R23	T14
AE26	VSSA#H6	VSS#R24	P18
AE27	VSSA#H6	VSS#R25	T16
AE28	VSSA#H6	VSS#R26	T18
AE29	VSSA#H6	VSS#R27	U17
AE30	VSSA#H6	VSS#R28	W19
AE31	VSSA#H6	VSS#R29	J27
AE32	VSSA#H6	VSS#R30	U15
AE33	VSSA#H6	VSS#R31	N17
AE34	VSSA#H6	VSS#R32	M18
AE35	VSSA#H6	VSS#R33	V16
AE36	VSSA#H6	VSS#R34	W17
AE37	VSSA#H6	VSS#R35	M26
AE38	VSSA#H6	VSS#R36	V12
AE39	VSSA#H6	VSS#R37	W13
AE40	VSSA#H6	VSS#R38	V14
AE41	VSSA#H6	VSS#R39	W15
AE42	VSSA#H6	VSS#R40	U23
AE43	VSSA#H6	VSS#R41	U24
AE44	VSSA#H6	VSS#R42	V28
AE45	VSSA#H6	VSS#R43	AG24
AE46	VSSA#H6	VSS#R44	AA24
AE47	VSSA#H6	VSS#R45	AA23
AE48	VSSA#H6	VSS#R46	F30
AE49	VSSA#H6	VSS#R47	K23
AE50	VSSA#H6	VSS#R48	D20
AE51	VSSA#H6	VSS#R49	A19
AE52	VSSA#H6	VSS#R50	D17
AE53	VSSA#H6	VSS#R51	D14
AE54	VSSA#H6	VSS#R52	F27
AE55	VSSA#H6	VSS#R53	D4
AE56	VSSA#H6	VSS#R54	M23
AE57	VSSA#H6	VSS#R55	B30
AE58	VSSA#H6	VSS#R56	B1
AE59	VSSA#H6	VSS#R57	AK29
AE60	VSSA#H6	VSS#R58	AK22

GND

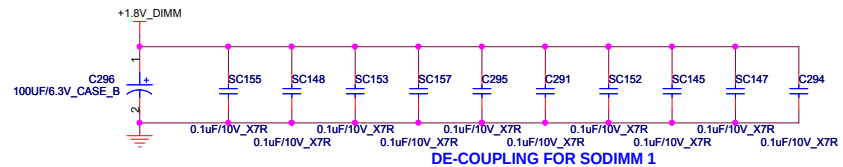
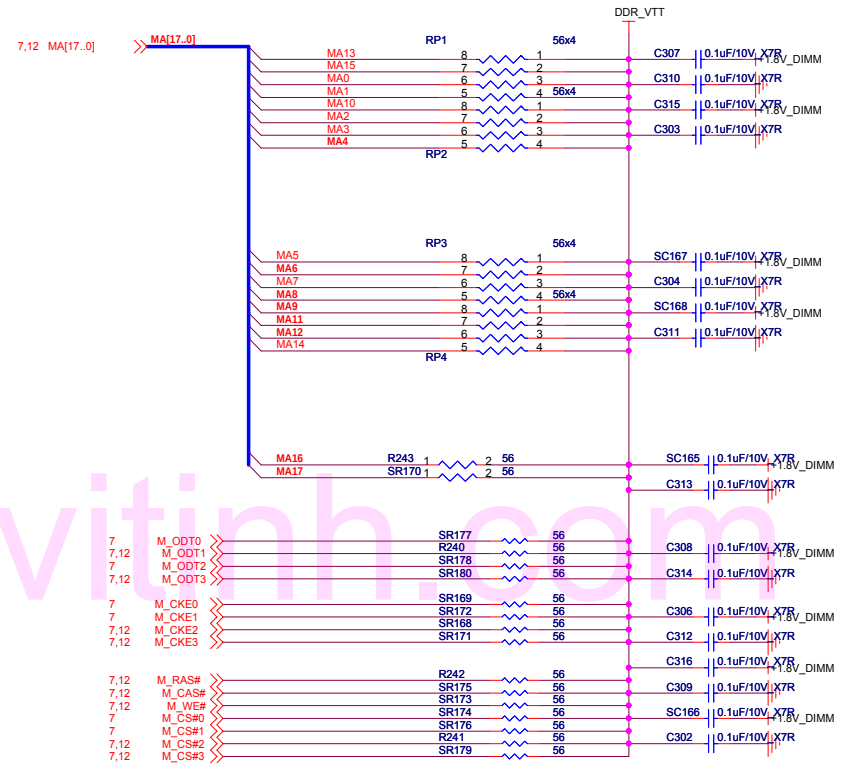
RC410MB

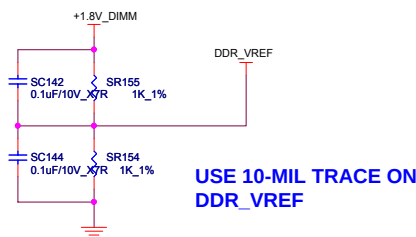
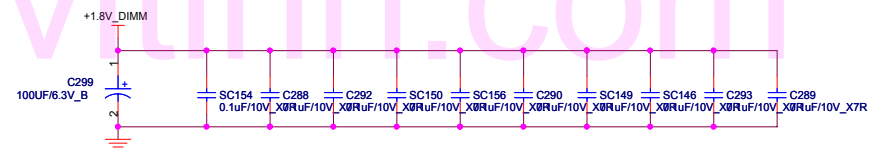
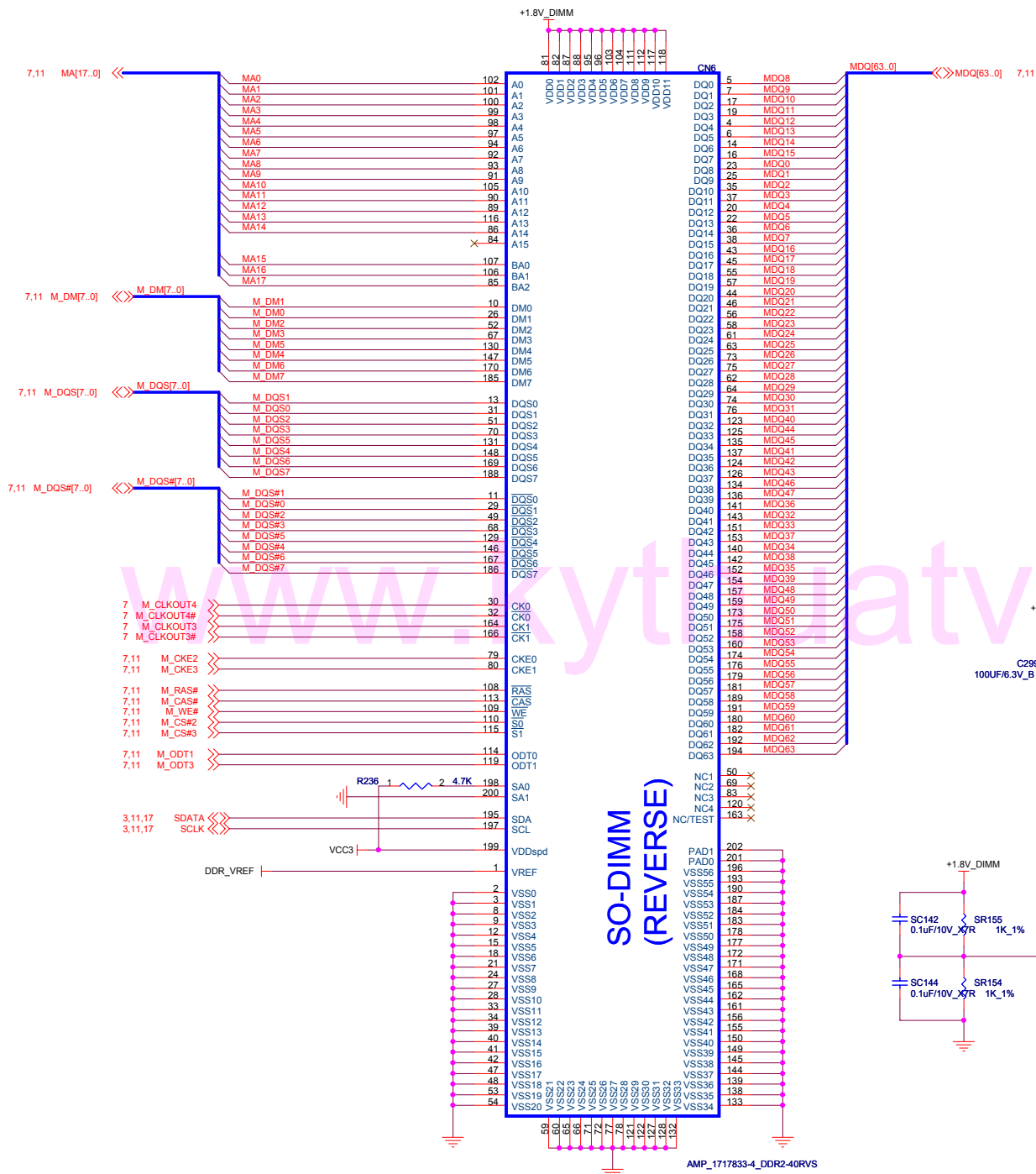




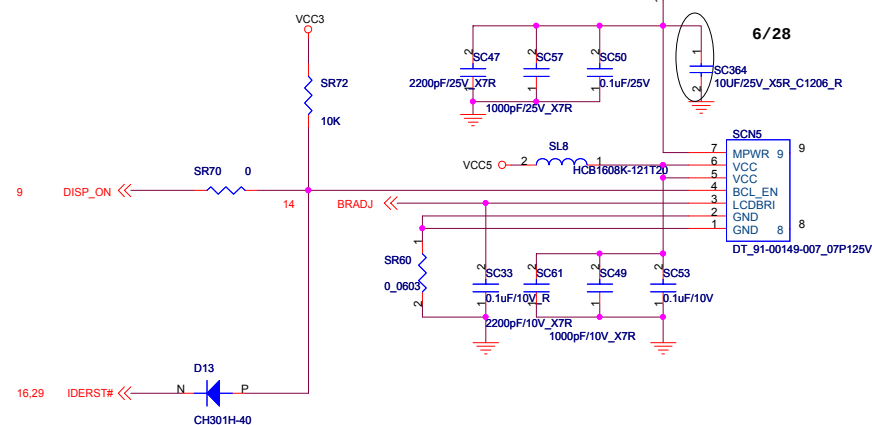
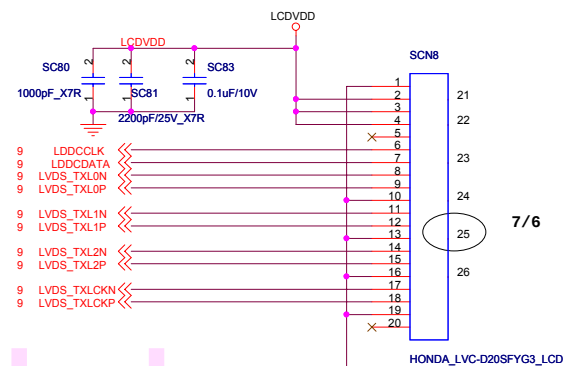
SO-DIMM
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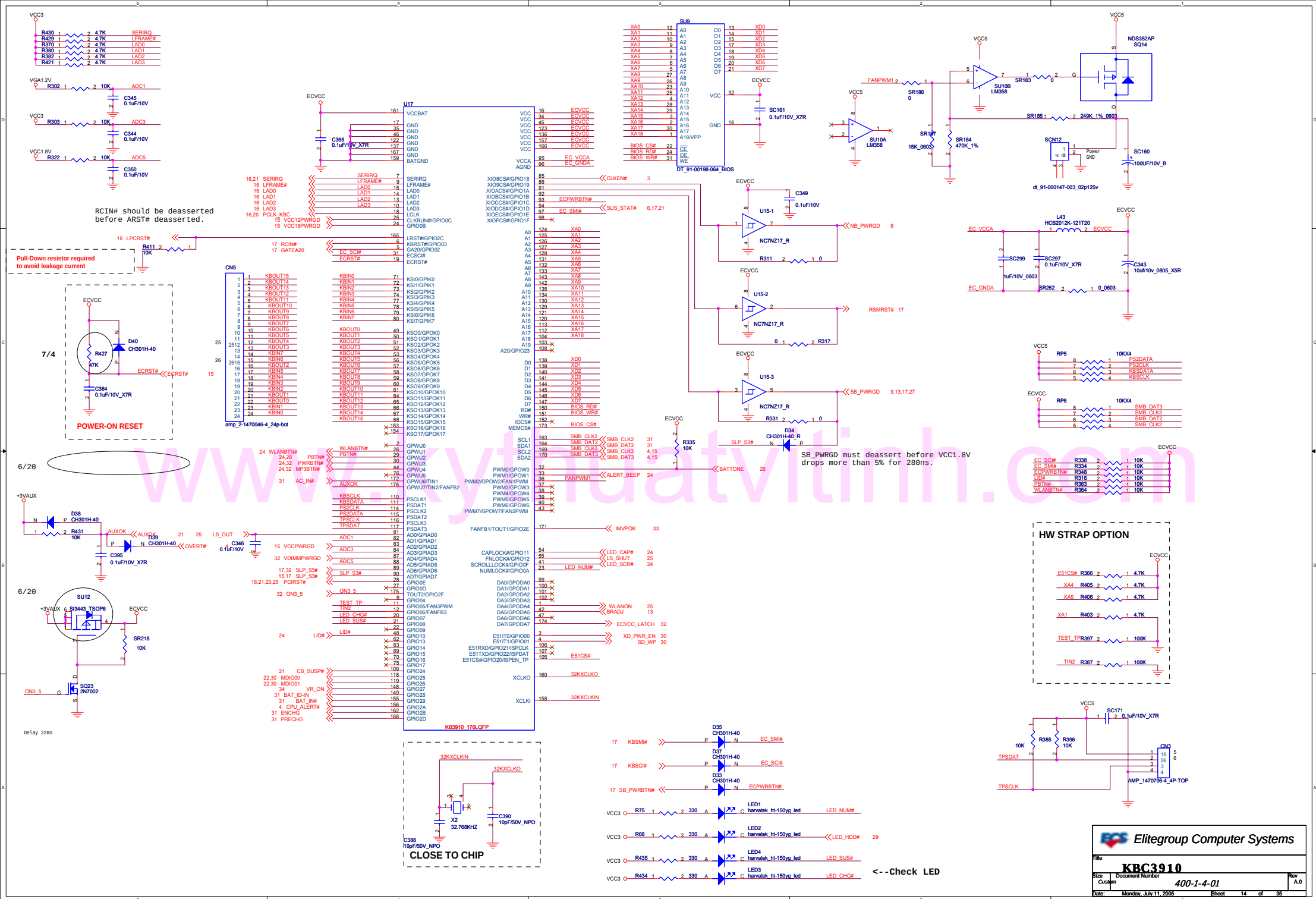
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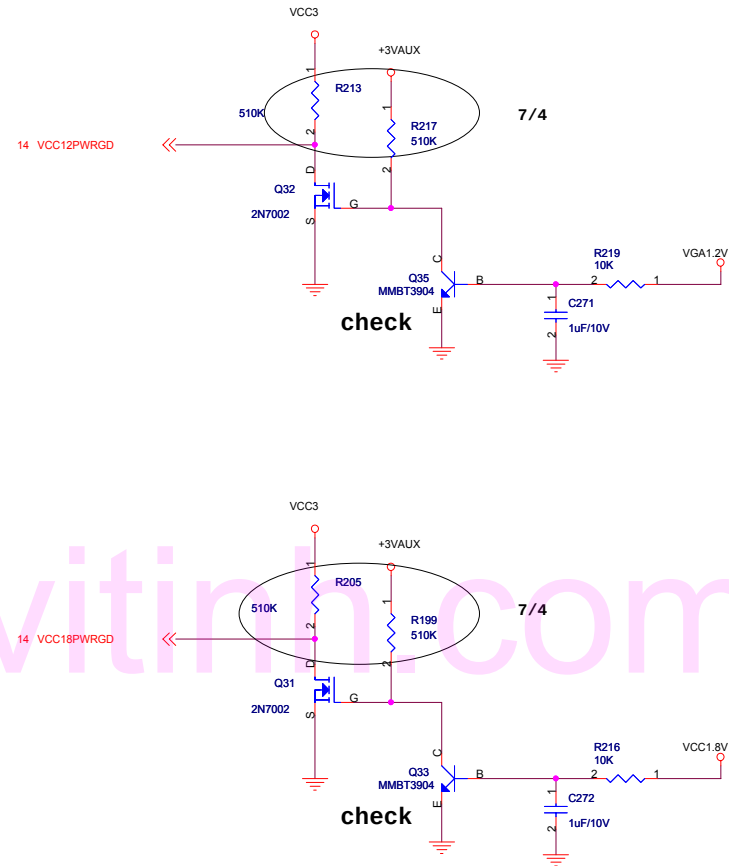
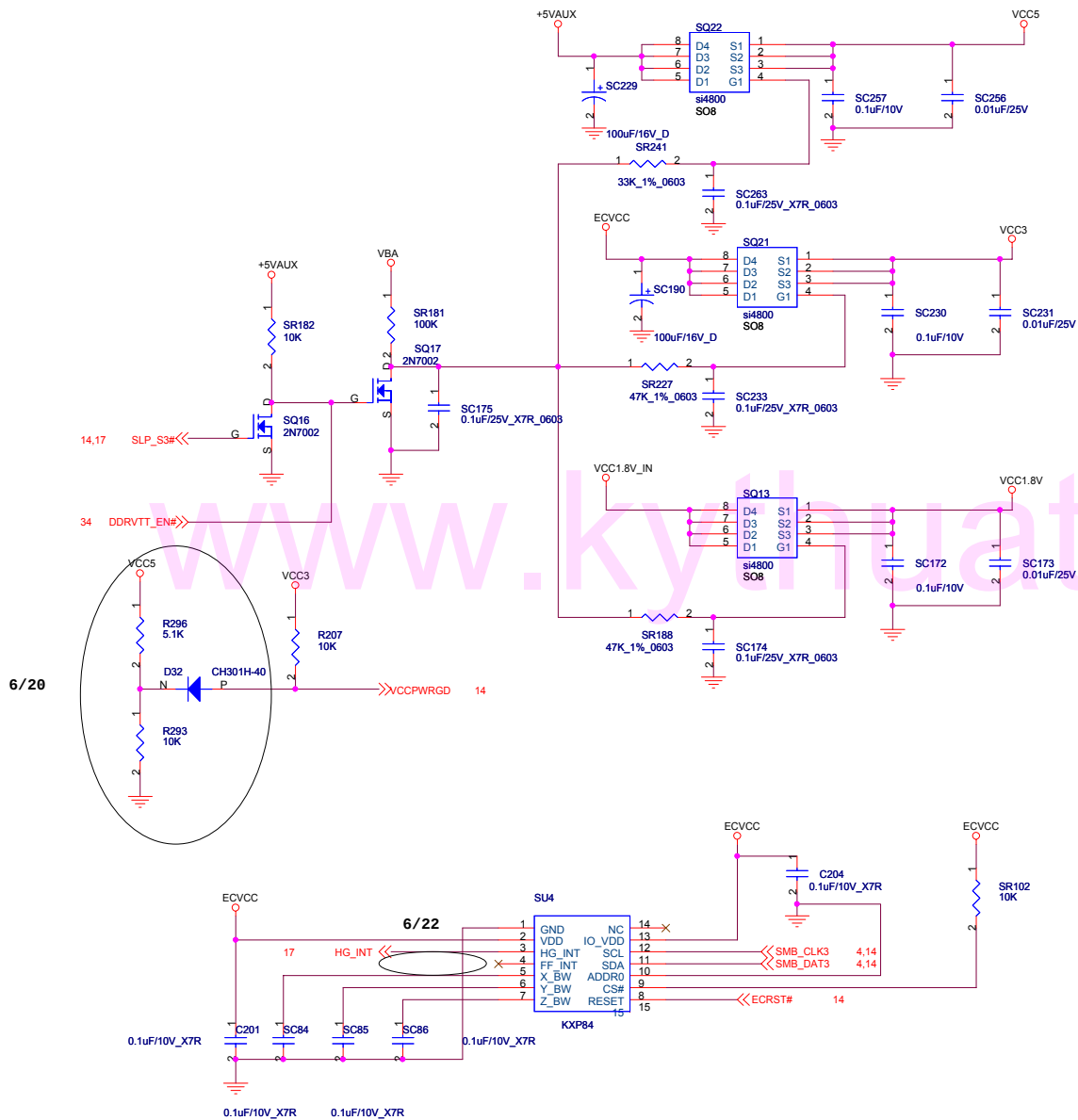


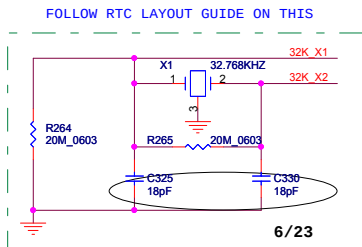


DDR2 SODIMM2		
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<- PA_IXP400AY3

Note: RTC crystal need to lay down

LDRQ#0

LDRQ#1

INT#A

INT#B

INT#C

INT#D

INT#E

INT#F

INT#G

INT#H

INT#I

INT#J

INT#K

INT#L

INT#M

INT#N

INT#O

INT#P

INT#Q

INT#R

INT#S

INT#T

INT#U

INT#V

INT#W

INT#X

INT#Y

INT#Z

INT#AA

INT#AB

INT#AC

INT#AD

INT#AE

INT#AF

INT#AG

INT#AH

INT#AI

INT#AJ

INT#AK

INT#AL

INT#AM

INT#AN

INT#AO

INT#AP

INT#AQ

INT#AR

INT#AS

INT#AT

INT#AU

INT#AV

INT#AW

INT#AX

INT#AY

INT#AZ

INT#BA

INT#BB

INT#BC

INT#BD

INT#BE

INT#BF

INT#BG

INT#BH

INT#BI

INT#BJ

INT#BK

INT#BL

INT#BM

INT#BN

INT#BO

INT#BP

INT#BQ

INT#BR

INT#BS

INT#BT

INT#BU

INT#BV

INT#BW

INT#BX

INT#BY

INT#BZ

INT#CA

INT#CB

INT#CC

INT#CD

INT#CE

INT#CF

INT#CG

INT#CH

INT#CI

INT#CJ

INT#CK

INT#CL

INT#CM

INT#CN

INT#CO

INT#CP

INT#CQ

INT#CR

INT#CS

INT#CT

INT#CU

INT#CV

INT#CW

INT#CX

INT#CY

INT#CZ

INT#DA

INT#DB

INT#DC

INT#DD

INT#DE

INT#DF

INT#DG

INT#DH

INT#DI

INT#DJ

INT#DK

INT#DL

INT#DM

INT#DN

INT#DO

INT#DP

INT#DQ

INT#DR

INT#DS

INT#DT

INT#DU

INT#DV

INT#DW

INT#DX

INT#DY

INT#DZ

INT#EA

INT#EB

INT#EC

INT#ED

INT#EE

INT#EF

INT#EG

INT#EH

INT#EI

INT#EJ

INT#EK

INT#EL

INT#EM

INT#EN

INT#EO

INT#EP

INT#EQ

INT#ER

INT#ES

INT#ET

INT#EU

INT#EV

INT#EW

INT#EX

INT#EY

INT#EZ

INT#FA

INT#FB

INT#FC

INT#FD

INT#FE

INT#FF

INT#FG

INT#FH

INT#FI

INT#FJ

INT#FK

INT#FL

INT#FM

INT#FN

INT#FO

INT#FP

INT#FQ

INT#FR

INT#FS

INT#FT

INT#FU

INT#FV

INT#FW

INT#FX

INT#FY

INT#FZ

INT#GA

INT#GB

INT#GC

INT#GD

INT#GE

INT#GF

INT#GG

INT#GH

INT#GI

INT#GJ

INT#GK

INT#GL

INT#GM

INT#GN

INT#GO

INT#GP

INT#GQ

INT#GR

INT#GS

INT#GT

INT#GU

INT#GV

INT#GW

INT#GX

INT#GY

INT#GZ

INT#HA

INT#HB

INT#HC

INT#HD

INT#HE

INT#HF

INT#HG

INT#HH

INT#HI

INT#HJ

INT#HK

INT#HL

INT#HM

INT#HN

INT#HO

INT#HP

INT#HQ

INT#HR

INT#HS

INT#HT

INT#HU

INT#HV

INT#HW

INT#HX

INT#HY

INT#HZ

INT#IA

INT#IB

INT#IC

INT#ID

INT#IE

INT#IF

INT#IG

INT#IH

INT#II

INT#IJ

INT#IK

INT#IL

INT#IM

INT#IN

INT#IO

INT#IP

INT#IQ

INT#IR

INT#IS

INT#IT

INT#IU

INT#IV

INT#IW

INT#IX

INT#IY

INT#IZ

INT#JA

INT#JB

INT#JC

INT#JD

INT#JE

INT#JF

INT#JG

INT#JH

INT#JI

INT#JJ

INT#JK

INT#JL

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INT#JR

INT#JS

INT#JT

INT#JU

INT#JV

INT#JW

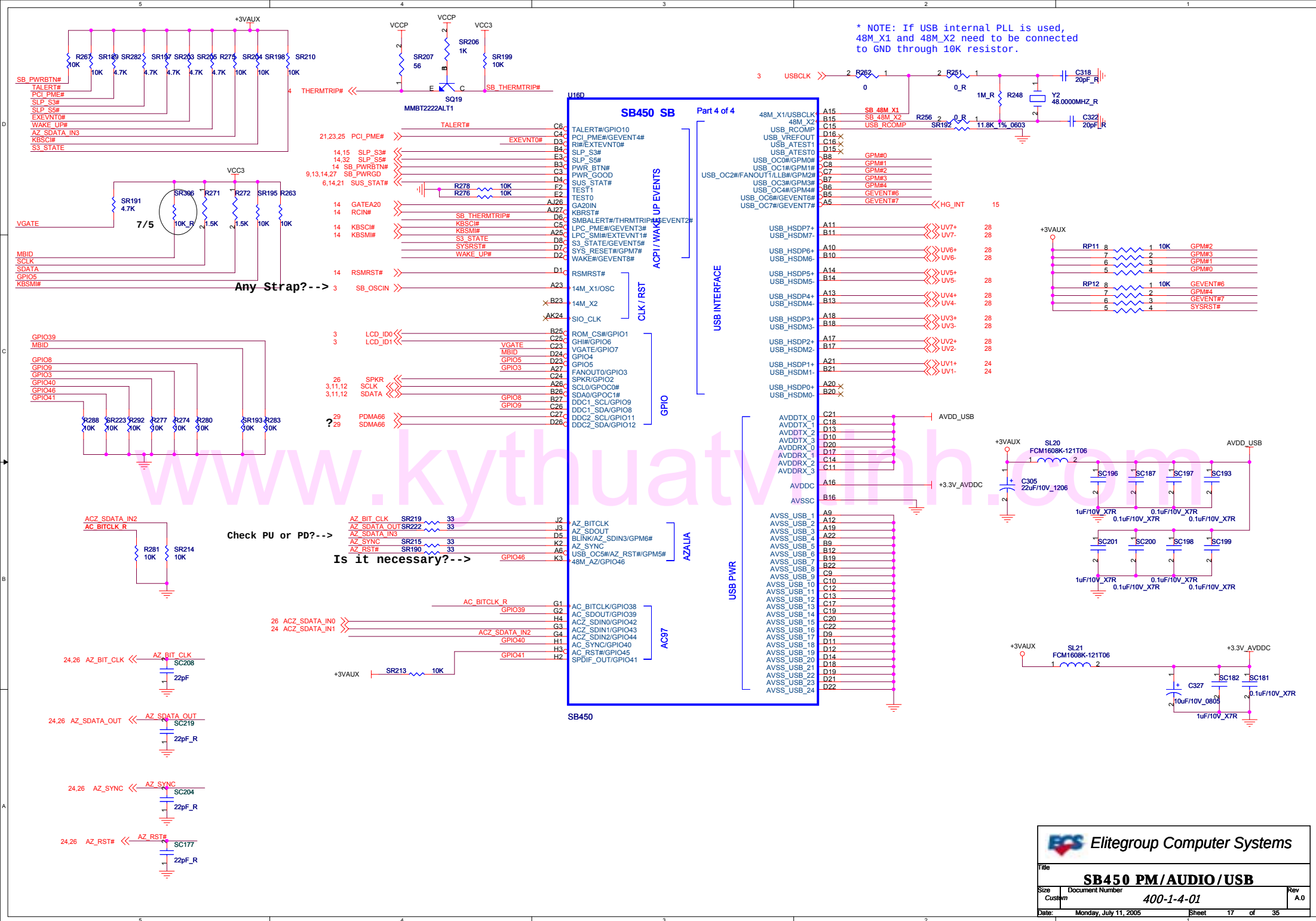
INT#JX

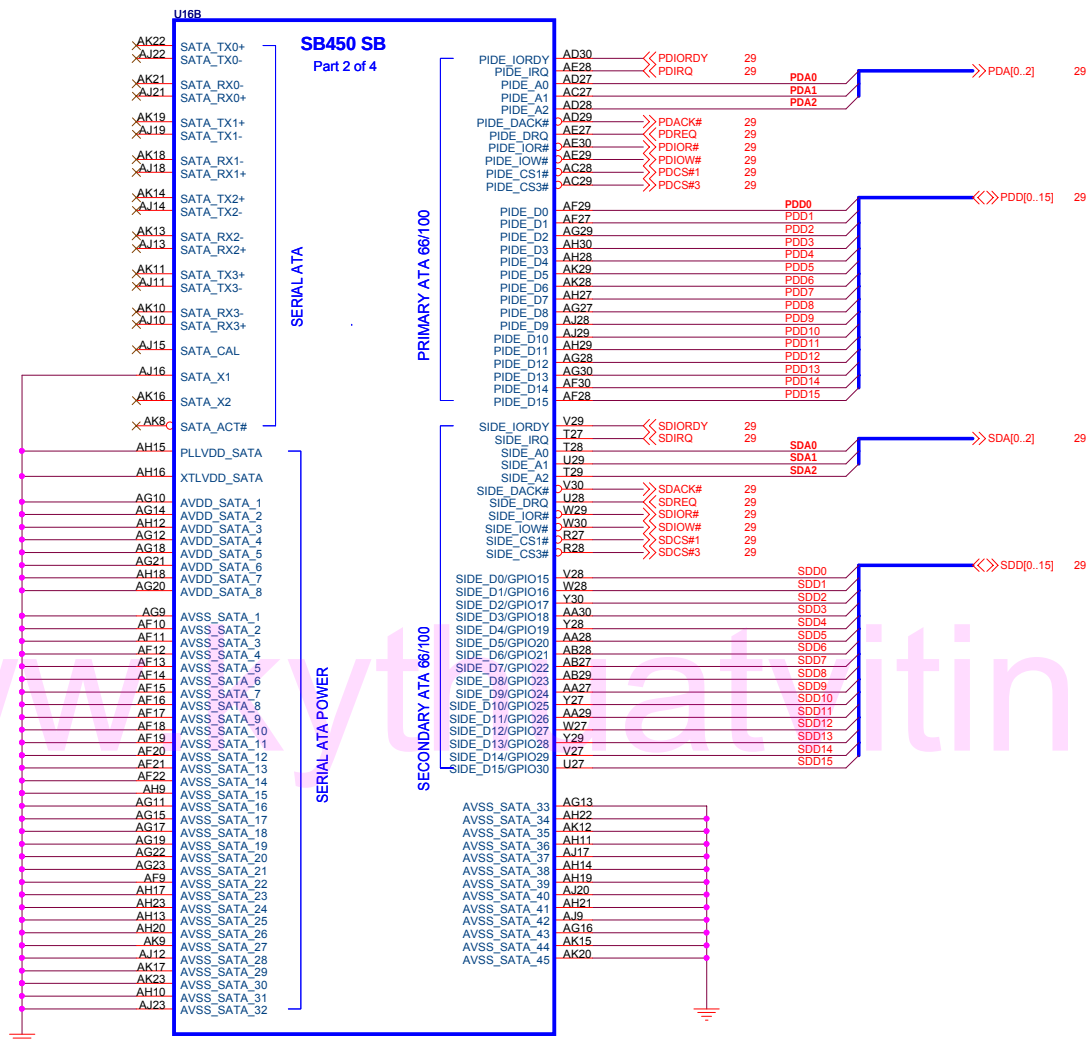
INT#JY

INT#JZ

INT#KA

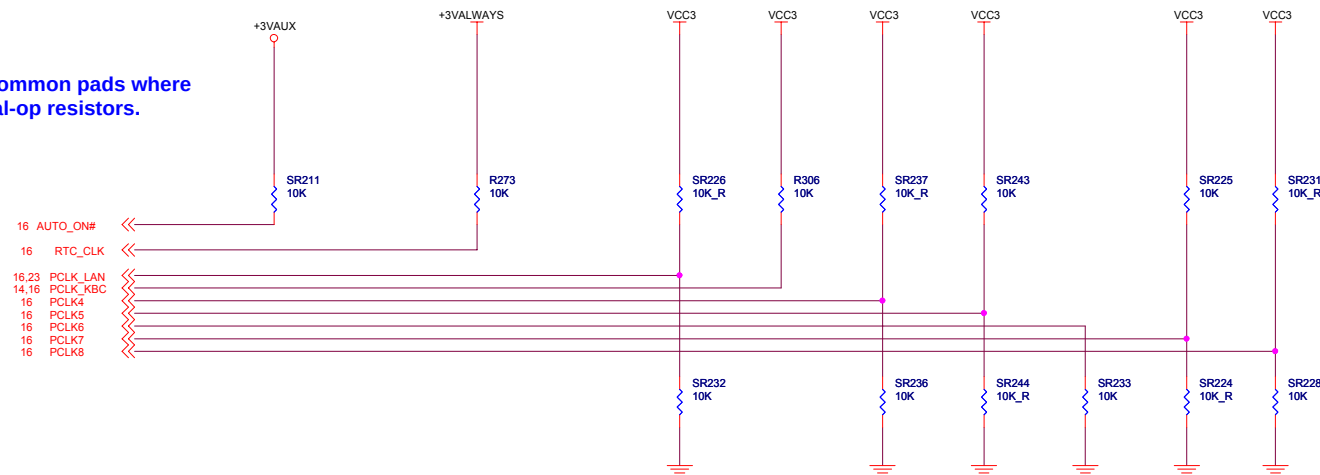
INT#KB





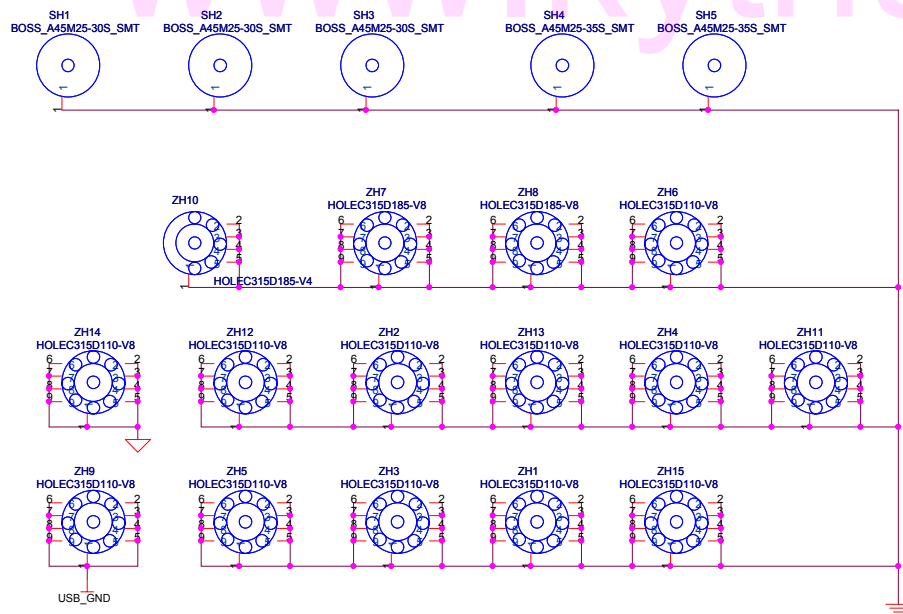


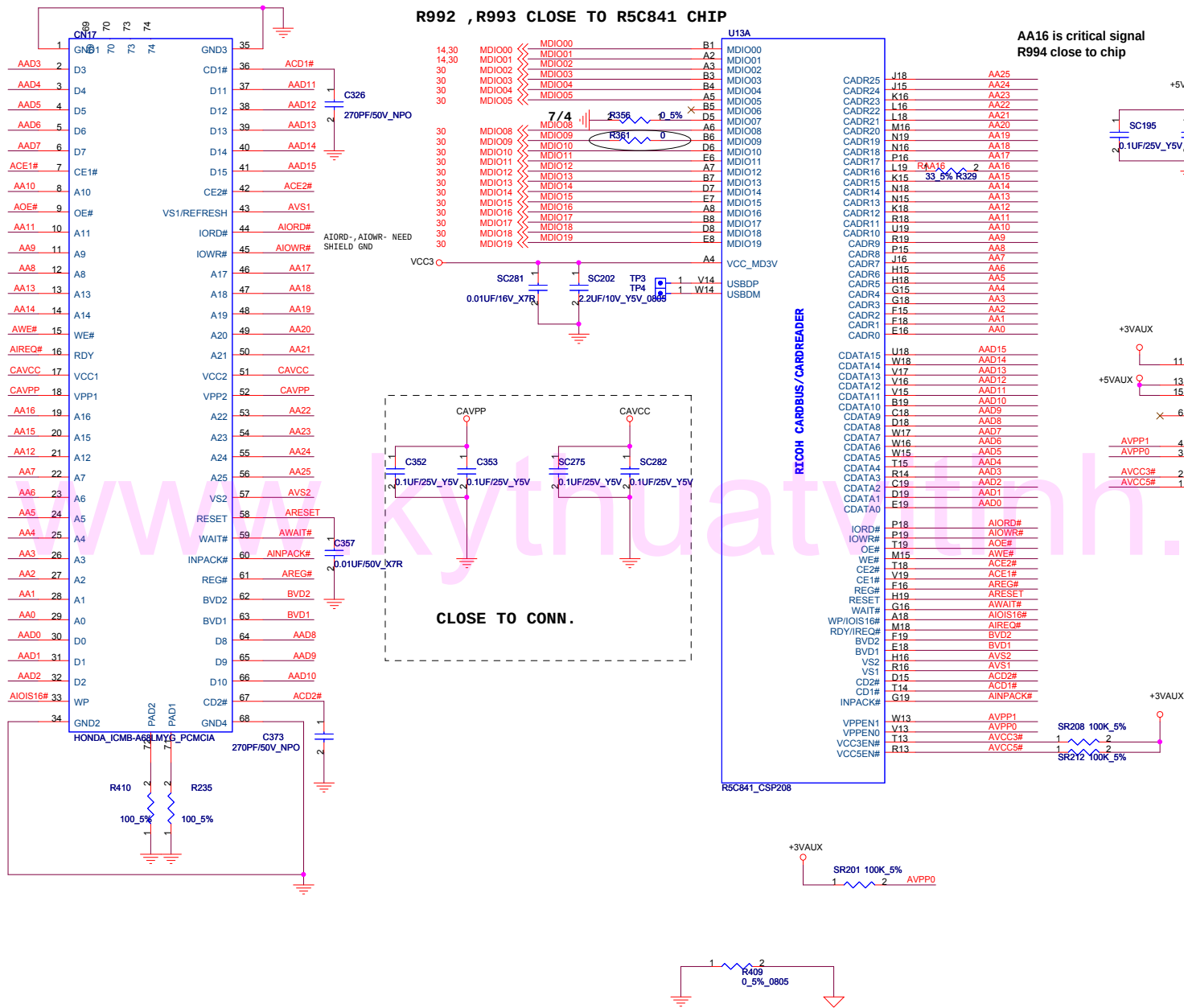
Note: Overlap common pads where possible for dual-op resistors.

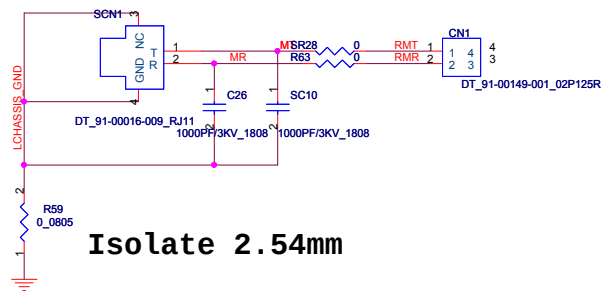
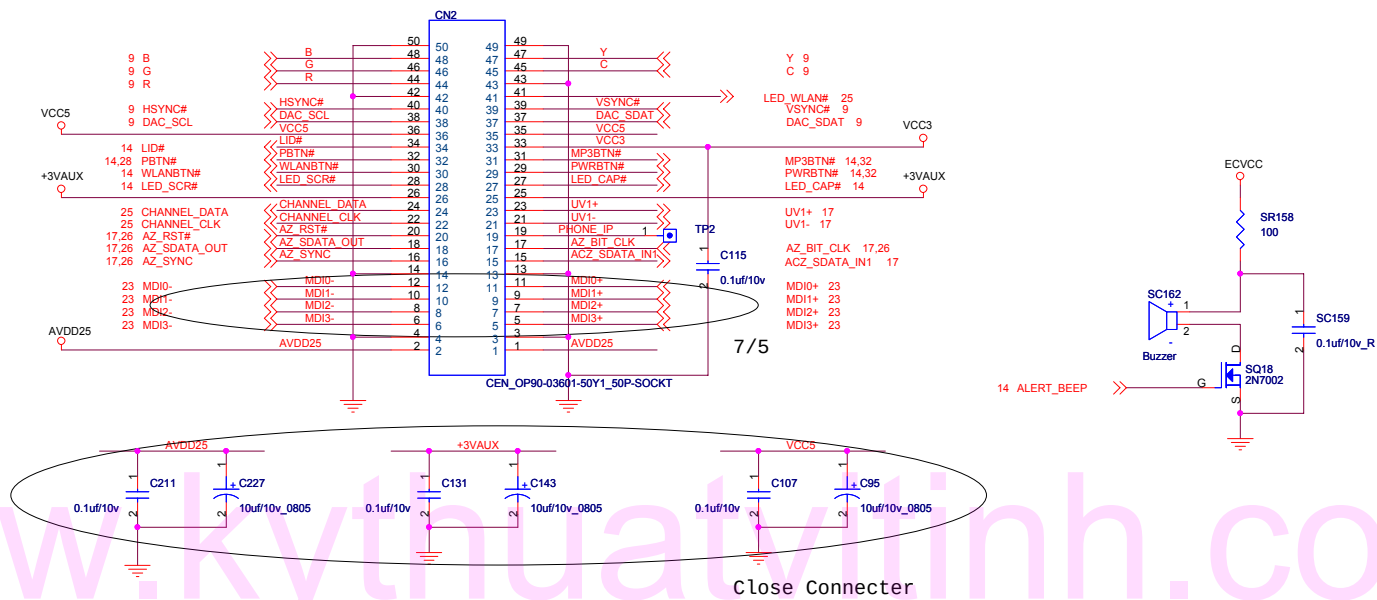


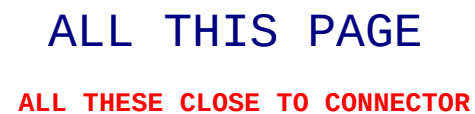
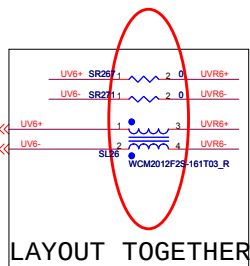
	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK2 PCLK_LAN	PCI_CLK3 PCLK_KBC	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7	PCI_CLK8
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz Crystal Pad DEFAULT	USB PHY PWRDOWN DISABLE DEFAULT	48MHz from Internal USB PLL DEFAULT	A-Link Auto Detect DEFAULT	CPU I/F = K8	ROM TYPE H,H = PCI ROM	
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	48MHz Clock Input Buffer	USB PHY PWRDOWN ENABLE	48MHz from external	A-Link 2 Lanes	CPU I/F = P4 DEFAULT	H,L = LPC ROM I LPC Address Mapped to top 4G L,H = LPC ROM II LPC Address Mapped below 1M L,L = FWH ROM	

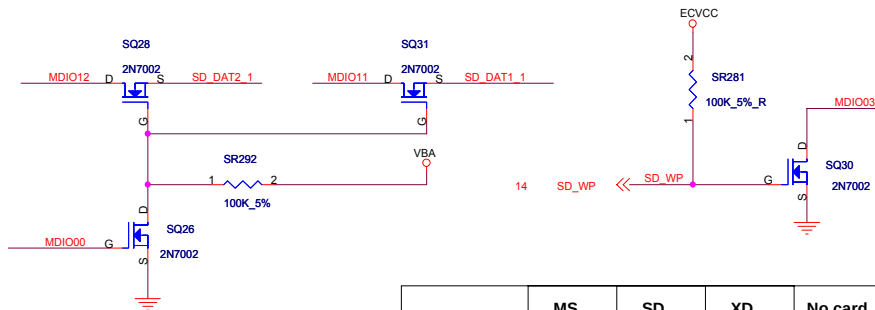
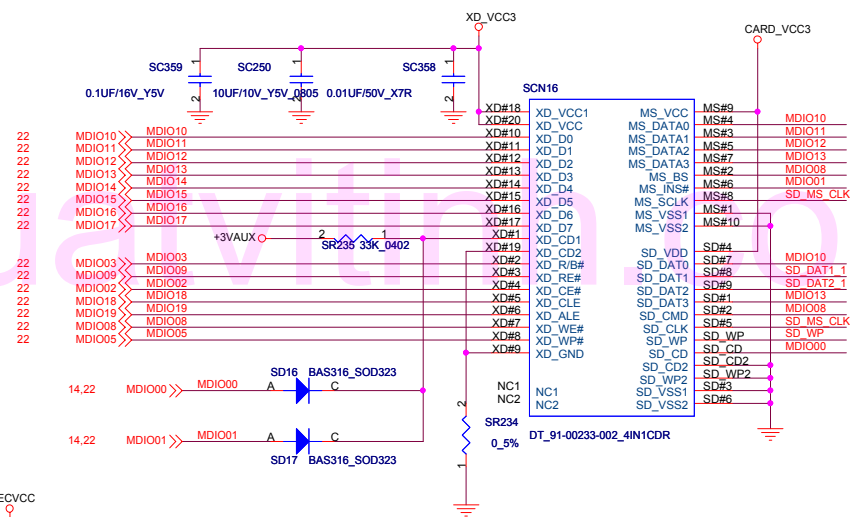
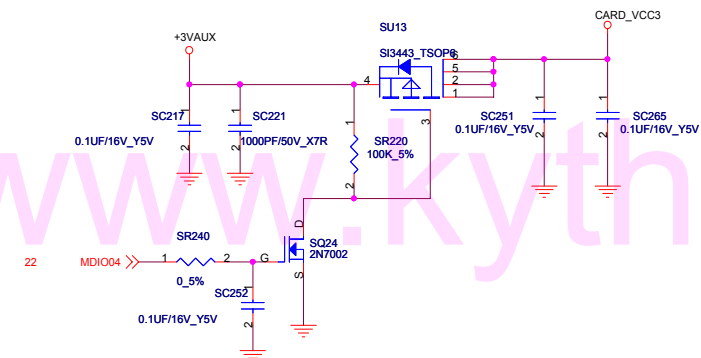
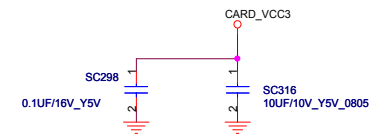
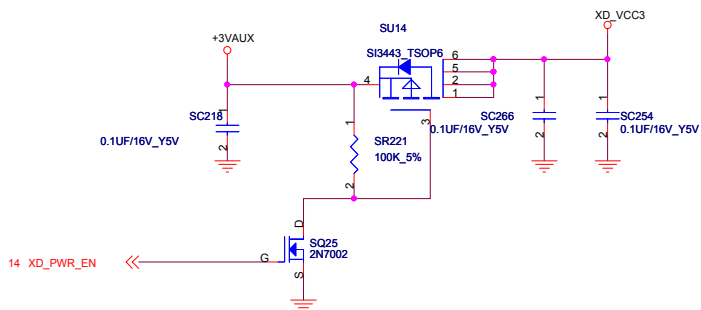
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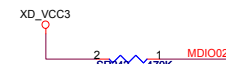








	MS	SD	XD	No card
MDIO00	HIGH	LOW	LOW	HIGH
MDIO01	LOW	HIGH	LOW	HIGH
XD_PWR_EN	LOW	LOW	HIGH	LOW
SD_WP	LOW	HIGH	LOW	LOW



Elitegroup Computer Systems

Card Reader Slot

File

Size

Custom

Document Number

400-1-4-01

Rev

A.0

Date:

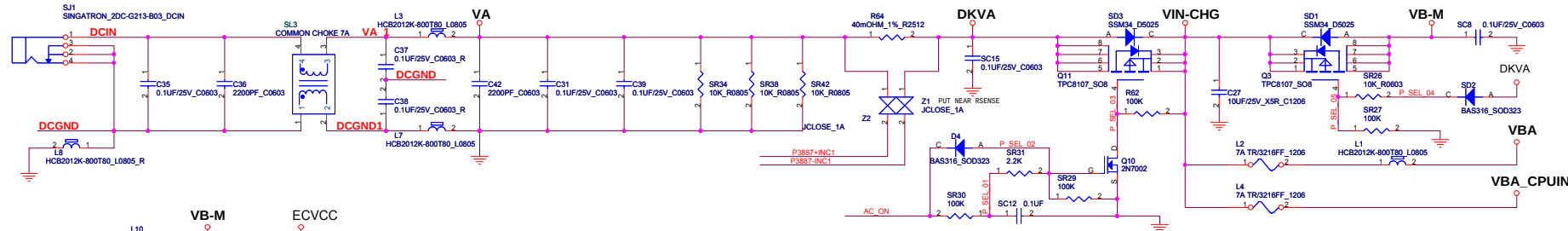
Monday, July 11, 2005

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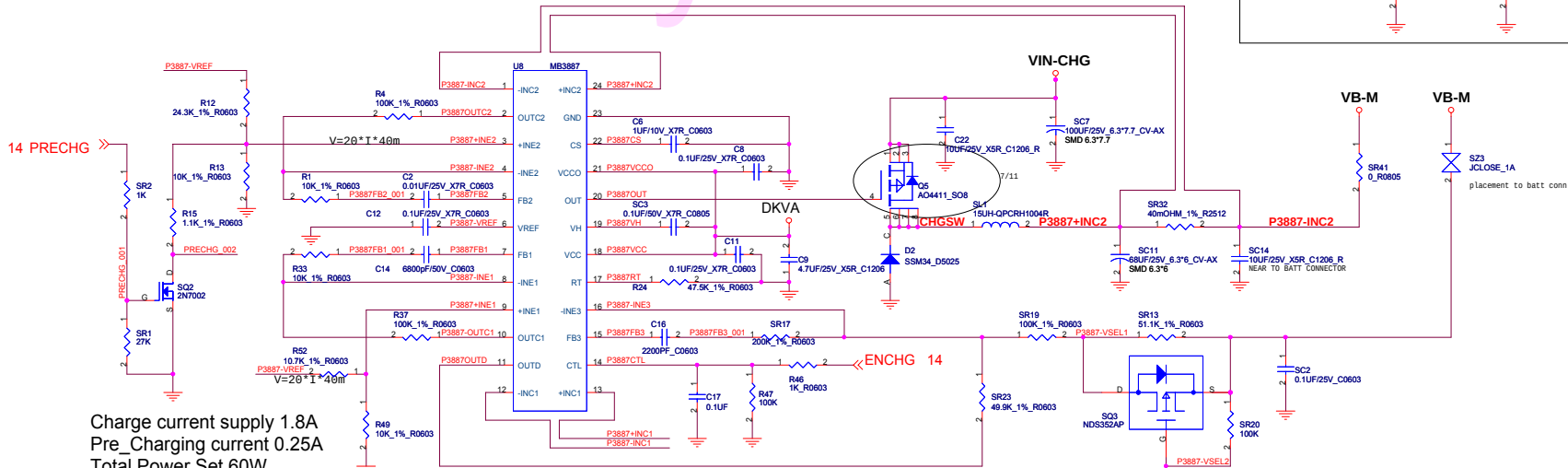
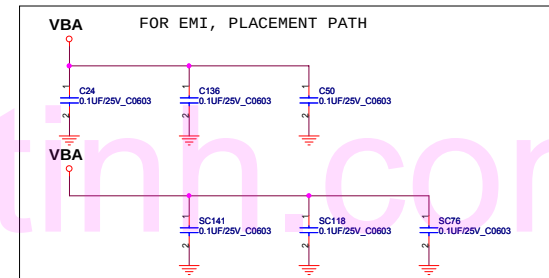
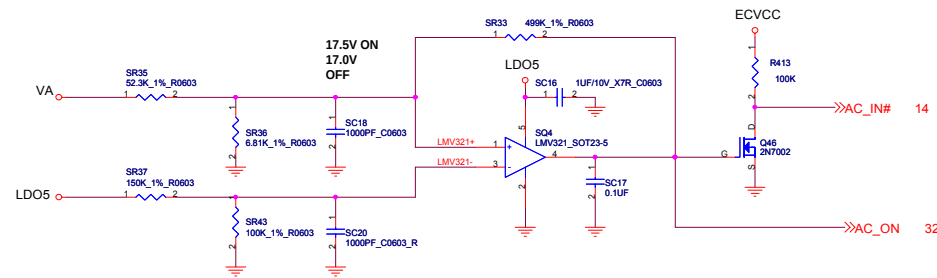
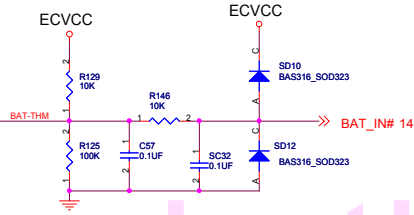
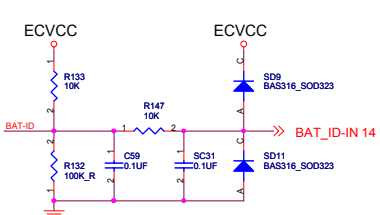
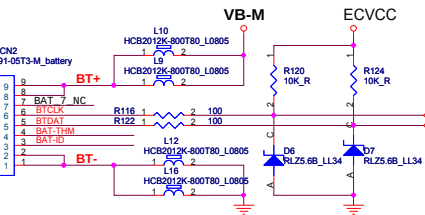
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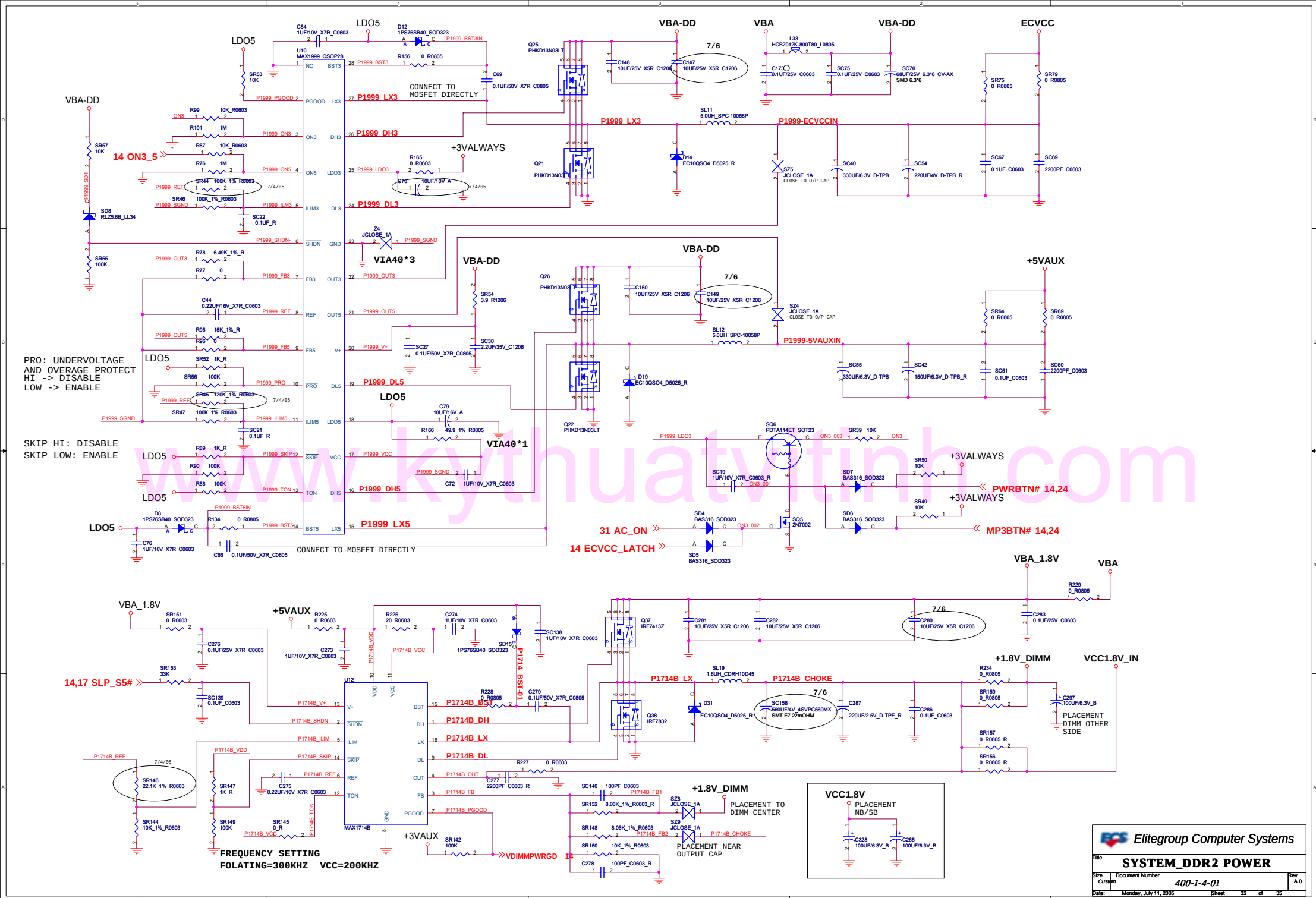
BAT-THM:
300 ohm: Battery present
Floating: No battery insert

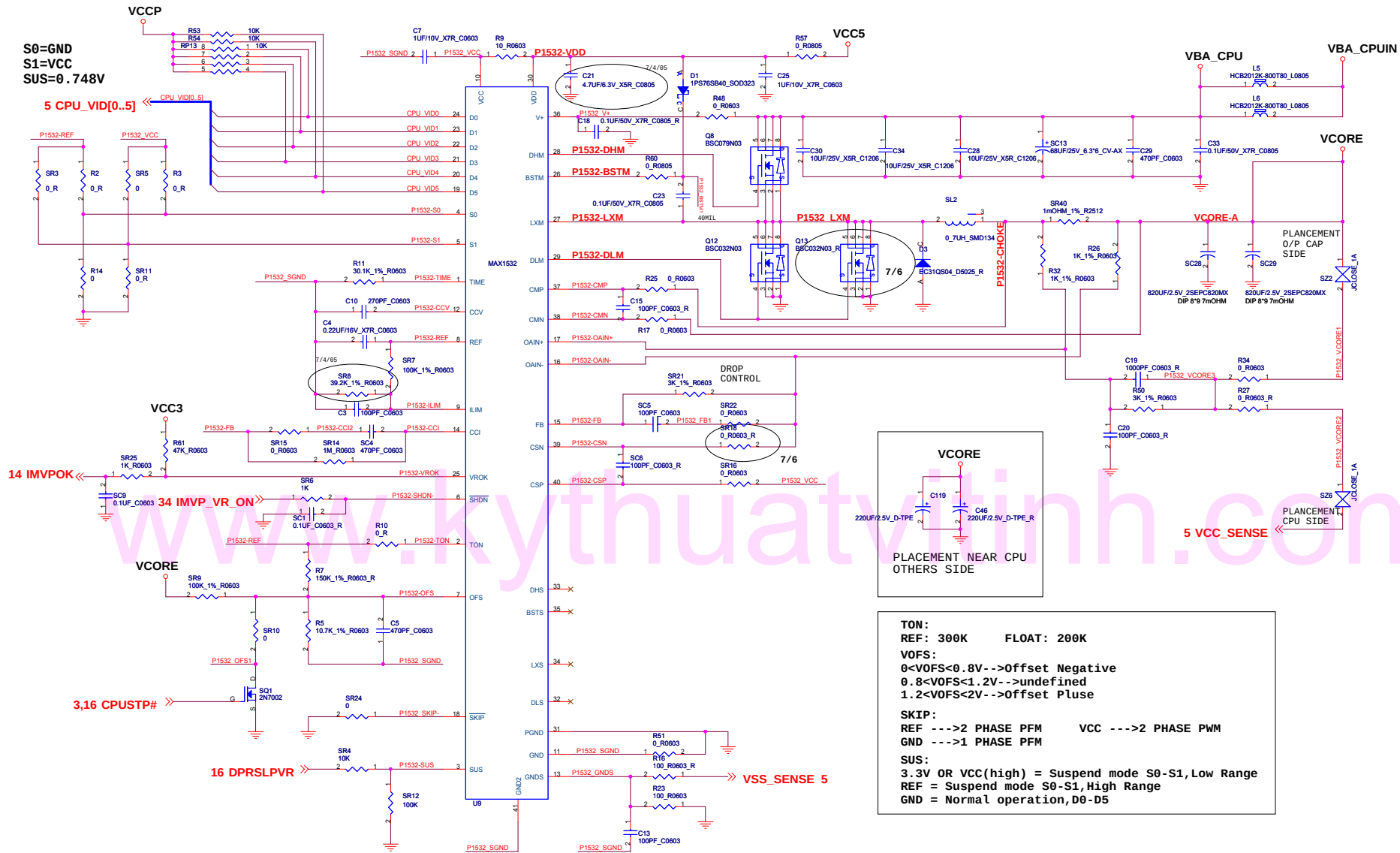
BAT-ID:
300 ohm: 4S2P 8 Cells
Floating: 3S2P 6 Cells



Charge current supply 1.8A
Pre-Charging current 0.25A
Total Power Set 60W

Battery 6Cell/12.6V &
4/8Cell/16.8V





V.A: 2005/07/11 Initial Release 15-F66-010010

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Title		
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