

EA40-CX UMA/Muxless Schematics Document Ivy Bridge Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

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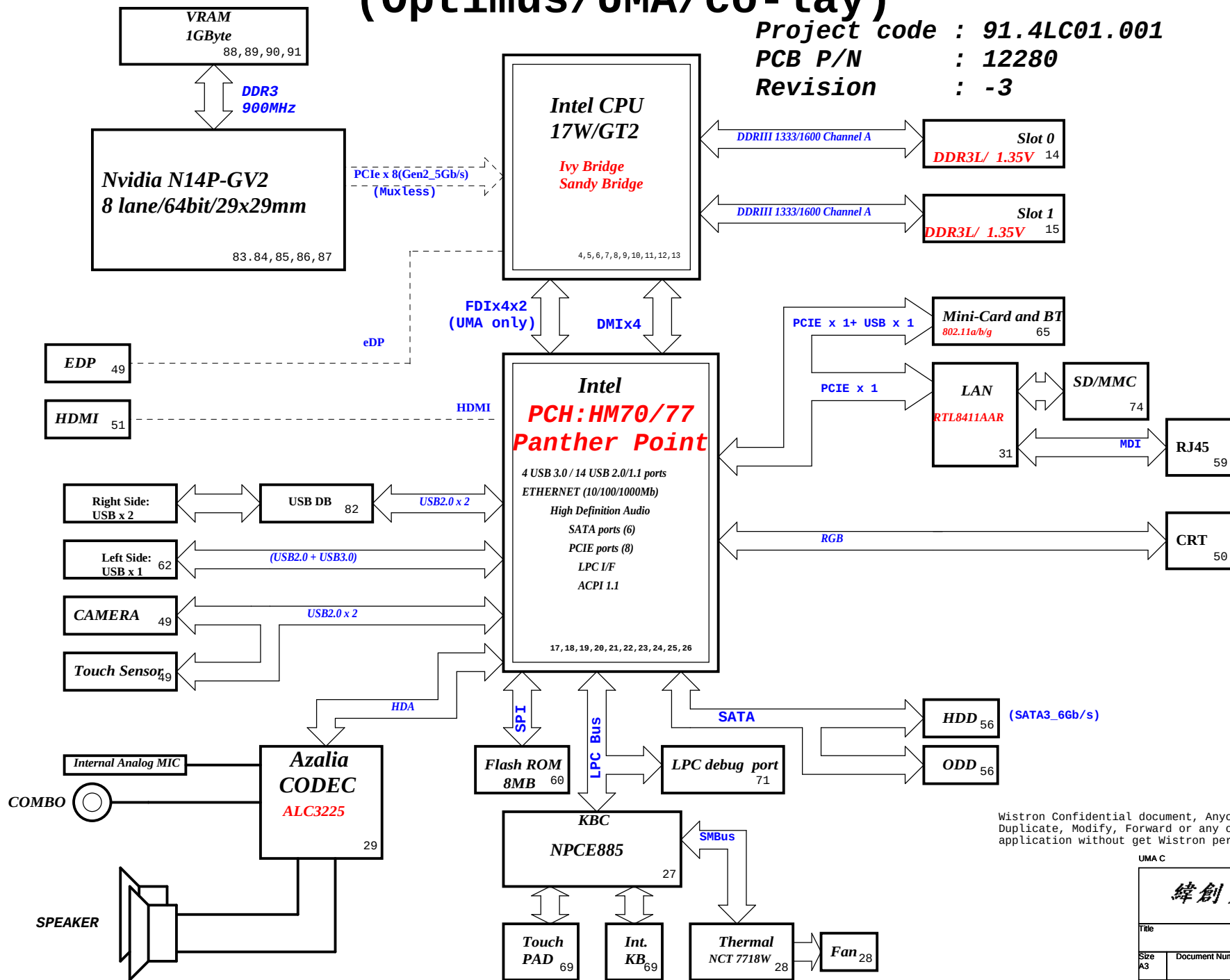
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Title			
Cover Page			
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EA40_CX Block Diagram (Optimus/UMA/co-lay)

Project code : 91.4LC01.001

PCB P/N : 12280

Revision : -3



CHARGER BQ24727		40
INPUTS	OUTPUTS	
DCBATOUT	BT+	
SYSTEM DC/DC RT8223MGQW		41
INPUTS	OUTPUTS	
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5	
CPU DC/DC ISL95833HRTZ		42~43
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
SYSTEM DC/DC ISL95833HRTZ		44
INPUTS	OUTPUTS	
DCBATOUT	VCC_GFXCORE	
SYSTEM DC/DC SY8208D		45
INPUTS	OUTPUTS	
DCBATOUT	1D05V_VTT	
SYSTEM DC/DC RT8207L		46
INPUTS	OUTPUTS	
DCBATOUT	1D35V_S3 0D675V_S0 DDR_VREF_S3	
LDO RT9025-25ZSP		47
INPUTS	OUTPUTS	
3D3V_S0 3D3V_S0	1D8V_S0 1D5V_S0	
LDO G978		48
INPUTS	OUTPUTS	
1D05_VTT	0D05V_S0	
VGA ISL62882CHRTZ		92
INPUTS	OUTPUTS	
DCBATOUT	VGA_CORE	
SY8208D/TPS22966D		93
INPUTS	OUTPUTS	
DCBATOUT	1D5V_VGA_S0	
3D3V_S0 1D05V_VTT	3D3V_VGA_S0 1D05V_VGA_S0	
PCB LAYER		
L1:Top		L4:Signal
L2:VCC		L5:GND
L3:Signal		L6:Bottom

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PCB Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SD0	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

USB Table

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	N/A
2	N/A
3	N/A
4	ODD
5	ESATA

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA / USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

A

B

C

D

E

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to Embedded DisplayPort. Enabled - An external Display Port device is connect to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	ALL S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I ² C / SMBus Addresses		Ref Des	HURON RIVER ORB
Device	Address	Hex	Bus
EC SMBus 1 Battery CHARGER			BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP			SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SD-DIMM(A) (SPD) SD-DIMM(B) (SPD) Digital Pot G-Sensor MINI			PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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EA40 CX

Rev

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Date: Thursday, June 06, 2013

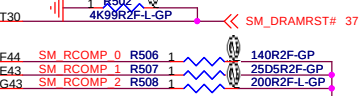
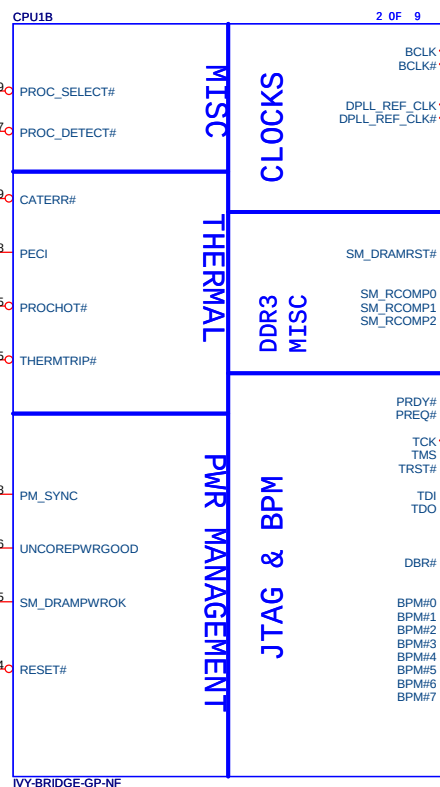
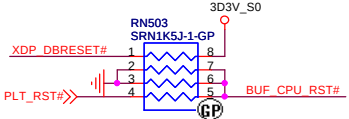
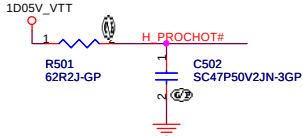
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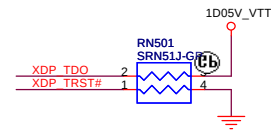
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SSID = CPU



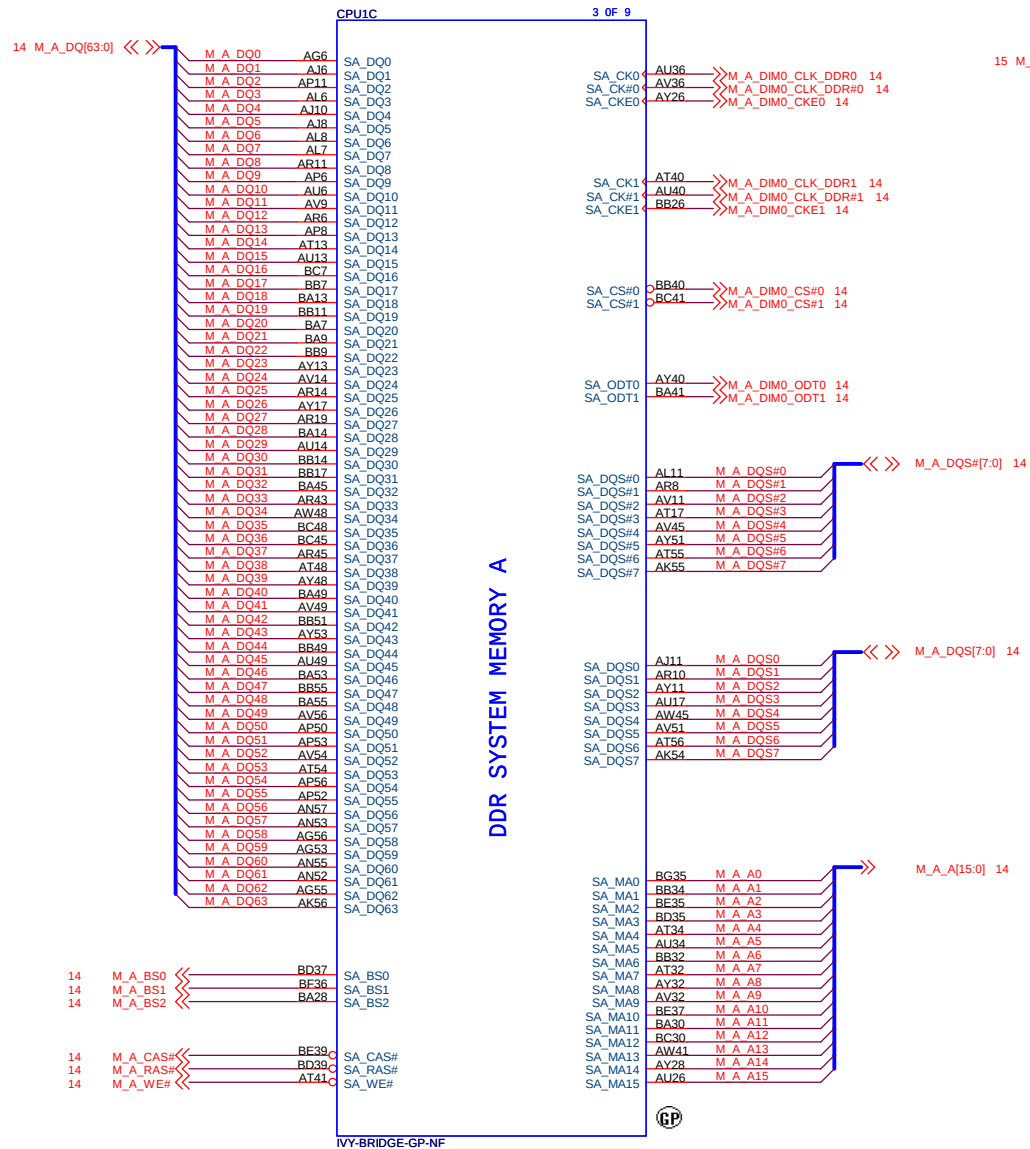
Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.



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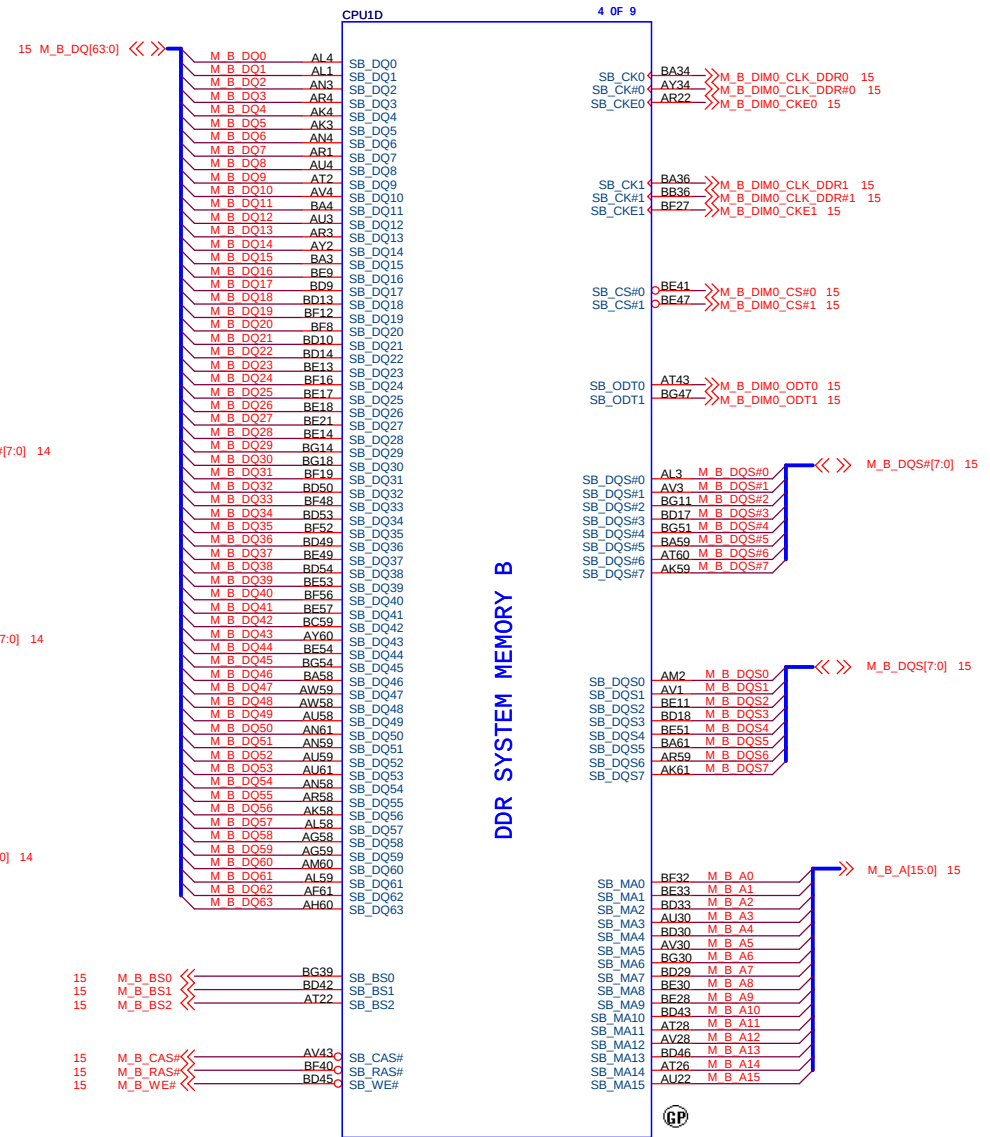
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Title CPU (THERMAL/CLOCK/PM)		
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SSID = CPU



IVY-BRIDGE-GP-NF

71.00IVY.A0U



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Title

CPU (DDR)

Size

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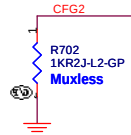
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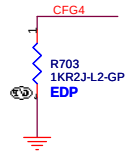
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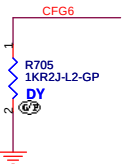
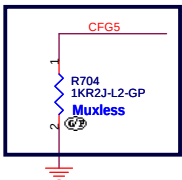
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



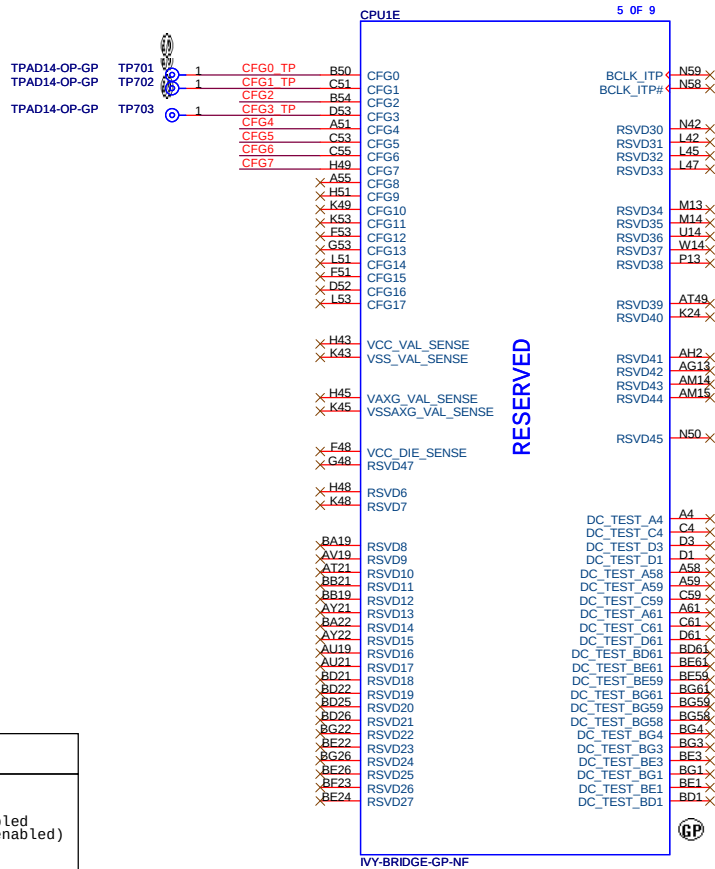
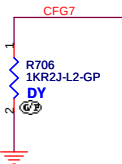
Enabl EDP function	
CFG4	1: Disable 0: Enable



PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



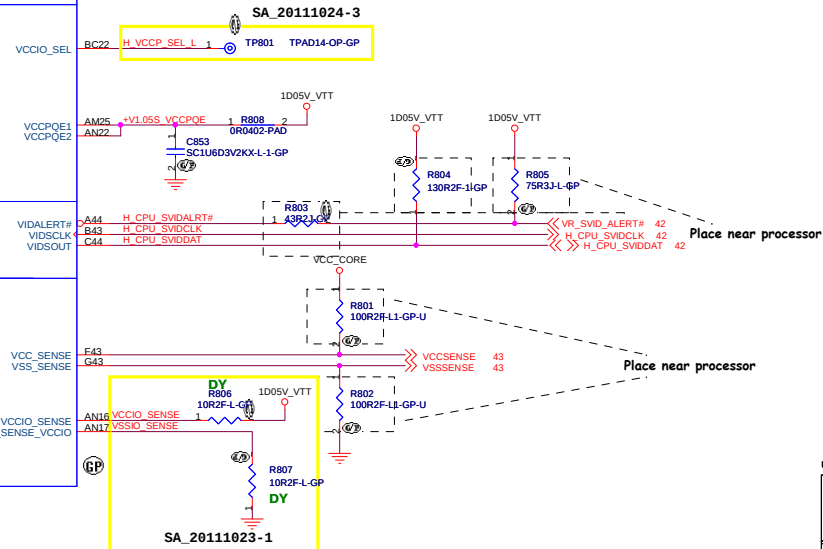
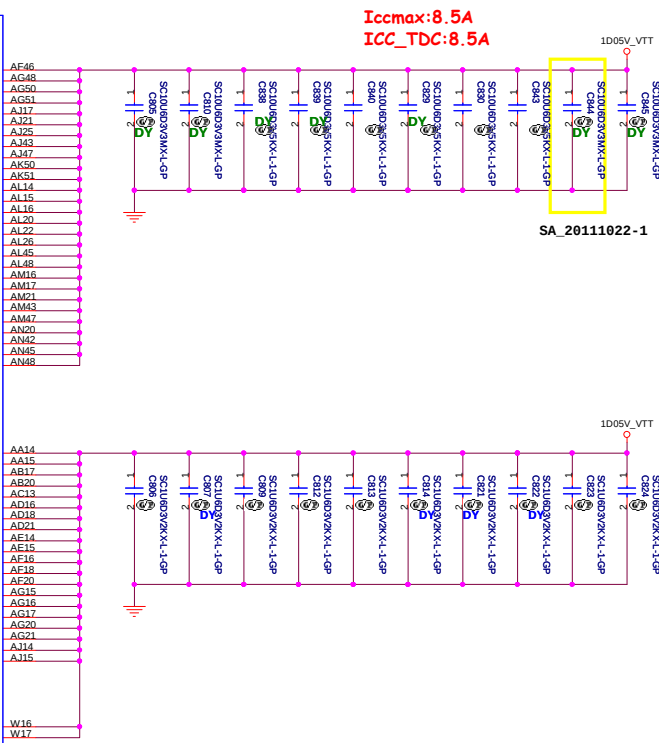
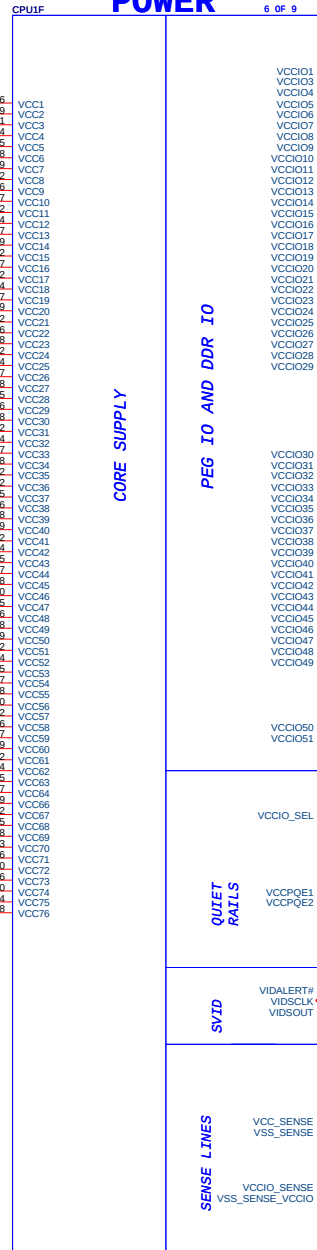
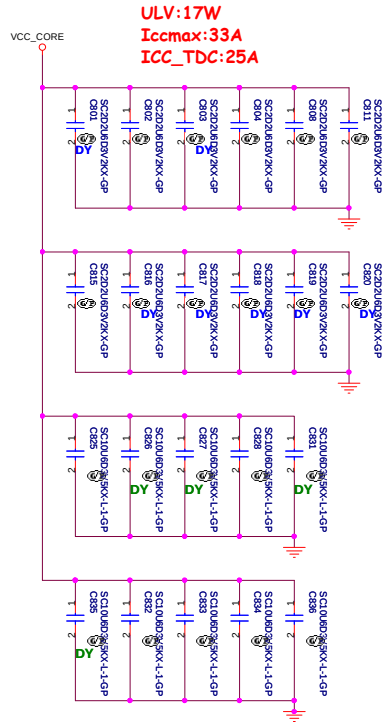
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CPU (RESERVED)		
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Title CPU (VCC CORE)

Size Custom

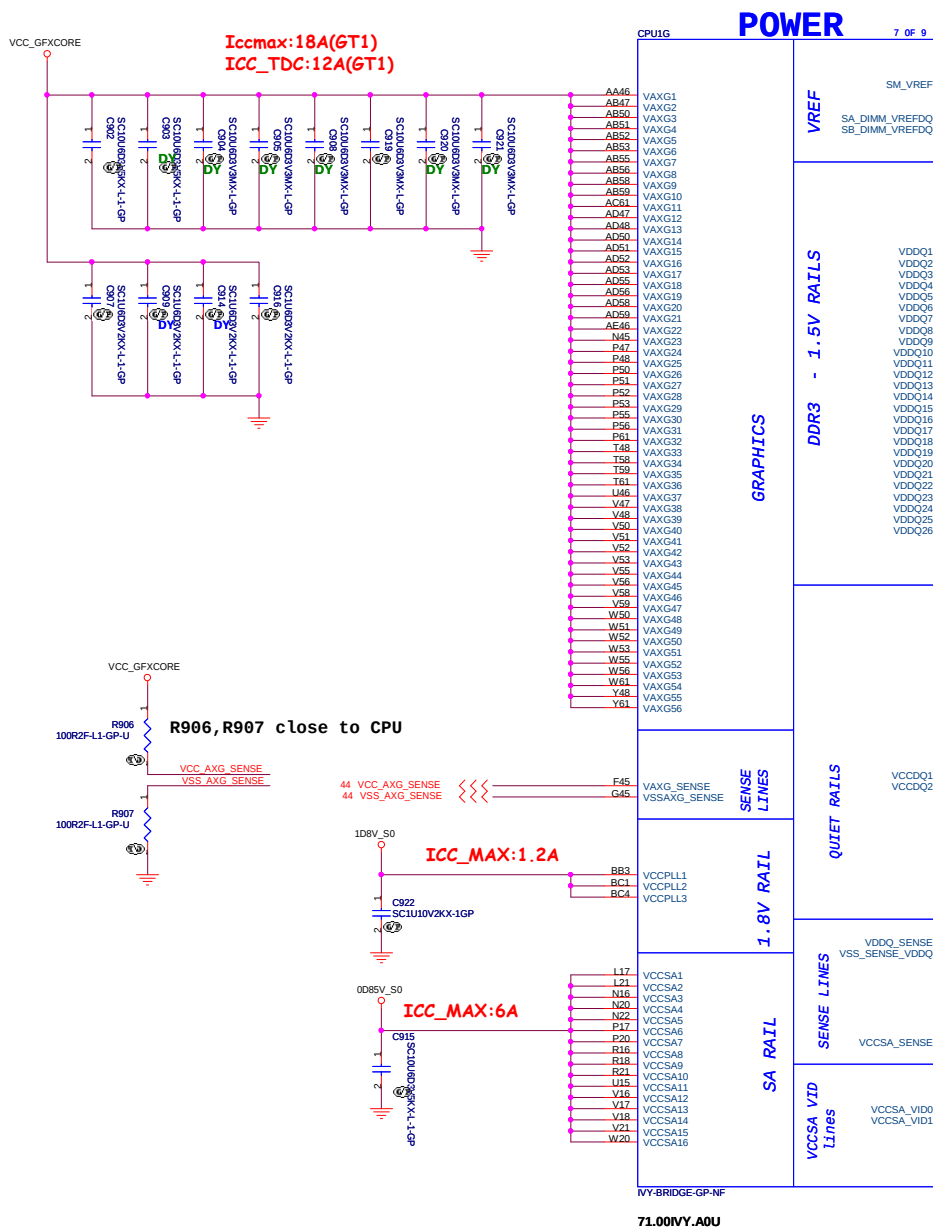
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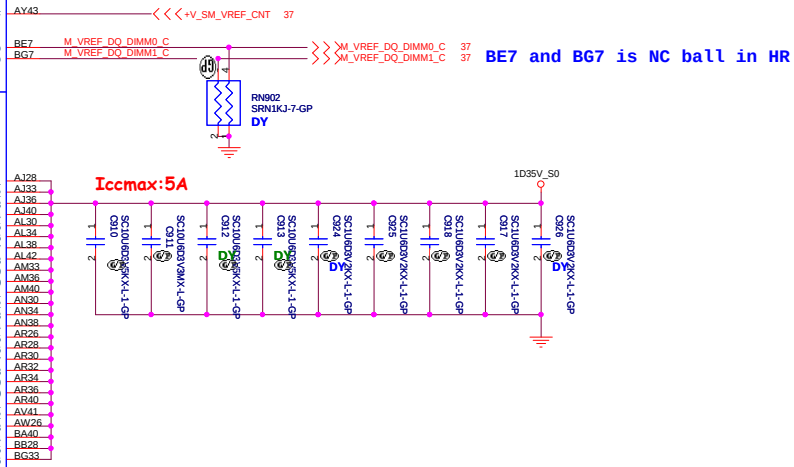
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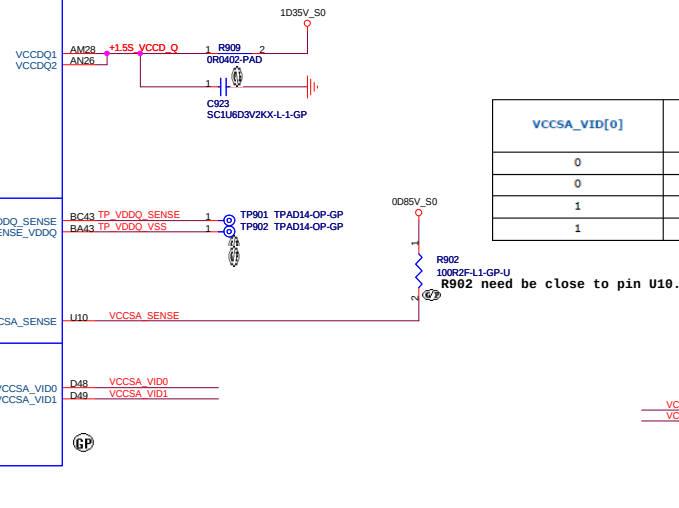
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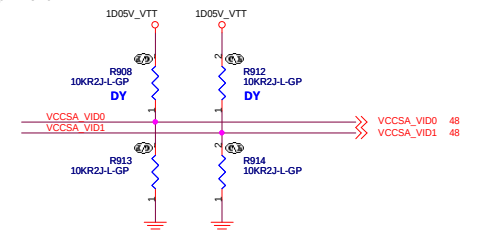
Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.



PROCESSOR DDR 1.5V QUIET RAIL (BGA only)
+V1.5S_VCCD_Q should be short to +V1.5S_VCCDDQ on board



VCCSA_VID[0]	VCCSA_VID[1]	Selected VCCSA (XE & SV segments)	Selected VCCSA (ULV segment)
0	0	0.9 V	0.9 V
0	1	0.8 V	0.85 V
1	0	0.725 V	0.775 V
1	1	0.675 V	0.75 V



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CPU (VCC_GFXCORE)

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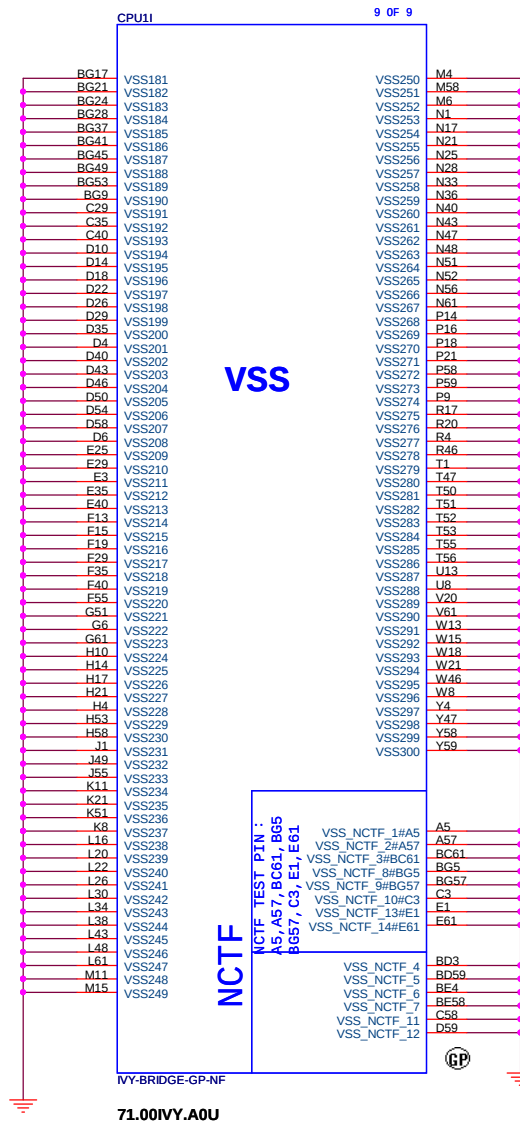
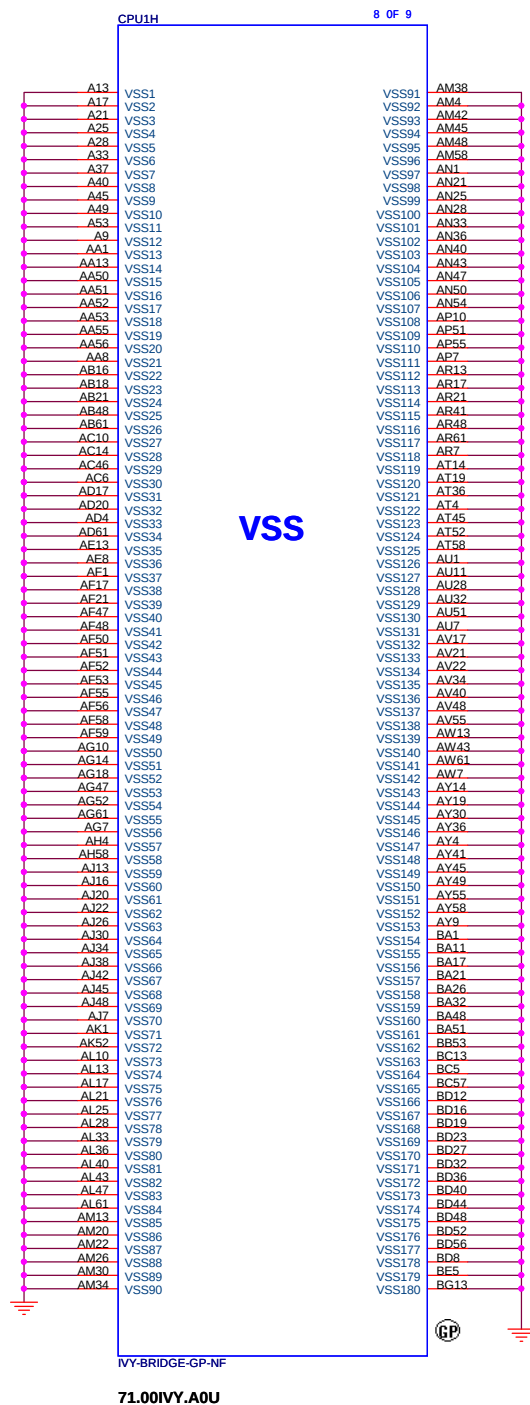
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SSID = CPU



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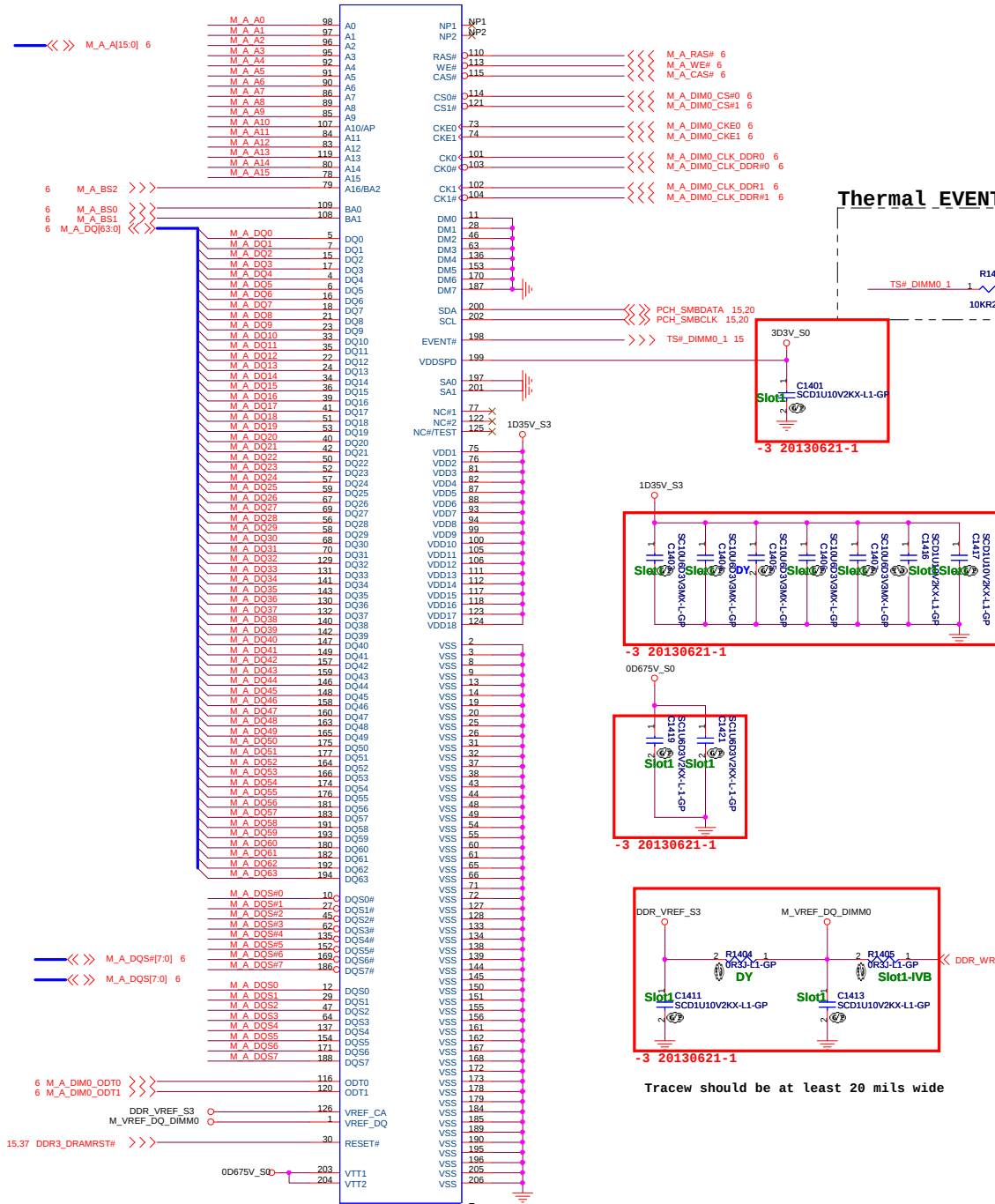
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SSID = MEMORY

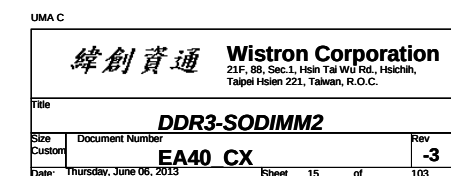


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DDR3-SODIMM1		
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		DM2
	M.B.A0	98
	M.B.A1	A0
	M.B.A2	A1
	M.B.A3	95
	M.B.A4	92
	M.B.A5	91
	M.B.A6	86
	M.B.A7	80
	M.B.A8	89
	M.B.A9	85
	M.B.A10	107
	M.B.A11	84
	M.B.A12	81
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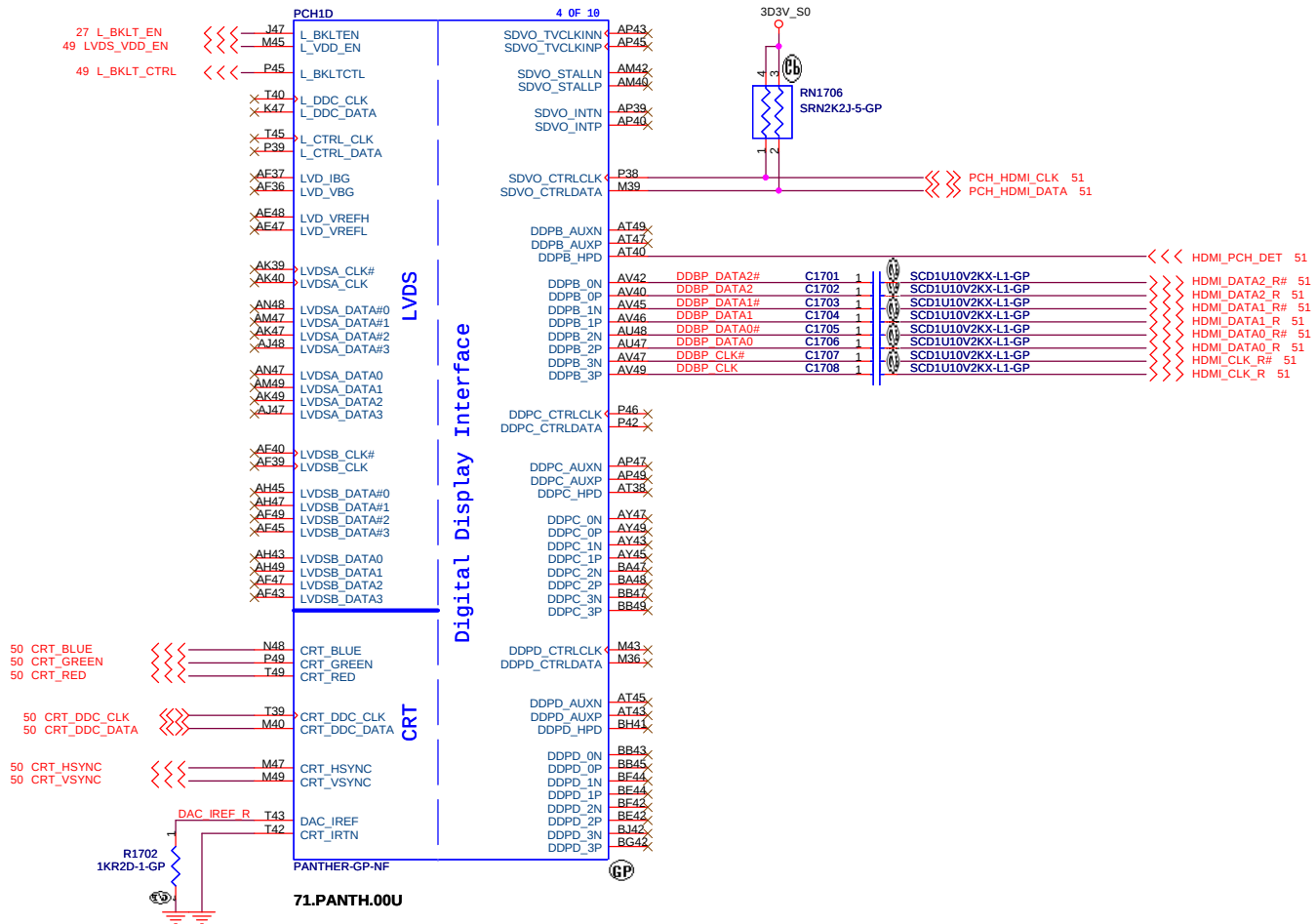
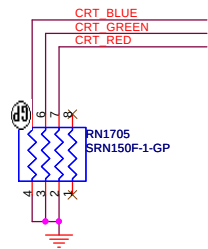
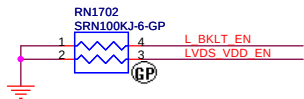


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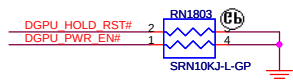
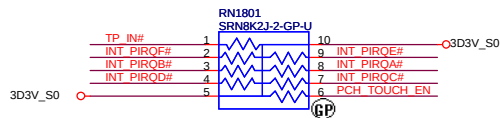
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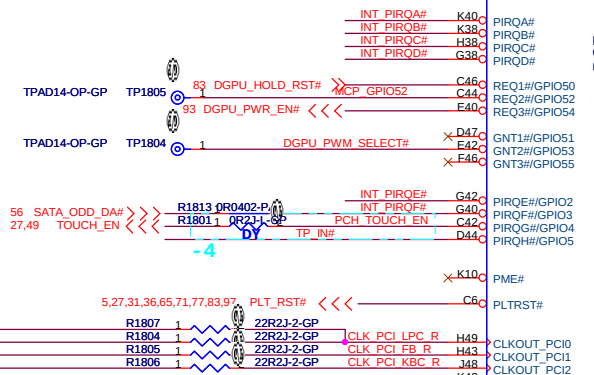


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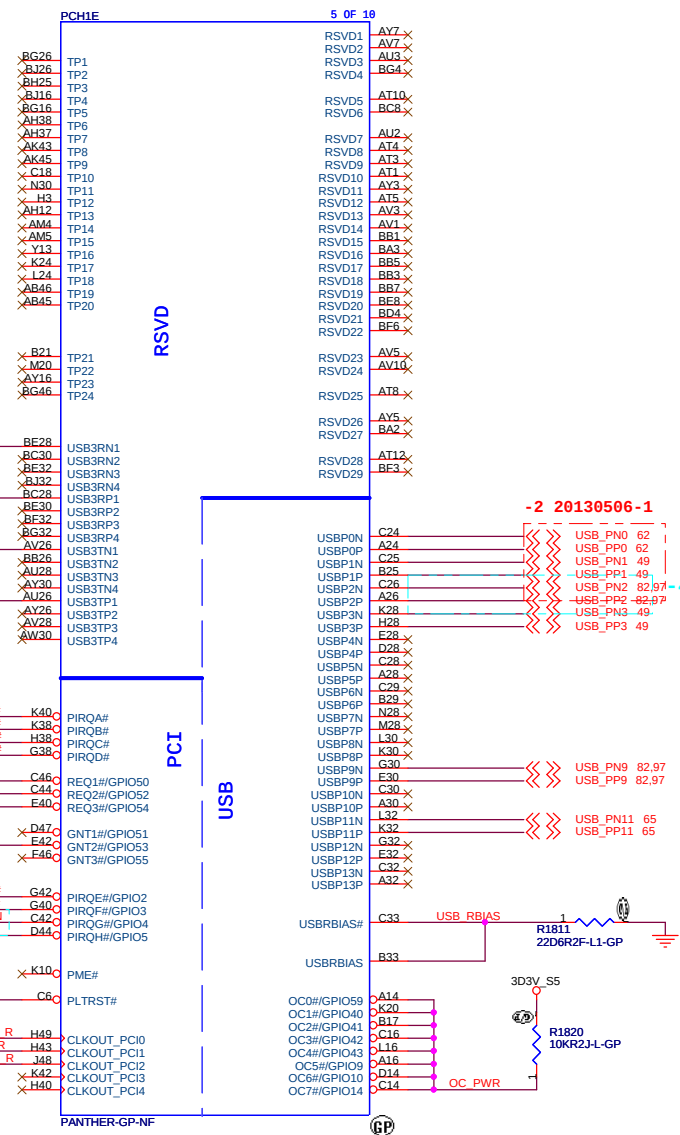
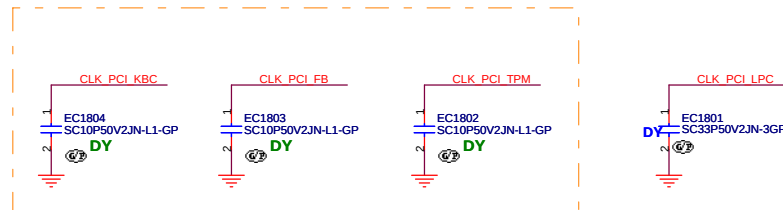
SSID = PCH



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



-1_20130315_EMI



USB Table

Pair	Device
0	USB2.0/USB3.0 Ext. port 1
1	Touch panel -3 20130606-1
2	USB2.0 Ext. port 1
3	CCD
4	
5	
6	may not be available
7	may not be available
8	
9	USB2.0 Ext. port 3
10	
11	Mini Card1 (WLAN+BT)
12	
13	

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Title	Author	Year	Journal	Volume	Page
1. The Effect of Temperature on the Rate of Reaction of Hydrogen Peroxide with Potassium Iodide	John Doe	2018	Journal of Chemical Education	95	1234
2. Synthesis and Characterization of a New Polymeric Material	Jane Smith	2019	Polymer Letters	15	5678
3. Kinetic Study of the Reaction Between Sulfuric Acid and Sodium Hydroxide	Michael Brown	2020	Chemical Kinetics	10	9101
4. Investigation of the Catalytic Activity of Various Metals in the Decomposition of Hydrogen Peroxide	Sarah White	2021	Catalysis Letters	20	2345
5. The Role of pH in the Stability of Aqueous Solutions of Various Salts	David Green	2022	Environmental Chemistry	12	6789

PCH (PCI/USB/NVRAM)

Size

Document Number

EA40 CX

Date:

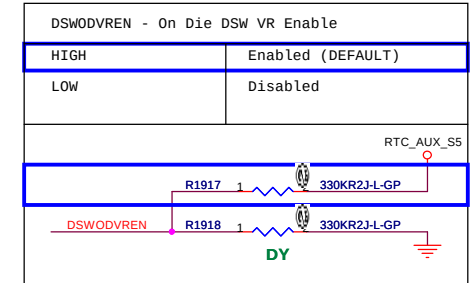
Friday, June 21, 2013

Sheet

Rev

-3

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and
routing length less than 500
mils.
DMI_IRCOMP keep W=4 mils and
routing length less than 500
mils.



3D3V_S5

R1901
SRN10KJ-6-GP

8 1 BATLOW#

7 2 PM R#

6 3 AC PRESENT

5 4 SUS_PWR_ACK_R

R1921 1
10KR2J-L-GP

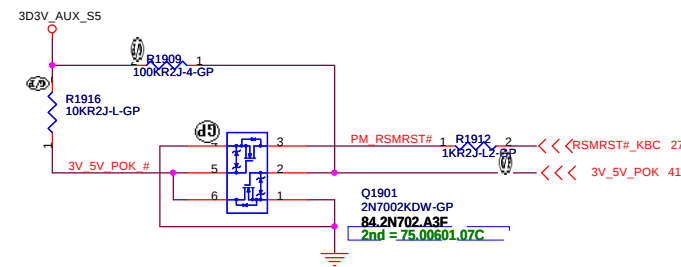
PCIE_WAKE#

R1922 1
10KR2J-L-GP

SUS_PWR_ACK#

R1908 1
100KR2J-4-GP

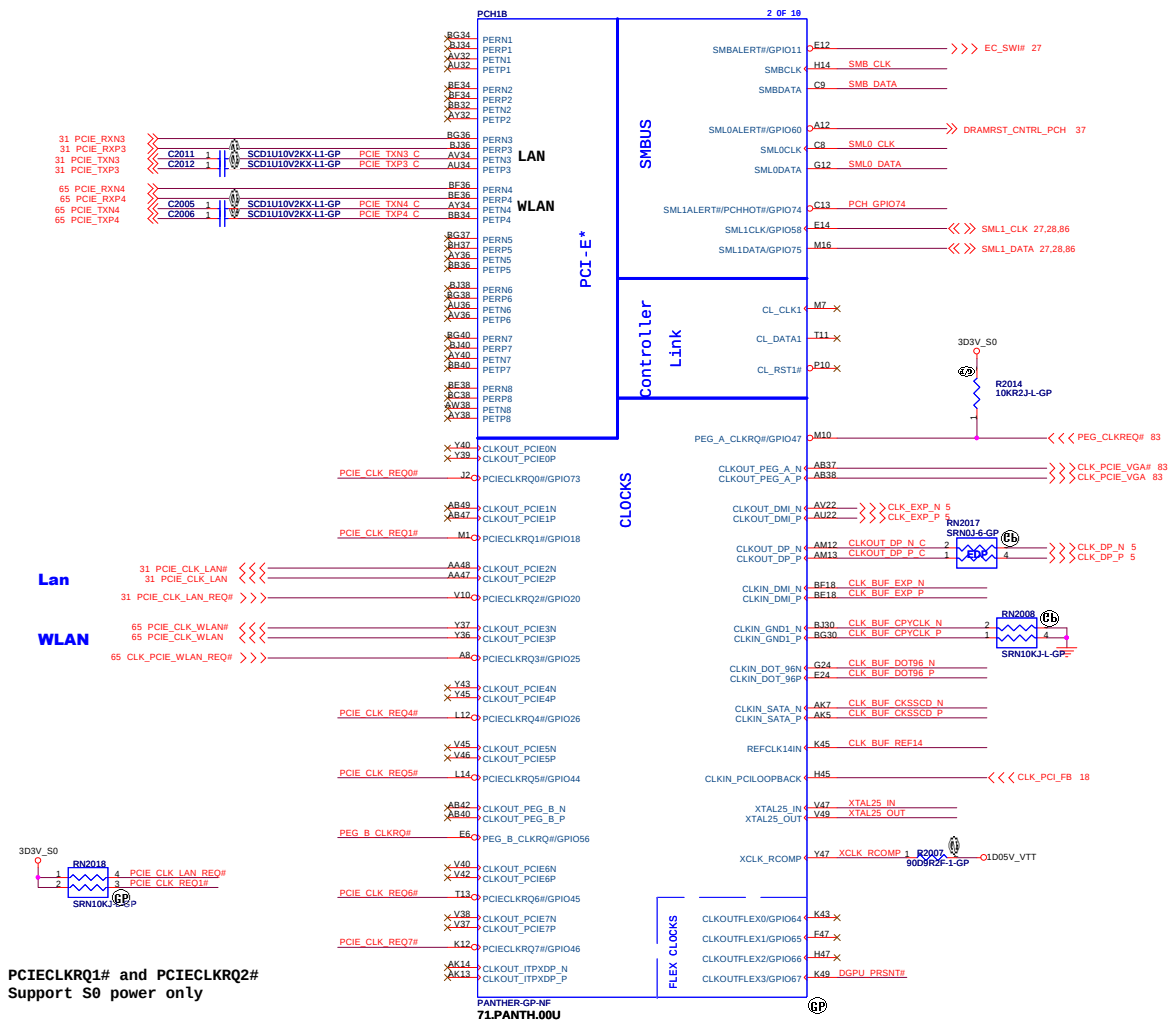
PM RSMRST#



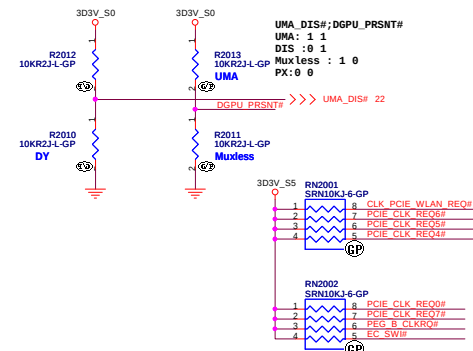
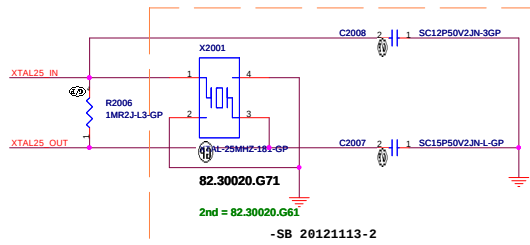
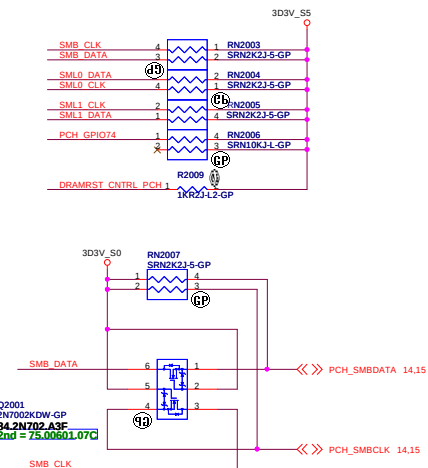
UMA C

Title			
PCH (DM I/FDI/PM)			
Size A3	Document Number	Rev	
	EA40 CX	-3	
Date:	Friday, June 21, 2013	Sheet	19 of 103

SSID = PCH

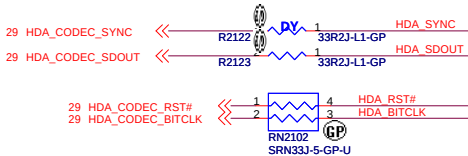
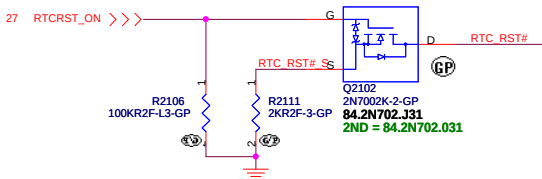
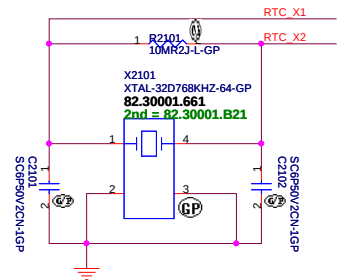


PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

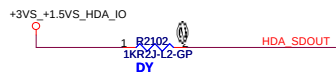


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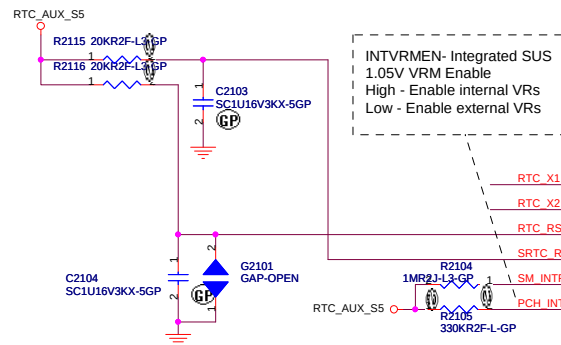
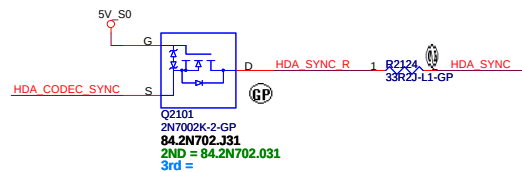
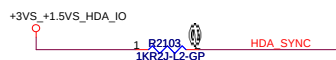
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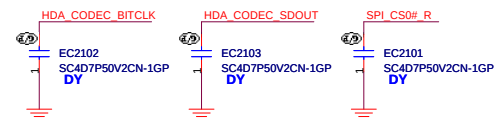
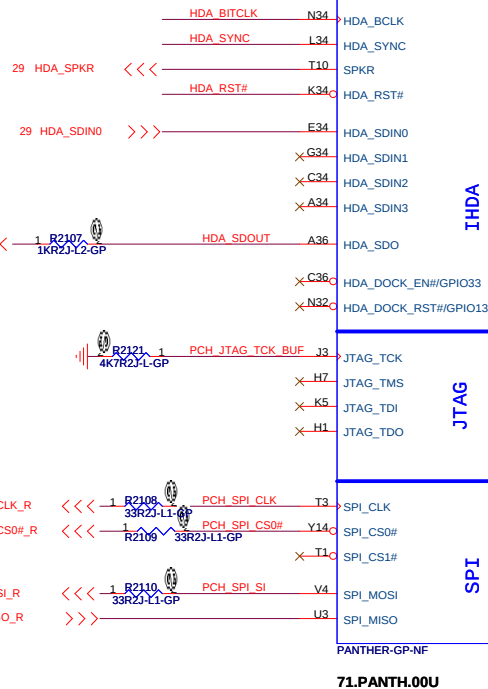
Flash Descriptor Security Override	
HDA_SDOUT	Low = Default High = Enable



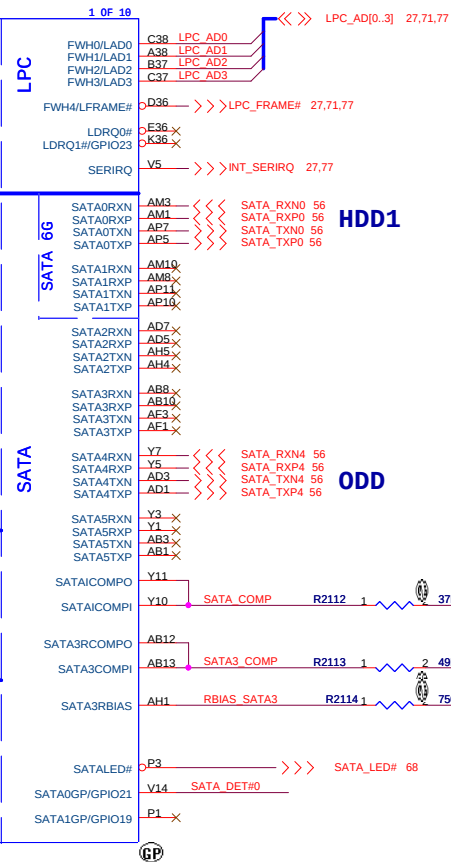
PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V



RTC Reset



HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVCRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.



HDD1

ODD

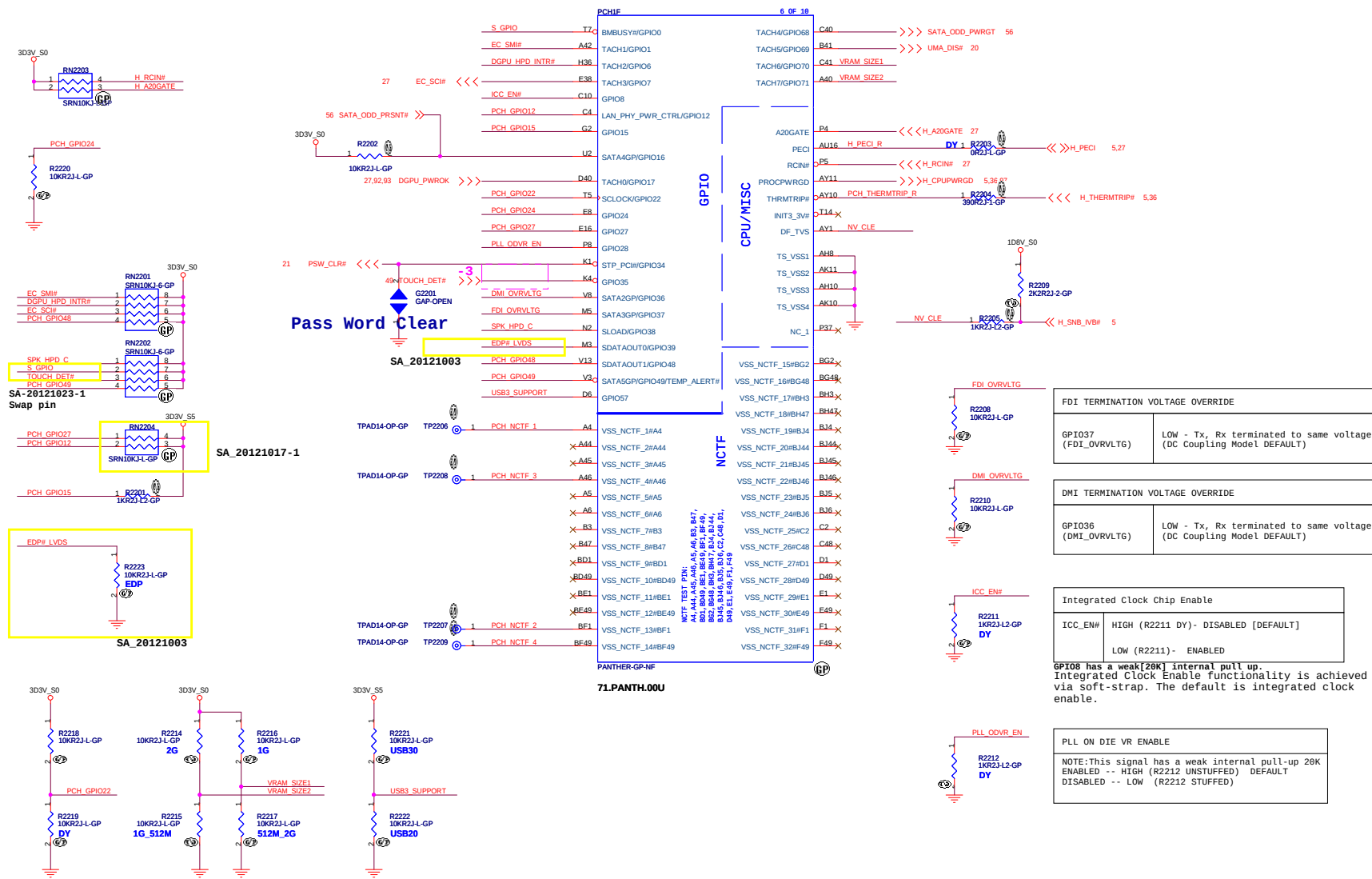


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Title			
PCH (SPI/RTC/LPC/SATA/IHDA)			
Size Custom	Document Number		Rev
	EA40 CX		-3
Date:	Thursday, June 20, 2013	Sheet 21 of	103



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Title			
PCH (GPIO/CPU)			
Size Custom	Document Number	Rev	
	EA40 CX	-3	
Date:	Thursday, June 20, 2013	Sheet 22 of	103

SSID = PCH

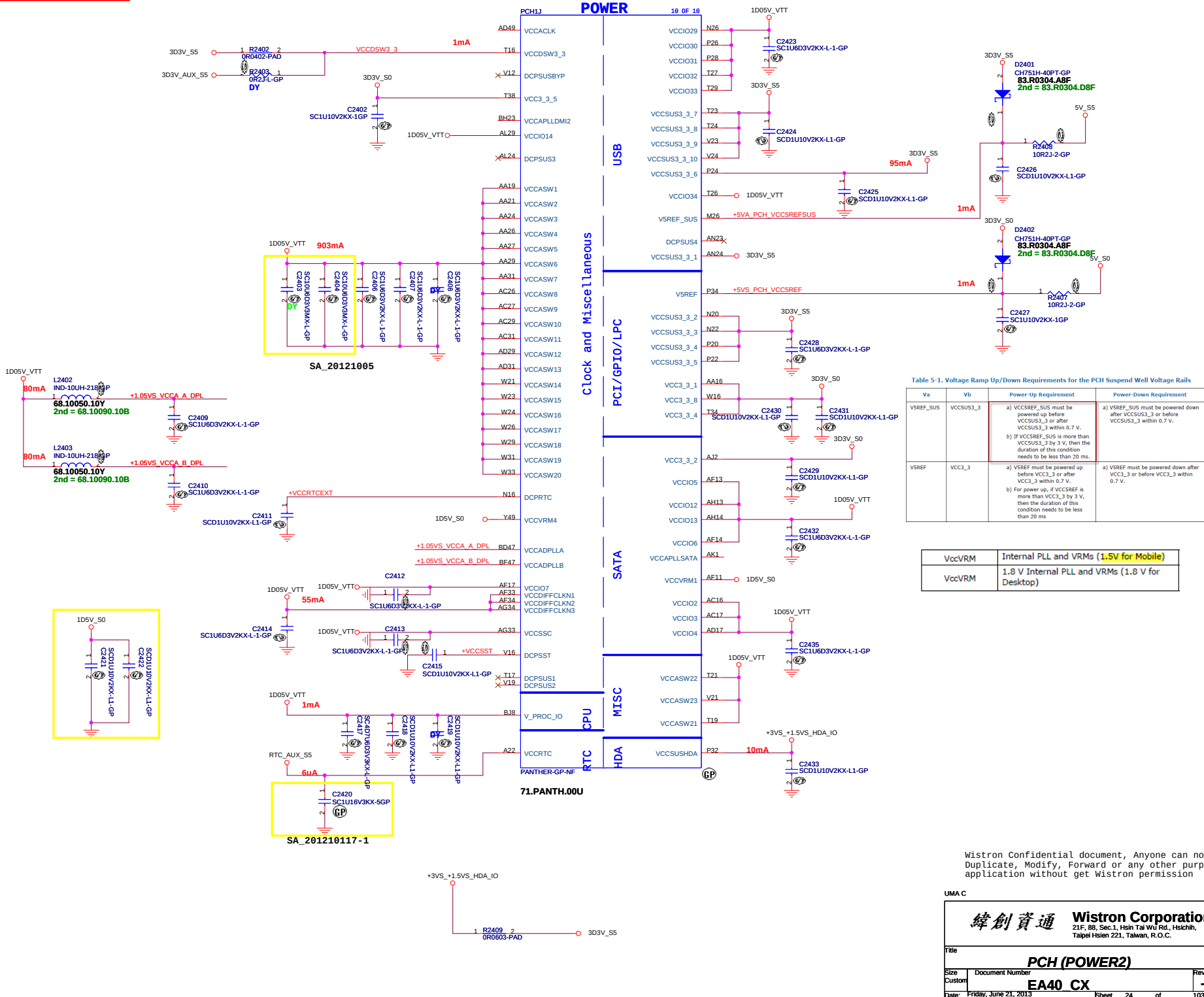


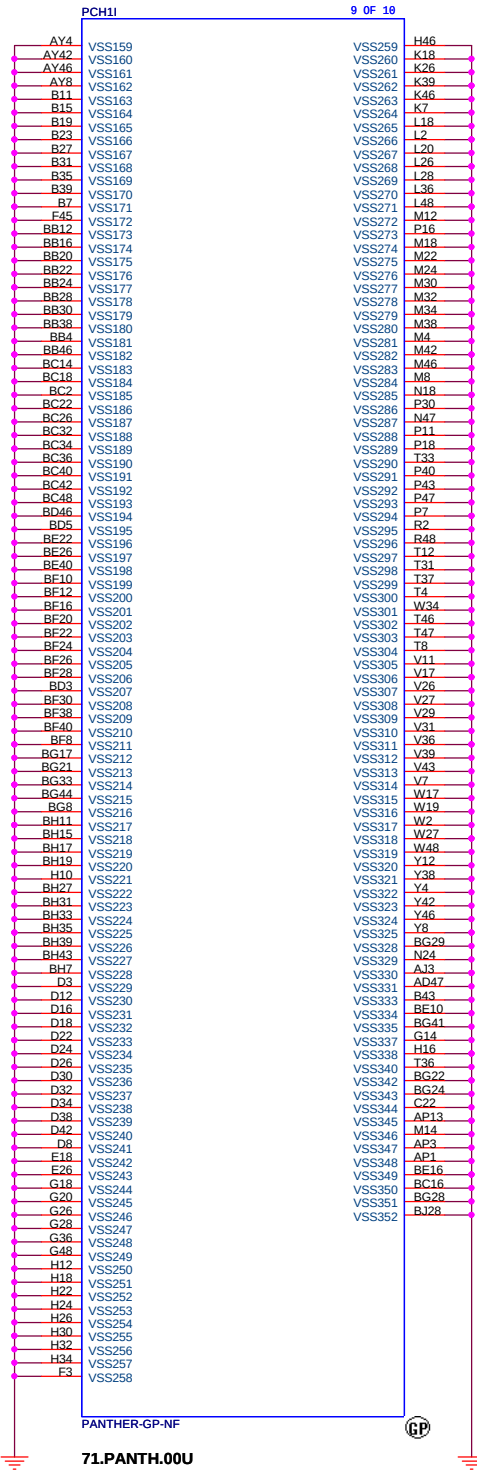
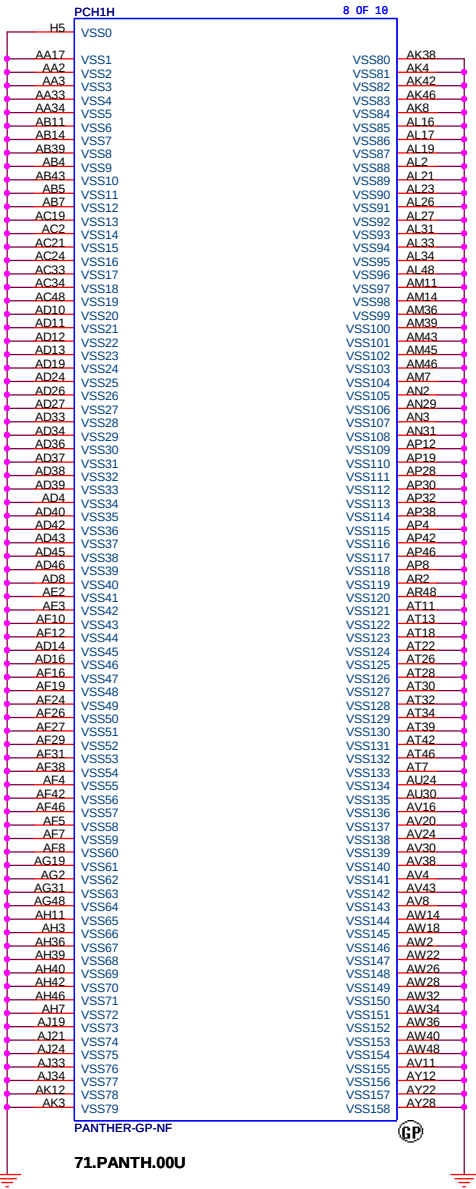
Table 5-1. Voltage Ramp Up/Down Requirements for the PCH Suspend Well Voltage Rail

Va	Vi	Power-Up Requirement	Power-Down Requirement
VSREF_SUS	VCCSUS3_3	a) VSREFRES_SUS must be powered up before VCCSUS3_3 or after VCCSUS3_3 within 0.7 V. b) If VSREFRES_SUS is more than VCCSUS3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) VSREFRES_SUS must be powered down after VCCSUS3_3 or before VCCSUS3_3 within 0.7 V.
VSREF	VCC3_3	a) VSREF must be powered up before VCC3_3 or after VCC3_3 within 0.7 V. b) For power up, if VSREFRES is more than VCC3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) VSREF must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)

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SSID = PCH



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Title **PCH (VSS)**

Size A3 Document Number **EA40 CX** Rev **-3**

Date: Thursday, June 06, 2013 Sheet 25 of 103

5	4	3	2	1
D				D
C				C
B				B
A				A

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Title Clock(colay)		
Size A4	Document Number EA40 CX	Rev -3
Date: Thursday, June 06, 2013		Sheet 26 of 103

Thermal sensor NCT 7718W

ev

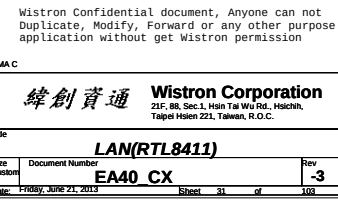
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C				
B				
A				

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Title			
Audio AMP			
Size	Document Number		Rev
A3	EA40 CX		-3
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1



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D				D
C				C
B				B
A				A
5	4	3	2	1

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Title	
RTS5159 (CARD READER)	
Size Custom	Document Number
	EA40 CX
Date: Thursday, June 06, 2013	Rev -3
Sheet 32 of 103	

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Title Reserved		
Size A4	Document Number EA40 CX	Rev -3
Date: Thursday, June 06, 2013		Sheet 33 of 103

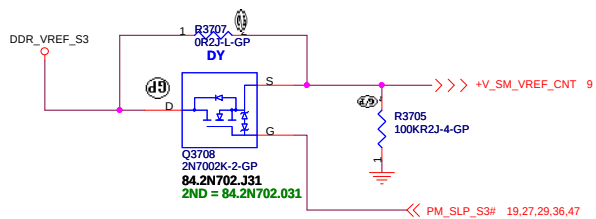
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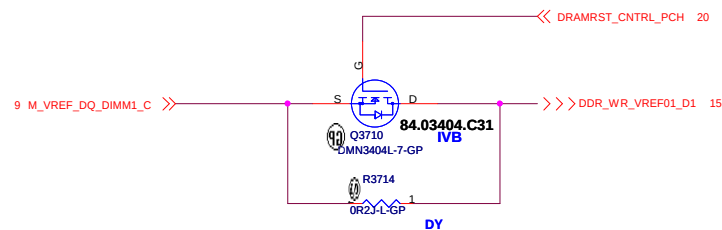
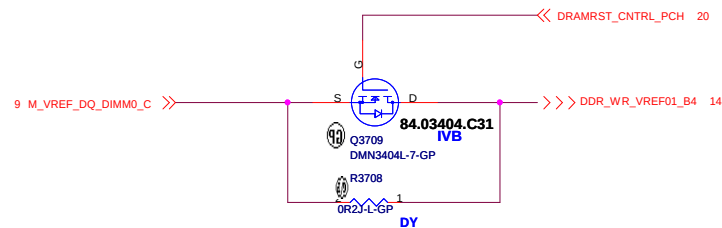
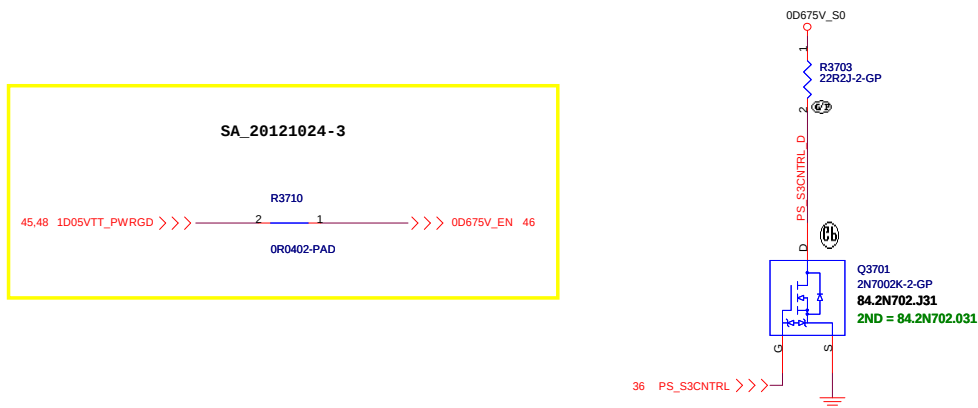
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Title Reserved		
Size A4	Document Number EA40 CX	Rev -3
Date: Thursday, June 06, 2013		Sheet 34 of 103

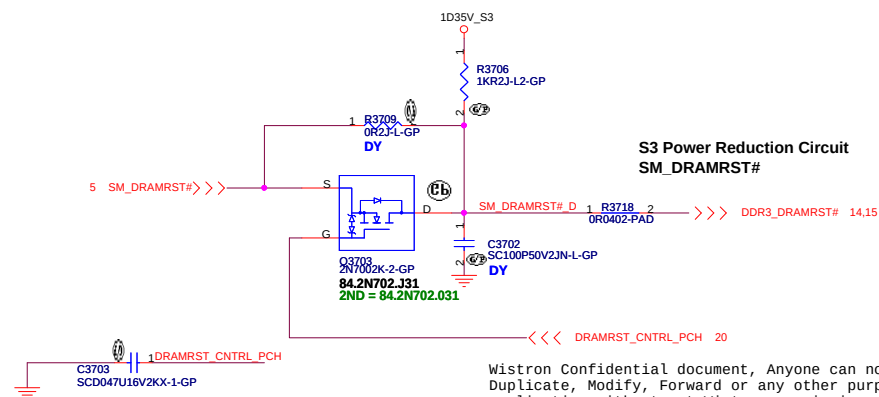
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

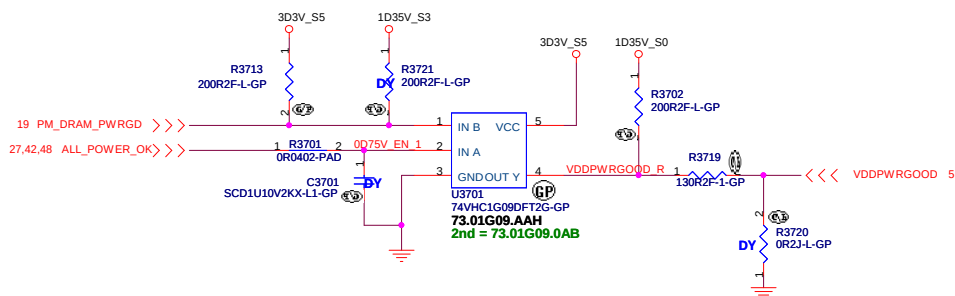


Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



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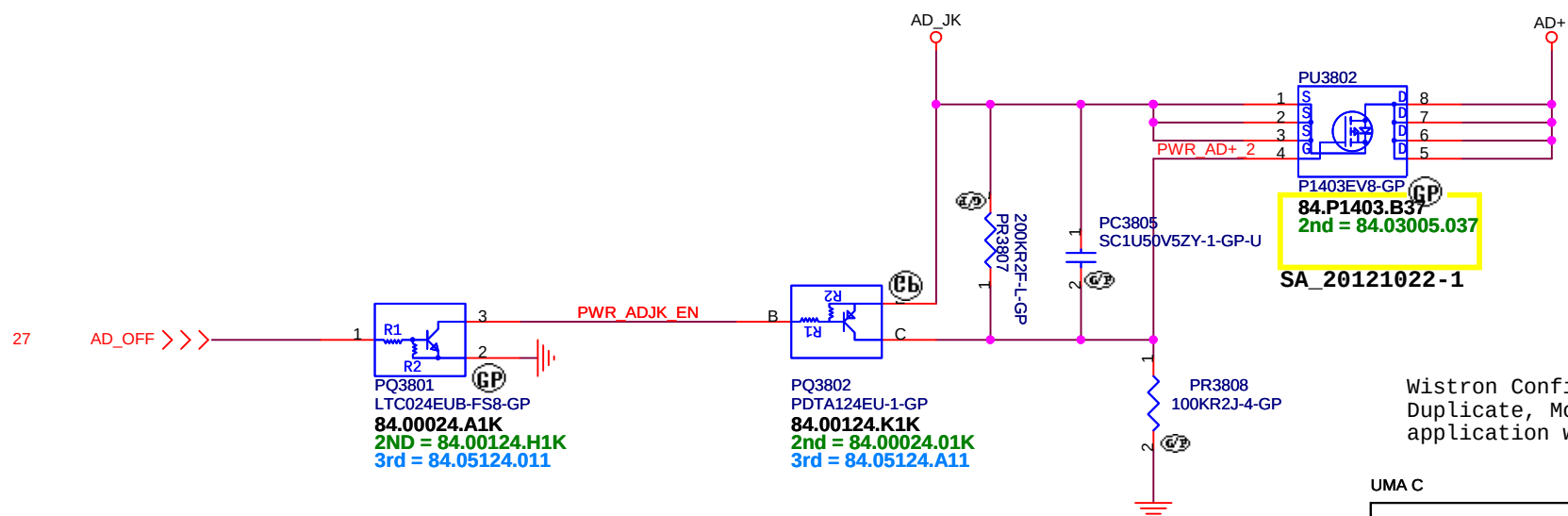
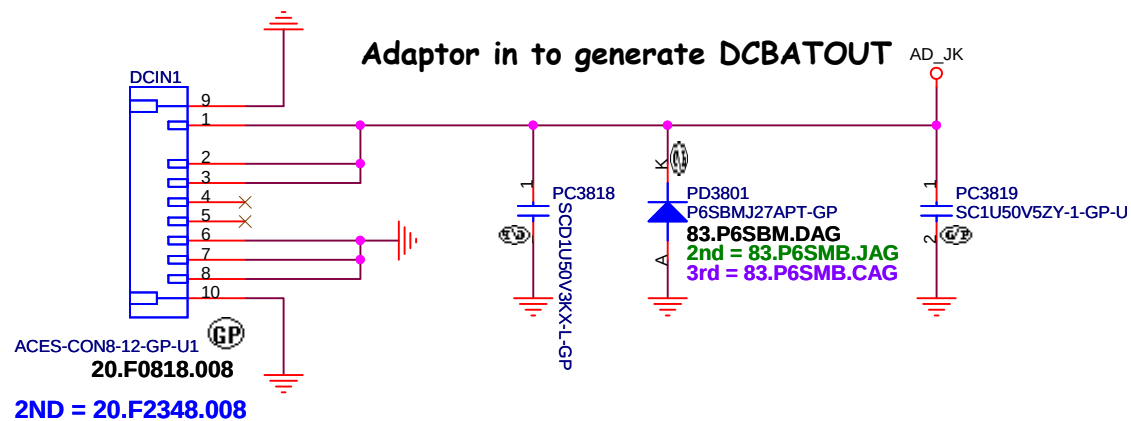
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



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Title		
ADAPTER		
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Title

DCIN JACK

Size
A4

Document Number

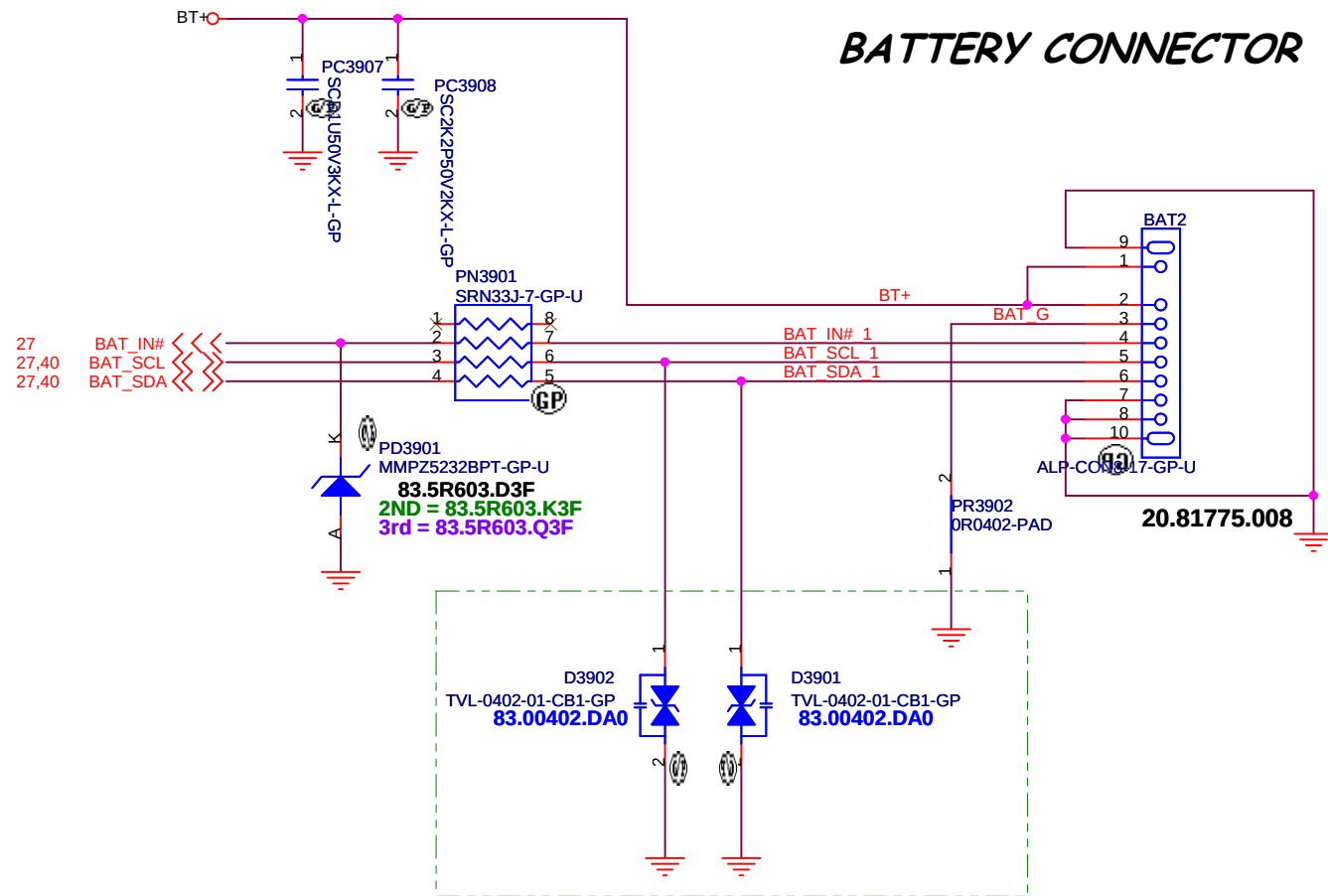
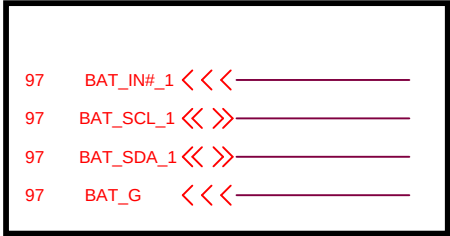
EA40 CX

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BATTERY CONNECTOR



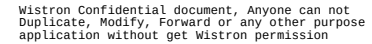
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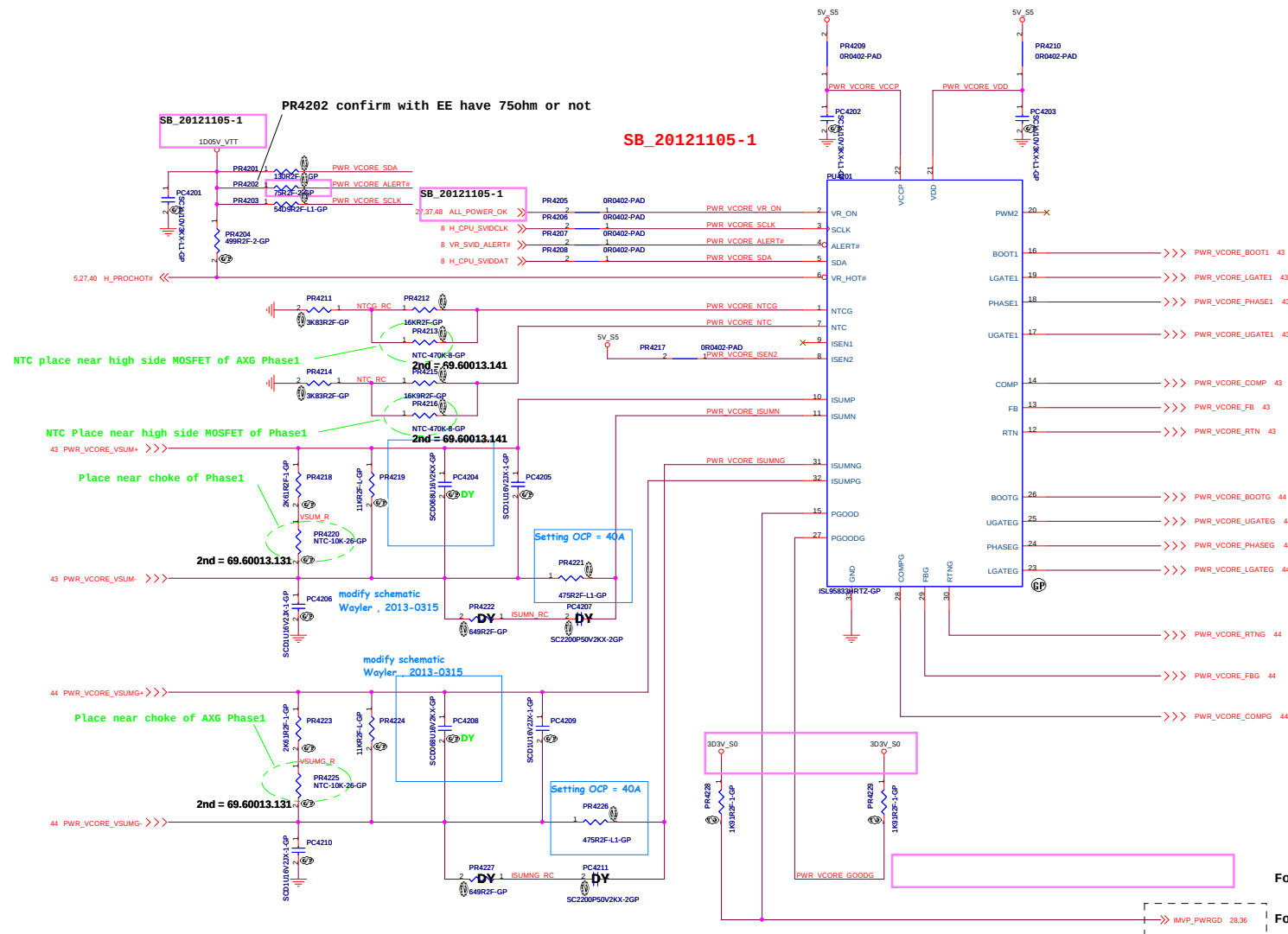
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Title		
BATT CONN		
Size	Document Number	Rev
A4	EA40 CX	-3
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3 (ANNIE/ASTRO)
R4014, PR4016



SSID = CPU.Regulator

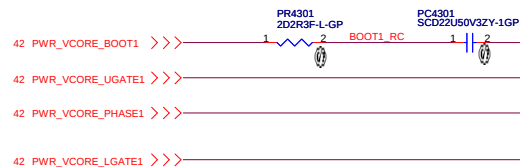
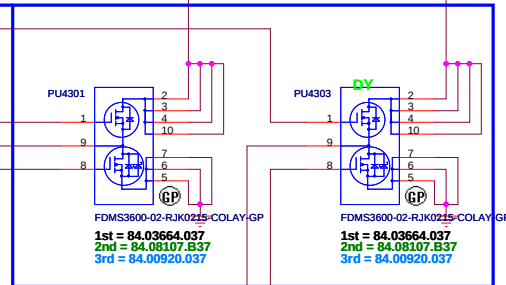


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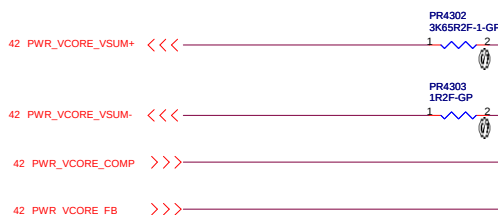
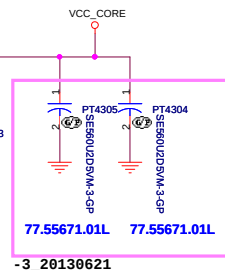
BOM control

	Main source	2nd source
PU4301	84.03664.037 (FDMS3664S)	Mount
PU4302	84.03664.037 (FDMS3664S)	DY

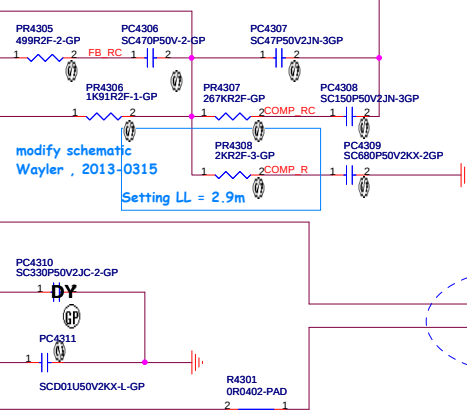
BOM control



Pana . 10 x 10 x 4
DCR 1.1 mOhm
Isat : 24A

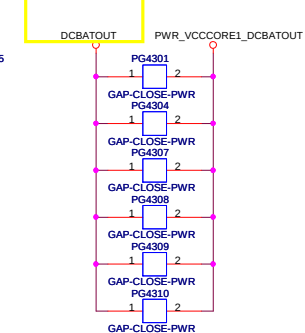


Parallel



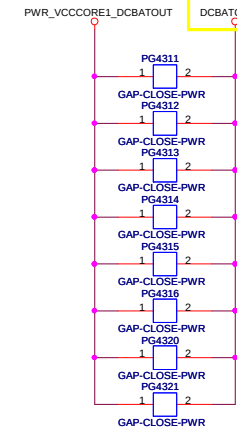
Parallel

SA_20121019



SC_20130206

SA_20121019



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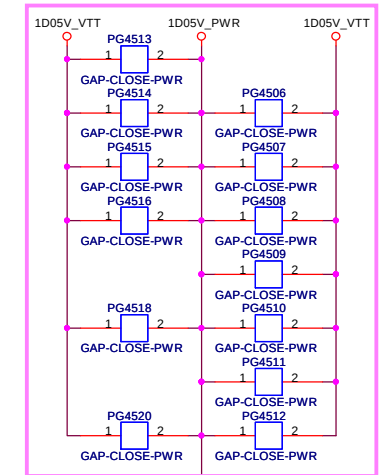
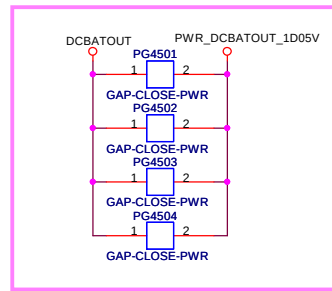
UMA C

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Title ISL95833_CPU_CORE(2/3)		
Size	Document Number	Rev
Custom	EA40 CX	-3
Date: Friday, June 21, 2013	Sheet 43	of 103

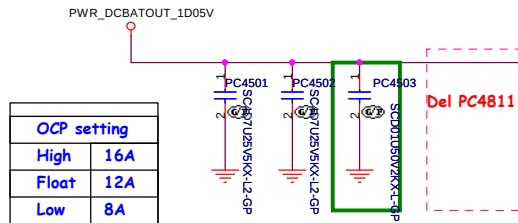
SY8208D for 1D05V

SB_20121105-1

SB_20121105-1

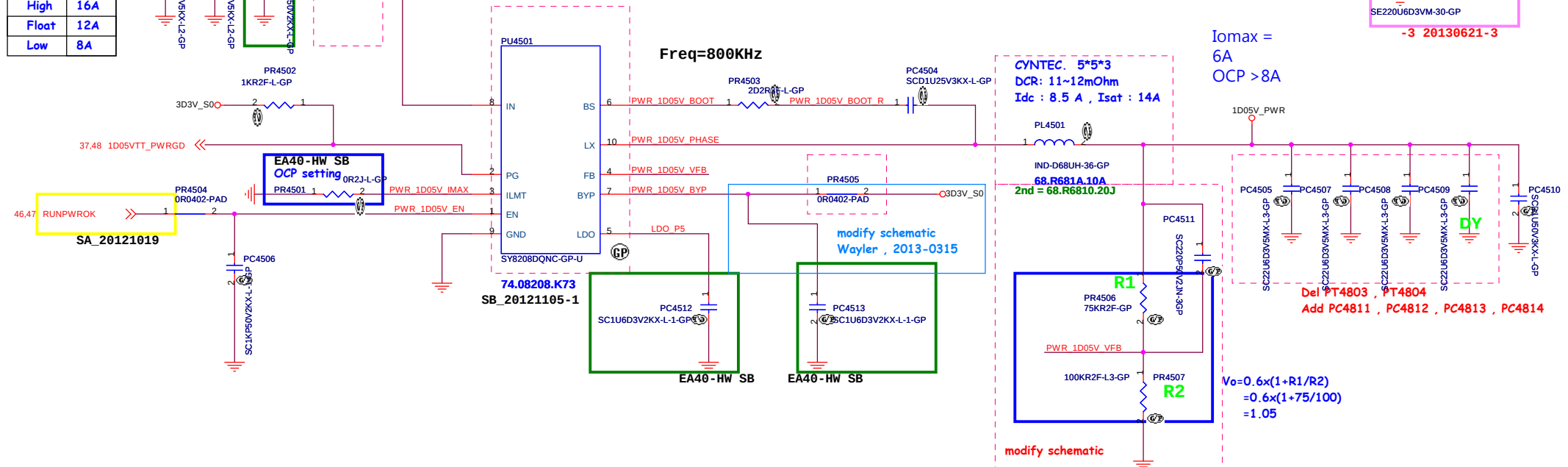


PT4501
DY
2ND = 77.52271.09L
3rd = 77.52271.12L
SE220U6D3VM-30-GP
-3 20130621-3



OCP setting	
High	16A
Float	12A
Low	8A

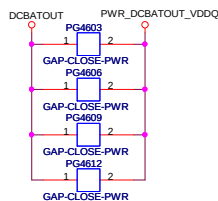
Change to SY8208D SA_20121019



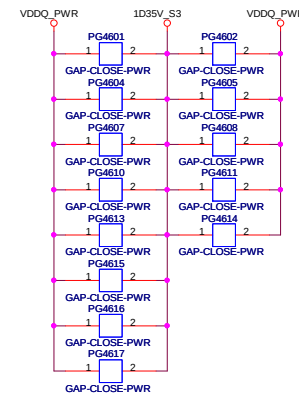
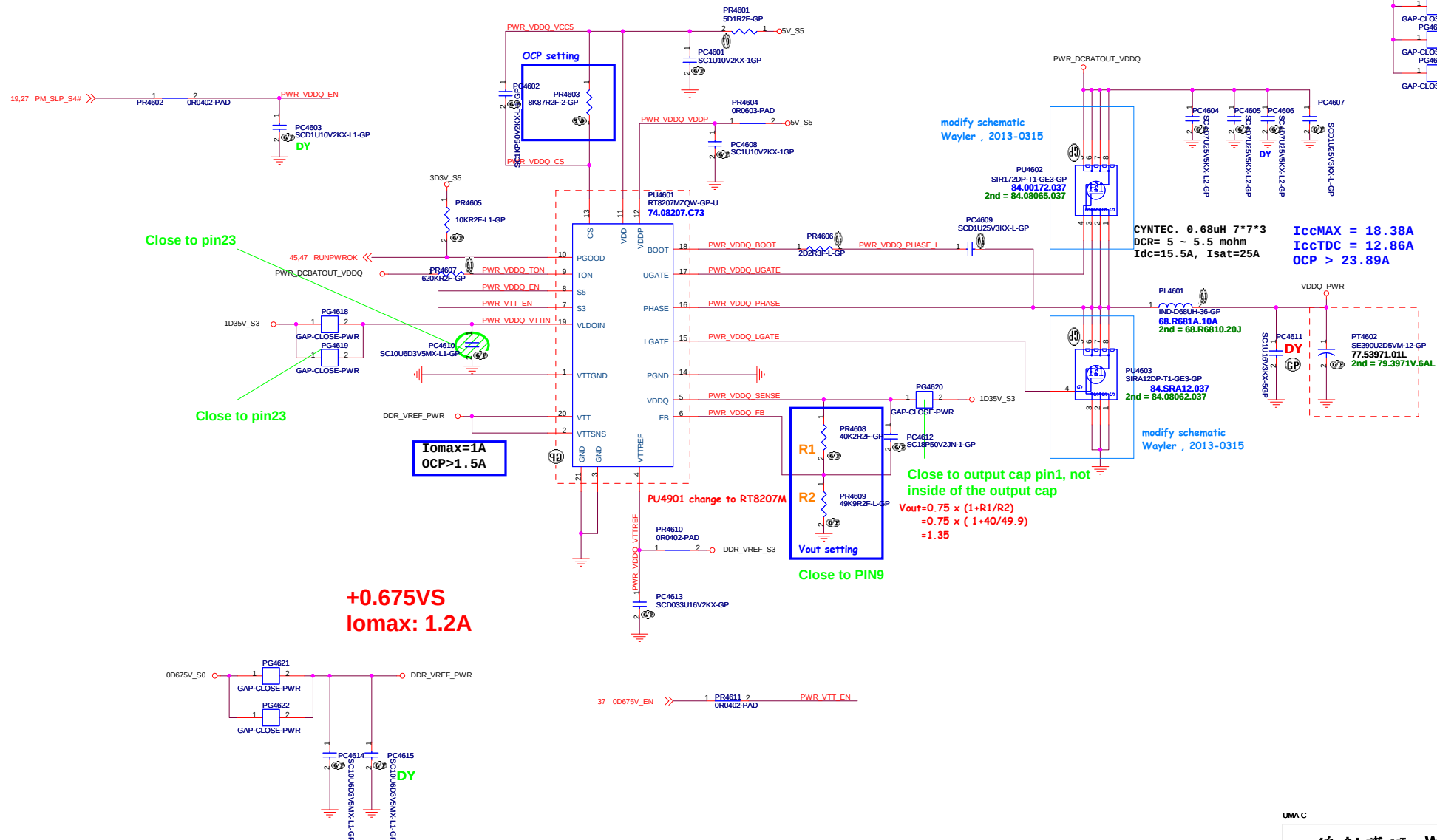
Iomax = 6A
OCP > 8A

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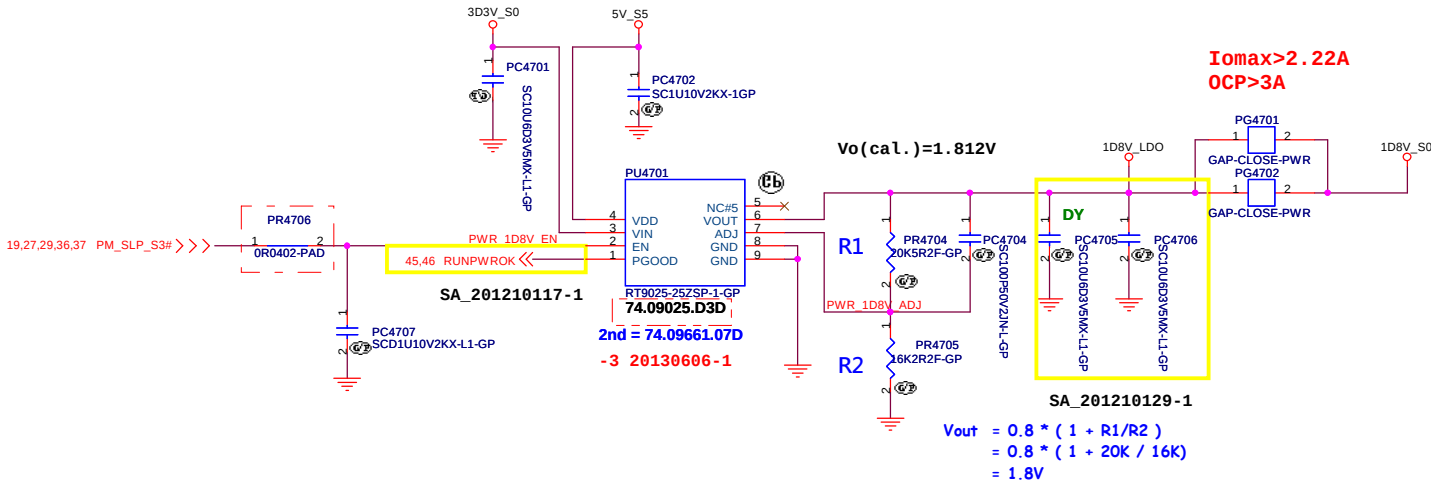


RT8207L for VDDQ



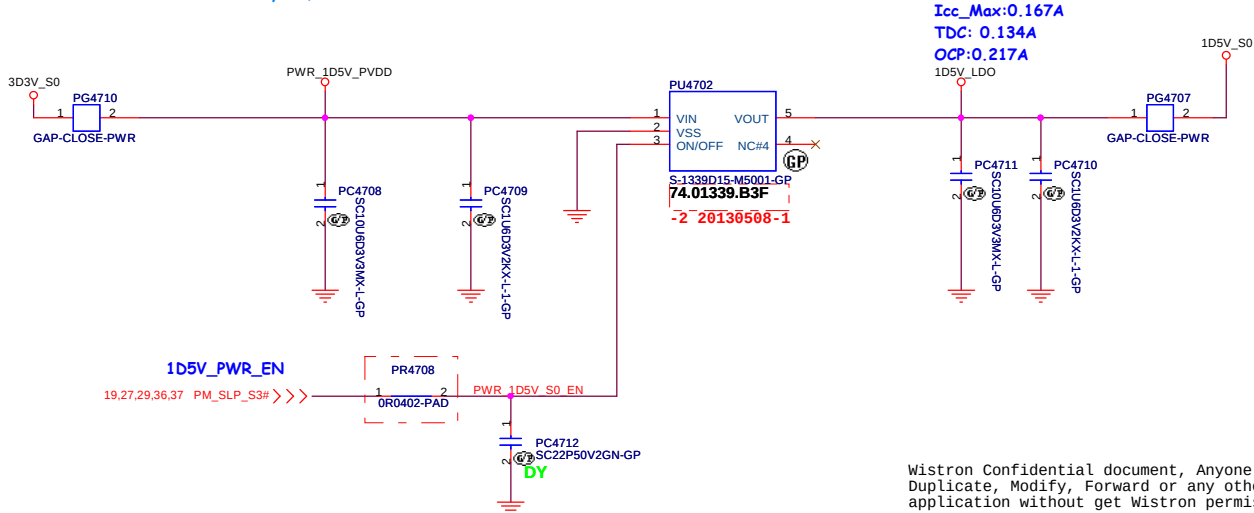
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RT9025 for 1D8V_S0



S-1339D15 for 1D5V_S0

modify schematic
Wayler , 2013-0315



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Title	Author	Year	Source
1. The Role of the Teacher in the 21st Century	John Hattie	2009	Visible Learning
2. The Science of Learning: How the Brain Works	David Sousa	2006	Corwin Press
3. The Power of Learning Styles	Richard Mayer	2008	Cambridge University Press
4. The Art of Teaching: A Practical Guide	William G. Perry	1998	Harvard University Press
5. The Future of Education: A Vision for the 21st Century	Bill Gates	2007	Microsoft Press

LDO 1D8V&1D5V(RT9025)

Size

Document Number

EA40 CX

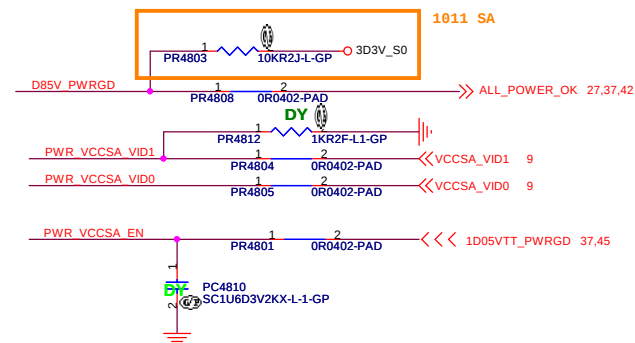
Rev

-3-

Date: Thursday, June 20, 2013

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LDO G978 for VCCSA



D0, D1 V_O Selection Table

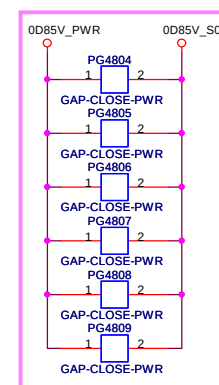
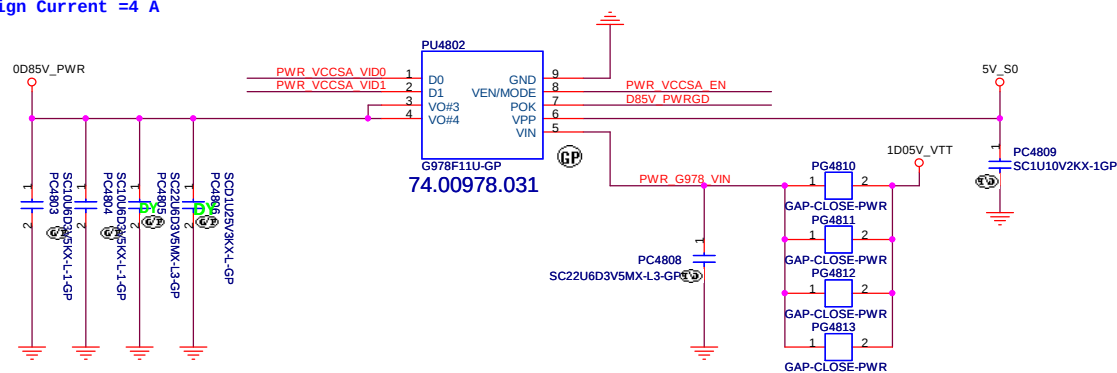
D0	D1	V _O , MODE=0	V _O , MODE=1
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

"x" means "don't care".

VEN/MODE Logic

VEN/MODE (VPP=5V)	EN logic	VEN/MODE (VPP=5V)	MODE logic
<0.6V	0	<2.0V	0
>1.0V	1	>2.6V	1

Design Current = 4 A



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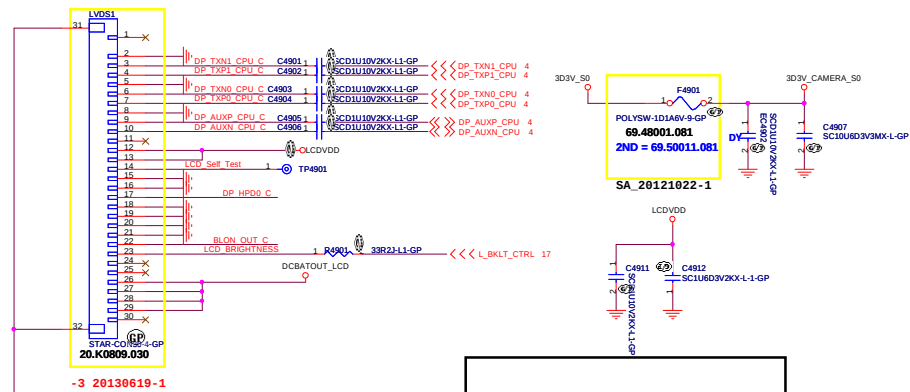
UMA C

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Title			
VCCSA LDO G978			
Size	Document Number		Rev
A3	EA40_CX		-3
Date: Thursday, June 20, 2013		Sheet 48 of	103

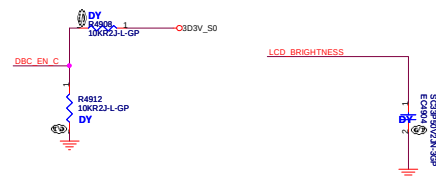
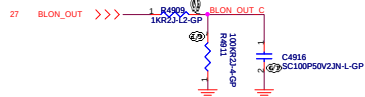
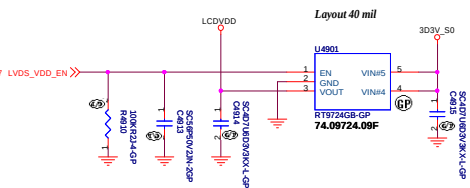
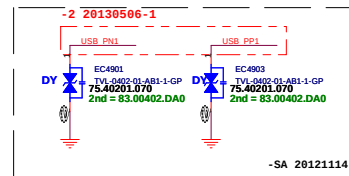
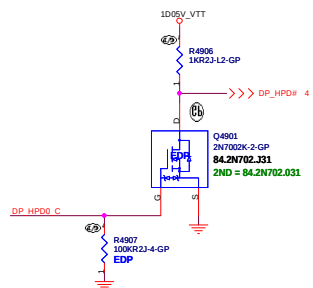
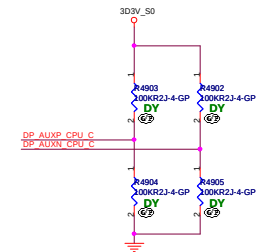
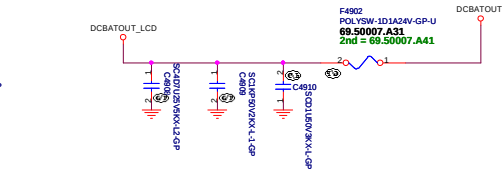
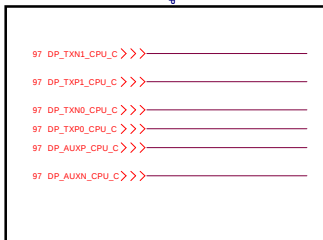
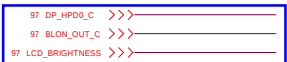
SSID = VIDEO

eDP Conn.

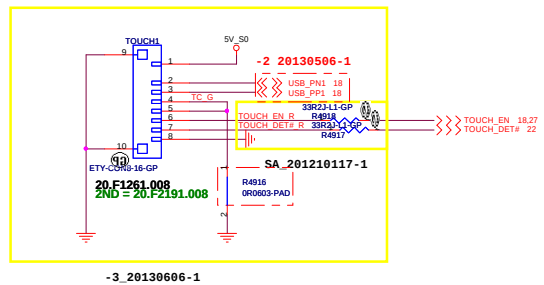
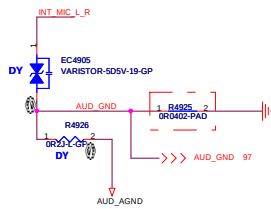
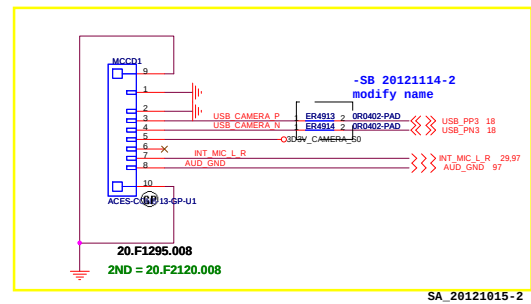


```
BY cable
L(pin5 GND):DMIC
H(pin5:floating):AMIC
```

For TestPoint



Touch Conn.



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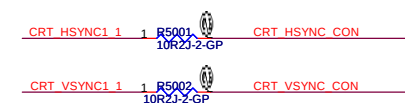
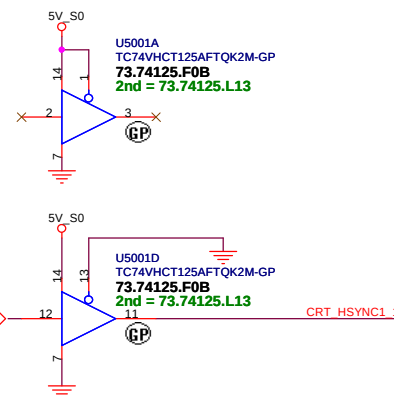
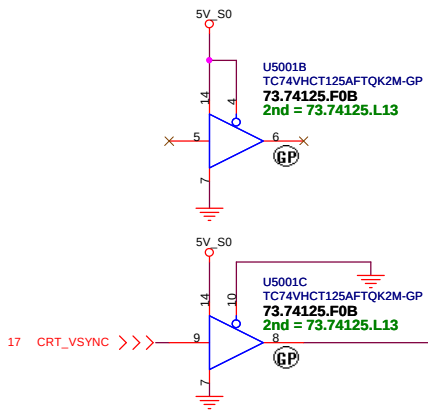
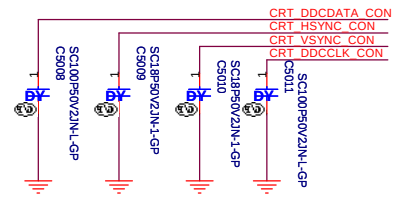
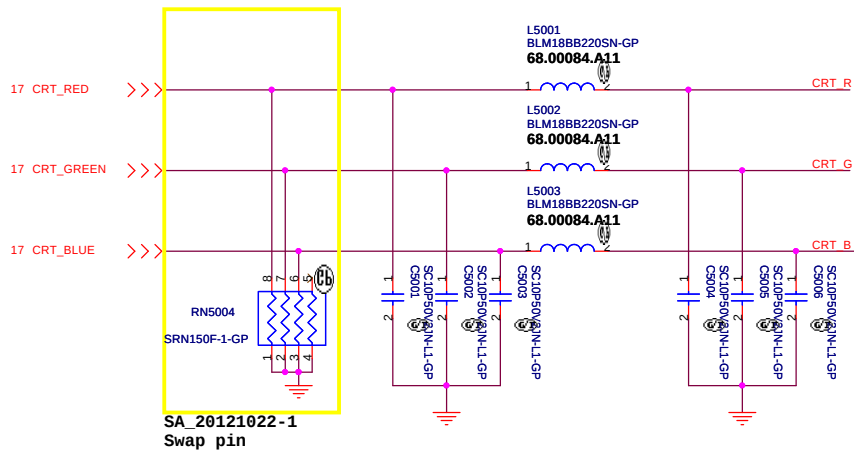
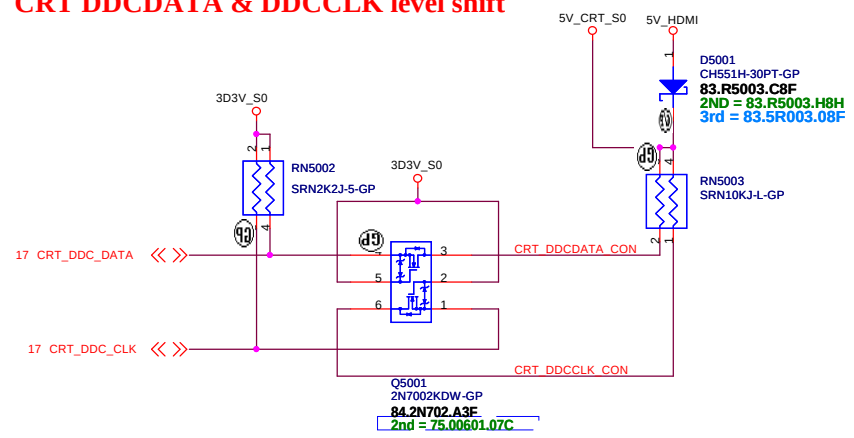
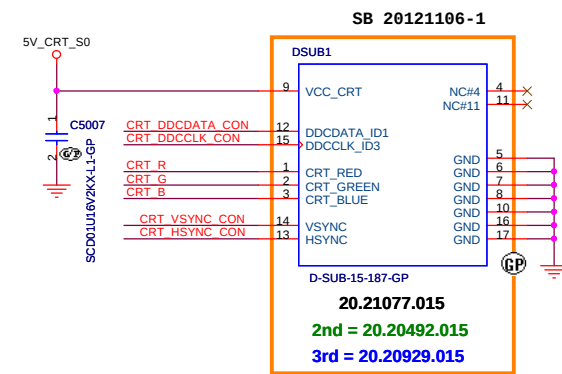
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Title

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CRT DDCDATA & DDCCLK level shift



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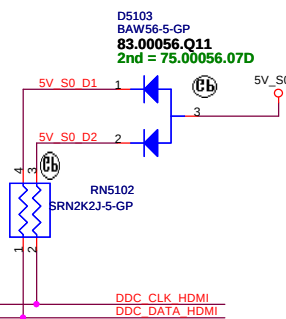
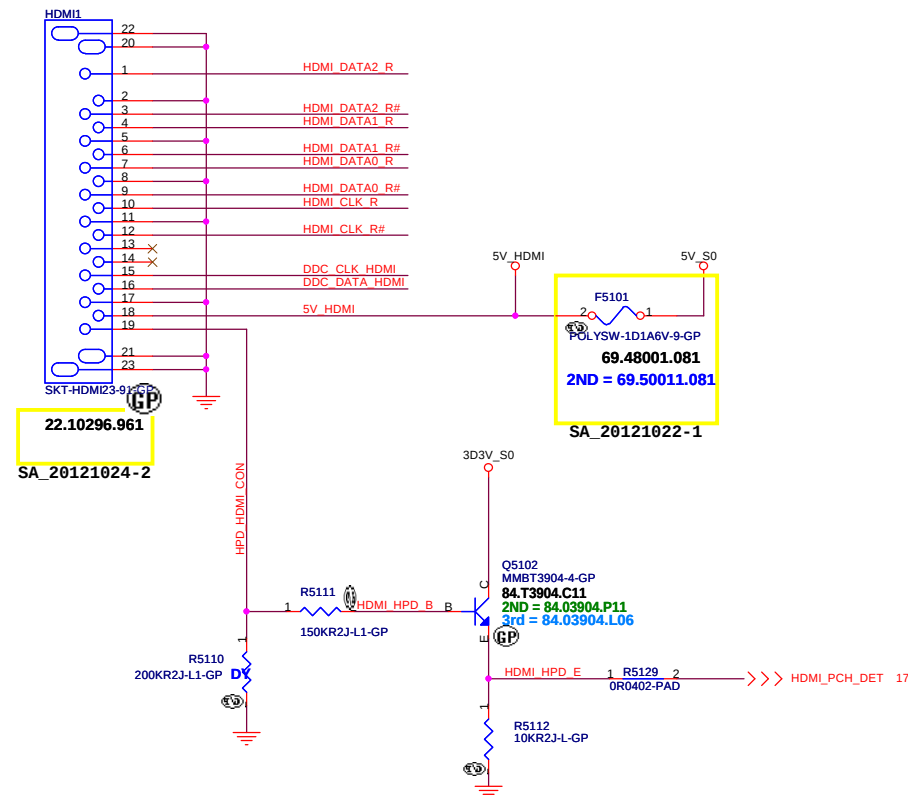
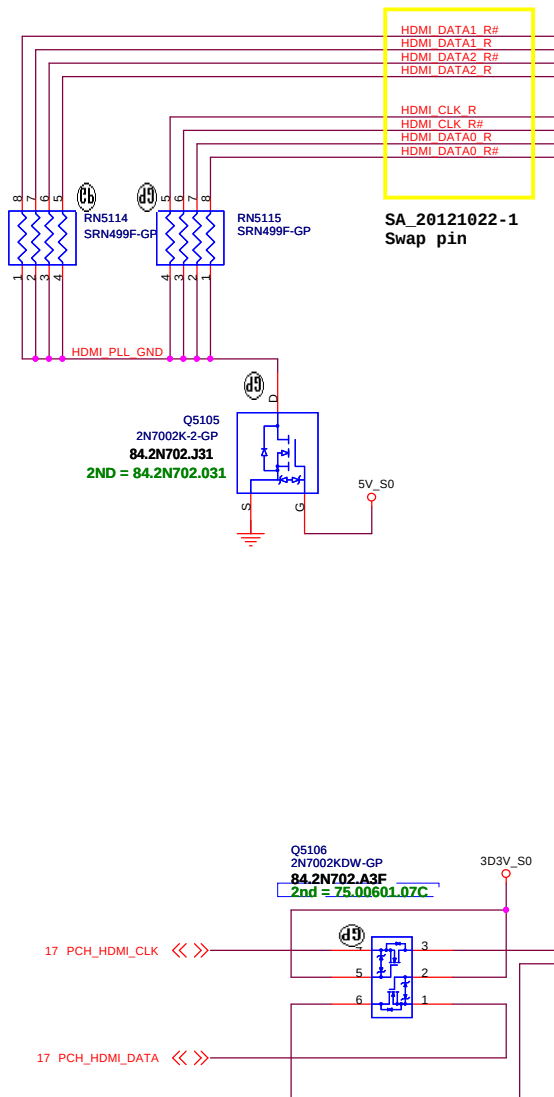
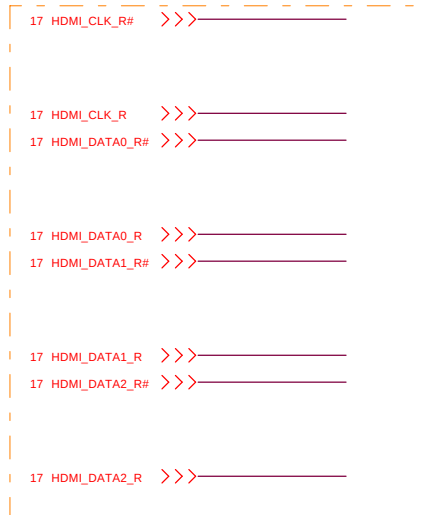
SSID = VIDEO

HDMI Level Shifter & CONNECTOR

Close to HDMI Connector

change = DIS:499 ohm
Fist = UMA Muxless:680 ohm

-1_20130315A



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Title		
HDMI Level Shifter/Connector		
Size	Document Number	Rev
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Date:	Thursday, June 20, 2013	Sheet 51 of 103

LED BACKLIGHT CONVERTER POWER

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Title			
eDP			
Size	Document Number		Rev
A3	EA40 CX		-3
Date:	Thursday, June 06, 2013		Sheet 52 of 103

1

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Title		
S-VIDEO		
Size	Document Number	Rev
A4	EA40 CX	-3
Date: Thursday, June 06, 2013		Sheet 53 of 103

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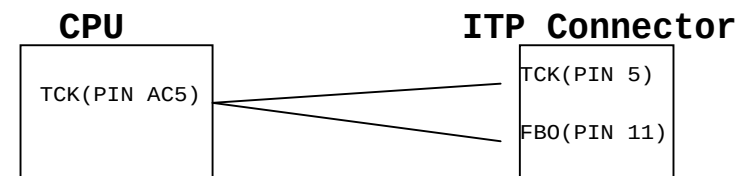
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Title Reserved		
Size A4	Document Number EA40 CX	Rev -3
Date: Thursday, June 06, 2013		Sheet 54 of 103

SSID = User.Interface

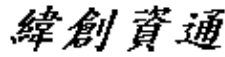
ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



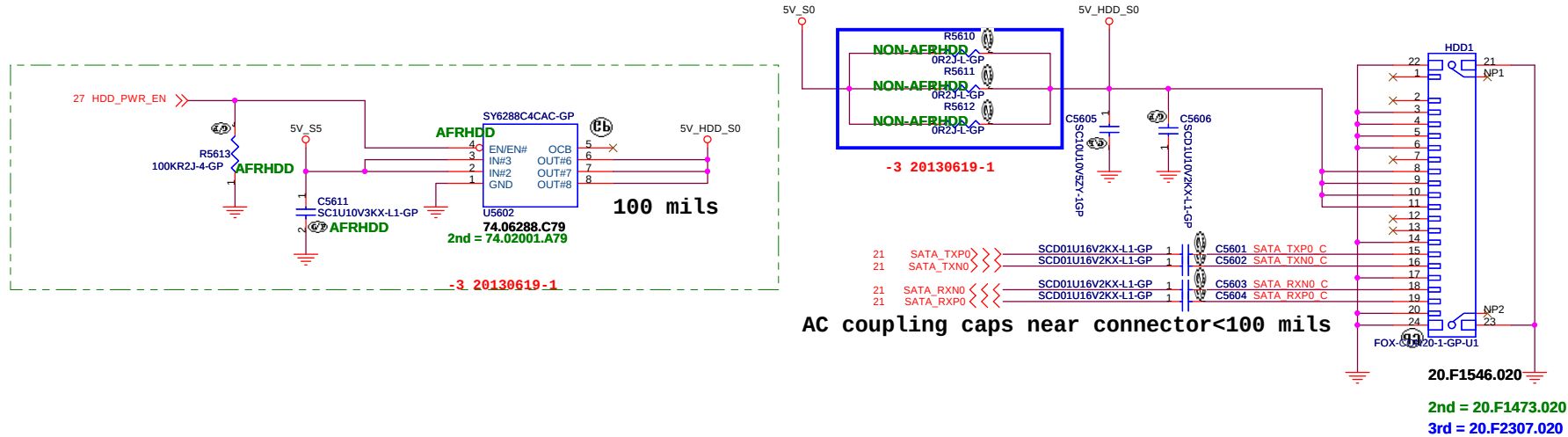
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Title ITP		
Size A4	Document Number EA40 CX	Rev -3
Date: Thursday, June 06, 2013	Sheet 55 of	103

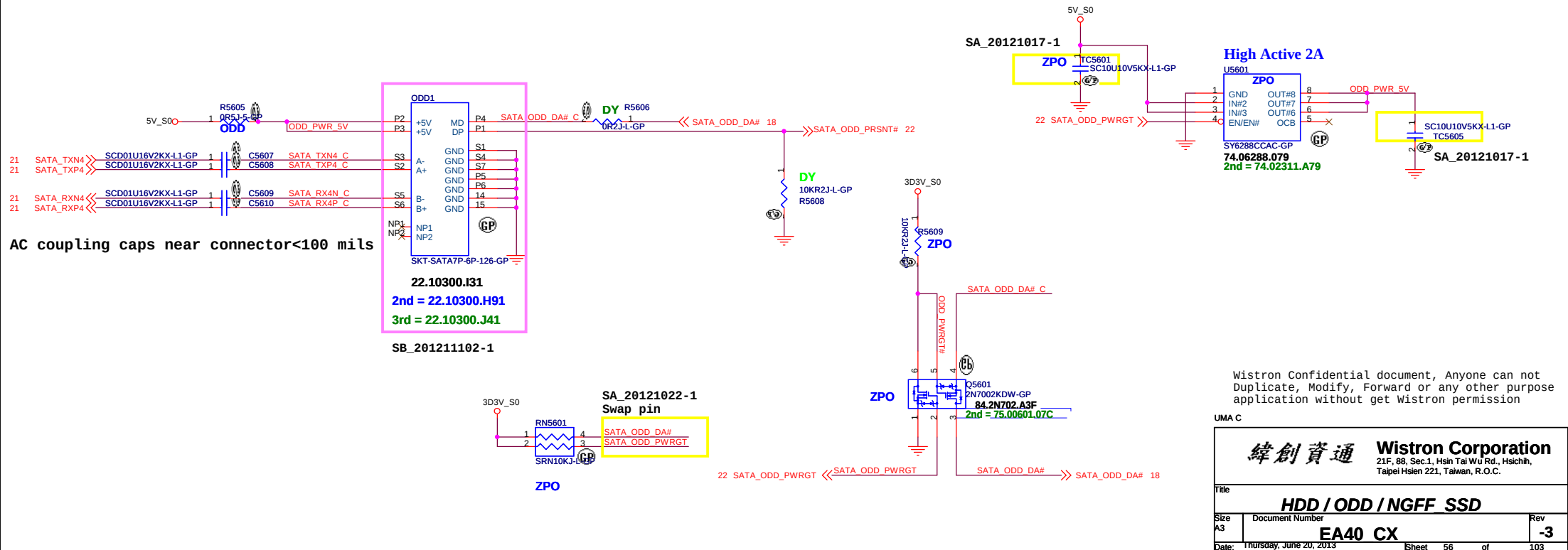
SSID = SATA

SATA HDD Connector



ODD Connector

SATA Zero Power ODD



5	4	3	2	1
D				
C				
B				
A				

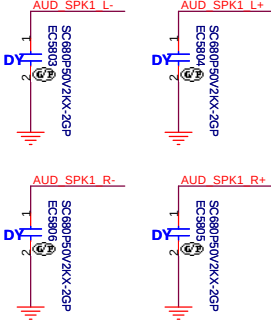
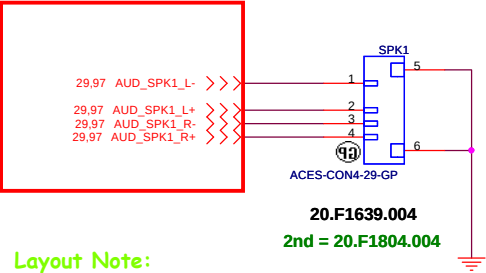
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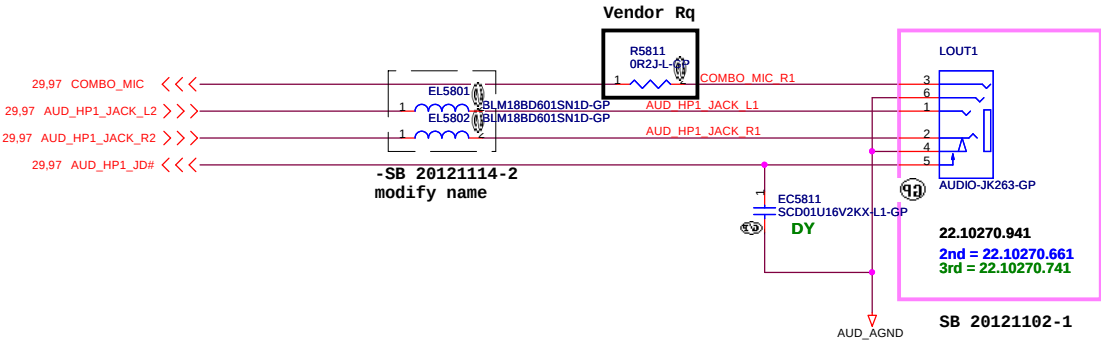
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
E-SATA/USB CHARGER		
Size	Document Number	Rev
A3	EA40 CX	-3
Date:	Thursday, June 06, 2013	Sheet 57 of 103

1

SSID = AUDIO *Speaker*

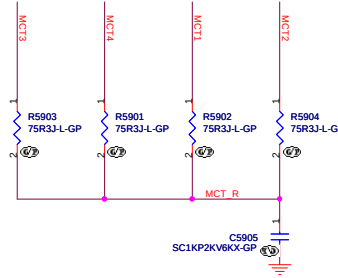
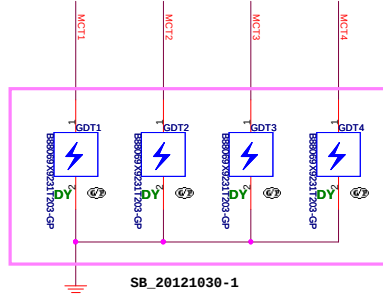
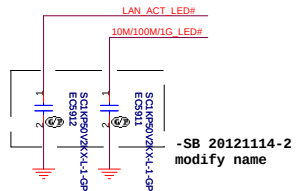
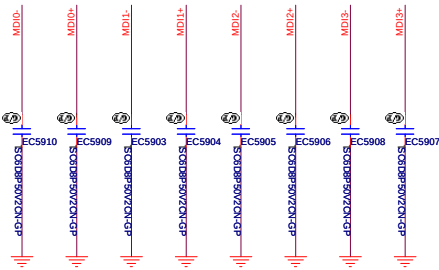
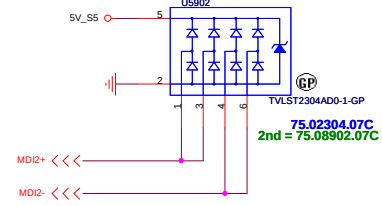
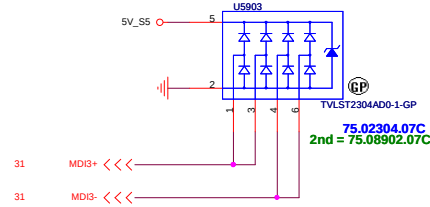
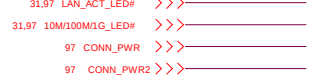
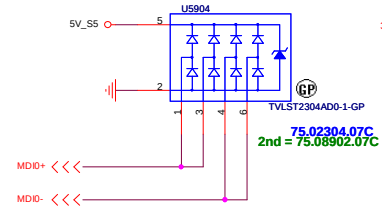
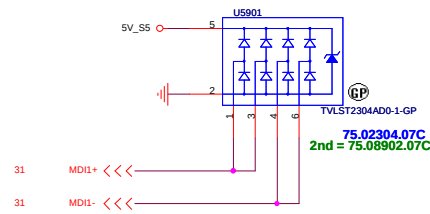
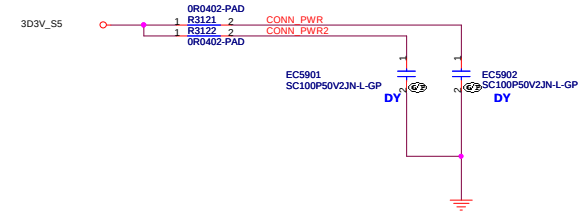
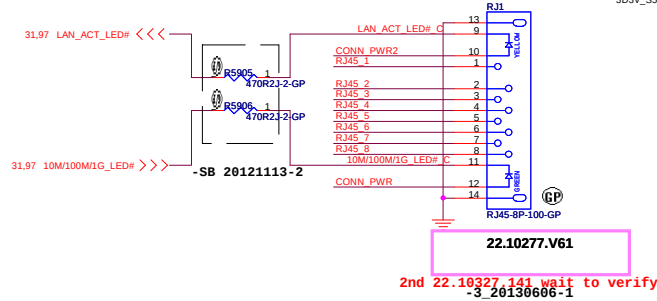
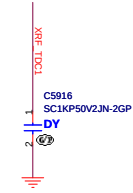
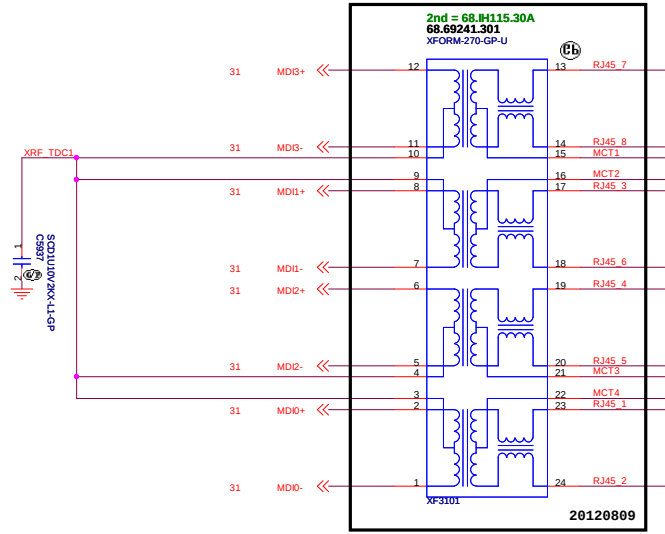


Combo Jack



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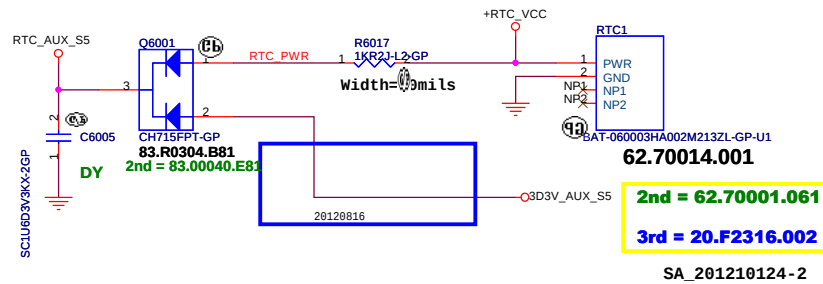
SSID = LAN



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UMAC		緯創資通 Wistron Corporation	
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Title	LAN CONNECTOR		
Size	Document Number	Rev	-3
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Date: Thursday, June 20, 2013			

SSID = RTC



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Title			
Flash/RTC			
Size	Document Number	Rev	
Custom	EA40 CX	-3	
Date:	Thursday, June 20, 2013	Sheet 60 of 103	

SSID = USB

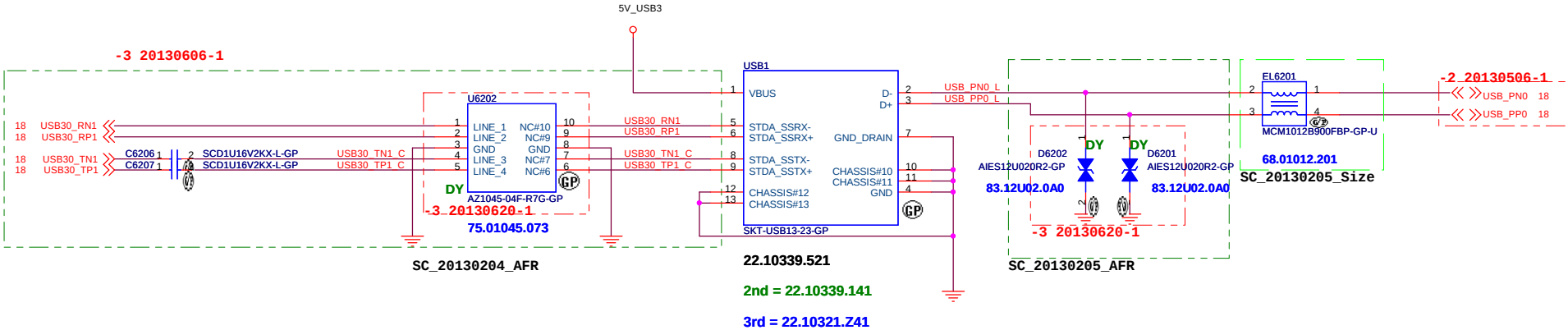
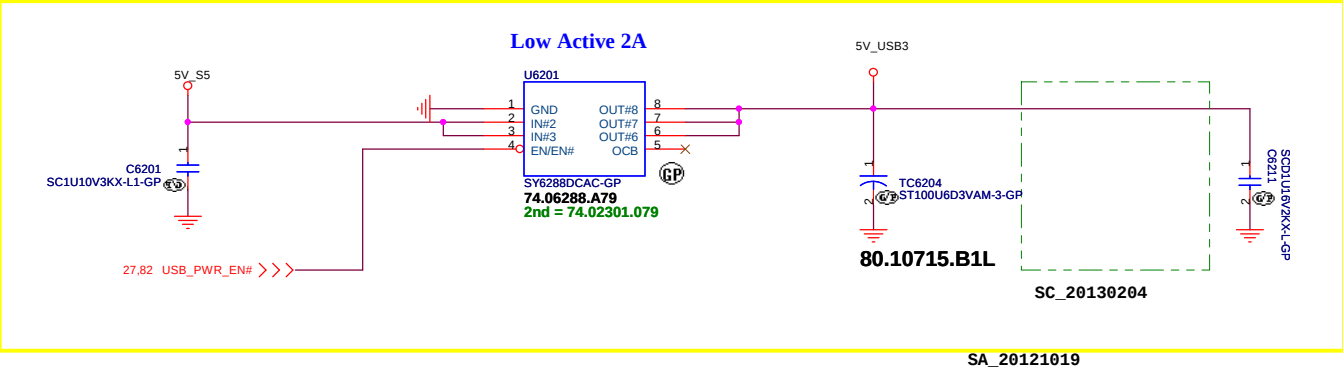
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Title		
USB Power SW		
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1

USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	



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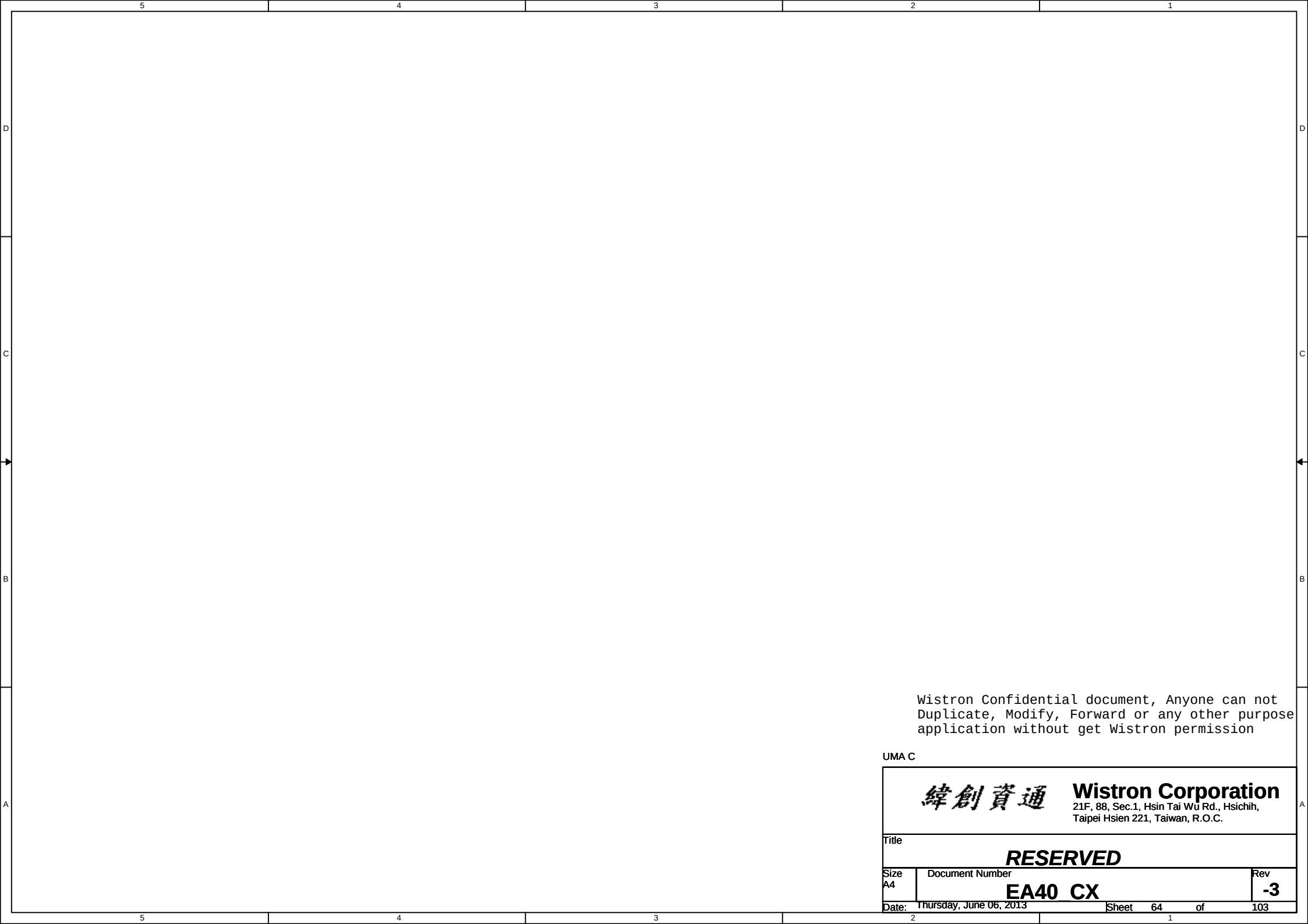
SSID = User.Interface
Bluetooth Module conn.

ANNIE Bluetooth Module

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Title		
Bluetooth		
Size	Document Number	Rev
A4	EA40 CX	-3
Date: Thursday, June 06, 2013		Sheet 63 of 103

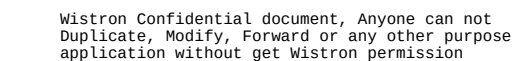


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Title		
RESERVED		
Size A4	Document Number EA40 CX	Rev -3
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Mini Card Connector(802.11a/b/g/n)



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Title			
MINICARD(WLAN)/ITP CONN			
Size A3	Document Number		Rev
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Date:	Friday, June 21, 2013	Sheet 65 of	103

SSID = Wireless

Mini Card Connector(WWAN)

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Title		
WWAN Connector		
Size	Document Number	Rev
A4	EA40 CX	-3
Date: Thursday, June 06, 2013		Sheet 66 of 103

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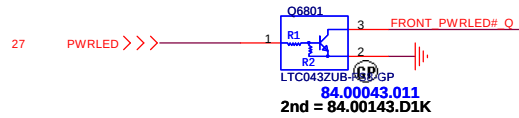
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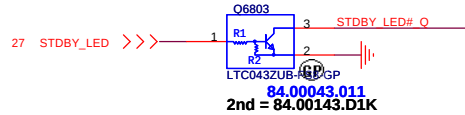
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Title Reserved		
Size A4	Document Number EA40 CX	Rev -3
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SSID = User.Interface

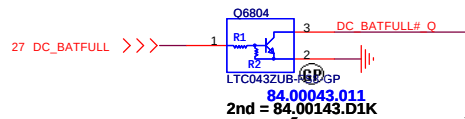
Power button LED



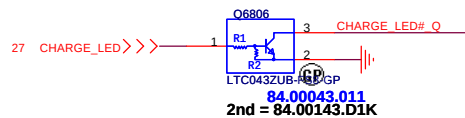
Power STDBY_LED



Battery LED2(DC_BATFULL)

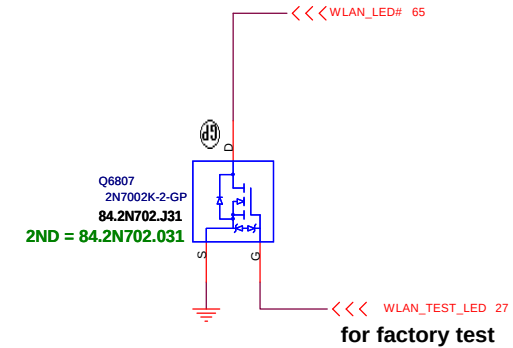


Battery LED1(CHARGE)

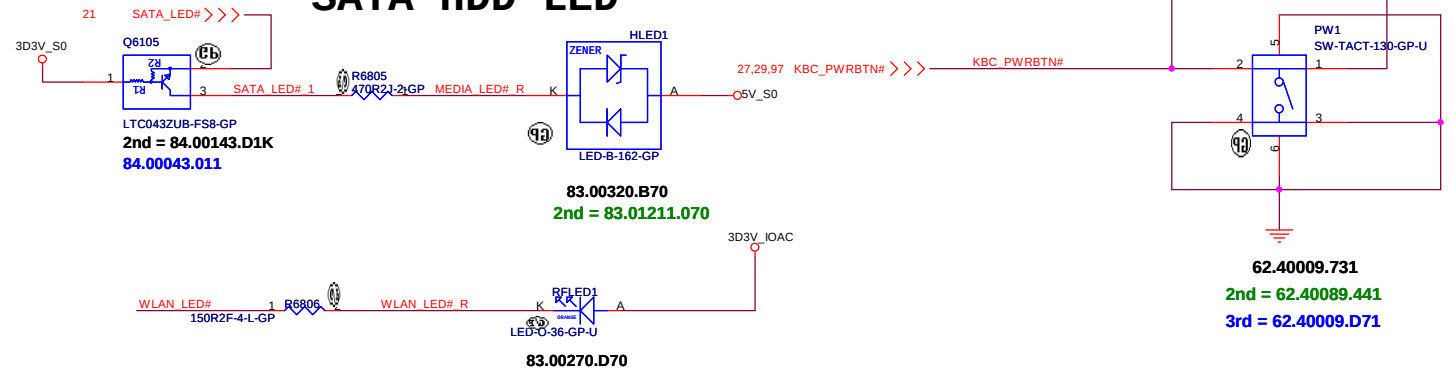


WLAN_LED

From module



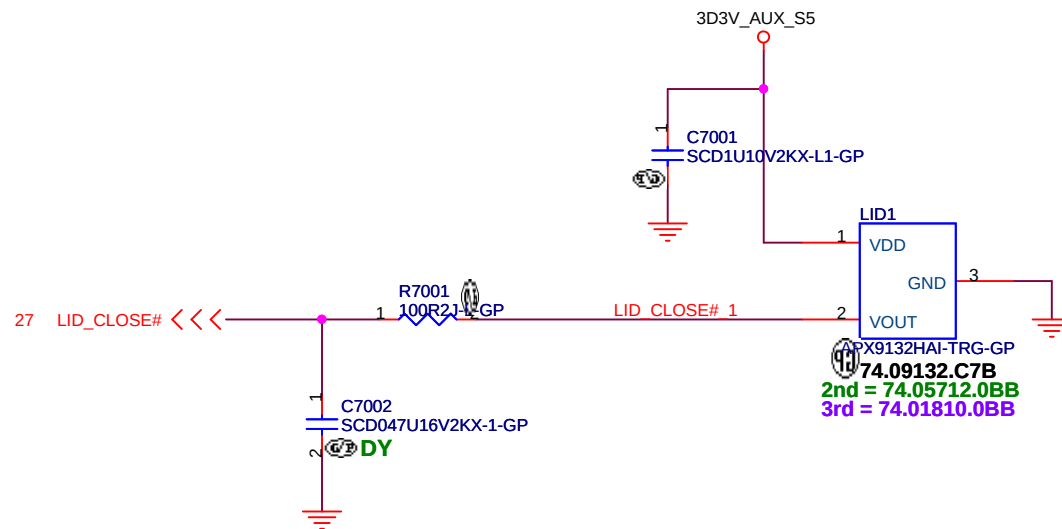
SATA HDD LED



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Title			
LED Bard/Power Button			
Size	Document Number	Rev	
Custom	EA40-0X	-3	
Date	Thursday, June 20, 2013	Sheet	68 of 103



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Title

Hall Sensor

Size
A4

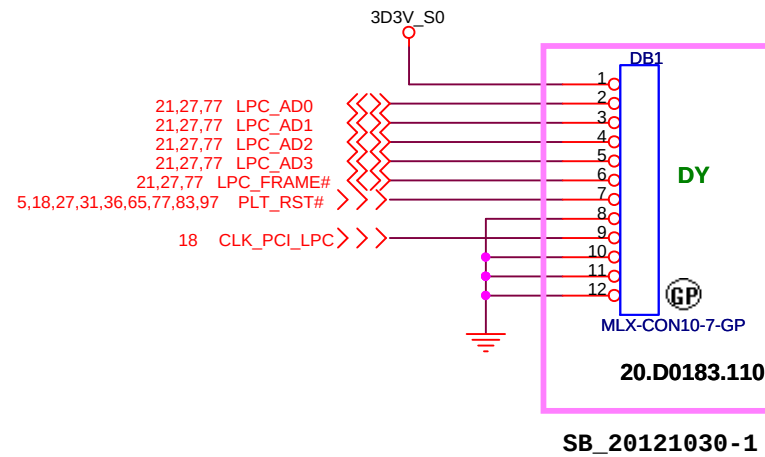
Document Number

EA40 CX

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-3

Date: Thursday, June 20, 2013

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Title					
Dubug connector					
Size	Document Number				Rev
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Title		
Reserved		
Size	Document Number	Rev
A3	EA40 CX	-3
Date:	Thursday, June 06, 2013	Sheet 72 of 103

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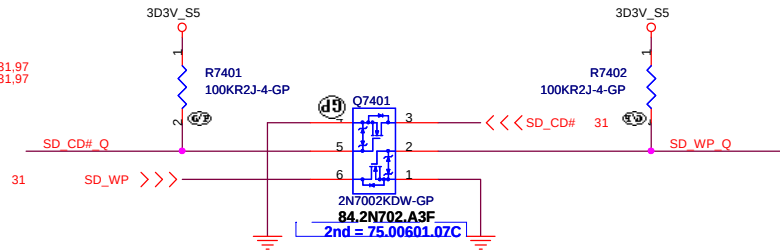
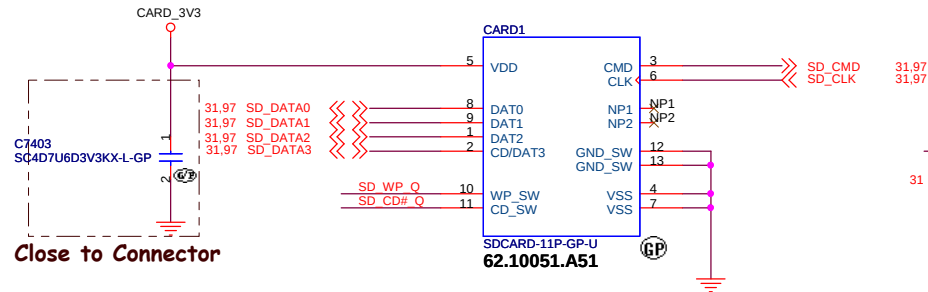
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Wistron Corporation		
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SSID = SDIO

SD/MMC Card Reader



SP1	SP1	SD_D7	MS_INS#	xD_RDY
SP2	SP2	SD_D6	MS_INS#	xD_RE#
SP3	SP3	SD_D5	MS_INS#	xD_CE#
SP4	SP4	SD_D4	MS_INS#	xD_WE#
SP5	SP5	SD_D1	MS_CLK	xD_D6
SP6	SP6	SD_D0	MS_D7	xD_D5
SP7	SP7	SD_CLK	MS_D3	xD_D4
SP8	SP8	SD_CMD	MS_D6	xD_D3
SP9	SP9	SD_D3	MS_D2	xD_D2
SP10	SP10	SD_D2	MS_D2	xD_D7
SP11	SP11	SD_WP	MS_BS	xD_CLE
SP12	SP12	SD_WP	MS_D1	xD_WP#
SP13	SP13	SD_CD#	MS_D5	xD_ALE
SP14	SP14	MS_D4	MS_D4	xD_D0
SP15	SP15	MS_D0	MS_D0	xD_D1
SP16	SP16	MS_D0	MS_D0	xD_CD#

97 SD_WP_Q >>>
97 SD_CD#_Q >>>

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Title CARD Reader CONN
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SSID = ExpressCard

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SSID = User.Interface

Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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A4

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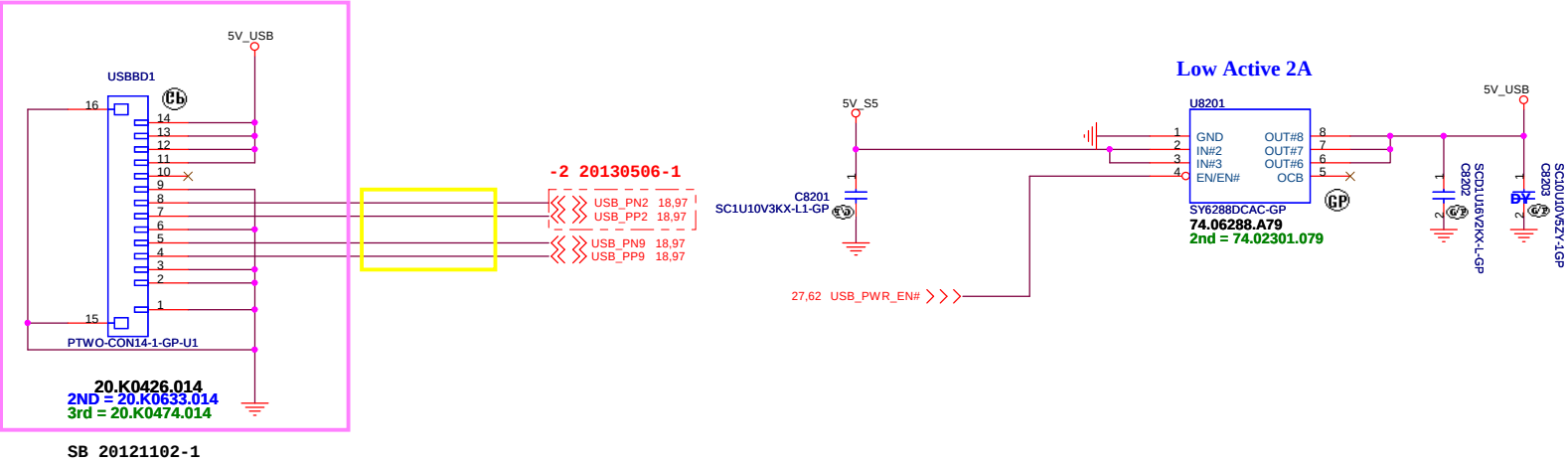
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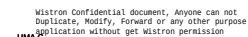
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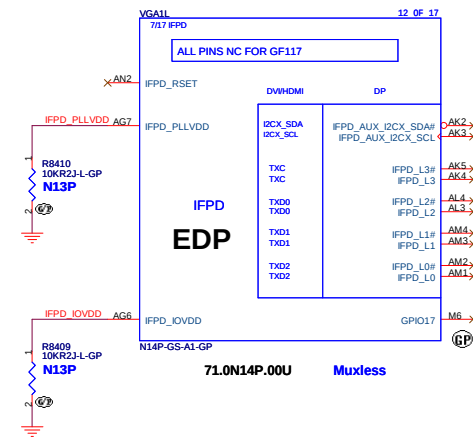
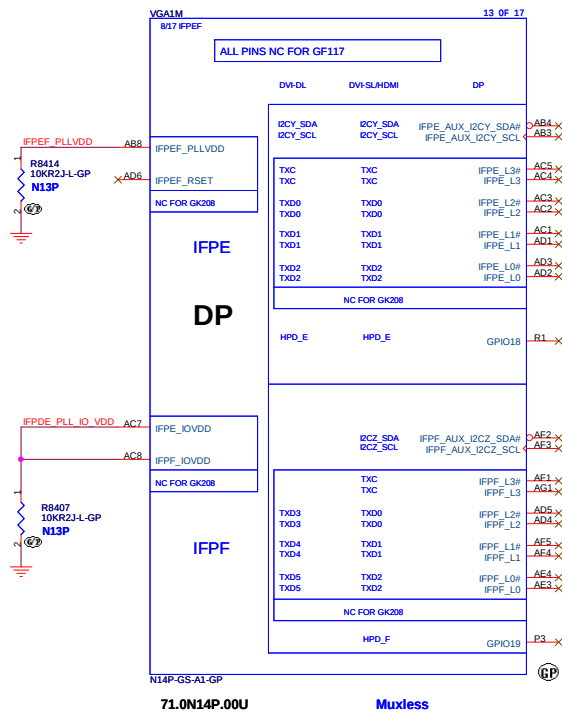
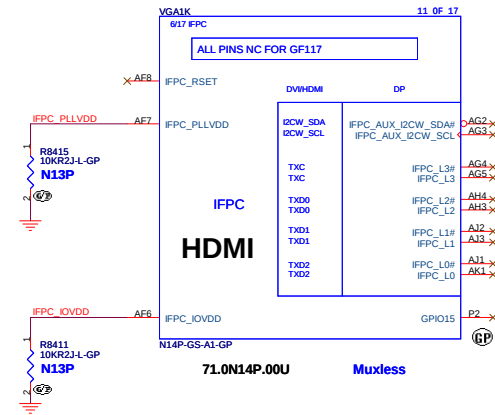
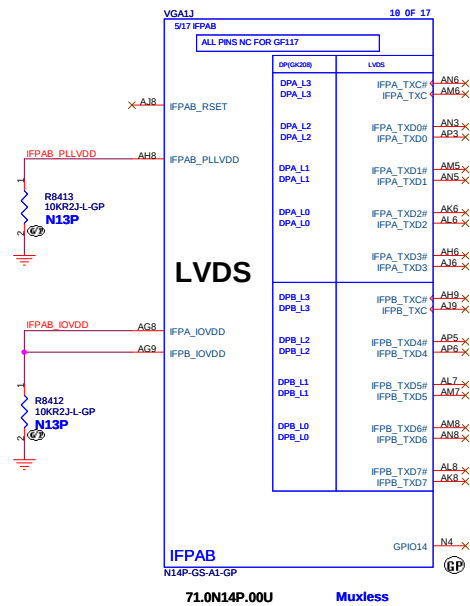
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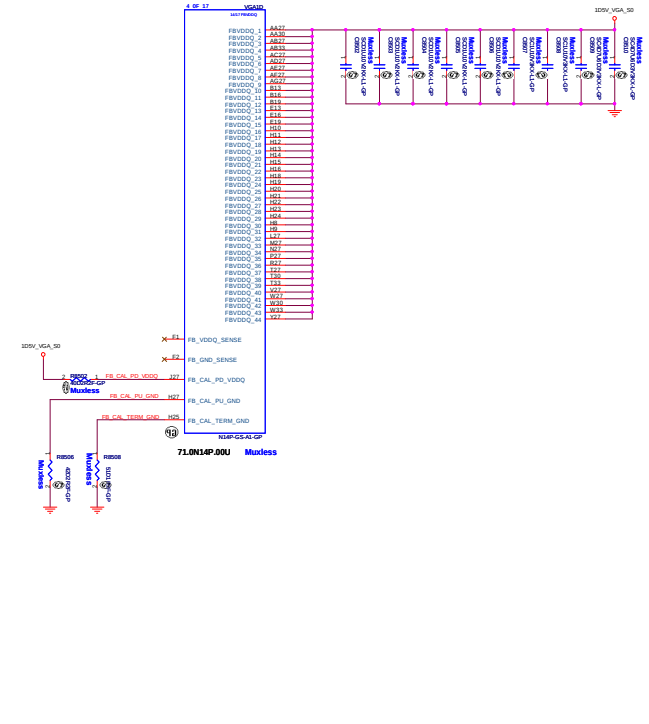
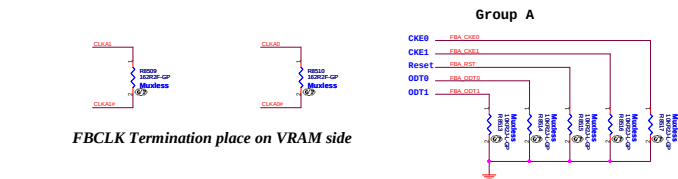


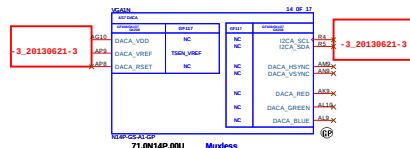


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GPU (DIGITALOUT)			
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unknown function

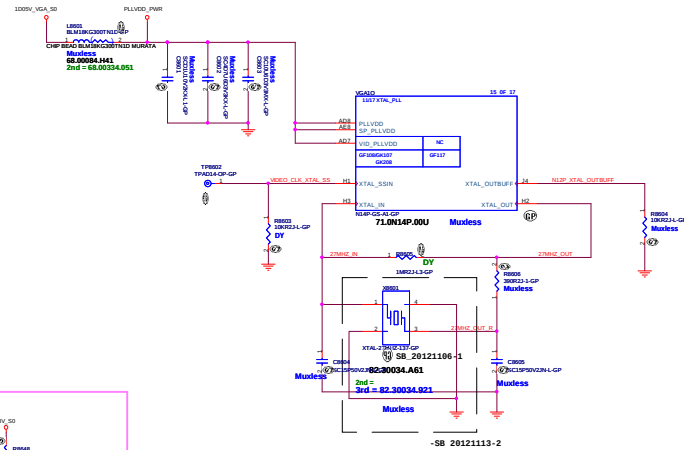
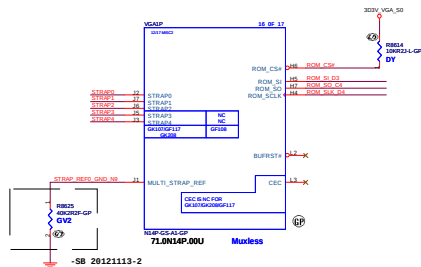
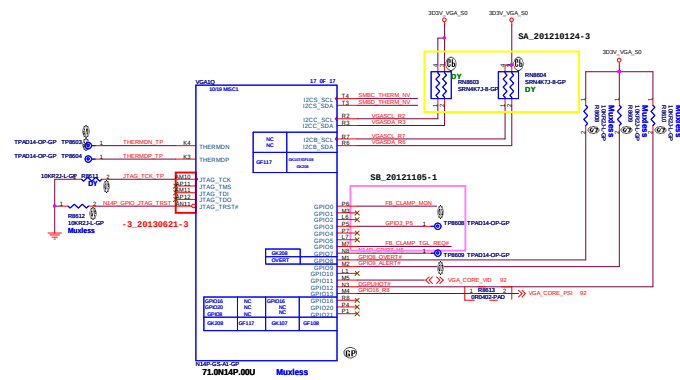
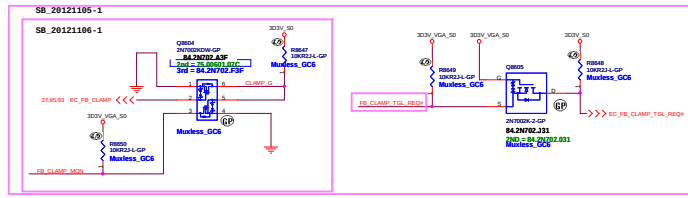
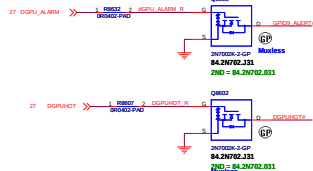


Table 113. Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

4.99Kohm
10Kohm
15Kohm
20Kohm
24.9Kohm
30.1Kohm
34.8Kohm
45Kohm

Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed Ck (MHz)	Memory Data Code Minimum	Status
128Mx16 DDR3	Micron	0x0	1.5 V	MT47L228M16JF-107G1E	1000	1214	Production ready
	Samsung	0x5	1.5 V	K4V2G1648E-BC1A	1000	1204	Production ready
	Hynix	0x6	1.5 V	H5TQ2G63DFR-11C	900	1104	Production ready
		0x7	1.5 V	H5TQ2G63DFR-11C	900	1104	Production ready
		0x8	1.5 V	H5TQ2G63DFR-11C	900	1104	Production ready

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed Ck (MHz)	Memory Data Code Minimum	Status
256Mx16 DDR3	Samsung	0x0	1.5 V	K4V4G1648E-HC11	900	N/A	Production ready
	Micron	0x0	1.5 V	MT47L228M16JF-107G1E	900	N/A	Production ready
	Hynix	0x3	1.5 V	H5TQ4G63MFR-11C	900	N/A	Production ready
		0x4	1.5 V	H5TQ4G63MFR-11C	900	N/A	Production ready

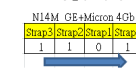
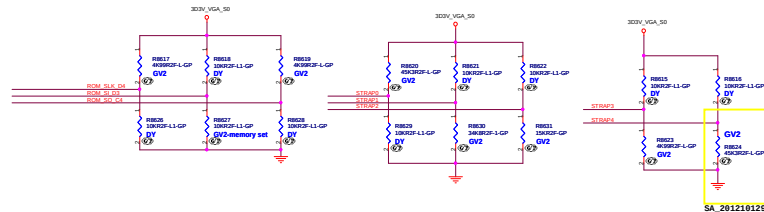
N14M-GE use Binary Strap. Please see the below information.

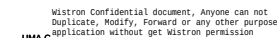
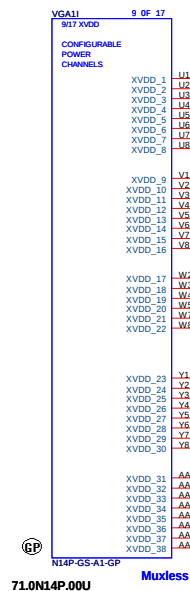
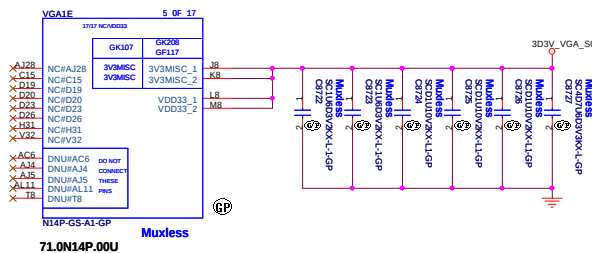
Table 122 Binary Strap Mode Mapping

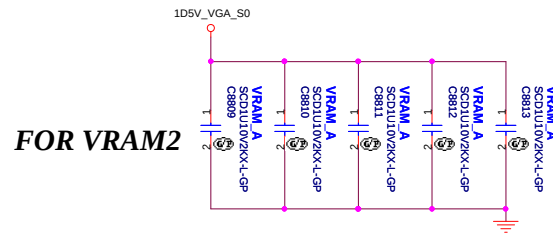
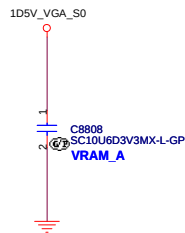
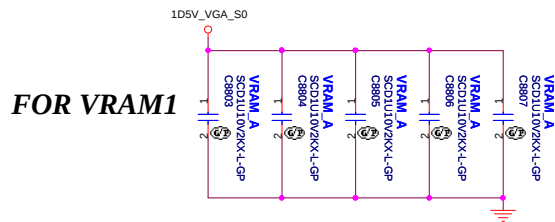
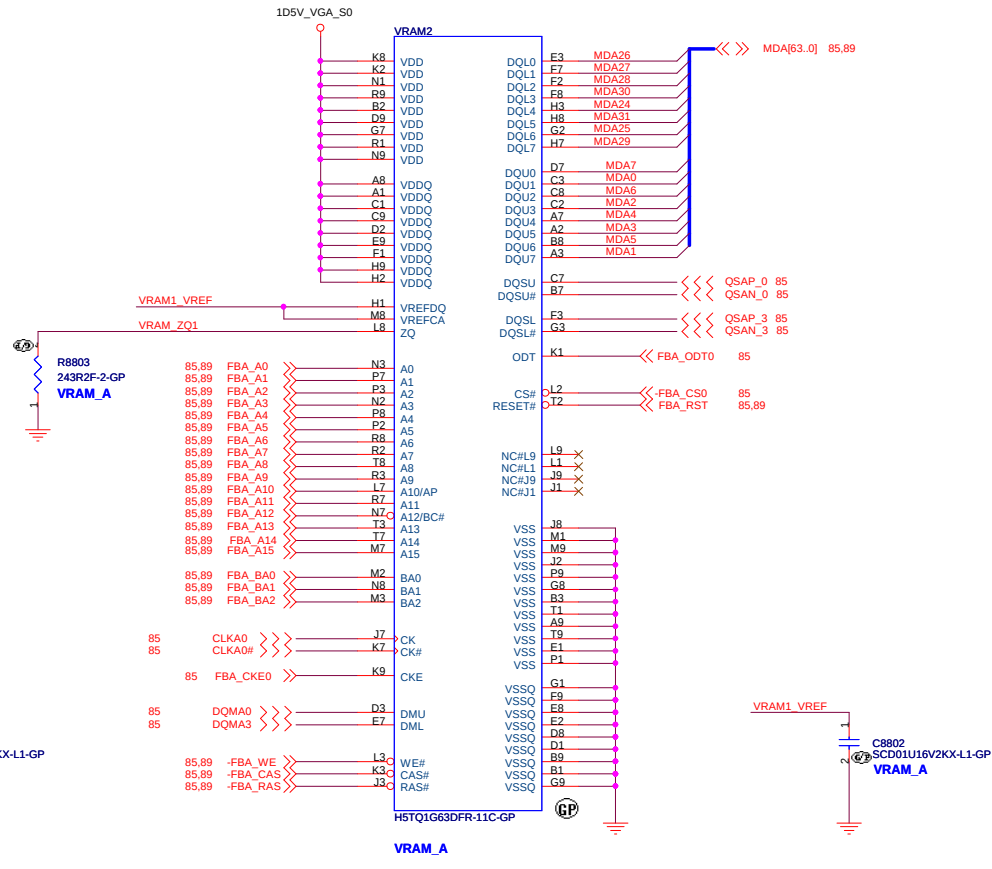
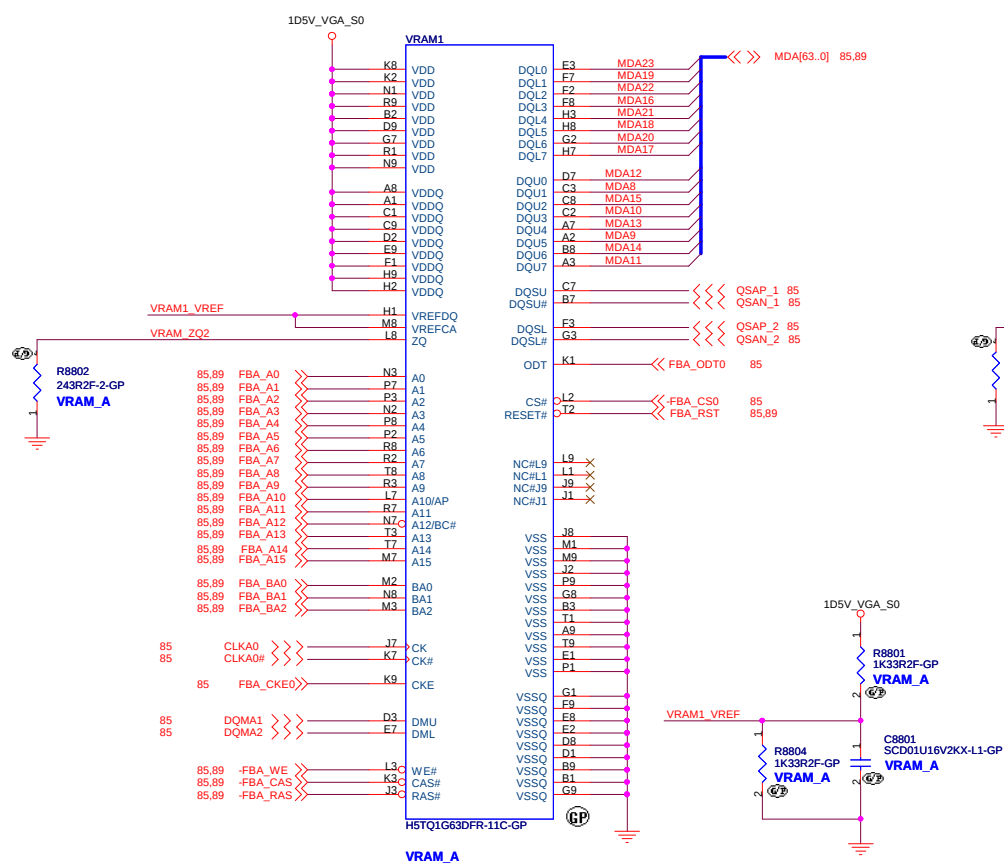
Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10K Ω	Pull-down to GND
ROM_SI	SMB_VENOR	10K Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10K Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10K Ω	See Note below
STRAP1	RAM_CFG[1]	10K Ω	See Note below
STRAP2	RAM_CFG[2]	10K Ω	See Note below
STRAP3	RAM_CFG[3]	10K Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10K Ω	Pull-down to GND

N14P-GV2	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP 4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

N14M-GT1-A2	0x0FE4	0010	15K ohm pull-down	0100	25K ohm pull-down
N14P-GV2-B-A1	0x1292	1000	5K ohm pull-up	0010	15K ohm pull-down

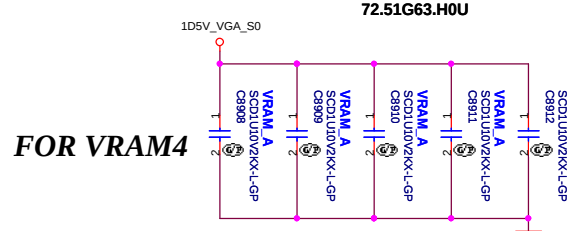
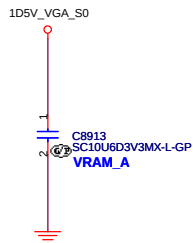
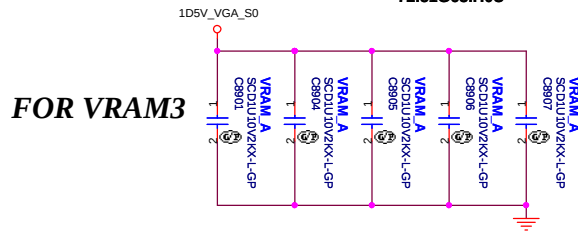
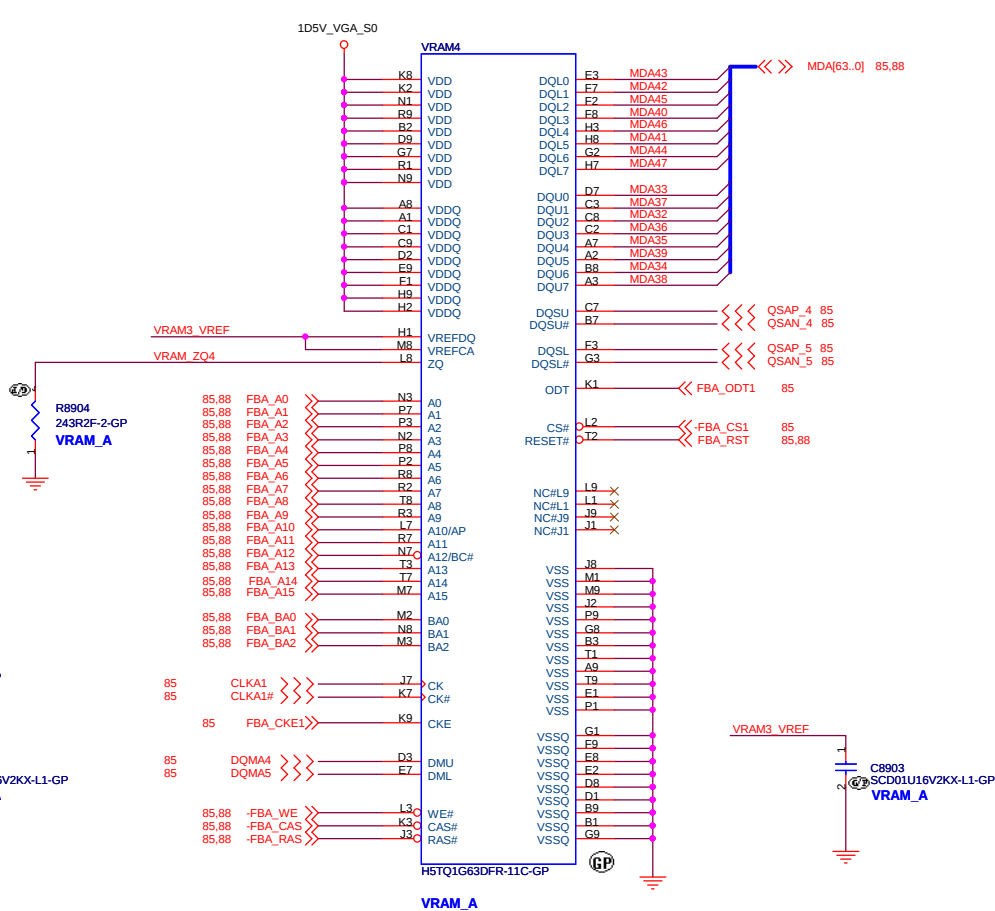
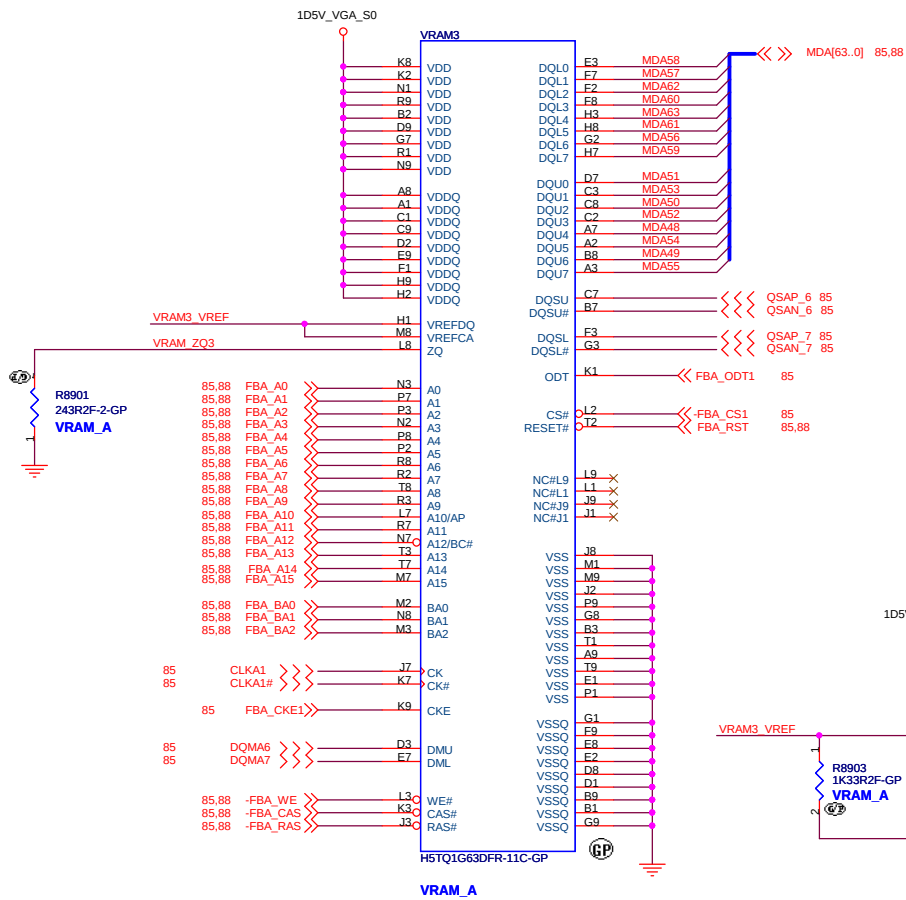






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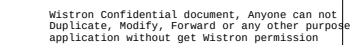
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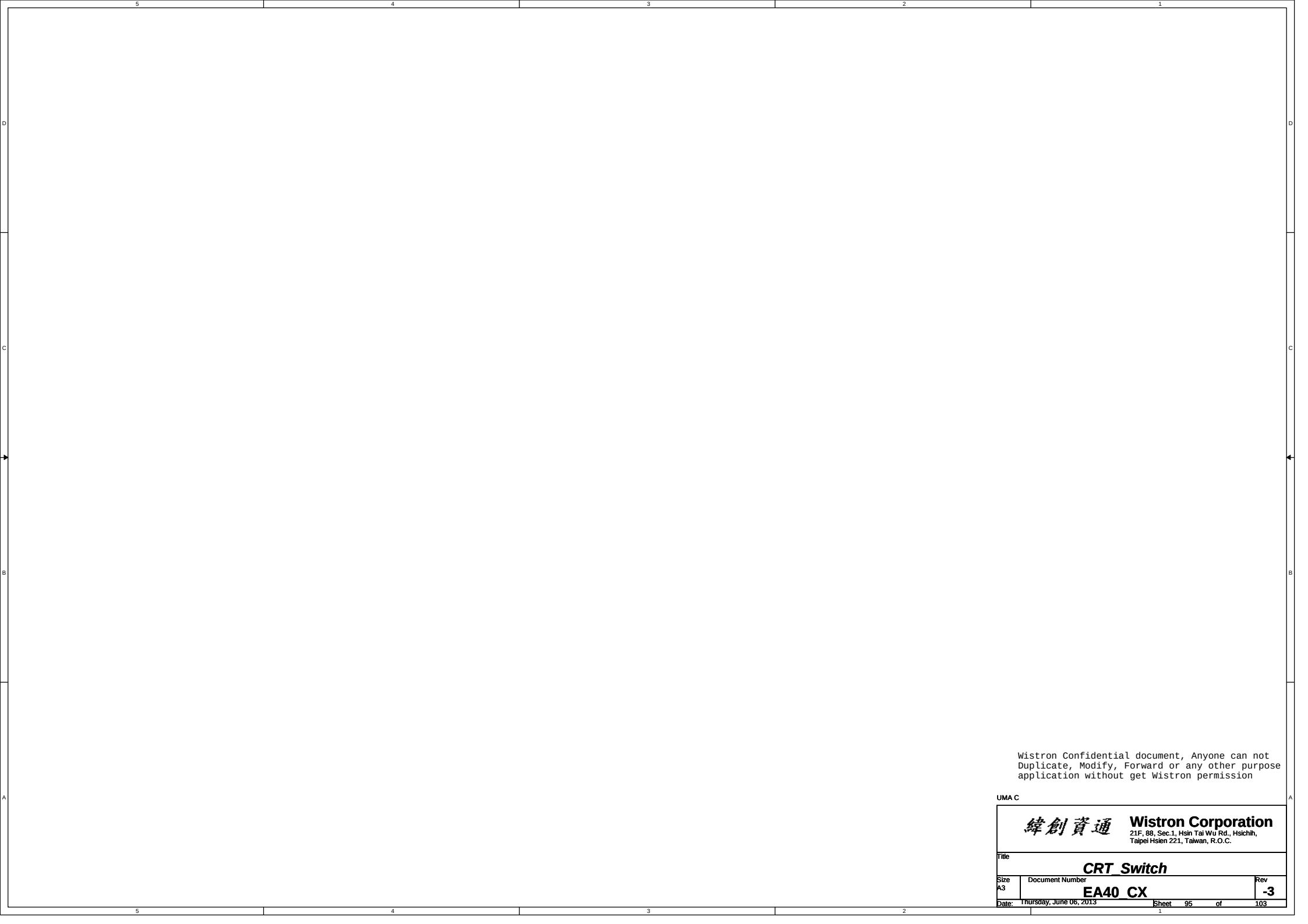
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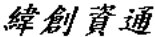
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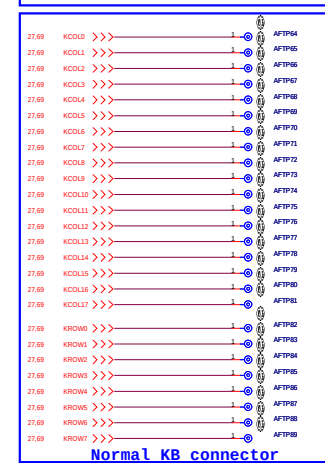
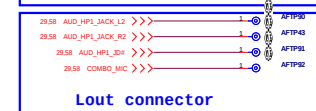
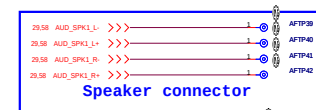
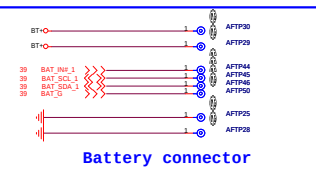
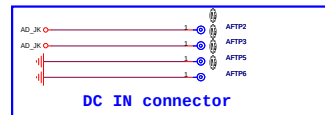
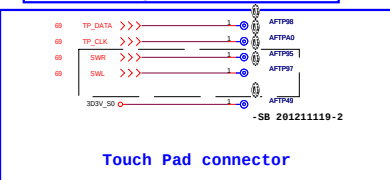
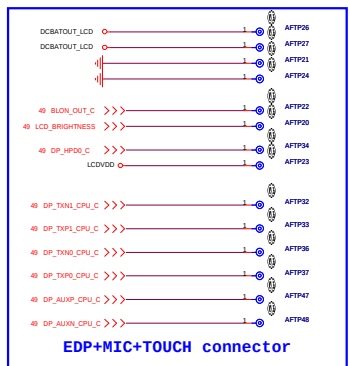
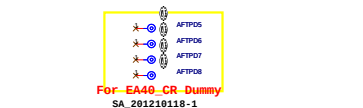
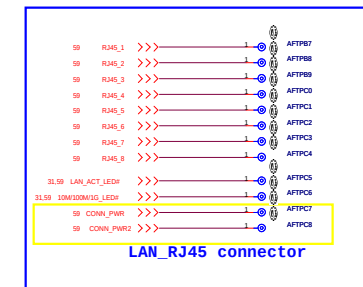
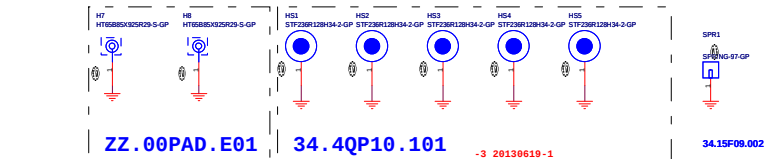
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SSID = SDIO

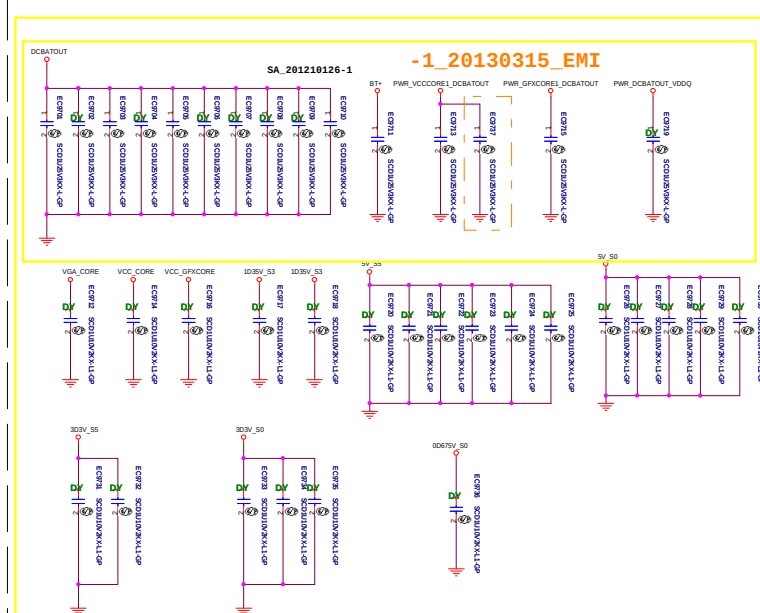
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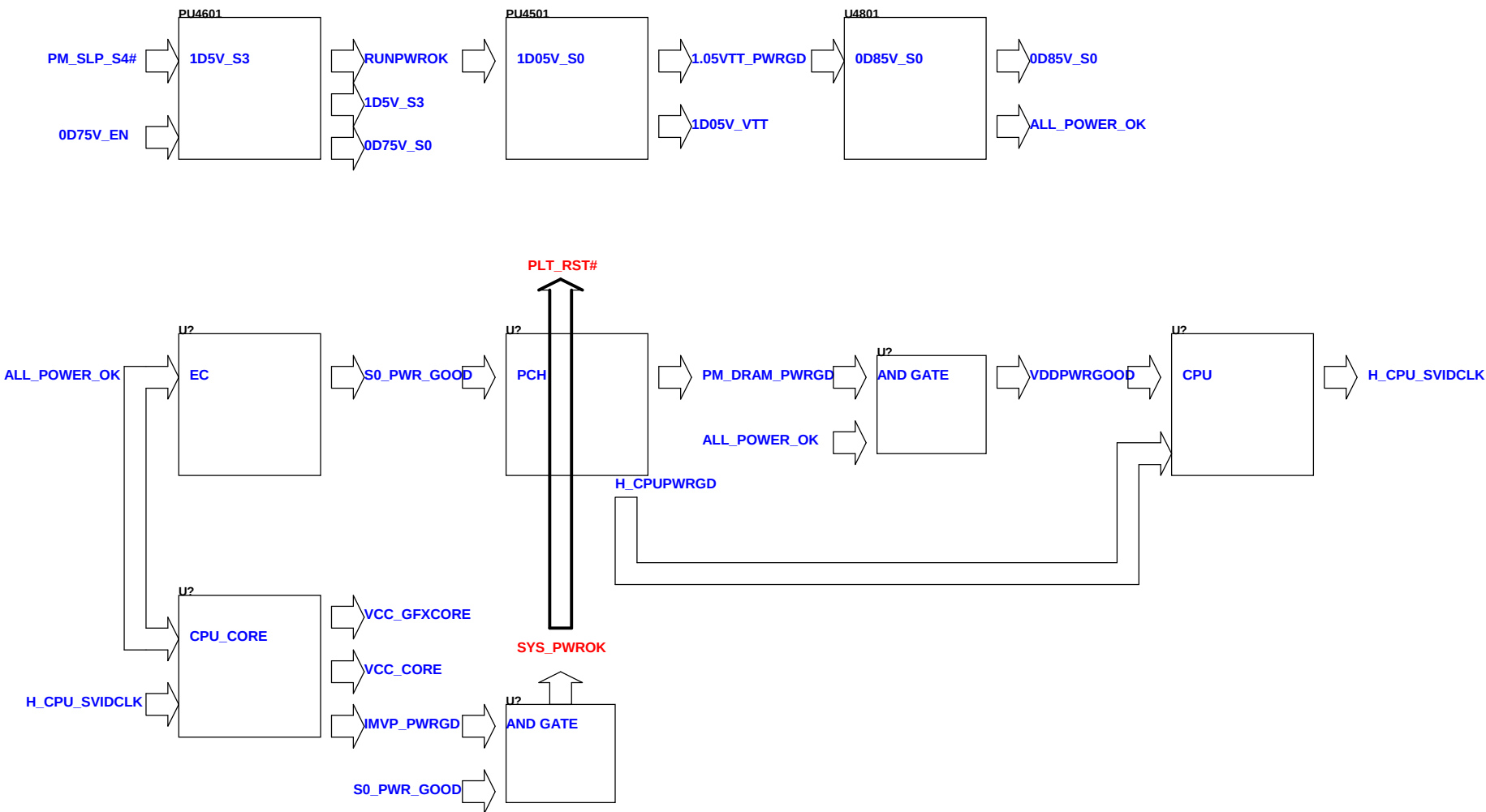
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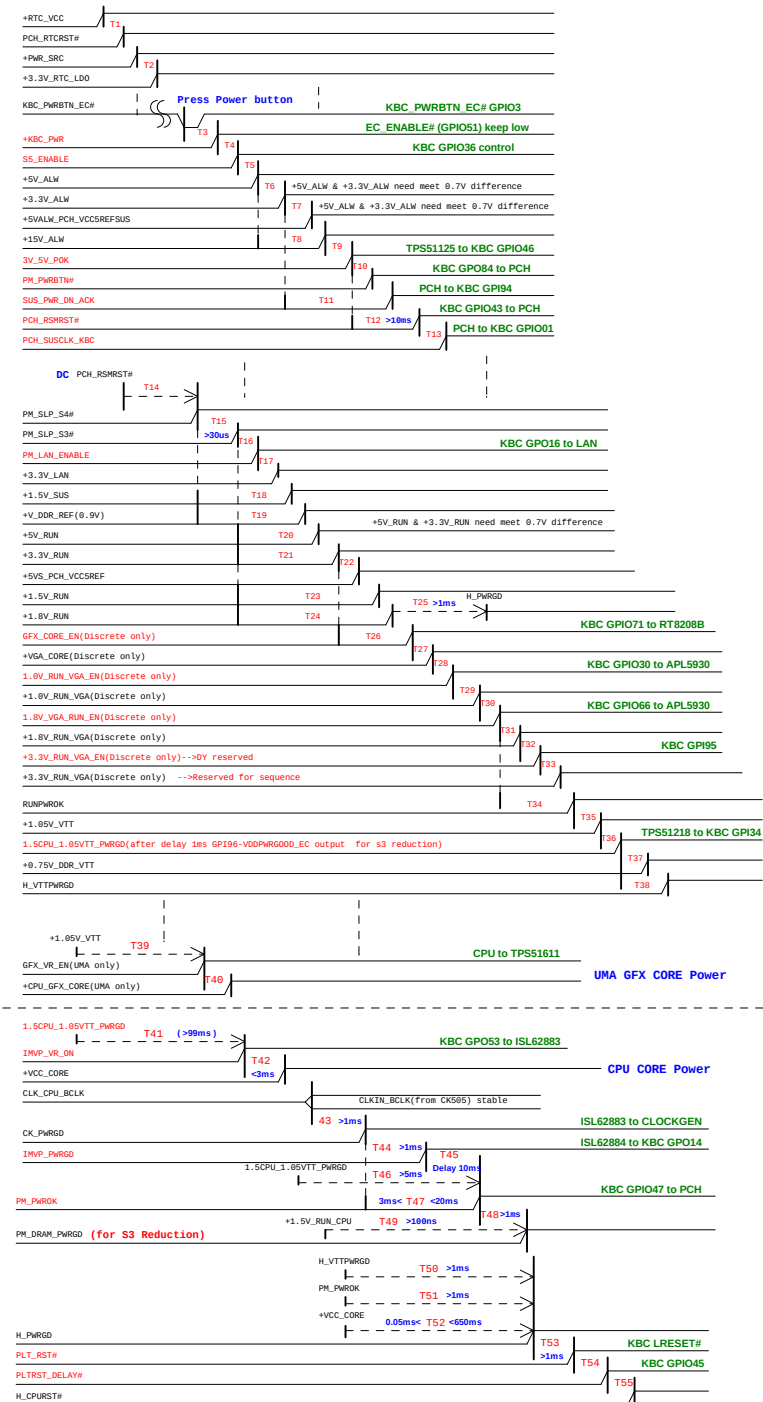
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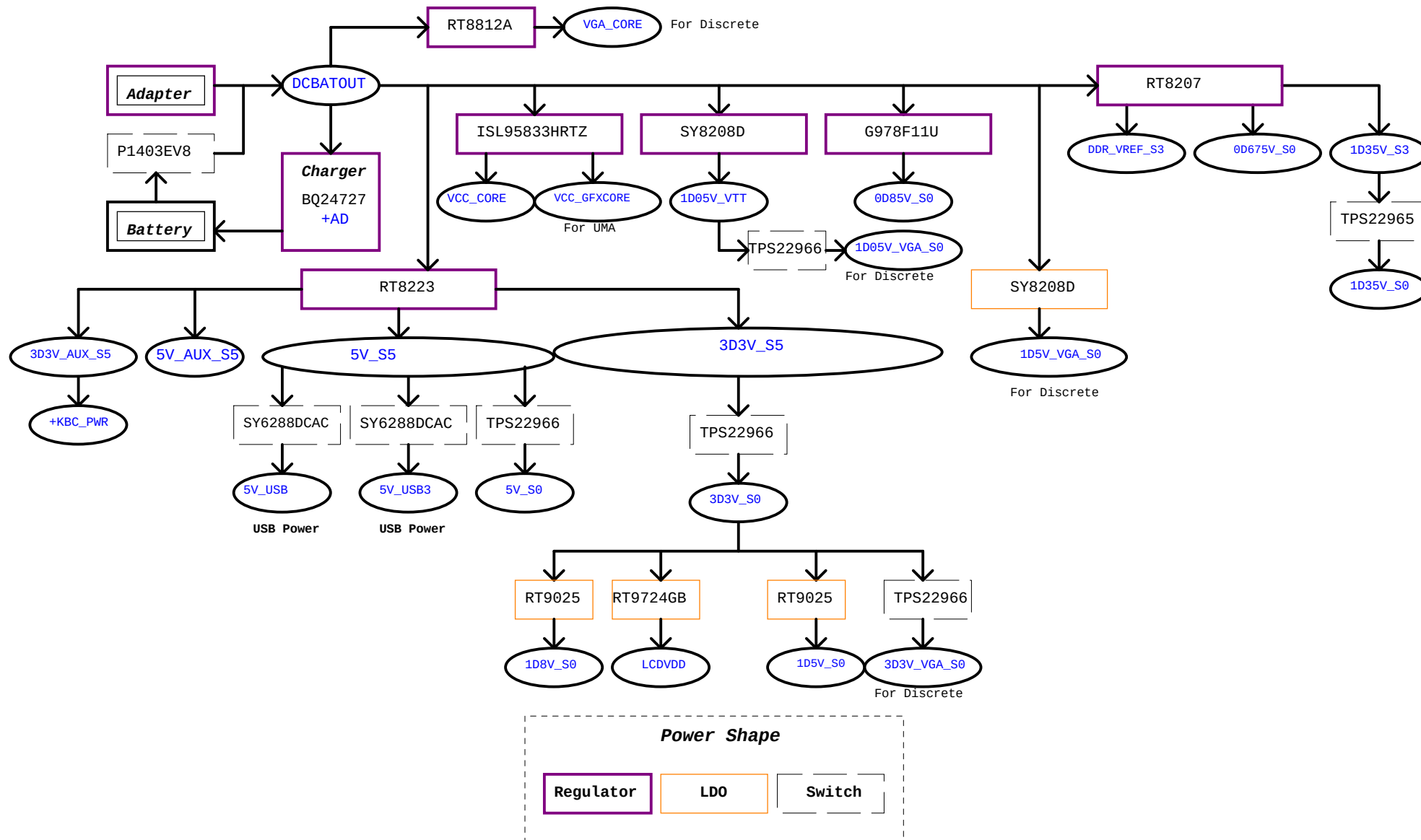


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(AC mode)

red word: KBC GPIO





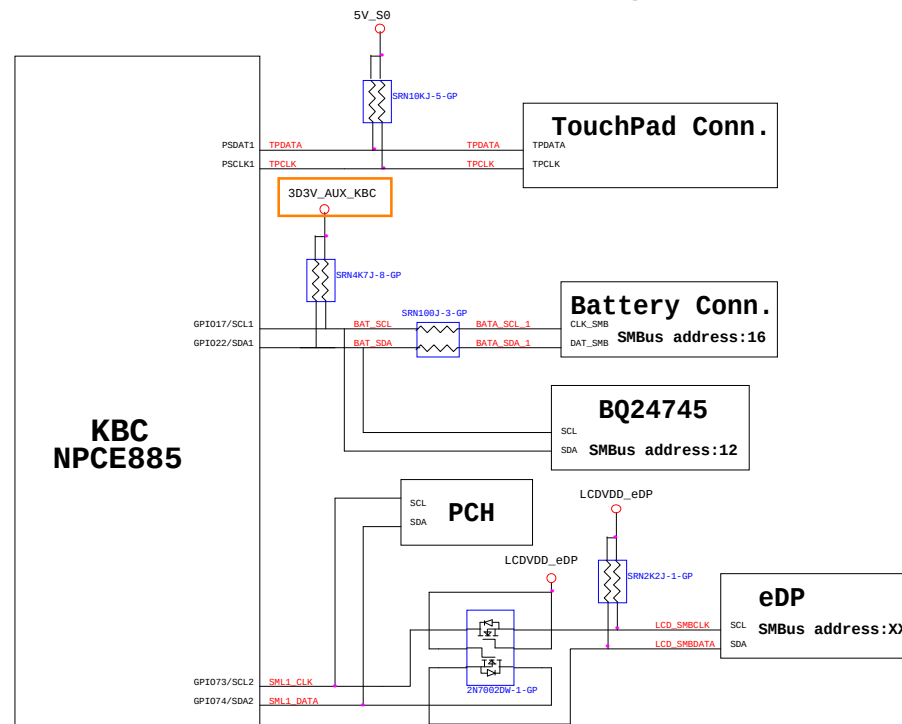
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Title Power Block Diagram	
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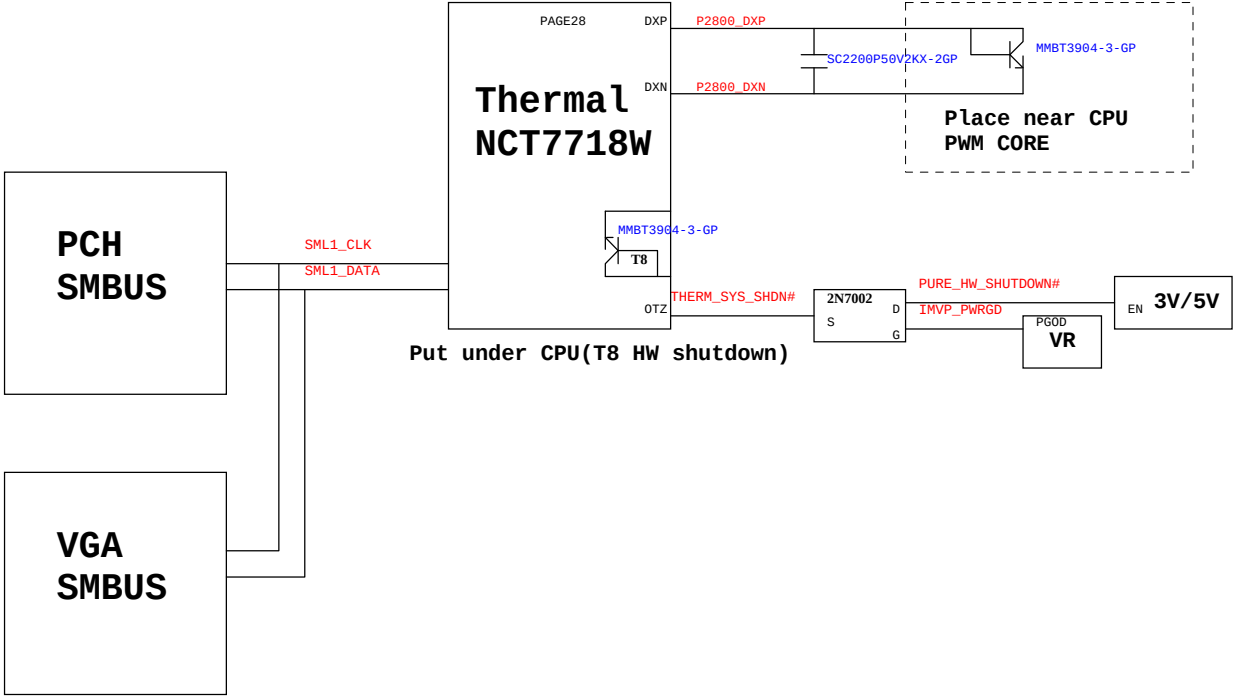
Rev -3

KBC SMBus Block Diagram

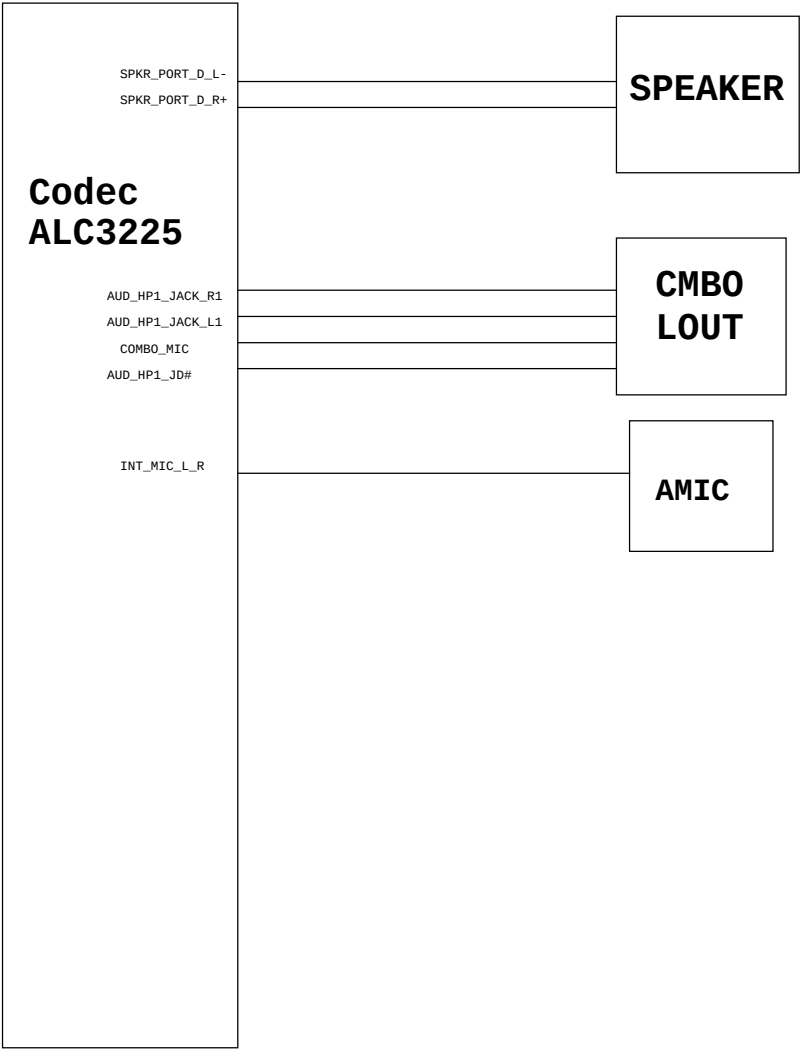


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Title			
SMBUS Block Diagram			
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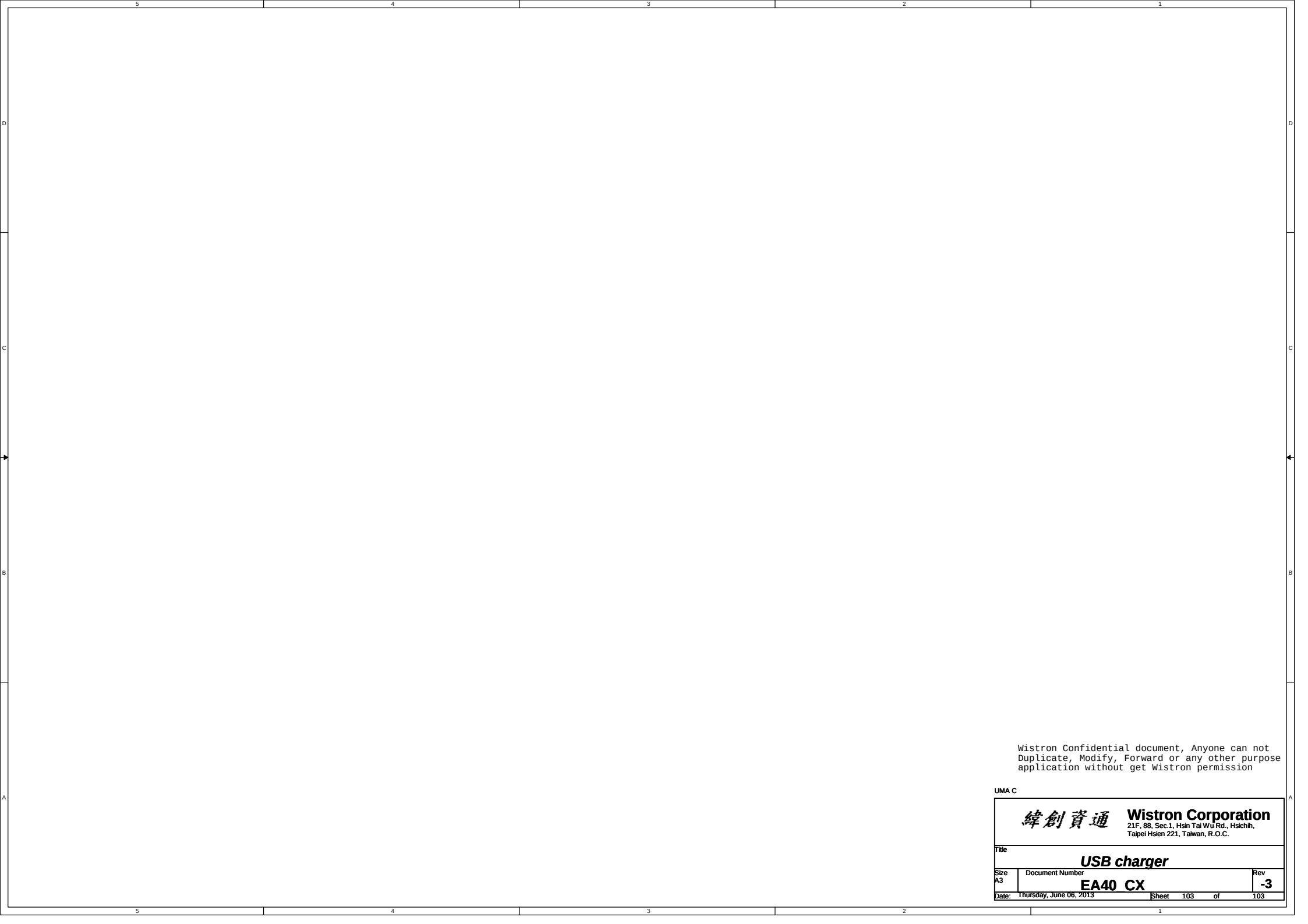
Thermal Block Diagram



Audio Block Diagram

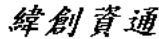


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