

Compal Schematic

HCL51 Schematics Document

Intel Yonah Processor with ATIRC410MD/E + DDRII + SB460M

www.RanAsiaLaptop.com

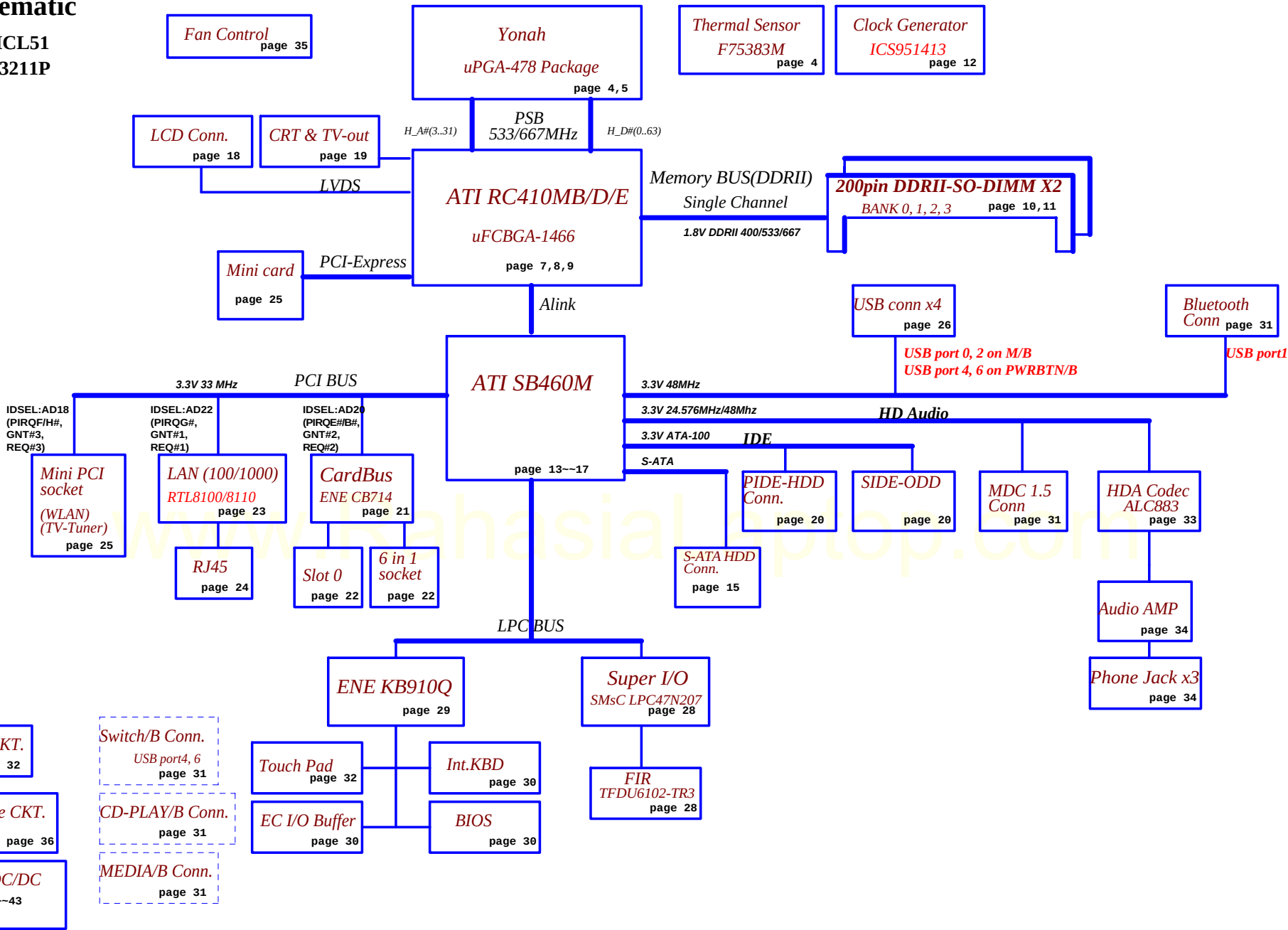
2006-04-05

REV: 1

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Compal Schematic

Model Name : HCL51
File Name : LA-3211P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQE/PIRQH
1394	AD16	0	PIRQA
LAN(10/100)	AD22	1	PIRQG
Mini-PCI(WLAN/TV-Tuner)	AD18	3	PIRQF/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

SB460M SM Bus address

Device	Address
Clock Generator (ICS951413)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra/Rc/Re	100K +/- 5%				
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	
0	0	0 V	0 V	0 V	
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

BOARD ID Table

Board ID	PCB Revision
0	
1	0.2
2	0.2
3	
4	
5	
6	
7	

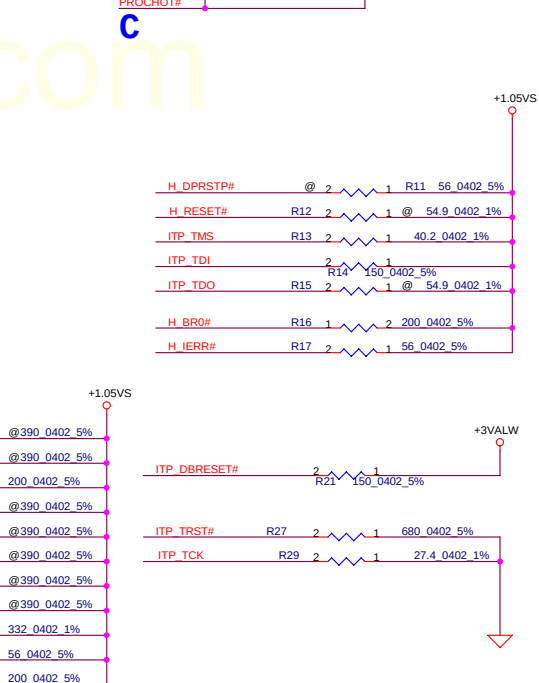
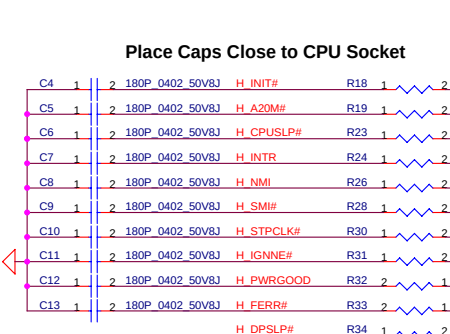
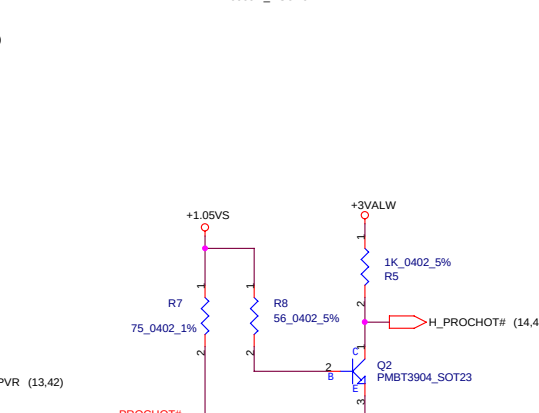
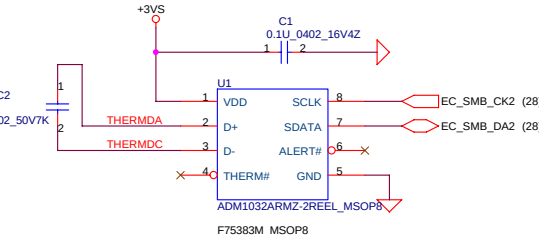
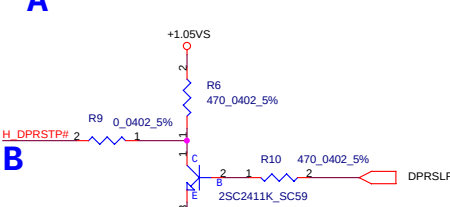
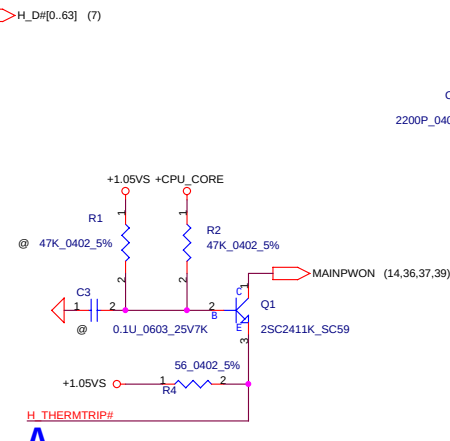
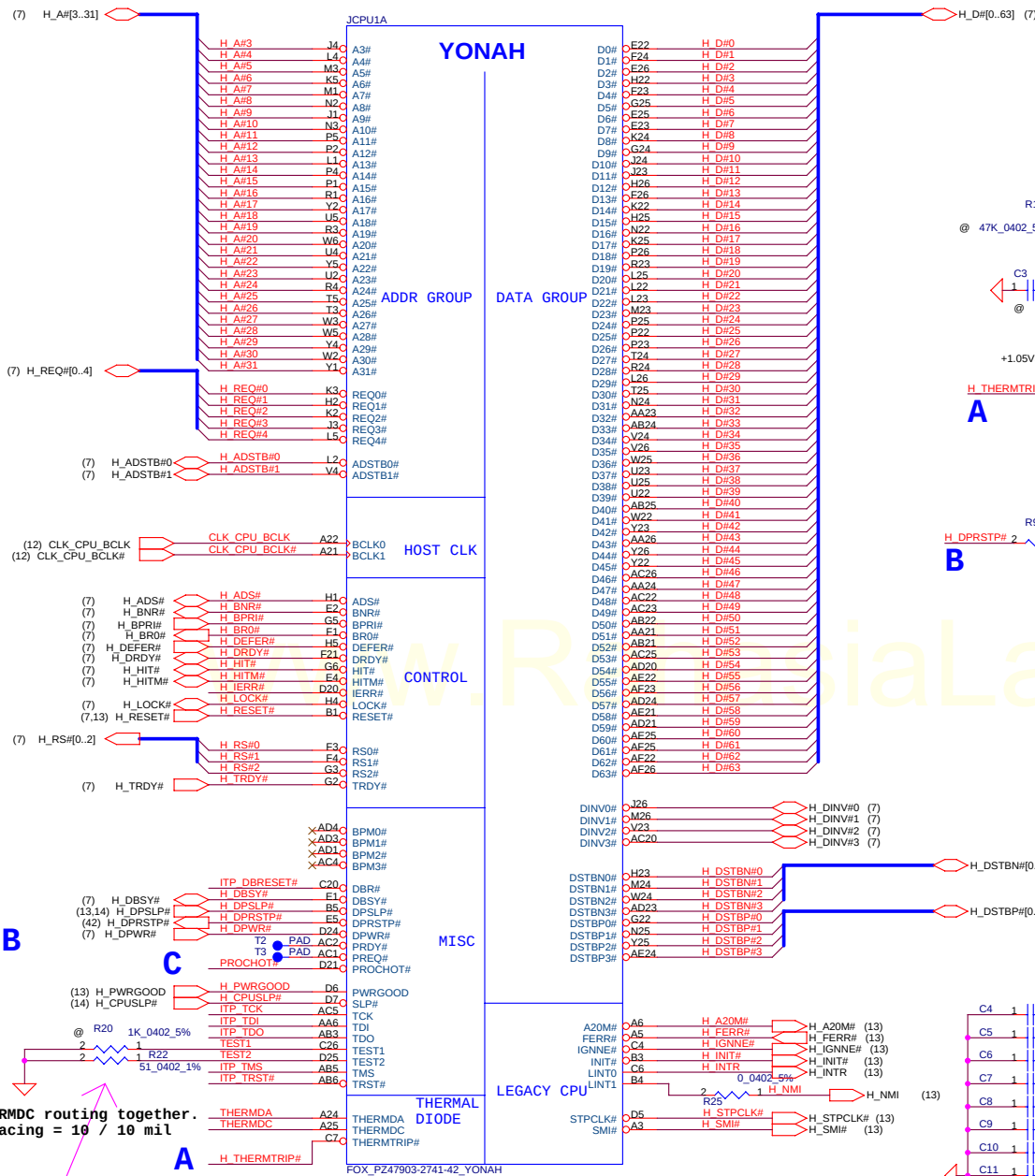
BTO Option Table

BTO Item	BOM Structure
LAN(10/100)	8100C@
LAN(GIGA)	8110S@
FIR	FIR@
MINI_CARD1	MINI1@
SATA_HDD	SATA@
CardReader	4IN1@

SKU ID Table

SKU ID	SKU
0	
1	
2	
3	
4	
5	
6	
7	

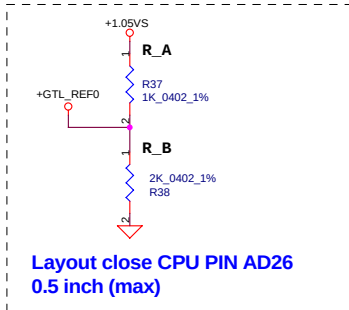
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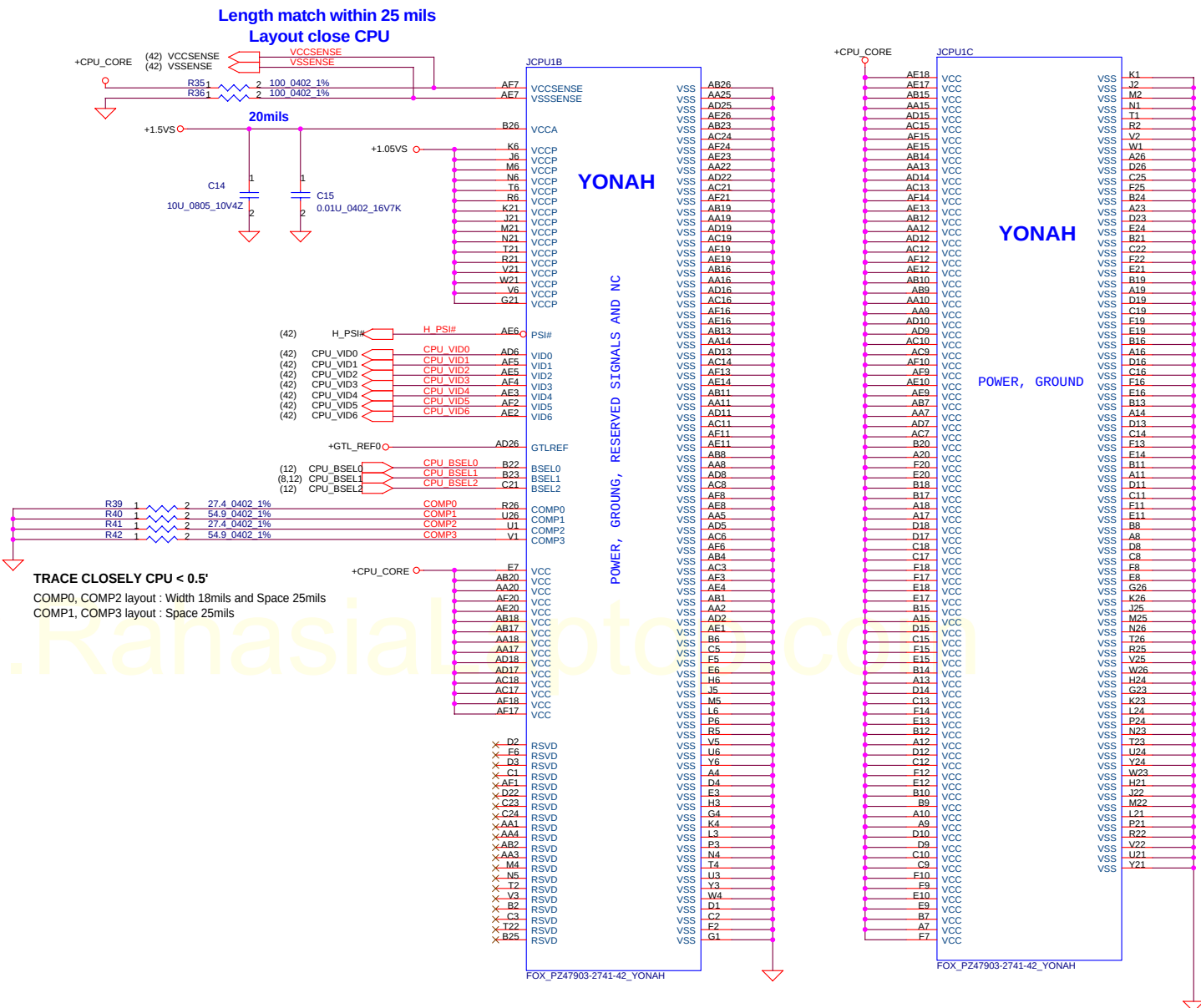
H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil

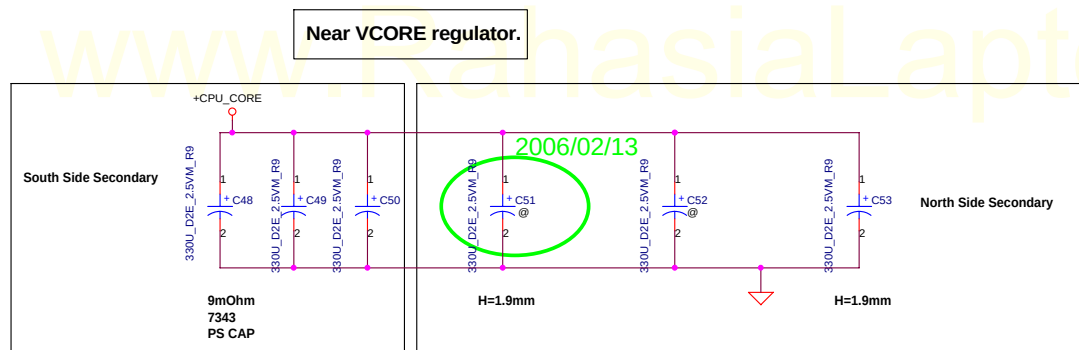
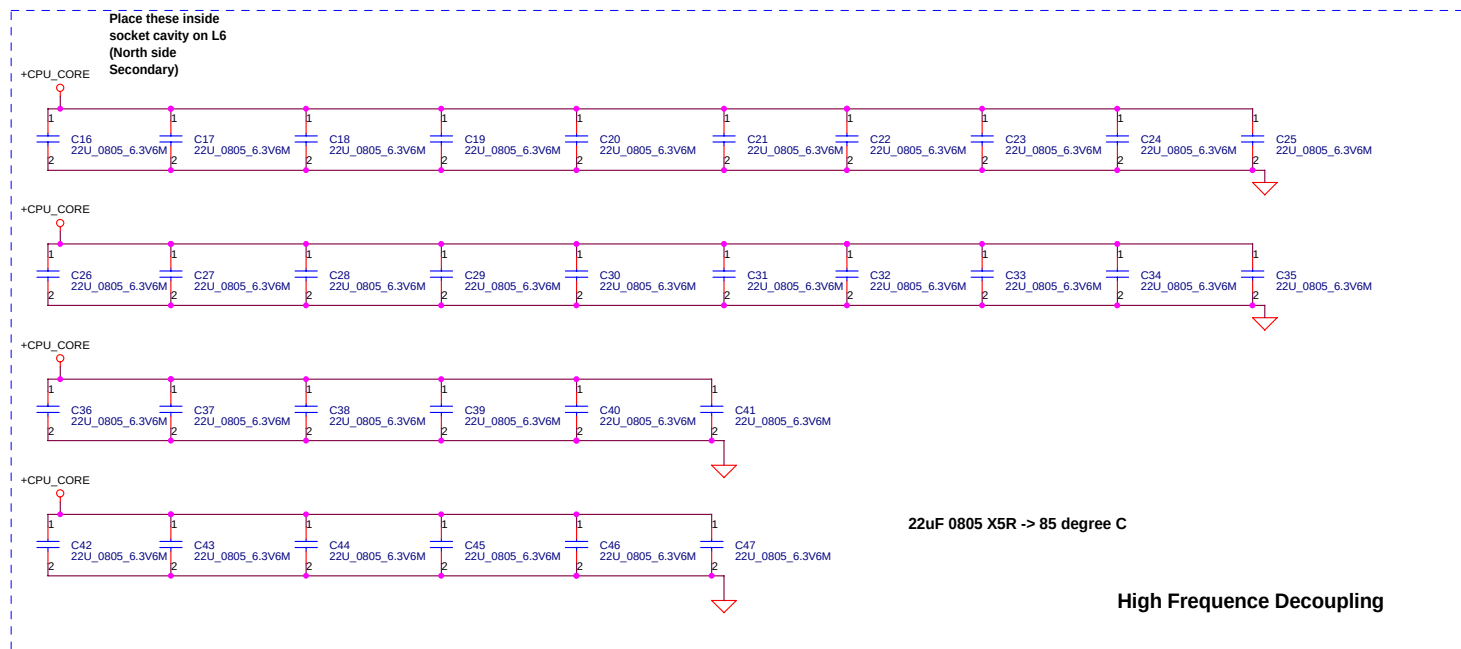
For B-0 stepping engineering samples (ES) of Celeron M processor need to pop this 51 ohm resistor.

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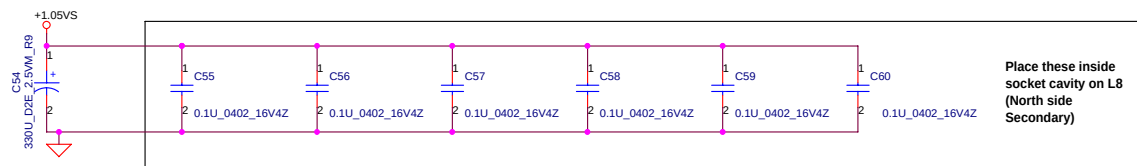


CPU_BSEL	CPU_BSEL0	CPU_BSEL1	CPU_BSEL2
133	0	0	1
166	0	1	1

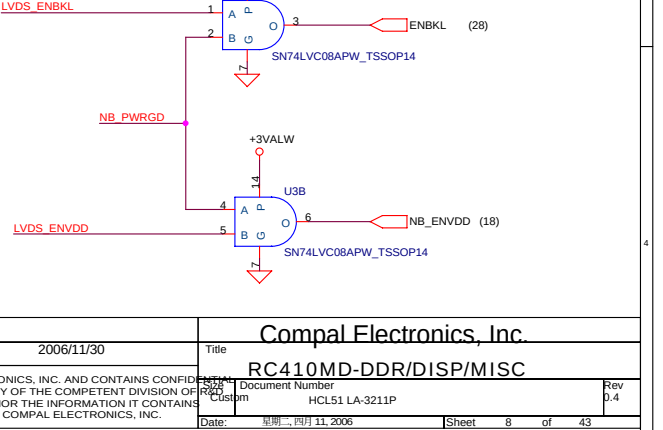
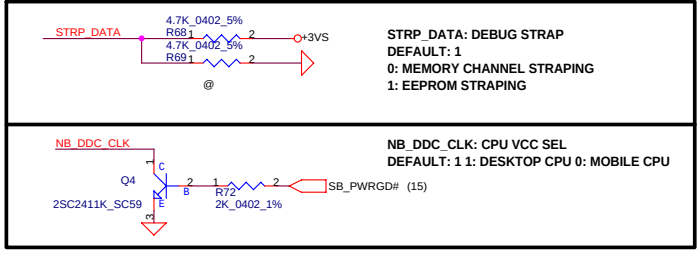
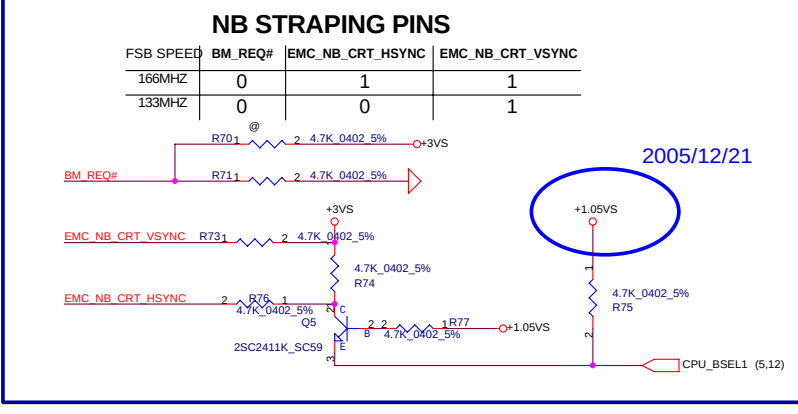
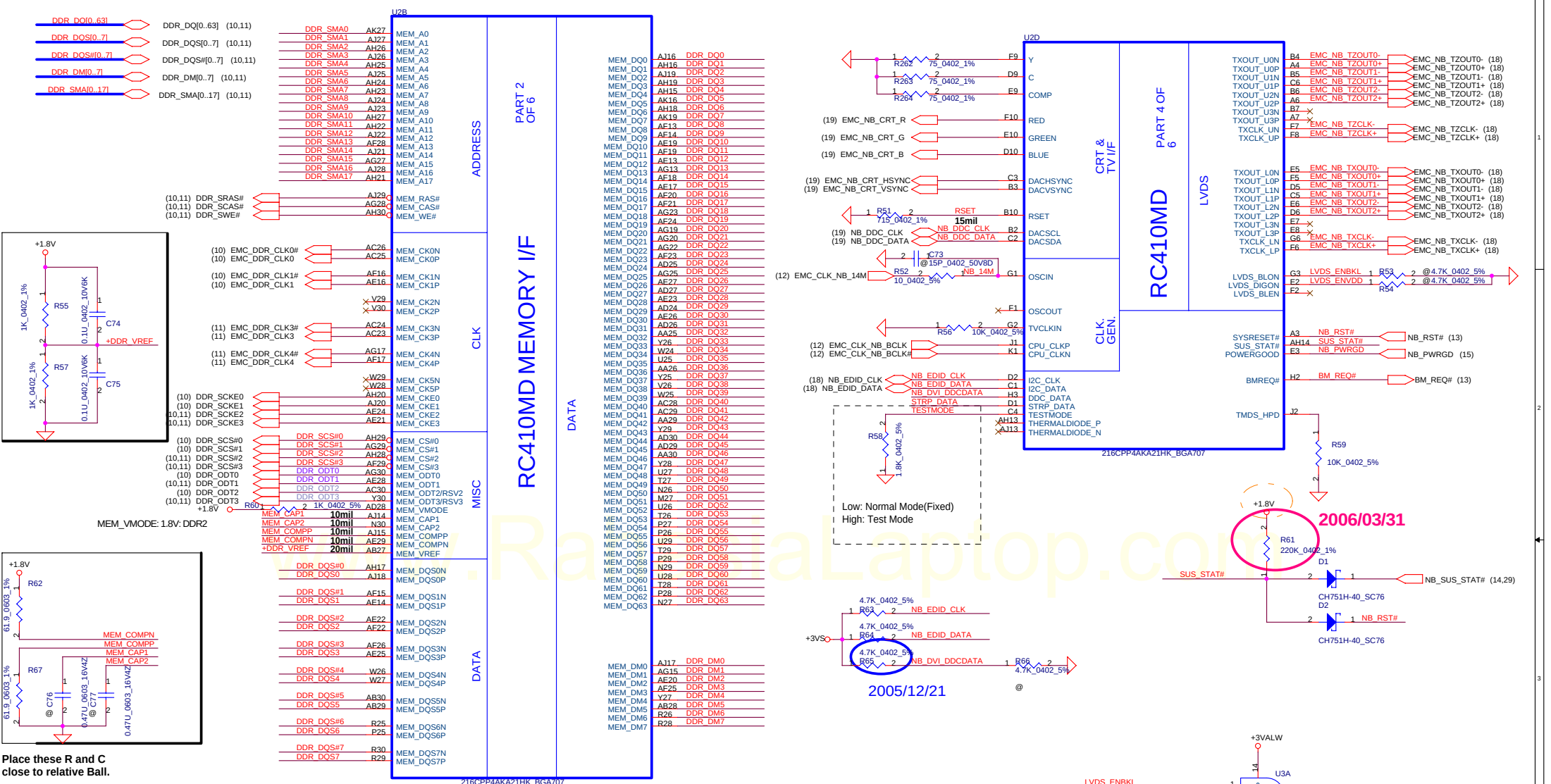




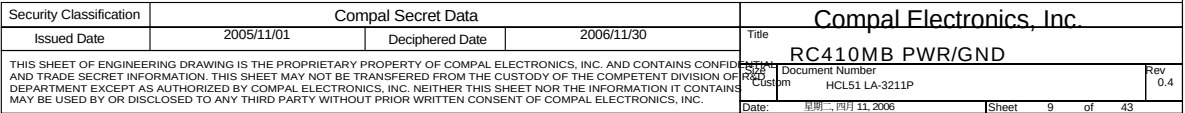
ESR <= 1.5m ohm
Capacitor > 1980uF



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Layout Note:

Place near JDIM1

Layout Note:

Place one cap close to every 2 pullup resistors terminated to V_DDR_MCH_REF

Layout Note:

Every four parallel termination resistors with two caps, one is connected to ground, the other one is connected between +1.8V and +0.9VS. Need to place each parallel resistor with one cap to GND and one cap between +1.8V and +0.9VS

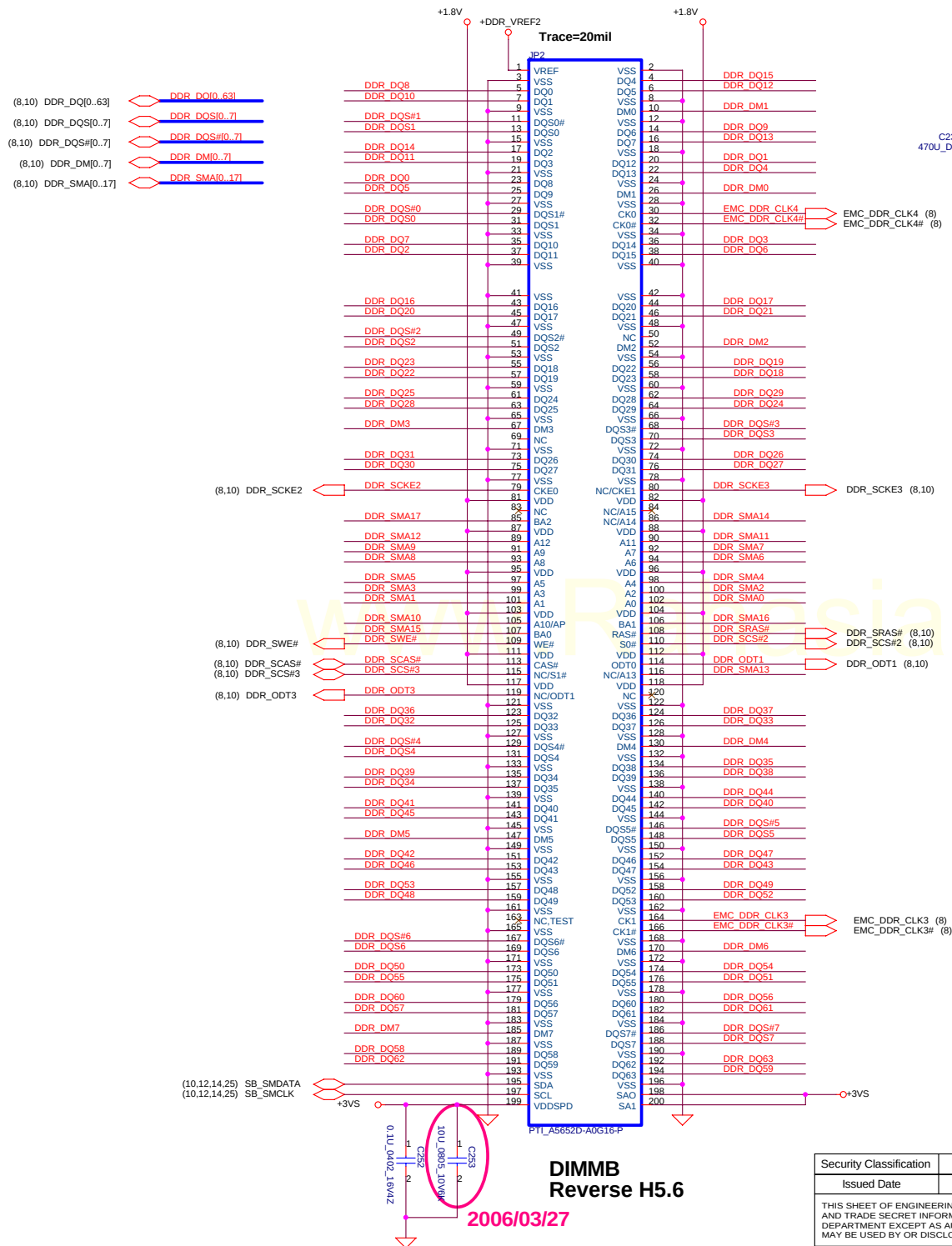
2006/01/23

2005/12/26

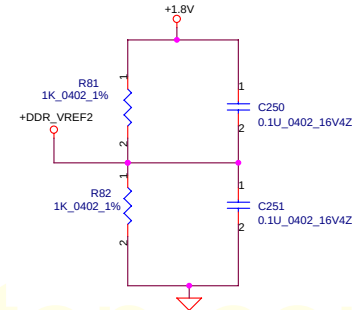
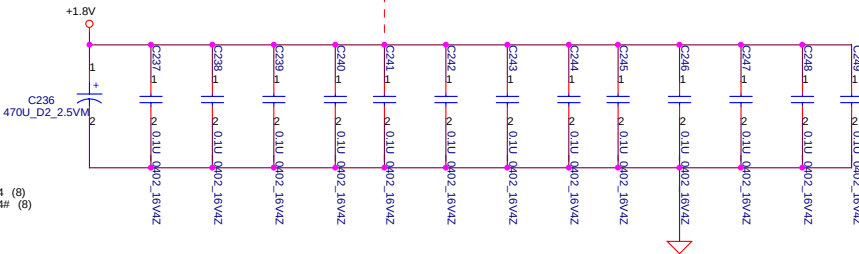
DIMMA
Reverse H9.2

2006/03/27

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Layout Note:
Place near JDIM1



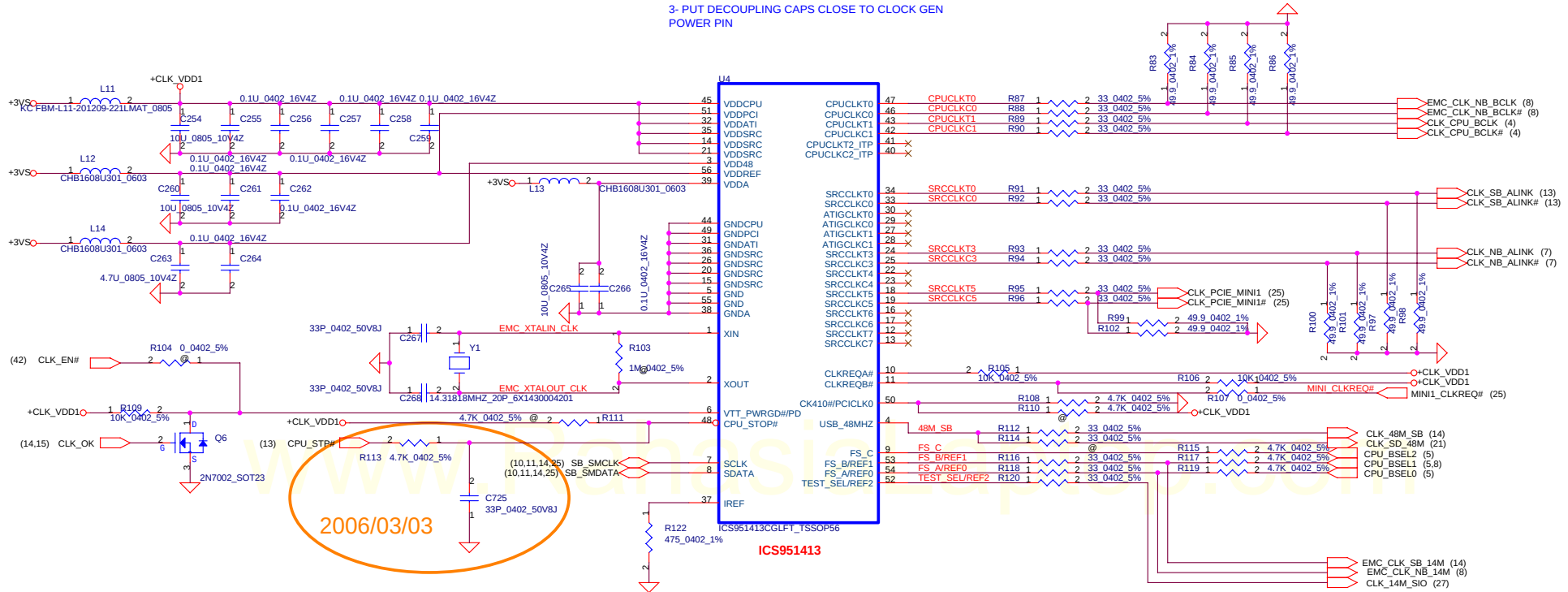
DIMMB
Reverse H5.6

2006/03/27

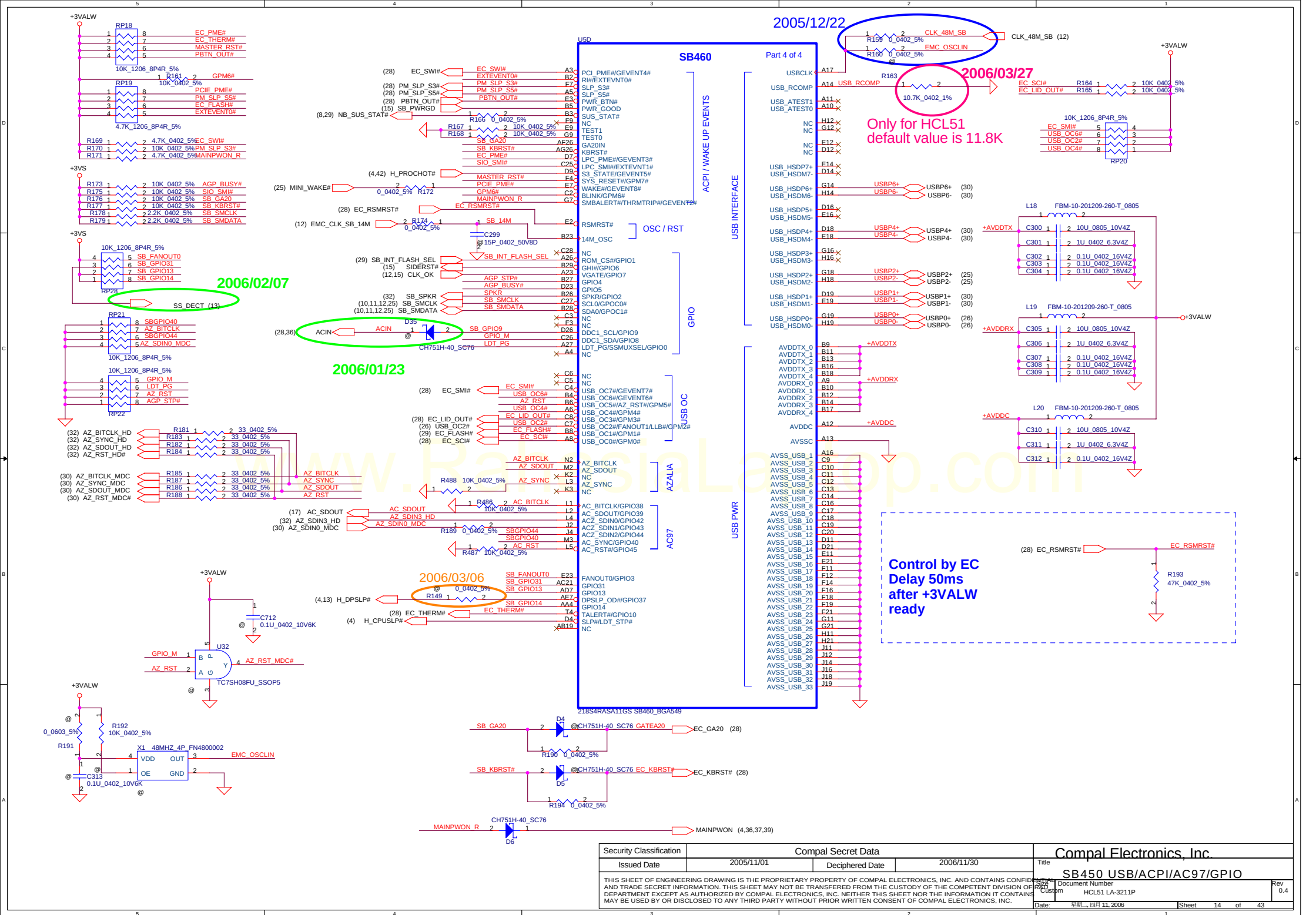
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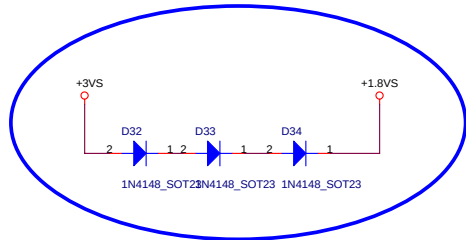
Clock Generator

- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLOCK GEN AS POSSIBLE
- 2- ROUTE ALL CPUCCLK#, NBCLK#, ITPCLK# AND SRCCLK# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN

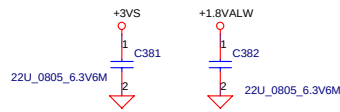


FS_C	FS_B	FS_A	CPU	SRC	PCI	REF	USB
1	0	1	100.00	100.00	33.33	14.318	48.000
0	0	1	133.33	100.00	33.33	14.318	48.000
0	1	1	166.66	100.00	33.33	14.318	48.000

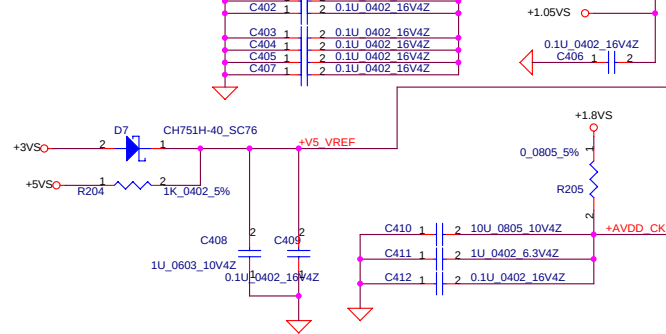




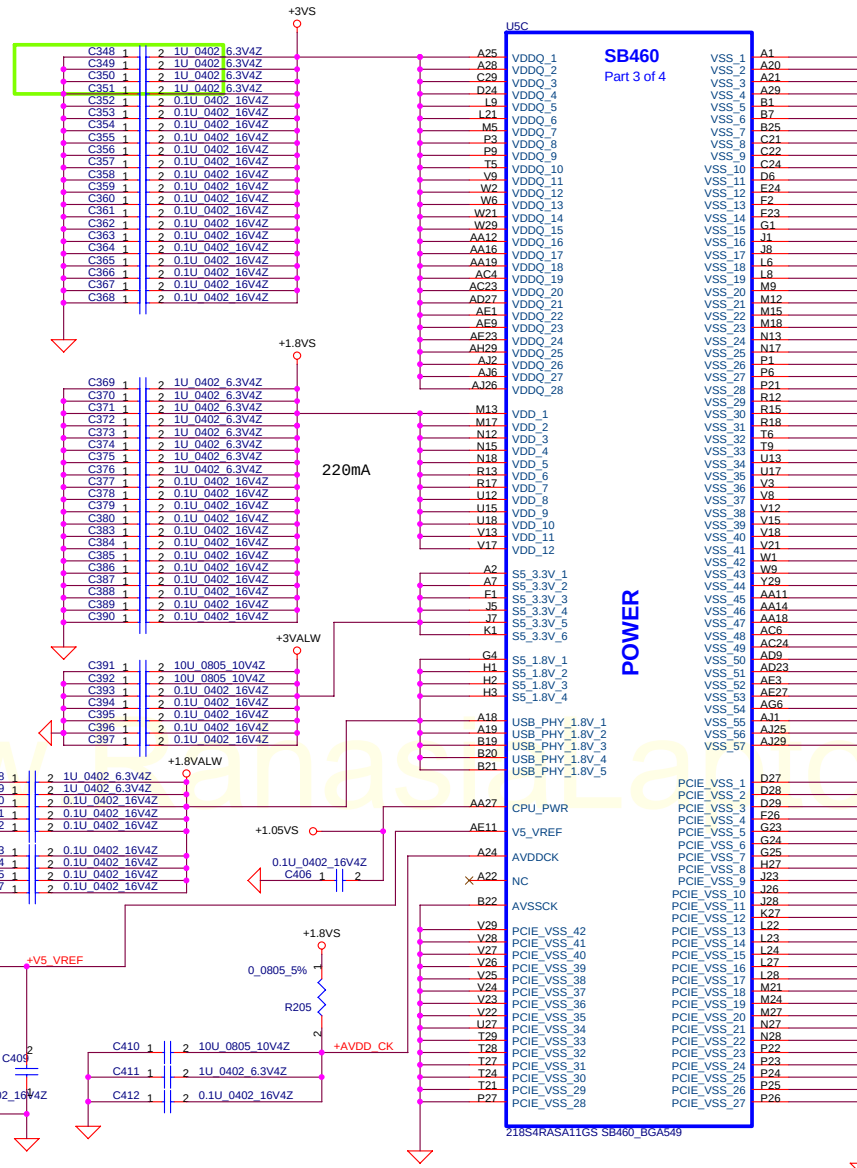
2005/12/21



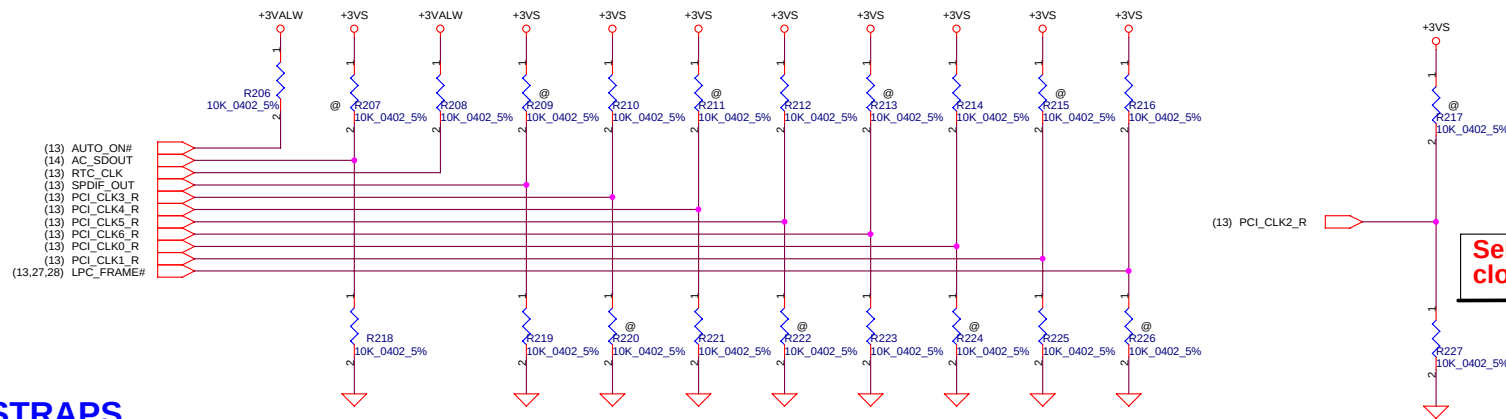
www.analog.com



+V5_VREF (20mils)
+AVDD_CK(40mils)



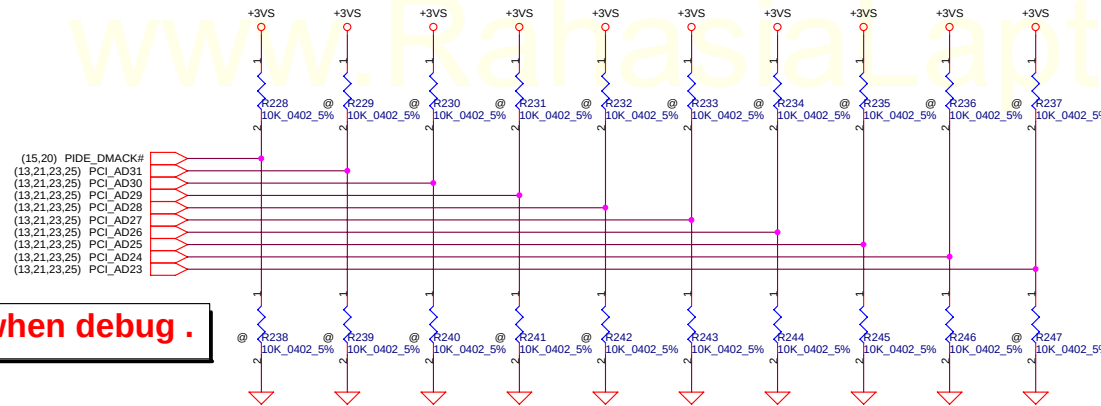
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REQUIRED STRAPS



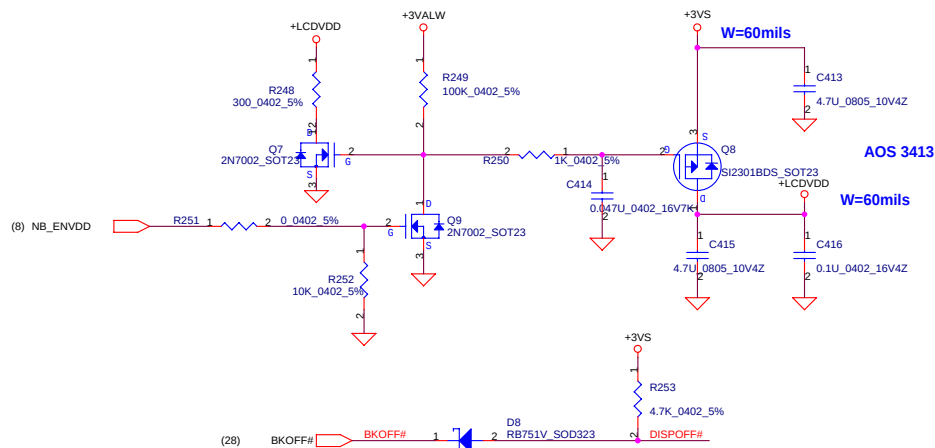
	AUTO_ON#	AC97_SDOUT	RTC_CLK	SPDIF_OUT	CLK_PCI3	CLK_PCI4	CLK_PCI5	PCI_CLK6	PCI_CLK0	PCI_CLK1	LFRAME#	CLK_PCI2
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	PU for 48Mhz XTAL mode DEFAULT	USB PHY PWRDOWN DISABLE DEFAULT	Internal PLL	PCIE AUTO detect DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = LPC ROM I L,L = FWH ROM	THERMTRIP# ENABLE DEFAULT		Crystal Pad
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	48M OSC mode DEFAULT	USB PHY PWRDOWN ENABLE	External Clock DEFAULT	Forcing PCIE to 2 lanes (debug only)	CPU I/F = P4 DEFAULT		THERMTRIP# DISABLE		Clock input buffer DEFAULT



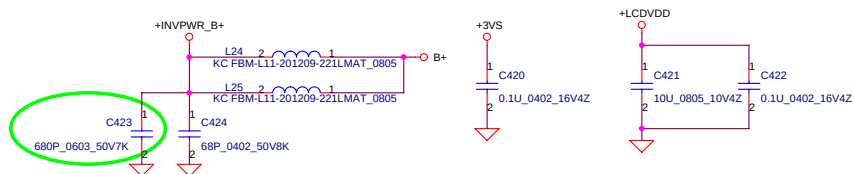
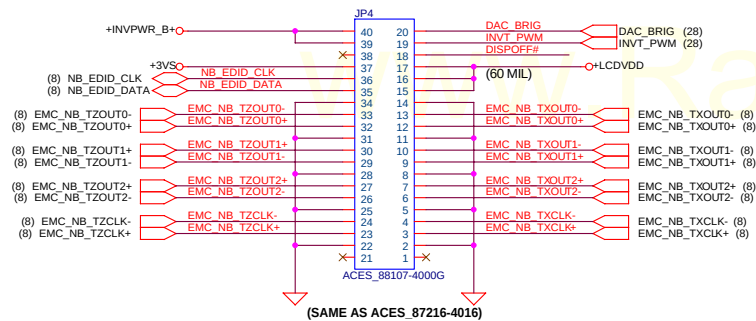
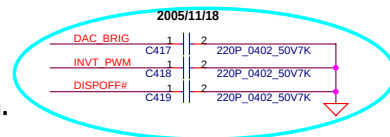
DEBUG STRAPS

	PIDE_DMACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS	

LCD POWER CIRCUIT

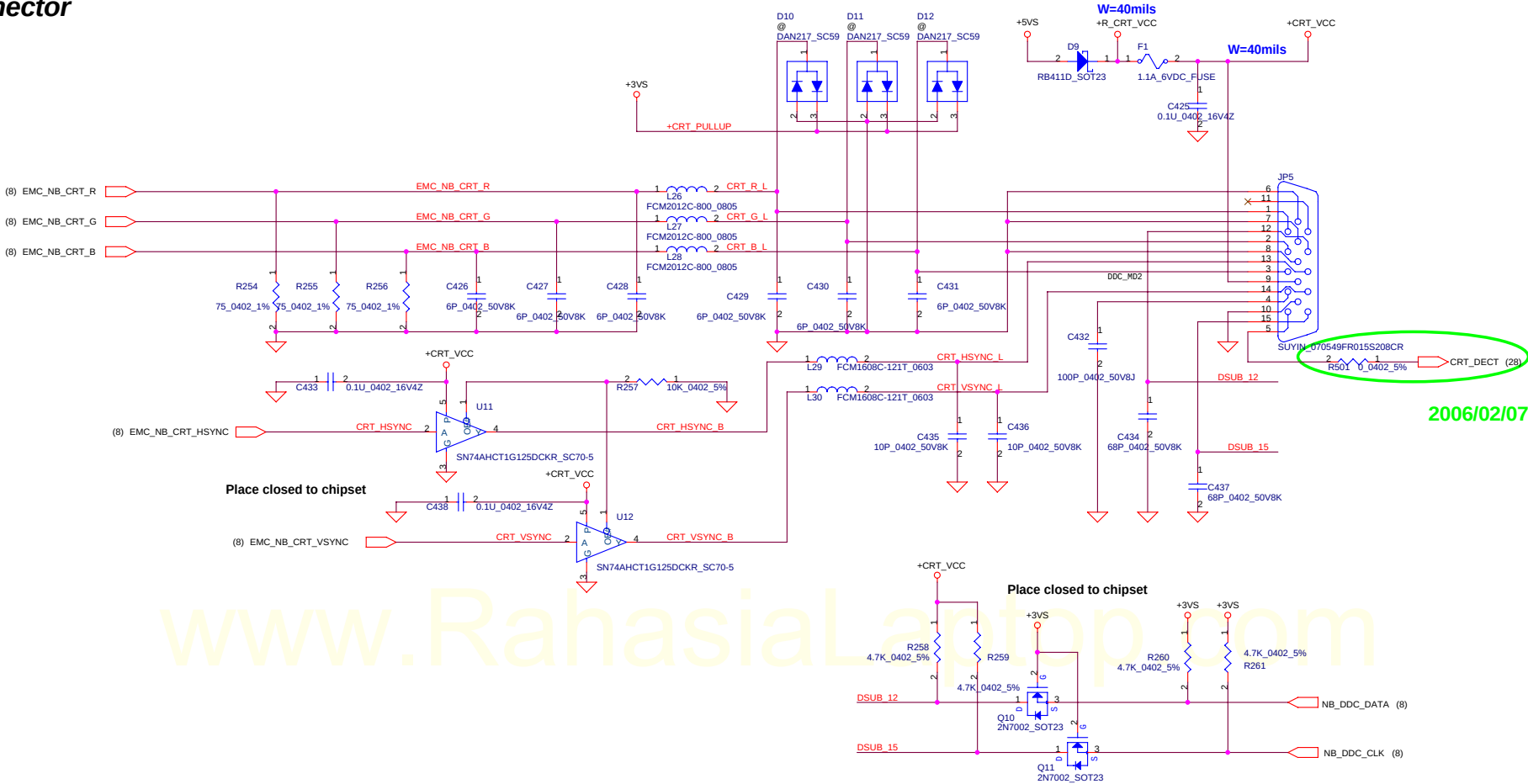


LCD/PANEL BD. Conn.

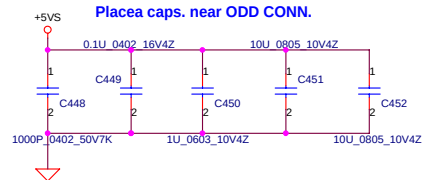


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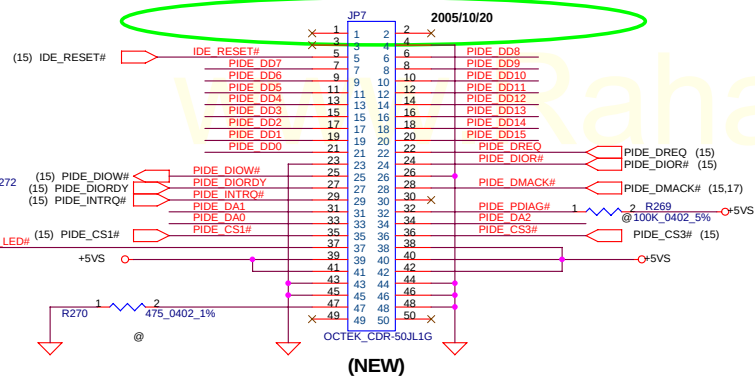
CRT Connector



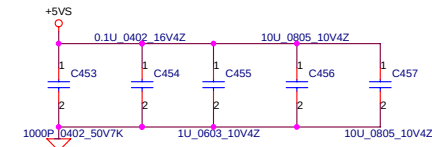
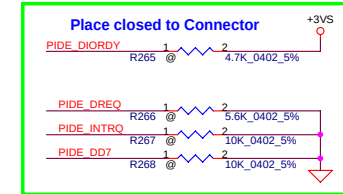
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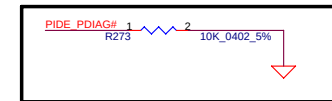
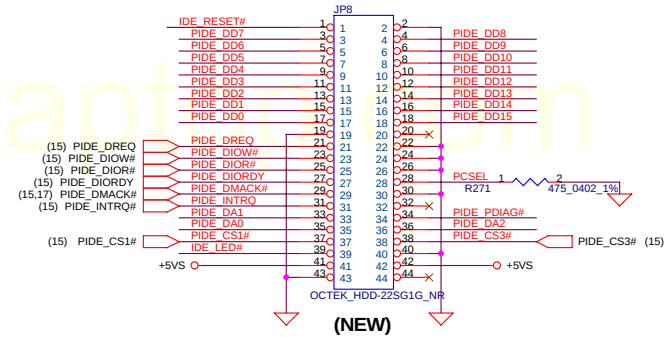
ODD Conn.



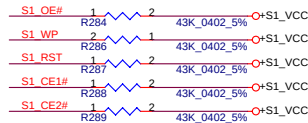
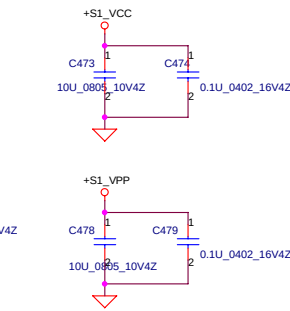
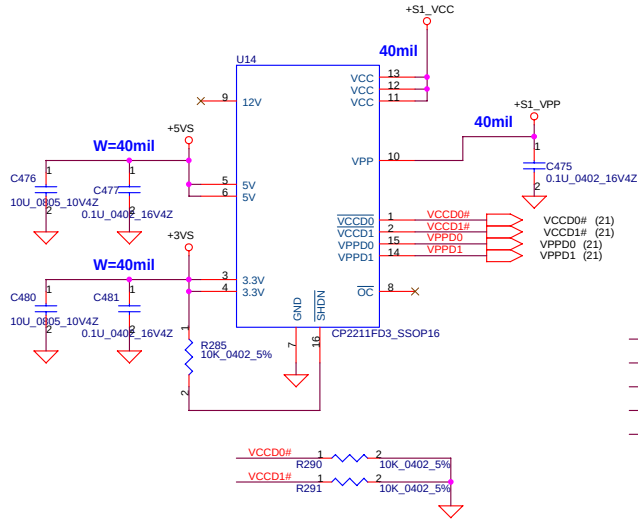
(15) PIDE_DA[0..2] $\Rightarrow$ PIDE_DAI[0..2]
 (15) PIDE_DD[0..15] $\Rightarrow$ PIDE_DD[0..15]



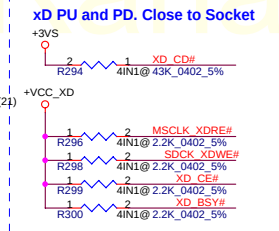
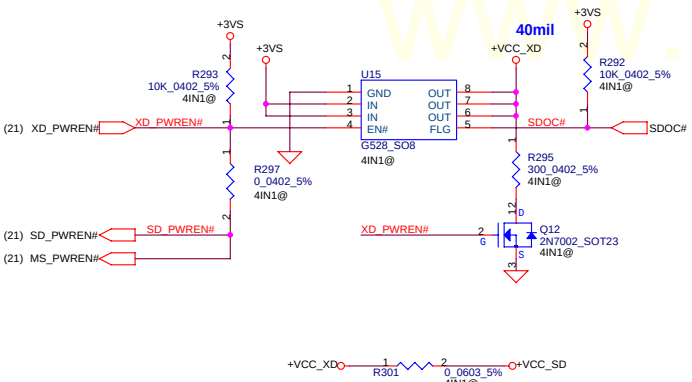
PATA HDD Conn.



PCMCIA Power Control



SD/MS Power Control XD Power Control



(13,17,21,25,31) PCI_AD[0..31]

PCI AD0 104
PCI AD1 103
PCI AD2 102
PCI AD3 98
PCI AD4 97
PCI AD5 96
PCI AD6 95
PCI AD7 93
PCI AD8 90
PCI AD9 89
PCI AD10 87
PCI AD11 86
PCI AD12 85
PCI AD13 83
PCI AD14 82
PCI AD15 79
PCI AD16 58
PCI AD17 57
PCI AD18 55
PCI AD19 53
PCI AD20 51
PCI AD21 49
PCI AD22 47
PCI AD23 43
PCI AD24 42
PCI AD25 40
PCI AD26 37
PCI AD27 36
PCI AD28 34
PCI AD29 33
PCI AD30 33
PCI AD31 33

IDSEL:AD22
(PIRQG#,
GNT#1,
REQ#1)

(13,21,25,31) PCI_CBE#0
(13,21,25,31) PCI_CBE#1
(13,21,25,31) PCI_CBE#2
(13,21,25,31) PCI_CBE#3

PCI AD22 46
LAN IDSEL 46

(13,21,25) PCI_PAR 61
(13,21,25,31) PCI_FRAME# 63
(13,21,25) PCI_IRDY# 67
(13,21,25,31) PCI_TRDY# 68
(13,21,25) PCI_DEVSEL# 69
(13,21,25) PCI_STOP# 69

(13,21,25) PCI_PERR# 70
(13,21,25) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

(13) PCI_PERR# 70
(13) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

(13) PCI_PERR# 70
(13) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

(13) PCI_PERR# 70
(13) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

(13) PCI_PERR# 70
(13) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

(13) PCI_PERR# 70
(13) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

(13) PCI_PERR# 70
(13) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

(13) PCI_PERR# 70
(13) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

(13) PCI_PERR# 70
(13) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

(13) PCI_PERR# 70
(13) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

(13) PCI_PERR# 70
(13) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

(13) PCI_PERR# 70
(13) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

(13) PCI_PERR# 70
(13) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

(13) PCI_PERR# 70
(13) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

(13) PCI_PERR# 70
(13) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

(13) PCI_PERR# 70
(13) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

(13) PCI_PERR# 70
(13) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

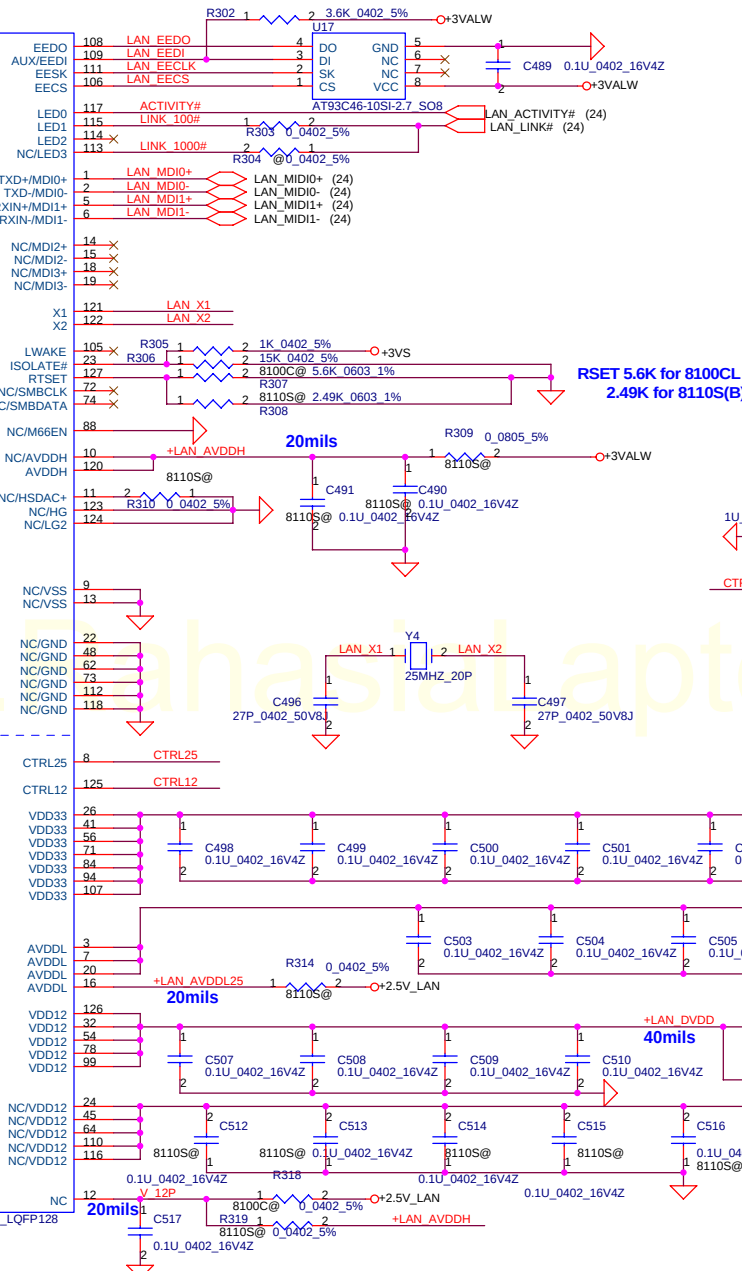
(13) PCI_PERR# 70
(13) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

(13) PCI_PERR# 70
(13) PCI_SERR# 75
(13) PCI_REQ#1 30
(13) PCI_GNT#1 29

PCI I/F

LAN I/F

Power



PIN	8100CL(10/100 LAN)	8110SBL(10/100/1000 LAN)
RSET	5.6K	2.49K

BOM structure	8100CL(10/100 LAN)	8110SBL(10/100/1000 LAN)
8100C@	Stuff	No_Stuff
8110S@	No_Stuff	Stuff
@	No_Stuff	No_Stuff

RTL8110SBL change to Ver.D

8100CL(10/100 LAN) P/N:SA081000310 ver.A.2

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				Date: 星期三, 四月 11, 2006	Sheet 23 of 43

6V4Z

C528

0.1uF 0402 16V4Z

R345 MDI3+ R334 1 2 0 0402 5%

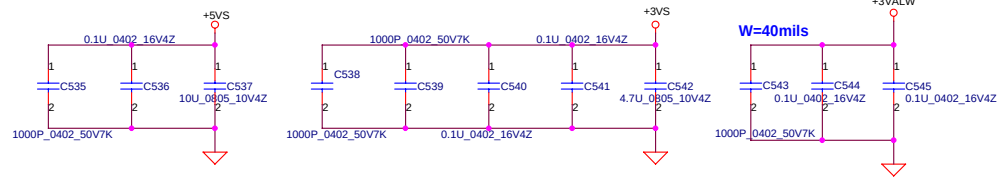
R345 MDI3- R335 1 2 0 0402 5%

(23) LAN_LINK#

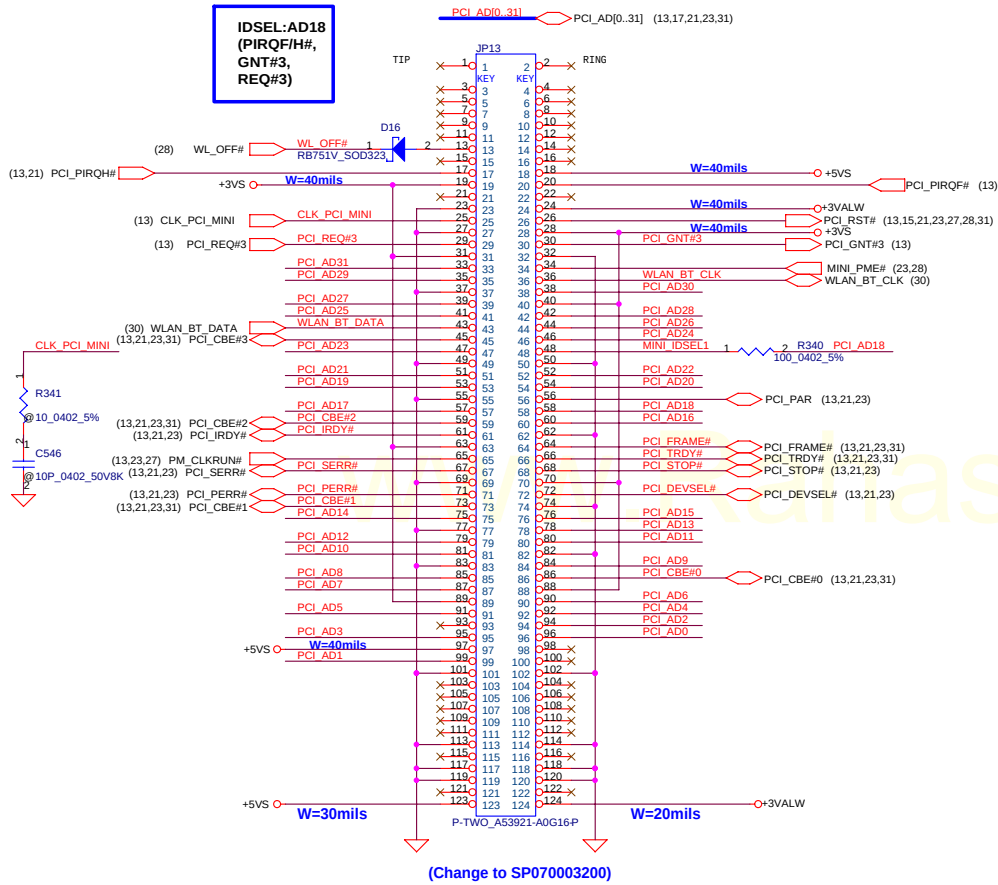
+3VALW R327



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						Part Number		Document Number		Rev	
						HCL51 LA-3211P		0.4			
Date: 星期二, 四月 11, 2006						Sheet 24 of 43					

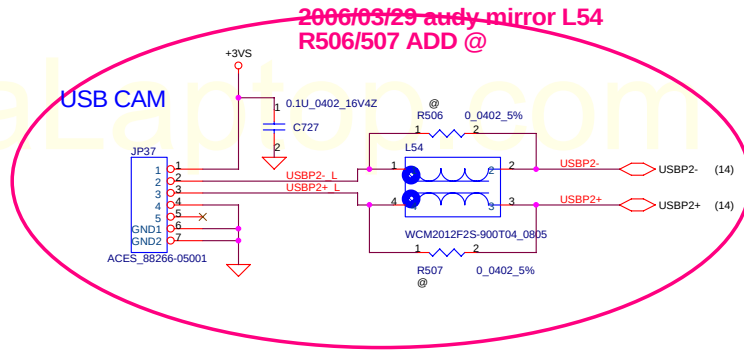
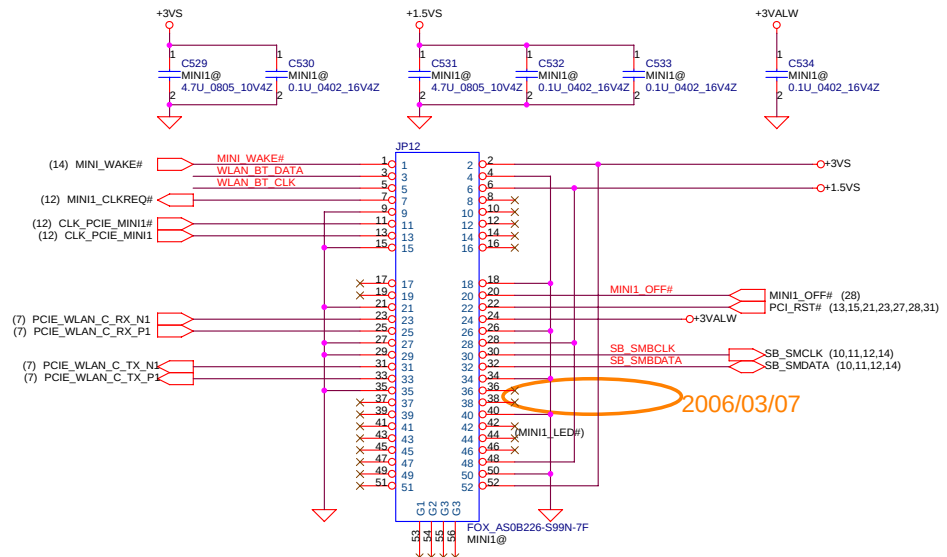


**IDSEL:AD18
(PIRQ#IH#,
GNT#3,
REQ#3)**



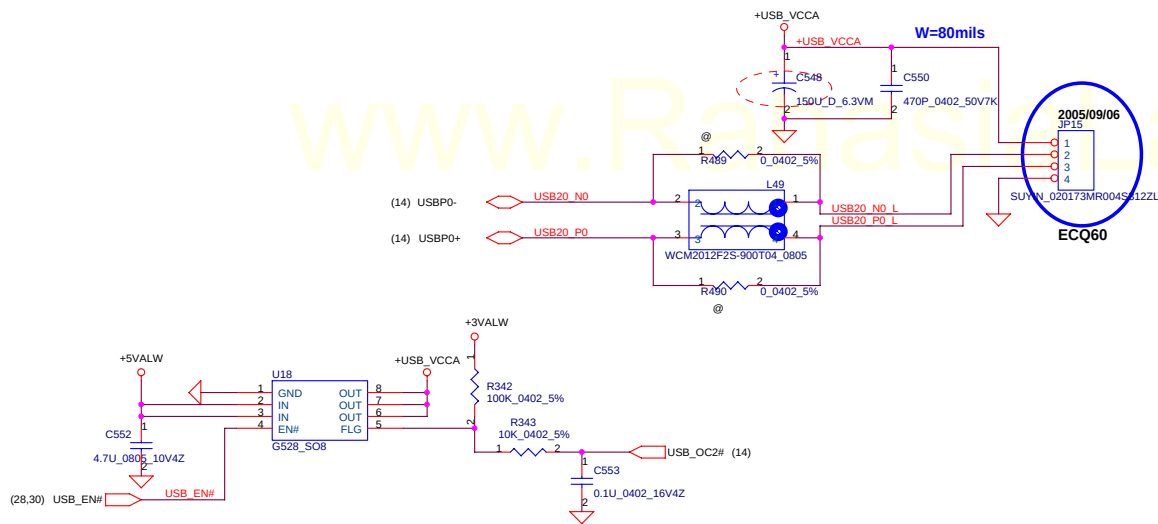
(Change to SP070003200)

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



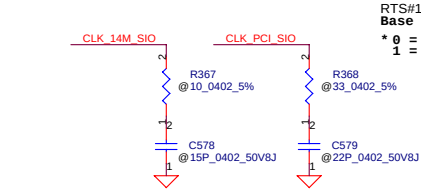
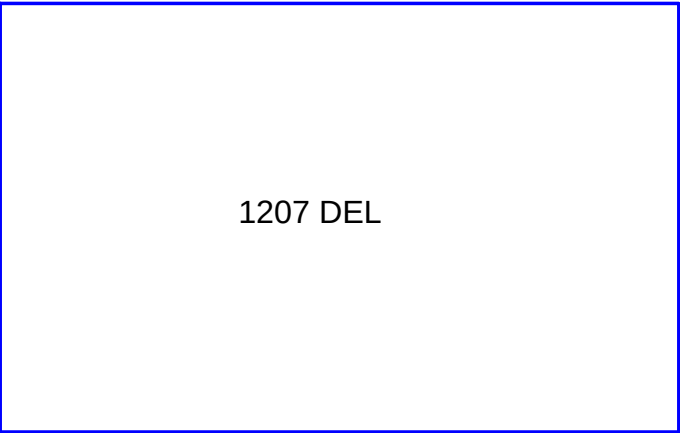
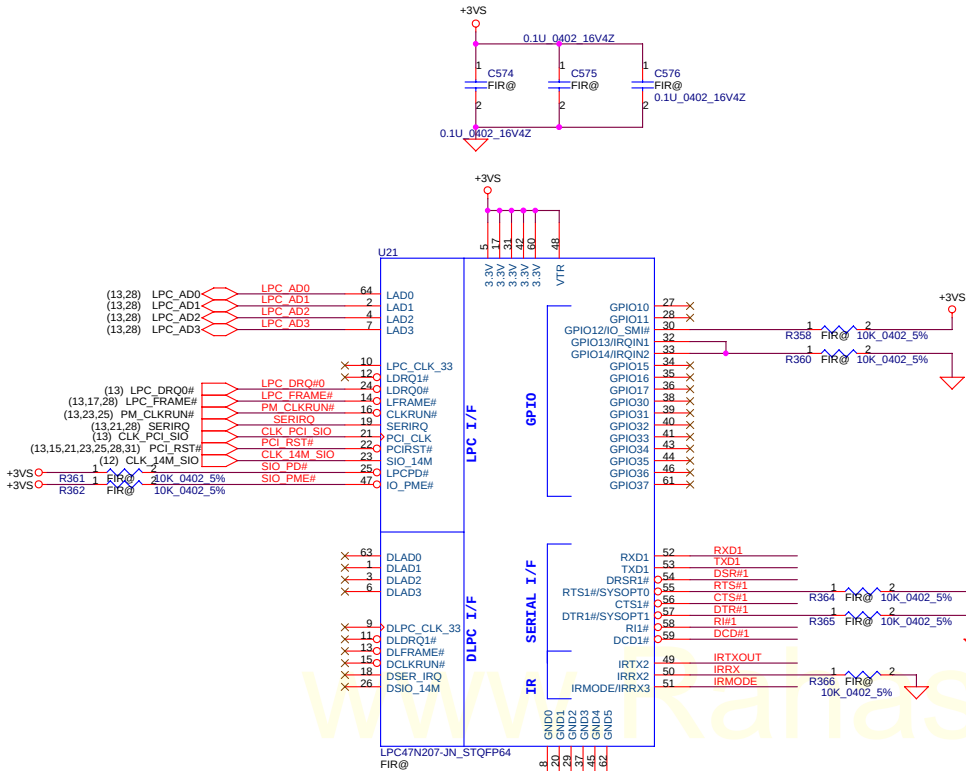
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Document Number				HCL51 LA-3211P	
Date: 星期二, 四月 11, 2006				Rev 0.4	
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USB CONN. 1 & 2

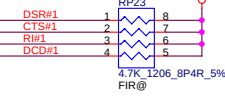
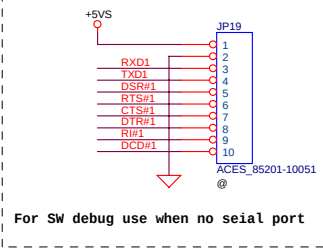


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				Date: 星期二, 四月 11, 2006
				Sheet 26 of 43

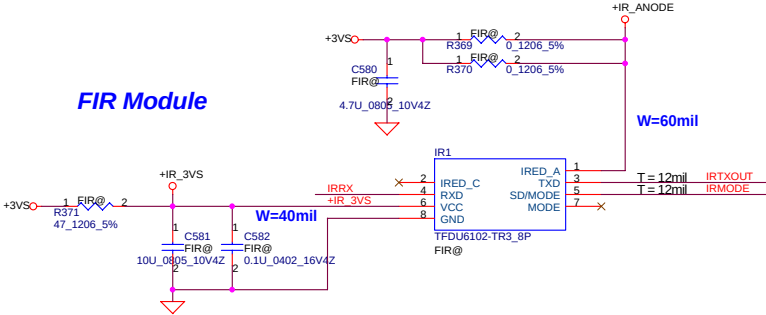
SUPER I/O SMSc LPC47N207



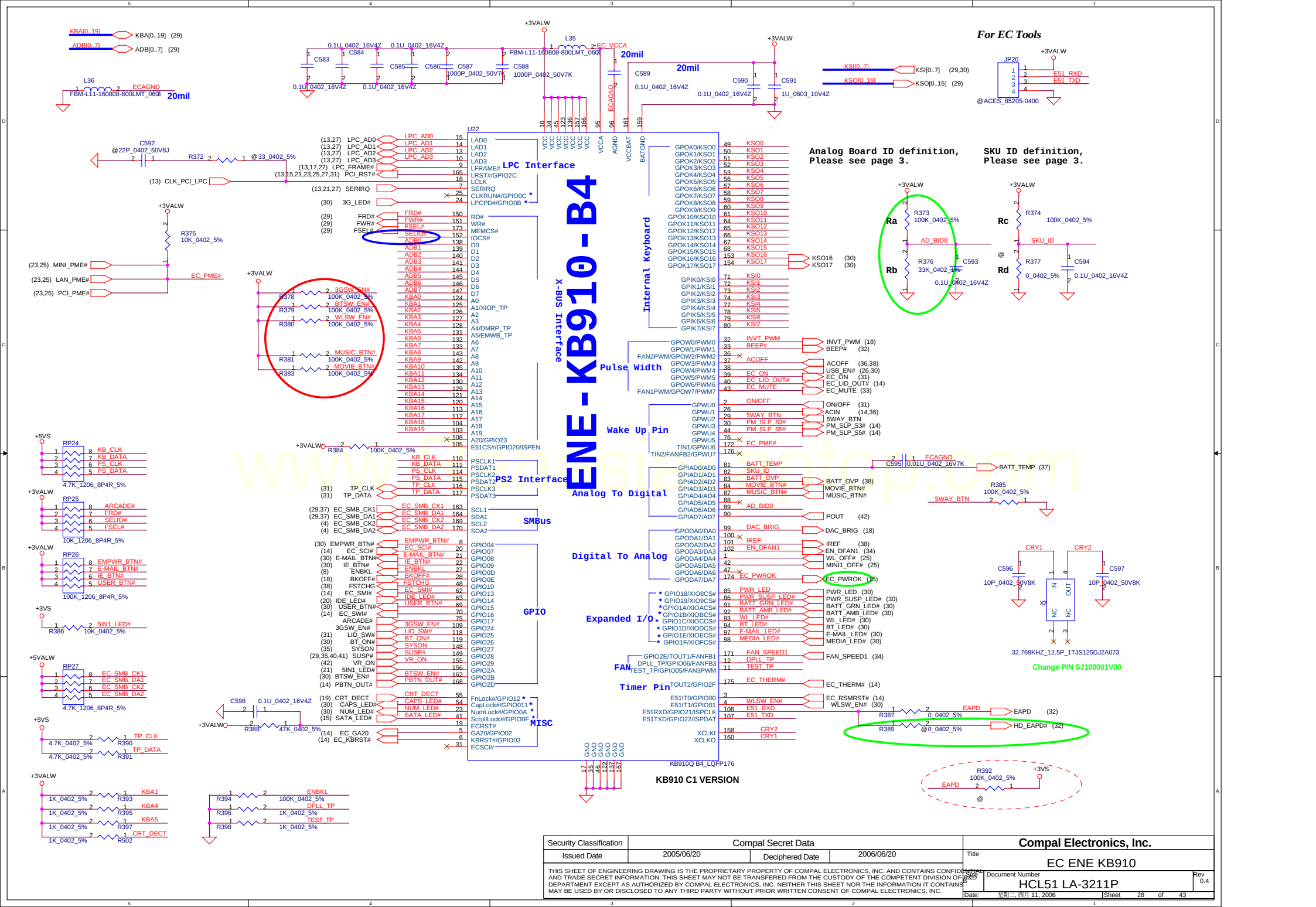
Place on the BOT side(near MINIPCI conn.)

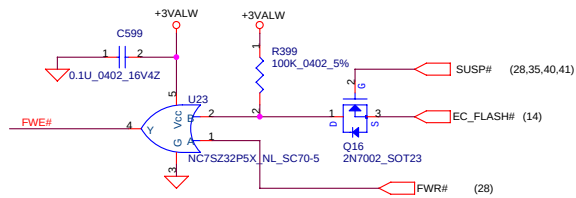


FIR Module

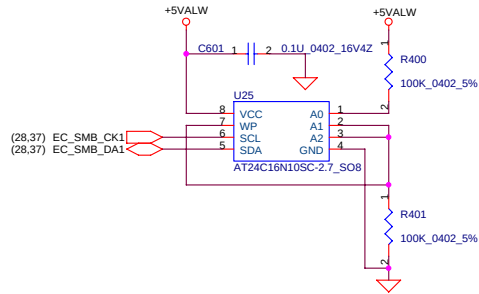


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				Date	Rev 0.4

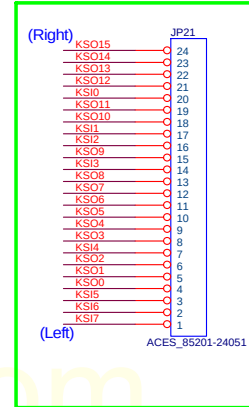
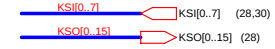




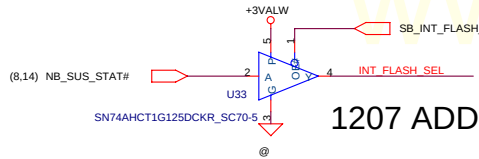
Check PCB Footprint



INT_KBD Conn.

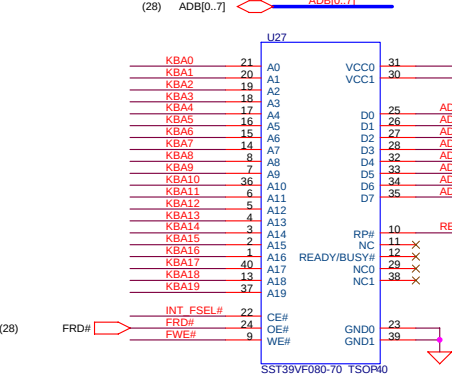


FOR DEBUG ONLY

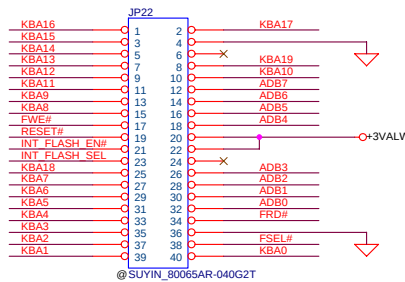


1MB Flash ROM

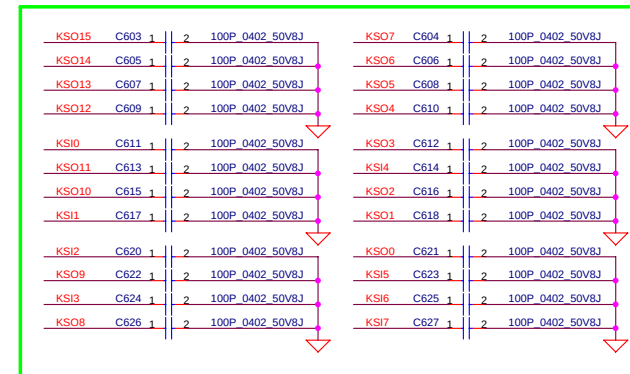
(28) KBA[0..19]
(28) ADB[0..7]



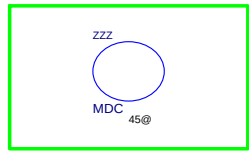
1MB ROM Socket



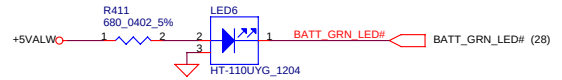
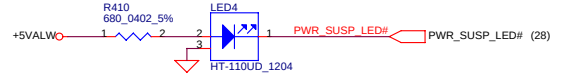
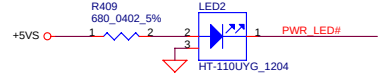
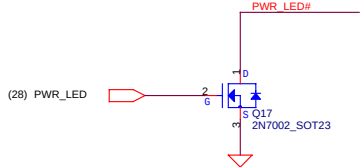
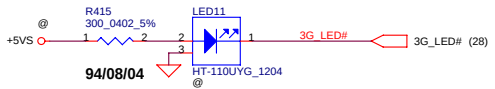
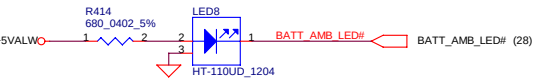
2006/01/23
DEL SB_INT_FLASH_SEL



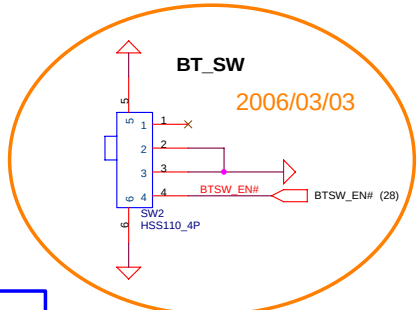
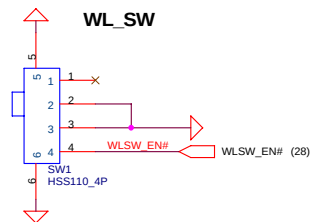
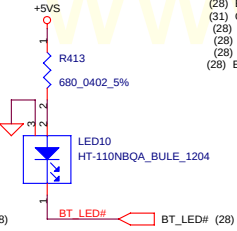
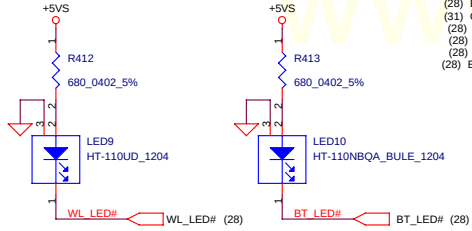
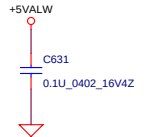
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title	BIOS, I/O Port & K/B Connector
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				Date	2006/04/11
				Sheet	29 of 43



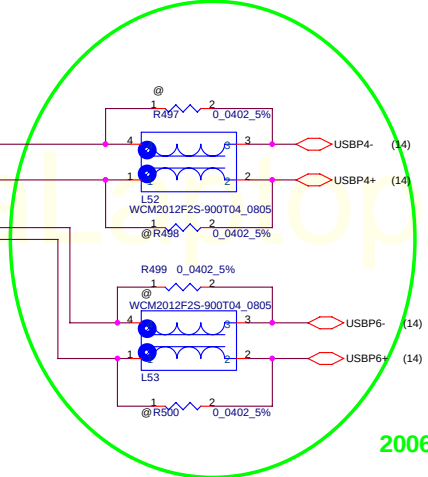
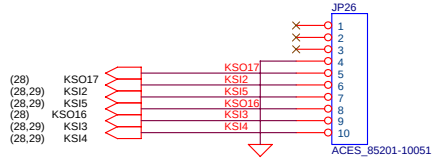
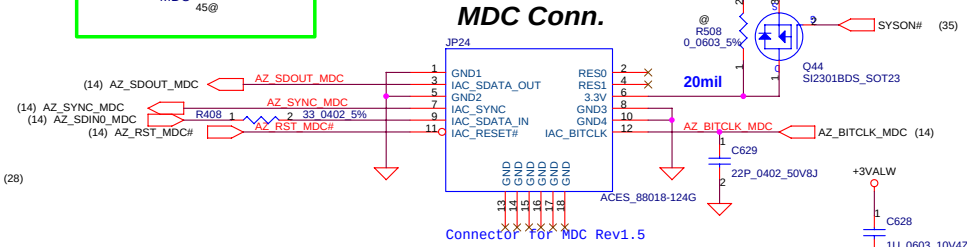
2006/01/23



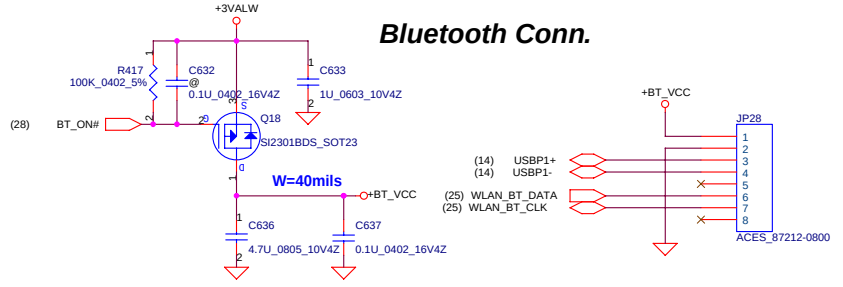
To LED/B Conn.



Geneva			Grapevine		
	KSO16	KSO17		KSO16	KSO17
KSI0	VOL_UP	LEFT			
KSI1	RIGHT	VOL_DOWN			
KSI2	PLAY	ENTER	KSI2	PLAY	
KSI3	STOP		KSI3	STOP	VOL_UP
KSI4	NEXT		KSI4	NEXT	VOL_DOWN
KSI5	REV		KSI5	REV	ARCADE_TV
KSI6		RECORD			

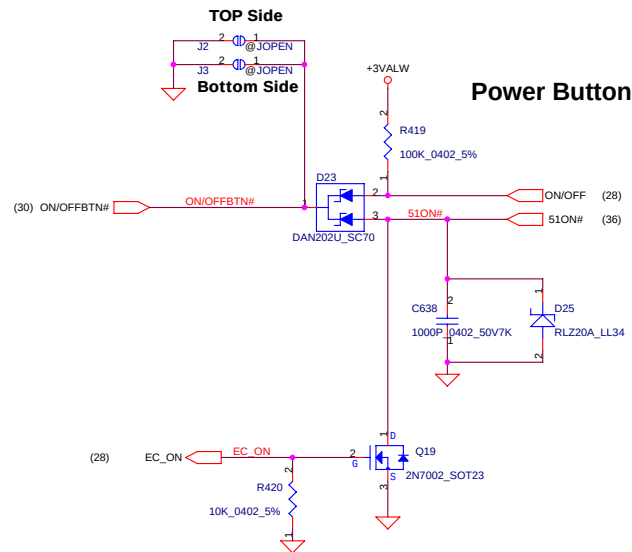


2006/01/24

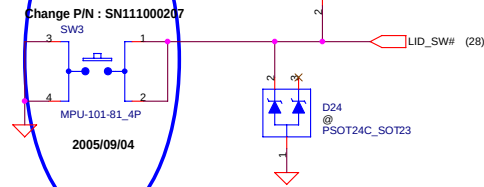


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Date:		2006/01/24		Sheet		30		of		43	

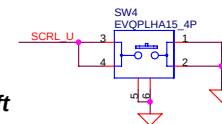
ON/OFF switch



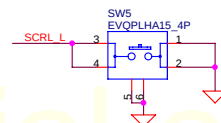
Lid Switch



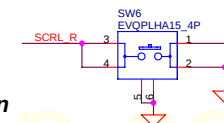
Scroll Up



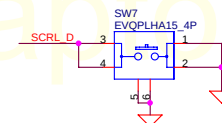
Scroll Left



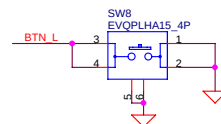
Scroll Right



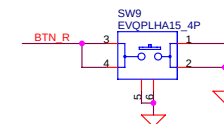
Scroll Down



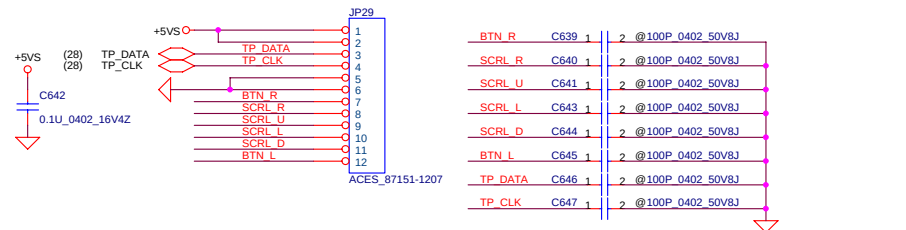
Left



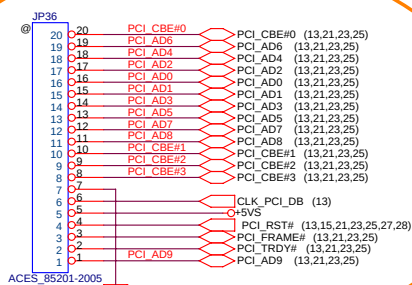
Right



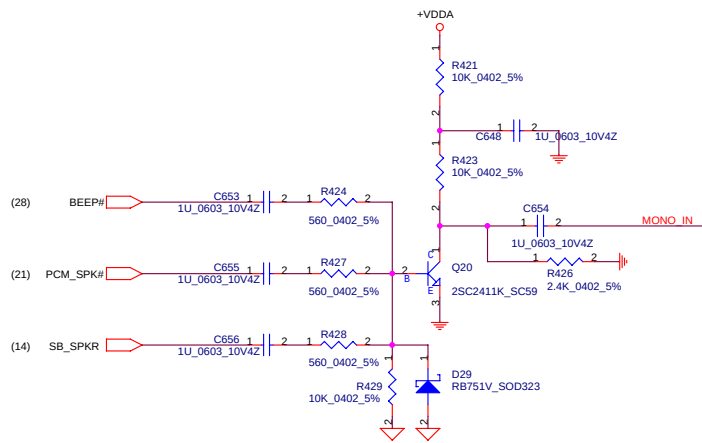
To TP/B Conn.



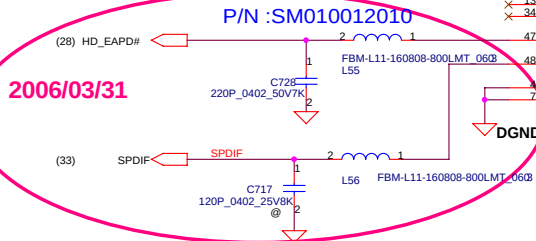
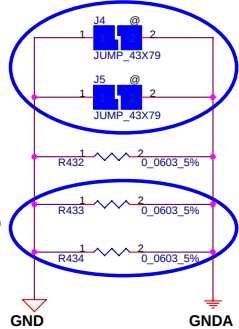
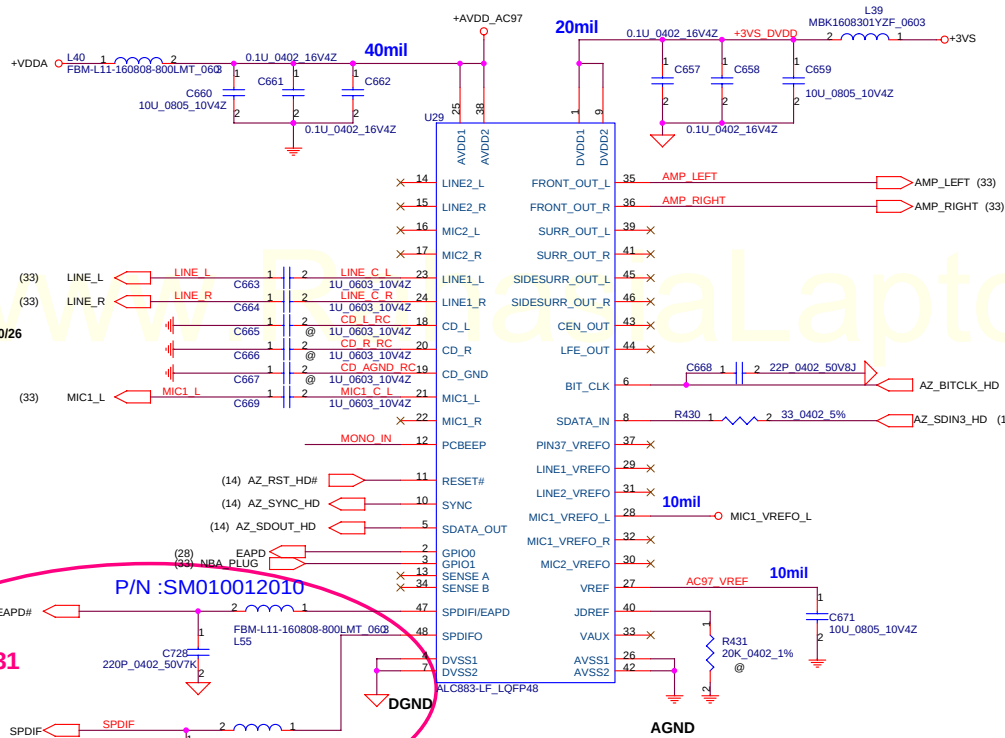
2006/03/07



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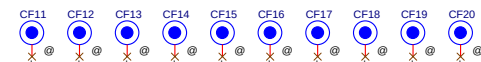
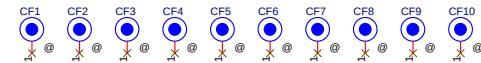
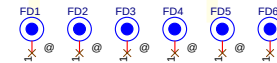
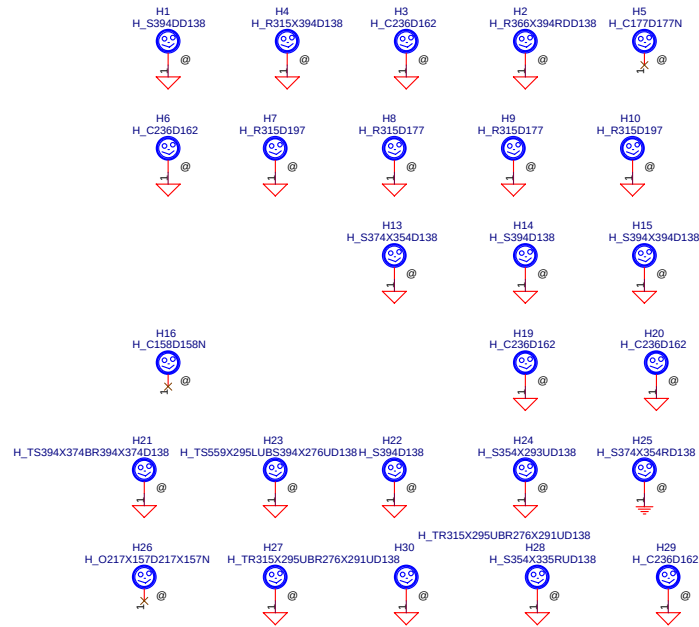
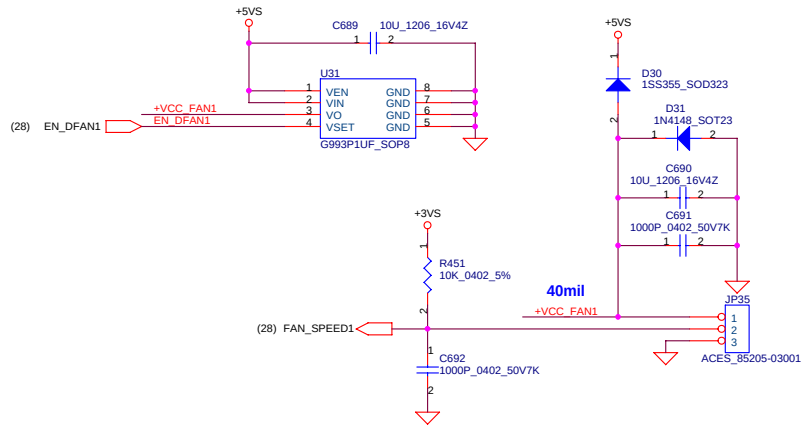


HD Audio Codec



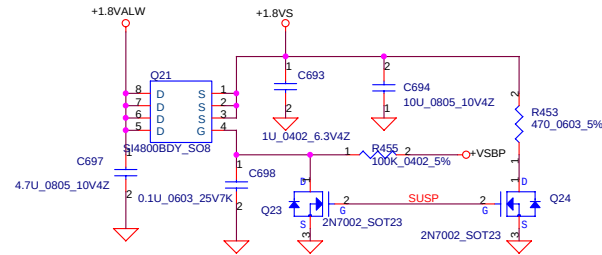
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FAN1 Conn

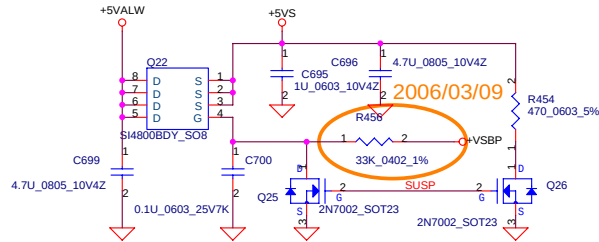


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+1.8VALW TO +1.8VS

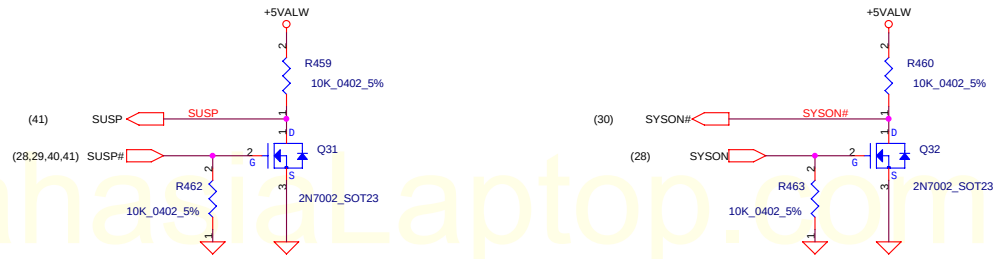
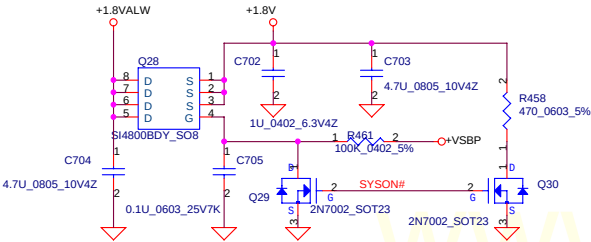


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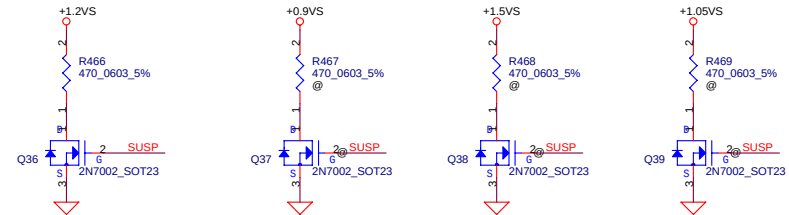
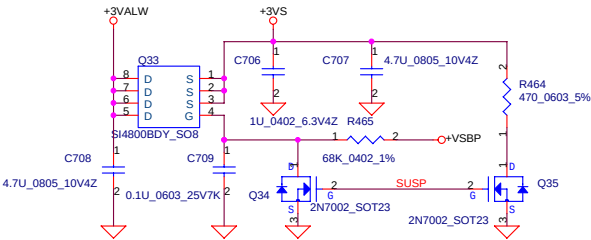


1207 DEL

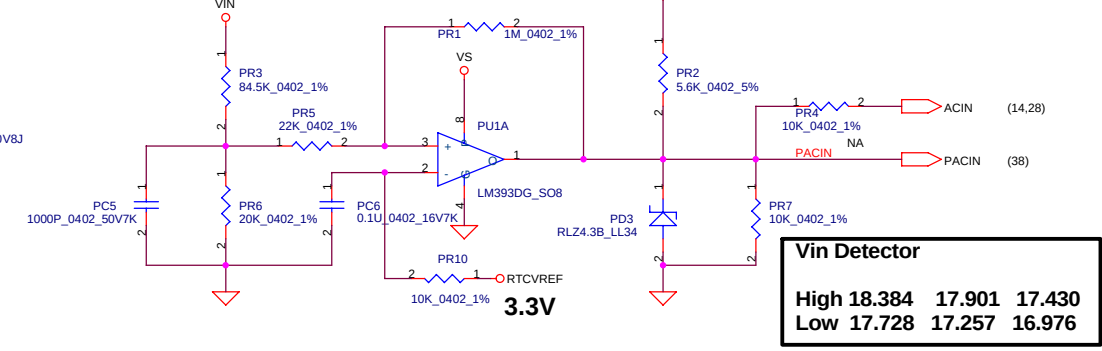
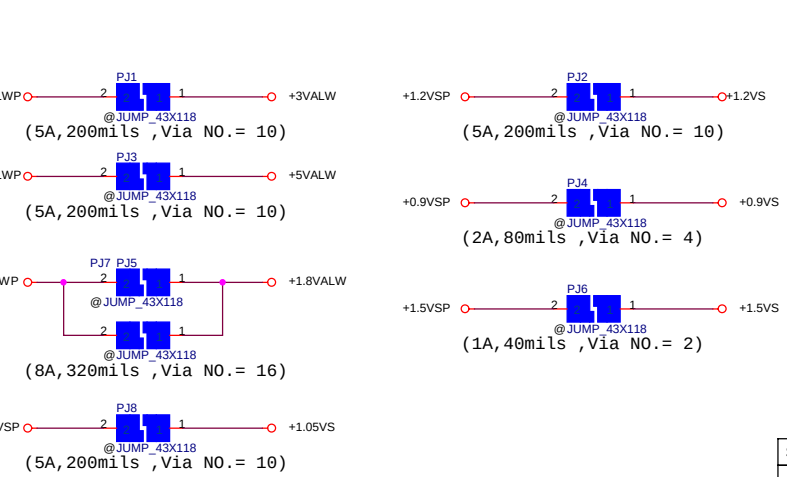
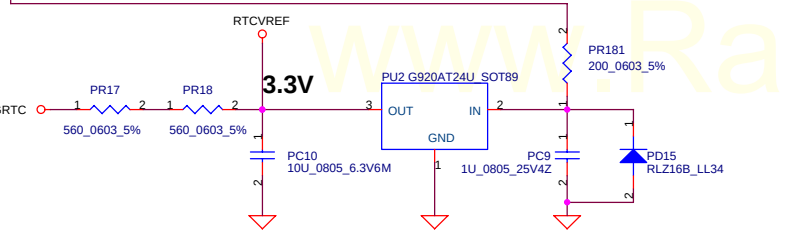
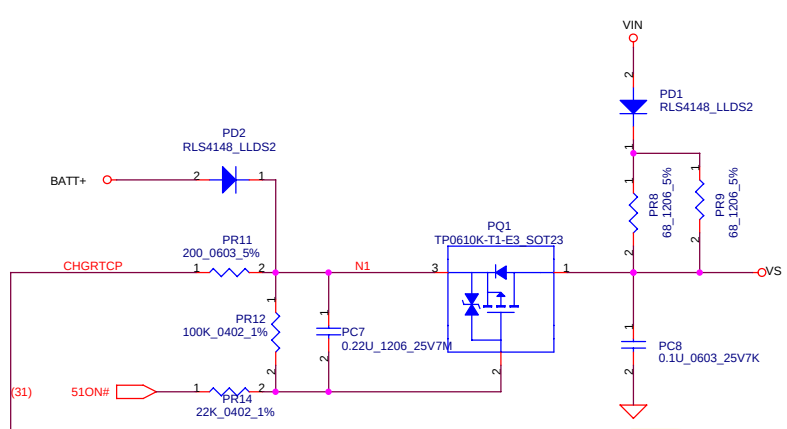
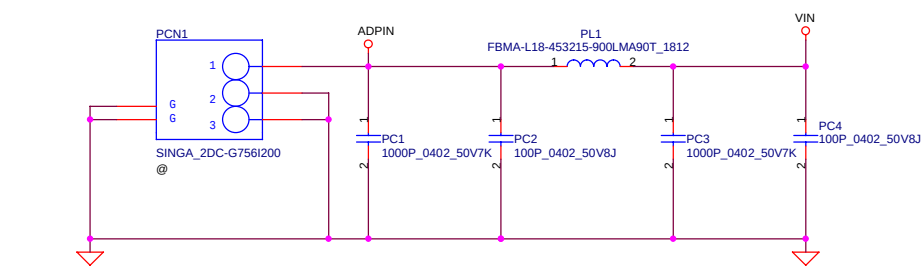
+1.8VALW TO +1.8V



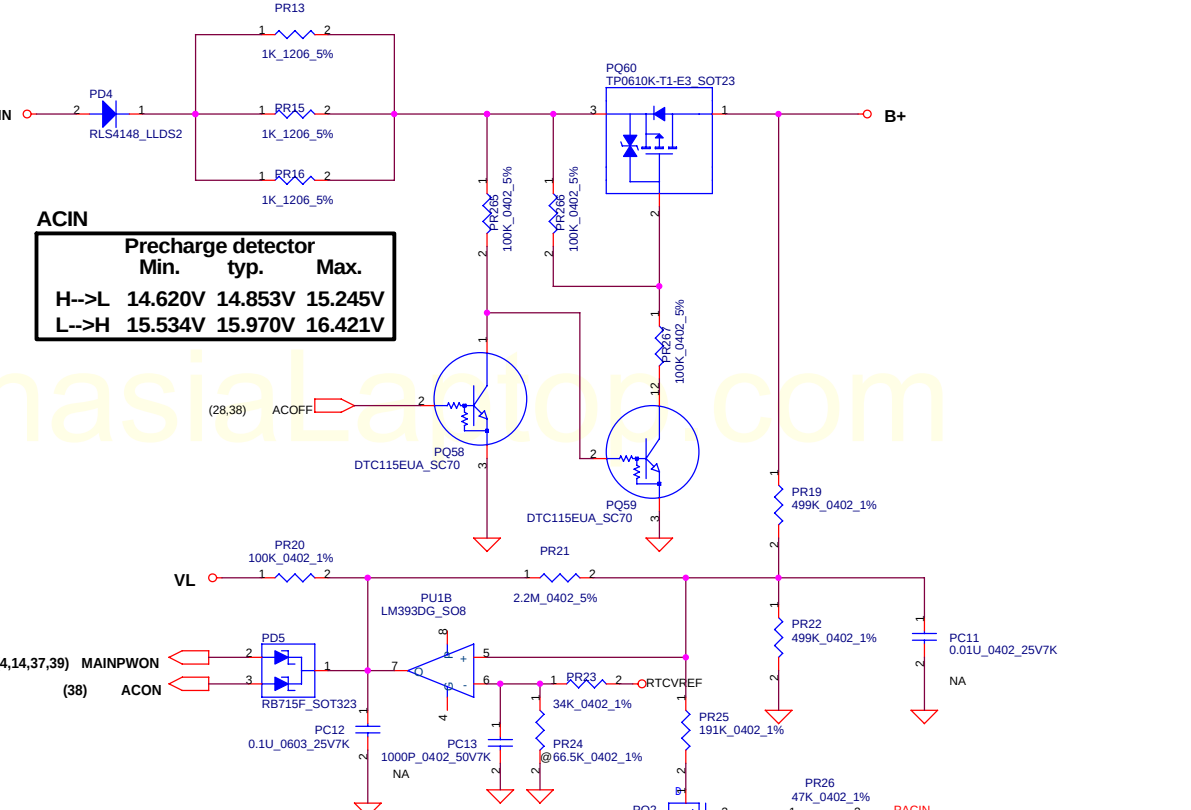
+3VALW TO +3VS



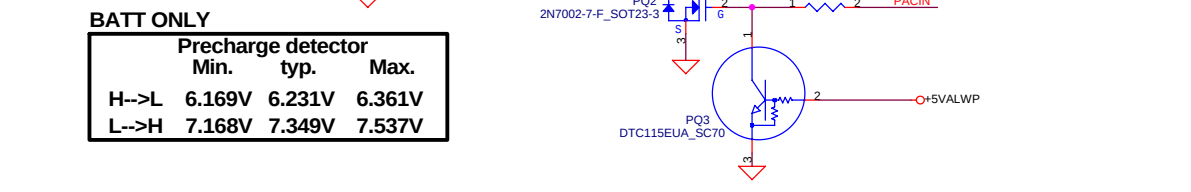
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Date: 2006/11/30					



Vin Detector			
High	18.384	17.901	17.430
Low	17.728	17.257	16.976

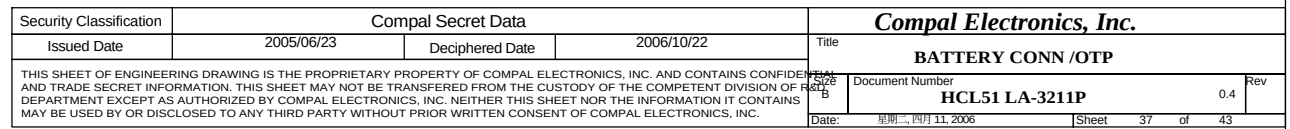
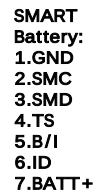
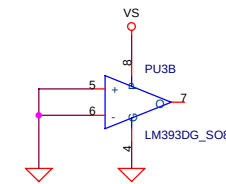


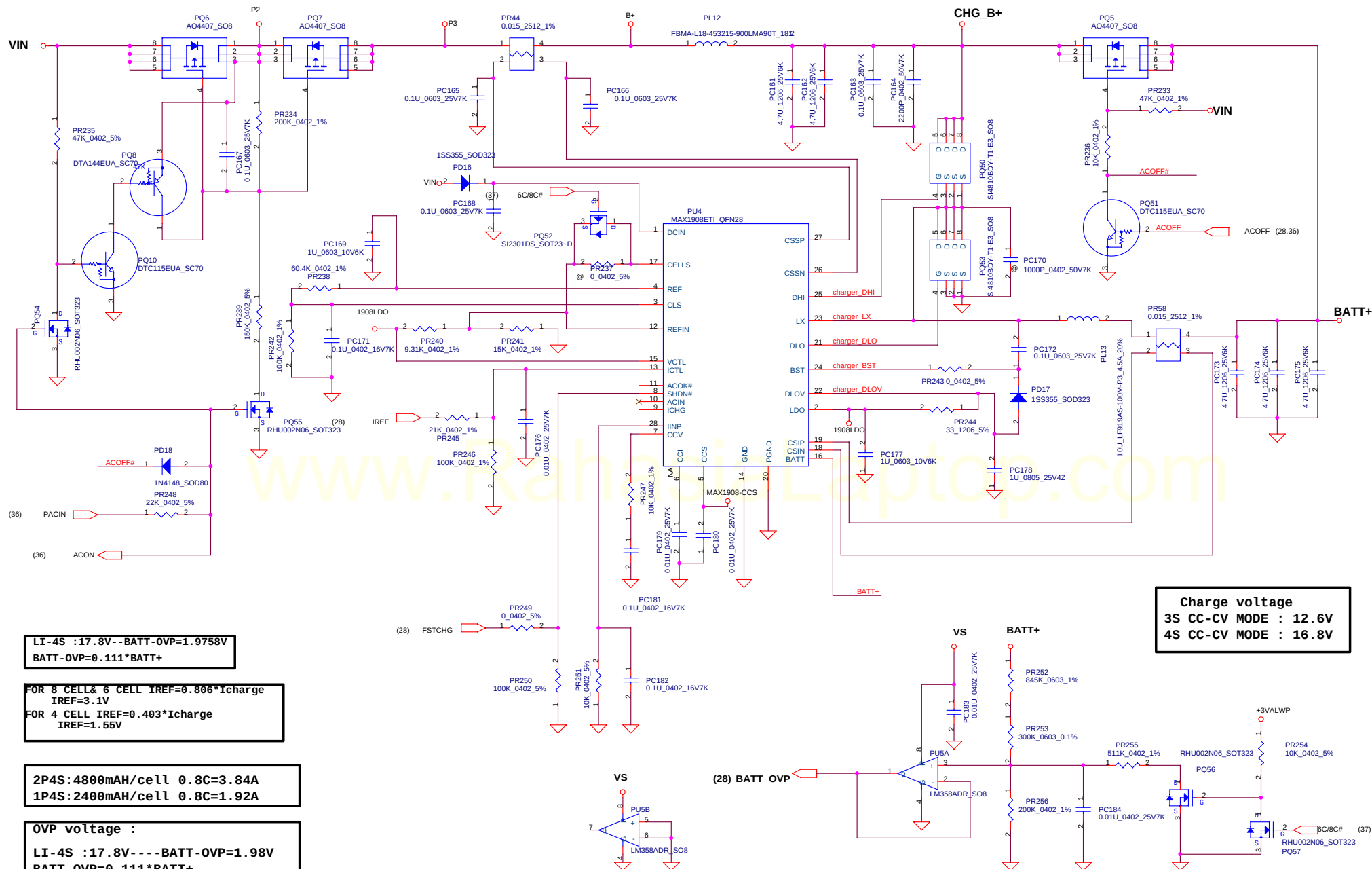
ACIN			
	Precharge detector		
	Min.	typ.	Max.
H-->L	14.620V	14.853V	15.245V
L-->H	15.534V	15.970V	16.421V



BATT ONLY			
	Precharge detector		
	Min.	typ.	Max.
H-->L	6.169V	6.231V	6.361V
L-->H	7.168V	7.349V	7.537V

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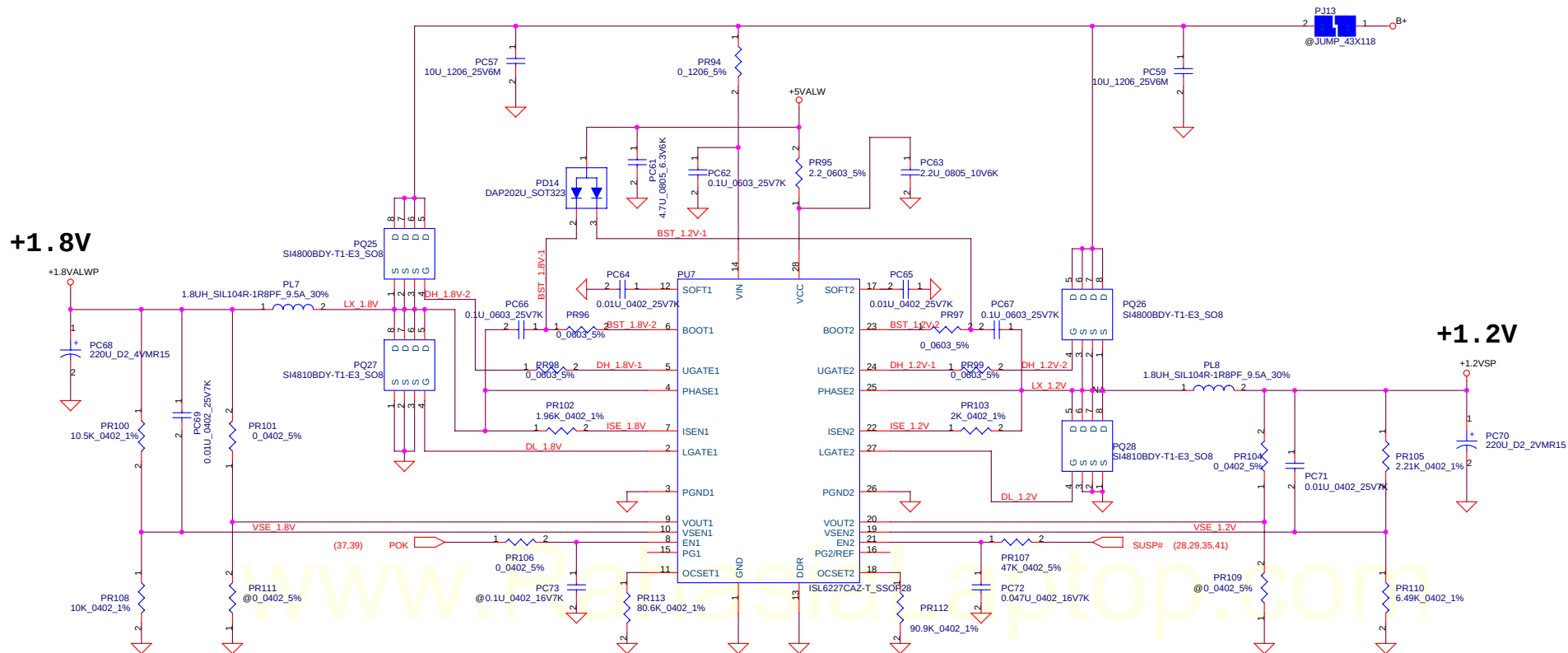
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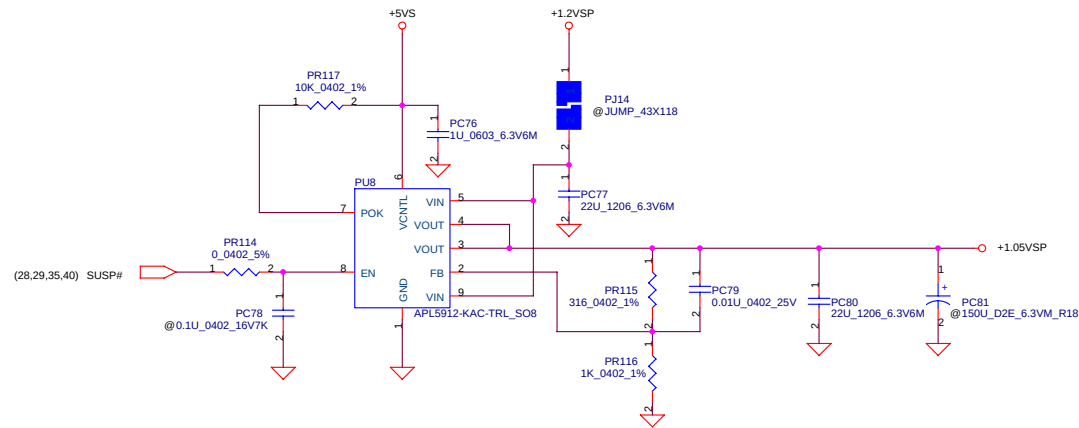
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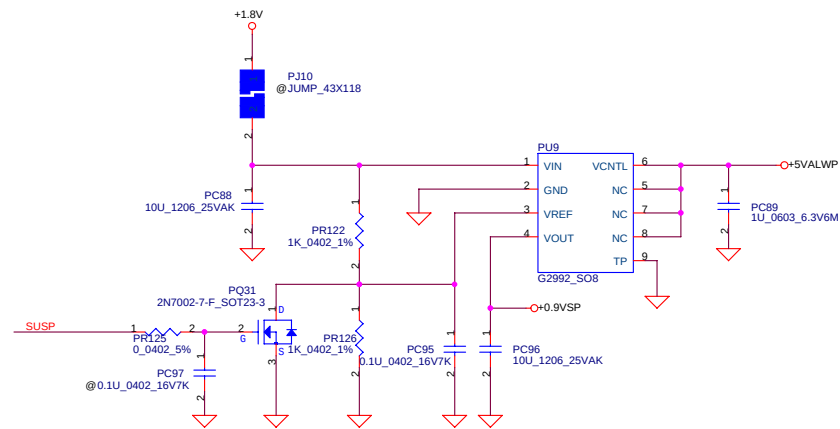
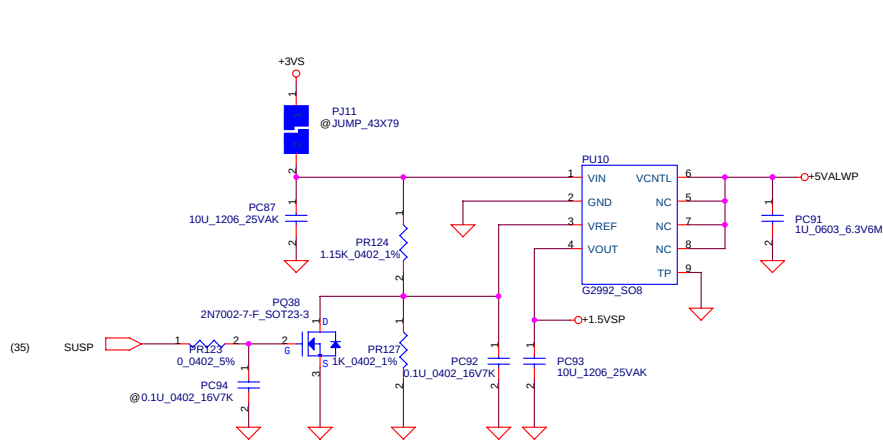
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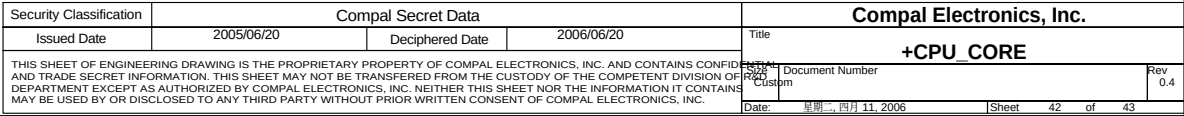
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Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	VER	Phase
1		For EMI require CPU core change from 0 to 2.2		42	MODIFY PR268/PR269 FROM 0 TO 2.2		DVT
2		modify 1.2V sequence(HW require)		40	change PR107 from 0 to 1k ;add PC72: :0.01uF		DVT
3		modify 1.2V sequence(HW require)		40	change PR107 from 1K to 47K ;change PC72: : from 0.01uF to 0.047uF		PVT
4							
5							
6							
7							
8							
9							
10							
11							
8							
9							