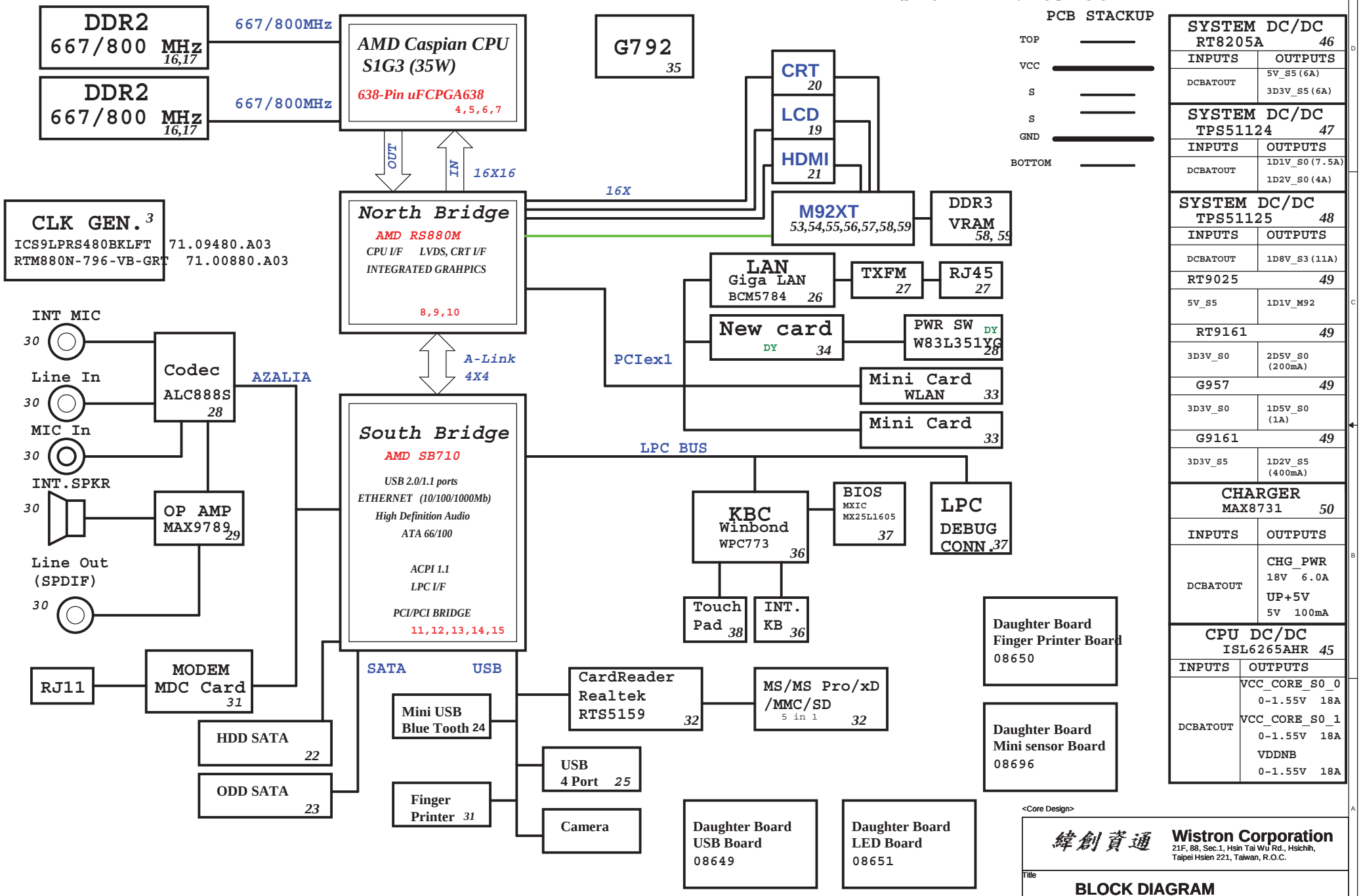
JV50-TR Block Diagram

Project code: 91.4FN01.001
PCB P/N : 48.4FN01.001
REVISION : 09230- -1



PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC RT8205A 46

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC TPS51124 47

INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(7.5A) 1D2V_S0(4A)

SYSTEM DC/DC TPS51125 48

INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(11A)

RT9025 49

5V_S5	1D1V_M92

RT9161 49

3D3V_S0	2D5V_S0 (200mA)

G957 49

3D3V_S0	1D5V_S0 (1A)

G9161 49

3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731 50

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265AHR 45

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: JV50-TR | Rev: SB
Date: Tuesday, June 16, 2009 | Sheet 1 of 61

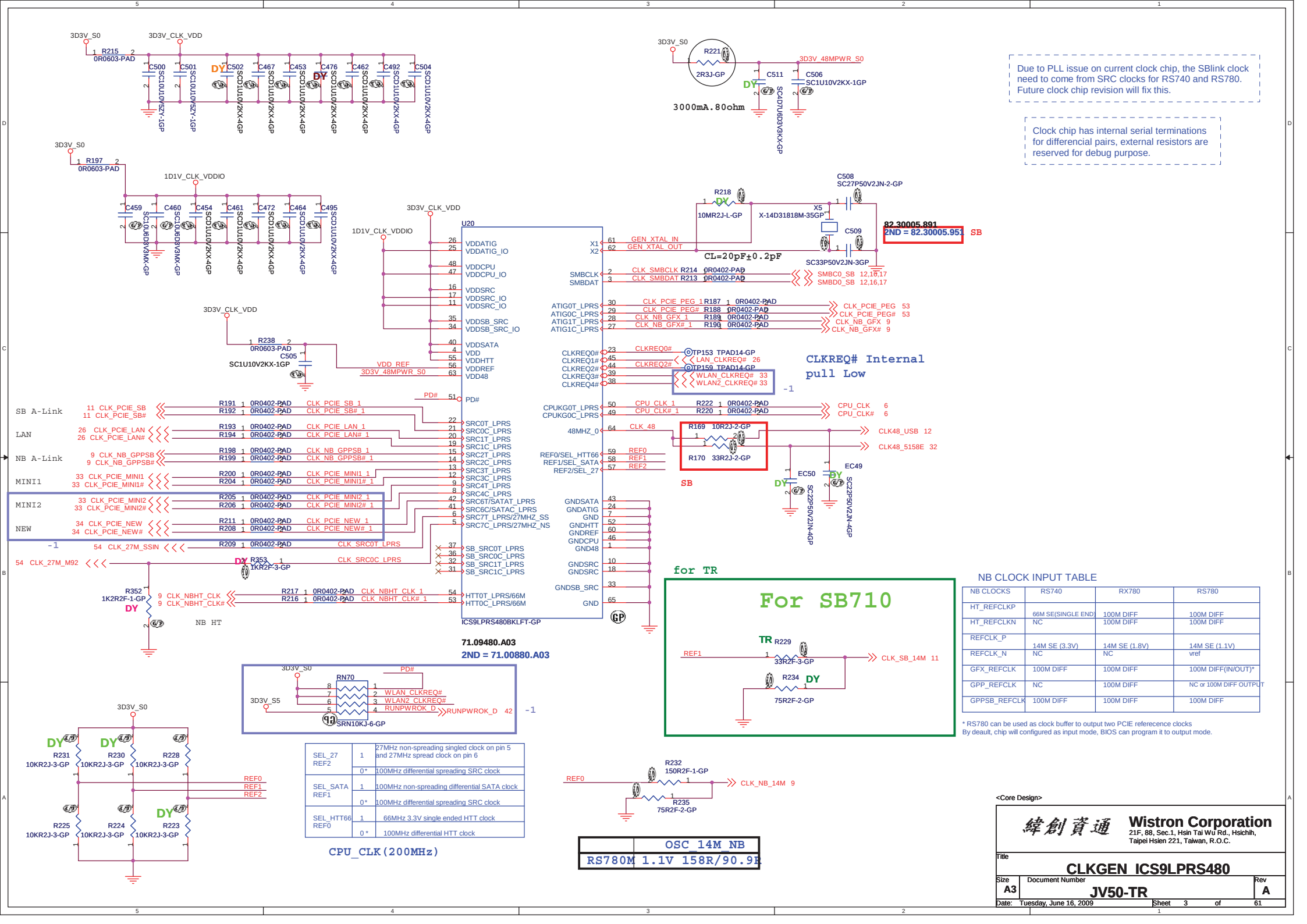
<Core Design>

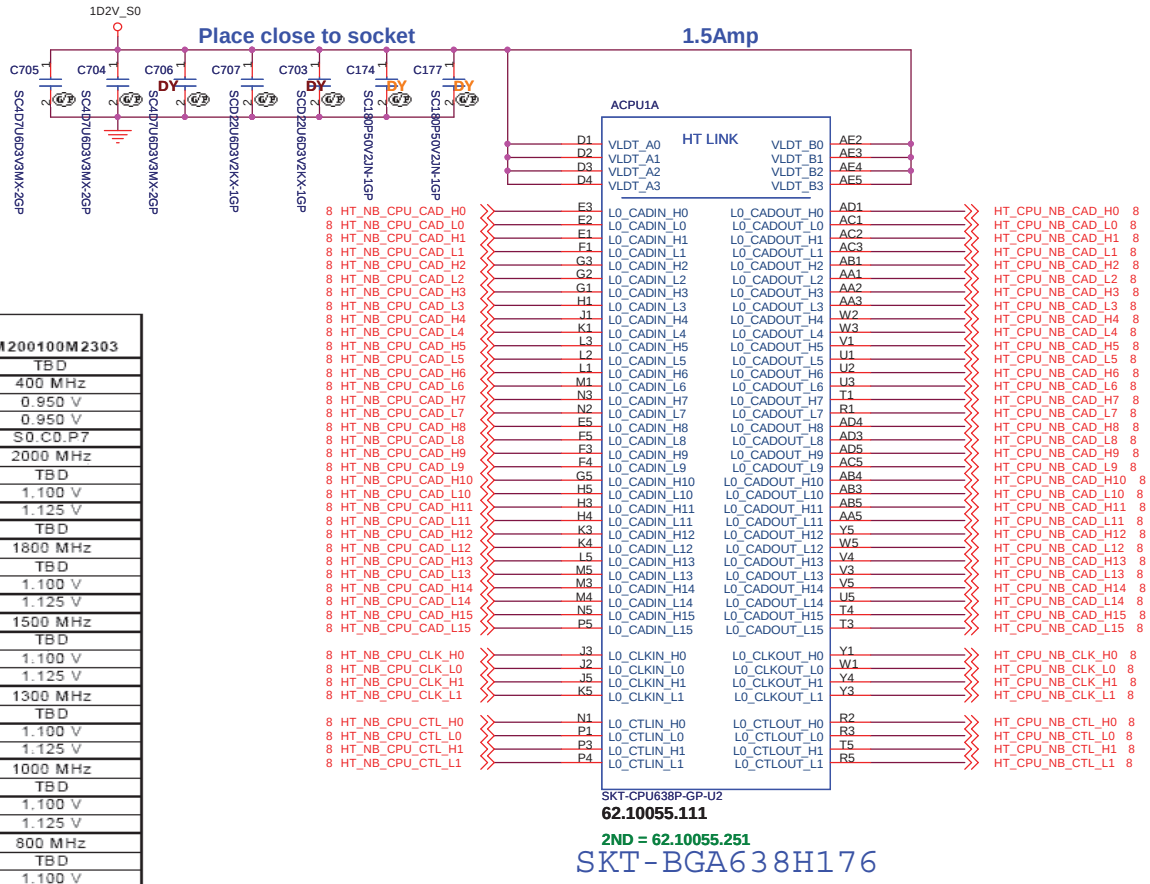
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB/PCIE Routing**

Size	Document Number	Rev
A3	JV50-TR	A

Date: Tuesday, June 16, 2009 Sheet 2 of 61


3D3V_S0
3D3V_CLK_VDD
R215 0R0603-PAD
C500 SC10U10V5ZY-1GP
C501 SC10U10V5ZY-1GP
C502 SC1U10V2KX-4GP
C467 SC1U10V2KX-4GP
C453 SC1U10V2KX-4GP
C476 SC1U10V2KX-4GP
C462 SC1U10V2KX-4GP
C492 SC1U10V2KX-4GP
C504 SC1U10V2KX-4GP
DY
3D3V_S0
R221 2R3J-GP
3D3V_48MPWR_S0
C511 SC4D7U6D3V3KX-GP
C506 SC1U10V2KX-1GP
3000mA.80ohm
Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.
3D3V_S0
R197 0R0603-PAD
1D1V_CLK_VDDIO
C459 SC10U6D3V3MX-GP
C460 SC10U6D3V3MX-GP
C454 SC1U10V2KX-4GP
C461 SC1U10V2KX-4GP
C472 SC1U10V2KX-4GP
C464 SC1U10V2KX-4GP
C495 SC1U10V2KX-4GP
3D3V_CLK_VDD
1D1V_CLK_VDDIO
U20
VDDATIG
VDDATIG_IO
VDDCPU
VDDCPU_IO
VDDSRC
VDDSRC_IO
VDDSRC_IO
VDDSB_SRC
VDDSB_SRC_IO
VDDSATA
VDD
VDDHTT
VDDREF
VDD48
R218 10MR2J-L-GP
X5 X-14D31818M-35GP
C508 SC27P50V2JN-2-GP
C509 SC33P50V2JN-3GP
82.30005.891
2ND = 82.30005.951 SB
CL=20pF±0.2pF
X1
X2
GEN_XTAL_IN
GEN_XTAL_OUT
SMBCLK
SMBDAT
CLK_SMBCLK R214 0R0402-PAD
CLK_SMBDAT R213 0R0402-PAD
SMBC0_SB 12,16,17
SMBD0_SB 12,16,17
3D3V_CLK_VDD
R238 0R0603-PAD
C505 SC1U10V2KX-1GP
VDD_REF
3D3V_48MPWR_S0
ATIG0T_LPRS
ATIG0C_LPRS
ATIG1T_LPRS
ATIG1C_LPRS
CLK_PCIE_PEG_1 R187 0R0402-PAD
CLK_PCIE_PEG# R188 0R0402-PAD
CLK_NB_GFX_1 R189 0R0402-PAD
CLK_NB_GFX#_1 R190 0R0402-PAD
CLK_PCIE_PEG 53
CLK_PCIE_PEG# 53
CLK_NB_GFX 9
CLK_NB_GFX# 9
CLKREQ0#
CLKREQ1#
CLKREQ2#
CLKREQ3#
CLKREQ4#
TP153 TPAD14-GP
TP159 TPAD14-GP
LAN_CLKREQ# 26
WLAN_CLKREQ# 33
WLAN2_CLKREQ# 33
CLKREQ# Internal pull Low
-1
PD#
SB A-Link
LAN
NB A-Link
MINI1
MINI2
NEW
SRC0T_LPRS
SRC0C_LPRS
SRC1T_LPRS
SRC1C_LPRS
SRC2T_LPRS
SRC2C_LPRS
SRC3T_LPRS
SRC3C_LPRS
SRC4T_LPRS
SRC4C_LPRS
SRC6T/SATAT_LPRS
SRC6C/SATAC_LPRS
SRC7T_LPRS/27MHZ_SS
SRC7C_LPRS/27MHZ_NS
CPUKG0T_LPRS
CPUKG0C_LPRS
CPU_CLK_1 R222 0R0402-PAD
CPU_CLK#_1 R220 0R0402-PAD
CPU_CLK 6
CPU_CLK# 6
48MHZ_0
CLK_48
R169 10R2J-2-GP
R170 33R2J-2-GP
CLK48_USB 12
CLK48_5158E 32
SB
REF0/SEL_HTT66
REF1/SEL_SATA
REF2/SEL_27
REF0
REF1
REF2
EC50 SC22P50V2JN-4GP
EC49 SC22P50V2JN-4GP
GNDSATA
GNDATIG
GND
GNDHTT
GNDREF
GNDCPU
GND48
GNDSRC
GNDSRC
GNDSB_SRC
GND
SB_SRC0T_LPRS
SB_SRC0C_LPRS
SB_SRC1T_LPRS
SB_SRC1C_LPRS
HTT0T_LPRS/66M
HTT0C_LPRS/66M
ICS9LPRS480BKLFT-GP
71.09480.A03
2ND = 71.00880.A03
11 CLK_PCIE_SB
11 CLK_PCIE_SB#
26 CLK_PCIE_LAN
26 CLK_PCIE_LAN#
9 CLK_NB_GPPSB
9 CLK_NB_GPPSB#
33 CLK_PCIE_MINI1
33 CLK_PCIE_MINI1#
33 CLK_PCIE_MINI2
33 CLK_PCIE_MINI2#
34 CLK_PCIE_NEW
34 CLK_PCIE_NEW#
R191 0R0402-PAD CLK_PCIE_SB_1
R192 0R0402-PAD CLK_PCIE_SB#_1
R193 0R0402-PAD CLK_PCIE_LAN_1
R194 0R0402-PAD CLK_PCIE_LAN#_1
R198 0R0402-PAD CLK_NB_GPPSB_1
R199 0R0402-PAD CLK_NB_GPPSB#_1
R200 0R0402-PAD CLK_PCIE_MINI1_1
R204 0R0402-PAD CLK_PCIE_MINI1#_1
R205 0R0402-PAD CLK_PCIE_MINI2_1
R206 0R0402-PAD CLK_PCIE_MINI2#_1
R211 0R0402-PAD CLK_PCIE_NEW_1
R208 0R0402-PAD CLK_PCIE_NEW#_1
54 CLK_27M_SSIN
R209 0R0402-PAD CLK_SRC0T_LPRS
54 CLK_27M_M92
DY R353 1KR2F-3-GP
CLK_SRC0C_LPRS
R352 1K2R2F-1-GP
DY
9 CLK_NBHT_CLK
9 CLK_NBHT_CLK#
NB HT
R217 0R0402-PAD CLK_NBHT_CLK_1
R216 0R0402-PAD CLK_NBHT_CLK#_1
HTT0T_LPRS/66M
HTT0C_LPRS/66M
for TR
For SB710
TR R229 33R2F-3-GP
REF1
CLK_SB_14M 11
R234 DY 75R2F-2-GP
NB CLOCK INPUT TABLE
NB CLOCKS | RS740 | RX780 | RS780
HT_REFCLKP | 66M SE(SINGLE END) | 100M DIFF | 100M DIFF
HT_REFCLKN | NC | 100M DIFF | 100M DIFF
REFCLK_P | 14M SE (3.3V) | 14M SE (1.8V) | 14M SE (1.1V)
REFCLK_N | NC | NC | vref
GFX_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF(IN/OUT)*
GPP_REFCLK | NC | 100M DIFF | NC or 100M DIFF OUTPUT
GPPSB_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF
* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.
3D3V_S0
3D3V_S5
RN70 SRN10KJ-6-GP
PD#
WLAN_CLKREQ#
WLAN2_CLKREQ#
RUNPWROK_D
RUNPWROK_D 42
-1
3D3V_S0
R231 10KR2J-3-GP
R230 10KR2J-3-GP
R228 10KR2J-3-GP
R225 10KR2J-3-GP
R224 10KR2J-3-GP
R223 10KR2J-3-GP
REF0
REF1
REF2
SEL_27 REF2
1 27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
0* 100MHz differential spreading SRC clock
SEL_SATA REF1
1 100MHz non-spreading differential SATA clock
0* 100MHz differential spreading SRC clock
SEL_HTT66 REF0
1 66MHz 3.3V single ended HTT clock
0* 100MHz differential HTT clock
CPU_CLK(200MHz)
REF0
R232 150R2F-1-GP
R235 75R2F-2-GP
CLK_NB_14M 9
OSC_14M_NB
RS780M 1.1V 158R/90.9R
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CLKGEN_ICS9LPRS480
Size A3
Document Number JV50-TR
Rev A
Date: Tuesday, June 16, 2009
Sheet 3 of 61



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

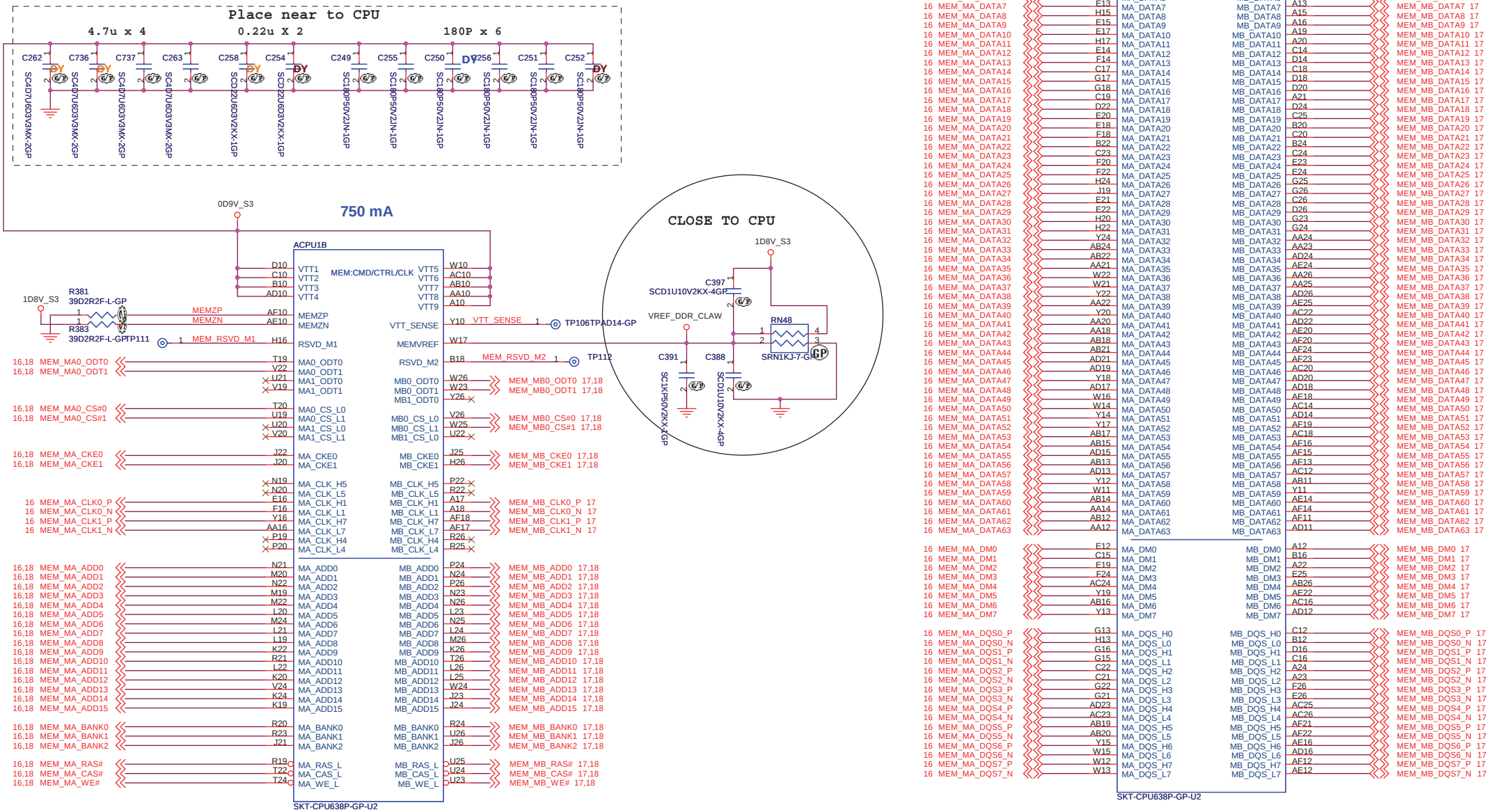
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU HT LINK I/F (1/4)

Size: A3 | Document Number: JV50-TR | Rev: SB

Date: Tuesday, June 16, 2009 | Sheet 4 of 61



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU_DDR_(2/4)**

Size	Document Number	Rev
A3	JV50-TR	SB

Date: Tuesday, June 16, 2009 Sheet 5 of 61

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

SB

Cloce To CPU

For HDT DBG

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

for TR

PU-->300R
TR-->510R

Near CPU PIN

CPU exceeds to 125℃

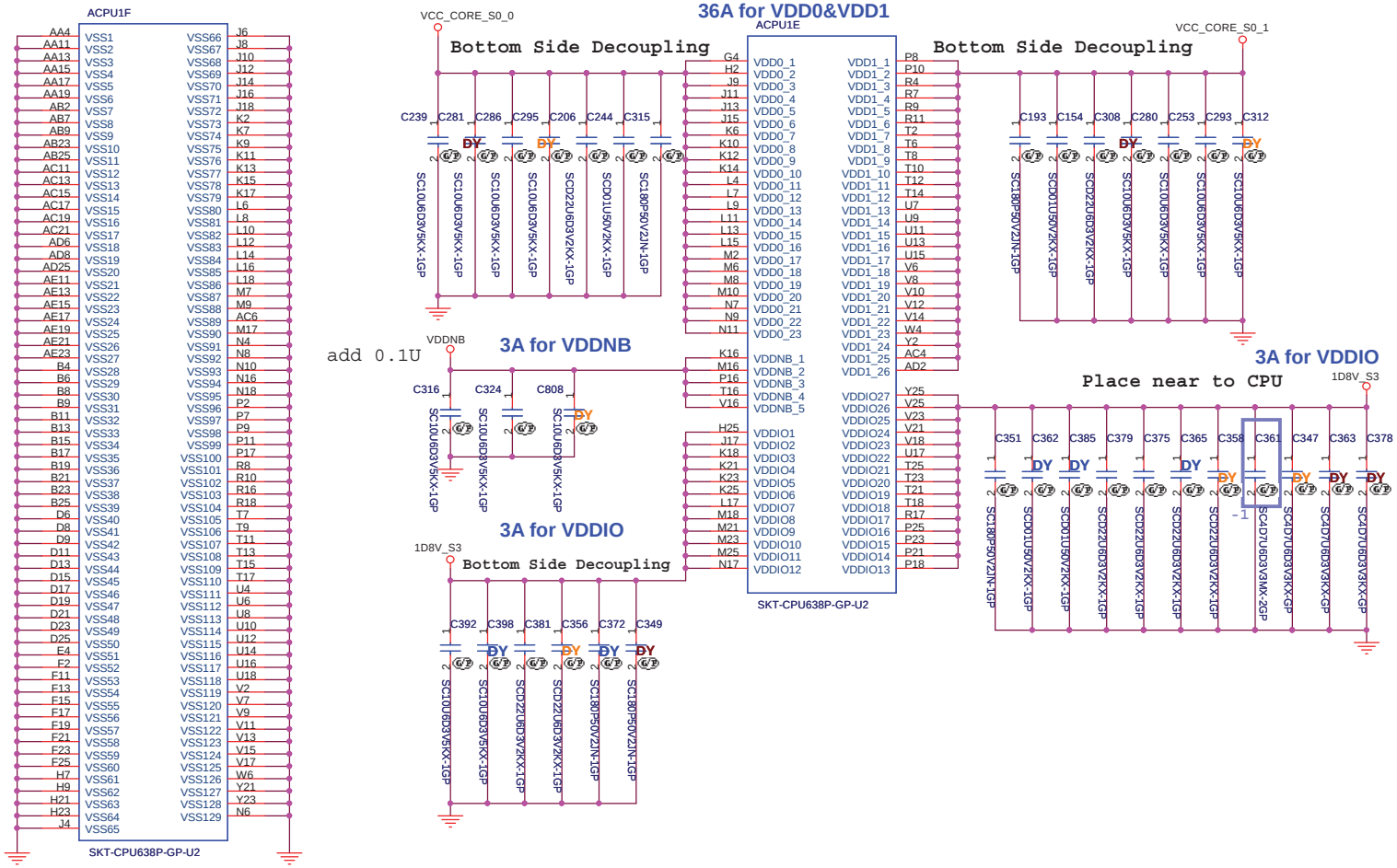
84.T3904.C11
2ND = 84.03904.L06

SKT-CPU638P-GP-U2

HDT Connectors

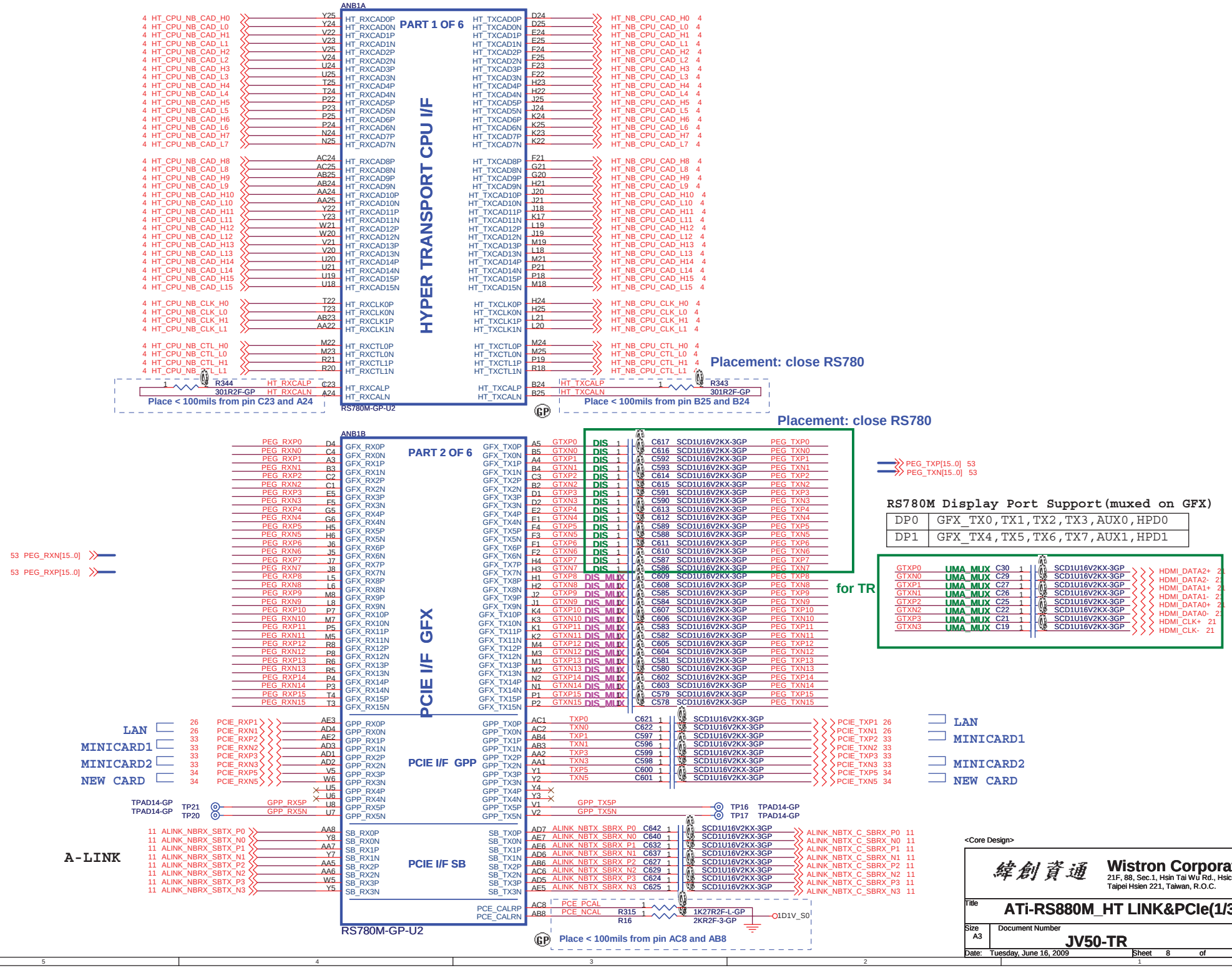
<Core Design>

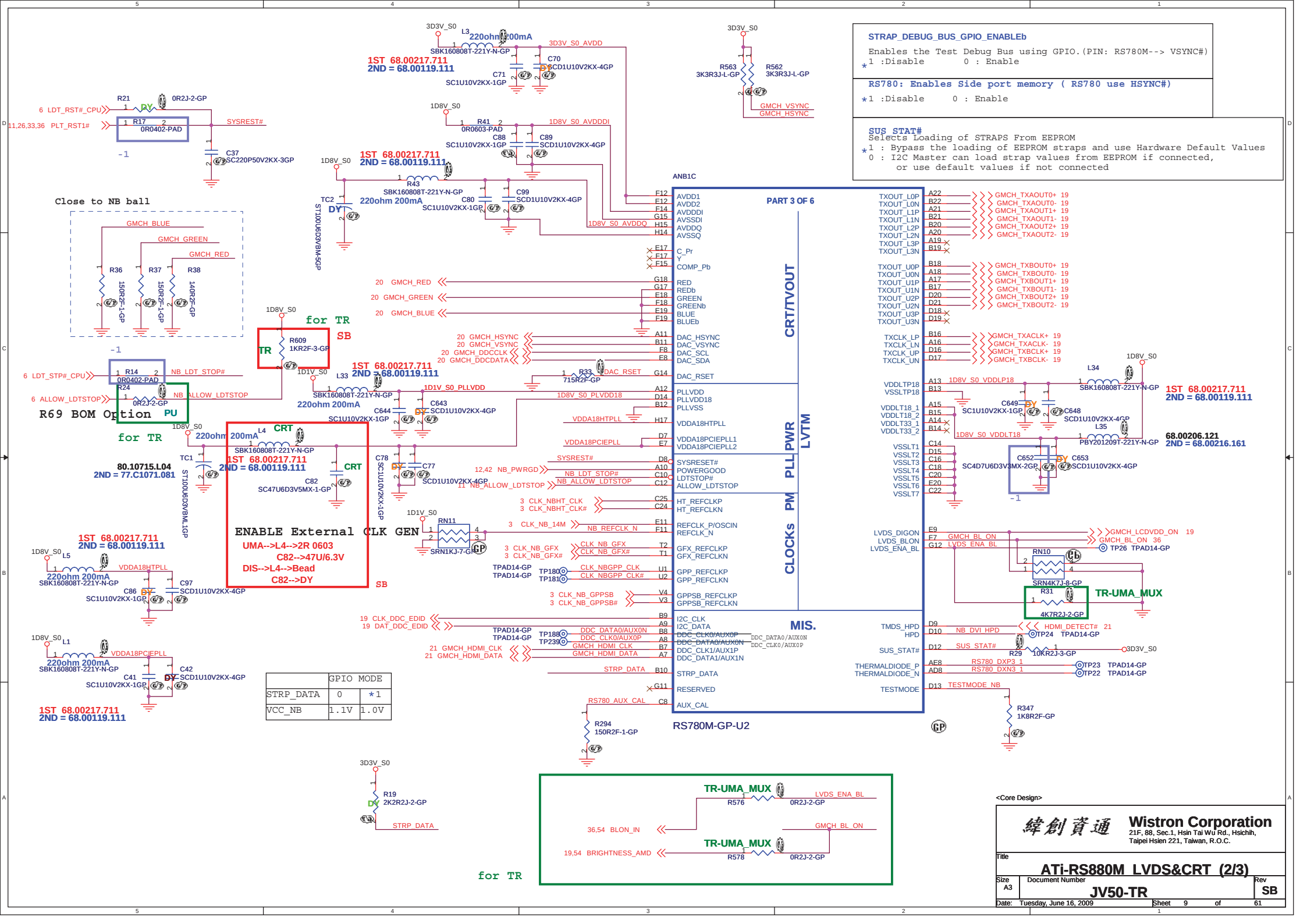
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU_Control&Debug_(3/4)		
Size: A3	Document Number: JV50-TR	Rev: SB
Date: Tuesday, June 16, 2009	Sheet 6 of 61	

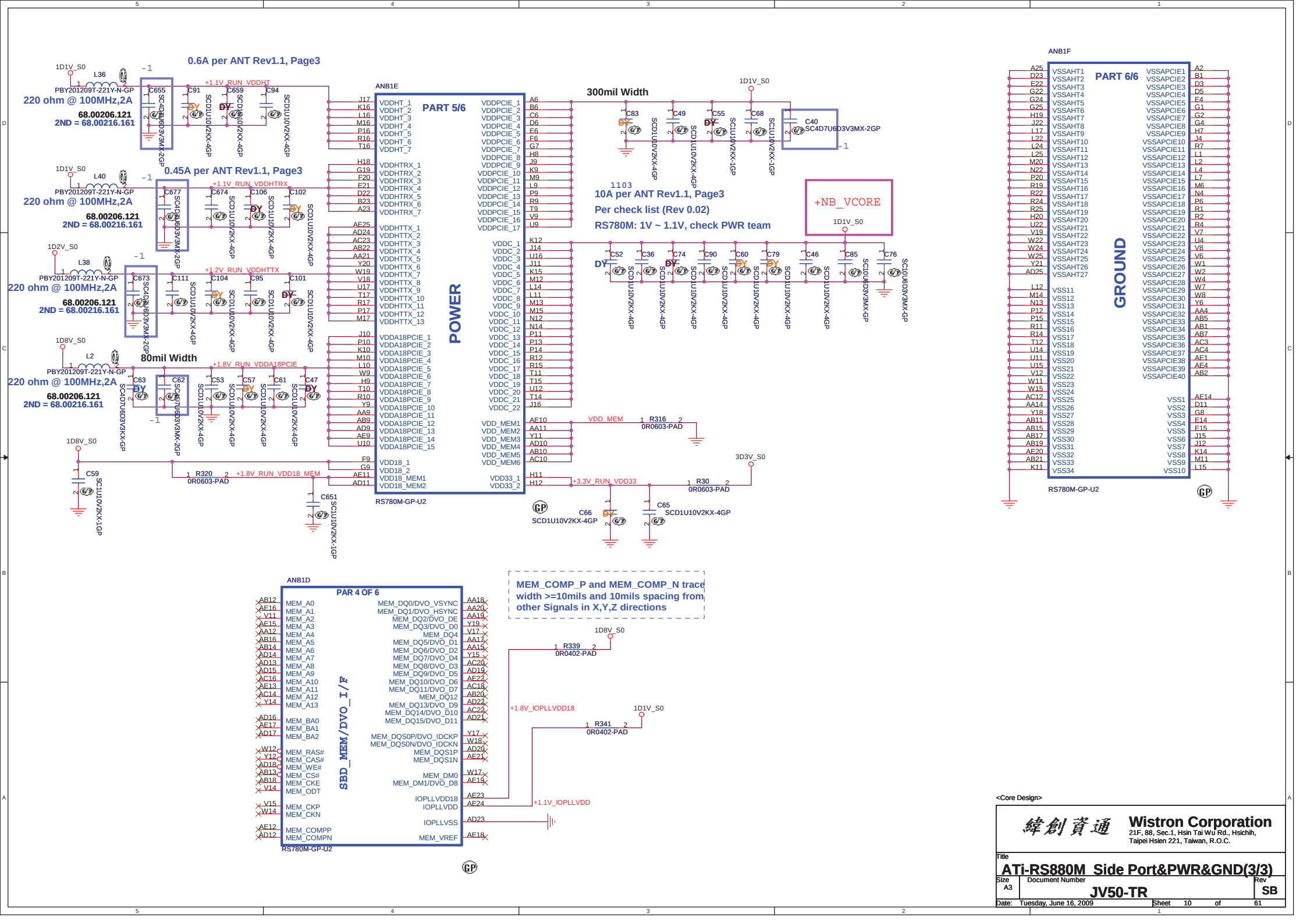


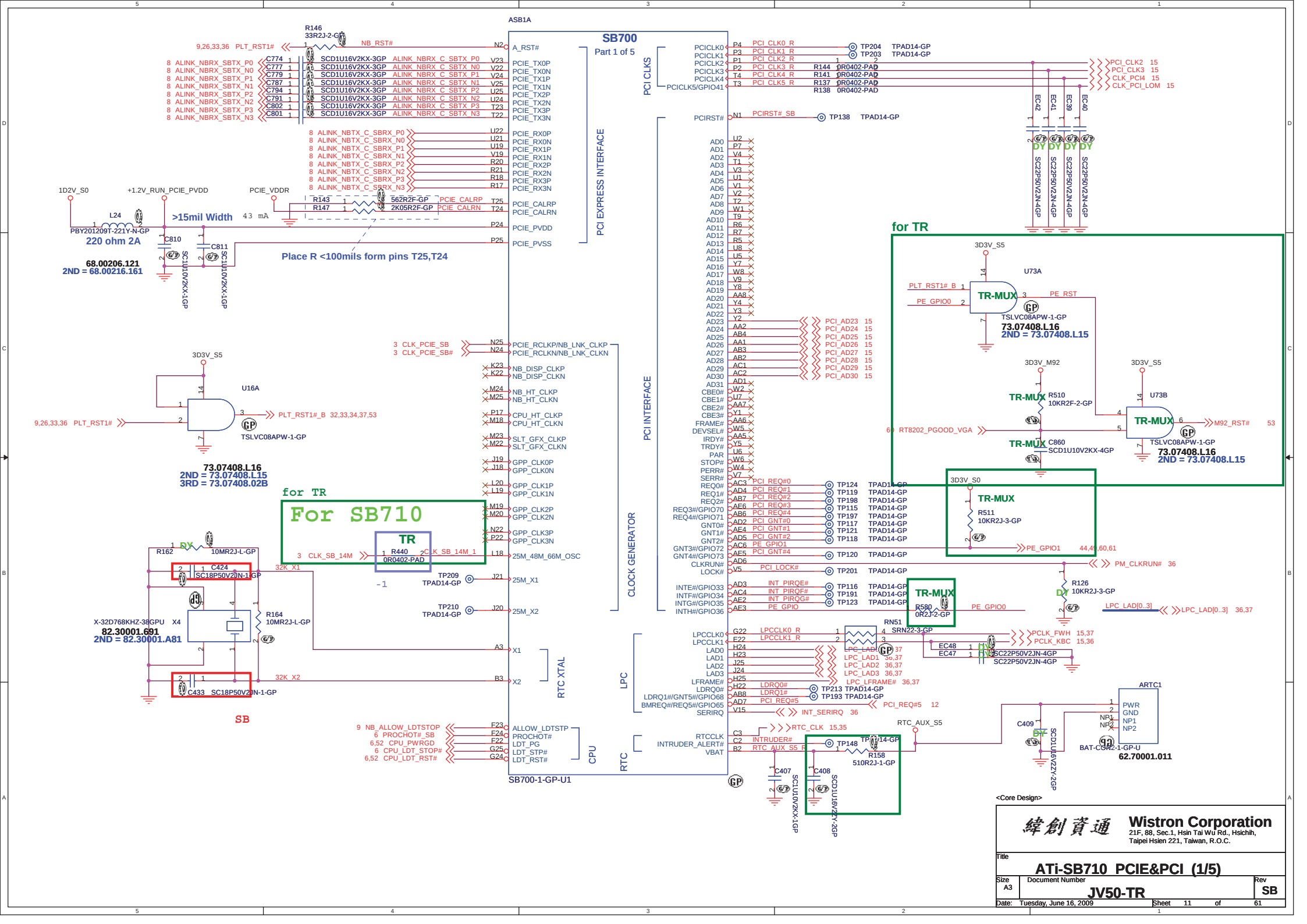
<Core Design>

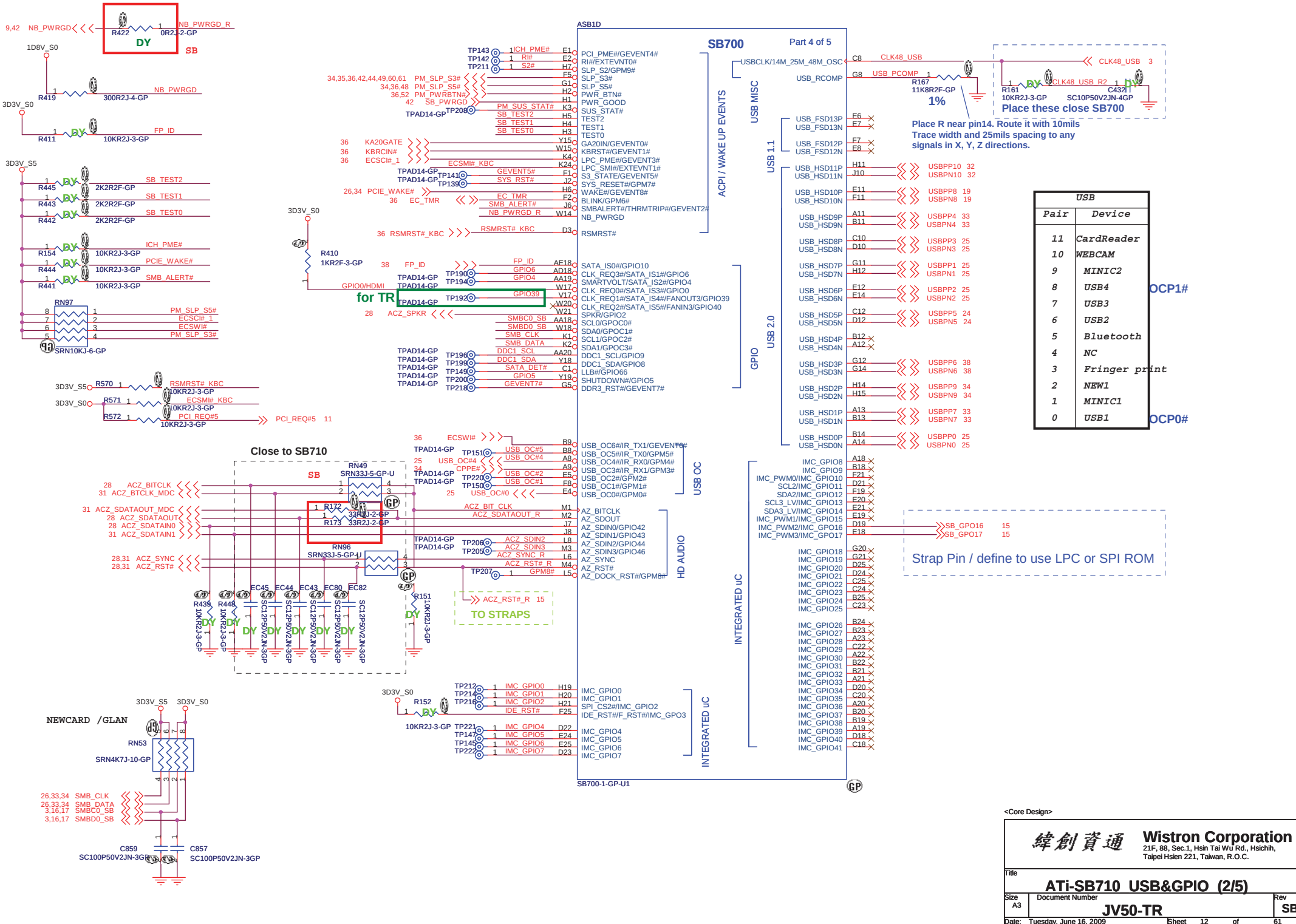
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CPU_Power_(4/4)**	
Size A3	Document Number **JV50-TR**	Rev **SB**
Date: Tuesday, June 16, 2009	Sheet 7 of 61	


ANB1A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780M-GP-U2
Placement: close RS780
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
ANB1B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS780M-GP-U2
Placement: close RS780
for TR
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
LAN
MINICARD1
MINICARD2
NEW CARD
A-LINK
Place < 100mils from pin AC8 and AB8
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS880M_HT LINK&PCIe(1/3)
Size A3
Document Number
JV50-TR
Rev SB
Date: Tuesday, June 16, 2009
Sheet 8 of 61


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
ANB1C
PART 3 OF 6
RS780M-GP-U2
CRT/TVOUT
LVTM
PLL
PWR
CLOCKs
PM
MIS.
Close to NB ball
R69 BOM Option PU
for TR
SB
ENABLE External CLK GEN
UMA-->L4-->2R 0603
C82-->47U/6.3V
DIS-->L4-->Bead
C82-->DY
TR-UMA_MUX
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS880M LVDS&CRT (2/3)
JV50-TR
Rev SB
Tuesday, June 16, 2009
Sheet 9 of 61


0.6A per ANT Rev1.1, Page3
0.45A per ANT Rev1.1, Page3
80mil Width
300mil Width
10A per ANT Rev1.1, Page3
Per check list (Rev 0.02)
RS780M: 1V ~ 1.1V, check PWR team
+NB_VCORE
ANB1E
PART 5/6
POWER
RS780M-GP-U2
ANB1F
PART 6/6
GROUND
ANB1D
PAR 4 OF 6
SBD_MEM/DVO_I/F
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS880M Side Port&PWR&GND(3/3)
Size A3
Document Number JV50-TR
Rev SB
Date: Tuesday, June 16, 2009
Sheet 10 of 61


ASB1A
SB700
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
SB700-1-GP-U1
for TR
For SB710
TR
for TR
TR-MUX
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
U16A
U73A
U73B
R510 10KR2F-2-GP
R511 10KR2J-3-GP
C860 SCD1U10V2KX-4GP
R126 10KR2J-3-GP
R580 0R2J-2-GP
RN51 SRN22-3-GP
R146 33R2J-2-GP
R143 562R2F-GP
R147 2K05R2F-GP
L24 PBY201209T-221Y-N-GP
220 ohm 2A
68.00206.121
2ND = 68.00216.161
>15mil Width
43 mA
Place R <100mils form pins T25,T24
R162 10MR2J-L-GP
R164 10MR2J-L-GP
R158 510R2J-1-GP
X-32D768KHZ-38GPU X4
82.30001.691
2ND = 82.30001.A81
C424 SC18P50V2JN-1-GP
C433 SC18P50V2JN-1-GP
SB
ARTC1
BAT-CON2-1-GP-U
62.70001.011
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB710 PCIE&PCI (1/5)
Size A3
Document Number JV50-TR
Rev SB
Date: Tuesday, June 16, 2009
Sheet 11 of 61


ASB1D
SB700
Part 4 of 5
SB700-1-GP-U1
USB MISC
USB 1.1
USB 2.0
GPIO
ACPI / WAKE UP EVENTS
USB OC
HD AUDIO
INTEGRATED uC
INTEGRATED uC
Close to SB710
SB
DY
SB
for TR
Place these close SB700
Place R near pin14. Route it with 10mils
Trace width and 25mils spacing to any
signals in X, Y, Z directions.
Strap Pin / define to use LPC or SPI ROM
TO STRAPS
NEWCARD /GLAN
USB
Pair
Device
11 CardReader
10 WEBCAM
9 MINIC2
8 USB4
7 USB3
6 USB2
5 Bluetooth
4 NC
3 Fringer print
2 NEW1
1 MINIC1
0 USB1
OCP1#
OCP0#
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB710 USB&GPIO (2/5)
Size A3
Document Number
JV50-TR
Rev SB
Date: Tuesday, June 16, 2009
Sheet 12 of 61

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB710

SATA HDD
SATA ODD

SB700
Part 2 of 5

SERIAL ATA
ATA 66/100/133
SPI ROM
SATA PWR
HW MONITOR

SB700-1-GP-U1

Very Close to SB710

1ST 82.30020.851
2ND = 82.30020.791
SB

Dummy CKG select

CLK_ID
(1,0)
ICS: 0,0
SEG: 0,1
RTM: 1,0

Layout connect to Cap then GND

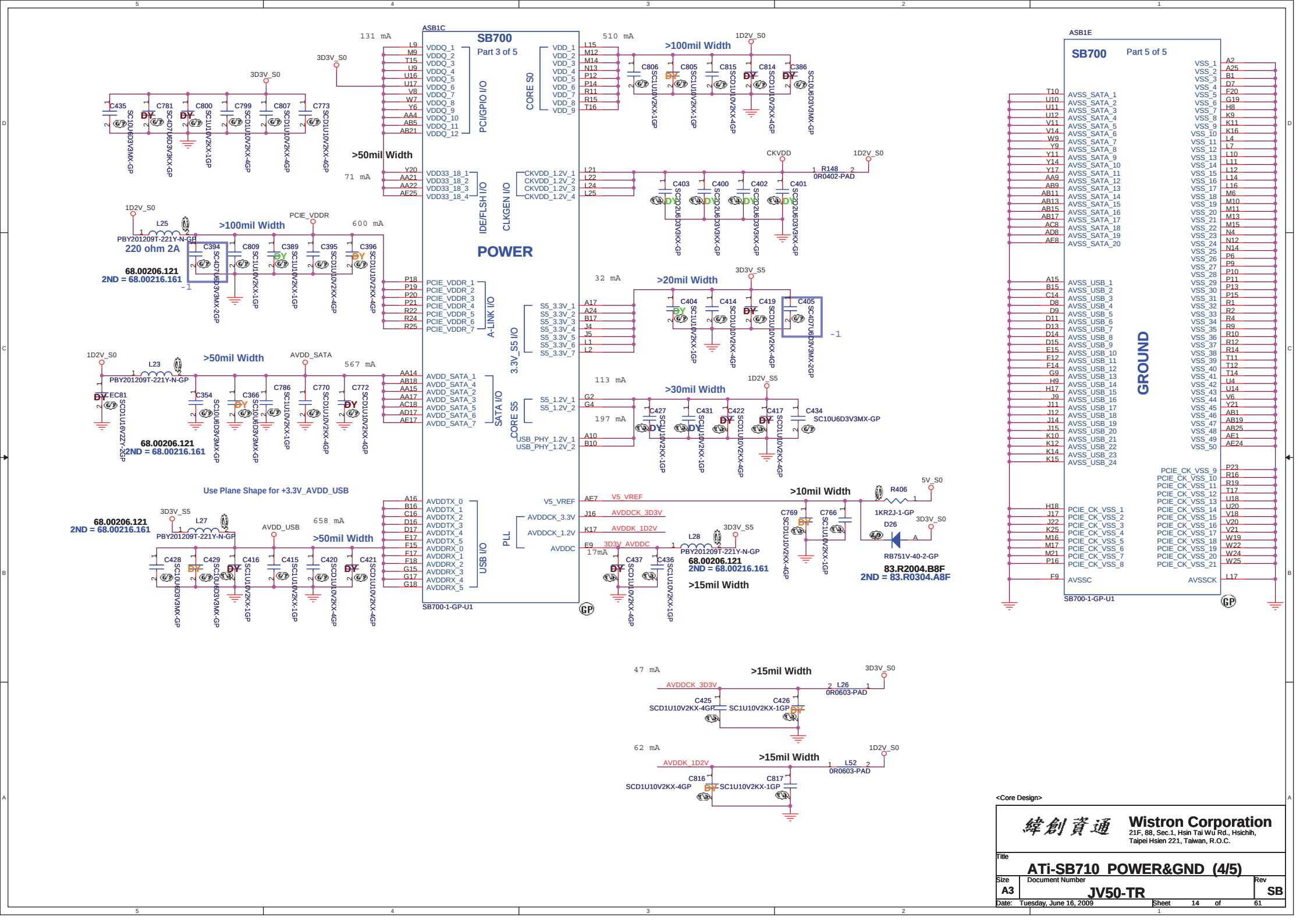
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB710 SATA-IDE (3/5)

Size	Document Number	Rev
A3	JV50-TR	SB

Date: Tuesday, June 16, 2009 Sheet 13 of 61


ASB1C
SB700
Part 3 of 5
POWER
131 mA
>50mil Width
71 mA
510 mA
>100mil Width
1D2V_S0
3D3V_S0
CKVDD
R148
0R0402-PAD
600 mA
PCIE_VDDR
220 ohm 2A
68.00206.121
2ND = 68.00216.161
32 mA
>20mil Width
3D3V_S5
113 mA
>30mil Width
1D2V_S5
197 mA
567 mA
AVDD_SATA
>50mil Width
Use Plane Shape for +3.3V_AVDD_USB
658 mA
AVDD_USB
17mA
>15mil Width
>10mil Width
5V_S0
1KR2J-1-GP
RB751V-40-2-GP
83.R2004.B8F
2ND = 83.R0304.A8F
47 mA
62 mA
L26
0R0603-PAD
L52
0R0603-PAD
VDDQ_1
VDDQ_2
VDDQ_3
VDDQ_4
VDDQ_5
VDDQ_6
VDDQ_7
VDDQ_8
VDDQ_9
VDDQ_10
VDDQ_11
VDDQ_12
VDD_1
VDD_2
VDD_3
VDD_4
VDD_5
VDD_6
VDD_7
VDD_8
VDD_9
PCI/GPIO I/O
CORE S0
VDD33_18_1
VDD33_18_2
VDD33_18_3
VDD33_18_4
IDE/FLSH I/O
CKVDD_1.2V_1
CKVDD_1.2V_2
CKVDD_1.2V_3
CKVDD_1.2V_4
CLKGEN I/O
PCIE_VDDR_1
PCIE_VDDR_2
PCIE_VDDR_3
PCIE_VDDR_4
PCIE_VDDR_5
PCIE_VDDR_6
PCIE_VDDR_7
A-LINK I/O
S5_3.3V_1
S5_3.3V_2
S5_3.3V_3
S5_3.3V_4
S5_3.3V_5
S5_3.3V_6
S5_3.3V_7
3.3V_S5 I/O
S5_1.2V_1
S5_1.2V_2
CORE S5
USB_PHY_1.2V_1
USB_PHY_1.2V_2
SATA I/O
AVDD_SATA_1
AVDD_SATA_4
AVDD_SATA_2
AVDD_SATA_3
AVDD_SATA_5
AVDD_SATA_6
AVDD_SATA_7
AVDDTX_0
AVDDTX_1
AVDDTX_2
AVDDTX_3
AVDDTX_4
AVDDTX_5
AVDDRX_0
AVDDRX_1
AVDDRX_2
AVDDRX_3
AVDDRX_4
AVDDRX_5
USB I/O
V5_VREF
AVDDCK_3.3V
AVDDCK_1.2V
AVDDC
PLL
AVDDCK_3D3V
AVDDK_1D2V
3D3V_AVDD
SB700-1-GP-U1
ASB1E
SB700
Part 5 of 5
GROUND
AVSS_SATA_1
AVSS_SATA_2
AVSS_SATA_3
AVSS_SATA_4
AVSS_SATA_5
AVSS_SATA_6
AVSS_SATA_7
AVSS_SATA_8
AVSS_SATA_9
AVSS_SATA_10
AVSS_SATA_11
AVSS_SATA_12
AVSS_SATA_13
AVSS_SATA_14
AVSS_SATA_15
AVSS_SATA_16
AVSS_SATA_17
AVSS_SATA_18
AVSS_SATA_19
AVSS_SATA_20
AVSS_USB_1
AVSS_USB_2
AVSS_USB_3
AVSS_USB_4
AVSS_USB_5
AVSS_USB_6
AVSS_USB_7
AVSS_USB_8
AVSS_USB_9
AVSS_USB_10
AVSS_USB_11
AVSS_USB_12
AVSS_USB_13
AVSS_USB_14
AVSS_USB_15
AVSS_USB_16
AVSS_USB_17
AVSS_USB_18
AVSS_USB_19
AVSS_USB_20
AVSS_USB_21
AVSS_USB_22
AVSS_USB_23
AVSS_USB_24
PCIE_CK_VSS_1
PCIE_CK_VSS_2
PCIE_CK_VSS_3
PCIE_CK_VSS_4
PCIE_CK_VSS_5
PCIE_CK_VSS_6
PCIE_CK_VSS_7
PCIE_CK_VSS_8
AVSSC
PCIE_CK_VSS_9
PCIE_CK_VSS_10
PCIE_CK_VSS_11
PCIE_CK_VSS_12
PCIE_CK_VSS_13
PCIE_CK_VSS_14
PCIE_CK_VSS_15
PCIE_CK_VSS_16
PCIE_CK_VSS_17
PCIE_CK_VSS_18
PCIE_CK_VSS_19
PCIE_CK_VSS_20
PCIE_CK_VSS_21
AVSSCK
VSS_1
VSS_2
VSS_3
VSS_4
VSS_5
VSS_6
VSS_7
VSS_8
VSS_9
VSS_10
VSS_11
VSS_12
VSS_13
VSS_14
VSS_15
VSS_16
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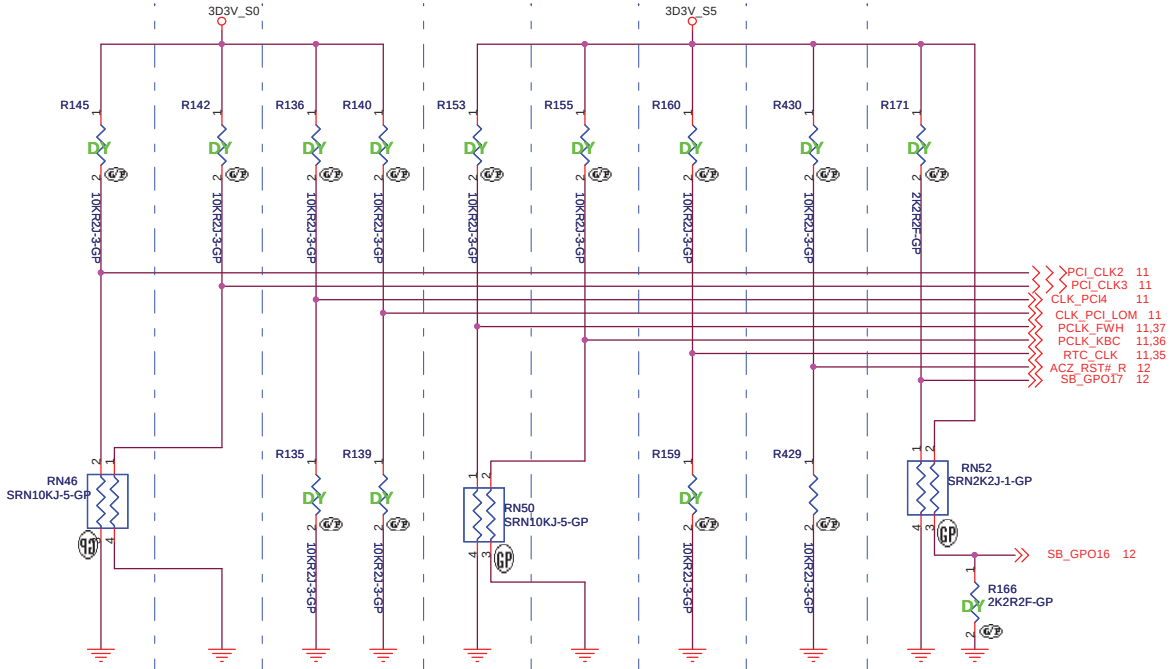
VSS_40
VSS_41
VSS_42
VSS_43
VSS_44
VSS_45
VSS_46
VSS_47
VSS_48
VSS_49
VSS_50
SB700-1-GP-U1
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB710 POWER&GND (4/5)
Size
A3
Document Number
JV50-TR
Rev
SB
Date: Tuesday, June 16, 2009
Sheet 14 of 61

REQUIRED STRAPS

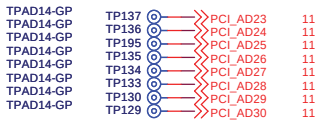
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM DEFAULT L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

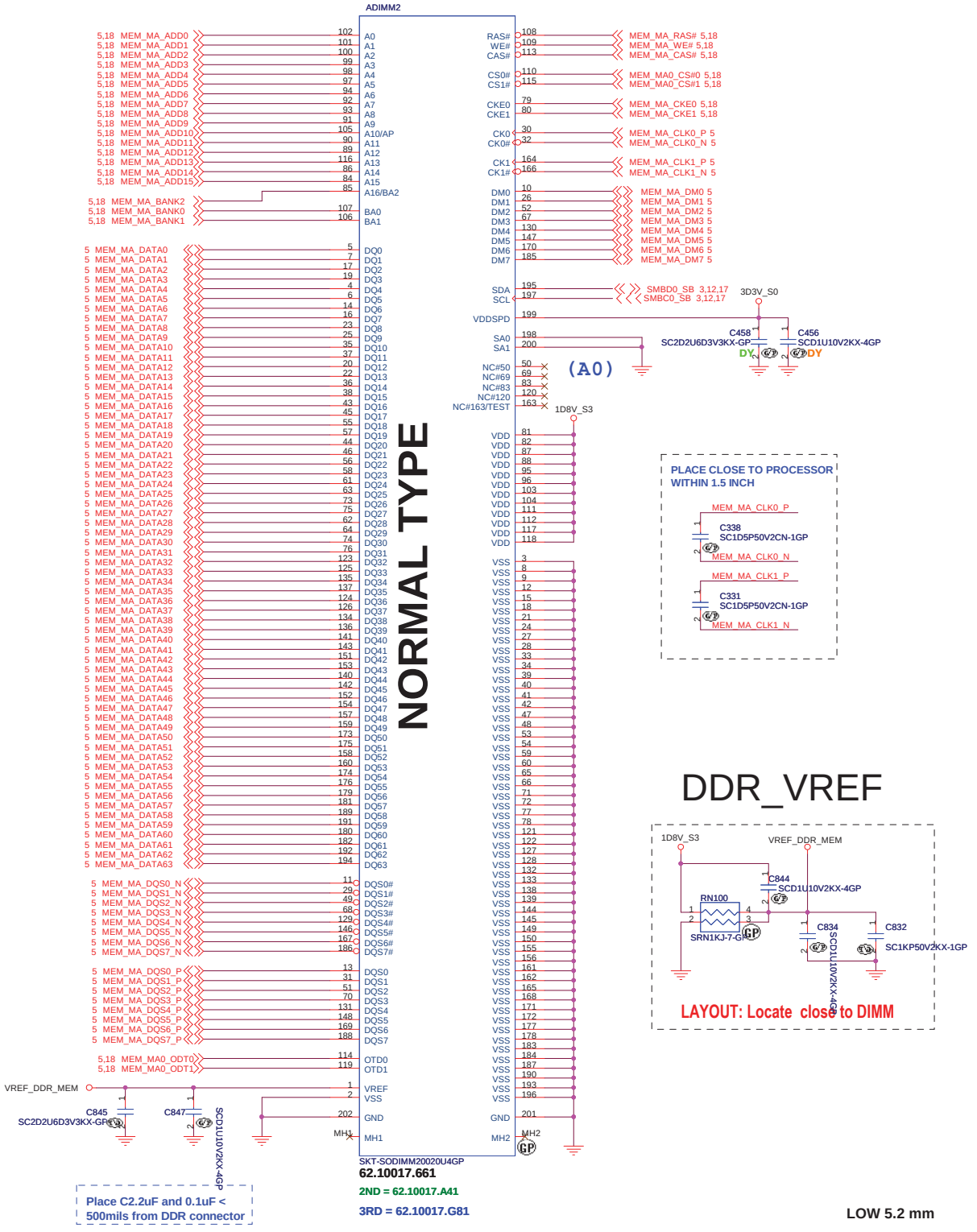
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB710 STRAPPING (5/5)

Size: A3 | Document Number: JV50-TR | Rev: SB

Date: Tuesday, June 16, 2009 | Sheet 15 of 61



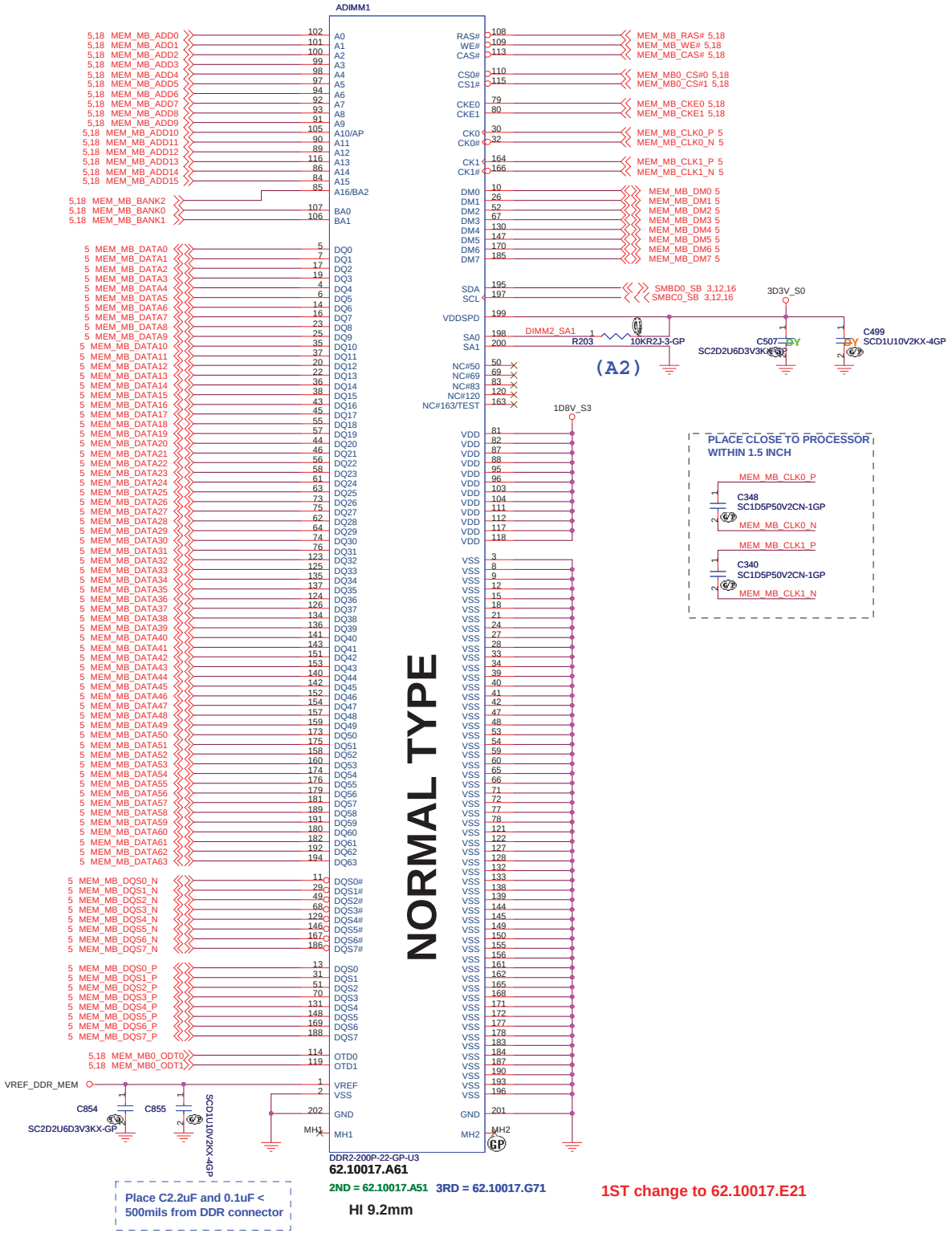
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_1

Size: Custom | Document Number: JV50-TR | Rev: SB

Date: Tuesday, June 16, 2009 | Sheet 16 of 61



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

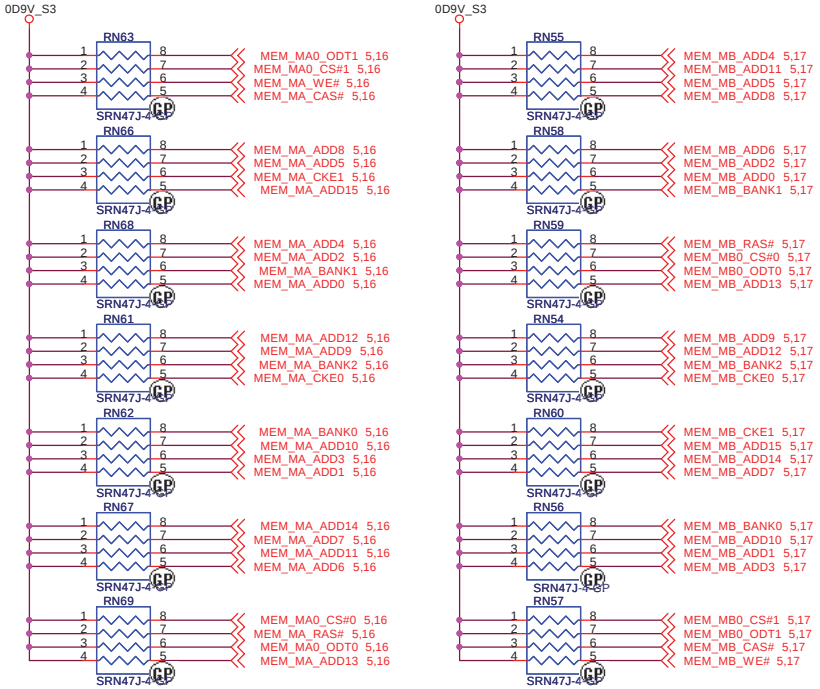
Title: DDR_SO-DIMM SKT_2

Size	Document Number	Rev
Custom	JV50-TR	SB

Date: Tuesday, June 16, 2009 Sheet 17 of 61

PARALLEL TERMINATION

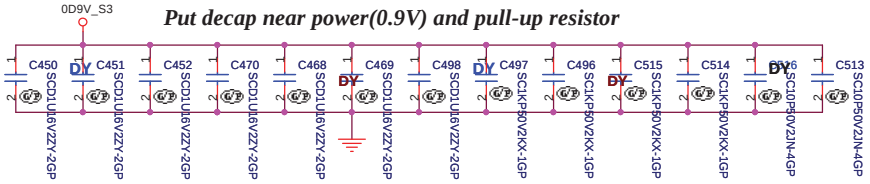
Put decap near power(0.9V) and pull-up resistor



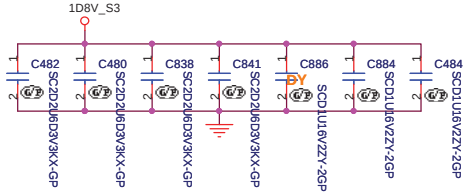
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

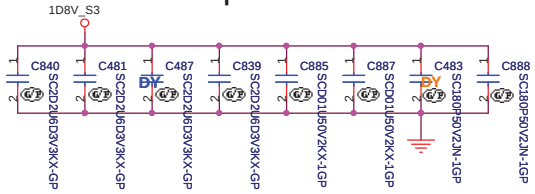


Place these Caps near DM1



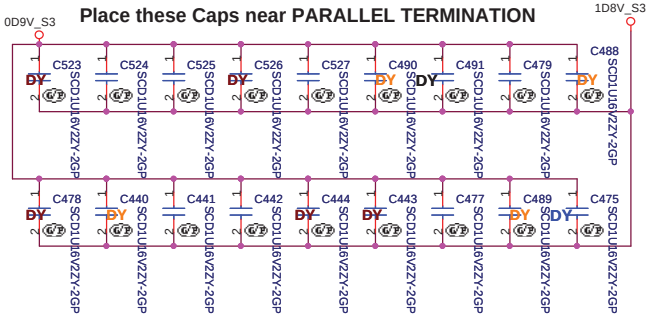
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



<Core Design>

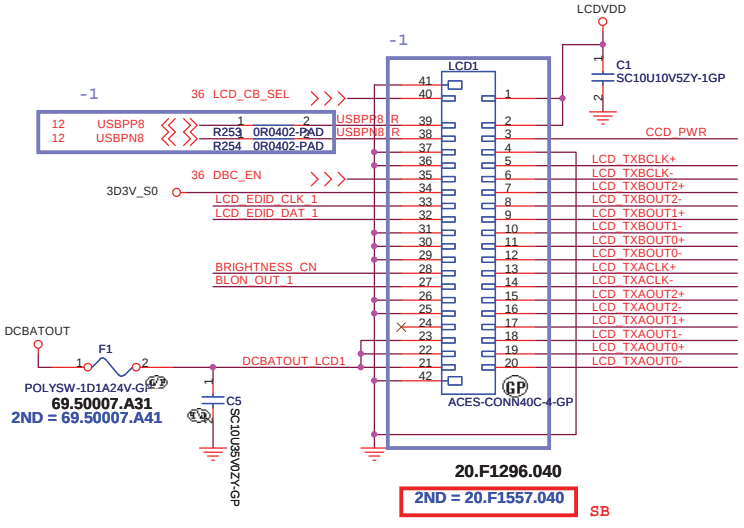
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

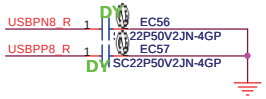
Title: **DDR_DAMPING & TERMINATION**

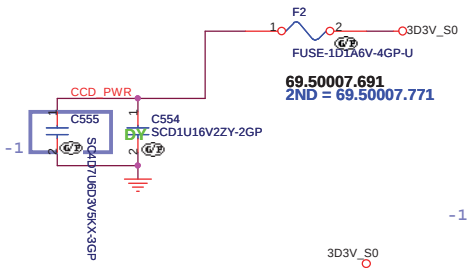
Size	Document Number	Rev
A3	JV50-TR	SB

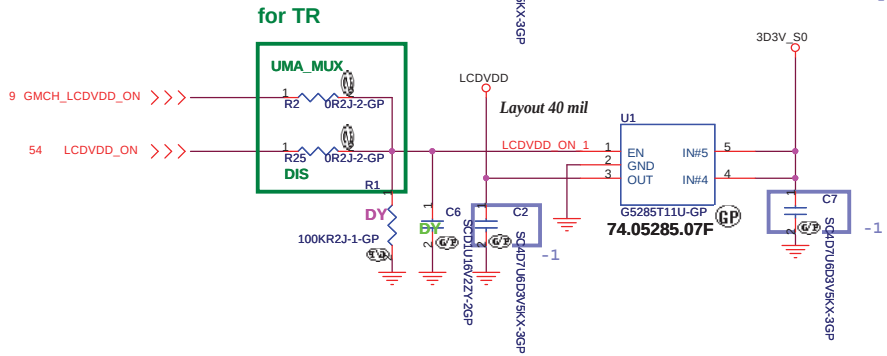
Date: Tuesday, June 16, 2009 Sheet 18 of 61

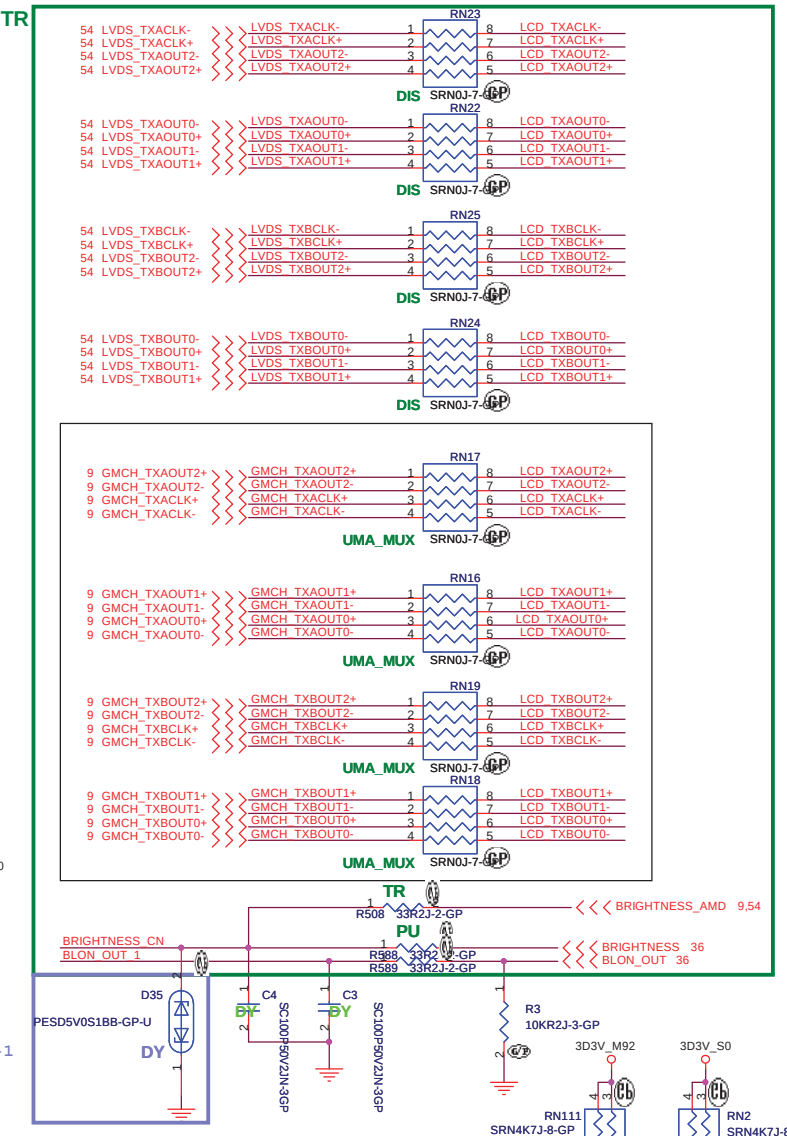
LCD/INVERTER/CCD CONN











Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

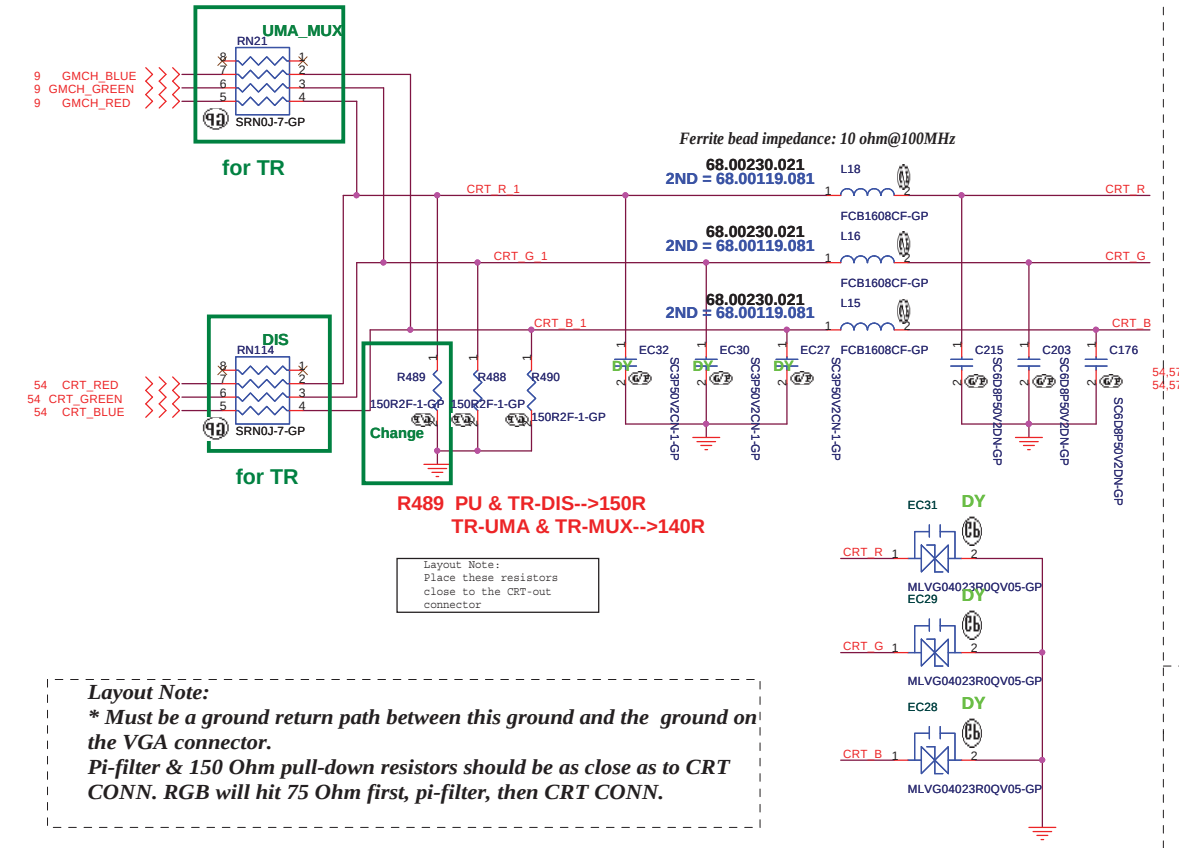
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

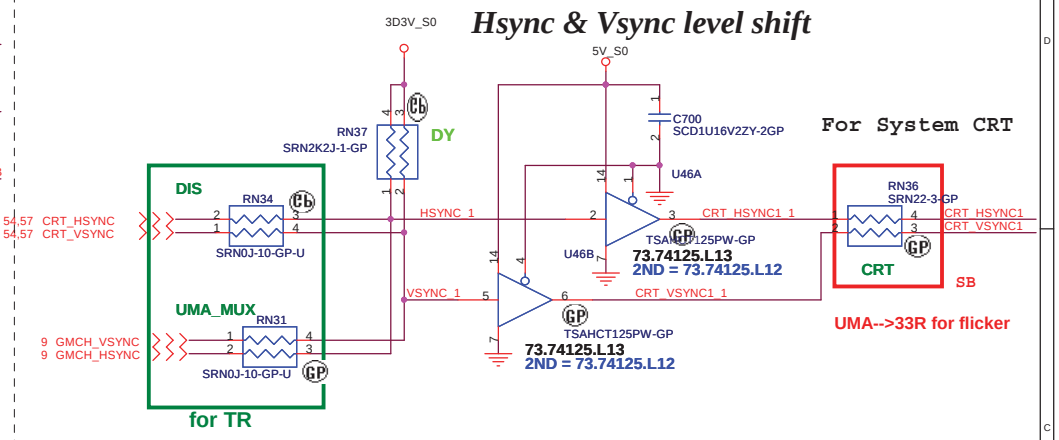
Title: LCD CONN

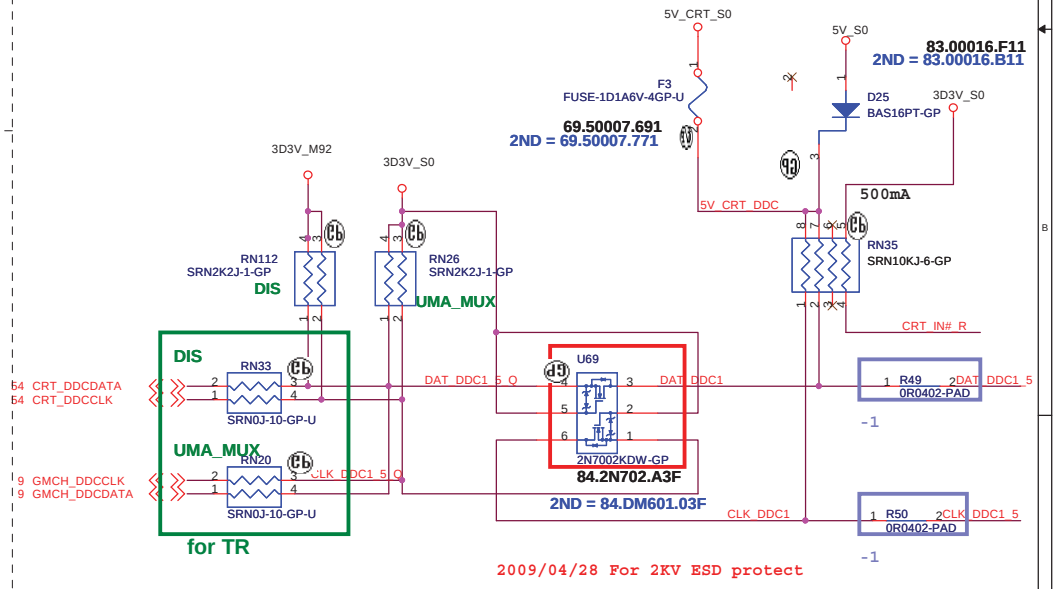
Size: A3 | Document Number: JV50-TR | Rev: SB

Date: Tuesday, June 16, 2009 | Sheet 19 of 61

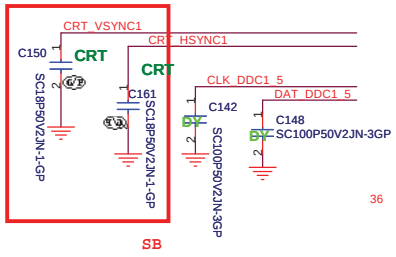


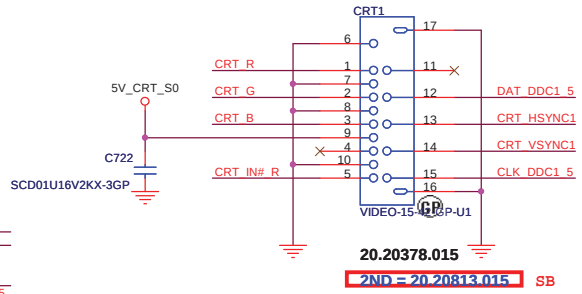
Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

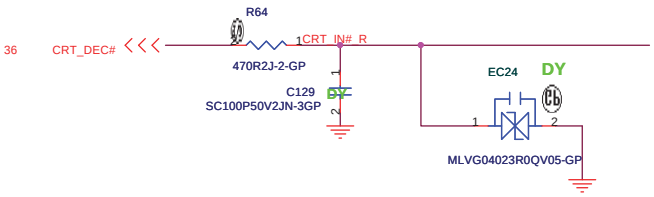




CRT I/F & CONNECTOR



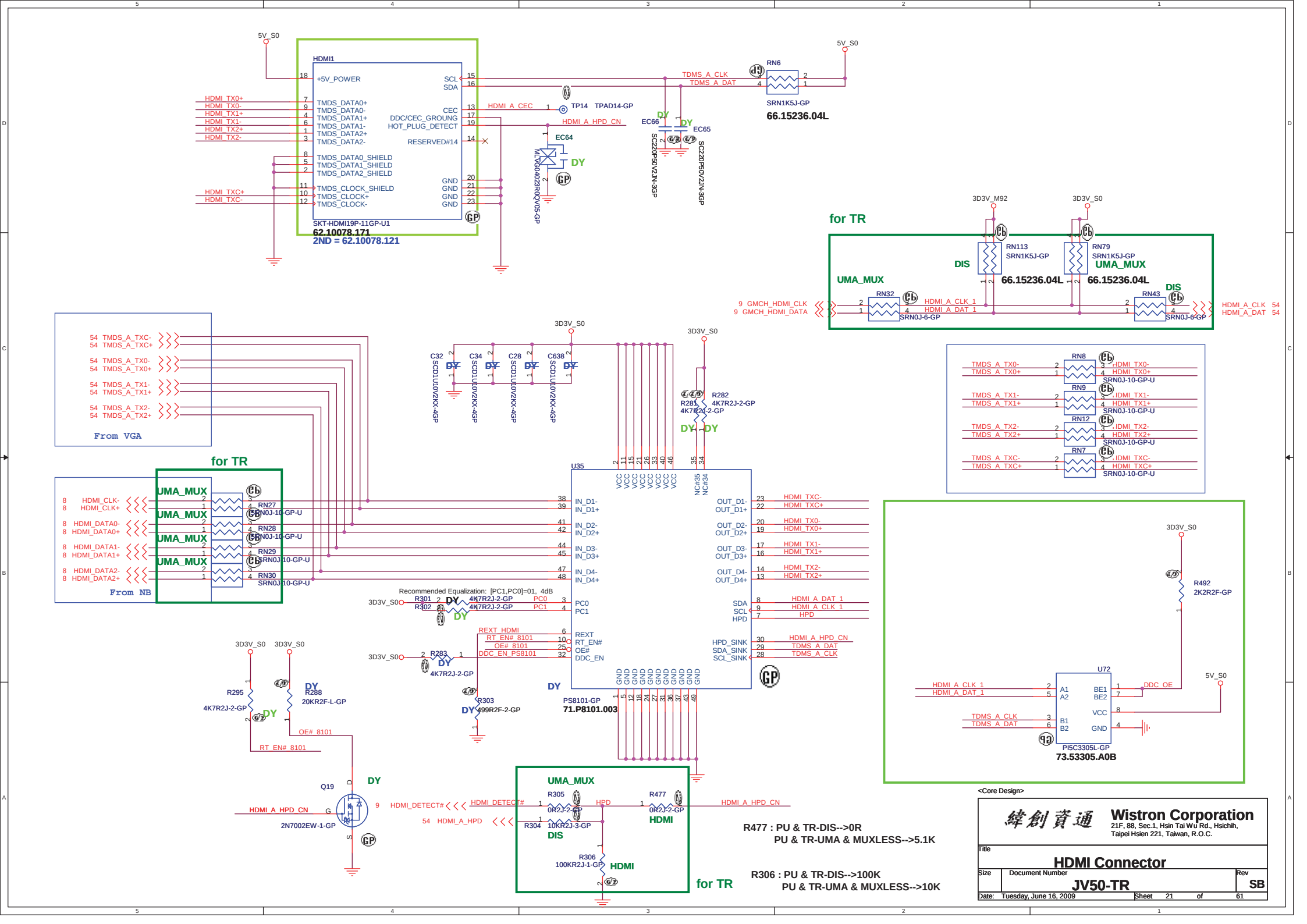




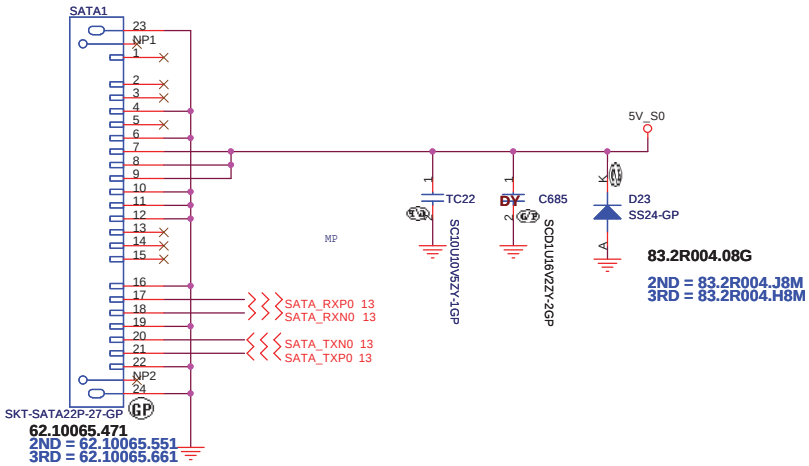
UMA-->C150, C161 DY for flicker

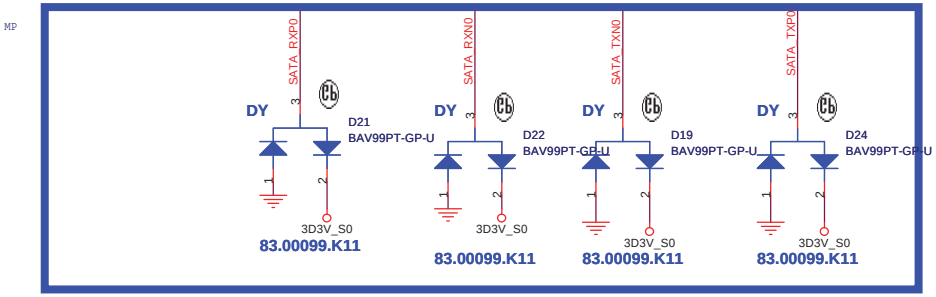
<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector
Size: | Document Number: JV50-TR | Rev: SB
Date: Tuesday, June 16, 2009 | Sheet 20 of 61


HDMI1
SKT-HDMI19P-11GP-U1
62.10078.171
2ND = 62.10078.121
RN6
SRN1K5J-GP
66.15236.04L
TP14 TPAD14-GP
EC64
EC65
EC66
SC220P50V2JN-3GP
MLVG0402S3R0QV05-GP
for TR
UMA_MUX
DIS
RN113
RN79
RN32
RN43
SRN0J-6-GP
3D3V_M92
3D3V_S0
From VGA
From NB
RN27
RN28
RN29
RN30
SRN0J-10-GP-U
RN8
RN9
RN12
RN7
SRN0J-10-GP-U
U35
PS8101-GP
71.P8101.003
Recommended Equalization: [PC1,PC0]=01, 4dB
R301
R302
R283
R303
R295
R288
20KR2F-L-GP
Q19
2N7002EW-1-GP
R305
R306
R304
R477
HDMI
R492
2K2R2F-GP
U72
PI5C3305L-GP
73.53305.A0B
R477 : PU & TR-DIS-->0R
PU & TR-UMA & MUXLESS-->5.1K
R306 : PU & TR-DIS-->100K
PU & TR-UMA & MUXLESS-->10K
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI Connector
Size
Document Number
JV50-TR
Rev
SB
Date: Tuesday, June 16, 2009
Sheet 21 of 61

SATA Connector



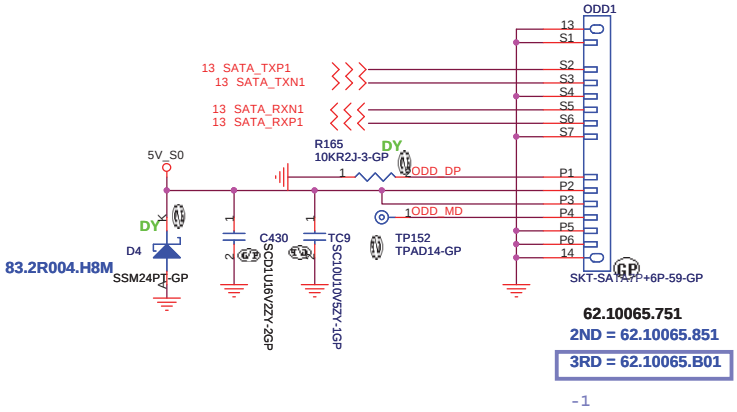


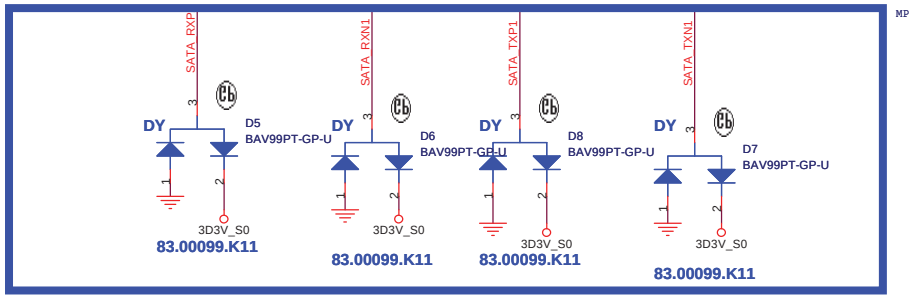
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD		
Size	Document Number: JV50-TR	Rev: SB
Date: Tuesday, June 16, 2009	Sheet 22 of 61	

SATA ODD Connector





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

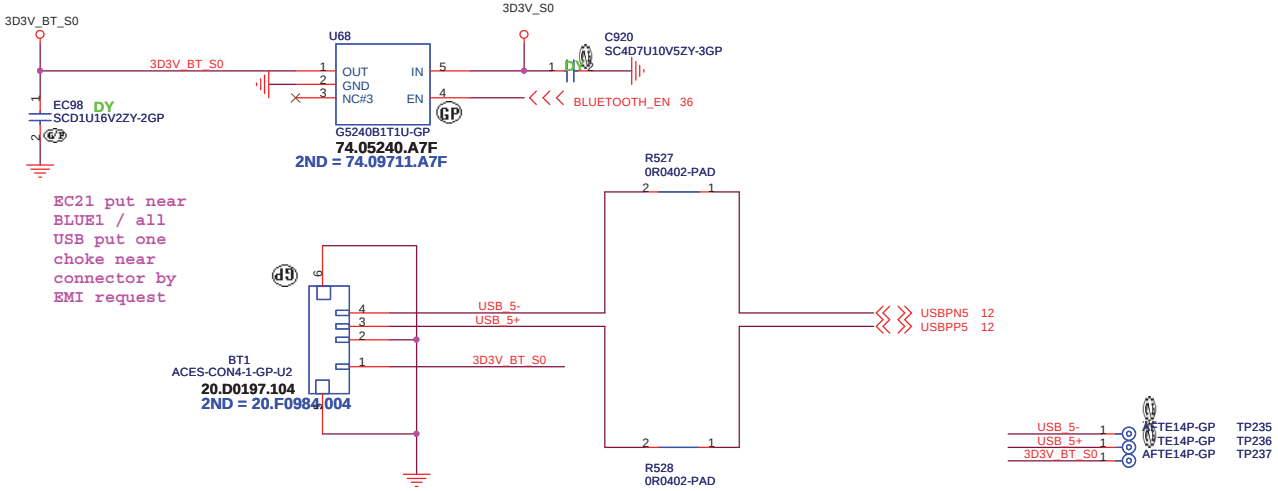
Title: ODD

Size | Document Number: JV50-TR | Rev: SB

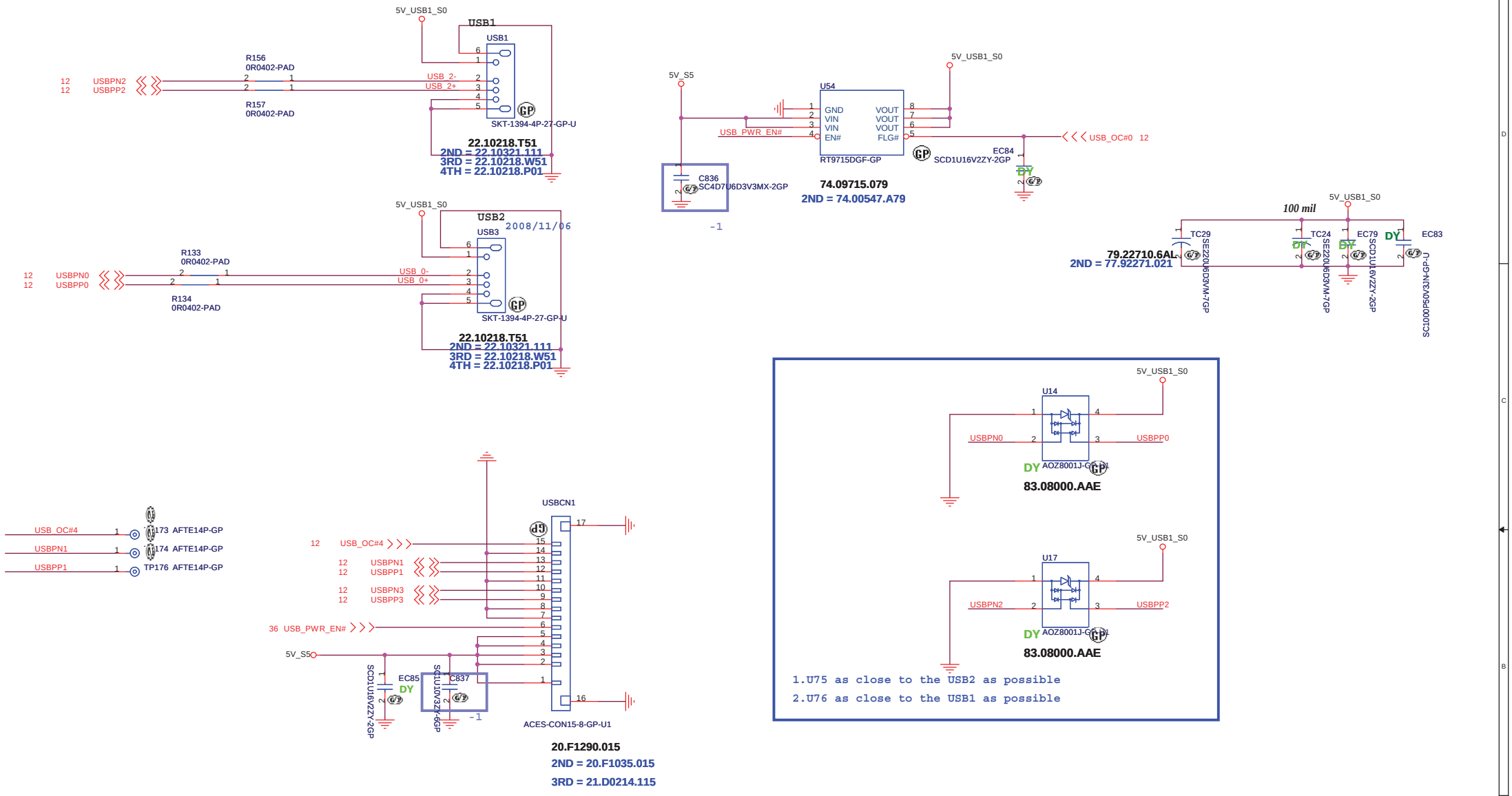
Date: Tuesday, June 16, 2009 | Sheet 23 of 61

BLUETOOTH MODULE

1.5A / High Active Voltage 2V



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BLUETOOTH		
Size	Document Number: JV50-TR	Rev: SB
Date: Tuesday, June 16, 2009	Sheet 24 of 61	



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**USB**	
Size	Document Number **JV50-TR**	Rev **SB**
Date: Tuesday, June 16, 2009	Sheet 25 of 61	

CO-Layout BCM5764 and BCM5784
modify BOM :71.05784.M03

U4
BCM5764MKMLG-GP
71.05764.M01

Place PLLVDD/AVDDL
CKT as close to chip as
possible

1ST 82.30020.851
2ND = 82.30020.791
SB

1ST 84.DCP69.01B
2ND = 84.00069.B1B

U3
AT24C02BN-SH-T-GP
72.24C02.R01
2ND = 72.24C02.M01

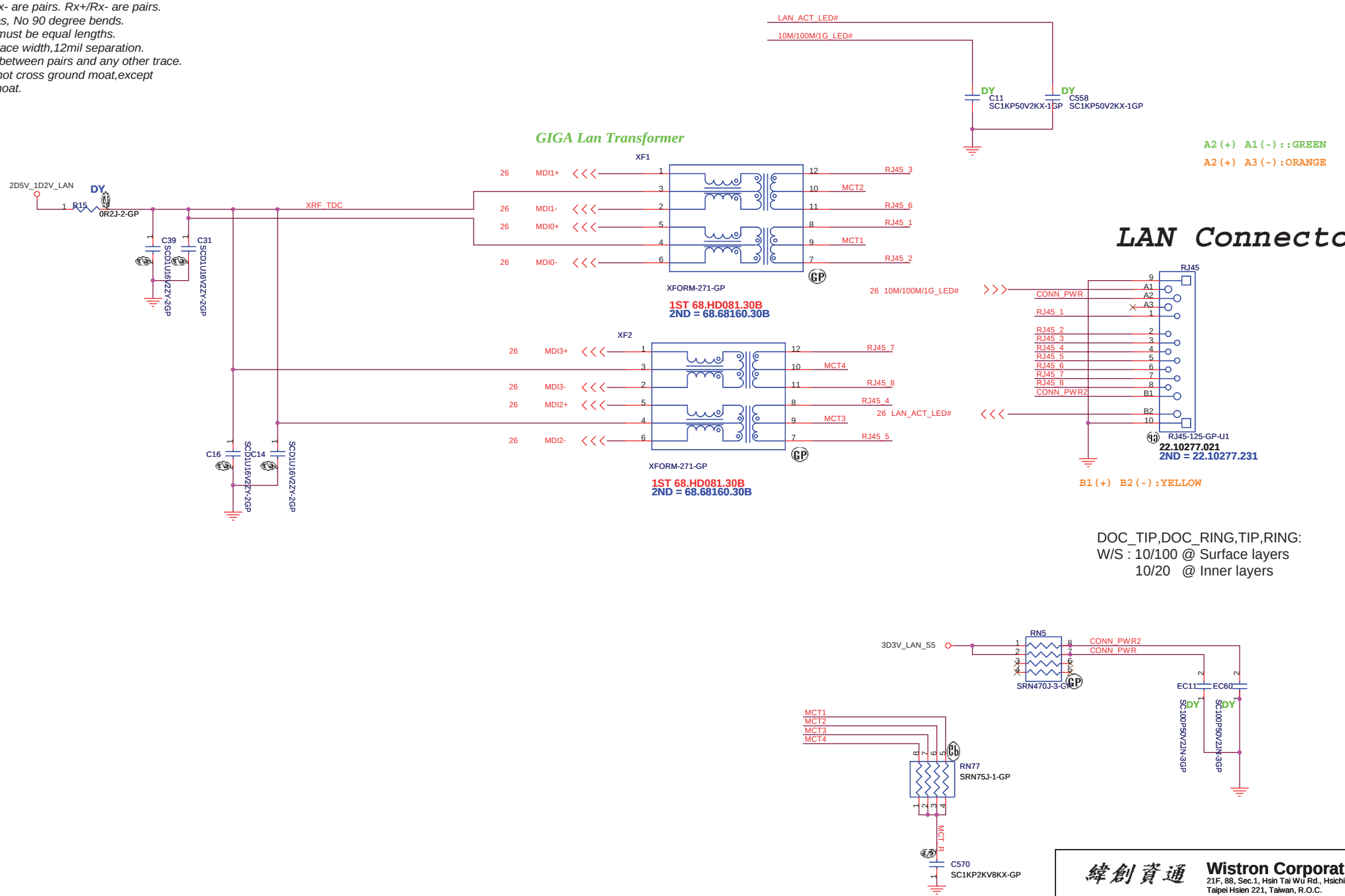
SRN4K7J-10-GP
SRN1KJ-10-GP

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

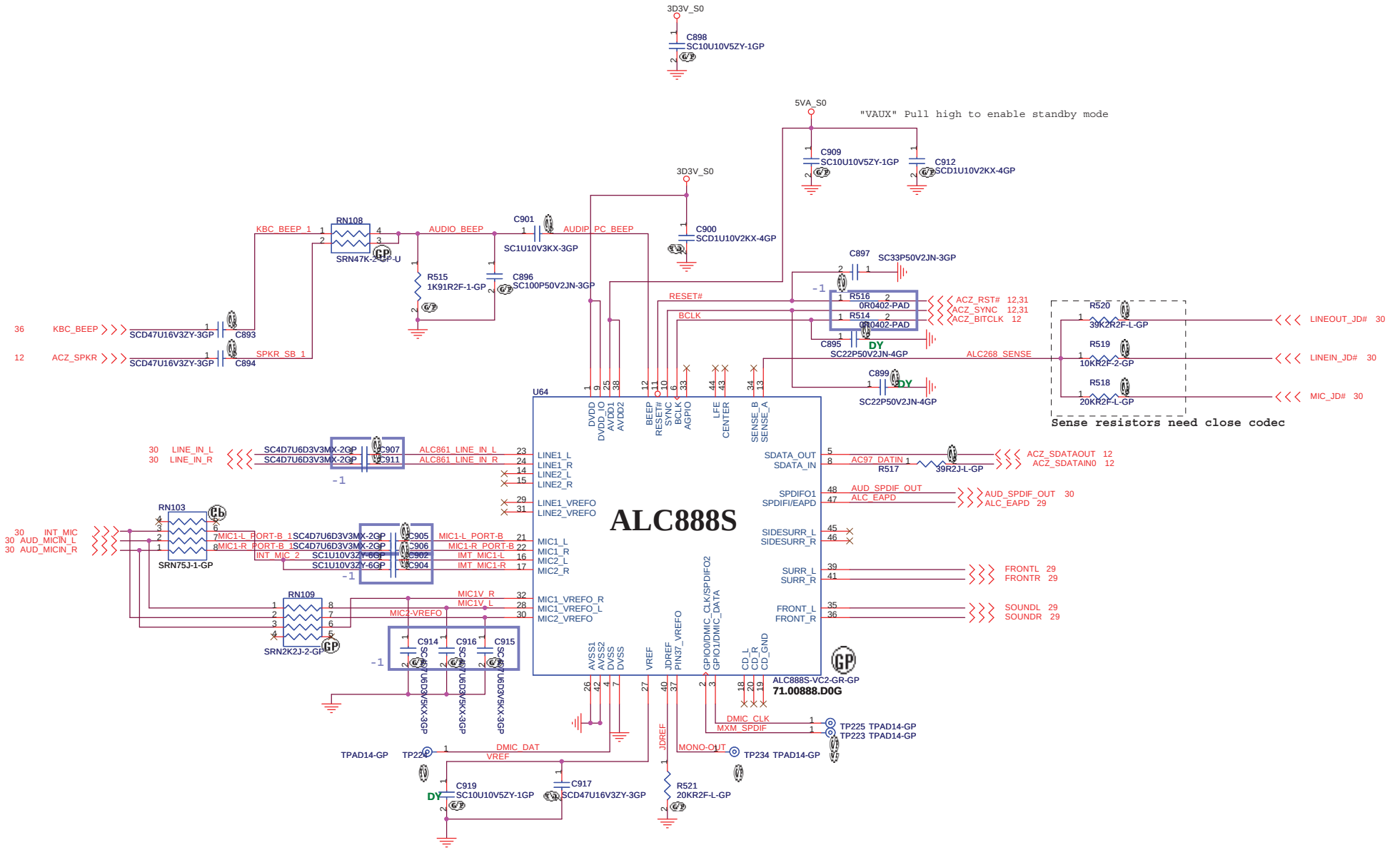
Title	BCM5764MKMLG	
Size A3	Document Number JV50-TR	Rev SB
Date: Tuesday, June 16, 2009	Sheet 26 of 61	

LAN Connector

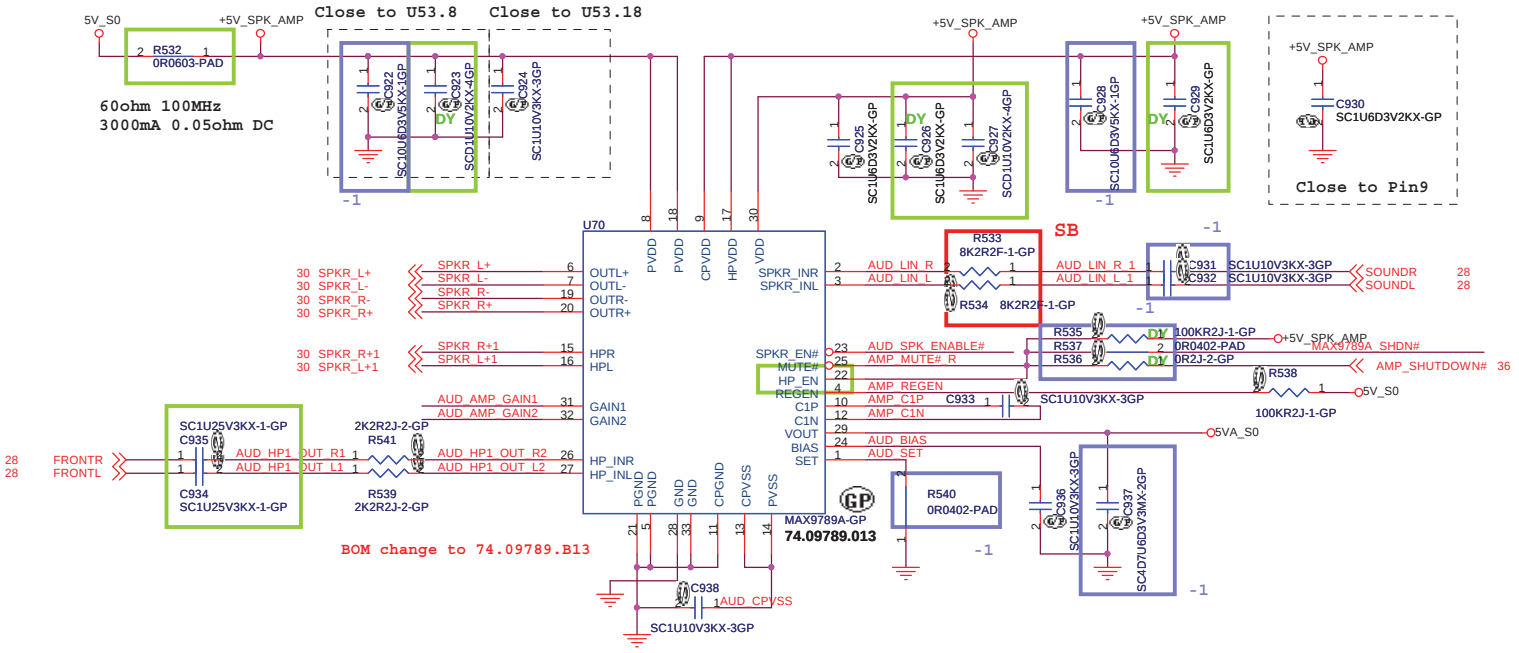
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

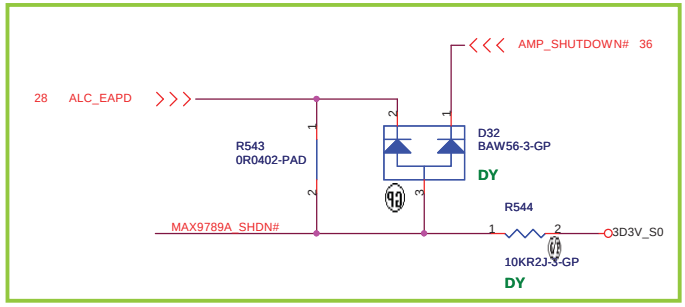


緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LAN CONN	
Size A3	Document Number JV50-TR	Rev SB
Date: Tuesday, June 16, 2009	Sheet 27 of 61	

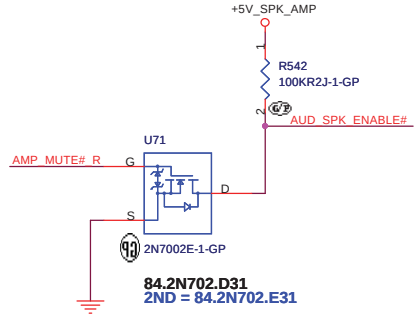


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Azalia codec ALC888**	
Size A3	Document Number **JV50-TR**	Rev **SB**
Date: Tuesday, June 16, 2009	Sheet 28 of 61	

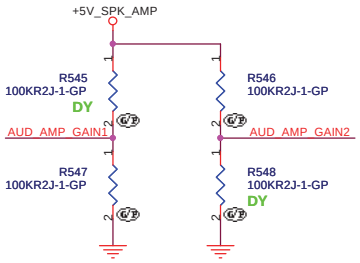




Signal inverter for speaker shutdown



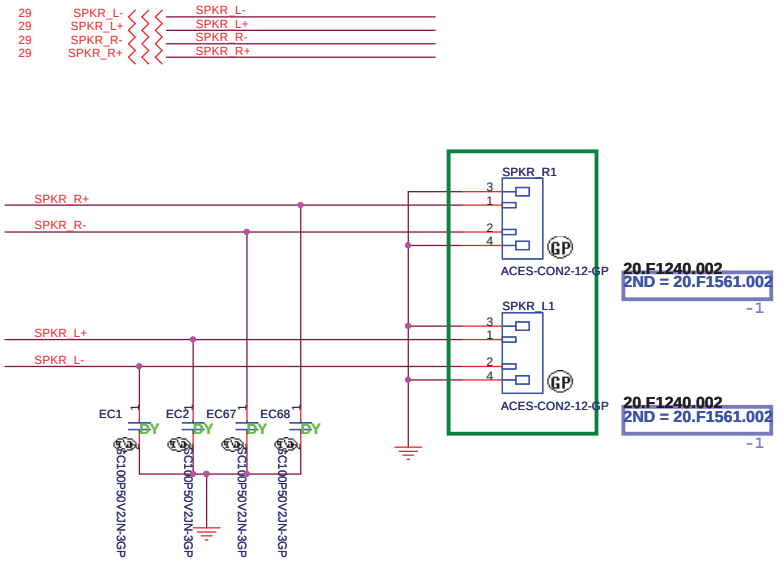
GAIN SETTING



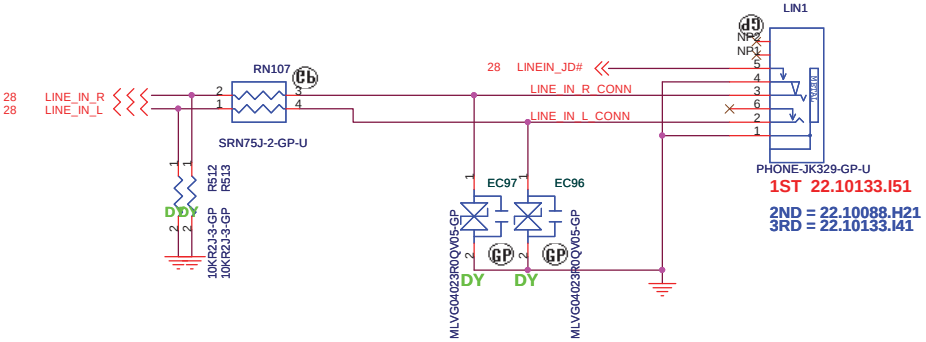
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**AUDIO AMP**
Size	Document Number: **JV50-TR** — Rev: **SB**
Date: Tuesday, June 16, 2009	Sheet 29 of 61

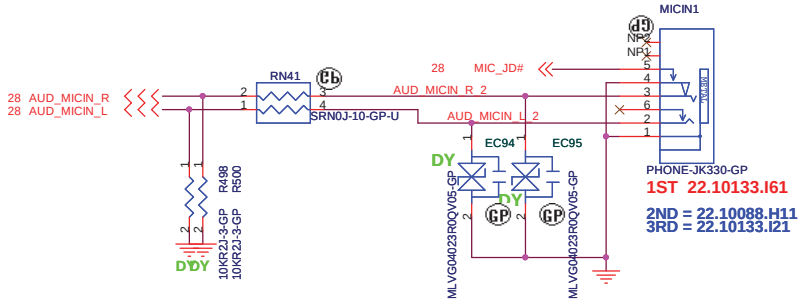
Internal Speaker

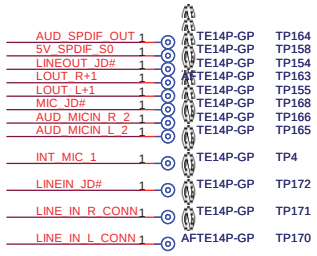


LINE IN

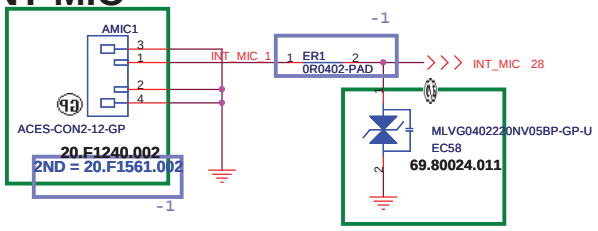


MIC IN

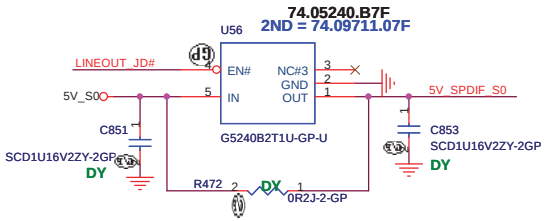


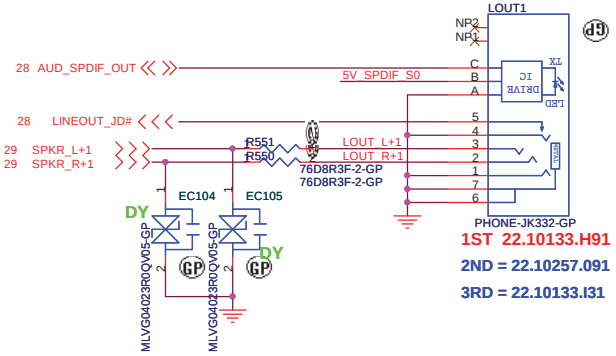


INT MIC



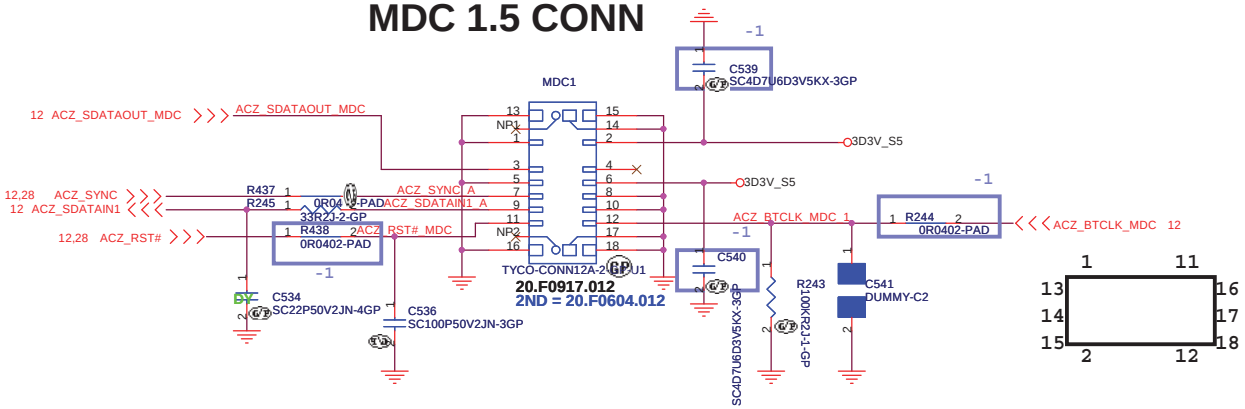
LINE OUT



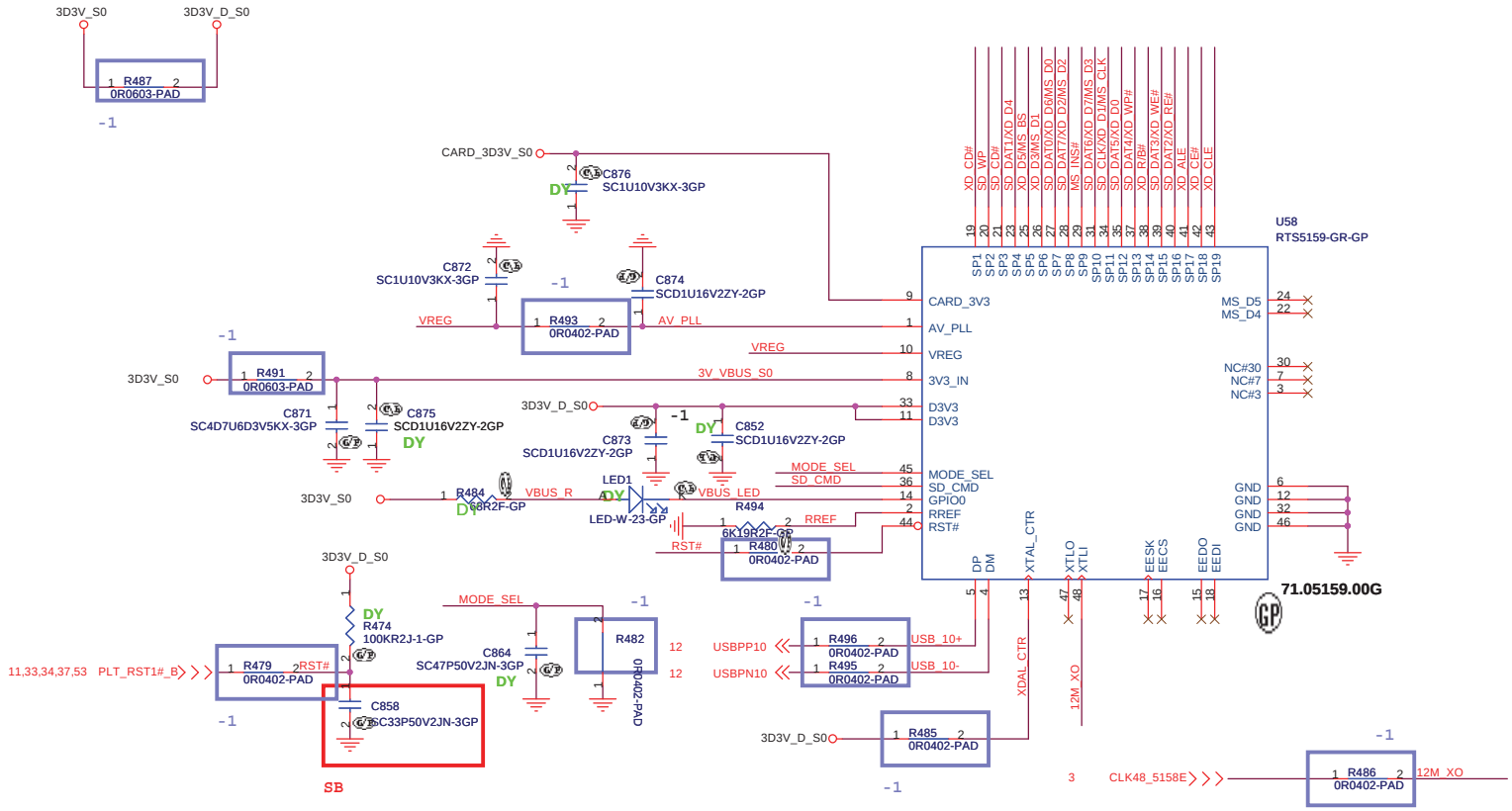


緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO JACK		
Size	Document Number: JV50-TR	Rev: SB
Date: Tuesday, June 16, 2009	Sheet 30 of 61	

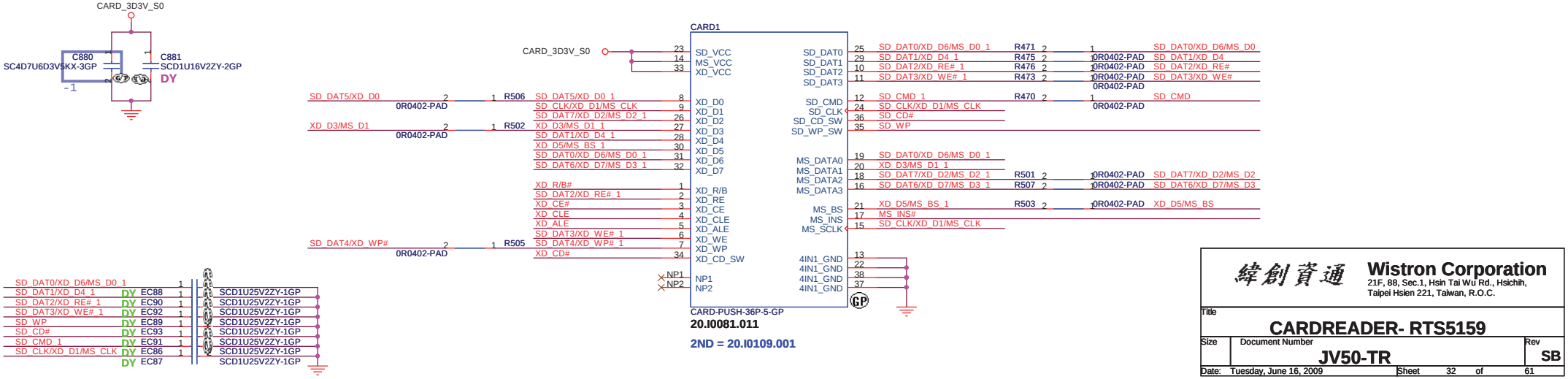
MDC 1.5 CONN



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MDC		
Size	Document Number: JV50-TR	Rev: SB
Date: Tuesday, June 16, 2009	Sheet 31 of 61	



5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



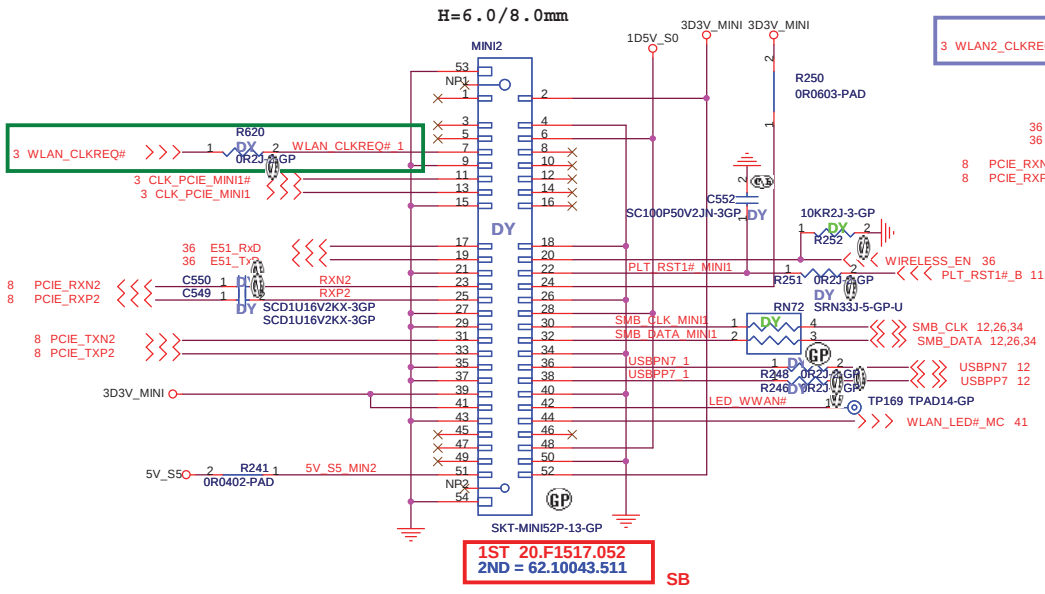
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

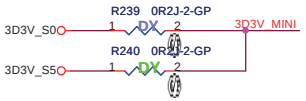
Title: CARDREADER- RTS5159

Size | Document Number: JV50-TR | Rev: SB

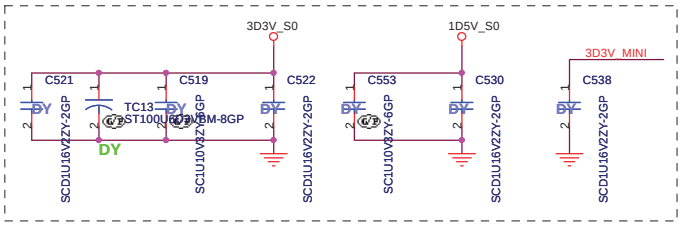
Date: Tuesday, June 16, 2009 | Sheet 32 of 61

Mini Card Connector(WLAN)

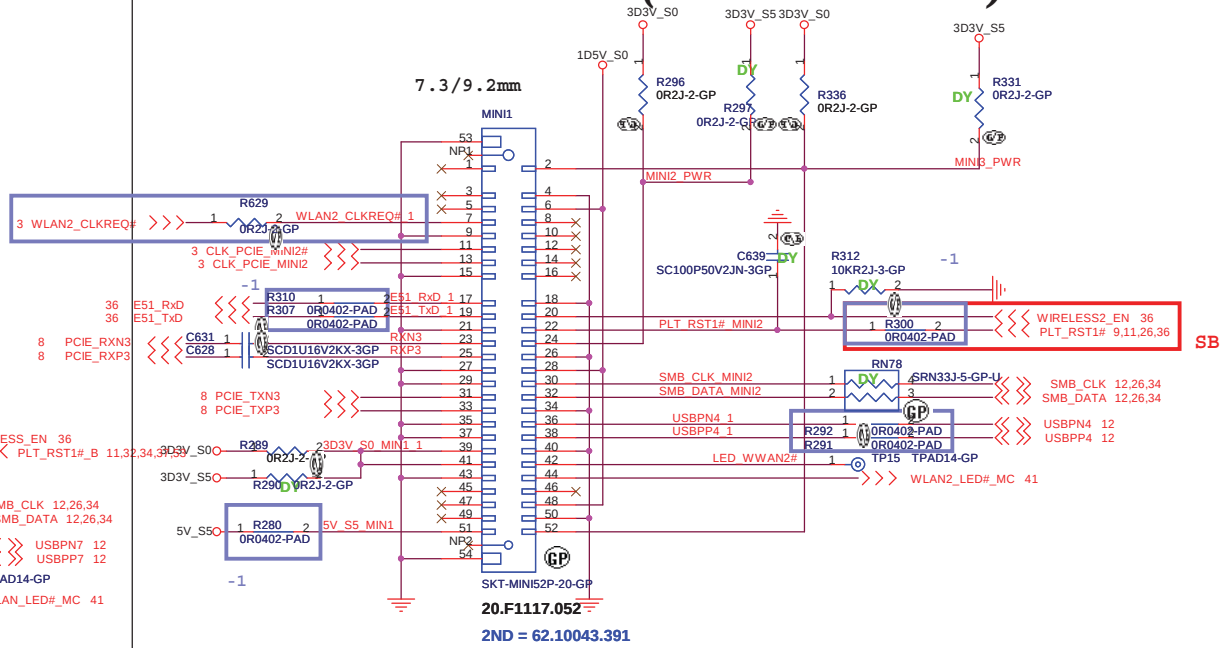




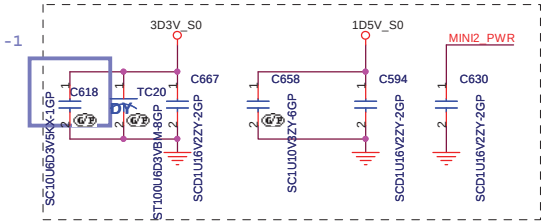
Place near MINI2



Mini Card Connector(Robson2 and 3G)

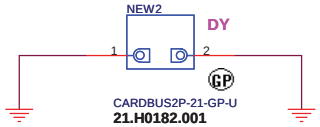


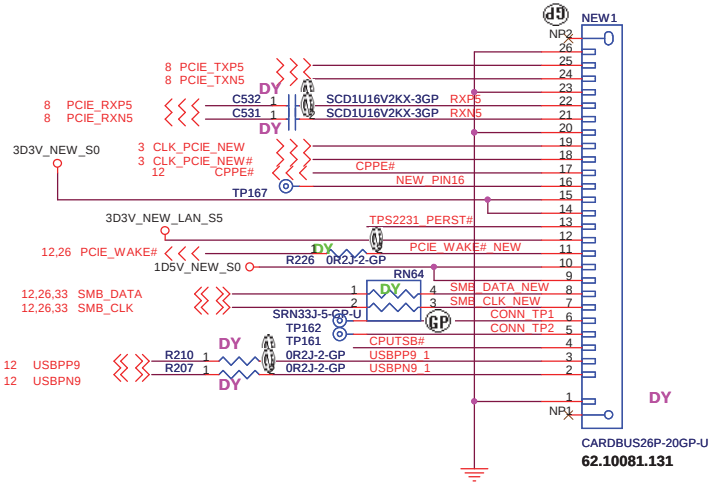
Place near MINI1

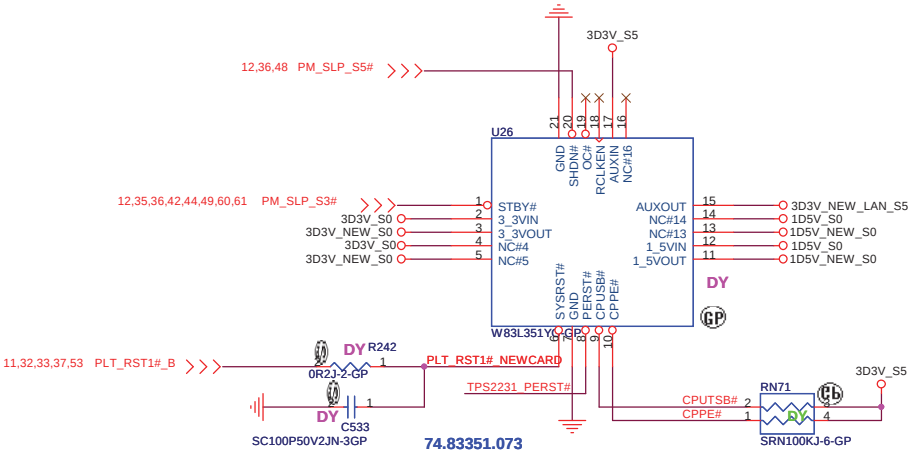


緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: MINI CARD		
Size	Document Number: JV50-TR	Rev: SB
Date: Tuesday, June 16, 2009	Sheet 33 of 61	

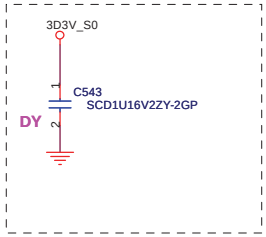
NEWCARD Connector



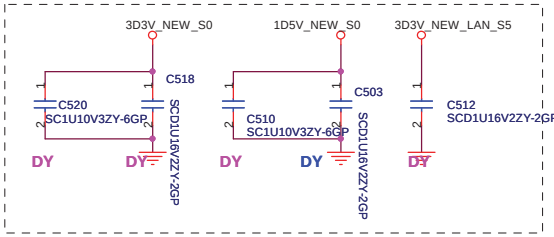




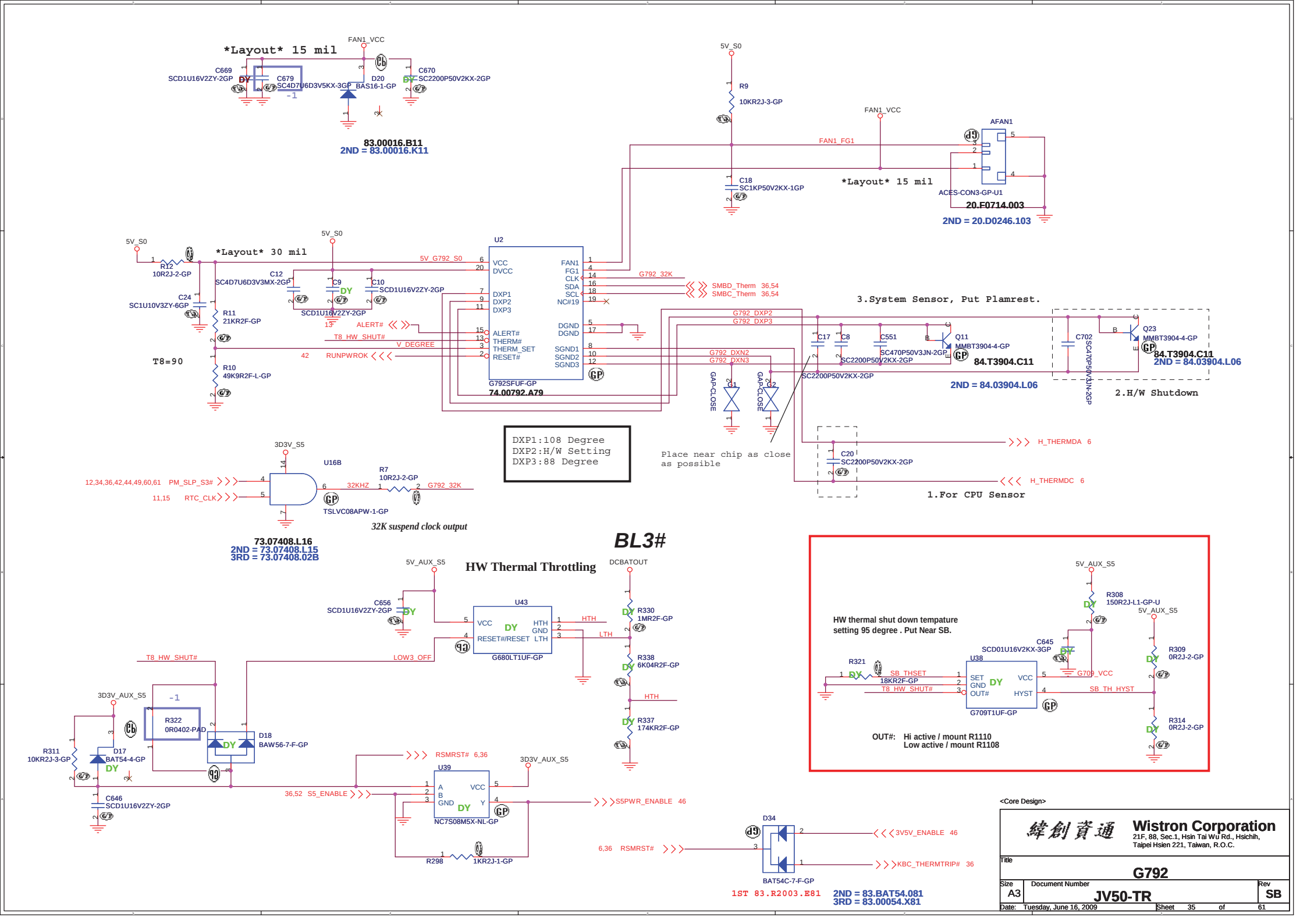
Place them Near to Chip



Place them Near to Connector



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**NEW CARD**	
Size	Document Number **JV50-TR**	Rev **SB**
Date: Tuesday, June 16, 2009	Sheet 34 of 61	



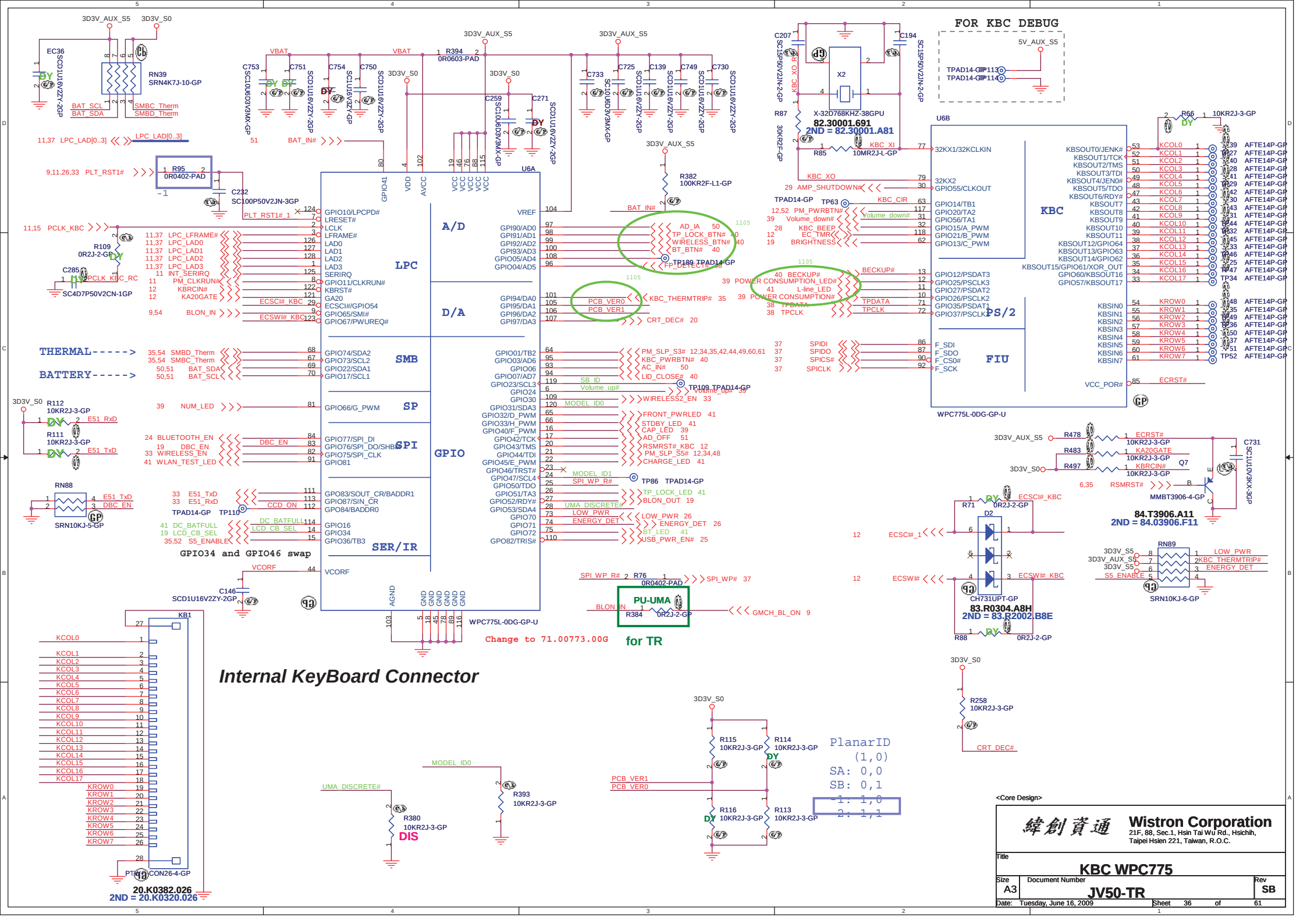
<Core Design>

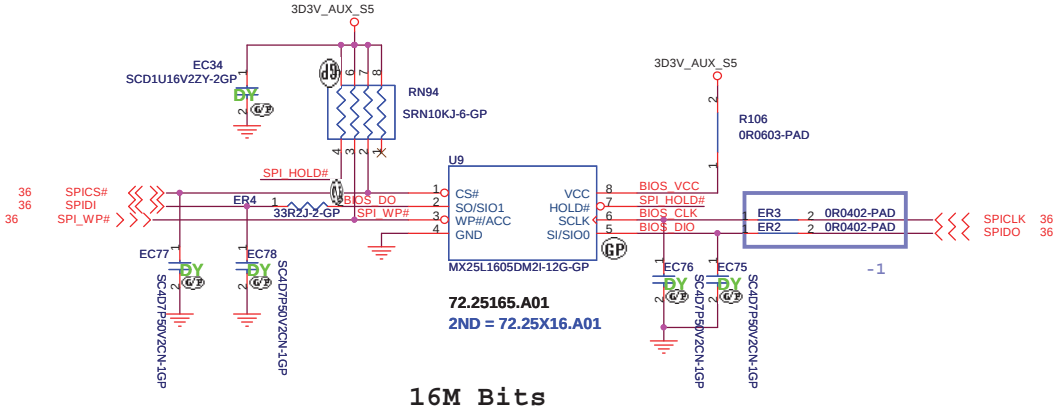
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G792

Size	Document Number	Rev
A3	JV50-TR	SB

Date: Tuesday, June 16, 2009 Sheet 35 of 61

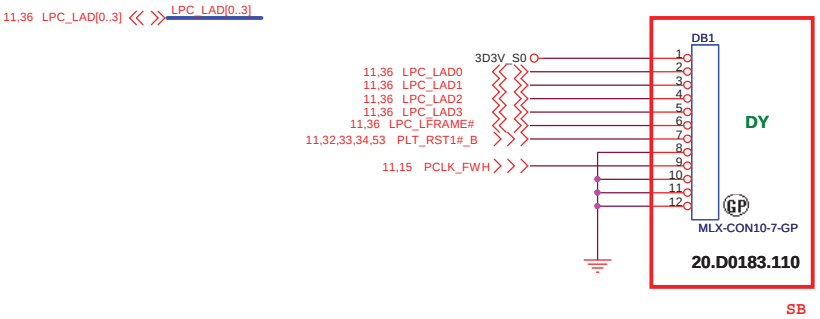

FOR KBC DEBUG
U6A
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
U6B
KBC
PS/2
FIU
WPC775L-0DG-GP-U
THERMAL----->
BATTERY----->
GPIO34 and GPIO46 swap
Change to 71.00773.00G
for TR
PU-UMA
Internal KeyBoard Connector
KB1
CON26-4-GP
20.K0382.026
2ND = 20.K0320.026
82.30001.691
2ND = 82.30001.A81
84.T3906.A11
2ND = 84.03906.F11
83.R0304.A8H
2ND = 83.R2002.B8E
PlanarID
(1,0)
SA: 0,0
SB: 0,1
-1: 1,0
2: 1,1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC775
JV50-TR
Tuesday, June 16, 2009



16M Bits

SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD

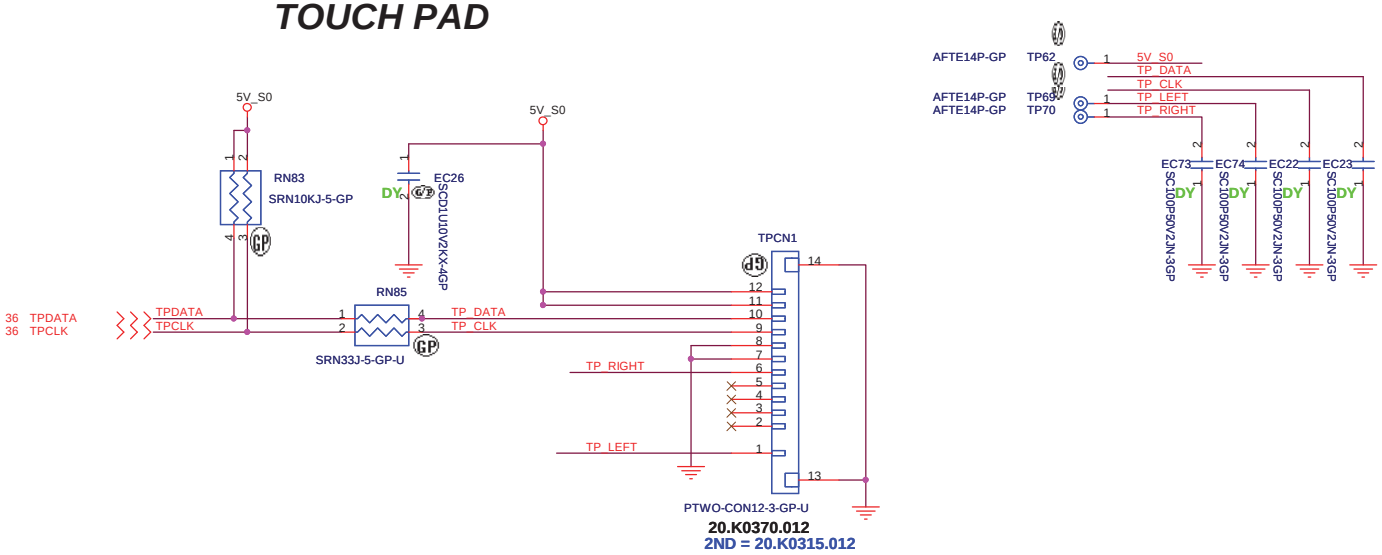


<Core Design>

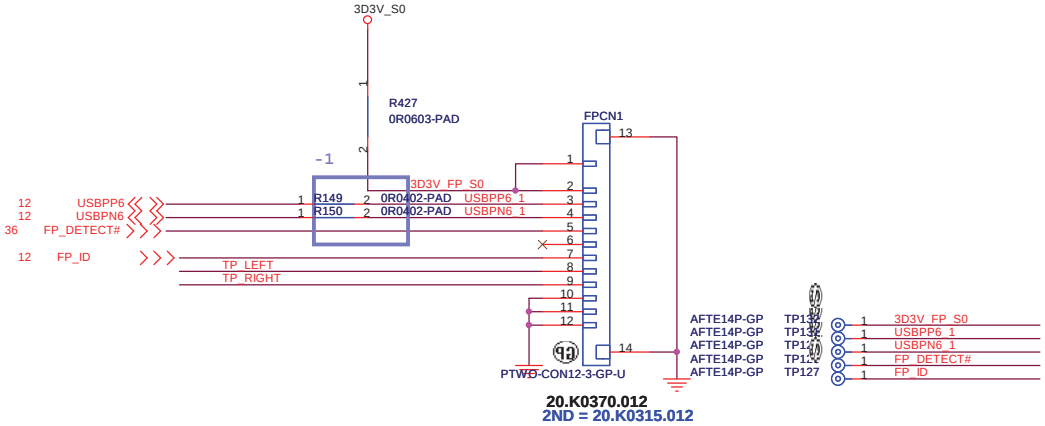
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS		
Size: A3	Document Number: JV50-TR	Rev: SB
Date: Tuesday, June 16, 2009	Sheet 37 of 61	

TOUCH PAD



Finger printer



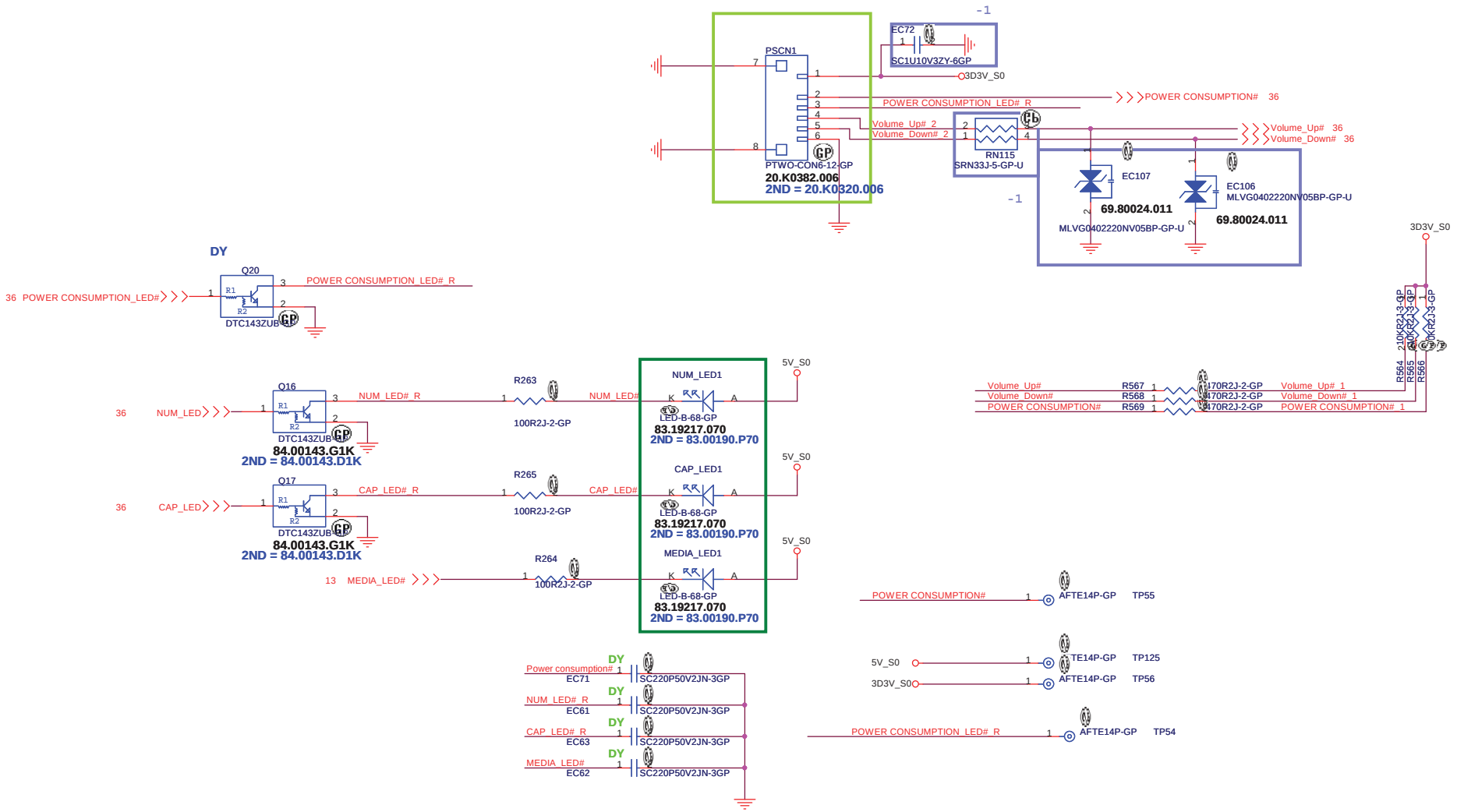
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Touch PAD/Finger printer

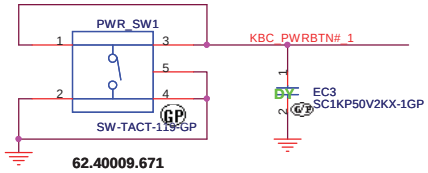
Size	Document Number	Rev
A3	JV50-TR	SB

Date: Tuesday, June 16, 2009 Sheet 38 of 61

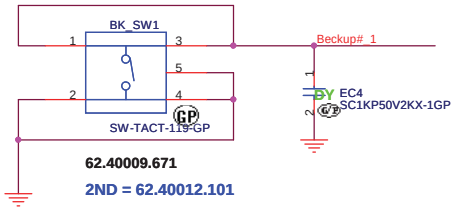


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**LAUNCH BOARD**	
Size: A3	Document Number: **JV50-TR**	Rev: **SB**
Date: Tuesday, June 16, 2009	Sheet 39 of 61	

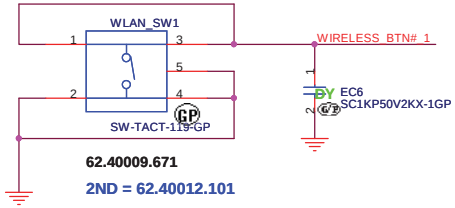
Power Button



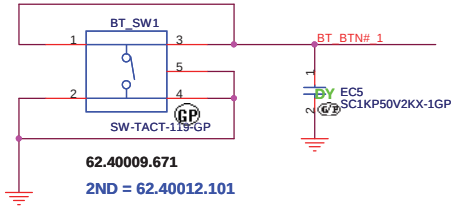
Beckup Button



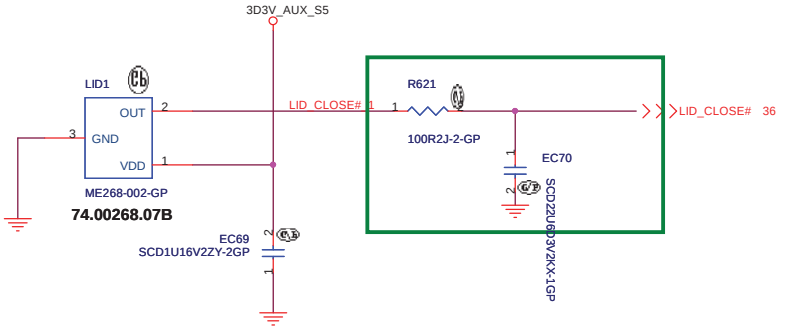
WIRELESS Button

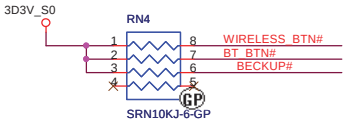


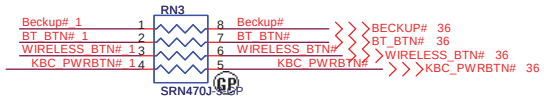
BT/3G Button



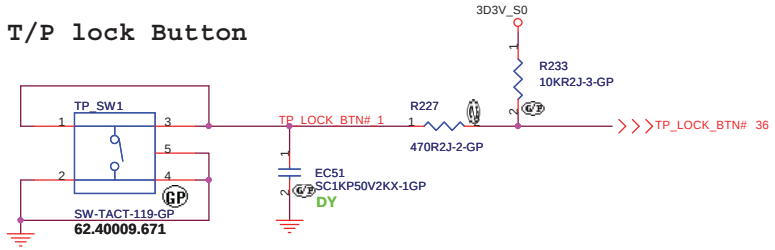
Cover Up Switch



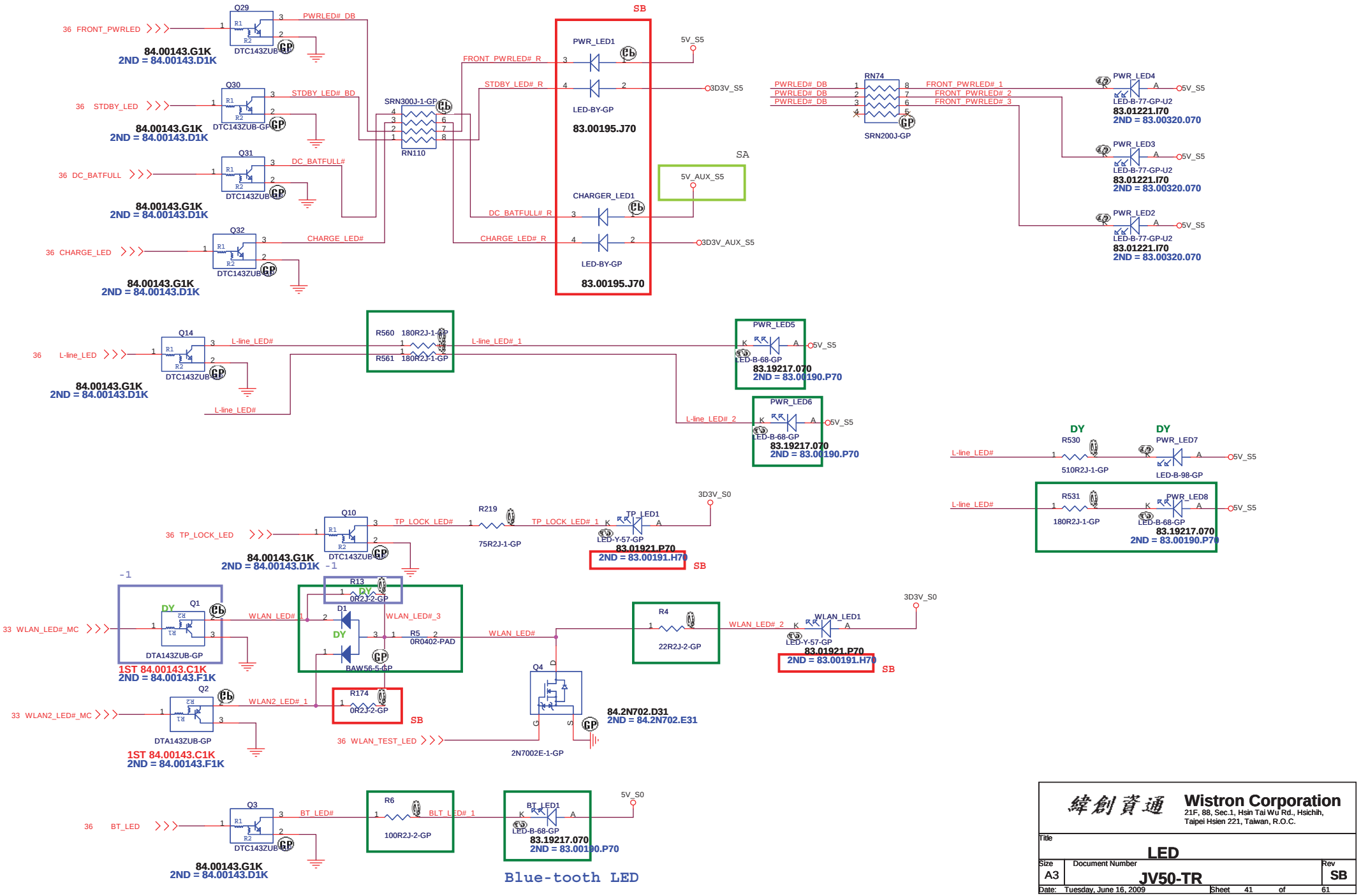




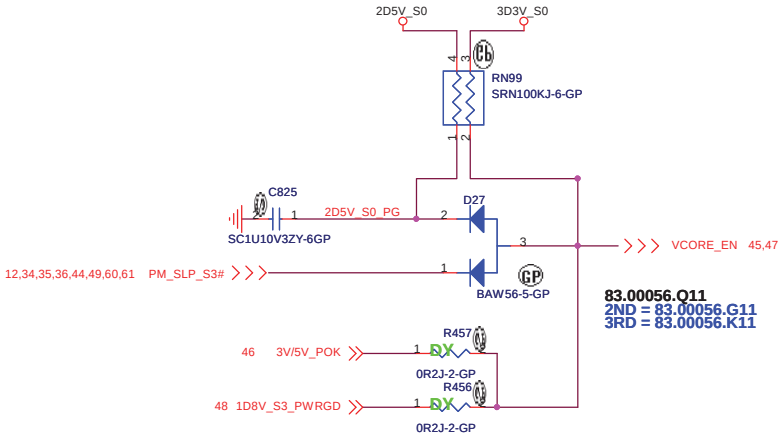
T/P lock Button



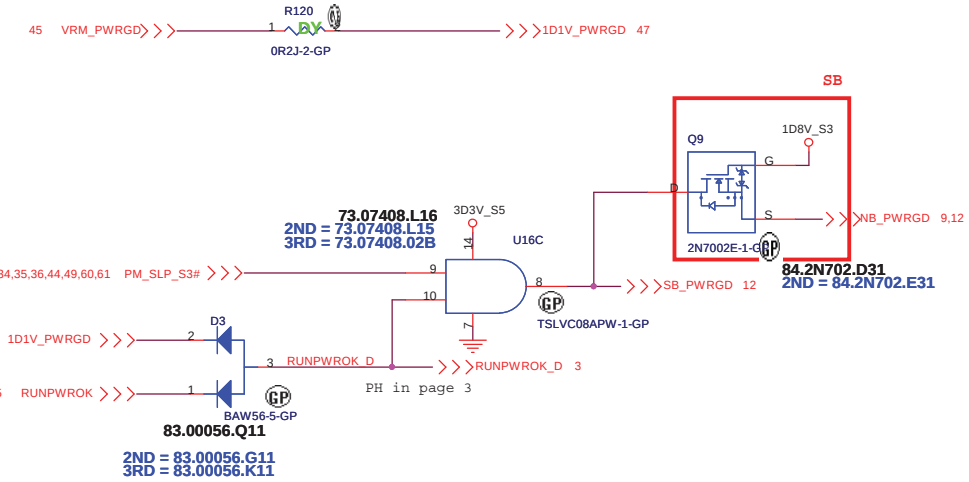
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: SWITCH		
Size: A3	Document Number: JV50-TR	Rev: SB
Date: Tuesday, June 16, 2009	Sheet 40 of 61	



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**LED**	
Size: A3	Document Number: **JV50-TR**	Rev: **SB**
Date: Tuesday, June 16, 2009	Sheet 41 of 61	



P/H @ 1D8V_S3 PAGE



<Core Design>

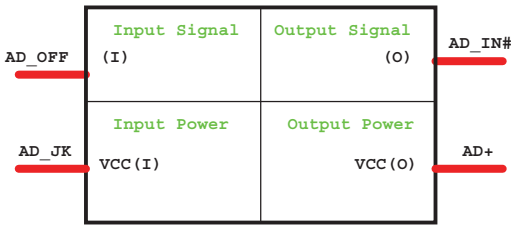
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER ON LOGIC

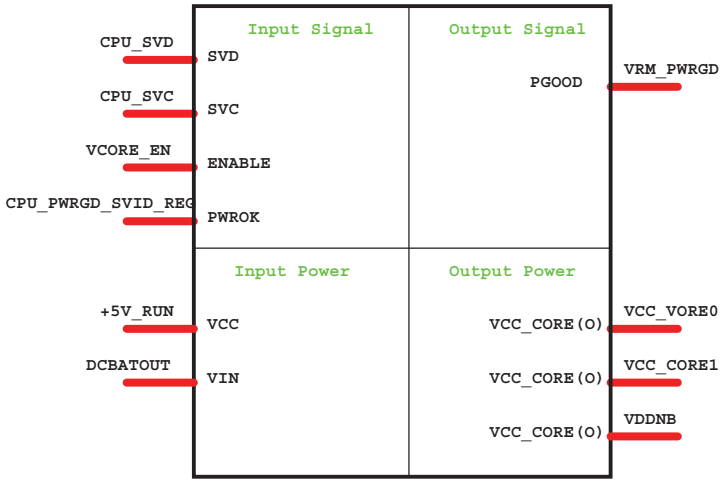
Size	Document Number	Rev
A3	JV50-TR	SB

Date: Tuesday, June 16, 2009 Sheet 42 of 61

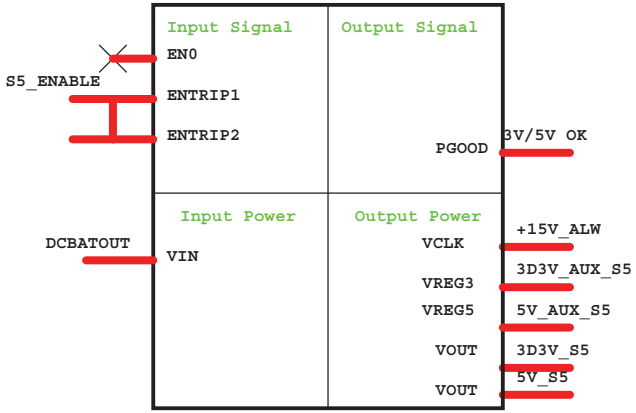
Adapter



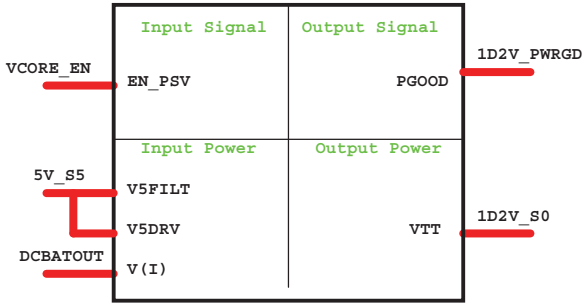
CPU_CORE
ISL6265HRTZ



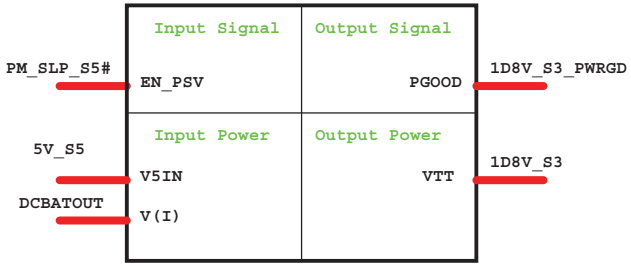
DCDC 5V/3D3V(RT8205A)



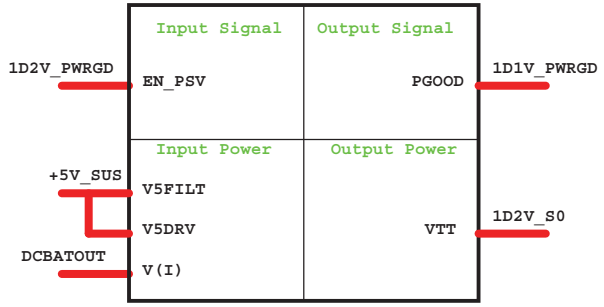
DCDC 1D2V(TPS51124)



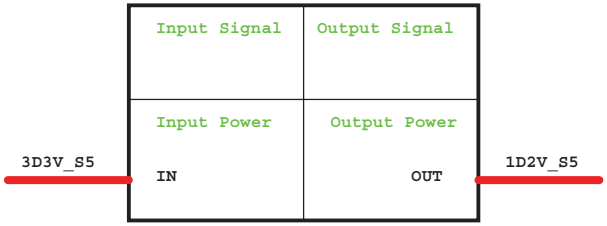
DCDC 1D8V(RT8209B)



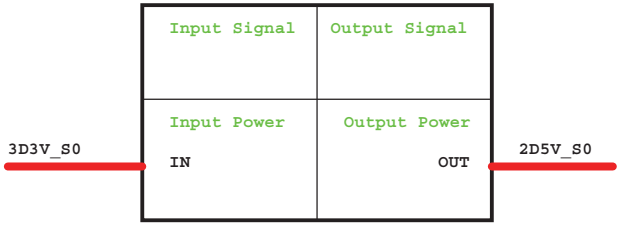
DCDC 1D1V(TPS51124)



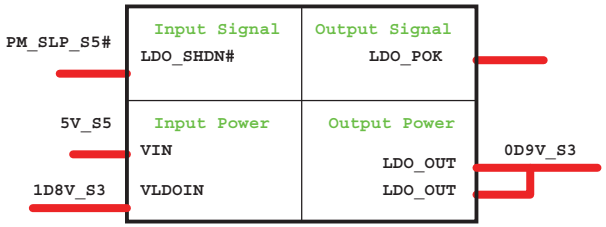
1D2V LDO G9161



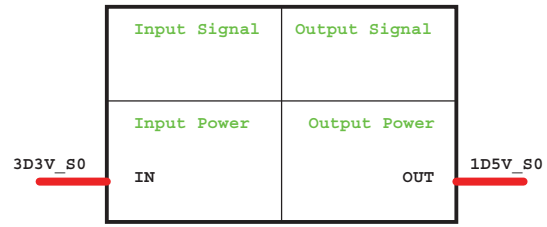
2D5V LDO R9161



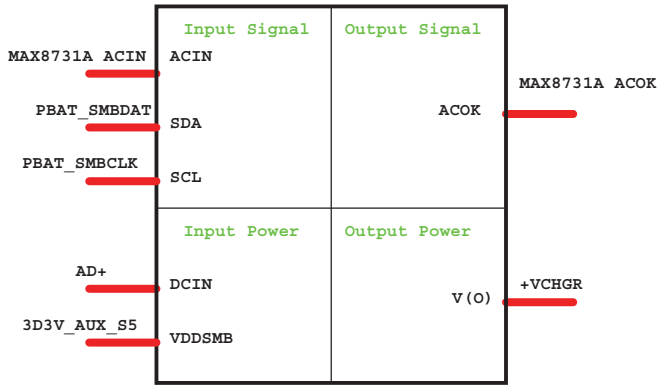
0D9V LDO RT9026



1D5V LDO G9571



CHARGER MAX8731



<Core Design>

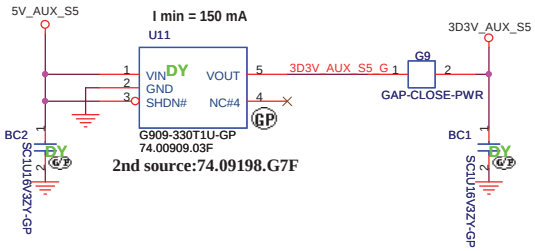
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

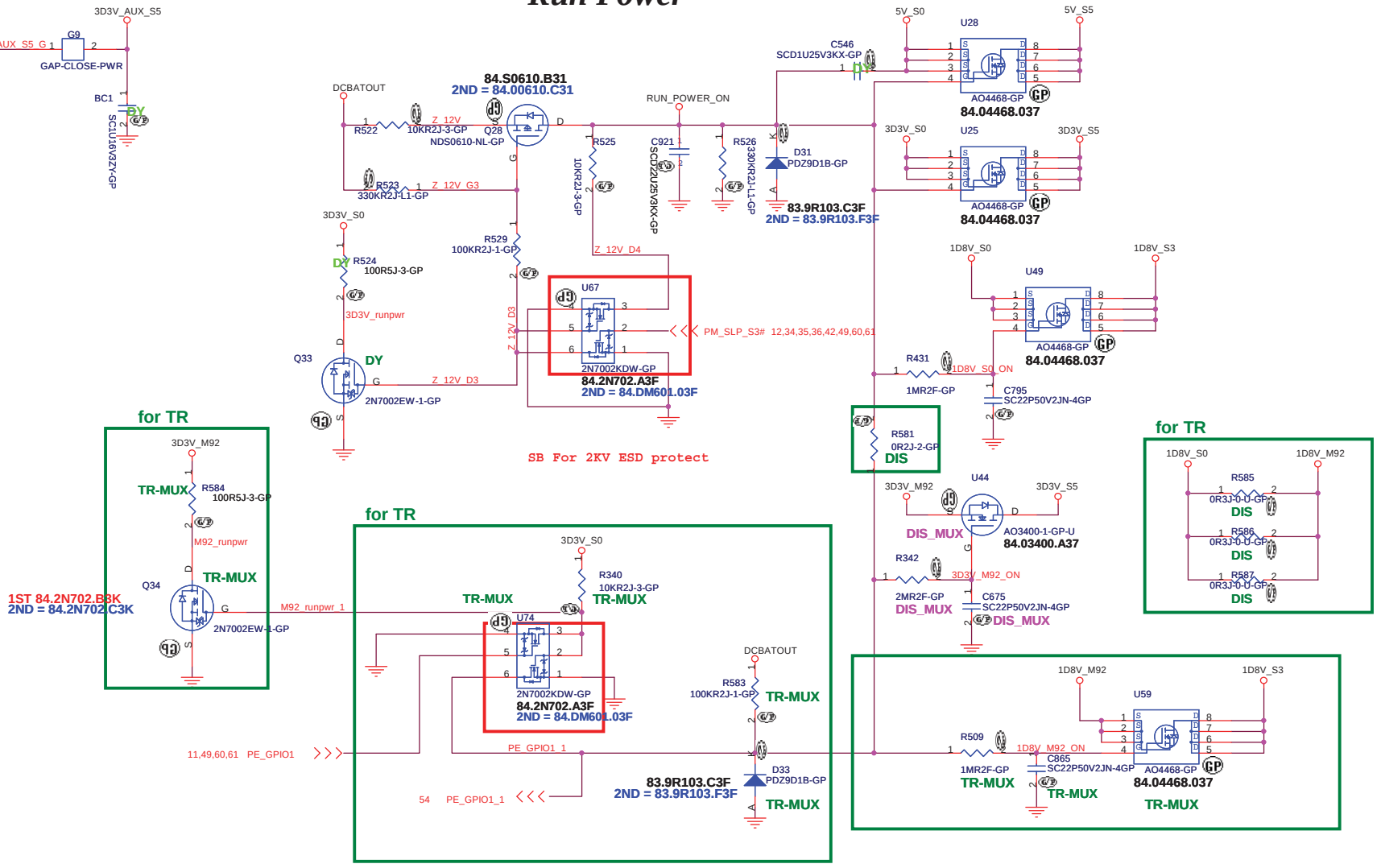
Size	Document Number	Rev
A3	JV50-TR	SB

Date: Tuesday, June 16, 2009 Sheet 43 of 61

Aux Power 3D3V_AUX_S5



Run Power



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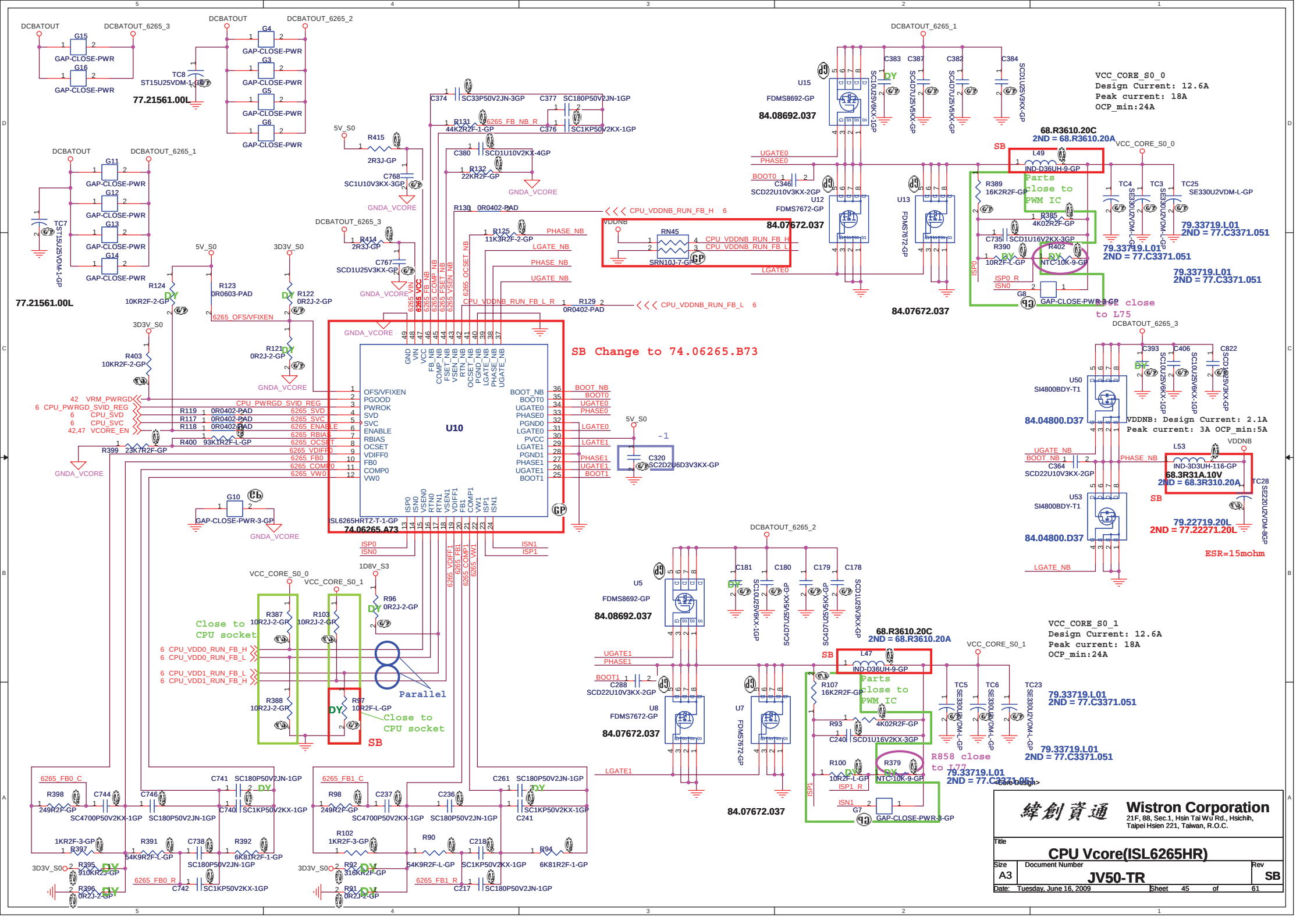
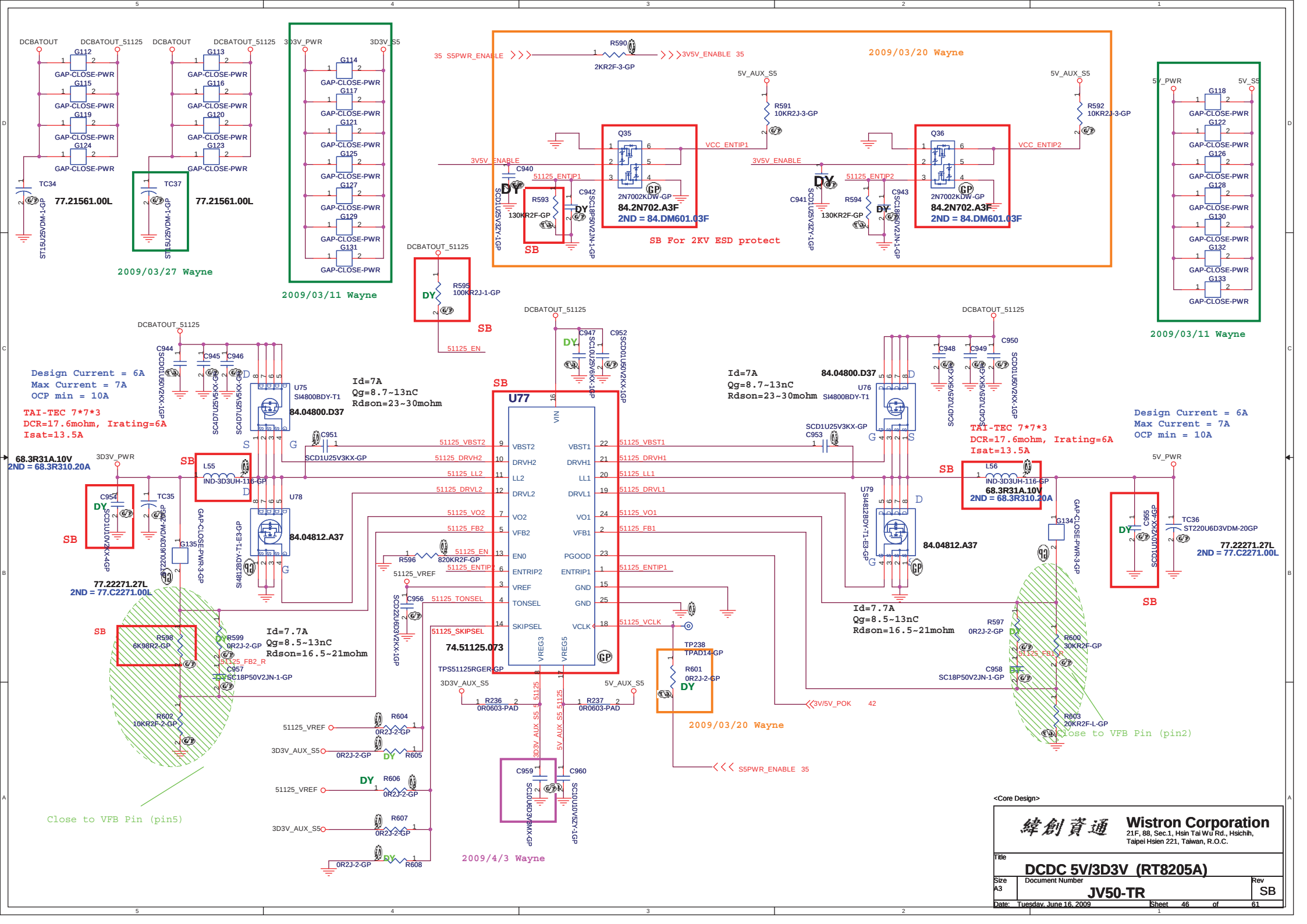
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

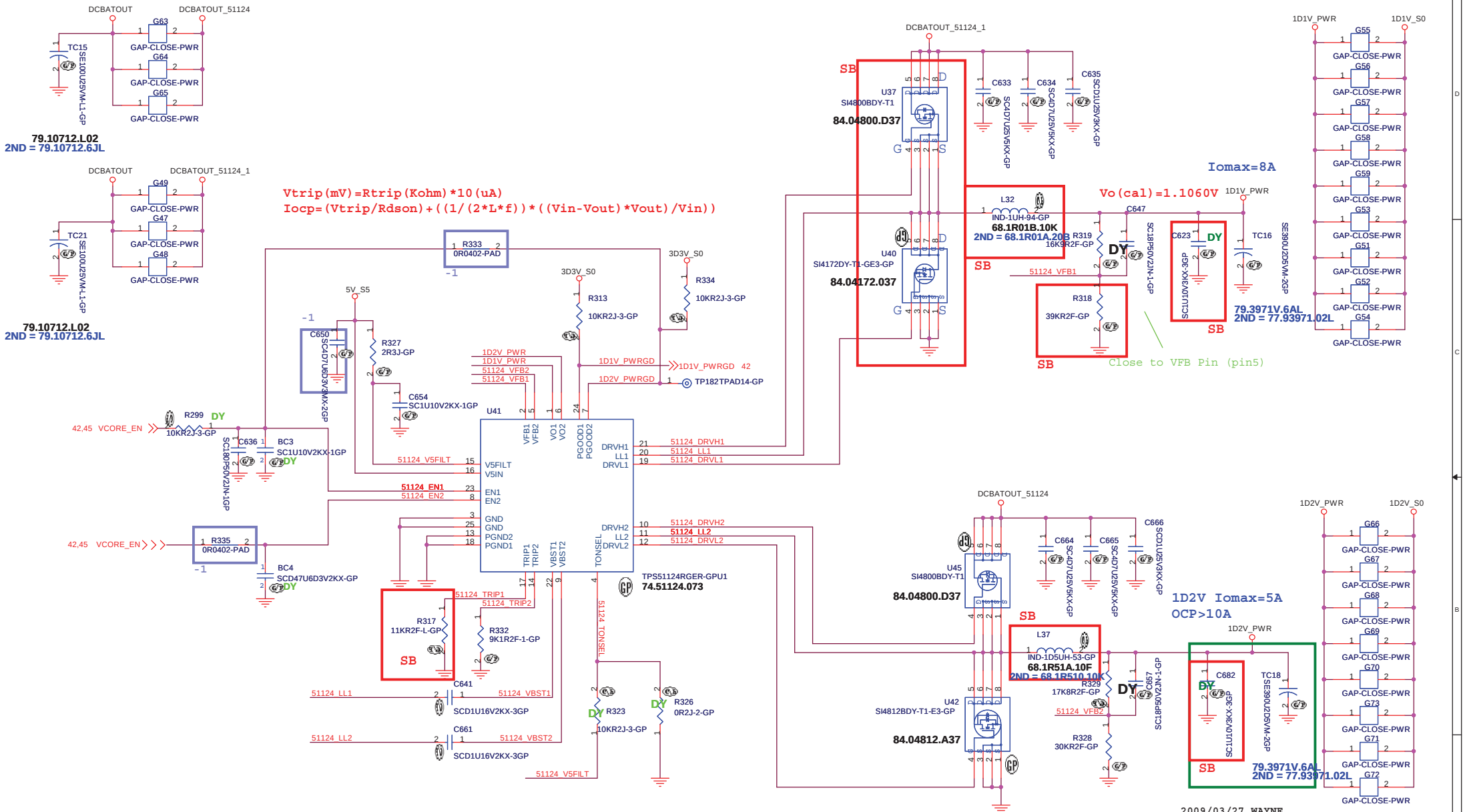
Title: RUN AND AUX POWER

Size	Document Number	Rev
A3	JV50-TR	SB

Date: Tuesday, June 16, 2009 Sheet 44 of 61


U10
SL6265HRTZ-T-1-GP
74.06265.A73
SB Change to 74.06265.B73
U15
FDMS8692-GP
84.08692.037
U12
FDMS7672-GP
U13
84.07672.037
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
68.R3610.20C
2ND = 68.R3610.20A
L49
IND-D36UH-9-GP
Parts close to PWM IC
79.33719.L01
2ND = 77.C3371.051
R3 close to L75
U50
SI4800BDY-T1
84.04800.D37
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
L53
IND-3D3UH-116-GP
68.3R31A.10V
2ND = 68.3R310.20A
U53
79.22719.20L
2ND = 77.22271.20L
ESR=15mohm
U5
U8
U7
VCC_CORE_S0_1
L47
R858 close to r77
Close to CPU socket
Parallel
SB
77.21561.00L
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
JV50-TR
Size A3
Rev SB
Date: Tuesday, June 16, 2009
Sheet 45 of 61


DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_PWR
5V_S5
5V_AUX_S5
35 S5PWR_ENABLE
3V5V_ENABLE 35
R590
2KR2F-3-GP
R591
10KR2J-3-GP
R592
10KR2J-3-GP
Q35
Q36
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
VCC_ENTIP1
VCC_ENTIP2
3V5V_ENABLE
51125_ENTIP1
51125_ENTIP2
C940
C941
C942
C943
R593
130KR2F-GP
R594
SCD1U25V2ZY-1GP
SC18P50V2JN-1-GP
DY
SB
SB For 2KV ESD protect
2009/03/20 Wayne
2009/03/27 Wayne
2009/03/11 Wayne
GAP-CLOSE-PWR
TC34
TC37
77.21561.00L
ST15U25VDM-1-GP
R595
100KR2J-1-GP
51125_EN
U77
U75
U76
U78
U79
SI4800BDY-T1
84.04800.D37
SI4812BDY-T1-E3-GP
84.04812.A37
VIN
VBST2
DRVH2
LL2
DRVL2
VO2
VFB2
EN0
ENTRIP2
VREF
TONSEL
SKIPSEL
VBST1
DRVH1
LL1
DRVL1
VO1
VFB1
PGOOD
GND
VCLK
VREG3
VREG5
TPS51125RGER-GP
51125_VBST2
51125_DRVH2
51125_LL2
51125_DRVL2
51125_VO2
51125_FB2
51125_EN
51125_ENTIP2
51125_VREF
51125_TONSEL
51125_SKIPSEL
51125_VBST1
51125_DRVH1
51125_LL1
51125_DRVL1
51125_VO1
51125_FB1
51125_ENTIP1
51125_VCLK
3V/5V_POK 42
S5PWR_ENABLE 35
Design Current = 6A
Max Current = 7A
OCP min = 10A
TAI-TEC 7*7*3
DCR=17.6mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
68.3R31A.10V
2ND = 68.3R310.20A
77.22271.27L
2ND = 77.C2271.00L
74.51125.073
IND-3D3UH-116-GP
L55
L56
G134
G135
R596
820KR2F-GP
R597
0R2J-2-GP
R598
6K98R2-GP
R599
0R2J-2-GP
R600
30KR2F-GP
R601
0R2J-2-GP
R602
10KR2F-2-GP
R603
20KR2F-L-GP
R604
R605
R606
R607
R608
0R2J-2-GP
R236
R237
0R0603-PAD
TP238
TPAD14-GP
C951
C952
C953
C954
C955
C956
C957
C958
C959
C960
SCD1U25V3KX-GP
SCD1U10V2KX-4GP
SC18P50V2JN-1-GP
SCD22U6D3V3MX-GP
SCD1U10V6ZY-1GP
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
2009/4/3 Wayne
2009/03/20 Wayne
2009/03/11 Wayne
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 5V/3D3V (RT8205A)
Size
A3
Document Number
JV50-TR
Rev
SB
Date: Tuesday, June 16, 2009
Sheet 46 of 61



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

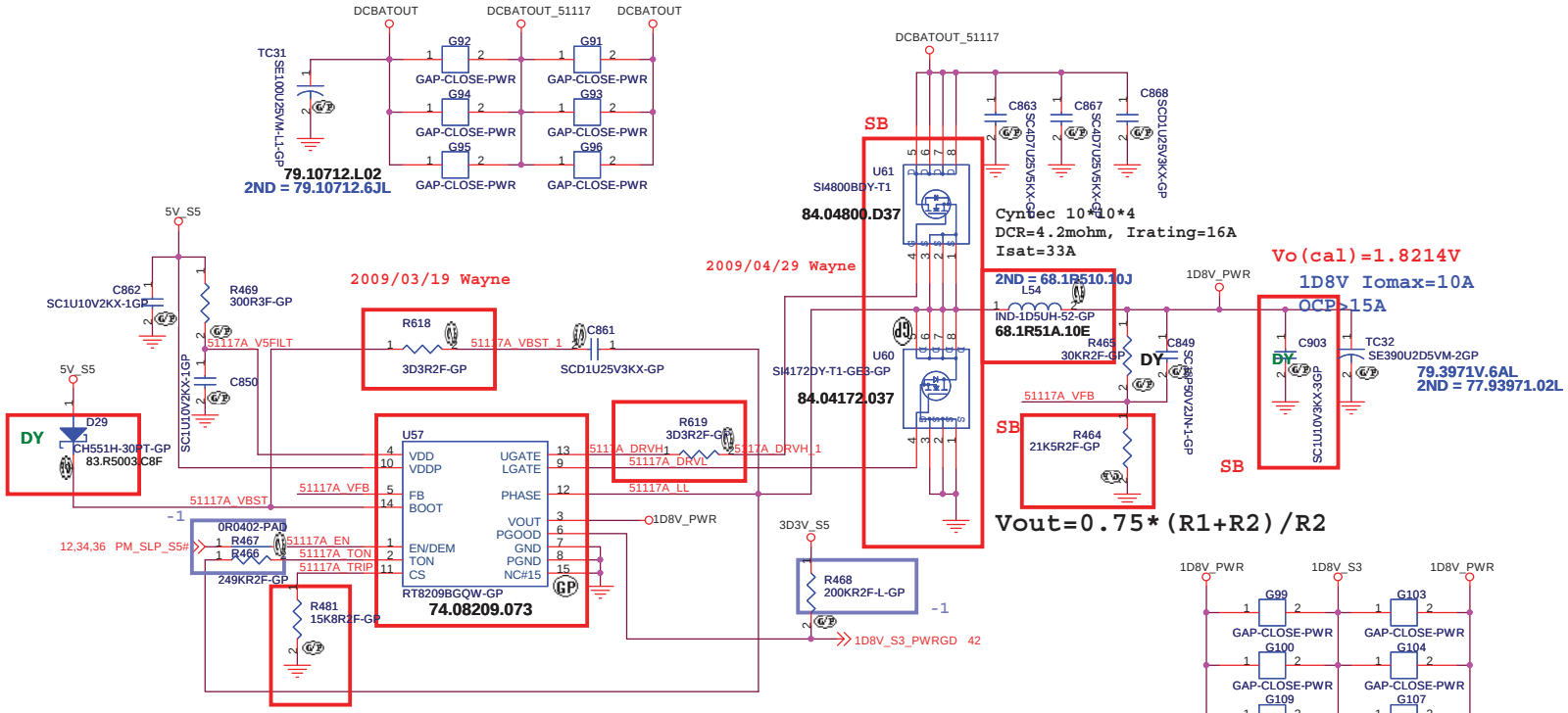
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D1V_1D2V

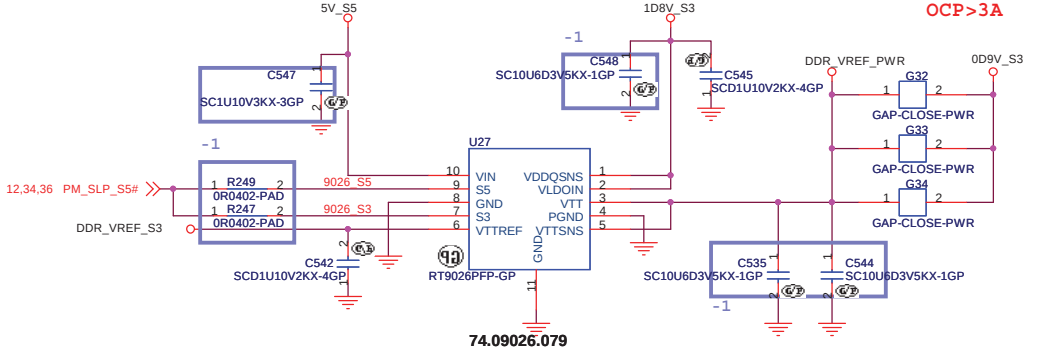
Size	Document Number	Rev
A3	JV50-TR	SB

Date: Tuesday, June 16, 2009 Sheet 47 of 61



DDR_0.9V

Iomax=1.5A
OCP>3A



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

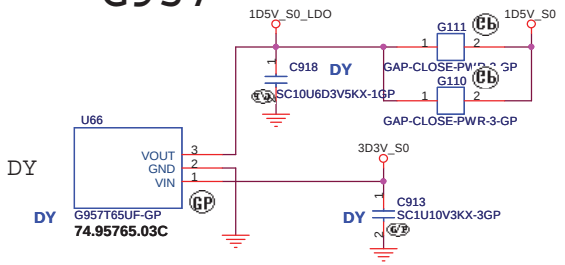
Title: DCDC_1D8V_RT8209B/LDO 0D9V

Size	Document Number	Rev
A3	JV50-TR	SB

Date: Tuesday, June 16, 2009 Sheet 48 of 61

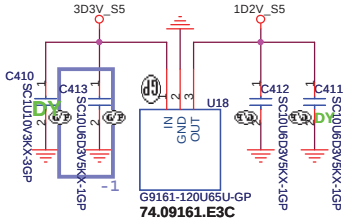
1D5V_S0
Iomax=1A

G957



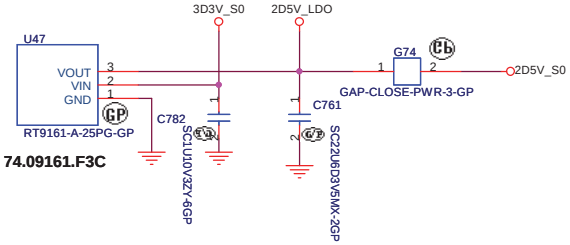
For MINI Card.NEW Card power SW

1D2V_S5
Iomax=400mA



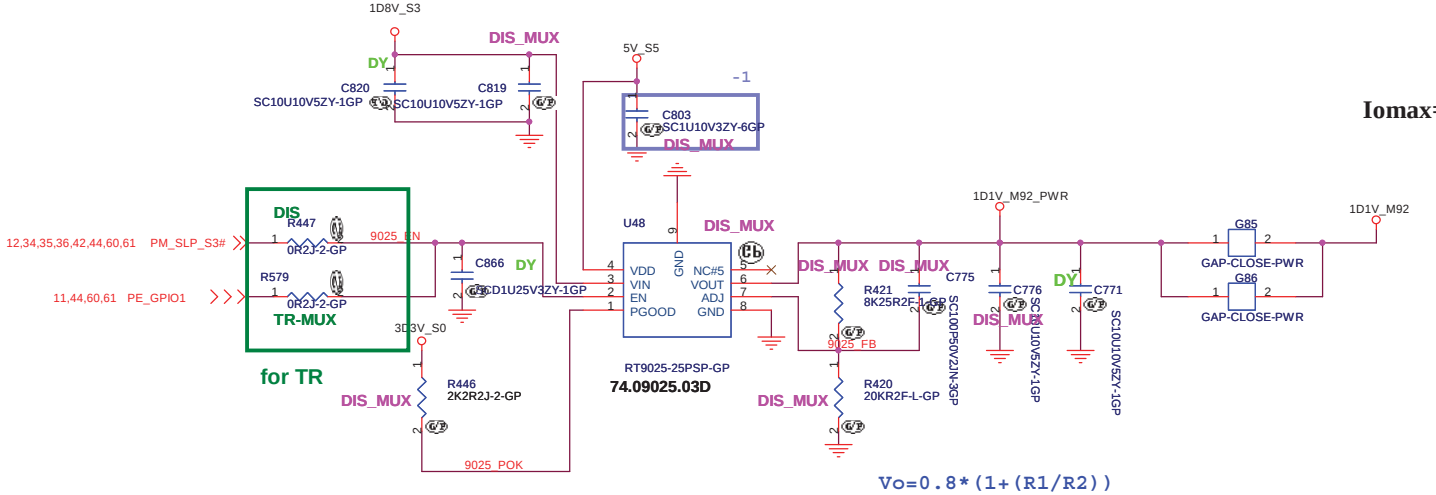
Place near to SB700

2D5V
Iomax=0.2A



Place near to CPU

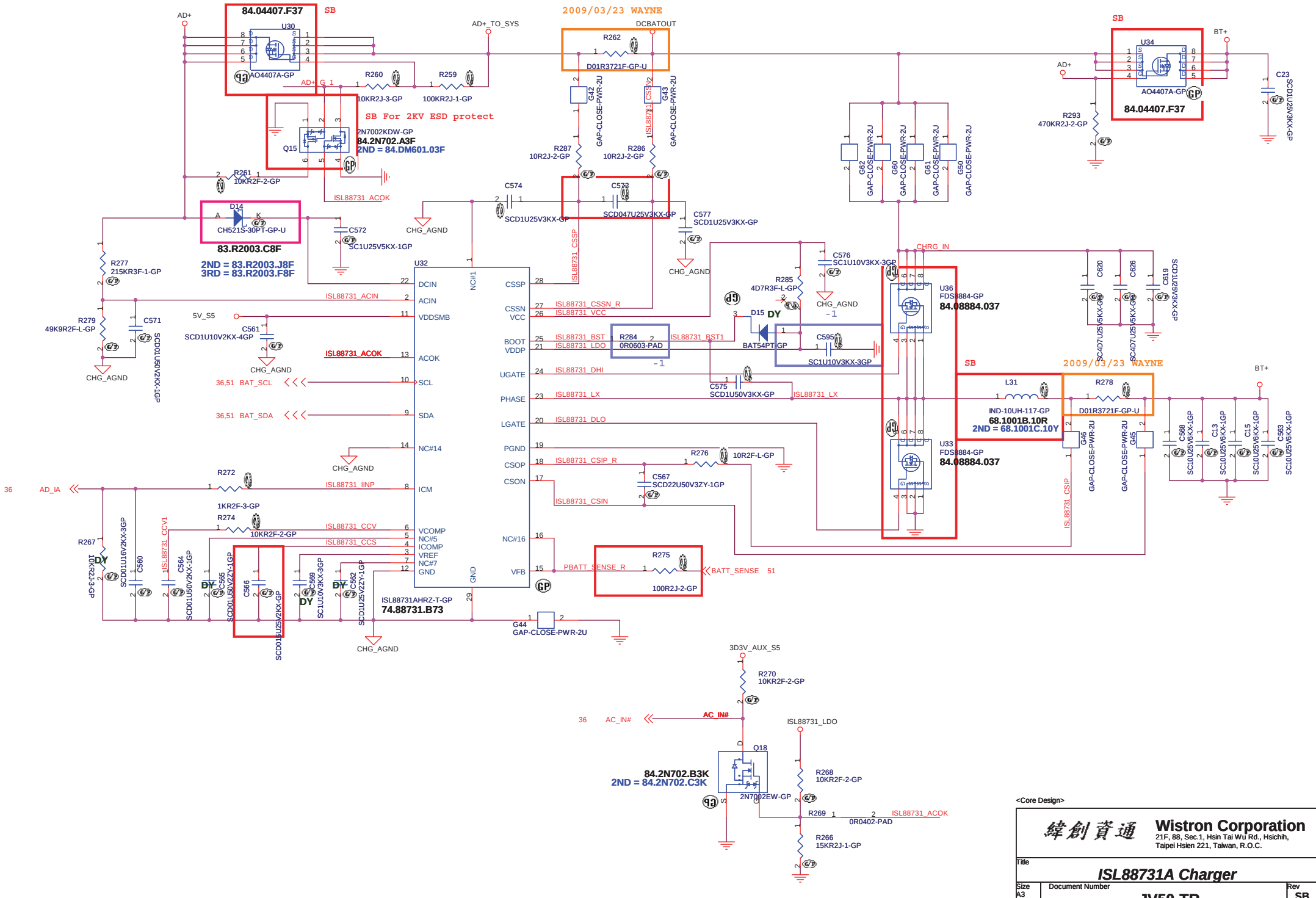
Iomax=0.8A



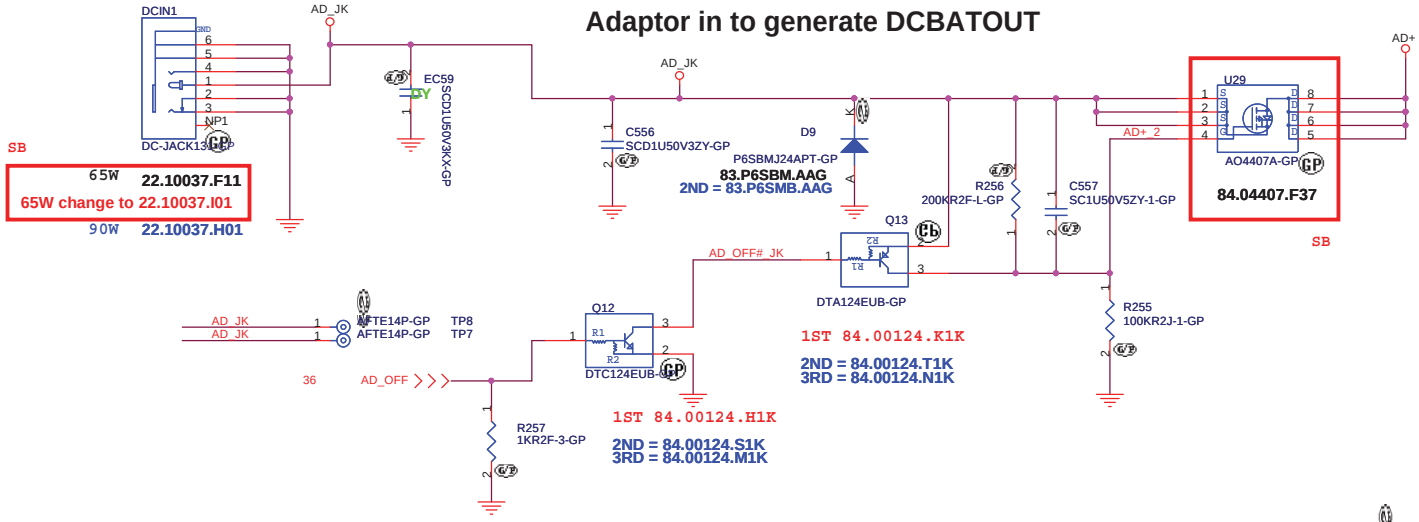
Vo=0.8*(1+(R1/R2))

<Core Design>

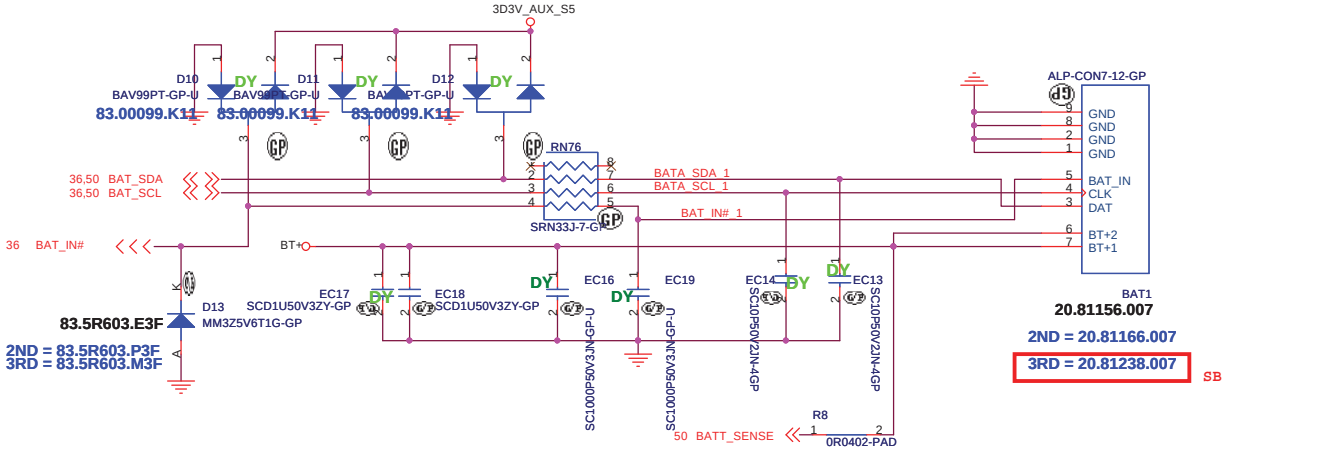
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LDO 2D5V/1D5V/1D2V_S5		
Size: A3	Document Number: JV50-TR	Rev: SB
Date: Tuesday, June 16, 2009	Sheet 49 of 61	


84.04407.F37
SB
U30
AO4407A-GP
AD+
AD+_TO_SYS
2009/03/23 WAYNE
DCBATOUT
R262
D01R3721F-GP-U
R260
10KR2J-3-GP
R259
100KR2J-1-GP
SB For 2KV ESD protect
Q15
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
R261
10KR2F-2-GP
ISL88731_ACOK
D14
CH521S-30PT-GP-U
83.R2003.C8F
2ND = 83.R2003.J8F
3RD = 83.R2003.F8F
C572
SC1U25V5KX-1GP
CHG_AGND
C574
SCD1U25V3KX-GP
C573
SCD047U25V3KX-GP
C577
SCD1U25V3KX-GP
R287
10R2J-2-GP
R286
10R2J-2-GP
G42
G43
GAP-CLOSE-PWR-2U
ISL88731_CSSN
ISL88731_CSSP
U32
ISL88731AHRZ-T-GP
74.88731.B73
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
NC#1
R277
215KR3F-1-GP
R279
49K9R2F-L-GP
C571
SCD1U10V2KX-1GP
5V_S5
C561
SCD1U10V2KX-4GP
36,51 BAT_SCL
36,51 BAT_SDA
R272
1KR2F-3-GP
36 AD_IA
R274
10KR2F-2-GP
R267
10KR2J-3-GP
DY
SCD01U16V2KX-3GP
C560
C564
SCD01U50V2KX-1GP
C565
SCD01U50V2ZY-1GP
C566
SCD01U25V2KX-GP
C569
SC1U10V3KX-3GP
C562
SCD1U25V2ZY-1GP
ISL88731_CCV1
ISL88731_CCV
ISL88731_CCS
ISL88731_IINP
ISL88731_DHI
ISL88731_LX
ISL88731_DLO
ISL88731_CSIP_R
ISL88731_CSIN
ISL88731_VCC
ISL88731_CSSN_R
ISL88731_BST
ISL88731_LDO
ISL88731_BST1
R284
0R0603-PAD
-1
D15
BAT54PT-GP
C595
SC1U10V3KX-3GP
C575
SCD1U50V3KX-GP
R285
4D7R3F-L-GP
C576
SC1U10V3KX-3GP
CHRG_IN
U36
FDS8884-GP
84.08884.037
U33
FDS8884-GP
84.08884.037
L31
IND-10UH-117-GP
68.1001B.10R
2ND = 68.1001C.10Y
R278
D01R3721F-GP-U
BT+
C620
C626
C619
SC4D7U25V5KX-GP
C568
C13
C15
C563
SC10U25V6KX-1GP
G46
G45
GAP-CLOSE-PWR-2U
R276
10R2F-L-GP
R275
100R2J-2-GP
PBATT_SENSE_R
BATT_SENSE
51
G44
GAP-CLOSE-PWR-2U
G62
G60
G61
G50
GAP-CLOSE-PWR-2U
U34
AO4407A-GP
84.04407.F37
R293
470KR2J-2-GP
C23
SCD1U25V3KX-GP
3D3V_AUX_S5
R270
10KR2F-2-GP
36 AC_IN#
AC_IN#
Q18
2N7002EW-GP
84.2N702.B3K
2ND = 84.2N702.C3K
R268
10KR2F-2-GP
R269
0R0402-PAD
R266
15KR2J-1-GP
ISL88731_ACOK
ISL88731_LDO
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A Charger
Size A3
Document Number
JV50-TR
Rev SB
Date: Tuesday, June 16, 2009
Sheet 50 of 61

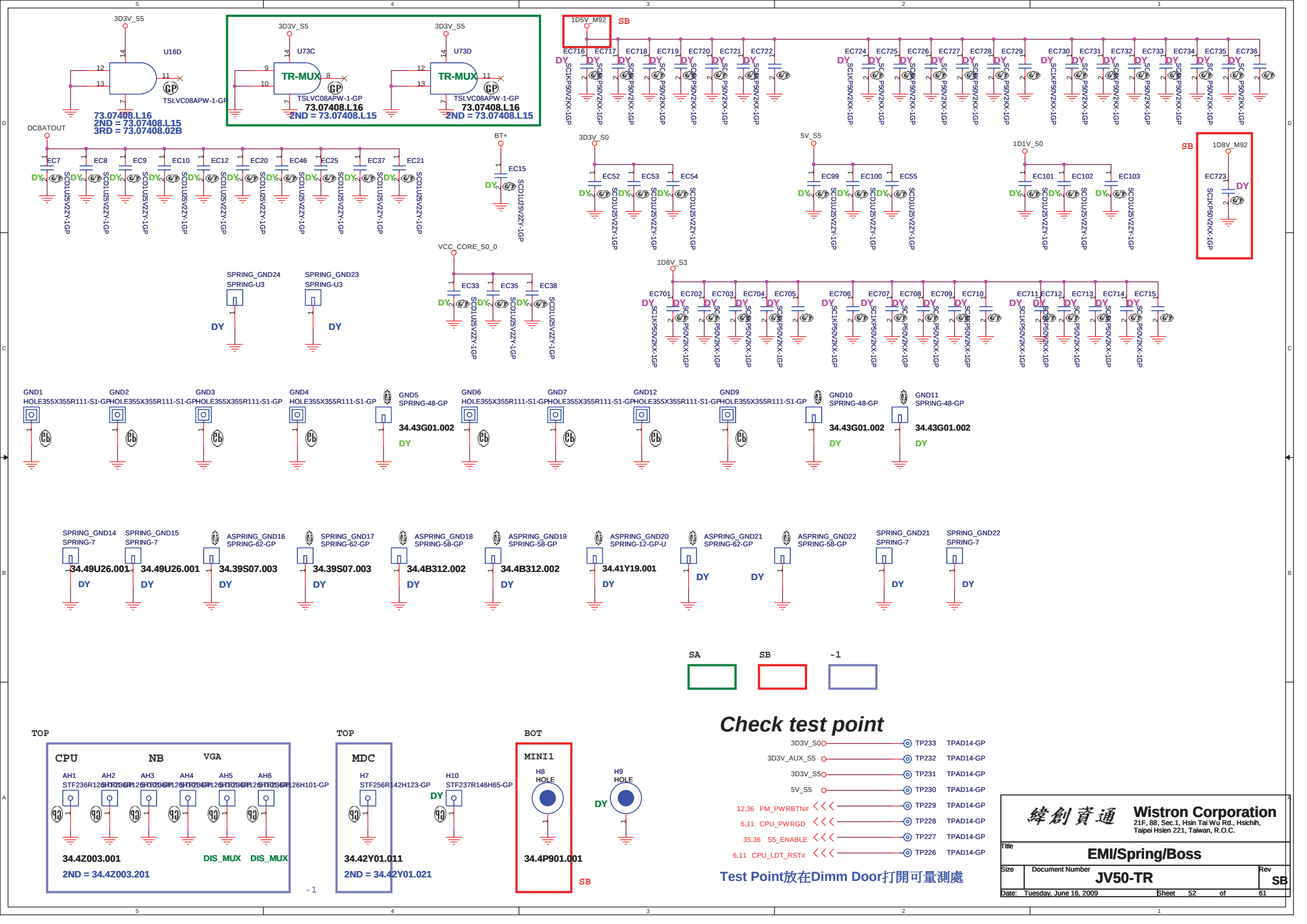
Adaptor in to generate DCBATOUT

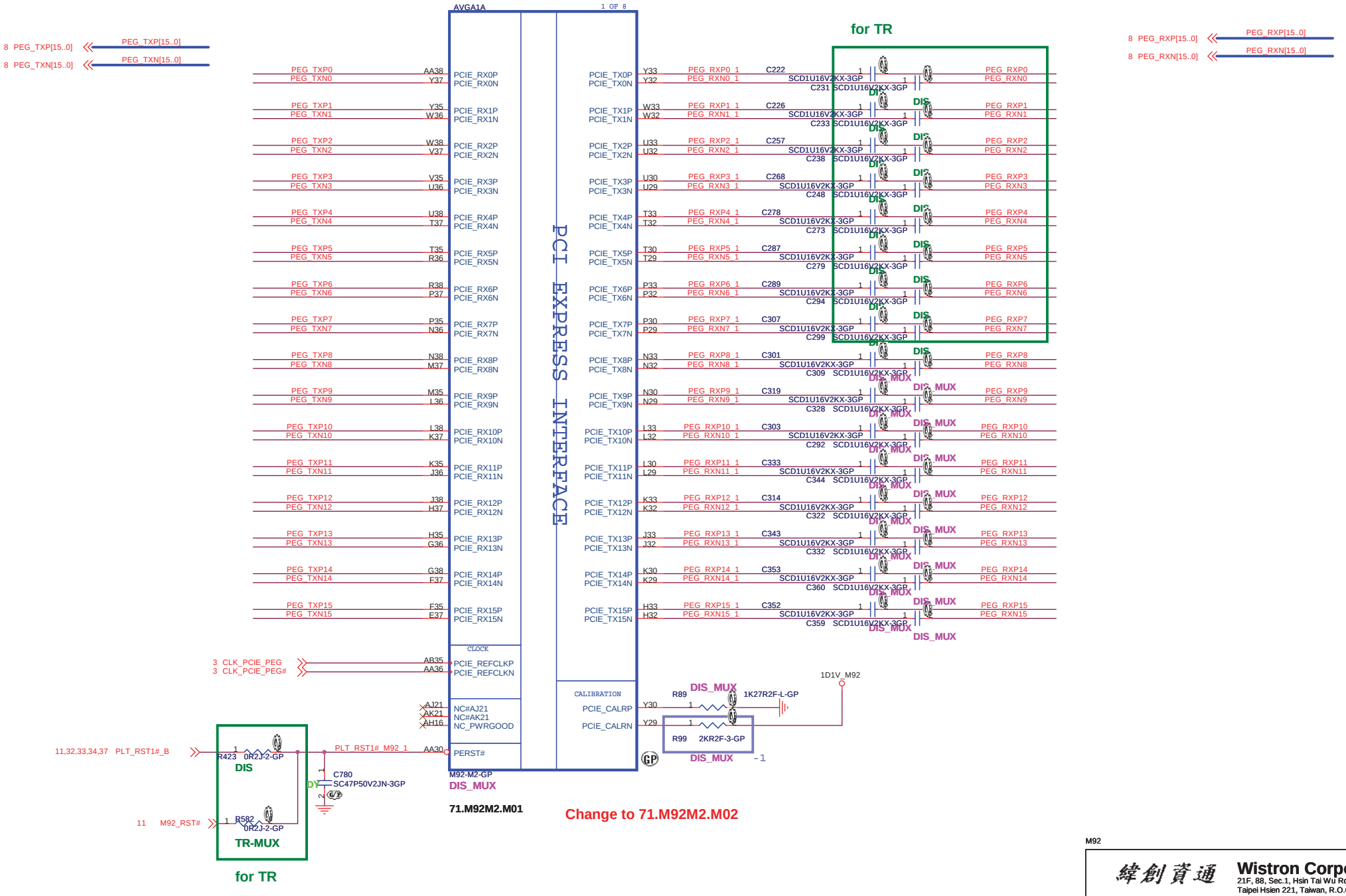


BATTERY CONNECTOR



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AD/BATT CONN	
Size	Document Number: JV50-TR	Rev: SB
Date: Tuesday, June 16, 2009	Sheet 51 of 61	


3D3V_S5
U16D
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
U73C
U73D
TR-MUX
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
1D5V_M92
SB
DCBATOUT
BT+
3D3V_S0
5V_S5
1D1V_S0
1D8V_M92
SB
VCC_CORE_S0_0
1D8V_S3
SPRING_GND24
SPRING-U3
SPRING_GND23
SPRING-U3
GND1
HOLE355X355R111-S1-GP
GND2
HOLE355X355R111-S1-GP
GND3
HOLE355X355R111-S1-GP
GND4
HOLE355X355R111-S1-GP
GND5
SPRING-48-GP
34.43G01.002
GND6
HOLE355X355R111-S1-GP
GND7
HOLE355X355R111-S1-GP
GND12
HOLE355X355R111-S1-GP
GND9
HOLE355X355R111-S1-GP
GND10
SPRING-48-GP
34.43G01.002
GND11
SPRING-48-GP
34.43G01.002
SPRING_GND14
SPRING-7
34.49U26.001
SPRING_GND15
SPRING-7
34.49U26.001
ASPRING_GND16
SPRING-62-GP
34.39S07.003
SPRING_GND17
SPRING-62-GP
34.39S07.003
ASPRING_GND18
SPRING-58-GP
34.4B312.002
ASPRING_GND19
SPRING-58-GP
34.4B312.002
ASPRING_GND20
SPRING-12-GP-U
34.41Y19.001
ASPRING_GND21
SPRING-62-GP
ASPRING_GND22
SPRING-58-GP
SPRING_GND21
SPRING-7
SPRING_GND22
SPRING-7
SA
SB
-1
Check test point
3D3V_S0 TP233 TPAD14-GP
3D3V_AUX_S5 TP232 TPAD14-GP
3D3V_S5 TP231 TPAD14-GP
5V_S5 TP230 TPAD14-GP
12,36 PM_PWRBTN# TP229 TPAD14-GP
6,11 CPU_PWRGD TP228 TPAD14-GP
35,36 S5_ENABLE TP227 TPAD14-GP
6,11 CPU_LDT_RST# TP226 TPAD14-GP
Test Point放在Dimm Door打開可量測處
TOP
CPU
NB
VGA
34.4Z003.001
DIS_MUX
DIS_MUX
2ND = 34.4Z003.201
TOP
MDC
34.42Y01.011
2ND = 34.42Y01.021
BOT
MINI1
H8 HOLE
H9 HOLE
34.4P901.001
SB
-1
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
Document Number
JV50-TR
Rev
SB
Date: Tuesday, June 16, 2009
Sheet 52 of 61



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: M92 PCIE	
Size: A3	Document Number: JV50-TR
Rev: SB	
Date: Tuesday, June 16, 2009	Sheet 53 of 61

Layout notice:
It should be pleace near HDMI connector

DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request

DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)

It's strap for GDDR3-136ball
Need to Clarify

Back Bias (body bias) which minimizes power consumption in battery modes.
PD = Disable
PU = Enable

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

Depending on OSC used select voltage divider resist values R25 R70 to ensure XTALIN voltage level of 1.8V

For Thermal sensor

1ST 82.30034.461
2ND = 82.30034.701

2009/04/28 For 2KV ESD protect

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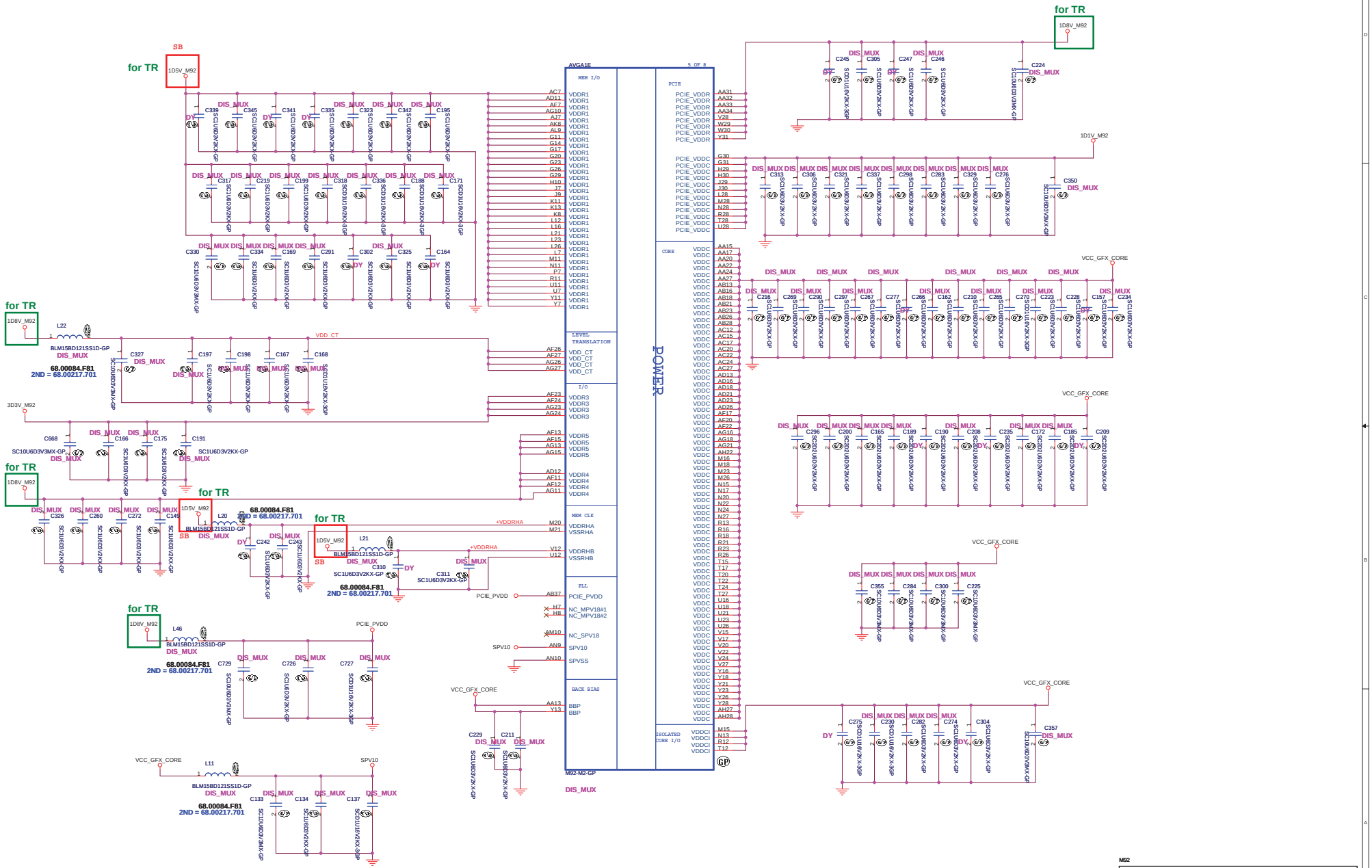
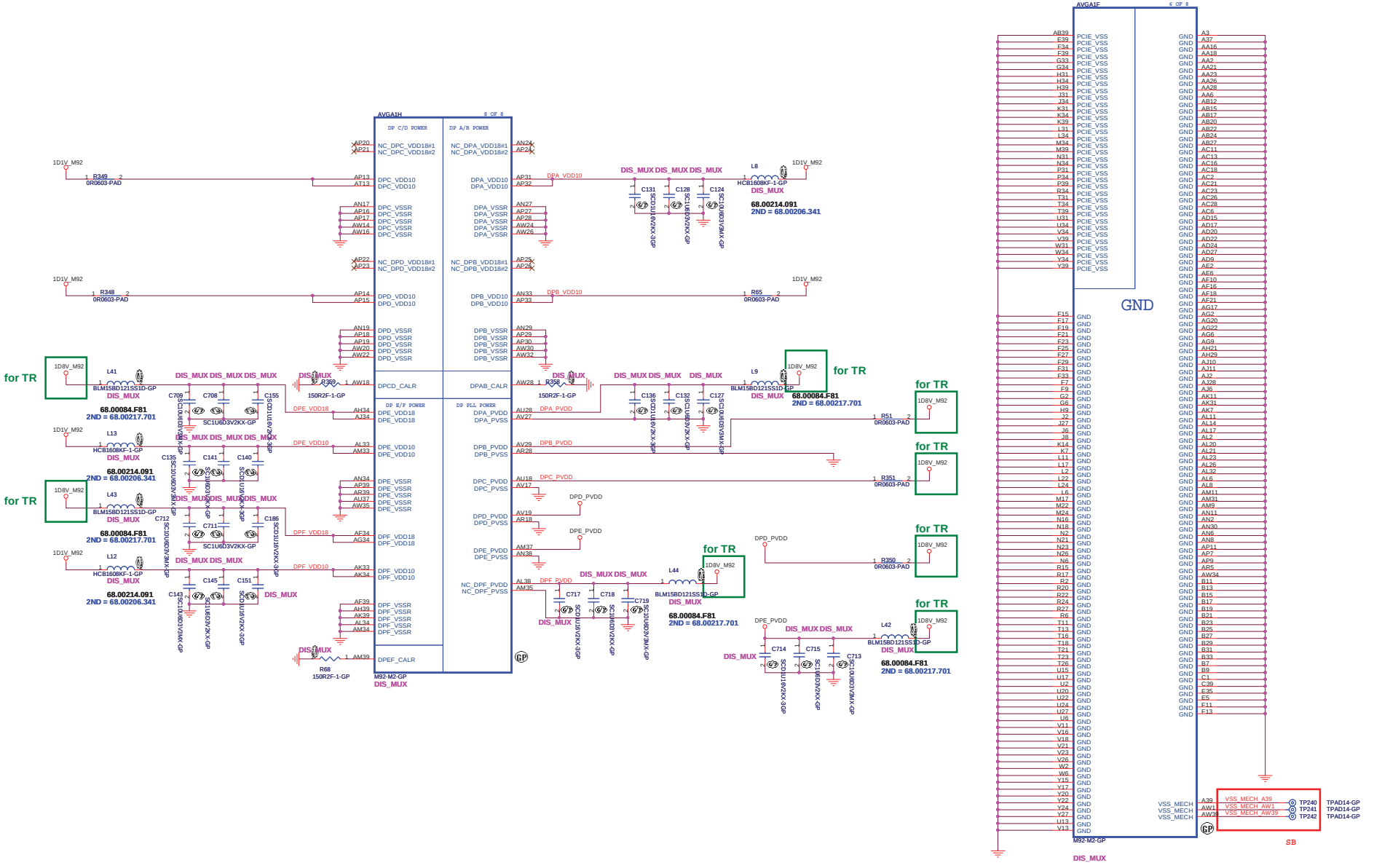
Title: M92 IO
Size: A2
Document Number: JV50-TR
Rev: SB
Date: Tuesday, June 16, 2009
Sheet 54 of 61



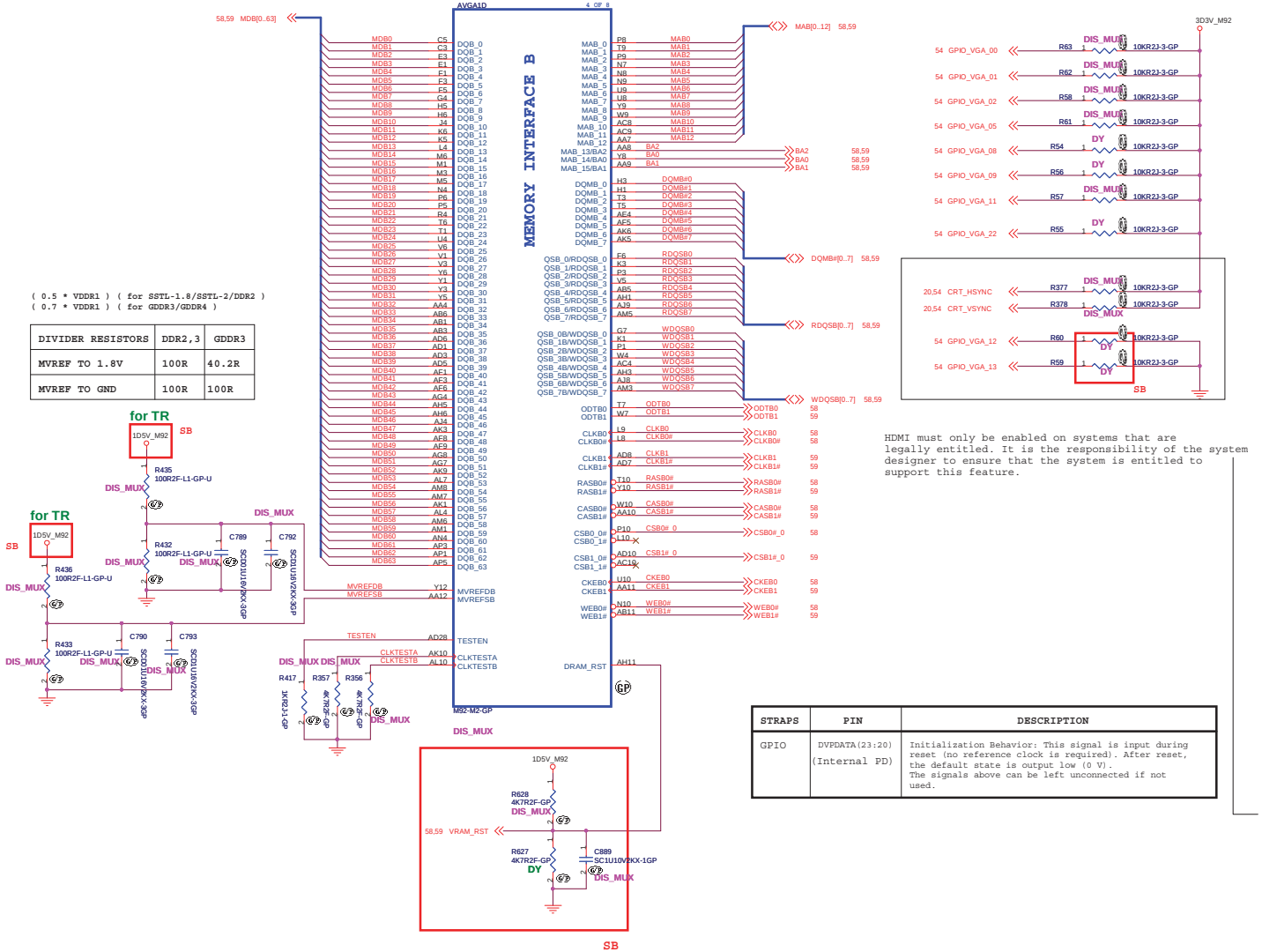
M92		
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: M92 POWER		
Size: A2	Document Number: JV50-TR	Rev: SB
Date: Tuesday, June 16, 2009	Sheet 55 of 61	



M92

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DP POWER_GND	
Size A2	Document Number JV50-TR	Rev SB
Date: Tuesday, June 16, 2009	Sheet 56 of 61	

M92-M2 uses memory group B only



DIVIDER RESISTORS	DDR2,3	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO , GPIO21_BB_EN

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
V 64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BIF_CLK_PM_EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory aperture size	X X X
PWRCNTL_[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	1
CCBYPASS	GENERICC		0

M92

緯創資通 Wistron Corporation
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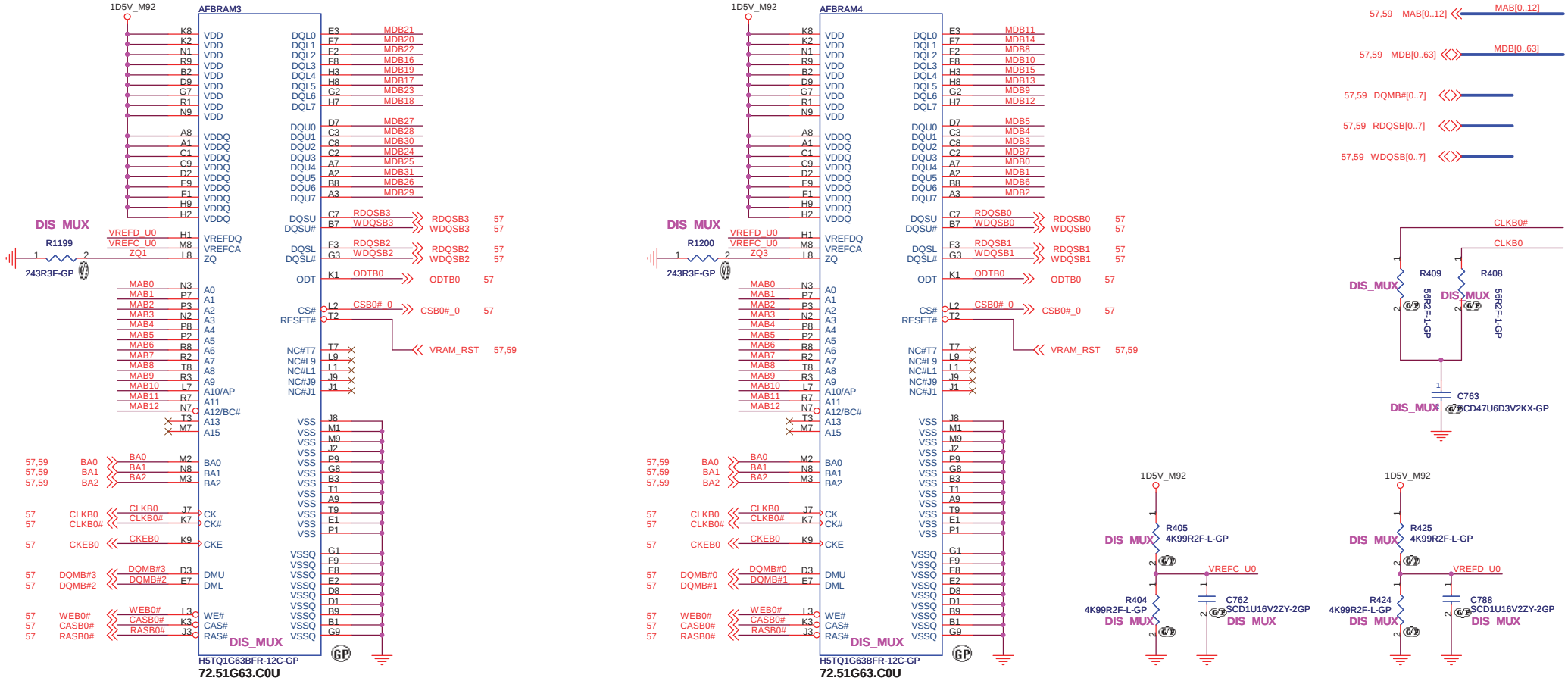
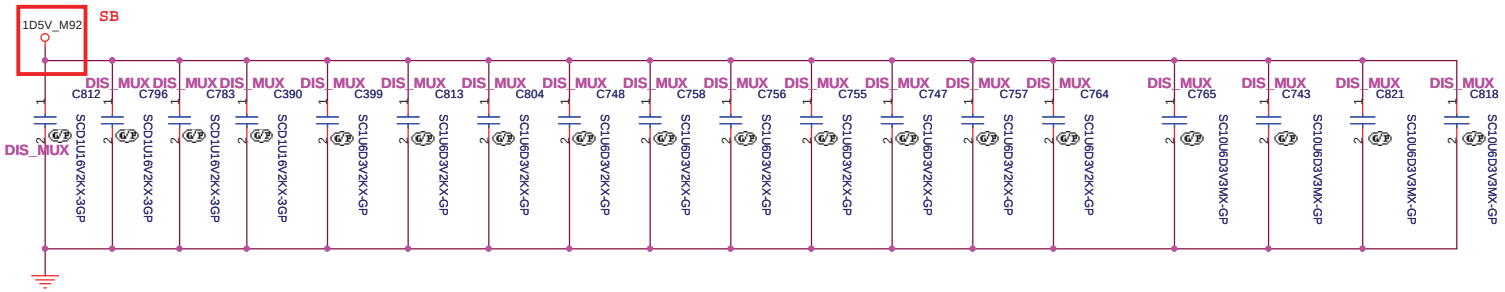
Title: Memory / Straps

Size: A2 | Document Number: JV50-TR | Rev: SB

Date: Tuesday, June 16, 2009 | Sheet 57 of 61

DDR3

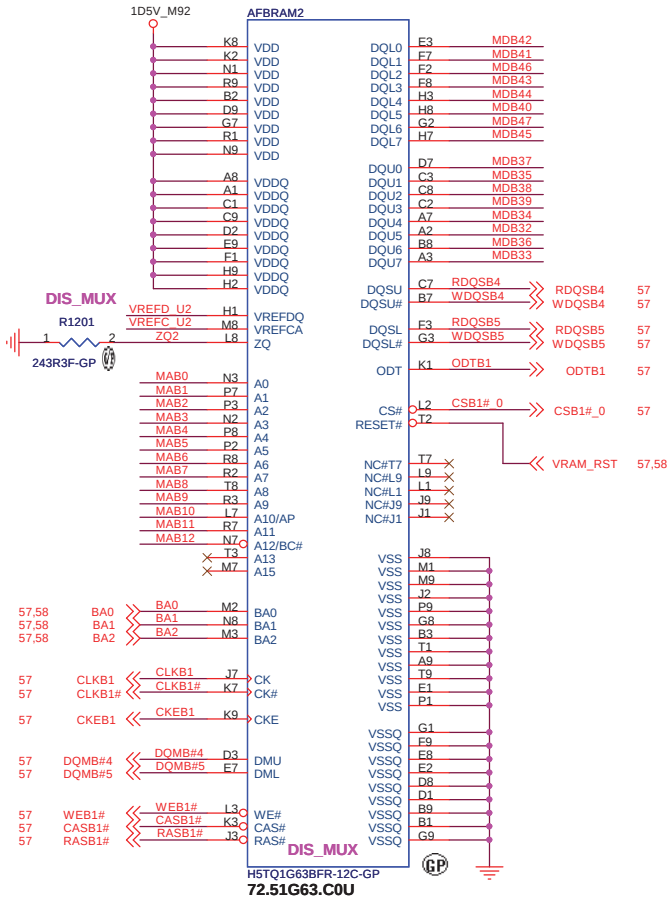


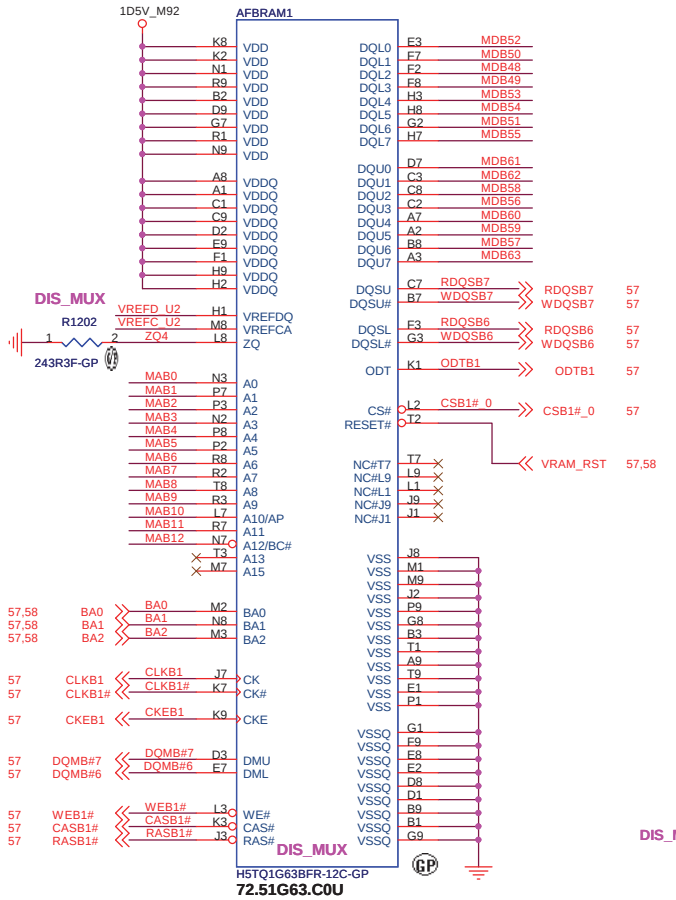


M92

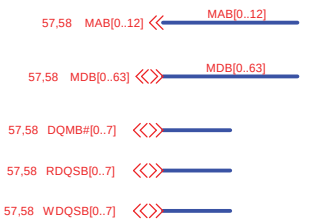
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	M92 DDR3 B0	
Size A3	Document Number JV50-TR	Rev A
Date: Tuesday, June 16, 2009	Sheet 58 of 61	

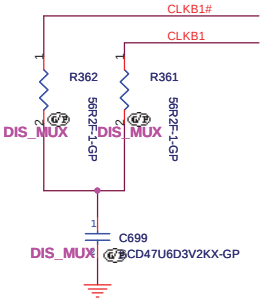
DDR3

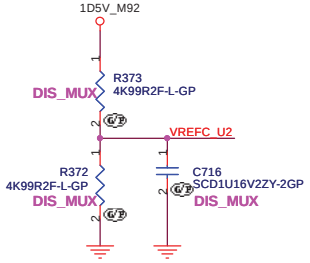


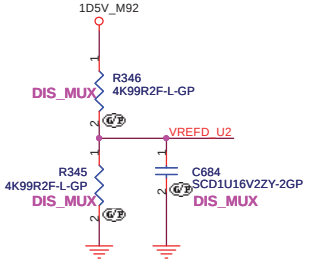


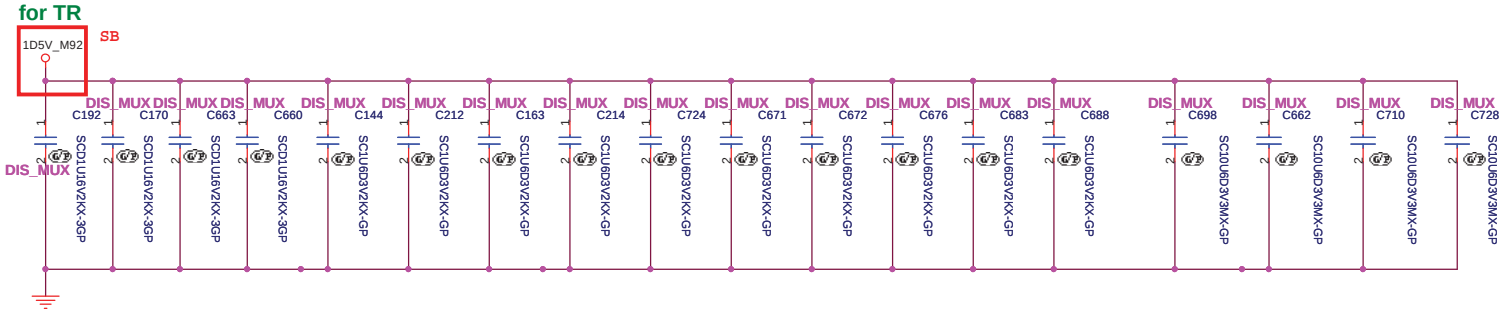
SAMSUNG 1ST=72.41164.H0U
HYUNIX 2ND=72.51G63.C0U





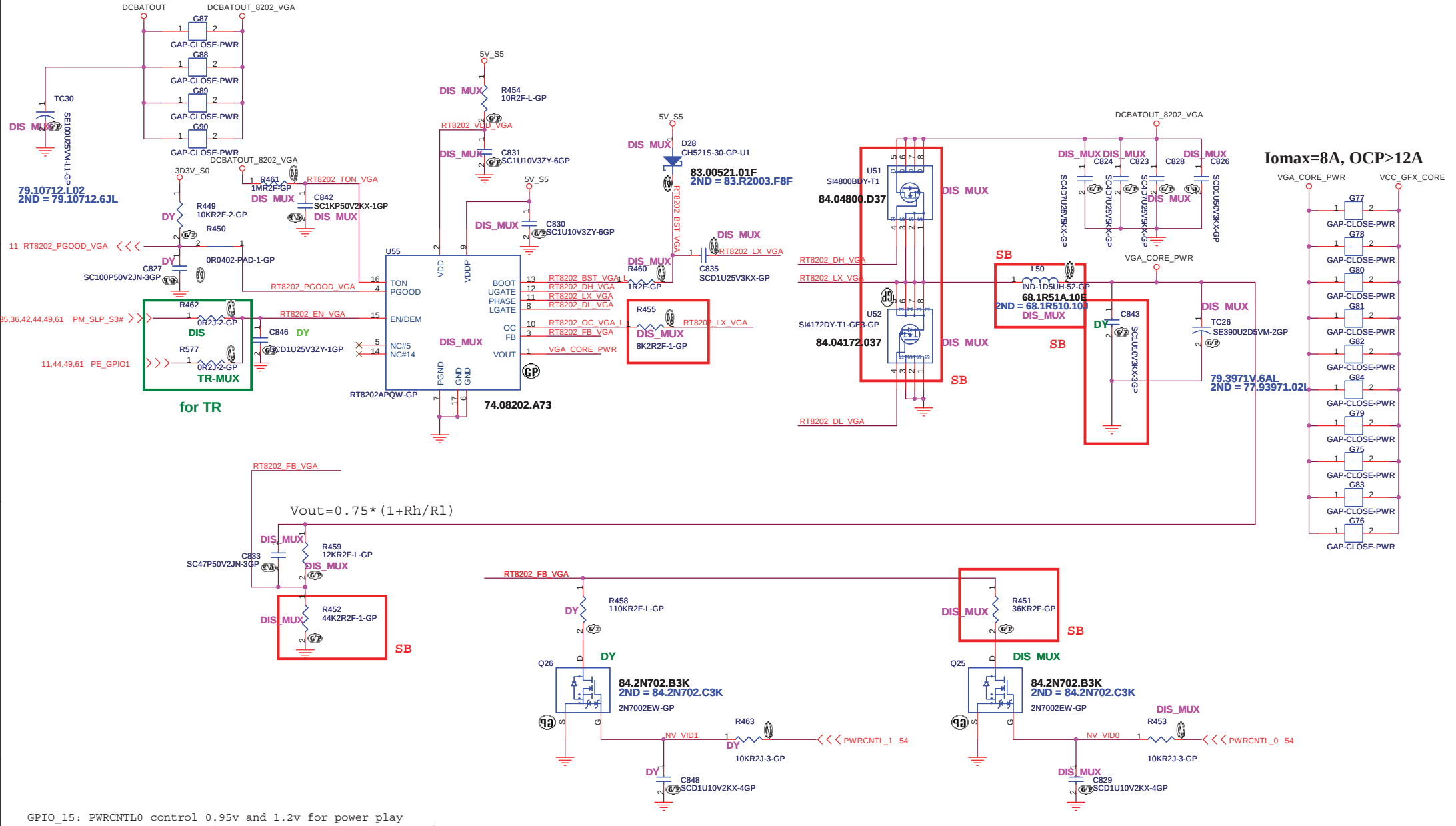






M92

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: M92 DDR3 B1		
Size: A3	Document Number: JV50-TR	Rev: SB
Date: Tuesday, June 16, 2009	Sheet 59 of 61	



GPIO_15: PWRCNTL0 control 0.95v and 1.2v for power play
M92 XT - PowerPlay States will base your power control setting change as below,
High state: 1.2V, e680/m500MHz
Medium state: 0.95V, e300/m500 MHz
Low state: 0.95V, e220/m250 MHz
UVD state: 1.2V, e600/m500 MHz

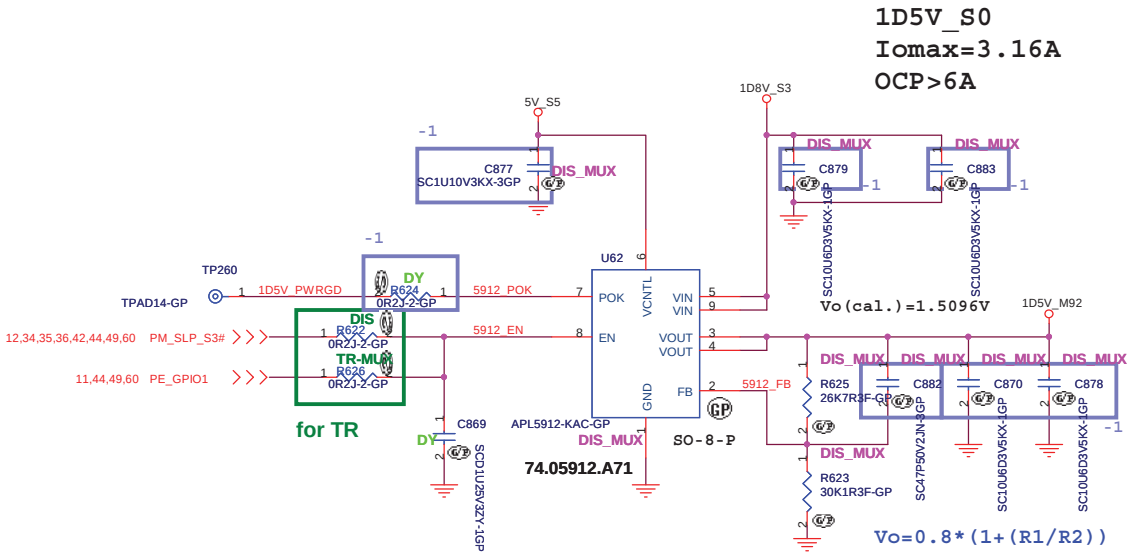
	I/O	Inter pull low	GPIO TABLE
PWRCNTL_0	O	Yes	GPU Voltage H:=1.210V GPU Voltage L:=0.954V

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8202A VGA CORE

Size	Document Number	Rev
A3	JV50-TR	SB

Date: Tuesday, June 16, 2009 Sheet 60 of 61



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APL5912 1D5V VRAM POWER

Size	Document Number	Rev
A3	JV50-TR	SB

Date: Tuesday, June 16, 2009 Sheet 61 of 61