

Compal Confidential

JALA0 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRII + ICH9M

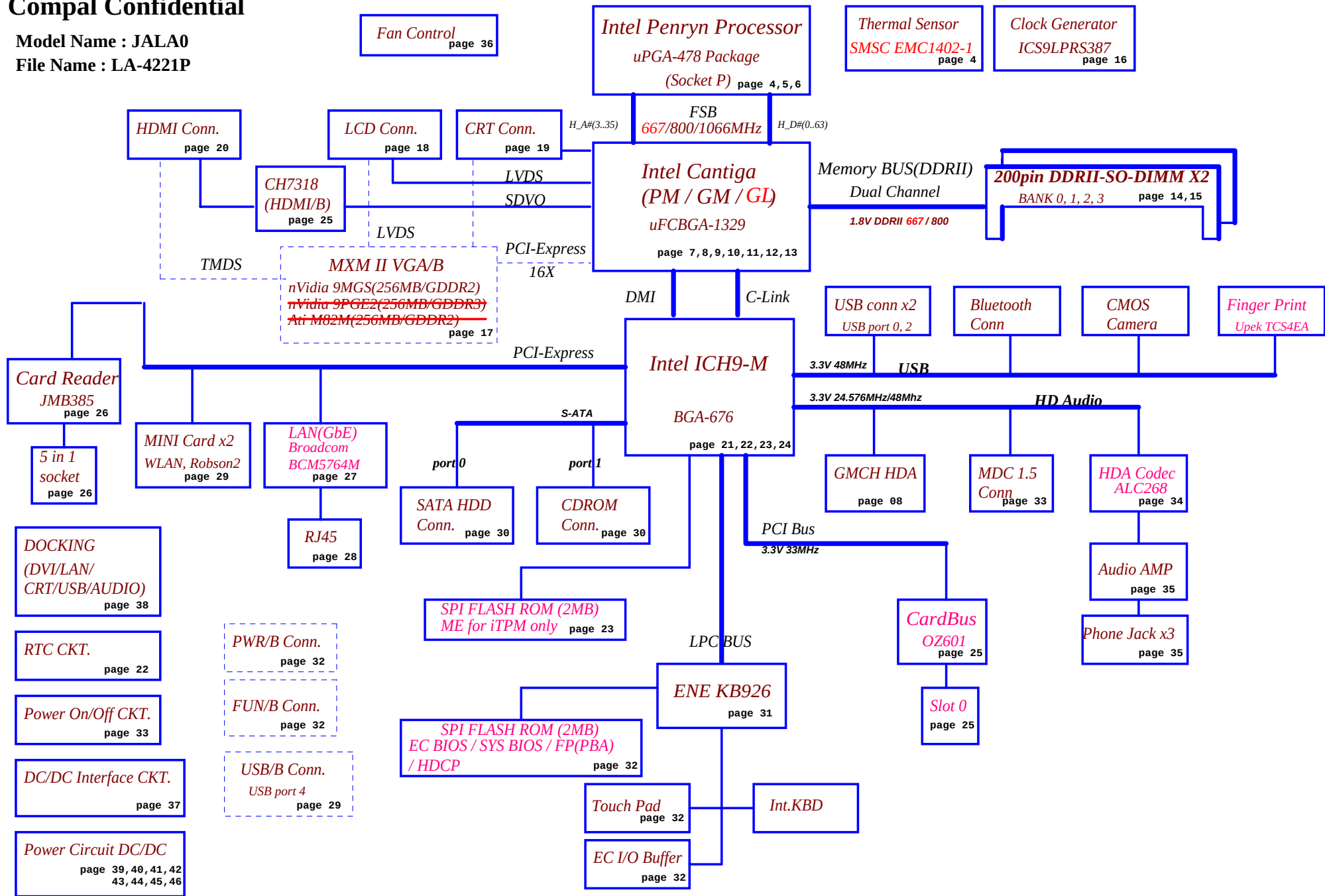
(With Ati & nVidia MXM/B)

2008-04-18

REV:1.0

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				Date	Friday, May 16, 2008	Sheet 1 of 50

Model Name : JALAO
File Name : LA-4221P



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				401552	
				Date Friday, May 16, 2008	Sheet 2 of 50

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Cardbus OZ601	AD16	0	PIRQE

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADT7421	1001 100X b
EEPROM(24C16/02)	1010 000X b	(LAN BCM5764M)	Reserved
GPU(MXM/B)	1001 111X b		

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM1	1001 010Xb
LAN BCM5764M	Reserved
(MINI CARD_WL_Robson)	Reserved

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

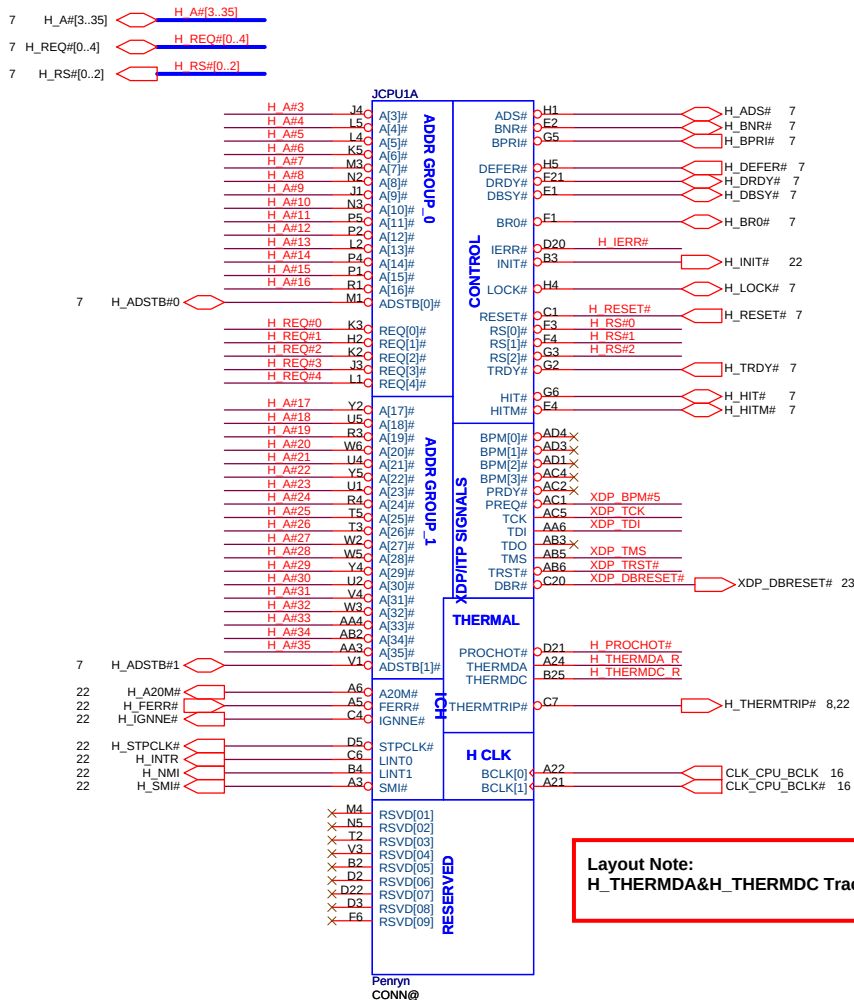
BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

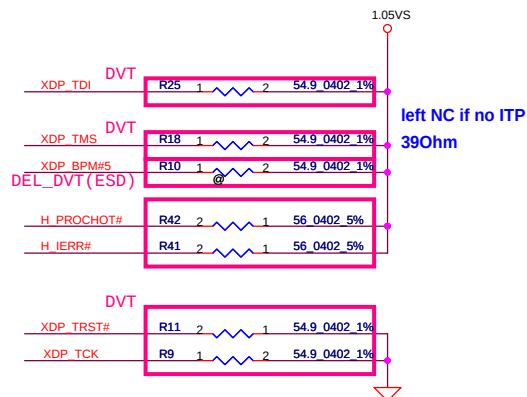
BTO Option Table

BTO Item	BOM Structure
Discrete_H	PM@
UMA	GM@
UMA_H	UMAGM@
UMA_L	UMAGL@
Kinabalu_H	MAIN@
Kinabalu_L	VALUE@
RTC Batt	45@
ICH9M BASE	ICH9MB@
ICH9M ENHANCE	ICH9ME@
SB ROM(2MB)	SPI2MB@
SB ROM(4MB)	SPI4MB@

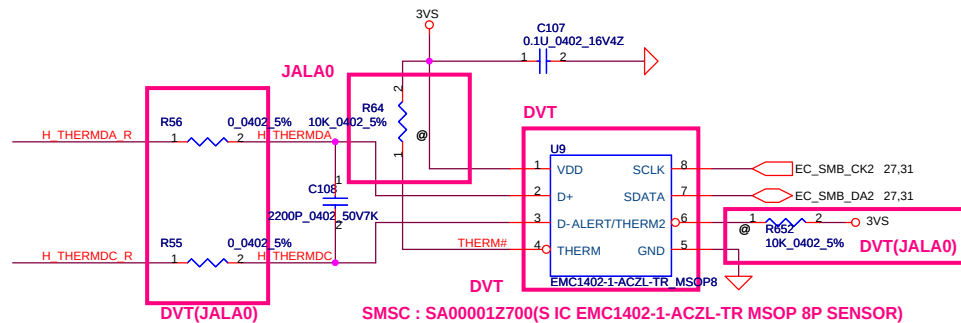
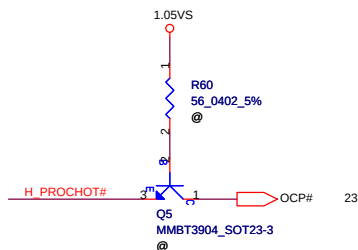
Kinabalu_L : UMA(GL) & w/o Dock & w/o Mini card 2 & w/o iTPM



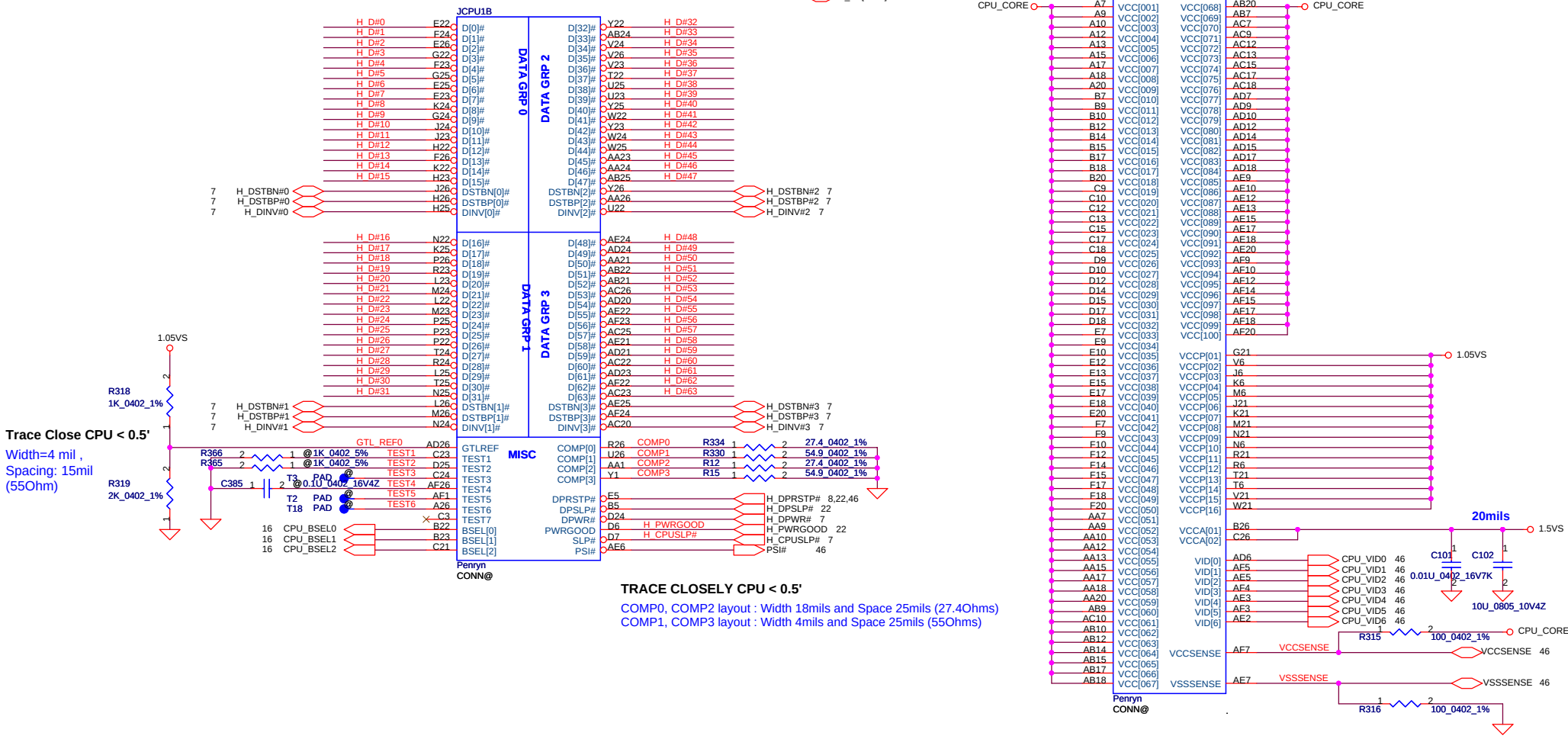
Layout Note:
H_THERMDA&H_THERMDC Trace / Space = 10 / 10 mil

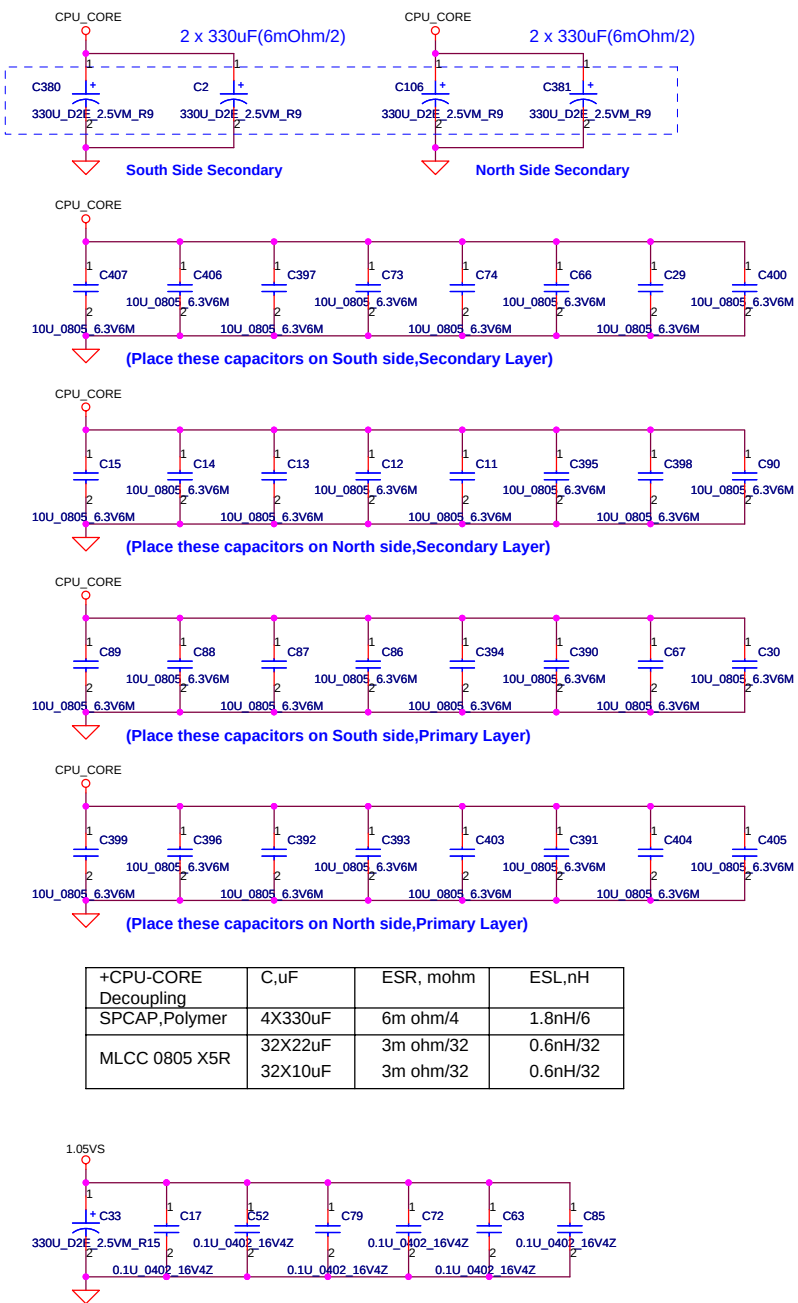
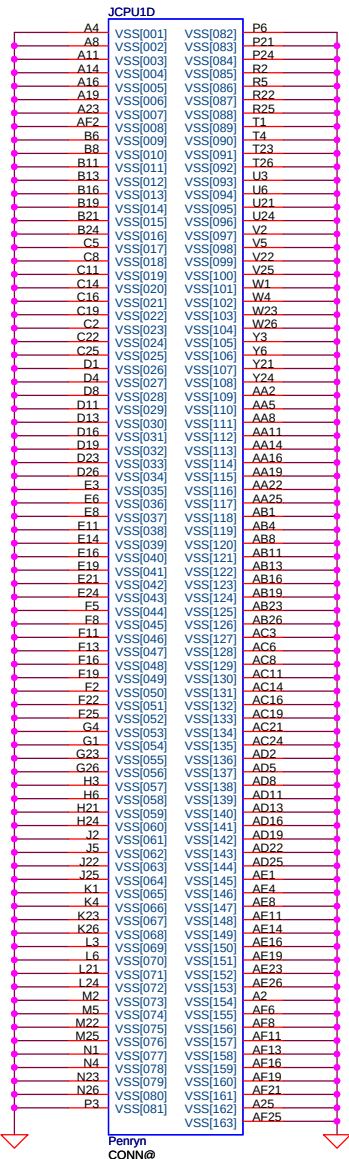


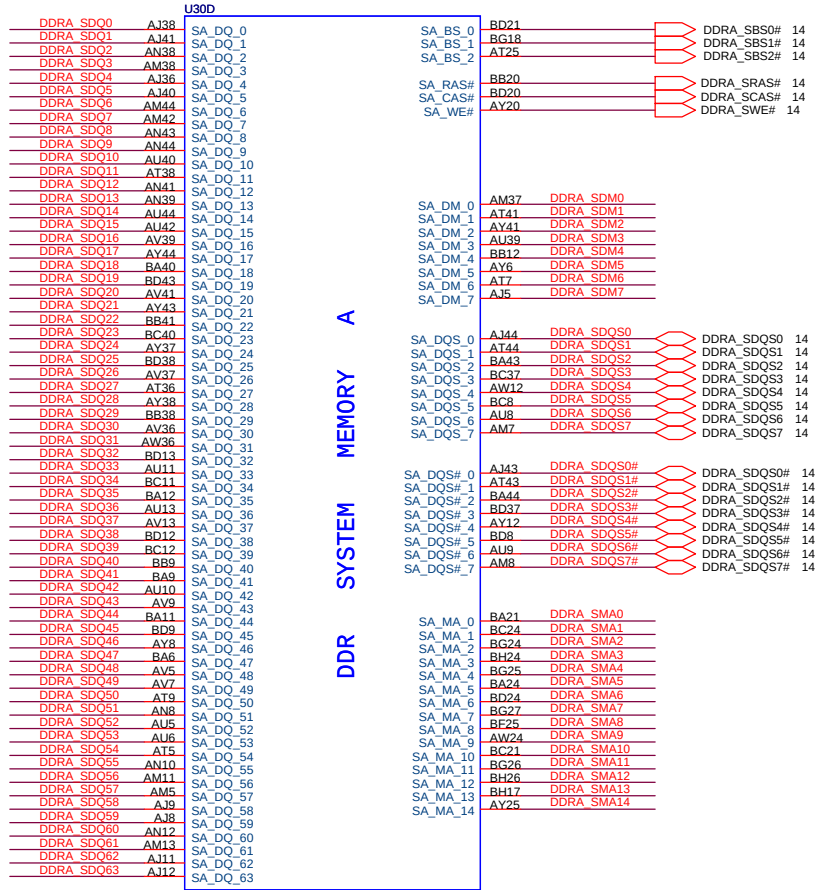
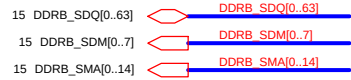
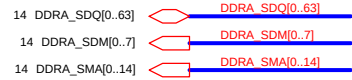
BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166



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				Date	Friday, May 16, 2008
				Sheet	4 of 50







CANTIGA ES_FCBGA1329
UMAGM@



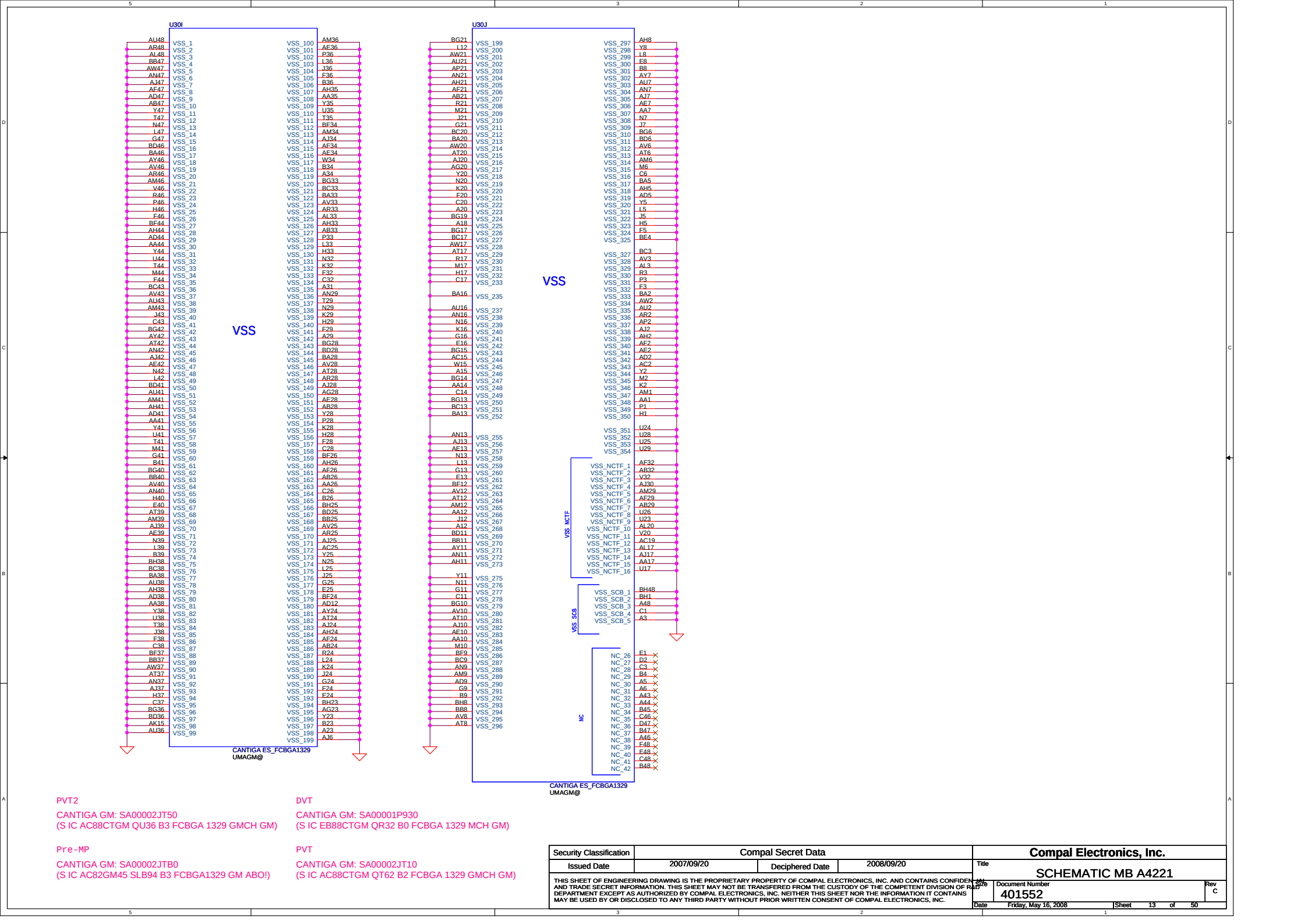
CANTIGA ES_FCBGA1329
UMAGM@

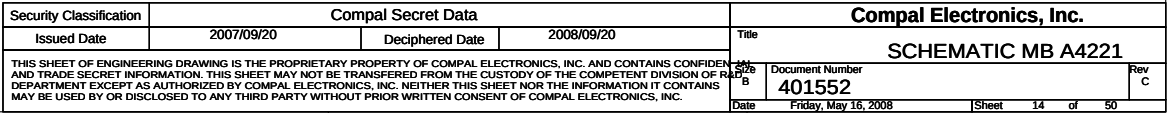
DVT CANTIGA GM: SA00001P930 Pre-MP CANTIGA GM: SA00002JTBO
(S IC EB88CTGM QR32 B0 FCBGA 1329 MCH GM) (S IC AC82GM45 SLB94 B3 FCBGA1329 GM ABO!)

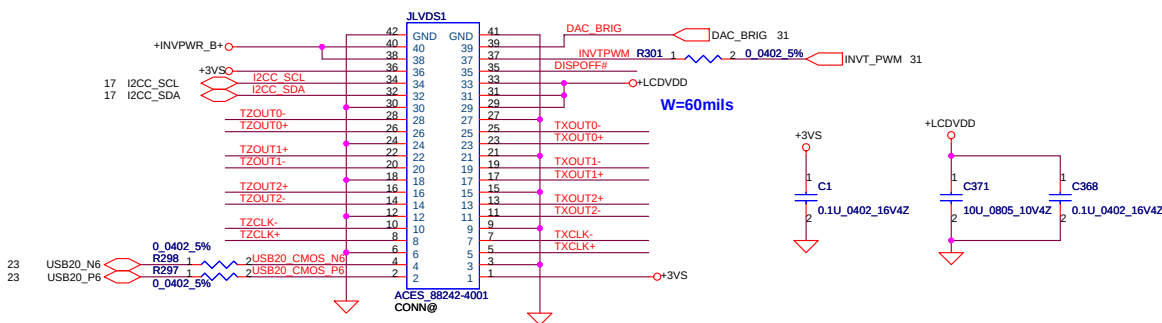
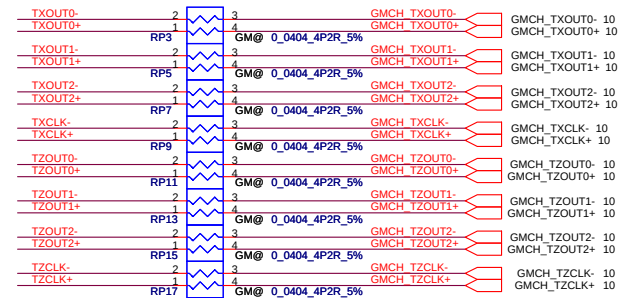
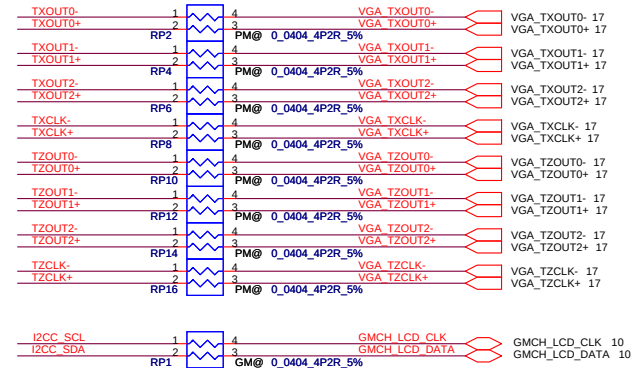
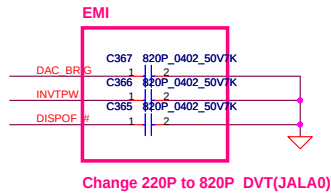
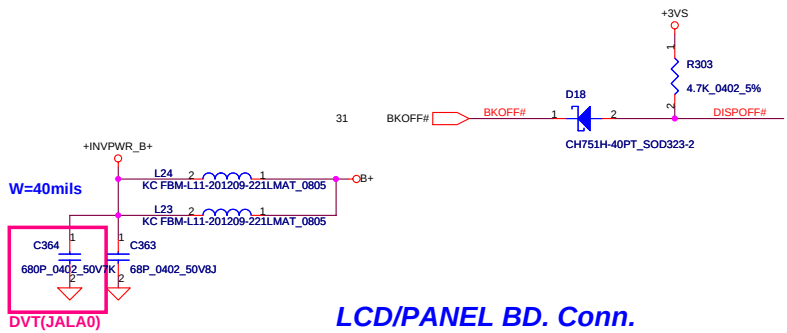
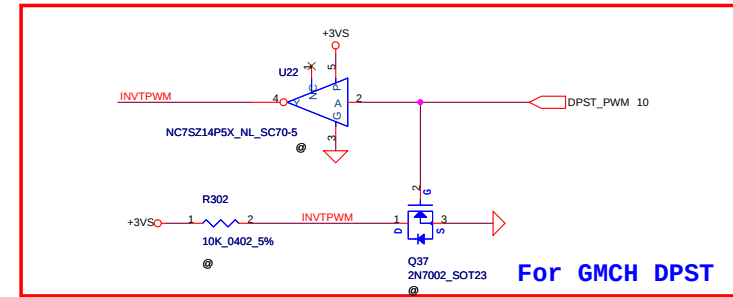
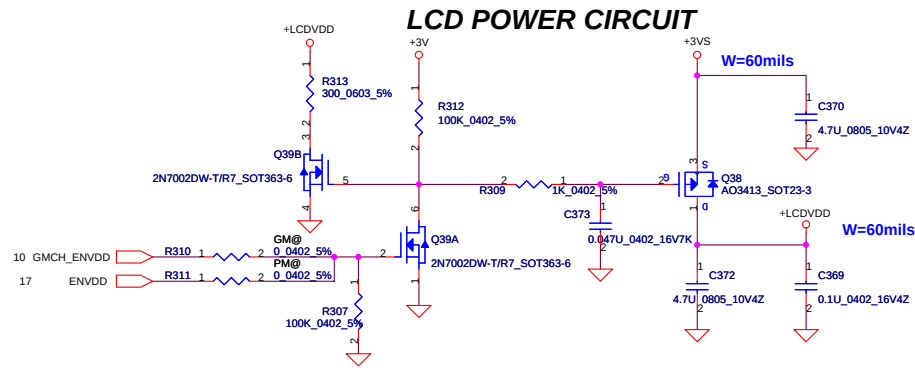
PVT CANTIGA GM: SA00002JT10
(S IC AC88CTGM QT62 B2 FCBGA 1329 GMCH GM)

PVT2 CANTIGA GM: SA00002JT50
(S IC AC88CTGM QU36 B3 FCBGA 1329 GMCH GM)

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Size B	Document Number 401552	Rev C	Date: Friday, May 16, 2008	Sheet 9	of 50

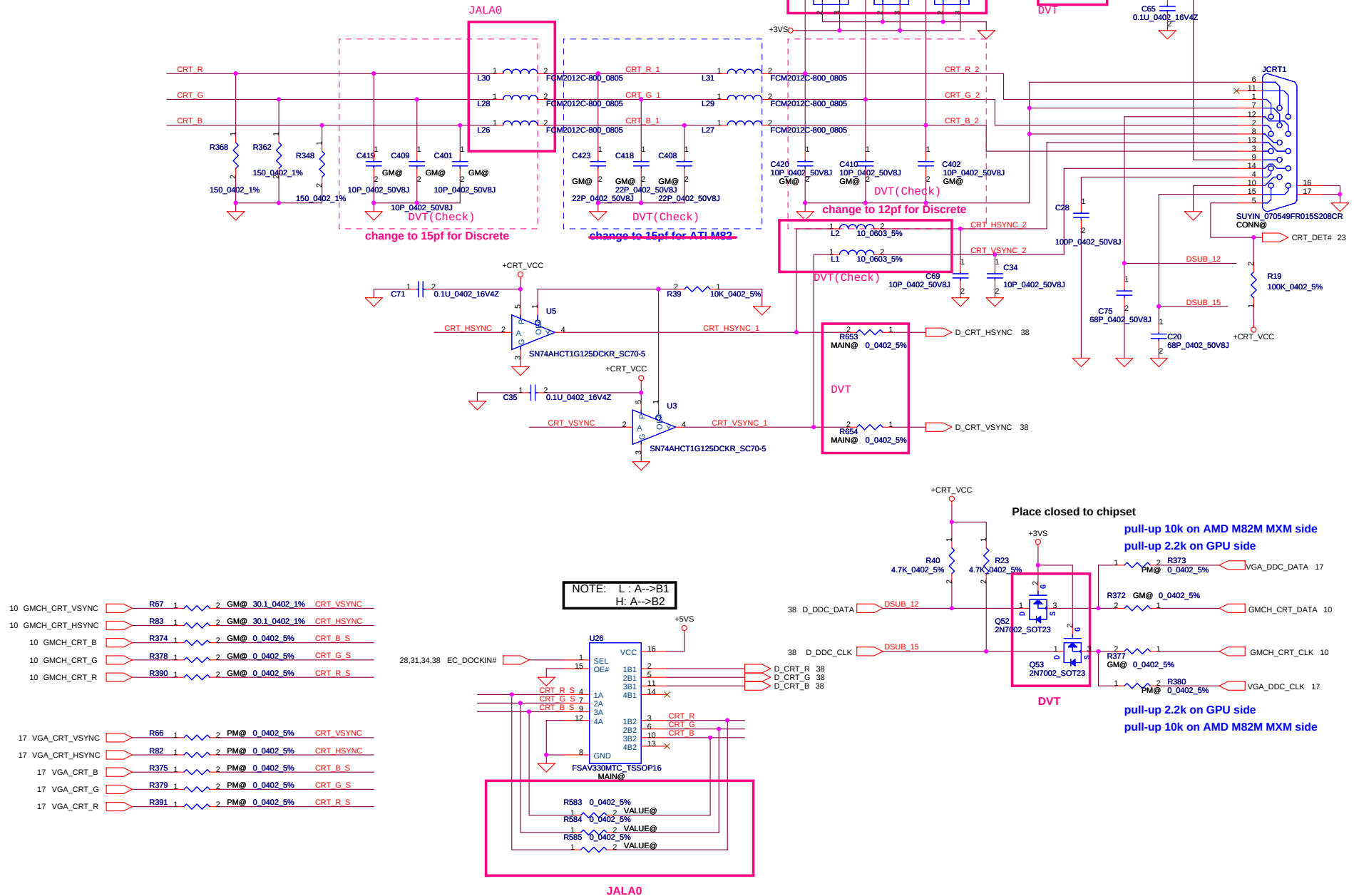




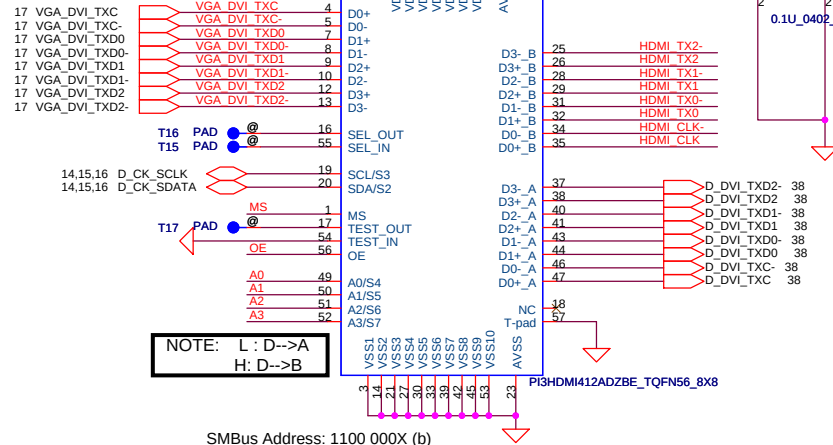
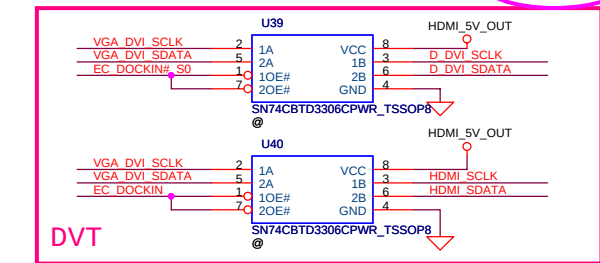
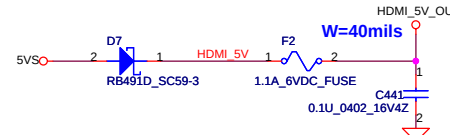
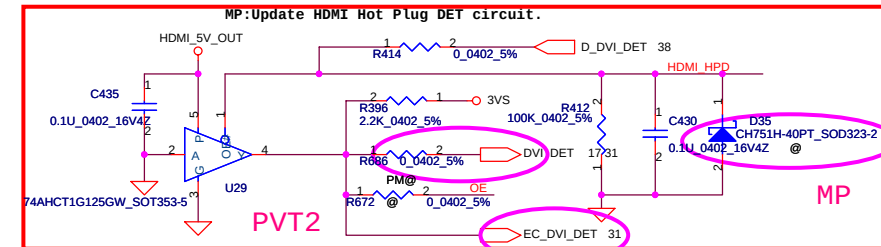
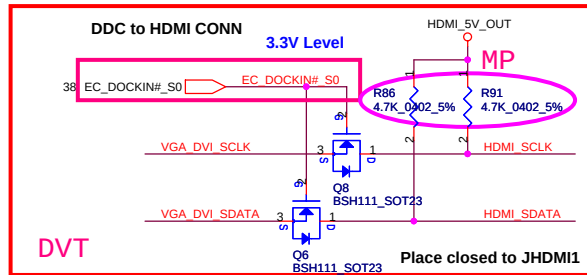
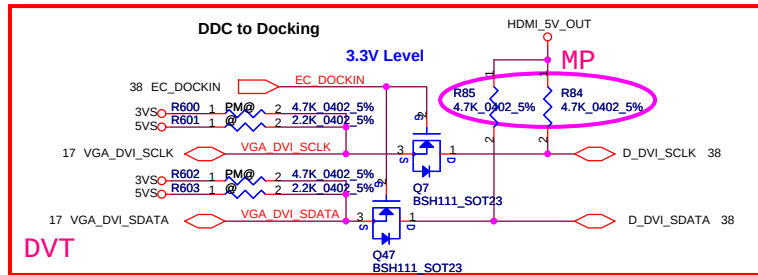


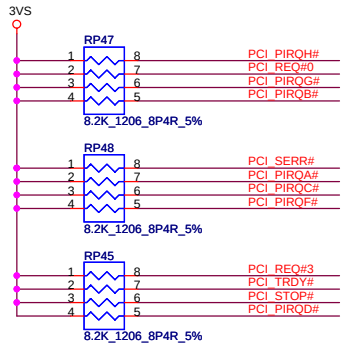
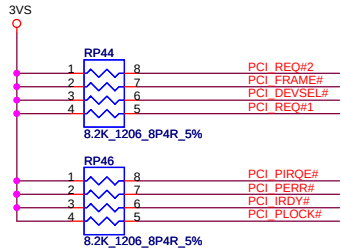
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Date				Friday, May 16, 2008				Sheet 18 of 50			

CRT Connector



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				401552				C			
Date				Friday, May 16, 2008				Sheet 19 of 50			

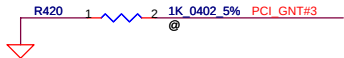




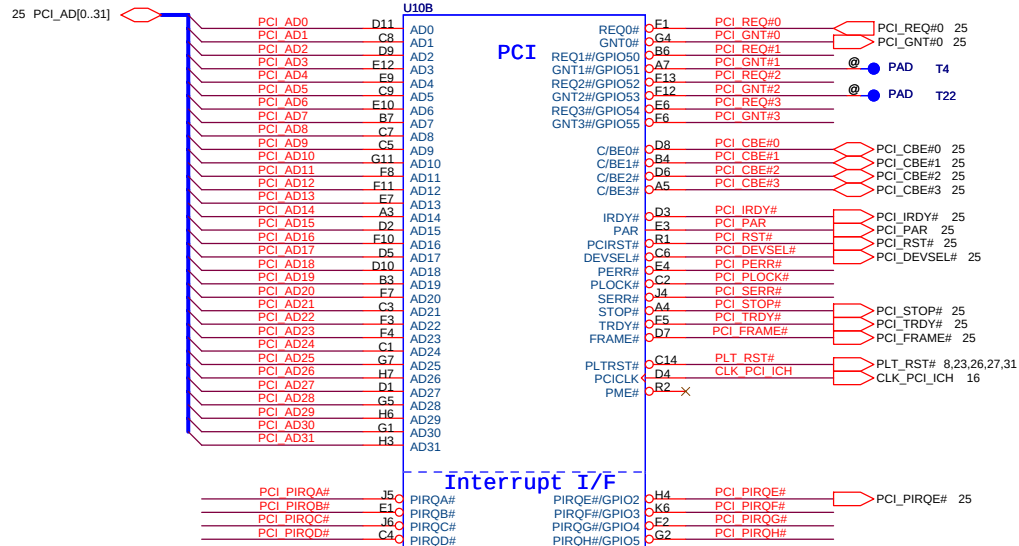
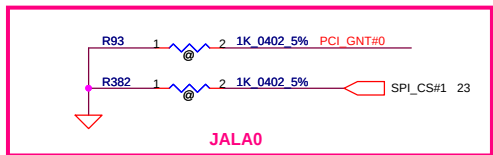
A16 Swap Override Strap

Low= A16 swap override Enable
High= Default*

PCI_GNT#3



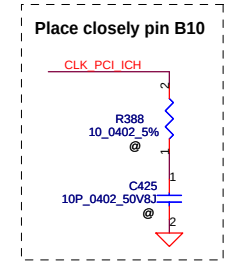
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



DMI for ESI-compatible operation

Low= DMI for ESI-compatible operation
High= Default* (Internal pull-up)

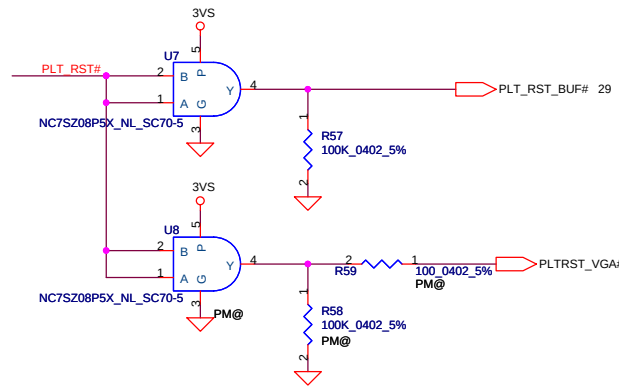
PCI_GNT#1



DVT ICH9-M: SA00002AN10
(S IC NH82801IBM QP23 A2 FCBGA 676P ICH9M)

PVT ICH9-M: SA00002JH00
(S IC AF82801IBM QT09 A3 PBG 676P ICH9M)

Pre-MP ICH9-M: SA00002JH70
(S IC AF82801IBM SLB8Q A3 676P ICH9M ABO!)

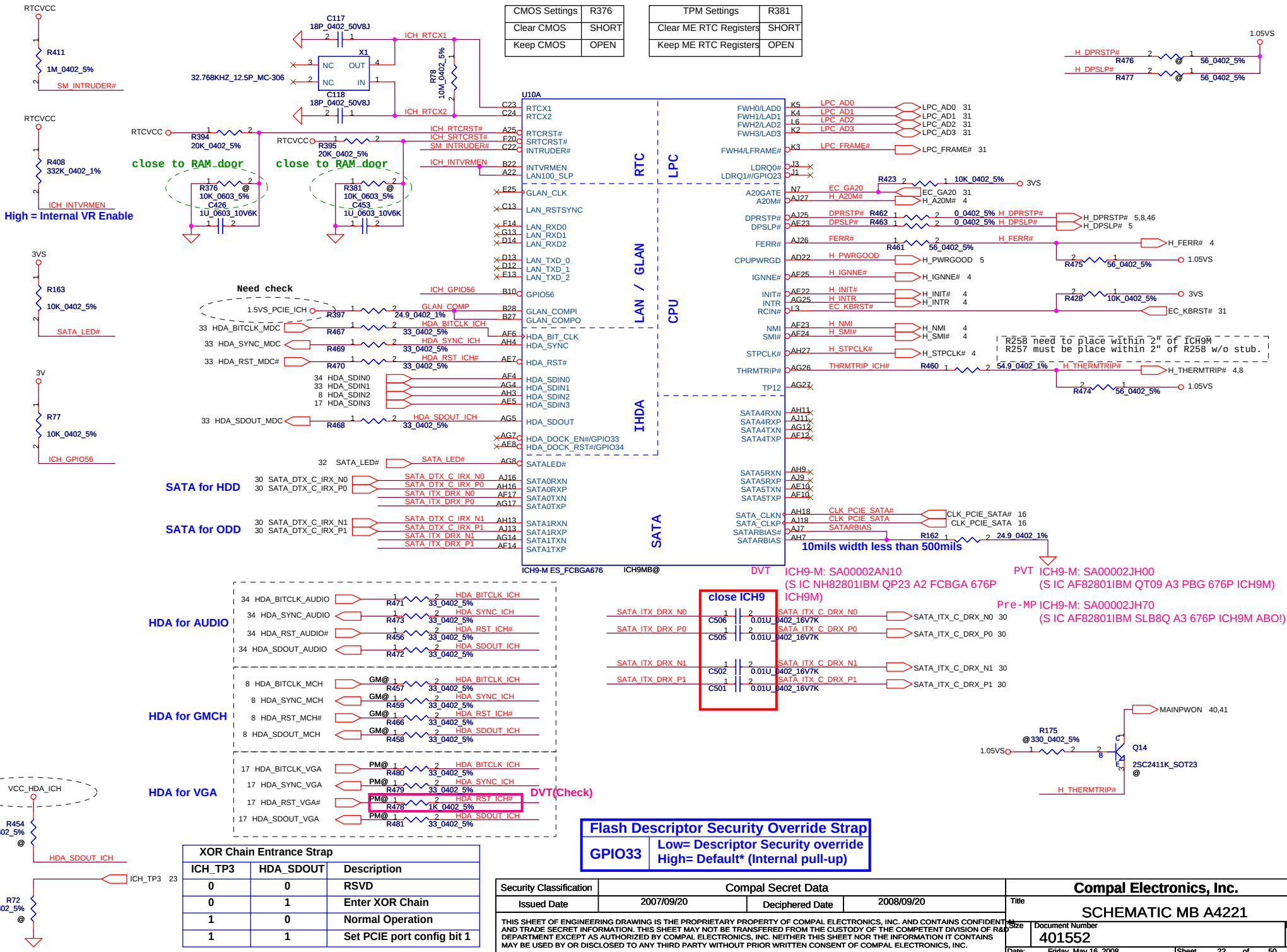


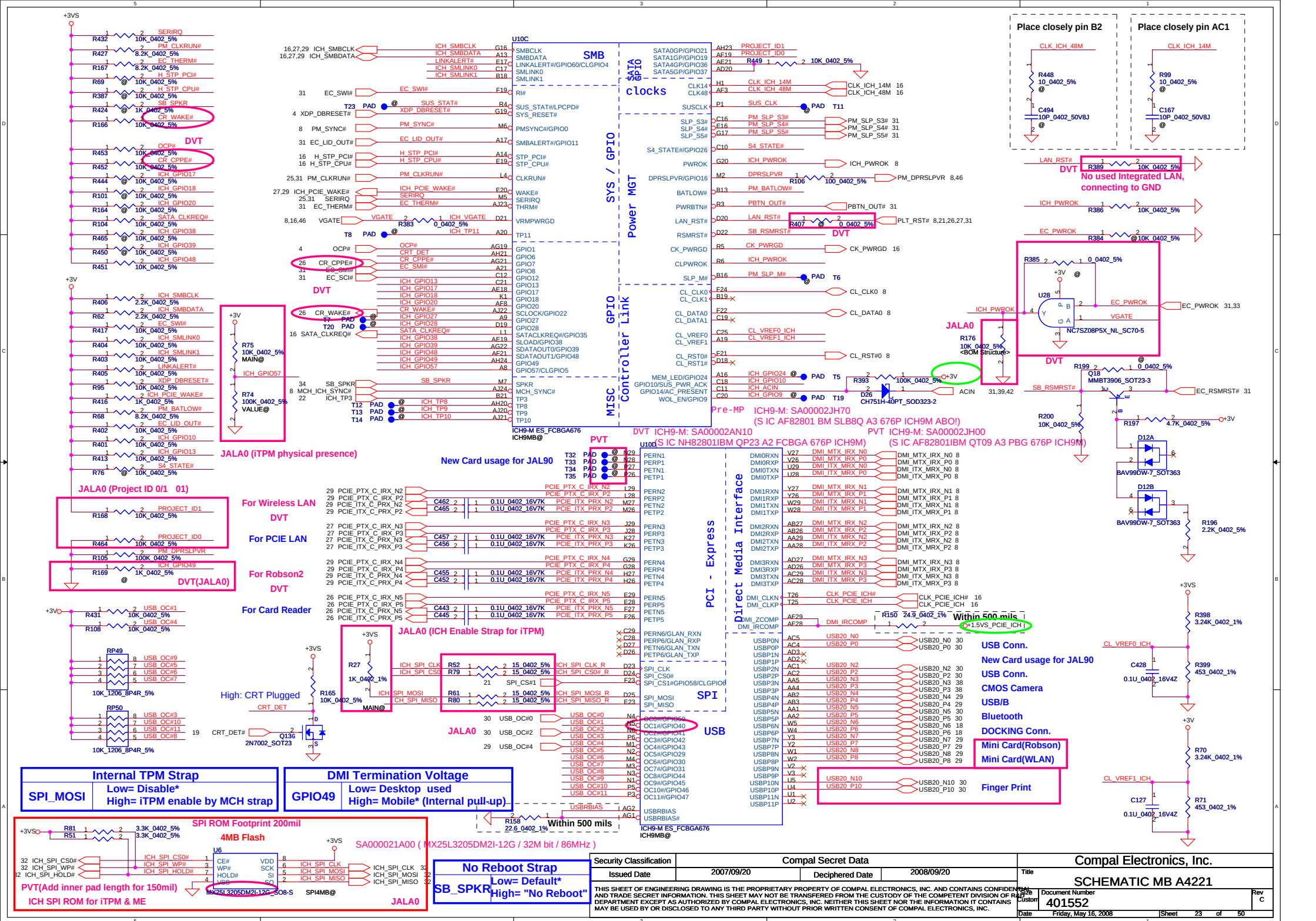
For VGA/B

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				Date	Friday, May 16, 2008
				Sheet	21 of 50

CMOS Settings	
Clear CMOS	SHORT
Keep CMOS	OPEN

TPM Settings	
Clear ME RTC Registers	SHORT
Keep ME RTC Registers	OPEN

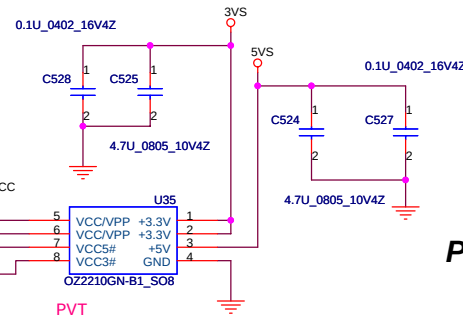
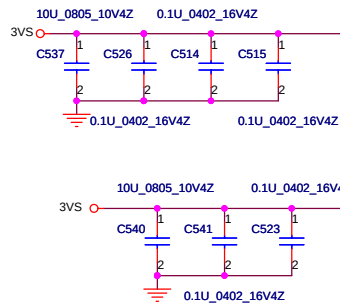




21 PCI_AD[0..31] PCI AD[0..31]

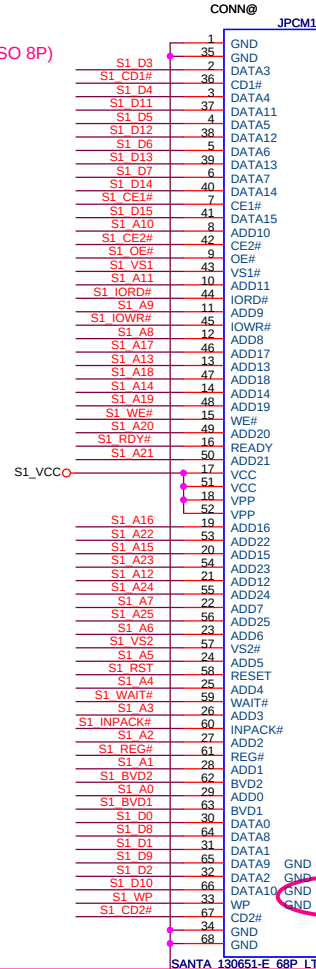
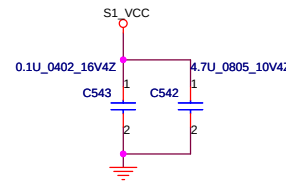
21 PCI_CBE#[0..3] PCI CBE#[0..3]

IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)



PCMCIA Socket

PVT
SA000026P10 (S IC OZ2210GN-B1 SO 8P)



Footprint as SANTA_130651-E_68P_LT-S
DVT(JALA0)

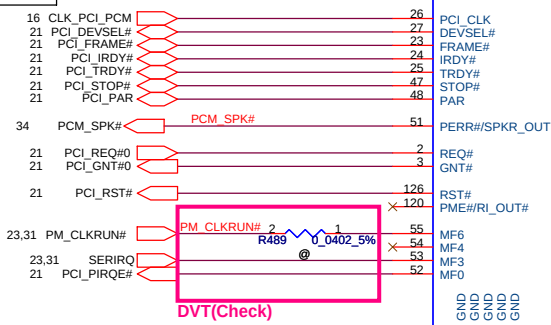
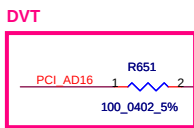
NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME. IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS. THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

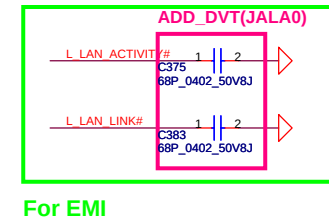
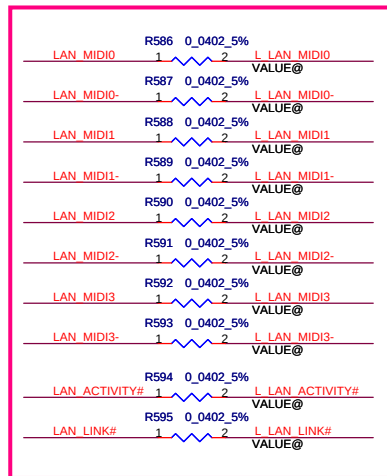
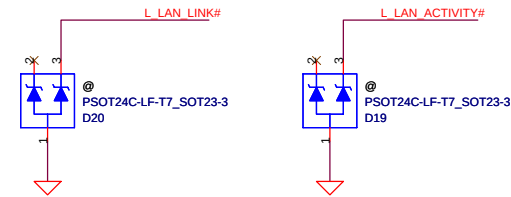
CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN F4



22K TO 47K PULL-UPS MUST BE PLACED ON INTA#, PME#, SERIRQ# & CLKRUN#.

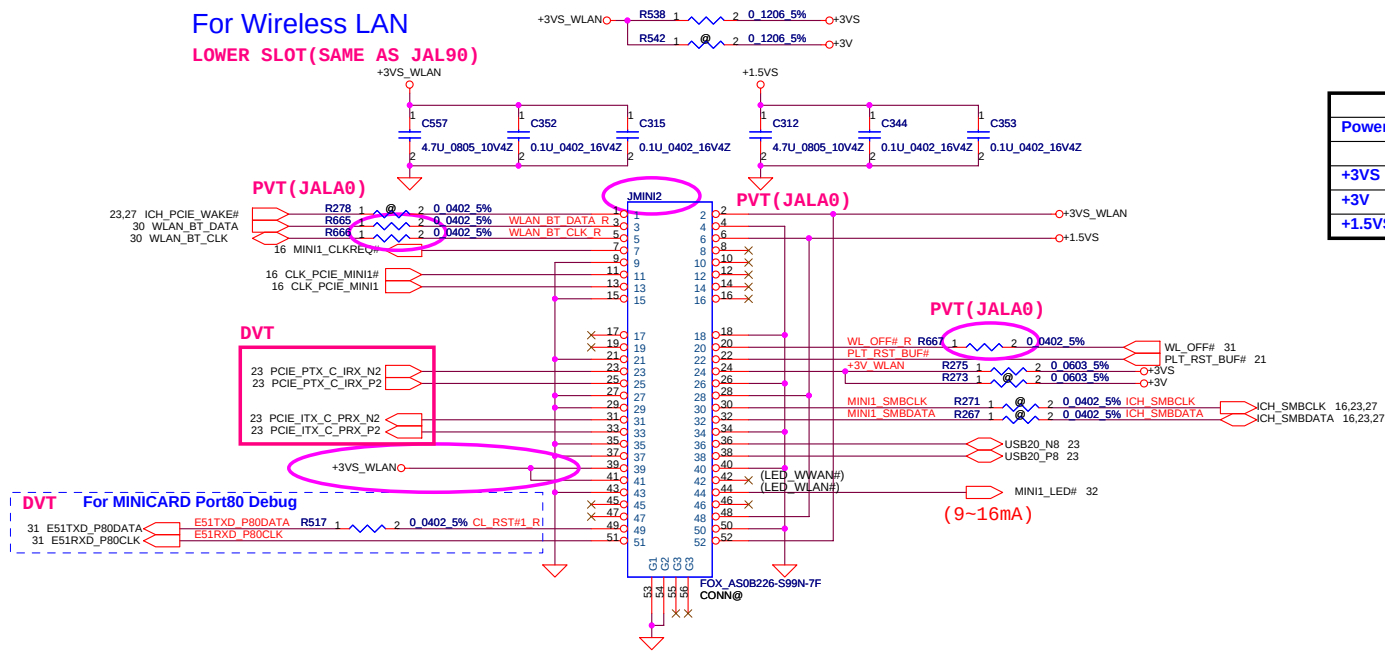
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Date: Friday, May 16, 2008				Sheet	25 of 50



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For Wireless LAN

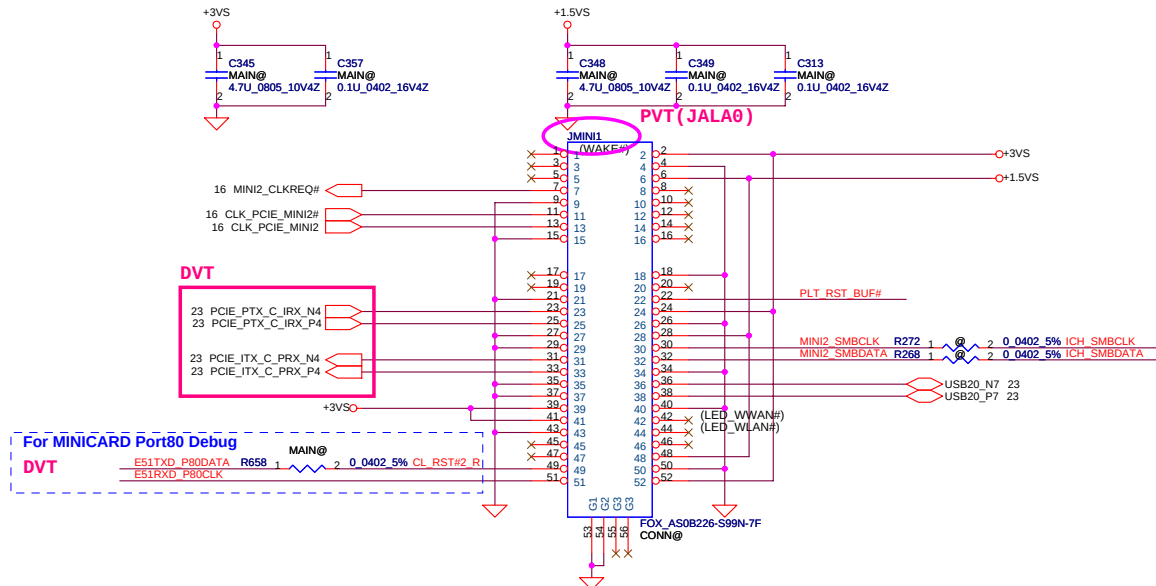
LOWER SLOT(SAME AS JAL90)



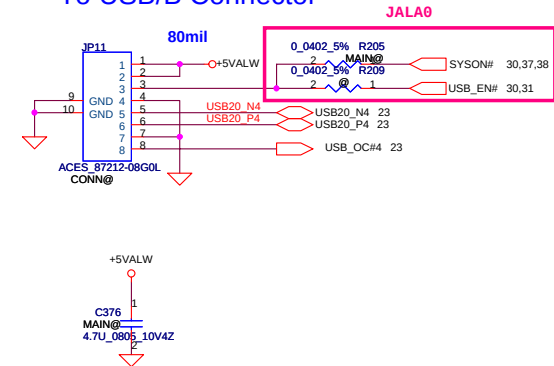
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

For Robson2

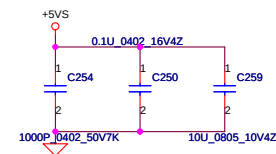
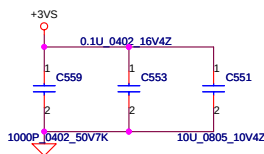
UPPER SLOT(SAME AS JAL90)



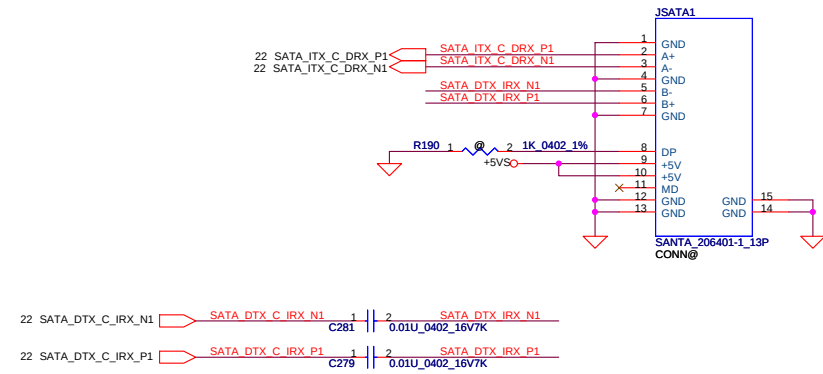
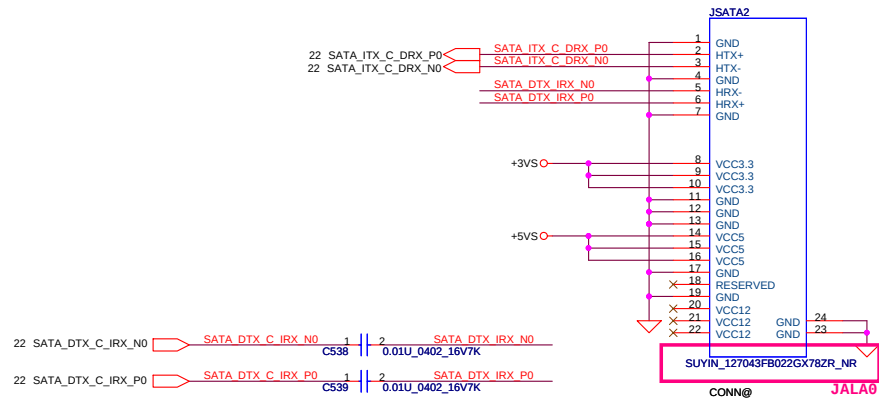
To USB/B Connector



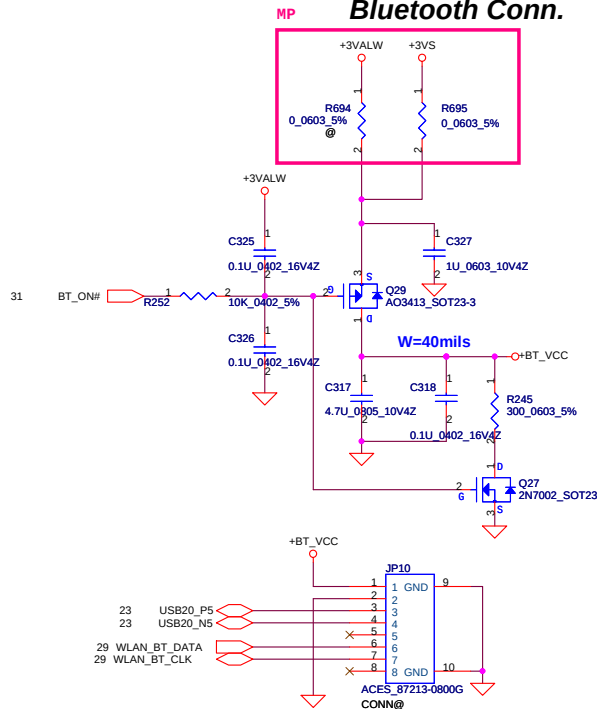
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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Date				Friday, May 16, 2008				Document Number			
401552				Rev C				Sheet 29 of 50			



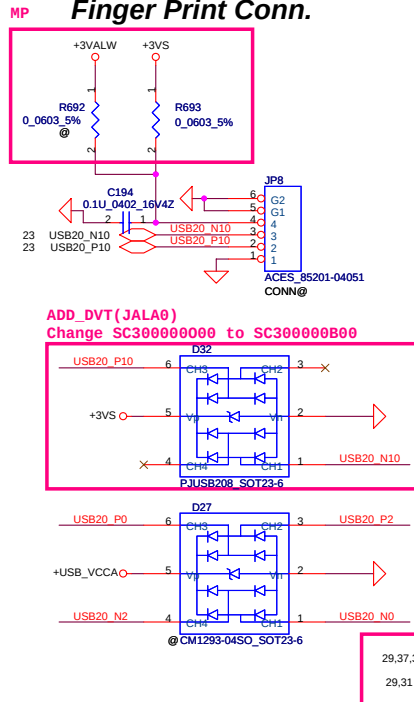
SATA HDD Conn.



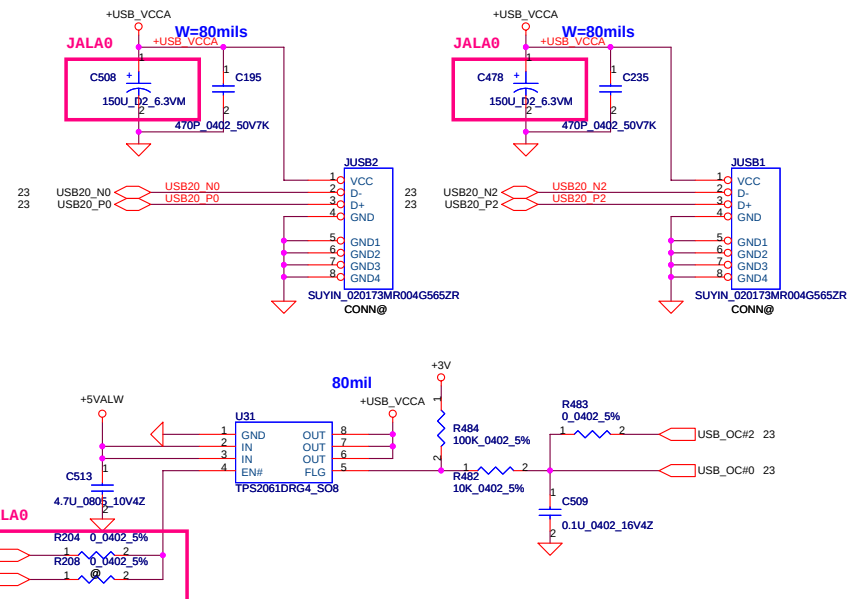
Bluetooth Conn.



Finger Print Conn.

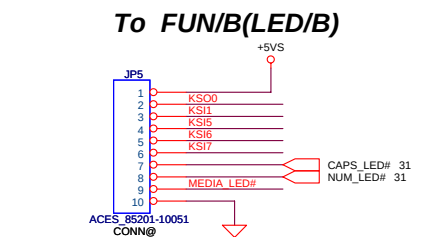
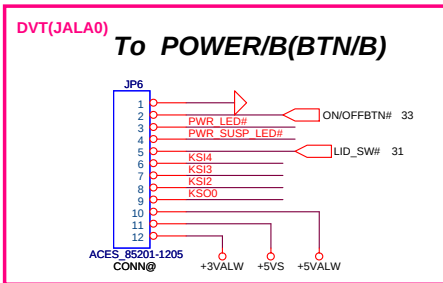
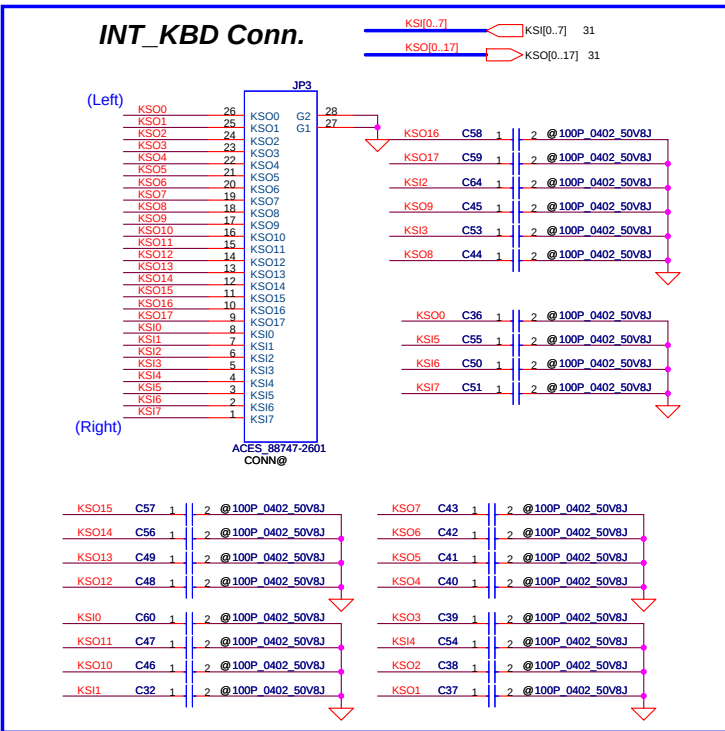
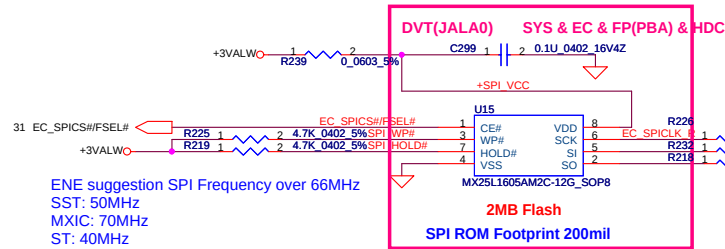


USB CONN. (Stack-up Type)

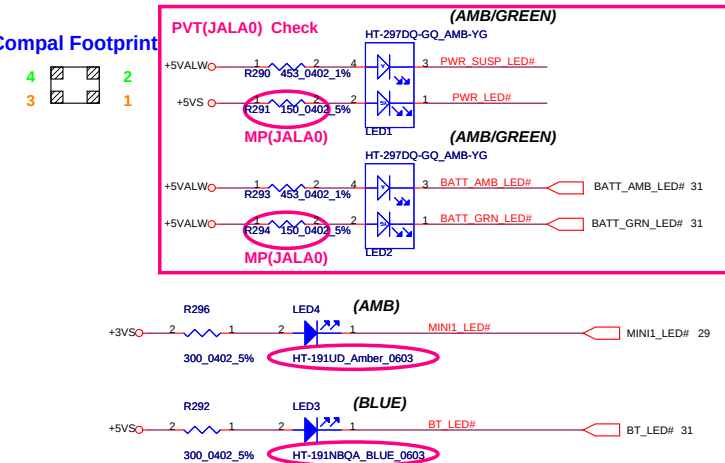
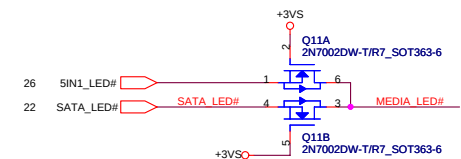
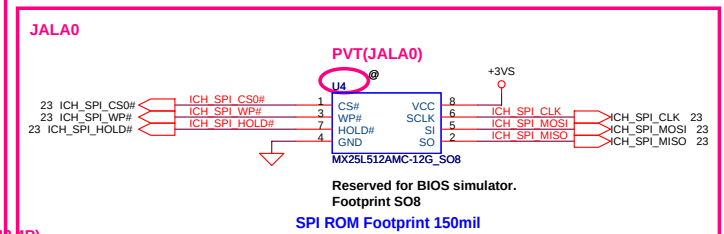
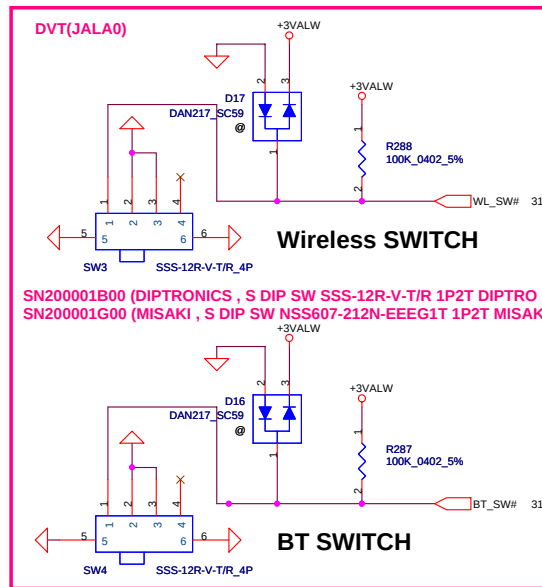
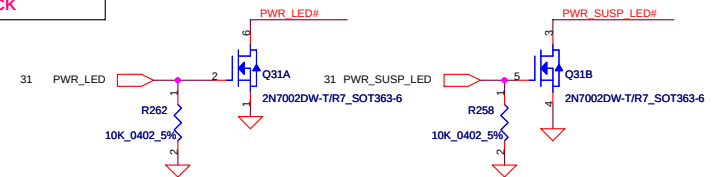
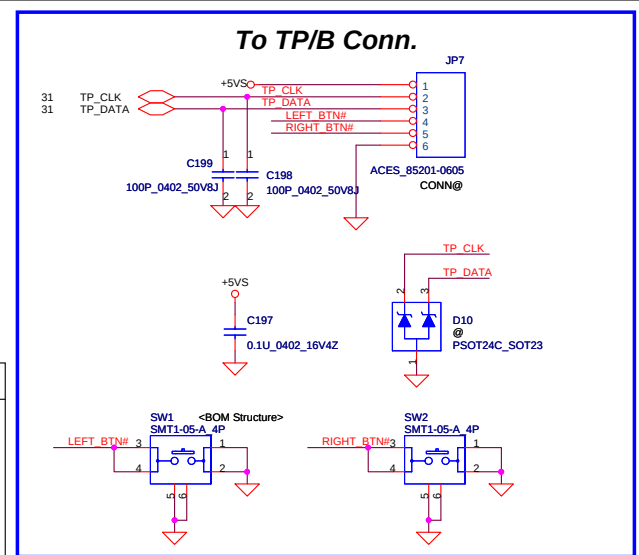


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				401552		
Date	Friday, May 16, 2008	Sheet	30	of	50	

2MB SA00001J700 (MXIC, S IC FL 16MBIT MX25L1605AM2C-12G S08 ROM, 85MHz)
2MB SA00001O200 (WINBOND, S IC FL 32MBIT W25X32VSSIG SOIC 8P 3.3V, 75MHz)



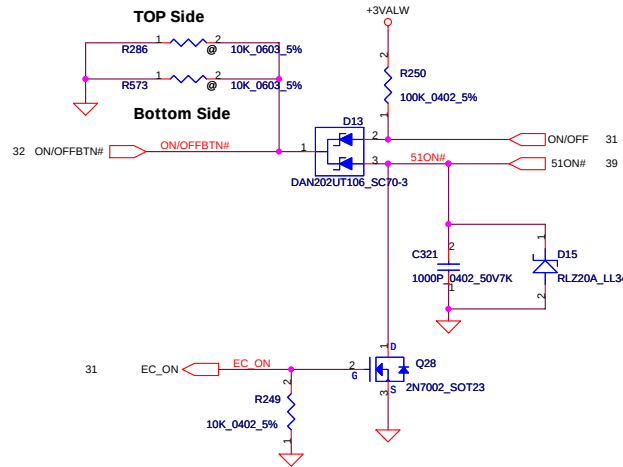
	KSO0
KSI1	PRESENTATION
KSI2	Program BTN#
KSI3	EMAIL BTN#
KSI4	IE BTN#
KSI5	E-KEY BTN#
KSI6	SYNC
KSI7	LOCK



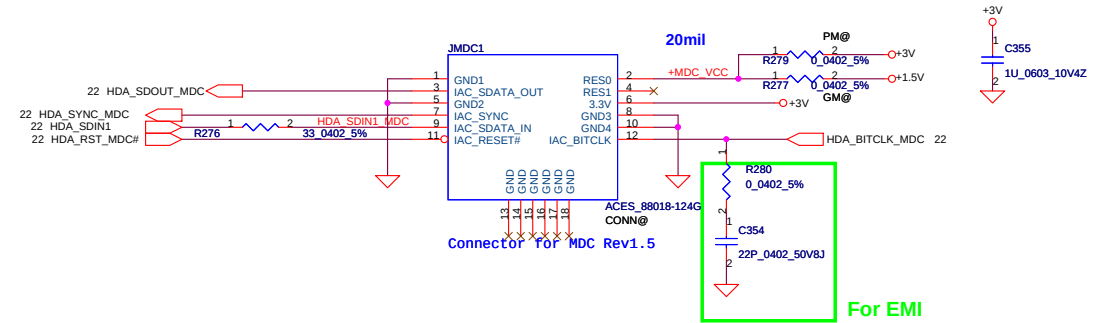
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				401552
				Rev C
				Friday May 16 2008
				Sheet 32 of 50

Power Button

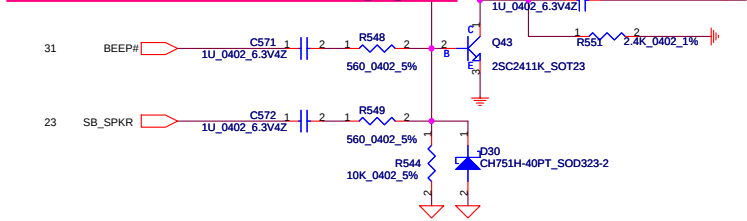
ON/OFF switch



HDA MDC Conn.

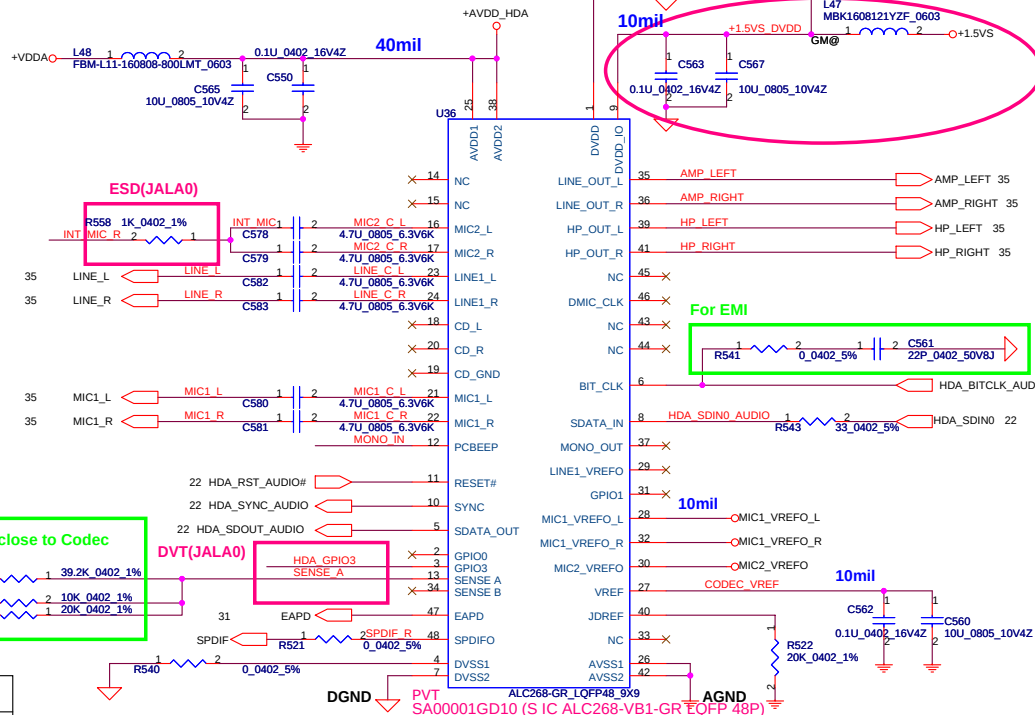


Cardbus usage for JALA0



BOM Option	
ALC268	268@
ALC888S-VB	888VB@
ALC888S-VC	888VC@

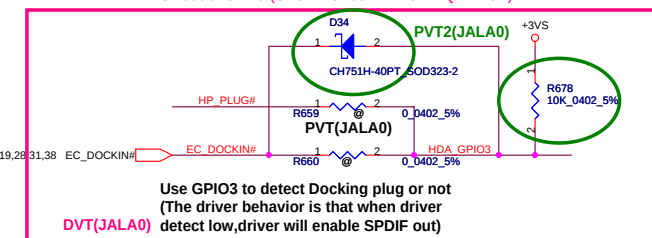
HD Audio Codec



Place close to Codec

DVT(JALA0)

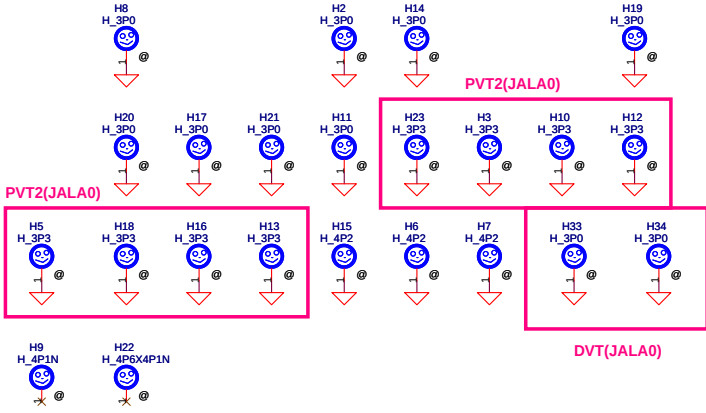
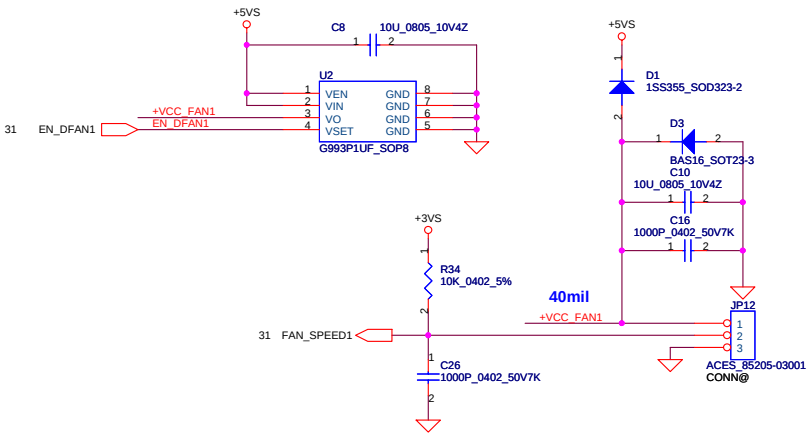
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



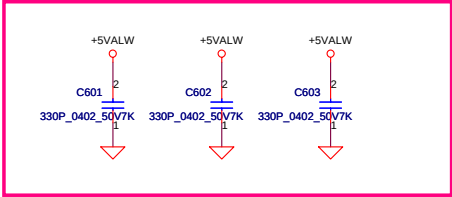
Use GPIO3 to detect Docking plug or not
(The driver behavior is that when driver detect low, driver will enable SPDIF out)

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Issued Date	2007/09/20	Deciphered Date	2008/09/20	SCHEMATIC MB A4221	
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				401552	
				Friday, May 16, 2008	Sheet 34 of 50

FAN1 Conn



EMI



ADD DVT(JALA0)

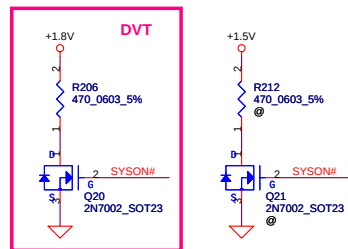
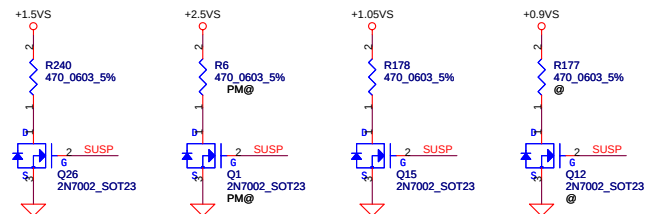
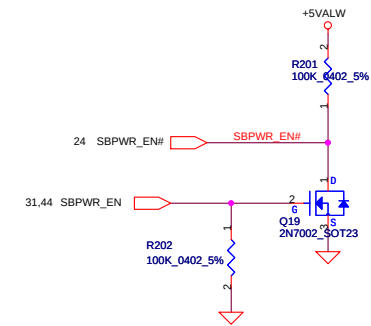
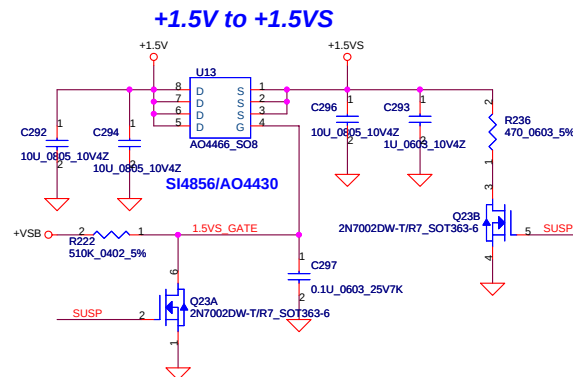
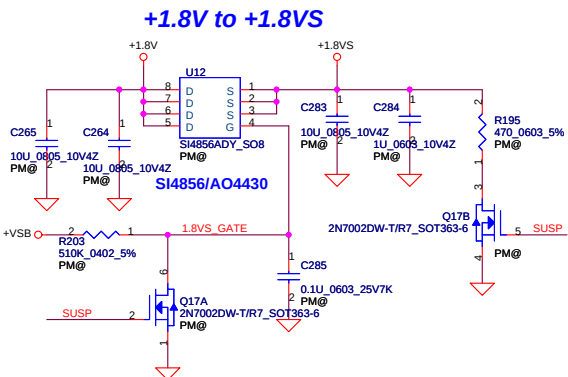
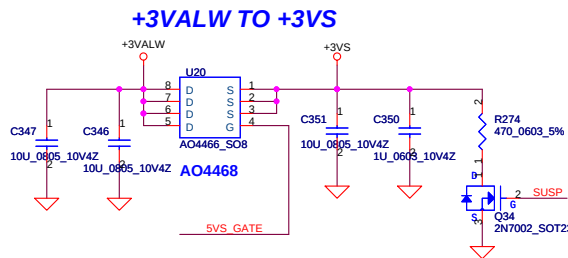
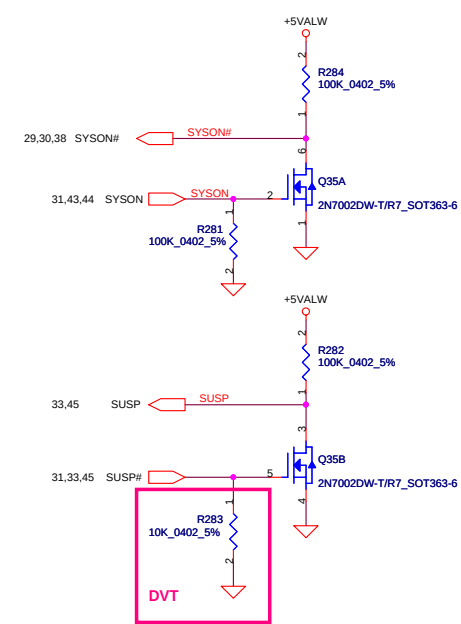
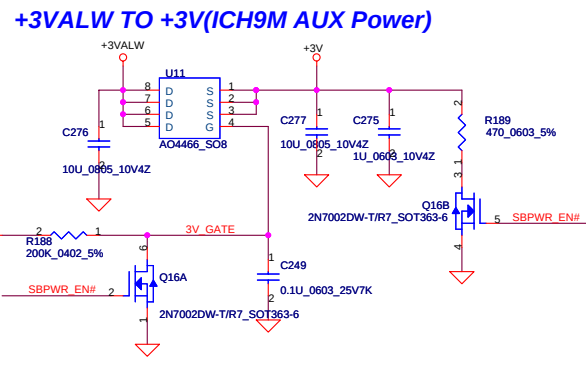
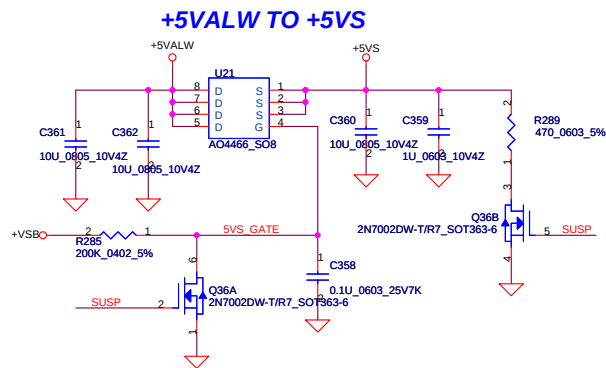
EMI



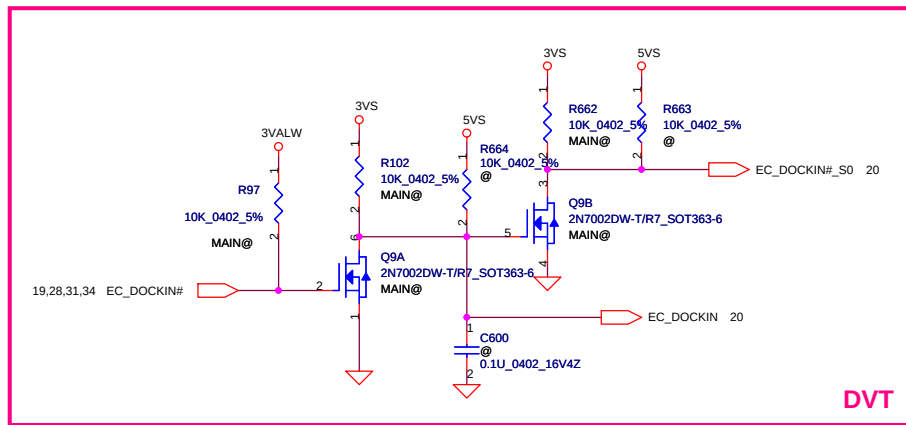
ADD PVT(JALA0)



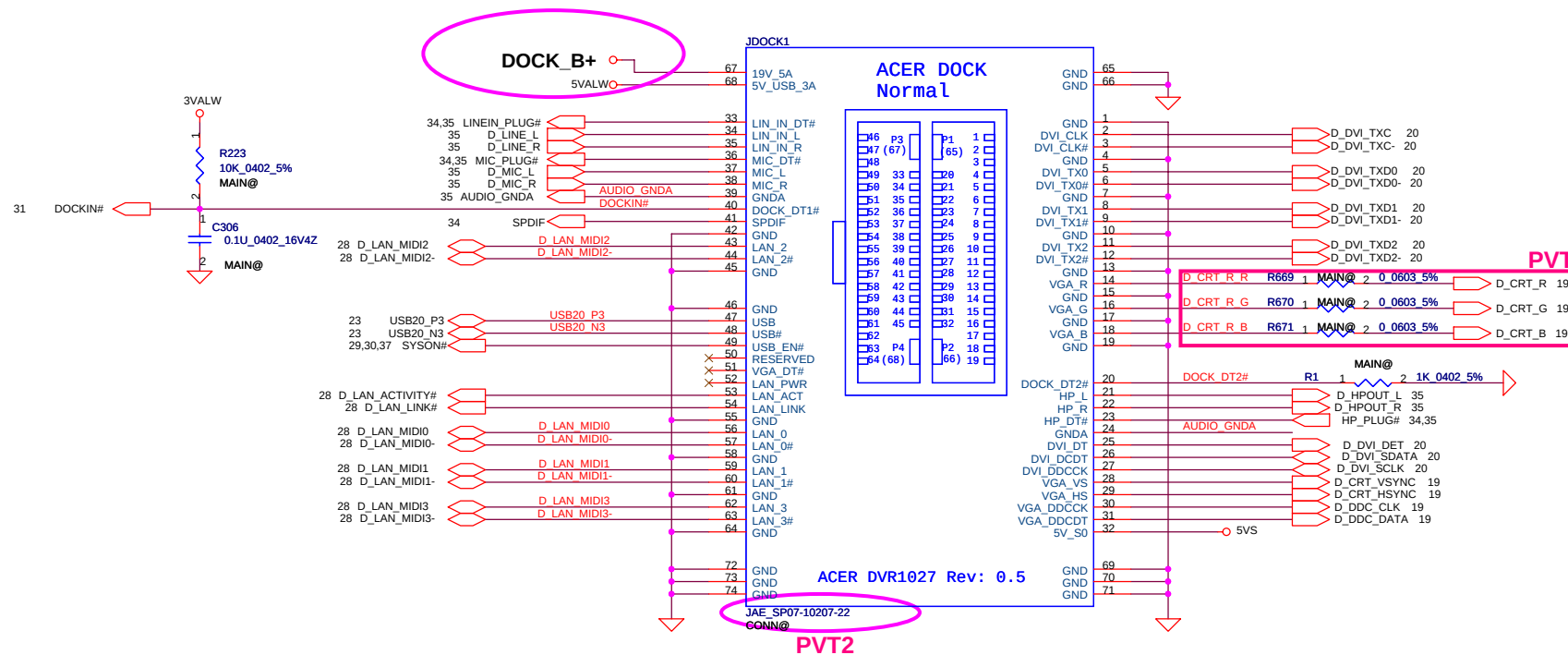
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				Date	Friday May 16 2008	Sheet 36 of 50



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Issued Date		2007/09/20		Deciphered Date		2008/09/20		Title		SCHEMATIC MB A4221			
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								A		401552			
								B					
								Date		Friday, May 16, 2008		Sheet 37 of 50	

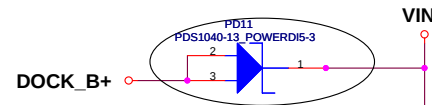


10/15 Acer DVR 1028 Rev0.3

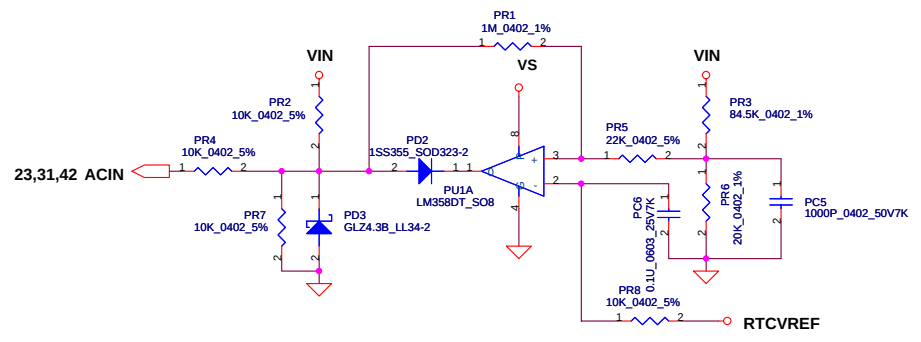
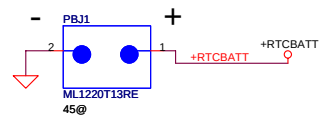
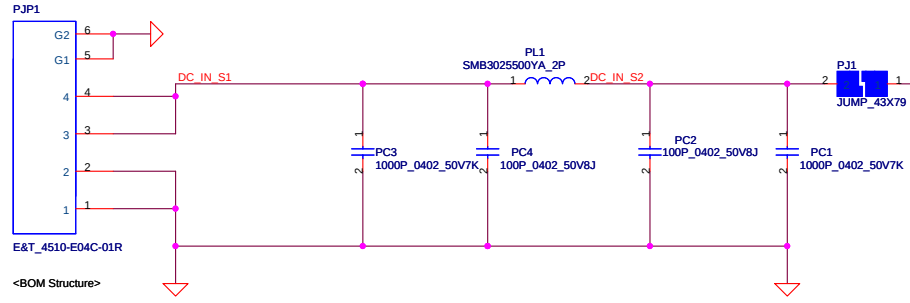


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				Date	Friday, May 16, 2008
				Sheet	38 of 50

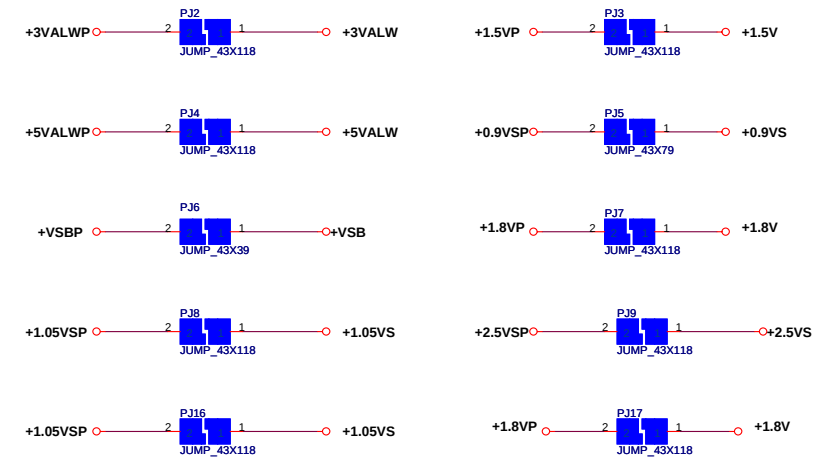
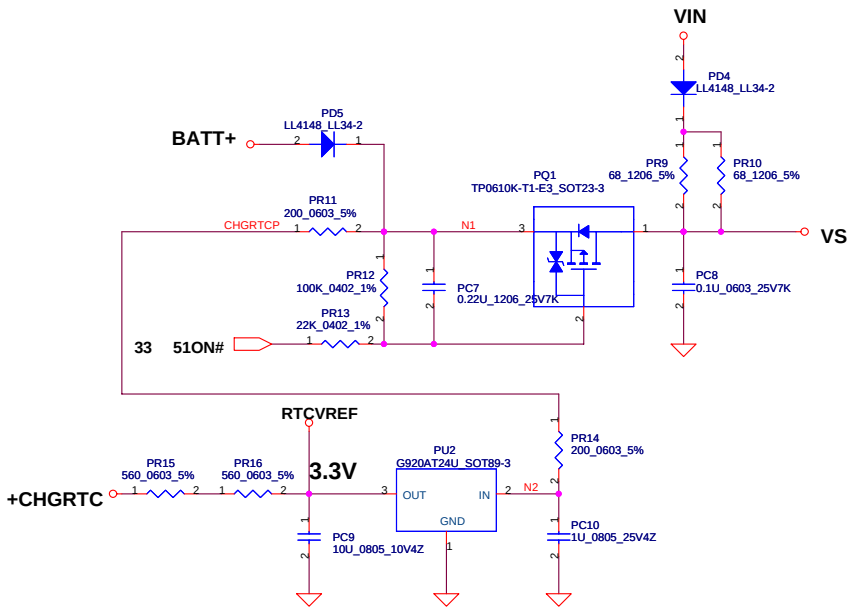
Place at HW side



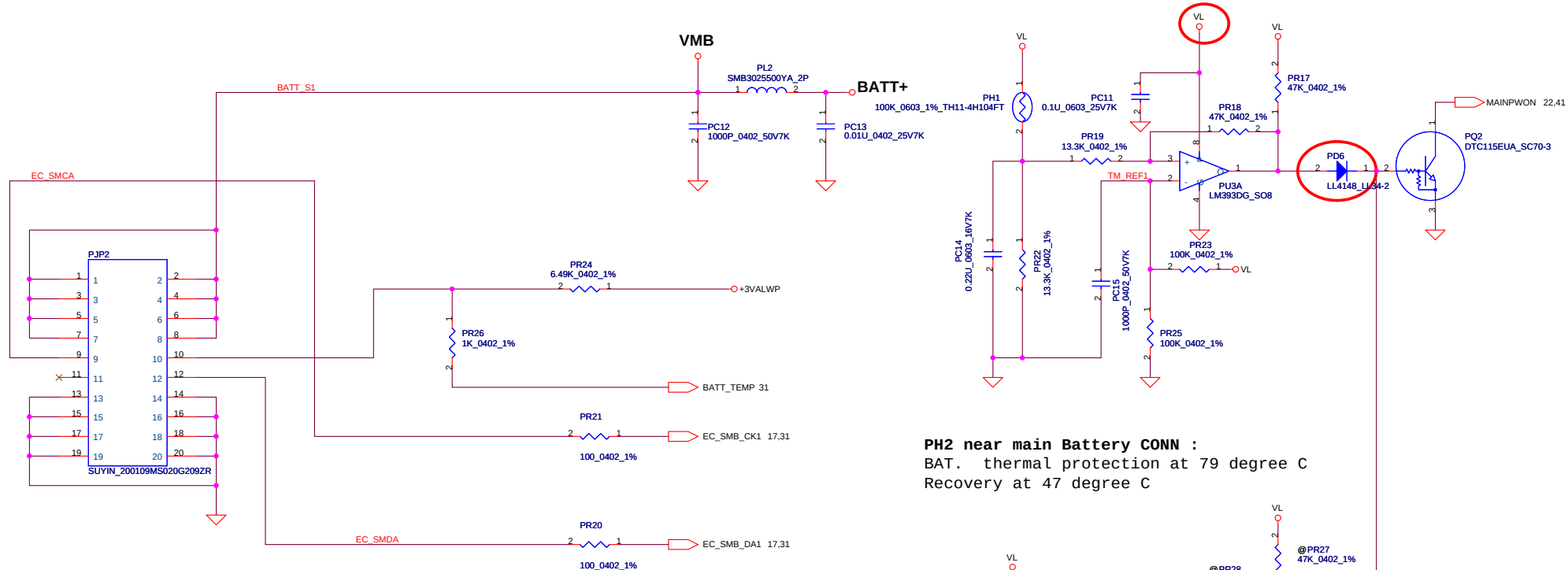
SP02000EF00



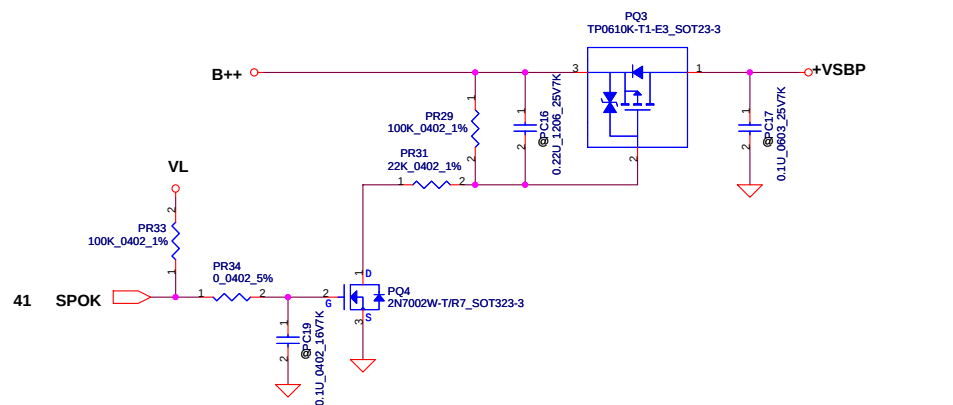
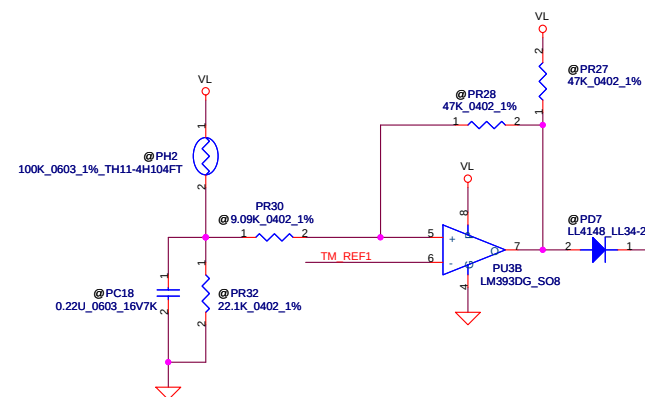
Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



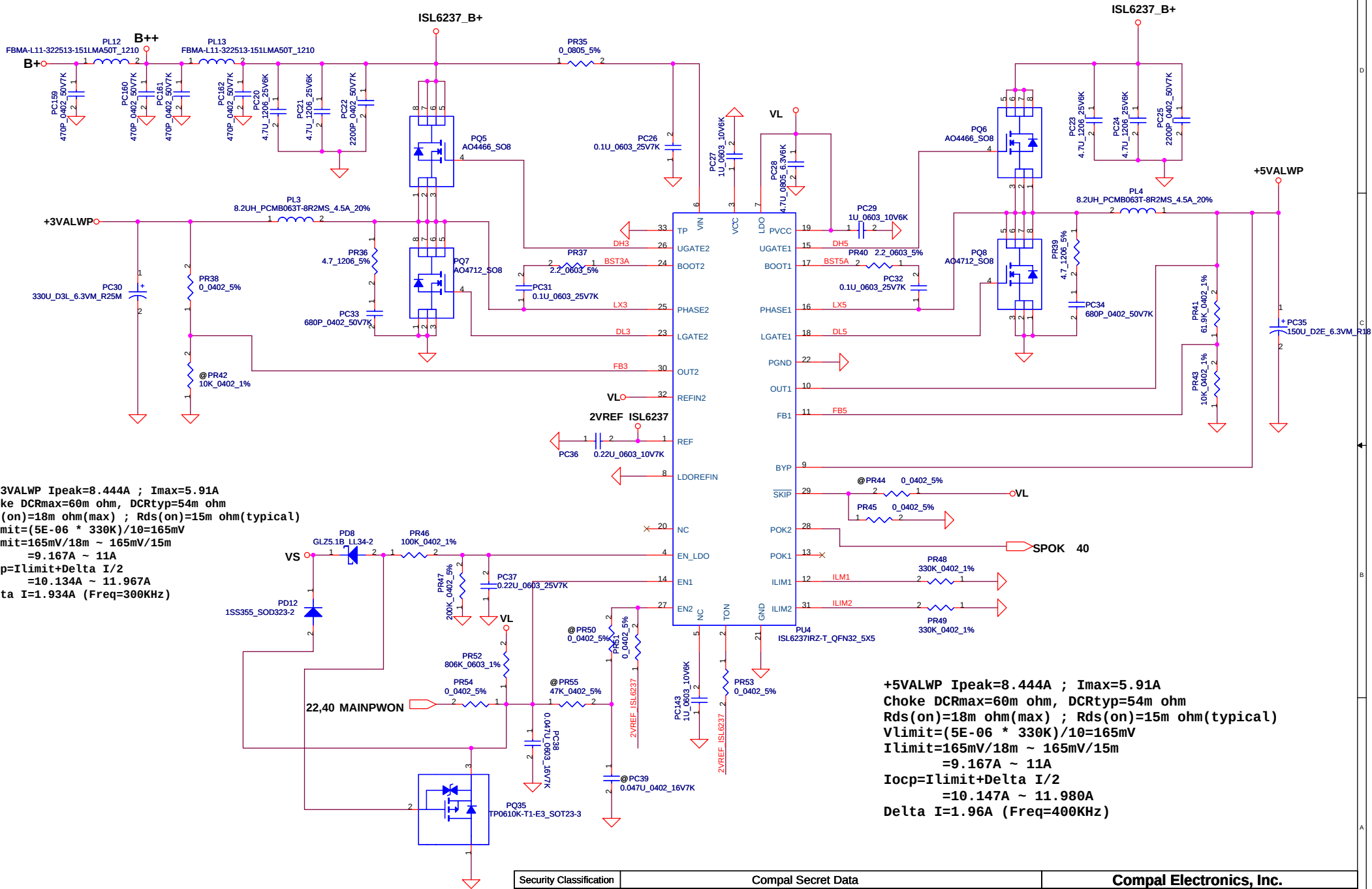
PH1 under CPU botten side :
CPU thermal protection at 96 degree C
Recovery at 60 degree C



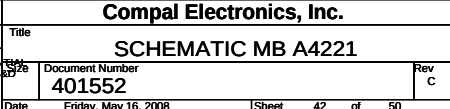
PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 47 degree C

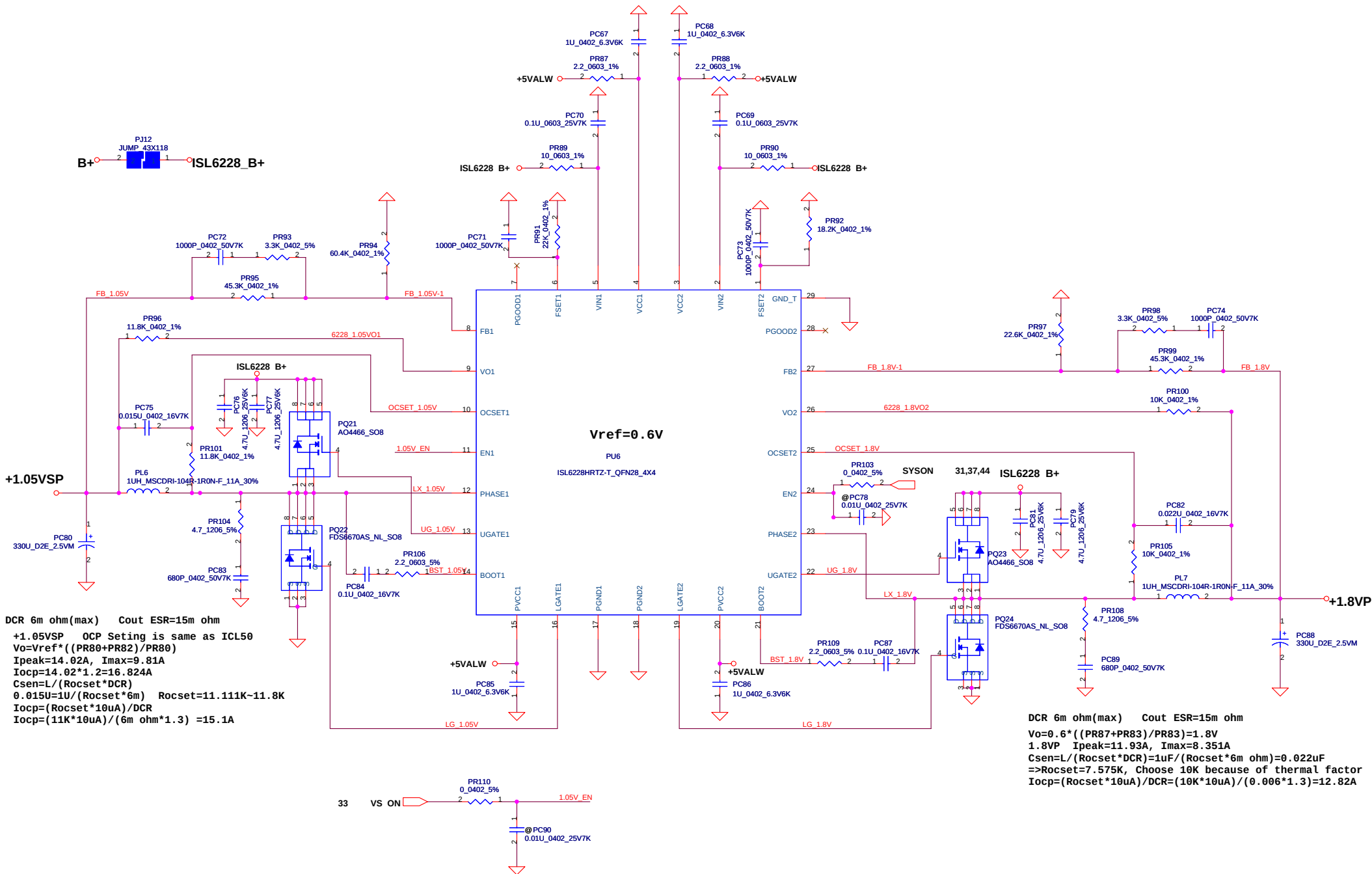


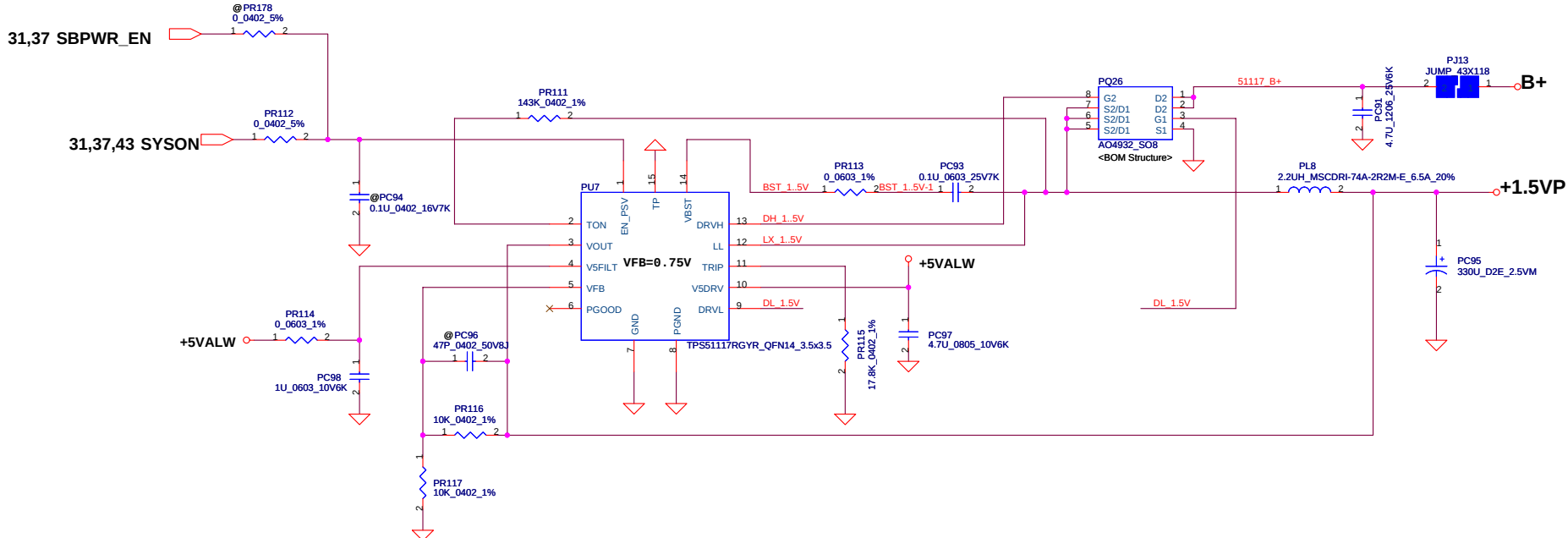
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				Date	Friday, May 16, 2008
				Sheet	40 of 50
				Rev	C



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				Document Number	Rev C
				Date	Friday, May 16, 2008
				Sheet	41 of 50



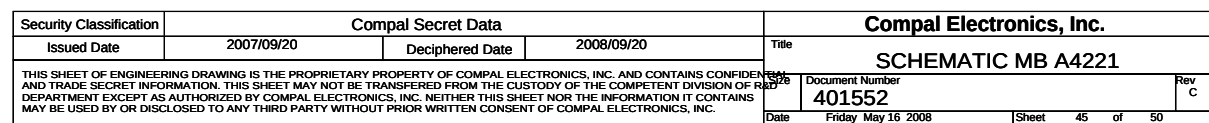




VFB=0.75V
 $V_o = VFB \cdot (1 + PR87 / PR88) = 0.75 \cdot (1 + 10K / 10K) = 1.5V$
 $Ton = 19 \cdot e^{-12 \cdot 143000 \cdot ((2/3) \cdot V_o + 100mV) / 19} + 50ns$
 $= 2.645e-7 \text{ us}$
 $\Rightarrow V_o / Vin = D = Ton / Ts \Rightarrow Ts = 3.35us$
 $Fsw = 298KHz$

$Cout \text{ ESR} = 15m \text{ ohm}$
 $I_{peak} = 4.71A, I_{max} = 3.297A, I_{ocp} = 5.652A$
 $\Delta I = ((19 - 1.5) \cdot (1.5 / 19)) / (L \cdot Fsw) = 2.107A$
 $\Rightarrow 1/2 \Delta I = 1.053A$
 $V_{trip} = R_{trip} \cdot I_{ocp} = 17.8K \cdot 10uA = 0.178V$
 $I_{ocpmin} = V_{trip} / R_{dsonmax} \cdot 1.2 + 1.053A$
 $= 0.178 / (0.027 \cdot 1.2) + 1.053 = 5.493A + 1.053A = 6.546A$
 $I_{ocpmax} = (0.178 / (0.021 \cdot 1.1)) + 1.053A = 7.705A + 1.053A$
 $= 8.758A$
 $I_{ocp} = 6.546A \sim 8.758A$

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				401552
				Rev C
				Date
				Friday May 16 2008
				Sheet 44 of 50



Version change list (P.I.R. List)

Page 1 of 2
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	Delete PD1.	Because we can cost down and DOCK_B+ has another one.	0.1	39	1 Delete PD1 SCSB540C080 (S SCH DIO B540C-13-F SMC)	20071108	EVT
2	3/5V exit on battery mode shutdown.	To prevent 3/5V exit on battery mode shutdown.	0.2	41	Add SC100001K00 (S DIO 1SS355 SOD323 T/R-5K	20071221	DVT
3	PD11 has over temp. issue.	Because PD11 has over temperature issue in JAQ60, we change it to a 10A diode.	0.2	39	Change PD11 from SCSB540C080 to SCS00002F00 .	20071221	DVT
4	Add snubber in 3/5V by EMI request.	Add snubber in 3/5V by EMI request.	0.2	41	Add PR36 and PR39 to SD001470B80	20071221	DVT
5	Down size.	Down size. by sourcer request.	0.2	46	Change PC136 from SE025821K80 to SE000003W00	20071221	DVT
6	Down size.	Down size. by sourcer request.	0.2	46	Change PC120 and PC129 from SE024681J80 to SE074681K80	20071221	DVT
7	Down size.	Down size. by sourcer request.	0.2	43	Change PC72 and PC74 from SE068102J80 to SE074102K80	20071221	DVT
8	2nd source trial run TI controller.	2nd source trial run TI controller.	0.2	41	Add PC143 SE080105K80	20071221	DVT
9	Add snubber in 3/5V by EMI request.	Add snubber in 3/5V by EMI request.	0.2	41	Add PC33 and PC34 SE074681K80	20071221	DVT
10	To meet Jeta SPEC.	To meet Jeta SPEC.	0.2	42	Add PC144 SE074102K80	20071221	DVT
12	Add EMI solution.	Add 3/5V boost resistor.	0.3	41	Add PR37, PR40 SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	20080102	DVT
13	Add EMI solution.	Add charger boost resistor.	0.3	42	Add PR61 SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	20080102	DVT
14	Add EMI solution.	Add charger snubber.	0.3	42	Add PR64 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC55 SE074681K80(S CER CAP 680P 50V K X7R 0402)	20080102	DVT
15	Add EMI solution.	Add 1.05V/1.8V boost resistor.	0.3	43	Add PR106, PR109 SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	20080102	DVT
16	Add EMI solution.	Add 1.05V snubber.	0.3	43	Add PR104 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC83 SE074681K80(S CER CAP 680P 50V K X7R 0402)	20080102	DVT
17	Add EMI solution.	Add 1.8V snubber.	0.3	43	Add PR108 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC89 SE074681K80(S CER CAP 680P 50V K X7R 0402)	20080102	DVT
18	Add EMI solution.	Add CPU boost resistor.	0.3	46	Add PR138, PR152 SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	20080102	DVT
19	Add EMI solution.	Add 3/5V input capacitor filter..	0.3	41	Add PC159, PC160, PC161, PC162 SE074471K80(S CER CAP 470P 50V K X7R 0402)	20080102	DVT
20	Add EMI solution.	Add 3/5V input beat	0.3	41	Add PL12, PL13 SM010016410(S SUPPRE KC FBMA-L11-322513-151LMA50T)	20080102	DVT
21							
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				Date	Friday, May 16, 2008
				Sheet	47 of 50

PHASE		PAGE	MODIFICATION LIST	PURPOSE
DVT	P.31		C286 change from 3.3U as 4.7U	Stable KB926 internal +1.8V regulator , ENE suggestion value
	P.32		JP6 pin define reverse	NA
	P.32		Change SW3 & SW4 type	NA
	P.32		U15 change from 1MB as 2MB capacity SPI ROM	Add Finger print code
	P.33		R261 change from 10K as 31.6K	Fix ATI MXM sku can't power on for battery mode issue
	P.33		C334 change from 0.1U as 1U	Fix nVIDIA MXM sku power on issue
	P.34		Delete Internal(Digital) MIC reserved circuit	NA
	P.34		Change R574 (0 ohm) as L59 (MBC1608121YZF)	For EMI
	P.34		Add R660 to connect HDA_GPI03 with DOCKIN#	For docking spdif feature enable
	P.34		Change R574 (0 ohm) as L59 (MBC1608121YZF)	For EMI
	P.35		R559 / R560 change from 47 ohm as 75 ohm	For Audio precision FS0V
	P.35		R561 / R562 / R566 / R571 change from 75 ohm as 1K ohm	For ESD , Realtek suggestion value
	P.36		Add C601 , C602 , C603 (330P) on +5VALW	For EMI
	P.37		R283 change from 100K to 10K	NA
	P.37		R206 , Q20 stuff	For +1.8V discharge
	P.38		Add switch to enable/disable EC_DOCKIN#_S0 for HDMI SMBUS	NA
	P.38		Update JDOCK1 footprint	NA
PVT1	P.16		Change C308 / C311 (33P) as 27P	For RTC accuracy
	P.23		Use 4MB SPI ROM	For Kinabalu_High & Kinabalu_Low
	P.23		Add test point T32 / T33 / T34 / T35	Reserved for PCIE(X1) port 1
	P.25		Change U35 as SA000026P10(OZ2210GN-B1)	For B1 version
	P.27		Change U23 as SA000025P20(BCM5764MKMLG P20)	For B0 version
	P.27		Reserved R673 , R674 (0 ohm)	For Lan SMBUS
	P.27		Reserved Lan GPI00(LAN_ALERT#) / LAN_ALERT#_EC / R675 , R676 , R677 to EC	For Lan ASF workaround
	P.27		U23 Pin17 / Pin5 / Pin55 connect to U23 Pin18 for power +Lan_VDDIO_1.2	U23 Pin18 is power source +Lan_VDDIO_1.2 for U23 Pin17 / Pin5 / Pin55
	P.27		U23 Pin38 / Pin52 NC	NA
	P.29		Change JMINI1 for Robson2 , chnage JMINI2 for Wireless	NA
	P.31		Add LAN_ALERT#_EC & EC_ACIN for EC	Reserved for ASF workrund & Nvidia MXM power saving
	P.33		Add R668(10K) & reserved R263(10K)	Fine tune +1.05VS timing for UMA boot display flash
	P.34		Change U36 as ALC268-VB1-GR(SA00001GD10)	Version upgrade
	P.34		Stuff R659 & un-stuff R660	For SPDIF feature on docking
	P.36		Add C604 , C605 (820P_0402)	For EMI
	P.50		Chipset change as GM(SA00002JT10) / PM(SA00002JJ00) / ICH9M(SA00002JH00)	Version upgrade
PVT2	P.27		Update U23 CIS symbol	U23 Pin38 , 52 can't be changed as NC
	P.34		Add D34 , R678	For ACER docking SPDIF feature (No SPDIF on board)
	P.38		Update JDOCK1 CIS symbol	Docking connector modify (add boss x 2) for DFX
	P.35		Delete D2 , D4 (Int SPK ESD diode)	NA
	P.34		Delete D9 (Int MIC ESD diode)	NA
	P.35		Add C609 , C610 (330P_0603) on Right SPK	For EMI
	P.34		Add C608 (330P_0603) on Int MIC	For EMI
	P.08		Add Test point (T39 , T40 , T41 , T42)	Add Management Engine JTAG pins
	P.27		Add C612 , C614 (0.1u_0402) for +LAN_AVDD	For lower 1000Base-T Comm-Mode O/P Voltage < 50mV
	P.27		Add C615 , C616 , C617 (0.1u_0402) for +LAN_AVDDL	For lower 1000Base-T Comm-Mode O/P Voltage < 50mV
	P.08		Add U41, R679 , R680 , R681 , R682 , R683 , R684 , R685 , T43	Reserved for Management Engine JTAG debug
	P.07		Chipset change as GM(SA00002JT50) / PM(SA00002JJ50)	Version upgrade
	P.20 , P.31		Add EC_DVI_DET , EC_GPI0B , EC_GPI0C , R687 , R688 , R691	Reserved for DVI detect delay control (by EC)
MP	P.24		R73 , R148 change from 10_0402 to 100_0402 C128 , C204 change from 0.1U_0402 to 1U_0402	For USB issue on ICH9M A3 stepping
	P.34 , P.35		C608 , C609 , C610 change from 330P_0603 to 330P_0402	For 330P_0402 is standard part
	P.31		Change R248 as 33K	Board ID upgrade
	P.30		Add R692 / R693 (0_0603)	Reserved S3 power rail for check finger print sensor S3 resume too slow
			Security Classification	Compal Secret Data
			Issued Date	2007/09/20
			Deciphered Date	2008/09/20
			Title	
			Compal Electronics, Inc.	
			SCHEMATIC MB A4221	
			Document Number	
			401552	
			Date	
			Friday, May 16, 2008	
			Sheet	
			49 of 50	

PHASE	PAGE	MODIFICATION LIST	PURPOSE
P.20		Add D35	Reserved for HDMI_HPD
P.30		Add R694 / R695 (0_0603)	Reserved for check
P.27		Delete C612 , C614 , C615 , C616 , C617 (0.1u_0402)	No need
P.16		Stuff R689 / R690	Reserved for LAN power saving
P.35		R559 , R560 change from 75 to 54.9 ohm	For FSOV between 420mv~480mv
		Chipset change as GM(SA00002JTB0) / PM(SA00002JJA0) / ICH9M(SA00002JH70)	Version upgrade
P.32		R291 , R294 change from 300_0402_5% to 150_0402_5%	For ACER Hank's request to fine tune brighter
P.20		R84 , R85 , R86 , R91 change from 2K_0402_5% to 4.7K_0402_5%	For UMA DVI/HDMI monitor P193WA (x) detect issue (On JAL90)

PCB



PCB 047 LA-4221P REV1 M/B

LA4221MB Rev0: DA600007R00
LA4221MB Rev1: DA600007R10
LA4221MB with Sub/B Rev1: DAZ04800100

IC



CANTIGA ES_FCBGA1329

DVT CANTIGA PM: SA00001ZO30 (S IC EB88CTPM QR34 B0 FCBGA 1329 ES)
PVT CANTIGA PM: SA00002JJ00 (S IC AC88CTPM QT78 B2 FCBGA 1329 PM)
PVT2 CANTIGA PM: SA00002JJ50 (S IC AC88CTPM QU38 B3 FCBGA 1329 PM)
Pre-MP CANTIGA PM: SA00002JJA0 (S IC AC82PM45 SLB97 B3 FCBGA1329 PM ABO!)



CANTIGA ES_FCBGA1329

DVT(Check_TBD) CANTIGA GL: SA000023Z00 (S IC CANTIGA ES FCBGA 1329 MCH GL)

DC Cable



DC Cable (65W)
@ PVT(54 Rank)

DC301003R00(CONN SET 048 DCJACK-MB 2DW-G756-I50 65W)



DC Cable (90W)
@ PVT(54 Rank)

DC301003S00(CONN SET 048 DCJACK-MB 2DW-G756-I49 90W)



ICH9-M ES_FCBGA676

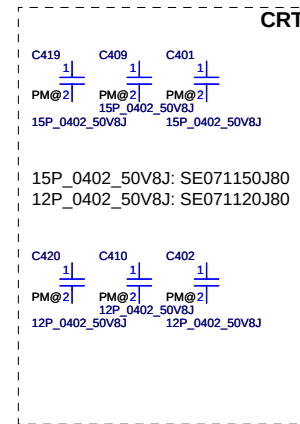
ICH9-M: SA00002G120
(S IC AF82801IEM QT10 A3 PBGA 676P ICH9M)



W25X16-VSSIG_S08

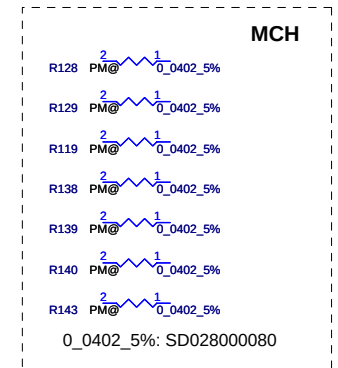
MP Winbond: SA00001KN00
(S IC FL 16MBIT W25X16-VSSIG SOIC 8P)

For Discrete



DVT(Check)

CRT



MCH

0_0402_5%: SD028000080

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					401552
				Date	Friday, May 16, 2008
				Sheet	50 of 50
				Rev	C