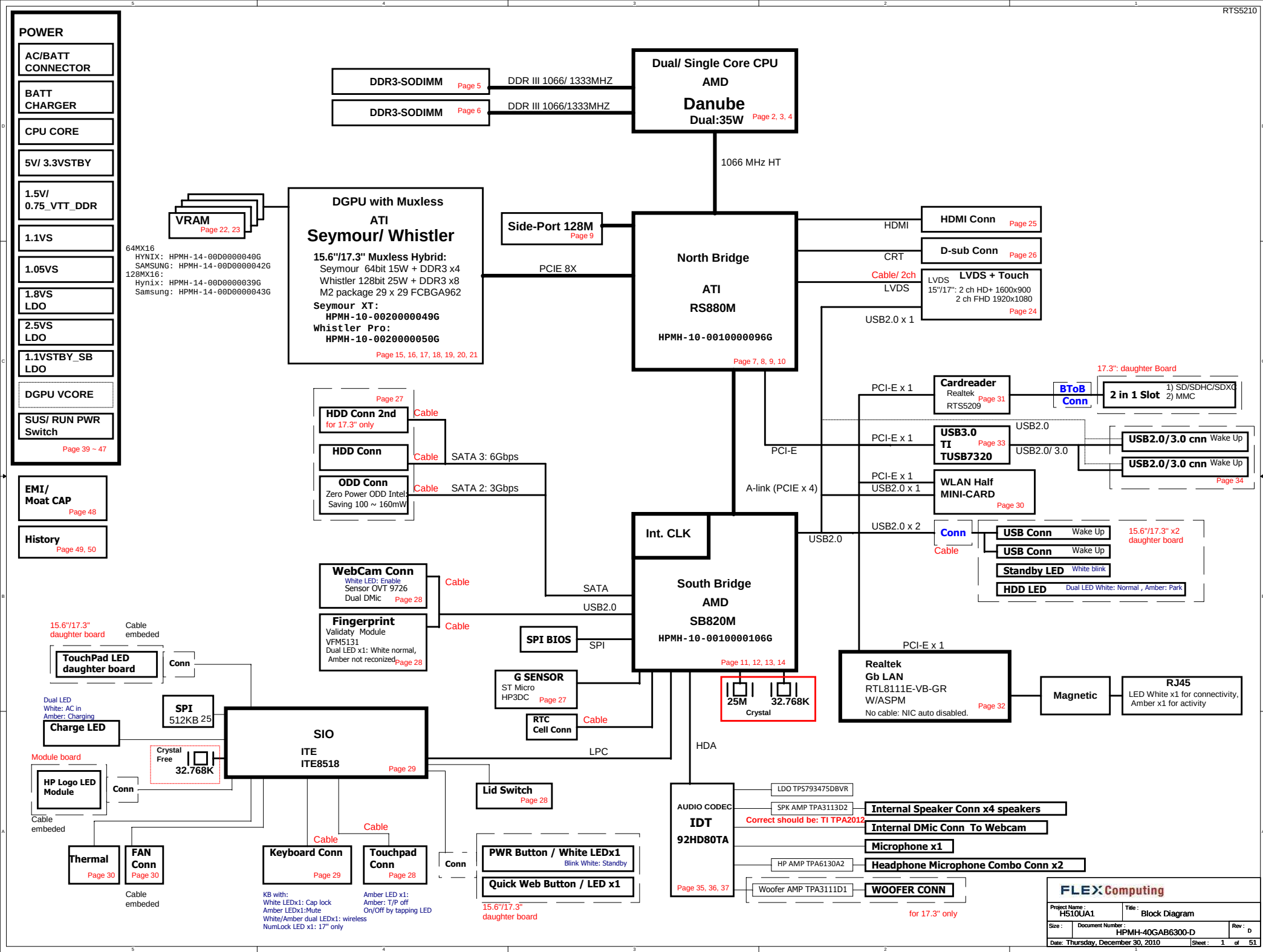
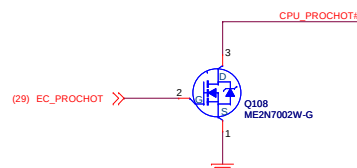
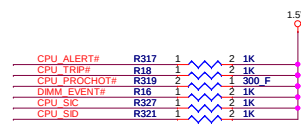


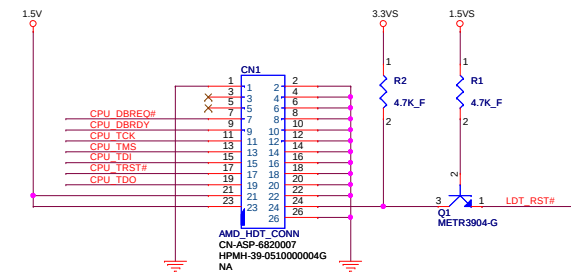


AMD Debug Termination

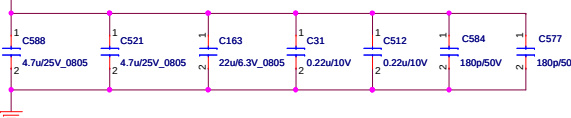
Signal Name	Type	Connection	Termination	Voltage
TEST6 TEST7 TEST8		Remain unconnected	-	
TEST9	I	Tie to VSS	-	VSS
TEST10		S1g2: Leave unconnected	-	
		S1g3: Pulled up to VLDT (0603 DNI)	-	
TEST12		Test point access required for scan function. Connection to scan header preferred but not required.	1 K Ω to VSS No pop	VSS
TEST14 TEST15 TEST16 TEST17		Test point access required, header is preferred	-	-
TEST18			1 K Ω to VSS No pop	VSS
TEST19			1 K Ω to VSS No pop	VSS
TEST20		Test point access required for scan function. Connection to scan header preferred but not required.	300 Ω^6	VSS
TEST21			300 Ω^6	VSS
TEST22			1 K Ω to VSS No pop	VSS
TEST23			300 Ω^6	VSS
TEST24	I	Test point access required for scan function. Connection to scan header preferred but not required.	300 Ω^6	VSS
TEST25_H			510 Ω^6	VSS
TEST25_L			510 Ω^6	VDDIO
TEST27 TEST28_H TEST28_L TEST29_H TEST29_L		Need test point on board	-	-



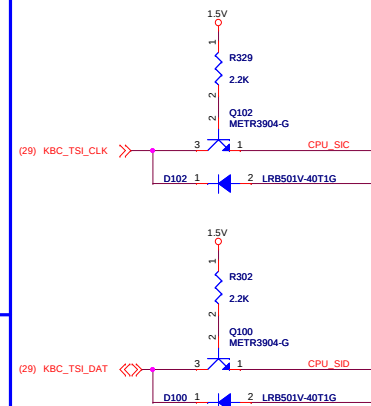
HDT Header



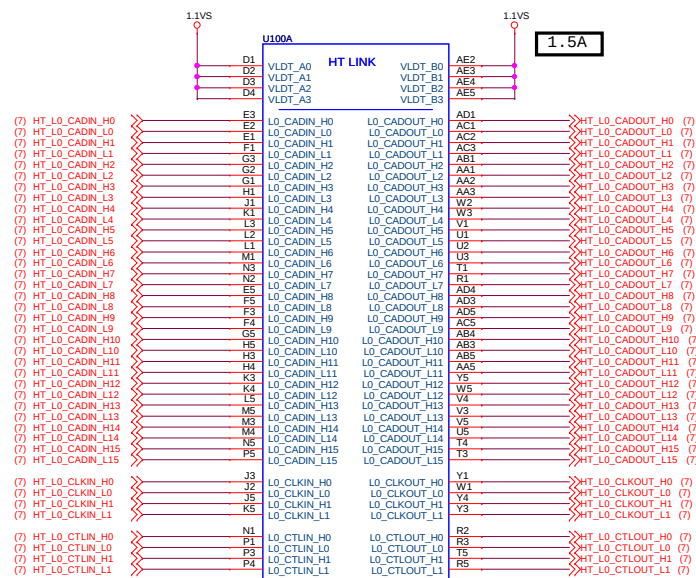
Place close to socket



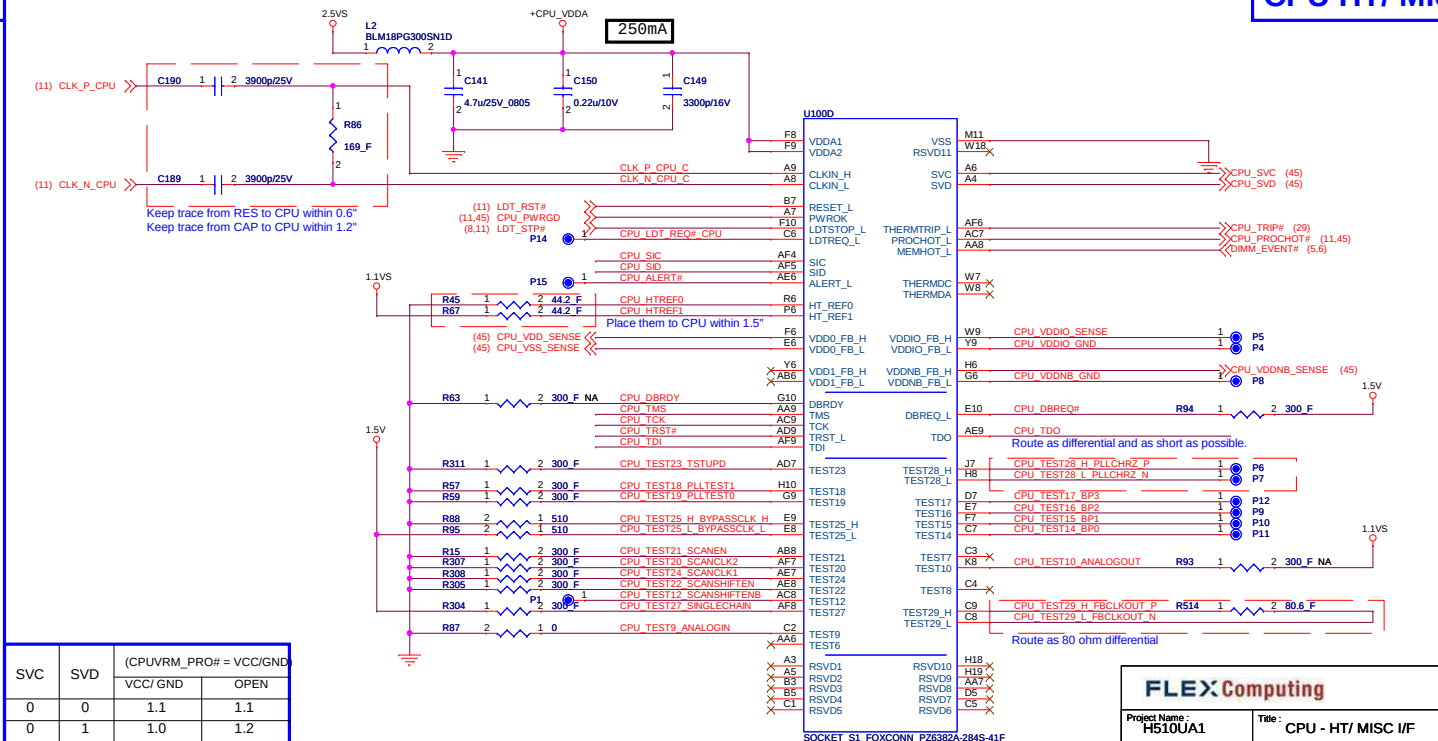
TSI Function



CPU HT/ MISC



SOCKET_S1_FOXCNN_P26382A-284S-41F



SVC	SVD	(CPUVRM_PRO# = VCC/GND)	VCC/ GND	OPEN
0	0	1.1	1.1	
0	1	1.0	1.2	
1	0	0.9	1.0	
1	1	0.8	0.8	

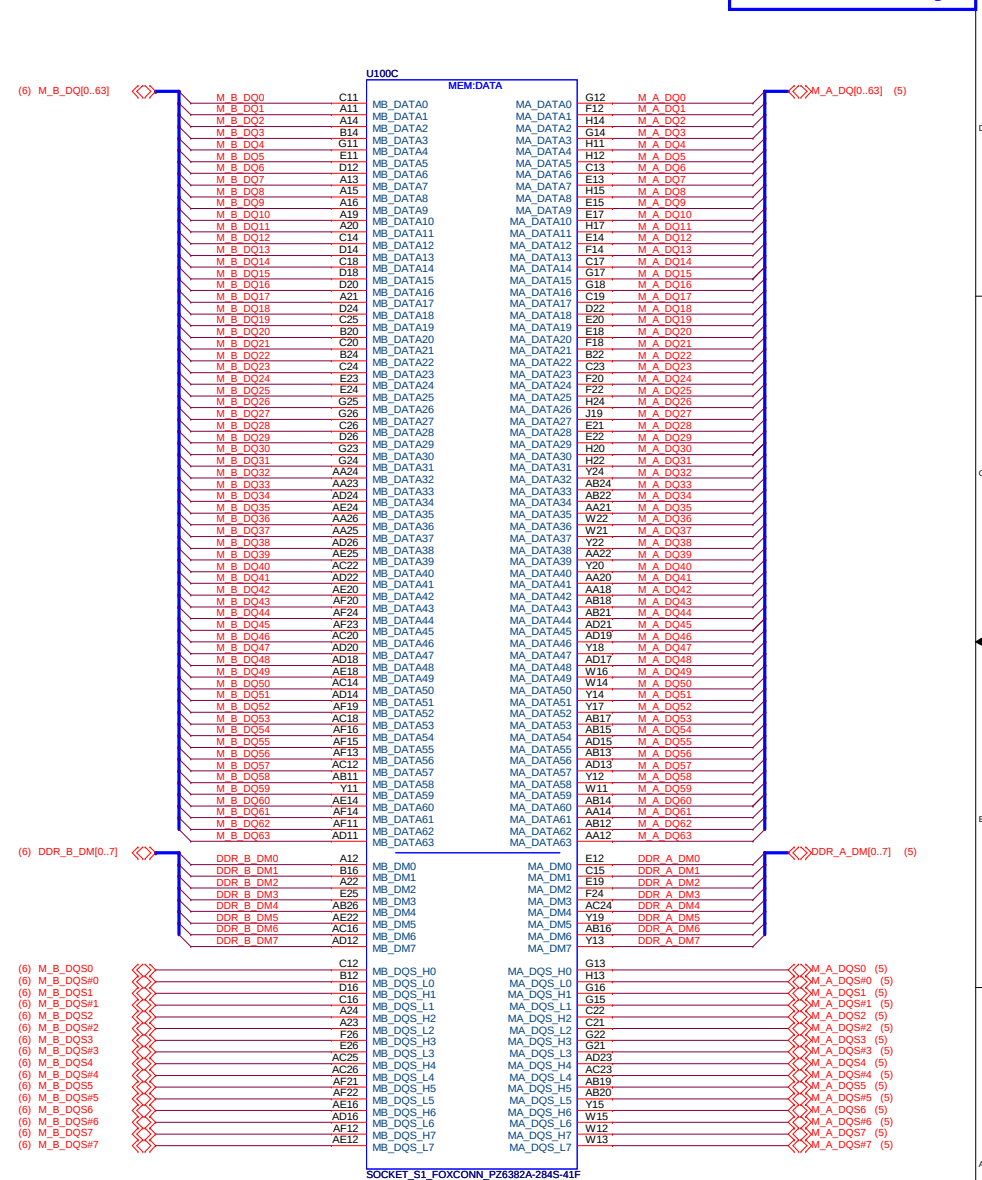
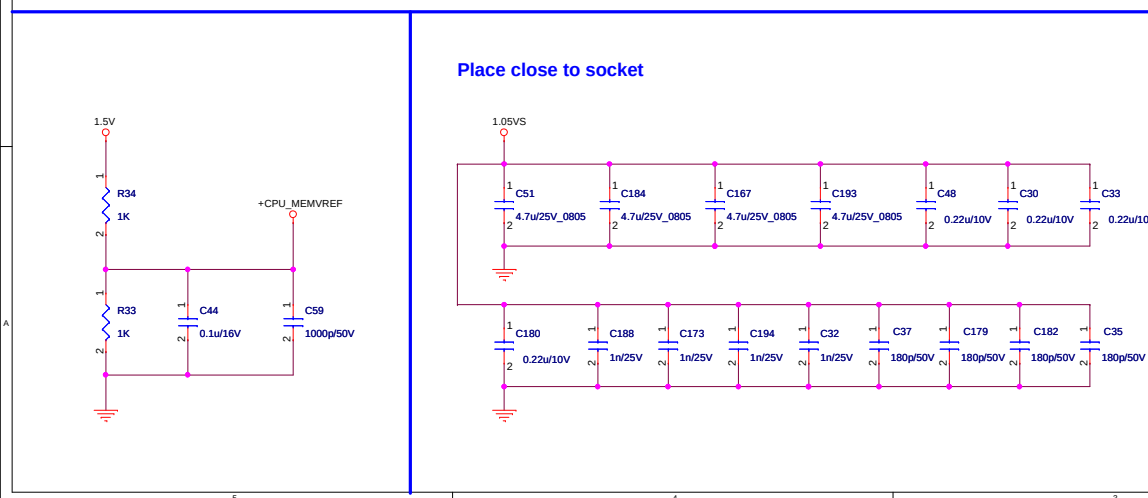
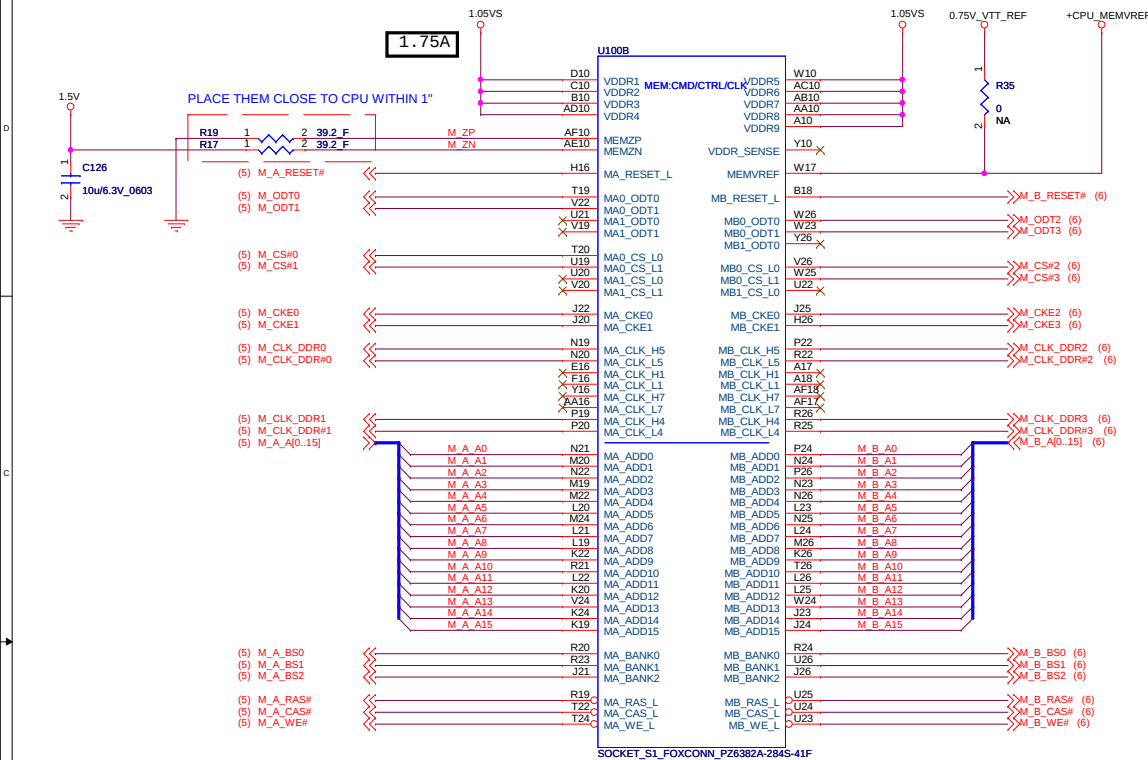
FLEX Computing

Project Name: H510UA1 Title: CPU - HT/ MISC I/F

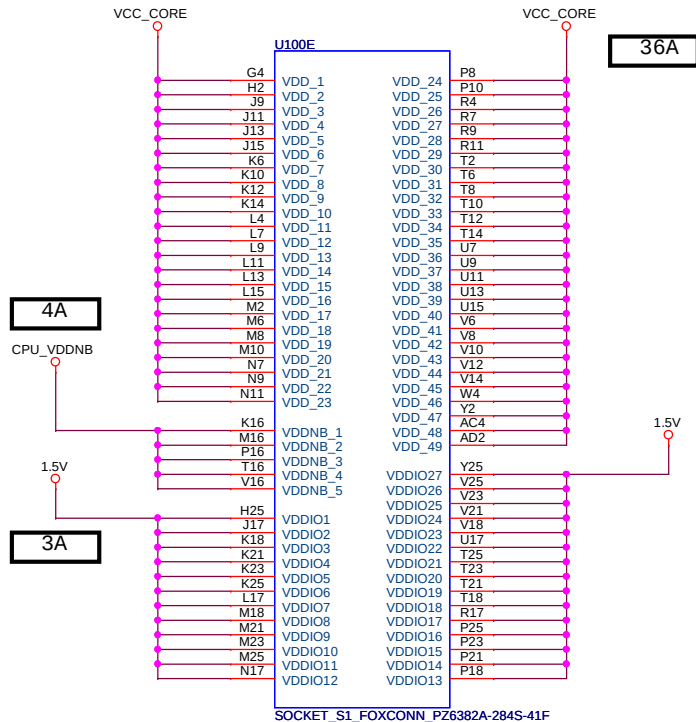
Size: Document Number: HPMH-40GAB6300-D Rev: D

Date: Thursday, December 30, 2010 Sheet: 2 of 51

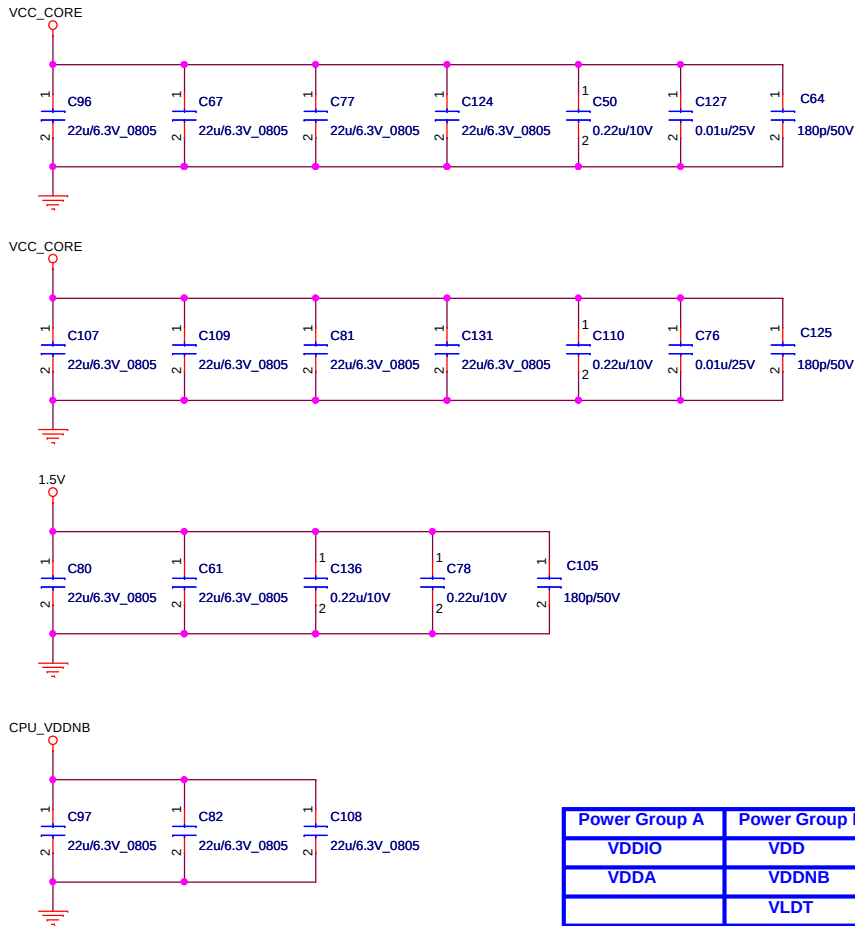
CPU Memory



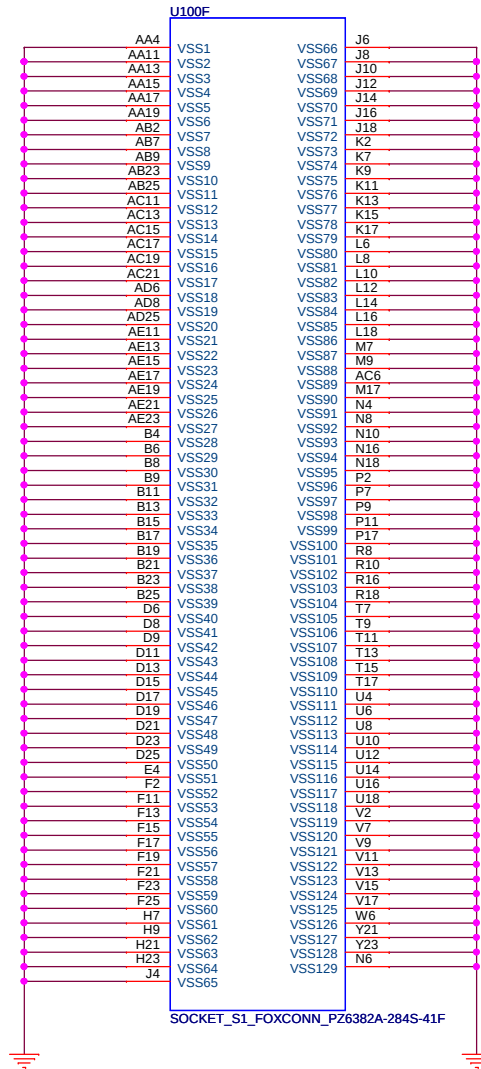
CPU PWR



BOTTOM SIDE DECOUPLING

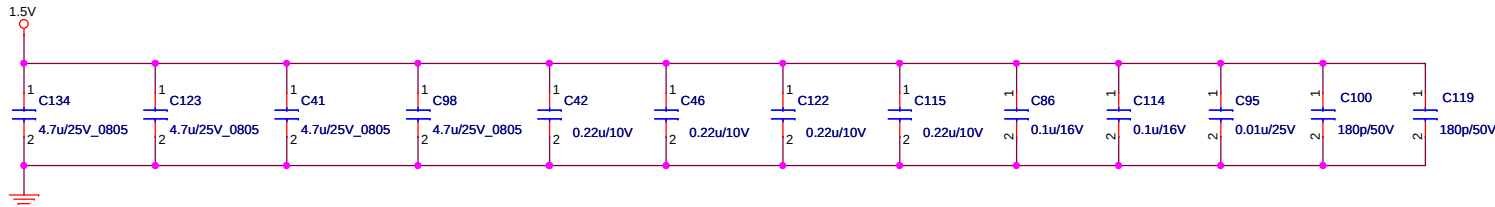


CPU GND



DECOUPLING BETWEEN PROCESSOR AND DIMMs

PLACE CLOSE TO PROCESSOR AS POSSIBLE

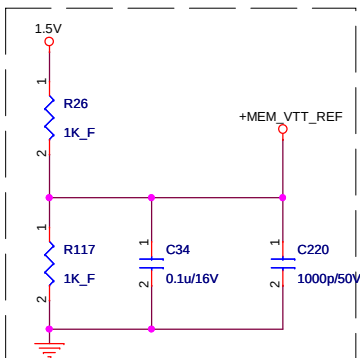
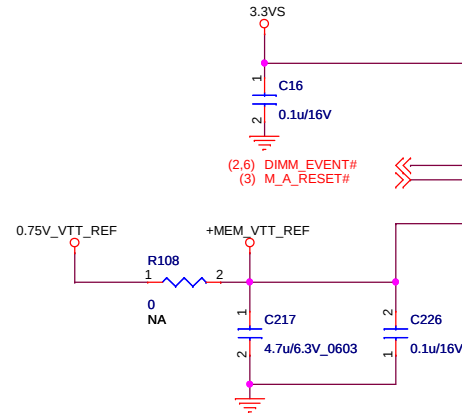
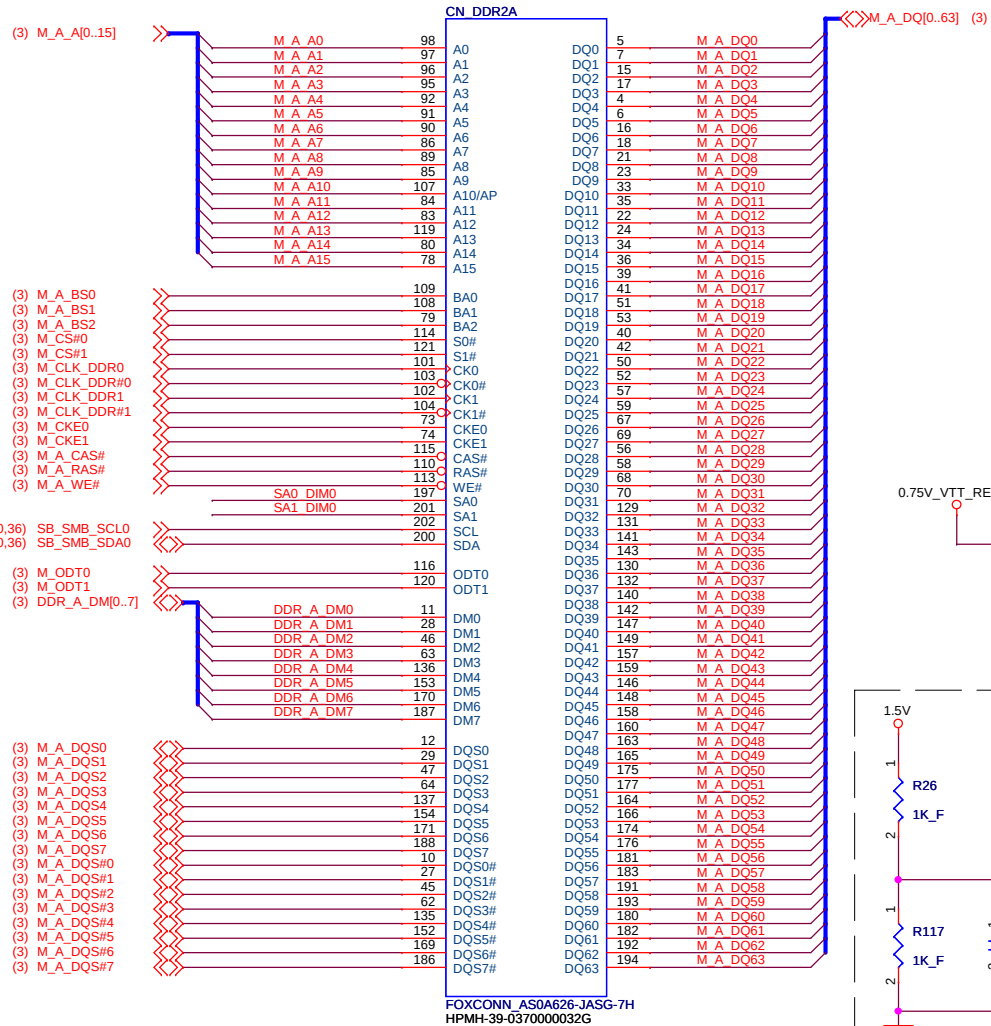


Power Group A	Power Group B
VDDIO	VDD
VDDA	VDDNB
	VLDT
	VDDR

FLEXComputing

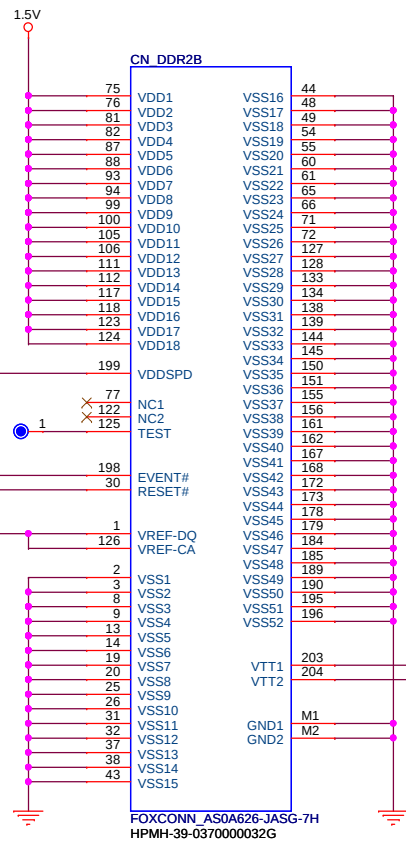
Project Name : H510UA1	Title : CPU - PWR/ GND
Size : Document Number : HPMH-40GAB6300-D	Rev : D
Date : Thursday, December 30, 2010	Sheet : 4 of 51

MEM CH-A



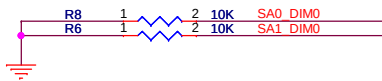
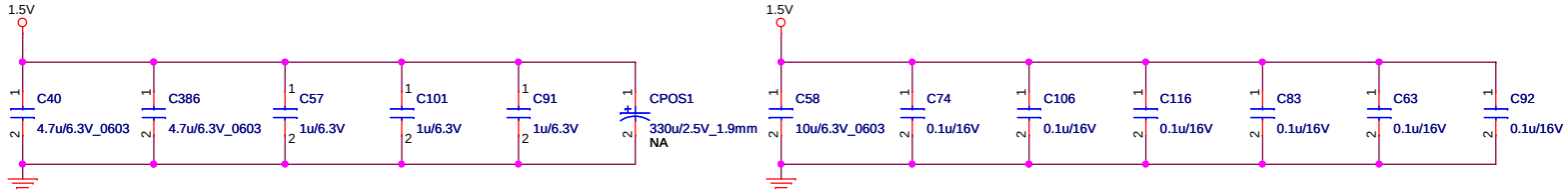
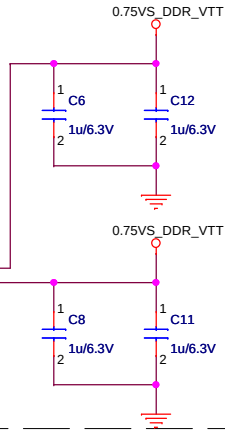
Layout

0.1uF Caps for CMD,CLK,CTRL return path
Place Caps on the same side as SO-DIMM
and close to VDD Pin .



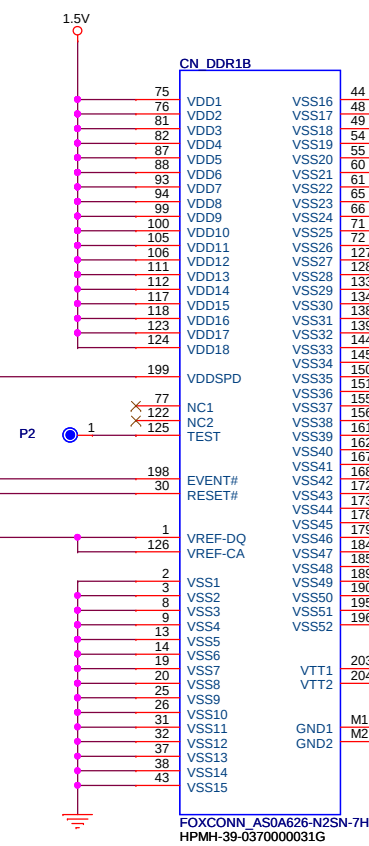
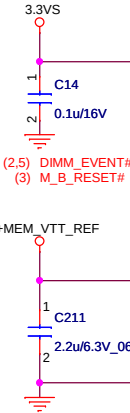
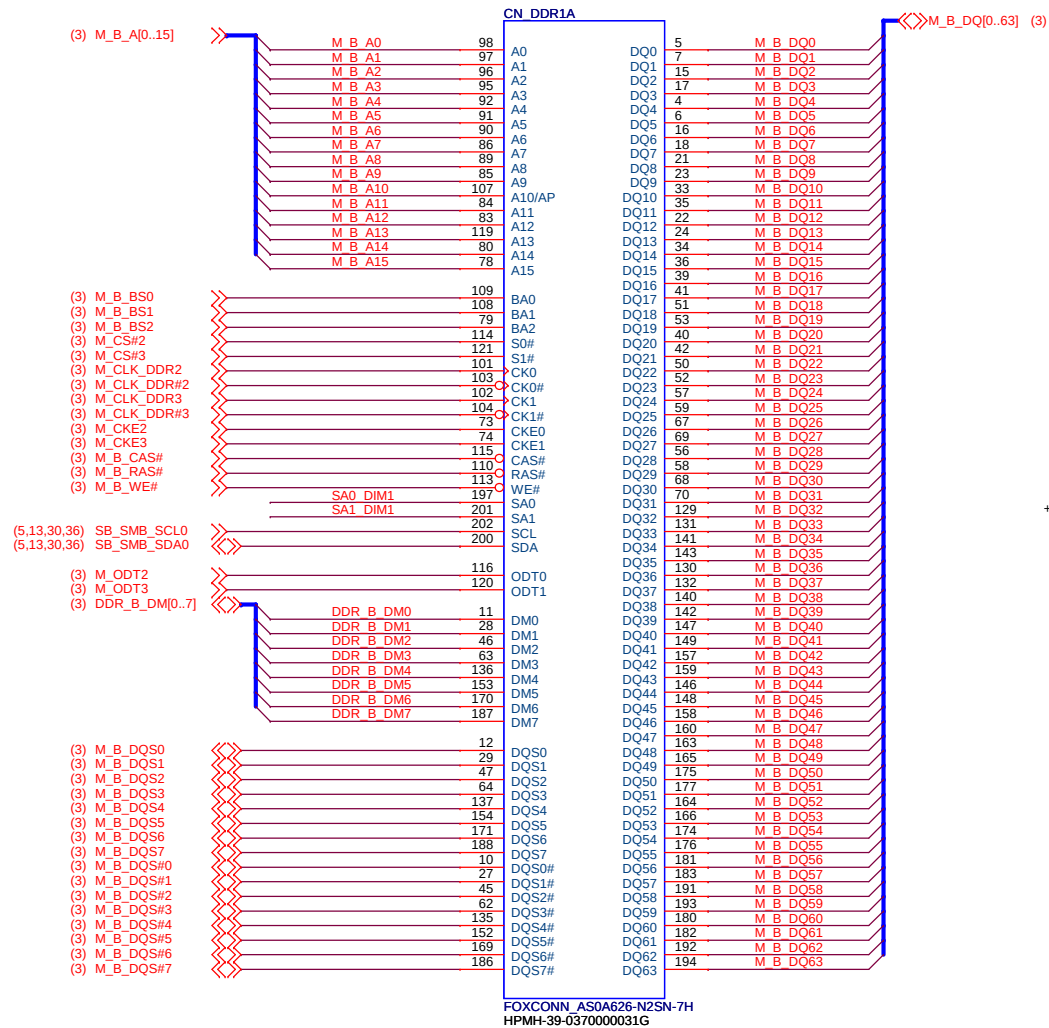
Layout

Place these caps close to Pin203 and 204.

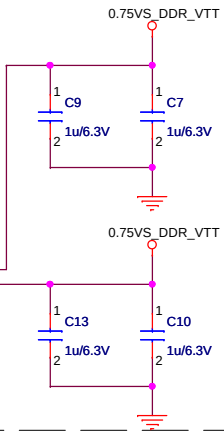


FLEX Computing

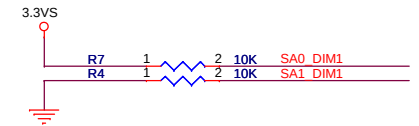
Project Name : H510UA1	Title : SO-DIMM Channel - A
Size : Document Number : HPMH-40GAB6300-D	Rev : D
Date : Thursday, December 30, 2010	Sheet : 5 of 51

**Layout**

Place these caps close to Pin203 and 204.

**Layout**

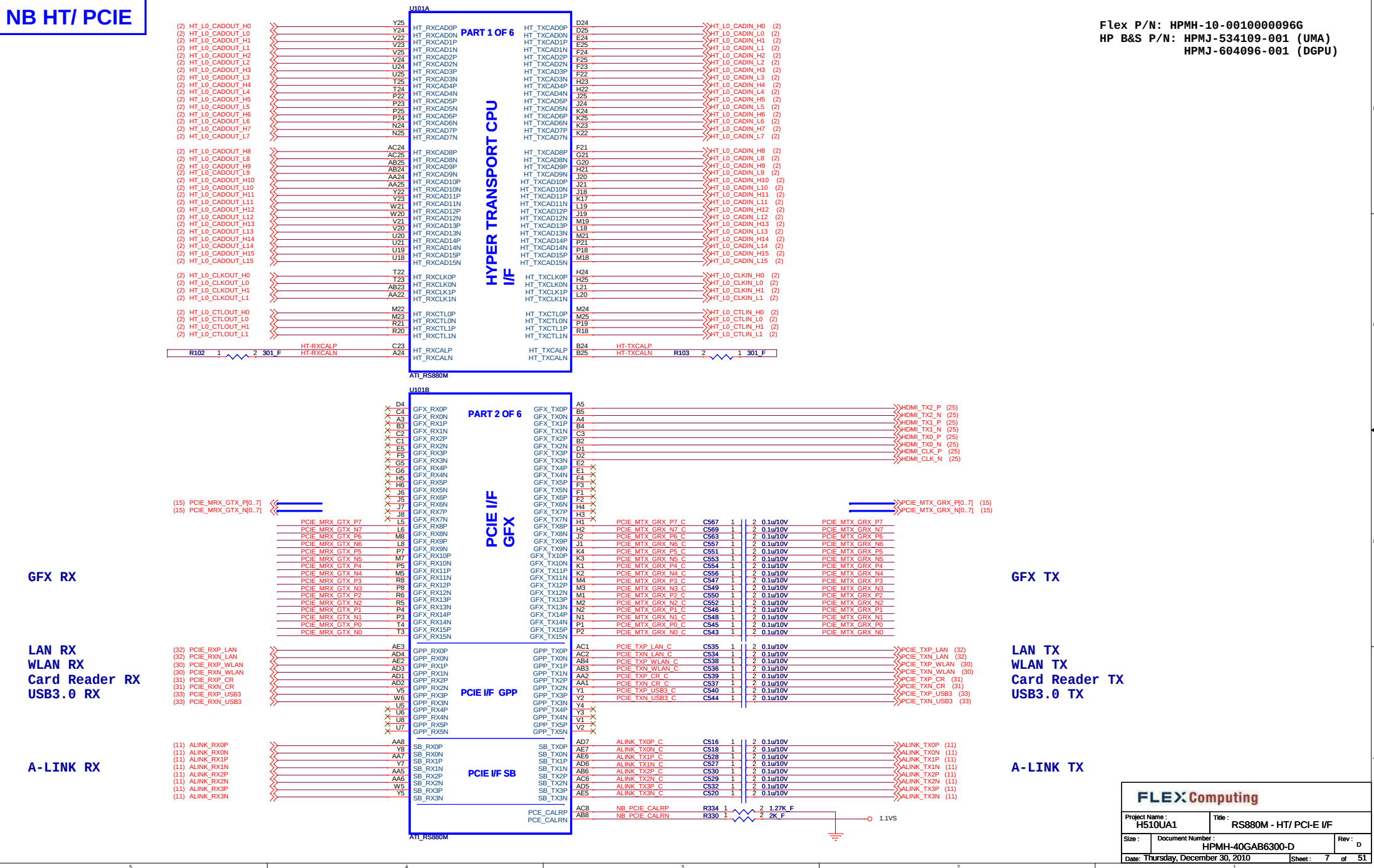
0.1uF Caps for CMD,CLK,CTRL return path
Place Caps on the same side as SO-DIMM
and close to VDD Pin .

**FLEXComputing**

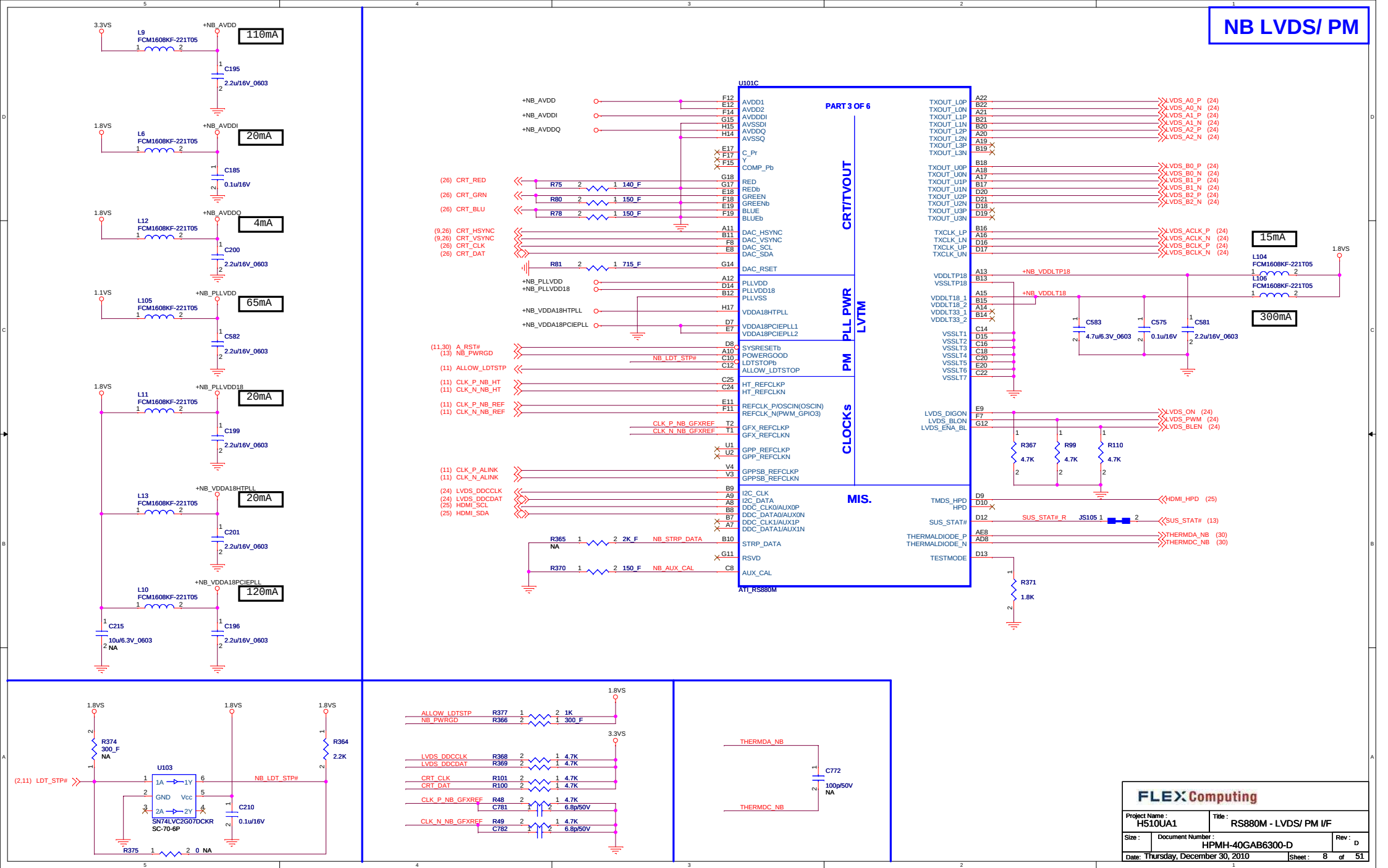
Project Name :	H510UA1	Title :	SO-DIMM Channel - B
Size :	Document Number :	HPMH-40GAB6300-D	Rev : D
Date : Thursday, December 30, 2010	Sheet : 6	of 51	

NB HT/ PCIE

Flex P/N: HPMH-10-00100000966
HP B&S P/N: HPMJ-534109-001 (UMA)
HPMJ-604096-001 (DGPU)



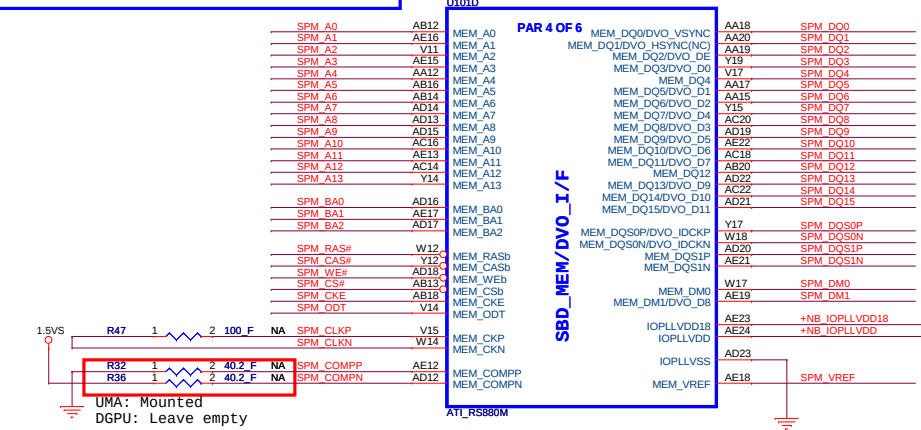
FLEX Computing	
Project Name : H510UA1	Title : RS880M - HT/ PCI-E I/F
Size : Document Number : HPMH-40GAB300-D	Rev : D
Date : Thursday, December 30, 2010	Sheet : 7 of 51



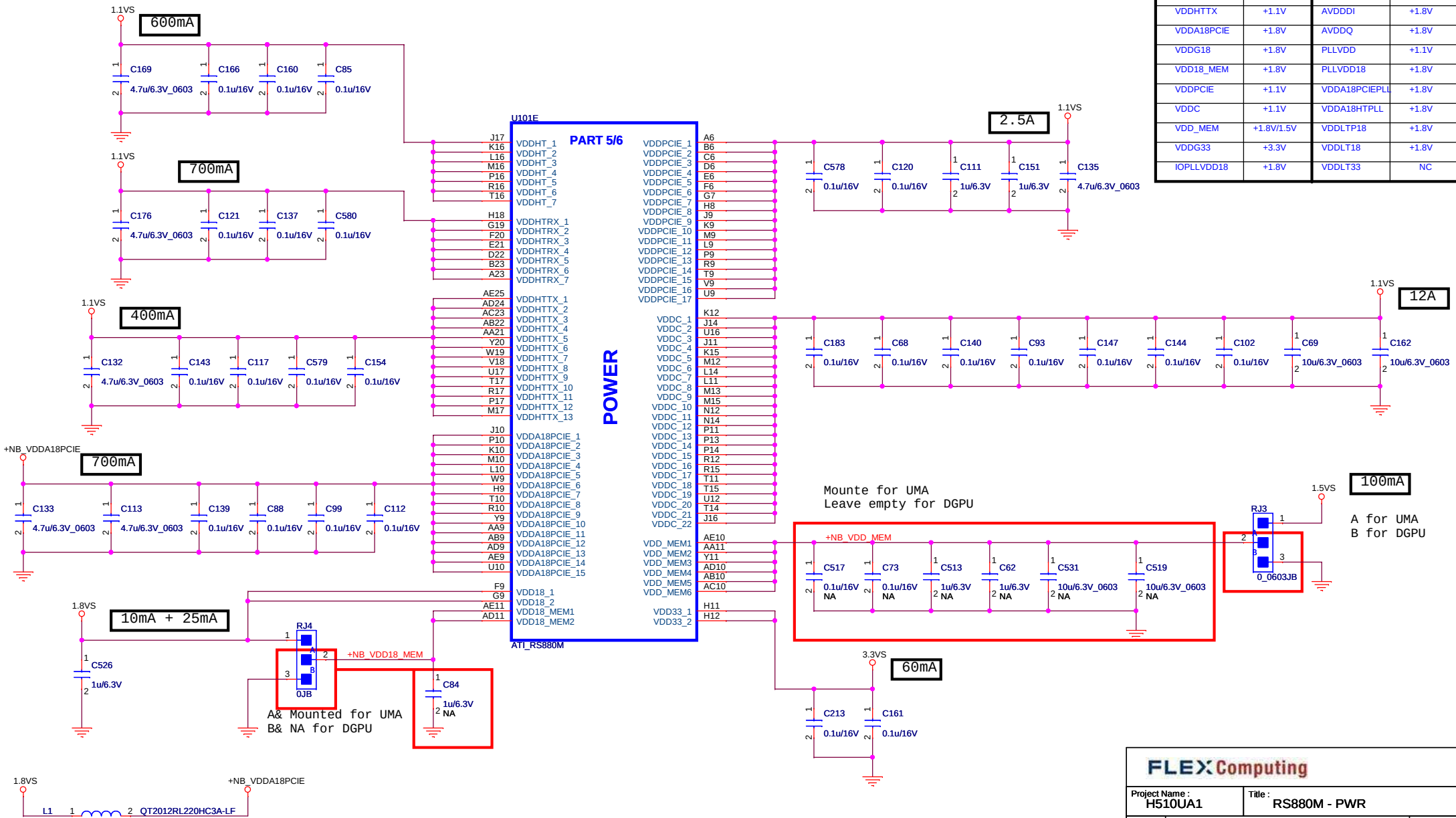
FLEXComputing

Project Name : H510UA1	Title : RS880M - LVDS/ PM I/F
Size : Document Number : HPMH-40GAB6300-D	Rev : D
Date: Thursday, December 30, 2010	Sheet : 8 of 51

NB Side Port/ Strapping



NB PWR



RS880M POWER TABLE

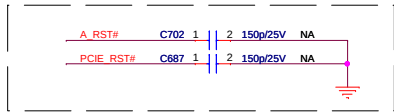
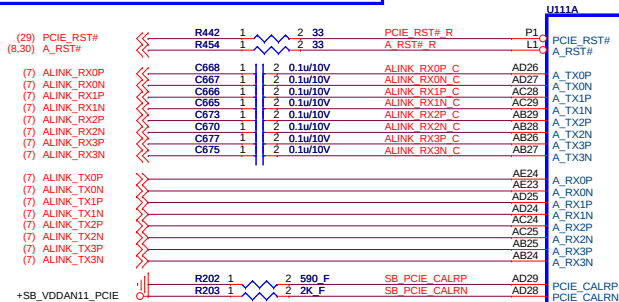
PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.1V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL18T33	NC

FLEX Computing

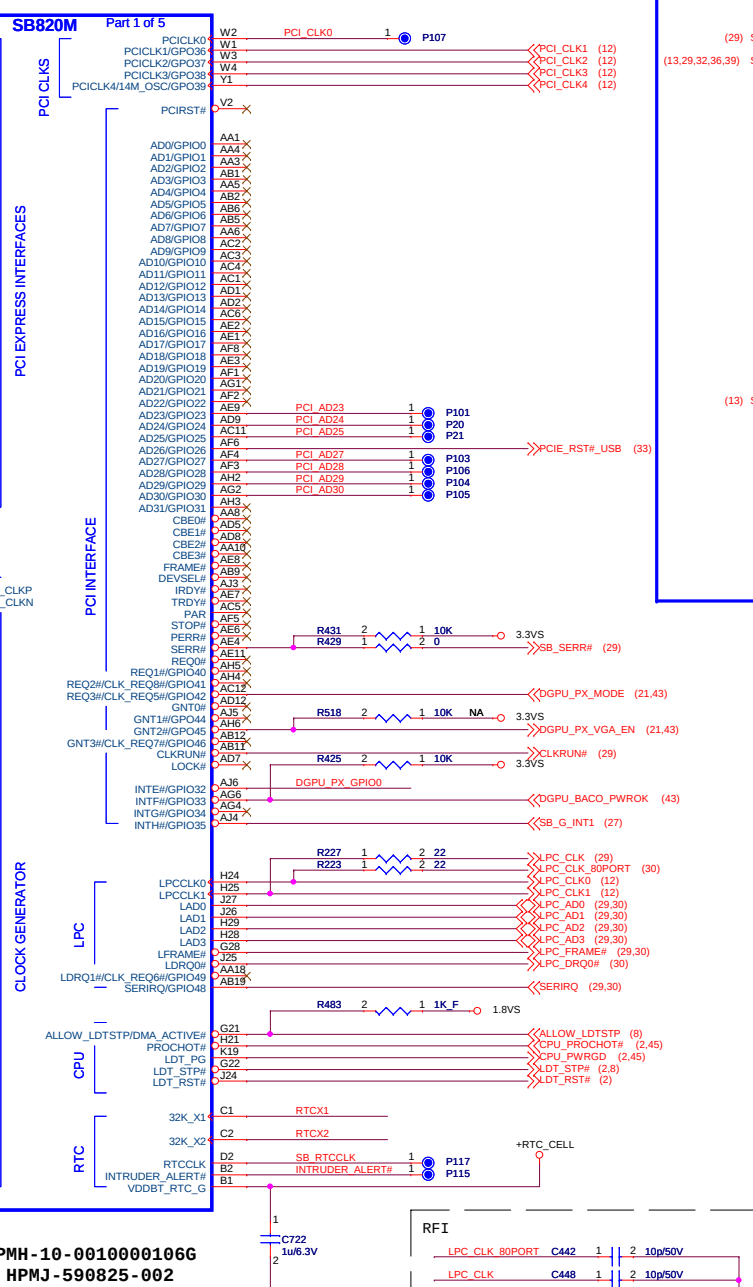
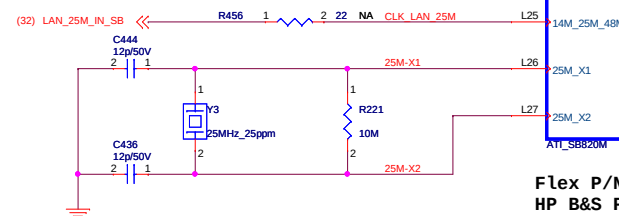
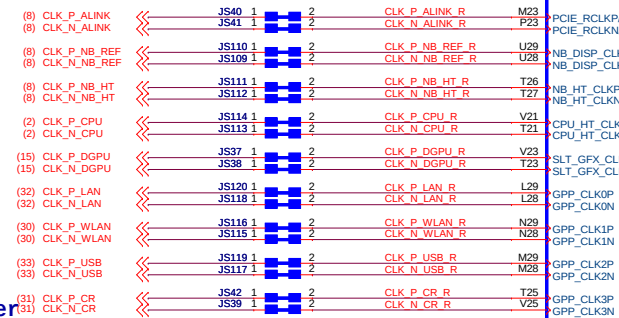
Project Name : H510UA1		Title : RS880M - PWR	
Size :	Document Number : HPMH-40GAB6300-D		Rev : D
Date: Thursday, December 30, 2010		Sheet : 10 of 51	

SB PCI-E/ CPU/ Alink/ CLK I/F

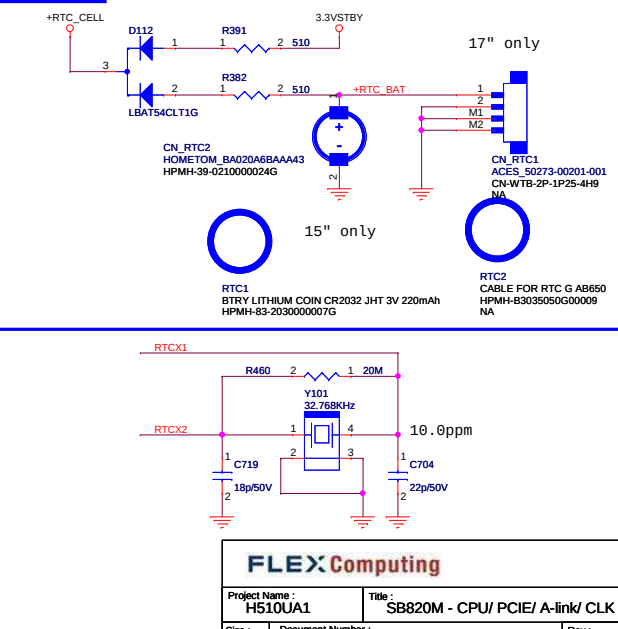
A-Link



GFX LAN WLAN USB3.0 Card Reader



RTC



FLEXComputing

Project Name:	H510UA1	Title:	SB820M - CPU/ PCIE/ A-link/ CLK
Size:	Document Number:	HPMH-40GAB6300-D	Rev: D
Date:	Thursday, December 30, 2010	Sheet:	11 of 51

SB820M Debug Straps

PciIIByp (PCI AD27)

Bypass PCI PLL
(Used in functional test at tester):

L: Bypass internal PLL clock
H: Use internal PLL generated PLL CLK (Internal Pull-Up of 15Kohm)

ILAAutorunEnB (PCI AD26)

ILA Auto run Enable

L: ILA Auto run enable
H: ILA Auto run disable (Internal Pull-Up of 15Kohm)

FCCIkByP (PCI AD25)

Bypass FC CLK

L: Bypass internal FC CLK (Used in functional test at tester)
H: Use internal FC CLK

I2CROMEn (PCI AD24)

I2C ROM Enable. Load the setting for A-Link Express/ PLL/
music control from I2C ROM

L: Getting the value from I2C EPROM
H: Disable I2C ROM
(Internal Pull-Up of 15Kohm)

PCI_ROM_BOOT (PCI AD23)

Bootting from PCI memory

L: Route ROM fetch tp PCI bus on the very first boot. Use
ROMTYPE to determine the ROM type on the subsequent boots.
H: Use ROMTYPE straps to determine the ROM type
(Internal Pull-Up of 15Kohm)

PCIe EEPROM Data/ Clock (PCI_REQ3/ PCI_GNT3)

PCIe EEPROM Data/ Clock

Connected to PCIe EEPROM SDA/ SCL pin or provided test
point access for lad use.

SB820M H/W STRAPS

ECEnableStrap (LPCCLK0)

Embedded Controller (EC):

L: Disable
H: Enable



Type I are captured on RSMRST#
Type II are captured on PWRGD.

CLKGEN (LPCCLK1)

Define Clock Generator:

L: External clock mode
H: Internal clock mode

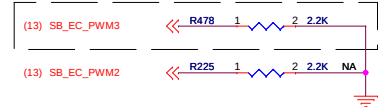


ROMTYPE_1&0 (EC_PWM3& EC_PWM2)

ROMTYPE_1 EC_PWM3	ROMTYPE_0 EC_PWM2	ROM type
0	0	FWH
0	1	LPC& PMC ROM
1	0	SPI
1	1	Reserve

Default Pull-High Pull-Low --> 2.2Kohm

Reserved for Pull-Low selection.



BIF_GEN2_COMPLIANCE_Strap (PCI_CLK1)

Set PCIe to Gen II mode:

SB820M: Only provision for Pull
down is required, not install
by default.



BootFailTmrEn (PCI_CLK2)

Watchdog function:

L: Disable BootFailtmr function
H: Enable BootFailtmr function



DefaulStrapMode (PCI_CLK3)

Default Debug Straps:

L: Disable Debug Straps
H: Select external Debug Straps



CPUClkSel (PCI_CLK4)

CPU/ NB HT Clock Selection:

L: Reserved
H: Required setting for
integrated clock mode



CoreSpeedMode (AZ_SDOUT)

Slow down core clock for low power
mobile platform:

L: Performance Mode
H: Low Power Mode

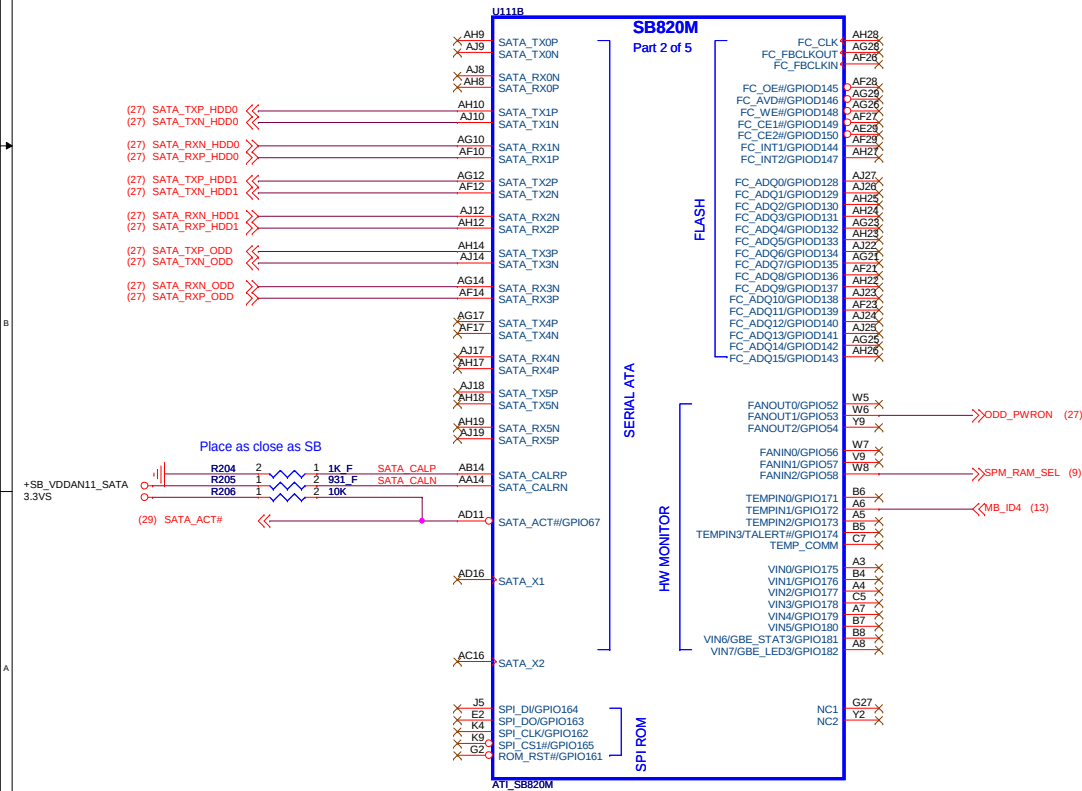


Type I : LPCCLK0, EC_PWM3& EC_PWM2
Type II : the rest of strapping

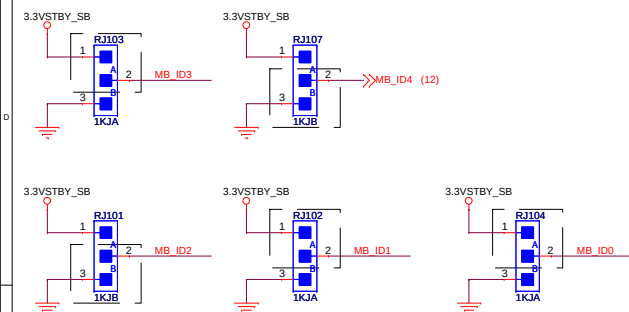
FLEXComputing

Project Name : H510UA1	Title : SB820M - SATA/ SPI/ Strap
Size :	Document Number : HPMH-40GAB6300-D
Date: Thursday, December 30, 2010	Rev : D
Sheet : 12	of 51

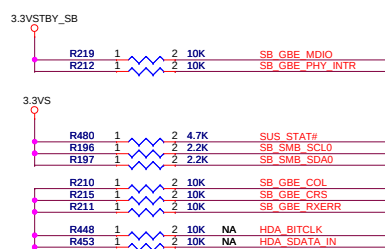
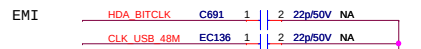
SB SATA/ SPI/ STRAP



Mother Board ID:



ID4	ID3	ID2	ID1	ID0	Board ID	Board ID
0	0	1	1	0	0x366A	Kelly 1.x UMA (IMR)
0	0	1	1	1	0x366B	Kelly 1.x Seymour XT (IMR)
0	1	0	0	0	0x366C	Kelly 1.x Whistler Pro (IMR)
0	1	0	0	1	0x1649	Kelly 1.x UMA
0	1	0	1	0	0x164A	Kelly 1.x Seymour XT
0	1	0	1	1	0x164B	Kelly 1.x Whistler Pro
0	1	1	0	0	0x164C	Young 1.x UMA
0	1	1	0	1	0x164D	Young 1.x Seymour XT
0	1	1	1	0	0x164E	Young 1.x Whistler Pro



(11,29,32,36,39) SLP_S3#
(29) SLP_S5#
(29) SB_PWRBTN#
(11) SB_PWRGD
(8) SUS_STAT#

(29) A20GATE
(29) KB_RST#
(29) SB_EXT_SC#
(29) SB_EXT_SM#

(32,33) PCIE_WAKE#

(8) NB_PWRGD
(29) RSMRST#

(31) CR_CLKREQ#

(32) LAN_CLKREQ#

(35) SPKR
(5,6,30,36) SB_SMB_SCL0
(5,6,30,36) SB_SMB_SDA0

(33) USB3_CLKREQ#
(30) WLAN_CLKREQ#

(9) SPM_RST#

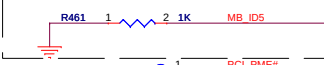
(29) SIO_EXT_WAKE#
(31) CR_GPIO

(27) ODD_PLUGIN#
(33) USB3_SM#
(34) USB_OC#
(38) USB_OC#

(35) HDA_BITCLK
(35) HDA_SDAT_A OUT
(35) HDA_SDAT_A IN
(12) HDA_SDAT_A OUT_R

(35) HDA_SYNC
(35,36) HDA_RESET#

Stage ID
High --> SI (Default internal PU)
Low --> PV



(29) A20GATE
(29) KB_RST#
(29) SB_PWRBTN#
(11) SB_PWRGD
(8) SUS_STAT#

(29) A20GATE
(29) KB_RST#
(29) SB_PWRBTN#
(11) SB_PWRGD
(8) SUS_STAT#

(32,33) PCIE_WAKE#

(8) NB_PWRGD
(29) RSMRST#

(31) CR_CLKREQ#

(32) LAN_CLKREQ#

(35) SPKR
(5,6,30,36) SB_SMB_SCL0
(5,6,30,36) SB_SMB_SDA0

(33) USB3_CLKREQ#
(30) WLAN_CLKREQ#

(9) SPM_RST#

(29) SIO_EXT_WAKE#
(31) CR_GPIO

(27) ODD_PLUGIN#
(33) USB3_SM#
(34) USB_OC#
(38) USB_OC#

(35) HDA_BITCLK
(35) HDA_SDAT_A OUT
(35) HDA_SDAT_A IN
(12) HDA_SDAT_A OUT_R

(35) HDA_SYNC
(35,36) HDA_RESET#

U1110

PCI_PME#/GVENT4#
Rst#GVENT22#
SPL_CS#/GBE_STAT1/GVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GVENT0#
KBRST#GVENT1#
LPC_PME#GVENT3#
LPC_SM#GVENT23#
GVENT5#
SYS_RESET#GVENT19#
WAKE#GVENT6#
IR_RX1/GVENT20#
THRMTRIP#SMBALERT#GVENT2#
NB_PWRGD
RSMRST#

AD19
RA16
AB17
AC18
AF20
AE19
AF19
AD22
AE22
SA20/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ1#FANOUT4/GPIO61
IR_LED#ILB#GPIO184
SMARTVOLT2#SHUTDOWN#GPIO51
DDR3_RST#GVENT7#
GBE_LED#GVENT9#
GBE_LED2/GVENT10#
GBE_STAT0/GVENT11#
CLK_REQ#GPIO65/OSCIN

BLINK#USB_OC7#GVENT18#
USB_OC#IR_TX1/GVENT16#
USB_OC#IR_TX0/GVENT17#
USB_OC#IR_RX0/GVENT16#
USB_OC#AC_PRESENT/GVENT15#
USB_OC#TCK/GVENT14#
USB_OC#TDI/GVENT13#
USB_OC#TRST#GVENT12#

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#

GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR

PS2_DAT#SDA4/GPIO187
PS2_CLK#SCL4/GPIO188
SPL_CS#GBE_STAT2/GPIO166
FC_RST#GPIO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/GPIO223
KSO_15/GPIO224
KSO_16/GPIO225
KSO_17/GPIO226

EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/GPIO199
EC_PWM3/EC_TIMER3/GPIO200

SB_GBE_COL
SB_GBE_CRS
SB_GBE_MDIO
SB_GBE_MDCK
SB_GBE_RXERR
SB_GBE_PHY_INTR

SB_GBE_COL
SB_GBE_CRS
SB_GBE_MDIO
SB_GBE_MDCK
SB_GBE_RXERR
SB_GBE_PHY_INTR

SB_GBE_COL
SB_GBE_CRS
SB_GBE_MDIO
SB_GBE_MDCK
SB_GBE_RXERR
SB_GBE_PHY_INTR

SB_GBE_COL
SB_GBE_CRS
SB_GBE_MDIO
SB_GBE_MDCK
SB_GBE_RXERR
SB_GBE_PHY_INTR

SB_GBE_COL
SB_GBE_CRS
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SB_GBE_MDCK
SB_GBE_RXERR
SB_GBE_PHY_INTR

SB_GBE_COL
SB_GBE_CRS
SB_GBE_MDIO
SB_GBE_MDCK
SB_GBE_RXERR
SB_GBE_PHY_INTR

SB_GBE_COL
SB_GBE_CRS
SB_GBE_MDIO
SB_GBE_MDCK
SB_GBE_RXERR
SB_GBE_PHY_INTR

USBCCLK/14M_25M_48M_OSC

USB_RCOMP
USBS_FSD1P/GPIO186
USB_FSD1N
USBS_FSD0P/GPIO185
USB_FSD0N

USBS_HSD13P
USBS_HSD13N
USBS_HSD12P
USBS_HSD12N
USBS_HSD11P
USBS_HSD11N
USBS_HSD10P
USBS_HSD10N

USBS_HSD9P
USBS_HSD9N
USBS_HSD8P
USBS_HSD8N
USBS_HSD7P
USBS_HSD7N
USBS_HSD6P
USBS_HSD6N

USBS_HSD5P
USBS_HSD5N
USBS_HSD4P
USBS_HSD4N
USBS_HSD3P
USBS_HSD3N
USBS_HSD2P
USBS_HSD2N

USBS_HSD1P
USBS_HSD1N
USBS_HSD0P
USBS_HSD0N

USBS_HSD1P
USBS_HSD1N
USBS_HSD0P
USBS_HSD0N

USBS_HSD1P
USBS_HSD1N
USBS_HSD0P
USBS_HSD0N

USBS_HSD1P
USBS_HSD1N
USBS_HSD0P
USBS_HSD0N

USBS_HSD1P
USBS_HSD1N
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USBS_HSD0N

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USBS_HSD0N

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USBS_HSD0P
USBS_HSD0N

USBS_HSD1P
USBS_HSD1N
USBS_HSD0P
USBS_HSD0N

USBS_HSD1P
USBS_HSD1N
USBS_HSD0P
USBS_HSD0N

A10 CLK_USB_48M R R479 1 2 22 NA

G19 USB-RCOMP R224 1 2 11.8K F

USBS_FSD1P/GPIO186
USB_FSD1N
USBS_FSD0P/GPIO185
USB_FSD0N

USBS_HSD13P
USBS_HSD13N
USBS_HSD12P
USBS_HSD12N
USBS_HSD11P
USBS_HSD11N
USBS_HSD10P
USBS_HSD10N

USBS_HSD9P
USBS_HSD9N
USBS_HSD8P
USBS_HSD8N
USBS_HSD7P
USBS_HSD7N
USBS_HSD6P
USBS_HSD6N

USBS_HSD5P
USBS_HSD5N
USBS_HSD4P
USBS_HSD4N
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USBS_HSD3N
USBS_HSD2P
USBS_HSD2N

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USBS_HSD0N

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USBS_HSD0N

USBS_HSD1P
USBS_HSD1N
USBS_HSD0P
USBS_HSD0N

A10 CLK_USB_48M R R479 1 2 22 NA

G19 USB-RCOMP R224 1 2 11.8K F

USBS_FSD1P/GPIO186
USB_FSD1N
USBS_FSD0P/GPIO185
USB_FSD0N

USBS_HSD13P
USBS_HSD13N
USBS_HSD12P
USBS_HSD12N
USBS_HSD11P
USBS_HSD11N
USBS_HSD10P
USBS_HSD10N

USBS_HSD9P
USBS_HSD9N
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USBS_HSD7N
USBS_HSD6P
USBS_HSD6N

USBS_HSD5P
USBS_HSD5N
USBS_HSD4P
USBS_HSD4N
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USBS_HSD3N
USBS_HSD2P
USBS_HSD2N

USBS_HSD1P
USBS_HSD1N
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USBS_HSD0N

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USBS_HSD0P
USBS_HSD0N

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USBS_HSD1P
USBS_HSD1N
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USBS_HSD0N

USBS_HSD1P
USBS_HSD1N
USBS_HSD0P
USBS_HSD0N

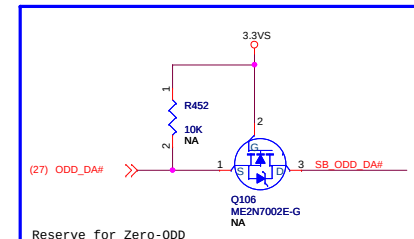
USBS_HSD1P
USBS_HSD1N
USBS_HSD0P
USBS_HSD0N

USBS_HSD1P
USBS_HSD1N
USBS_HSD0P
USBS_HSD0N

Touch
Screen
Web CAM

Finger
Print
WLAN

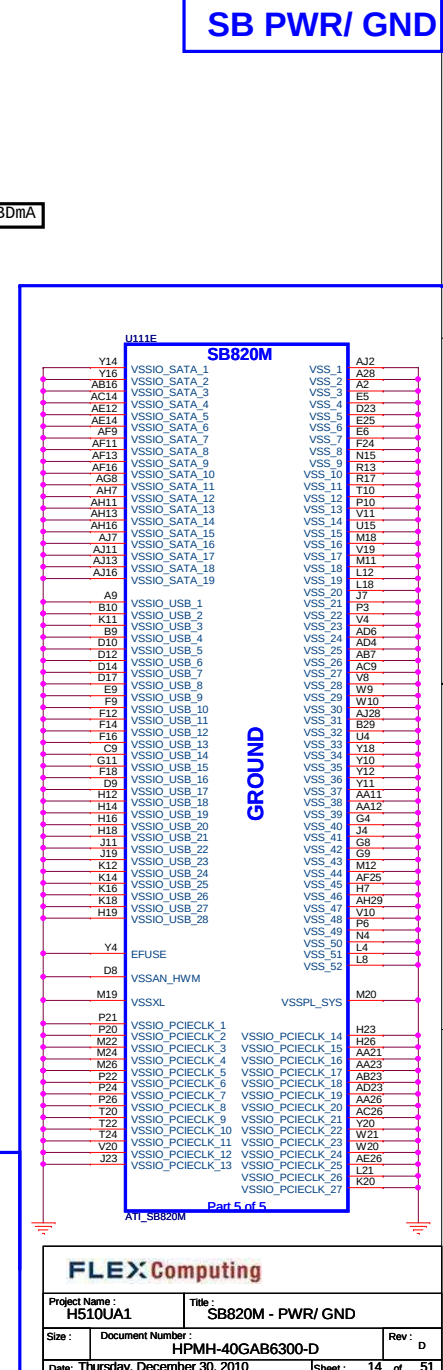
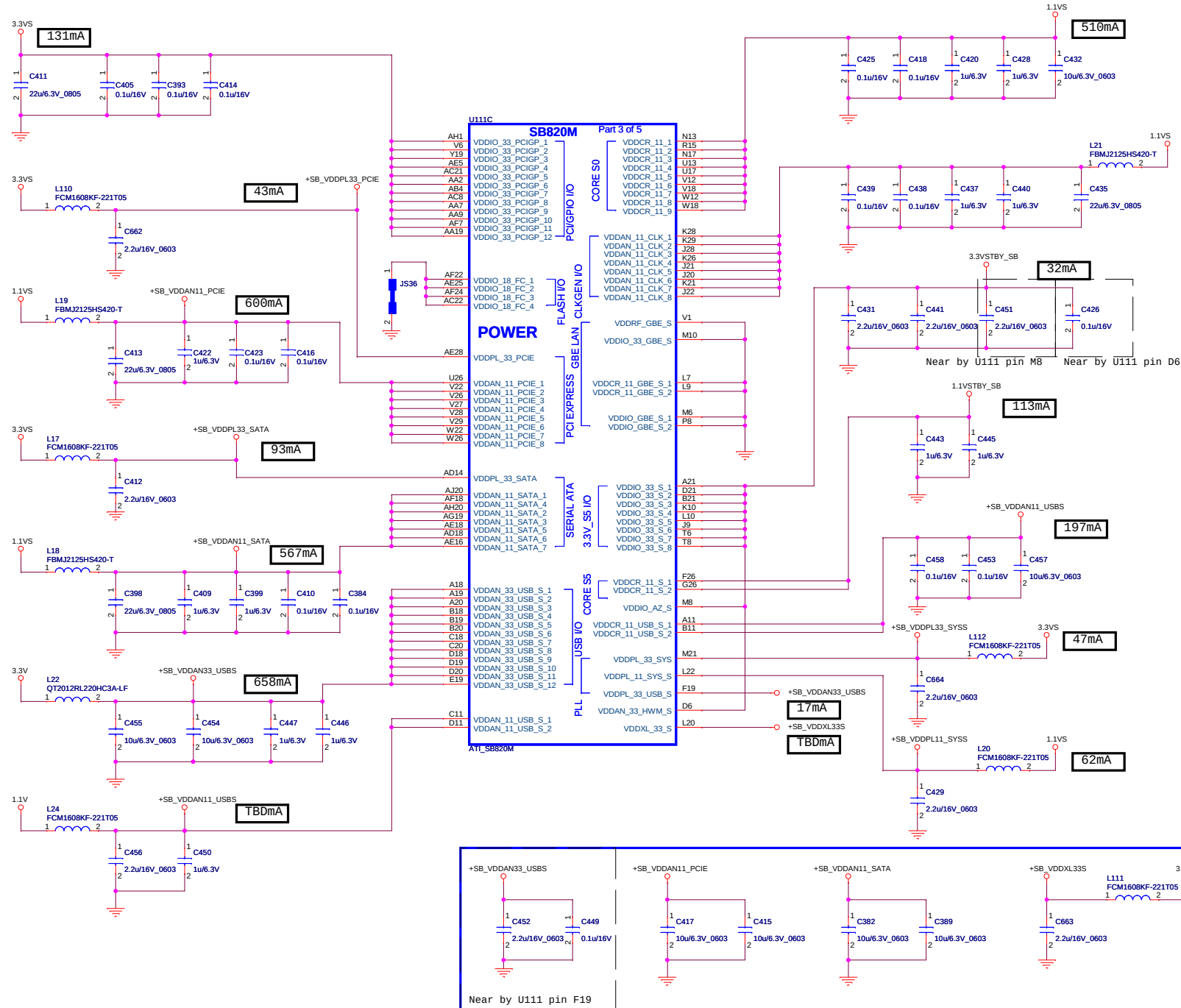
Port 3
Port 2
Port 1
Port 0



Reserve for Zero-ODD

Project Name : H510UA1		Title : SB820M - ACPI/ USB/ HDA/ GLAN	
Size :	Document Number :	Rev : D	
Date: Thursday, December 30, 2010		Sheet : 13 of 51	

SB PWR/ GND

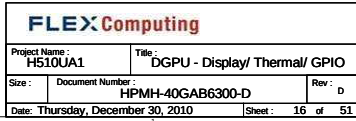
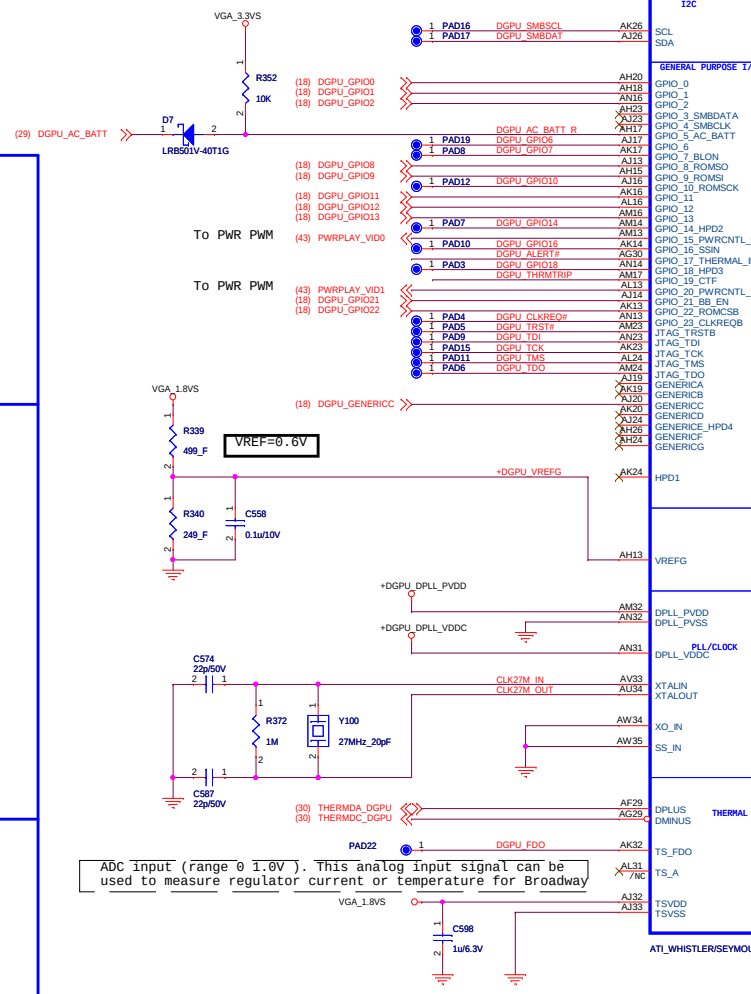


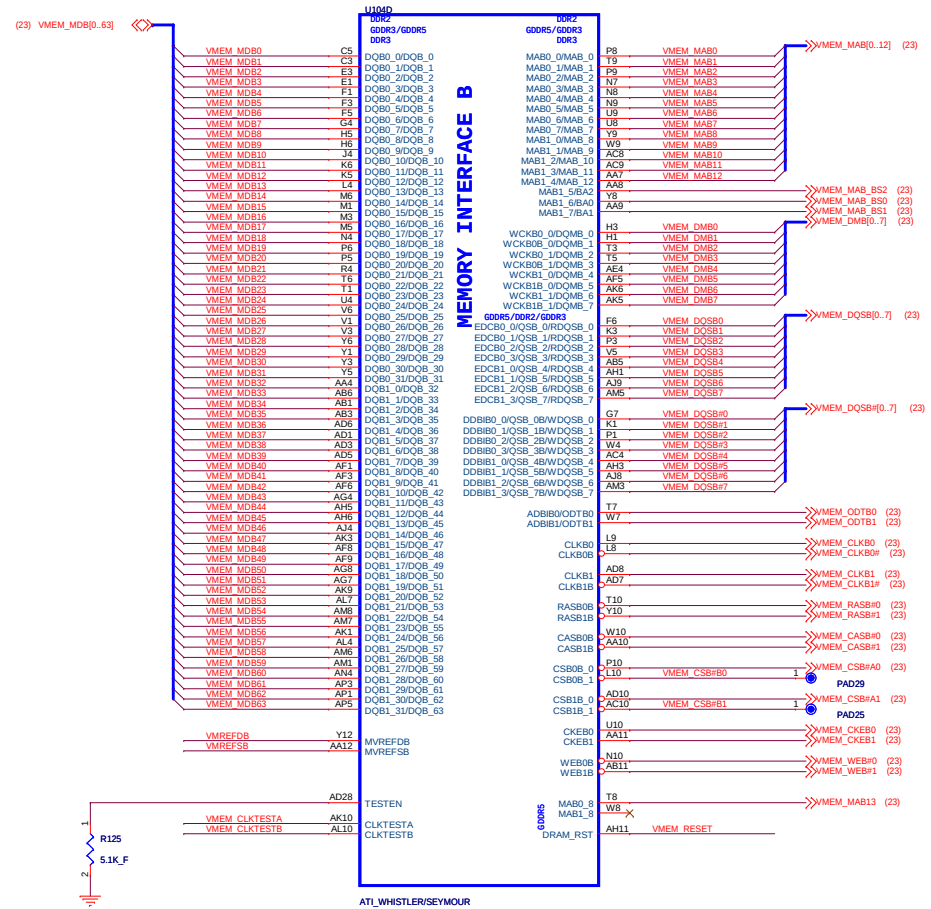
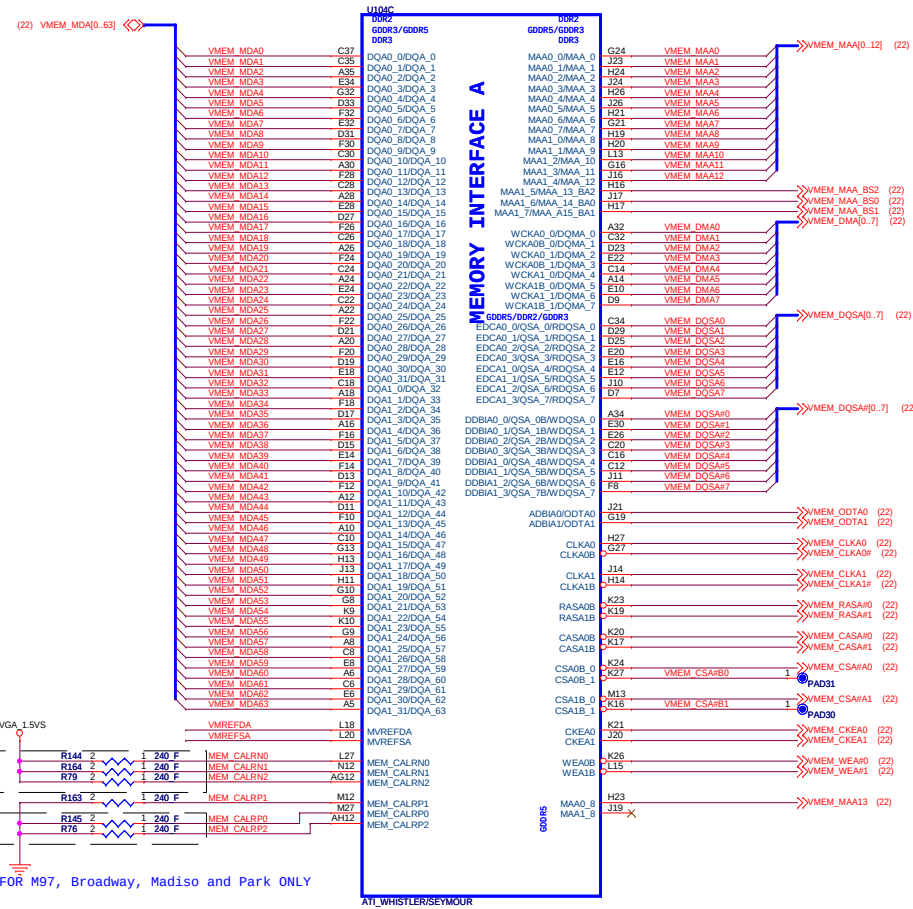
Seymour
Flex P/N: HPMH-10-0020000049G
HP B&S P/N: HPMJ-633843-001
Whistler
Flex P/N: HPMH-10-0020000050G
HP B&S P/N: HPMJ-628114-001



Project Name : H510UA1		Title : DGPU - PCI-E/ LVDS I/F	
Size :	Document Number : HPMH-40GAB6300-D		Rev : D
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```
128MX16:
  Hynix: HPMH-14-00D0000039G - IC DDR3 H5TQ2G63BFR-11C 128MX16 FBGA-96
  Samsung: HPMH-14-00D0000043G - IC K4W2G1646C-HC11 128Mb*16 96 FBGA
```

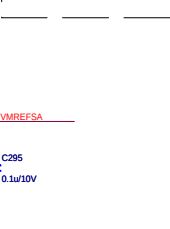
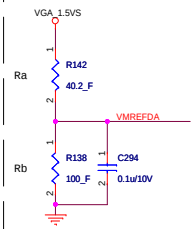




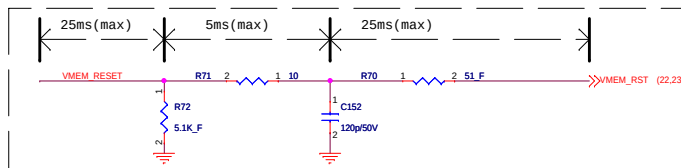
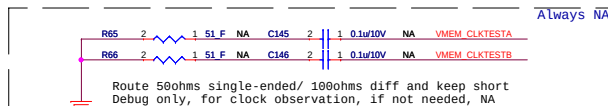
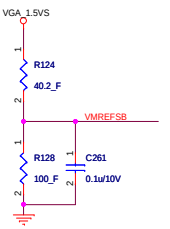
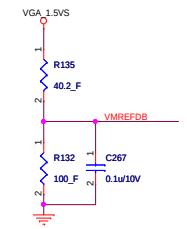
DIVIDER RESISTORS	DDR3/ GDDR3
MVREF TO 1.5V (Ra)	40.2R
MVREF TO GND (Rb)	100R

Place colse to Pin
For DDR3: 0.7 * VDDR1

Seymour: NA
Whistler: Mounte



Place colse to Pin
For DDR3: 0.7 * VDDR1

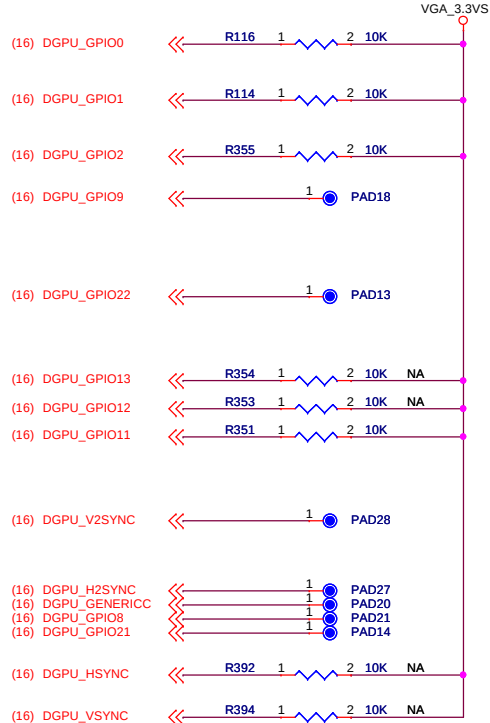


FLEX Computing

Project Name:	H510UA1	Title:	DGPU - VRAM I/F
Size:	Document Number:	HPMH-40GAB6300-D	Rev: D
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DGPU STRAP

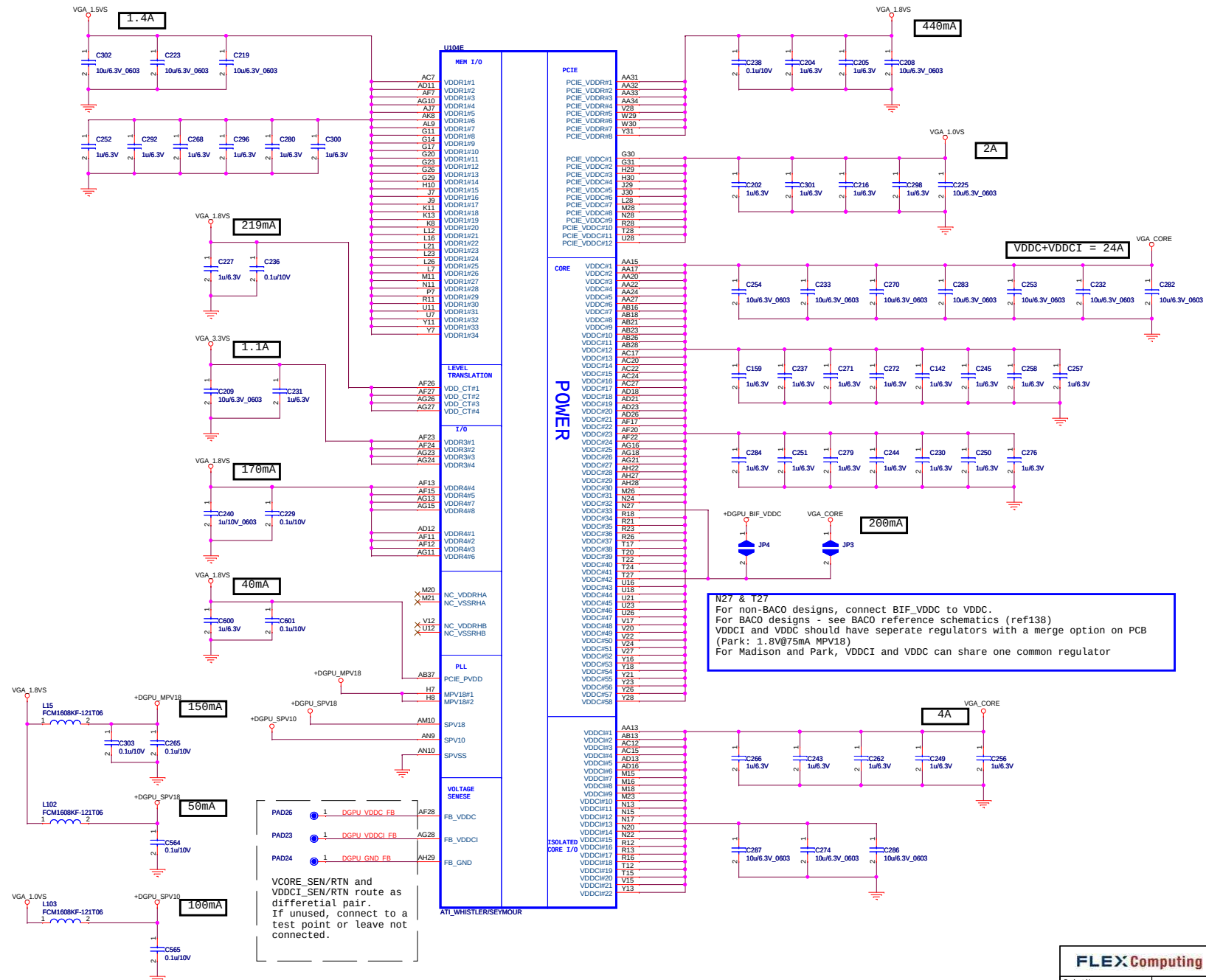
CONFIGURATION STRAPS				
STRAPS	PIN	DESCRIPTION	ASIC Deault	Status
TX_PWRS_ENB	GPIO0	Transmitter (Tx) power savings enable 0: 50% Tx output swing (DEFAULT) 1: Full Tx output swing	All Internal Pull Down	Mounted
TX_DEEMPH	GPIO1	PCI Express transmitter deemphasis enable. 0: Tx de-emphasis disabled (DEFAULT) 1: Tx de-emphasis enabled		Mounted
RESERVED	GPIO2	0 : PCIe device as 2.5 GT/s capable (DEFAULT) 1 : PCIe device as 5.0 GT/s capable		Mounted
VGA_DIS	GPIO9	VGA disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space): 0 : VGA Controller capacity enabled (DEFAULT) 1 : The device will not be recognized as the system's VGA controller		NA
BIOS_ROM_EN	GPIO_22_ROMCSB	0 - Disable external BIOS ROM device (DEFAULT) 1 - Enable external BIOS ROM device		NA
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	BIOS_ROM_EN = 1, Config[2:0] defines the ROM type. BIOS_ROM_EN = 0, Config[2:0] defines the primary memory aperture size. Size of the primary memory apertures CONFIG[2:0] 128 MB 000 256 MB 001 64MB 010 32MB 011		NA NA Mounted
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS L: Ignore VIP Device Strap (DEFAULT) H: Enable VIP Device Strap		NA
RSVD RSVD RSVD RSVD	H2SYNC GENERICC GPIO8 GPIO21_BB_EN			NA NA NA NA
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI		NA NA

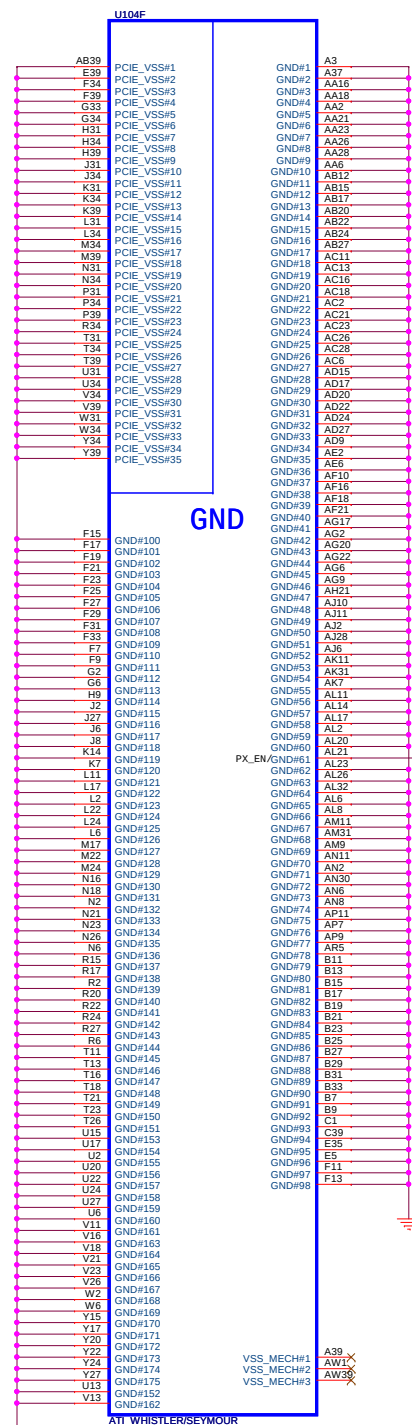


Signal	Seymour/Whistler	Robson/ Park/ Medison/ Capilano/ Broadway
Ball AJ21 on M2 Ball AG13 on S3	SWAPLOCKA SwaplockA/ B signals can be optionally used on a multi-GPU design with multiple display outputs to allow all displays in a group (group A or group B) to update at the same time and have synchronous left/ right stereo timing. Genlock of the GPUs is also needed, either via a genlock system, or by feeding all GPUs with the same reference clock. Also connecting SwaplockB is preferred, but not required. SwaplockA/ B are open drain, 3.3V signals. If this feature is not required, these signals can be used as 3.3V GPIOs or left unconnected on the PCB.	Ball AJ21 is NC on M2 packages Ball AG13 is R2SET on S3 package
Ball AK21 on M2 Ball H12 on S3	SWAPLOCKB - see above On a multi-gpu design, SwaplockB from all GPUs are connected together with an external pull-up resistor (10K Ohms). If this feature is not required, these signals can be used as 3.3V GPIOs or left unconnected on the PCB.	Ball AK21 is NC on M2 packages Ball AH12 is DAC2 Output - on S3 package

Signal	Seymour/Whistler	Robson/ Park/ Medison/ Capilano/ Broadway
Ball AC32 on M2	NC	DAC2 Output-C on M2 package
Ball AA29 on M2	NC	R2SET on M2 package
Ball AD32 on M2	NC	DAC2 Output- Y
Ball AG33 on M2	NC	A2VDD
Ball AD33 on M2	NC	A2VDDQ
Ball AF33 on M2	TSVSSQ	A2VSSQ
Ball AG33, AG32 on M2	NC	VDD2DI/VSS2DI
H2SYNC	GENLK_CLK (3.3V): Reference clock input (3.3V) for pixel PLL received from frame-lock/ gen-lock interface	H2SYNC
V2SYNC	GENLK_VSYNC (3.3V): Frame timing indicator.Output to frame-lock/genlock interface	V2SYNC

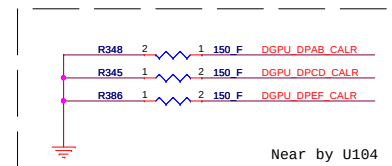
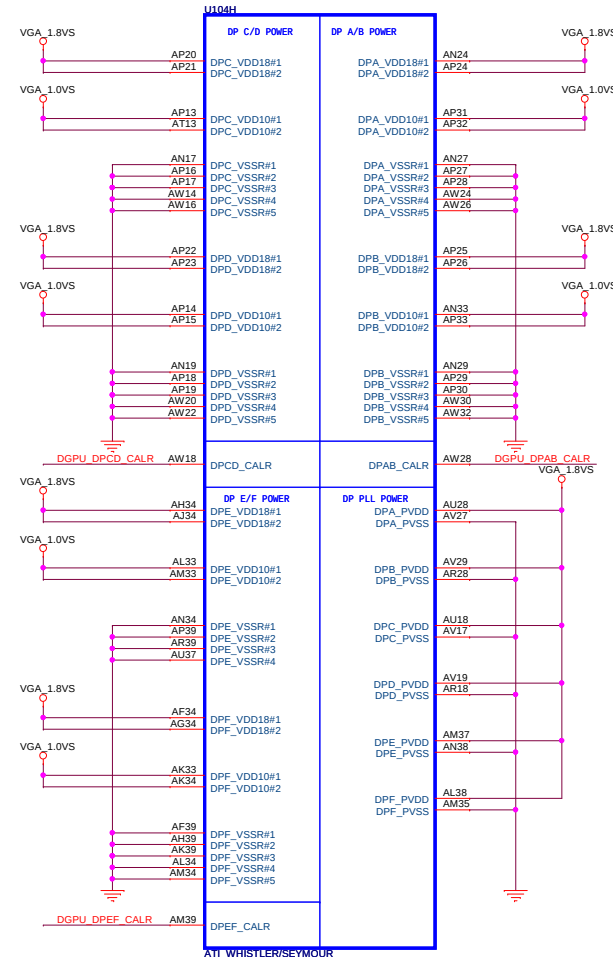
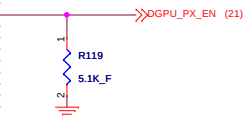
FLEX Computing			
Project Name : H510UA1		Title : DGPU - Strap	
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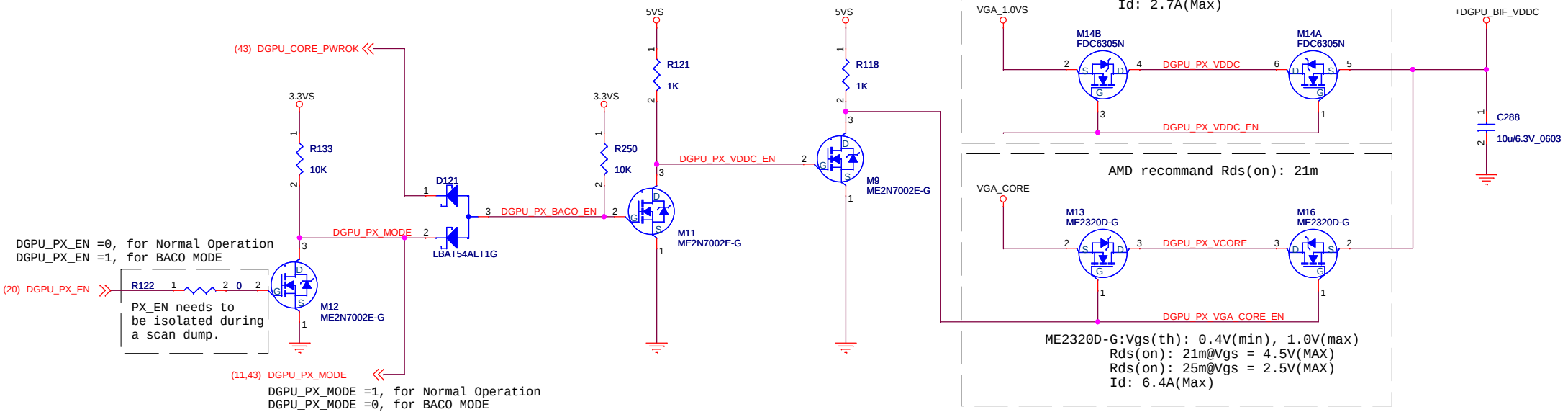
BACO design options as Apps Note Seymour/ Whistler/ Robson supported Park/ Madison/ Capilano/ Broadway not Applicable

For PX_EN, refer to the BACO reference schematics for detail.
PX_EN is used to control discrete GPU regulators for PowerXpress (Switchable graphics) BACO mode. A pull-down resistor is required. Leave signal unconnected if not used.

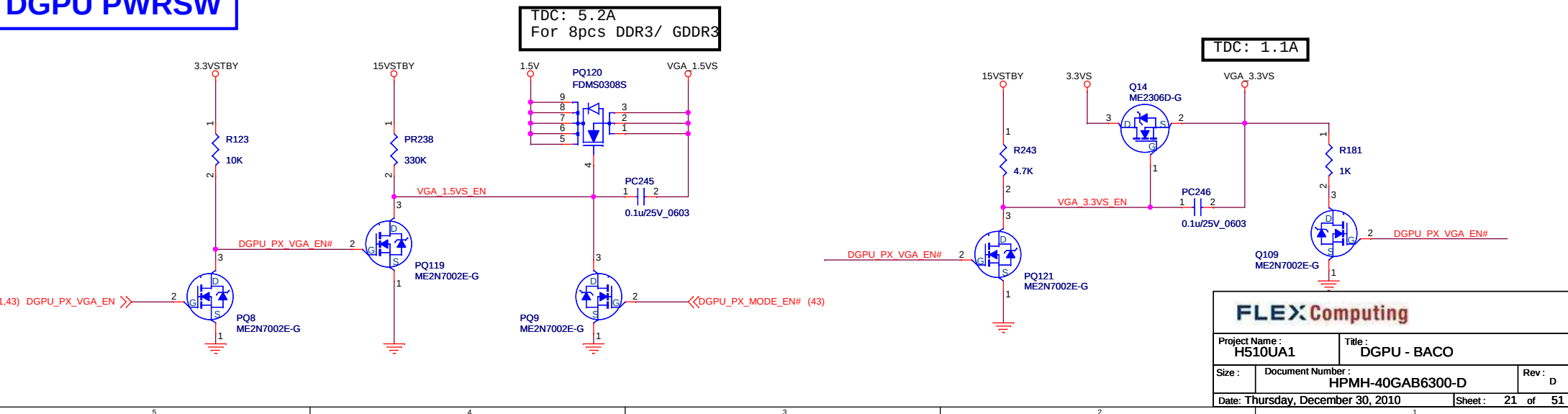


Near by U104

DGPU BACO



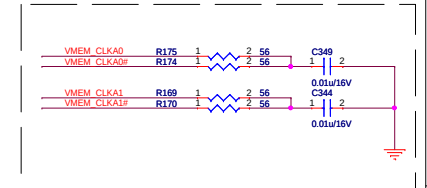
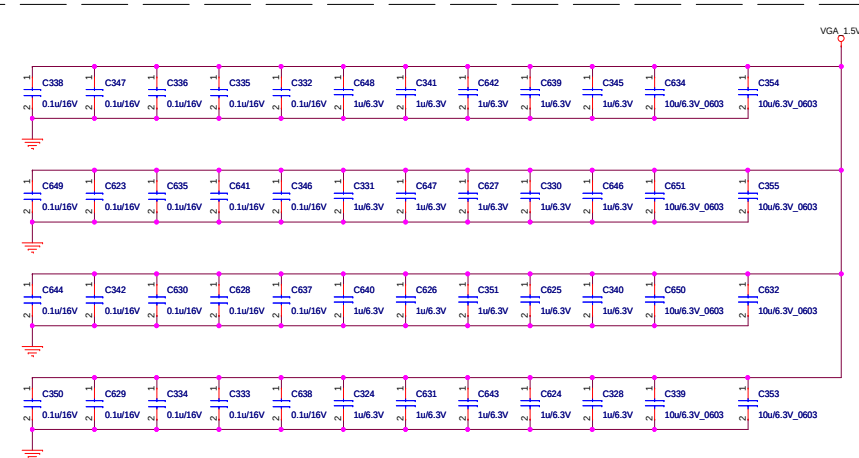
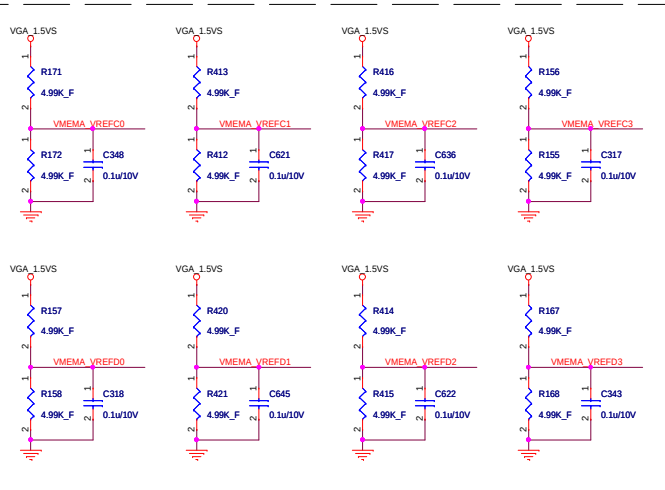
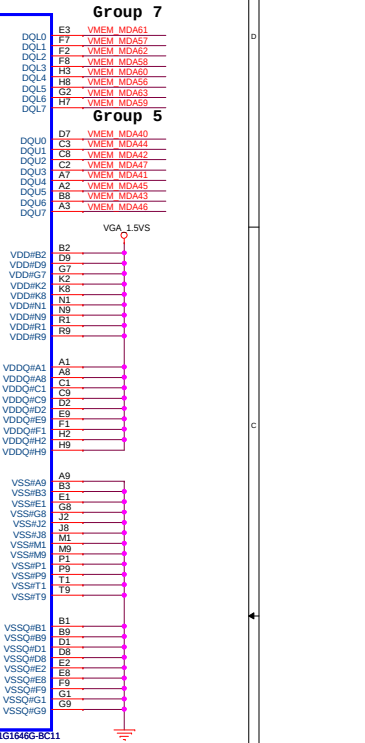
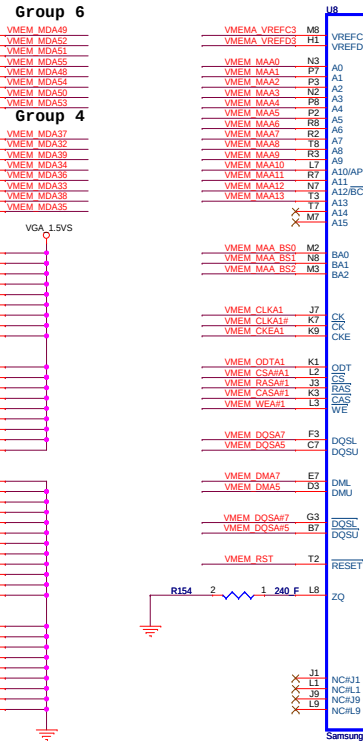
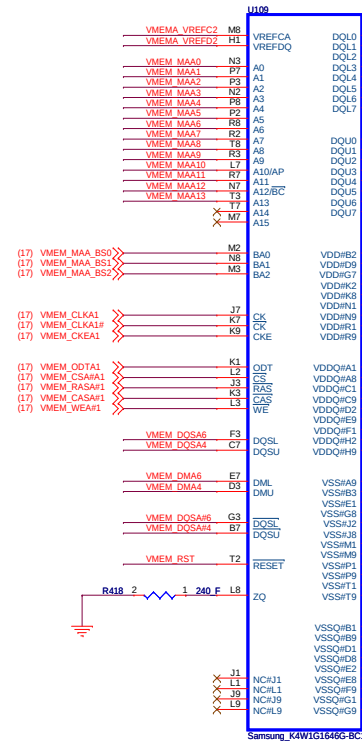
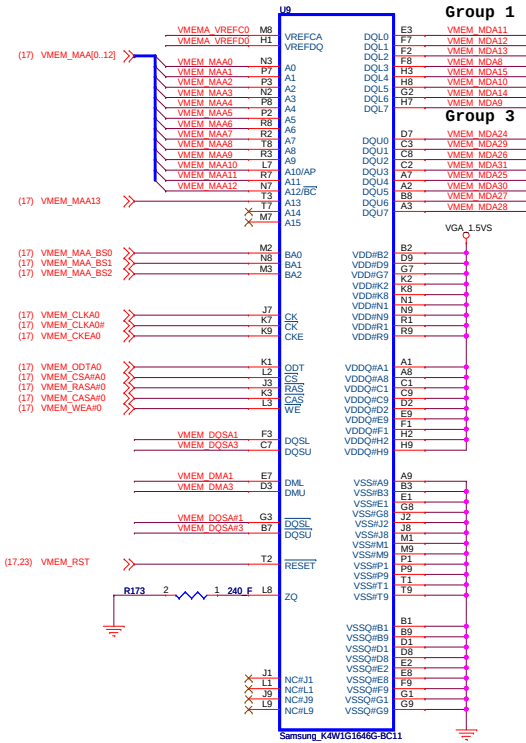
DGPU PWRSW



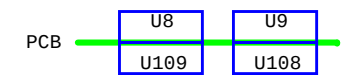
Samsung/ K4W1G1646G-BC11
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HP B&S P/N: HPMJ-506474-945
Hynix/ H5TQ1G63DFR-11C
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DGPU VRAM Channel - A

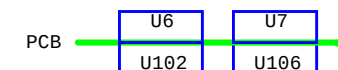
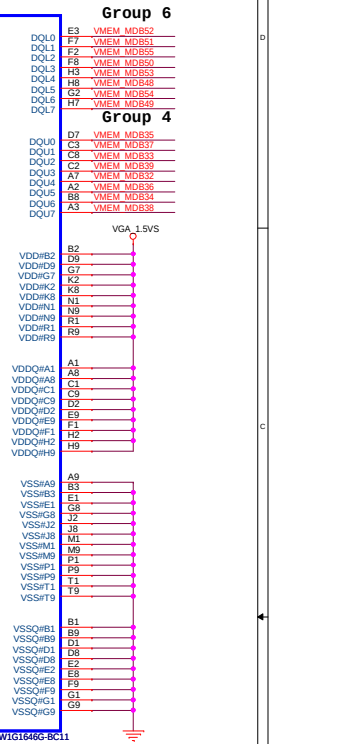
(17) VMEM_MDA0[0..3]
(17) VMEM_DMA0[0..7]
(17) VMEM_DQS0[0..7]
(17) VMEM_DQS0[0..7]



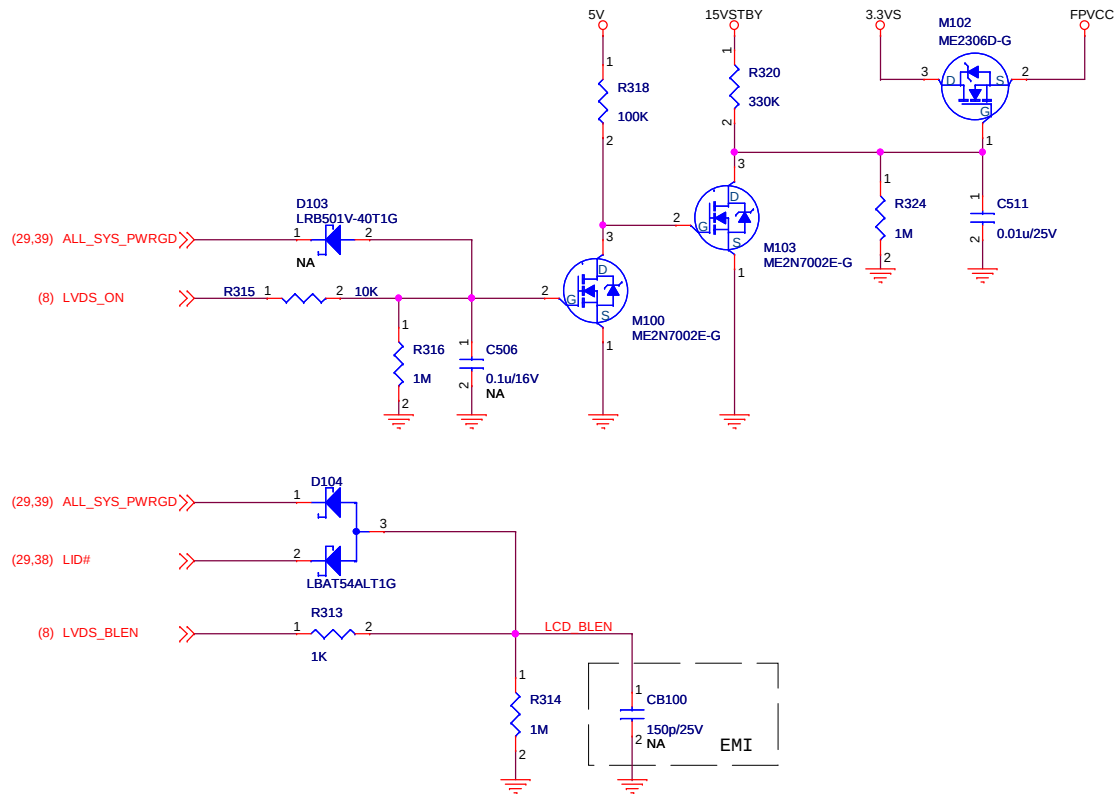
PCB Layout indicate



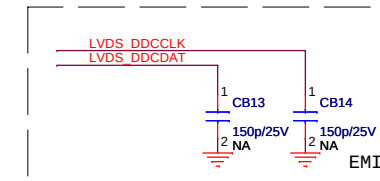
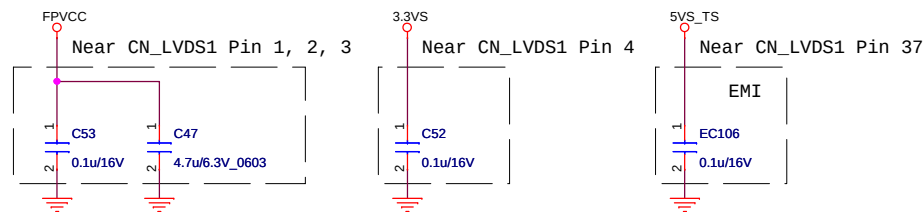
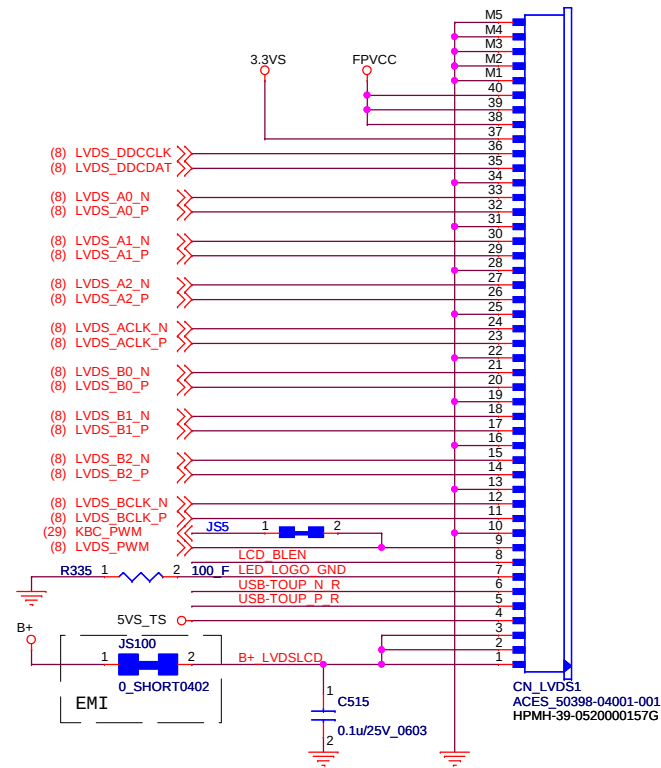
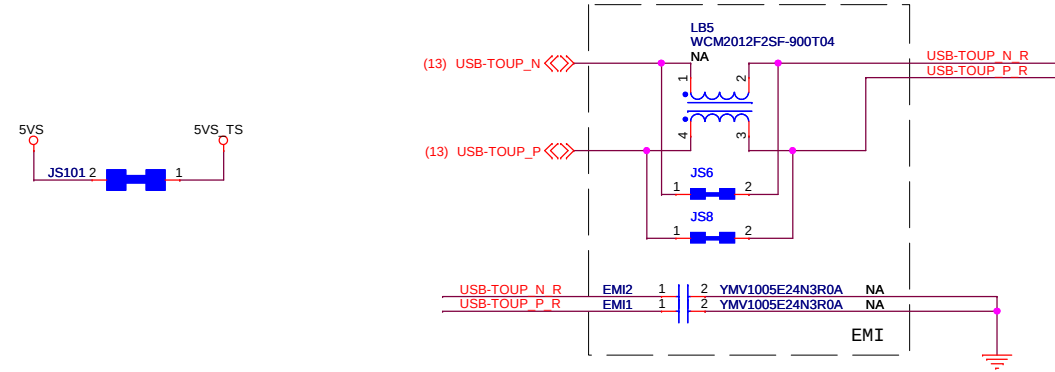
FLEX Computing



LVDS

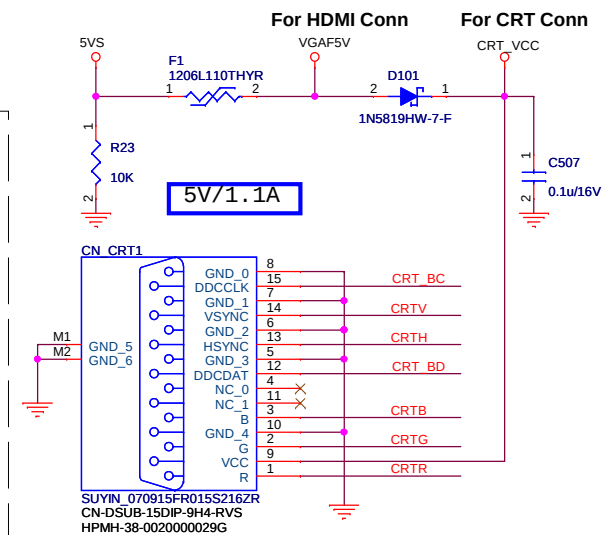
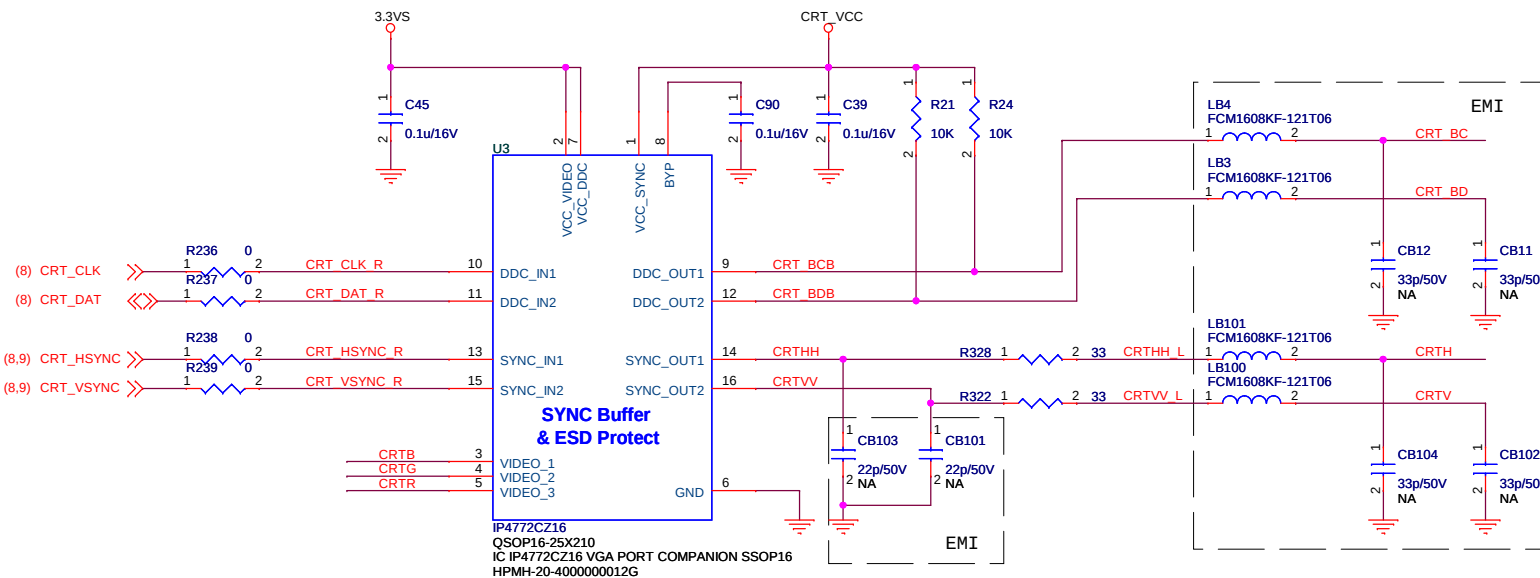
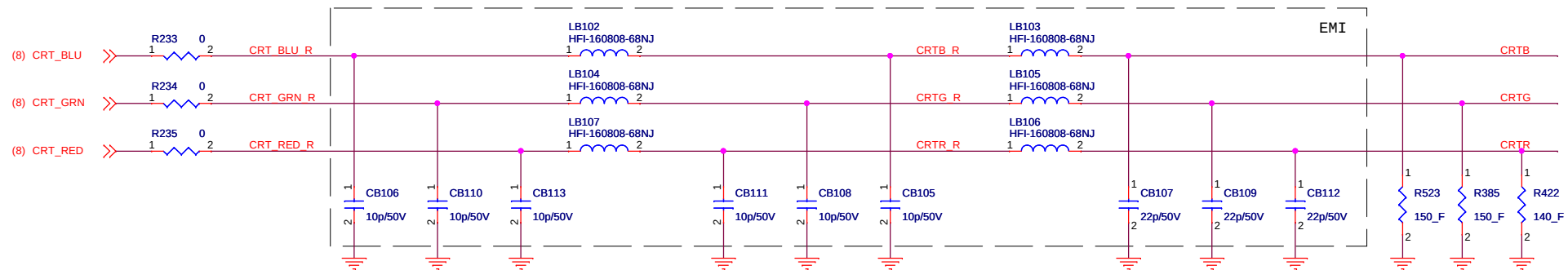


Touch Screen



FLEX Computing	
Project Name : H510UA1	Title : LVDS/ Touch Screen I/F
Size : Document Number : HPMH-40GAB6300-D	Rev : D
Date : Thursday, December 30, 2010	Sheet : 24 of 51

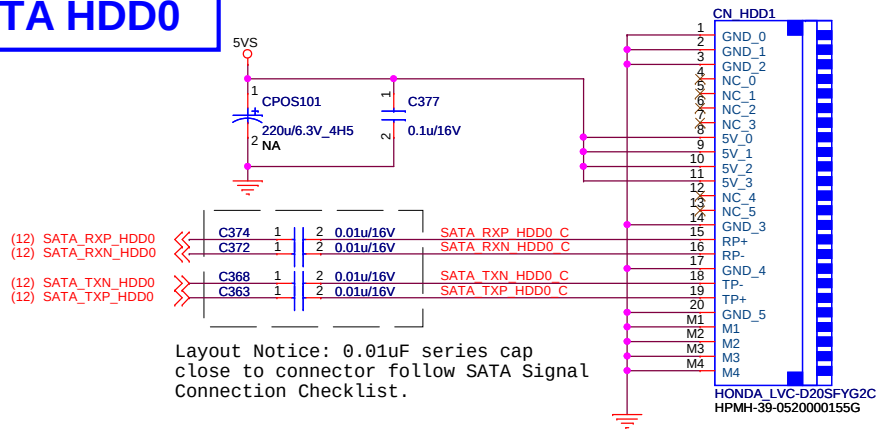
CRT



FLEX Computing

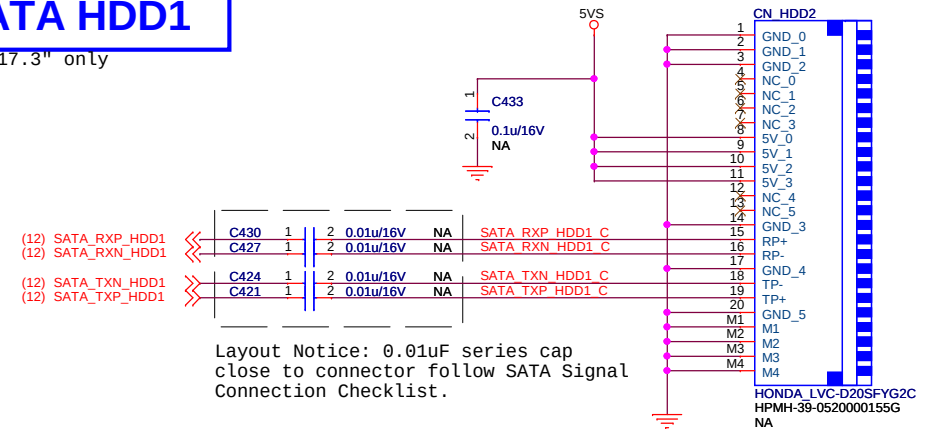
Project Name : H510UA1		Title : D-sub I/F	
Size :	Document Number : HPMH-40GAB6300-D		Rev : D
Date: Thursday, December 30, 2010		Sheet : 26 of 51	

SATA HDD0

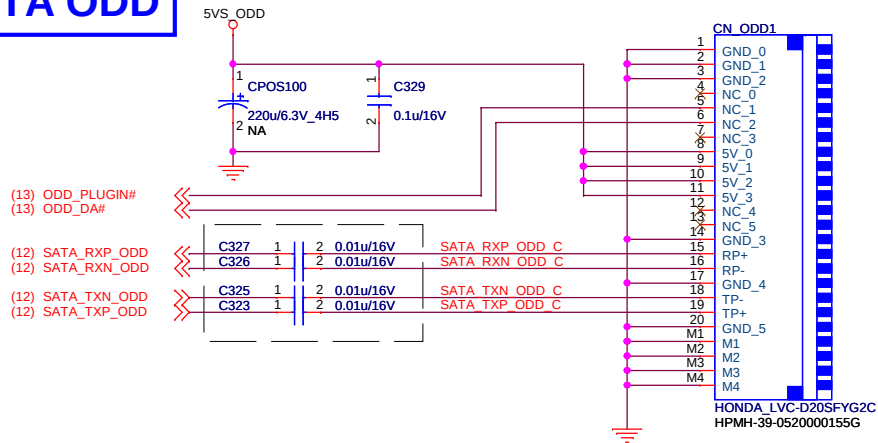


SATA HDD1

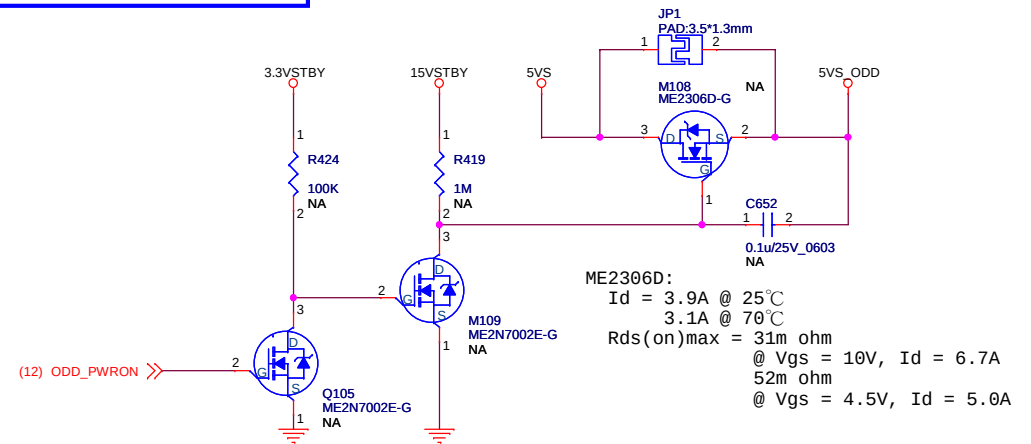
For 17.3" only



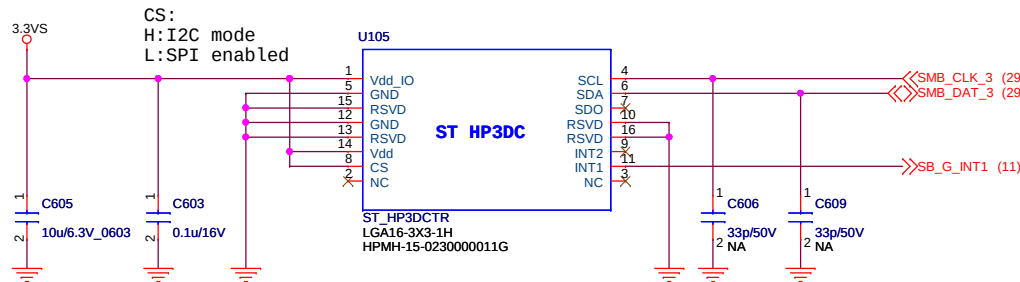
SATA ODD



ODD Zero PWR



G-Sensor



G-SENSOR - ST HP3DC

3.3VS

ADDR: 0001100x(30h) - SDO PD

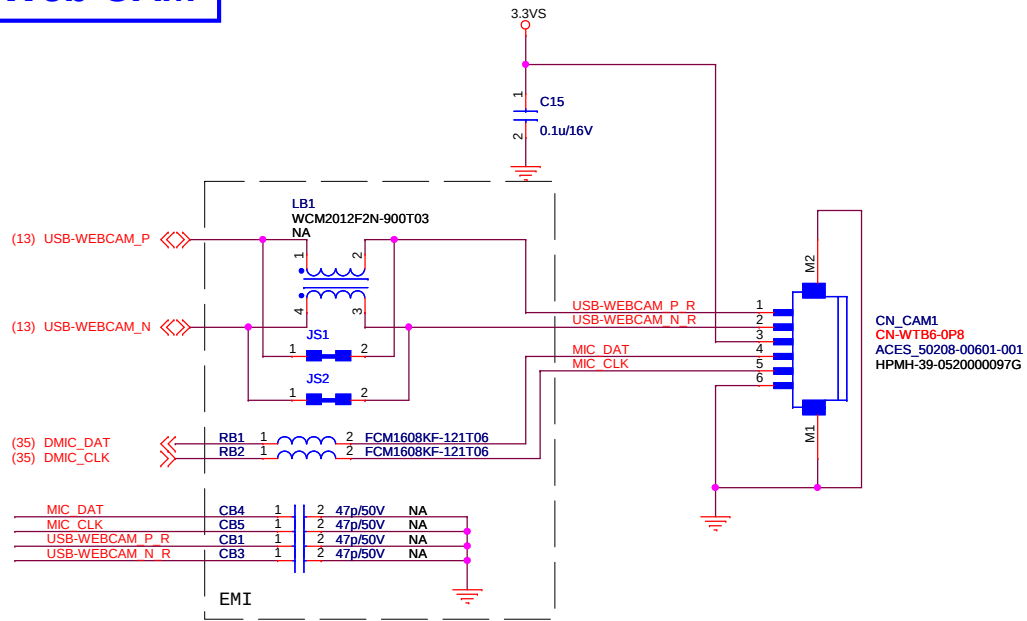
ADDR: 0011101x(32h) - SDO NC

SINK: ?mA@VoL=0.33V(MAX)

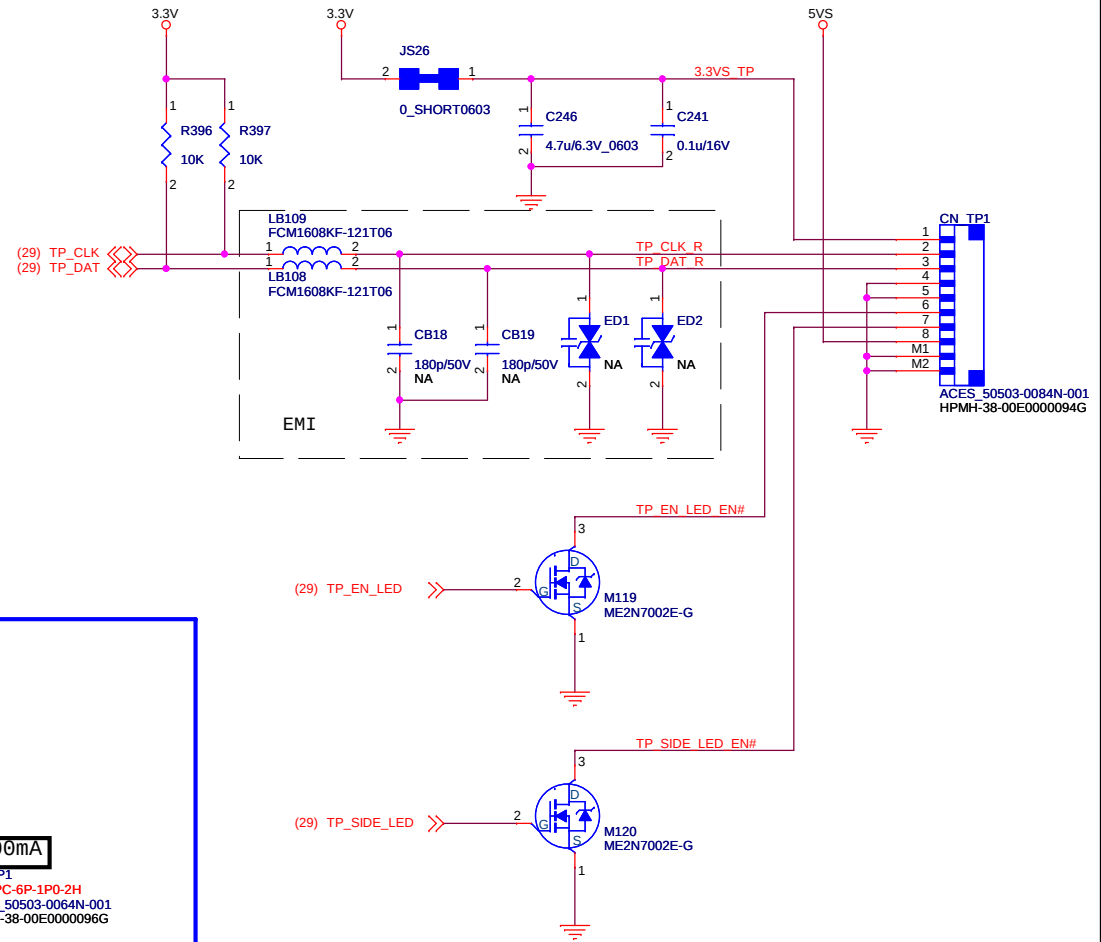
FLEXComputing

Project Name :	H510UA1	Title :	HDD/ ODD/ Zero PWR/ G-sensor
Size :	Document Number :	Rev :	D
Date :	Thursday, December 30, 2010	Sheet :	27 of 51

Web CAM

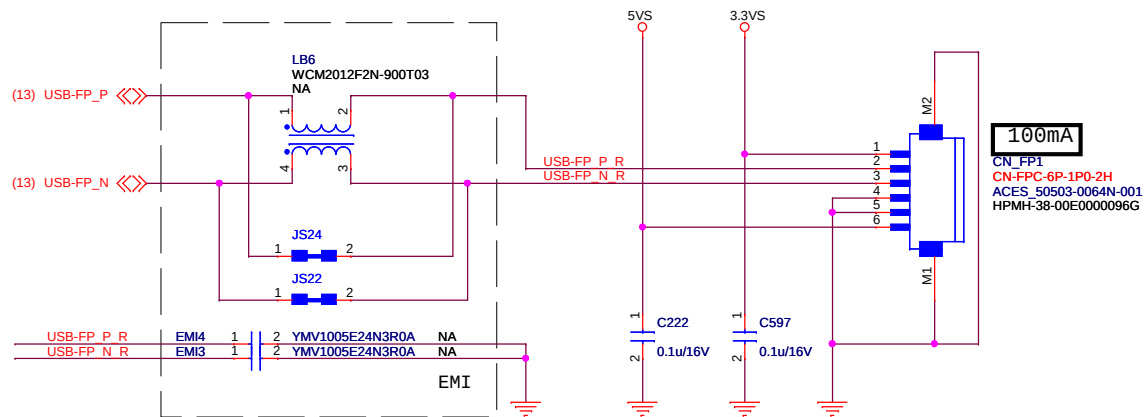


T/P



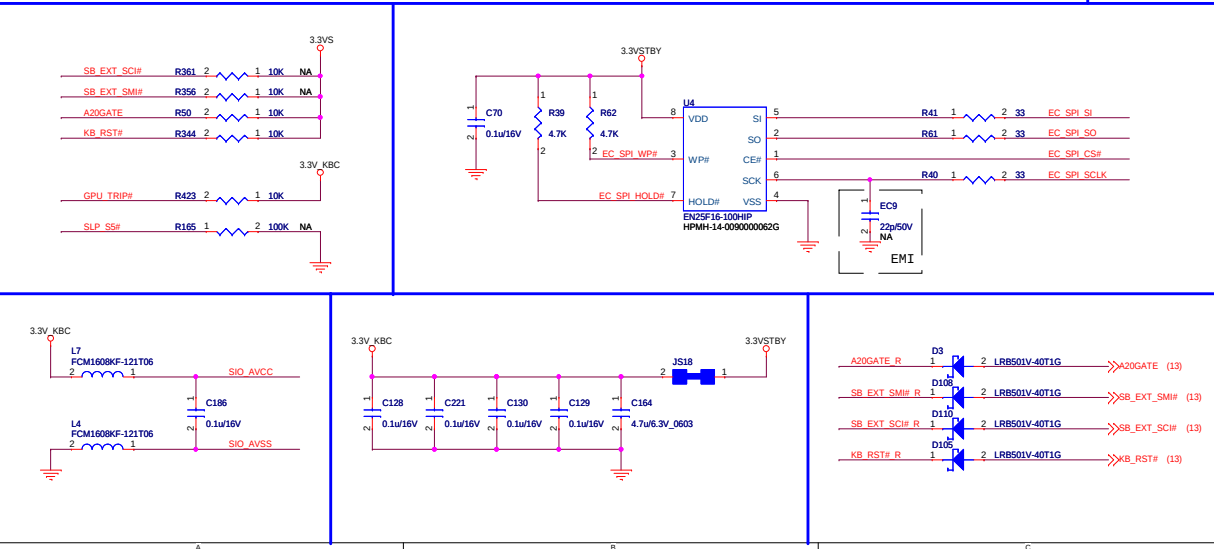
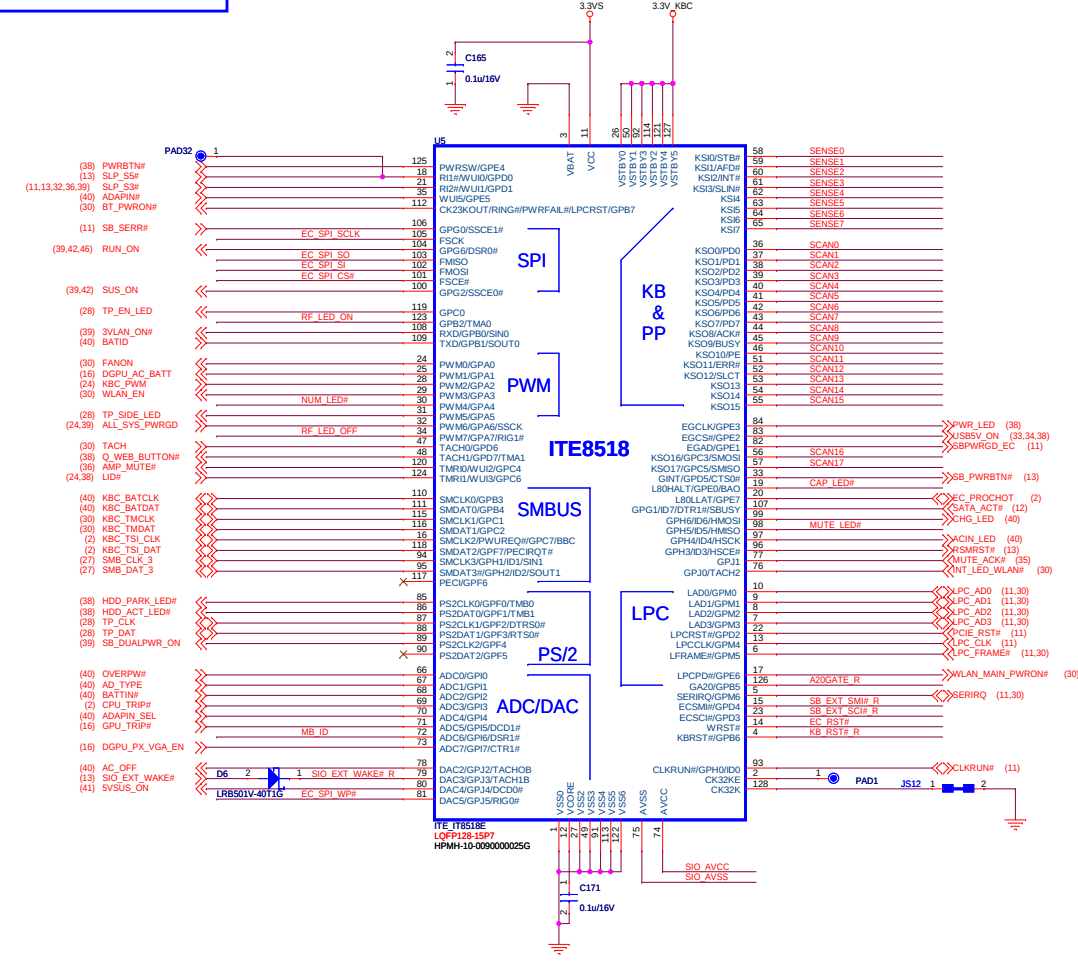
Finger Printer

Remve Finger Printer coponents for IMR

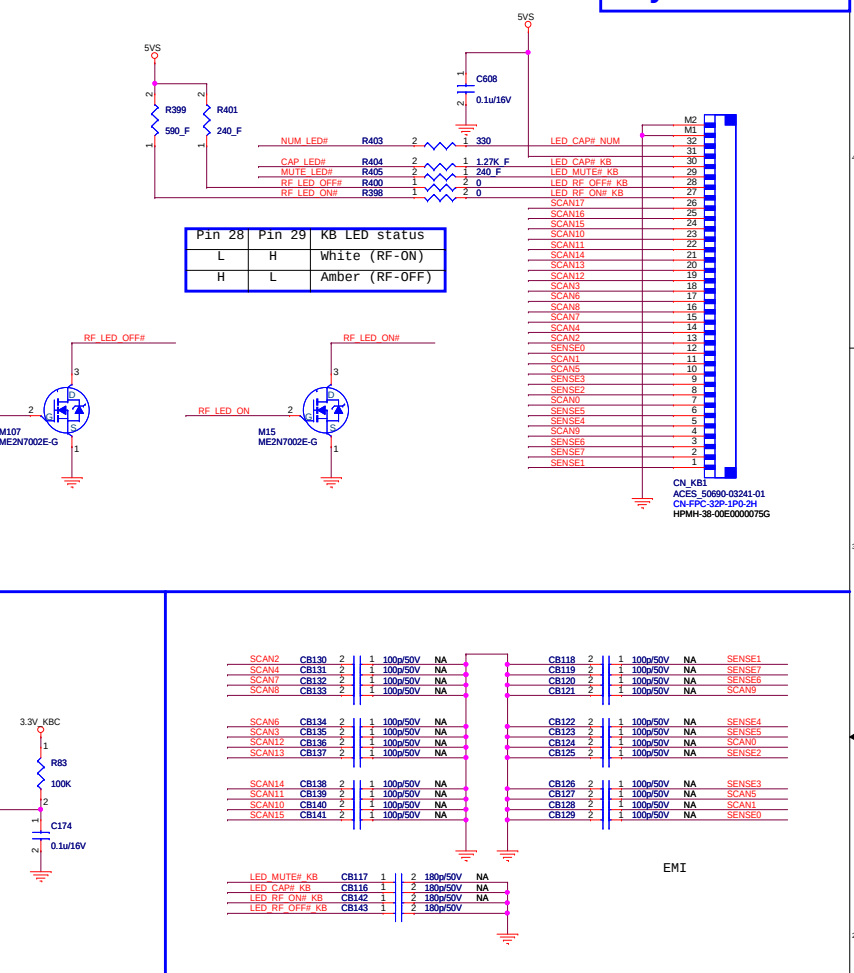


FLEXComputing

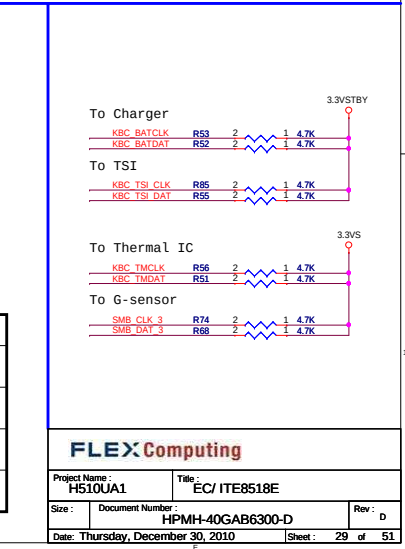
Project Name : H510UA1		Title : WebCAM/ BT/ FPI/ Touch Screen	
Size :	Document Number : HPMH-40GAB6300-D		Rev : D
Date: Thursday, December 30, 2010		Sheet : 28 of 51	

EC/ ITE8518E

Keyboard Conn



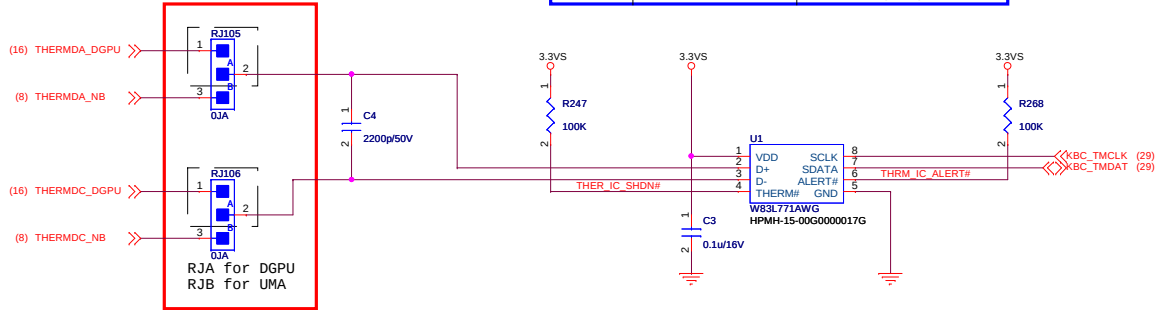
MB-ID		
3.3V	INTEL-DI	R92: 10K -- HPMH-30-301036-990G R104: NA
2.2V	INTEL-UI	R92: 10K -- HPMH-30-301036-990G R104: 20K -- HPMH-30-102036-990G
1.1V	AMD-DA	R92: 20K -- HPMH-30-102036-990G R104: 10K -- HPMH-30-301036-990G
GND	AMD-UA	R92: NA R104: 10K -- HPMH-30-301036-990G



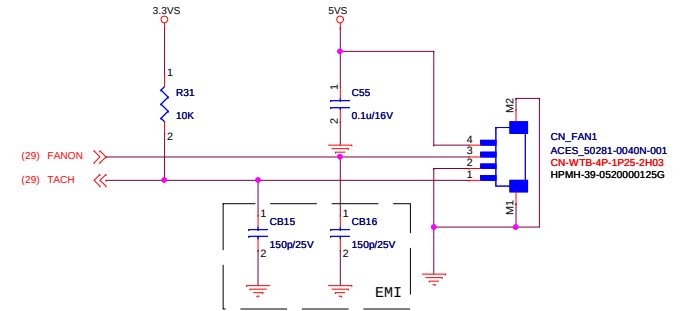
Thermal Sensor

THERMAL IC FOR CPU or DGPU

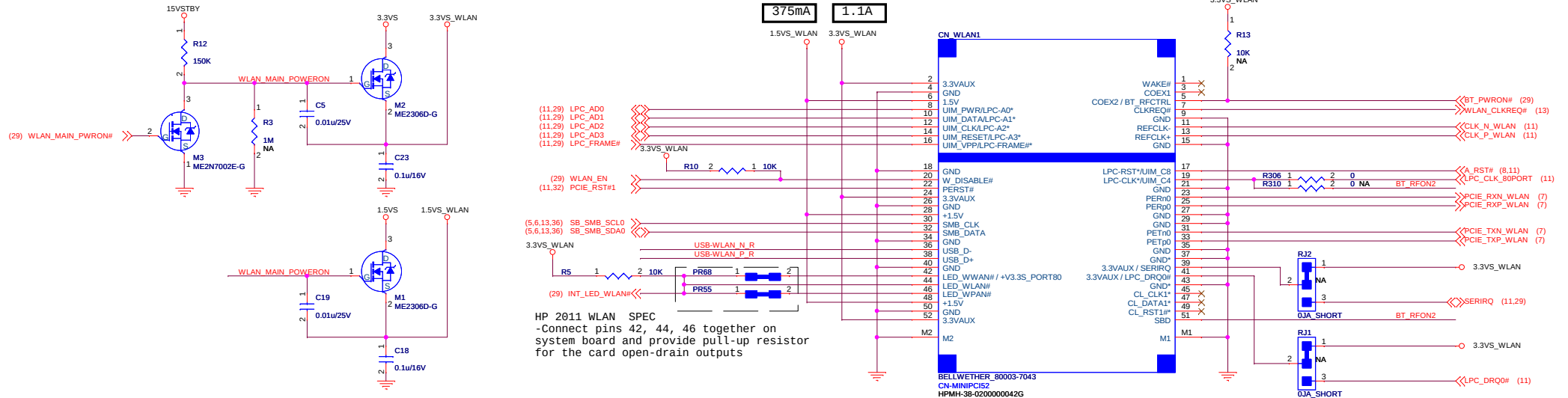
WINBOND	W83L771AWG	HPMH-15-00G0000017G 1001100x(98h)
TI	TMP431ADGKR	HPMH-15-0500000005G 1001100x(98h)



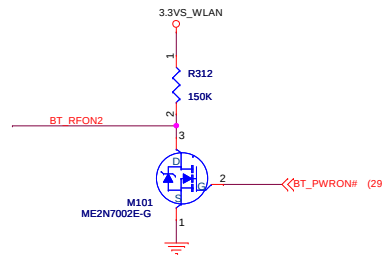
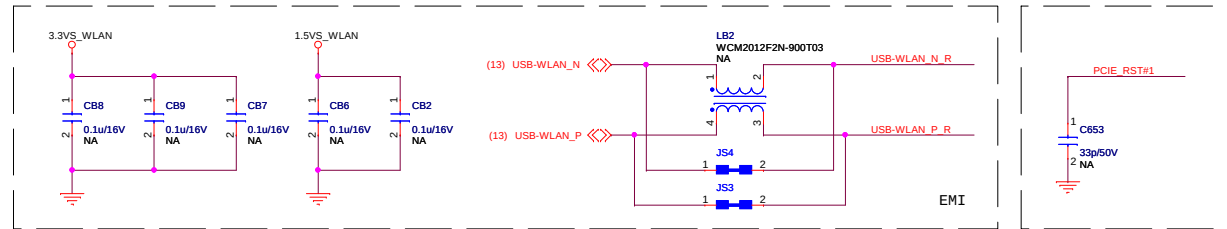
FAN



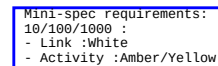
Mini PCI-E - WLAN (Half)



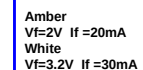
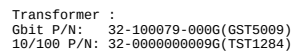
HP 2011 WLAN SPEC
-Connect pins 42, 44 together on system board and provide pull-up resistor for the card open-drain outputs



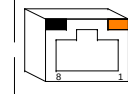
FLEX Computing	
Project Name : H510UA1	Title : Thermal/ FAN/ WLAN/ HP-Logo
Size : Document Number : HPMH-40GAB6300-D	Rev : D
Date : Tuesday, January 11, 2011	Sheet : 30 of 51

GbLAN

LEDS1-0s initial value comes from the EEPROM
if there is no EEPROM, the default value is 11



```
Reference:
RJ45 Phone Jack
Pin    define:
1      TXD+0
2      TXD-0
3      TXD+1
4      TXD+2
5      TXD-2
6      TXD-1
7      TXD+3
8      TXD-3
```



SVTP_v4.03 - 2.6 - Ethernet Checklist - Rev C.xls

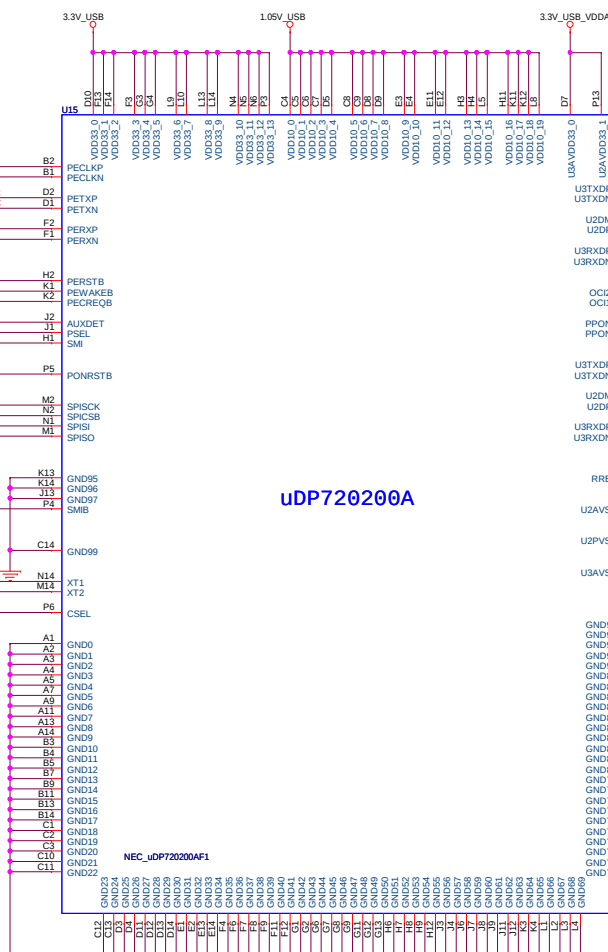
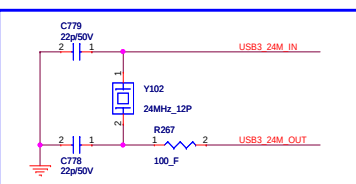
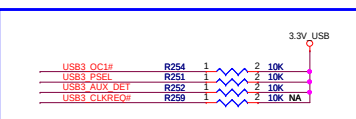
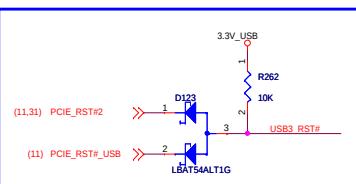
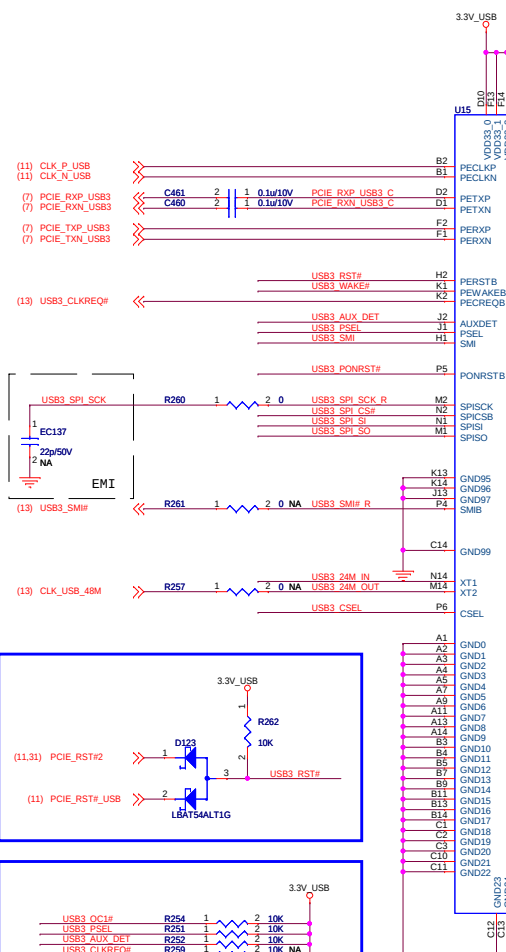
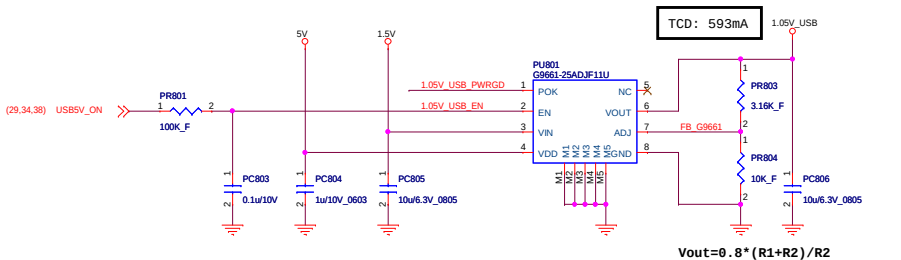
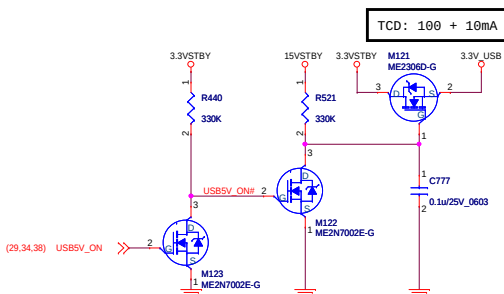
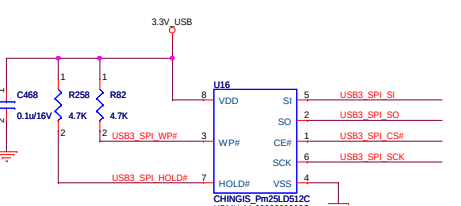
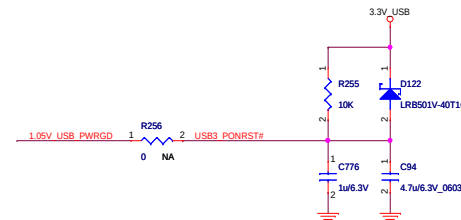
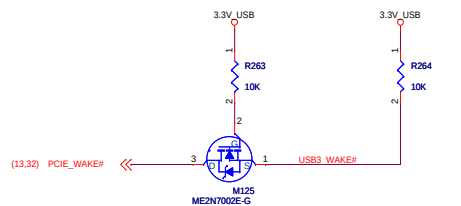
- Ch.3.1.4.4

Some older cheap RJ-45s only populate pins 1,2,3,6.
10/100 requires the other 4 pins for grounding. Gigabit Ethernet requires all 8 pins for data signals.

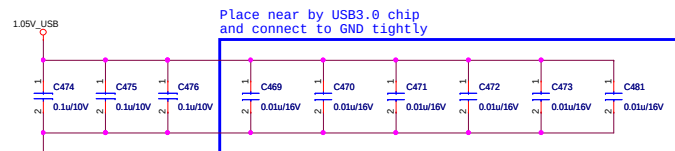
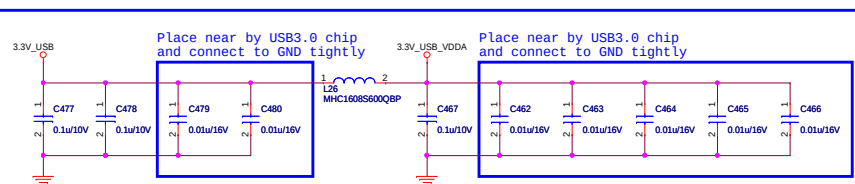
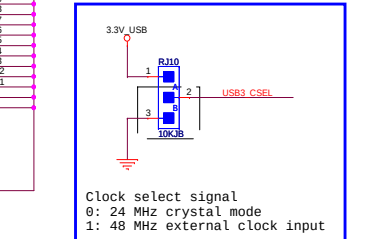
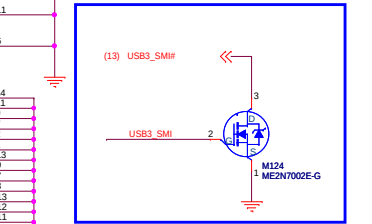
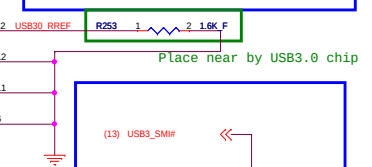
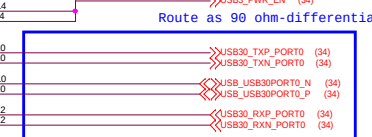
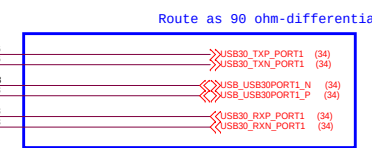
- Ch.3.1.4.13
Resistance from RJ-45 shell to any other chassis ground
point (ohms) less than 1 ohm

- Ch.3.1.4.14 & Ch.3.1.4.15
Protection against non-standard power-over-Ethernet (PoE)
:
Resistance between pins 1,3 (TXD0P,TXD1P) and pins 4,7
(TXD2P,TXD3P) of the RJ-45 greater than 58K ohms.

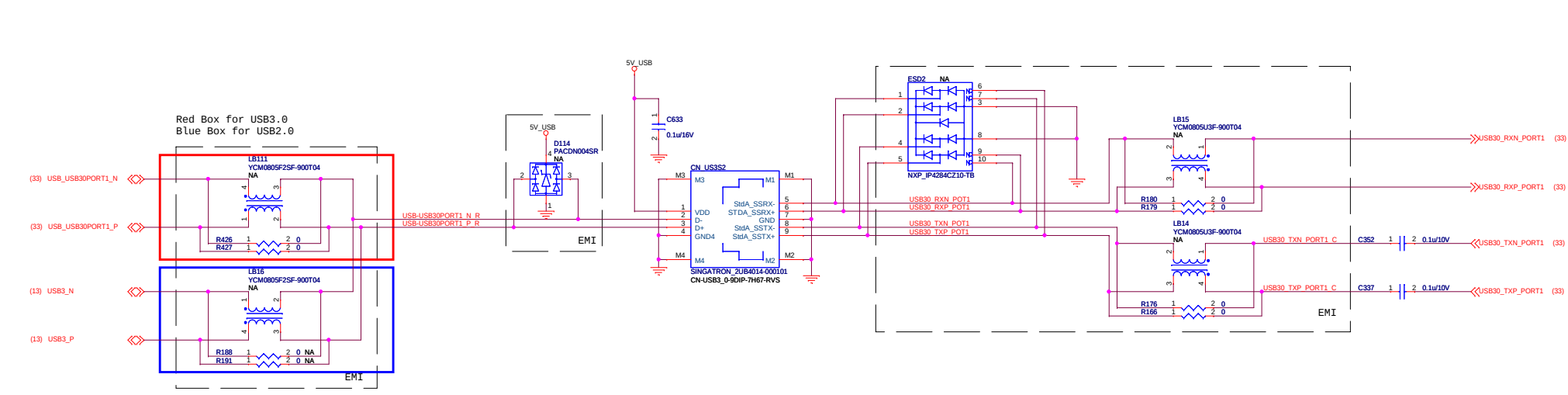
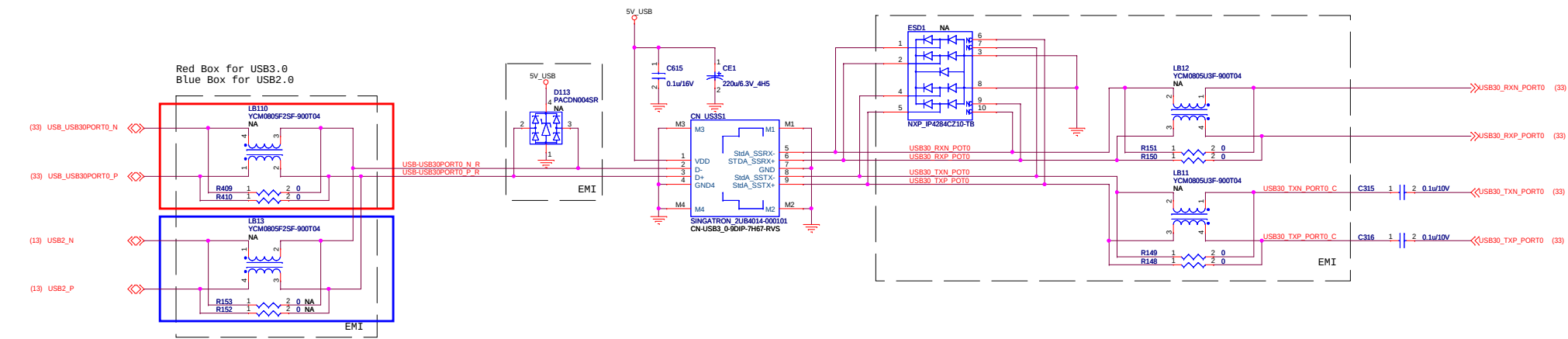
USB3.0 Controller



uDP720200A

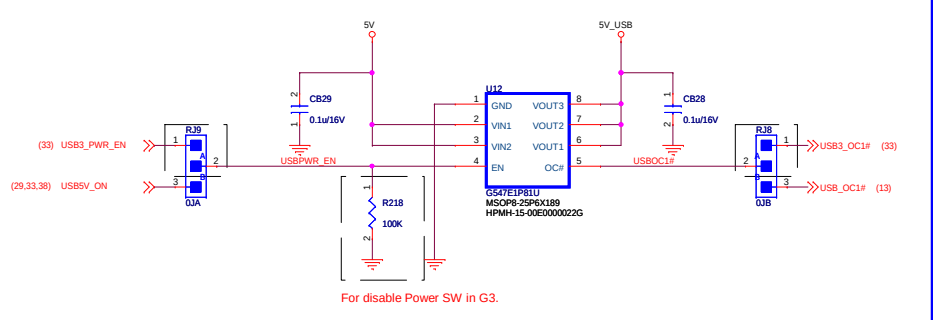


USB 3.0/ 2.0



USB PWR SW

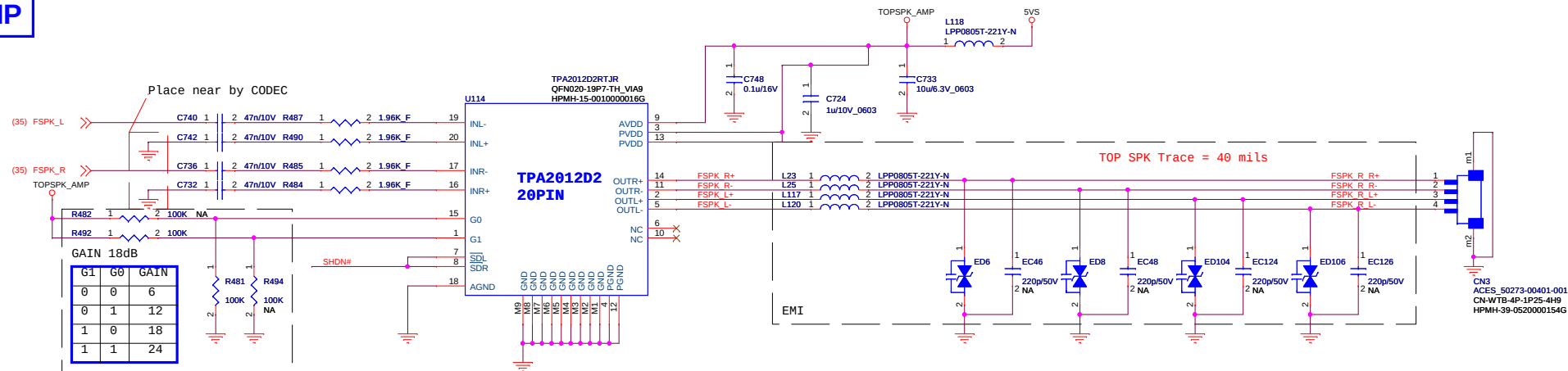
USB 3.0: RJ8& RJ9 mounted A, B.
USB 2.0: RJ8& RJ9 mounted B, B.



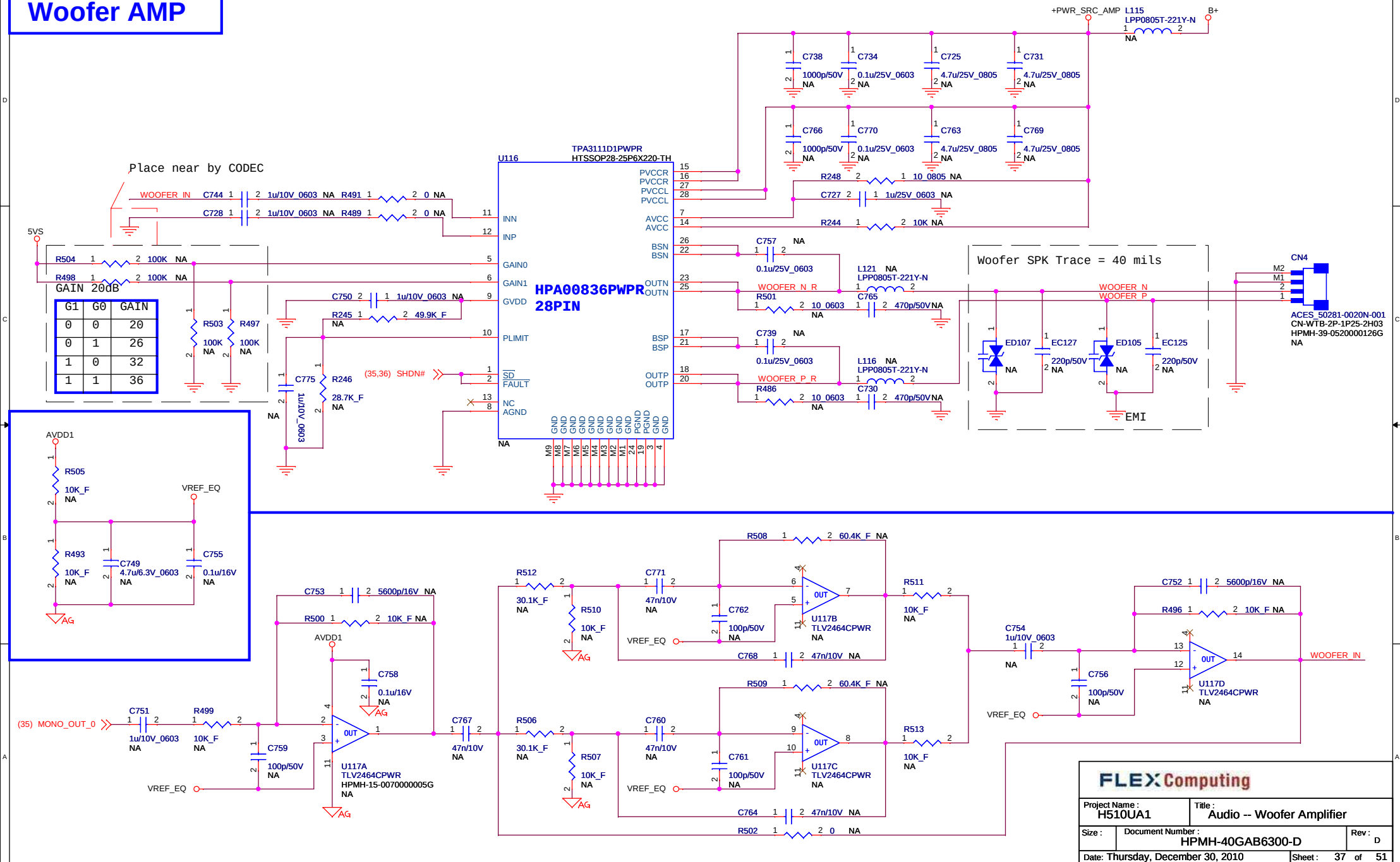
USB3.0 Conn:
HPMH-38-0040000065G -- CONN USB 3.0 9P 2UB4014-000101 SINGATRON
HPMH-38-0040000067G -- CONN USB 3.0 9PIN TARA7-9Y5391 ACON
HPMH-38-0040000068G -- CONN USB 3.0 9P USBF-D9F1-ANR1-00 E-CONN
HPMH-38-0040000088G -- CONN USB3.0 1-1932354-1 9P H:7.4mm

USB2.0 Conn:
HPMH-38-0040000066G -- CONN USB 2.0 4P 2UB4015-000111 SINGATRON
HPMH-38-0040000070G -- CONN USB 2.0 4PIN UARBS-4K5986 ACON
HPMH-38-0040000071G -- CONN USB 2.0 4P USBF-D4F1-ANR1-CA E-CONN

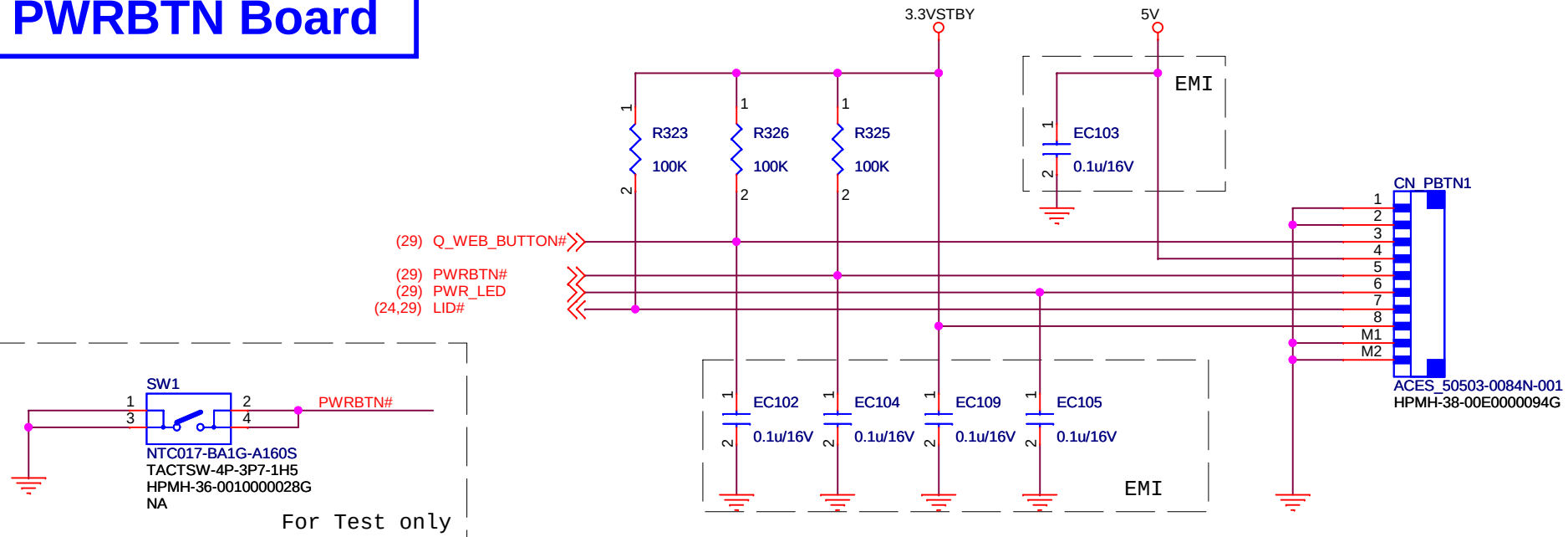
FRONT SPK AMP



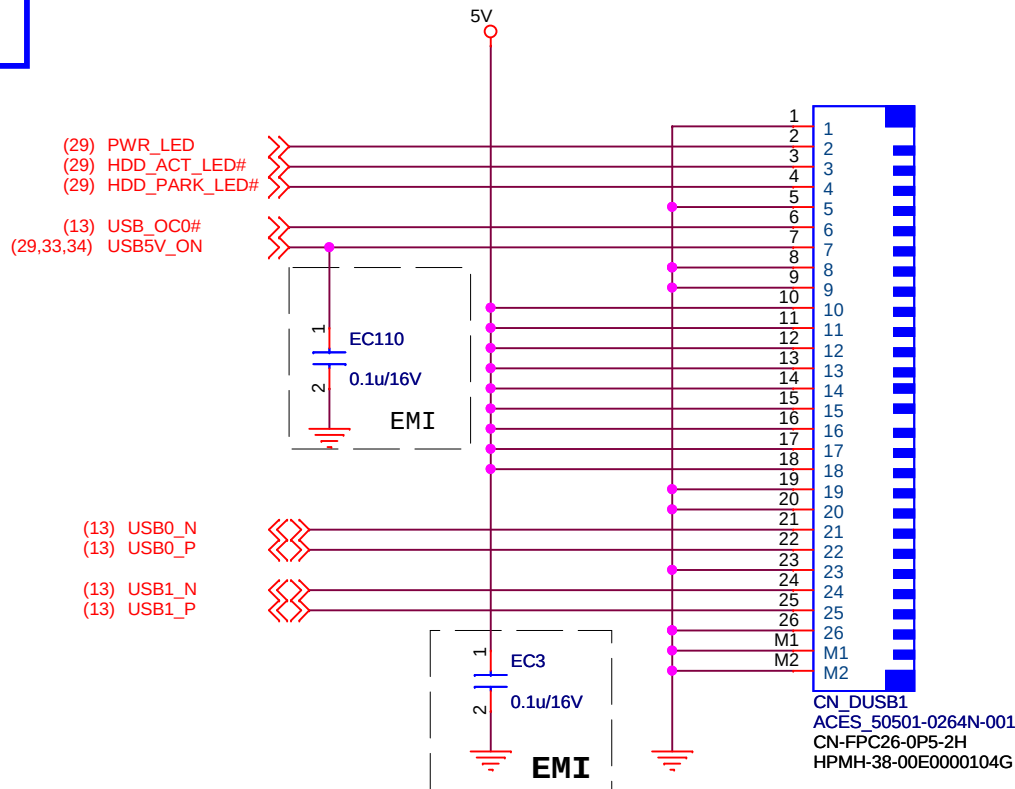
Woofers AMP



PWRBTN Board



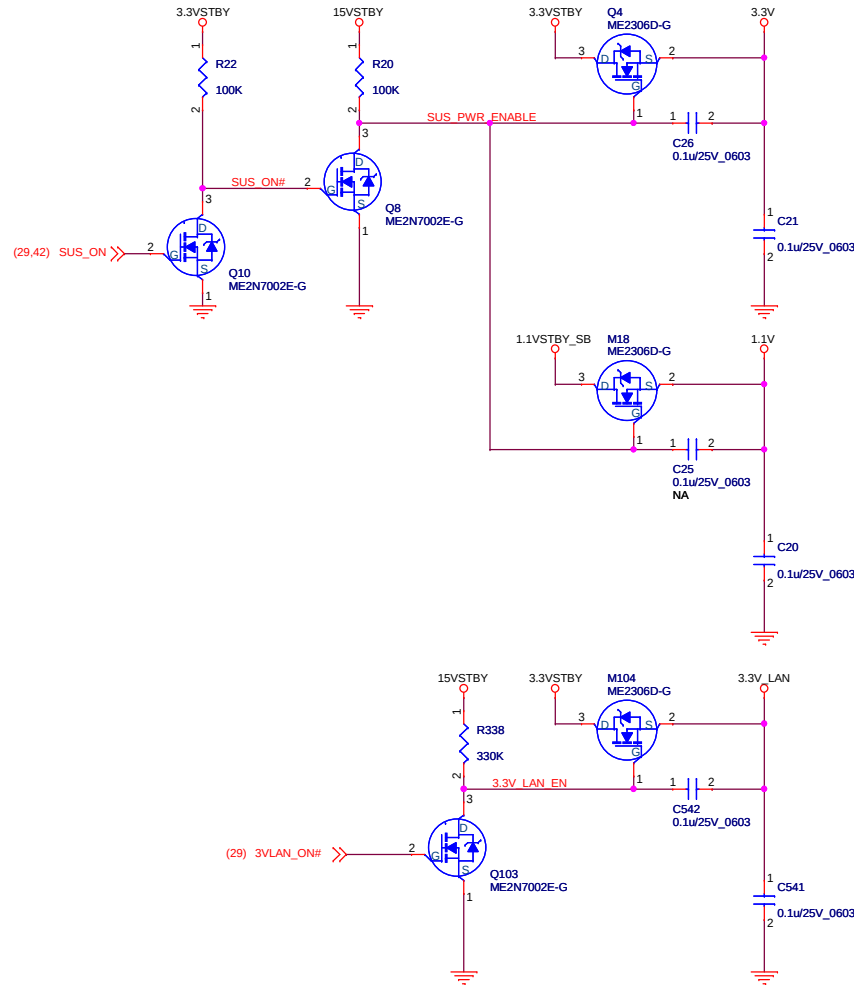
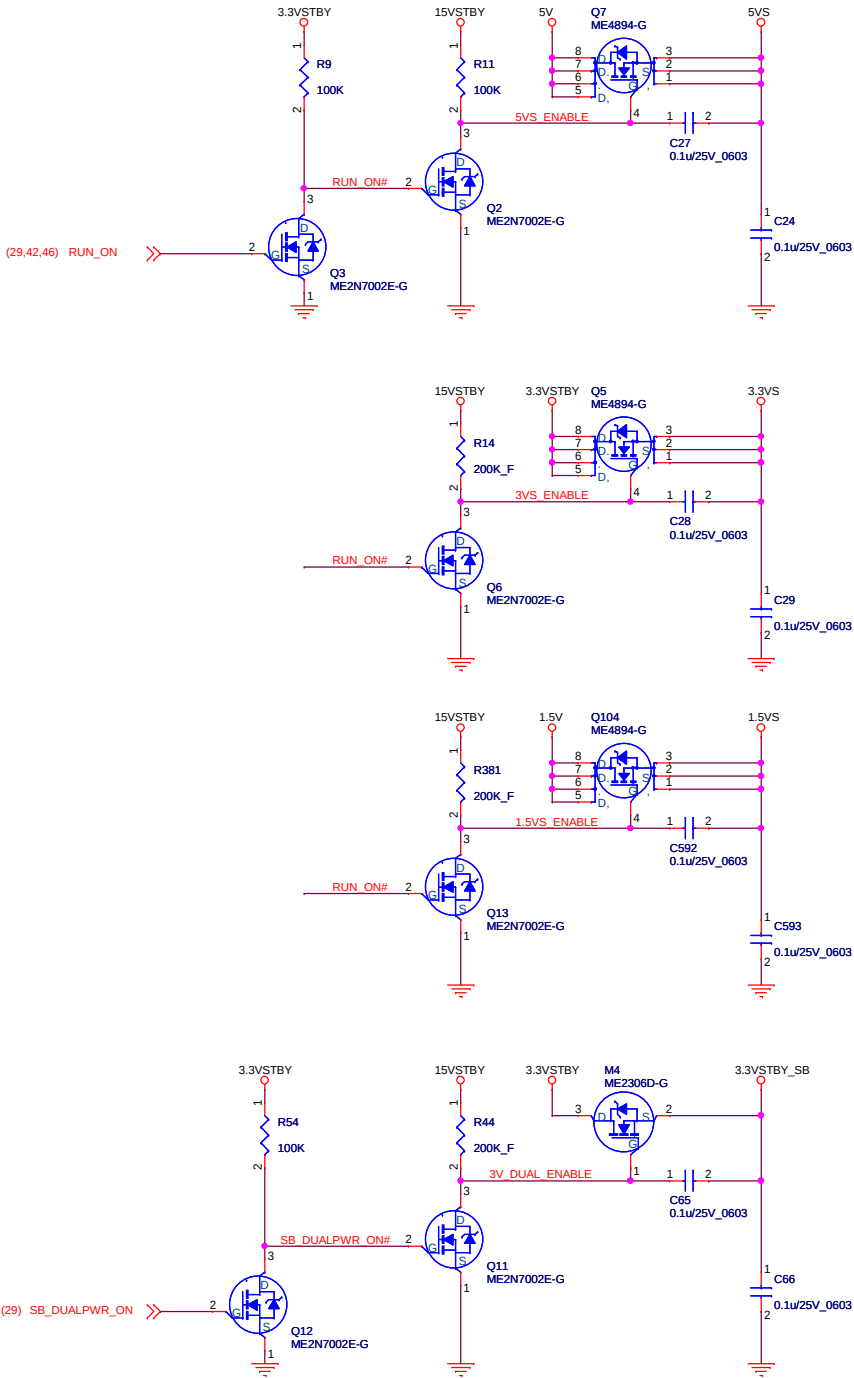
USB Board



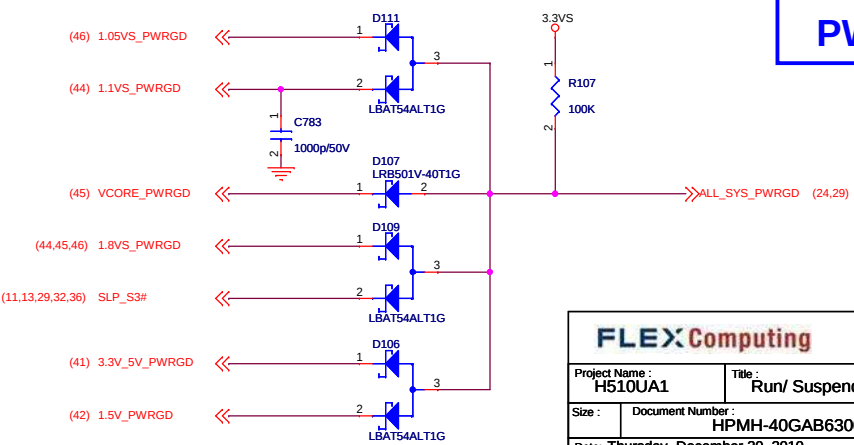
FLEXComputing

Project Name : H510UA1		Title : Daughter Board Connector	
Size :	Document Number : HPMH-40GAB6300-D		Rev : D
Date: Thursday, December 30, 2010		Sheet :	38 of 51

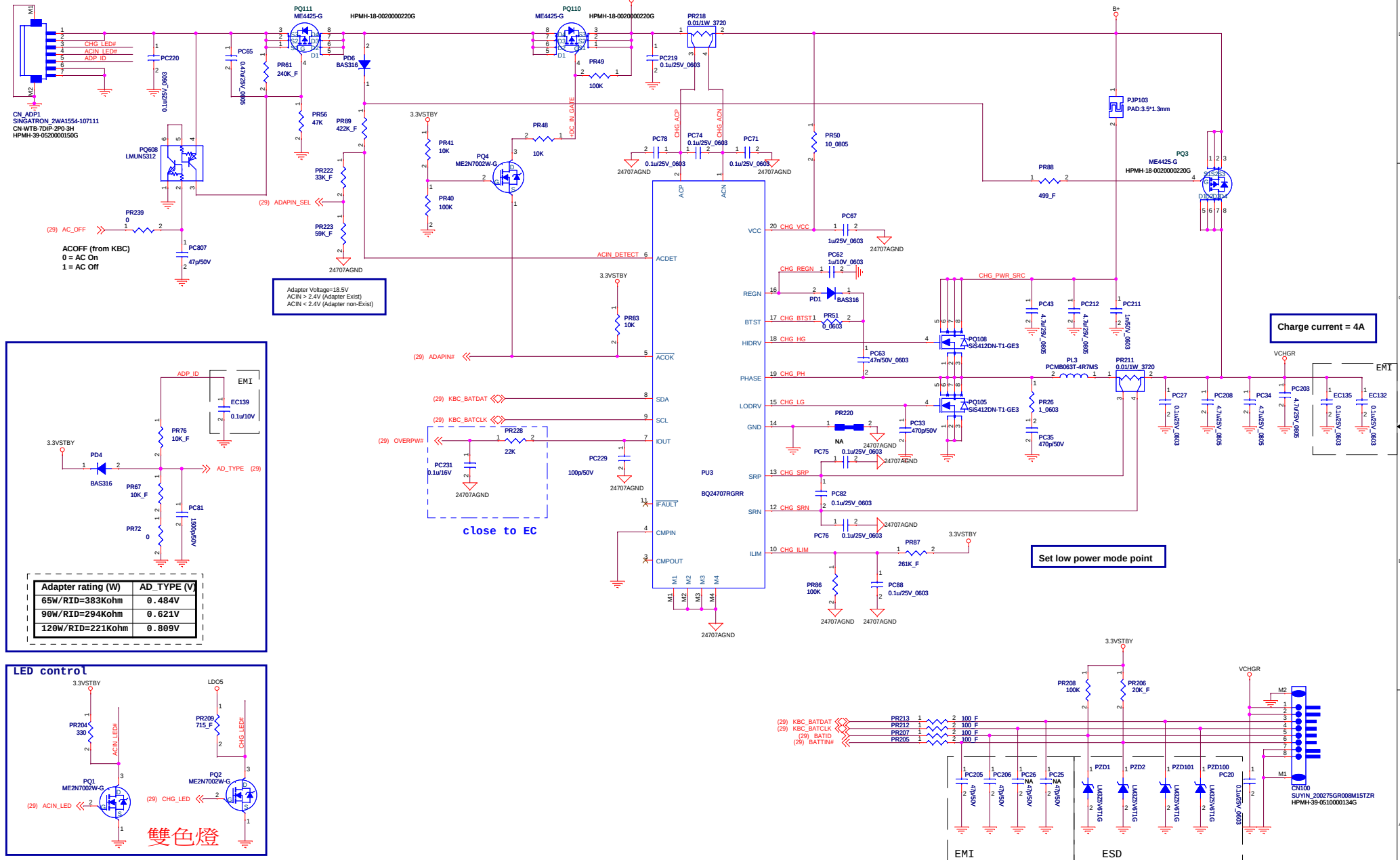
RUN/ SUS PWR



PWRGD



Charger



Adapter rating (W) AD_TYPE (V)

Adapter rating (W)	AD_TYPE (V)
65W/RID=383Kohm	0.484V
90W/RID=294Kohm	0.621V
120W/RID=221Kohm	0.809V

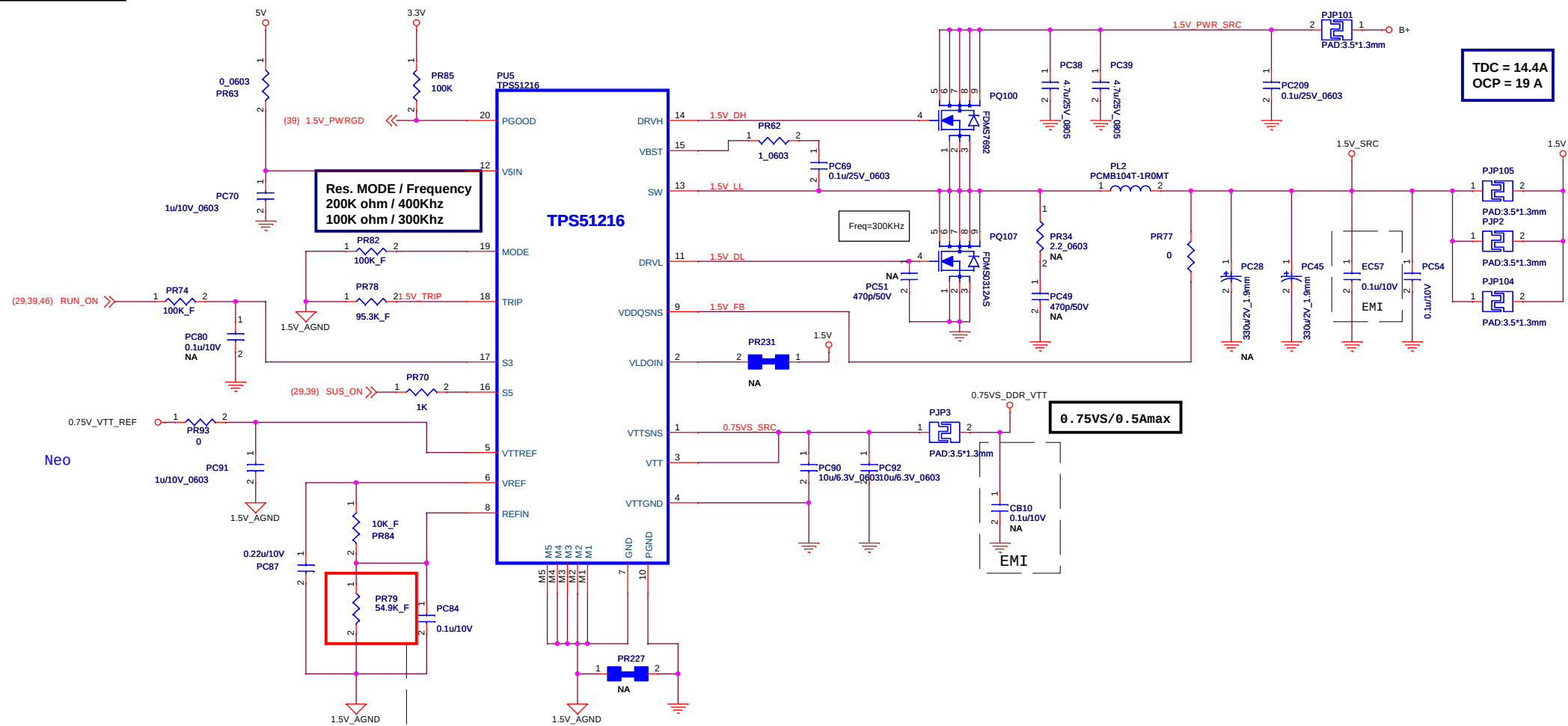
Adapter Voltages: 18.5V
ACIN > 2.4V (Adapter Exist)
ACIN < 2.4V (Adapter non-Exist)

LED control

雙色燈

AirLine Combo	AC available	Charge
2.032V > ADAPIN_SEL > 1.542V	V	X
ADAPIN_SEL > 2.032V	V	V
1.542V > ADAPIN_SEL	X	X

1.5V



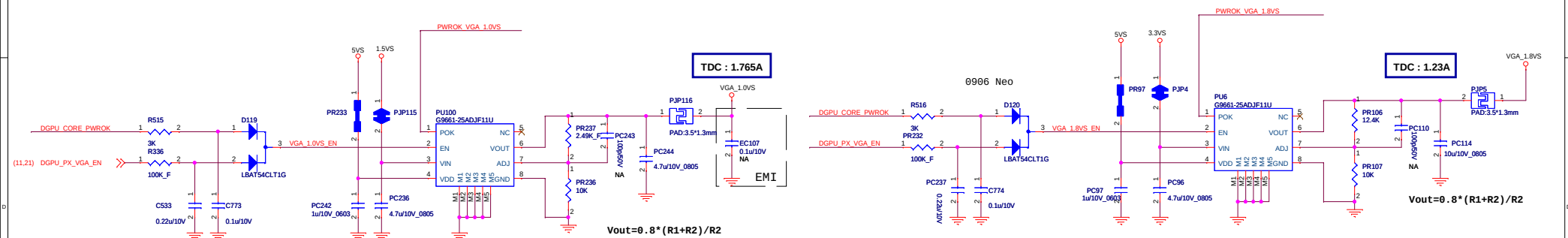
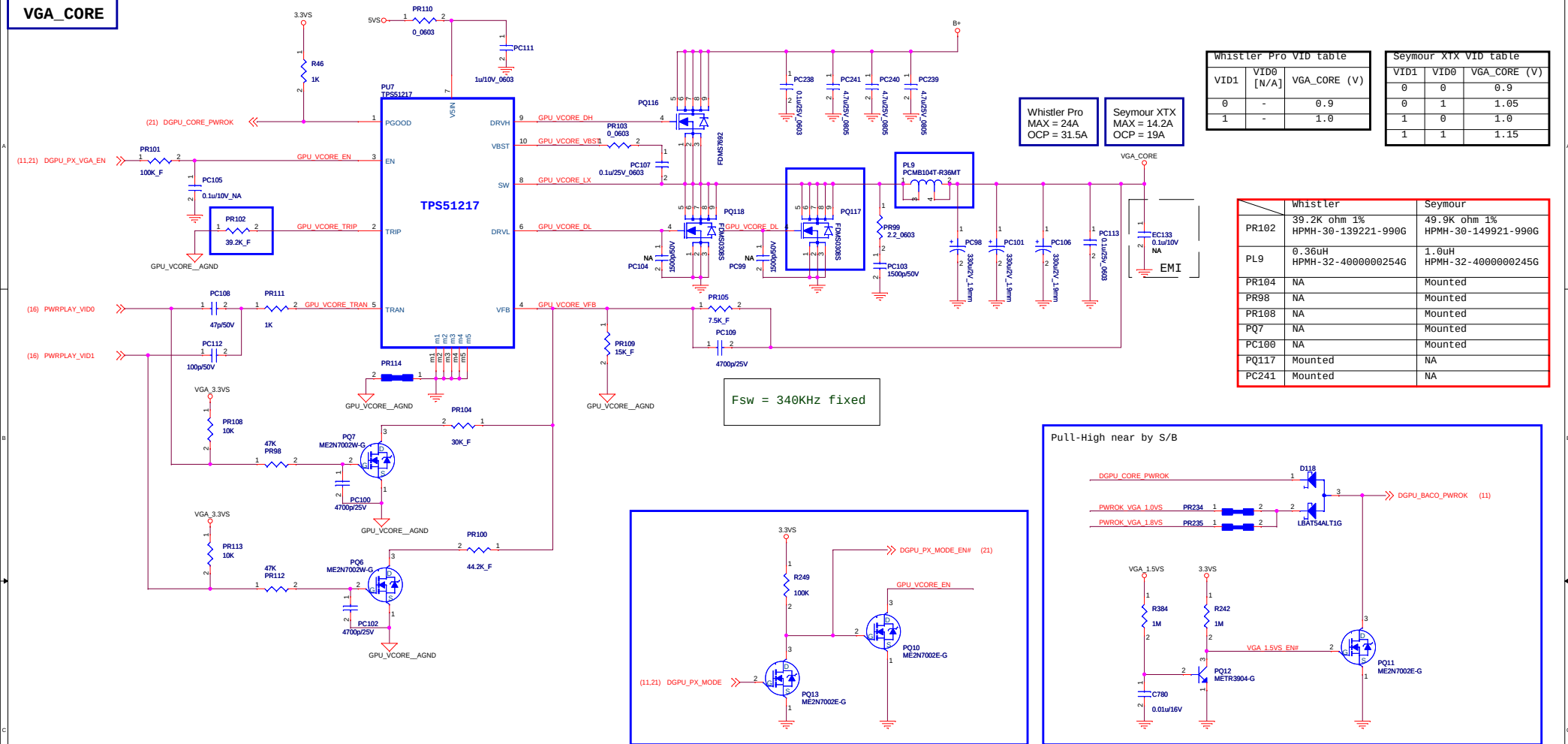
	UMA	Discret
PR79	49.9K ohm 1% HPMH-30-149921-990G	54.9K ohm 1% HPMH-30-154921-990G

Table 1. S3 and S5 Control Table

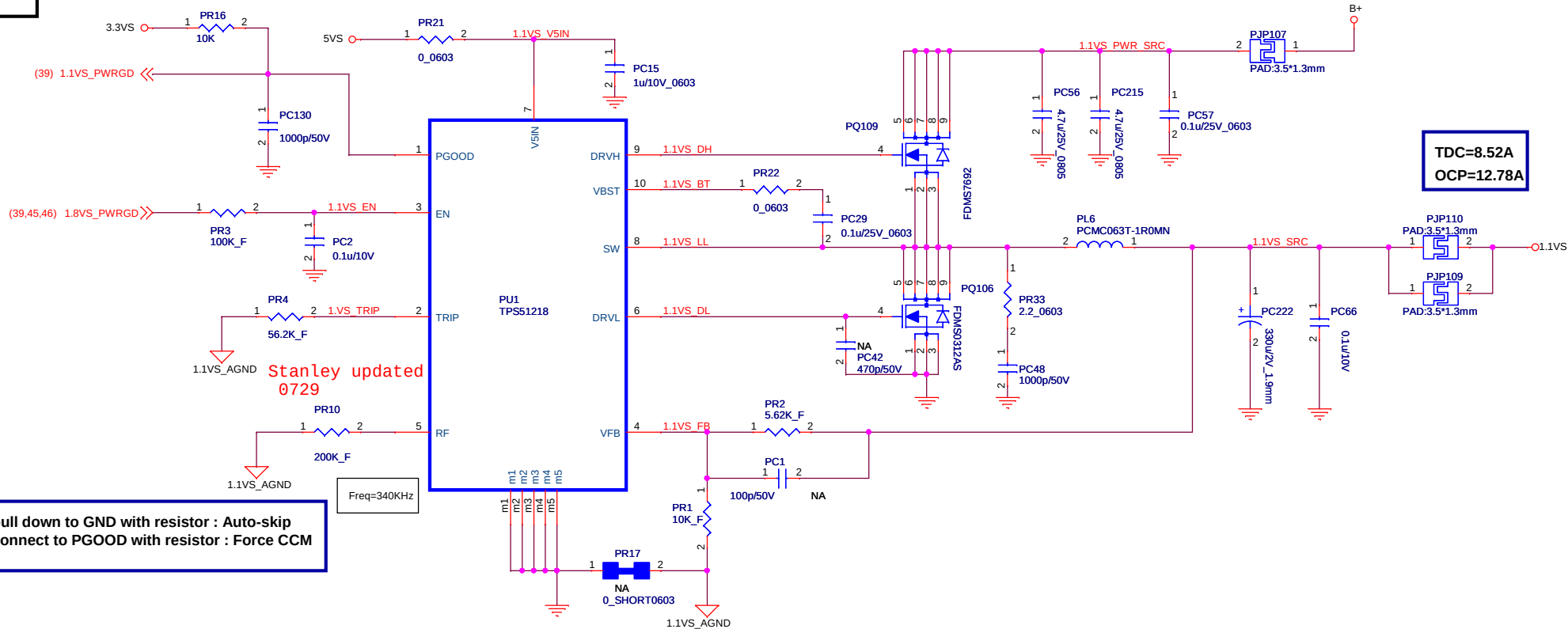
STATE	S3	S5	VTTREF	VTT
S0	H	H	1	1
S3	L	H	1	0 (high-Z)
S4/S5	L	L	0 (discharge)	0 (discharge)

FLEXComputing

Project Name : H510UA1		Title : PWR -- DDR PWR (TPS51216)	
Size :	Document Number :	Rev : D	
Date: Thursday, December 30, 2010		Sheet : 42 of 51	

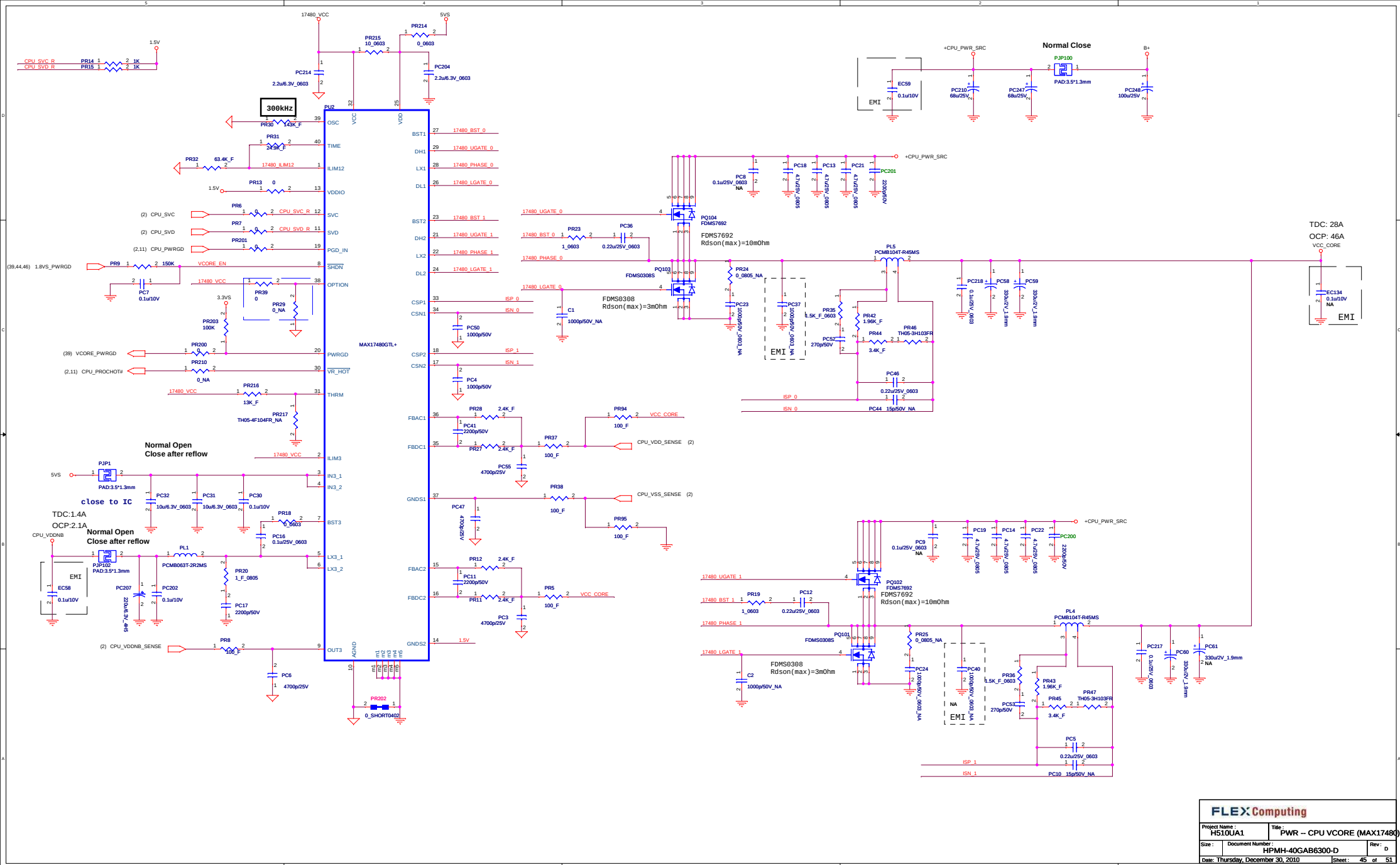
VGA_CORE

1.1VS

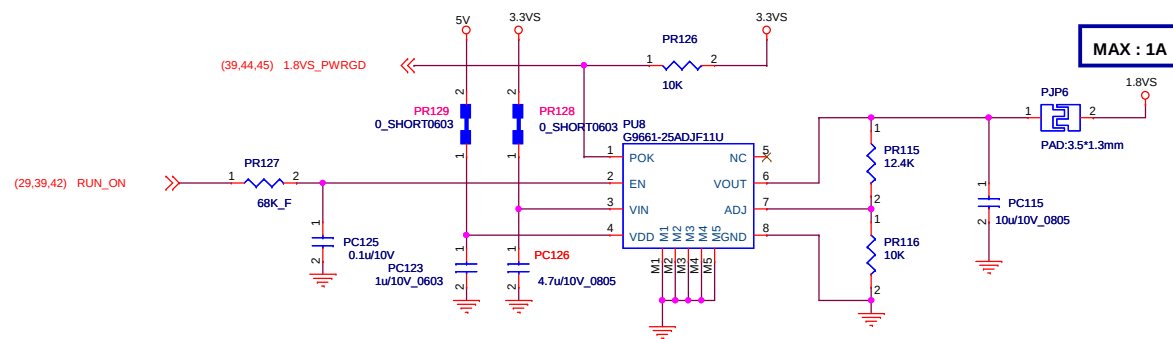


FLEX Computing

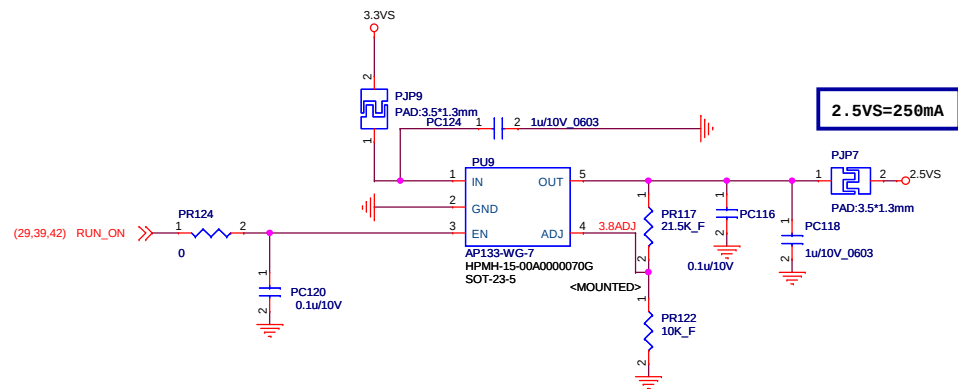
Project Name : H510UA1		Title : PWR -- 1.1VS (TPS51218)	
Size :	Document Number : HPMH-40GAB6300-D		Rev : D
Date: Thursday, December 30, 2010		Sheet :	44 of 51



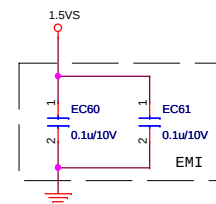
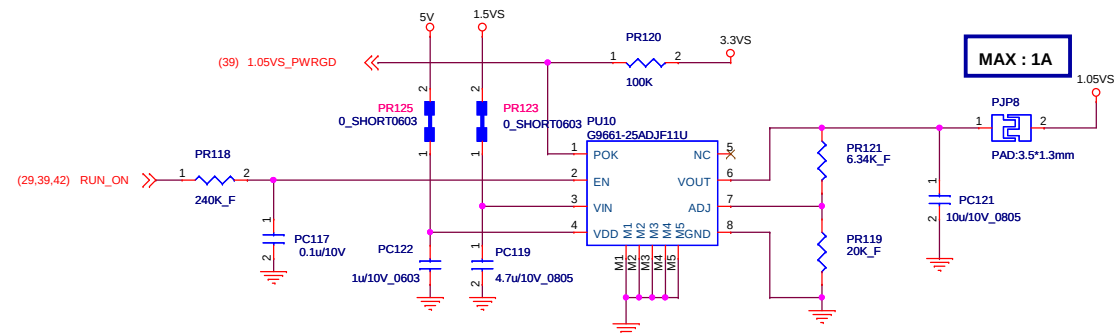
1.8VS



2.5VS



1.05VS

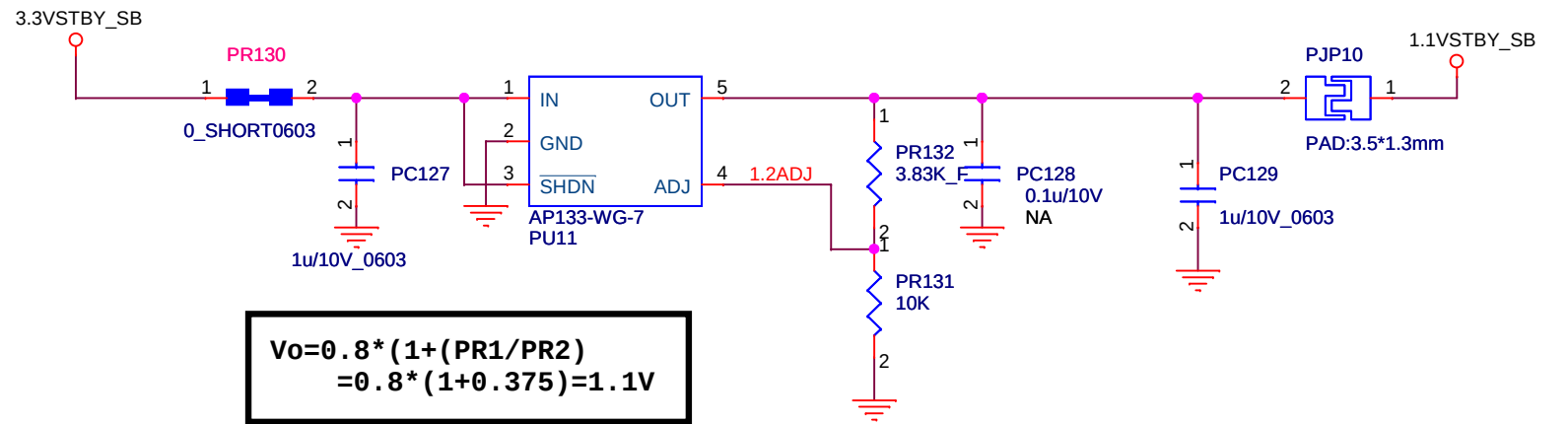


AP133:
Low dropout: 350mV at 300mA
EN logic low: <0.4V
EN logic high: >1.4V
Thermal shutdown: 145'C

FLEXComputing

Project Name : H510UA1		Title : PWR -- 1.8VS/ 1.05VS/ 2.5VS	
Size :	Document Number : HPMH-40GAB6300-D	Rev : D	
Date: Thursday, December 30, 2010		Sheet :	46 of 51

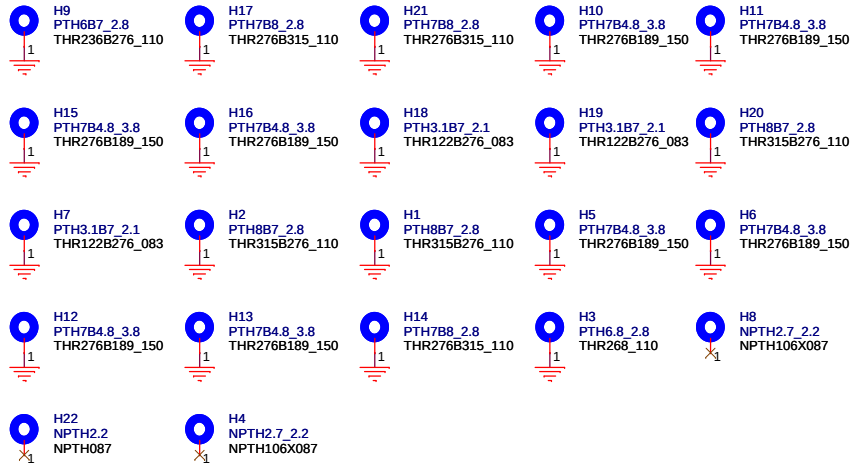
1.1VSTBY



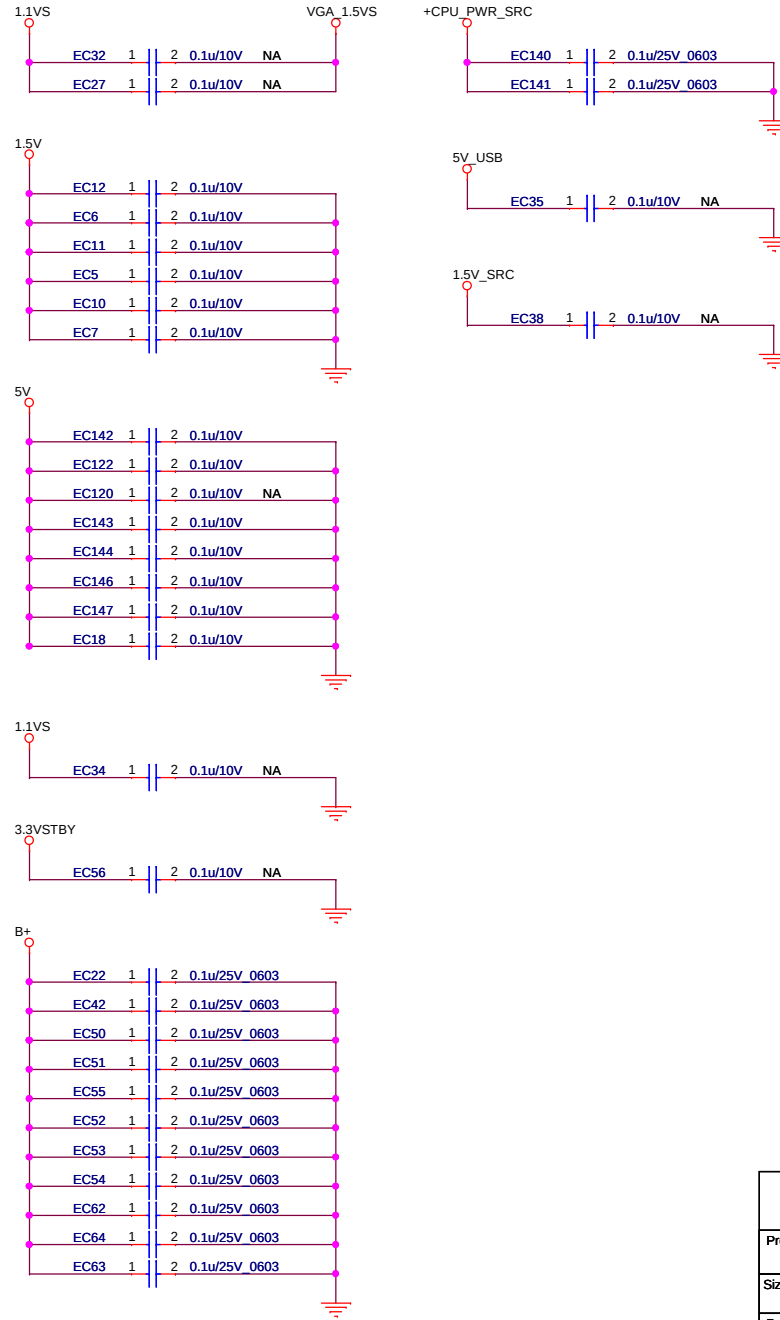
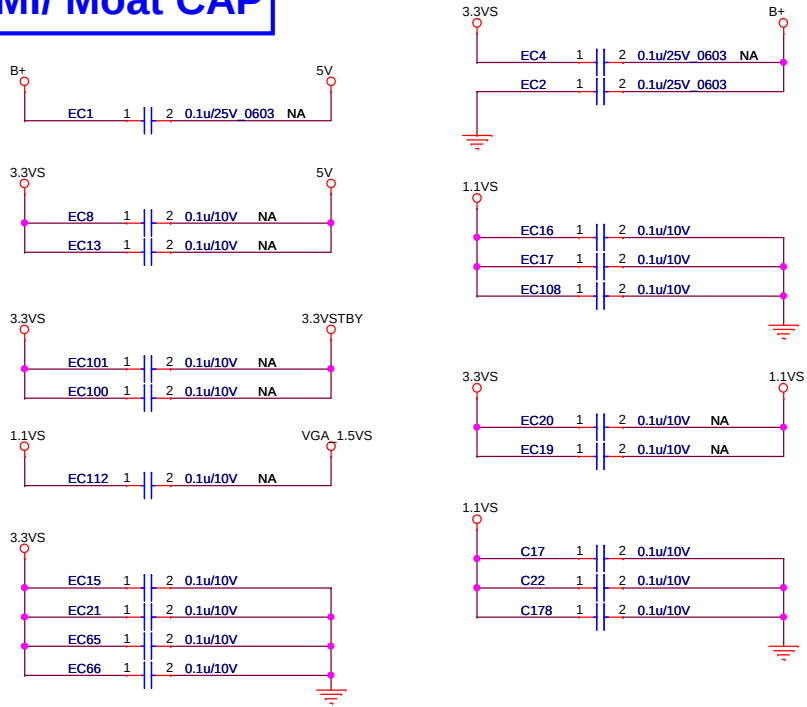
FLEXComputing

Project Name : H510UA1		Title : PWR -- 1.1VSTBY_SB (AP133)	
Size :	Document Number : HPMH-40GAB6300-D		Rev : D
Date: Thursday, December 30, 2010		Sheet :	47 of 51

Screw Hole



EMI/ Moat CAP



FID

FID1	FIDUCIAL	CAD-016
	1	NC, NO CONNECT TO ANY.
FID2	FIDUCIAL	CAD-016
	1	NC, NO CONNECT TO ANY.
FID3	FIDUCIAL	CAD-016
	1	NC, NO CONNECT TO ANY.
FID4	FIDUCIAL	CAD-016
	1	NC, NO CONNECT TO ANY.
FID5	FIDUCIAL	CAD-016
	1	NC, NO CONNECT TO ANY.
FID6	FIDUCIAL	CAD-016
	1	NC, NO CONNECT TO ANY.
FID7	FIDUCIAL	CAD-016
	1	NC, NO CONNECT TO ANY.
FID8	FIDUCIAL	CAD-016
	1	NC, NO CONNECT TO ANY.

FLEXComputing

Project Name : H510UA1		Title : Screw Hole/ EMI/ Unused	
Size :	Document Number :	Rev : D	
Date: Thursday, December 30, 2010		Sheet : 48 of 51	

Version change list (P.I.R. List)

Page 1 of 3

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phase
1	Rev. A Schematic released	Rev. A Schematic released	A			A0	DB
2	Modify F1 to smaller package	Modify F1 to smaller package	B	26	Modify F1 package to "FUSE-3L4X1W8X1H".	B0	SI
3	Add resistor for CPU test point resistor.	Add resistor for CPU test point resistor.	B	2	Add R514 for 80.6 ohm.	B0	SI
4	Add thermal sensor for NB thermal diode	Prevent N/B thermal break down	B	8, 30	Add RJ105, RJ106 and C772 to seperate DGPU& NB thermal signal.	B0	SI
5	Add DGPU CRT DDC source	Add DGPU CRT DDC channel for DDC6	B	16	Add U104 DDC channel test PAD (P27, P26) of pin AJ30, AJ31 (DDC6)	B0	SI
6	Modify CRT damping components.	Improve re-work performance	B	26	Modify JS102, JS103, JS104, JS7, JS9, JS10, JS11 to R233, R234, R235, R236, R237, R238, R239	B0	SI
7	Shift LAN transformer pin signal	Correct LAN transformer pin-out	B	32	Shift U107 pin-out to meet transformer spec	B0	SI
8	Update LAN 25M net-name	Correct LAN 25M for reserved signal.	B	32	Modify LAN 25M clock from S/B and named "LAN_25M_IN_SB"	B0	SI
9	Modify USB3.0 clock request signal	Modify USB3.0 clock request signal	B	33	Delete D7 for USB 3.0 clock request work properly	B0	SI
10	Reduce CPU/ DGPU screw hole size	To meet BGA& Screw hole keeping 3mm.	B	48	Reduce H5, H6, H12, H3 (CPU), H10, H11, H15, H16 (DGPU) to 7B4.8 3.8 mm	B0	SI
11	Prevent leakage current& fine-tune PWR seq	Prevent leakage current& fine-tune PWR seq	B	34, 39, 44, 45, 46	1. Modify R423 pin 1 to 3.3VSTBY 2. Leave C25 as empty for 1.1V seq 3. Modify R44 to 200K ohm 1% for 3.3VSTBY_SB seq. 4. Add R240, R241 for waveform improve 5. Add R519, R520 to Audio SM bus reserved. 6. Modify PR118 to 240Kohm 1% for 1.05VS seq. 7. Modify PR126 to 10Kohm for 1.8VS seq. 8. Modify PR9 to 150Kohm 1% for VCORE seq. 9. Modify PR3 to 100Kohm 1% for 1.1VS seq. 10. Del R82	B0	SI
12	Remove un-used circuit	Remove function by HP requirement	B		Remove Blue tooth& Keyboard bakclight circuit	B0	SI
13	Add KBC External Wake up event	Add KBC External Wake up event	B	13, 29	Add D6 and make link "SIO_EXT_WAKE#" from U5 pin 117 to U111 pin H3.	B0	SI
14	Modify components by ME/ height limitation	Modify components by ME/ height limitation	B	11, 28, 35, 37	1. Modify CN_RTC1 to ACES - "50273-0020N", CN2 to ACES - "50273-0020N", CN4 to ACES - "50281-00201", CN_LVDS1 to ACES "50398-04001" 2. Add M119, M120 for TP EN LED& TP Sidelight LED sinker.	B0	SI
15	Modify DGPU power sequence& BACO circuit	To meet DGPU power sequence& BACO required.	B	11, 21, 43	1. Modify U111 pin AH6 as "DGPU_PX_VGA_EN" 2. Modify PR238 to 620K ohm 1%. 3. Add R243, Q14, PQ121, PC246 for VGA 3.3VS gating circuit. 4. Modify VGA 1.5VS enable signal from DGPU_PX_EN to DGPU_PX_VGA_EN. 5. Delete D6 and connect DGPU_PX_MODE to BACO circuit as enable 6. Add D118, D119, D120, PR240, R249, R515, R516, C773, C774, PC130, PQ10, PQ11, PQ12, PQ13 for VGA PWR Seq. 7. Add JP3, JP4 for BACO mode reserved. 8. Add D121, R250, PQ9, PQ11, PQ12, R242 for DGPU_BACO PWROK seq. 9. Modify DGPU_PERST# from DGPU_PX_GPI00 and PCIE_RST# combined. Or shorted by RJ100B from DGPU_GPI00. 10. Modify entire 3.3VS of DGPU to VGA 3.3VS. 11. Update PCIE_RST#0 reset source.	B0	SI
16	DFB update	DFB update improvement (Factory)	B	26	Modify D101 to 1N5819HW-7-F.	B0	SI
17	X'tal accuracy modify	X'tal accuracy modify	B	11	1. Modify C704, C719 to 27pF for 32.768M Hz	B0	SI
18	Seperate PCI_WAKE# from different power source	Seperate PCI_WAKE# from different power source	B	11	Add D123, R200 and pull-high to 3.3V_LAN	B0	SI
19	Add transistor for LED sinker	Add transistor for LED sinker	B	28	Add M119& M120 for LED power sinker.	B0	SI
20	Update thermal circuit	Update thermal circuit	B	30	1. Add RJ105, RJ106, R247 for DGPU& NB thermal diode switch circuit. 2. Delete R23, R25, R30, R37, R38, R42, R43, C94, D1, D2, M5, M6, Q9.	B0	SI
21	Update USB3.0 solution to NEC	Update USB3.0 solution to NEC by HP required.	B	33	Modify USB3.0 soultion to NEC uDP720200	B0	SI
22	Audio circuit modify (Kevin.Yeh)	Audio circuit modify	B	36, 37	1. Modify R484, R485, R487& R490 to 1.96K ohm 1% 2. Add R517 (10K ohm) and pull-high to "HP_AMP". 3. Add R244, R245, R246, R248, C727, C775 for B+ break down issue.	B0	SI
23	Power circuit modify (Eva.Chao)	Power circuit modify	B	40, 42, 44, 45	1. Modify PR50, PC67 from 1206 to 0805& 0603 package. 2. Modify PC45, PC207 to 220uF/ 6.3V. 3. Leave PC22, PC45& PC61 empty. 4. Add PQ608, PR239 for AC-off funtion. 5. Modify PL8 to PCMC063T-3R3MN 6. Leave PR64 empty and PR53 mouted for charge-pump states. 7. Modify PR102 to 30.1K ohm 1%. 8. Modify PR16 to 10K ohm and Add PC130 for 1.1VS_PWRGD signal quality 9. Modify PC222 for double pulse issue.	B0	SI

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Item	Fixed Issue	Reason for Change	Rev	P6#	Modify List	B Ver#	Phase
24	Prevent GPU ACAVIN leakage current	Prevent GPU ACAVIN leakage current	C	16	Add R352& D7 to prevent GPU ACAVIN leakage current.	C0	PV
25	Update USB3.0 circuit	Update USB3.0 circuit	C	33, 34	1. Add R263, R264& M125 for USB3.0 Wake up event. 2. Add R262& D123 for USB3.0 reset timing issue. 3. Modify L26 to package 0603 for parts lead time issue. 4. Correct Analog& Digital power source 5. Add R261 for SMI BOM option 6. Delete M17 and update power switch circuit. 7. Update U16 footprint	C0	PV
26	KBC SLP_S5# signal setting	KBC SLP_S5# signal setting	C	29	Add R165 to setting SLP_S5# GND level	C0	PV
27	Logo LED broken issue	Logo LED module didn't have current limit resistor	C	24	Add R335 for Logo LED current limit	C0	PV
28	Zero power ODD function removal	Zero power ODD function removal	C	27	Leave C652, M108, M109, Q105, Q106, R419, R424& R452 empty for Zero Power ODD function removal.	C0	PV
29	EEPROM WP#	Add EEPROM WP# from EC	C	29	Add EC pin 81 as EEPROM WP# signal for EEPROM Write Protection.	C0	PV
30	NEC USB3.0 device disappear issue	Fine-tune NEC USB3.0 power up seq	C	33	1. Add C94 for NEC uPD700200A global reset timing fine-tune 2. Add R259 as empty for CLKREQ external pull-high	C0	PV
31	GPU thermal trip normal operation status	Set GPU thermal trip normal operation status	C	2, 29	1. Add R423 for GPU thermal trip normal operation status 2. Add Q108 for CPU processor hot	C0	PV
32	Hall sensor sense issue	Hall sensor can't work fine	C	28, 38	Modify SW100, C510 to D/B and modify CN_PBTN1 to 8 pin to meet M.E. modify	C0	PV
33	PX mode GPU thermal sensor fail	EC can't check GPU thermal status	C	2, 21, 29 30	1. Remove Q101, R303 remove CPU thermal alert. 2. Add R268 pull-high at alert of thermal sensor. 3. Connect DGPU_PX_VGA_EN to EC for PX mode indicates. 4.Add Q109, R181 for thermal sensor leakage issue	C0	PV
34	Stage ID indicate	Indicate SI/ PV stage for SW	C	12	Add R461 for Stage ID (Default internal PU: H-SI, L-PV)	C0	PV
35	Power seq fine-tune	Power seq fine-tune	C	33, 43	1. Modify PR801 to 100K_F for USB3.0 chip power seq 2. Modify R336, PR232 to 100K_F for VGA power seq	C0	PV
36	Power circuit modify (Staley Chiu)	Power circuit modify	C	41, 43, 44, 45, 46	1. PL8 change to 4R7 2. Leave PR66 as empty 3. PR81/ PR81 change to 22K/ 34.8K for USB port load issue 4. PR79 change to 54.9k for VRAM load issue 5. PR104 change to 30K for AMD VID Updated 6. PR100 change to 44.2k for AMD VID Updated 7. Modify MAX/OCP current text 8. Update VID table 9. PC114 change to 10u/10v0805 for Phase/Gain 10. PC222 change to 330u/2v for double purse 11. PC60 change to Panasonic source (use the same source with others) 12. Add PC247, PC248/ 68uF/25V for closing acoustic noise 13. PC115 change to 10u/10v0805 for Phase/Gain 14. PC121 change to 10u/10v0805 for Phase/Gain 15. Delete PJP114	C0	PV
37	RFI solution (Hank Tsai)	RFI solution	C	11	Modify C442, C448 to 10pF as mounted.	C0	PV
38	EMI solution (PV - Benson Ni)	Update EMI solution	C	30, 37, 38, 39, 40, 41, 42, 45, 46, 48	1. Modify CB15,CB16 as mounted. 2. Modify EC37,EC39,EC41,EC44 as mounted. 3. Modify EC102,EC104,EC105 as mounted. 4. Add EC110/ 0.1uF bypass caps. Between USB conn pin7 (USB5V_ON) and GND. 5. Add EC139/ 0.1uF bypass caps.Between CN_ADP1 pin 5 and GND. 6. Modify C500 as mounted. 7. Add EC138/ 0.1uF bypass caps. between 5VSTBY_SRC and GND. 8. Add EC57/ 0.1uF bypass caps. between 1.5V_SRC and GND. 9. Add EC45/ 0.1uF bypass caps. between CPU_VDDNB and GND. 10. Add EC59/ 0.1uF bypass caps. between +CPU_PWR_SRC and GND. 11. Add EC60, EC61/ 0.1uF bypass caps. between 1.5VS and GND. 12. Modify EC5,EC6,EC7,EC10,EC11,EC12,EC108,EC122 as mounted. 13. Add EC62, EC63, EC64/ 0.1uF bypass caps. between B+ and GND. 14. Add EC65/ 0.1uF bypass caps. between 3.3VS and GND. 15. Delete EC111,EC25,EC23,EC24,EC26,EC33,EC35,EC109,EC110,EC45,EC38.	C0	PV
39	ESD solution (PV - Stone Wang)	Update ESD solution	C	35, 36	1. EL1, EL2 from Bead 120ohm change to the Resistor 300ohm. 2. EC36, EC40 change to mounted. 3. Add a Varistor ED10 between CN_MIC1 pin5 and Net AGND. 4. ED3, ED4 change to 0603 Varistors. 5. Add a Varistor ED11 between CN_PHONE1 pin5 and Net AGND. 6. ED6, ED8, ED104, ED106 change to 0603 Varistors. 7. ED5, ED7, ED9, ED108 change to 0603 Varistors and keep them as empty	C0	PV

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40	RTC accuracy update (BOM)	RTC accuracy update	D	11	Modify C704& C719 to 22pF and 18pF.	D0	MV
41	Prevent adaptor level fail (Power)	Prevent adaptor level fail	D	40	Modify PR89 to 422Kohm 1%	D0	MV
42	Prevent leakage current from CRT	Prevent leakage current from CRT	D	26	Add R23 as 10Kohm to prevent leakage cuurent from CRT	D0	MV
43	Fine-tune LED brightness (BOM)	Fine-tune LED brightness by HP ID	D	29	1. Modify R399 to 590ohm 1% for RF on LED 2. Modify R481 to 240ohm 1% for RF off LED 3. Modify R404 to 1.27Kohm 1% for CAP lock LED 4. Modify R405 to 240ohm 1% for MUTE LED 5. Modify PR209 to 715ohm 1% for Charger LED	D0	MV
44	S5 wake-up event leakage issue (BOM)	Prevent leakage current from pull-high resistor	D	29	Leave R356, R361 as empty to prevent it.	D0	MV
45	DFX report improvement	Meet Factory DFX checking	D	45	Modify PJP100 to Normal close footprint	D0	MV
46	EMI solution improvement	EMI solution improvement	D	48	1. Modify EC15 from between 3.3VS& 5V to 3.3VS& GND 2. Modify EC18 from between 3.3VS& 5V to 5V& GND 3. Modify EC2 from between 3.3VS& B+ to B+& GND 4. Add EC35, EC38, EC66, EC140, EC141, EC142, EC143, EC144, EC146, EC147, EC148	D0	MV