

CLOCK
GENERATOR
RTM880N-796
PAGE 03

SO-DIMM A
Maximum 2+2GB
PAGE 7

SO-DIMM B
Maximum 2+2GB
PAGE 8

AMD
Conesus
PROCESSOR
10~15W
812 EPGA
PAGE 4,5,6

AMD Embedded with ATI RS780MN & SB710

	SLP S3#
(Full ON)	HIGH
(Suspend to RAM)	LOW
(Suspend to Disk)	LOW
(Soft OFF)	LOW

64M * 16 DDR3 667

SIDE- PORT
128MB
PAGE 12

CRT / LCD
PAGE 13

HDMI
PAGE 14

North Bridge
AMD
RS780M
INTEGRATED
GRAPHICS
6W
21x21 mm
528 FCBGA
PAGE 9,10,11,12

USB 2.0

PCIE x1

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PAGE	DESCRIPTION
1	Block Diagram
2	INDEX & POWER STATUS
3	CLOCK GEN
4-8	CPU
9-12	North bridge RS780
13	CONN - LVDS/CRT
14	CONN - HDMI
15-18	SOUTH BRIDGE RS780
19	LAN - RT8103EL
20	CARD READER - ALCOR AU6433B52-GEF
21	AUDIO - IDT 92HD81
22	USB CONN / SWITCH / LID
23	BT / WEBCAM / TOUCHPAD / G-SENSOR
24	WLAN / WWAN
25	KBC - ITE8502E
26	PWR - BATTERY CHARGER
27	PWR - CPU CORE
28	PWR - NB CORE
29	PWR 5V / 3.3 VSTBY
30	PWR 1.8V / 0.9V
31	PWR - 1.1VS / 2.5VS / 1.2V-USB
32	PWR - 1.5VS / 1.2VS
33	PWR - V / VS / VGA POWER
34	POWER SEQUENCE
35	OTHER SCREW / EMI CAPS

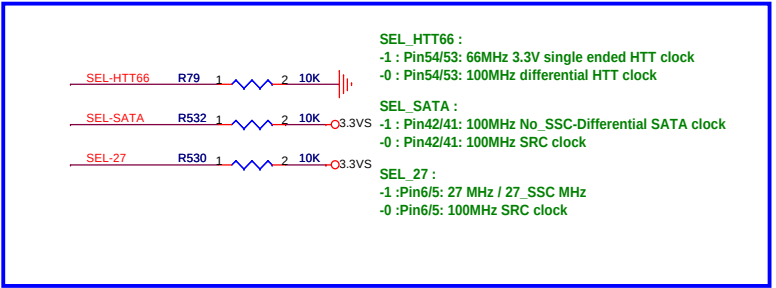
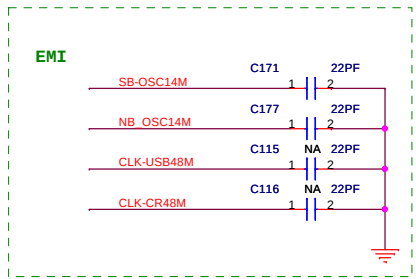
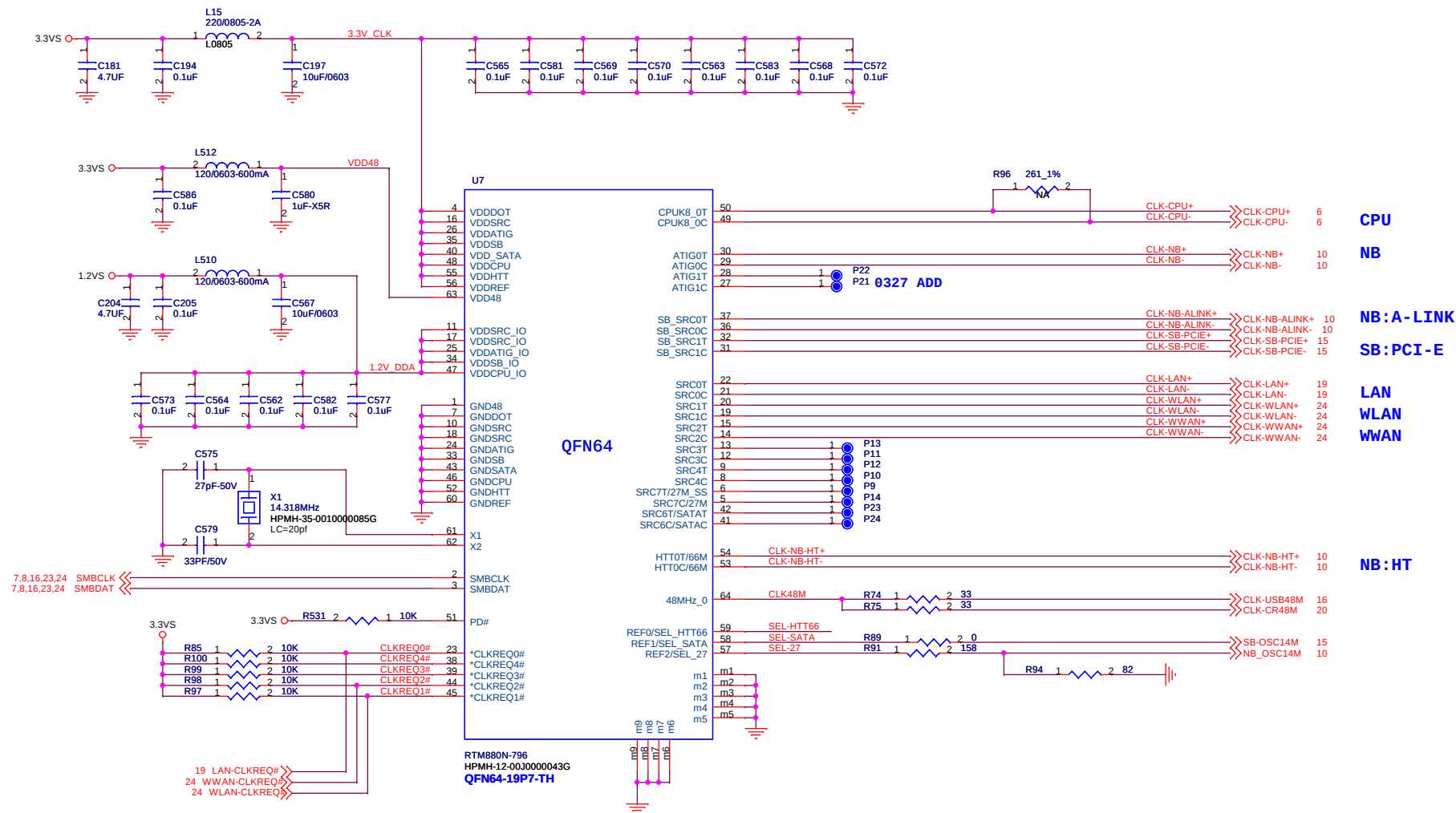
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
ACIN	~+19V	26	ADAPTER IN POWER		S0-S5
B+	+10~+19V	13,23,24,26,27,28,29,30,31,32,33	MAIN POWER		S0-S5
VBAT	+3.0V~+3.3V	15	RTC BATTERY		S0-S5
LDO5	+5V	22,29	LDO POWER	B+	S0-S5
LDO3	+3.3V	29	LDO POWER	B+	S0-S5
3.3VSTBY	+3.3V	15,16,17,22,25,26,29,31,33	STANDBY POWER	B+	S0-S5
3.3V-DUAL	+3.3V	15,16,17,18,25,31,33	EC CTRLD POWER	3.3VDUAL-ON#	BY EC CONTROL
1.2V-DUAL	+1.2V	18,31	3.3V-DUAL CTRLD POWER	3.3V-DUAL	BY EC CONTROL
5V	+5V	22,23,29,30,32,33,	SUS-C# CTRLD POWER	SUSC#	S0,S3
3.3V	+3.3V	13,33	SUS-C# CTRLD POWER	SUSC	S0,S3
1.8V	+1.8V	04,05,06,07,08,30,33	SUS-C# CTRLD POWER	SUSC#	S0,S3
0.9V	+0.9V	04,05,07,08,30	SUS-C# CTRLD POWER	SUSC#,SUSB#	S0,S3
5VS	+5V	06,13,14,17,18,21,22,23,25,27,28,31,32,33	SUS-B# CTRLD POWER	SUSB	S0
3.8VS	+3.8V	23,33	SUS-B# CTRLD POWER	SUSB#	S0
3.3VS	+3.3V	03,06,07,08,10,11,12,13,14,16,17,18,20,21,22,23,24,25,27,28,29,31,32,33	SUS-B# CTRLD POWER	SUSB	S0
2.5VS	+2.5V	06,31	SUS-B# CTRLD POWER	SUSB#	S0
1.8VS	+1.8V	06,10,11,12,15,16,33	SUS-B# CTRLD POWER	SUSB	S0
1.5VS	+1.5V	11,12,16,24,28,31,32	SUS-B# CTRLD POWER	SUSB#	S0
1.2VS	+1.2V	04,06,11,15,17,18,32	SUS-B# CTRLD POWER	SUSB#	S0
1.1VS	+1.1V	09,10,11,12,31	SUS-B# CTRLD POWER	SUSB#	S0
CPU_CORE		04,27	CPU CORE POWER	SUSB#	S0
NB_CORE	+1.0V~+1.1V	11,18,32	NORTH BRIDGE CORE POWER	1.1VS-PG	S0
BATA+	+10V~+17V	26	MAIN BATTERY		S0-S5

GND PLANE	PAGE	DESCRIPTION
 GND	ALL	
 AGND	19	
 LAN-GND	21	

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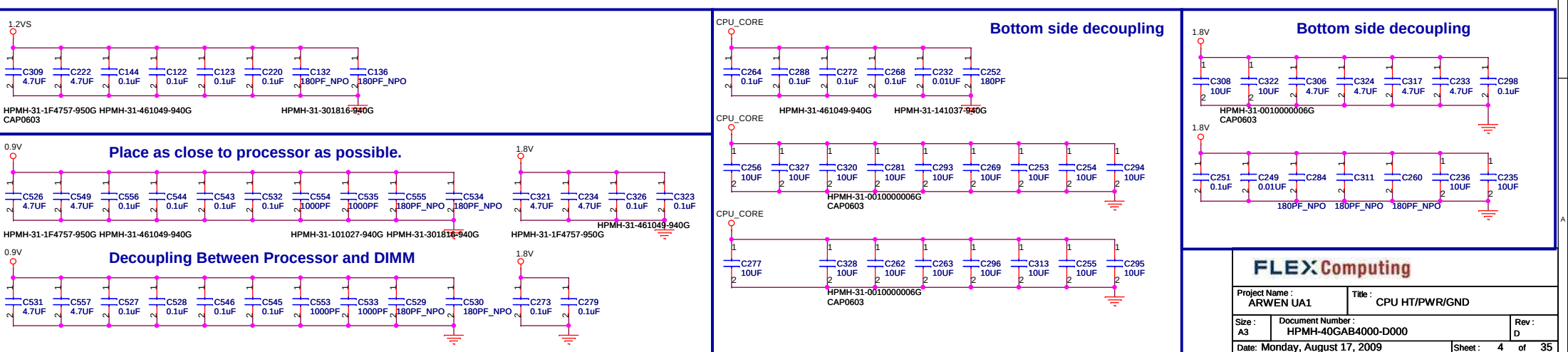
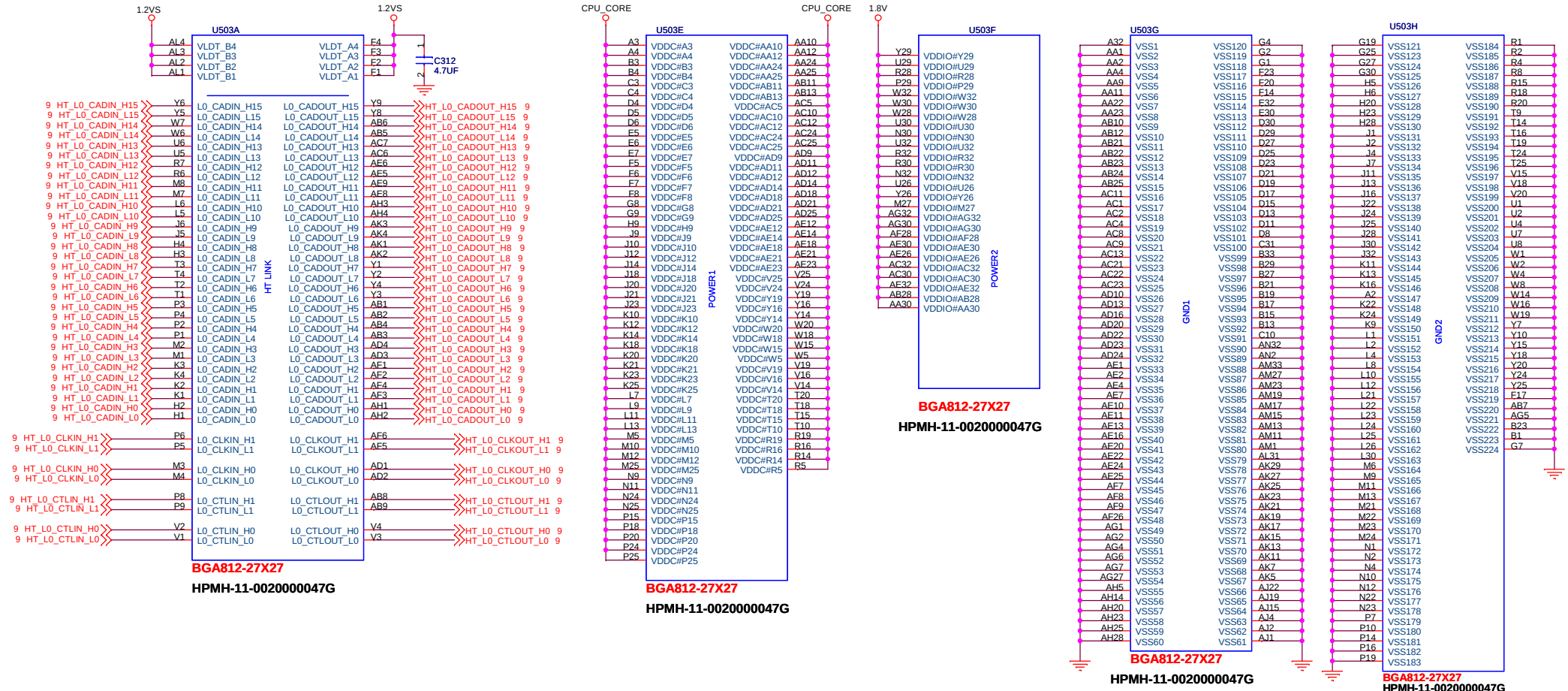
Project Name : ARWEN UA1		Title : Power Diagram	
Size : Custom	Document Number : HPMH-40GAB4000-D000		Rev : D
Date: Monday, August 17, 2009		Sheet : 2	of 35

CLOCK GENERATOR



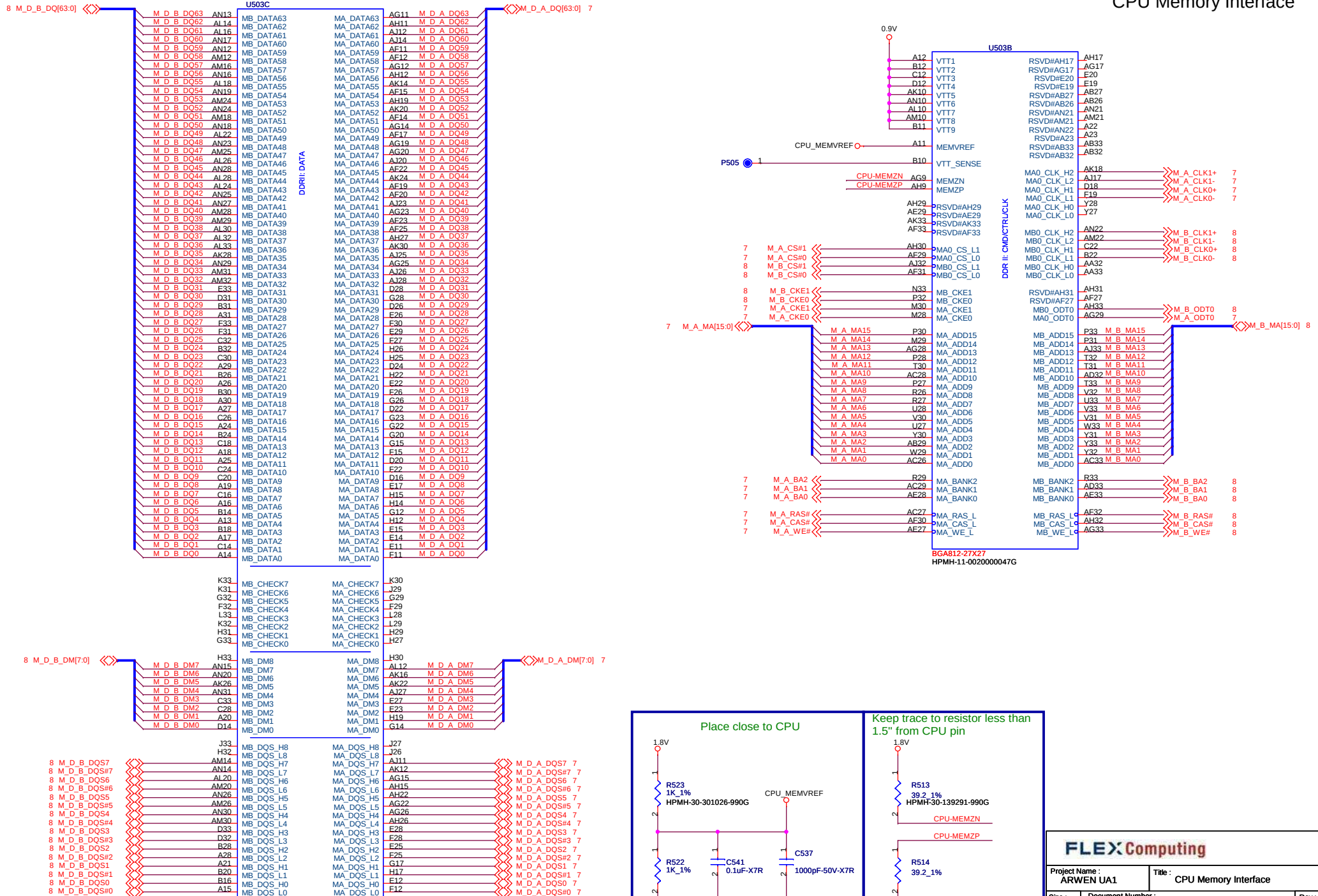
CPU HT/PWR/GND

VLDT Trace at Itast 200 mils wide



CPU MEMORY A/B

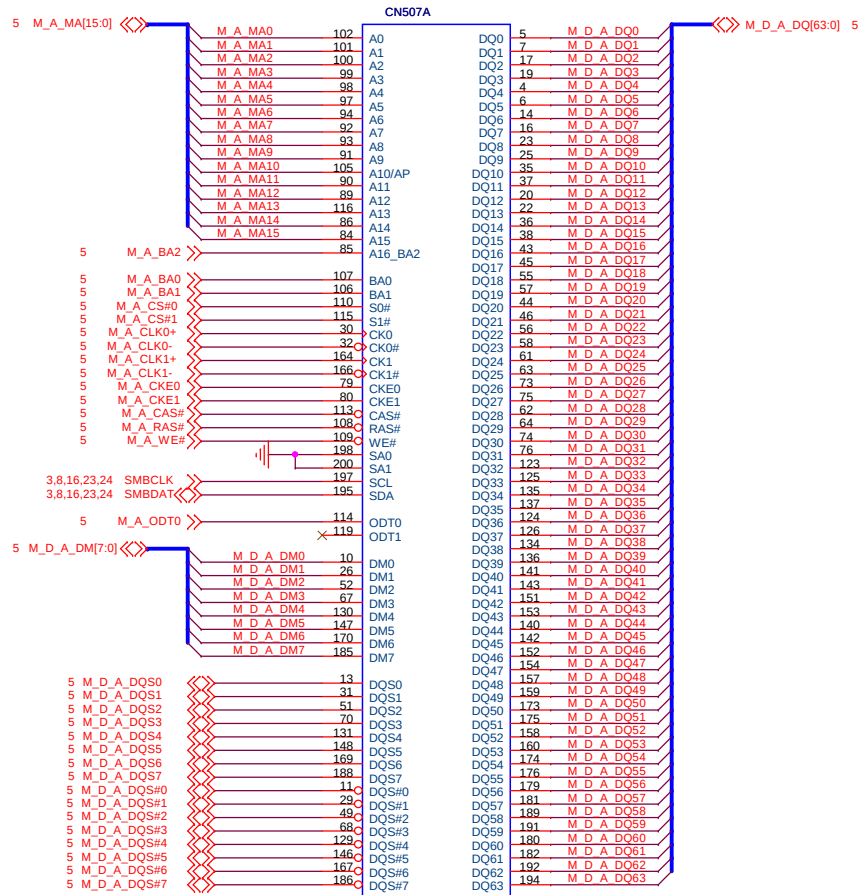
CPU Memory Interface



FLEX Computing

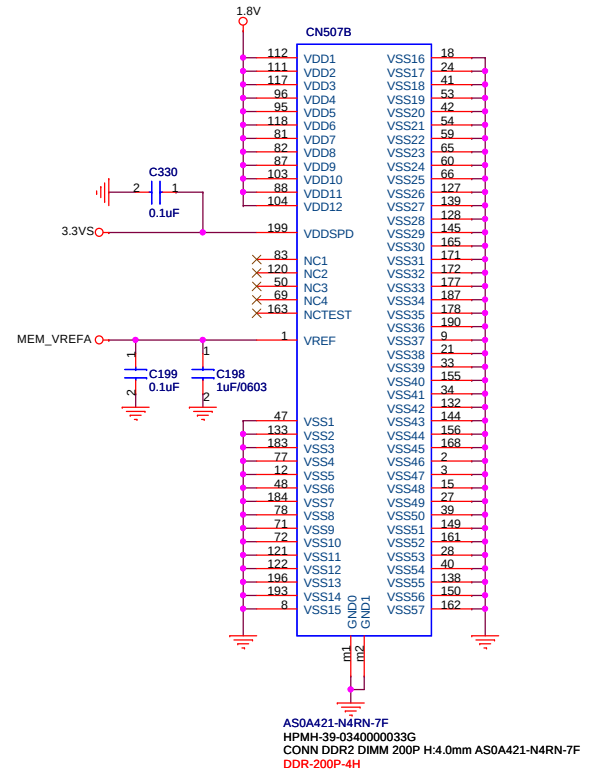
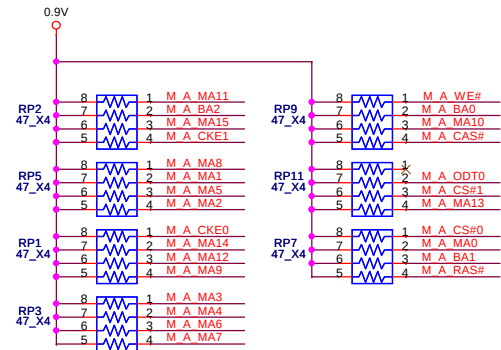
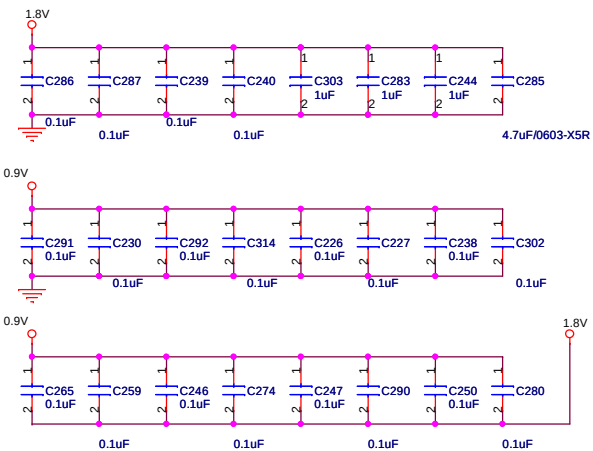
Project Name: ARWEN UA1		Title: CPU Memory Interface
Size: A3	Document Number: HPMH-40GAB4000-D000	Rev: D
Date: Monday, August 17, 2009		Sheet: 5 of 35

Memory Channel A

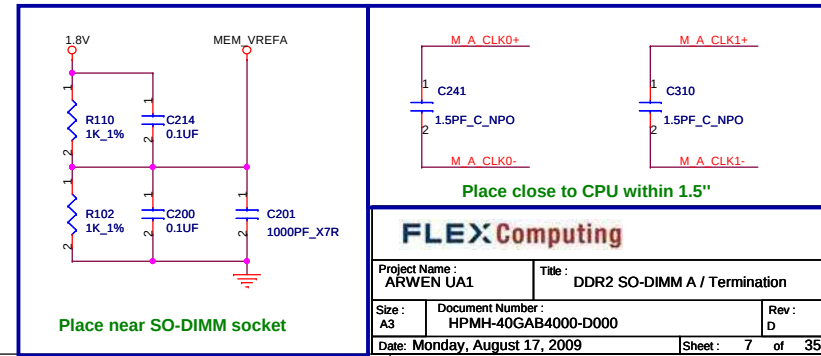


AS0A421-N4RN-7F
HPMH-39-0340000033G
CONN DDR2 200P H:4.0mm AS0A421-N4RN-7F
DDR-200P-4H

Layout :
Place these Caps near So-DimMA



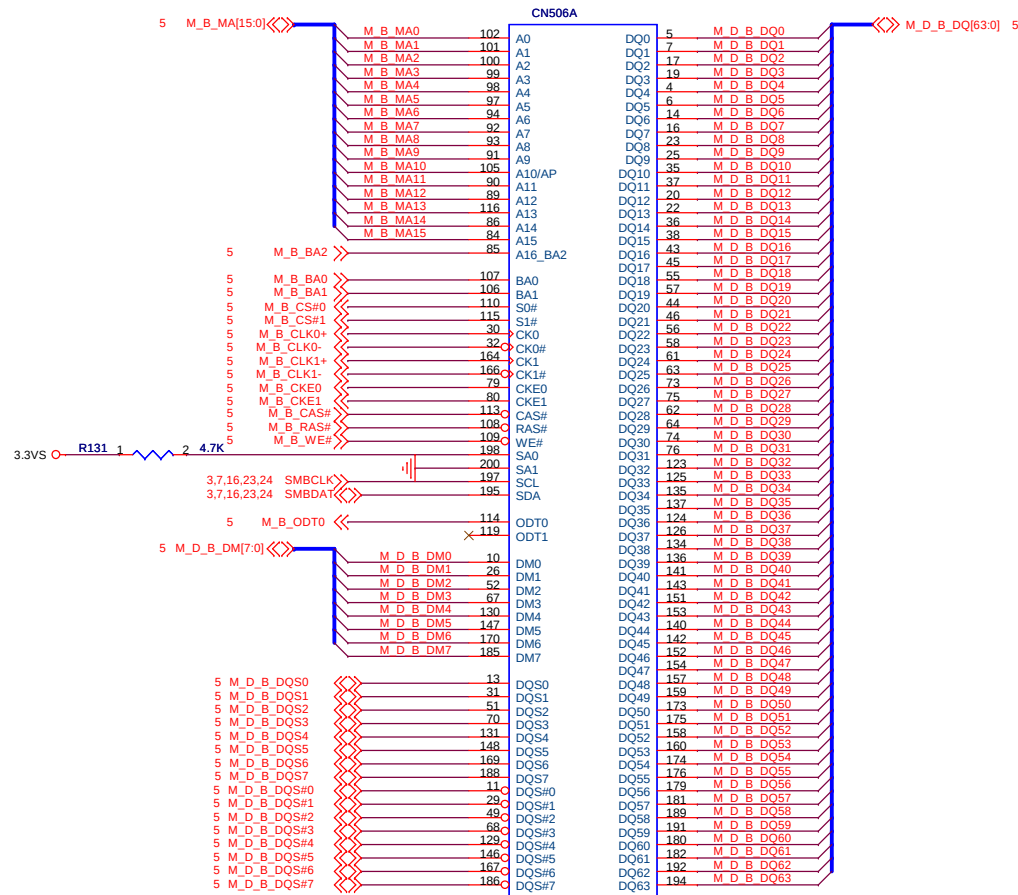
AS0A421-N4RN-7F
HPMH-39-0340000033G
CONN DDR2 DIMM 200P H:4.0mm AS0A421-N4RN-7F
DDR-200P-4H



FLEX Computing

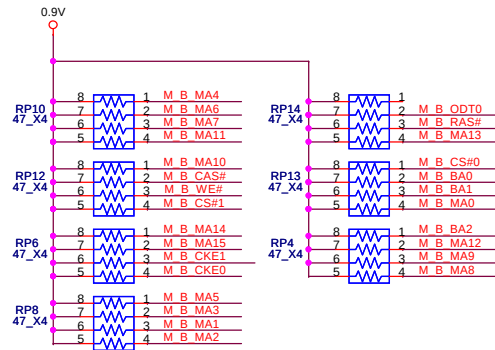
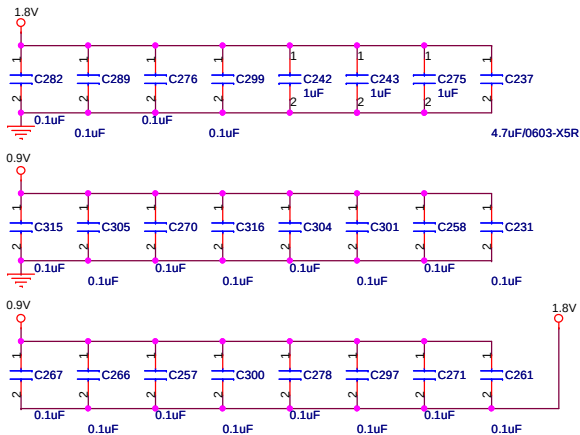
Project Name : ARWEN UA1		Title : DDR2 SO-DIMM A / Termination	
Size : A3	Document Number : HPMH-40GAB4000-D000		Rev : D
Date: Monday, August 17, 2009		Sheet : 7 of 35	

Memory Channel B

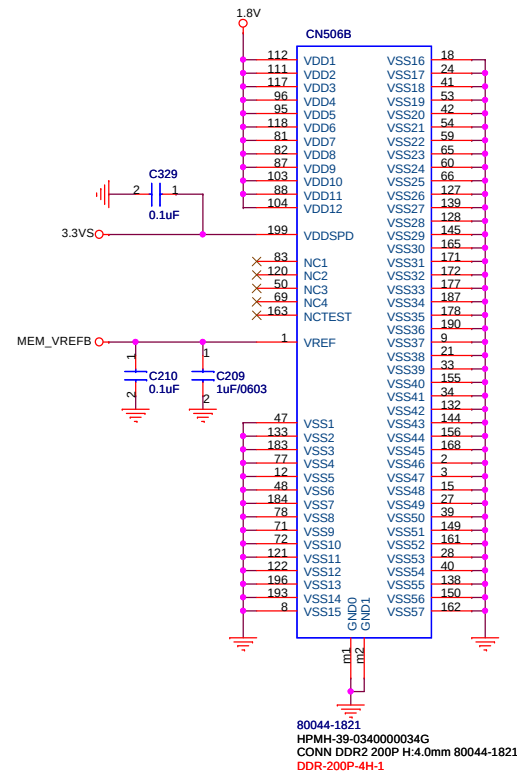


80044-1821
HPMH-39-0340000034G
CONN DDR2 200P H:4.0mm 80044-1821
DDR-200P-4H-1

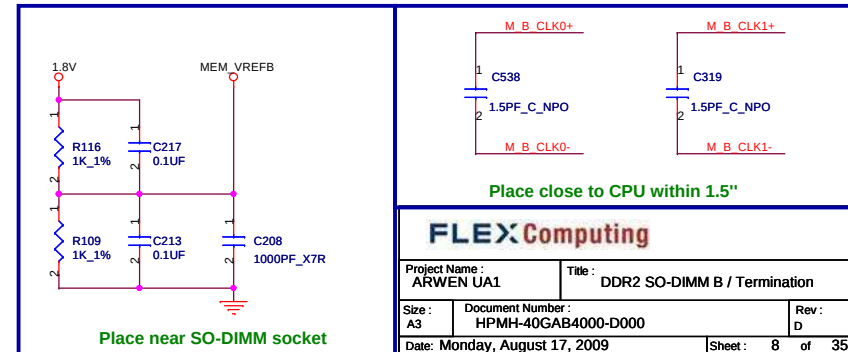
Layout :
Place these Caps near So-DimmA



DDR2 Termination DDR2 SO-DIMMB



80044-1821
HPMH-39-0340000034G
CONN DDR2 200P H:4.0mm 80044-1821
DDR-200P-4H-1



FLEX Computing

Project Name : ARWEN UA1		Title : DDR2 SO-DIMM B / Termination	
Size : A3	Document Number : HPMH-40GAB4000-D000		Rev : D
Date : Monday, August 17, 2009		Sheet : 8 of 35	

RS780M HT/PCIE/HDMI

U504A

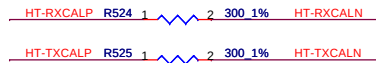
PART 1 OF 6

HYPER TRANSPORT CPU I/F



RS780MN
HPMH-10-0010000050G
FCBG4528-RS780M

301 ohm to 300 ohm



UMA HDMI

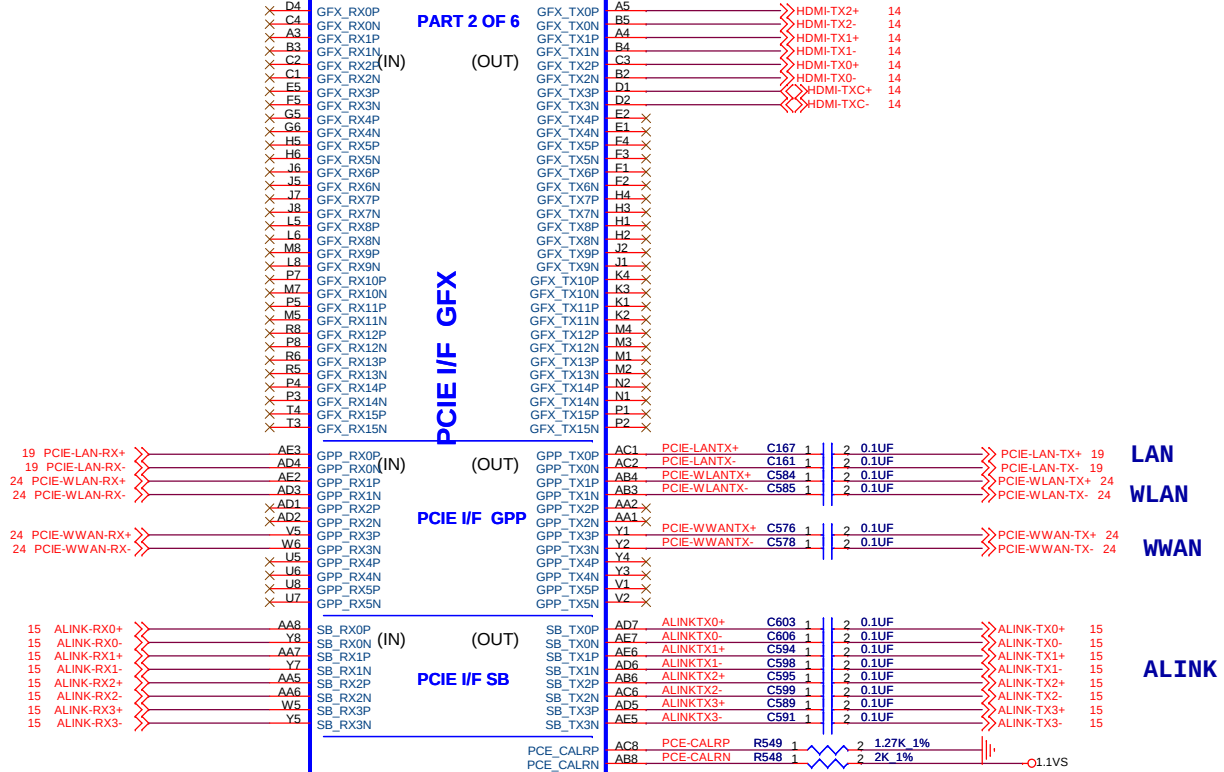
U504B

PART 2 OF 6

PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB

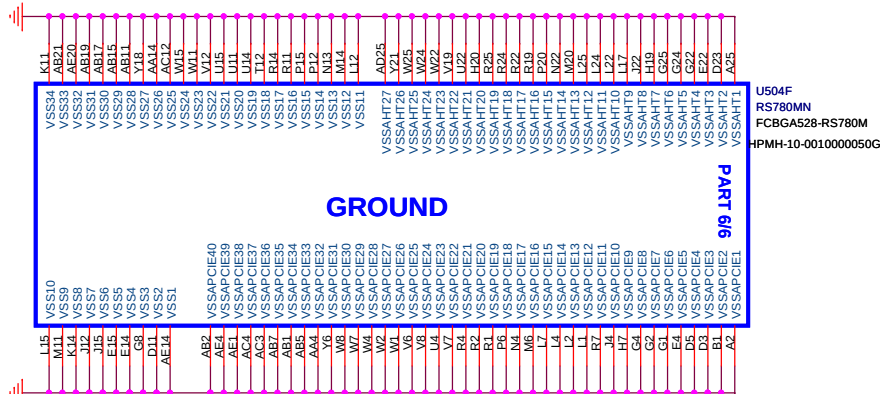
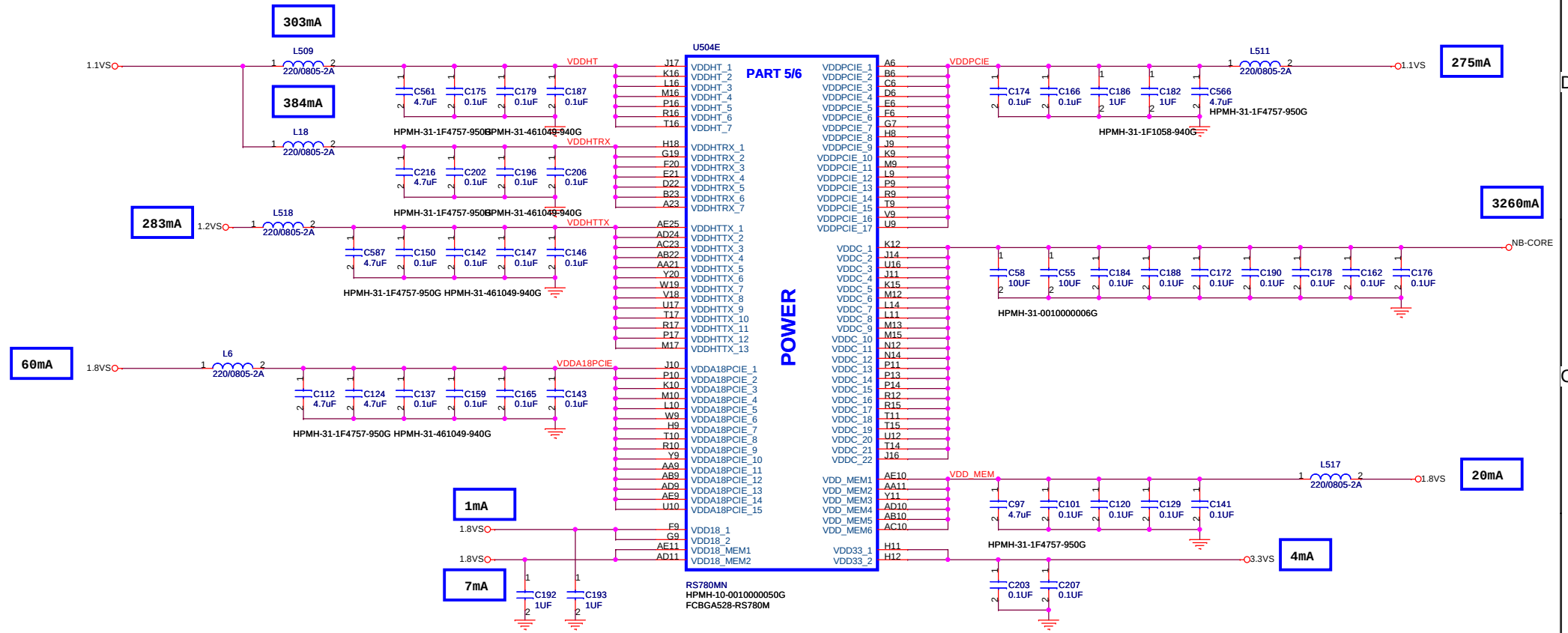


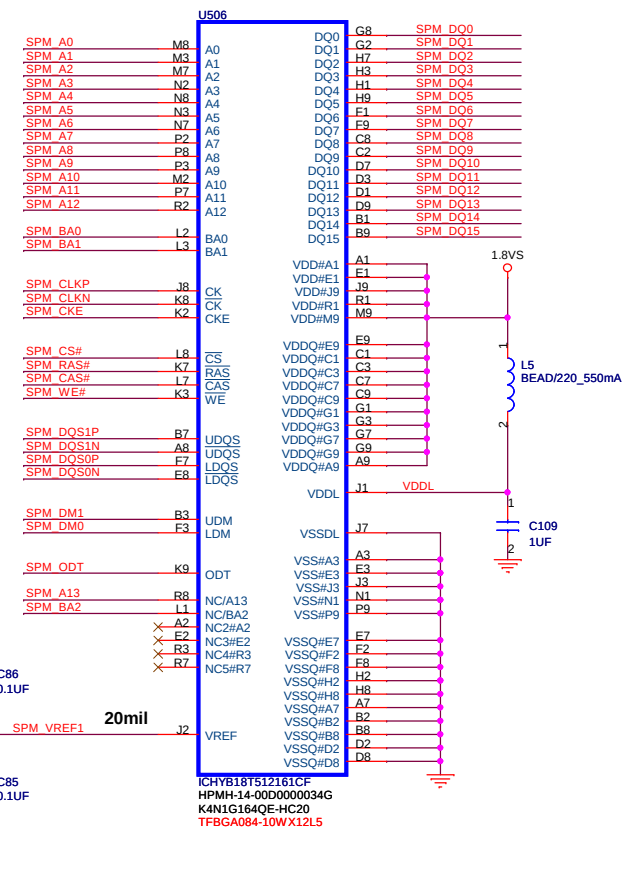
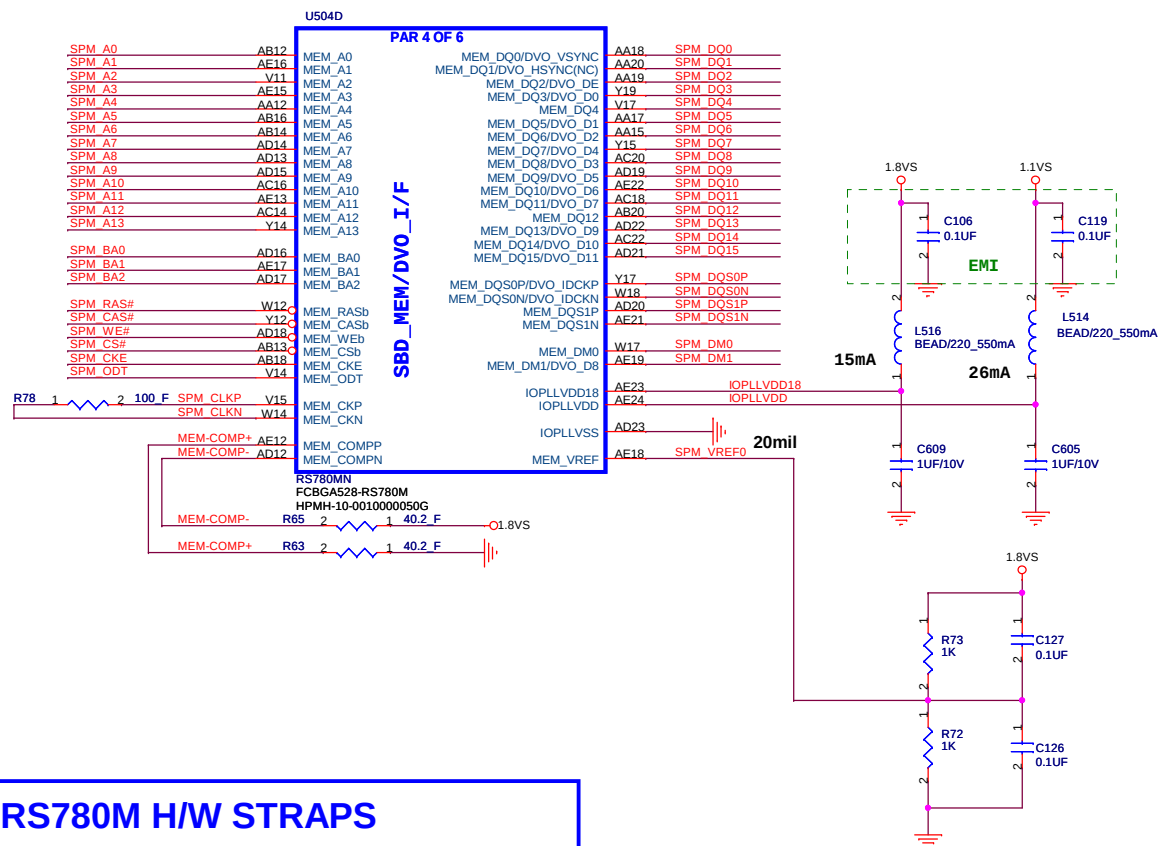
RS780MN
HPMH-10-0010000050G
FCBG4528-RS780M

FLEX Computing

Project Name : ARWEN UA1		Title : RS780M HT/PCIE/HDMI Interface	
Size : A3	Document Number : HPMH-40GAB4000-D000		Rev : D
Date: Monday, August 17, 2009		Sheet : 9	of 35

5
RS780M Power/Ground

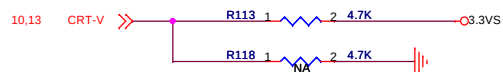


NB_SIDE PORT / STRAPS

RS780M H/W STRAPS

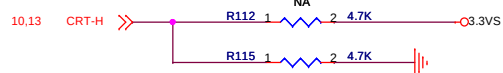
STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO.
DAC_VSYNC (RS780.Pin B11)
1 : Disable (RS780) (default)
0 : Enable (RS780)



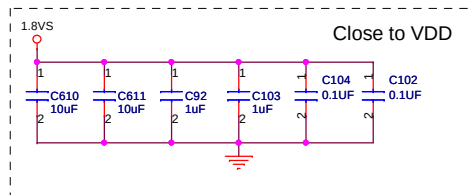
RS780: Enable Side Port Memory

```
Selects if Memory SIDE PORT is available or not
DAC_HSYNC (RS780.Pin A11)
1 : Disable (default)
0 : Enable
Register Readback of strap:
NB_CLKCFG:CLK_TOP_SPARE_D[1]
```

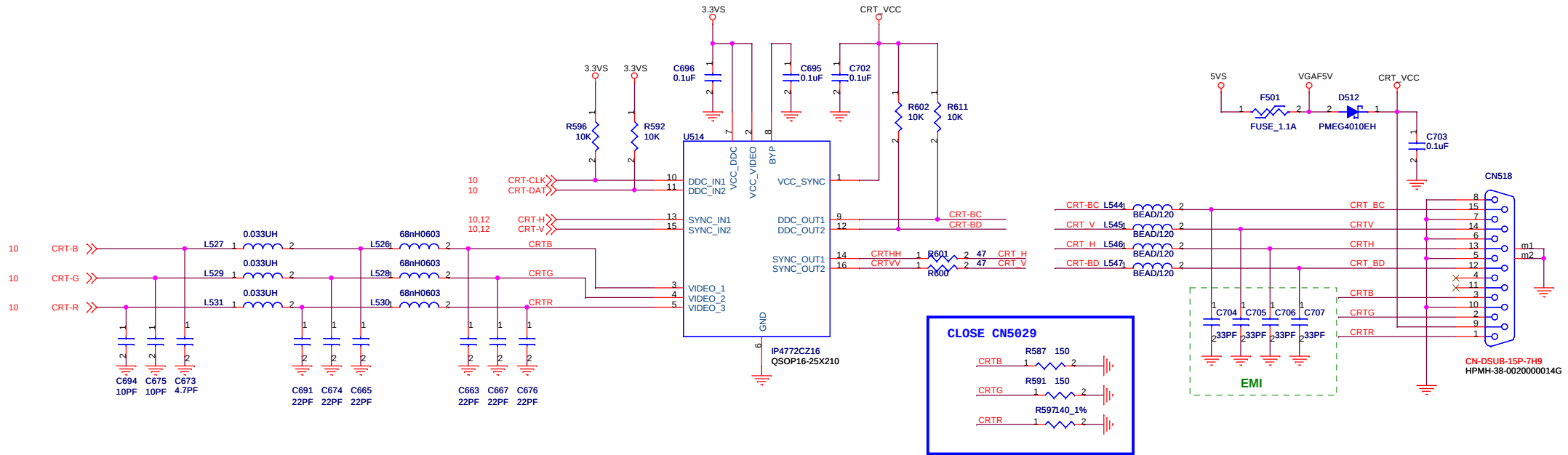


DFT_GPIO1: LOAD_EEPROM_STRAPS

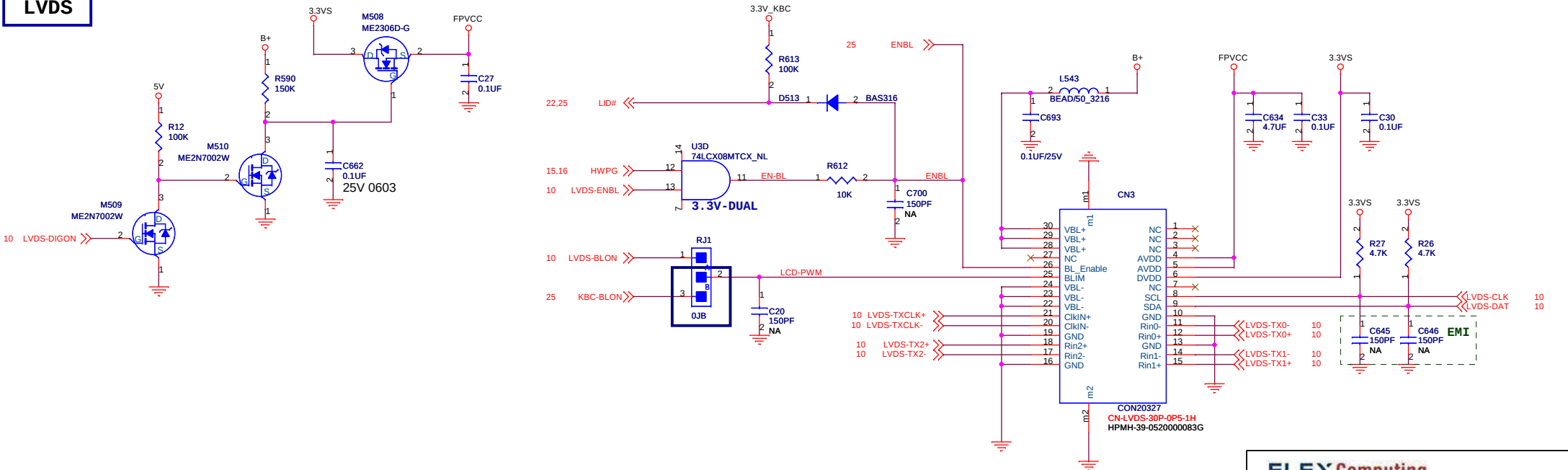
```
Selects Loading of STRAPS from EPROM
SUS_STAT# (RS780.Pin D12)
-1*: Bypass the loading of EEPROM straps and
    use Hardware Default Values
-0 : I2C Master can load strap values from EEPROM if connected
    , or use default values if not connected
```



CRT



LVDS



FLEXComputing

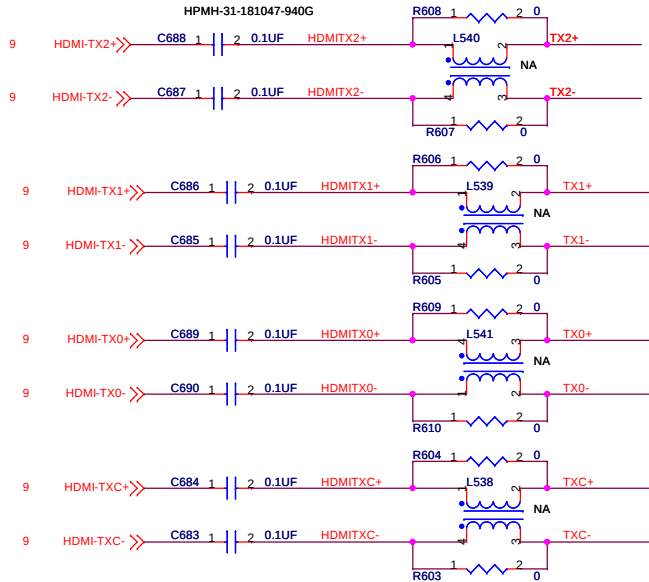
Project Name : ARWEN UA1		Title : LVDS / CRT Connector	
Size : A3	Document Number : HPMH-40GAB4000-D000	Rev : D	
Date : Monday, August 17, 2009		Sheet : 13 of 35	

HDMI

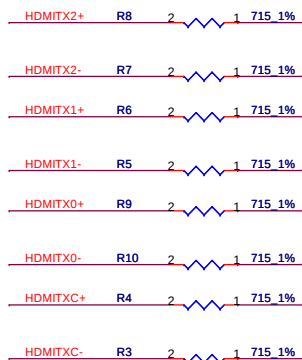
CLOSE CN5031

HPMH-32-4000000104G

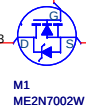
HPMH-31-181047-940G



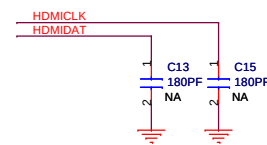
M92 SPEC SET 499 ohm



5VS

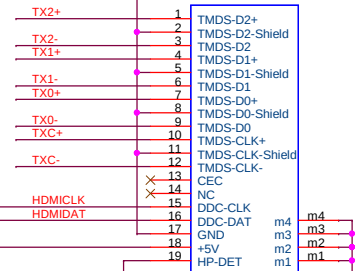


EMI

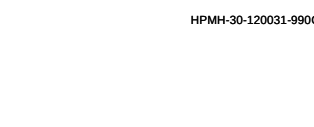
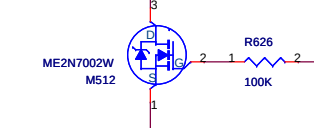
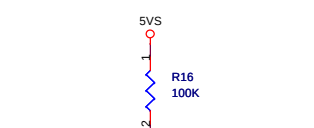
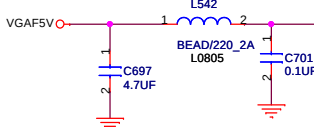
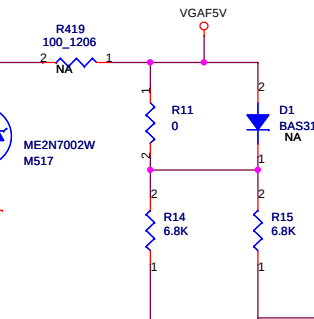


HDMI

CN515



CN-HDMI-19DIP-5H55
HPMH-38-00F0000008G



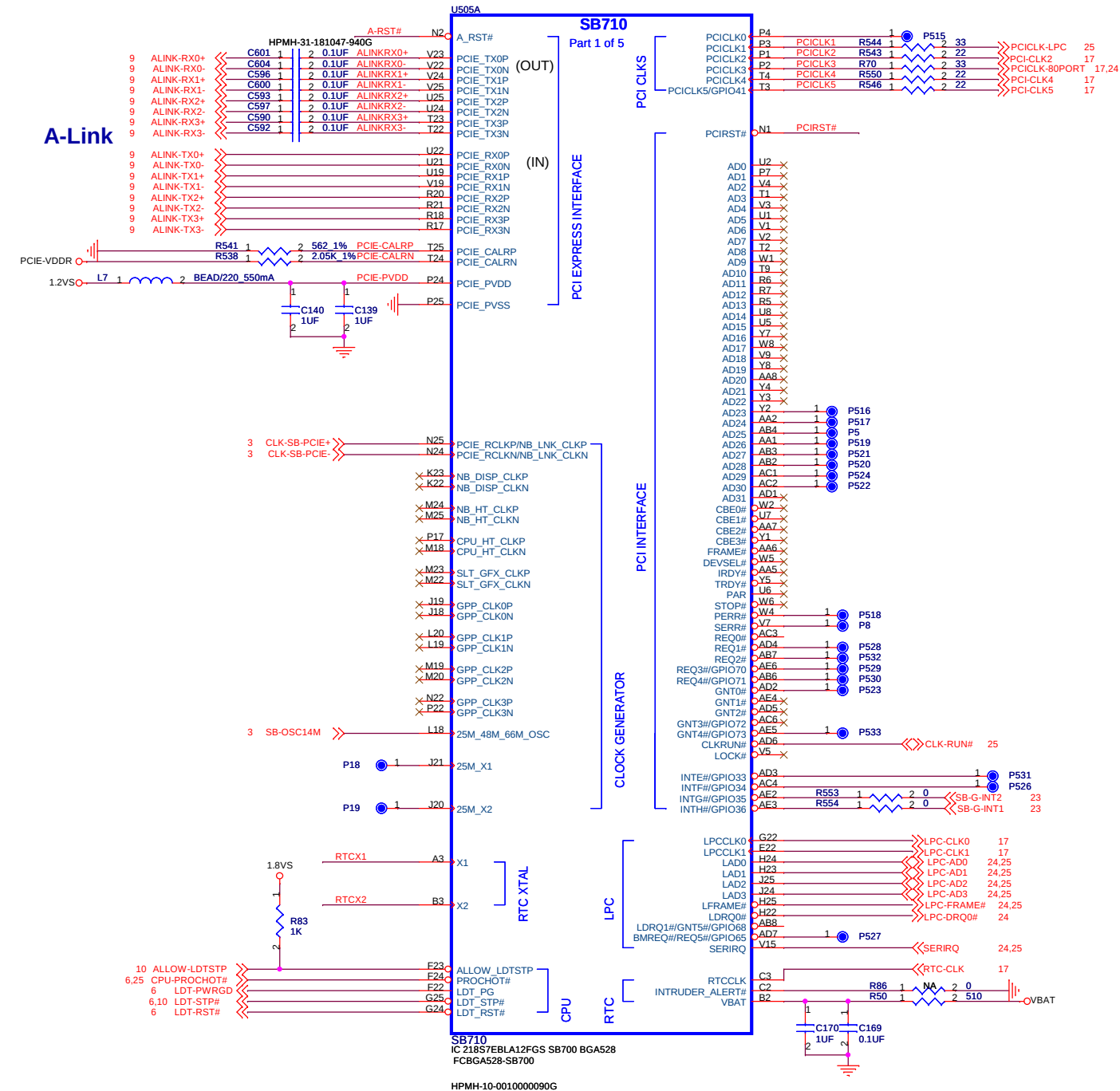
CLOSE CN5031

EMI

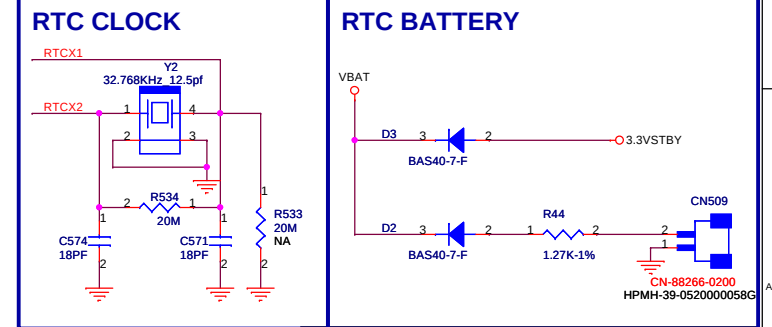
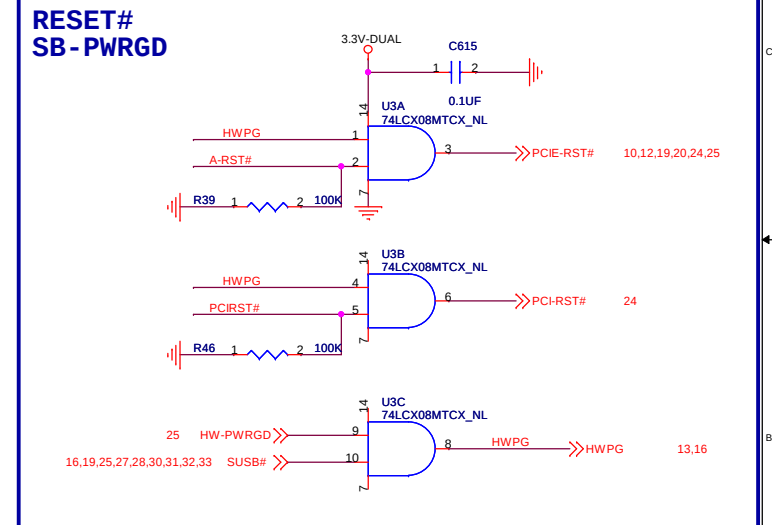
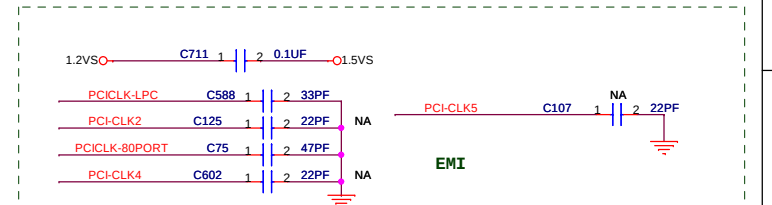
FLEX Computing

Project Name : ARWEN UA1		Title : HDMI Connector	
Size : A3	Document Number : HPMH-40GAB4000-D000		Rev : D
Date : Monday, August 17, 2009		Sheet : 14 of 35	

SB710 PCIE/PCI/CPU/LPC

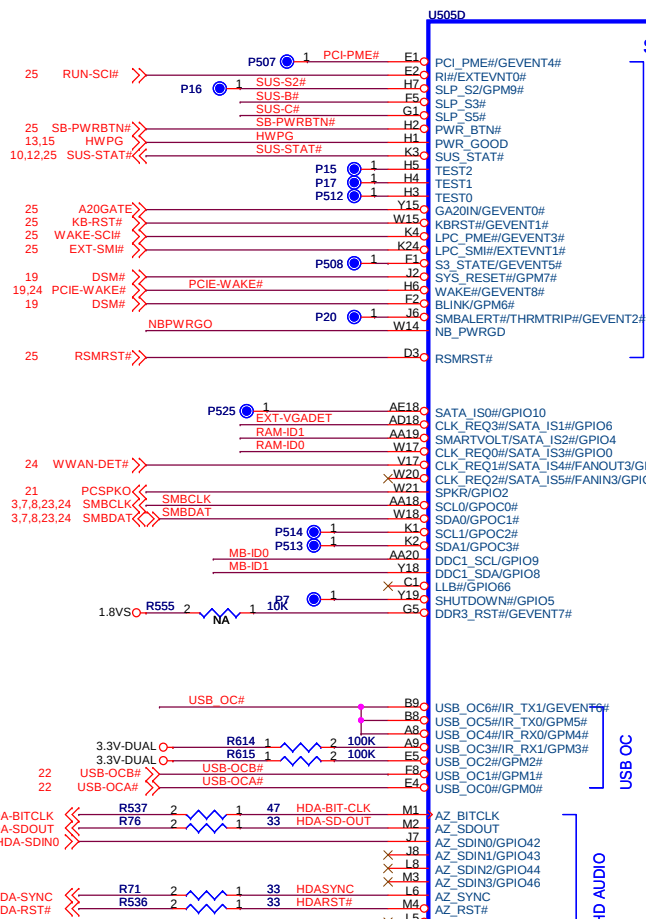
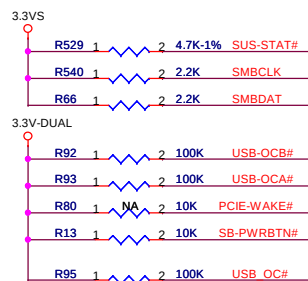


	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



FLEXComputing

Project Name : ARWEN UA1	Title : SB700 PCIE/PCI/CPU/LPC
Size : A3	Document Number : HPMH-40GAB4000-D000
Date : Monday, August 17, 2009	Rev : D
Sheet : 15	of 35



USB Ports 12 and 13 do not support wake from S1
SB700AA6

WWAN

WLAN

Card Reader

Webcam

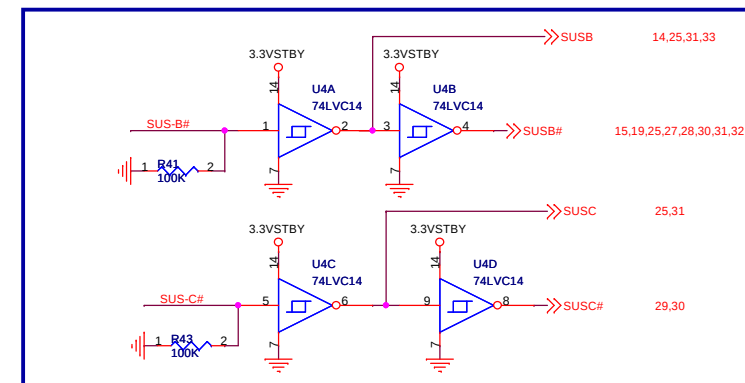
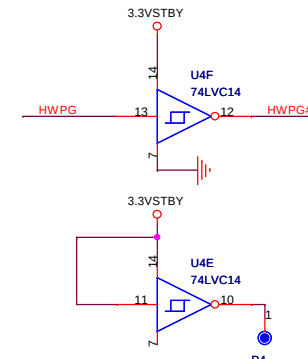
BT

PORT 3

PORT 2

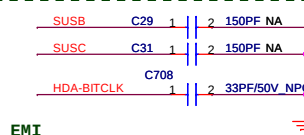
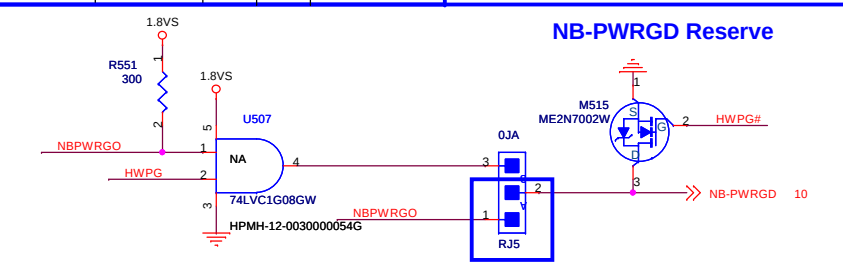
PORT 1

PORT 0



	EXT-VGADET	SIDE POST MEMORY		
		RAM-ID1	RAM-ID0	VENDER
PULL HIGH	H310DA	0	0	
PULL LOW	H310UA	1	0	Samsung
		1	1	Hynix

MB	ID
0 0	A
0 1	B
1 0	C
1 1	D



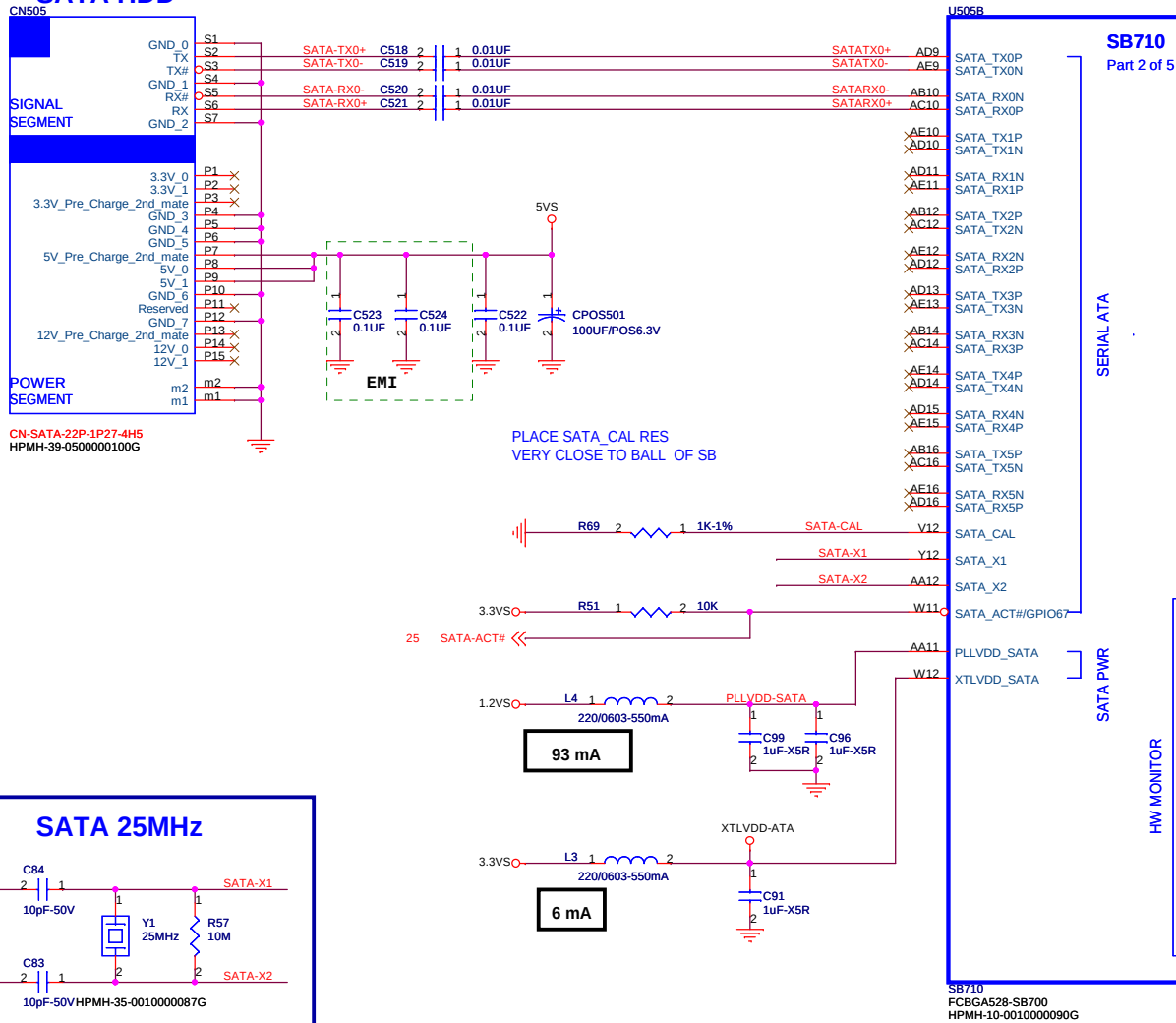
FLEX Computing

Project Name : ARWEN UA1 Title : SB710 ACPI/GPIO/USB/AUDIO

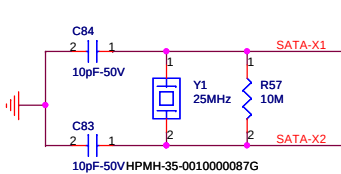
Size : A3 Document Number : HPMH-40GAB4000-D000 Rev : D

Date : Monday, August 17, 2009 Sheet : 16 of 35

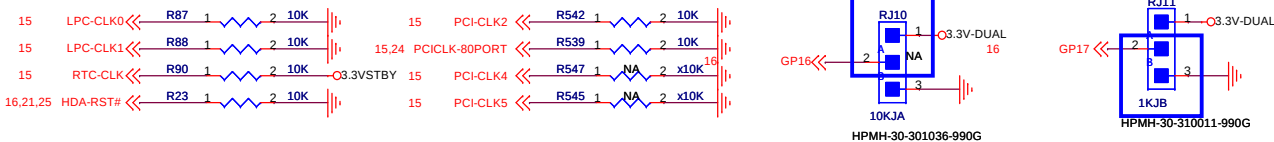
SATA HDD



SATA 25MHz



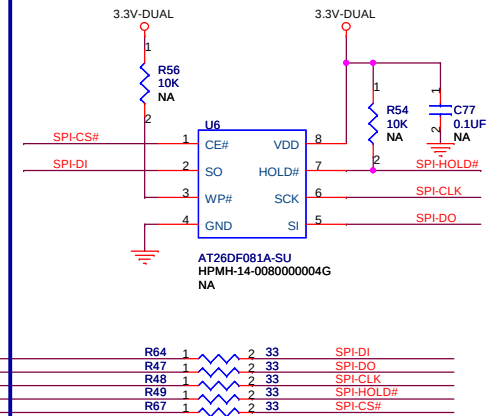
SB710 H/W STRAPS



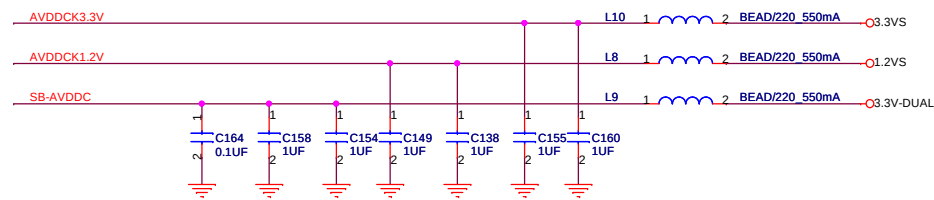
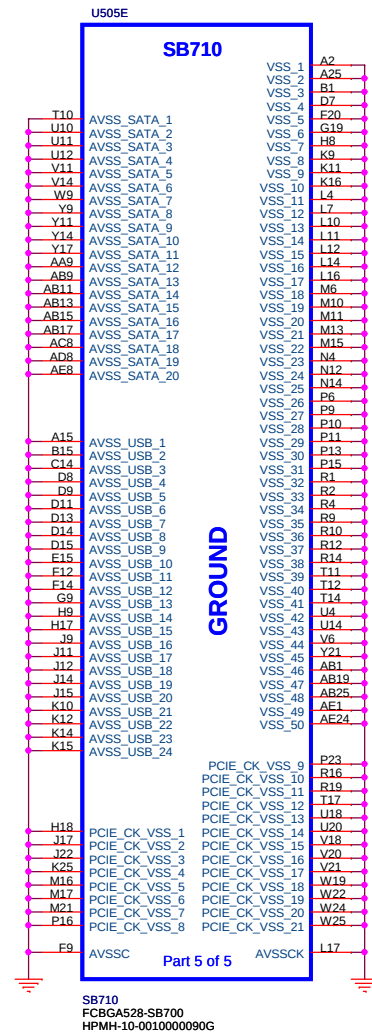
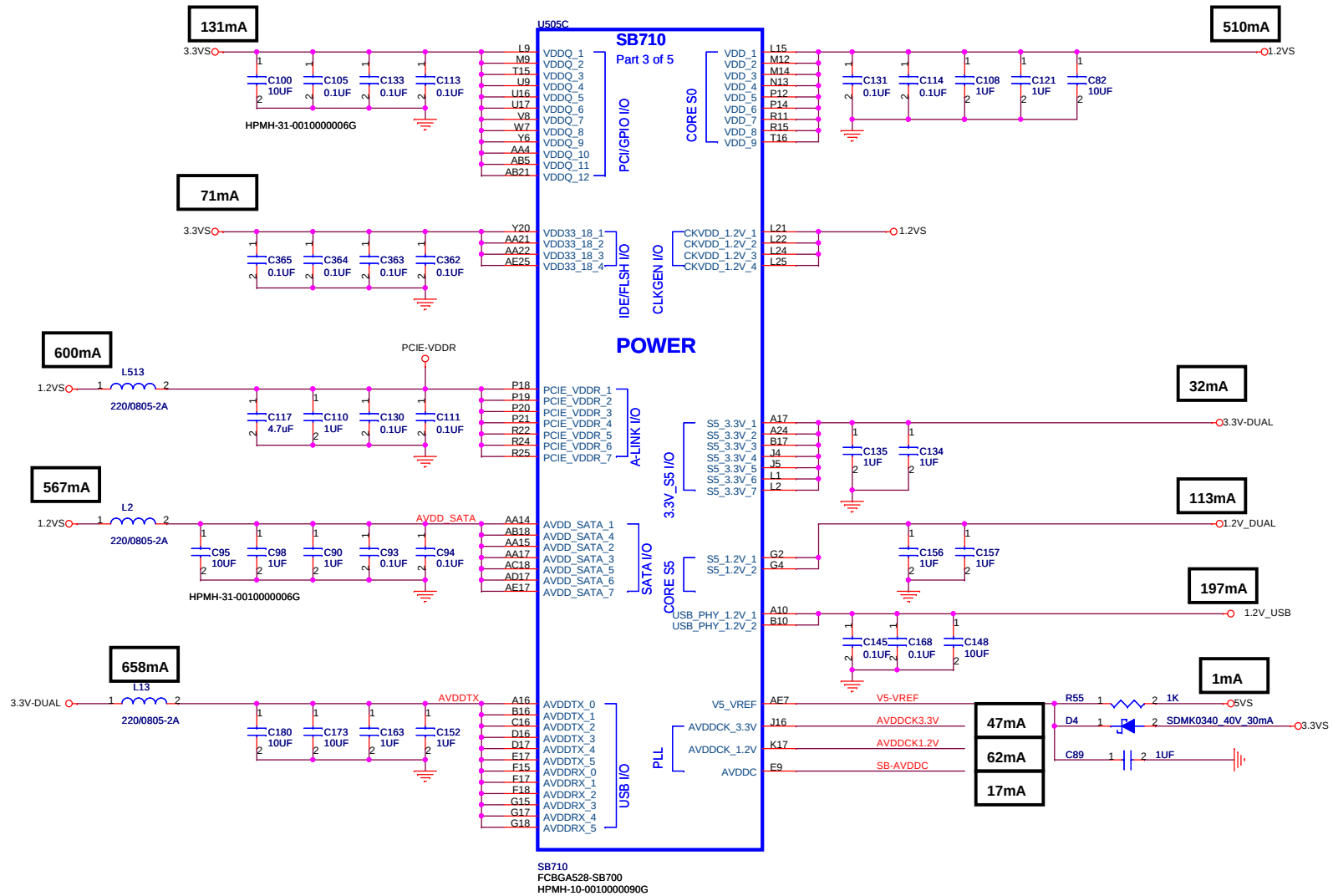
	PCI-CLK2	PCI-CLK3	PCI-CLK4	PCI-CLK5	LPC-CLK0	LPC-CLK1	RTC-CLK	AZ-RST#	GP17	GP16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT (A11) IMC ENABLED (A12)	CLKGEN ENABLED	INTERNAL RTC DEFAULT	IMC ENABLED (A11) ENABLE PCI MEM BOOT (A12)	H,H = Reserved H,L = SPI ROM (Default)	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT (A11) IMC DISABLED (A12) DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	IMC DISABLED (A11) DISABLE PCI MEM BOOT (A12) DEFAULT	L,H = LPC ROM L,L = FWH ROM	

SB710 SATA / IDE / HWM / SPI / STRAPS

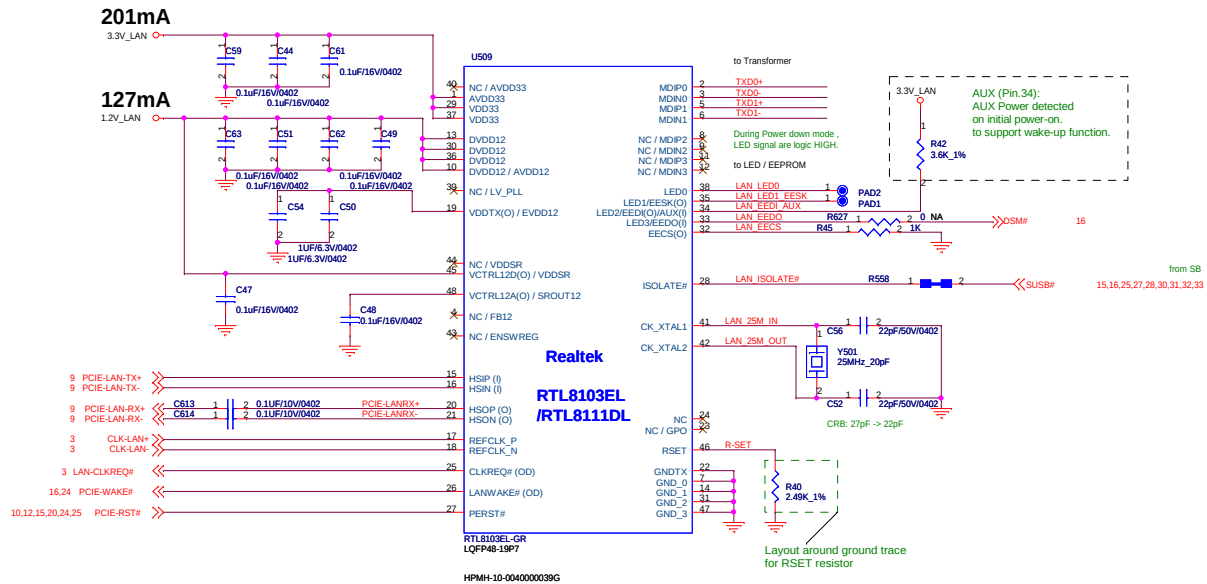
Reserve 8M-bit SPI ROM



5 mA



10/100 LAN



RTL8103E LED Configuration:

LED1-0	*00	01	10	11
LED0	Tx/Rx	Tx/Rx	Tx	Tx
LED1	LINK100	LINK	LINK	LINK100
LED2	LINK10	FULL	Rx	LINK10
LED3	NA	NA	NA	NA

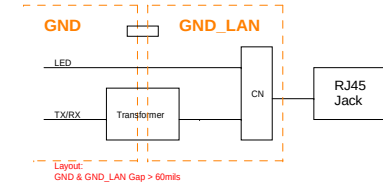
LEDS1-0's initial value comes from the 93C46
If there is no 93C46, the default value is 00

H310 mini-spec_v1.4

LAN LED:

- Amber : Activity (RX/TX)
- Green : Connectivity (Link)

Layout notes:

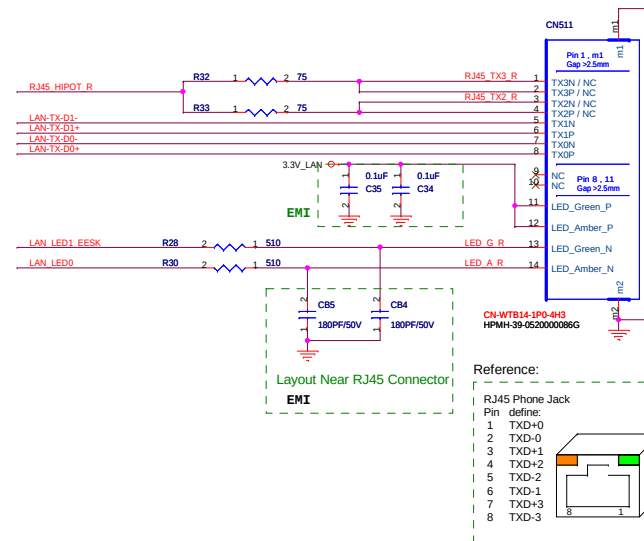
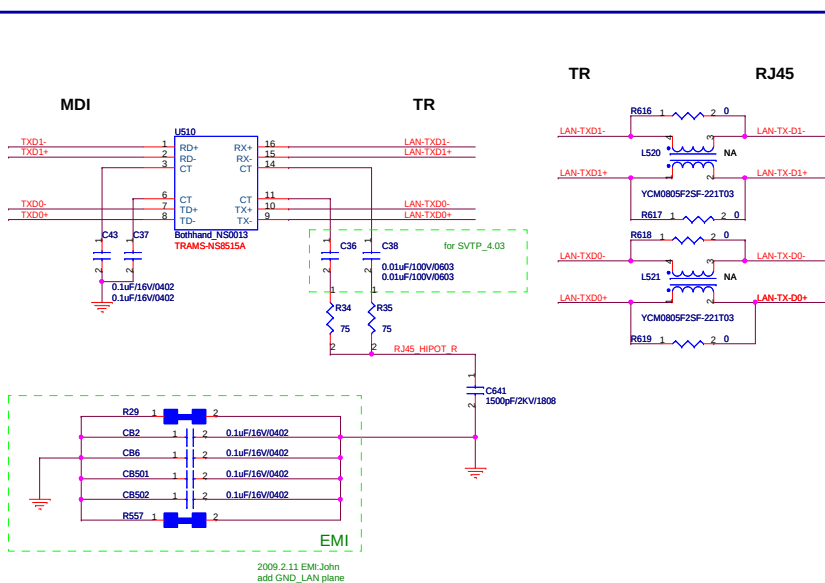
SVTP_v4.03
2.6 - Ethernet Checklist - Rev C.xls

- Ch.3.1.4.4

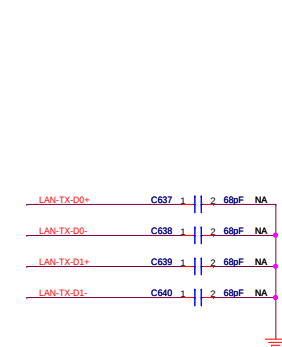
Some older cheap RJ-45s only populate pins 1,2,3,6. 10/100 requires the other 4 pins for grounding. Gigabit Ethernet requires all 8 pins for data signals.

- Ch.3.1.4.13
Resistance from RJ-45 shell to any other chassis ground point (ohms) less than 1 ohm

- Ch.3.1.4.14 & Ch.3.1.4.15
Protection against non-standard power-over-Ethernet (PoE) :
Resistance between pins 1,3 (TXD0P,TXD1P)
and pins 4,7 (TXD2P,TXD3P) of the RJ-45
greater than 58K ohms.



EMI



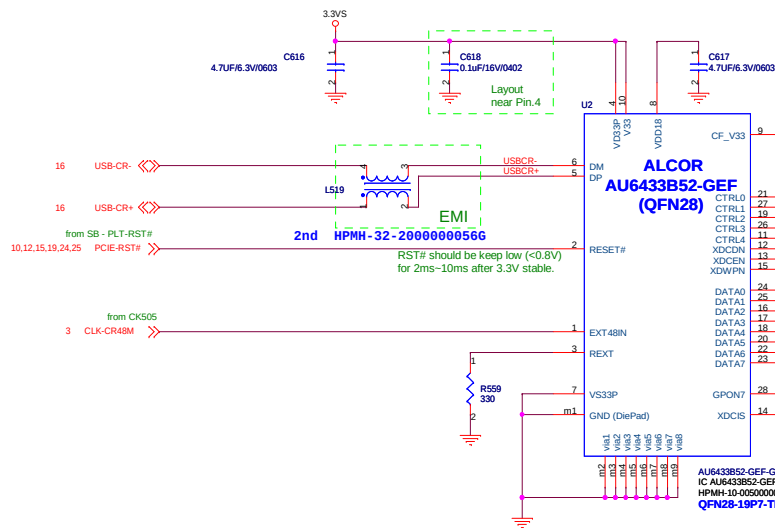
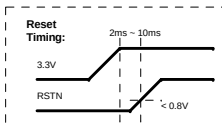
FLEX Computing

Project Name : ARWEN UA1		Title : RTL8103EL (LQFP48)	
Size : C	Document Number : HPMH-40GAB4000-D000		Rev : D
Date: Monday, August 17, 2009		Sheet :	19 of 35

Card Reader

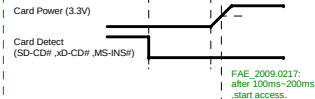
Alicor AU6433-GEF Card supported:

SD v2.0 (SDHC)
MMC v4.2
MS v1.43
MS-PRO v1.03
MS PRO-HG v1.01
xD v1.2



Card Power V33 = 3.3V ~ 2.8V
Card Power OCP = 420mA
FAE_2009.0217:
CF_V33 Internal P/D 1Kohm
for power-off discharge

Card detect Power-In Timing

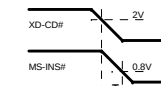


FAE_2009.0117:
Memory Stick Formatter for MS Logo
- Enable

FAE_2009.0117:
SD write protect
- Decided by SD-WP of SD Card

Solution for MS Adapter short issue

when T<128ms,
XD-CD# event will not be affected.

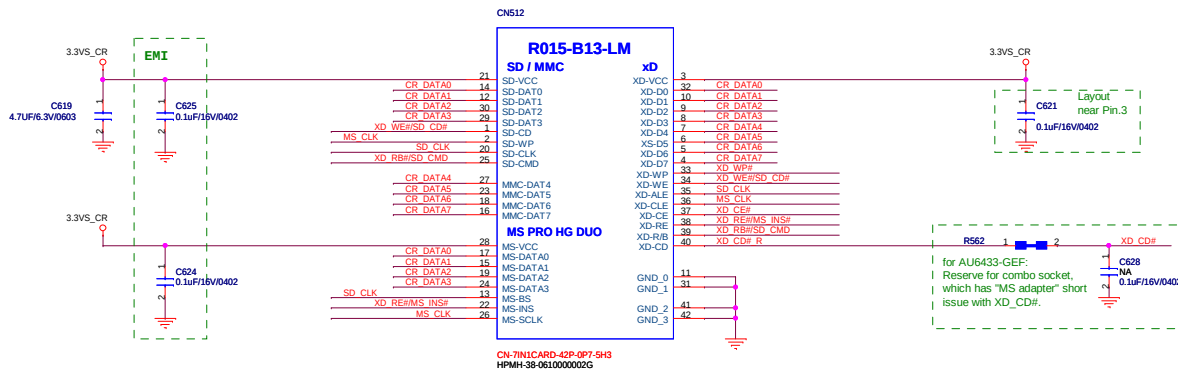


Memory Card Socket

R015-B13-LM
HPMH-38-0610000002G

Card type Supported:

- SD
- SD IO
- MMC
- MMC4.0
- MS
- MS Pro
- xD



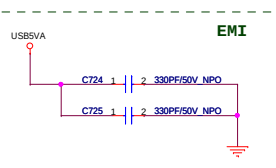
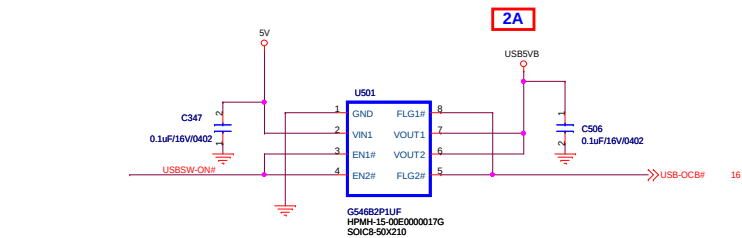
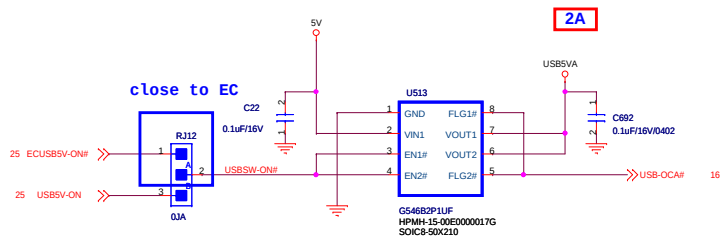
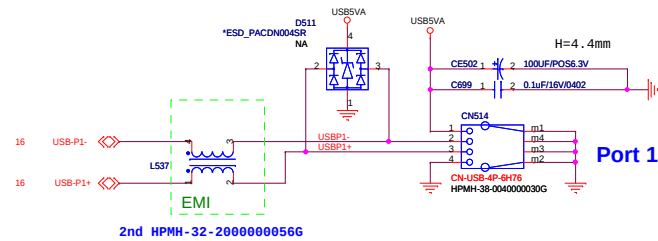
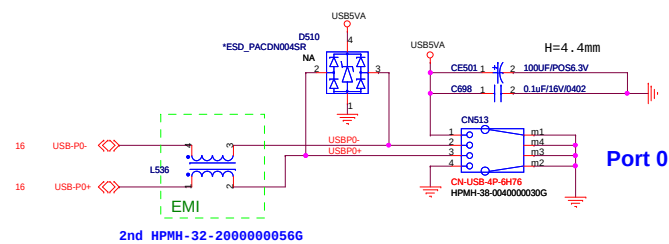
FLEX Computing

Project Name : ARWEN UA1		Title : AU6433-GEF CardReader	
Size : C	Document Number : HPMH-40GAB4000-D000	Rev : D	
Date : Monday, August 17, 2009		Sheet : 20 of 35	

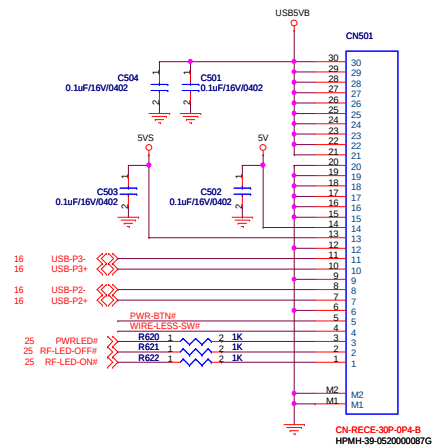
Audio CODEC



USB Port 0 / 1

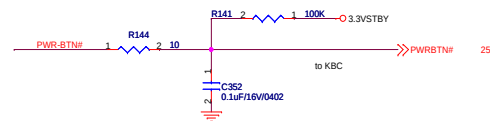


USB DB CONN

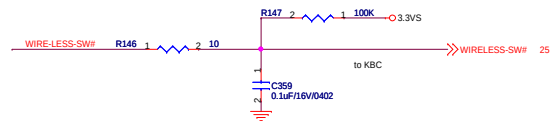


USB Power Connector needs >2A

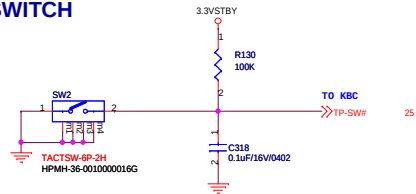
Power ON/OFF Button



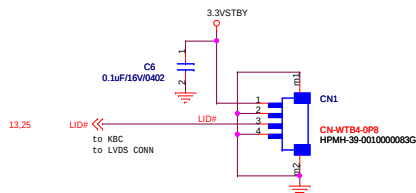
Wireless ON/OFF Button



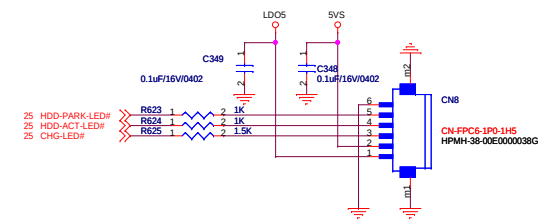
TP LOCK SWITCH



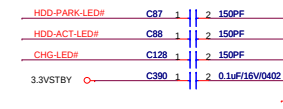
LID Switch



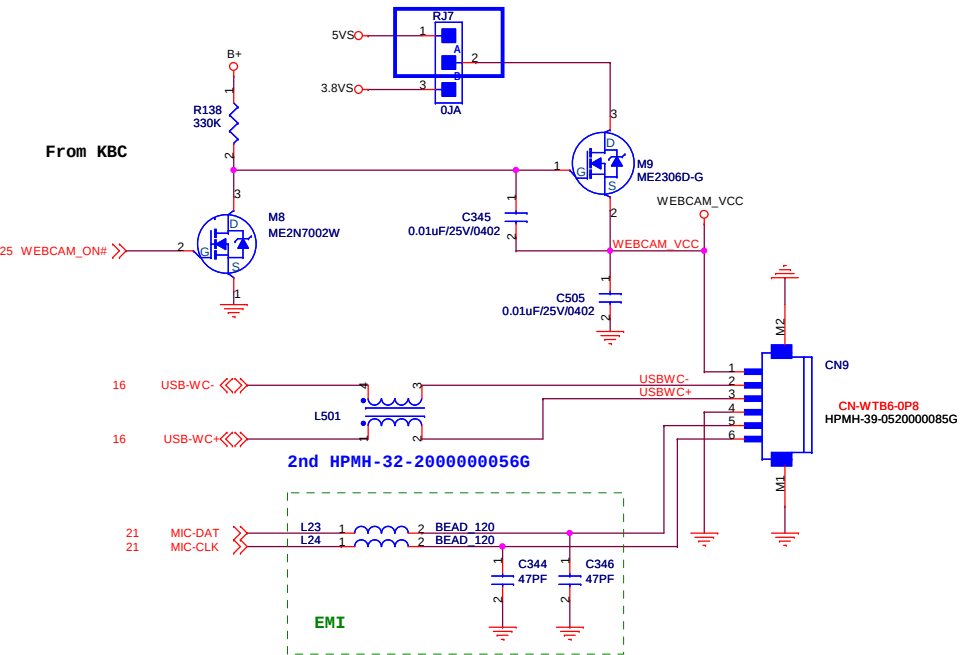
LED DB CONN



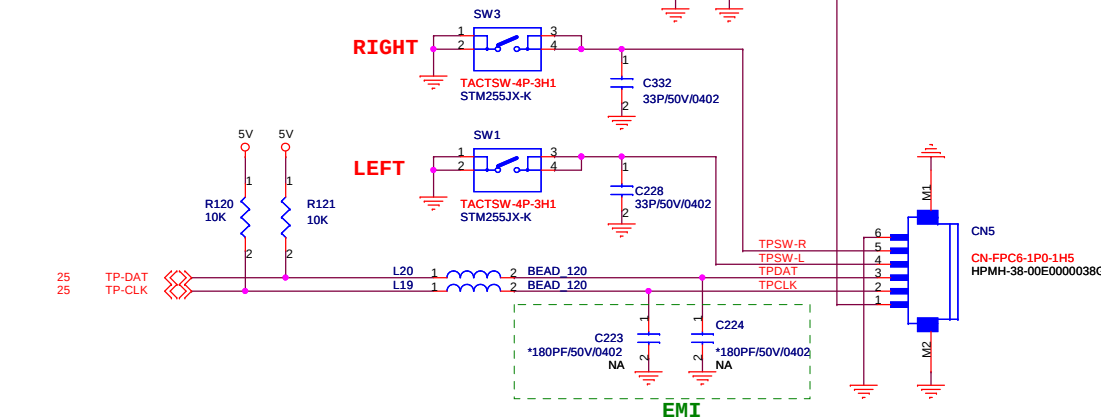
EMI



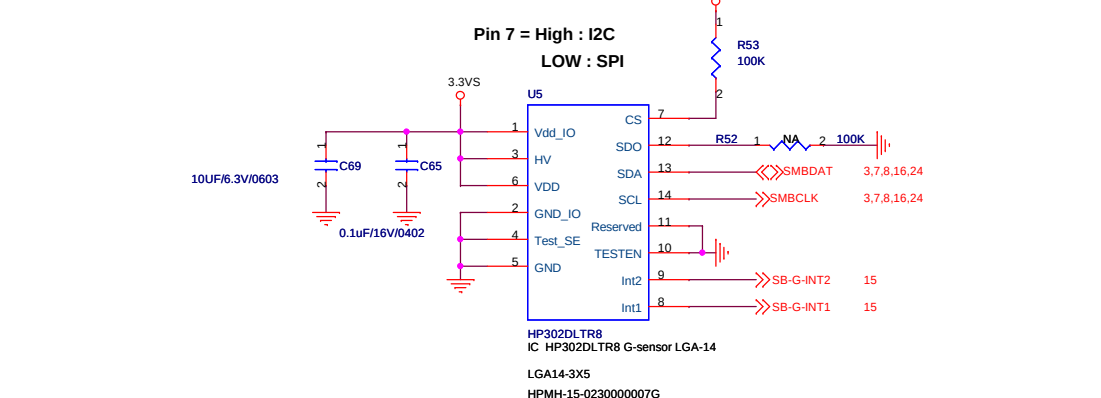
Web CAM



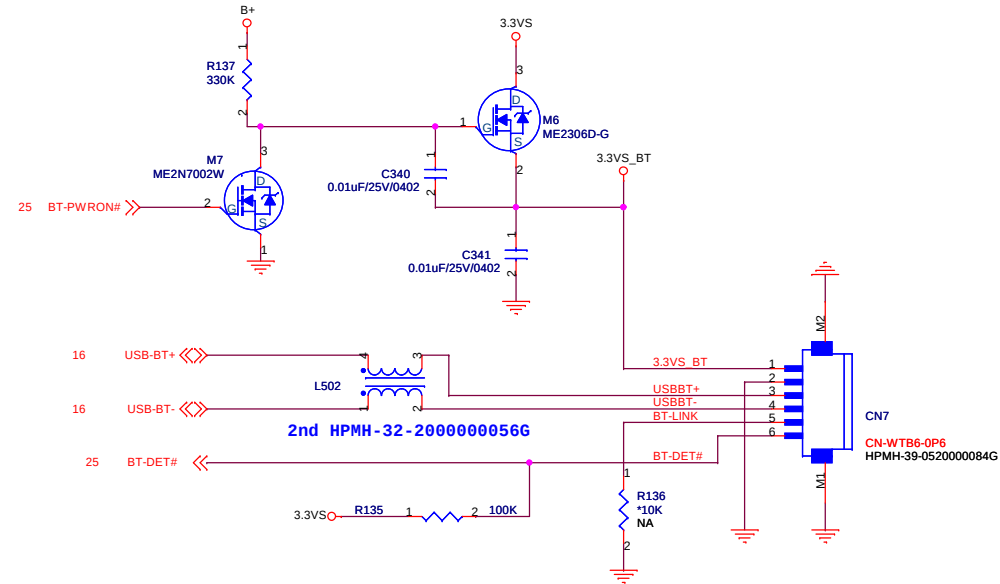
Touch Pad



G-Sensor



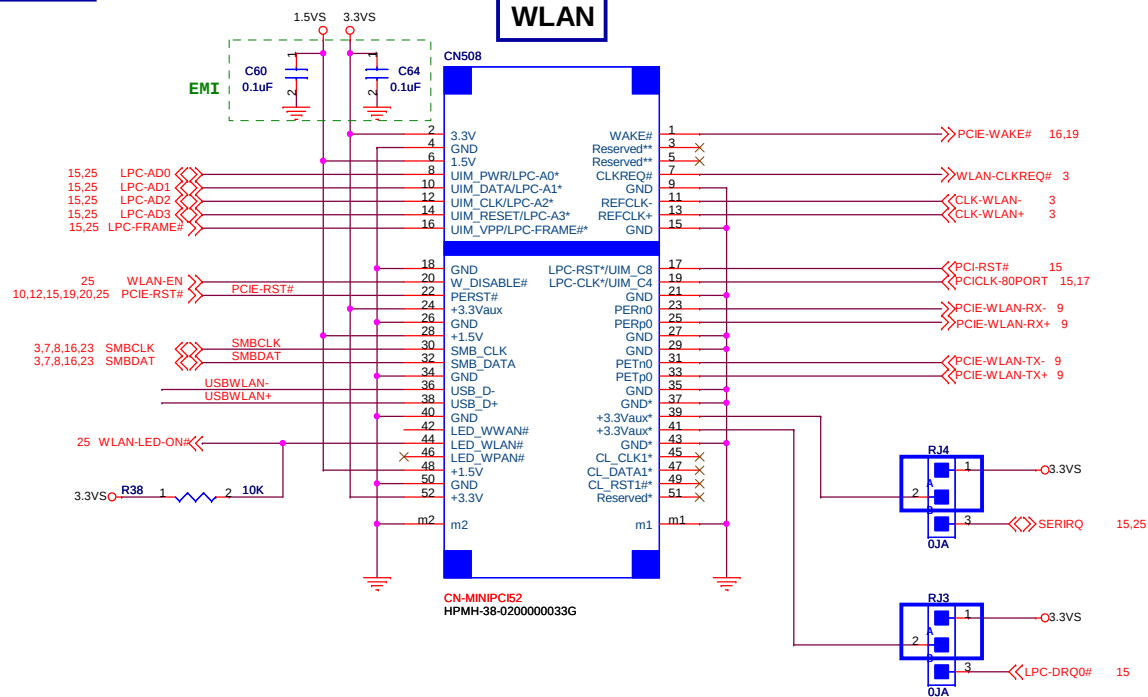
Blue Tooth



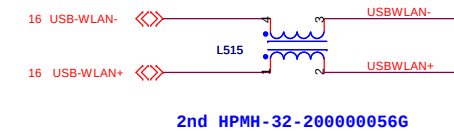
FLEX Computing

Project Name : ARWEN UA1		Title : BT/WEB CAM/TP/G-SENSOR	
Size : Custom	Document Number : HPMH-40GAB4000-D000	Rev : D	
Date : Monday, August 17, 2009		Sheet : 23 of 35	

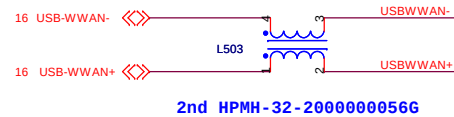
WLAN / WWAN



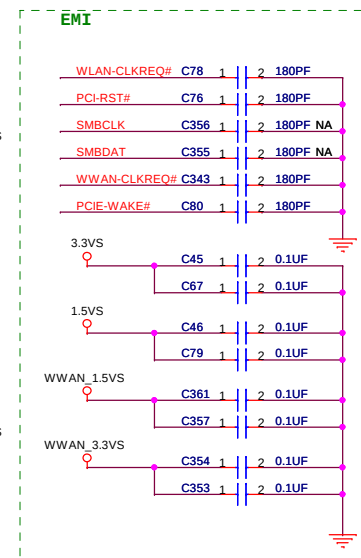
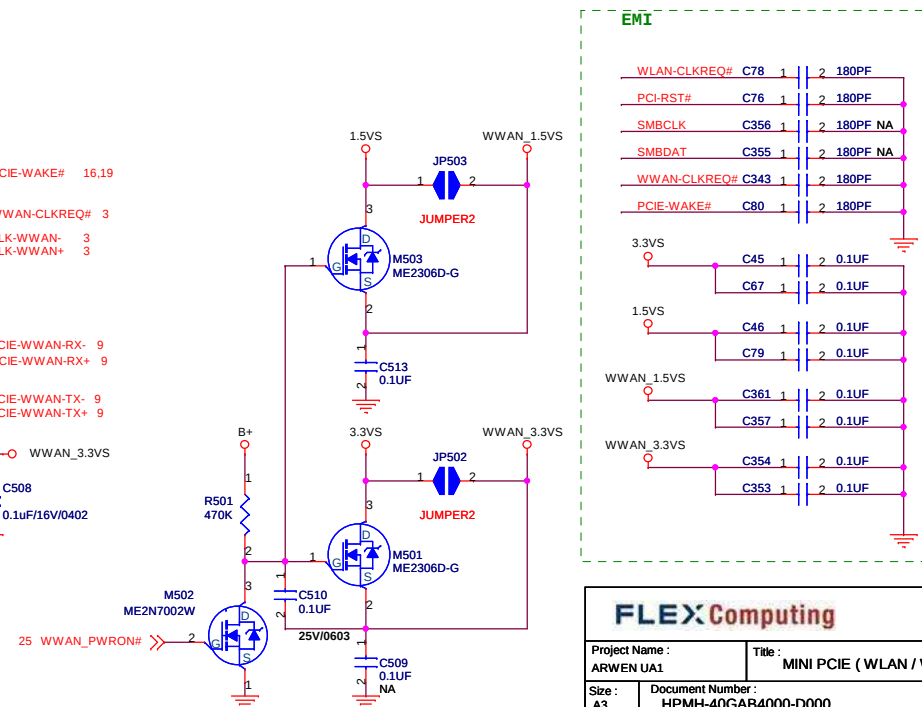
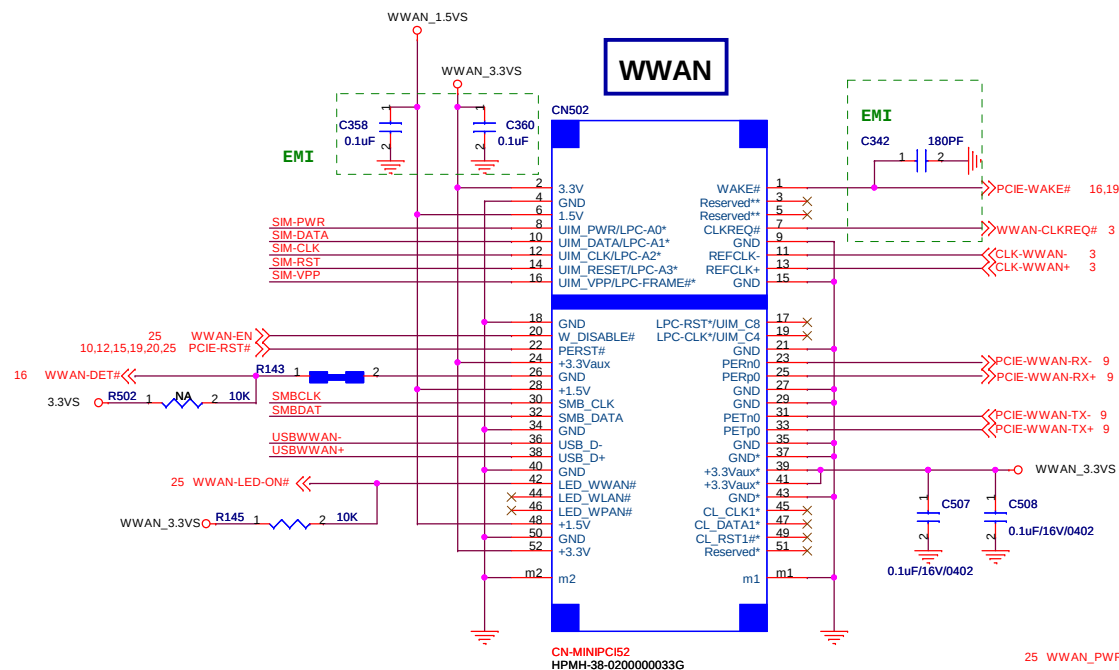
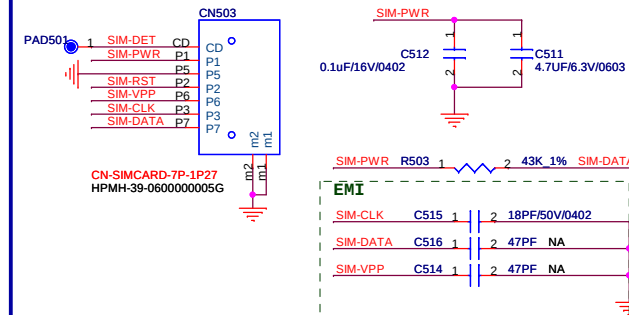
WLAN

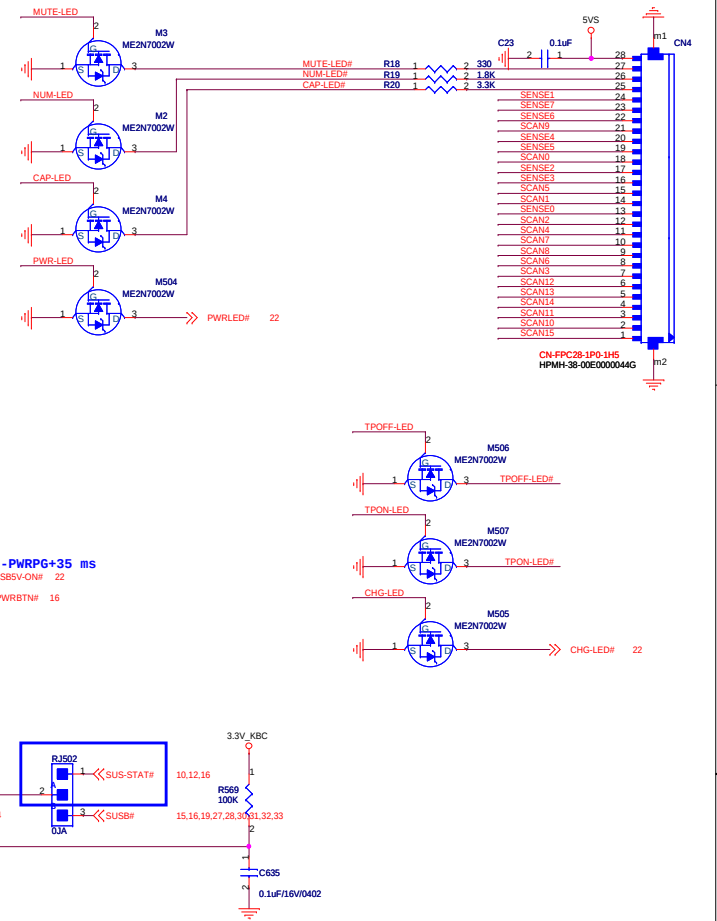
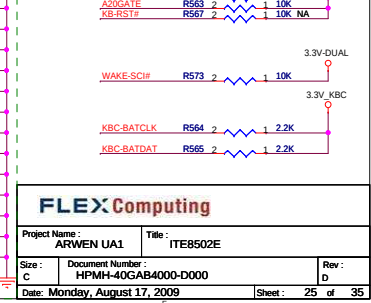
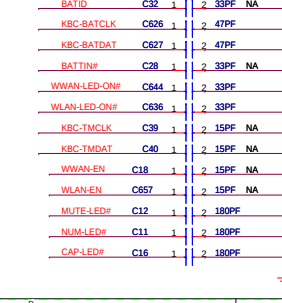
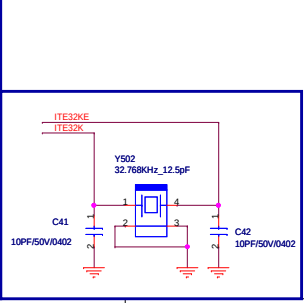
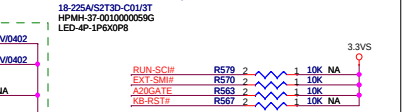


WWAN

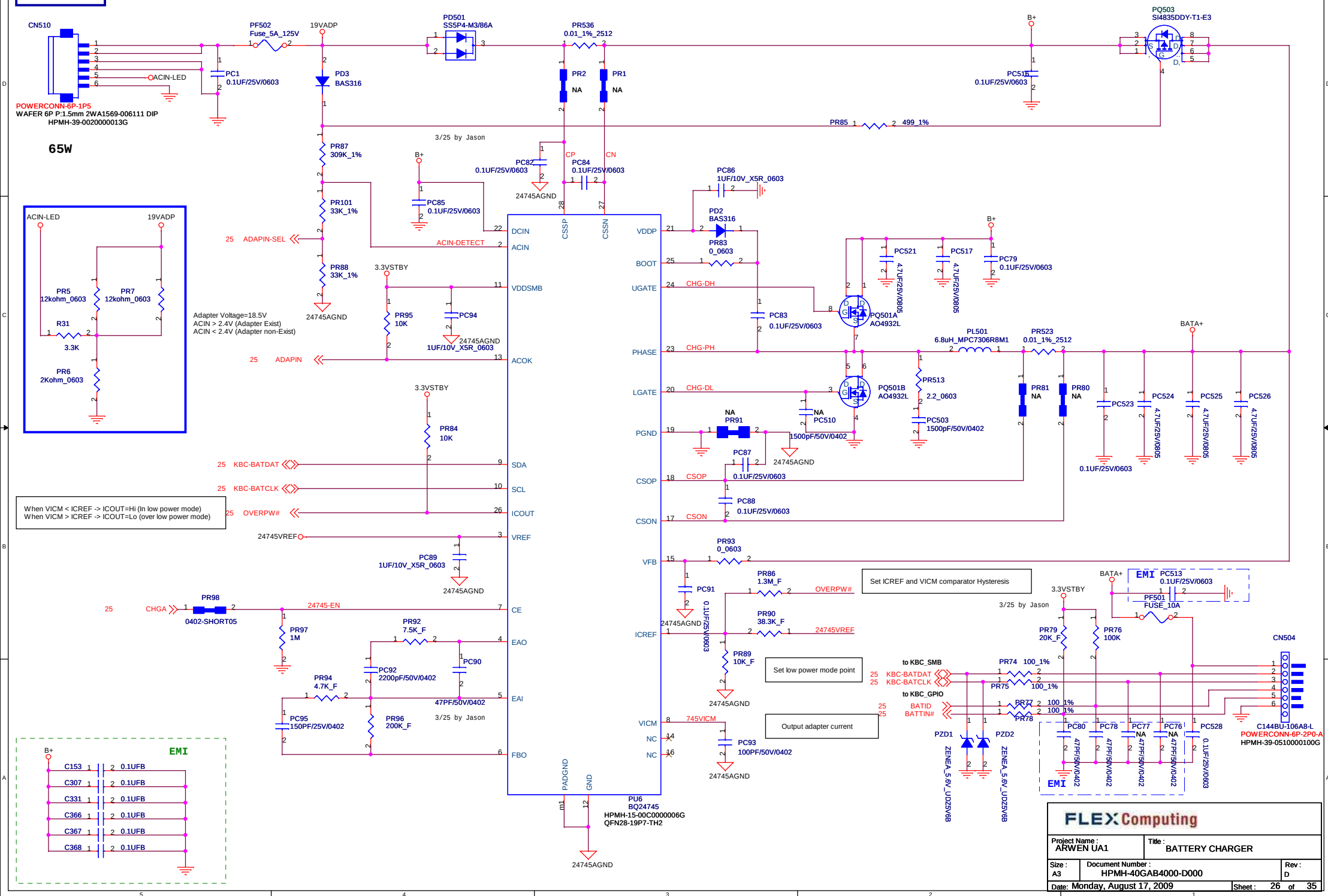


SIM

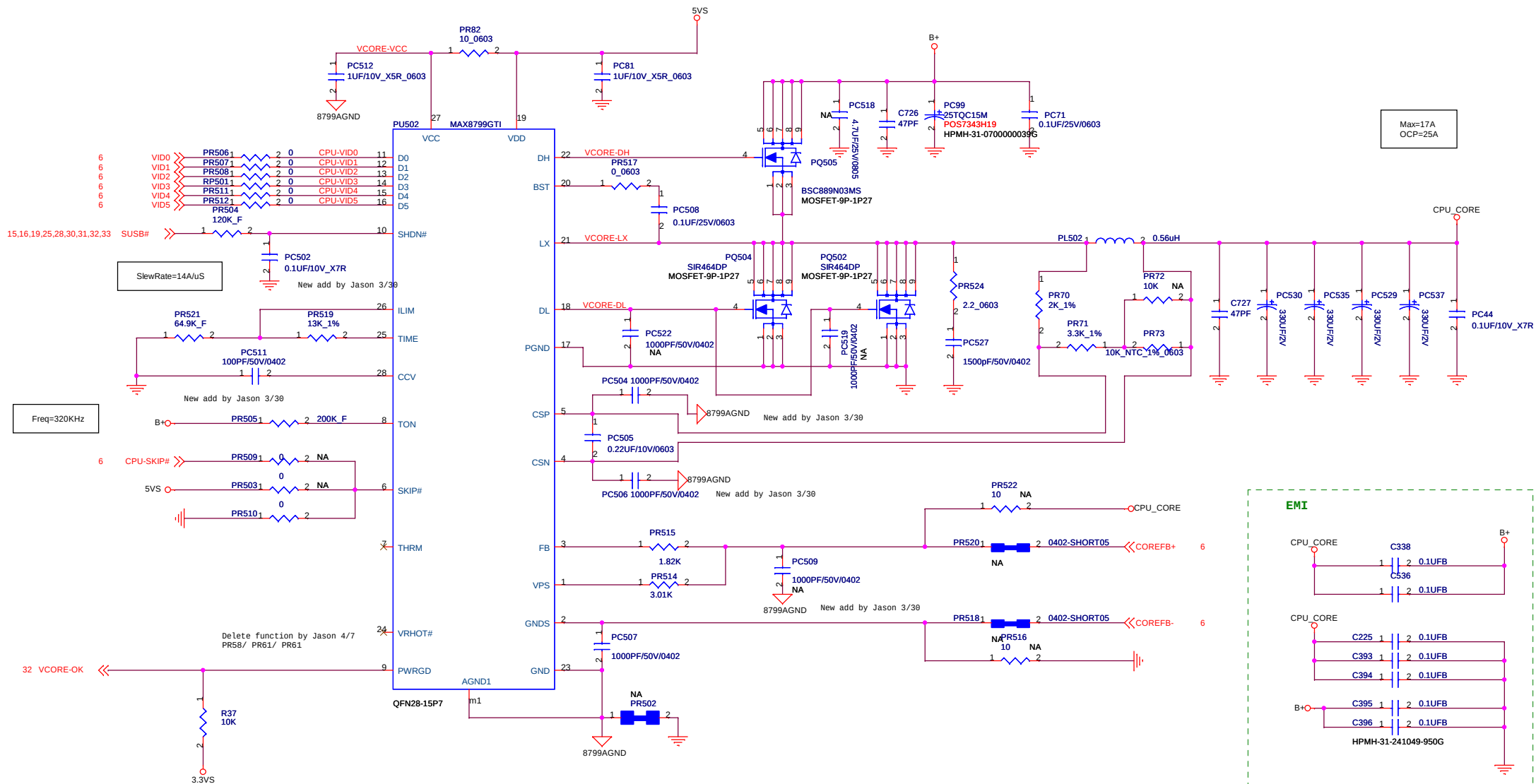


[illegible]

Charger

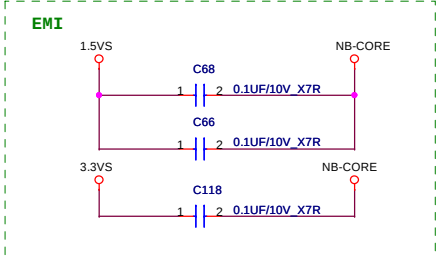
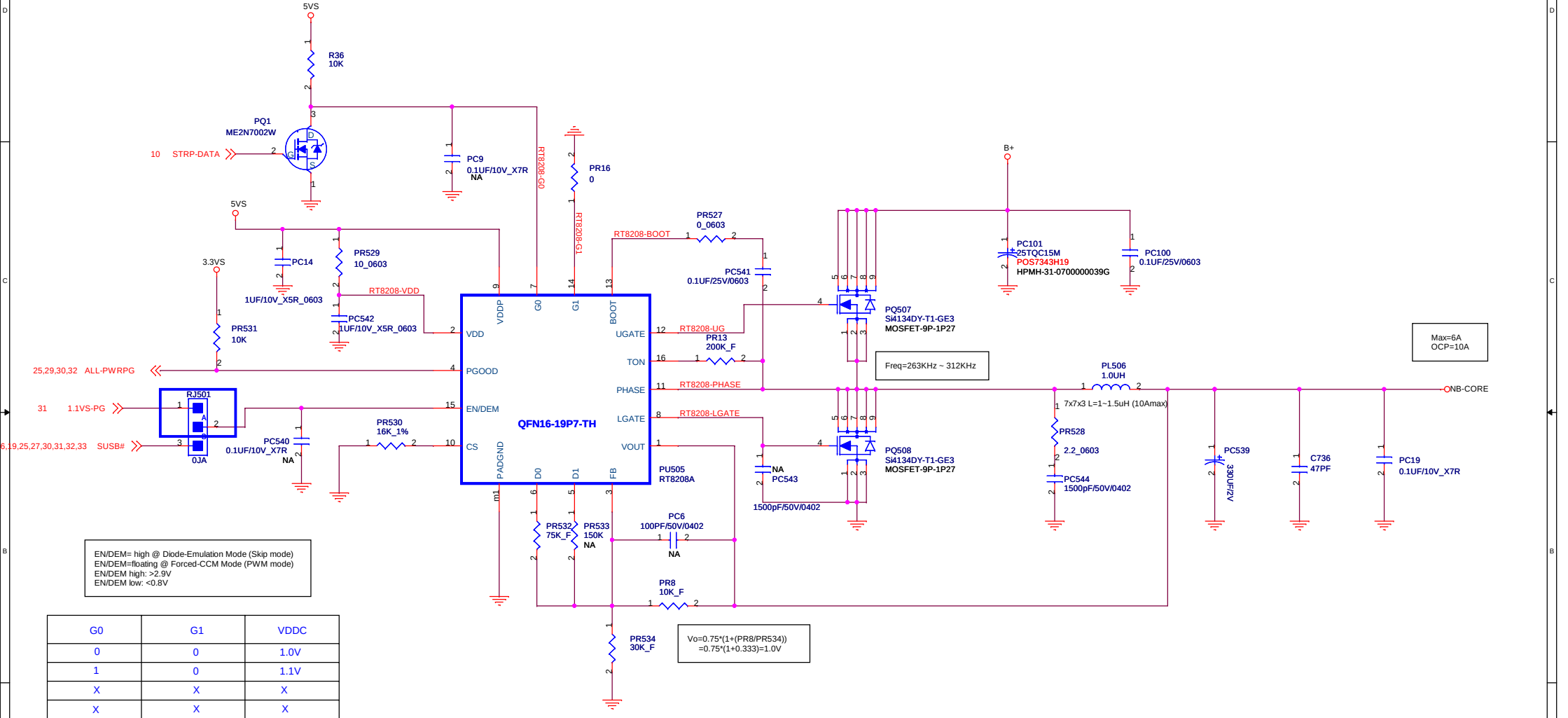


CPU_CORE



CPU Voltage	VID 0	VID 1	VID 2	VID 3	VID 4	VID 5
1.00V	0	1	1	0	1	0
1.05V	0	0	1	0	1	0
1.10V	0	1	0	0	1	0

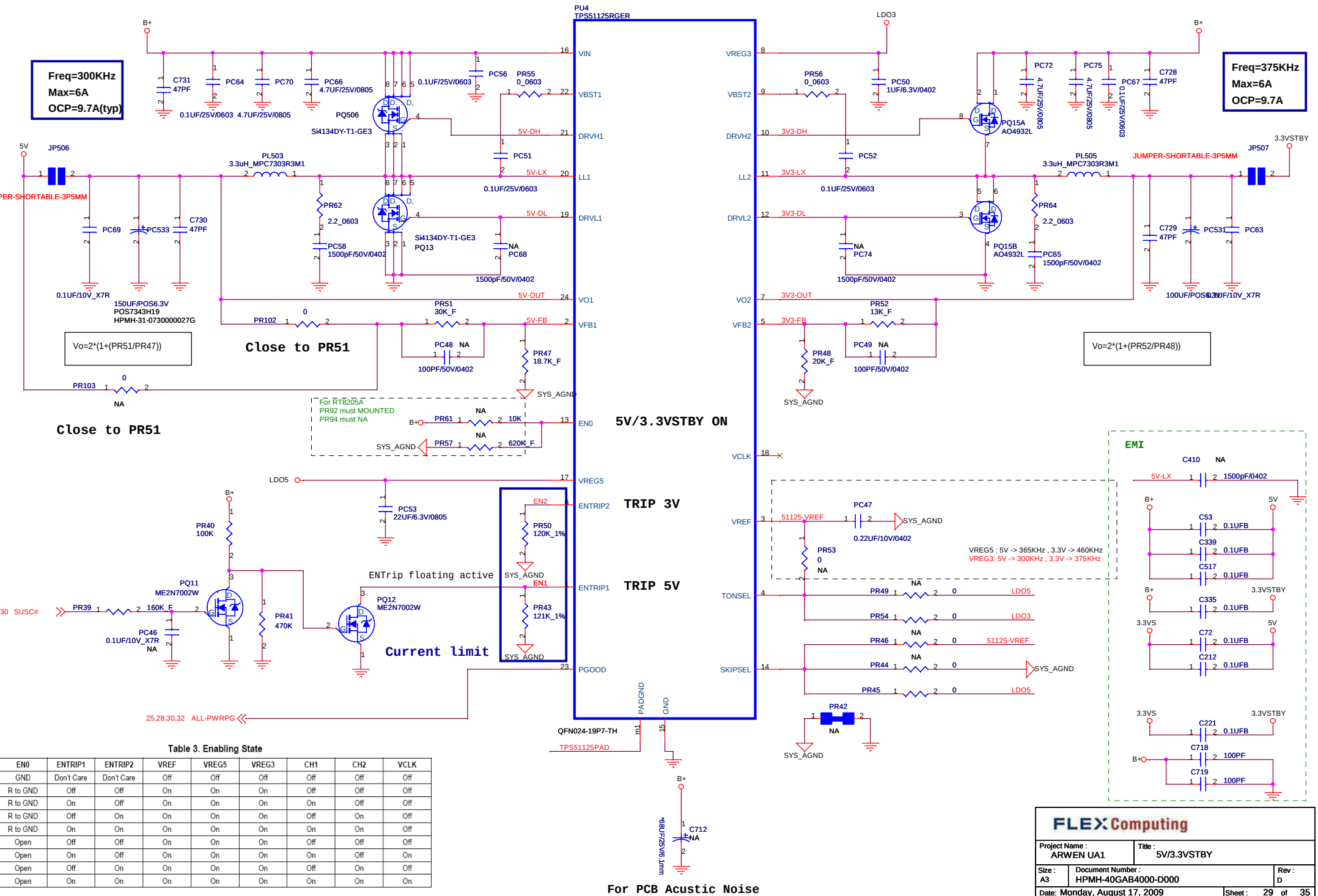
NB_CORE



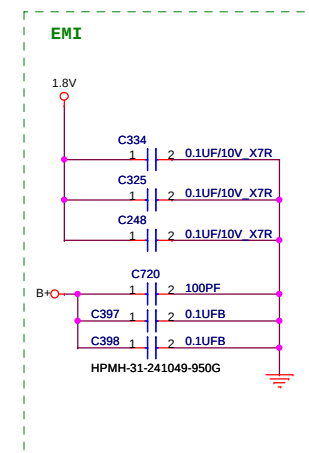
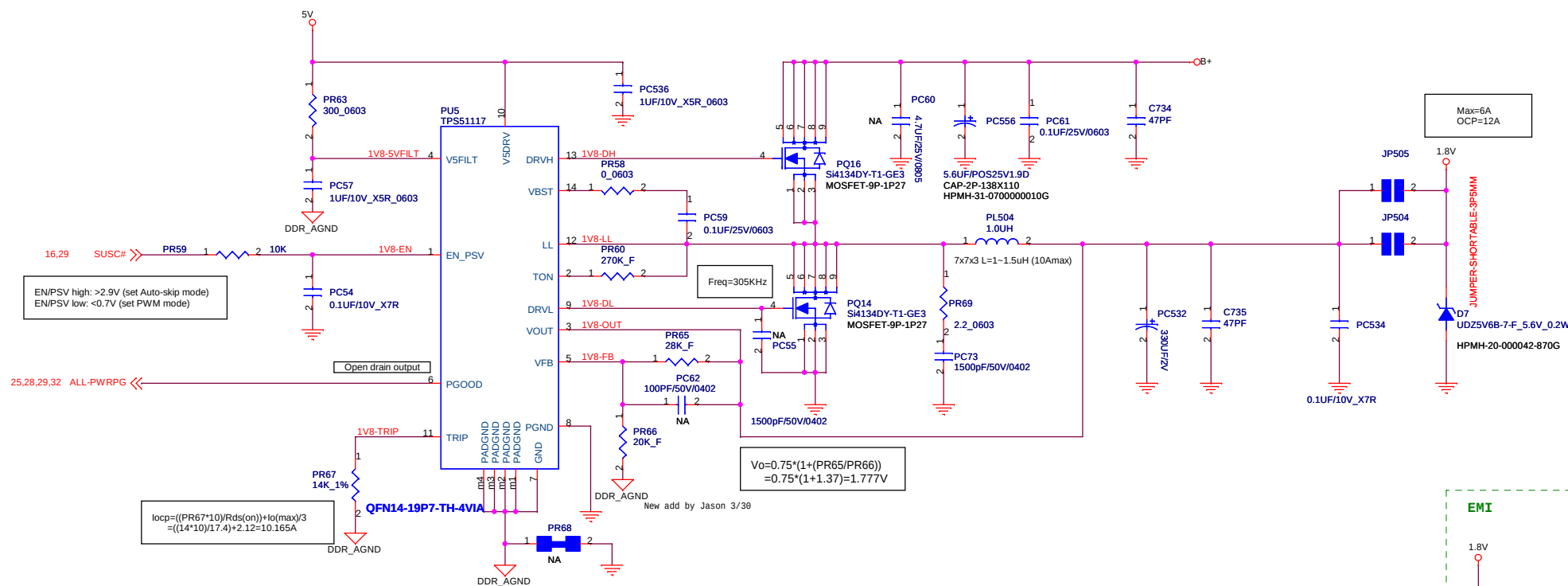
5V / 3.3VSTBY

Freq=300KHz
Max=6A
OCP=9.7A(1typ)

Freq=375KHz
Max=6A
OCP=9.7A



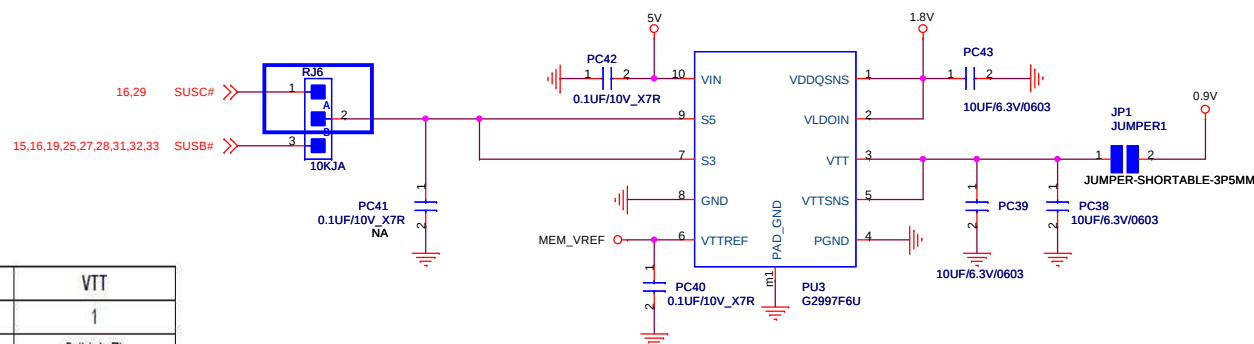
1.8V / 0.9V



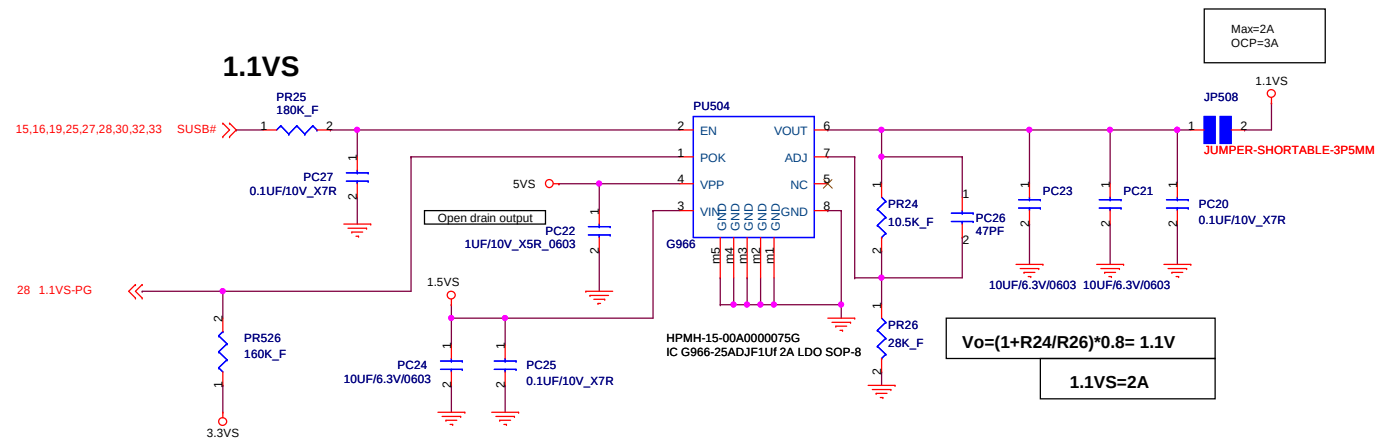
S3 and S5 Control Tabl

STATE	S3	S5	VTTREF	VTT
S0	H	H	1	1
S3 ⁽¹⁾	L	H	1	0 (high-Z)
S4/S5 ⁽¹⁾	L	L	0 (discharge)	0 (discharge)

(1) In case S3 is forced to H and S5 to L, VTTREF is discharged and VTT is at High-Z state. This condition is NOT recommended.



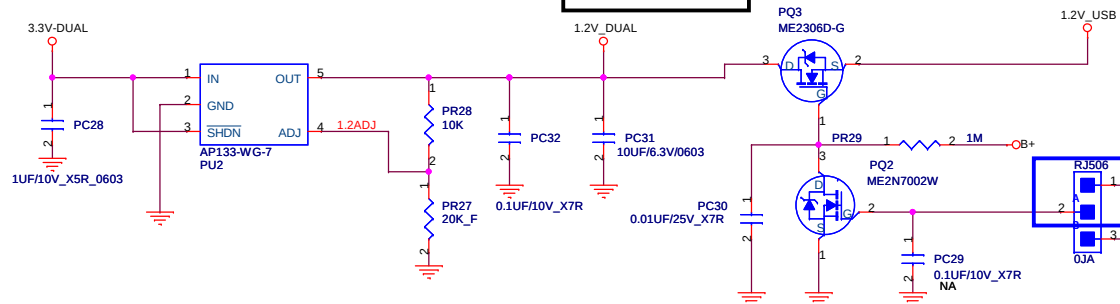
1.1VS



1.2VSTBY / 1.2V_USB

$$V_o = 0.8 * (1 + (PR160/PR162)) = 0.8 * (1 + 0.5) = 1.2V$$

1.2V_DUAL=250mA

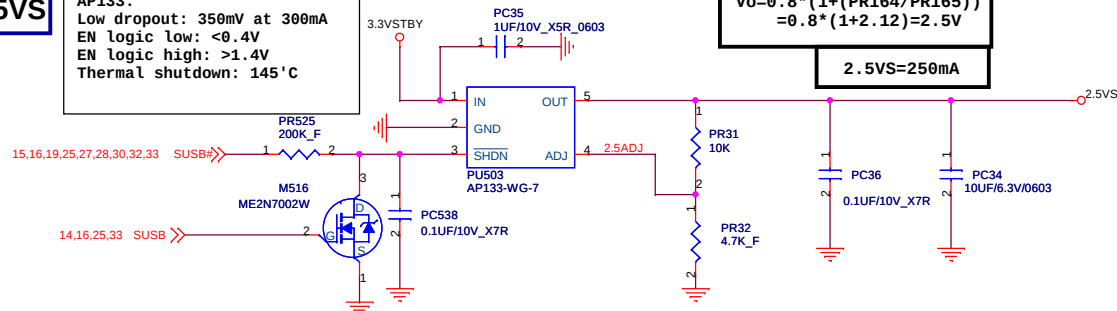


2.5VS

AP133:
Low dropout: 350mV at 300mA
EN logic low: <0.4V
EN logic high: >1.4V
Thermal shutdown: 145°C

$$V_o = 0.8 * (1 + (PR164/PR165)) = 0.8 * (1 + 2.12) = 2.5V$$

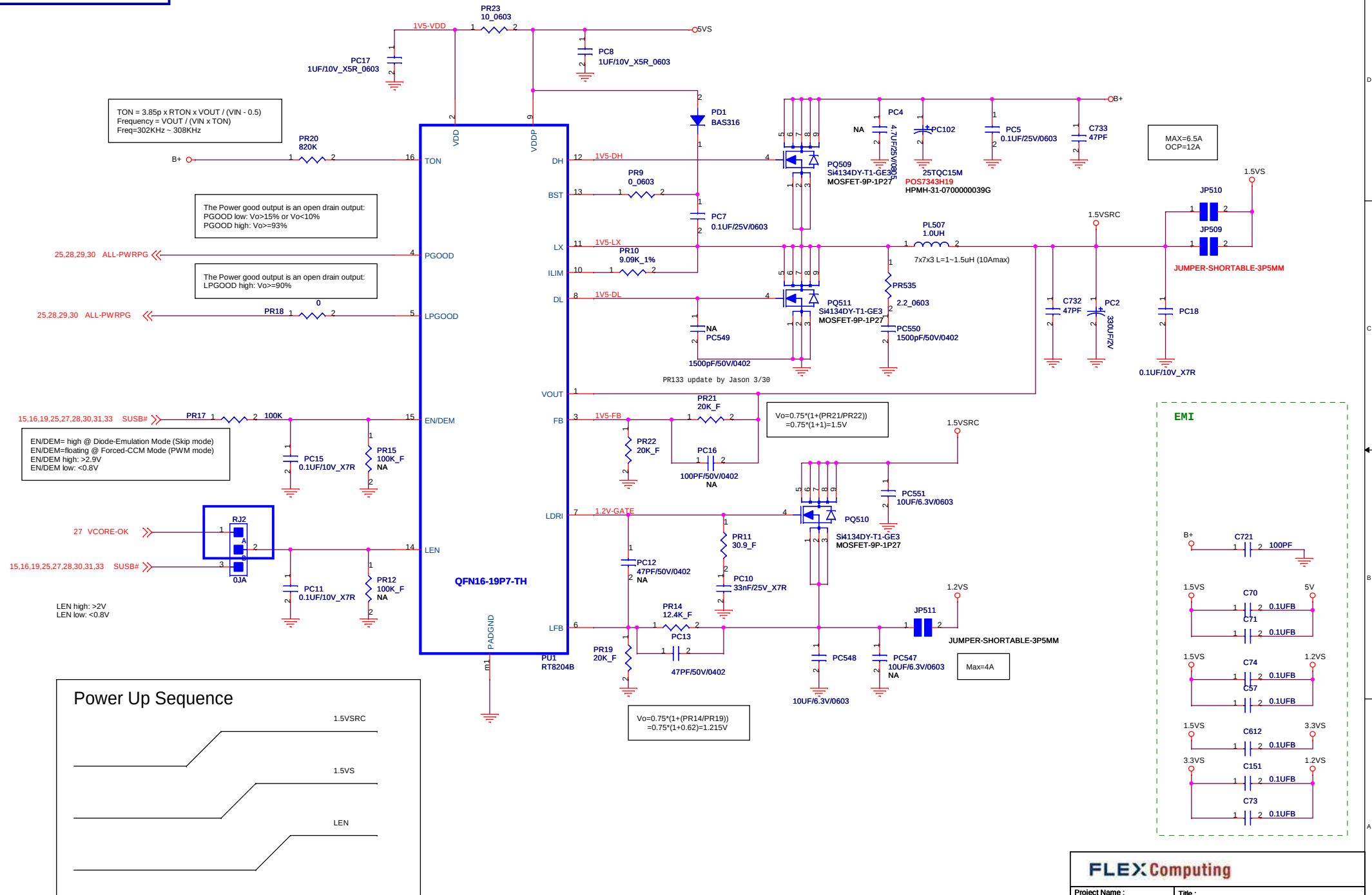
2.5VS=250mA



FLEXComputing

Project Name : ARWEN UA1		Title : 1.1VS/2.5VS/1.2V_USB	
Size : A3	Document Number : HPMH-40GAB4000-D000		Rev : D
Date: Monday, August 17, 2009		Sheet: 31 of 35	

1.5VS / 1.2VS



FLEXComputing

Project Name : ARWEN UA1		Title : 1.5VS/1.2VS	
Size : Custom	Document Number : HPMH-40GAB4000-D000		Rev : D
Date: Monday, August 17, 2009		Sheet: 32 of 35	

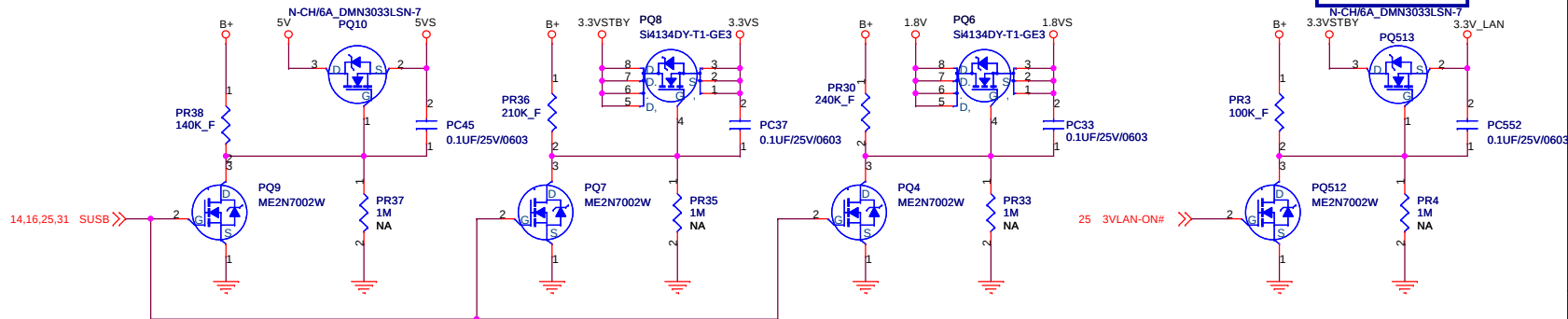
S4/S3 OFF

5VS

3.3VS

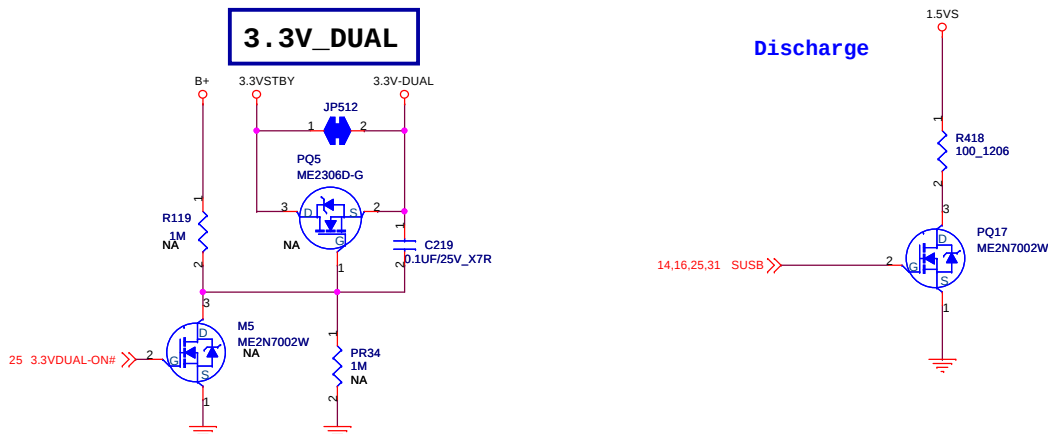
1.8VS

LAN_3.3V



3.3V_DUAL

Discharge

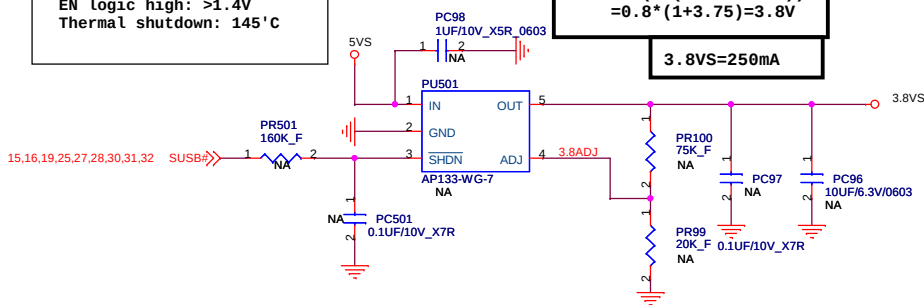


AP133:
Low dropout: 350mV at 300mA
EN logic low: <0.4V
EN logic high: >1.4V
Thermal shutdown: 145°C

3.8VS

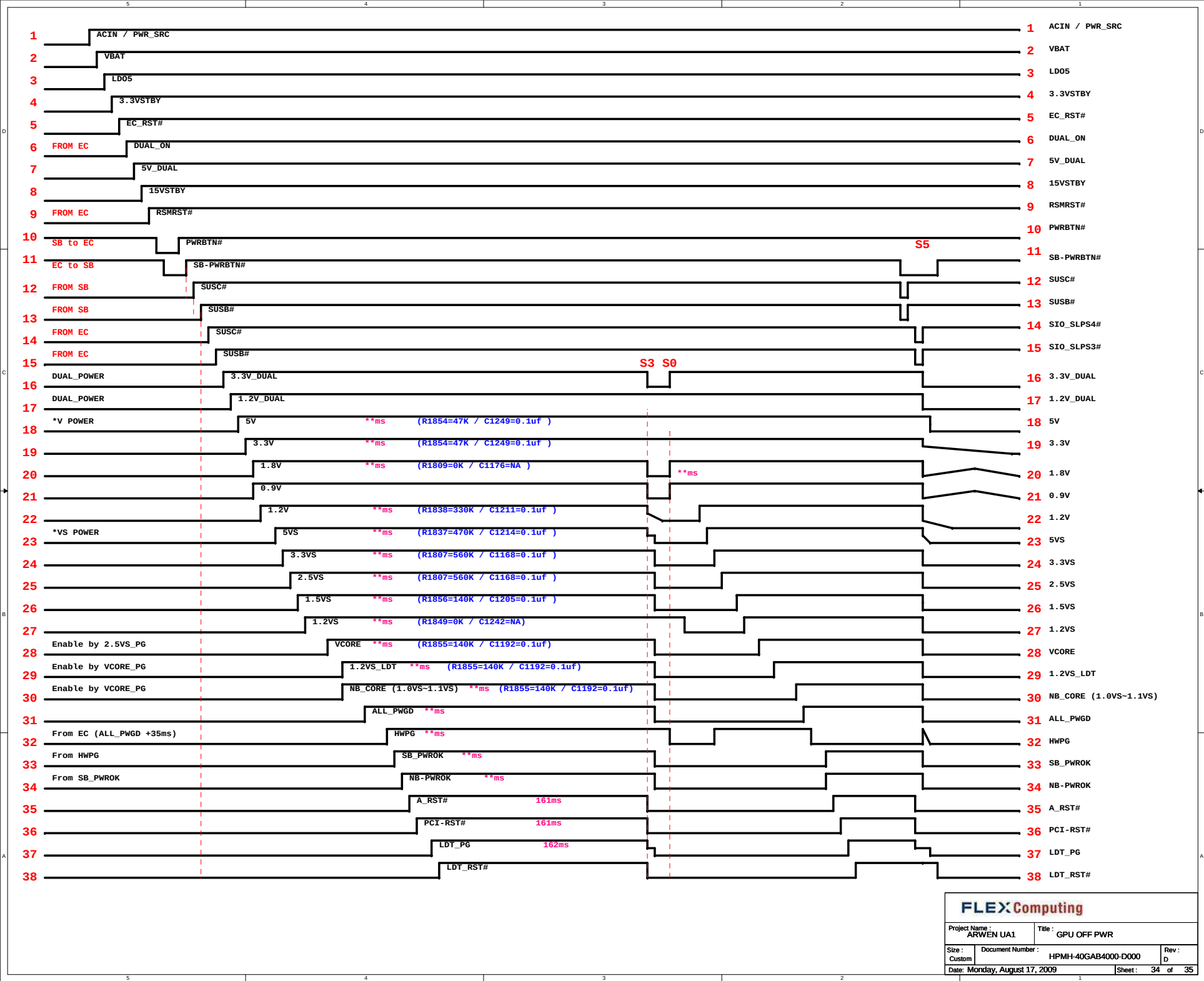
$$V_o = 0.8 * (1 + (PR100 / PR99)) = 0.8 * (1 + 3.75) = 3.8V$$

3.8VS=250mA



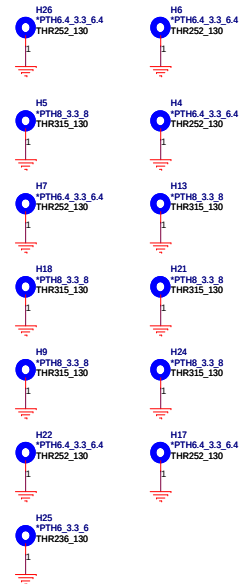
FLEX Computing

Project Name : ARWEN UA1		Title : VVS/VGA POWER	
Size : Custom	Document Number : HPMH-40GAB4000-D000		Rev : D
Date: Monday, August 17, 2009		Sheet : 33 of 35	

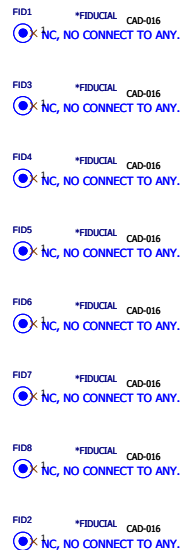


Screw Hole

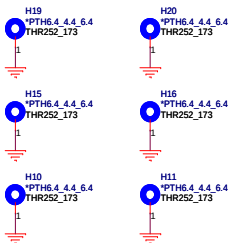
MB x 16



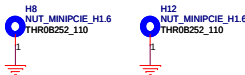
FID



CPU/VGA x 8



MINI CARD x 2



EMI x 2

