

Compal confidential

Schematics Document

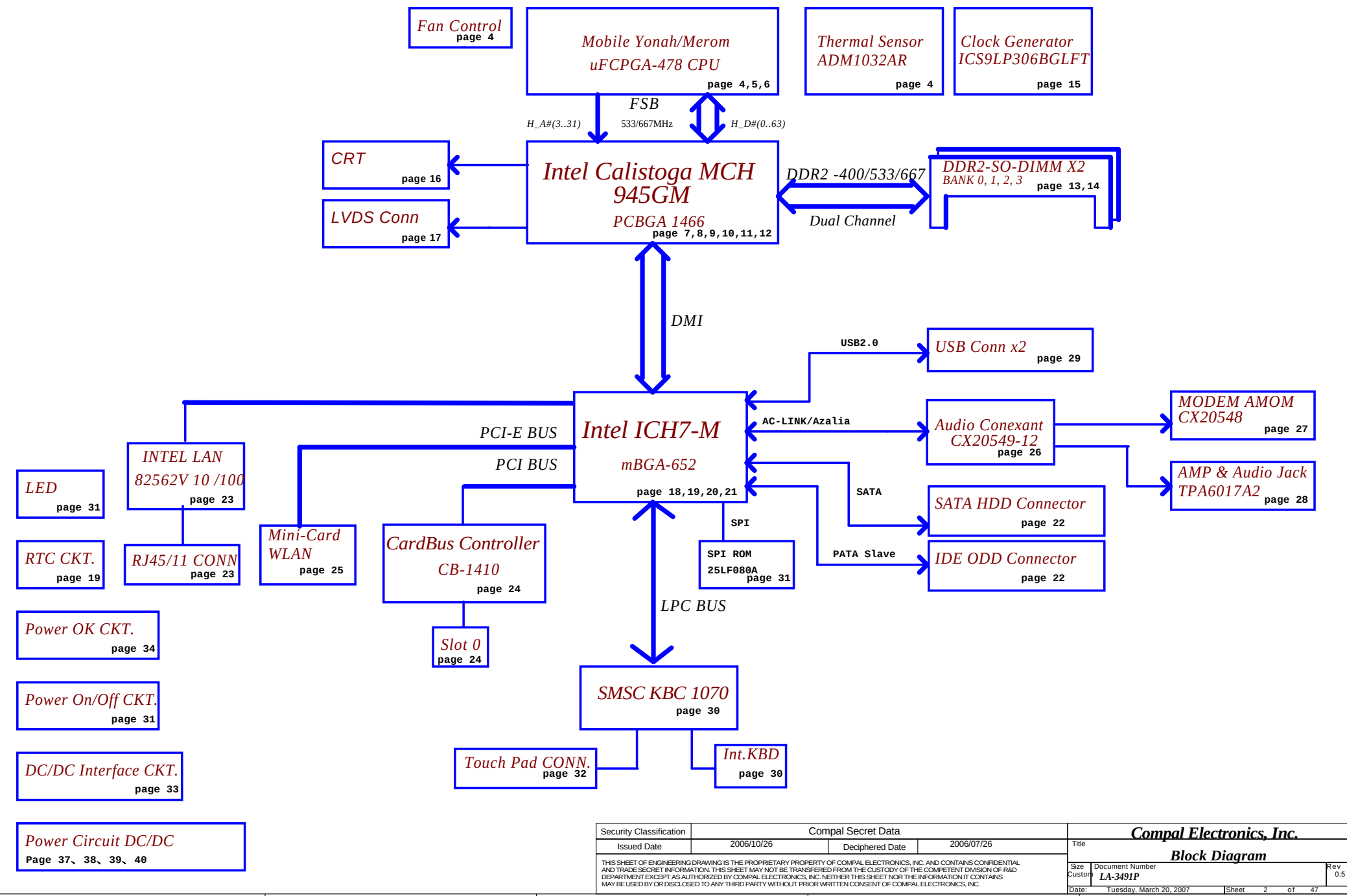
Mobile Yonah uFCPGA with Intel Calistoga_GM+ ICH7-M core logic

2007-03-20

REV:0.5

Security Classification		Compal Secret Data		Title	
Issued Date	2006/10/26	Deciphered Date	2006/07/26	Cover Sheet	
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Volga 2.0



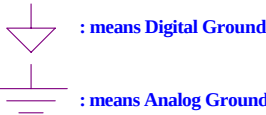
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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (18.5V)	NA	NA	NA
B+	AC or battery power rail for power circuit	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V power rail for Processor I/O and MCH/ICH core power	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_VCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Symbol Note :



NOXDP@ : means just build when XDP function disable.
LP@ : means just build when Low power clock gen. install
BATT@ : means need be mounted when 45 level assy or rework stage.
45@ : means need be mounted when 45 level assy or rework stage.
14@ : means need be mounted when 14.1"
WLAN@ : means need be mounted when have wireless LED Function
WLAN14@ : means need be mounted when have wireless LED Function and 14"

XDP@ : means just build when XDP function enable. When this time, docking PCI express will not work.
CONN@ : means ME parts
Debug@ : means Mini debug card use

Calistoga 945GM R3 SA0000059L0

Calistoga 945GM R1 SA0000059A0

Calistoga 940GML R3 SA000011C10

Calistoga 940GML R1 SA000011C00

ICH7 R3 SA00000V1A0

ICH7 R1 SA00000V1F0

IAT50 945GM FF 46147932L01

IAT50 940GML DF 46147932L02

IAT50 940GML DF 46147932L03 (No WLAN)

IAT60 945GM FF 46147932L21

IAT60 940GML DF 46147932L22

IAT60 940GML DF 46147932L23 (No WLAN)

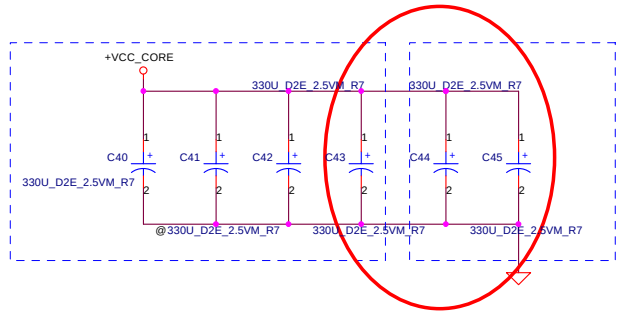
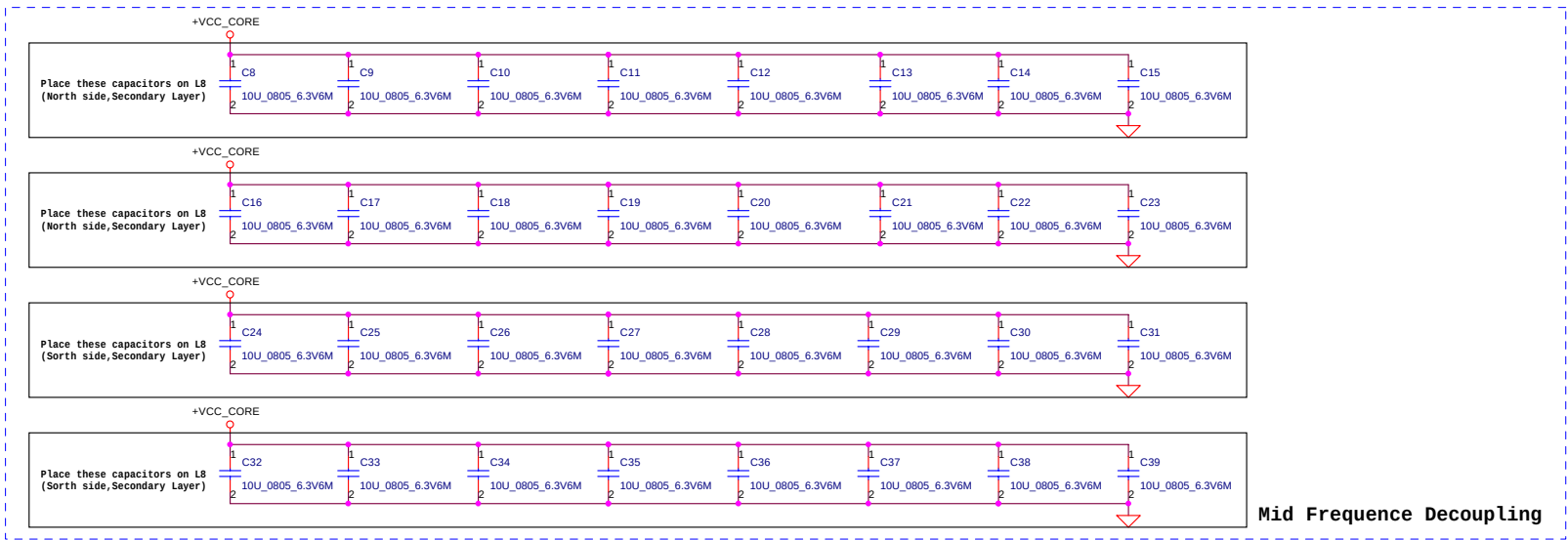
External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
CARD BUS	D6	AD22	2	C

I2C / SMBUS ADDRESSING

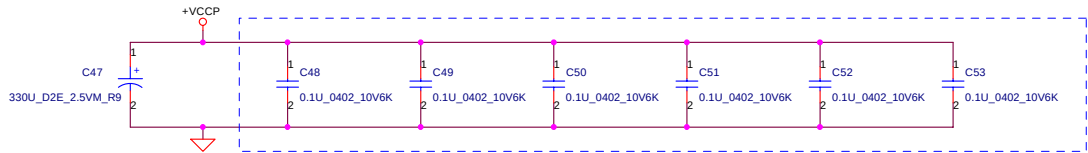
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

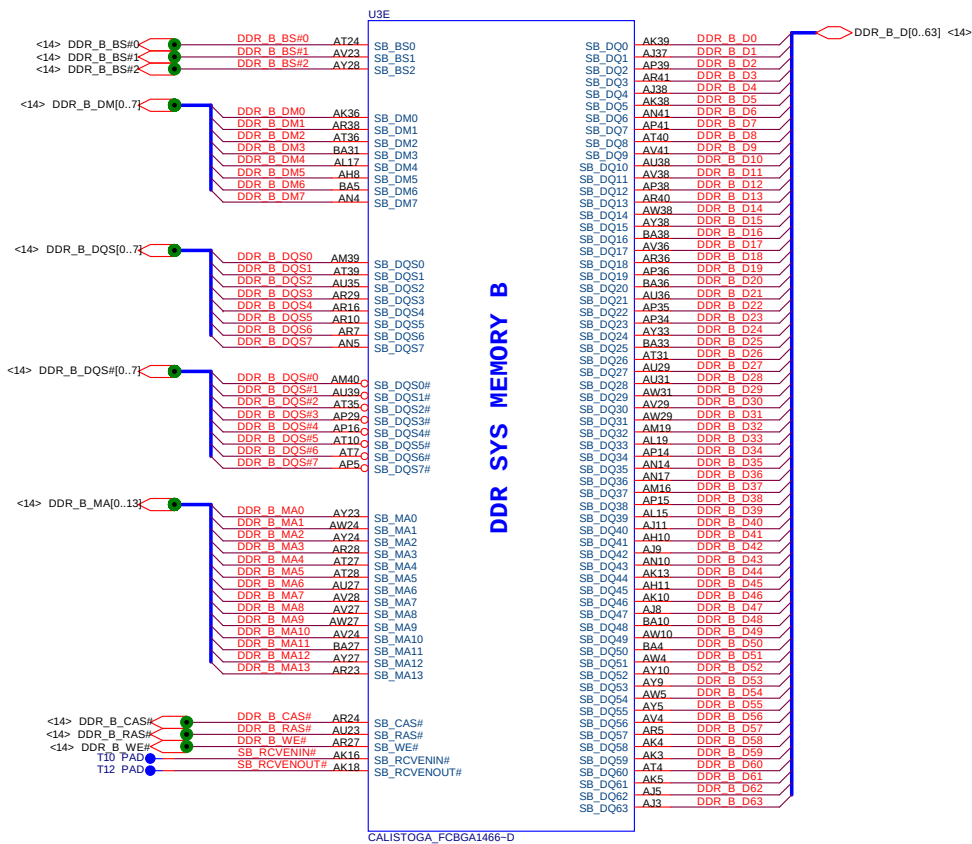
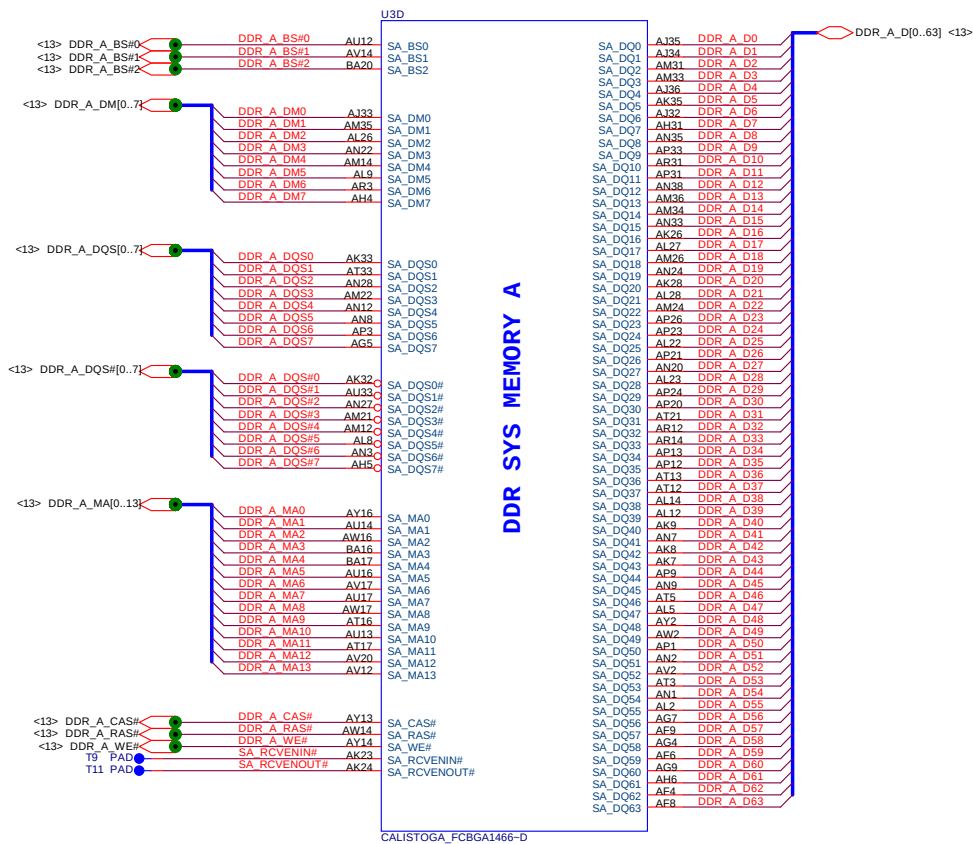
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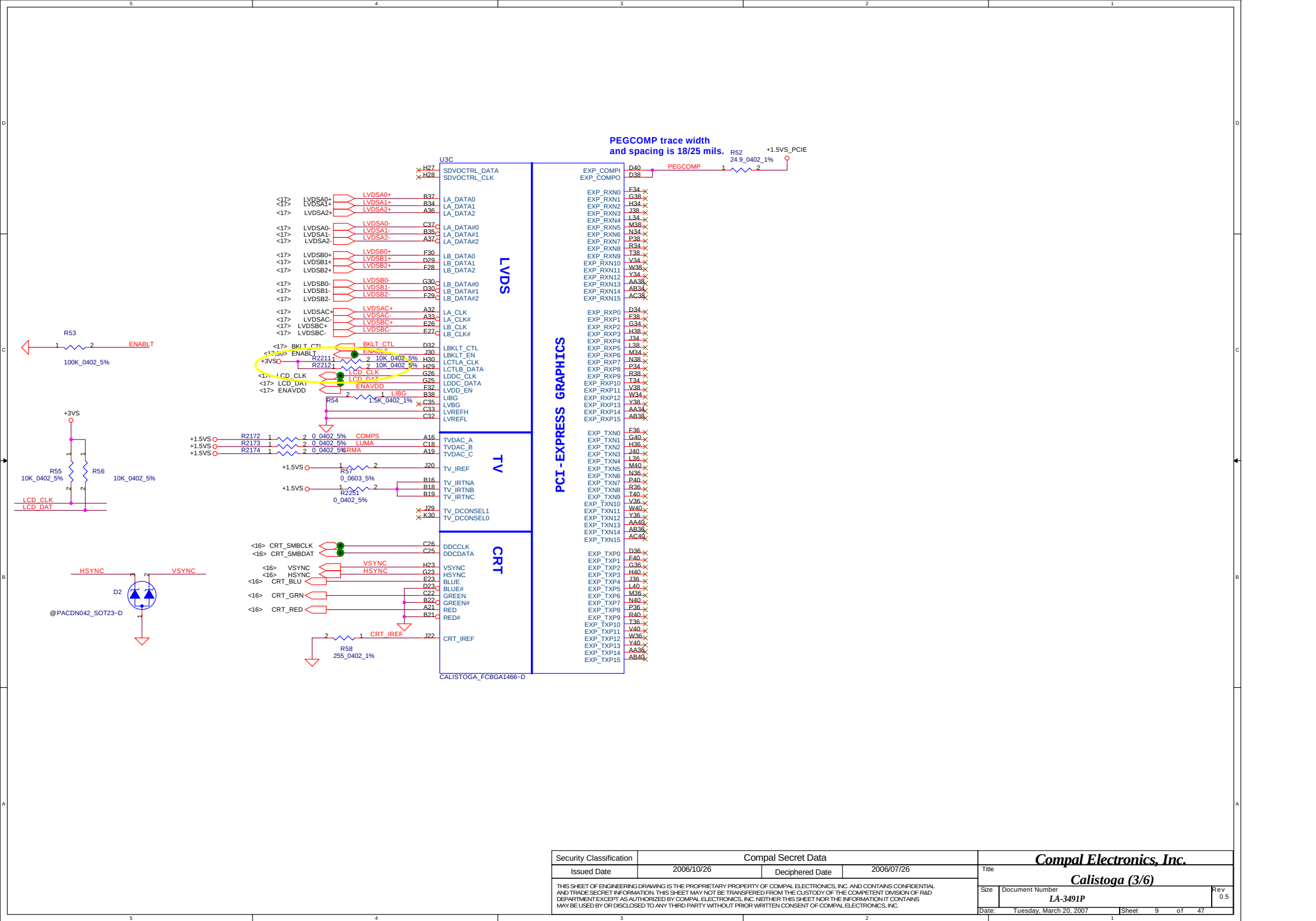
ESR $\leq$ 1.5m ohm
Capacitor > 1980uF

02/26 Change C43, C44, C45 to
1.9mm height for PV build short
term solution

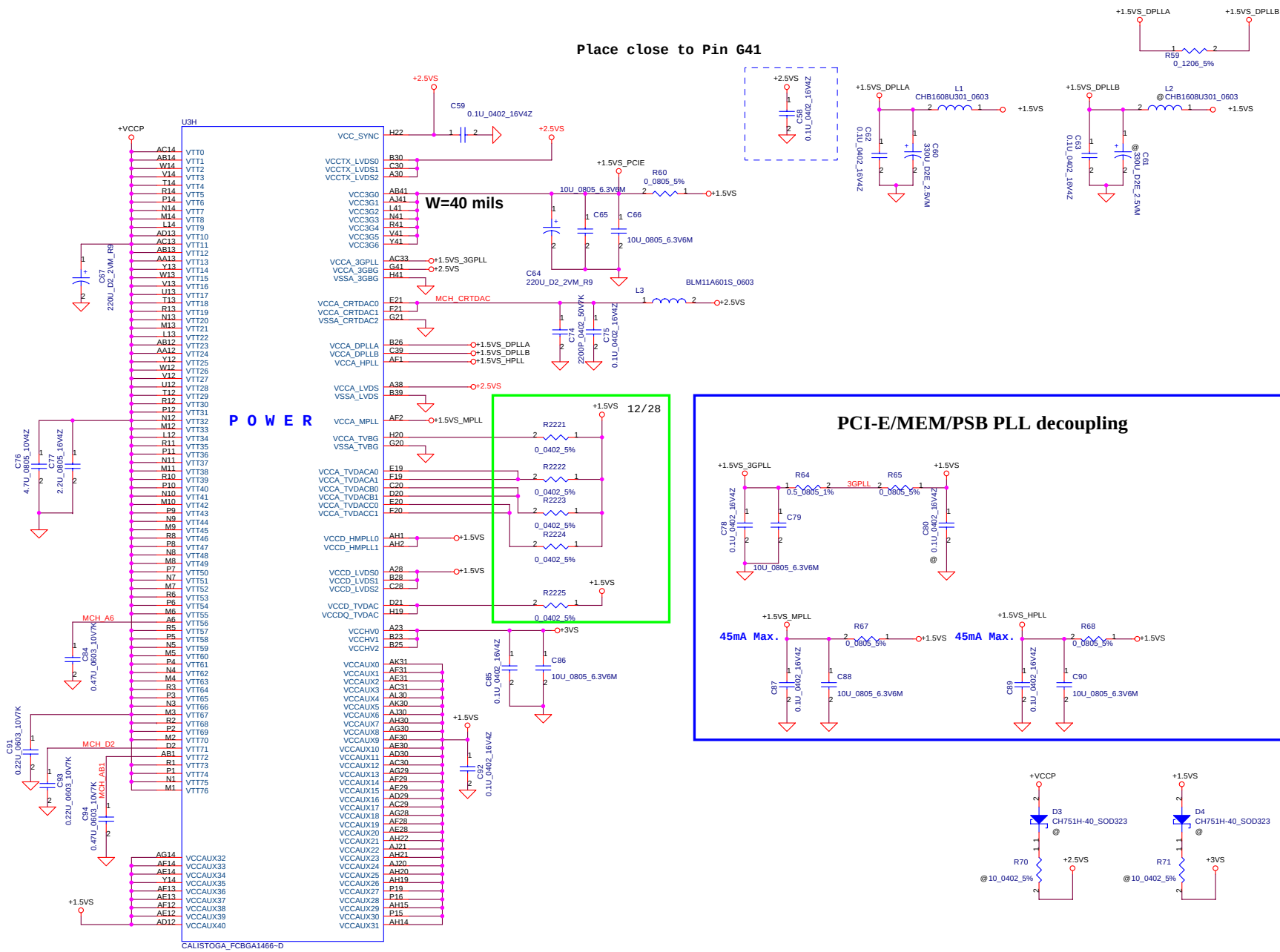




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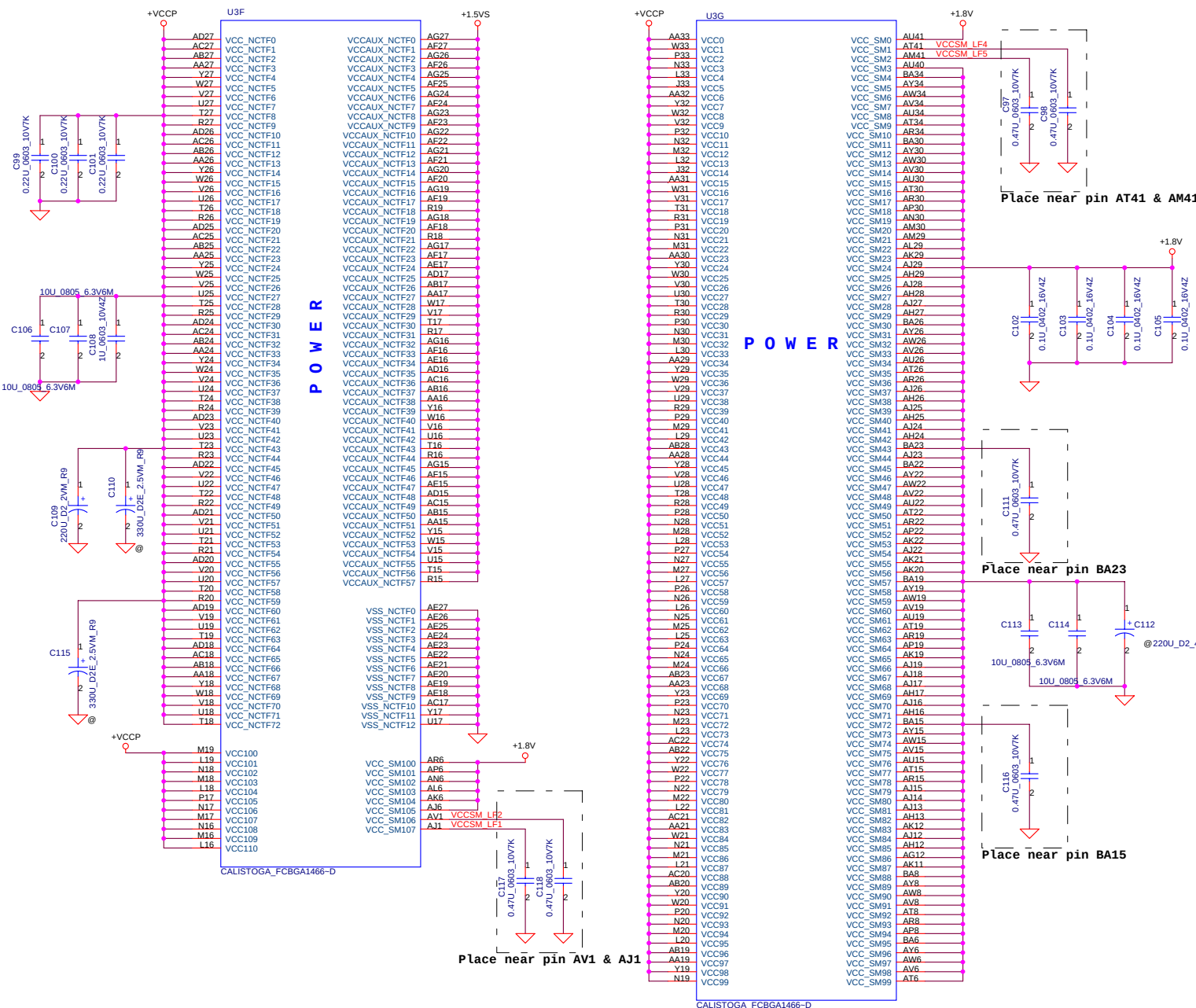
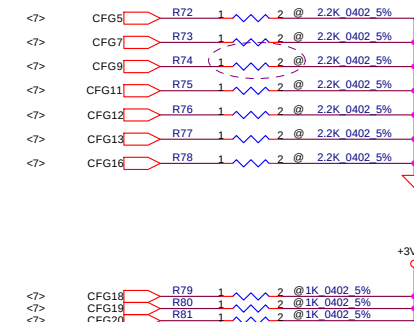
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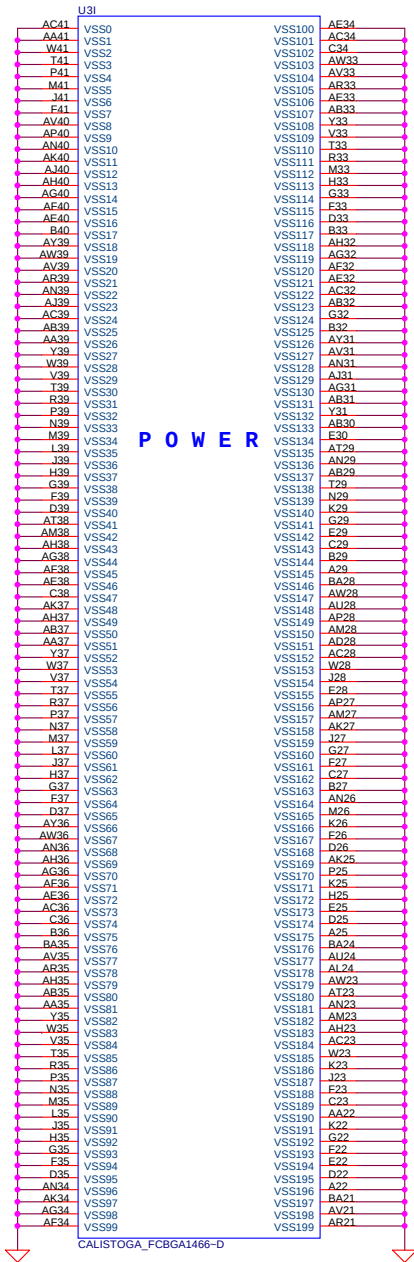


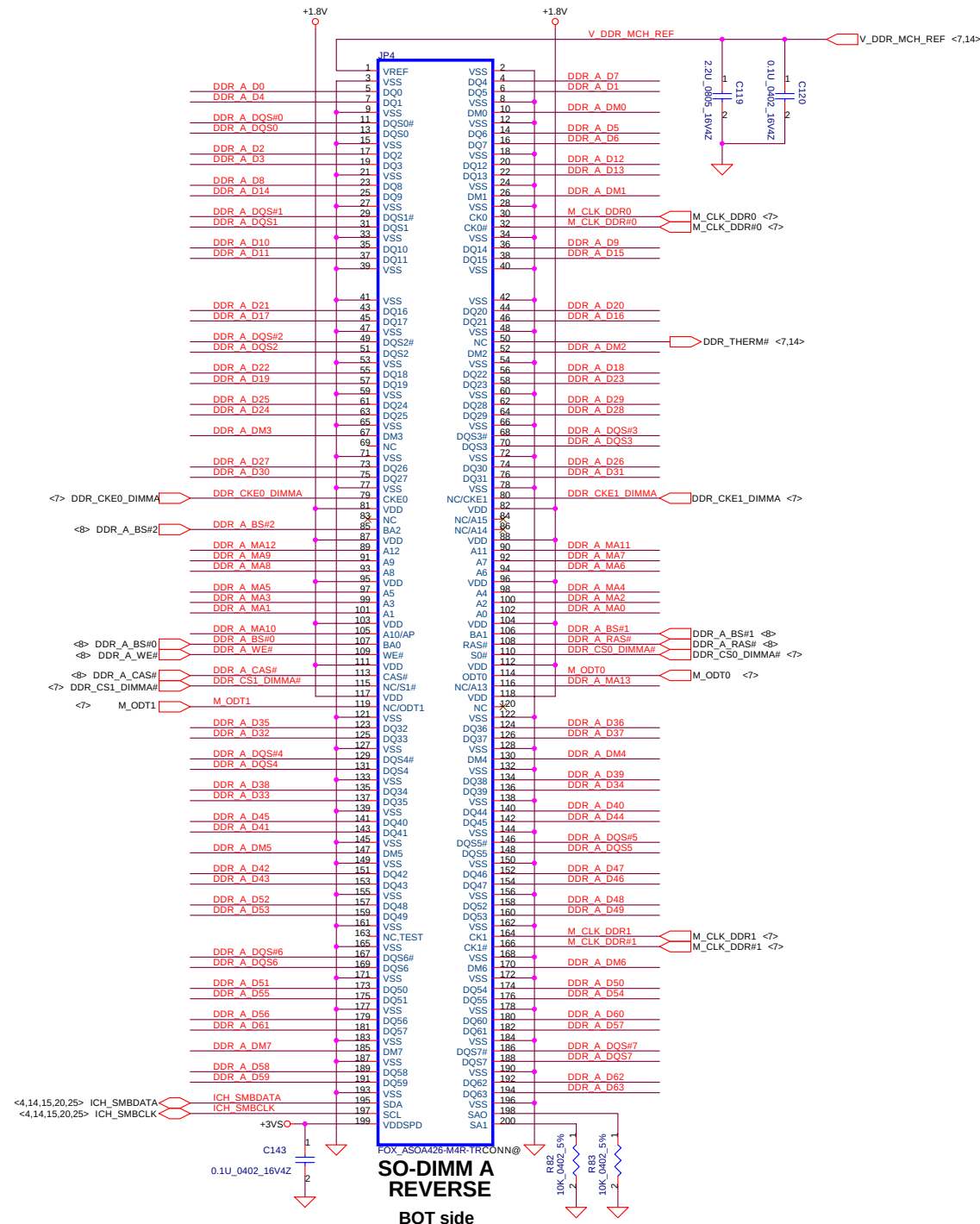
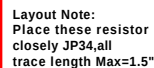
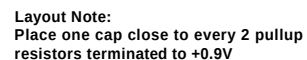
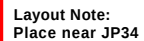
Strap Pin Table

CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

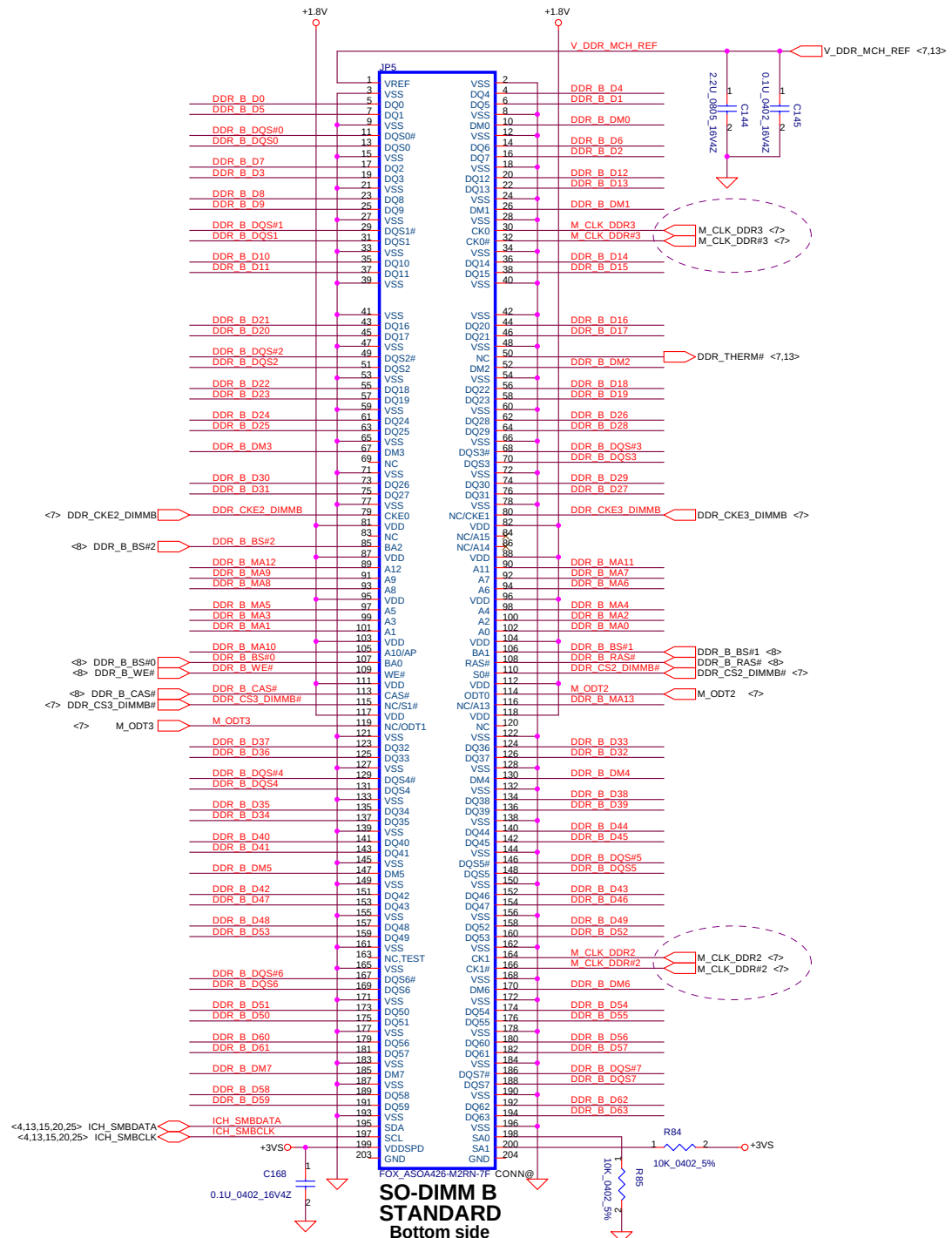
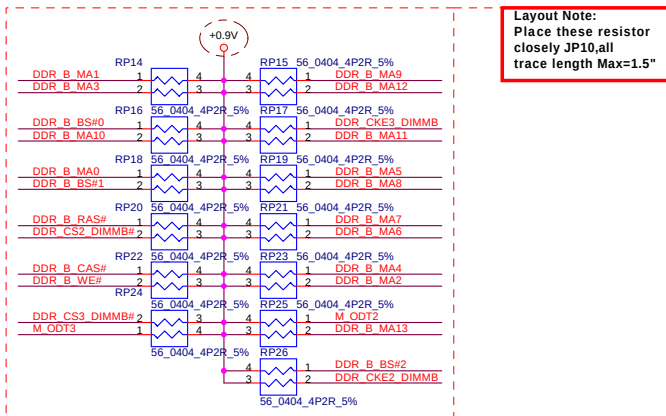
CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable * 1 = Normal operation *(Default)
CFG11	0 = Calistoga * (According to Intel Napa Schematic Checklist & CRB Rev1.301 document 2.2Kohm pull-downs resistor required)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.95V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.







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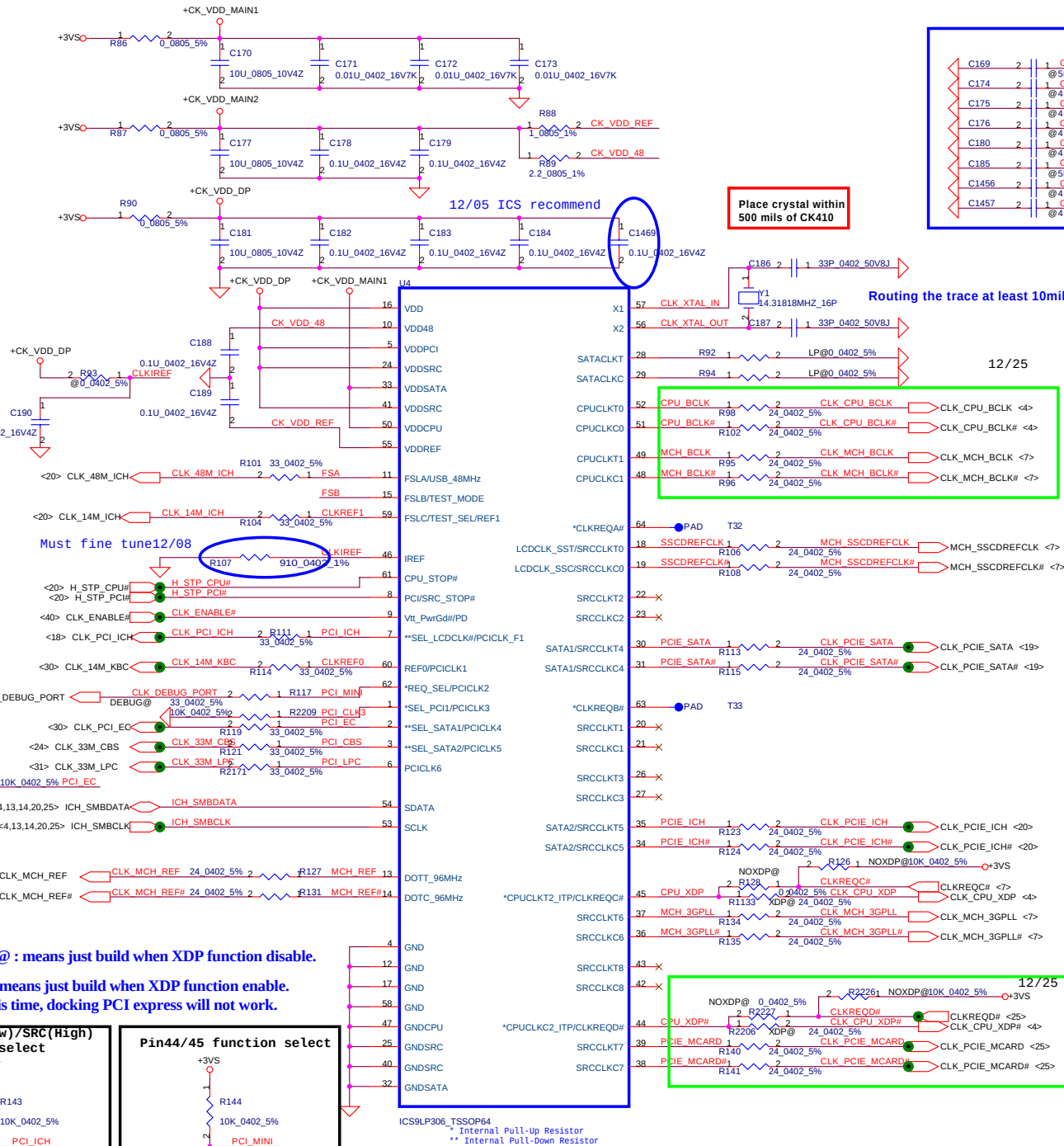
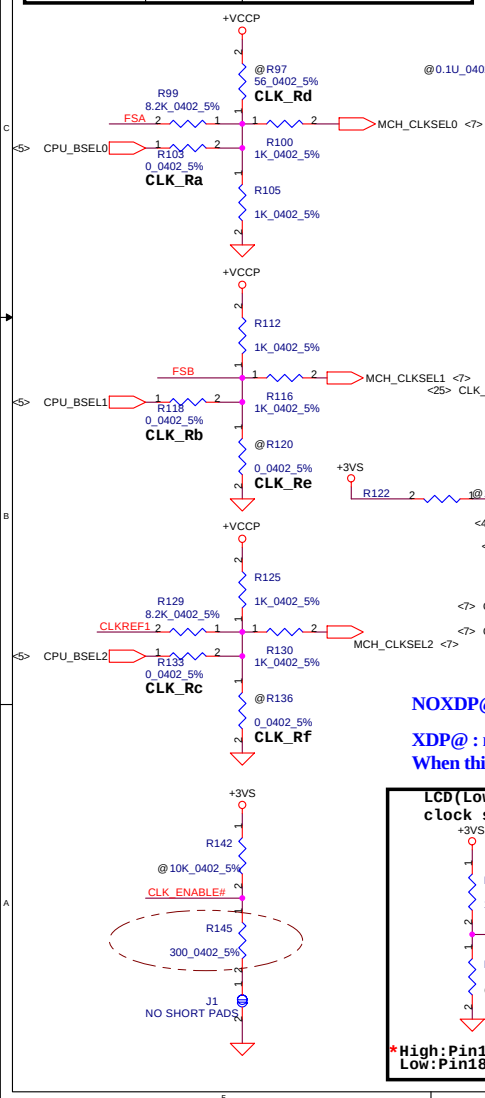


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Table : ICS954306

FSB Frequency Set:

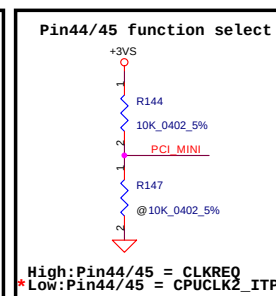
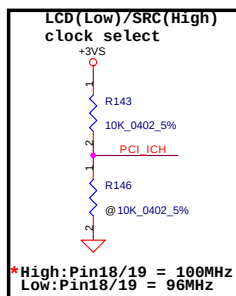
CPU Driven * (Default)	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
	No Stuff	CLK_Rd	CLK_Re	CLK_Rf
533MHz	Stuff	CLK_Rd	CLK_Re	CLK_Rf
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc
667MHz	Stuff	CLK_Rd		
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc
		CLK_Re	CLK_Rf	



Place near U4
Place these components
near each pin within 40
mils.

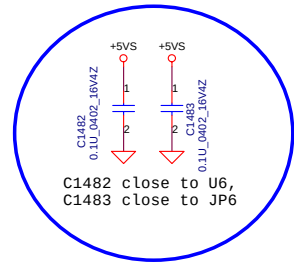
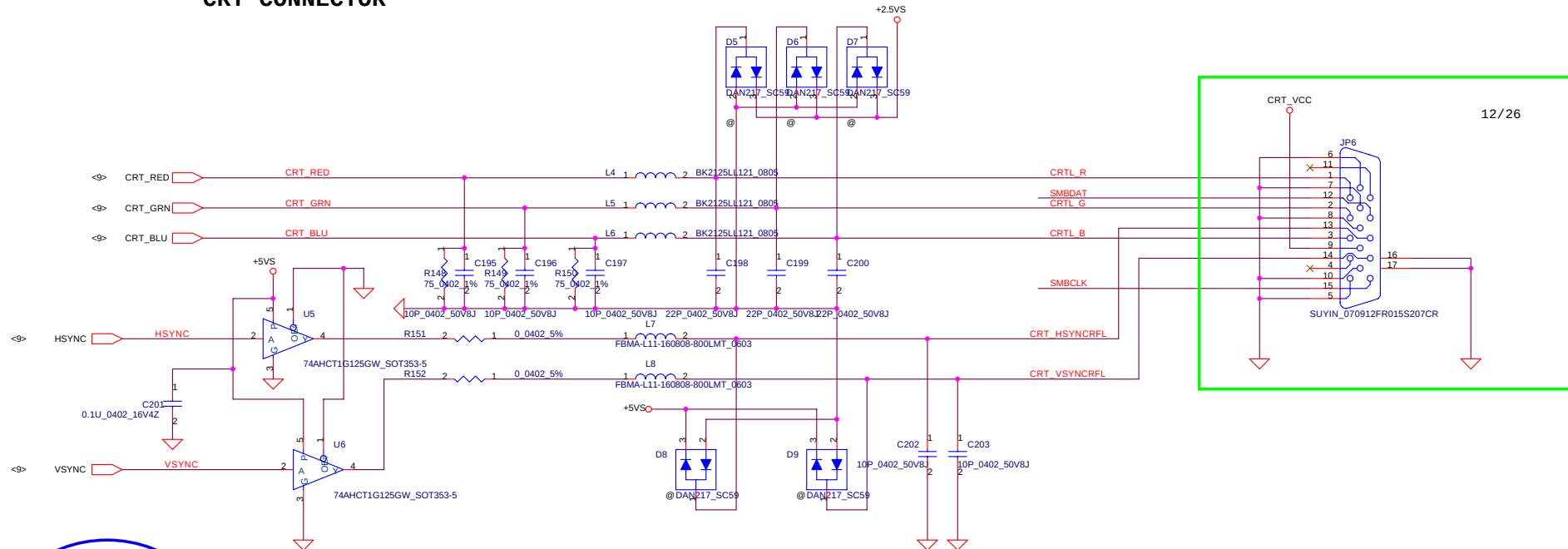
NOXDP@ : means just build when XDP function disable.

XDP@ : means just build when XDP function enable.
When this time, docking PCI express will not work.



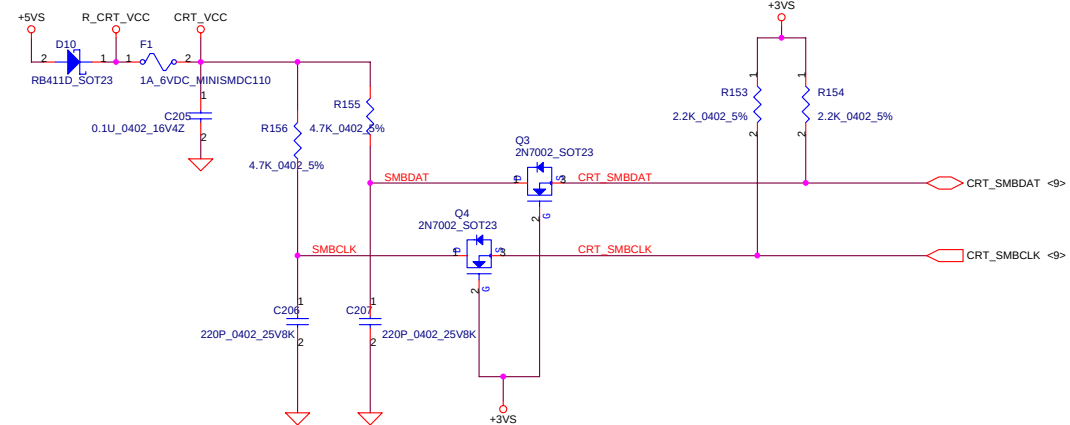
Security Classification		Compal Secret Data		Compal Electronics, Inc. Clock generator	
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CRT CONNECTOR



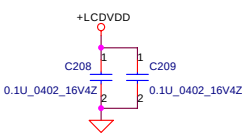
C1482 close to U6,
C1483 close to JP6

0119 HSYNC, VSYNC reference +5VS

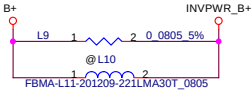
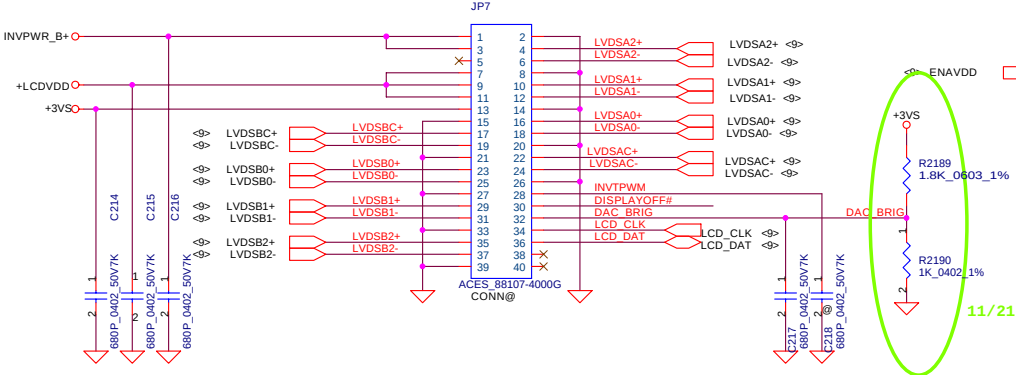


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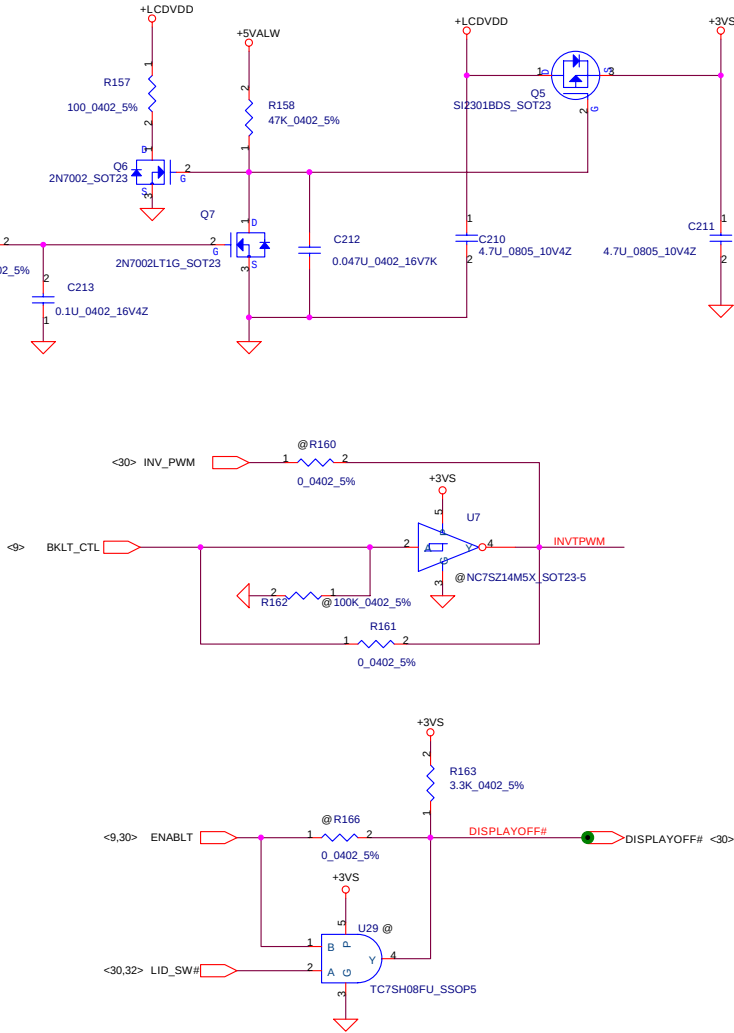
LVDS CONN



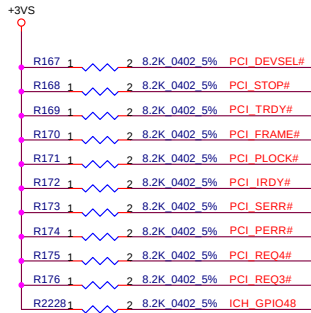
LVDS connector



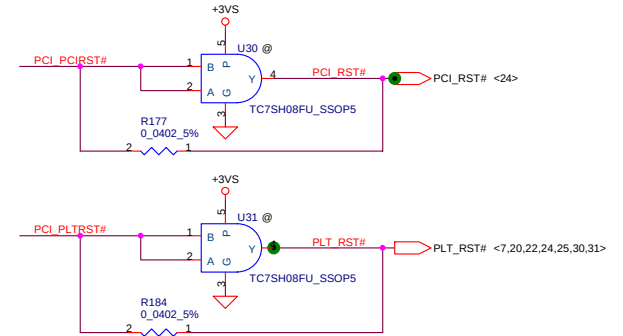
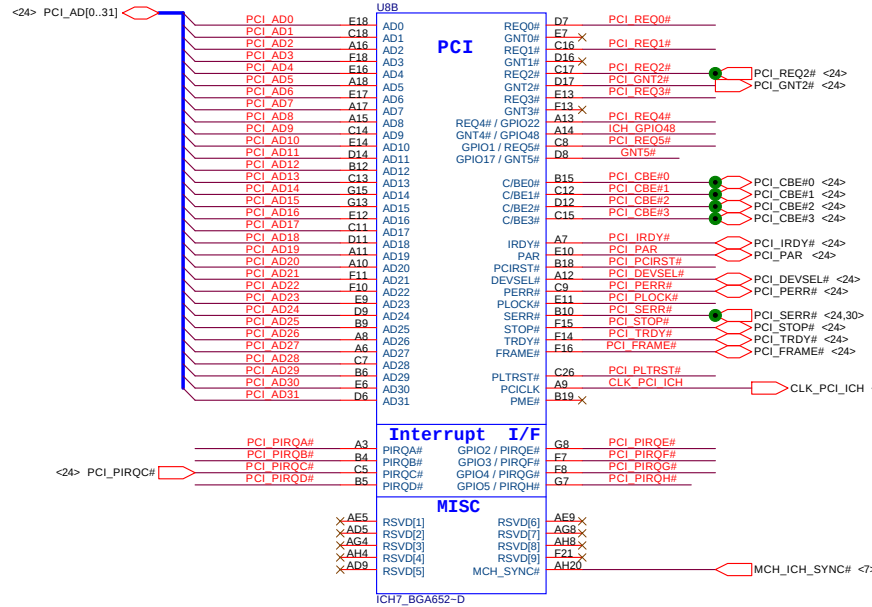
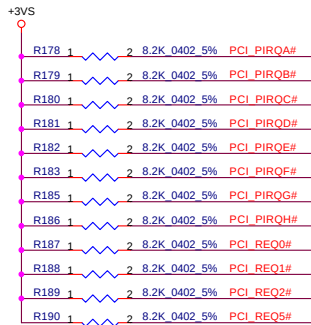
LCD/PANEL BD. CONN.



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				LCD CONN.	



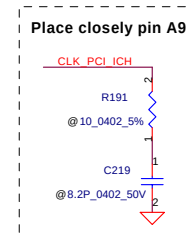
Change to RP before SI phase



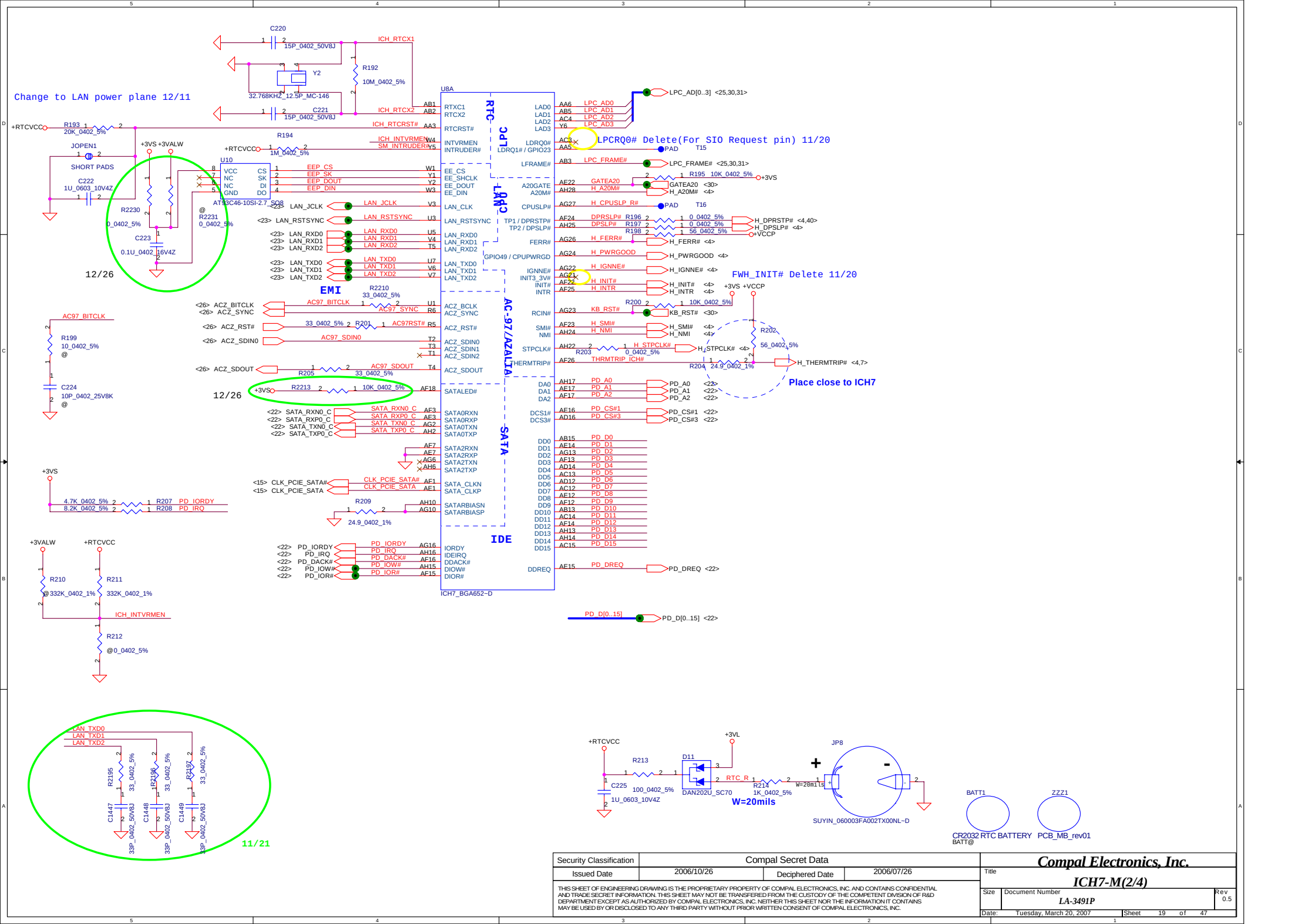
GNT5# and GNT4# have internal pull high 20K
Boot BIOS destination

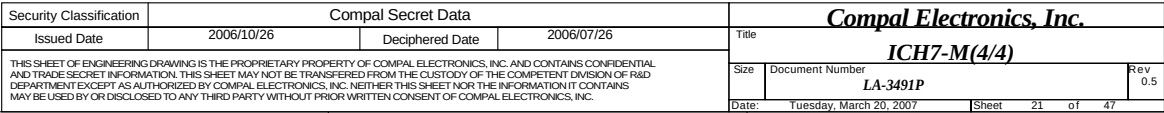
GNT5#	GNT4#	
0	1	SPI@ (Default)
1	0	PCI@
1	1	LPC@

The pad must be placed on PCB easily
contact space for BIOS team setting.



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SATA CONN

Near ICH7(U26) side.

<19> SATA_TXN0_C → SATA_TXN0_C → 3900P_0402_50V7K → SATA_TXN0

<19> SATA_TXP0_C → SATA_TXP0_C → 3900P_0402_50V7K → SATA_TXP0

Near Device(JP45) side.

<19> SATA_RXN0_C → SATA_RXN0_C → 3900P_0402_50V7K → SATA_RXN0

<19> SATA_RXP0_C → SATA_RXP0_C → 3900P_0402_50V7K → SATA_RXP0

JP9 Pinout:

Pin	Signal
1	GND
2	SATA_TXP0
3	A+
4	A-
5	GND
6	SATA_RXN0
7	B+
8	GND
9	V33
10	V33
11	GND
12	GND
13	GND
14	V5
15	V5
16	V5
17	GND
18	Reserved
19	GND
20	V12
21	V12
22	V12

Circuit Diagram:

CONN@ OCTEK_HDD-22SC1G_4P_RV

Capacitors: C269 (10uF), C270 (0.1uF), C271 (0.1uF), C1450 (3900L_D3E_25VML_R9).

Power: +SVS

11/21

12/26

<7,18,20,24,25,30,31> PLT_RST#

PLT_RST#

R256 1 33 0402_5%

PD_D0 PD_D1 PD_D2 PD_D3 PD_D4 PD_D5 PD_D6 PD_D7 PD_D8 PD_D9 PD_D10 PD_D11 PD_D12 PD_D13 PD_D14 PD_D15 PD_DREQ PD_IOR# PD_DACK# PD_A2 PD_CS#3 PD_IOW# PD_IORDY PD_IRQ PD_A1 PD_A0 PD_CS#1 IDE_ACT#

OCTAL CDR-50TA1

+5V

PRI_CSEL

R258 470_0402_5%

R259 10K_0402_5%

IDE_ACT#

+5V

PD_D0 PD_D1 PD_D2 PD_D3 PD_D4 PD_D5 PD_D6 PD_D7 PD_D8 PD_D9 PD_D10 PD_D11 PD_D12 PD_D13 PD_D14 PD_D15 PD_DREQ PD_IOR# PD_DACK# PD_A2 PD_CS#3 PD_IOW# PD_IORDY PD_IRQ PD_A1 PD_A0 PD_CS#1 IDE_ACT#

R257 100K_0402_5%

+5V

C274 0.1U_0402_16V4Z

C1451 0.1U_0402_16V4Z

C1452 1U_0805_10V4Z

C1453 1U_0805_10V4Z

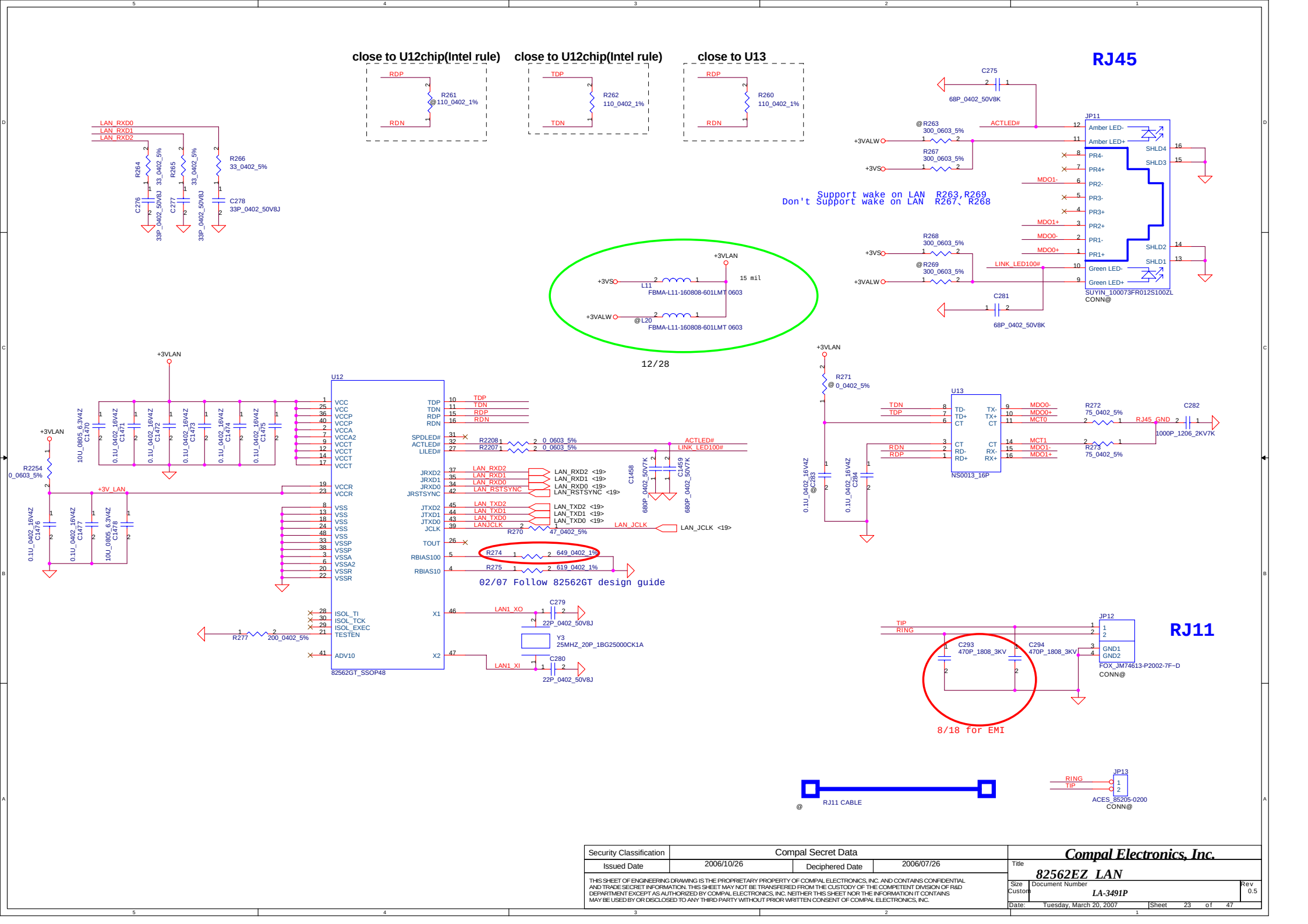
C1454 10U_0805_10V4Z

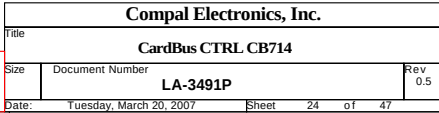
+5V

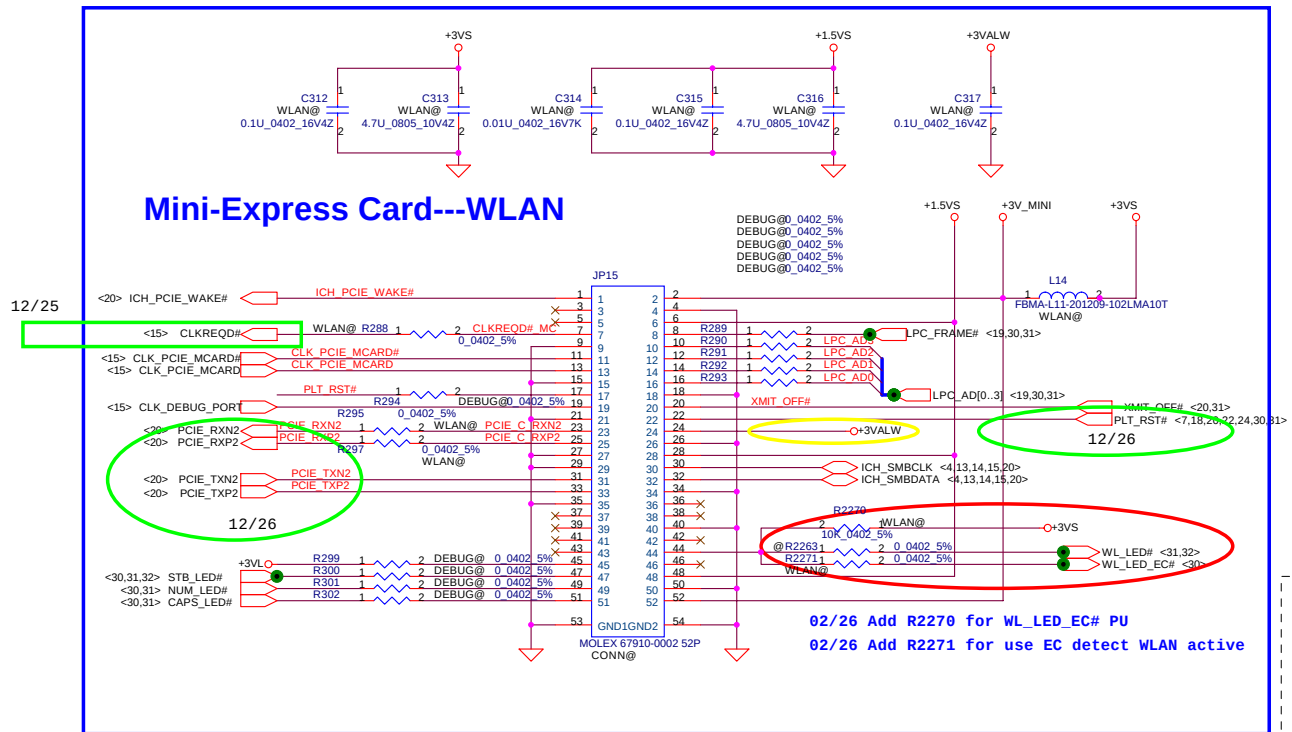
Placea caps. near ODD CONN.

11/21

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					Size	Document Number		Rev		
						LA-3491P		0.5		
					Date:	Tuesday, March 20, 2007	Sheet	22	of	47

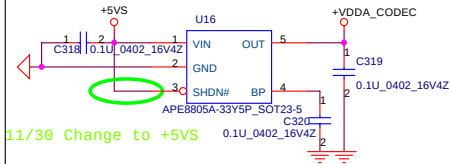






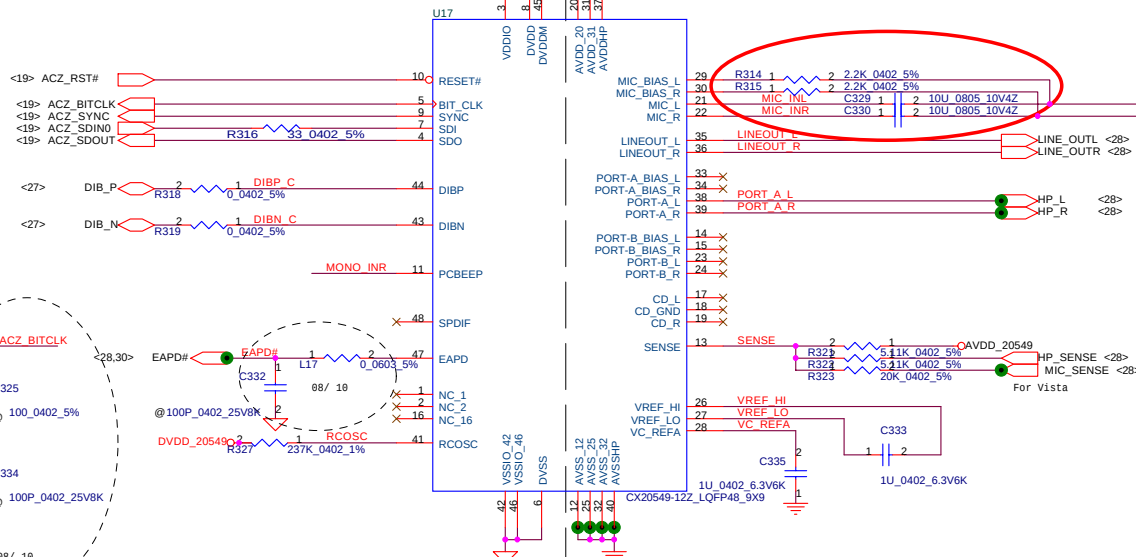
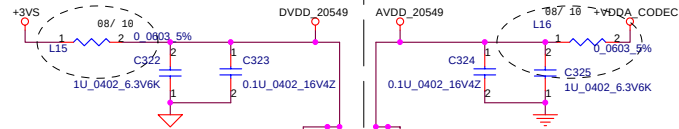
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					LA-3491P
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				Sheet	25 of 47

CODEC POWER

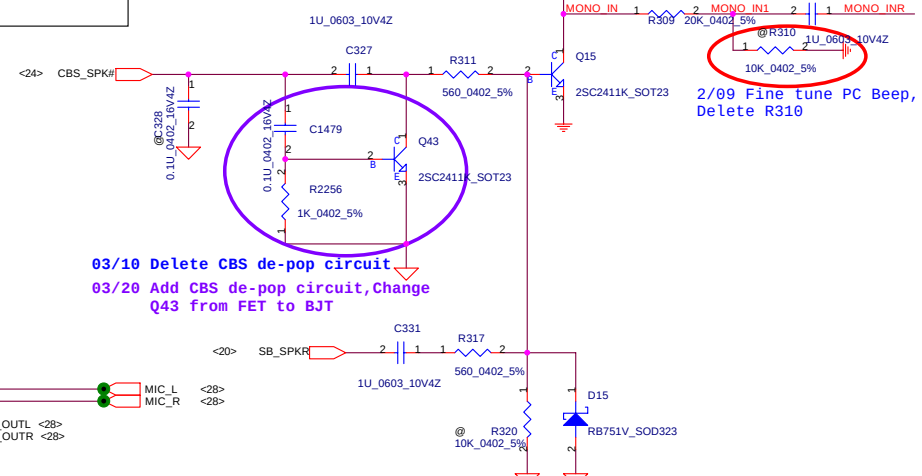


AUDIO CODEC

In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.



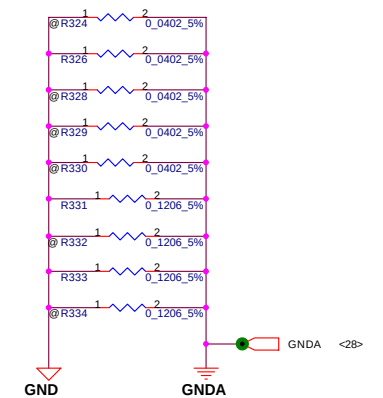
03/10 Delete CBS de-pop circuit
03/20 Add CBS de-pop circuit, Change Q43 from FET to BJT



2/09 Fine tune PC Beep, Delete R310

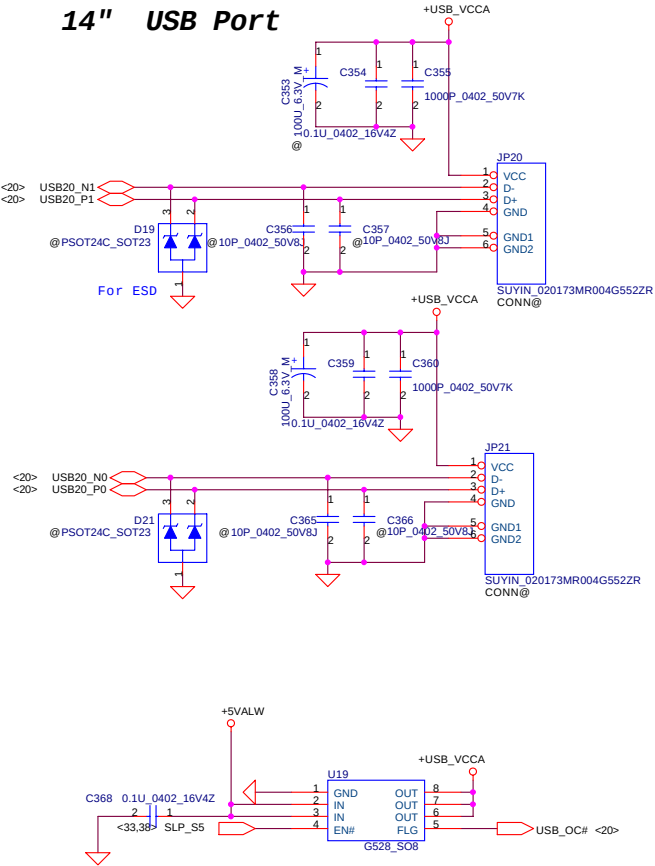
DIGITAL

ANALOG

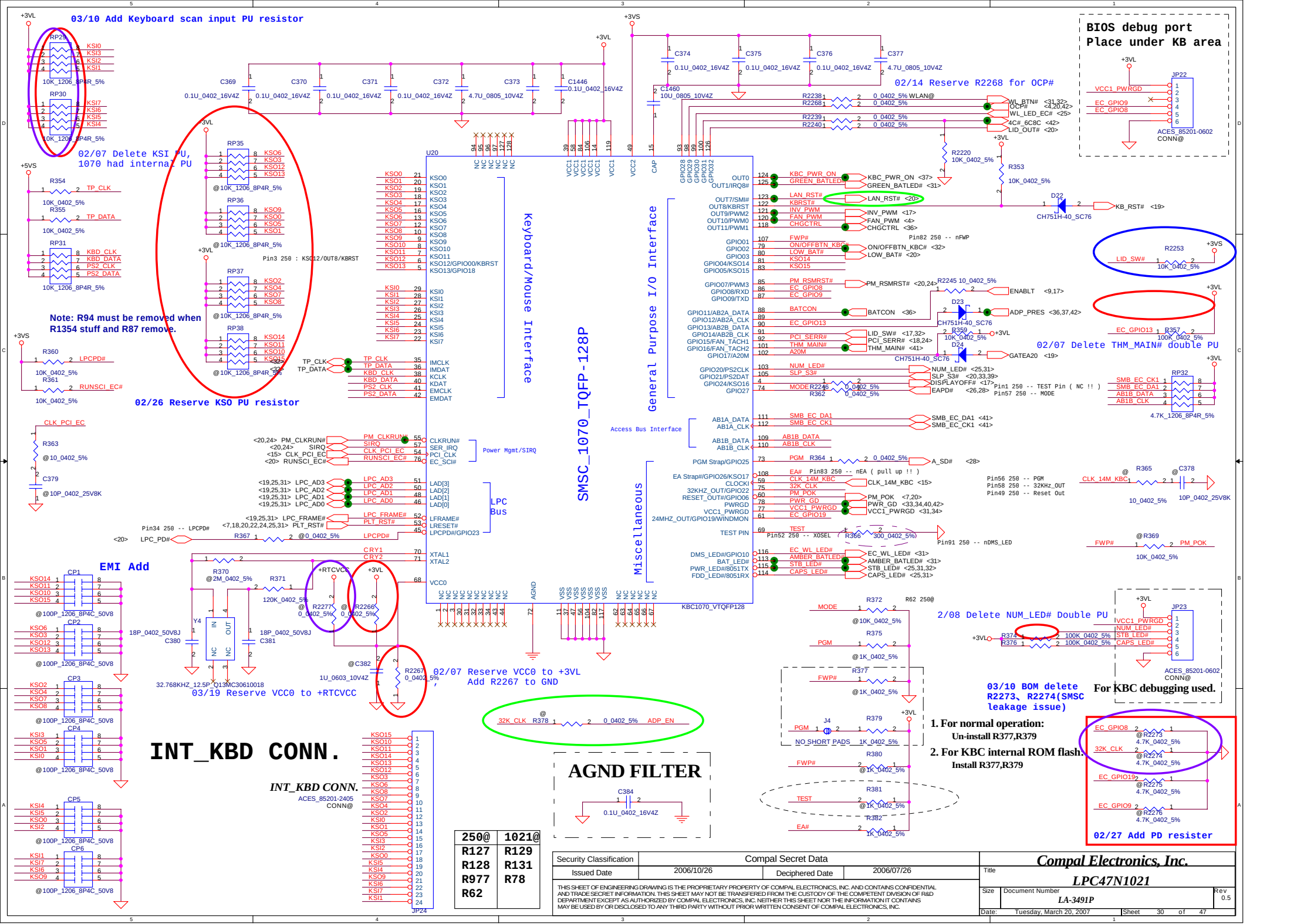


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14" USB Port

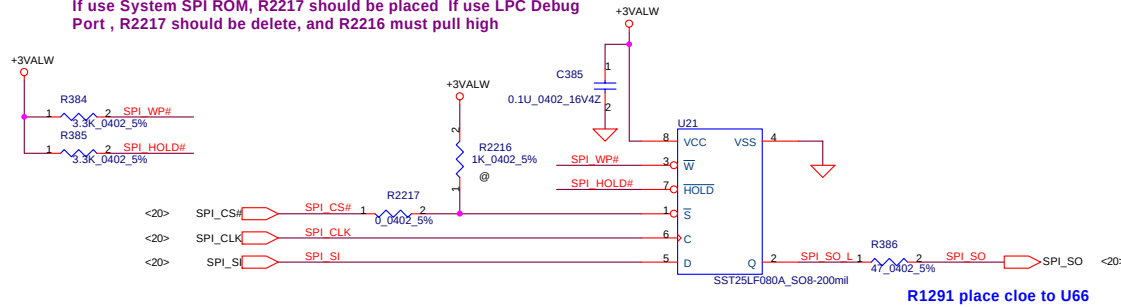


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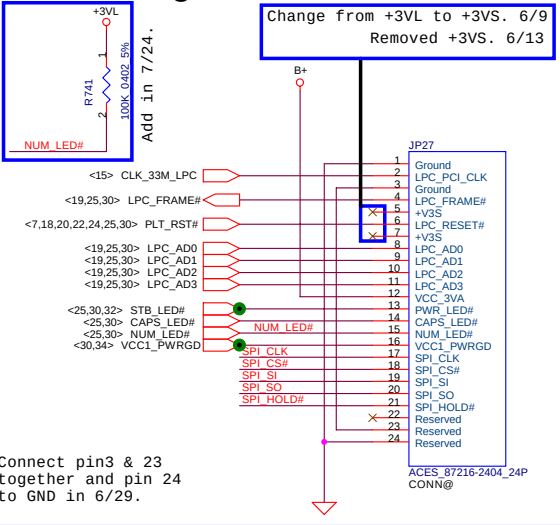


BIOS ROM

If use System SPI ROM, R2217 should be placed If use LPC Debug Port , R2217 should be delete, and R2216 must pull high



LPC Debug Port

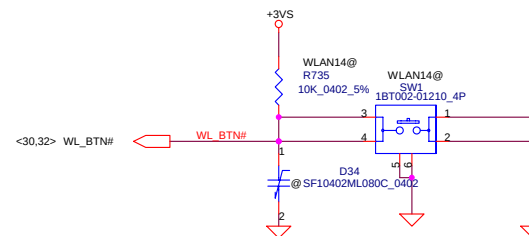
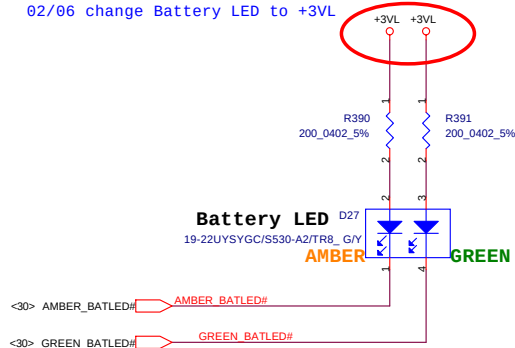


WL ON/OFF

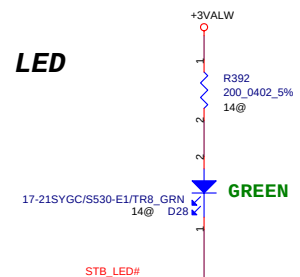
POWER LED

Charge LED

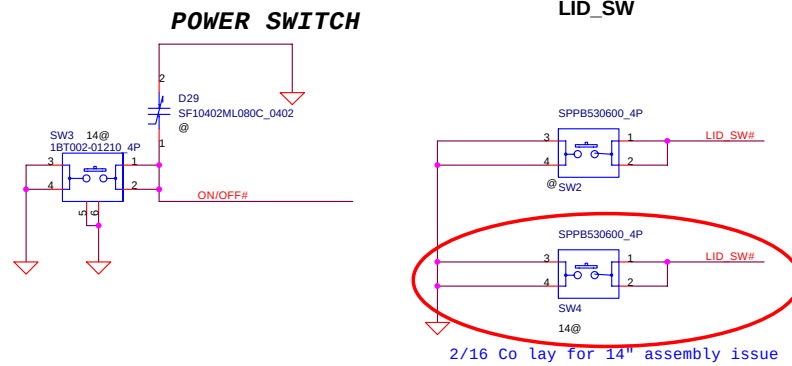
02/06 change Battery LED to +3VL



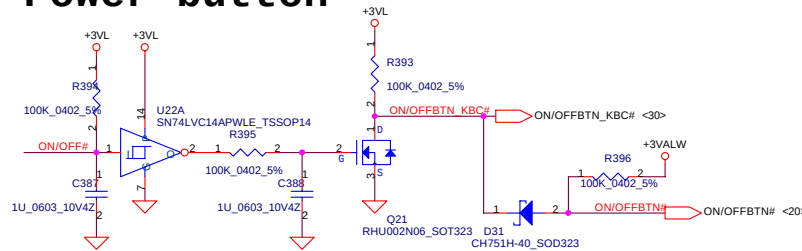
CAP LED



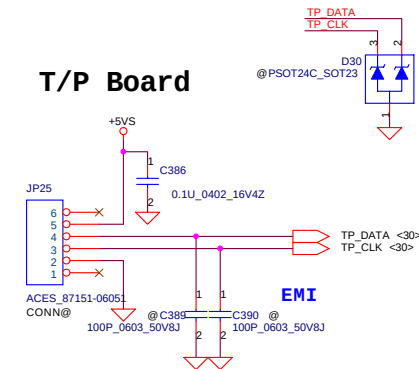
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Issued Date	2006/10/26	Deciphered Date	2006/07/26	BIOS ROM/PS2/LED/SW	
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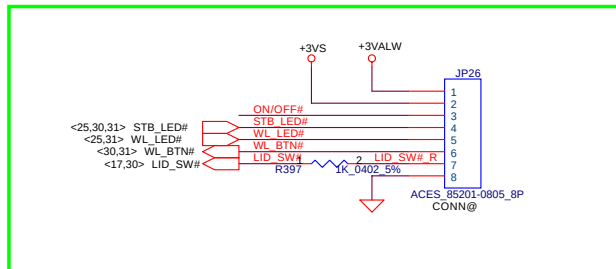
Power button



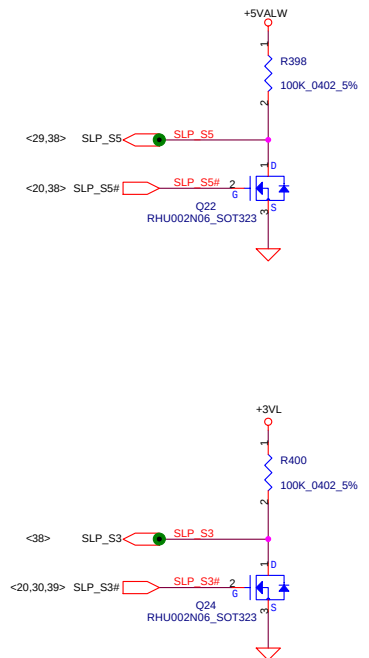
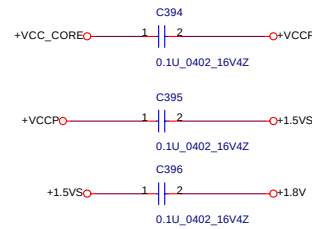
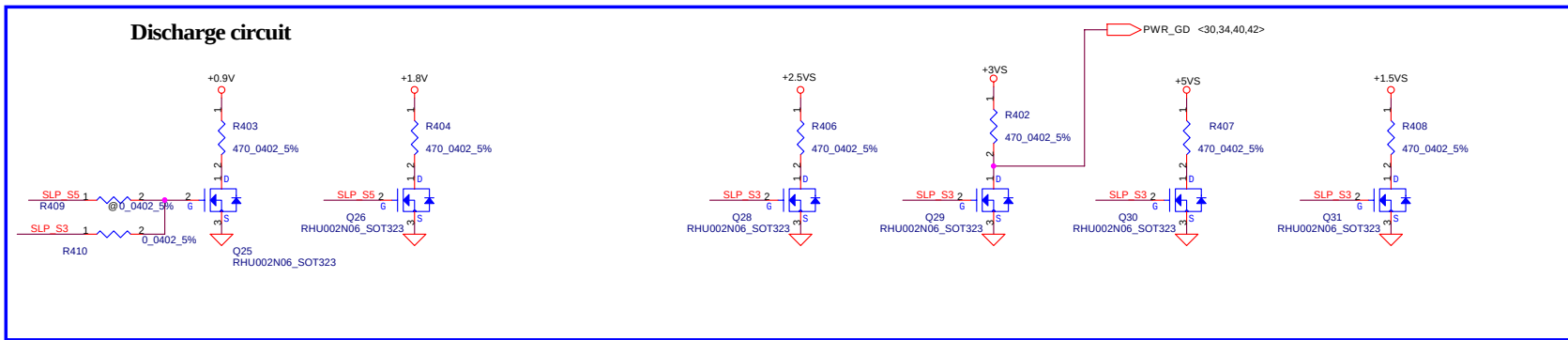
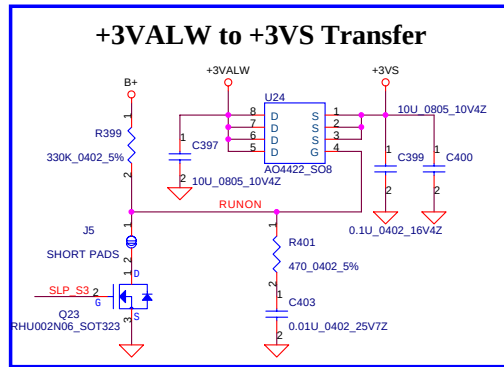
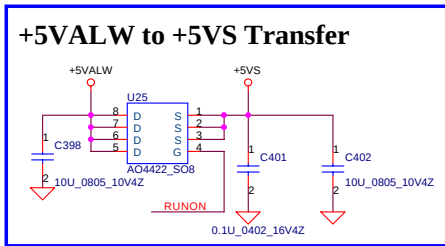
T/P Board



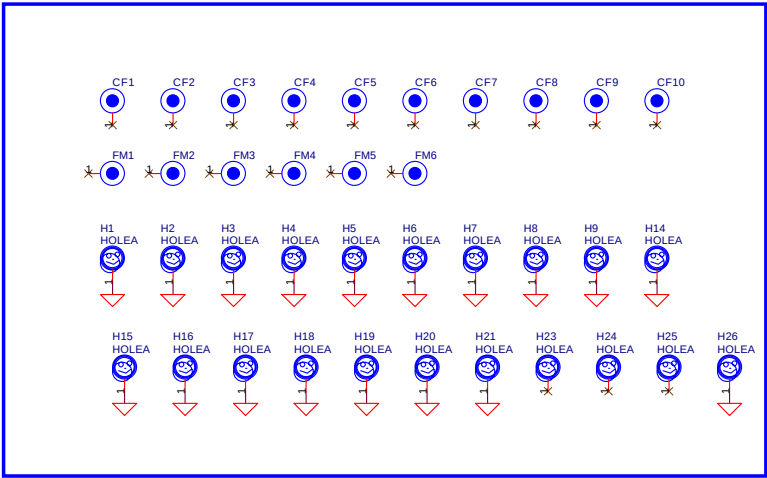
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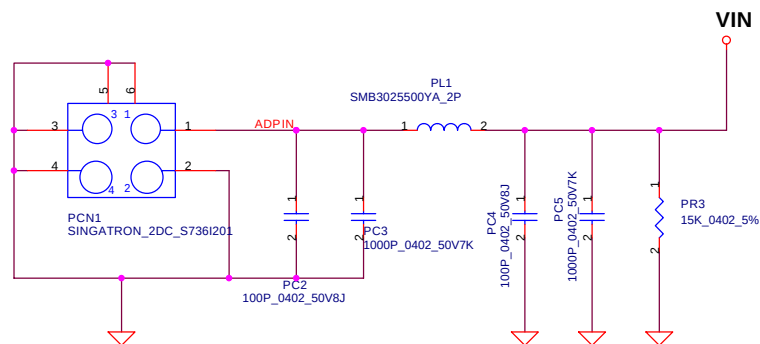


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				Size	Rev
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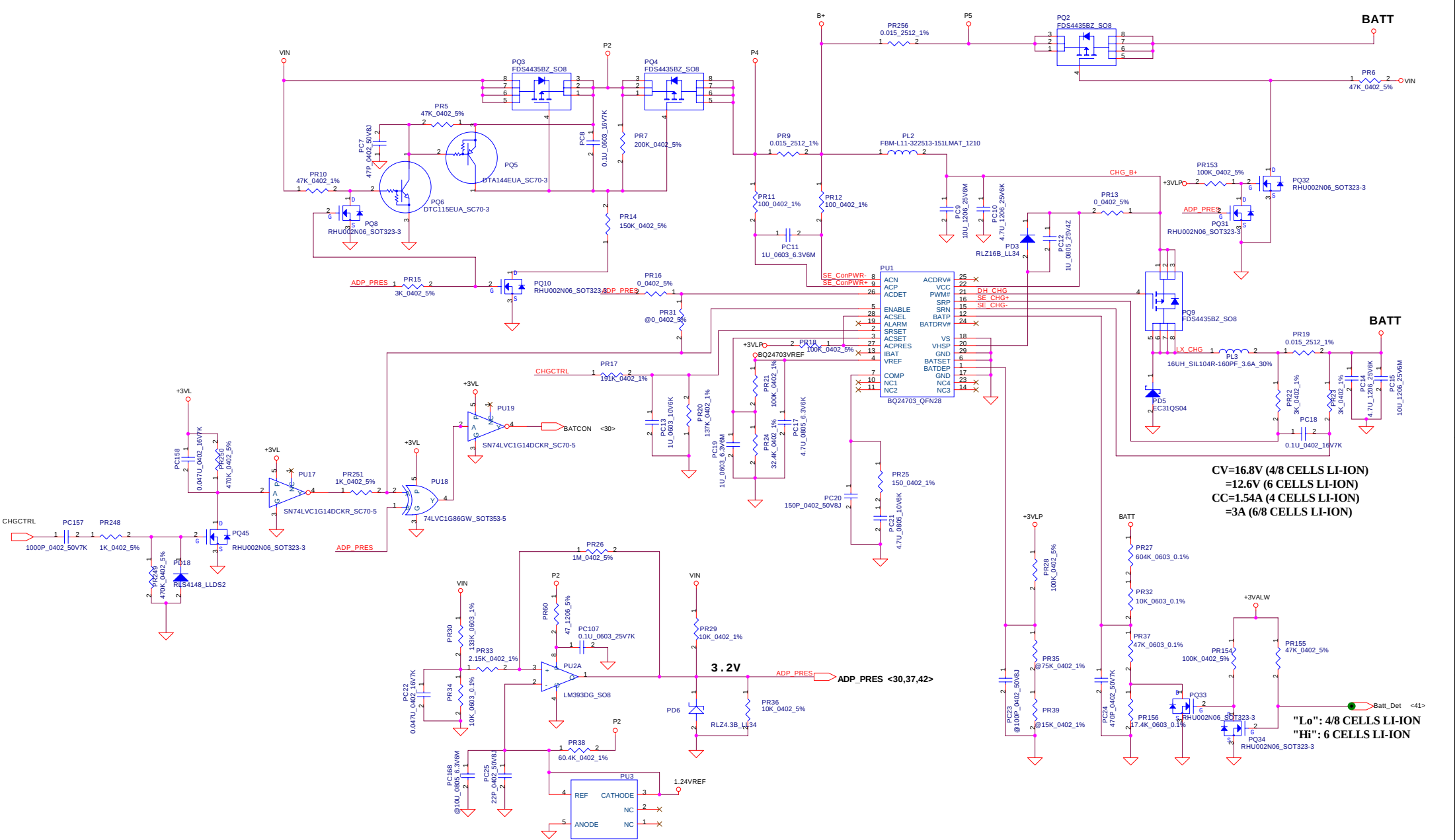


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								Size	Document Number	Rev
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								Date:	Tuesday, March 20, 2007	Sheet





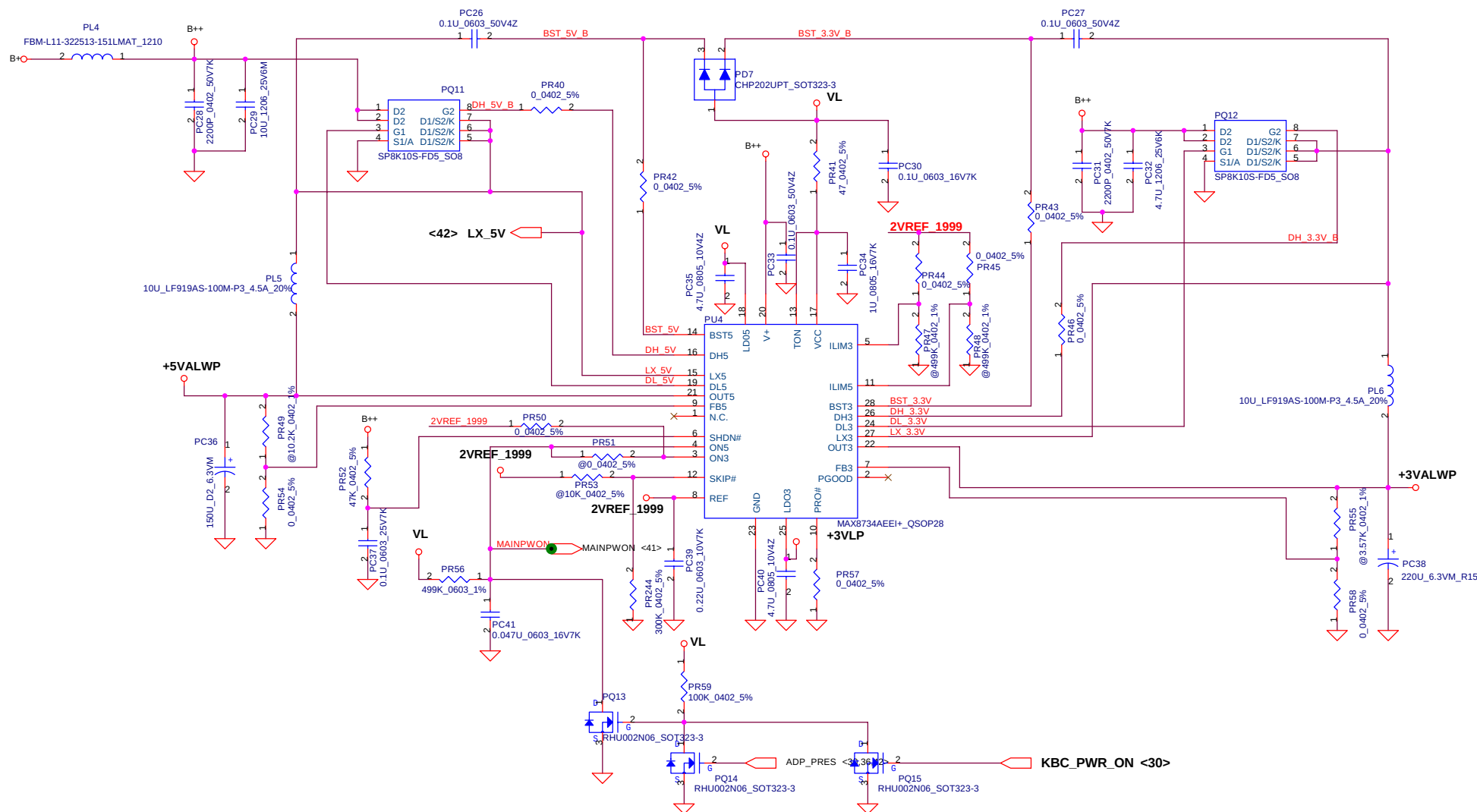
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				Size Custom	Document Number	Rev
				LA-3491P		
Date:		Tuesday, March 20, 2007		Sheet	35	of 47



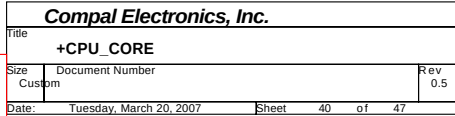
CV=16.8V (4/8 CELLS LI-ION)
=12.6V (6 CELLS LI-ION)
CC=1.54A (4 CELLS LI-ION)
=3A (6/8 CELLS LI-ION)

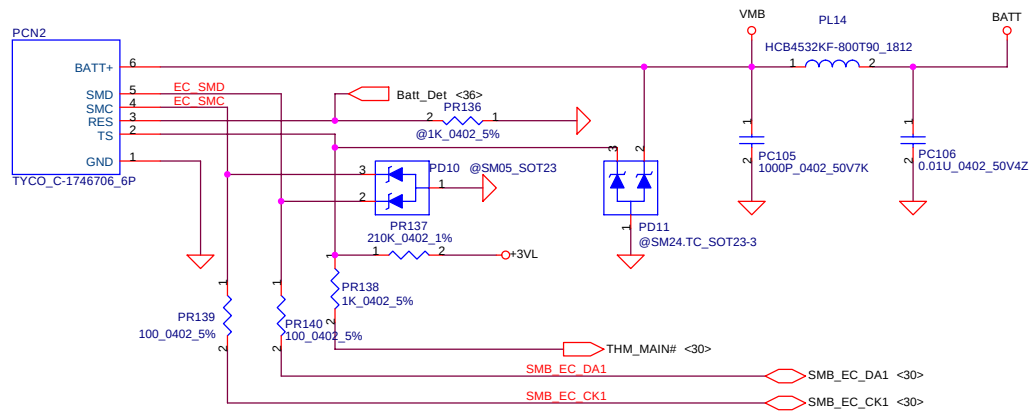
"Lo": 4/8 CELLS LI-ION
"Hi": 6 CELLS LI-ION

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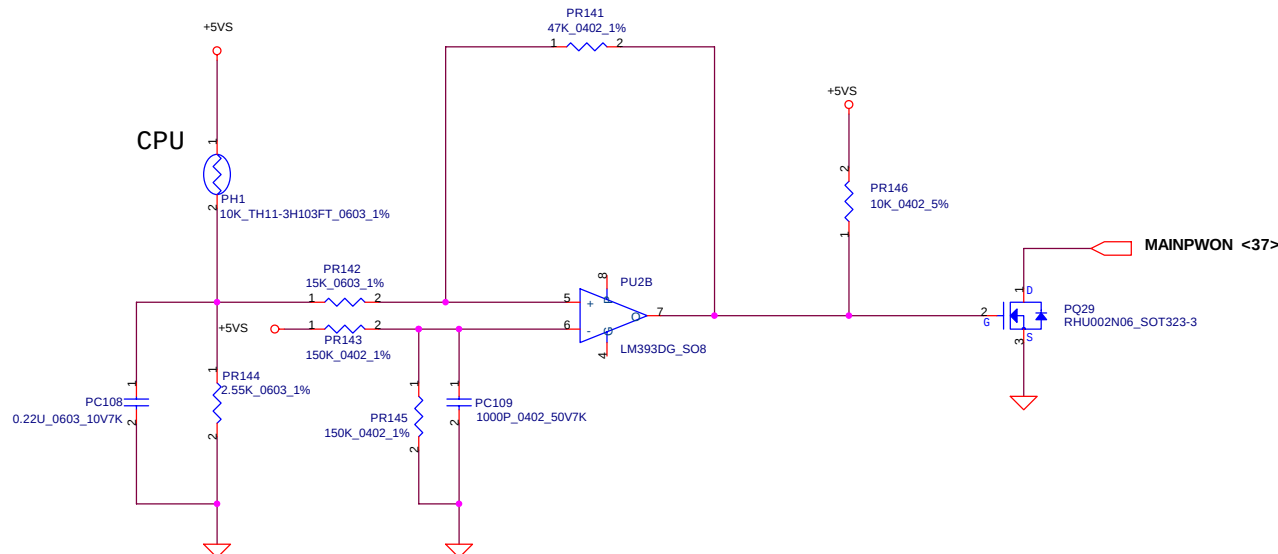


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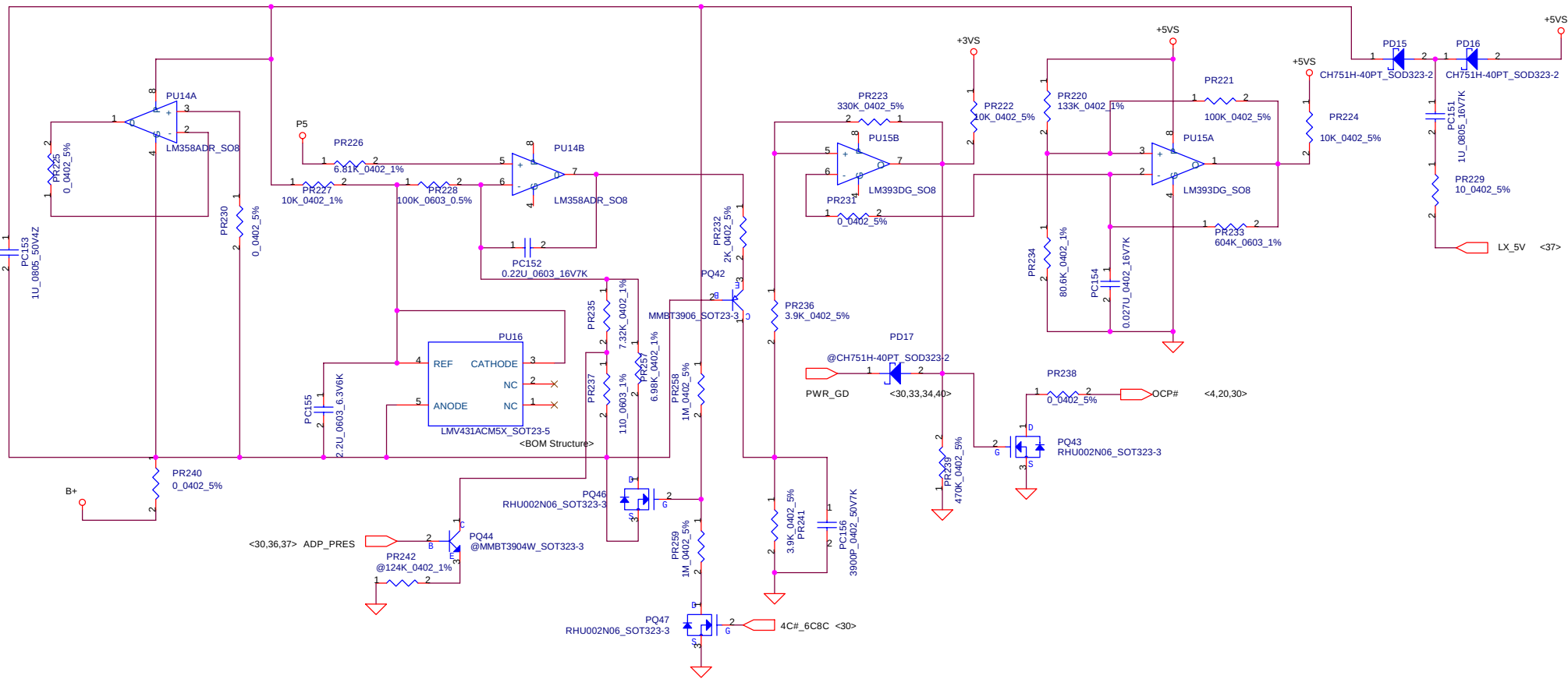




PH1 under CPU bottom side :
 CPU thermal protection at 90 $\pm$ 3 degree C
 Recovery at 47 $\pm$ 3 degree C



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Version change list (P.I.R. List)

HW section

Page 1 of 3

Item	Reason for change	PG #	Modify List	Date	Phase
1	Reserve Disable TV-out power plane resistor	Page 10	Add R2221、R2222、R2223、R2224、R2225 for Disable TV-out power plane	01/02	DB2
2	R2211、R2212 Change to 10k follow datasheet	Page 9	Change R2211、R2212 to 10K_0402_5%	01/02	DB2
3	Disable TV-out follow datasheet	Page 9	Add resistor to +1.5VS power TVDAC_A(R2172)、TVDAC_B(R2173)、TVDAC_C(R2174)、TV_IREF(R57) BTVIRTNA、TVIRTNB、TVIRTNC(R2251)	01/02	DB2
4	Change CPU and NB BCLK follow heavenly2.0	Page 15	CPU --->CPUCLKT0/C0 NB --->CPUCLKT1/C1	01/02	DB2
5	Change Mini card CLK From SRC3 to SRC7	Page 15	Change to SRC7	01/02	DB2
6	CRT connector PCB footprint error	Page 16	Change JP6 PCB Footprint form SUYIN_070912FR015S207CR_15P to ALLT0_C10510-115A5-L_15P	01/02	DB2
7	+ENAVDD add a 100k Pull low follow datasheet	Page 17	Add R2247 to GND	01/02	DB2
8	LCDVDD enable timing	Page 17	Change R159 to 47k、C213 to 0.1u	01/02	DB2
9	Change AND gate that one gate one chip	Page 18	Change U28(4 in 1) to U30、U31	01/02	DB2
10	Reserve EE PROM power plane +3VS	Page 19	Reserve R2230 for don't support wake up LAN Reserve R2231 for support wake up LAN	01/02	DB2
11	Add R2213 and verify need or not?	Page 19	Add R2213	01/02	DB2
12	Change PCIE from port 1 to port 2 follow caymus	Page 20 Page 25	Change MINI Card PCIE from Port 1to Port2	01/02	DB2
13	Reserve LAN_RST# that can fine tune from EC	Page 20 Page 30	Reserve R2233 for fine tune LAN_RST# timing	01/02	DB2
14	Change R to RP , keep original design	Page 20	Change to RP33、RP34	01/02	DB2
15	Reserve +3VS power plane for don't support wake up LAN	Page 21	If R2237 --->support wake up LAN If R2236 --->Don't support wake up LAN	01/02	DB2
16	Reserve +3VALW power plane to verify HDA codec	Page 21	If R2234 --->AC97 codec If R2235 --->HD Codec	01/02	DB2
17	Reserve +3VALW power plane support wake up LAN	Page 23	If L11 --->Don't support wake up LAN If L20 --->Support wake up LAN	01/02	DB2
18	Reserve +3VALW power plane support wake up LAN	Page 24	If L12、L13 --->Don't support wake up LAN If L21、L22 --->Support wake up LAN	01/02	DB2
19	Reserve 0 ohm resistor for SMSC1070	Page 30	Reserve R2238、R2239、R2240	01/02	DB2
			Compal Electronics, Inc.		
			HW PIR (1)		
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			Title Size Custom Document Number Date: Tuesday, March 20, 2007 Sheet 43 of 47 Rev 0.5		

Version change list (P.I.R. List)

HW section

Page 2 of 3

Item	Reason for change	PG #	Modify List	Date	Phase
20	Wireless LED design issue	Page 31	Delete Q20	01/02	DB2
21	Change P0K circuit form PG00D to VCCP_ON	Page 34	Add R2244、Q42, and reserve R2243	01/02	DB2
22	LID_SW# add 10k pull high	Page 30	Add R2253 for LID_SW# pull high	01/16	SI
23	Change use EAPD# to control Amp Shutdown	Page 28	Reserve R2198 and add R2252 pull high	01/16	SI
24	Change Battery LED power from +3VALW to +3VL	Page 31	Change Battery LED power from +3VALW to +3VL	02/06	PV
25	XMIT_OFF# control error	Page 31	Delete Q46	02/06	PV
26	Delete KSI PU, 1070 had internal PU	Page 30	Delete RP29、RP30	02/07	PV
27	Reserve SMSC 1070 VCC0 to +3VL,Add R2267 to GND	Page 30	Reserve R2266 to +3VL,Add R2267 to GND	02/07	PV
28	Change Codec Mix Resistor from 20k to 1k	Page 28	Change R2264、R2265 to 1K	02/07	PV
29	Change LAN82562GT RBIAS resistor to 649 ohm	Page 23	Change R274 to 649 ohm	02/07	PV
30	Reserve RESET IC for VCC1_PWRGD	Page 34	Reserve RESET IC U32 for VCC1_PWRGD	02/07	PV
31	THM_MAIN# Double pull high	Page 30	Delete R356	02/07	PV
32	Fine tune PC Beep	Page 26	BOM delete R310	02/09	PV
33	Change Hp series resistor to 60 ohm 0603	Page 28	Change R341、R343 to 60 ohm 0603	02/14	PV
34	Reserve OCP# to EC GPIO29(pin 98)	Page 30	Reserve R2268 to EC GPIO29(pin98)	02/14	PV
35	HP、MIC ESD Diode change to AGND	Page 28	HP、MIC ESD Diode change to AGND	02/14	PV
36	HP de pop when boot	Page 28	Add inverter to prevent HP pop noise	02/26	PV
37	C43、C44、C45 impact ME parts	Page 06	Change CPU core decoupling capacitor height limit 1.9mm for short term solution(SGA19331D00)	02/26	PV
38	WLAN LED use XMIT_OFF# have error beheive	Page 25 Page 30 Page 31	02/26 Add R2270 for WL_LED_EC# PU 02/26 Add R2271 for use EC detect WLAN active 02/26 Add R2272 for EC output and driver WLAN LED	02/26	PV
			Compal Electronics, Inc.		
			Title HW PIR (2)		
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Version change list (P.I.R. List)

Power section

Page 1 of 1

Item	Reason for change	PG #	Modify List	Date	Phase
1	The PR172 changes to HW side	39	Remove PR172	2006/12/29	DB2
2	Change the +1.05V_VCCP power sequence	39	Remove PR180	2006/12/29	DB2
3	The +1.05V_VCCP dynamic range is over spec.	39	Change PL9 from 3.3UH to 2.2UH	2007/01/03	DB2
4	Adjust +1.5VSP voltage range	39	Change PR165 from 75K_ohm to 73.2K_ohm	2007/01/03	DB2
5	Change the PD18 diode	36	Change PD18 from 1SS355 to RLS4148	2007/01/16	SI
6	Change the +3VALWP output capacitor.	37	Change PC38 from 150U_D2_6.3VM to 220U_6.3V_R15	2007/01/16	SI
7	Change the +0.9VP output capacitor.	38	Change PC59 from 22U to 10U	2007/01/16	SI
8	Change the +1.05V_VCCP output capacitor.	39	Change PC71 from 220U_V_4VM_R25M to 220U_6.3V_R15	2007/01/16	SI
9	Change the +1.5VSP output capacitor.	39	Change PC73 from 220U_6.3VM_R15 to 220U_6.3V_R15	2007/01/16	SI
10	Change the +1.5VSP choke size.	39	Change PL11 from 3.3UH_PCMC063T-3R3MN_6A_20% to 3.3UH_SIQB74-3R3RF_4.8A_30%	2007/01/16	SI
11	Change PD14 diode	38	Change PD14 from CH751H-40PT to 1SS355	2007/02/05	PV
12	Adjust PU3 operation current	36	Change PR38 from 75K_ohm to 60.4K_ohm	2007/02/05	PV
13	Change PC25 capacitor.	36	Change PC25 form .022U to 22P	2007/02/05	PV
14	Change the +1.5VSP power sequence	39	1. Change PR178 form 0_ohm to 10K_ohm 2. Add PC126 0.1U	2007/02/05	PV
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