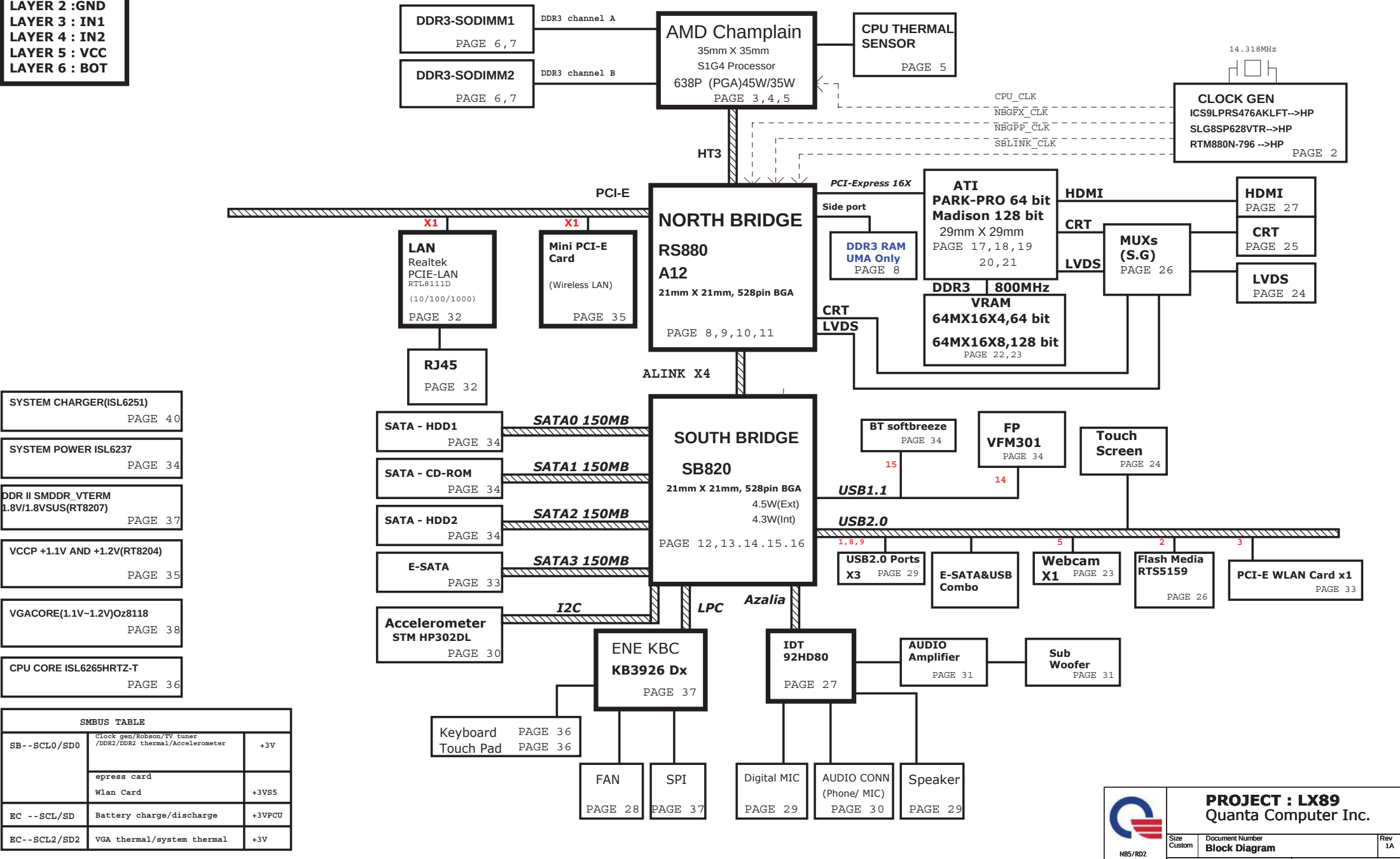


PCB STACK UP

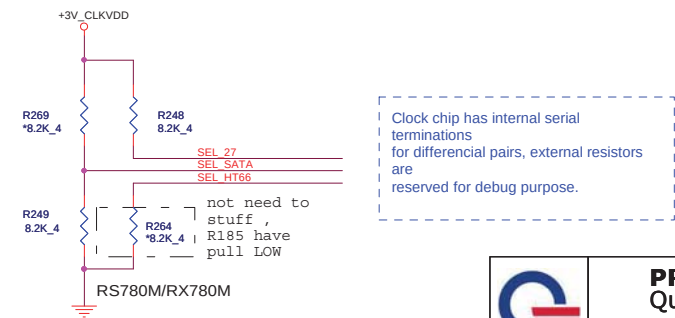
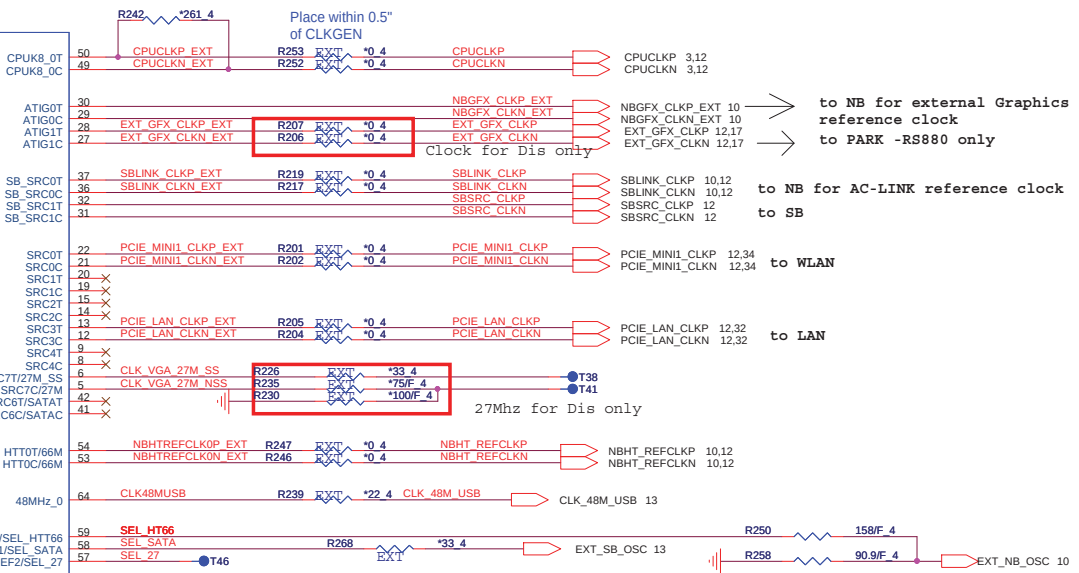
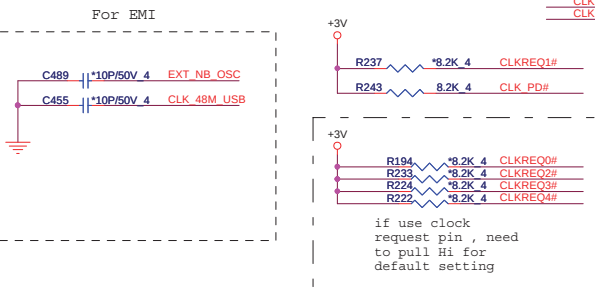
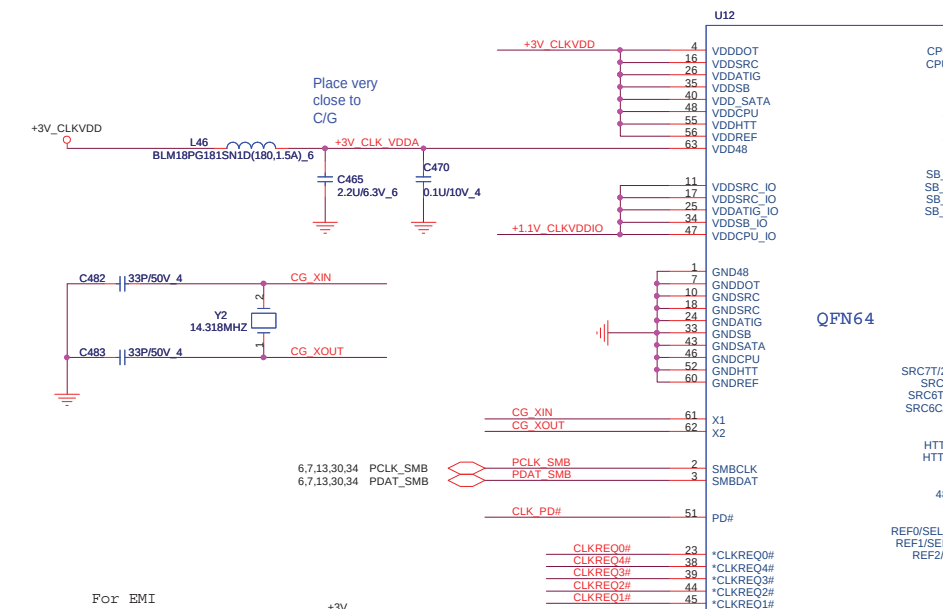
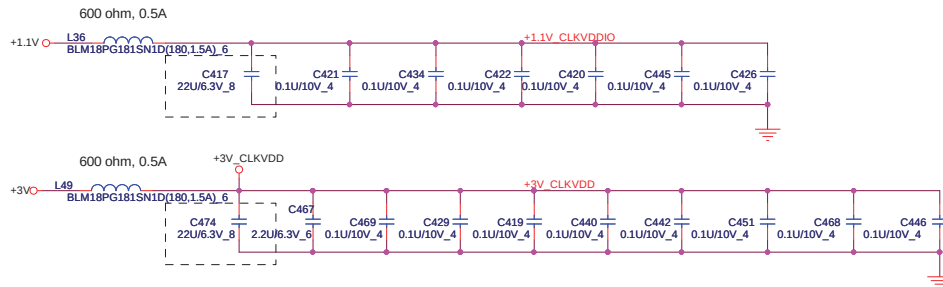
- LAYER 1 : TOP
- LAYER 2 :GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

LX89 SYSTEM DIAGRAM



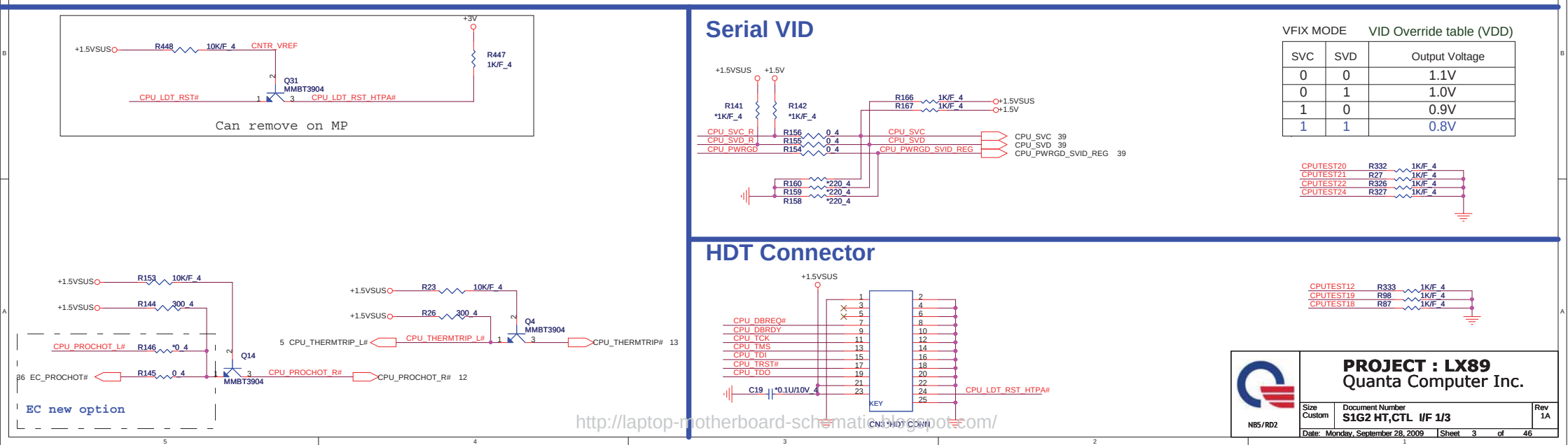
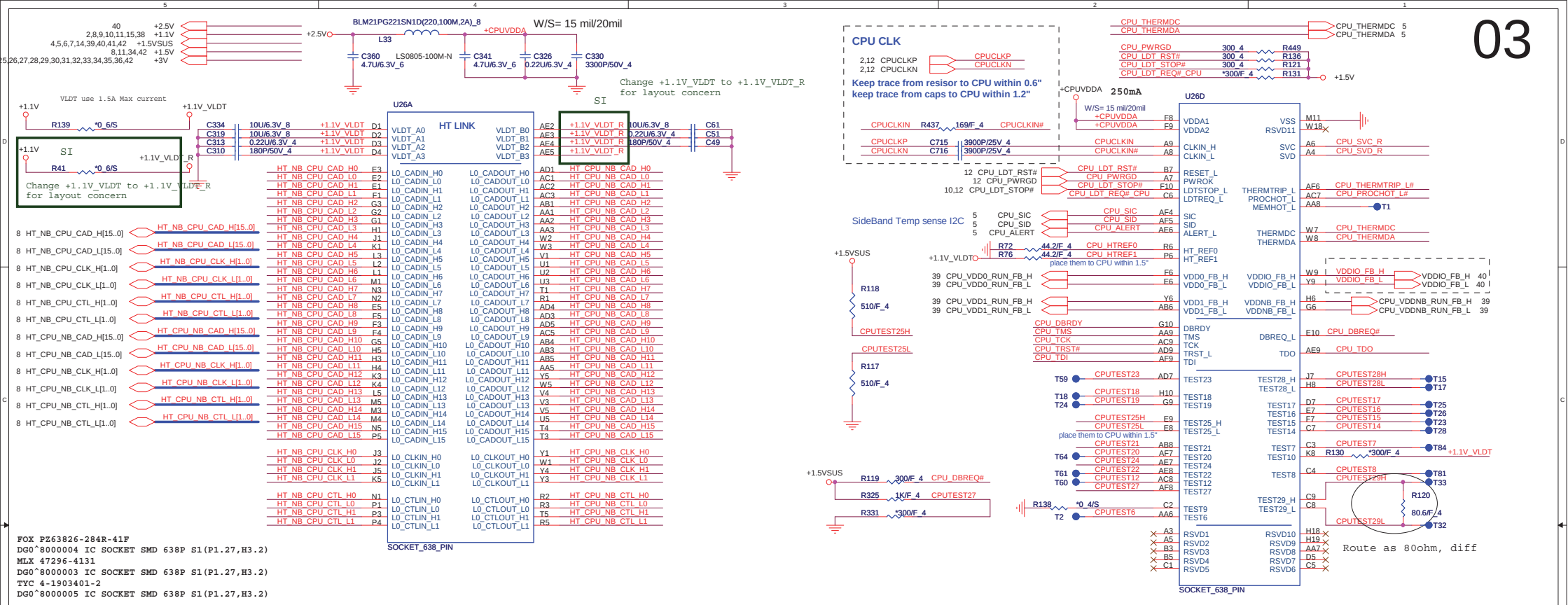
PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
Block Diagram		
Date: Monday, September 28, 2009 Sheet 1 of 46		



SLG8SP628VTR--AL8SP628000 RTM880N-796-- AL000880001		
* default		
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

- Clock chip has internal serial terminations
- for differential pairs, external resistors are reserved for debug purpose.

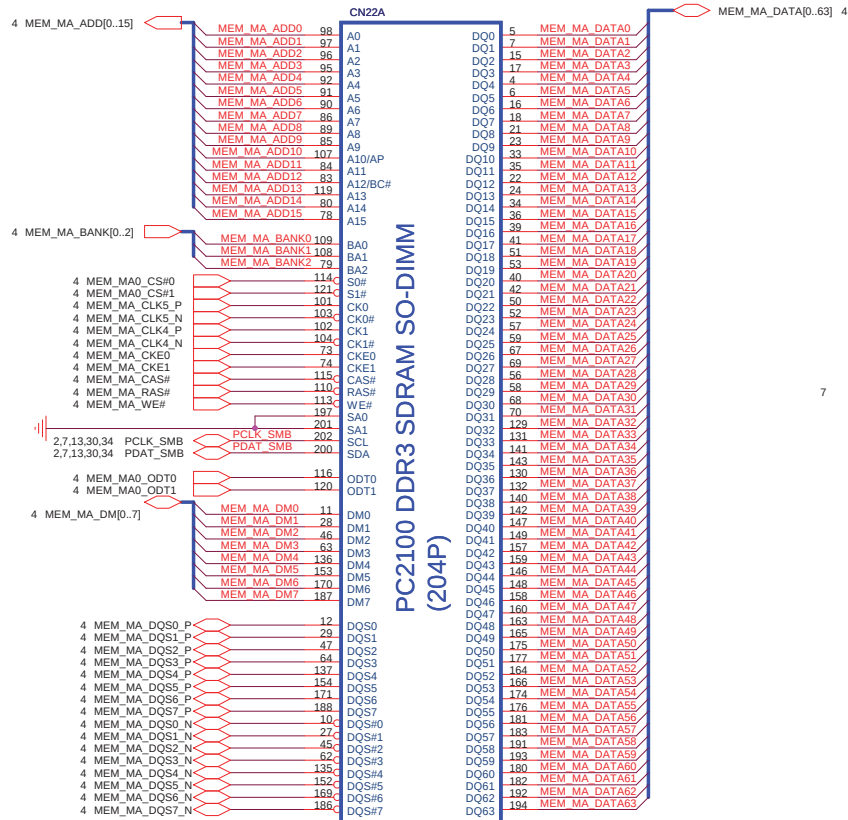





 +1.5VSUS 3,4,5,7,14,39,40,41,42

 +3V 2,3,5,7,10,11,12,13,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42

 +0.75V_DDR_VTT 7,40



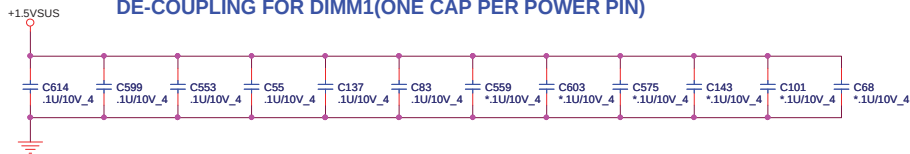
DDR3-DIMM1
H=5.2 footprint: "ddr-c-2013289-204p"
DGMK4000059

SO-DIMM BYPASS PLACEMENT :

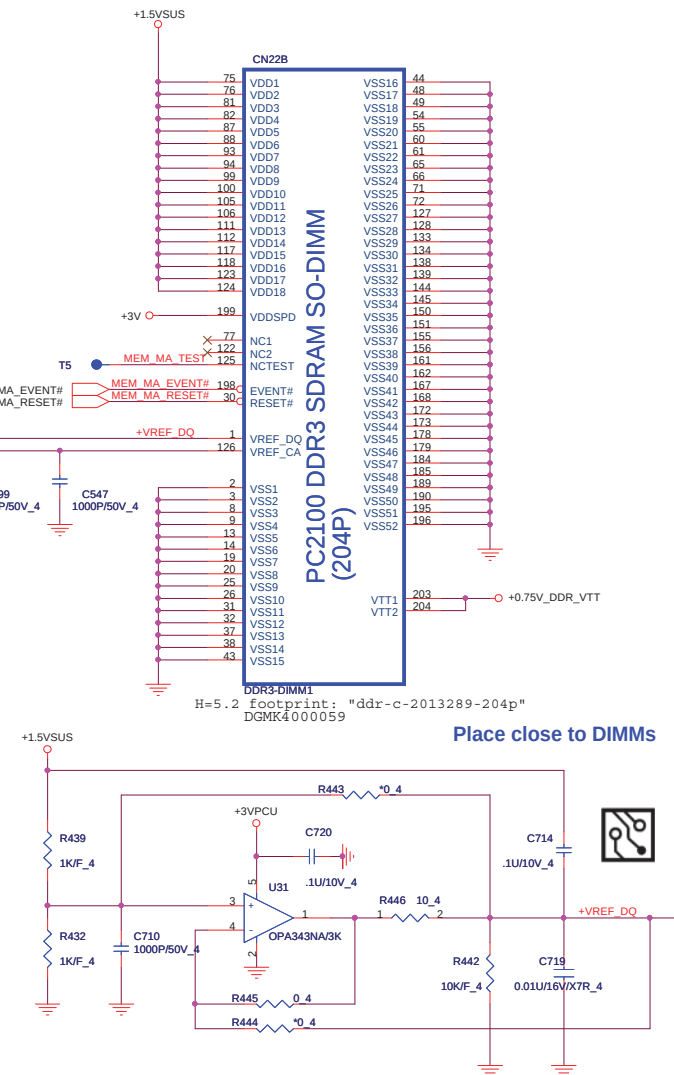
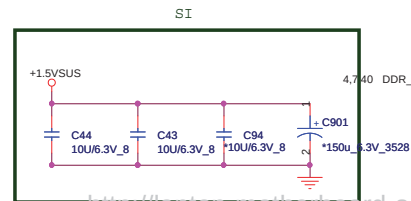
Place these Caps near So-Dimm1.

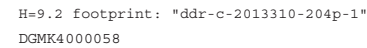
No Vias Between the Trace of PIN to CAP.

DE-COUPLING FOR DIMM1(ONE CAP PER POWER PIN)

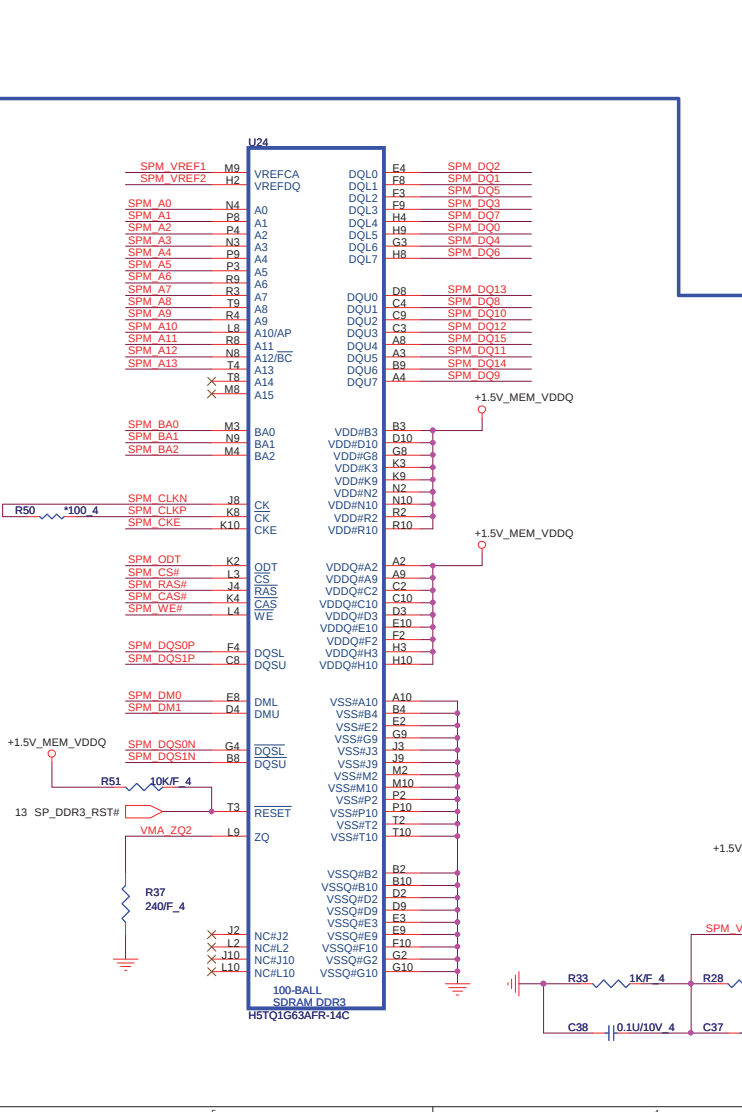


DE-COUPLING FOR DIMM1

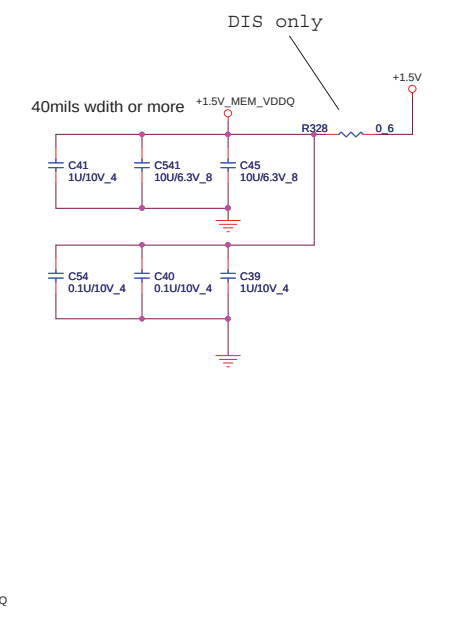


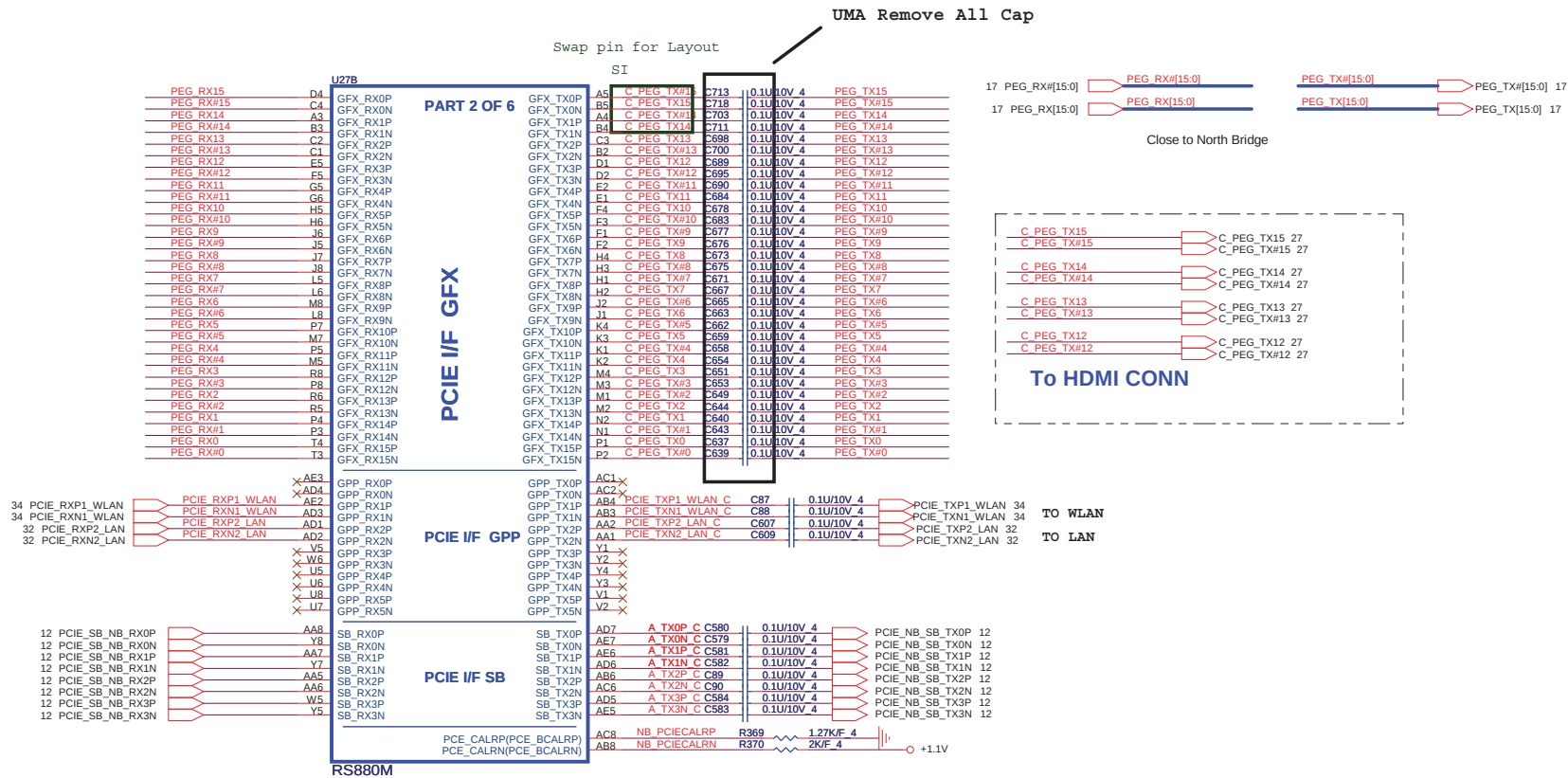


<http://laptop-motherboard-schematic.blogspot.com/>



signals	RS80	RX80
HT_TXCALP	Ra	Ra
HT_TXCALN	301 ohm 1%	1.21k ohm 1%
HT_RXCALP	Rb	Rb
HT_RXCALN	301 ohm 1%	1.21k ohm 1%



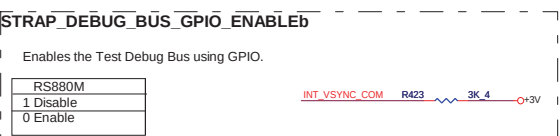
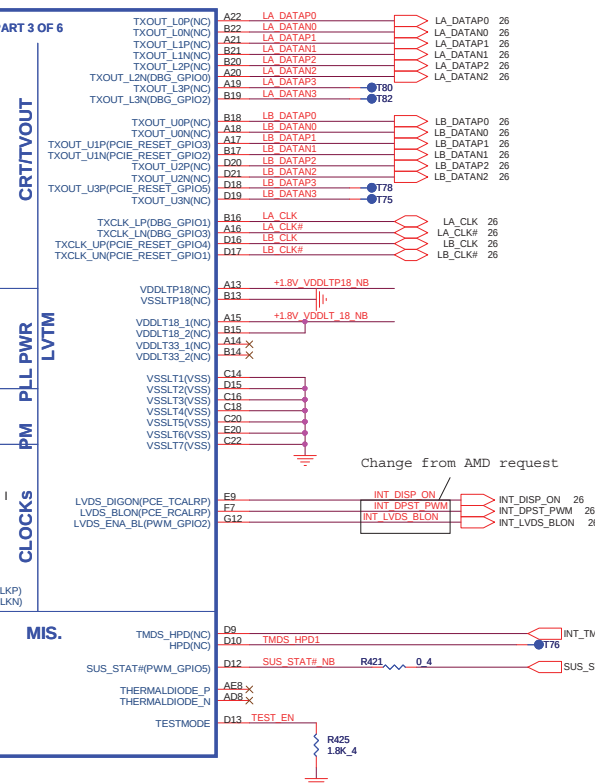
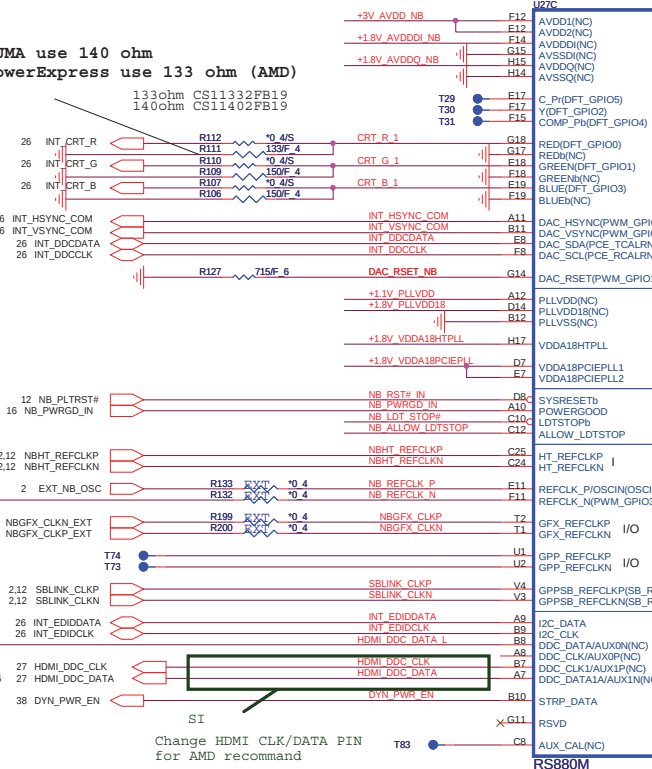
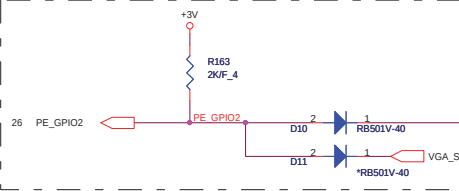
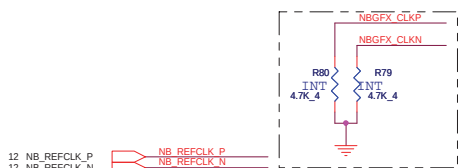


	+3V	2,3,5,6,7,11,12,13,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
	+1.8V	5,8,11,16,26,42
	+1.1V	2,3,8,9,11,15,38
	+1.5V	3,8,11,34,42

R11

R111 for UMA use 140 ohm
for DIS+PowerExpress use 133 ohm (AMD)

```
133ohm CS11332FB19
140ohm CS11402FB19
```

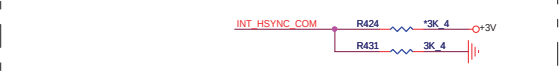


RS880M: Enables Side port memory

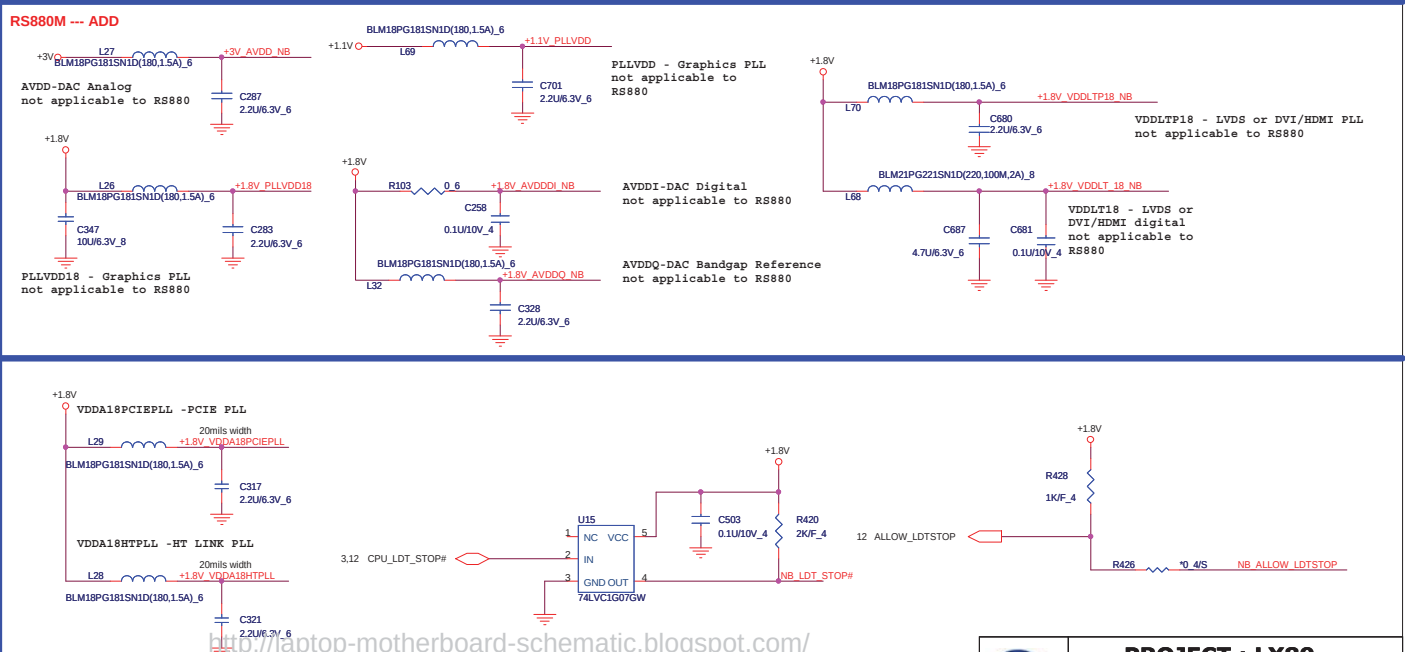
RS880M:INT_HSYNC_COM

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available

Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]



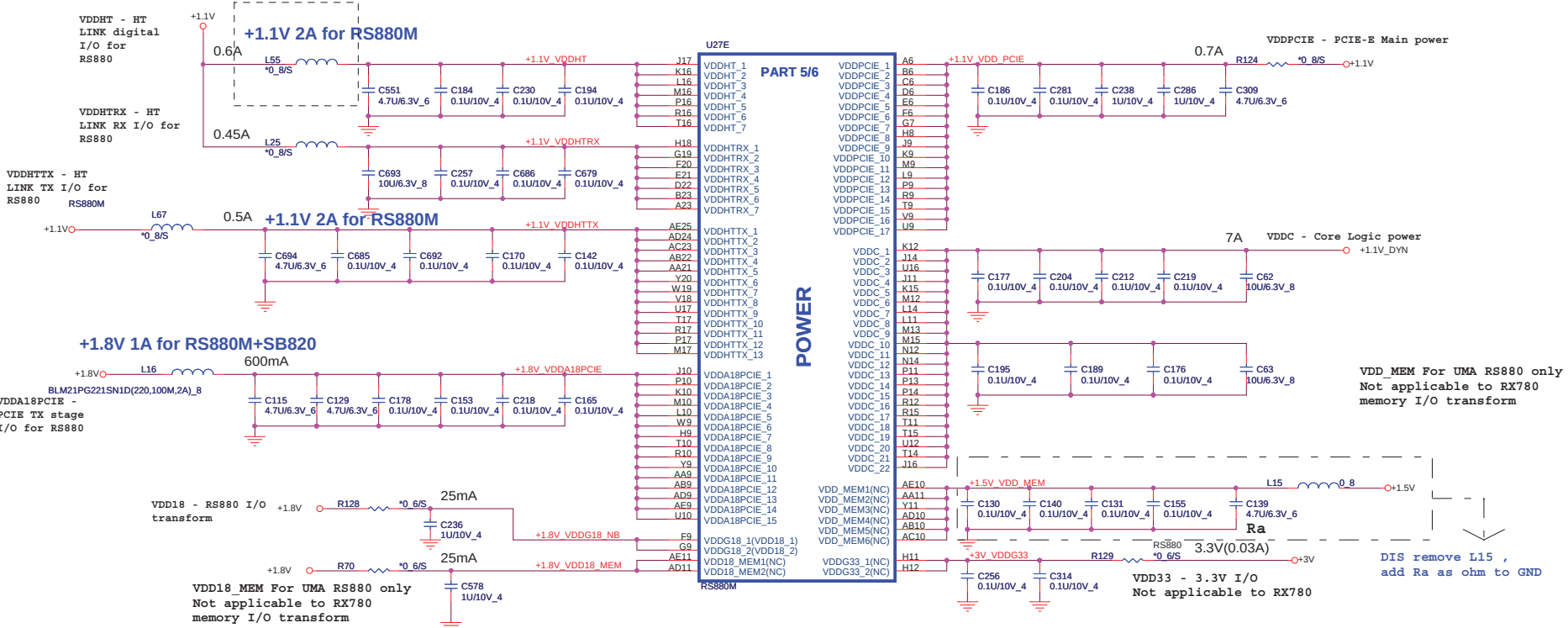
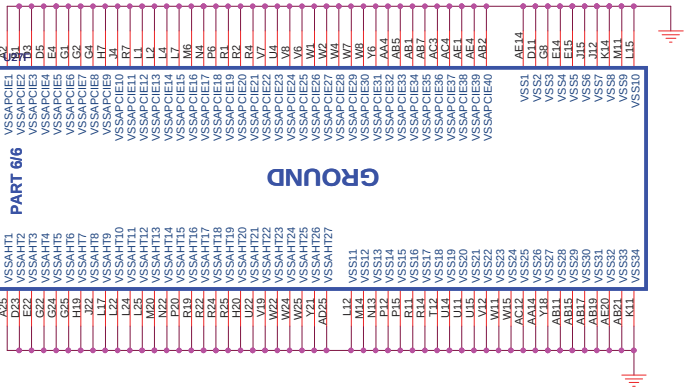
```
-----
For external EEPROM Debug only
```

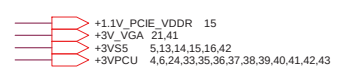


RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL33	NC

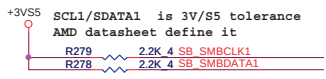
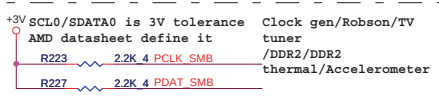
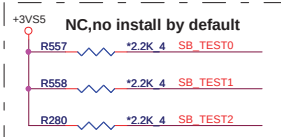
+1.1V_DYN	38
+3V	2,3,5,6,7,10,12,13,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
+1.1V	2,3,8,9,10,15,38
+1.5V	3,8,34,42
+1.8V	5,8,10,16,26,42



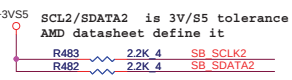


<http://laptop-motherboard-schematic.blogspot.com/>

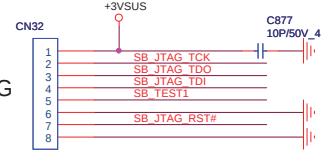
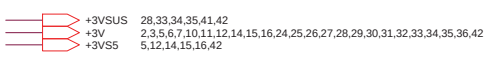
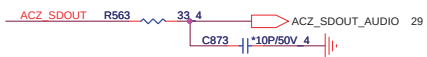
	PROJECT : LX89 Quanta Computer Inc.		
	Size Custom	Document Number SB820-PCIE/PCI/CPU/LPC 1/4	Rev 1A
N85 / RD2	Date: Monday, September 28, 2009	Sheet 12 of 46	



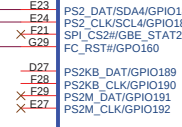
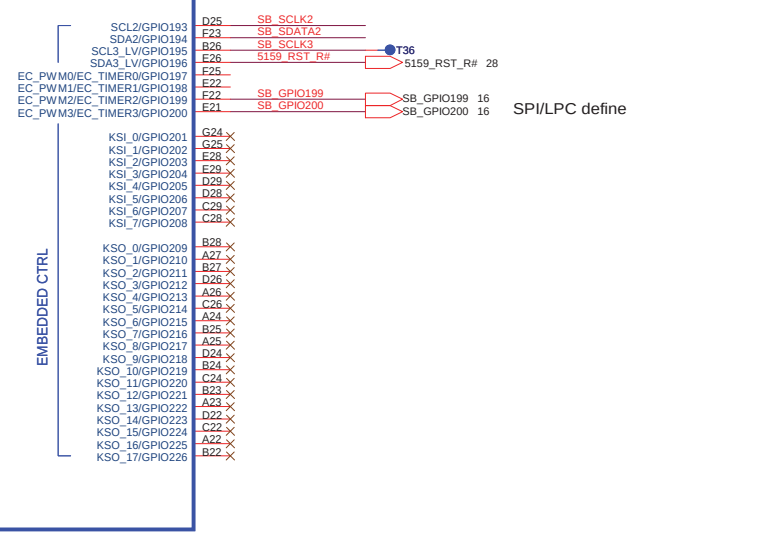
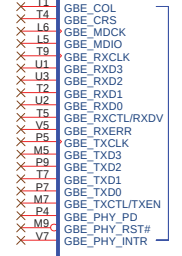
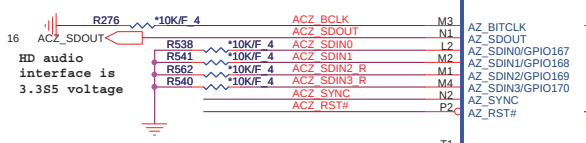
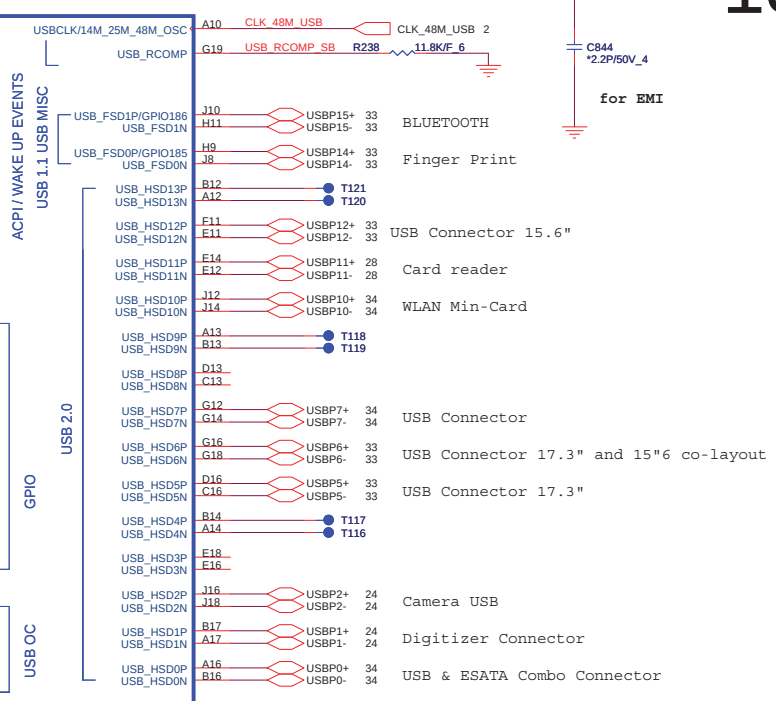
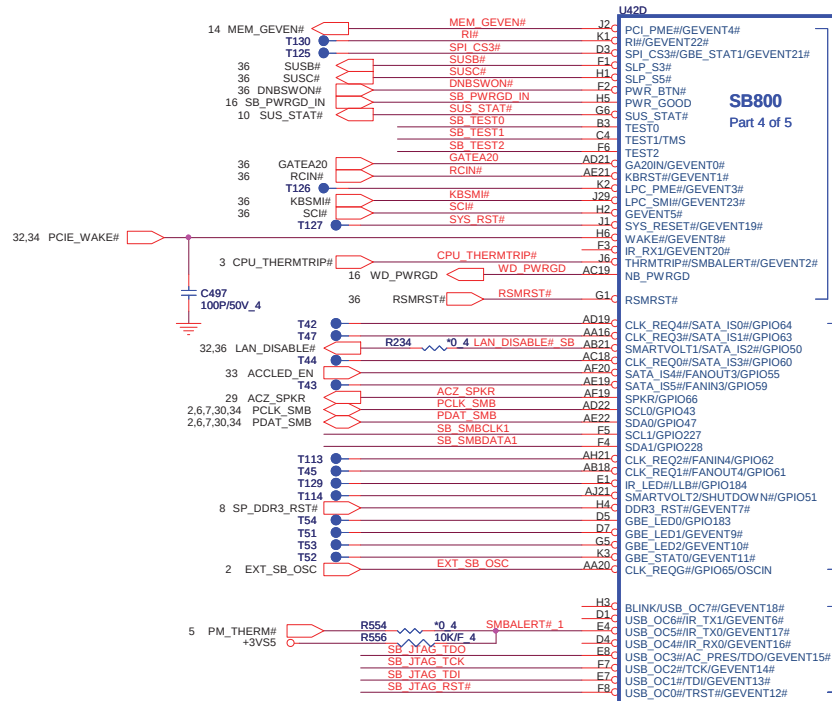
```
remove pull hi
( chip internal
have pull hi )
```



To Azalia



*S/W JTAG DEBUG



SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO SB820

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

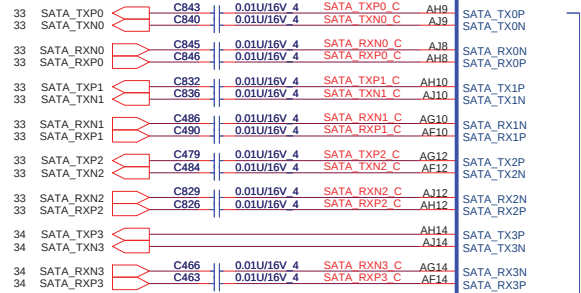


SATA1 HDD

SATA ODD

SATA2 HDD

E-SATA



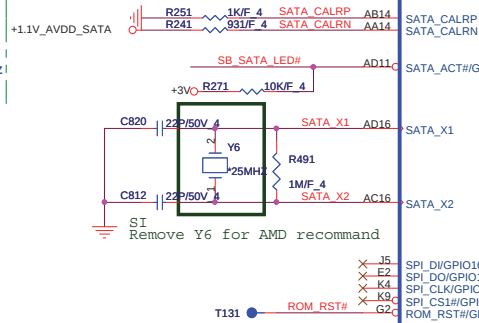
```
XTLVDD_SATA-- SATA
crystal power
```

PLVDD_SATA--
SATA PLL
POWER



PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

NOTE:
R361 IS 1K 1% FOR 25MHZ
XTAL, 4.99K 1% FOR 100MHZ
INTERNAL CLOCK

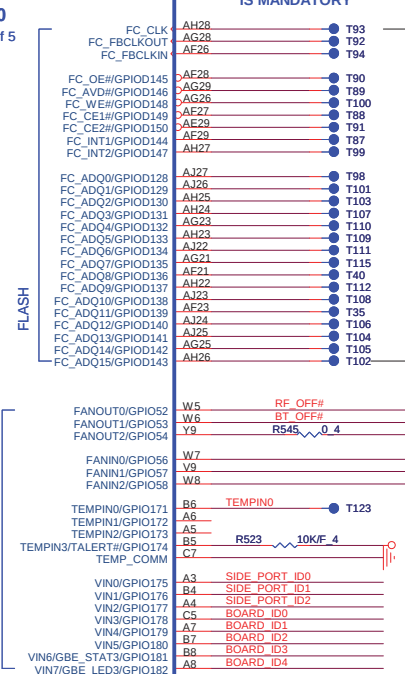


Remove Y6 for AMD recommand

SERIAL ATA

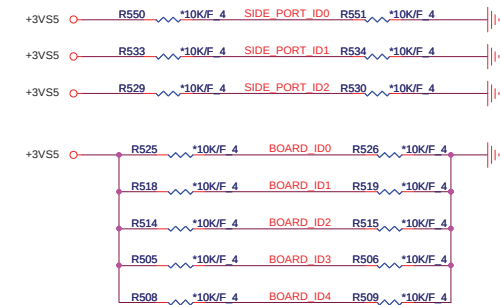
HW MONITOR

SPI ROM

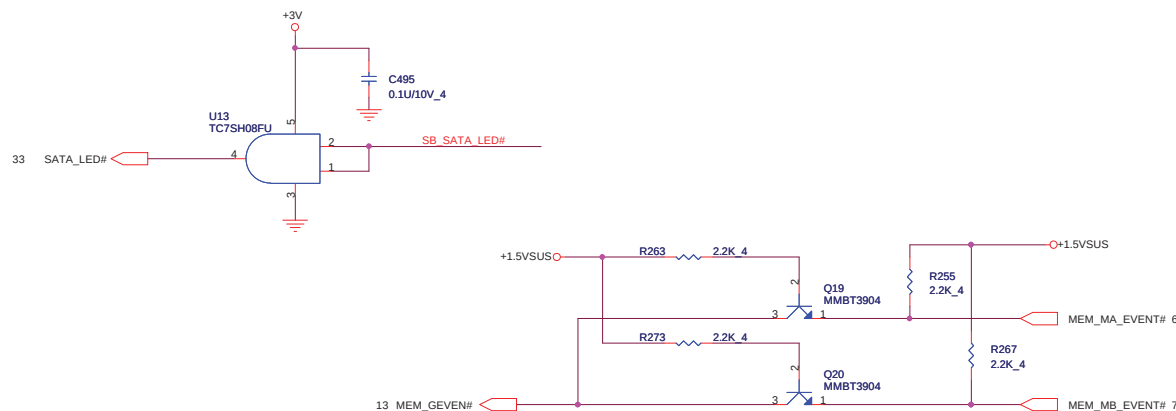


IF USE, power need ready

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port



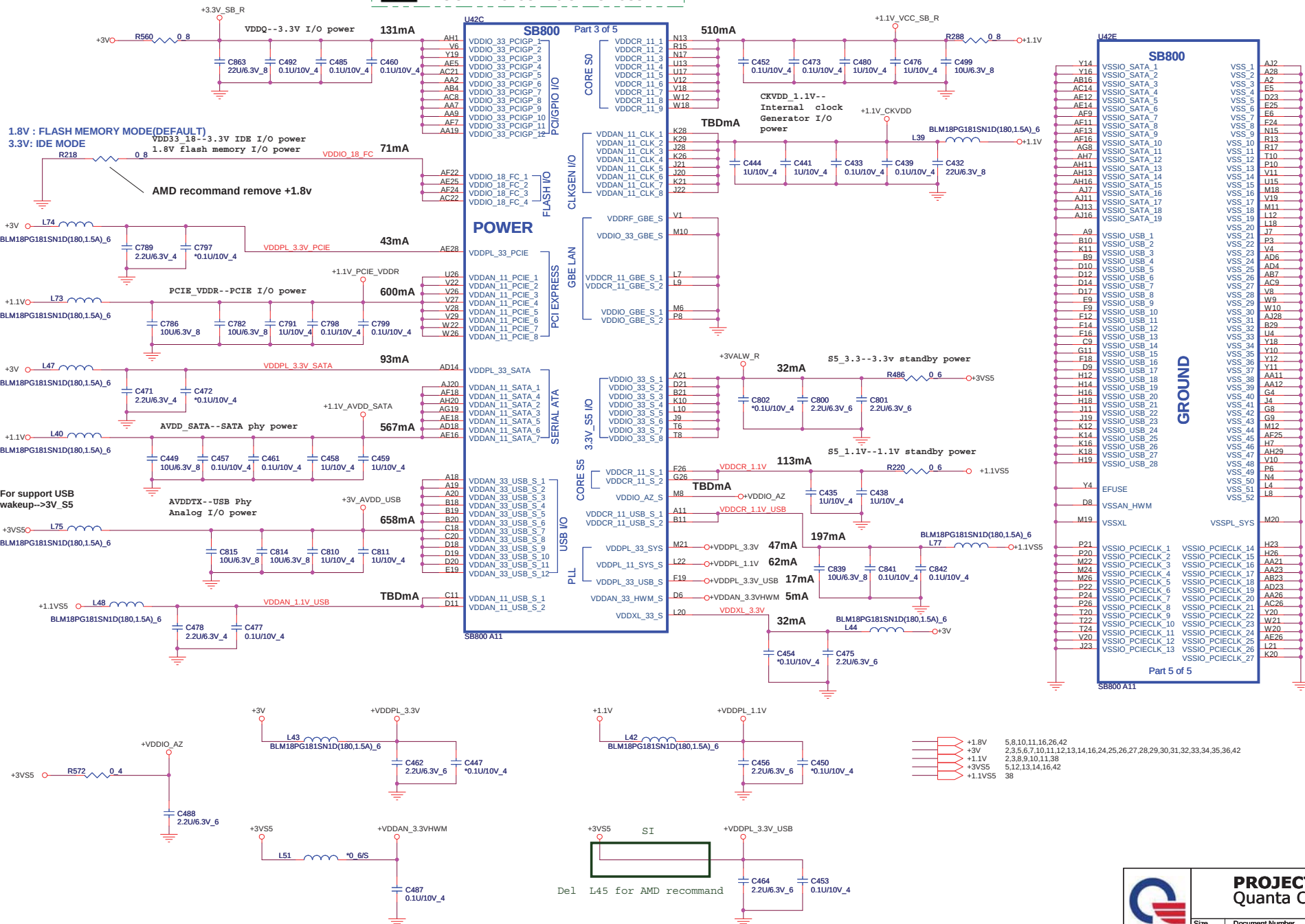
ID4	ID3	ID2	ID1	ID0	
0	0	0	0	0	LX8 UMA
0	0	0	0	1	LX9 UMA
0	0	0	1	0	LX8 Madison
0	0	0	1	1	LX8 Park
0	0	1	0	0	LX9 Park
0	0	1	0	1	
0	0	1	1	0	
0	0	1	1	1	





PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

VDD-- S/B CORE power



<http://laptop-motherboard-schematic.blogspot.com/>

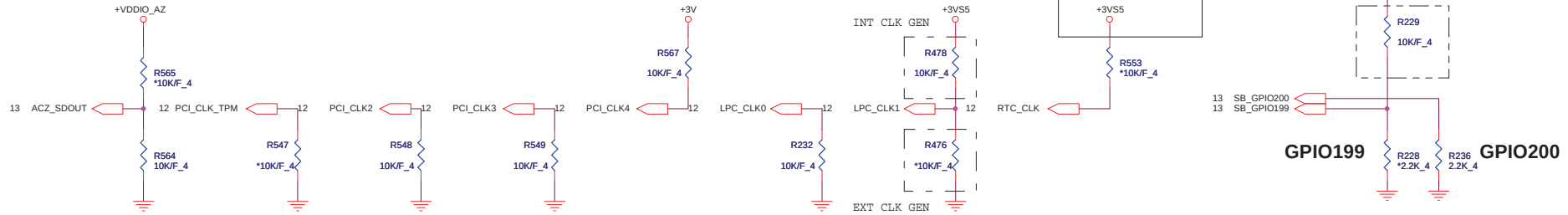


PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number SB820-PWR/DECOUPLING 4/4	Rev 1A
Date: Monday, September 28, 2009	Sheet 15 of 46	

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS



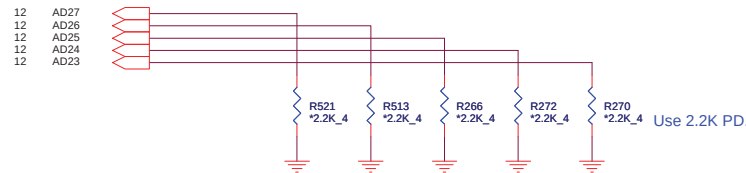
REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

TYPE	GPIO199	GPIO200
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

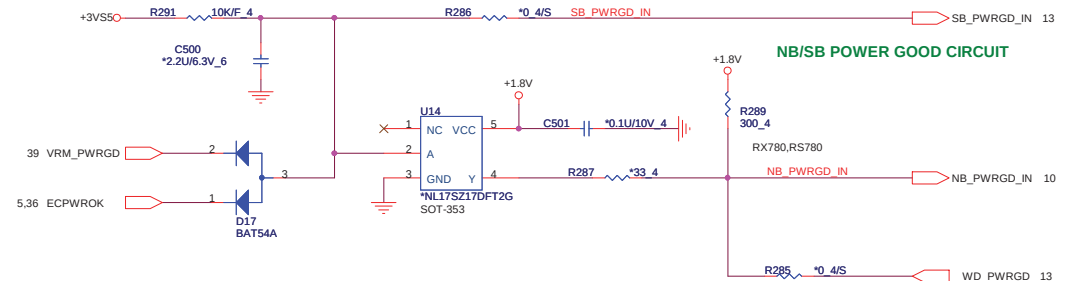
DEBUG STRAPS

SB820 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

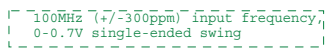
NB_PWRGD IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

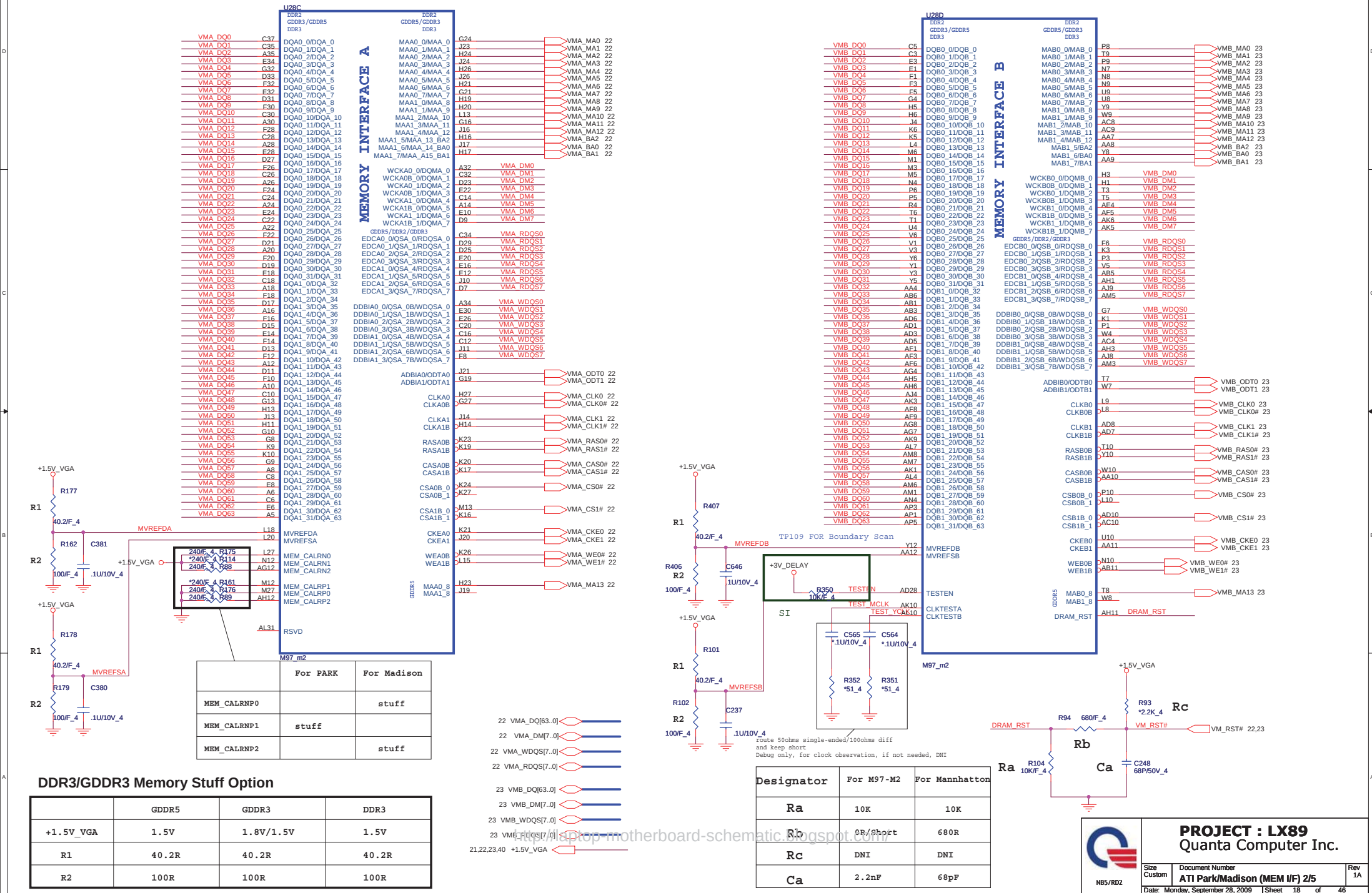


AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

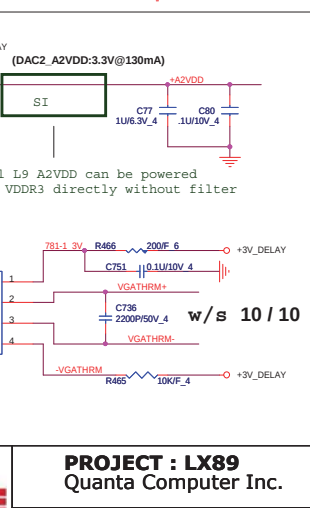
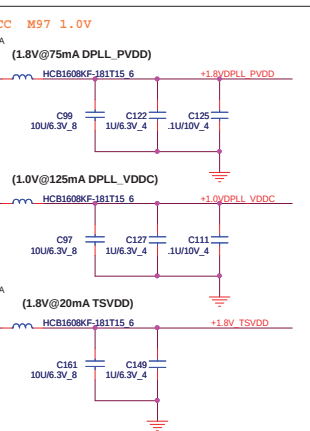
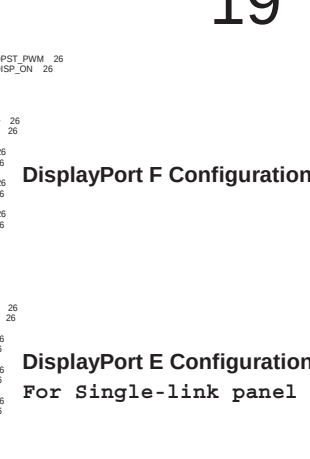
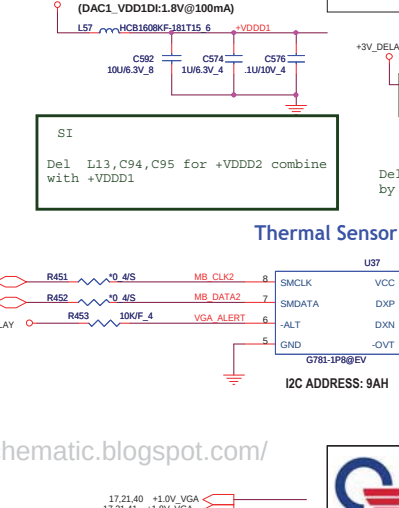
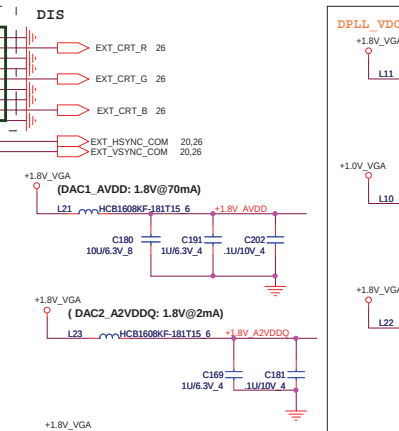
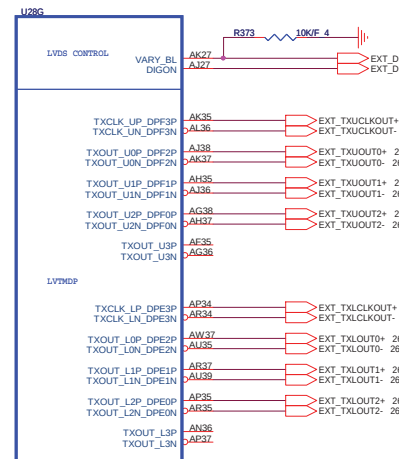
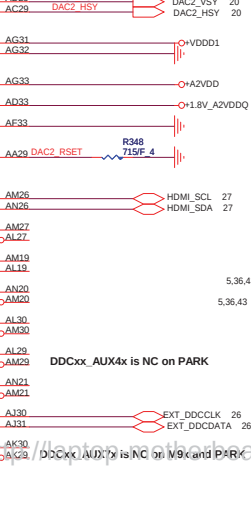
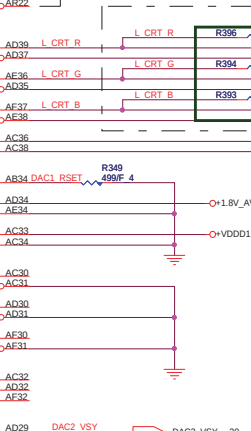
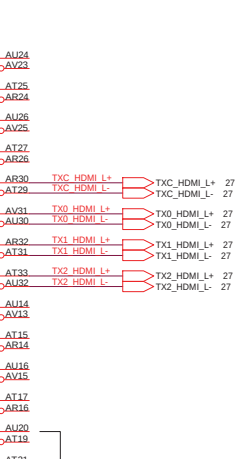
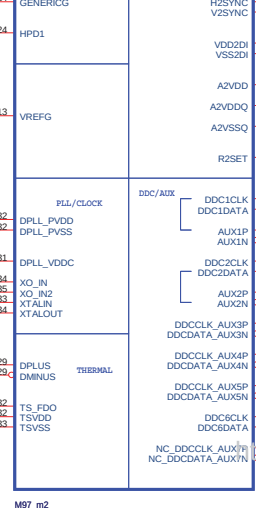
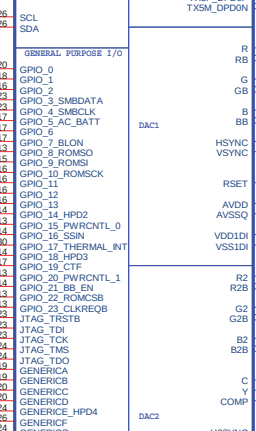
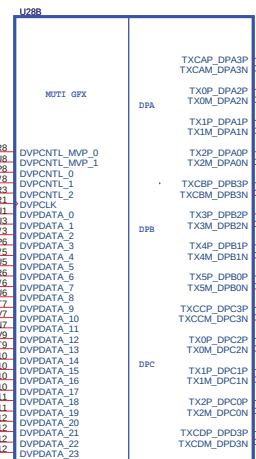
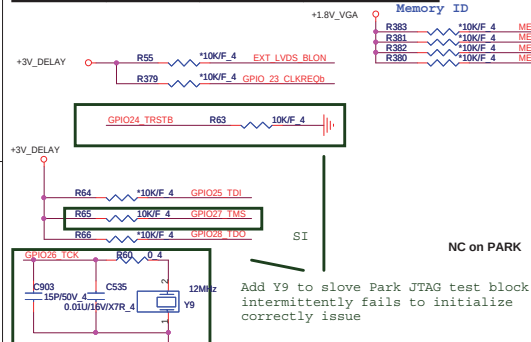
<http://laptop-motherboard-schematic.blogspot.com/>

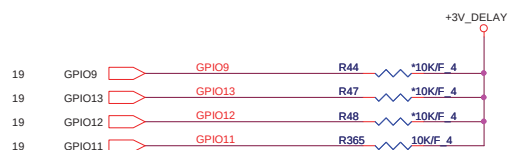
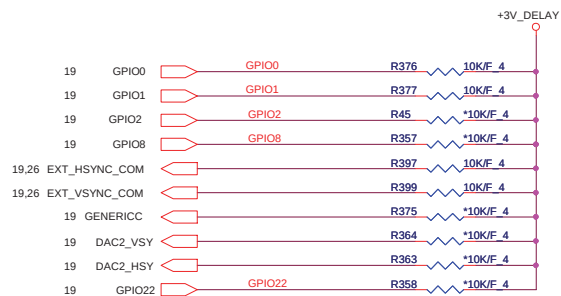
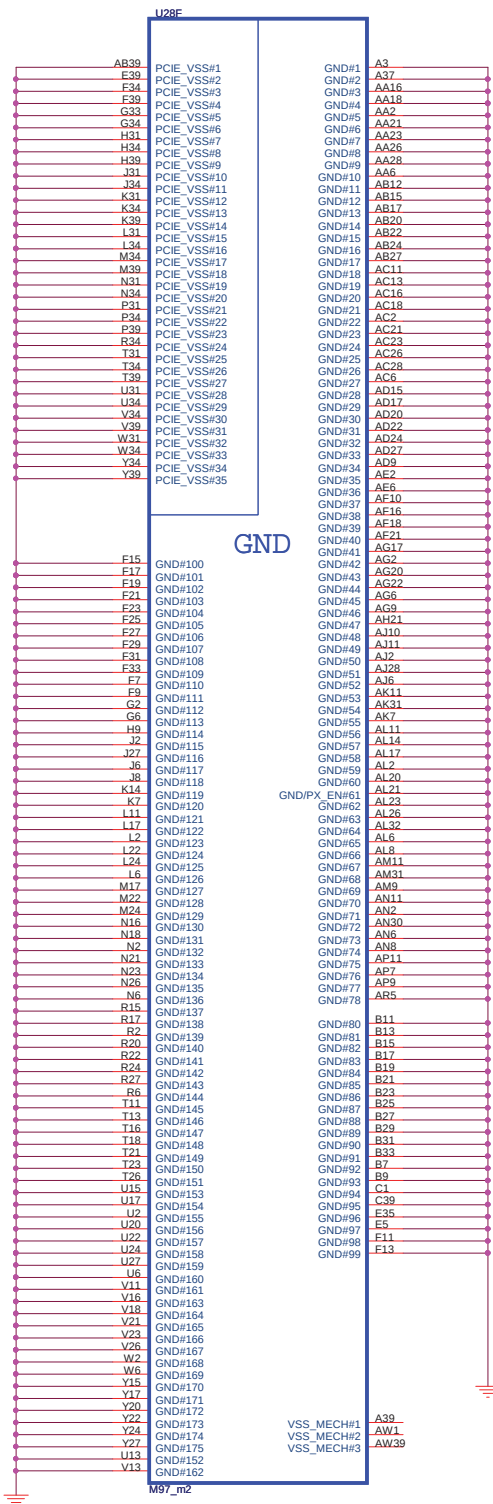
	PROJECT : LX89 Quanta Computer Inc.		
	Size Custom	Document Number SB820-STRAPS	Rev 1A
	Date: Monday, September 28, 2009 Sheet 16 of 46		





MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung	5416-800MHz	X4W1G1646E-HC12
0001	Hynix	5416-800MHz	H1T016384E-A12
0011			Reserved
0100			Reserved
0101			Reserved
0110			Reserved
0111			Reserved
1000			Reserved
1001			Reserved
1010			Reserved
1011			Reserved
1100			Reserved
1101			Reserved
1110			Reserved
1111			Reserved





Memory Aperture size fix 256M

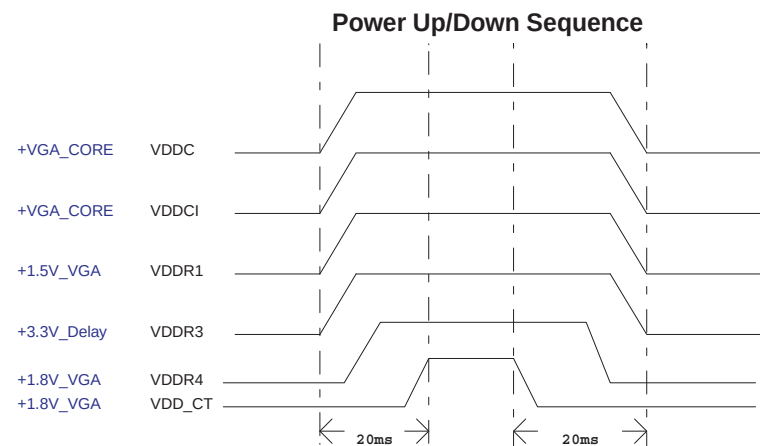
GPIO9		GPIO13	GPIO12	GPIO11
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

<http://laptop-motherboard-schematic.blogspot.com/>

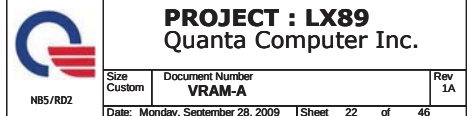
CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 - Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 - Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS	
H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO21_BB_EN	

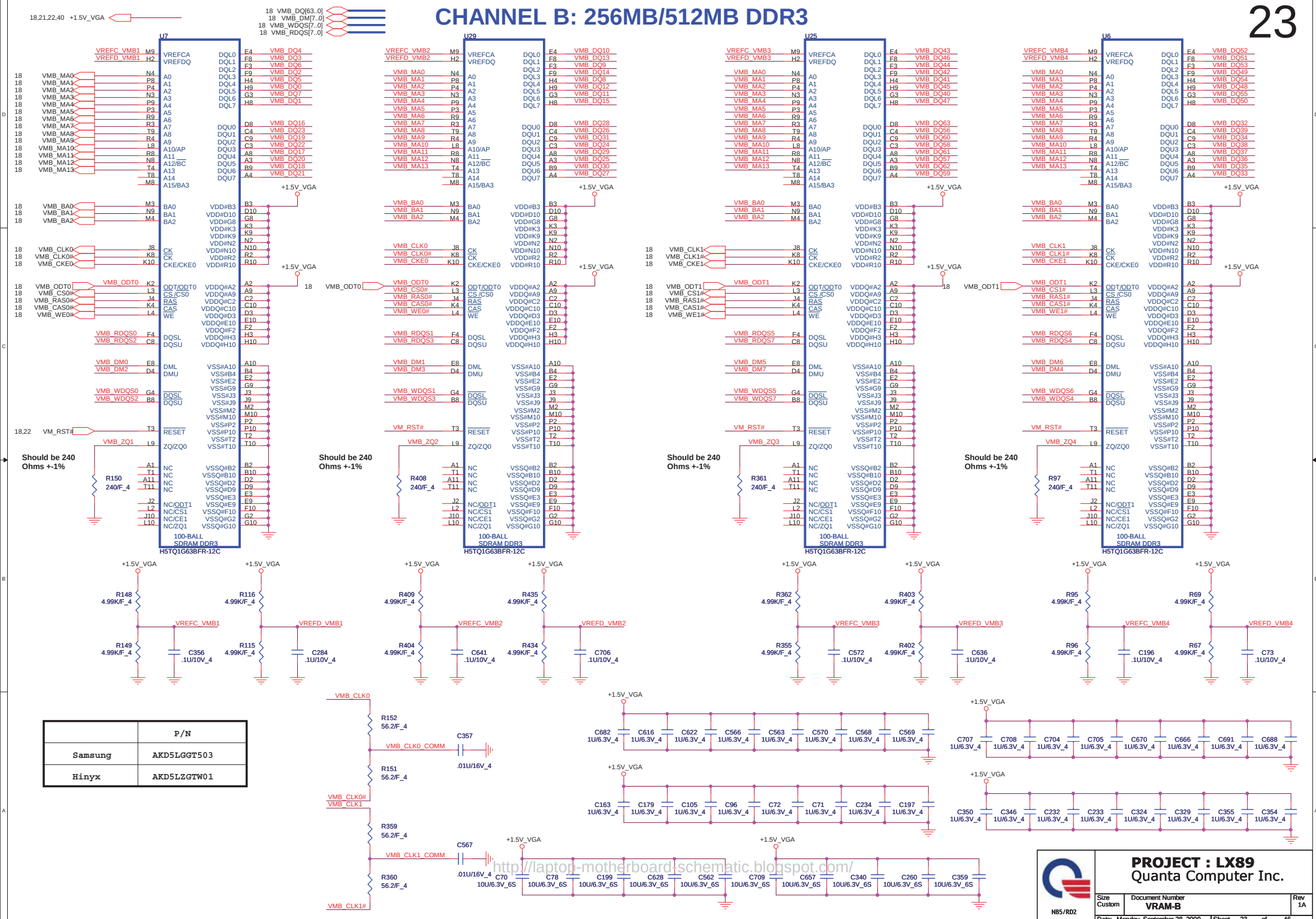


	PROJECT : LX89 Quanta Computer Inc.	
	Size Custom Date: Monday, September 28, 2009	Document Number ATI Park/Madison(GND&Str&Ther)4/5 Sheet 20 of 46

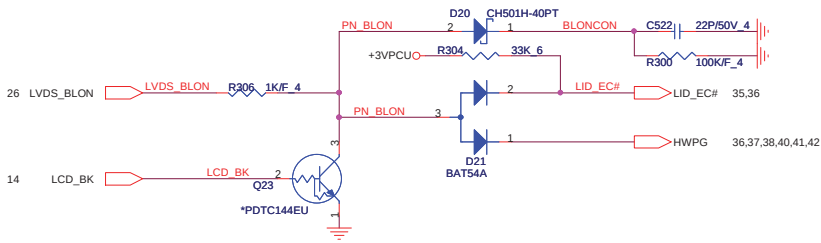
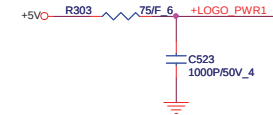
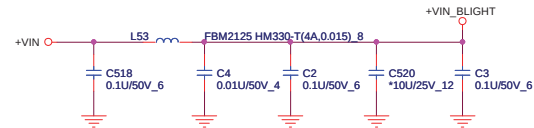




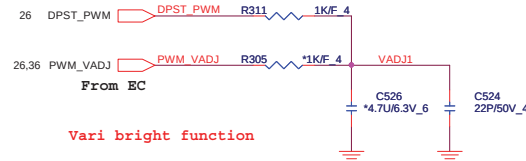
CHANNEL B: 256MB/512MB DDR3



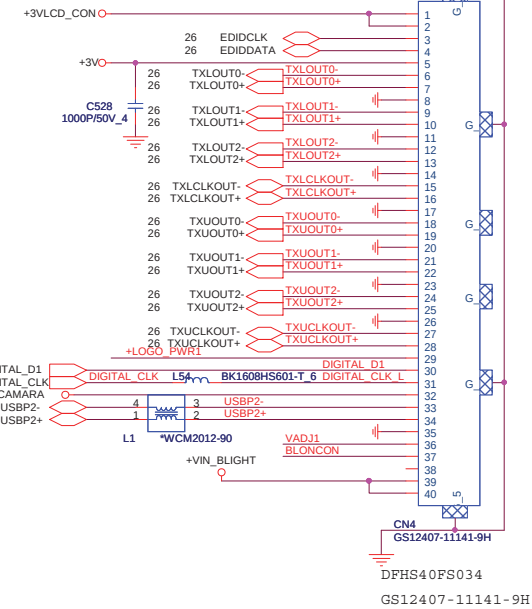
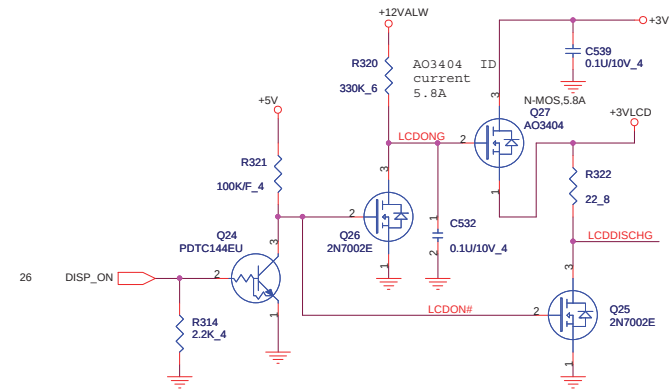
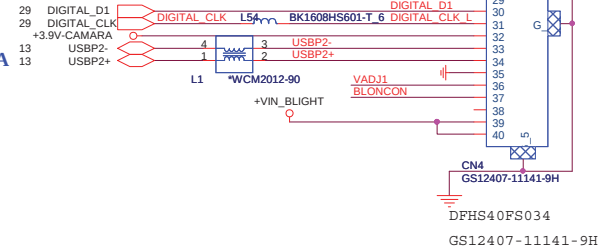
+VIN	31,37,38,39,40,41,42,43
+12VALW	33,35,40,41,42
+3V	2,3,5,6,7,10,11,12,13,14,15,16,25,26,27,28,29,30,31,32,33,34,35,36,42
+3V_DELAY	18,19,20,21,26,27
+5V	25,26,27,28,29,33,34,35,42



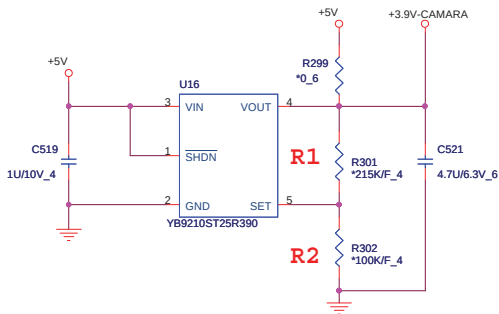
From Switch



Vari bright function

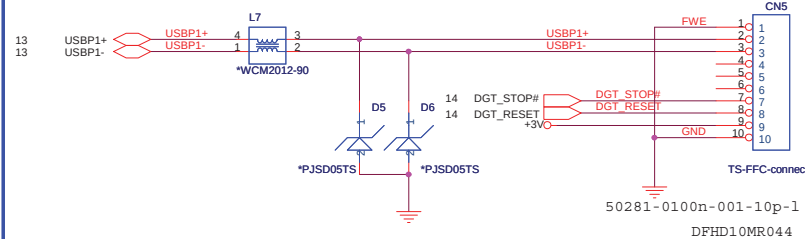
DMIC
CAMERA

CAMERA POWER



$$V_{out} = 1.25 (1 + R1/R2)$$

Digitizer Connector



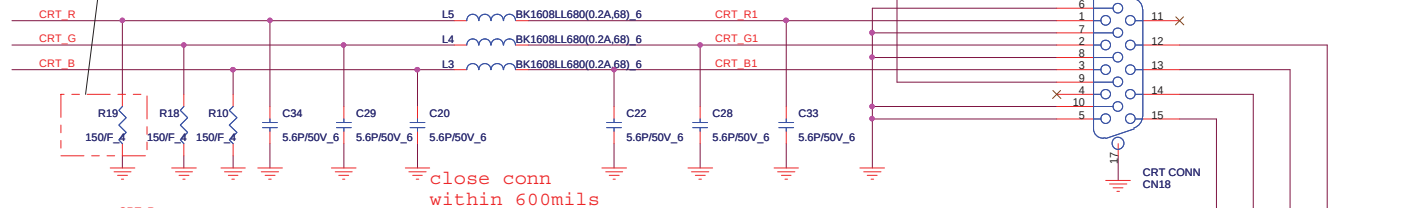
$$V_{out} = 1.25 (1 + R1/R2)$$

 NBS/RD2	PROJECT : LX89	
	Quanta Computer Inc.	
Size Custom	Document Number	Rev 1A
LCD CONN		
Date: Monday, September 28, 2009	Sheet 24	of 46

CRT PORT

+3V 2,3,5,6,7,10,11,12,13,14,15,16,24,26,27,28,29,30,31,32,33,34,35,36,42
+5V 24,26,27,28,29,33,34,35,42
+3V_DELAY 18,19,20,21,26,27

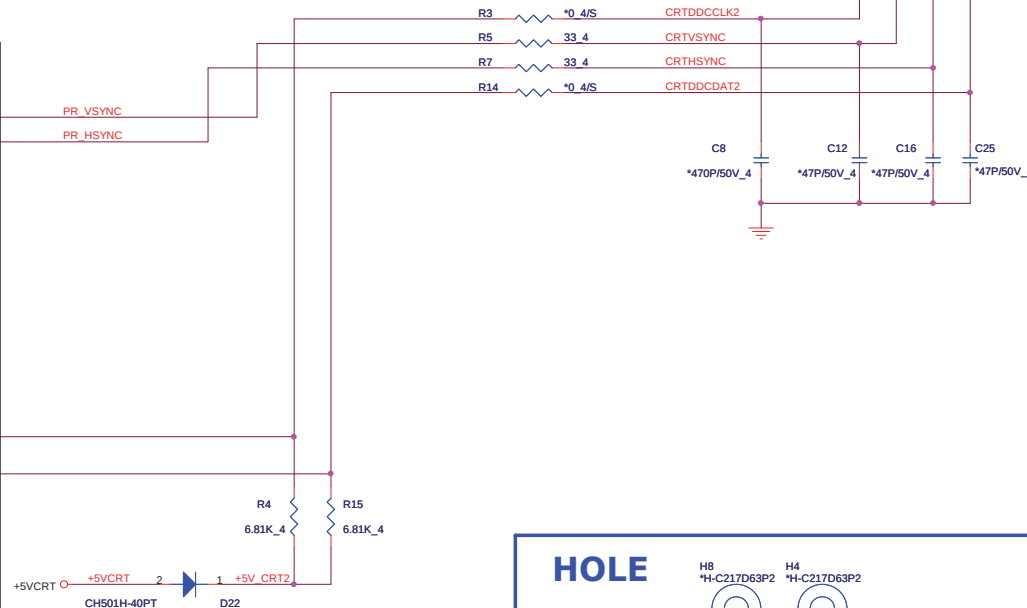
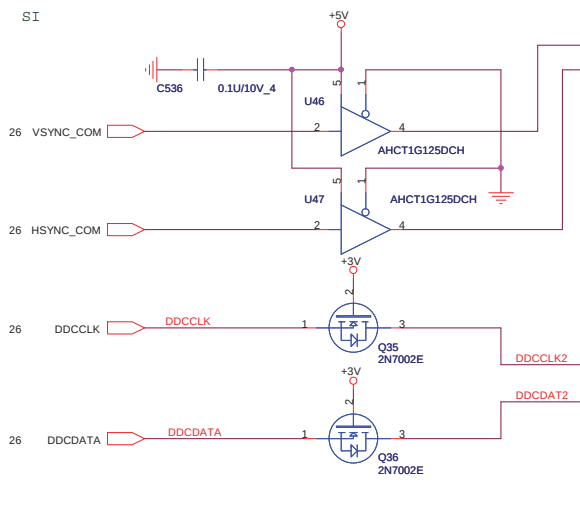
R19 for UMA use 140 ohm
for DIS+PowerExpress use 150 ohm (AMD)



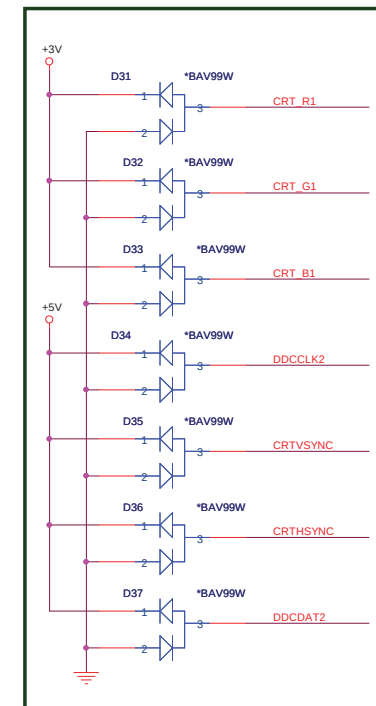
26 CRT_R CRT_R
26 CRT_G CRT_G
26 CRT_B CRT_B

Del U19,C534,C535 add U46,U47,Q35,Q36 for ME height limit

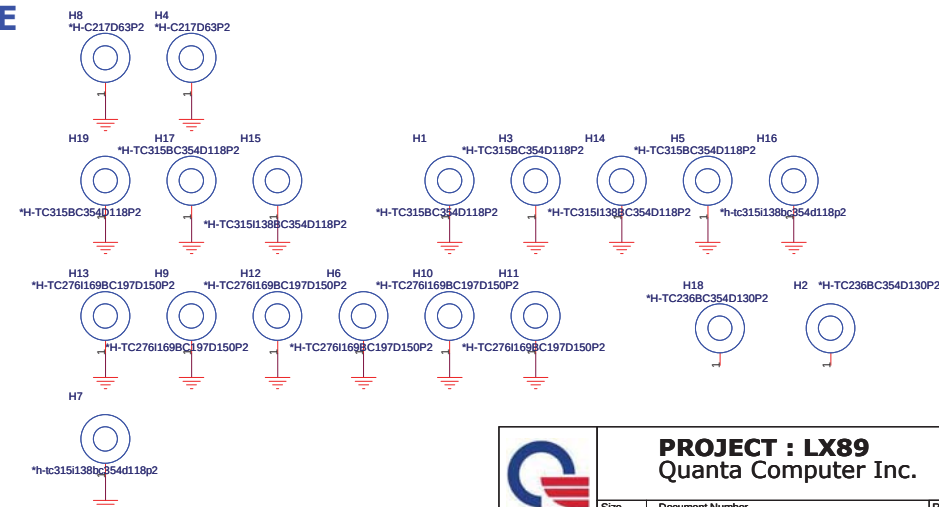
SI



SI Add D31-D37 for ME height limit



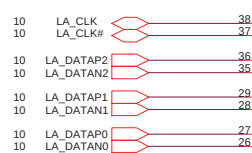
HOLE



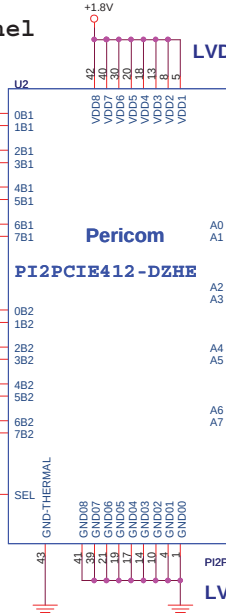
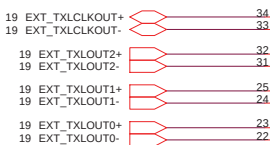
 PROJECT : LX89 Quanta Computer Inc.		
Size Custom	Document Number CRT&HOLE	Rev 1A
Date: Monday, September 28, 2009	Sheet 25	of 46

For Single-link panel

IGPU_Channel-A



DGPU_Channel-A



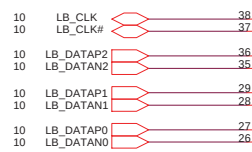
LVDS Channel Switch

SELx	Ay
HIGH	B2
LOW	B1

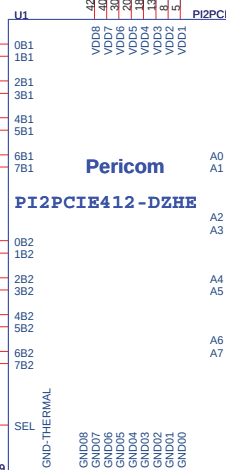
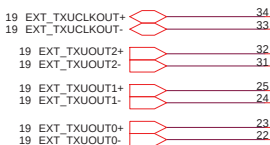
LVDS Channel Switch

SEL	FUNCTION
HIGH	DGPU
LOW	IGPU

IGPU_Channel-B



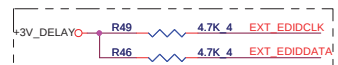
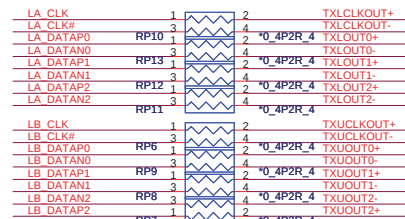
DGPU_Channel-B



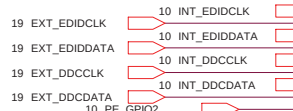
SELx	Ay
HIGH	B2
LOW	B1

SEL	FUNCTION
HIGH	DGPU
LOW	IGPU

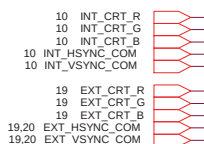
OPTION SIGNAL FROM NB to LVDS for UMA



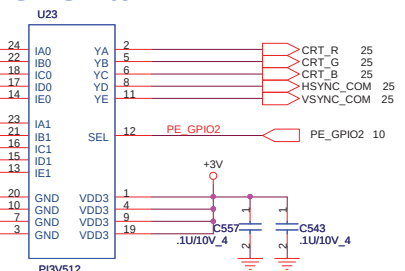
LVDS/CRT DDC Switch



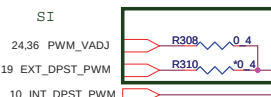
VGA Switch



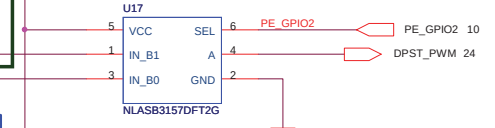
VGA Switch



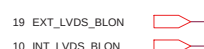
DIS Change Vari bright function from EC control



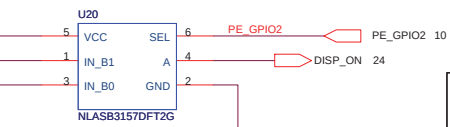
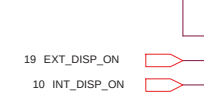
DPST Control



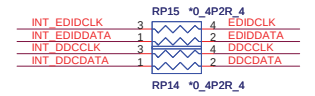
Back Light On control



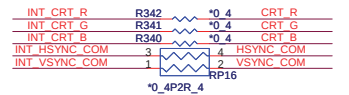
LCDVcc control



OPTION SIGNAL FROM NB to LVDS/CRT for UMA



OPTION SIGNAL FROM NB to CRT for UMA



OPTION DPST SIGNAL FROM NB to LVDS for UMA



OPTION Back Light SIGNAL FROM NB to LVDS for UMA

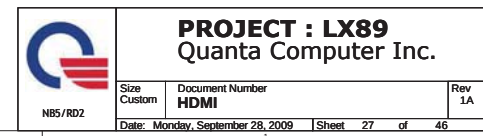
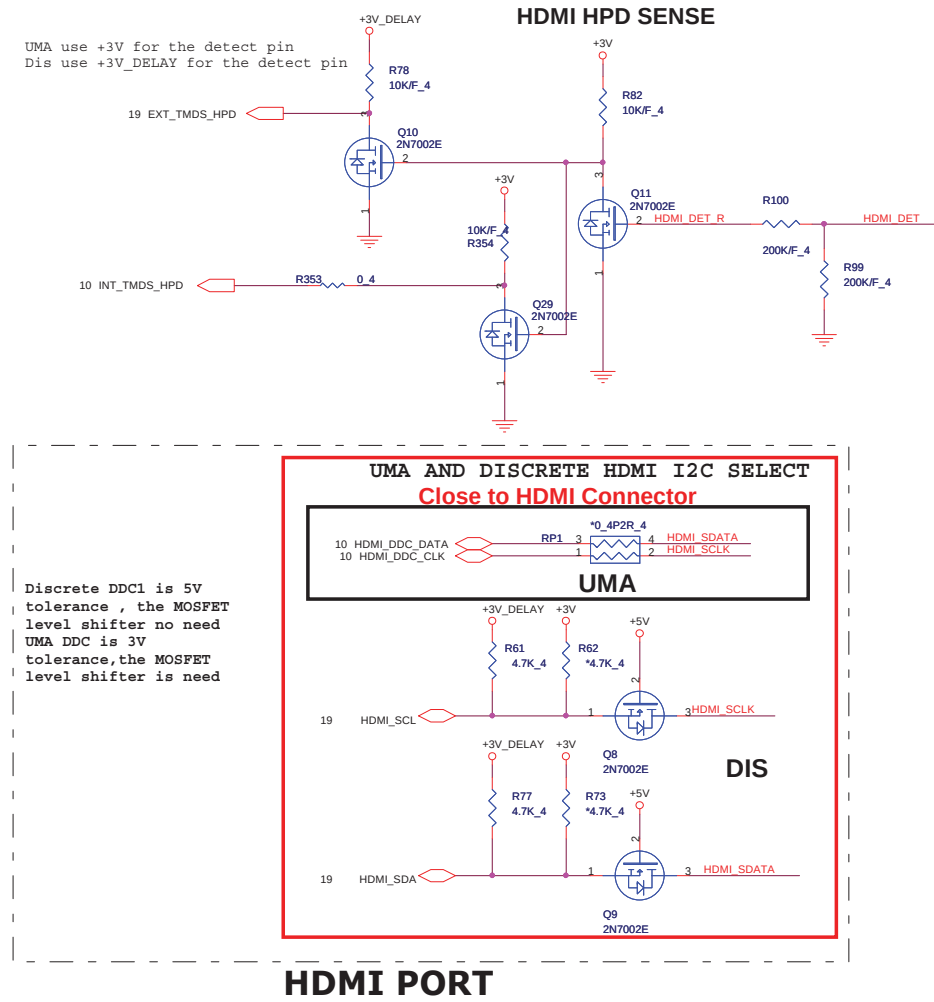


OPTION LCDVCC SIGNAL FROM NB to LVDS for UMA



PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LVDS/CRT Hyper_switch	1A
Date: Monday, September 28, 2009	Sheet 26 of 46	



XTAL control pin for
12Mhz crystal or 48Mhz
clk in

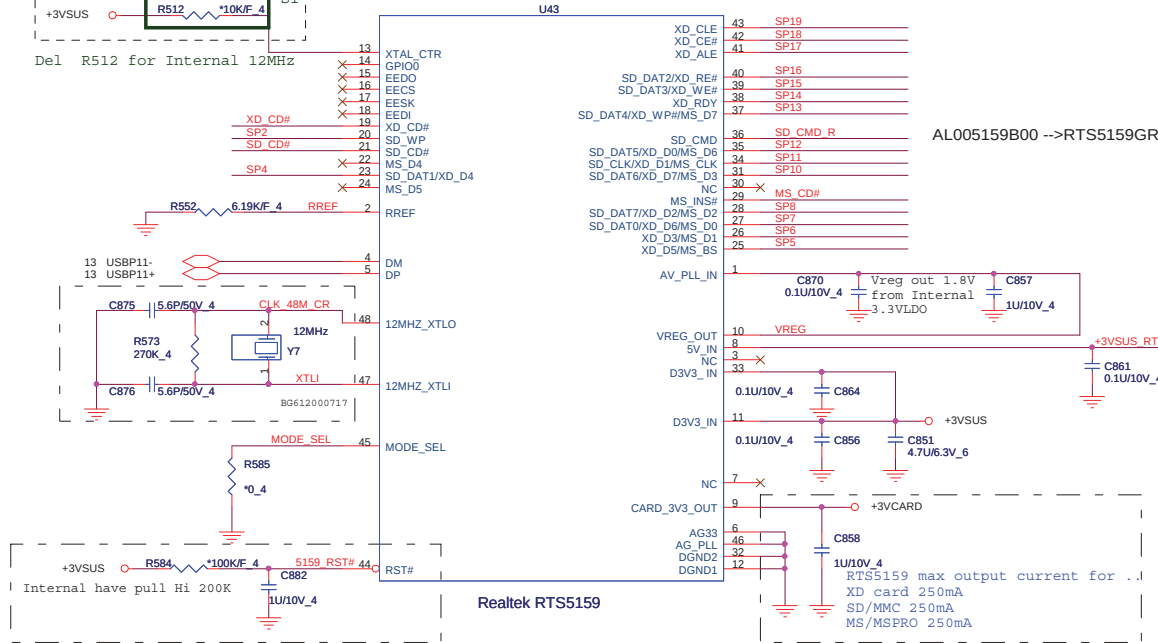
+3VSUS

R512

*10K/F 4

SI

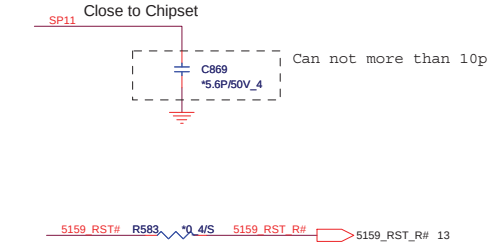
Del R512 for Internal 12MHz



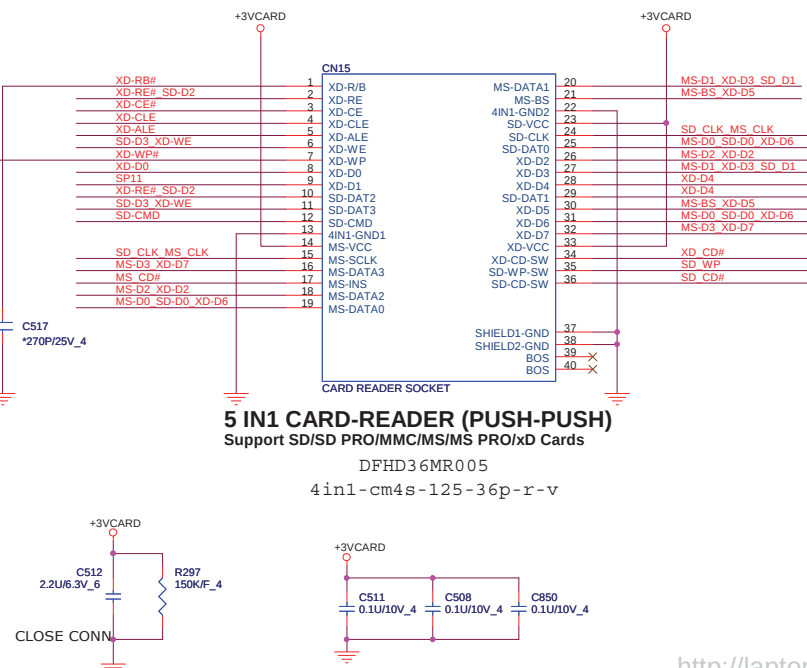
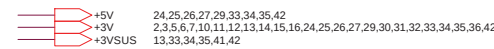
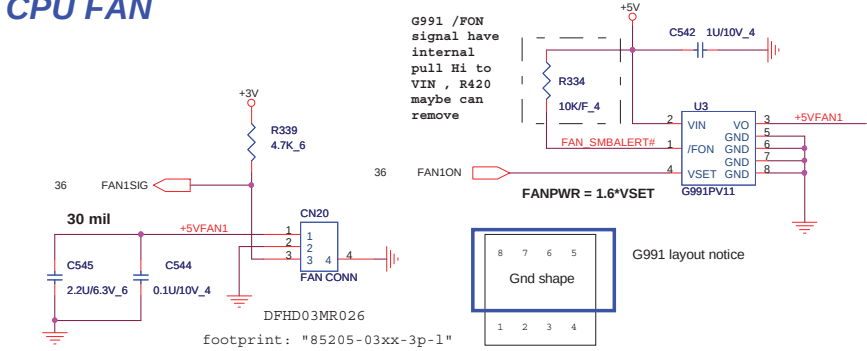
Note:

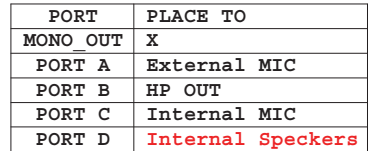
	SD/MMC	MS	XD
SP1			XD_CD#
SP2	SD WP		
SP3	SD CD#		
SP4	SD DAT1		XD D4
SP5		MS BS	XD D5
SP6		MS D1	XD D3
SP7	SD DAT0	MS D0	XD D6
SP8	SD DAT7	MS D2	XD D2
SP9		MS MS#	
SP10	SD DAT6	MS D3	XD D7
SP11	SD CLK	MS SCLK	XD D1
SP12	SD DAT5		XD D0
SP13	SD DAT4		XD WP#
SP14			XD RB#
SP15	SD DAT3		XD WE#
SP16	SD DAT2		XD RE#
SP17			XD ALE
SP18			XD CE#
SP19			XD CLE

SP7	R528	0	4	MS-D0	SD-D0	SD-D6
SP6	R524	0	4	MS-D1	SD-D1	SD-D6
SP8	R532	0	4	SD-D2	SD-D2	
SP16	R527	0	4	XD-RE	SD-D2	
SP5	R533	0	4	MS-BS	XD-D5	
SP15	R578	0	4	SD-D3	XD-WE	
SP11	R569	0	4	SD	CLK	MS_CLK
SP2	R511	0	4	SD	WP	
SP13	R576	0	4	XD	WP#	
SP19	R586	0	4	XD	CLE	
SP4	R530	0	4	XD	D4	
SP10	R537	0	4	MS-D3	XD-D7	
SP14	R577	0	4	XD	RB#	
SP12	R579	0	4	XD	D0	
SP17	R580	0	4	XD	ALE	
SP18	R581	0	4	XD	CE#	
SD_CMD	R571	0	4	SD	CMD	

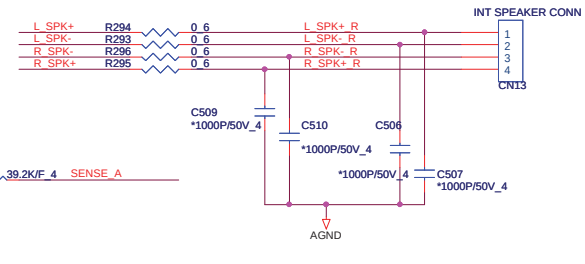


CPU FAN





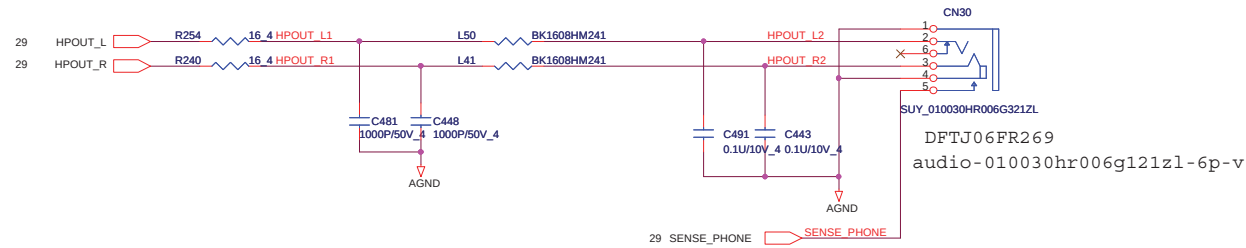
INT. SPEAKER



Note: JACK_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

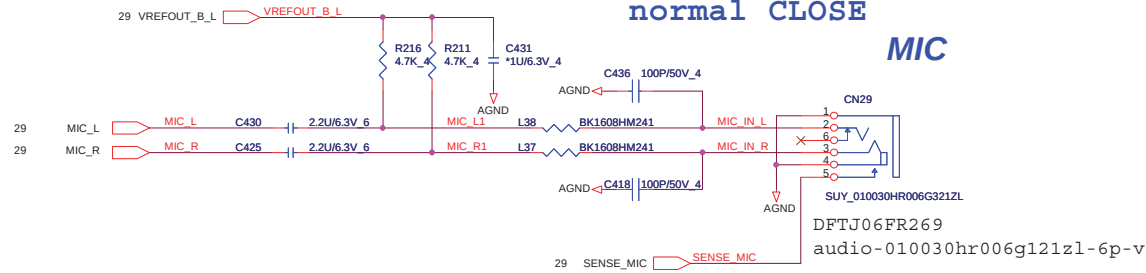
33,34,36,37,38,39,40,41,42,43 +5VPCU
2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,27,28,29,31,32,33,34,35,36,42 +3V

normal CLOSE Line out



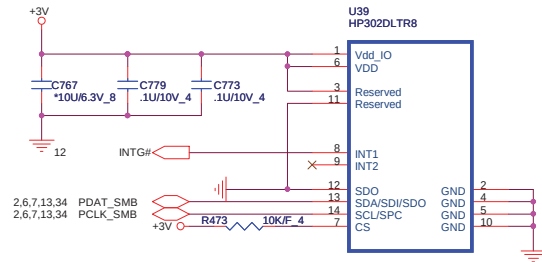
Note: JACK_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

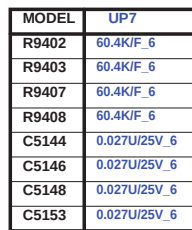
normal CLOSE MIC



Accelerometer Sensor

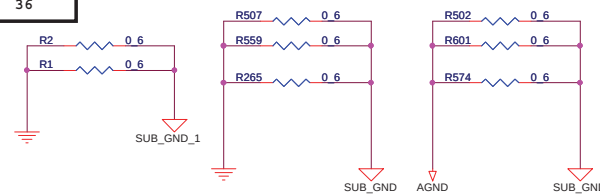
SGT-LIS302DLTR interrupt pin default is low / active Hi, BIOS need to programming 22h to change status from active Hi to low



[illegible]

GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

Sub-Woofer power

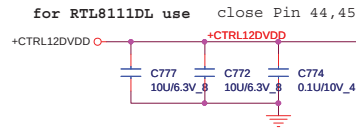


+3V	2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,27,28,29,30,32,33,34,35,36,42
+5V_AVDD	29
+VIN	24,37,38,39,40,41,42,43

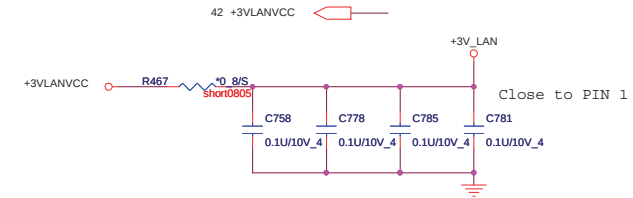


Size Custom	Document Number SUBWOOFER (EQ & AMP.)	Rev 1A
Date: Monday, September 28, 2009	Sheet 31 of 46	

T : Stuffed for RTL8111DL(10/100/1000)

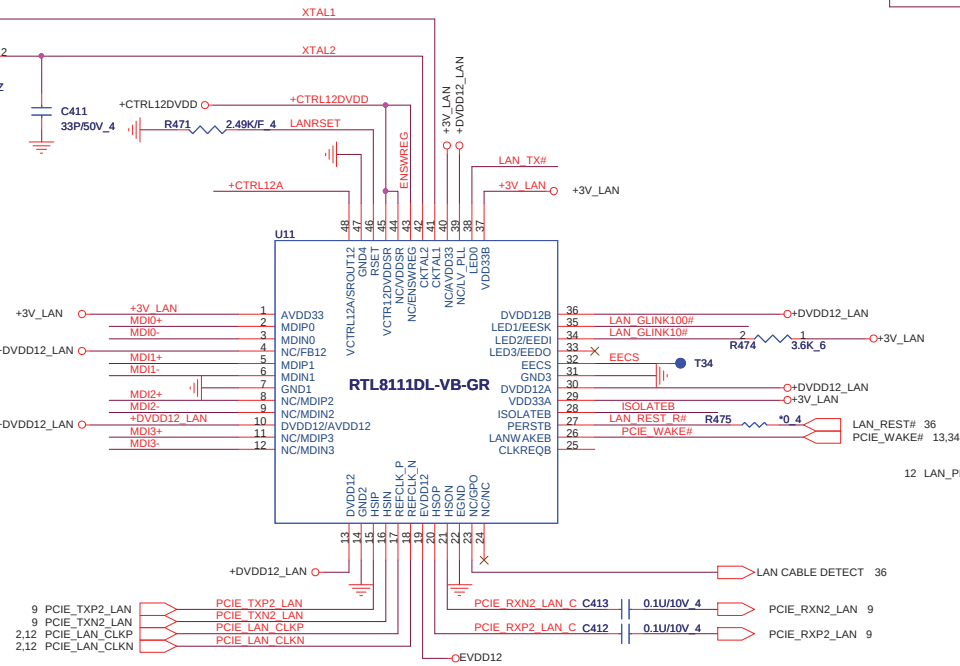
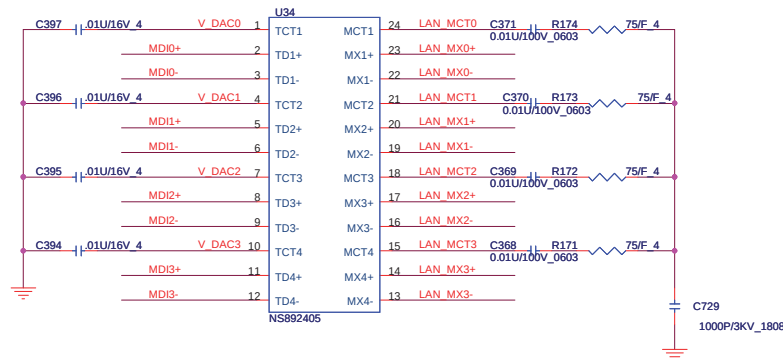
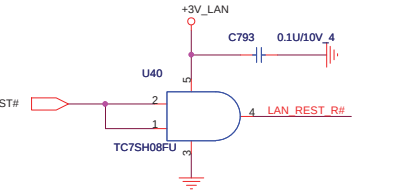
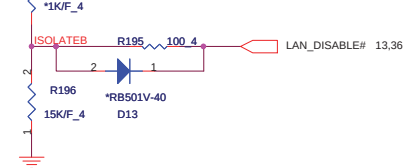


for RTL8111DL use



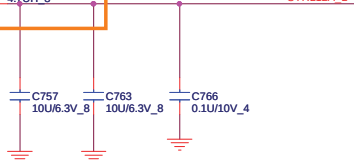
Close to PIN 1

if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

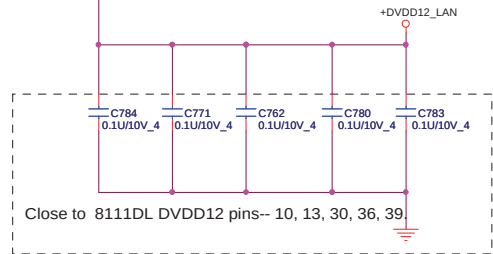
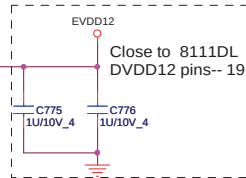


NS892402:GIGABIT DB0AT9LAN05

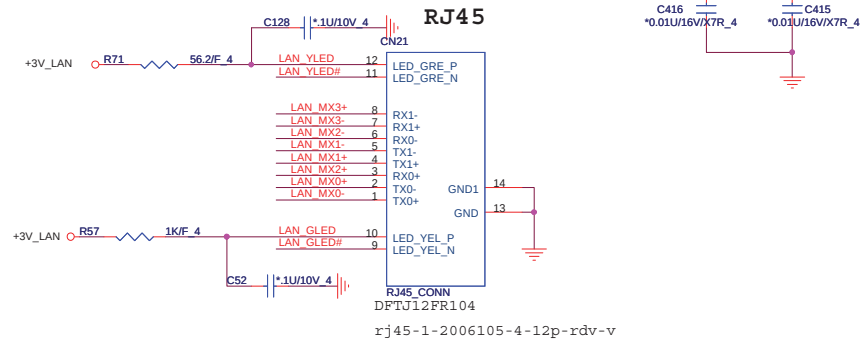
>60mil L72 4.7uH_8 Power trace Layout 寬度 >60mil



L149
RTL8111DL (Giga lan) use 4.7uH
power choke A>600mA tolerance
±15%



LAN_GLINK100# LAN_GLED#
LAN_TX# LAN_YLED#



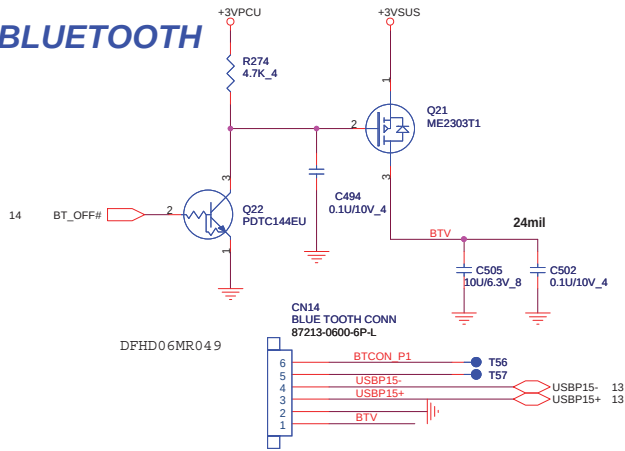
rj45-1-2006105-4-12p-rdv-v



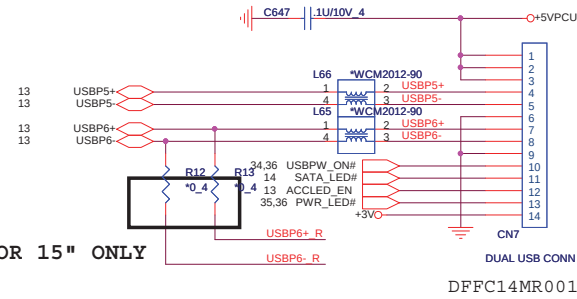
PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8111DL/RJ45	1A
Date: Monday, September 28, 2009	Sheet 32 of 46	

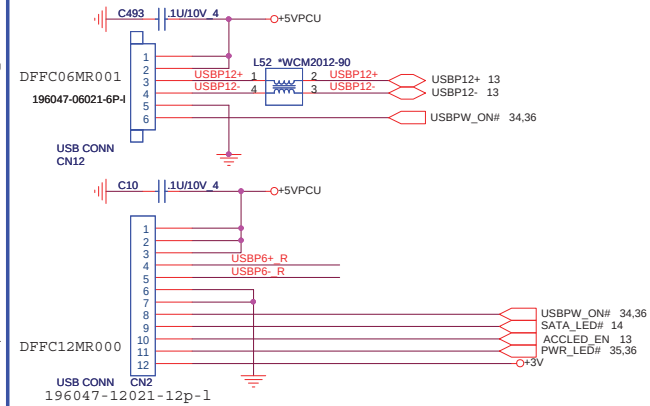
BLUETOOTH



RIGHT SIDE USBX2 for 17"

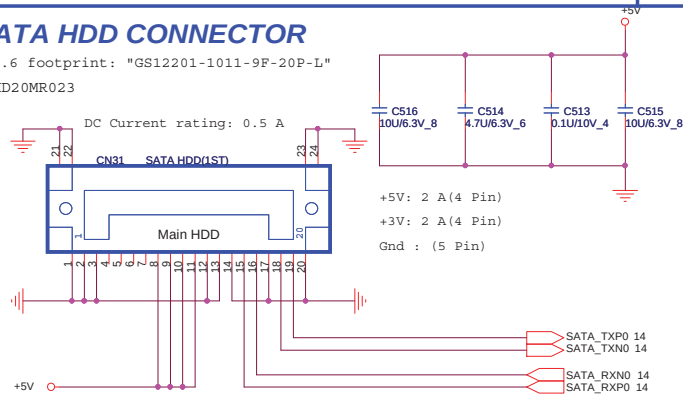


RIGHT SIDE USBX2 for 15"



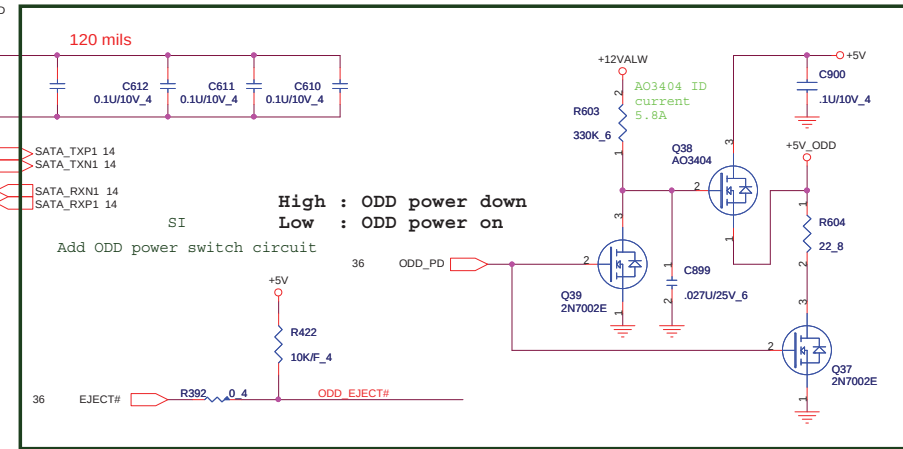
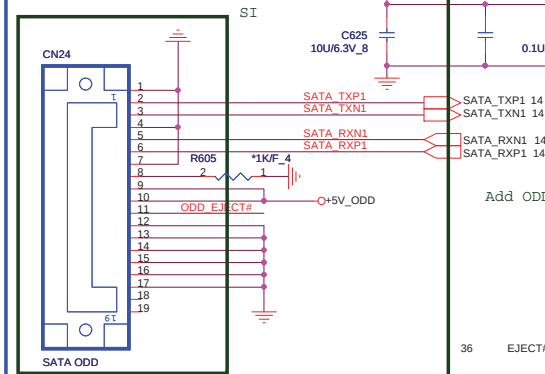
SATA HDD CONNECTOR

H=2.6 footprint: "GS12201-1011-9F-20P-L"
DFHD20MR023



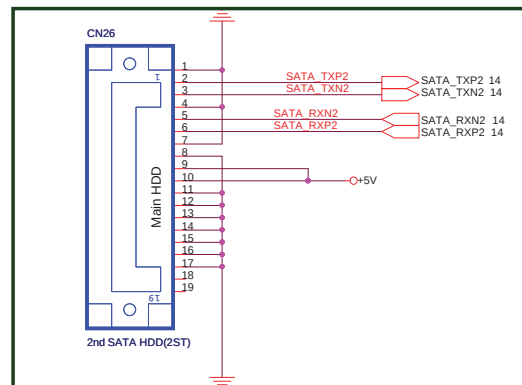
SATA CD-ROM

Change to ANT connector



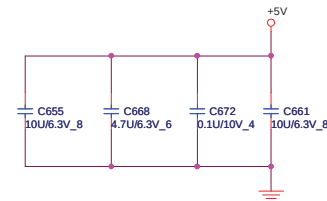
SATA_2 HDD CONNECTOR FOR 17.3"

```
+5V: 2 A(4 Pin)
Gnd : (5 Pin)
```



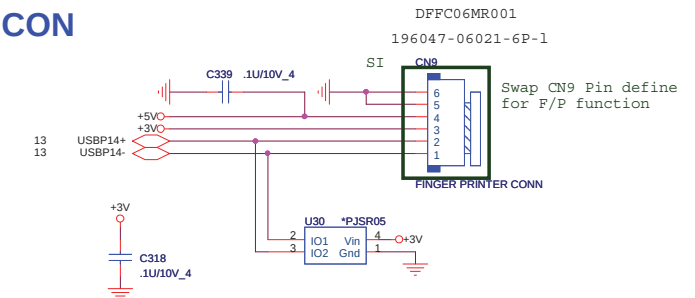
SI

Change to ANT connector



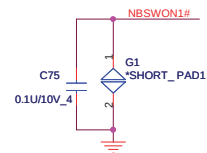
USB Fingerprint CON

1. SYSTEM GND
2. SYSTEM GND
- 3.LED PWR(+5V)
- 4.USB PWR(+3V)
5. USB1.1+
6. USB1.1-

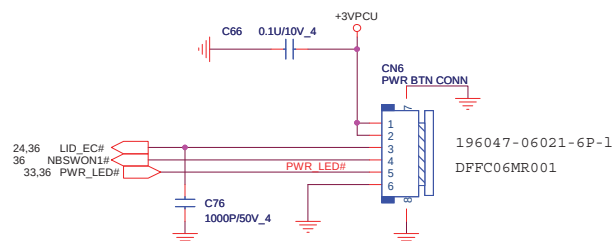


 NBS/RD2	PROJECT : LX89 Quanta Computer Inc.		
	Size Custom	Document Number BT/FP/USBX2/SATA HDDX2/ODD	Rev 1A
Date: Monday, September 28, 2009		Sheet 33 of 46	

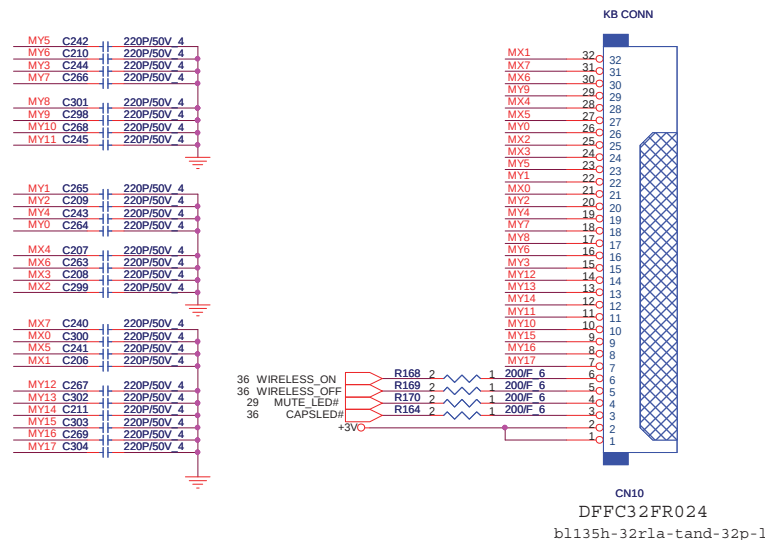
POWER BUTTON CONNECT



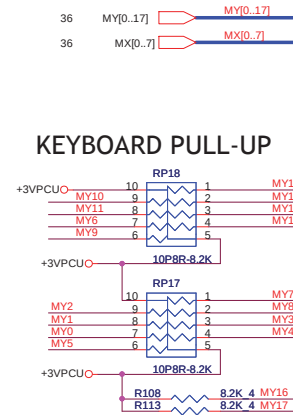
1. +3VPCU(LIDSWITCH PWR)
- 2.(+3VPCU)
3. LIDSWITCH
- 4.POWERON#
5. PWRLED#
6. GND



KEYBOARD Con.

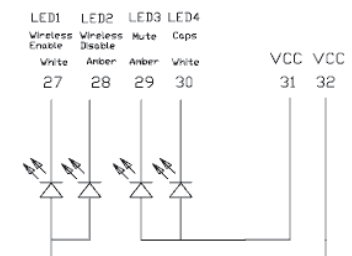
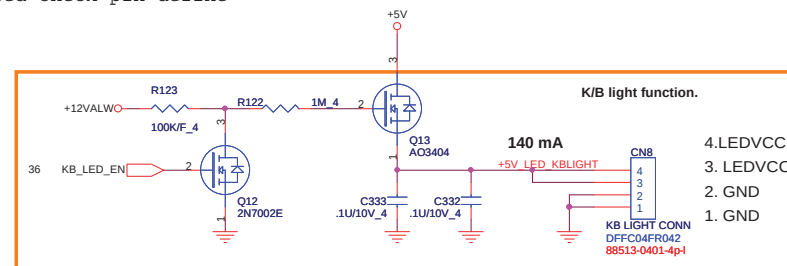
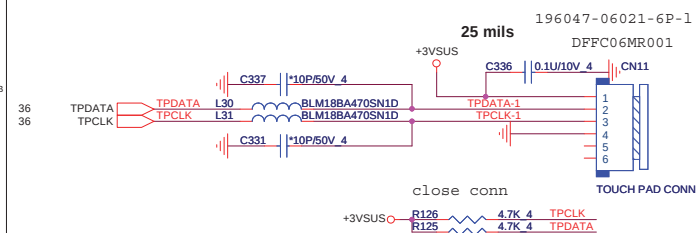


Need check pin define

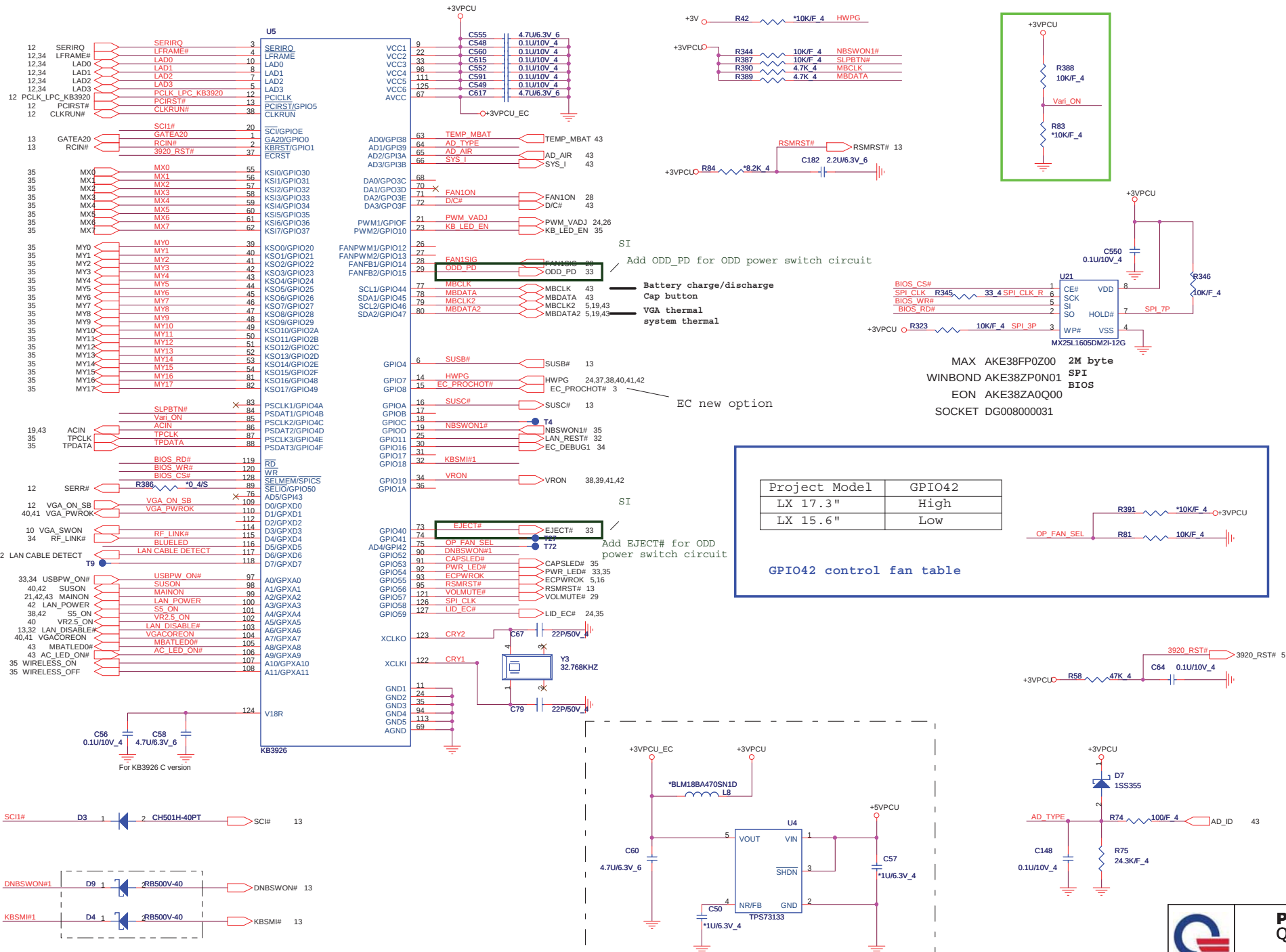


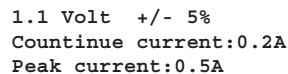
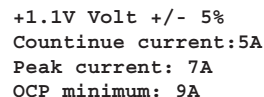
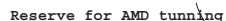
KEYBOARD PULL-UP

TOUCH PAD CONN



12		30	112		50	119	56		51		13	123		62	126	76	91	94
1		110	115	127	35	118	125		36		41	122	107		15	75	92	95
8	58	16	114		21	117	28		22		27	121			90	80	93	96
9		1	113	70	6	116	45	59	7		12	120	129	29 42	85	101	97	
5	64	31	33	71	34	32	38		37		40	39			43	86	106	104
6		46	48	72	49	47	53		52	44	55	54			61	81	100	103
3		2	4	73	5	3	9		8		11	10		60	84	89	99	102
2		17	19	74	20	18	24		23	57	26	25			83	79	105	108
	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	25	26

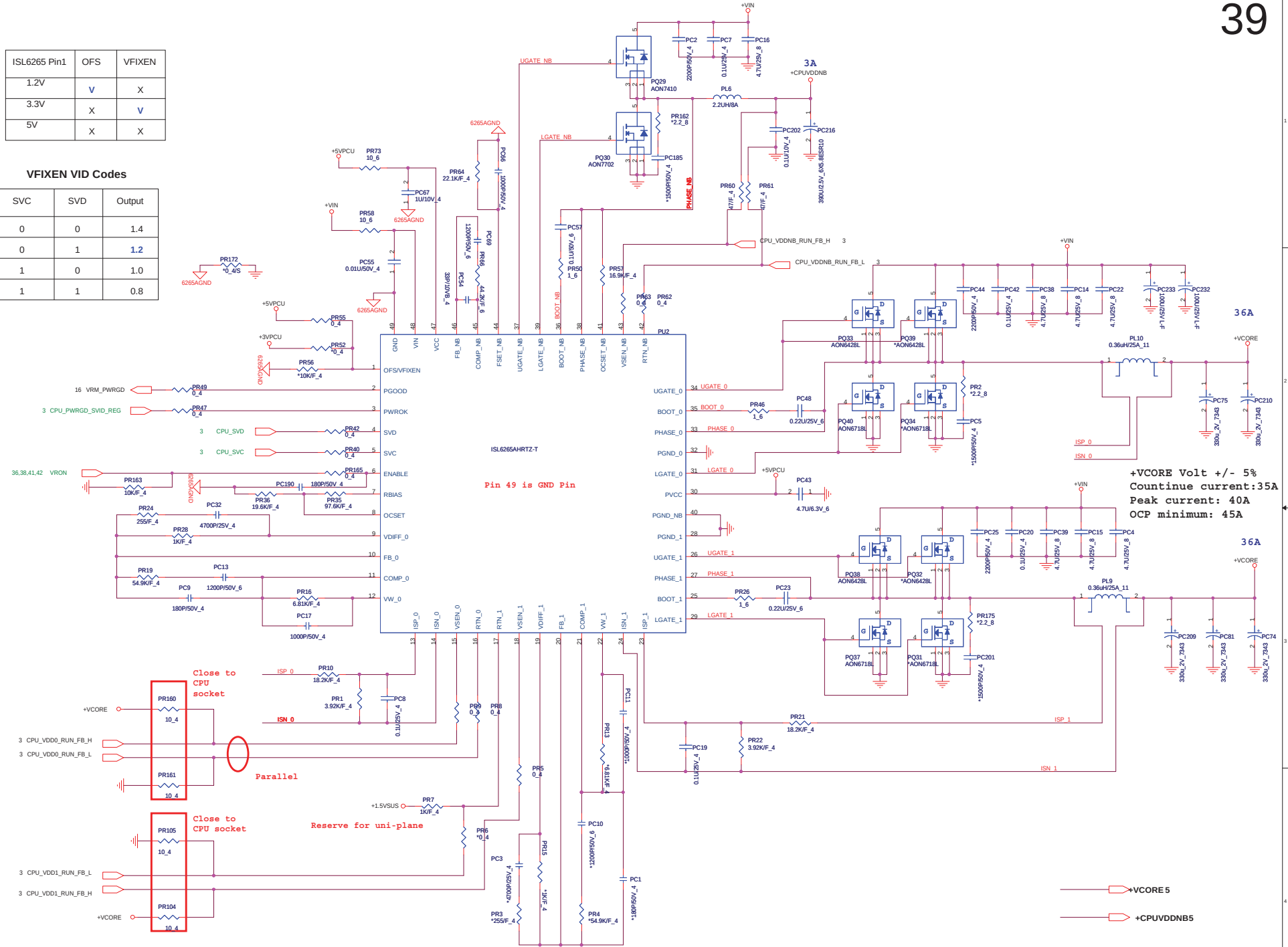




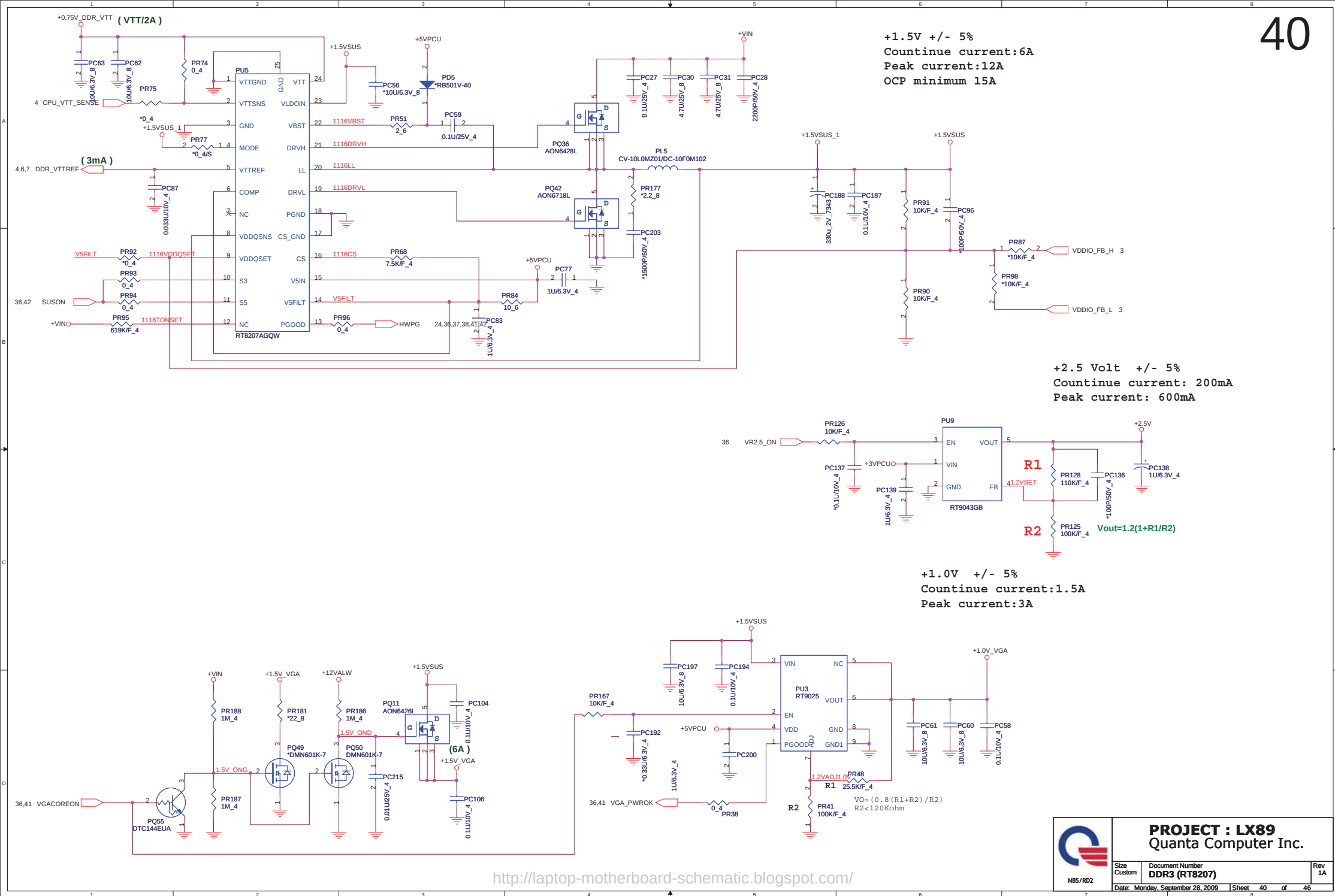
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

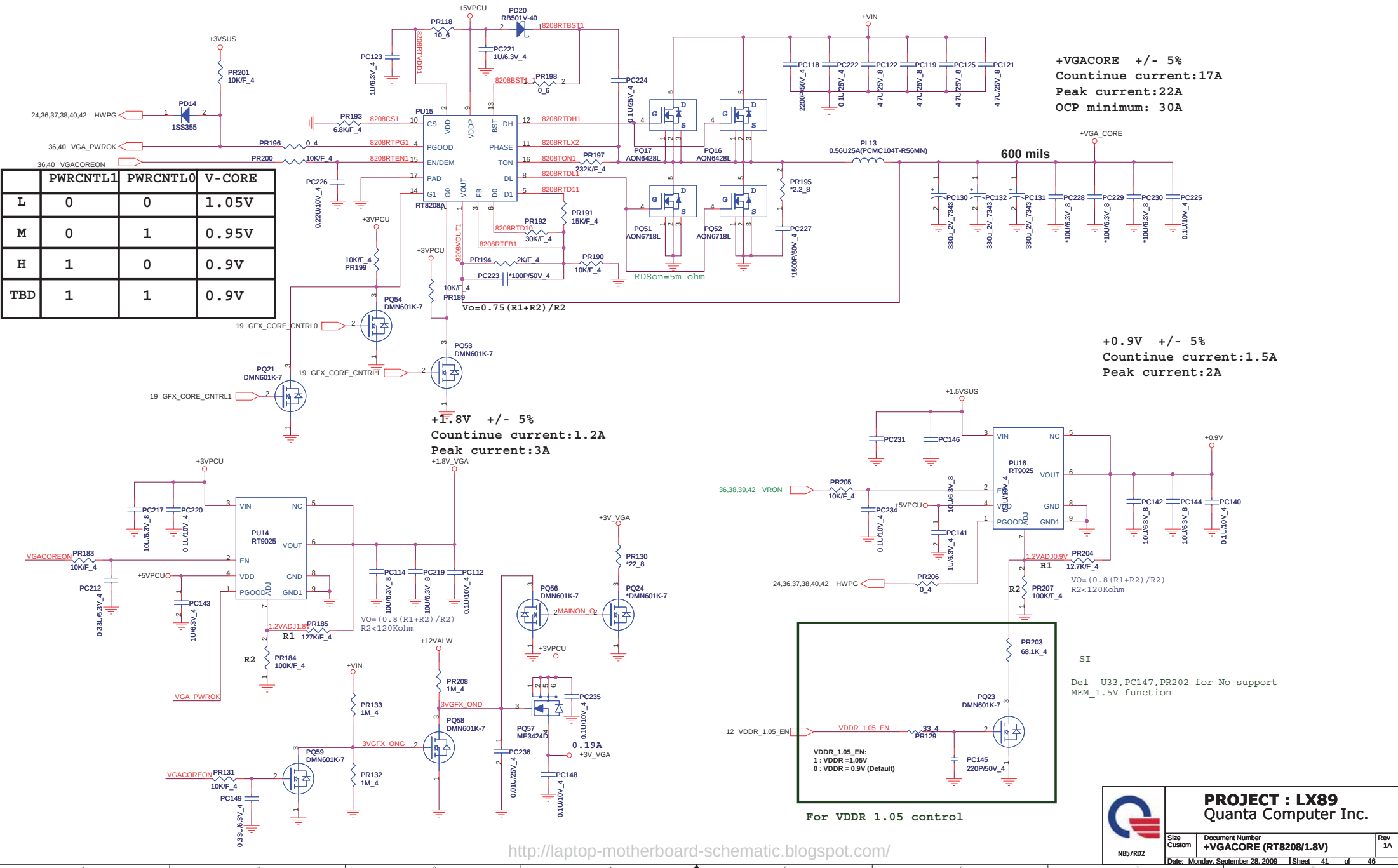
VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



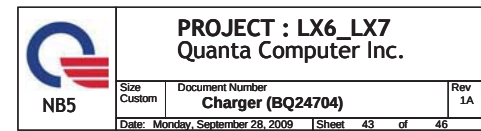
<http://laptop-motherboard-schematic.blogspot.com/>

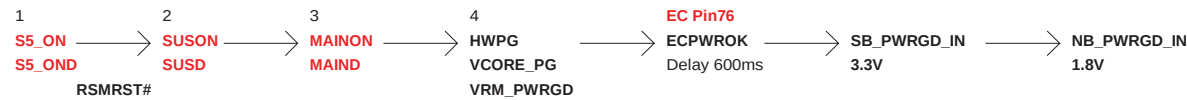
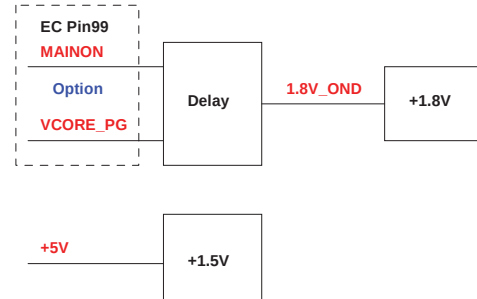
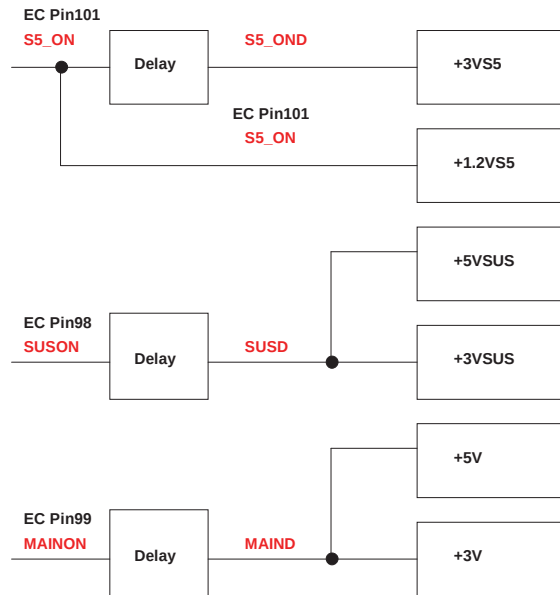
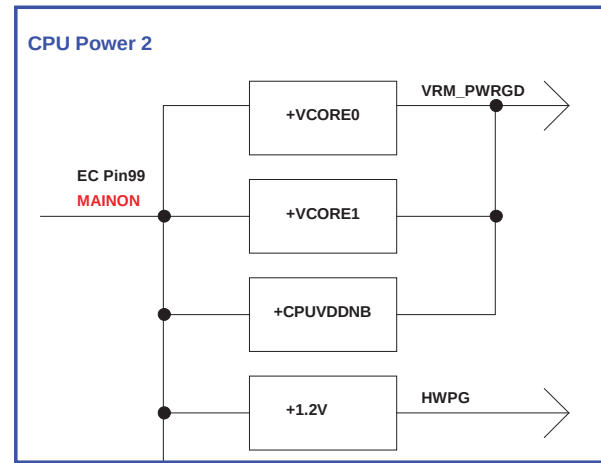
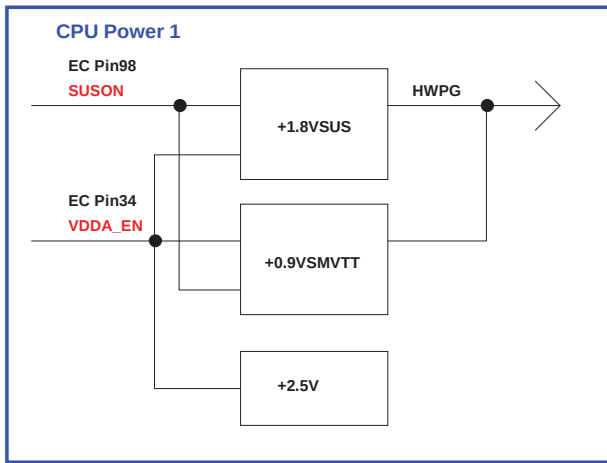




	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	1.05V
M	0	1	0.95V
H	1	0	0.9V
TBD	1	1	0.9V

20346-100n-1-10p-ldv





Power & Ground

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VLANVCC	S0		LAN_POWER
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+5V	S0		MAINON
+5V_VCC1			
+5VALW			
+10VALW			
+15VALW			
+1.8V	S0		+1.5_ON
+1.8VSUS	S0, S3		
+1.5V	S0		MAINON
+1.5VSUS	S0, S3	DDR CORE POWER	SUSON
+1.5VSUS_1			
+1.5V_VGA	S0	VGA , VRAM POWER	+1.5_ON
+1.2V	S0		VRON
+1.2VSUS	S0, S3		SUSON
+1.1V	S0	VDDPCIE - PCIE-E MAIN POWER	VRON
+1.1VS5	S0, S3, S4, S5	STANDBY POWER	S5_ON
+1.1V_DYN	S0	NB VDDC - CORE LOGIC POWER	DYN_PWR_EN
+1.05V	S0	HT POWER (1.05V)	VRON
+1.0V_VGA	S0	PARK DPX_VDD10 POWER	VRON
+2.5V	S0	CPU VDDA POWER	VR2.5_ON
+VCORE0	S0	CPU CORE POWER (?V)	VRON
+VCORE1	S0	CPU CORE POWER (?V)	VRON
+CPUVDDNB	S0	CPU VDDNB POWER	VRON
+0.75_DDR_VTT	S0	DDR COMMAND & CONTROL PULL UP POWER	SUSON
DDR_VTTREF	S0, S3	DDR REFERENCE POWER	SUSON
+VGA_CORE	S0	VGA CORE POWER	MAINON
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3_3V)	

SMBUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR3		
CPU THERMAL SENSOR		
CHARGER		

PCB STACK UP

LAYER 1 : TOP
LAYER 2 :GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT



PROJECT : LX89
Quanta Computer Inc.

Size	Document Number	Rev 1A
Date: Monday, September 28, 2009 Sheet 45 of 46		