

Wistron Confidential

MV

2008/05/15

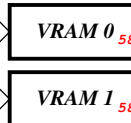
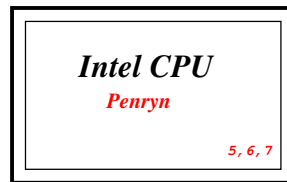
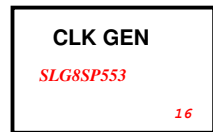
REV : -1

<Variant Name>

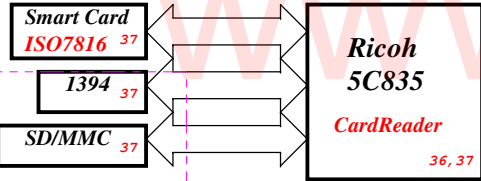
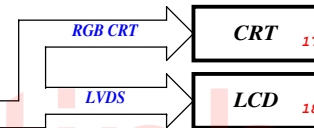
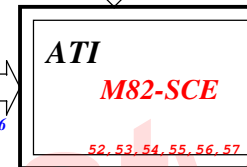
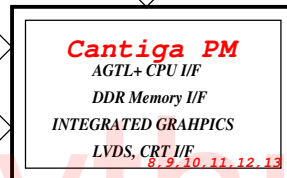
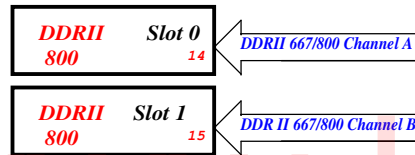
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Karia			
Size A3	Document Number		Rev SH
KARIA - DISCRETE			
Date: Friday, May 16, 2008	Sheet	1	of 58

KARIA DESCRETE BLOCK DIAGRAM

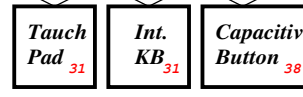
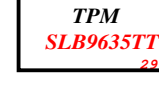
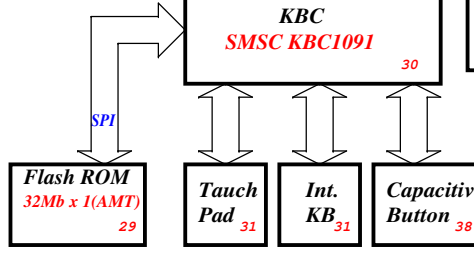
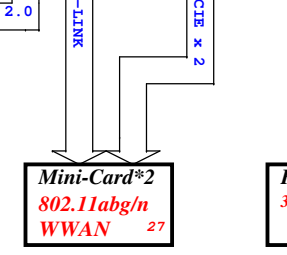
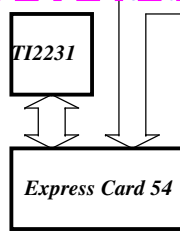
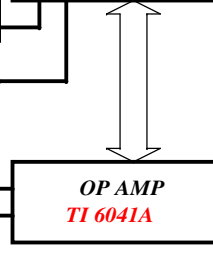
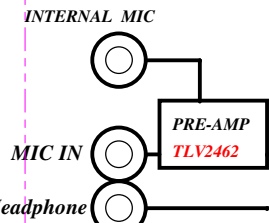
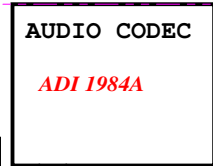
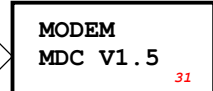
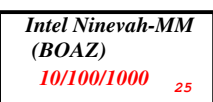
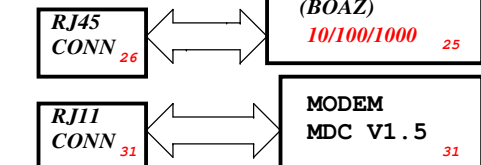
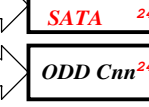
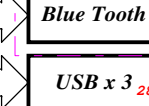
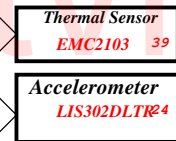
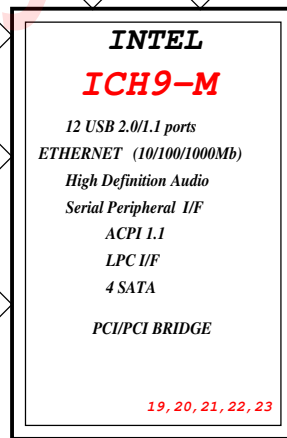
Project code :
91.4V901.001
PCB P/N :
Revision : MV



HOST BUS FSB
667/800/1067MHz



DMI x4 Controller link 0



SYSTEM DC/DC SC471AML	
INPUTS	OUTPUTS
B+	VGA_CORE 45

SYSTEM DC/DC TPS5116	
INPUTS	OUTPUTS
B+	+1.8V 7A 47 +0.9V 1A

SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
B+	+5VALW 7A +3VALW 6A 46

SYSTEM DC/DC SC412A	
INPUTS	OUTPUTS
B+	+1.5VS 3A 50 +1.05VM 13A 48

CHARGER BQ27470	
INPUTS	OUTPUTS
BATT_A BATT_B	BATT 18V 3.0A 5V 100mA 51

CPU DC/DC ISL6260A	
INPUTS	OUTPUTS
B+	+VCC_CORE 0.844~1.3V 44A 43

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	GND
L6:	VCC
L7:	Signal 4
L8:	Signal 5
L9:	GND
L10:	Signal 6

- Discrete PV
- 03/11/08:
- Page 51 - Change R118 to 287K ohm from Vox information.
 - Page 43 - Change R582.2 to +3VALW from +3VS to power U89.39 (3V3)
 - Page 45 - Change R232 to NO INSTALL
 - Page 30 - Remove D48, connect signal directly to ADP_PRES, and uninstall R558
 - Page 27 - Reserve a 1u 0603 cap (NO INSTALL) on MC2_DISALBE (same as MC1_DISABLE)
 - Page 19 - Add a 0 ohm series on PLT_RST# at U113.4
 - Page 33 - Add a 0 ohm series on PM_PWROK_R at R175.2
 - Page 13 - Uninstall BGA_CRACK circuit: U115, U116, R740, R744, R801, & R802
 - Page 23 - Uninstall BGA_CRACK circuit: U117, U118, R803, R804, R805, & R806
 - Page 39 - Change R710 (SHDN_SEL) to 15K 1% to use Internal Diode for H/W critical shutdown
 - Page 57 - Add a discharging FET (gate connect to Q15.D) on 3.3V_DELAY at Q42.D
 - Page 25 - May require a discharging FET for +3VM_LAN at Q39.D
 - Page 32 - May need to change RGB q-switches power to +5VALW or +5VS (depending on wavy impact)
 - Page 51 - Change R97 to 33K from 1.27K
 - Page 41 - Change DAUGTH1 pin 52 and pin 54 to +5VS from +5VALW
 - Page 41 - Remove ICH_SMB_CLK/DATA from DAUGTH1 pin 32 and 34

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Voltage Rails

o MEANS ON x MEANS OFF

power plane State	+BB LDO3 LDO5	+3VALW +5VALW	+1.8V +5V +0.9V	+5VS +3VS +1.8VS +1.5VS +VGA_CORE +CPU_CORE +VCCP	+3VM +1.05VM	CLOCK
S0	O	O	O	O	O	O
S3/M1	O	O	O	X	O	O
S3	O	O	O	X	O	O
S5 S4/AC	O	O	X	X	O	O
S5 S4/Battery only	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
Cardreader&1394	AD25	2	G,E

PCIE Devices

DEVICE	NUMBER	CHANNEL
UWB(no support)	1	1
WLAN	1	2
EXPRESS CARD	1	3
WWLAN	1	4
DOCKING	1	5
GIGA LAN	1	6

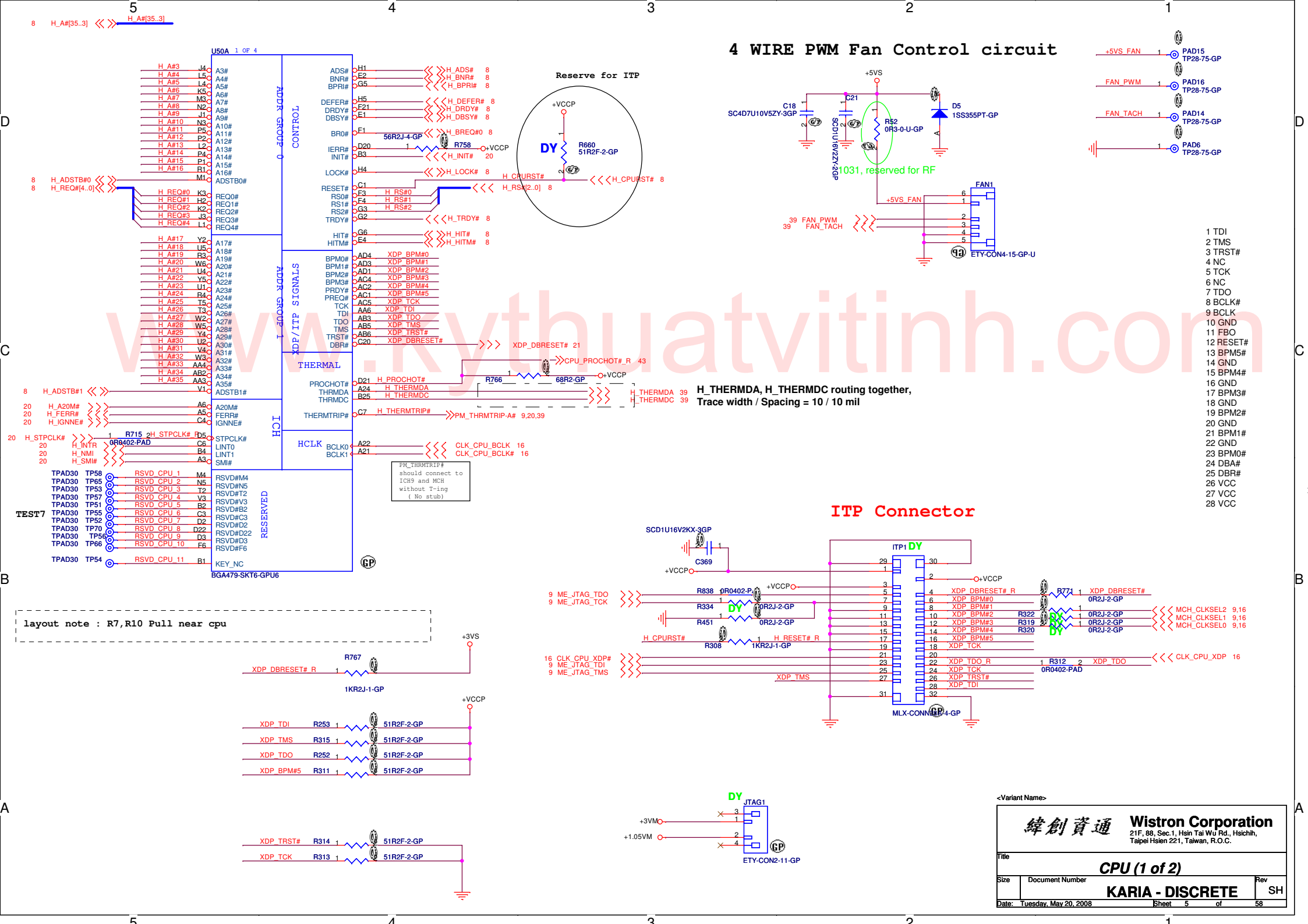
USB PORT	Device
0	USB1
1	Free
2	EX-P
3	WLAN
4	USB2
5	USB3
6	BLUETOOTH
7	WWAN
8	FignerPrint
9	Dock1
10	WEBCAM
11	DOCK2

Symbols	Description
DY/DUMMY	No install
1KR2J	Resistor 1K ohm ,Size 0402 ,5%
1KR3F	Resistor 1K ohm ,Size 0603 ,1%
GP	ROHS parts
NC	Pin no connect to anything
1U16V2ZY-2GP	Caps 1U ,Size 0402 Y5V
2D2U6D3V3MX	Caps 2.2U ,Size 0603 X5R

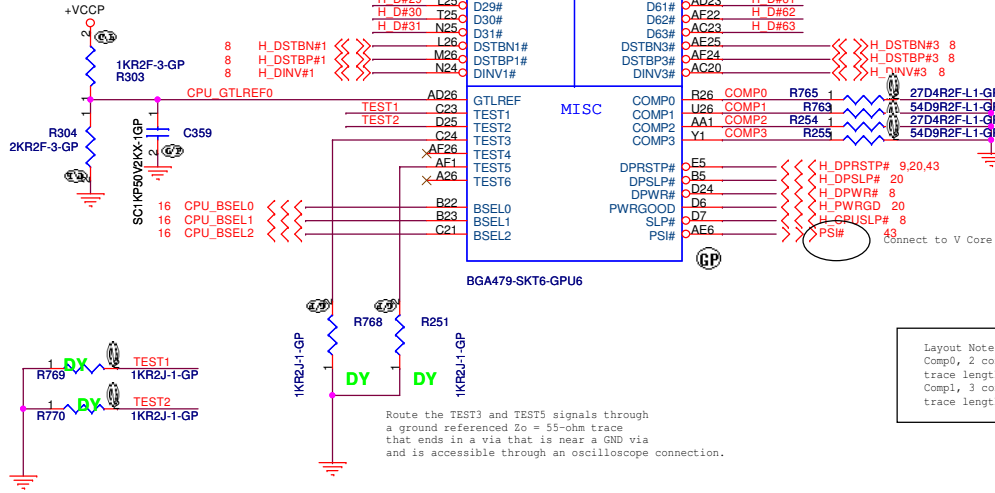
IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2) ,LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	Floppy
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Modem,LAN
11	Mass storage control/PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface ,HDD
15	Secondary IDE interface ,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Drive for High Definition Audio Intel 82801H (ICH9 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH9 Family) PCI Express Root Port -27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH9 Family) USB Universal Host Control
18	Intel 82801H (ICH9 Family) USB Universal Host Control Richo R5C835 Integrates FlashMedia Control Richo R5C835 Gemcore based SmartCard Control
19	Intel 82801H (ICH9 Family) PCI Express Root Port -27D6 Intel 82801H (ICH9 Family) USB Universal Host Control
20	Intel 82801H (ICH9 Family) USB Universal Host Control Intel 82801H (ICH9 Family) USB2 Enhanced Host Control
21	Intel 82801H (ICH9 Family) USB Universal Host Control
22	SDA Standard Compliant SD Host Control
23	HP Mobile Data Protection Sensor

<Variant Name>

Title		Wistron Corporation	
Size		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
A3		Karia List	
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Rev		SH	



Layout notes
Z= 55 Ohm 0.5" MAX for GTLREF

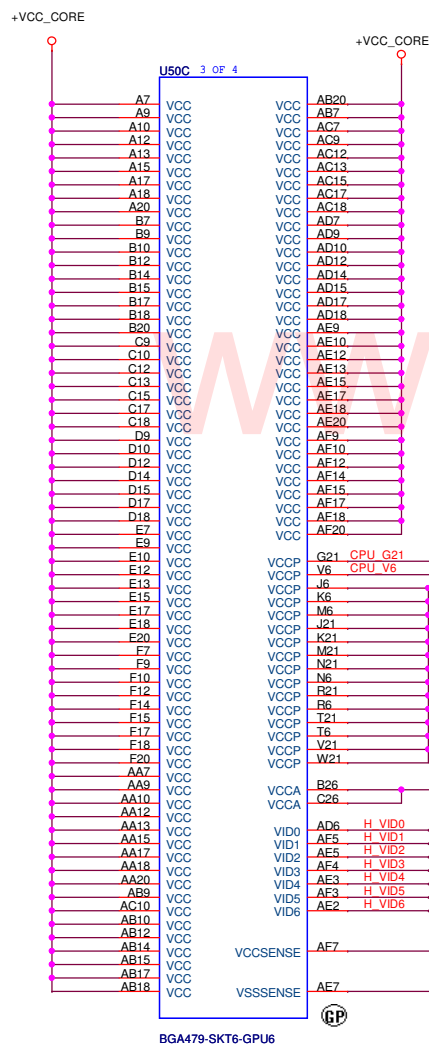


Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make
trace length shorter than 0.5" .
Comp1, 3 connect with Zo=55 ohm, make
trace length shorter than 0.5" .

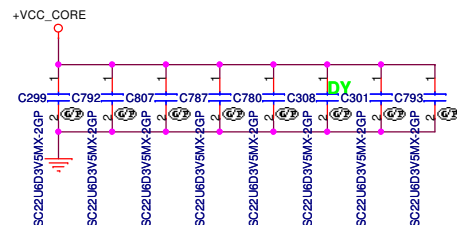
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
CPU (3 of 2)			
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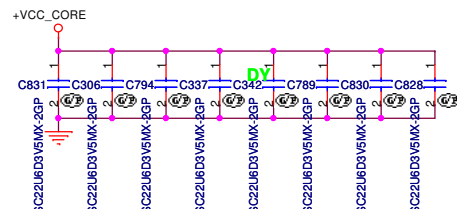
Please these inside socket
cavity on L8(North side Secondary)



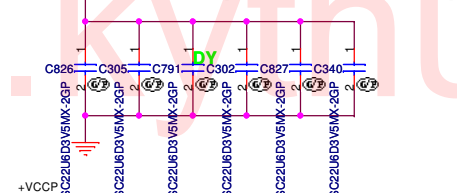
BGA479-SKT6-GPU6



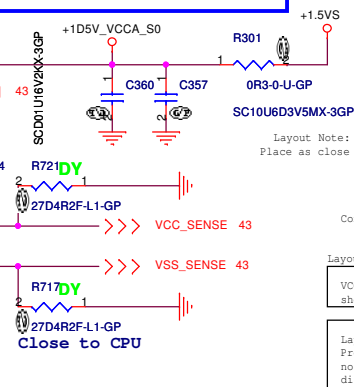
Please these inside socket cavity on L8(South side Secondary)



+VCC_CORE Please these inside socket cavity on L8(North side Primary)



layout note: "1D5V_VCCA_S0"
as short as possible



Layout Note:
Place as close as possible to the CPU VCCA pin.

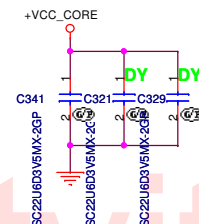
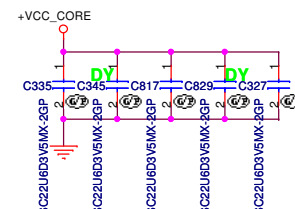
Layout Note:

VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

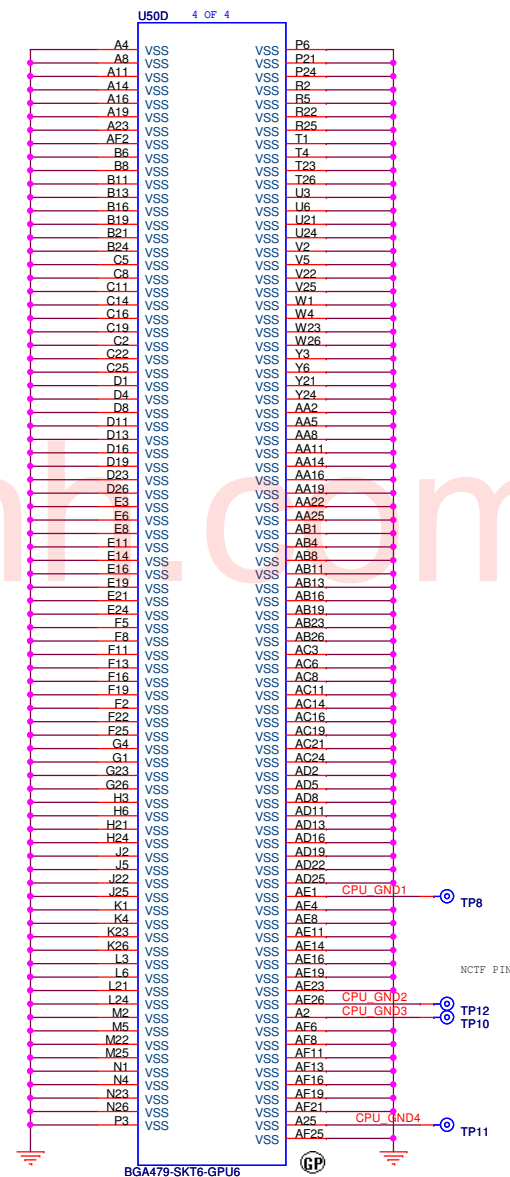
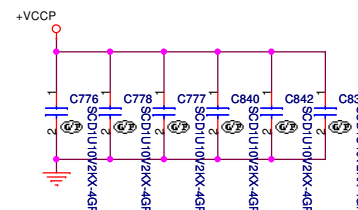
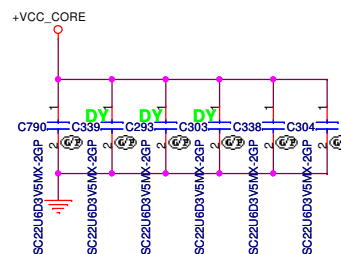
Please these inside socket
cavity on L8(North side Secondary)

Please these outside socket
cavity on L8(North side Secondary)



Please these outside socket cavity on L8(South side Secondary)

Please these inside socket
cavity on L8(South side Primary)



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CPU (3 of 3)

KARIA - DISCRETE

Title

Size	Document Number
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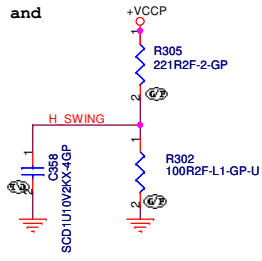
Date: Friday, May 16, 2008

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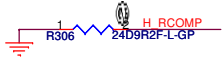
Rev	SH
-----	----

H_SWING routing Trace width and Spacing use 10 / 20 mil

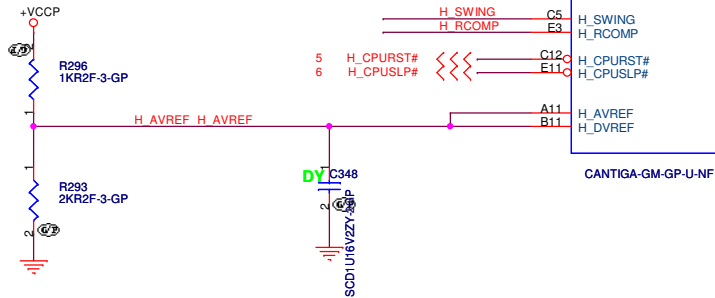
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



CANTIGA-GM-GP-U-NF

HOST

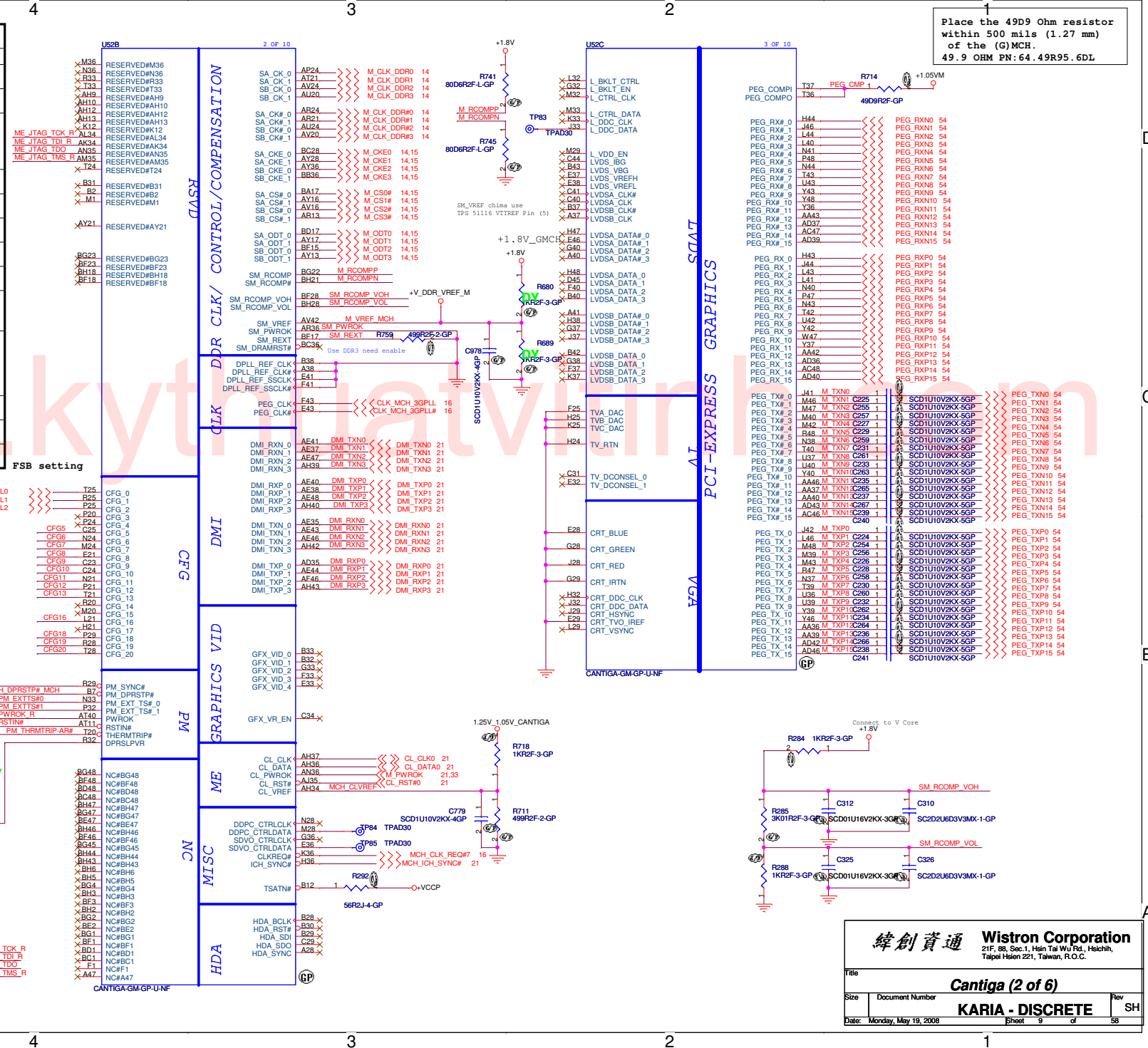
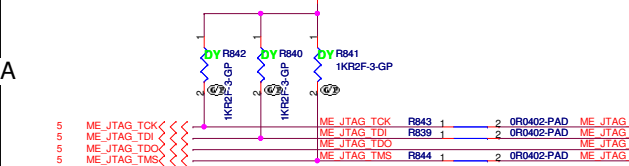
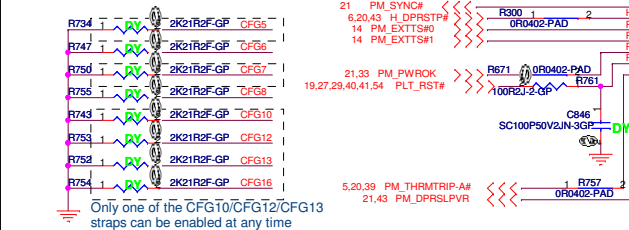
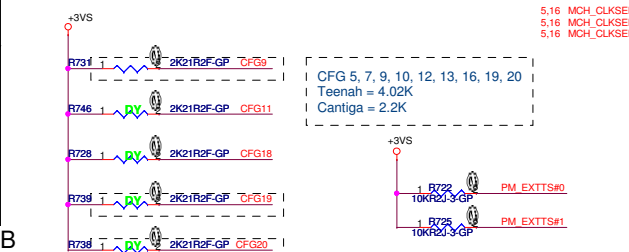
<Variant Name>

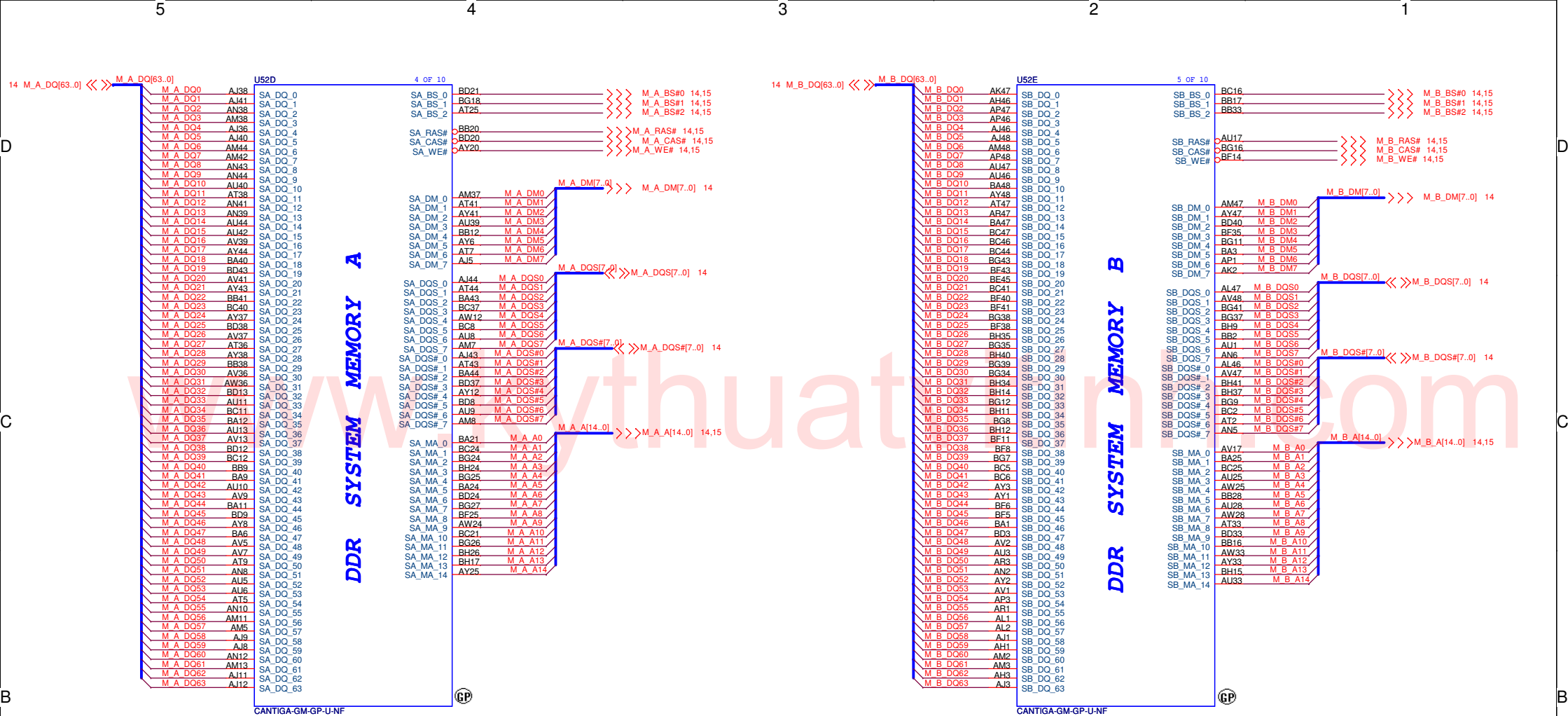
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

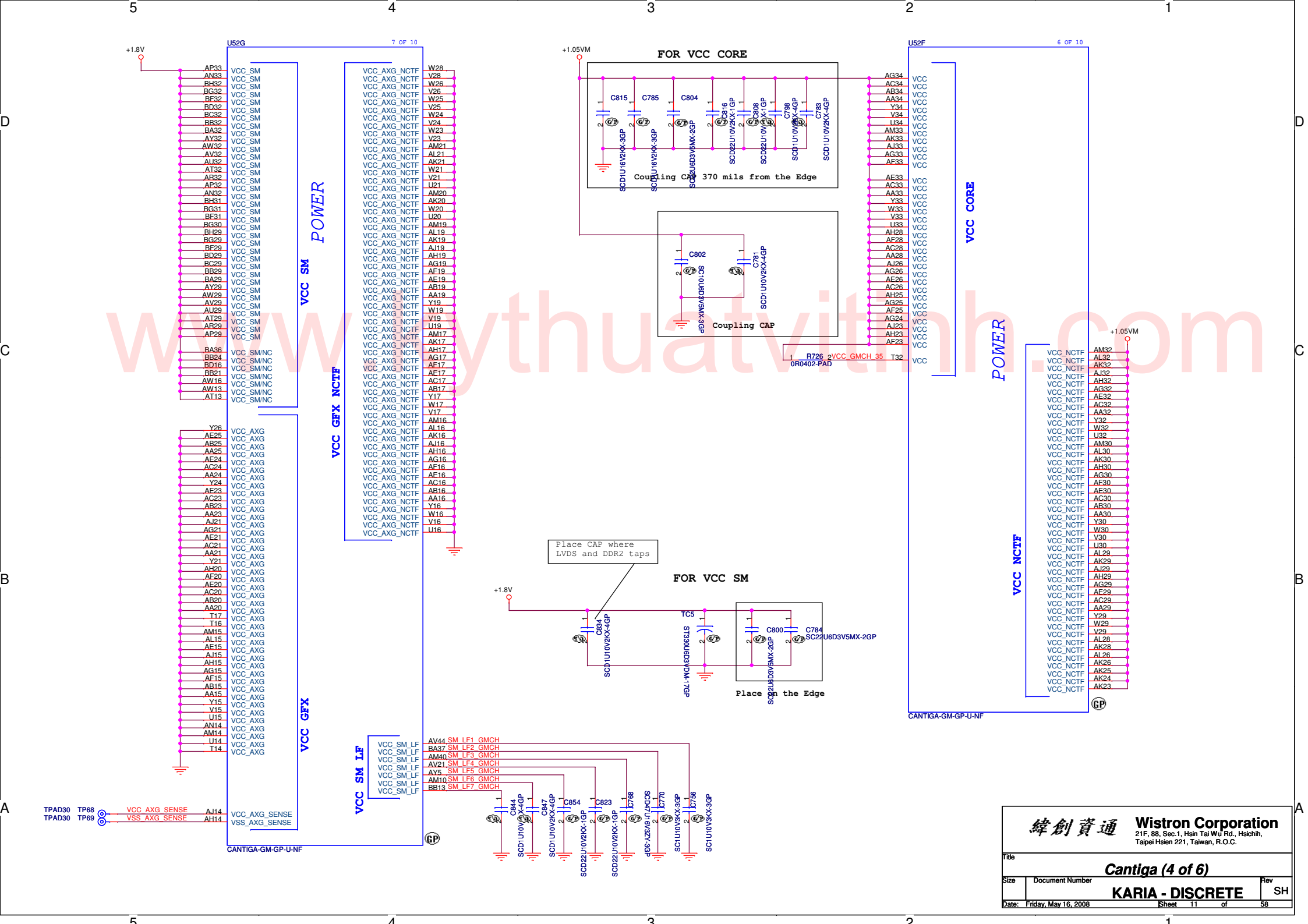
Title
Cantiga (1 of 6)
Size Document Number
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Rev SH

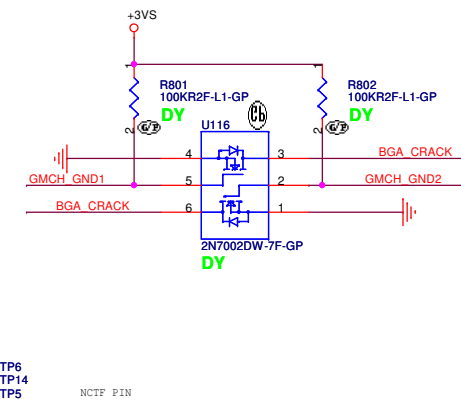
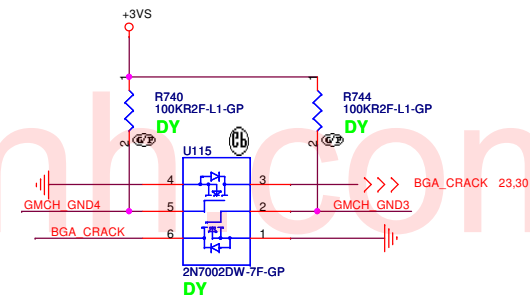
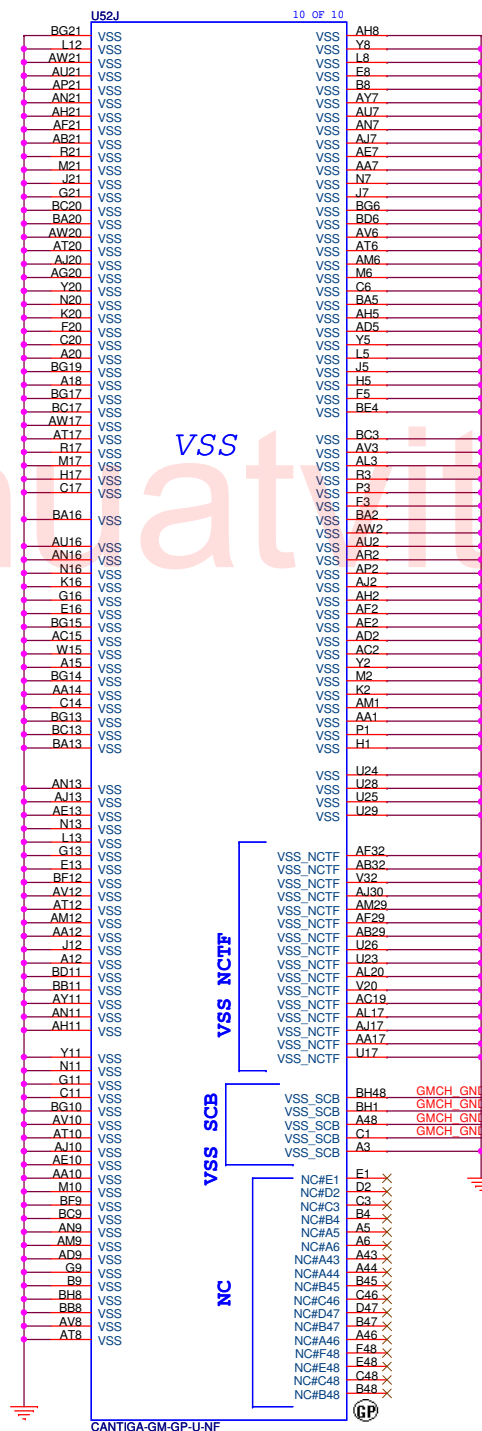
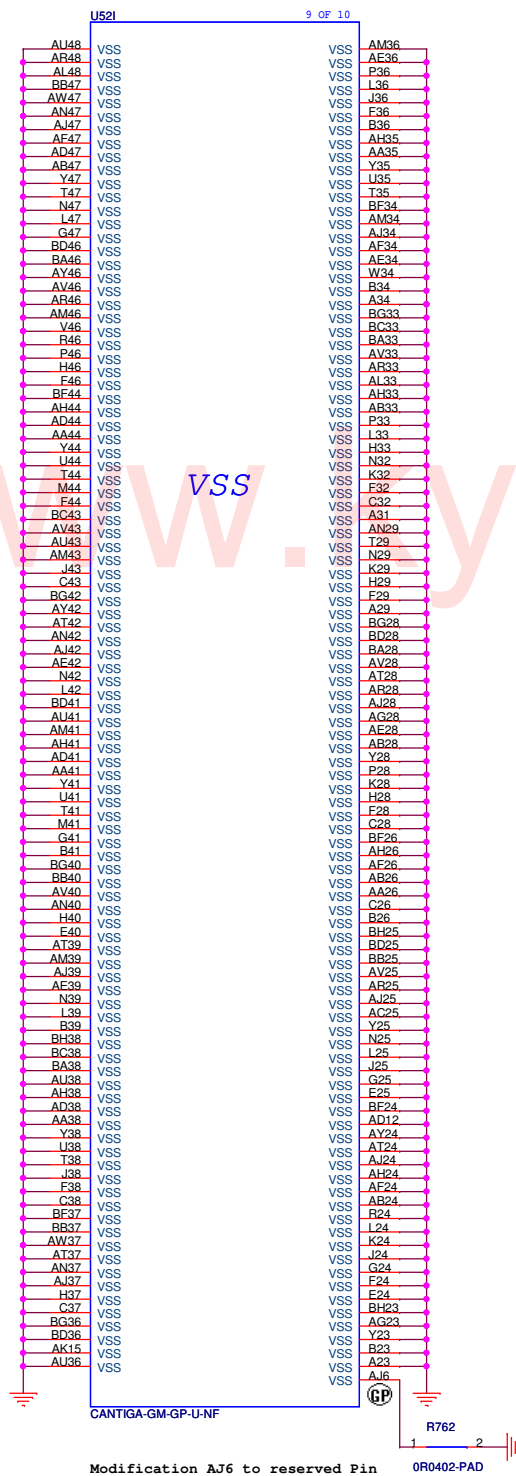
Strap Pin Table 5

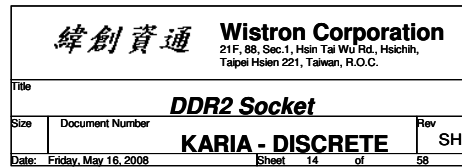
CFG[2:0] FSB Freq select	000 = FSB 1067MHz 010 = FSB 800MHz	011 = FSB 667MHz Others = Reserved
CFG4:3; 8; 11; 14:15; 17; 18	Reserved	
CFG5 (DMI select)	Low = DMI x 2 High = DMI x 4	*
CFG6 (ITPM Host Interface)	High = The ITPM Host Interface is disabled Low = The ITPM Host Interface is enabled	*
CFG7 (Intel Management Engine Crypto Strap)	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS Cipher suite with confidentiality	*
CFG9 (PCIE Graphics Lane)	Low = Reverse Lanes, 15->0, 14->1 etc... High = Normal operation: Lane Numbered in Order	*
CFG10 (PCIE Loopback enable)	Low = Enabled High = Disabled	*
CFG12 (ALLZ)	Low = ALLZ mode Enabled High = Disabled	*
CFG13 (XOR)	Low = XOR mode Enabled High = Disabled	*
CFG16 (FSB Dynamic ODT)	Low = Dynamic ODT Enabled High = Dynamic ODT Disabled	*
CFG19 (DMI Lane Reversal)	Low = Normal operation: Lane Numbered in Order High = Reverse Lanes DMI x 4 mode[MCH->ICH]: (0->3, 2->1, 1->2 and 0->3) DMI x 2 mode[MCH->ICH]: (3->0, 2->1)	*
CFG20 (Digital Display Port (SDVO/DP /iHDMI) Concurrent with PCIE)	Low = Only Digital Display Port (SDVO/iHDMI) or PCIE is operational High = Digital Display Port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via the PEG port	*
SDVO_CTRLDATA (SDVO Present)	Low = No SDVO Card Present High = SDVO Card Present	*
L_DDC_DATA (Local Flat Panel (LFP) Present)	Low = LFP Disabled High = LFP Card Present; PCIE disabled	*
DDPC_CTRLDATA (Digital Display Present)	Low = DisplayPort Disabled High = DisplayPort Device Present	*



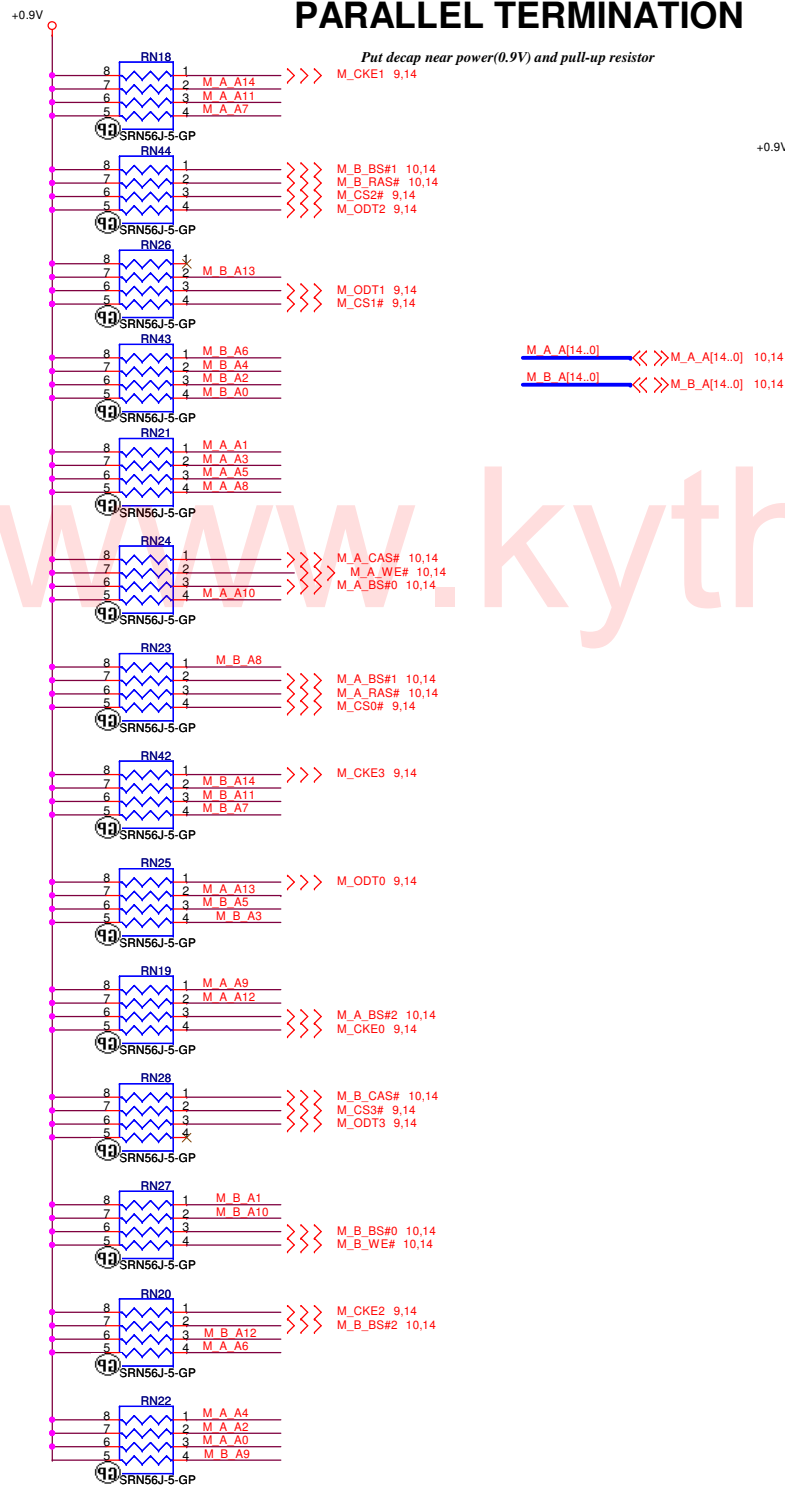




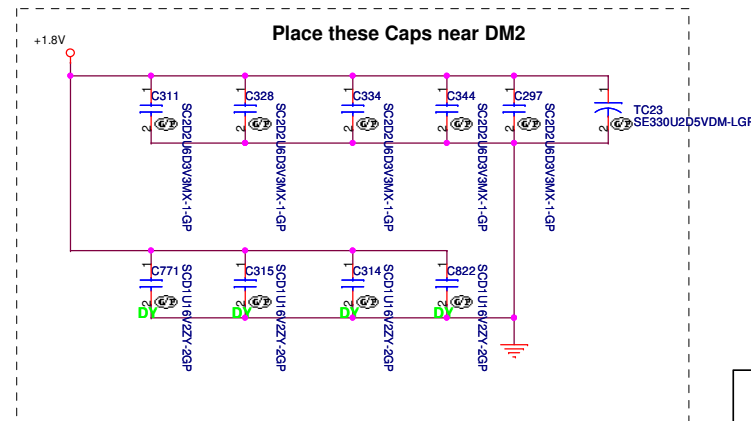
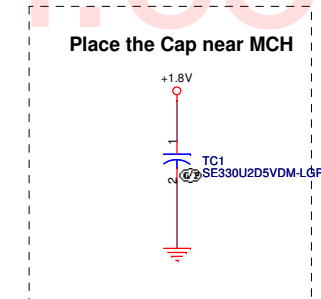
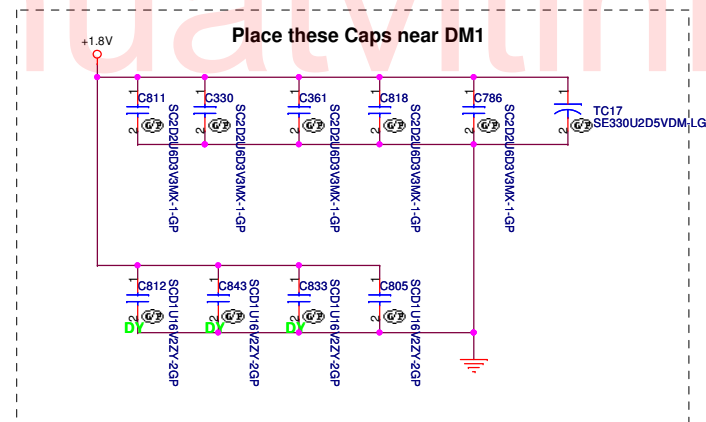
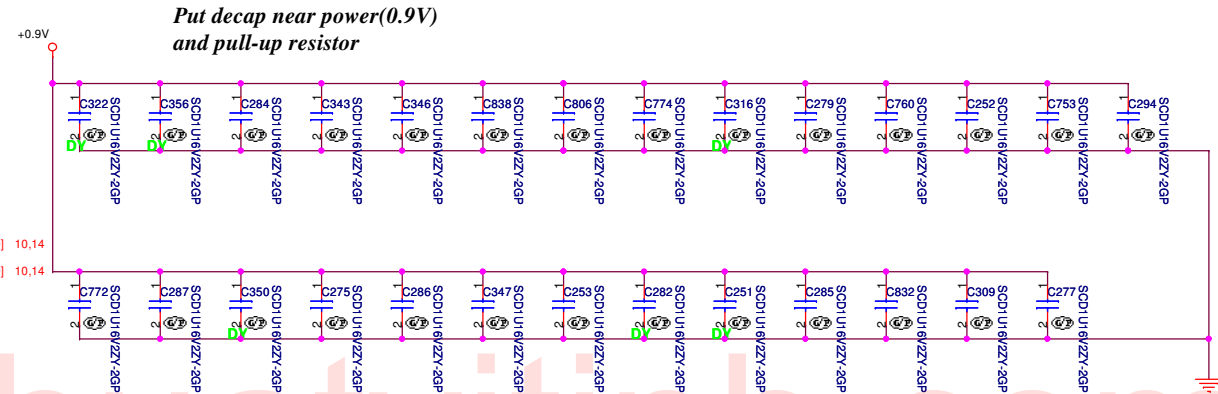




PARALLEL TERMINATION



Decoupling Capacitor



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Taipei Hsien 221, Taiwan, R.O.C.



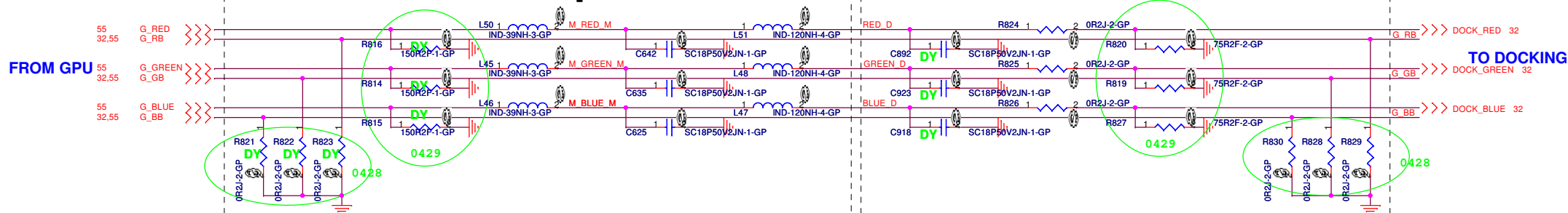
<Variant Name>

	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Clock Generator	
Date:	Monday, May 19, 2008
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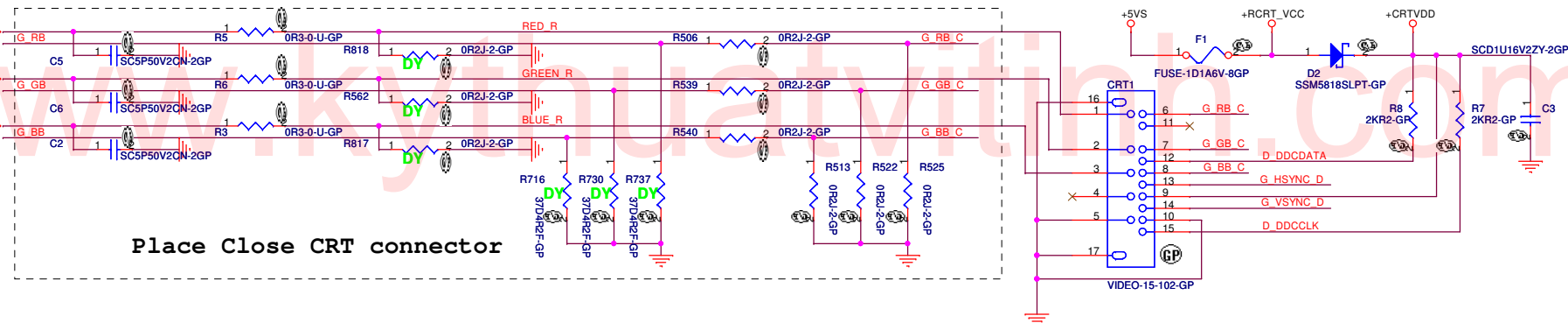
CRT

CRT Termination/EMI Filter

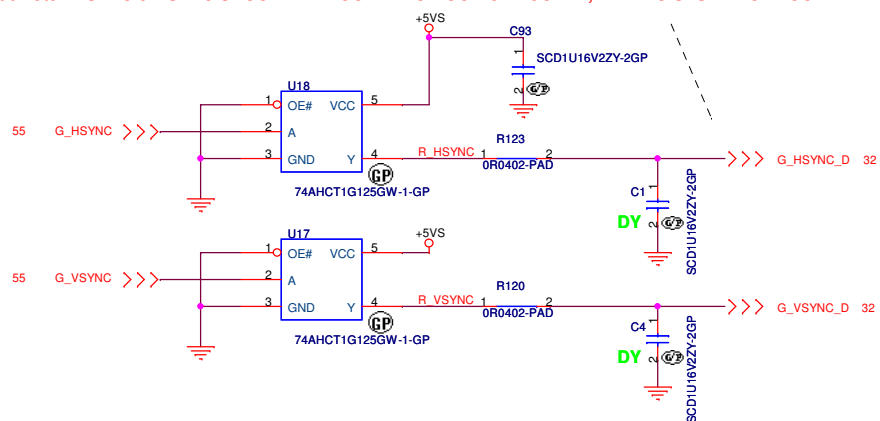
Place Close VGA Chip



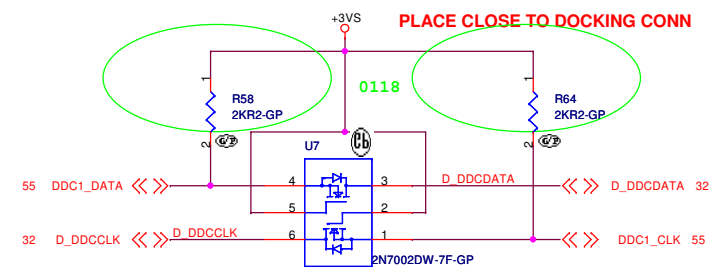
FROM DOCKING



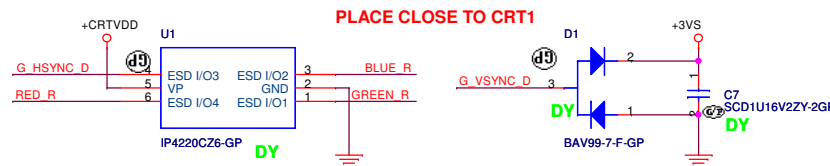
Layout Note : HSYNC & VSYNC SHOULD BE ROUTED TO DOCK CRT CONN., THEN TO SYSTEM CRT CONN.



PLACE CLOSE TO DOCKING CONN



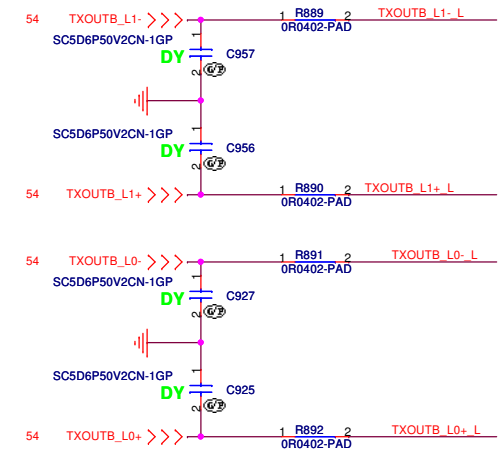
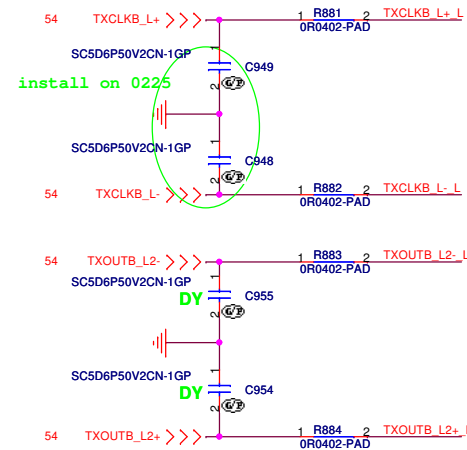
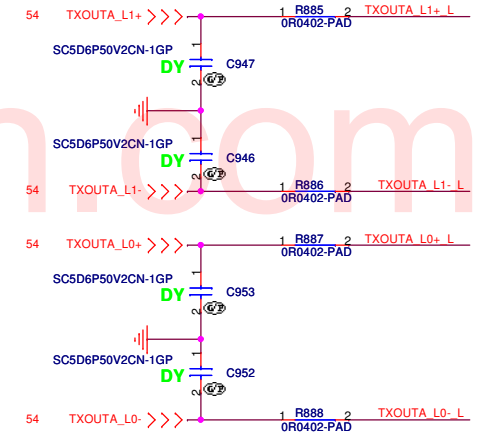
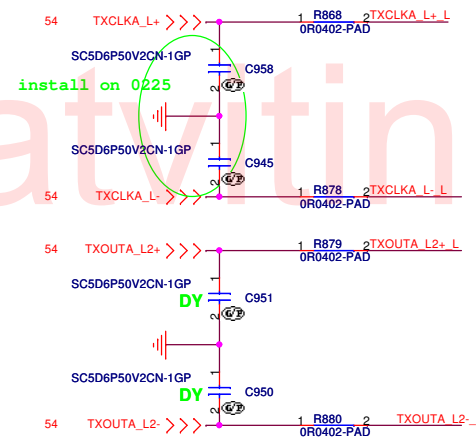
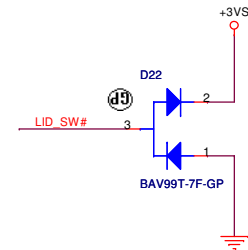
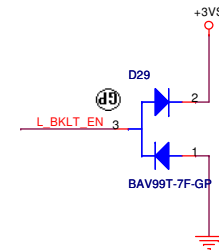
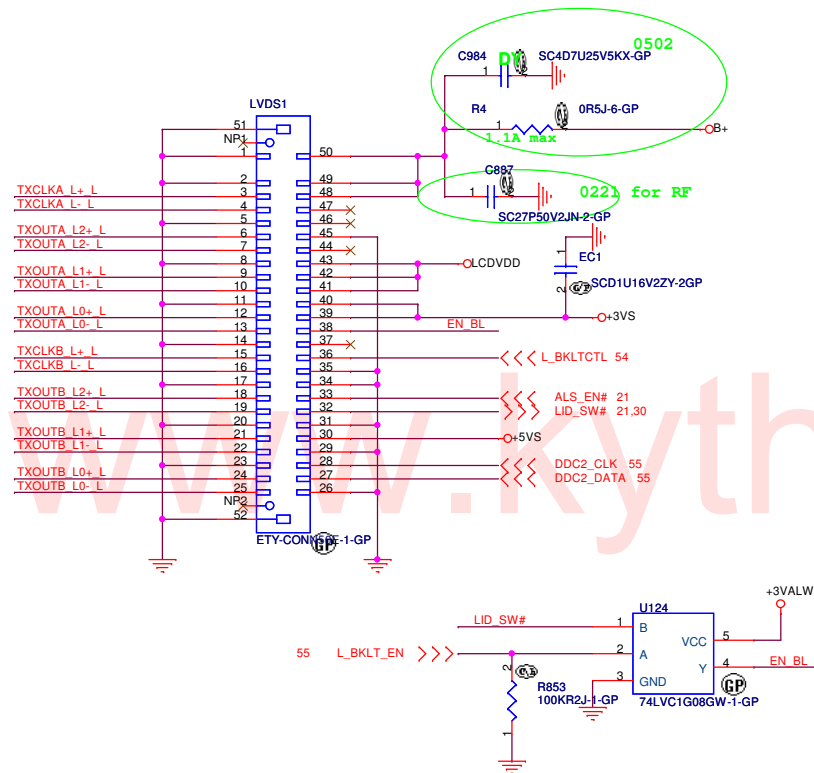
PLACE CLOSE TO CRT1



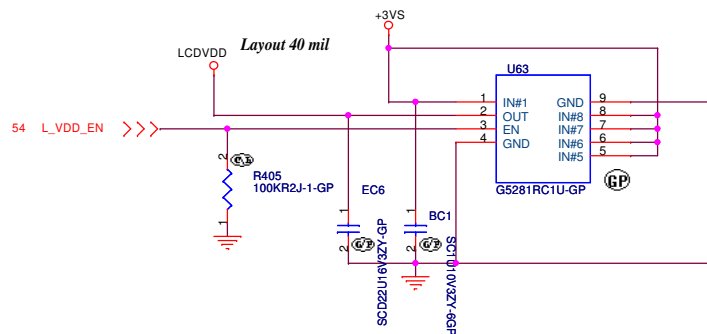
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			CRT CONNECTOR	
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LVDS CONN

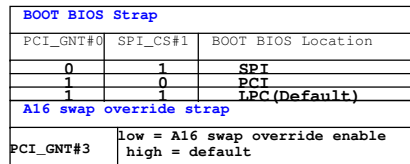


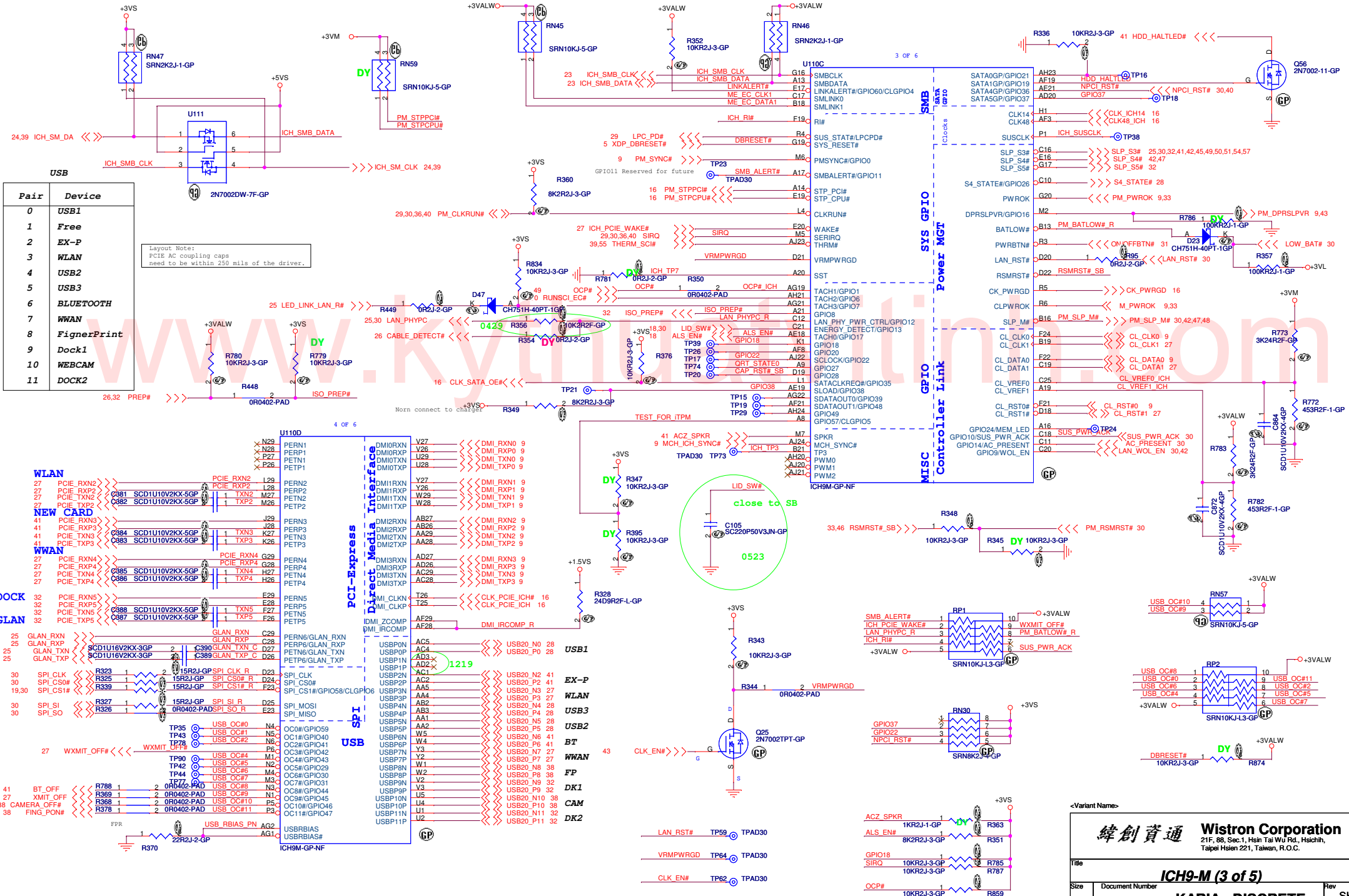
LCD POWER CIRCUIT

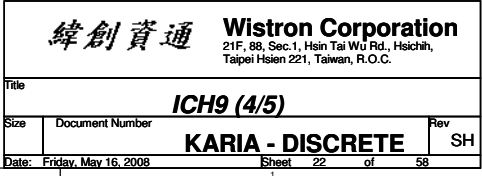


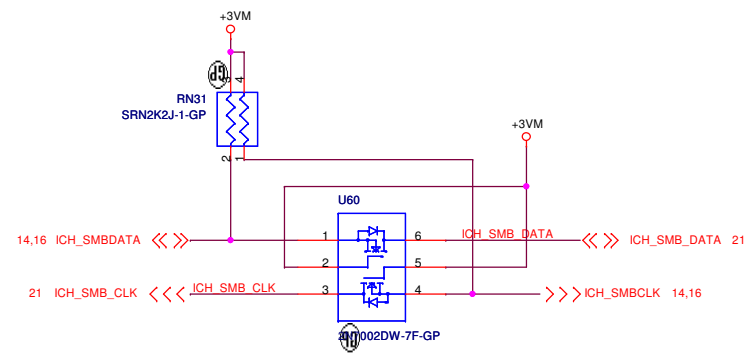
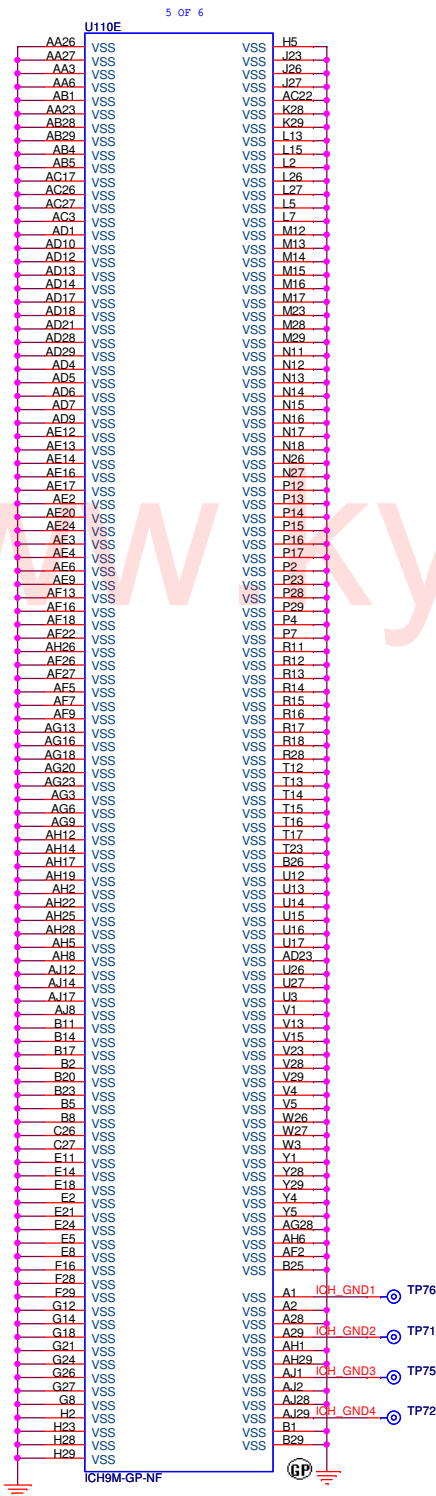
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
LCD CONN.			
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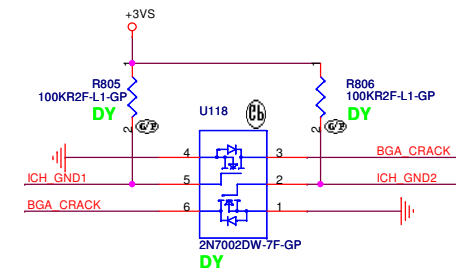
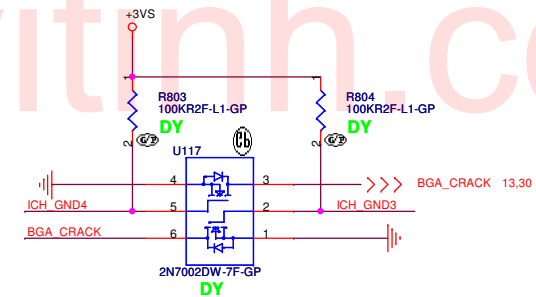






Q13 & Q14 connect SMLINK and
SMBUS in S) for SMBus 2.0
compliance

SMBUS

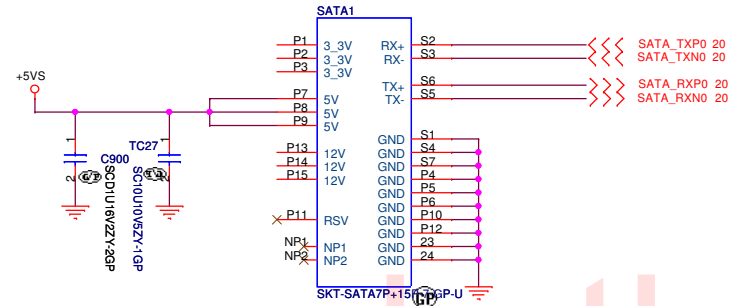


緯創資通

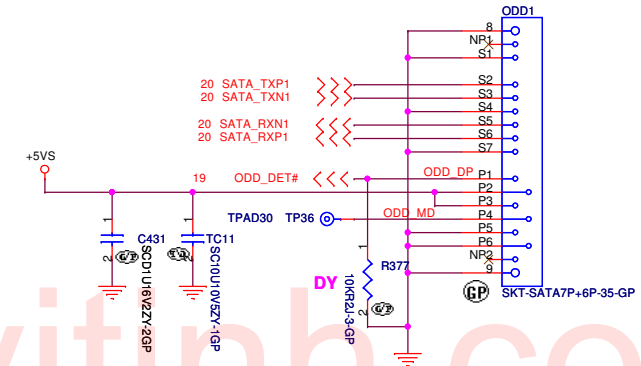
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title				
ICH9-M (5 of 5)				
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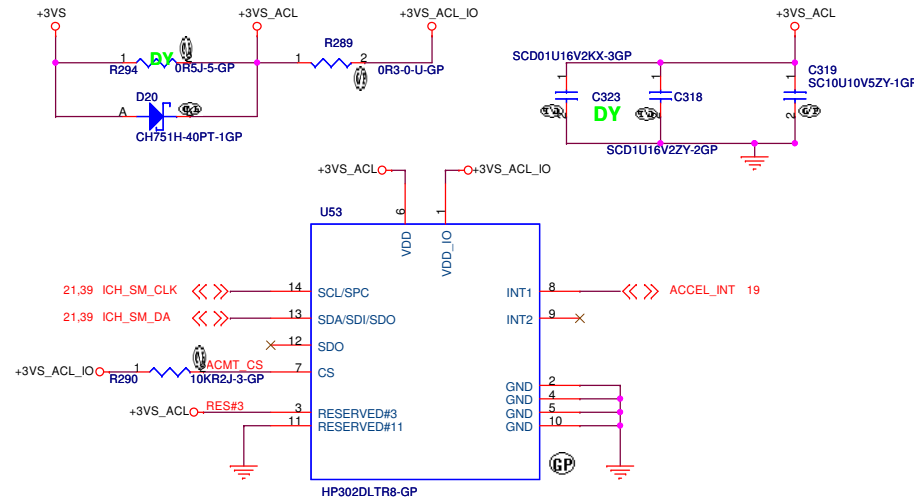
SATA HD Connector



ODD Connector



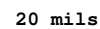
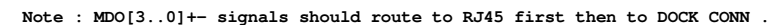
ACCELEROMETER

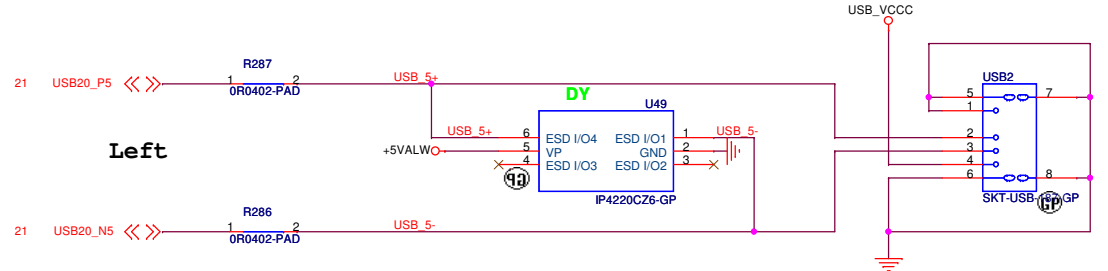
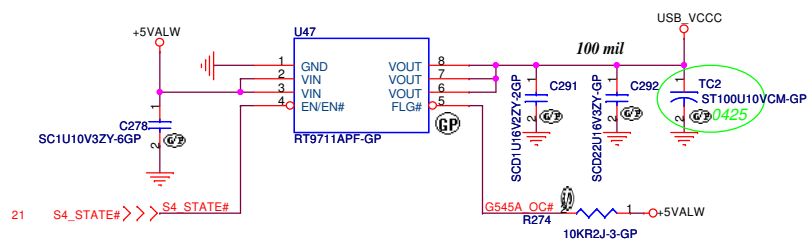
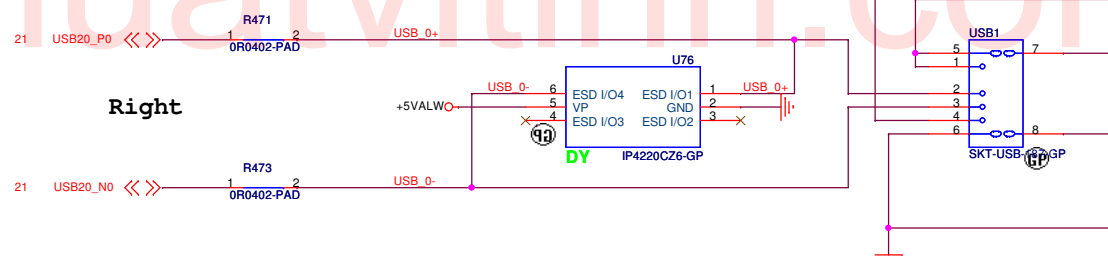
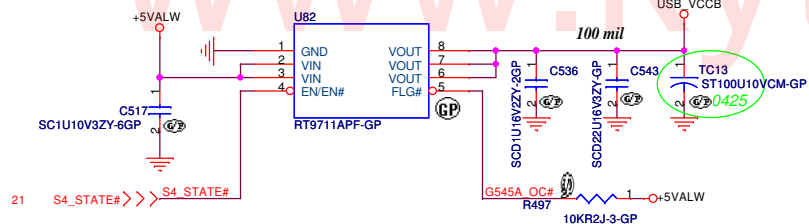
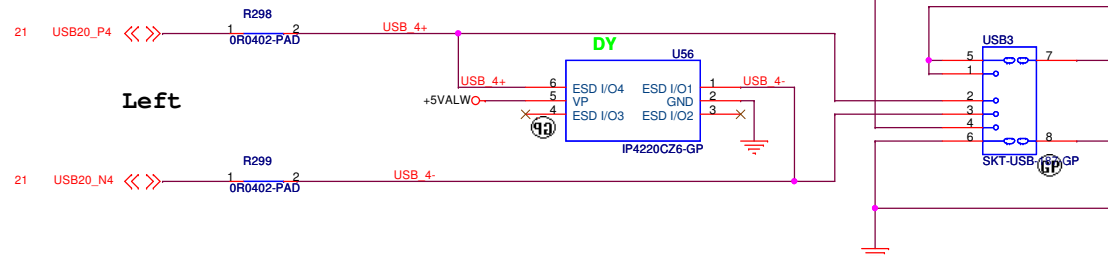
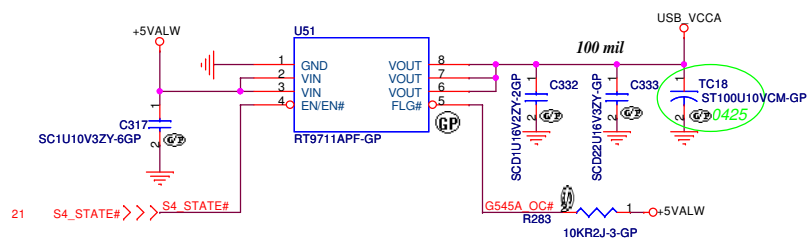


Must be placed in the center of the system

<Variant Name>

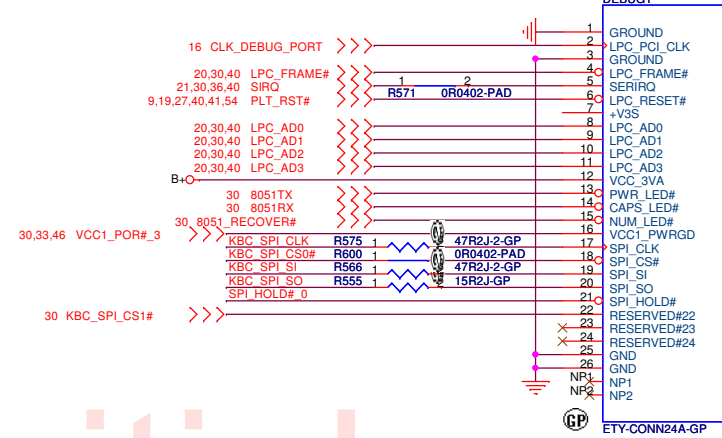
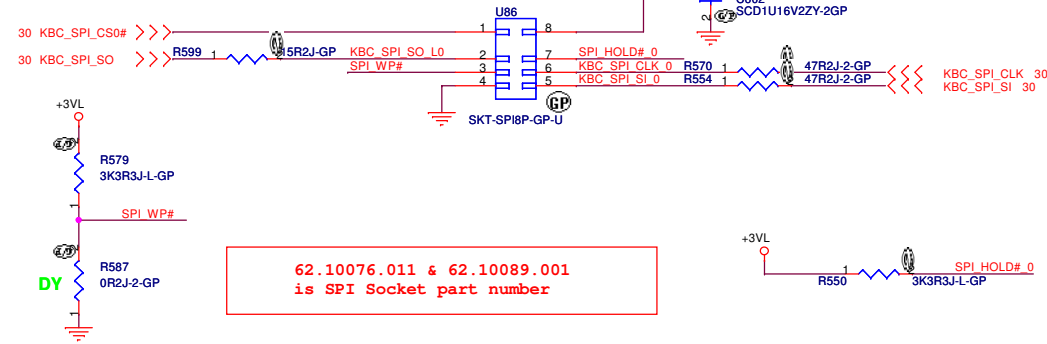
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
HDD/ODD/ACCELEROMETER			
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32Mb x 1

Debug port

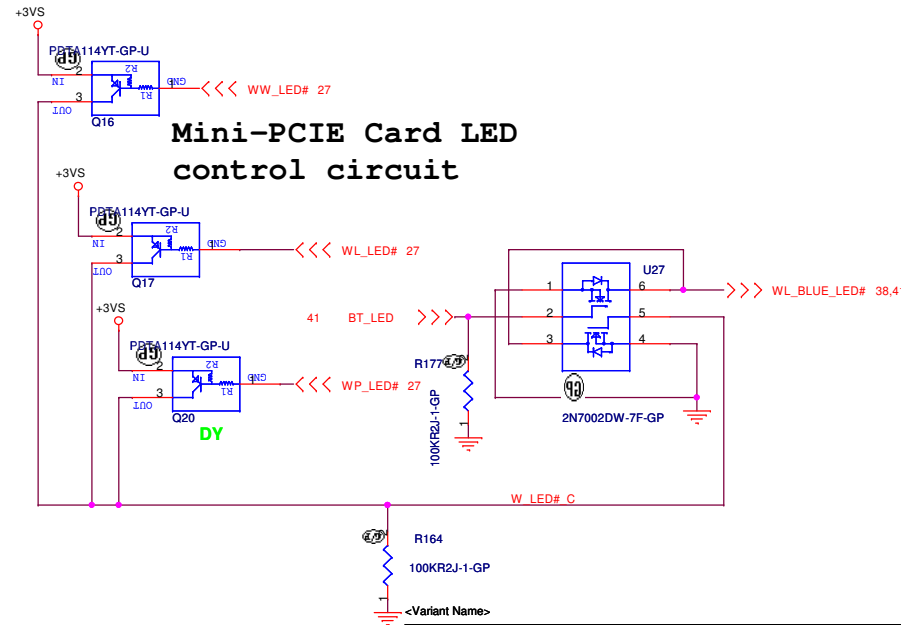
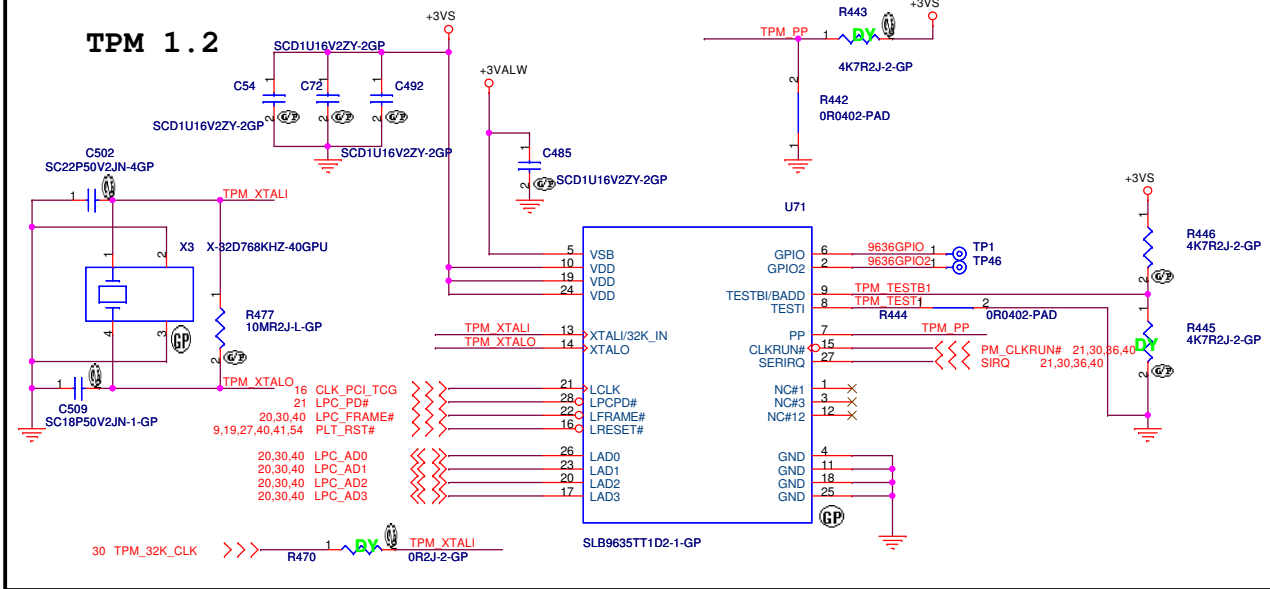


32M SPI
> 72.25325.A01 MXIC MX25L3205D
32M SPI
> 72.26321.A01 IC FEROM AT26DF321-SU, by Atmel

Keep traces of SPI as short as possible and keep trace spacing close to 7mils to any other signal (basically follow specs).

TPM 1.2

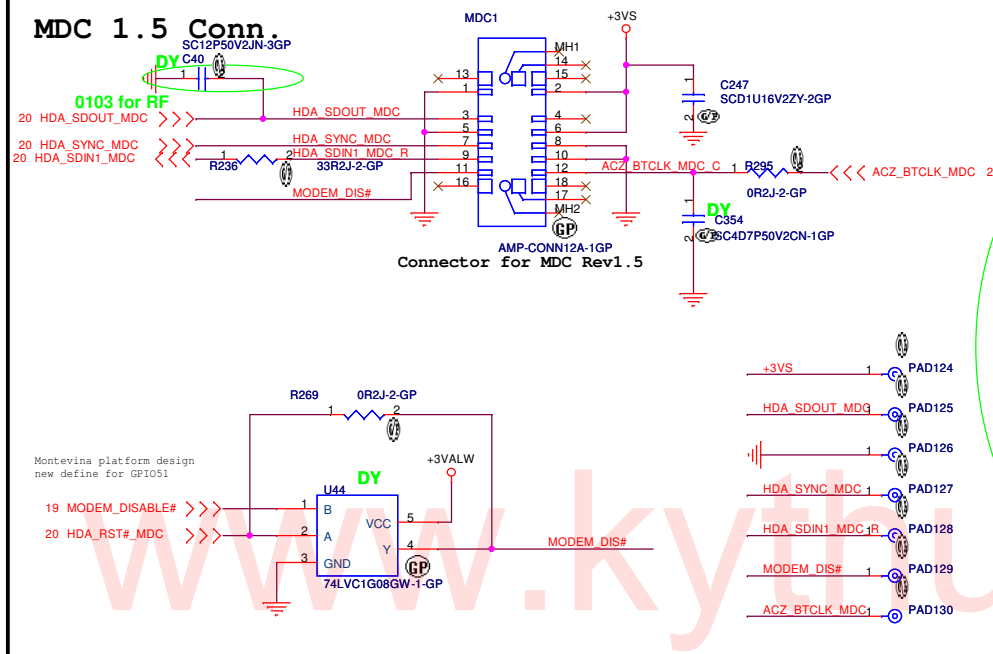
Mini-PCIE Card LED control circuit



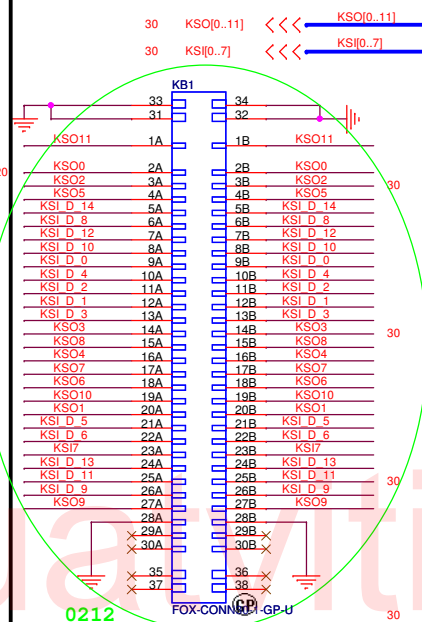
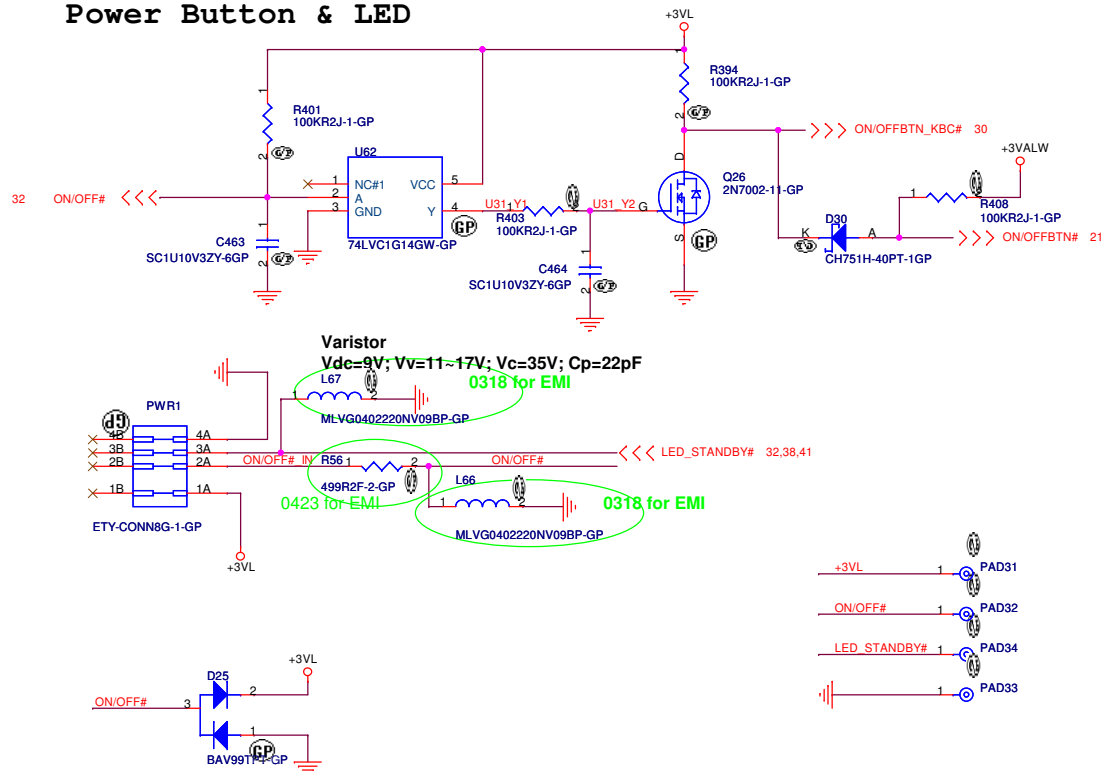
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.



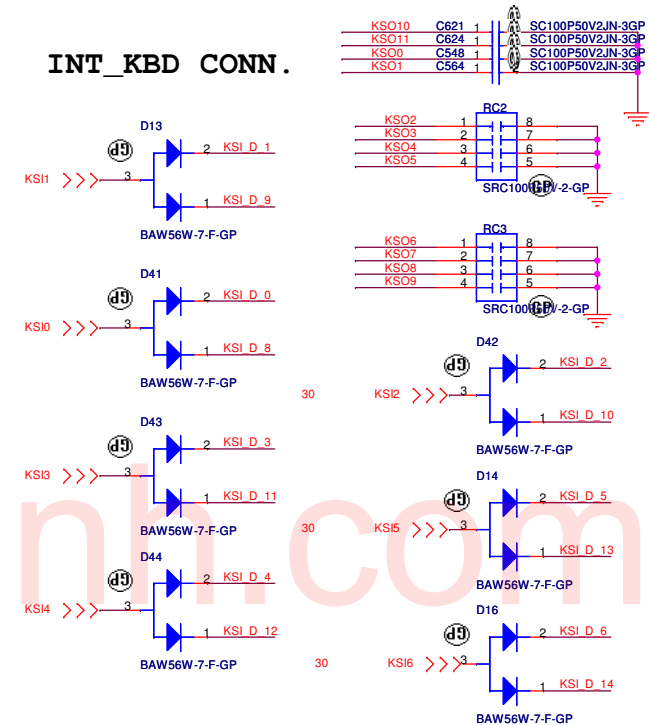
MDC 1.5 Conn.



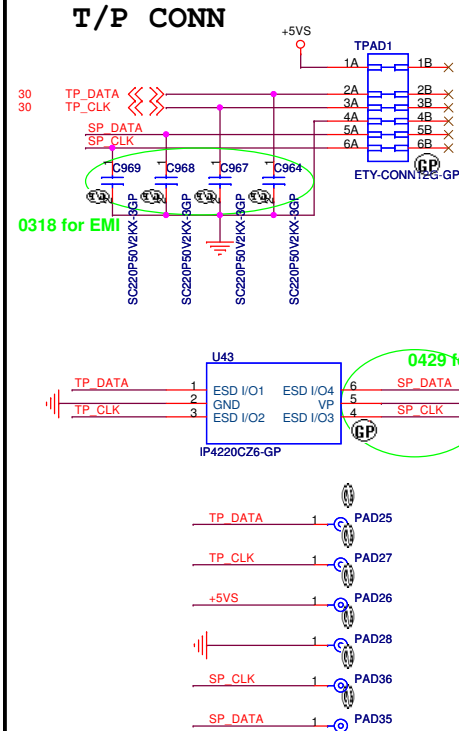
Power Button & LED



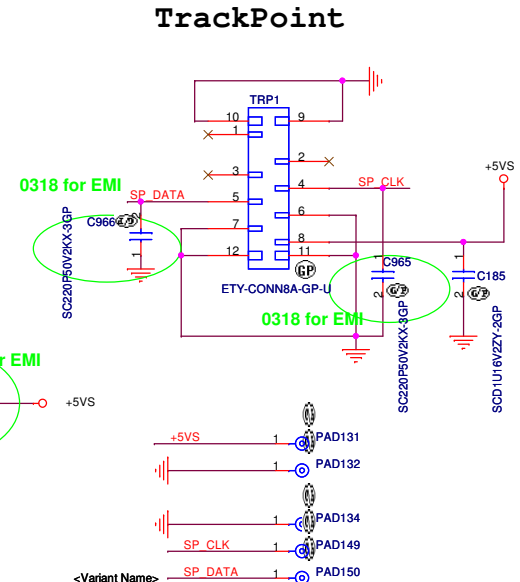
INT_KBD CONN.



T/P CONN



TrackPoint

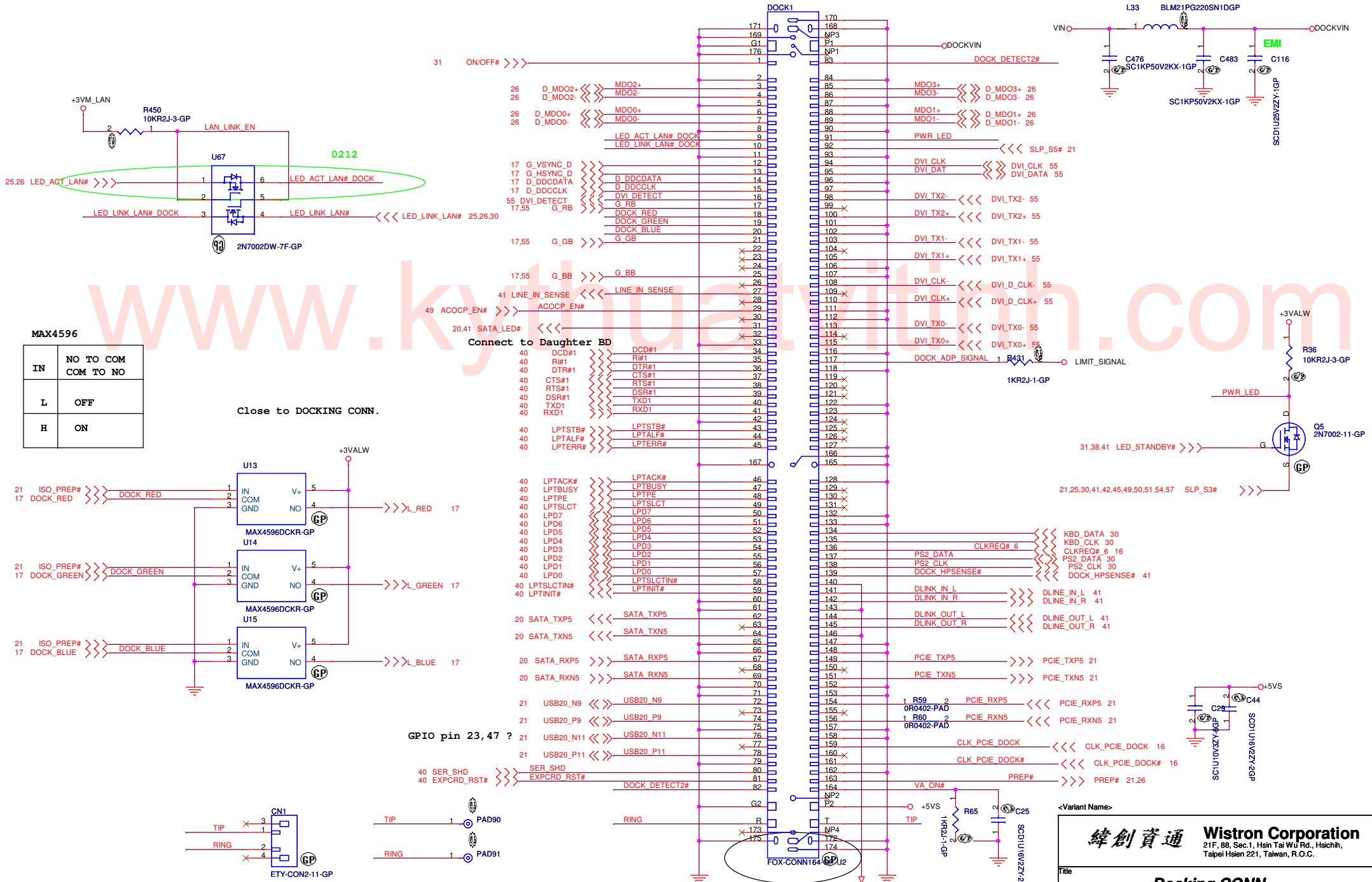


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
MDC/KBD/ON OFF/T.P.			
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Docking CONN. 164 PIN

current rating 6A



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Docking CONN

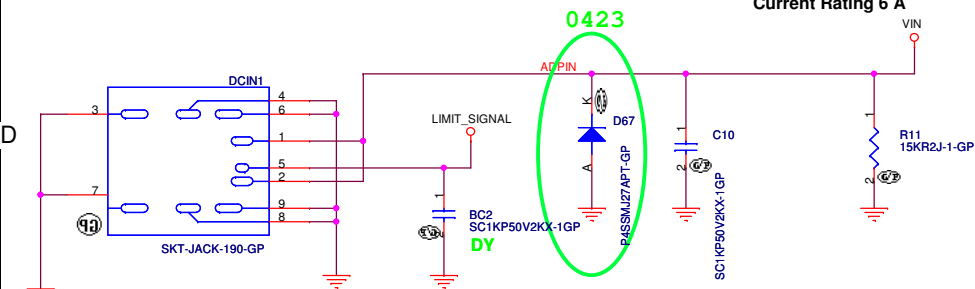
KARIA - DISCRETE

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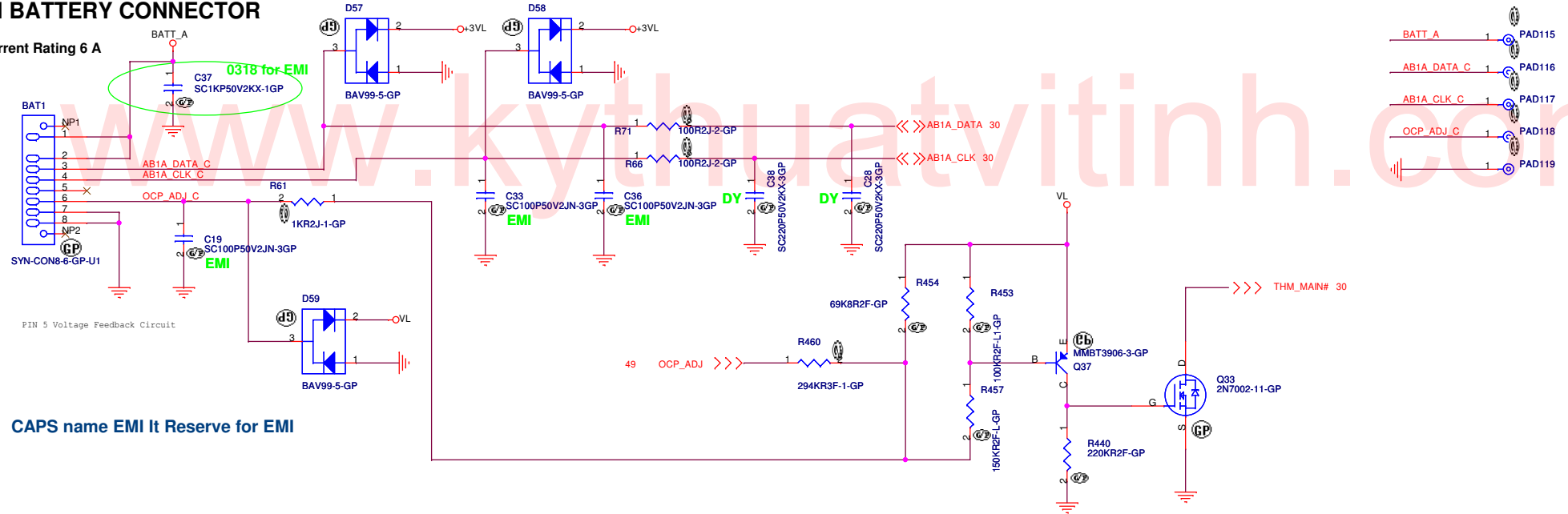
Adaptor in to generate DCBATOUT

Current Rating 6 A



MAIN BATTERY CONNECTOR

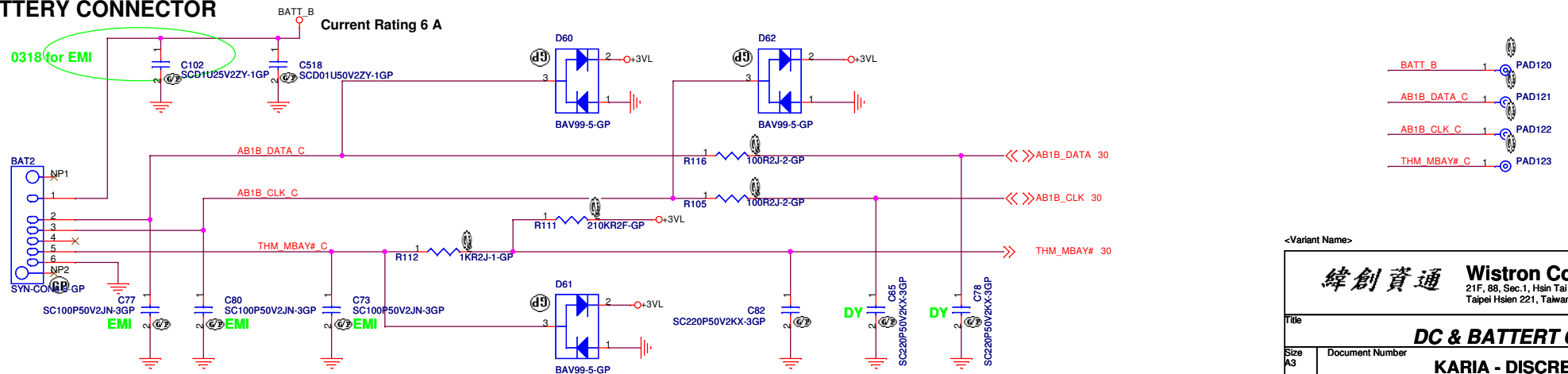
Current Rating 6 A



CAPS name EMI It Reserve for EMI

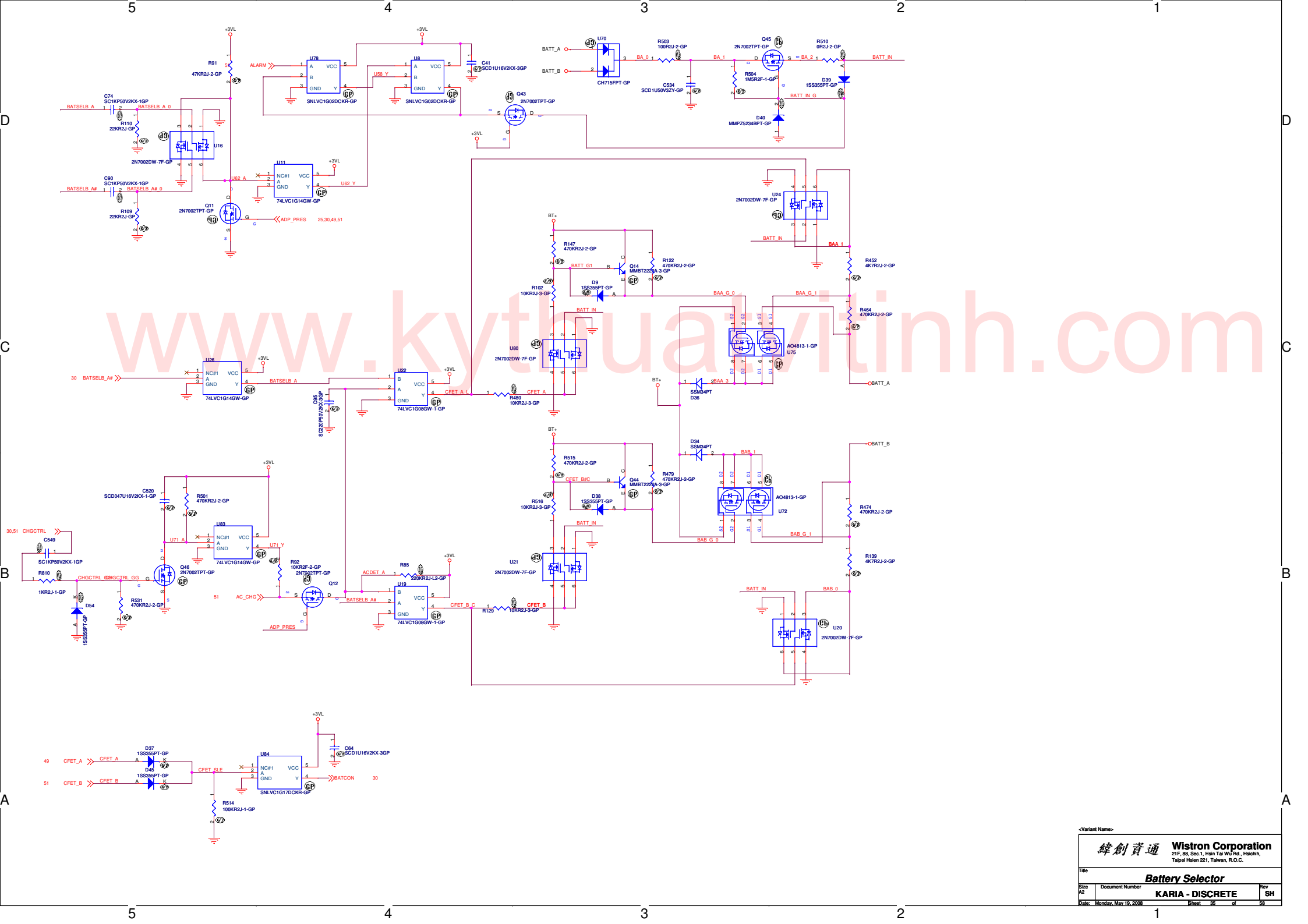
BAY BATTERY CONNECTOR

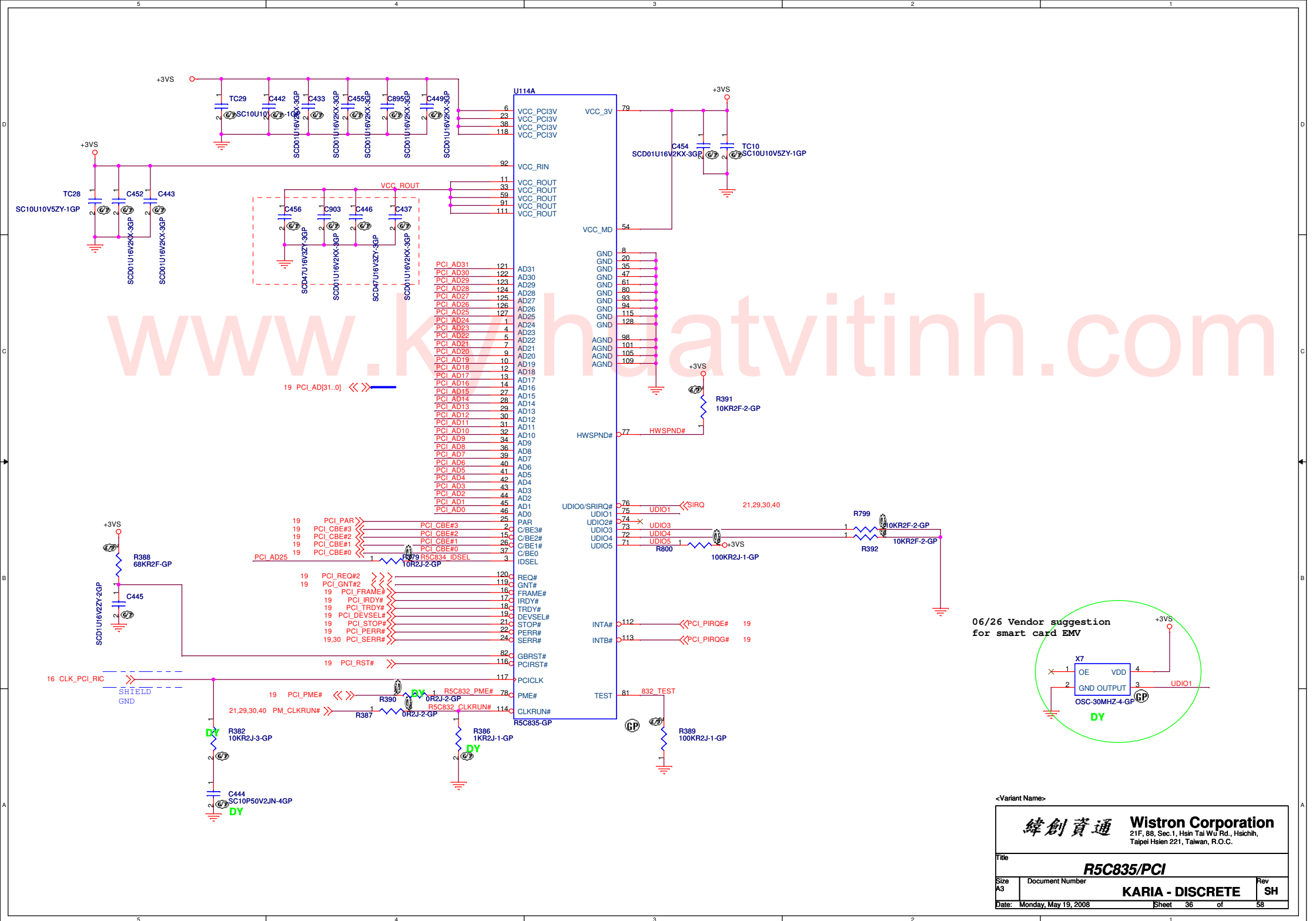
Current Rating 6 A

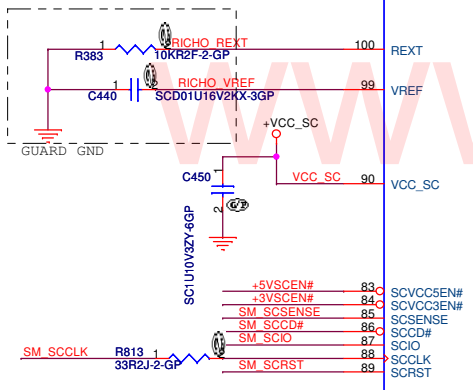
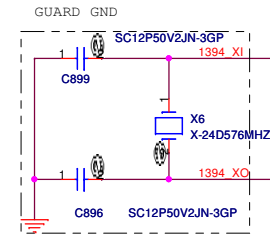


<Variant Name>

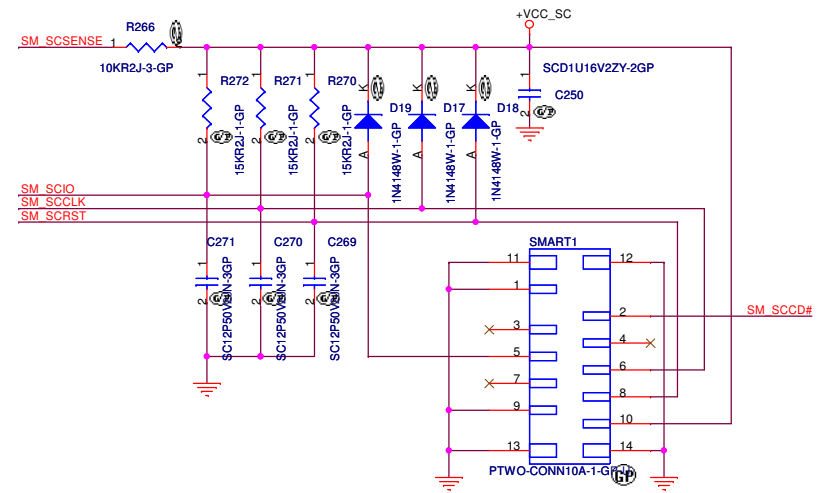
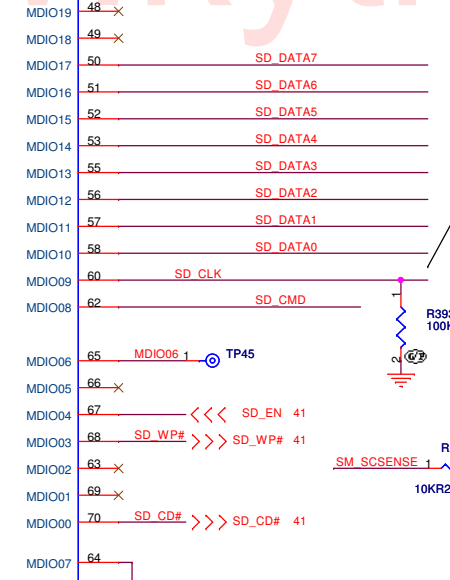
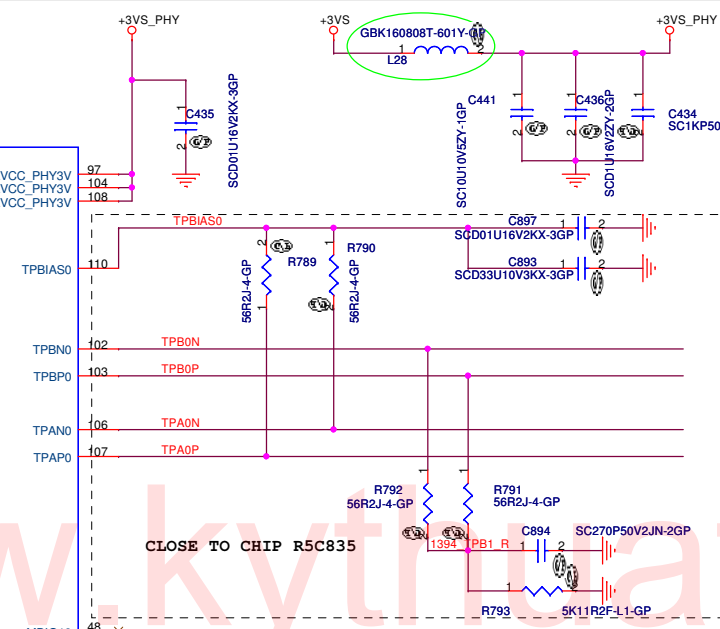
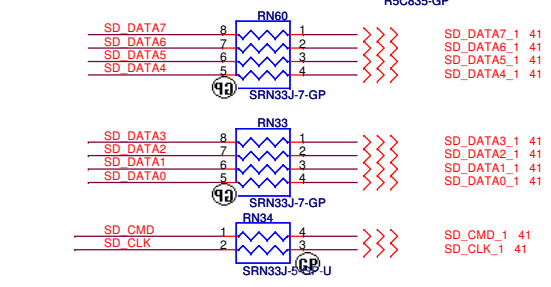
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		DC & BATTERT CONN.	
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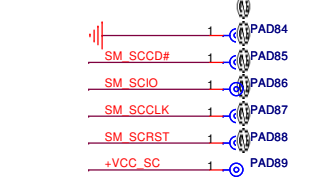
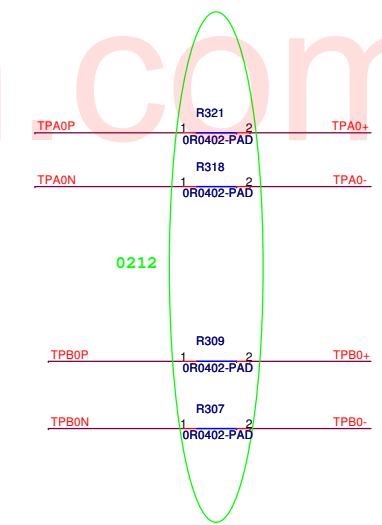
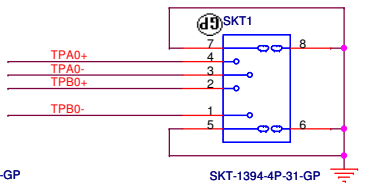
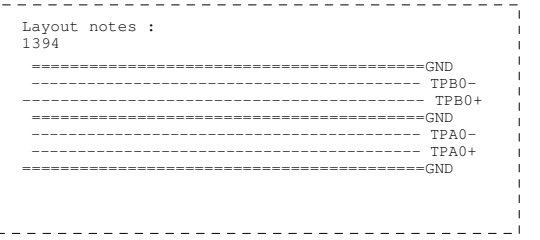




Layout notes :
external parts for
VREF, REXT and FIL0 as
close as possible to R5C833.

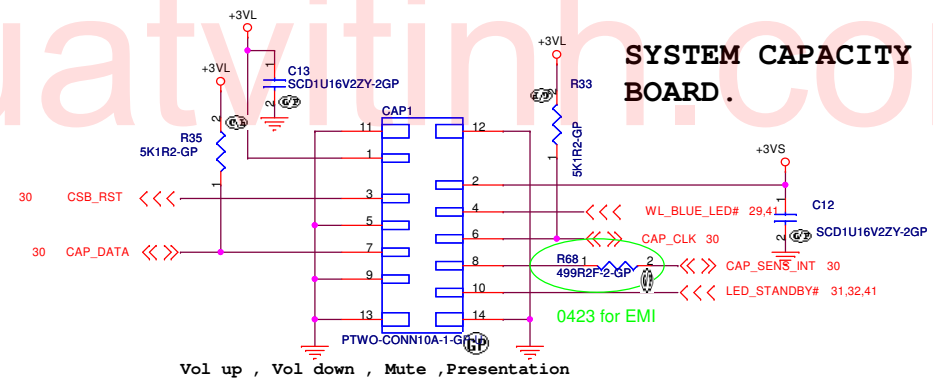
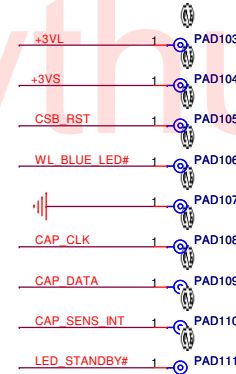
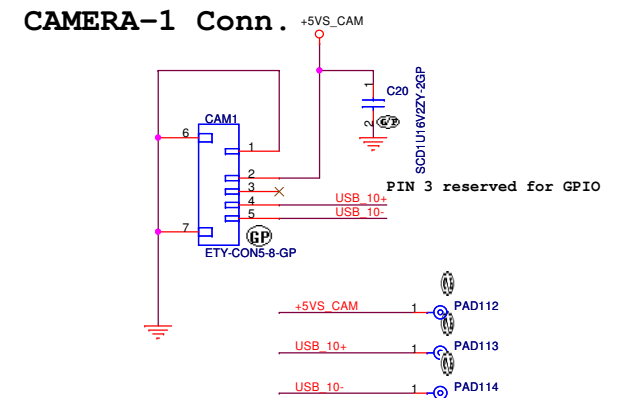
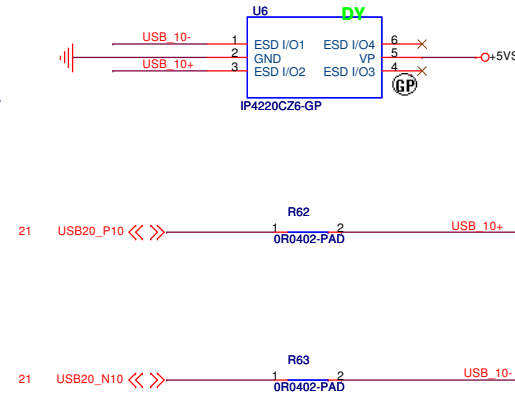
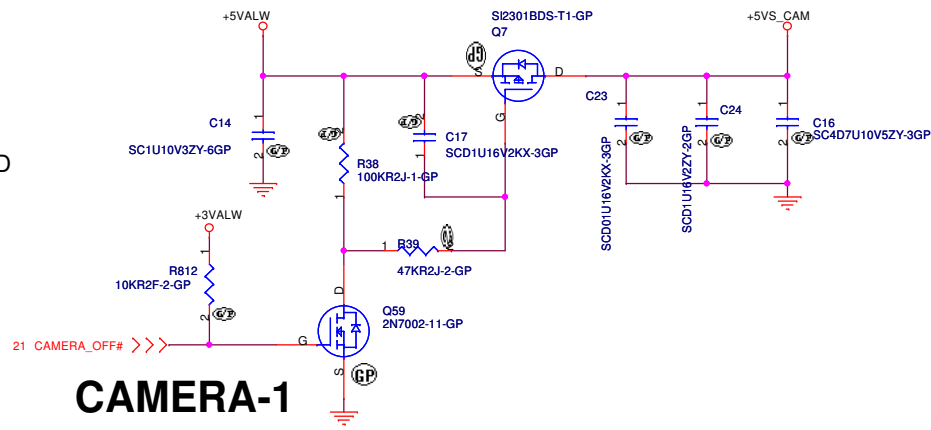


The shield GND is needed for SD_CLK(MDIO09).
Also, the wide-width (more than 0.02inch)
trace for MDIO09 should be used.

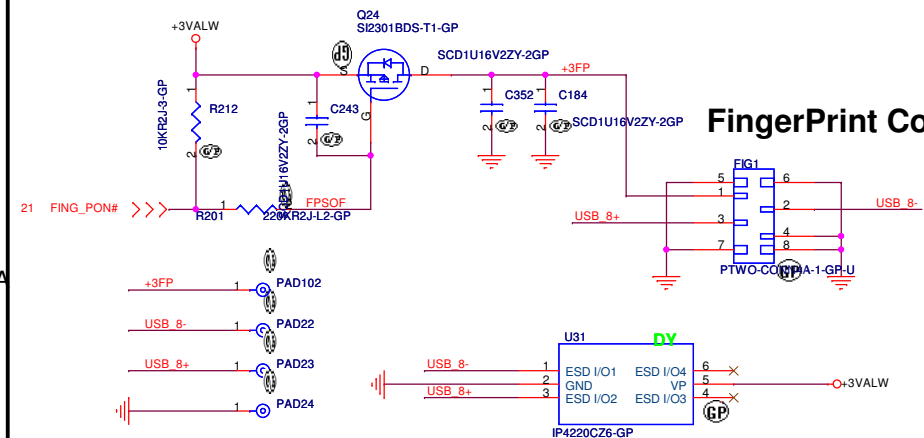


~Variant Name~

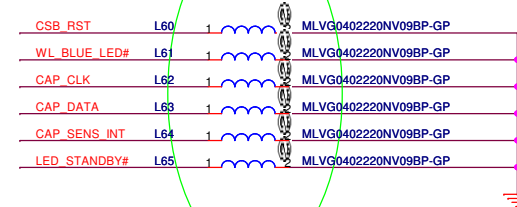
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.			
R5C835/1394/SD/Smart			
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FingerPrint



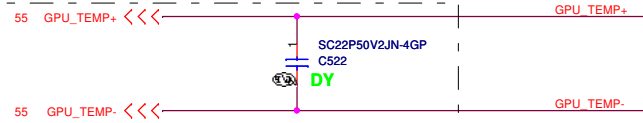
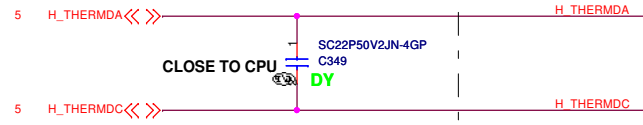
FingerPrint Conn.



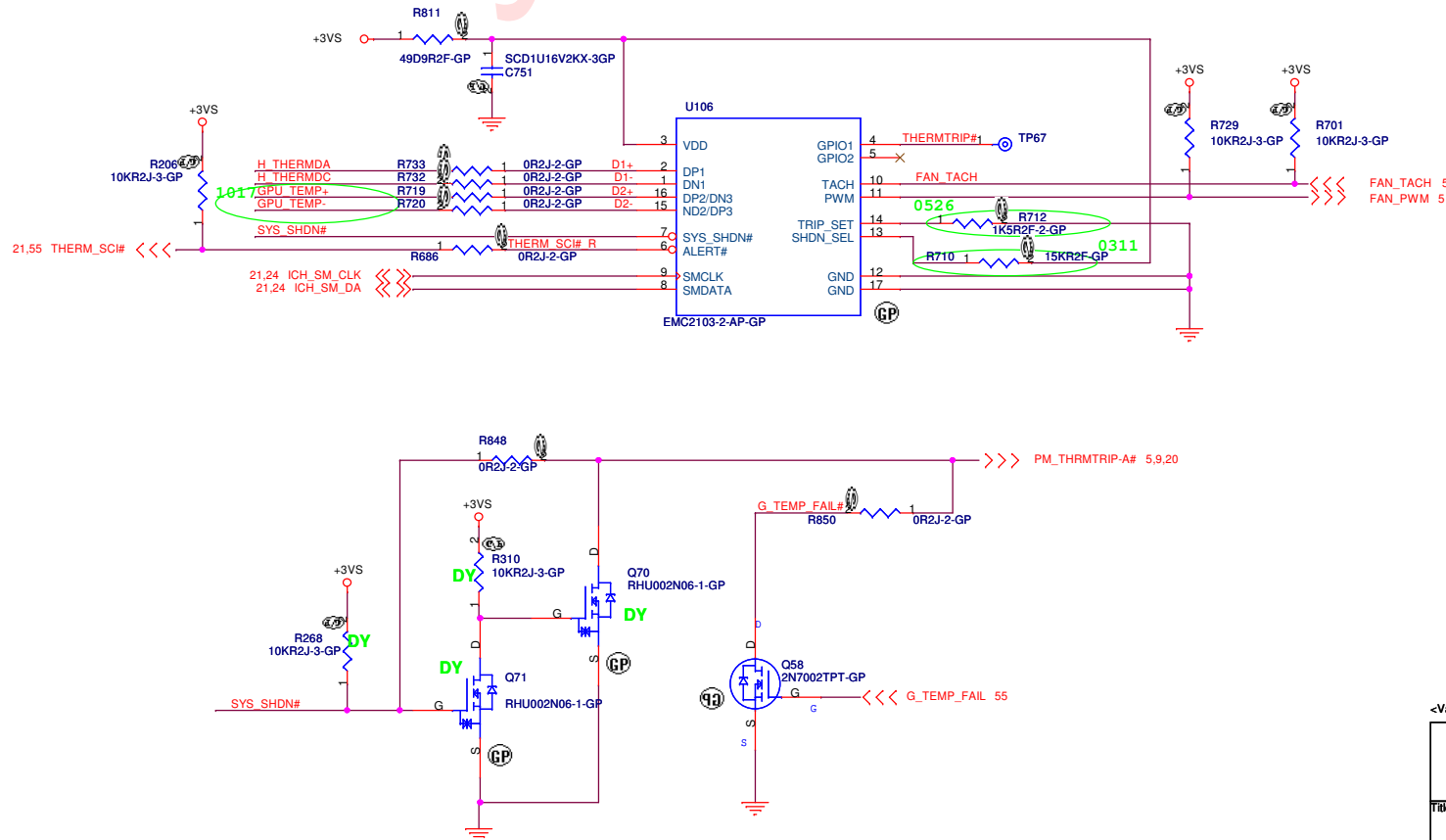
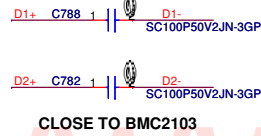
<Variant Name>

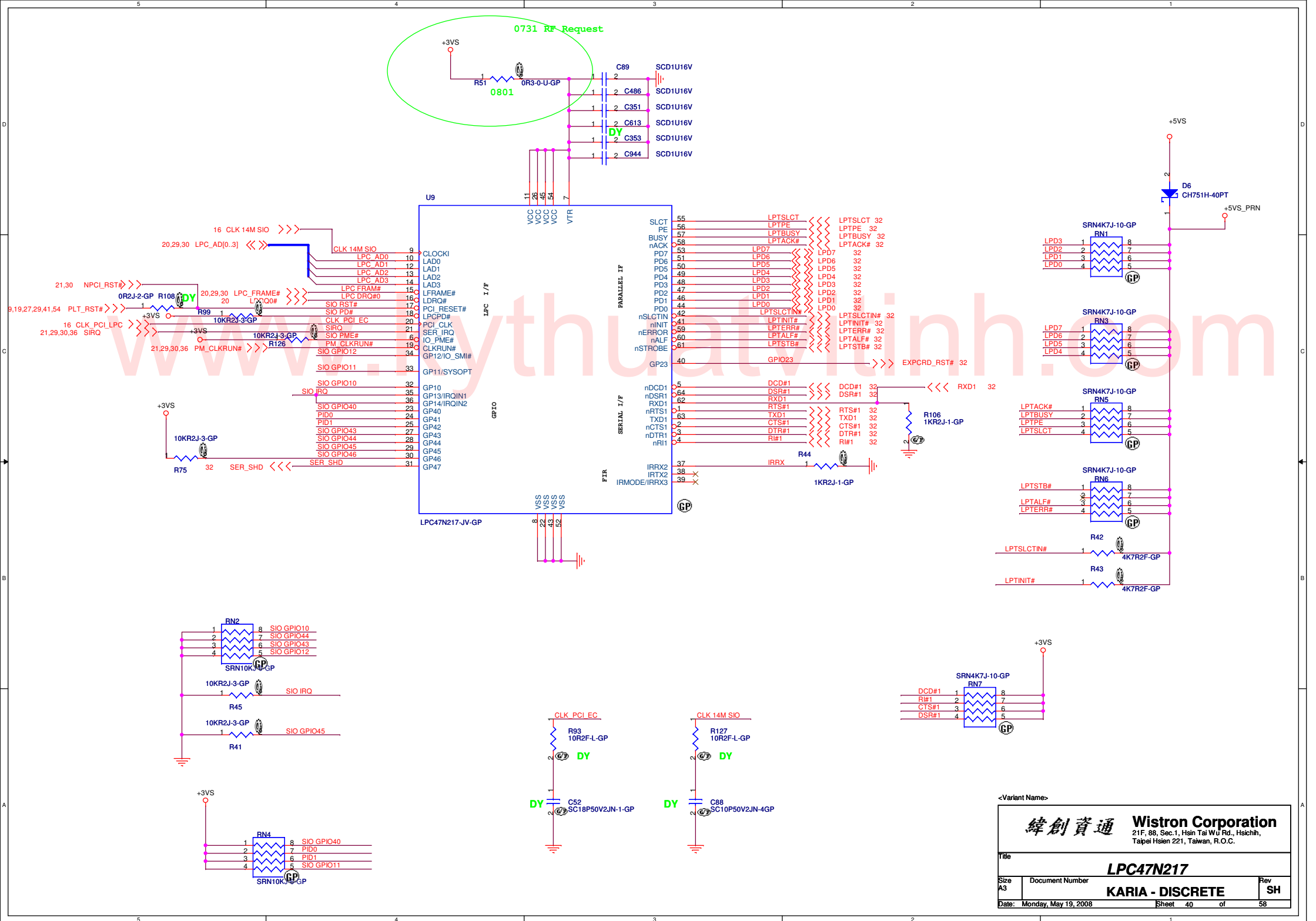
緯創資通 Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Size A3	Document Number
Camera/W-COM KARIA - DISCRETE	
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CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near thermal diode

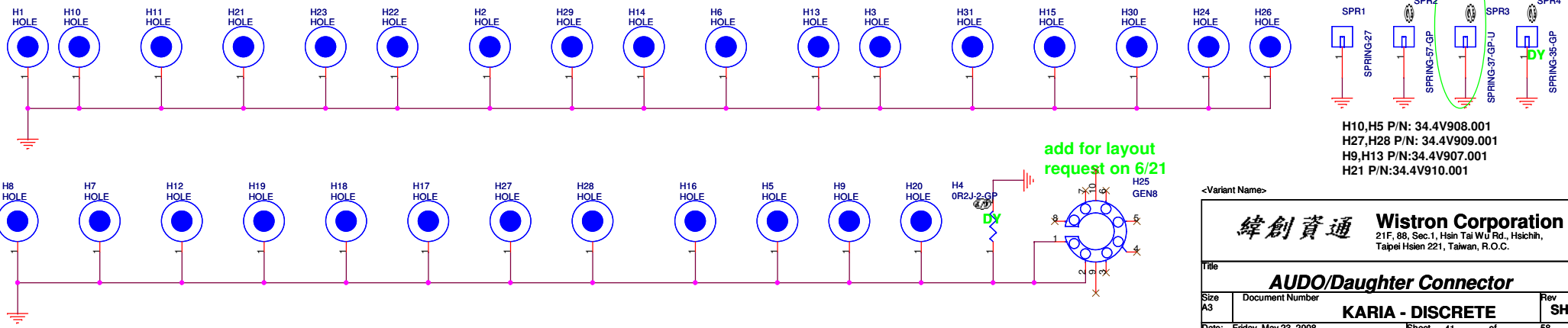
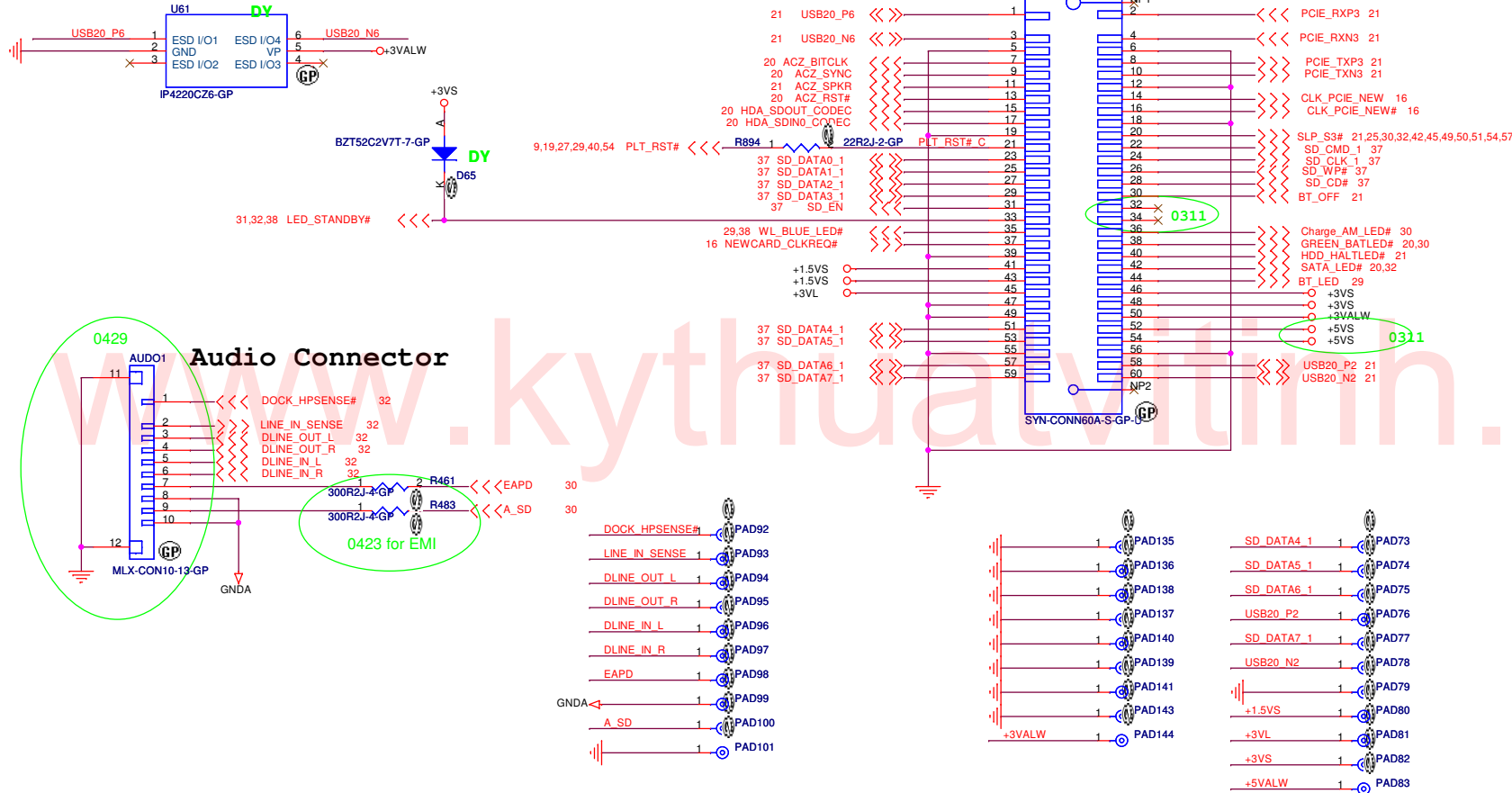


GPU DIE TEMP:
REMOTE2+ and REMOTE2- routing 10mil trace width and 10 mil spacing.

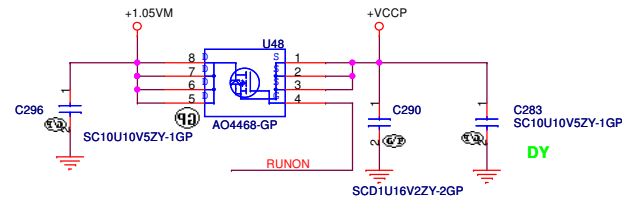




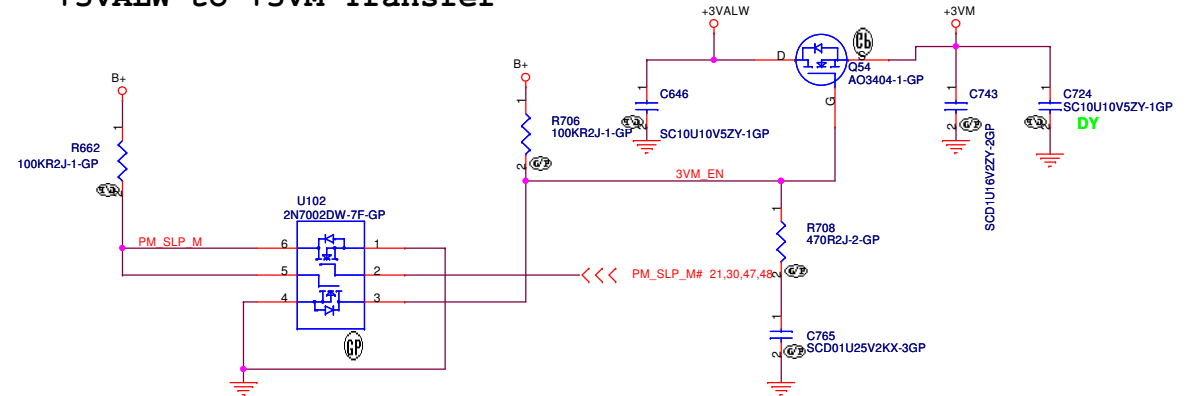
Daughter Board Connector



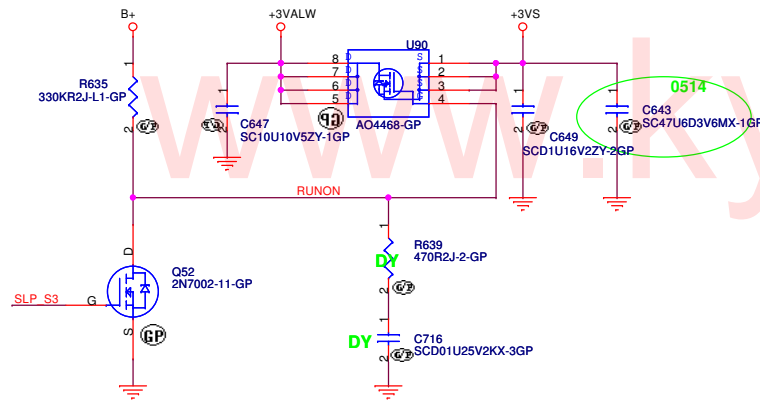
+1.05VM to +VCCP Transfer



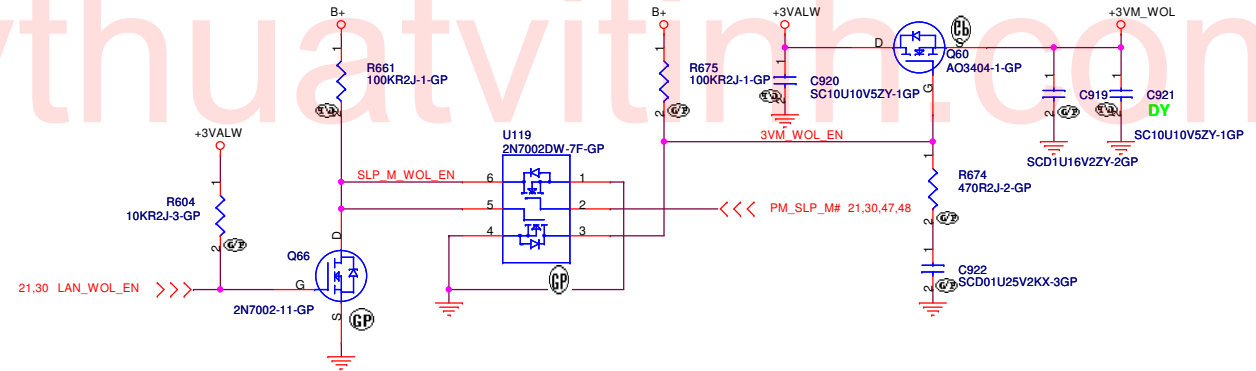
+3VALW to +3VM Transfer



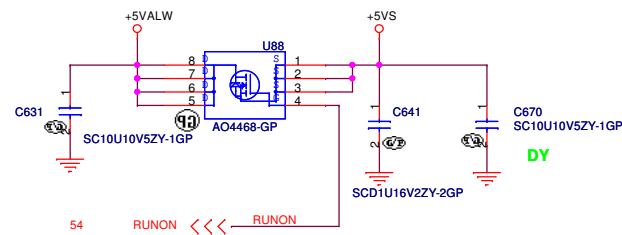
+3VALW to +3VS Transfer



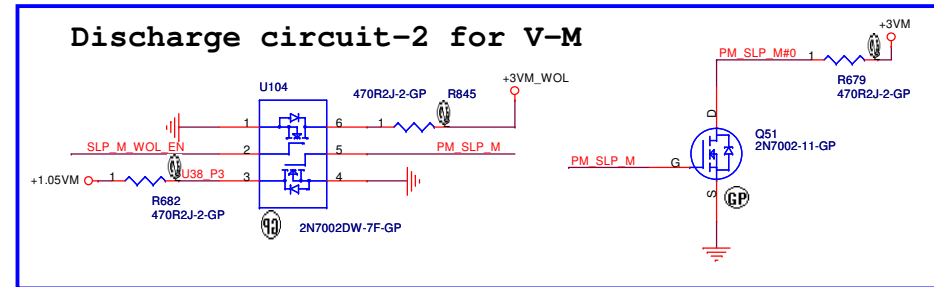
+3VALW to +3VM_WOL



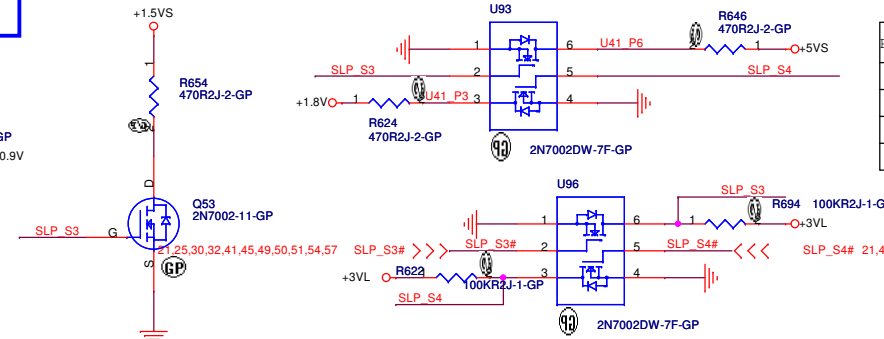
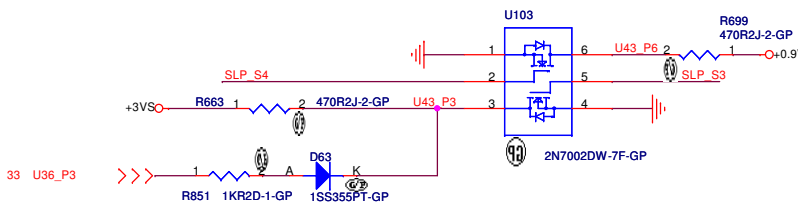
+5VALW to +5VS Transfer



Discharge circuit-2 for V-M



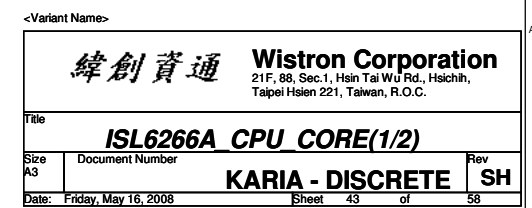
Discharge circuit-1

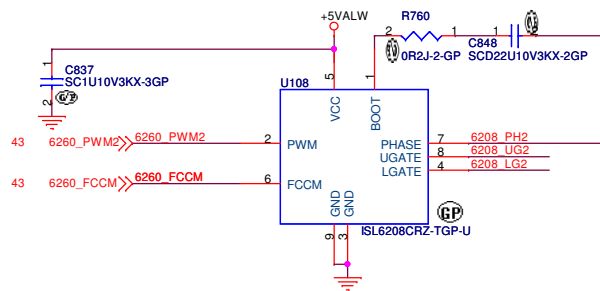


PM_SLP_M#	LAN_WOL_EN	+3VM_WOL	+3VM	SYSTEM STATE
0	0	0V	0V	Moff / No WOL
0	1	3.3V	0V	Legacy WOL/ Moff
1	0	3.3V	3.3V	M1
1	1	3.3V	3.3V	M1

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DC/DC Circuit		
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84.08692.037 FDMS8692
Power PAK Id=10.5A Qg=8~11nC
Rdson=10.5~14mΩ

1026
Use ZZ.COMBO.001
as Footprint

84.08670.036 FDMS8670AS
POWERPAK Id=17.9A
Qg=20~28nC Rdson=3.6~4.7mΩ

Change L21 to 68.R3610.20A for Main Source

CYNTEC 0.36uH
Idc=30A 10*11.5*4
DCR=1.05mOhm

Panasonic 330uF 2V
ESR=9mΩ
Iripple=3A

<Variant Name>

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Title ISL6266A CPU CORE(2/2)		
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84.08692.037 FDMS8692
Power PAK Id=10.5A
Qg=8~11nC Rdson=10.5~14mΩ

CYNTEC 0.82uH
Idc=13A 6.5*6.9*3
DCR=6.7m Ohm

VGA_CORE
Iomax=16A
OCP<19.5A

84.08670.036 FDMS8670AS
POWERPAK Id=17.9A
Qg=20~28nC
Rdson=3.6~4.7mΩ

Panasonic 470uF 2.5V
ESR=9mOhm
Iripple=3.725A

VGA_CORE TABLE

G1, G0	Vout Equation	R1 (R586)	R2 (R601)	R3 (R258+R262)	R4 (R595+R602)	Vout
(0,0)	$0.75 \cdot (1 + R1/R2 + R1/R3 + R1/R4)$	1K	100K	4.98K	3.82K	1.104V
(0,1)	$0.75 \cdot (1 + R1/R2 + R1/R4)$	1K	100K		3.08K	1.001V
(1,0)	$0.75 \cdot (1 + R1/R2 + R1/R3)$	1K	100K	4.98K		0.908V
(1,1)	$0.75 \cdot (1 + R1/R2)$	1K	100K			0.758V

Removed these GAP
by Power's Request

Removed these GAP
by Power's Request

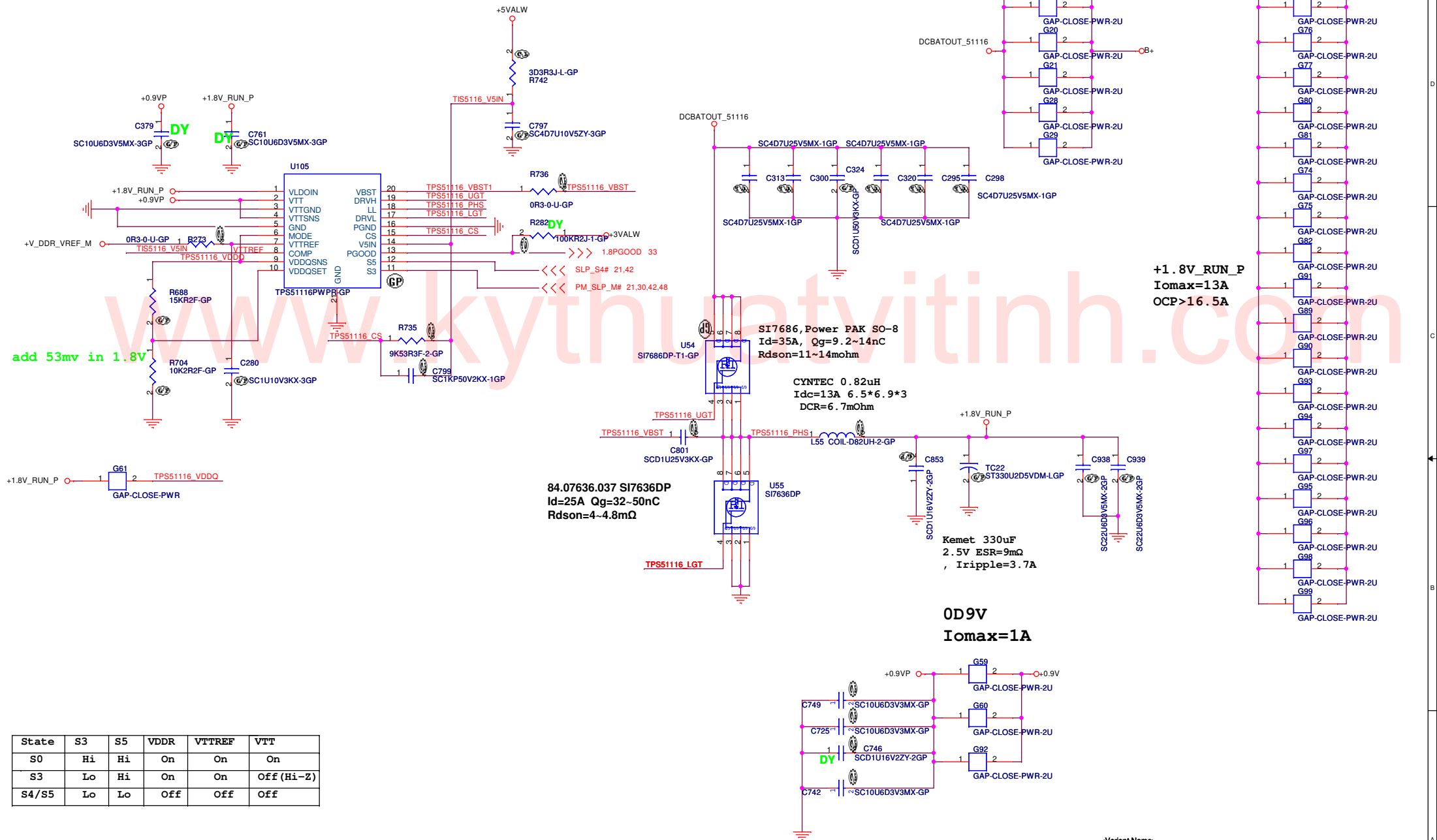
<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

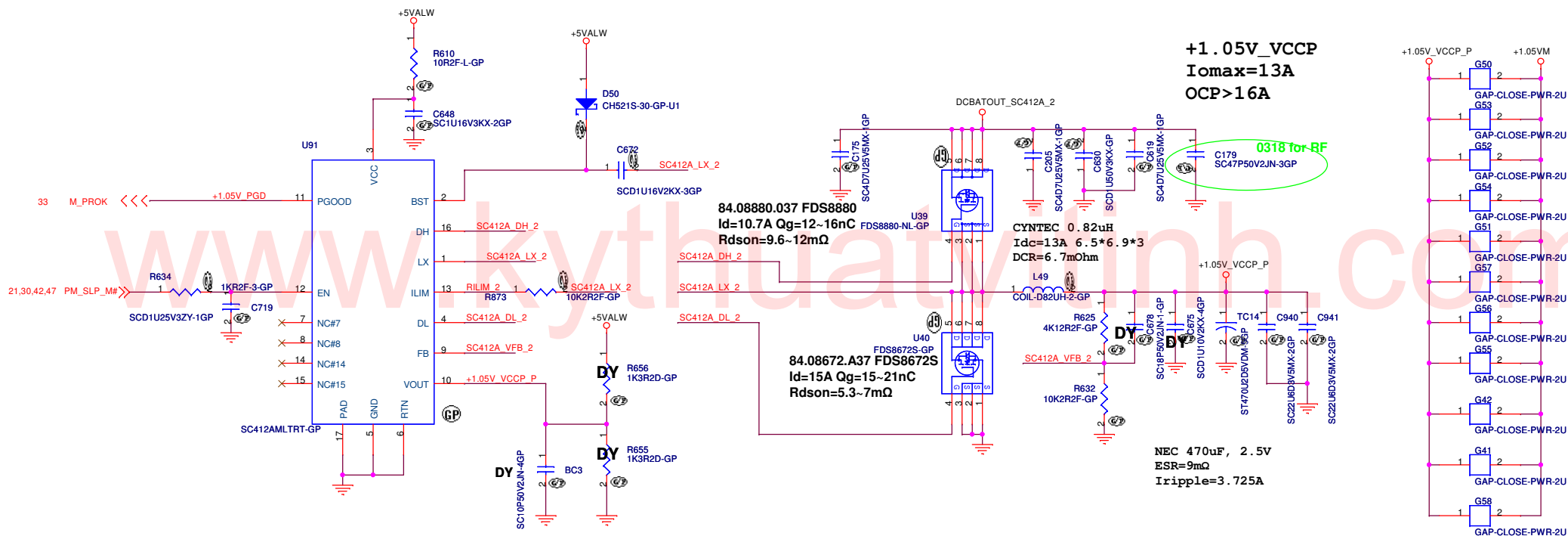
Title SC471A VGA CORE		
Size B	Document Number KARIA - DISCRETE	Rev SH
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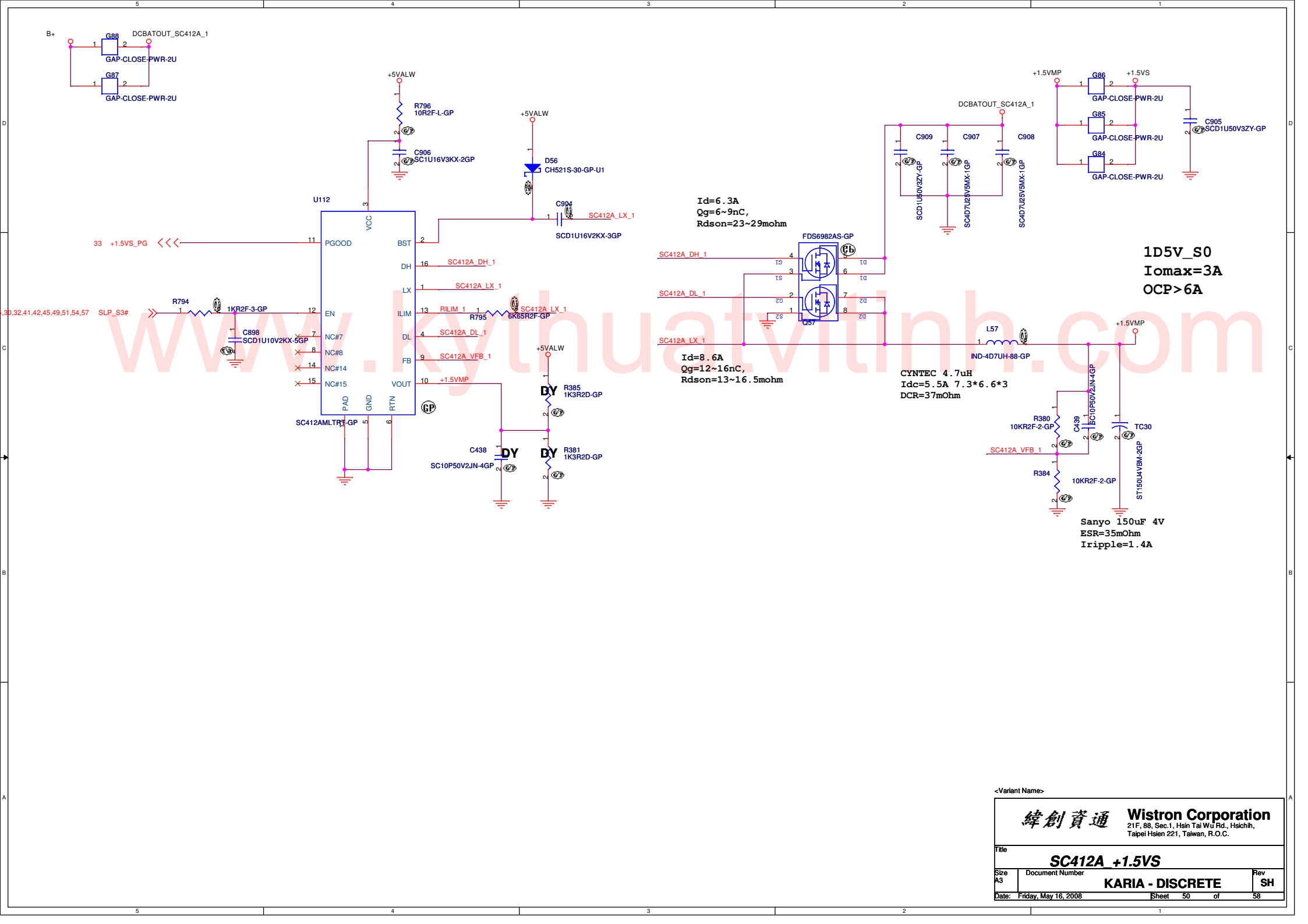


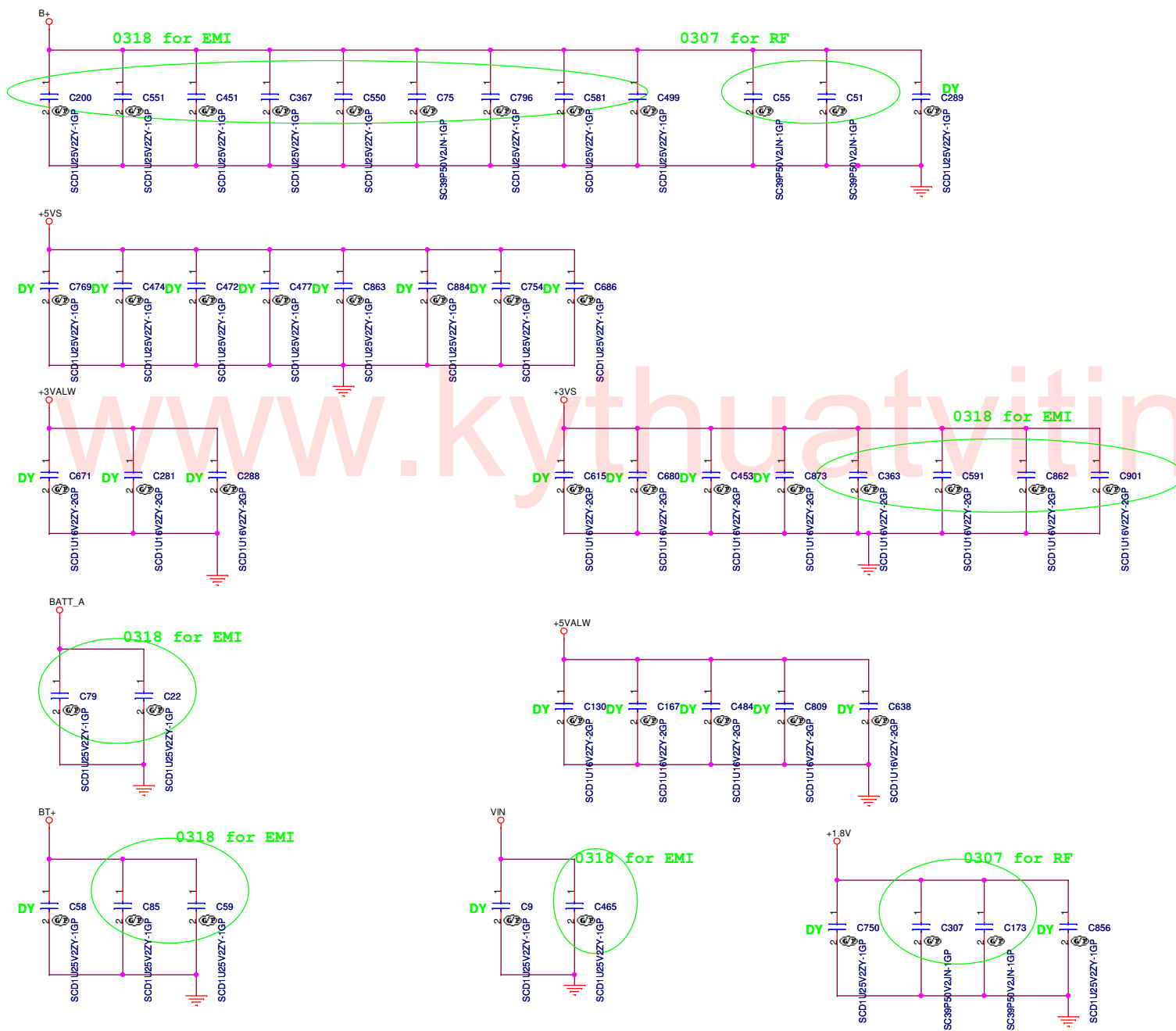
TI TPS51116 for 1D8V and 0D9V

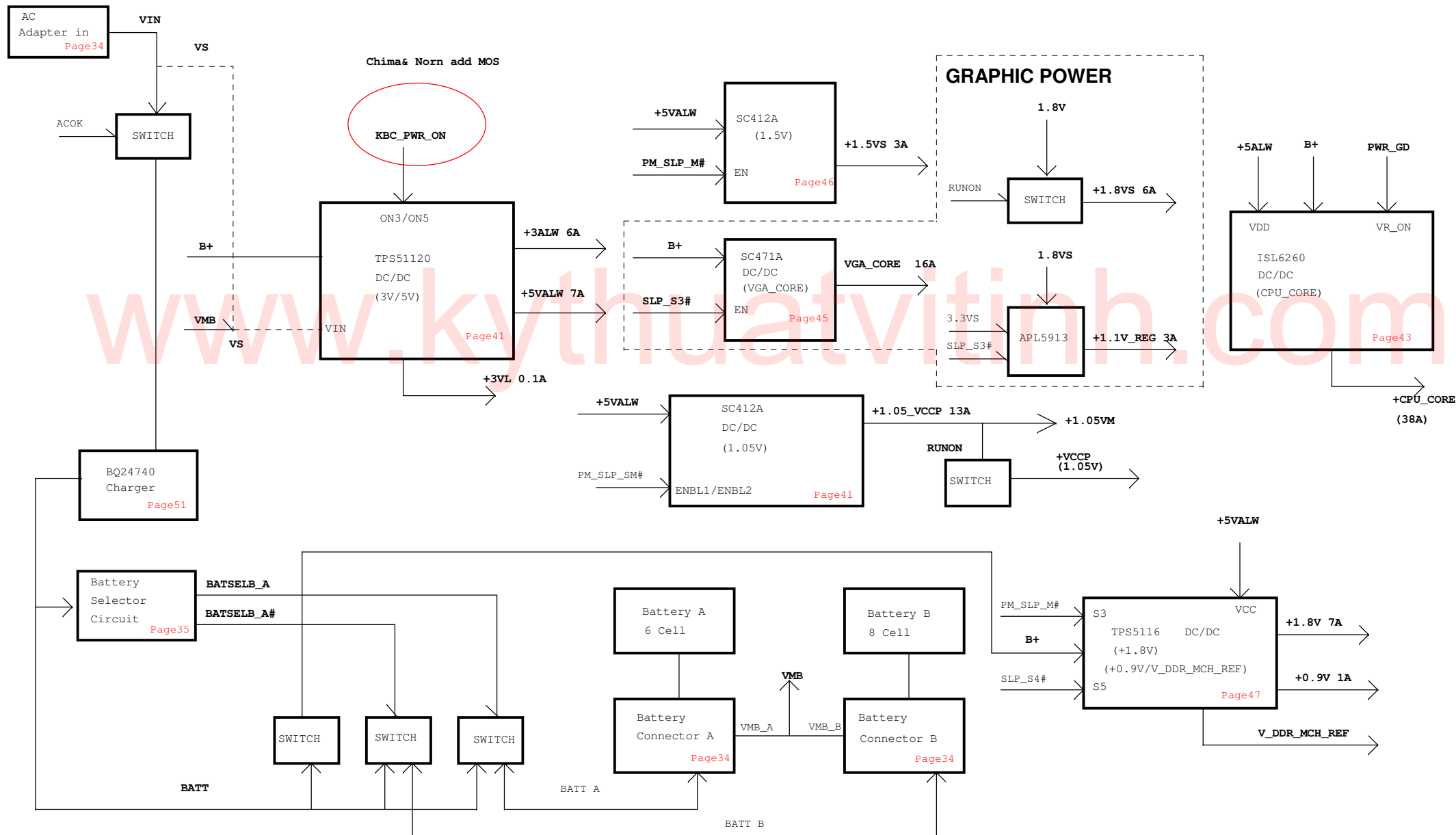


B+ DCBATOUT_SC412A_2









<Variant Name>

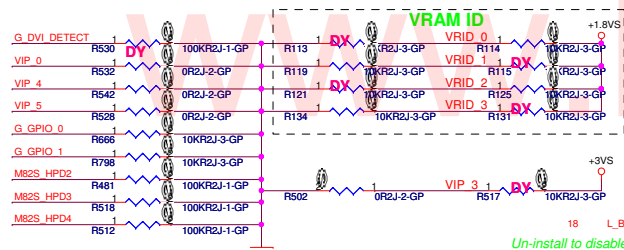
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Power Block Diagram	
Size A3	Document Number KARIA - DISCRETE
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CONFIGURATION STRAPS 0 = DON'T INSTALL RES 1 = INSTALL 10K RES NA = NOT APPLICABLE			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M82-SCE
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO (M8x)	1
BIF_GEN2_EN_A	GPIO5	ALLOW EITHER PCIE 2.50T/s OR 5GT/s OPERATION	1
ROM ID CFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X X
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA
VIP_DEVICE_STRAP_ENA	VSYN	IGNORE VIP DEVICE STRAPS	0
BIF_VGA_DIS	PSYN	VGA ENABLED	0
BIF_HDMI_EN	HSYN	HDMI ENABLE	1

VRID_[3..0]

VRID_[3..0]	00 00	01 01	10	11
00 --> 8M*32				00 --> Qimonda
01 --> 16M*32				01 --> Samsung
10 --> 32M*32				
11 --> 64M*32				

VRAM Configuration	Install Resistors
Samsung 16x32MB	R134, R125, R119, R114
Samsung 32x32MB	R131, R121, R119, R114
Qimonda 16x32MB	R134, R125, R119, R113
Qimonda 32x32MB	R131, R121, R119, R113



Aperture Config PIN	M82SCE GPIO	Strapping Resistor	64MB VRAM	128MB VRAM	256MB VRAM
CONFIG 0	GPIO_11	R597	0	0	1
CONFIG 1	GPIO_12	R831	1	0	0
CONFIG 2	GPIO_13	R832	0	0	0
CONFIG 3	GPIO_9	TP88	X	X	X

