JV50-TR_8VRAM Block Diagram

Project code: 91.4FN01.001
PCB P/N : 48.4FN02.001
REVISION : 09927-1

DDR2 667/800 MHz 16,17
DDR2 667/800 MHz 16,17
667/800MHz
667/800MHz
AMD Caspian CPU S1G3 (35W)
638-Pin uFCPGA638 4,5,6,7
OUT
IN
16X16
G792 35
CRT 20
LCD 19
HDMI 21
16X
CLK GEN. 3
ICS9LPRS480BKLFT 71.09480.A03
RTM880N-796-VB-GRT 71.00880.A03
North Bridge
AMD RS880M
CPU I/F LVDS, CRT I/F
INTEGRATED GRAHPICS
8,9,10
Madison 55,56,57,58,59
VRAM DDR3 60,61,62,63
A-Link 4X4
PCIex1
LAN Giga LAN BCM5784 26
TXFM 27
RJ45 27
New card DY 34
PWR SW DY W83L351YG 28
Mini Card WLAN 33
Mini Card DY 33
INT MIC 30
Line In 30
MIC In 30
INT.SPKR 30
Line Out (SPDIF) 30
Codec ALC888S 28
AZALIA
OP AMP MAX9789 29
South Bridge
AMD SB710
USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
ATA 66/100
ACPI 1.1
LPC I/F
PCI/PCI BRIDGE
11,12,13,14,15
LPC BUS
KBC Winbond WPC773 36
BIOS MXIC MX25L1605 37
LPC DEBUG CONN. 37
Touch Pad 38
INT. KB 36
RJ11
MODEM MDC Card 31
SATA
USB
HDD SATA 22
ODD SATA 23
Mini USB Blue Tooth 24
Finger Printer 31
CardReader Realtek RTS5159 32
MS/MS Pro/xD /MMC/SD 5 in 1 32
USB 2 Port 25
Camera
Daughter Board USB Board 08649-1
Daughter Board LED Board 08651-1
Daughter Board Finger Printer Board 08650-1
Daughter Board Mini sensor Board 08696-1

PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC RT8205A 46	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC TPS51124 47	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(7.5A) 1D2V_S0(4A)

SYSTEM DC/DC RT8209B 48	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(11A)
G9661 49	
5V_S5	1D1V_M92
RT9161 49	
3D3V_S0	2D5V_S0 (200mA)
G957 49	
3D3V_S0	1D5V_S0 (1A)
G9161 49	
3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731 50	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265AHR 45	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

JV50-TR8

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: JV50-TR8 | Rev: -1
Date: Monday, October 05, 2009 | Sheet 1 of 63

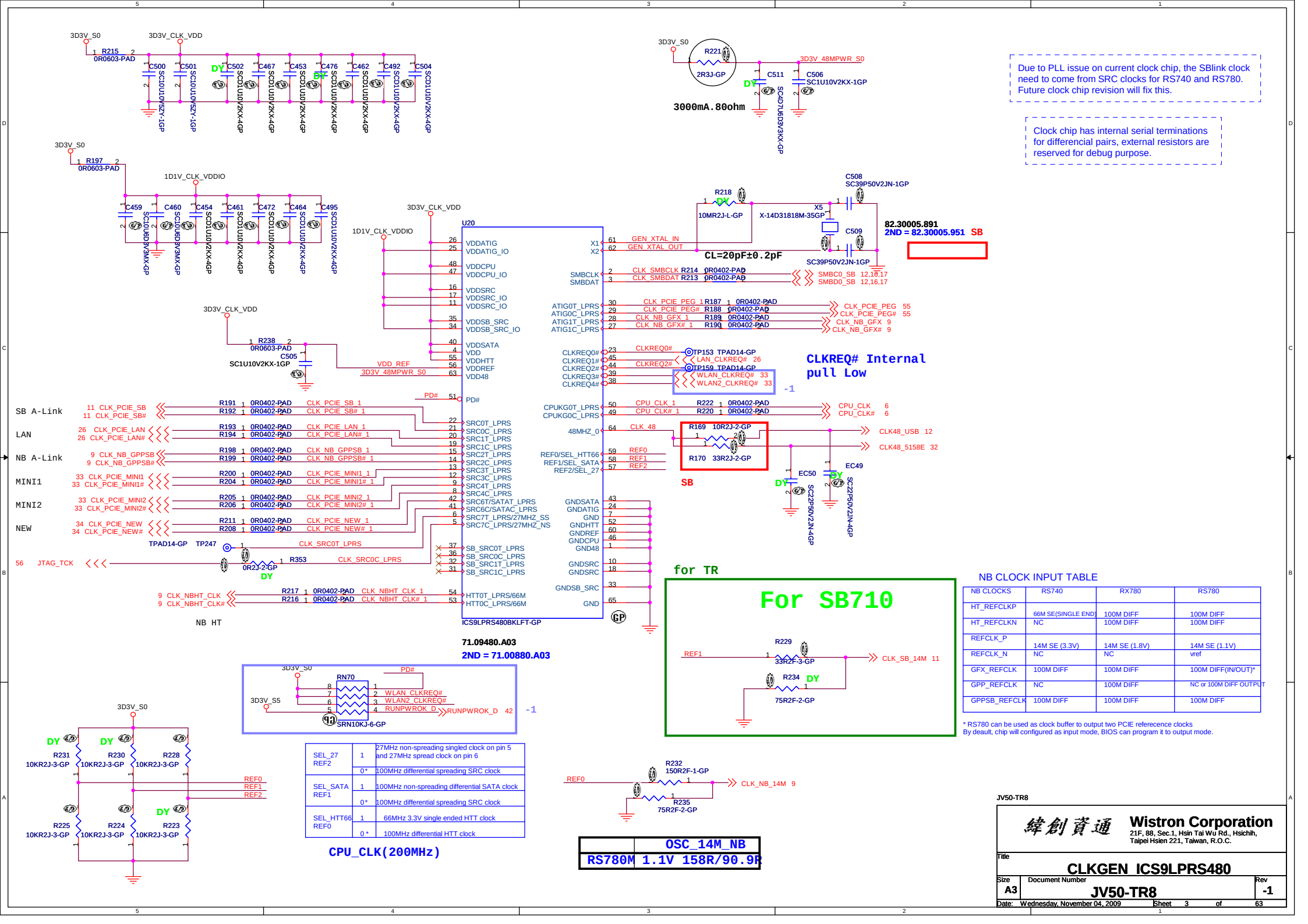
JV50-TR8

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB/PCIE Routing**

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 05, 2009 Sheet 2 of 63



NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

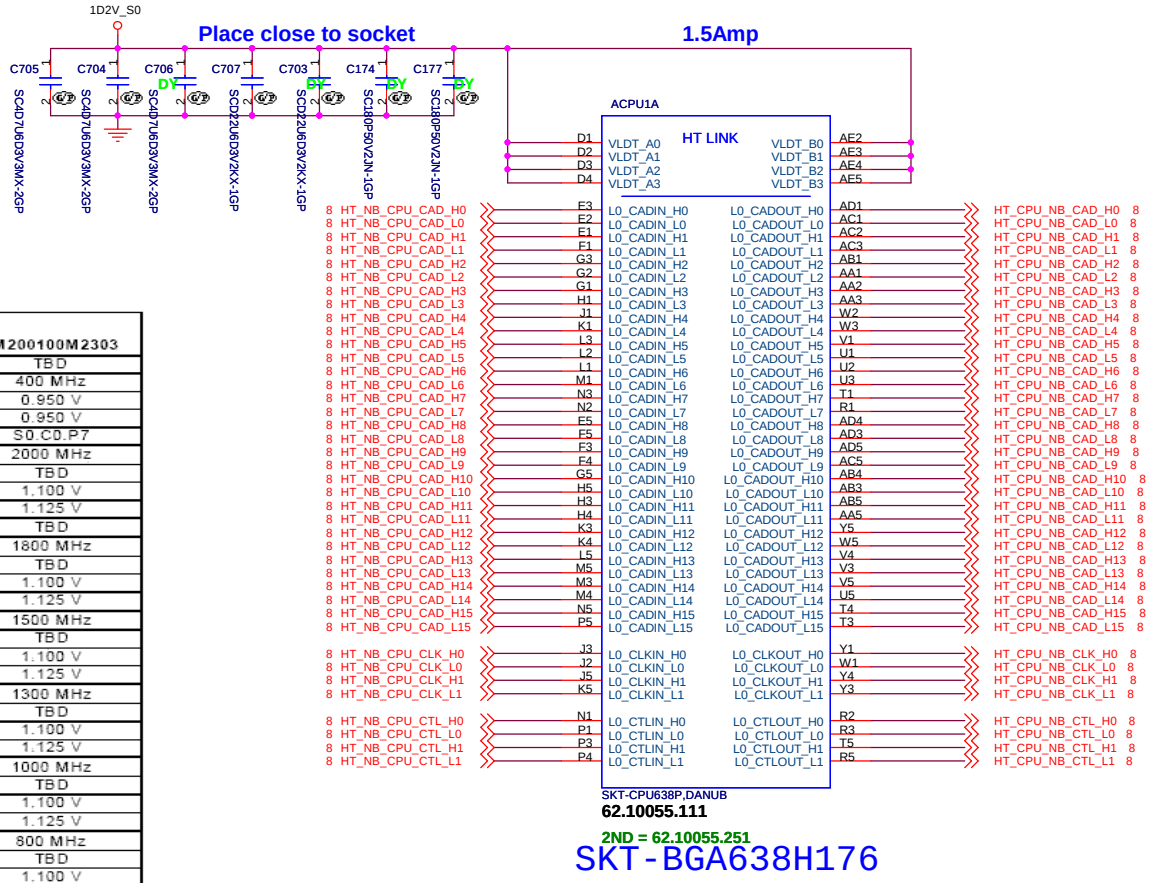
JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN ICS9LPRS480

Size: A3 | Document Number: JV50-TR8 | Rev: -1

Date: Wednesday, November 04, 2009 | Sheet 3 of 63



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

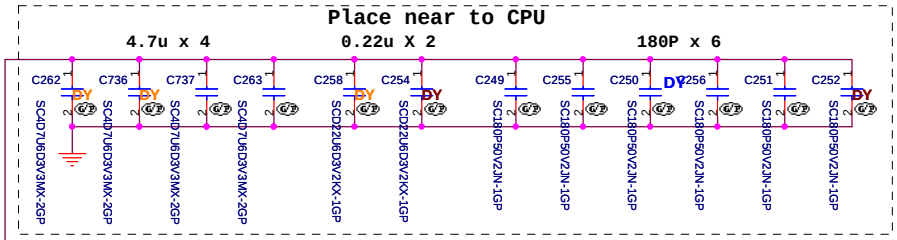
JV50-TR8

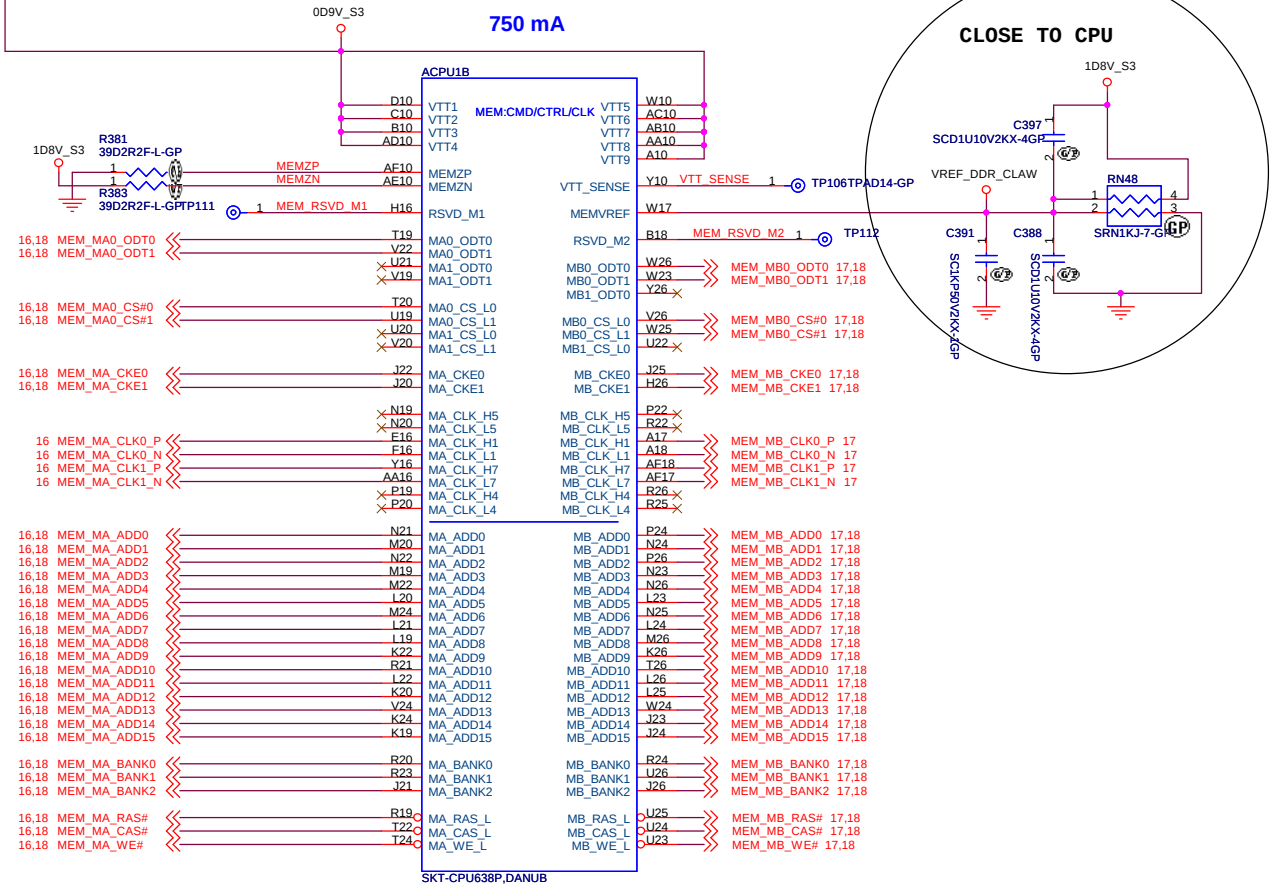
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

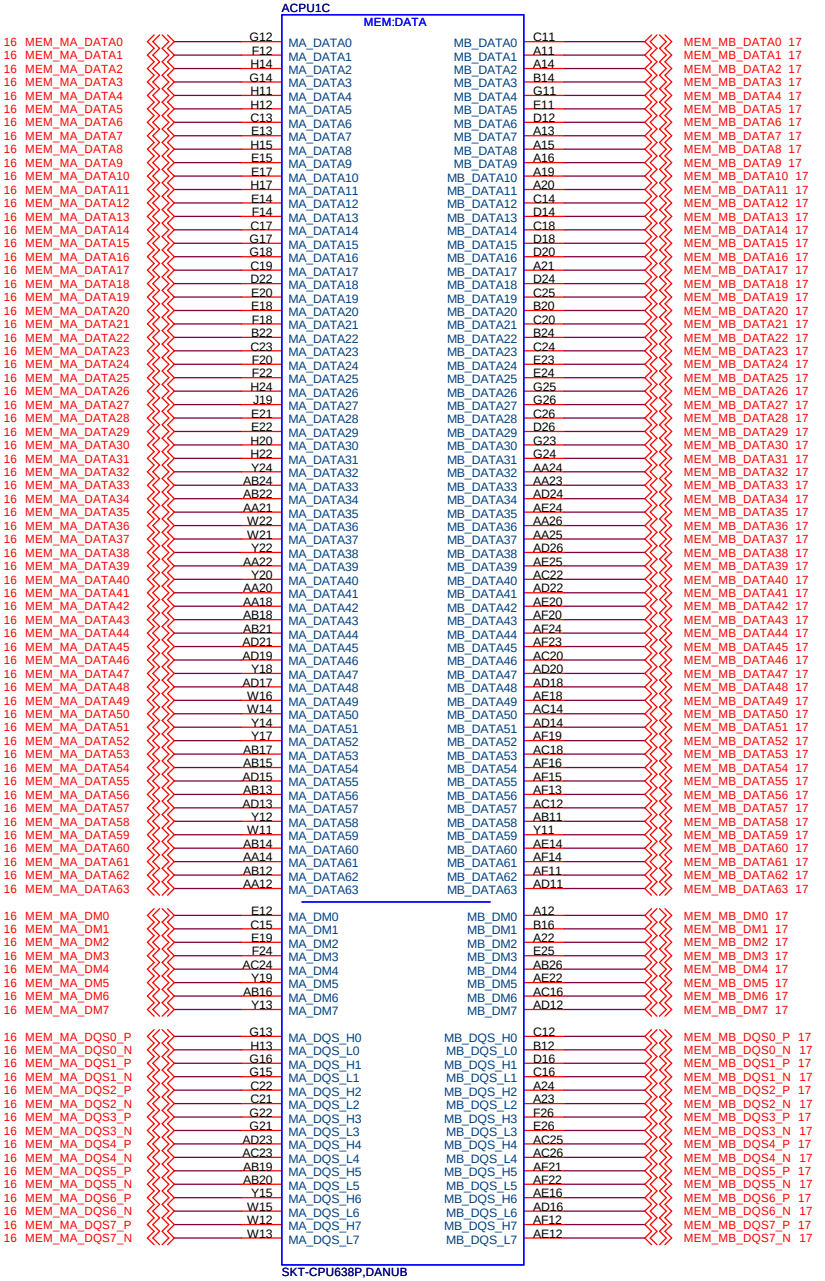
Title: CPU_HT_LINK I/F (1/4)

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 26, 2009 Sheet 4 of 63







62.10055.111

JV50-TR8

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU_DDR_(2/4)		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 5 of 63	

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

Cloce To CPU

for TR

for TR

For HDT DBG

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

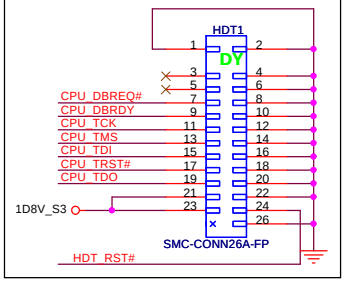
Near CPU PIN

-1_20091021

CPU exceeds to 125℃

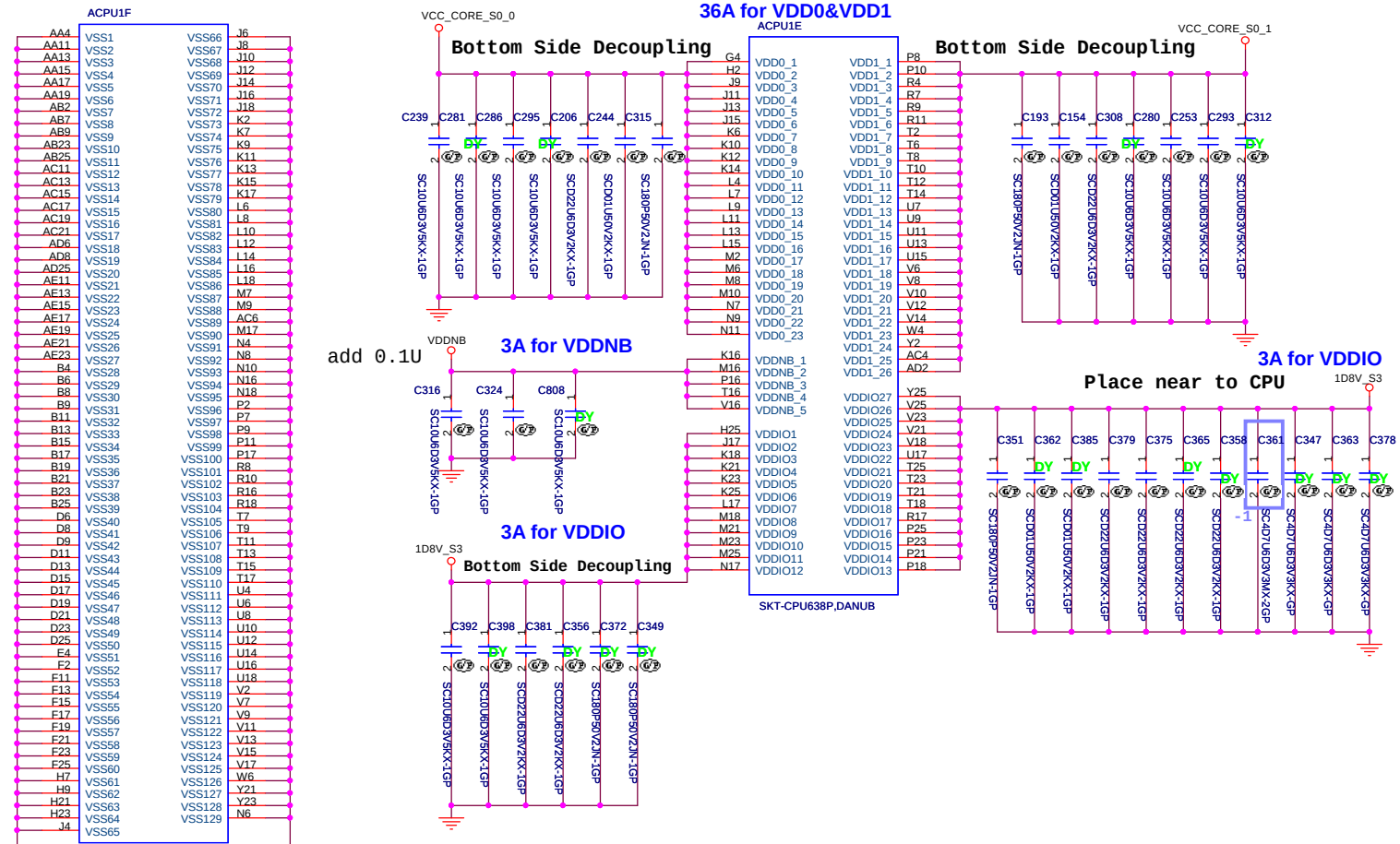
SKT-CPU638P,DANUB

HDT Connectors



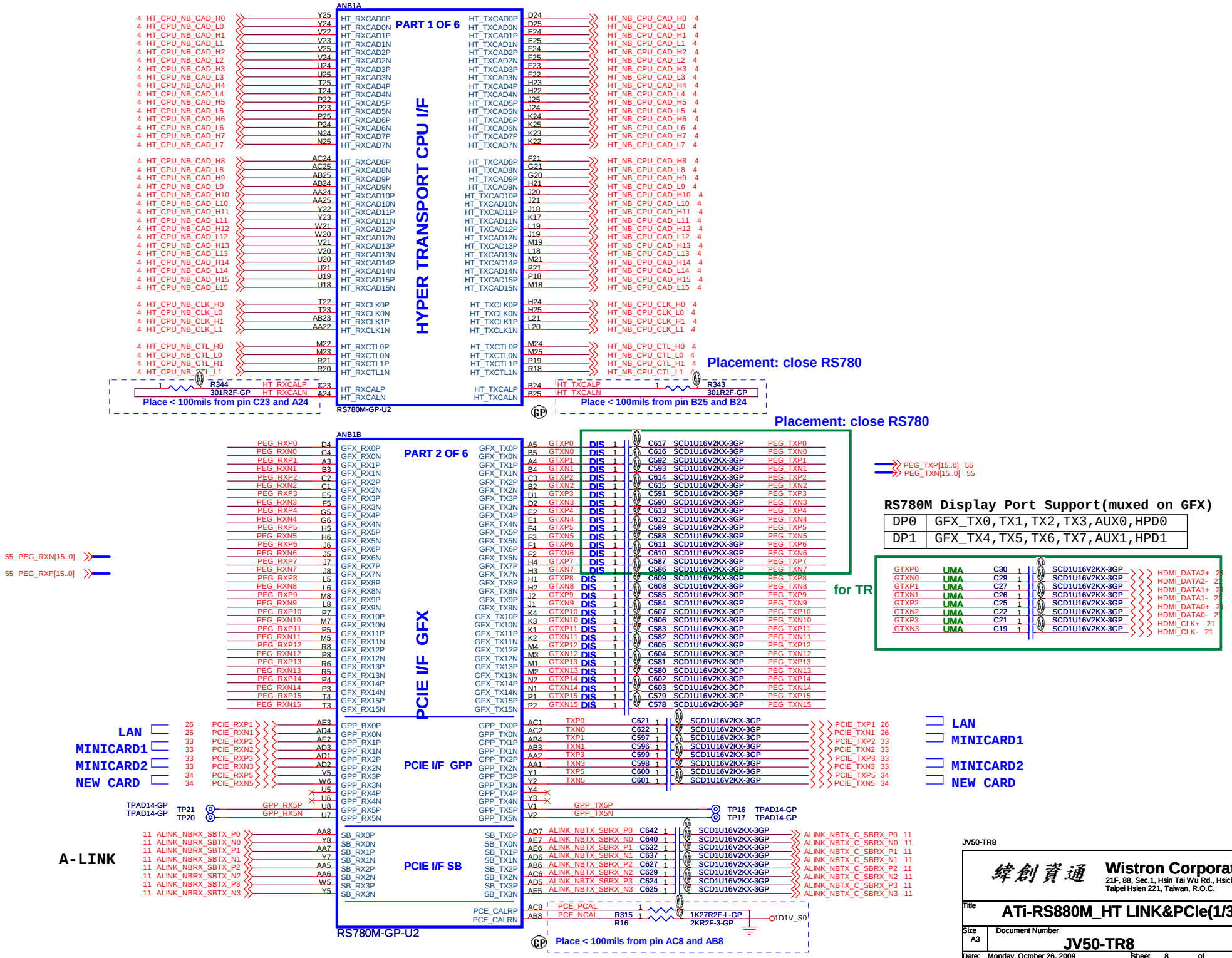
JV50-TR8

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU_Control&Debug_(3/4)	
Size A3	Document Number JV50-TR8	Rev -1
Date: Monday, October 26, 2009	Sheet 6 of 63	

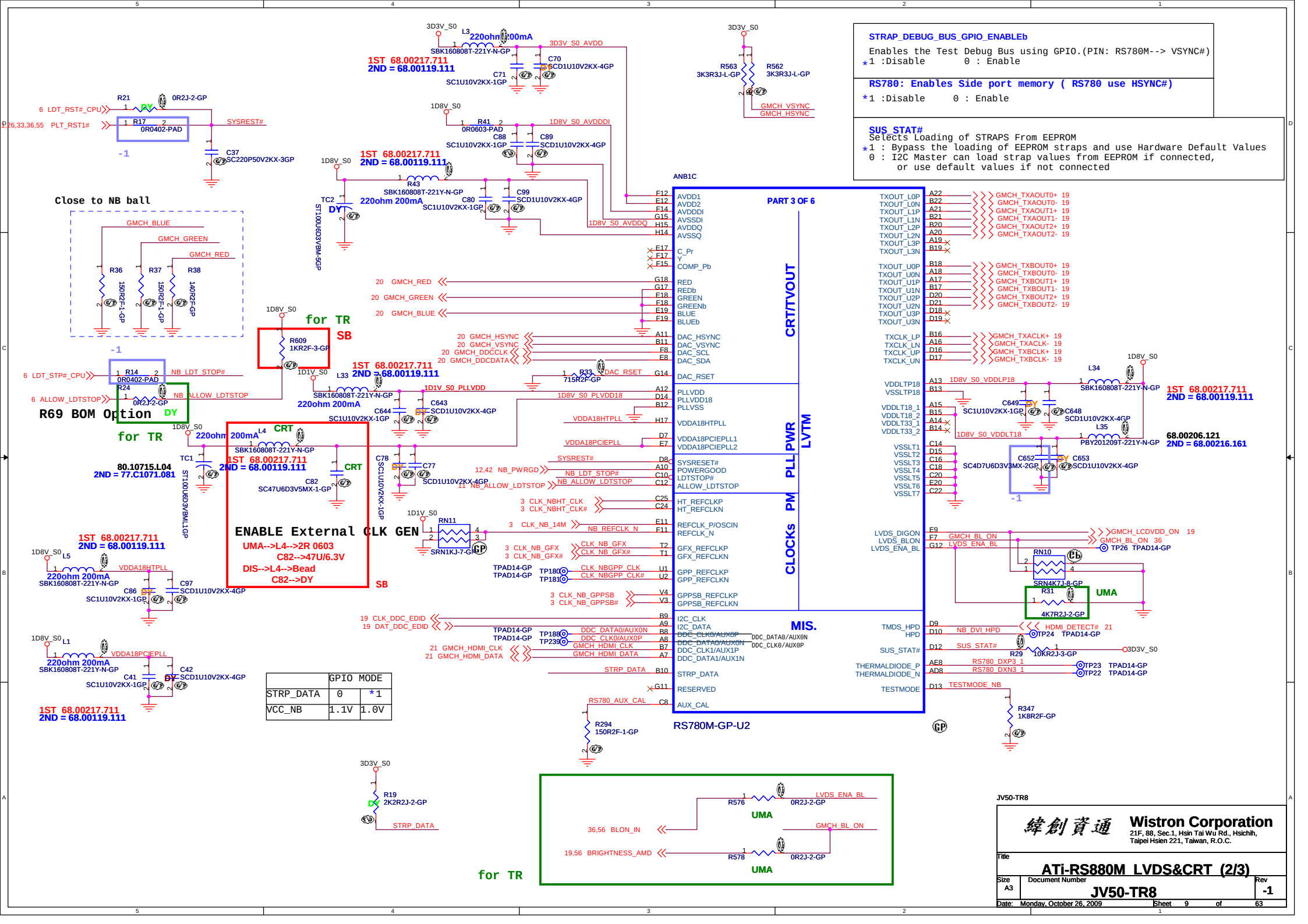


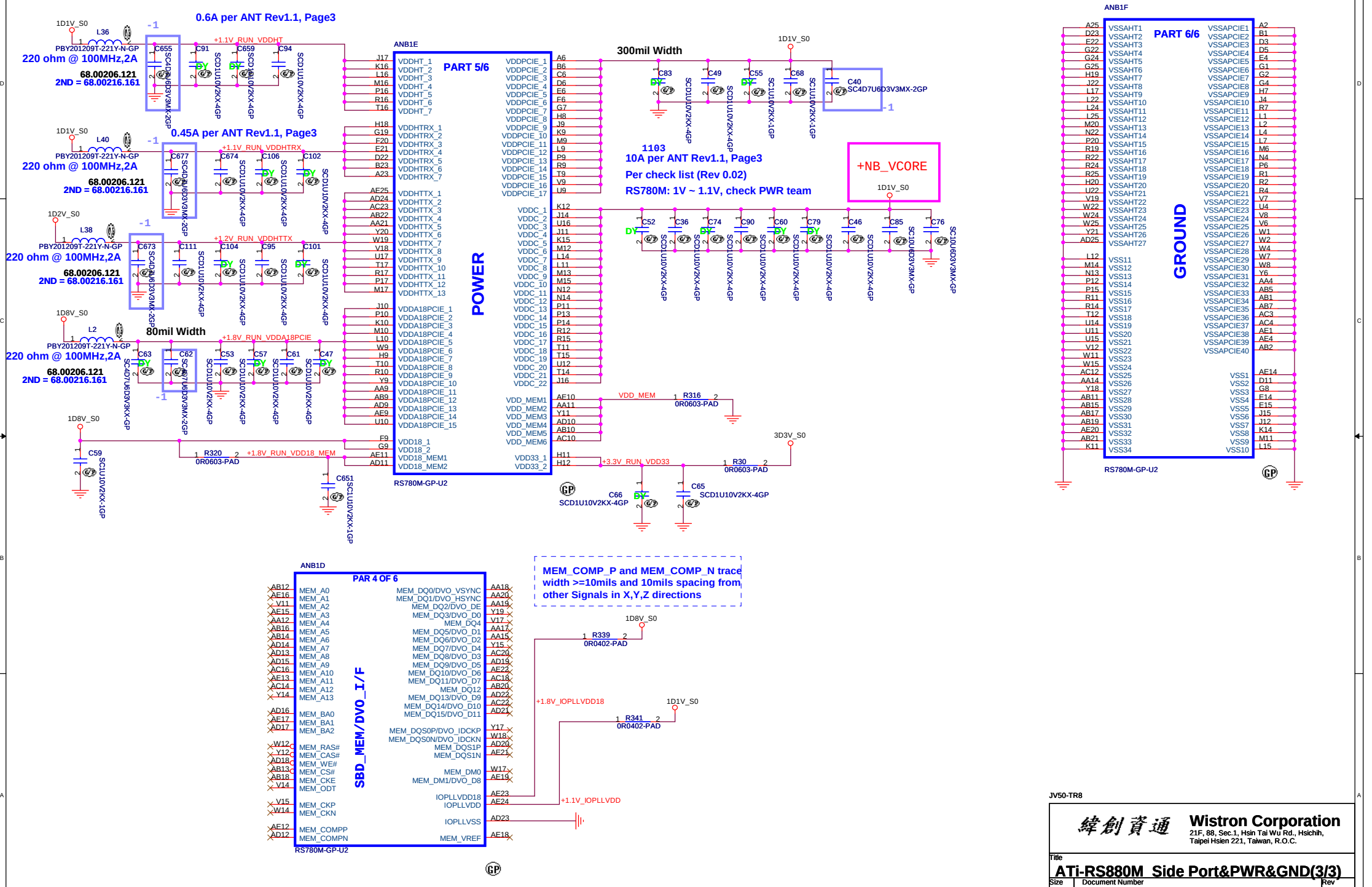
JV50-TR8

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **CPU_Power_(4/4)**		
Size: A3	Document Number: **JV50-TR8**	Rev: **-1**
Date: Monday, October 05, 2009	Sheet 7 of 63	



Wistron Corporation	Title	ATi-RS880M_HT LINK&PCIe(1/3)	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	Size A3	Document Number JV50-TR8	Rev -1
JV50-TR8	Date: Monday, October 26, 2009	Sheet 8 of 63	


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
Close to NB ball
R69 BOM Option
for TR
ENABLE External CLK GEN
UMA-->L4-->2R 0603
C82-->47U/6.3V
DIS-->L4-->Bead
C82-->DY
ANB1C
PART 3 OF 6
CRT/TVOUT
PLL/PWR
LVTM
CLOCKs
PM
MIS.
RS780M-GP-U2
GPIO MODE
STRP_DATA 0 *1
VCC_NB 1.1V 1.0V
for TR
UMA
JV50-TR8
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS880M LVDS&CRT (2/3)
Size A3
Document Number JV50-TR8
Rev -1
Date: Monday, October 26, 2009
Sheet 9 of 63



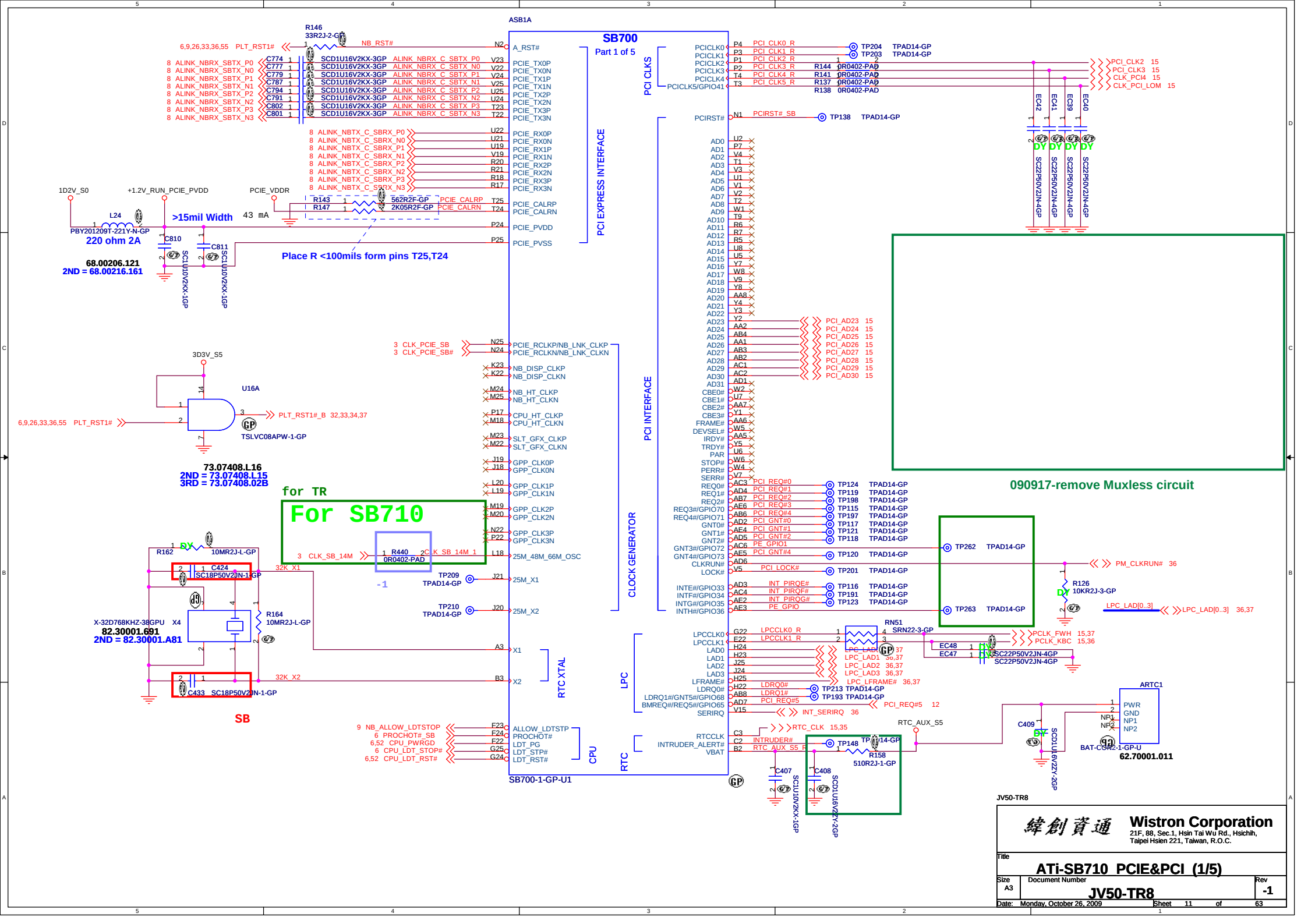
JV50-TR8

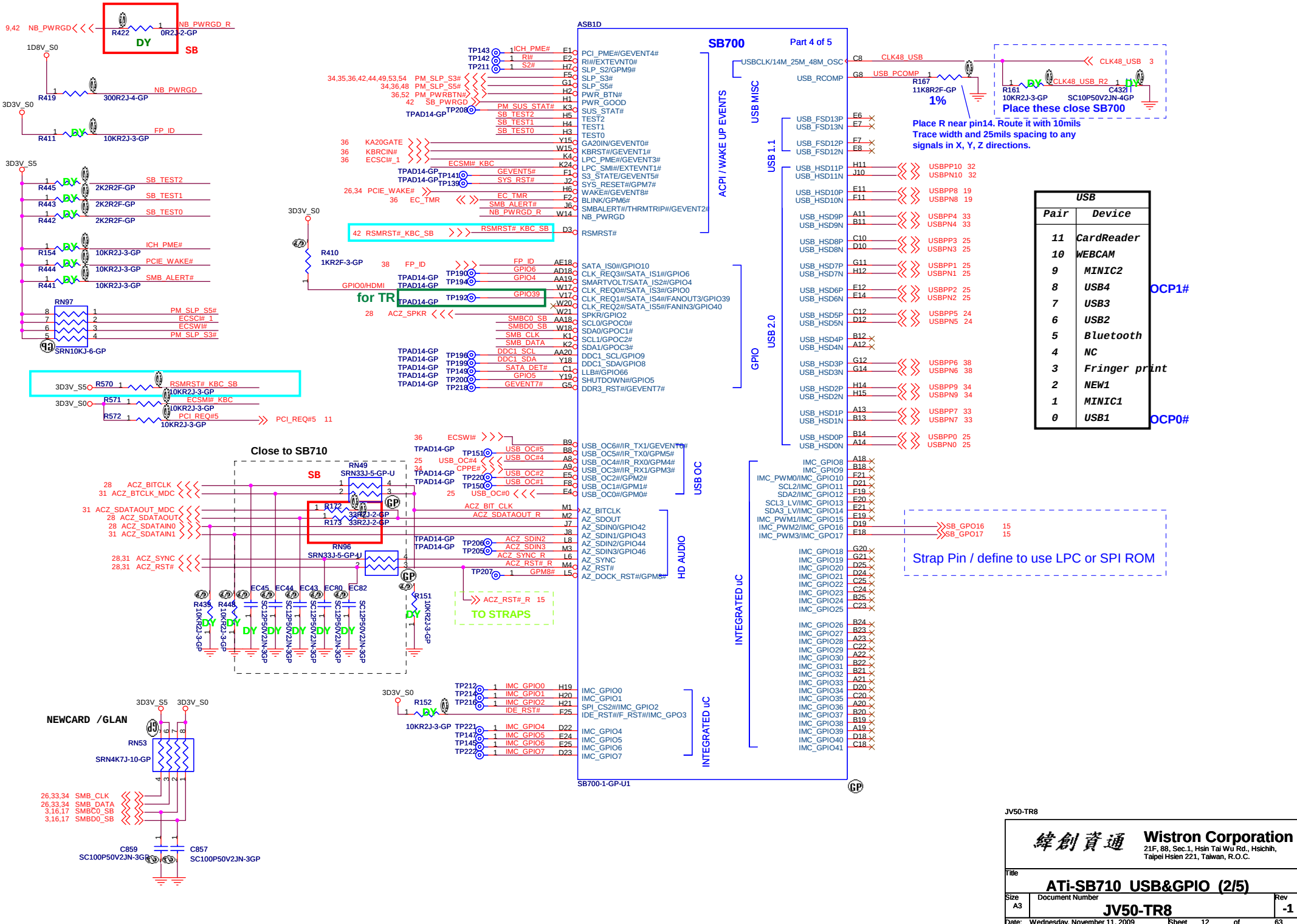
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS880M_Side Port&PWR&GND(3/3)

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 05, 2009 Sheet 10 of 63


SB700
Part 1 of 5
ASB1A
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
SB700-1-GP-U1
R146
33R2J-2-GP
NB_RST#
PLT_RST1#
ALINK_NBRX_SBTX_P0
ALINK_NBRX_SBTX_N0
ALINK_NBRX_SBTX_P1
ALINK_NBRX_SBTX_N1
ALINK_NBRX_SBTX_P2
ALINK_NBRX_SBTX_N2
ALINK_NBRX_SBTX_P3
ALINK_NBRX_SBTX_N3
SCD1U16V2KX-3GP
ALINK_NBTX_C_SBRX_P0
ALINK_NBTX_C_SBRX_N0
ALINK_NBTX_C_SBRX_P1
ALINK_NBTX_C_SBRX_N1
ALINK_NBTX_C_SBRX_P2
ALINK_NBTX_C_SBRX_N2
ALINK_NBTX_C_SBRX_P3
ALINK_NBTX_C_SBRX_N3
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
1D2V_S0
+1.2V_RUN_PCIE_PVDD
PCIE_VDDR
L24
PBY201209T-221Y-N-GP
220 ohm 2A
>15mil Width
43 mA
68.00206.121
2ND = 68.00216.161
R143
562R2F-GP
R147
2K05R2F-GP
PCIE_CALRP
PCIE_CALRN
Place R <100mils form pins T25,T24
PCIE_PVDD
PCIE_PVSS
3D3V_S5
U16A
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
CLK_PCIE_SB
CLK_PCIE_SB#
PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN
NB_DISP_CLKP
NB_DISP_CLKN
NB_HT_CLKP
NB_HT_CLKN
CPU_HT_CLKP
CPU_HT_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
for TR
For SB710
CLK_SB_14M
R440
0R0402-PAD
CLK_SB_14M_1
25M_48M_66M_OSC
25M_X1
25M_X2
X1
X2
R162
10MR2J-L-GP
C424
SC18P50V2JN-1-GP
32K_X1
X-32D768KHZ-38GPU
X4
82.30001.691
2ND = 82.30001.A81
R164
10MR2J-L-GP
32K_X2
C433
SC18P50V2JN-1-GP
SB
PCICLK0
PCICLK1
PCICLK2
PCICLK3
PCICLK4
PCICLK5/GPIO41
PCI_CLK0_R
PCI_CLK1_R
PCI_CLK2_R
PCI_CLK3_R
PCI_CLK4_R
PCI_CLK5_R
TP204
TP203
R144
R141
R137
R138
0R0402-PAD
PCI_CLK2 15
PCI_CLK3 15
CLK_PCI4 15
CLK_PCI_LOM 15
EC42
EC41
EC39
EC40
SC22P50V2JN-4GP
PCIRST#
PCIRST#_SB
TP138
TPAD14-GP
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
PCI_AD23 15
PCI_AD24 15
PCI_AD25 15
PCI_AD26 15
PCI_AD27 15
PCI_AD28 15
PCI_AD29 15
PCI_AD30 15
CBE0#
CBE1#
CBE2#
CBE3#
FRAME#
DEVSEL#
IRDY#
TRDY#
PAR
STOP#
PERR#
SERR#
REQ0#
REQ1#
REQ2#
REQ3#/GPIO70
REQ4#/GPIO71
GNT0#
GNT1#
GNT2#
GNT3#/GPIO72
GNT4#/GPIO73
CLKRUN#
LOCK#
PCI_REQ#0
PCI_REQ#1
PCI_REQ#2
PCI_REQ#3
PCI_REQ#4
PCI_GNT#0
PCI_GNT#1
PCI_GNT#2
PE_GPIO1
PCI_GNT#4
PCI_LOCK#
TP124
TP119
TP198
TP115
TP197
TP117
TP121
TP118
TP120
TP201
TP262
TP263
TPAD14-GP
090917-remove Muxless circuit
PM_CLKRUN# 36
R126
10KR2J-3-GP
LPC_LAD[0..3]
INTE#/GPIO33
INTF#/GPIO34
INTG#/GPIO35
INTH#/GPIO36
INT_PIRQE#
INT_PIRQF#
INT_PIRQG#
PE_GPIO
TP116
TP191
TP123
LPCCLK0
LPCCLK1
LAD0
LAD1
LAD2
LAD3
LFRAME#
LDRQ0#
LDRQ1#/GNT5#/GPIO68
BMREQ#/REQ5#/GPIO65
SERIRQ
LPCCLK0_R
LPCCLK1_R
RN51
SRN22-3-GP
PCLK_FWH 15,37
PCLK_KBC 15,36
EC48
EC47
SC22P50V2JN-4GP
LDRQ1#
PCI_REQ#5
TP213
TP193
INT_SERIRQ 36
RTCCLK
INTRUDER_ALERT#
VBAT
RTC_CLK 15,35
RTC_AUX_S5
TP148
R158
510R2J-1-GP
C407
C408
SC1U10V2KX-1GP
SCD1U16V2ZY-2GP
ARTC1
BAT-CON2-1-GP-U
62.70001.011
C409
SCD1U16V2ZY-2GP
9 NB_ALLOW_LDTSTOP
6 PROCHOT#_SB
6,52 CPU_PWRGD
6 CPU_LDT_STOP#
6,52 CPU_LDT_RST#
ALLOW_LDTSTP
PROCHOT#
LDT_PG
LDT_STP#
LDT_RST#
JV50-TR8
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB710 PCIE&PCI (1/5)
Size
A3
Document Number
JV50-TR8
Rev
-1
Date: Monday, October 26, 2009
Sheet 11 of 63


SB700
Part 4 of 5
ASB1D
SB700-1-GP-U1
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
INTEGRATED uC
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#
SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPIO16
IMC_PWM3/IMC_GPO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41
CLK48_USB
USB_PCOMP
R167 11K8R2F-GP 1%
Place R near pin14. Route it with 10mils
Trace width and 25mils spacing to any
signals in X, Y, Z directions.
CLK48_USB_R2
R161 10KR2J-3-GP
C432 SC10P50V2JN-4GP
Place these close SB700
USB
Pair Device
11 CardReader
10 WEBCAM
9 MINIC2
8 USB4
7 USB3
6 USB2
5 Bluetooth
4 NC
3 Fringer print
2 NEW1
1 MINIC1
0 USB1
OCP1#
OCP0#
USBPP10 32
USBPN10 32
USBPP8 19
USBPN8 19
USBPP4 33
USBPN4 33
USBPP3 25
USBPN3 25
USBPP1 25
USBPN1 25
USBPP2 25
USBPN2 25
USBPP5 24
USBPN5 24
USBPP6 38
USBPN6 38
USBPP9 34
USBPN9 34
USBPP7 33
USBPN7 33
USBPP0 25
USBPN0 25
SB_GPO16 15
SB_GPO17 15
Strap Pin / define to use LPC or SPI ROM
TO STRAPS
ACZ_RST#_R 15
Close to SB710
SB
RN49 SRN33J-5-GP-U
RN96 SRN33J-5-GP-U
R172 33R2J-2-GP
R173 33R2J-2-GP
R439 10KR2J-3-GP
R448 10KR2J-3-GP
R151 10KR2J-3-GP
R152 10KR2J-3-GP
EC45 EC44 EC43 EC80 EC82
SC12P50V2JN-3GP
NEWCARD /GLAN
RN53 SRN4K7J-10-GP
C859 SC100P50V2JN-3GP
C857 SC100P50V2JN-3GP
R410 1KR2F-3-GP
for TR
R422 0R2J-2-GP
R419 300R2J-4-GP
R411 10KR2J-3-GP
R445 2K2R2F-GP
R443 2K2R2F-GP
R442 2K2R2F-GP
R154 10KR2J-3-GP
R444 10KR2J-3-GP
R441 10KR2J-3-GP
RN97 SRN10KJ-6-GP
R570 10KR2J-3-GP
R571 10KR2J-3-GP
R572 10KR2J-3-GP
TP143 TP142 TP211 TP208 TP141 TP139 TP190 TP194 TP192 TP196 TP199 TP149 TP200 TP218 TP151 TP220 TP150 TP206 TP205 TP207 TP212 TP214 TP216 TP221 TP147 TP145 TP222
JV50-TR8
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB710 USB&GPIO (2/5)
Size A3
Document Number JV50-TR8
Rev -1
Date: Wednesday, November 11, 2009
Sheet 12 of 63

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB710

SATA HDD
SATA ODD

SB700
Part 2 of 5

ASB1B

SERIAL ATA
ATA 66/100/133
SPI ROM
SATA PWR
HW MONITOR

SB700-1-GP-U1

Very Close to SB710

1ST 82.30020.851
2ND = 82.30020.791
SB

93 mA

>15mil Width

Dummy CKG select

CLK_ID
(1,0)
ICS: 0,0
SEG: 0,1
RTM: 1,0

Layout connect to Cap then GND

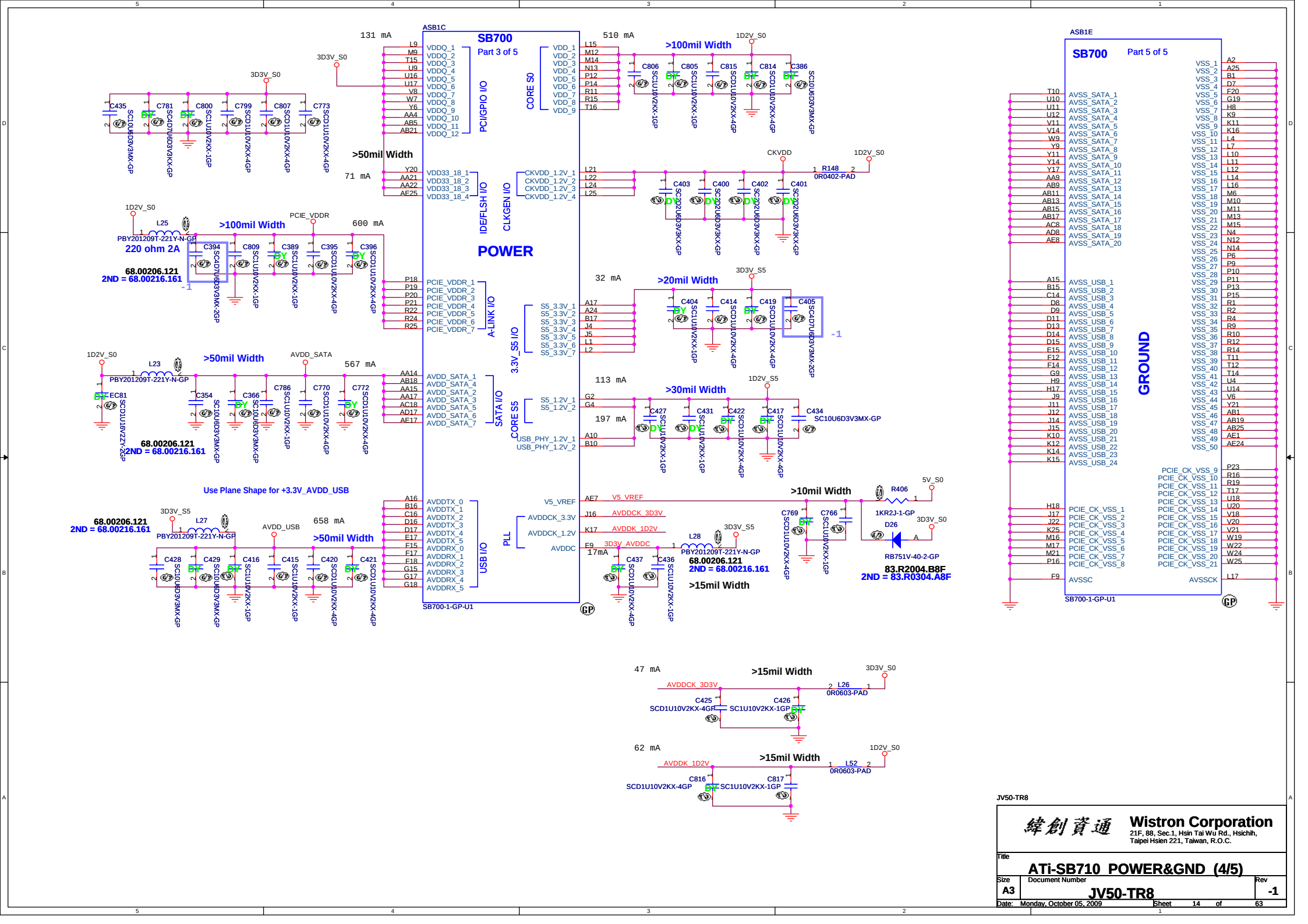
JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB710 SATA-IDE (3/5)

Size: A3 | Document Number: JV50-TR8 | Rev: -1

Date: Monday, October 26, 2009 | Sheet 13 of 63



JV50-TR8

緯創資通	**Wistron Corporation**
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

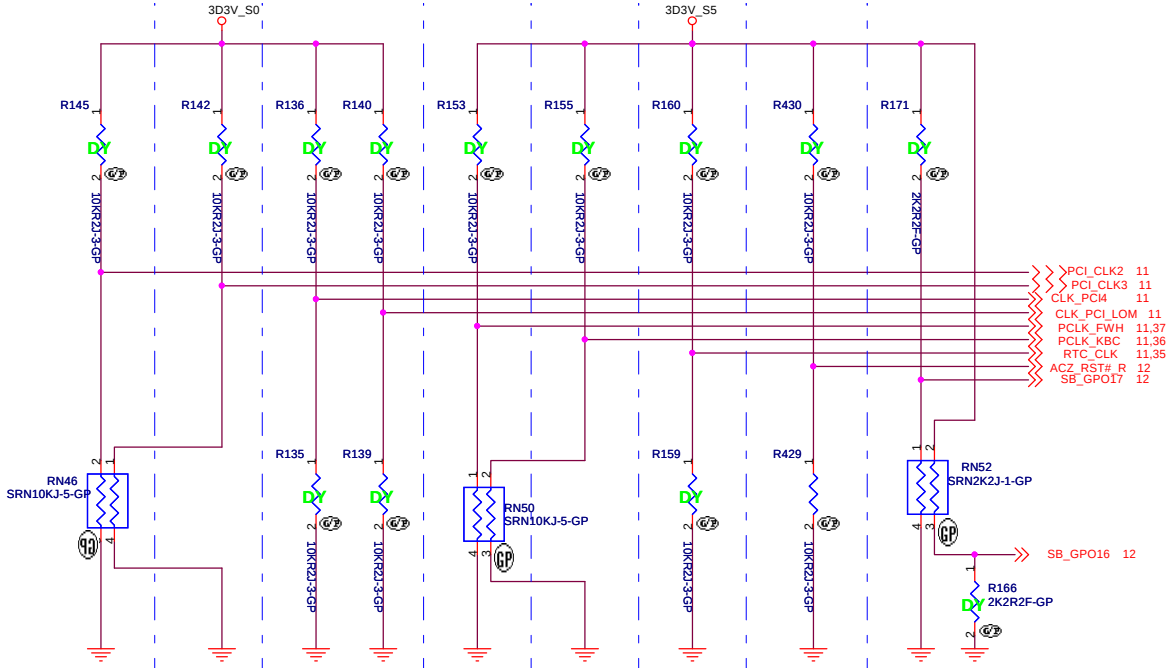
Title: **ATi-SB710 POWER&GND (4/5)**

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 05, 2009 Sheet 14 of 63

REQUIRED STRAPS

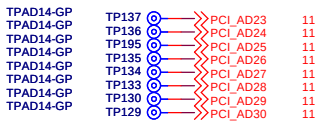
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

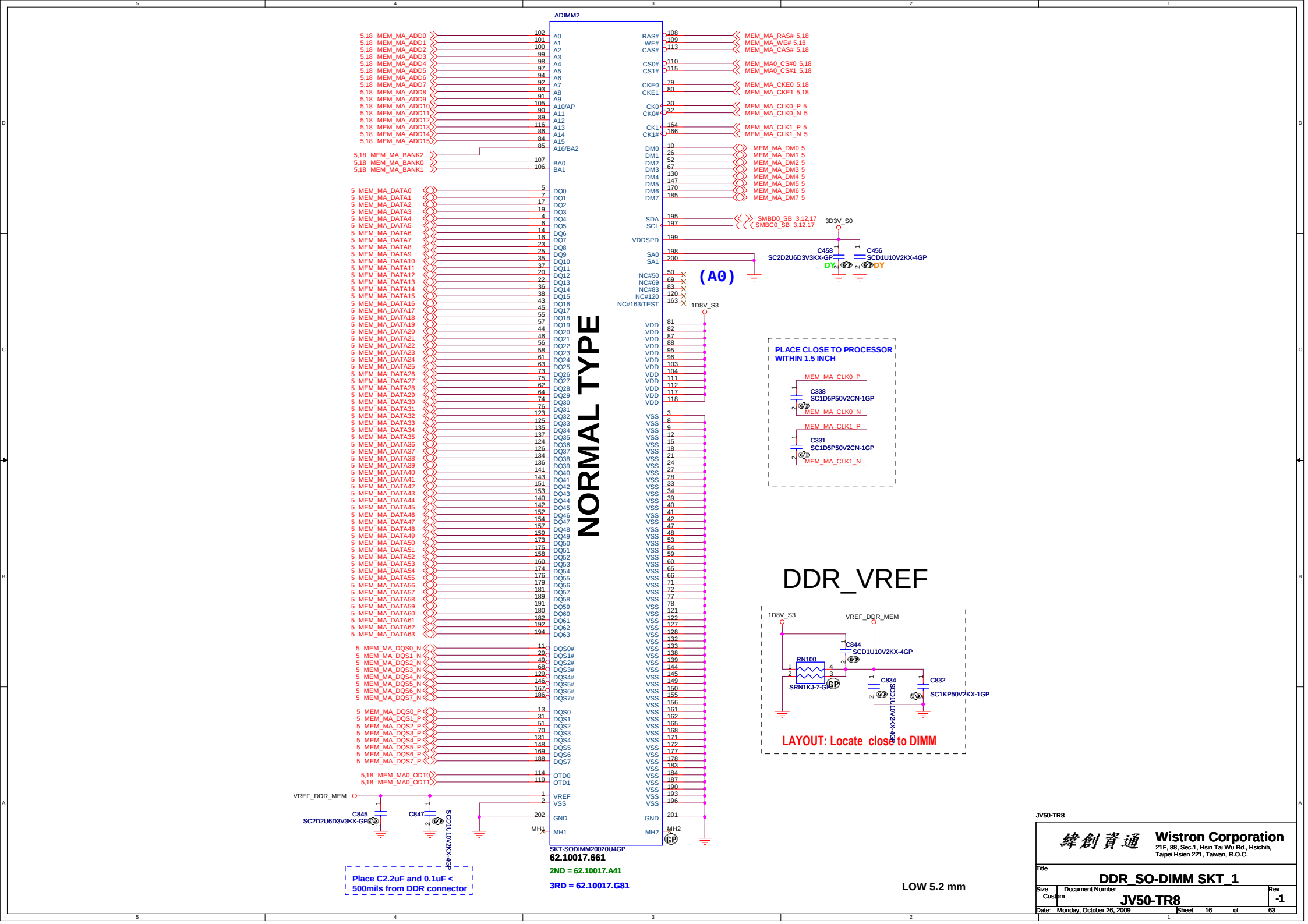
JV50-TR8

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB710 STRAPPING (5/5)

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 26, 2009 Sheet 15 of 63



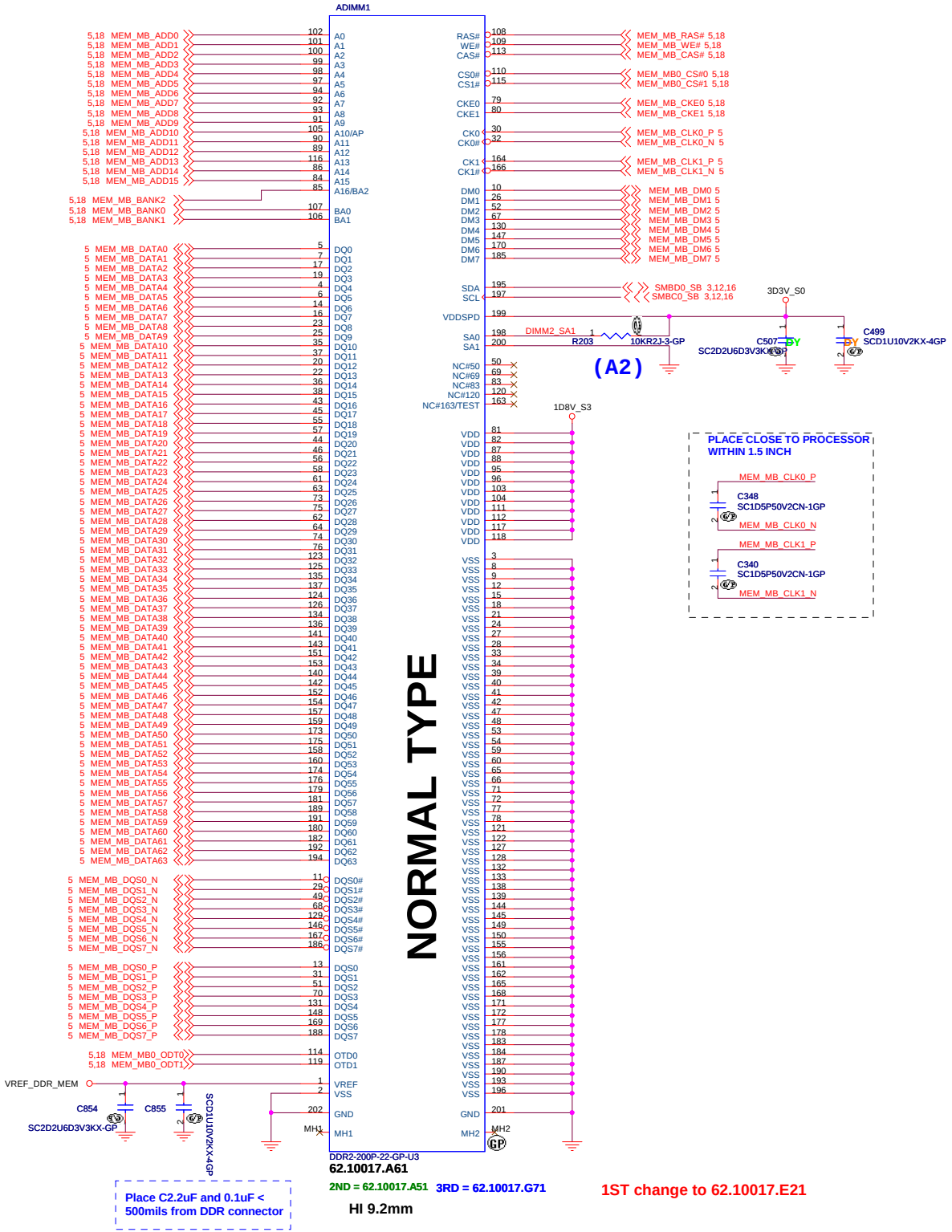
JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_1

Size: Custom | Document Number: JV50-TR8 | Rev: -1

Date: Monday, October 26, 2009 | Sheet 16 of 63



JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

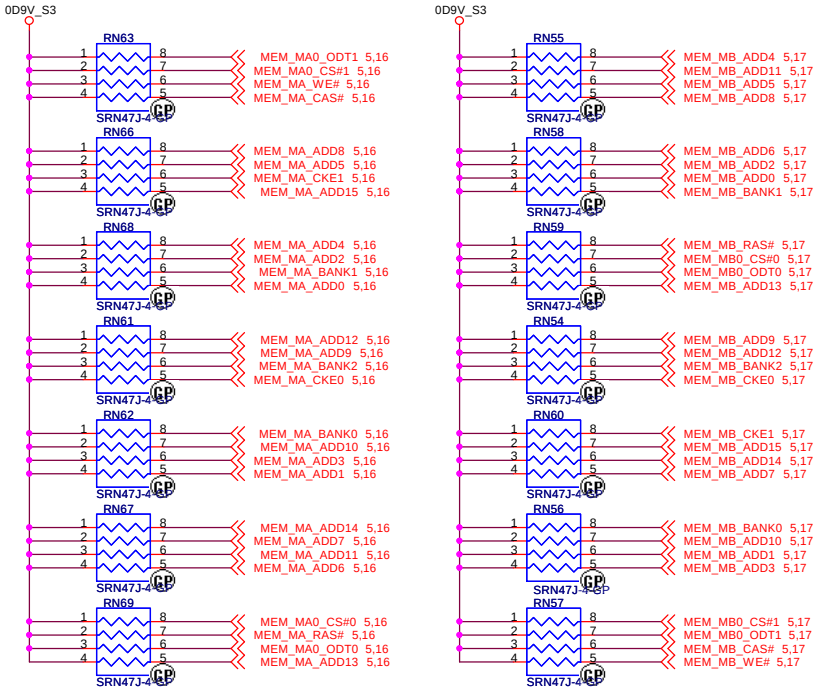
Title: DDR_SO-DIMM SKT_2

Size	Document Number	Rev
Custom	JV50-TR8	-1

Date: Monday, October 26, 2009 Sheet 17 of 63

PARALLEL TERMINATION

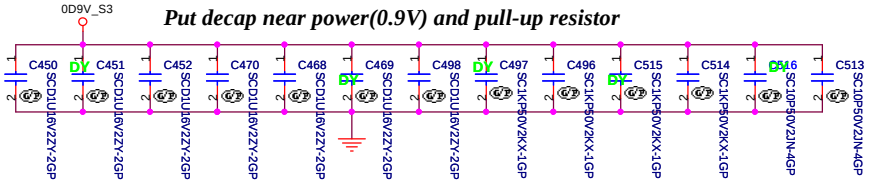
Put decap near power(0.9V) and pull-up resistor



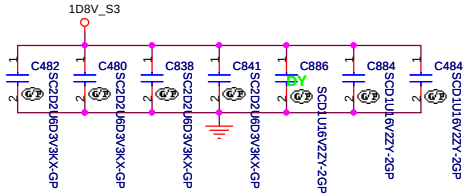
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

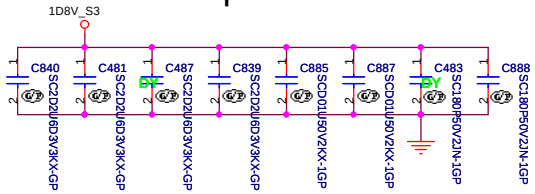


Place these Caps near DM1



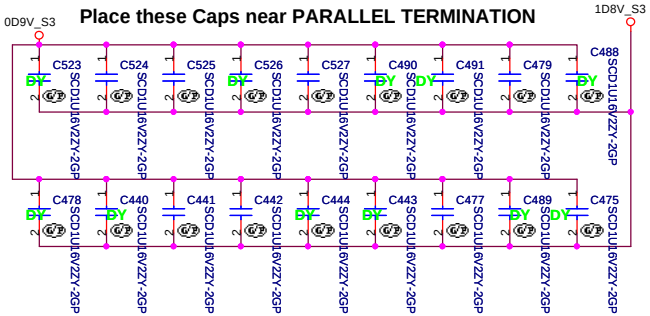
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



JV50-TR8

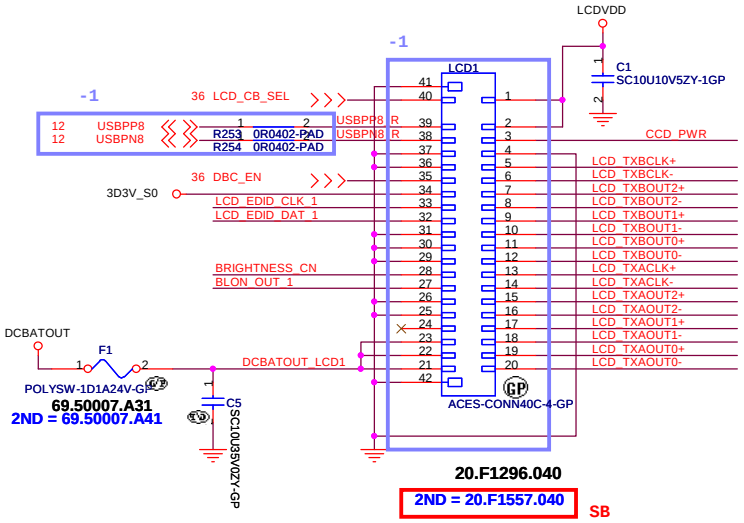
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

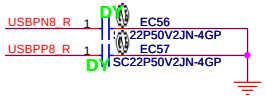
Title: **DDR_DAMPING & TERMINATION**

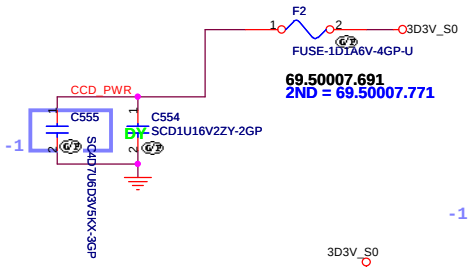
Size	Document Number	Rev
A3	JV50-TR8	-1

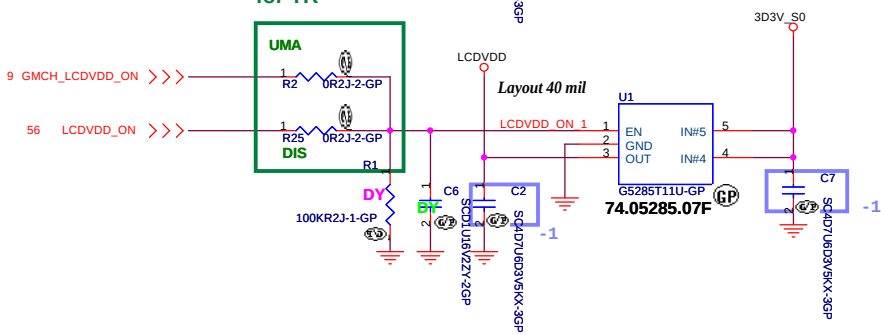
Date: Monday, October 26, 2009 Sheet 18 of 63

LCD/INVERTER/CCD CONN







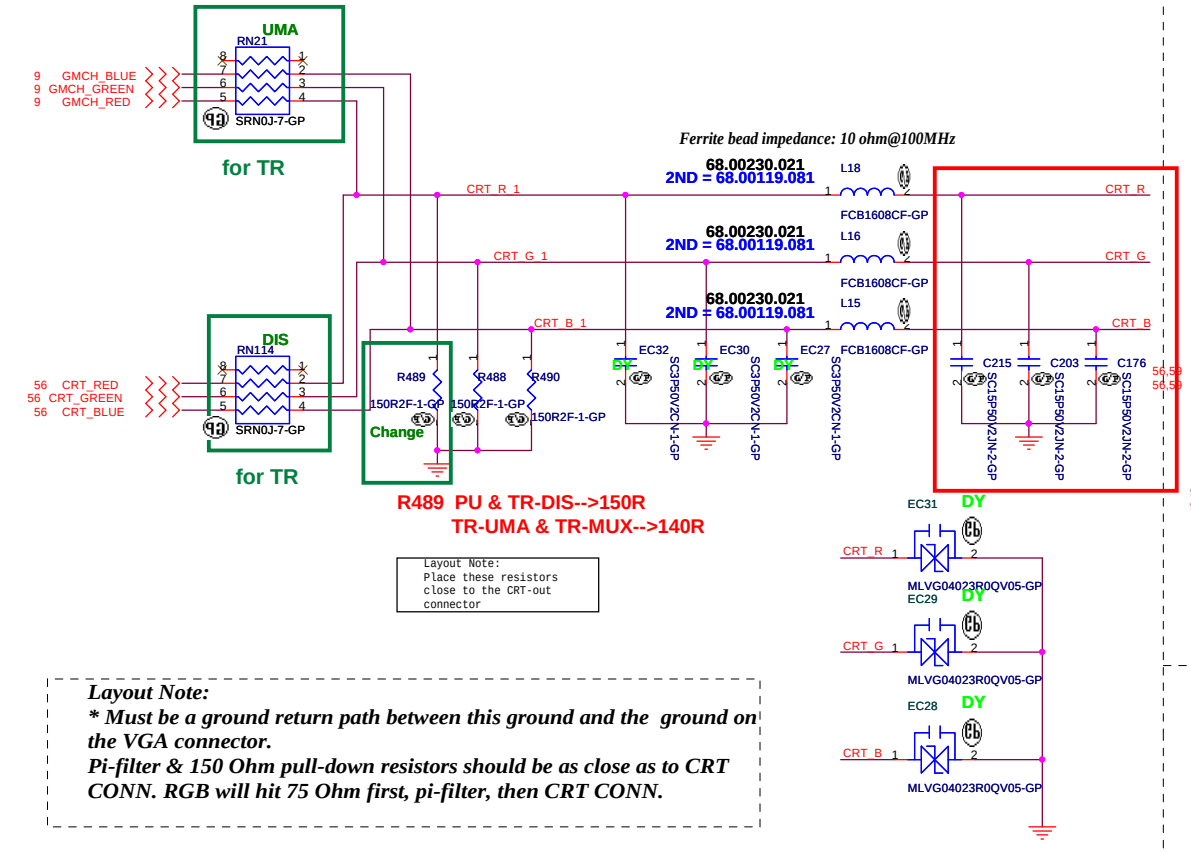


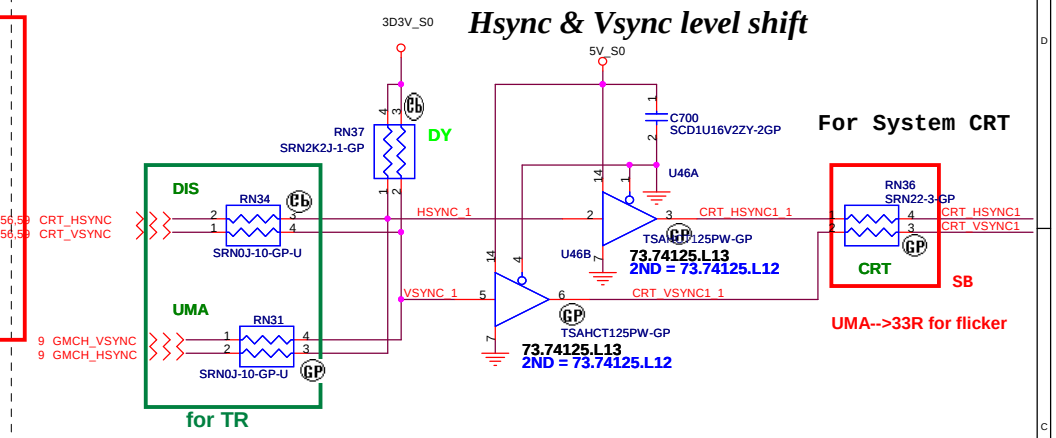
Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

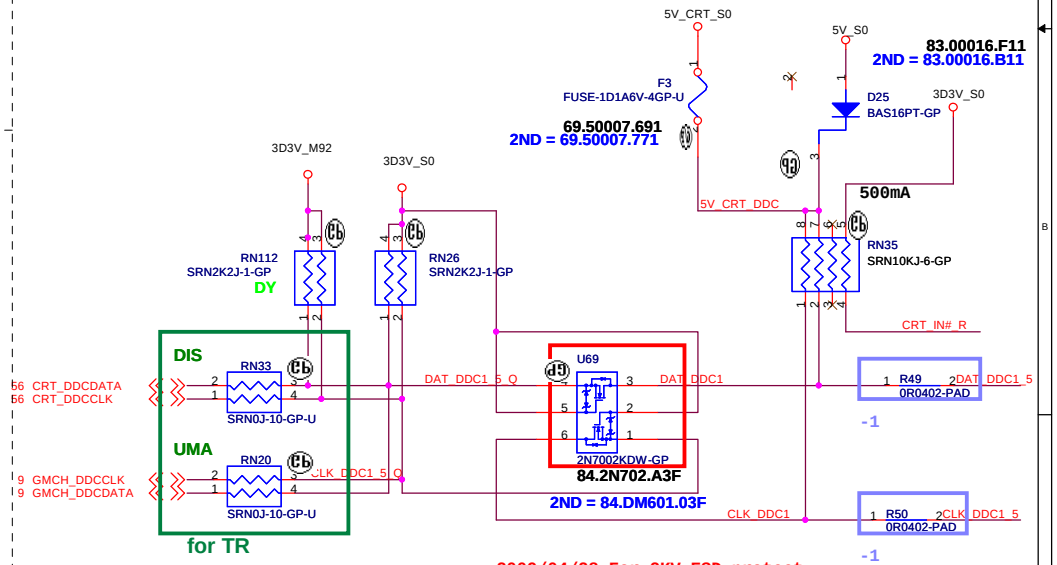
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

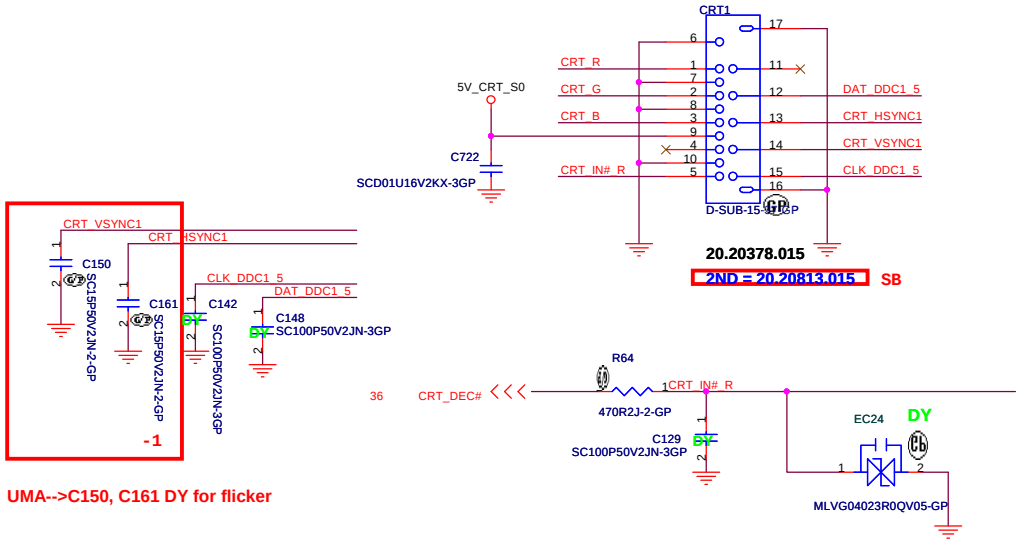
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 19 of 63	









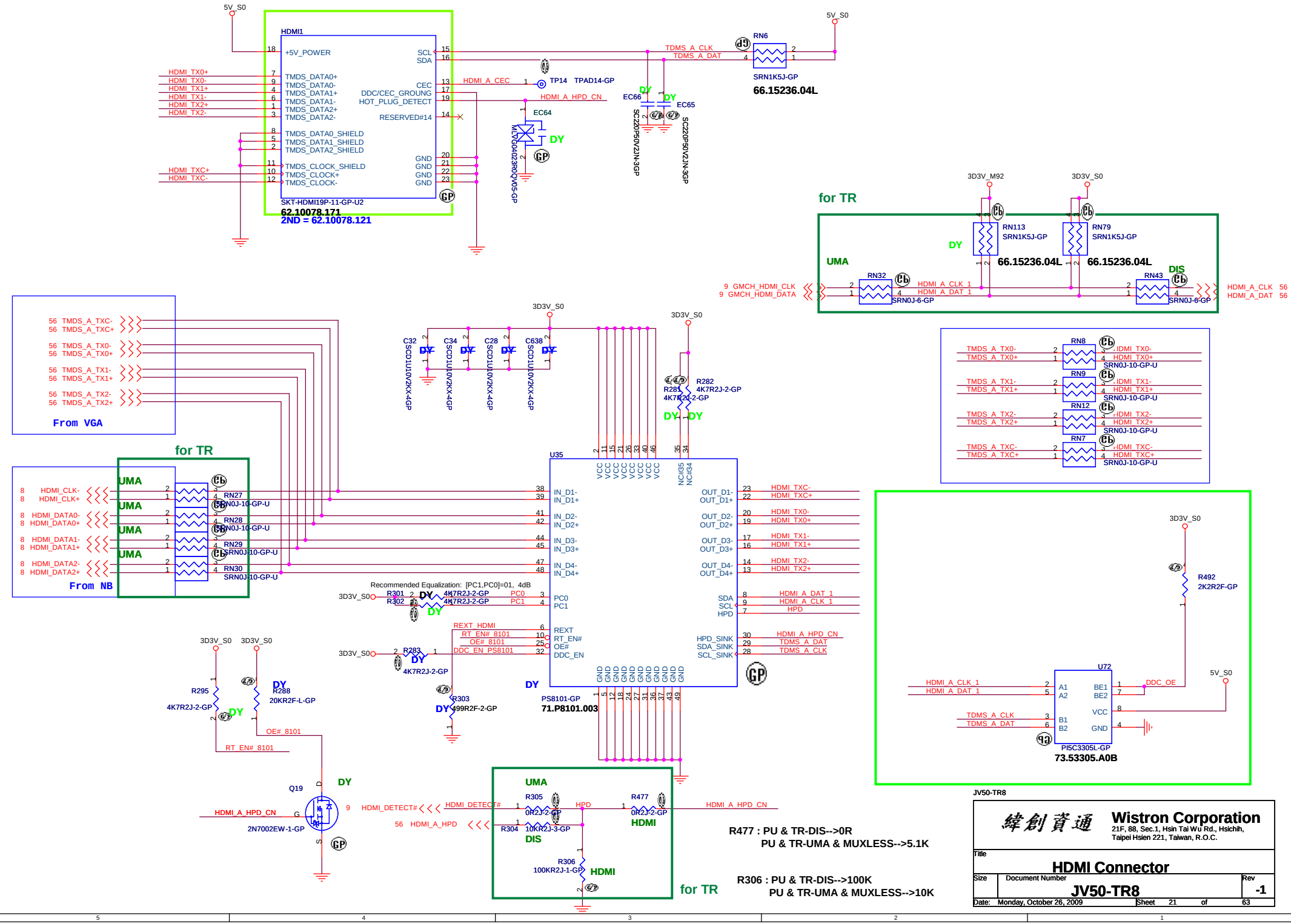
JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

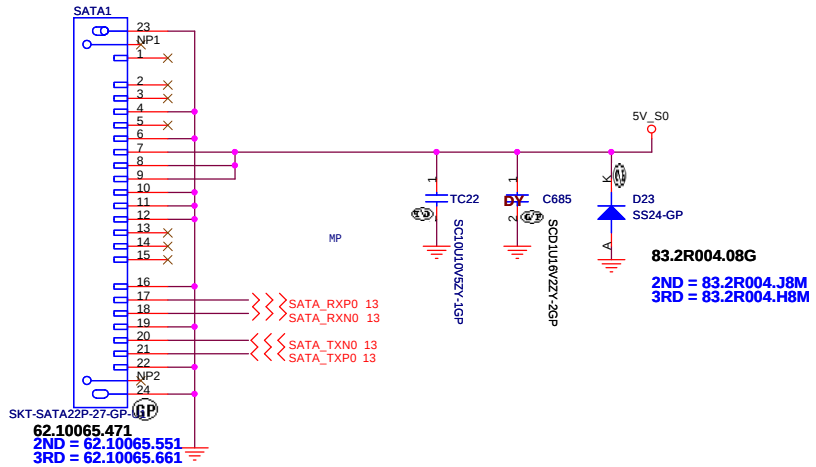
Title: CRT Connector

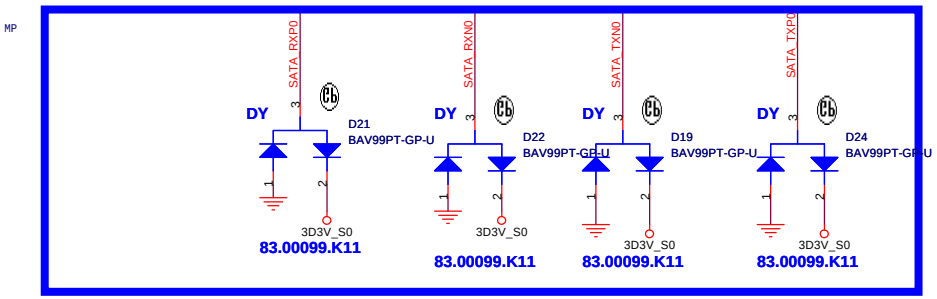
Size	Document Number	Rev
	JV50-TR8	-1

Date: Monday, October 26, 2009 Sheet 20 of 63


HDMI1
SKT-HDMI19P-11-GP-U2
62.10078.171
2ND = 62.10078.121
RN6
SRN1K5J-GP
66.15236.04L
TP14 TPAD14-GP
EC64
EC66
EC65
SC220P50V2JN-3GP
MLTG0402R30QW05-GP
for TR
UMA
DIS
RN113
RN79
RN32
RN43
SRN0J-6-GP
From VGA
From NB
RN27
RN28
RN29
RN30
SRN0J-10-GP-U
RN8
RN9
RN12
RN7
SRN0J-10-GP-U
C32
C34
C28
C638
SSCD1U10V2KX-4GP
R282
4K7R2J-2-GP
U35
PS8101-GP
71.P8101.003
Recommended Equalization: [PC1,PC0]=01, 4dB
R301
R302
R283
R303
499R2F-2-GP
R295
R288
20KR2F-L-GP
OE# 8101
RT_EN# 8101
Q19
2N7002EW-1-GP
R305
R306
100KR2J-1-GP
R304
10KR2J-3-GP
R477
0R2J-2-GP
HDMI
R492
2K2R2F-GP
U72
PI5C3305L-GP
73.53305.A0B
R477 : PU & TR-DIS-->0R
PU & TR-UMA & MUXLESS-->5.1K
R306 : PU & TR-DIS-->100K
PU & TR-UMA & MUXLESS-->10K
JV50-TR8
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI Connector
Size
Document Number
JV50-TR8
Rev
-1
Date: Monday, October 26, 2009
Sheet 21 of 63

SATA Connector

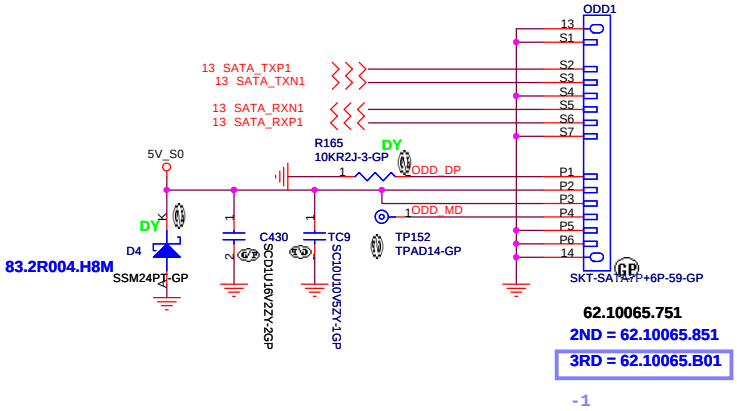


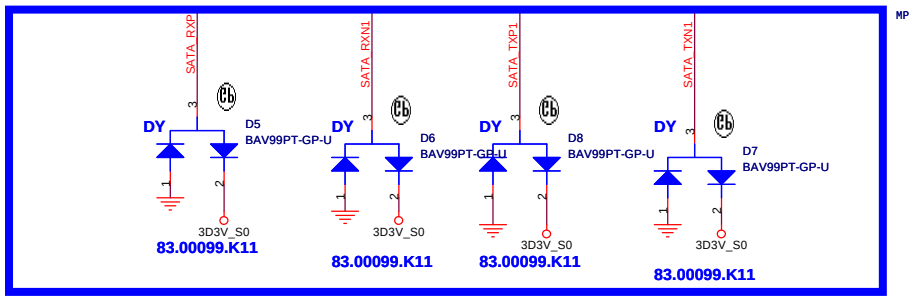


JV50-TR8

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **HDD**		
Size	Document Number: **JV50-TR8**	Rev: **-1**
Date: Monday, October 26, 2009	Sheet 22 of 63	

SATA ODD Connector





JV50-TR8

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

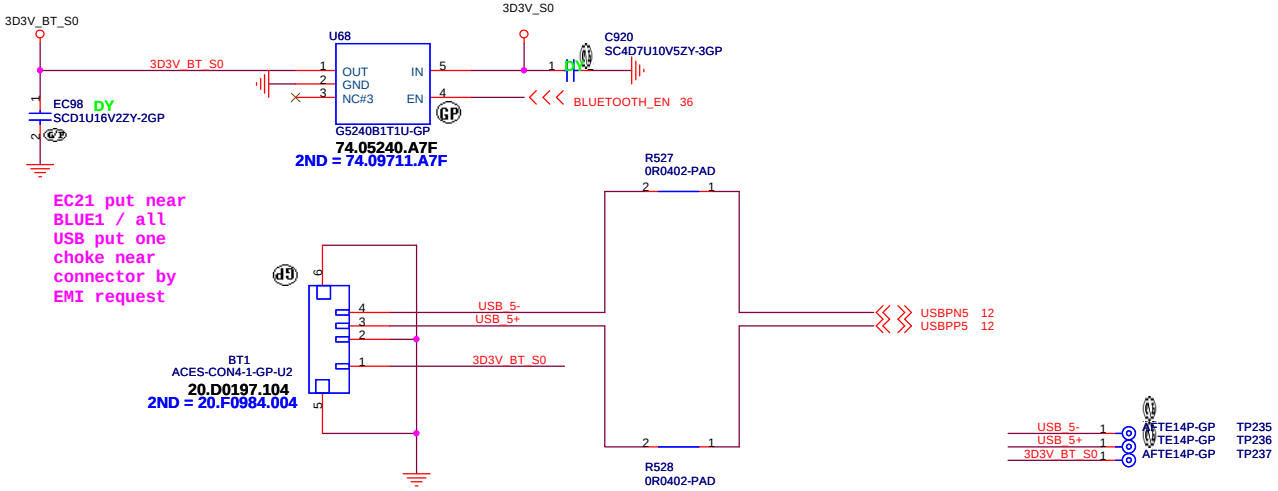
Title: ODD

Size | Document Number: JV50-TR8 | Rev: -1

Date: Monday, October 26, 2009 | Sheet 23 of 63

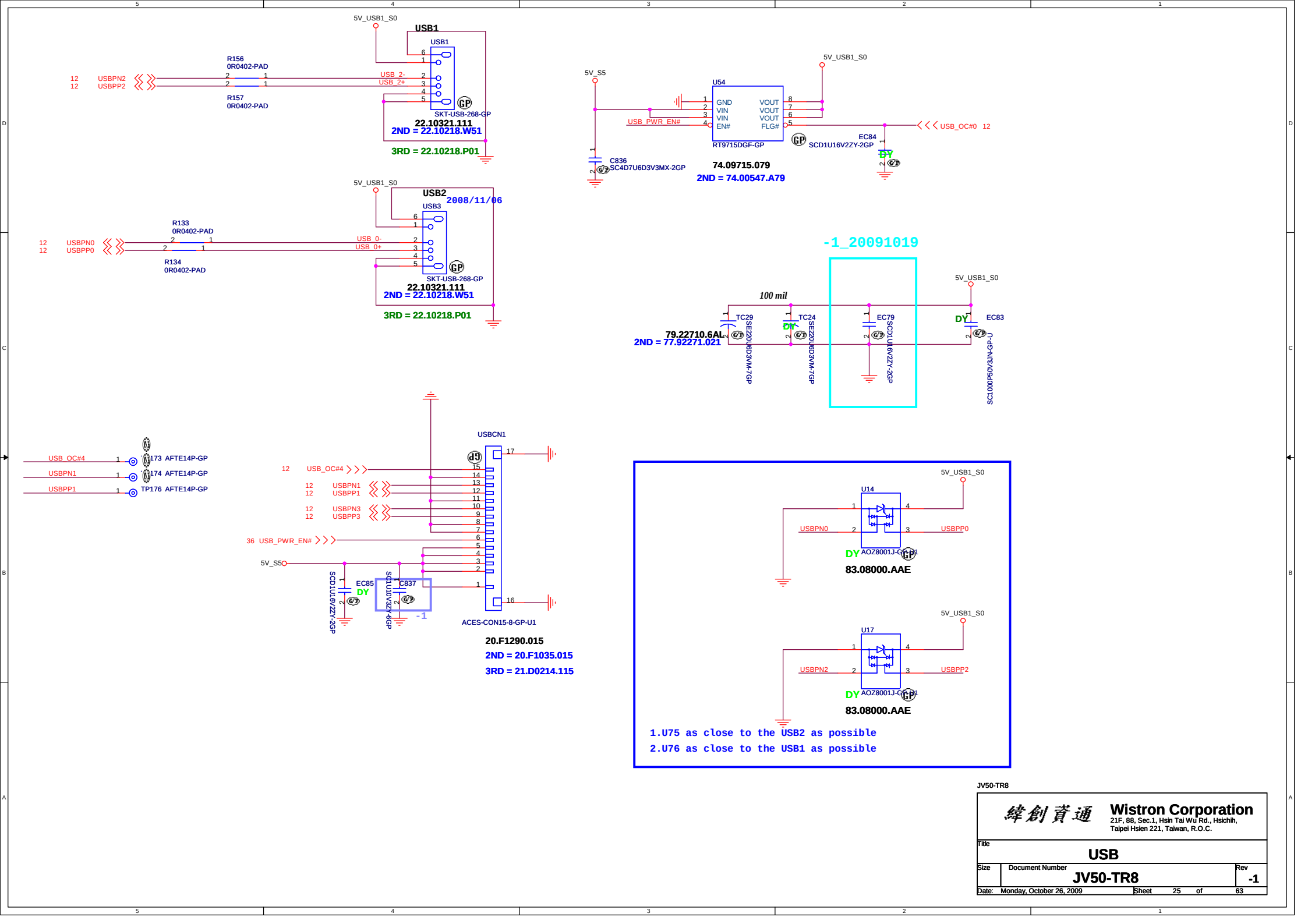
BLUETOOTH MODULE

1.5A / High Active Voltage 2V



JV50-TR8

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BLUETOOTH		
Size	Document Number: JV50-TR8	Rev: -1
Date: Thursday, November 12, 2009	Sheet 24 of 63	


5V_USB1_S0
USB1
R156
0R0402-PAD
R157
0R0402-PAD
USBPN2
USBPP2
USB_2-
USB_2+
SKT-USB-268-GP
22.10321.111
2ND = 22.10218.W51
3RD = 22.10218.P01
5V_S5
U54
GND
VIN
VIN
EN#
VOUT
VOUT
VOUT
FLG#
USB_PWR_EN#
RT9715DGF-GP
C836
SC4D7U6D3V3MX-2GP
EC84
SCD1U16V2ZY-2GP
USB_OC#0
74.09715.079
2ND = 74.00547.A79
USB2
2008/11/06
USB3
R133
0R0402-PAD
R134
0R0402-PAD
USBPN0
USBPP0
USB_0-
USB_0+
SKT-USB-268-GP
22.10321.111
2ND = 22.10218.W51
3RD = 22.10218.P01
-1_20091019
100 mil
TC29
TC24
EC79
EC83
SE220U6D3VM-7GP
SCD1U16V2ZY-2GP
SC1000P50V3JN-GP
79.22710.6AL
2ND = 77.92271.021
USB_OC#4
USBPN1
USBPP1
TP173 AFTE14P-GP
TP174 AFTE14P-GP
TP176 AFTE14P-GP
USBCN1
USB_OC#4
USBPN1
USBPP1
USBPN3
USBPP3
USB_PWR_EN#
5V_S5
EC85
C837
SCD1U16V2ZY-2GP
SC1U10V2ZY-6GP
-1
ACES-CON15-8-GP-U1
20.F1290.015
2ND = 20.F1035.015
3RD = 21.D0214.115
U14
U17
USBPN0
USBPP0
USBPN2
USBPP2
AOZ8001J-GP
83.08000.AAE
1.U75 as close to the USB2 as possible
2.U76 as close to the USB1 as possible
JV50-TR8
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
USB
Size
Document Number
JV50-TR8
Rev
-1
Date: Monday, October 26, 2009
Sheet 25 of 63

CO-Layout BCM5764 and BCM5784
modify BOM :71.05784.M03

U4
BCM5784MKMLG-GP
71.05784.M03

U3
AT24C02BN-SH-T-GP
72.24C02.R01
2ND = 72.24C02.M01

82.30020.851
2ND = 82.30020.791

1ST 84.DCP69.01B
2ND = 84.00069.B1B

Place PLLVDD/AVDDL
CKT as close to chip as
possible

JV50-TR8

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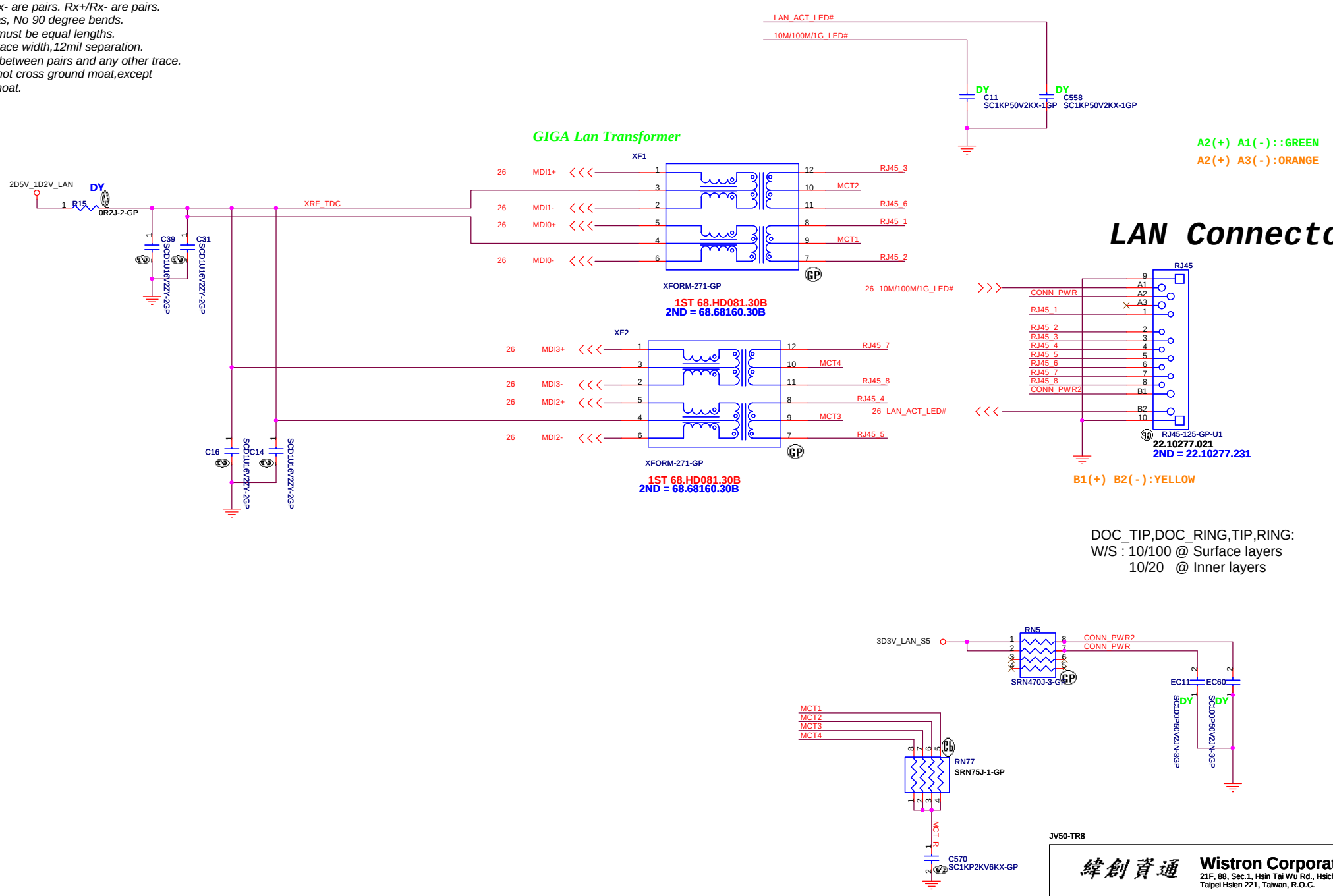
Taipei Hsien 221, Taiwan, R.O.C.

Title: BCM5784MKMLG
Size: Custom
Document Number: JV50-TR8
Rev: -1
Date: Monday, October 26, 2009
Sheet 26 of 63

LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.



JV50-TR8

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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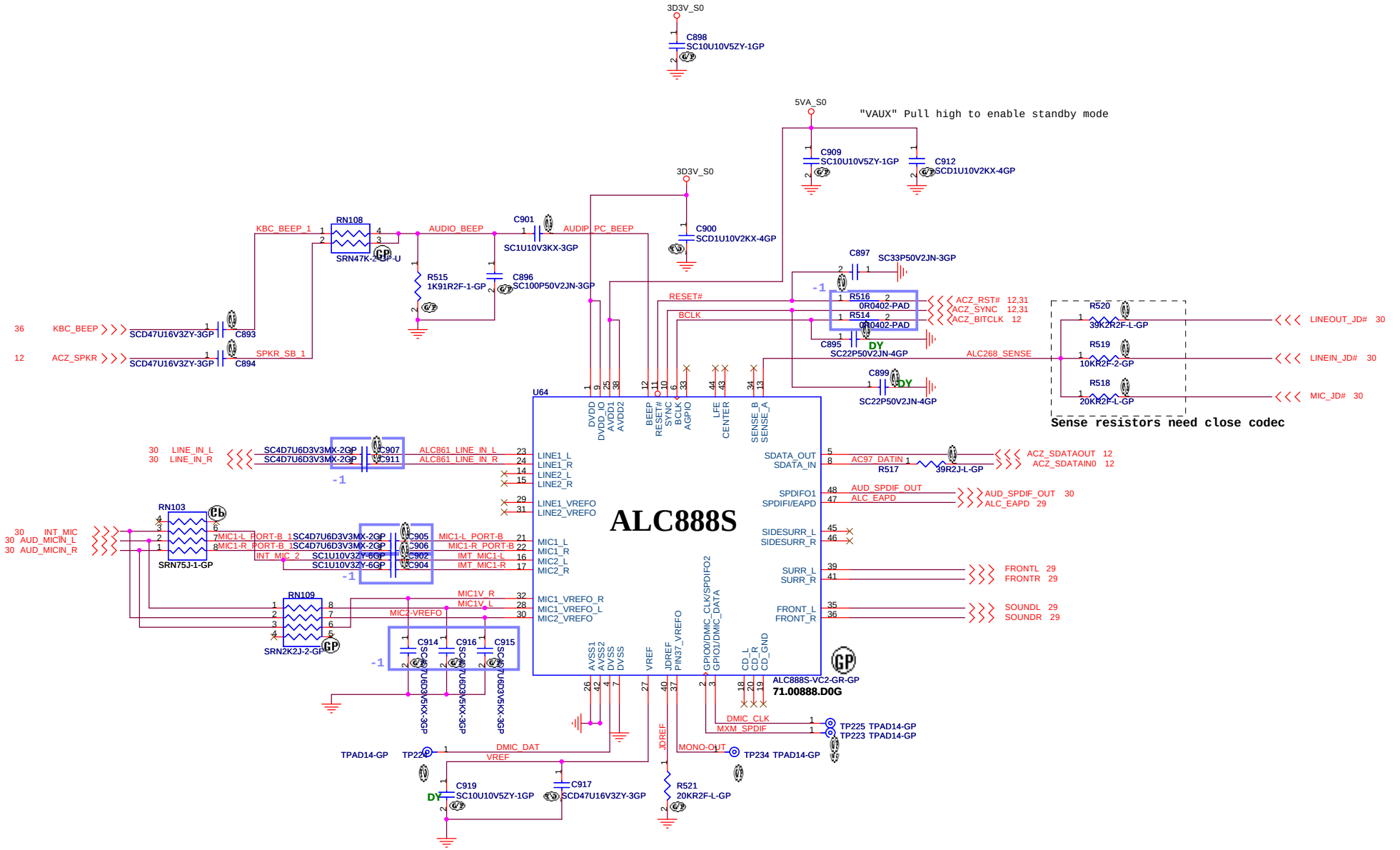
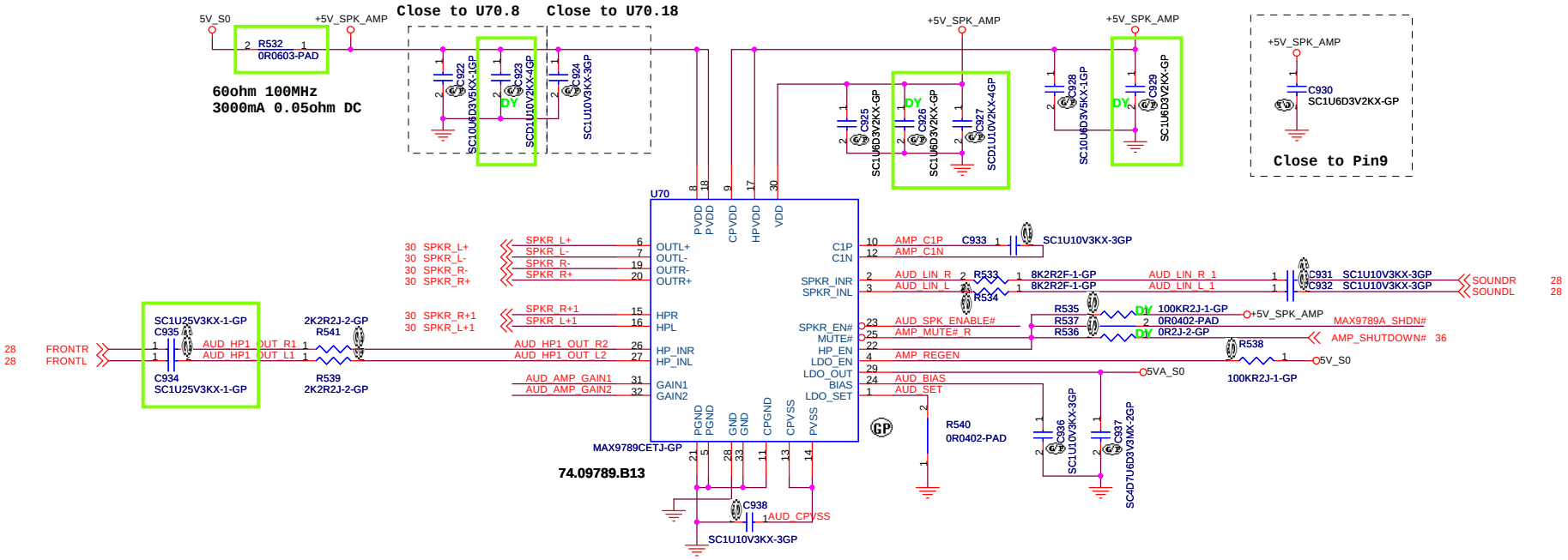
Title		
LAN CONN		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 27 of 63	

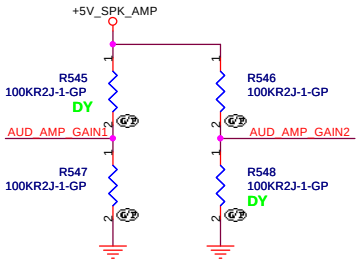


JV50-TR8

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Azalia codec ALC888**	
Size A3	Document Number **JV50-TR8**	Rev **-1**
Date: Monday, October 26, 2009	Sheet 28 of 63	

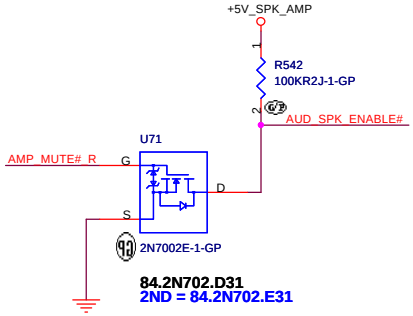


GAIN SETTING

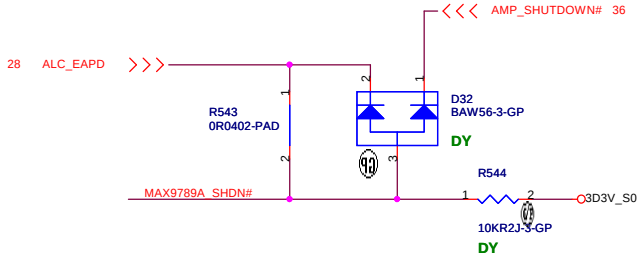


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Signal inverter for speaker shutdown



84.2N702.D31
2ND = 84.2N702.E31



JV50-TR8

Wistron Corporation
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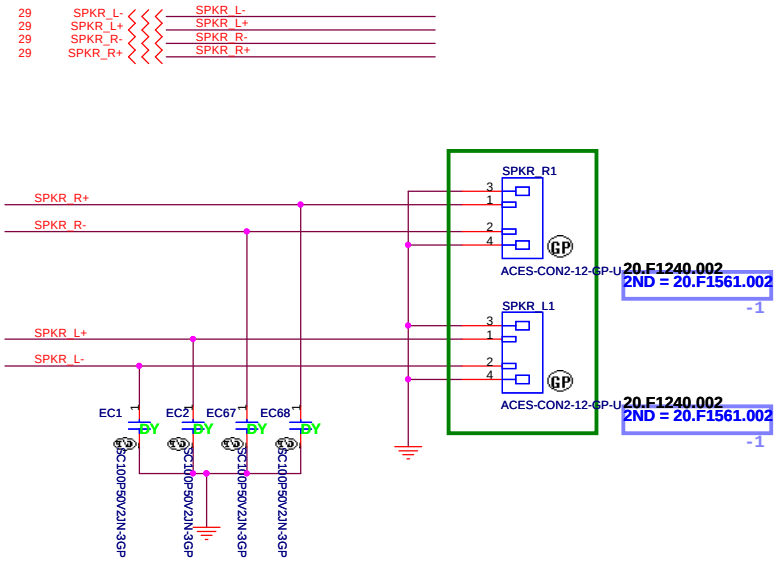
Taipei Hsien 221, Taiwan, R.O.C.

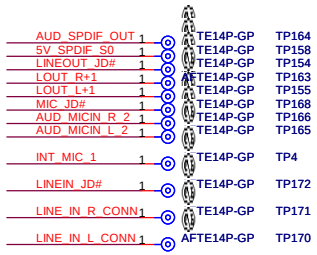
Title: AUDIO AMP

Size	Document Number	Rev
	JV50-TR8	-1

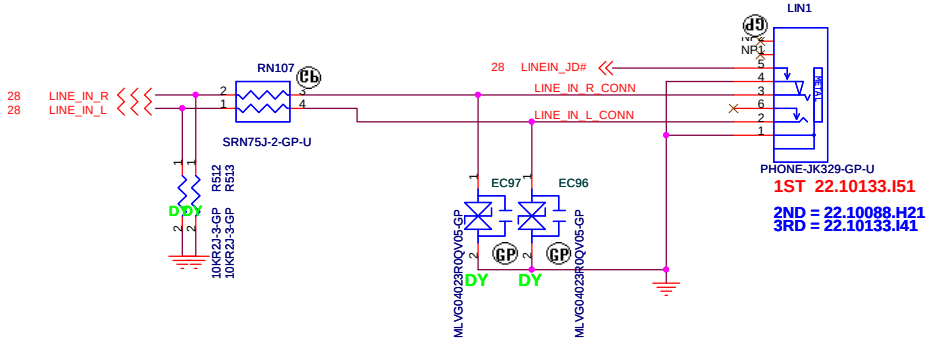
Date: Monday, October 26, 2009 Sheet 29 of 63

Internal Speaker

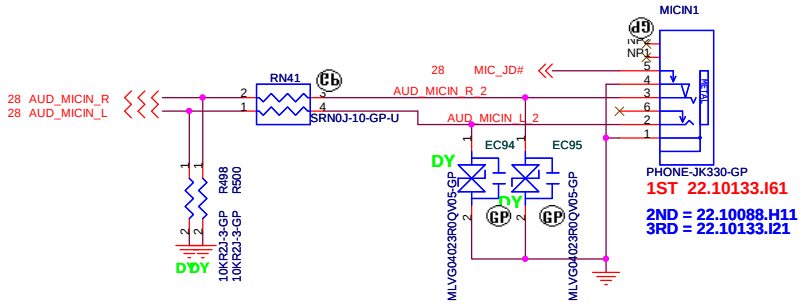




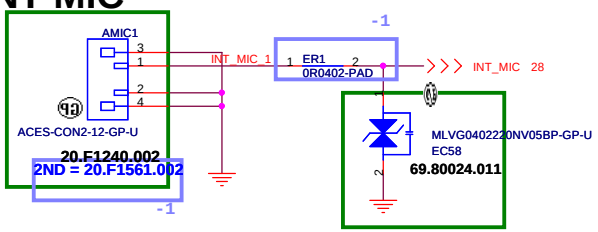
LINE IN



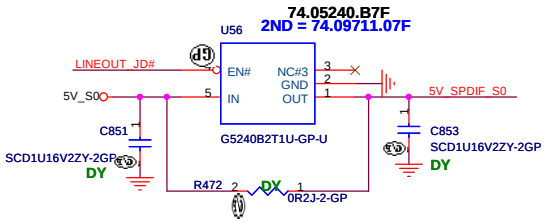
MIC IN

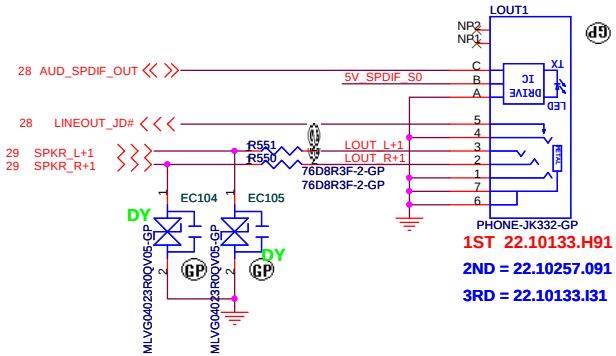


INT MIC



LINE OUT

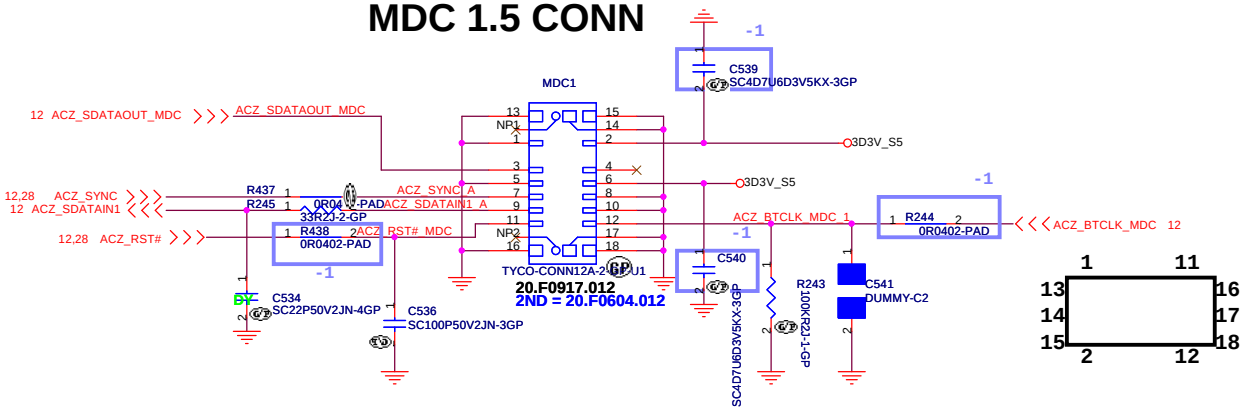




JV50-TR8

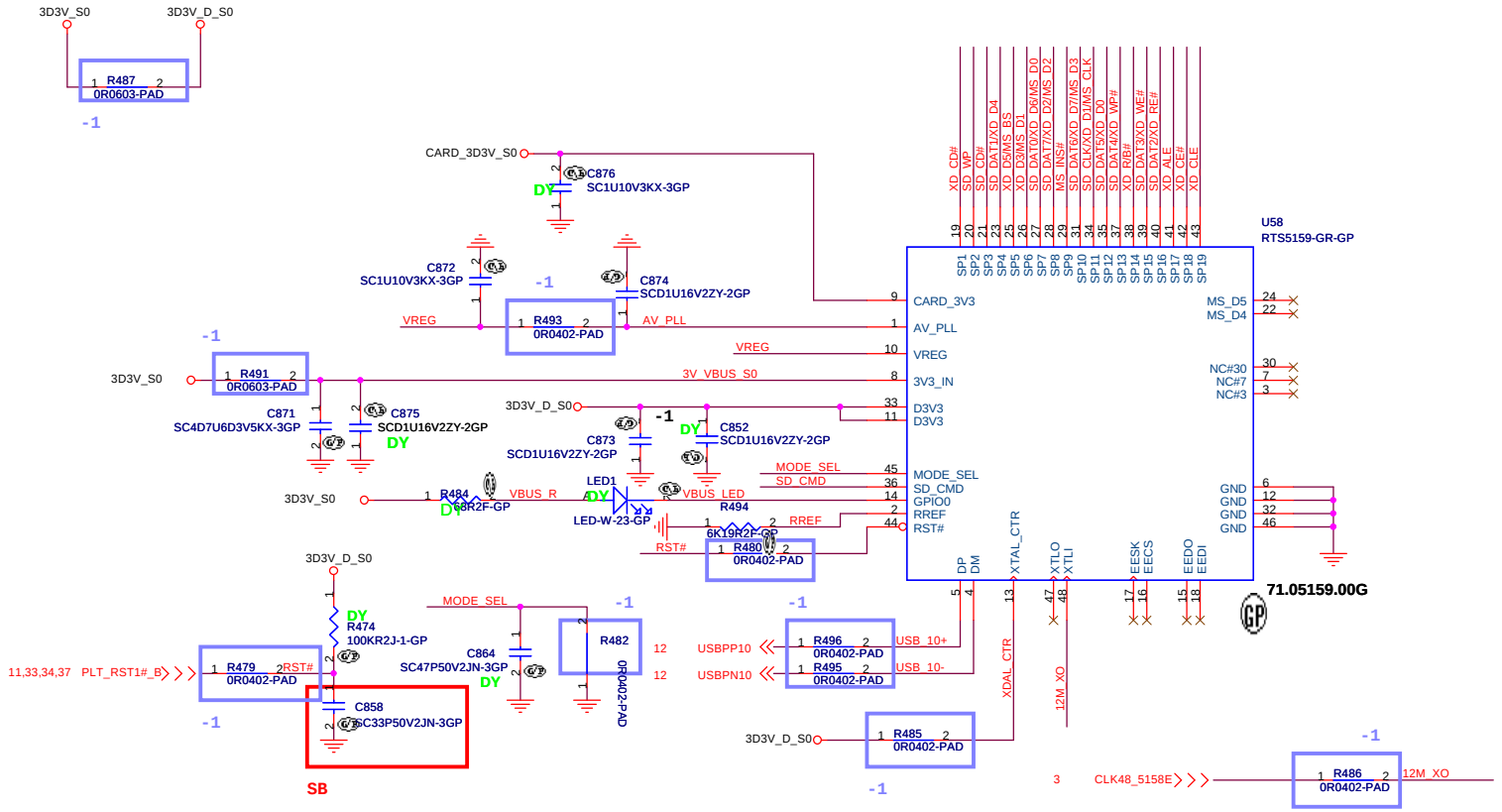
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**AUDIO JACK**	
Size	Document Number **JV50-TR8**	Rev -1
Date: Monday, October 26, 2009	Sheet 30 of 63	

MDC 1.5 CONN

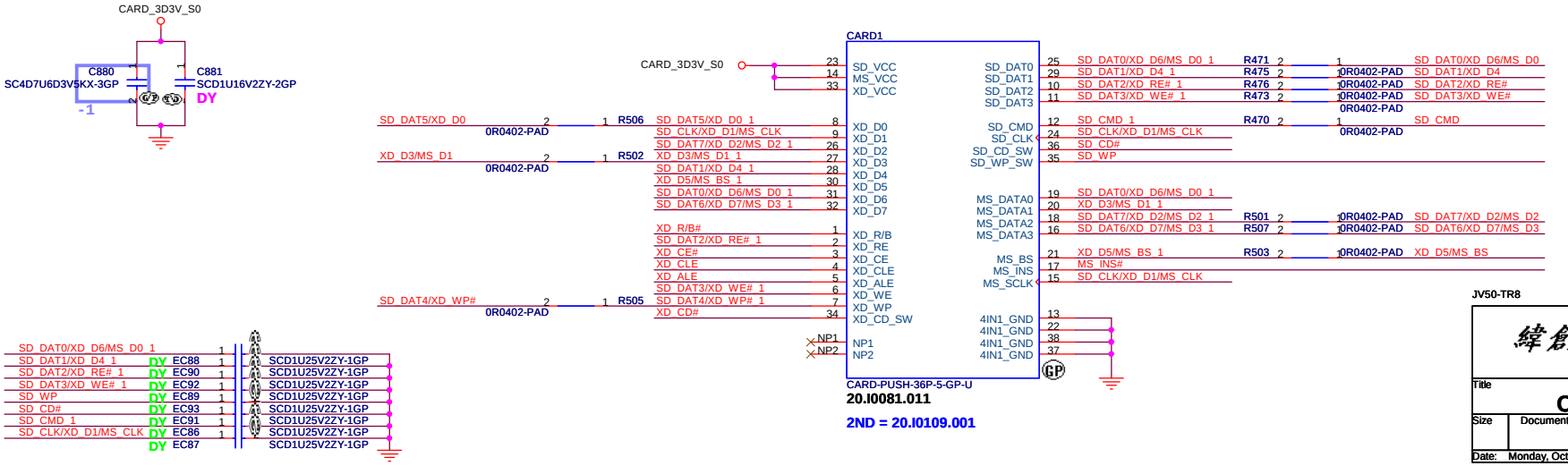


JV50-TR8

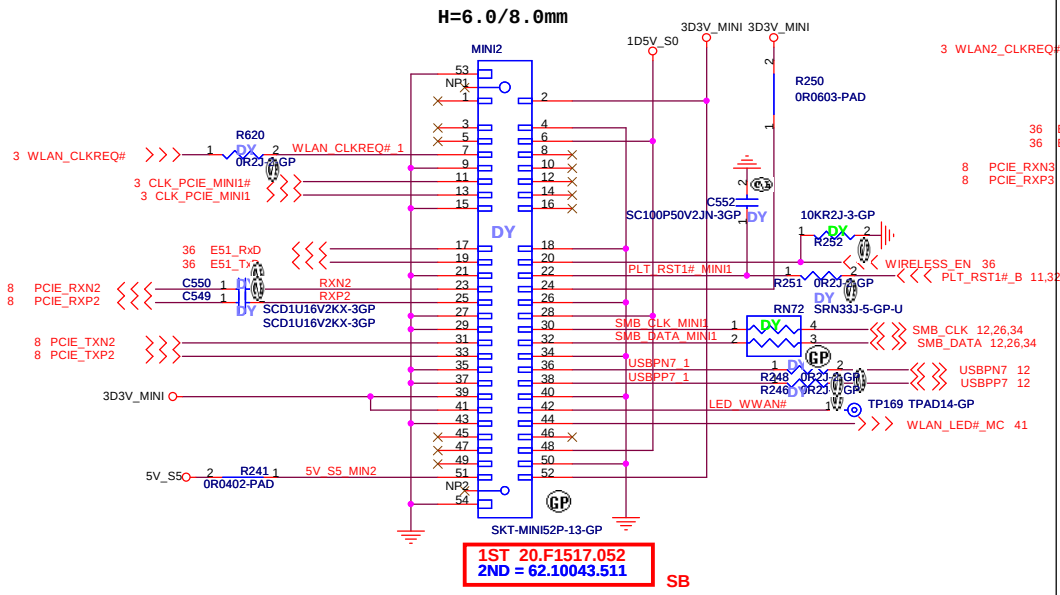
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MDC		
Size	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 31 of 63	



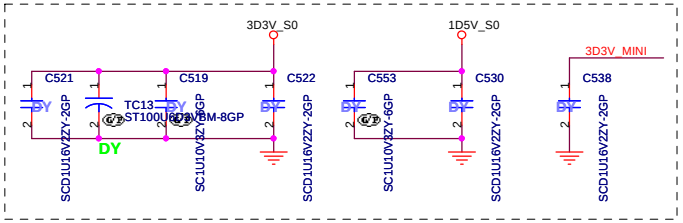
5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



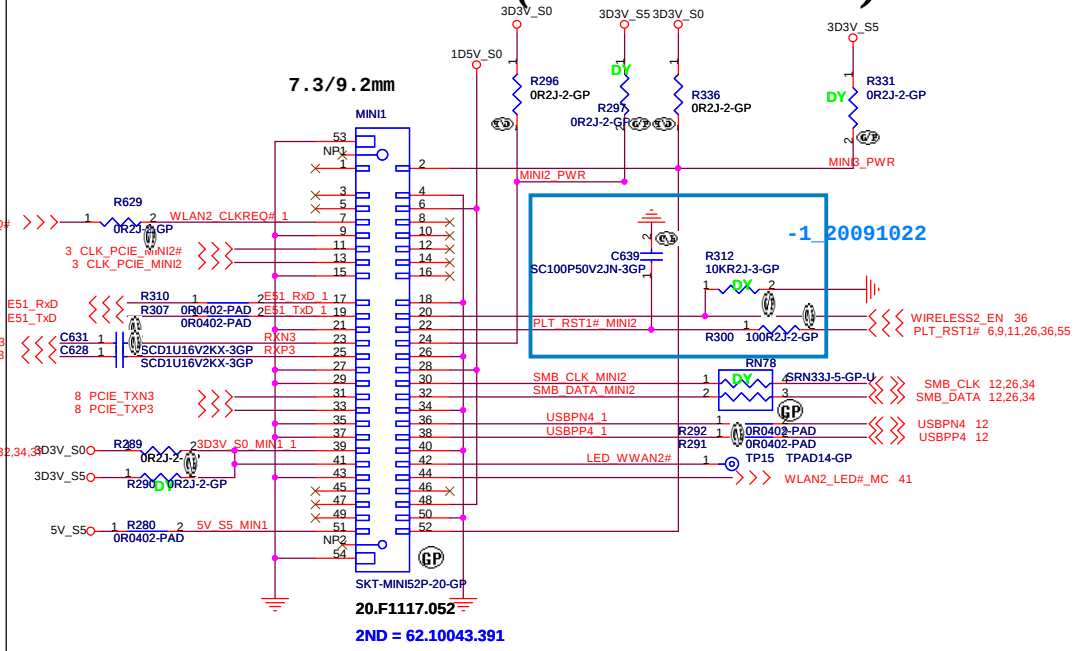
Mini Card Connector(WLAN)



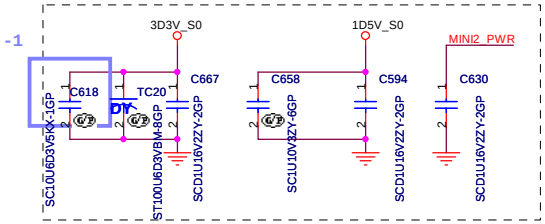
Place near MINI2



Mini Card Connector(Robson2 and 3G)



Place near MINI1



JV50-TR8

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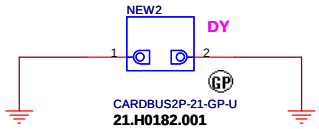
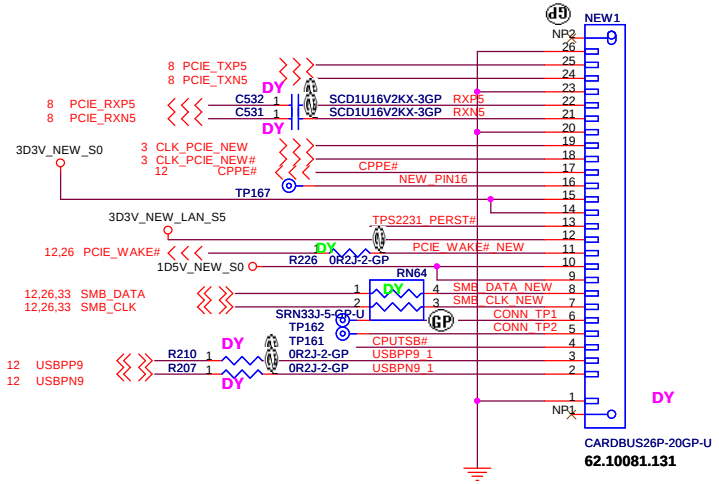
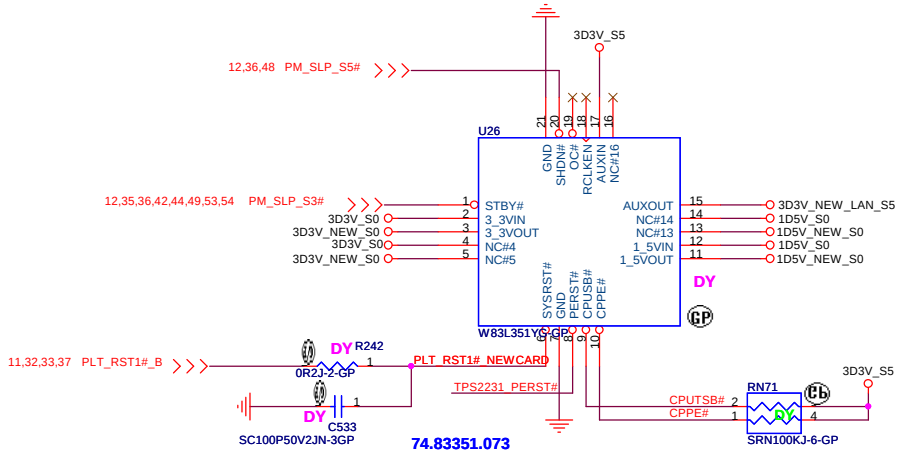
Title: MINI CARD		
Size	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 33 of 63	

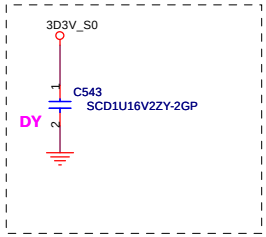
NEWCARD Connector



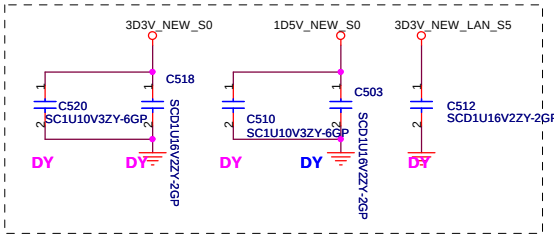




Place them Near to Chip



Place them Near to Connector



JV50-TR8

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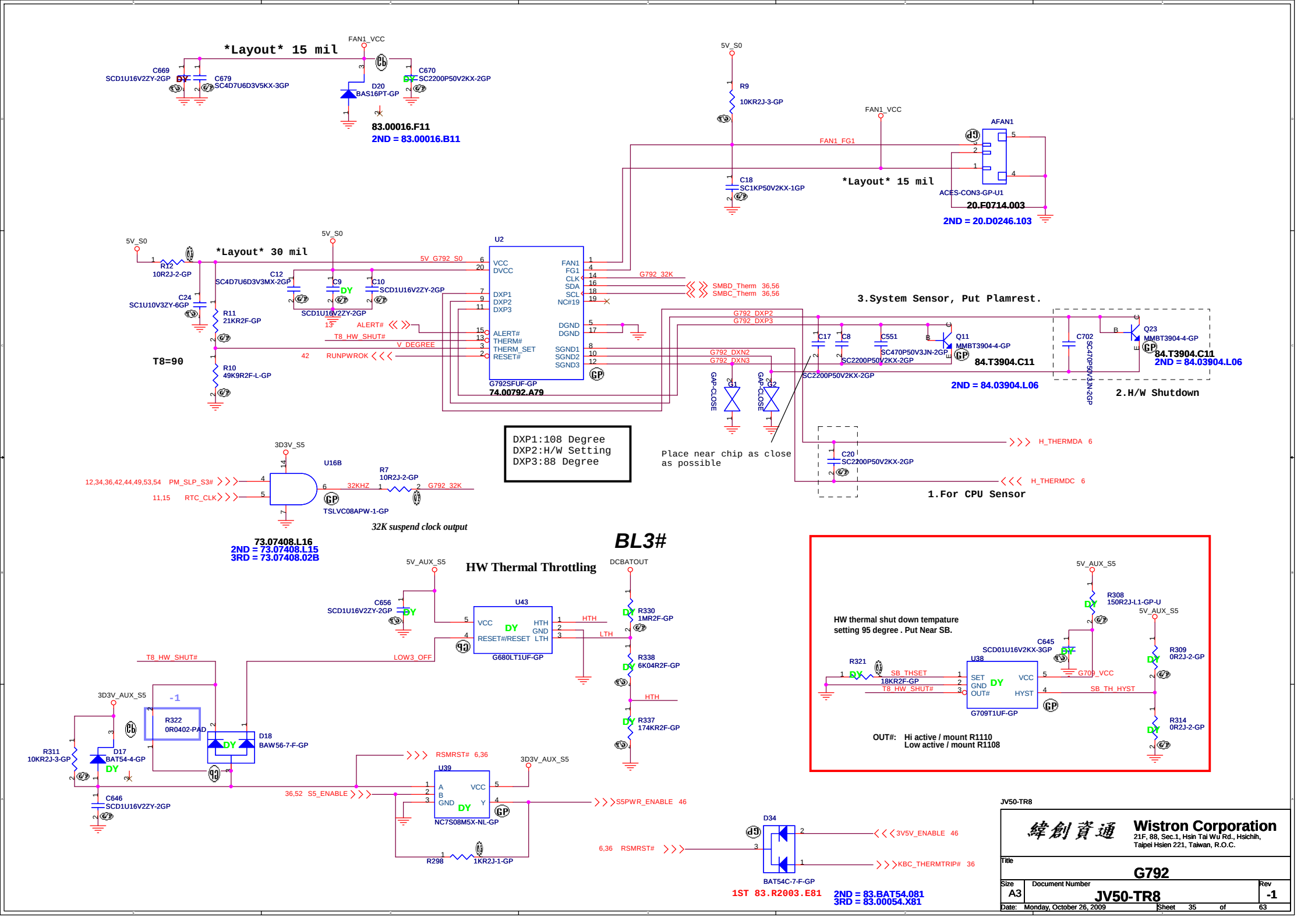
Title: NEW CARD		
Size	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 34 of 63	



JV50-TR8

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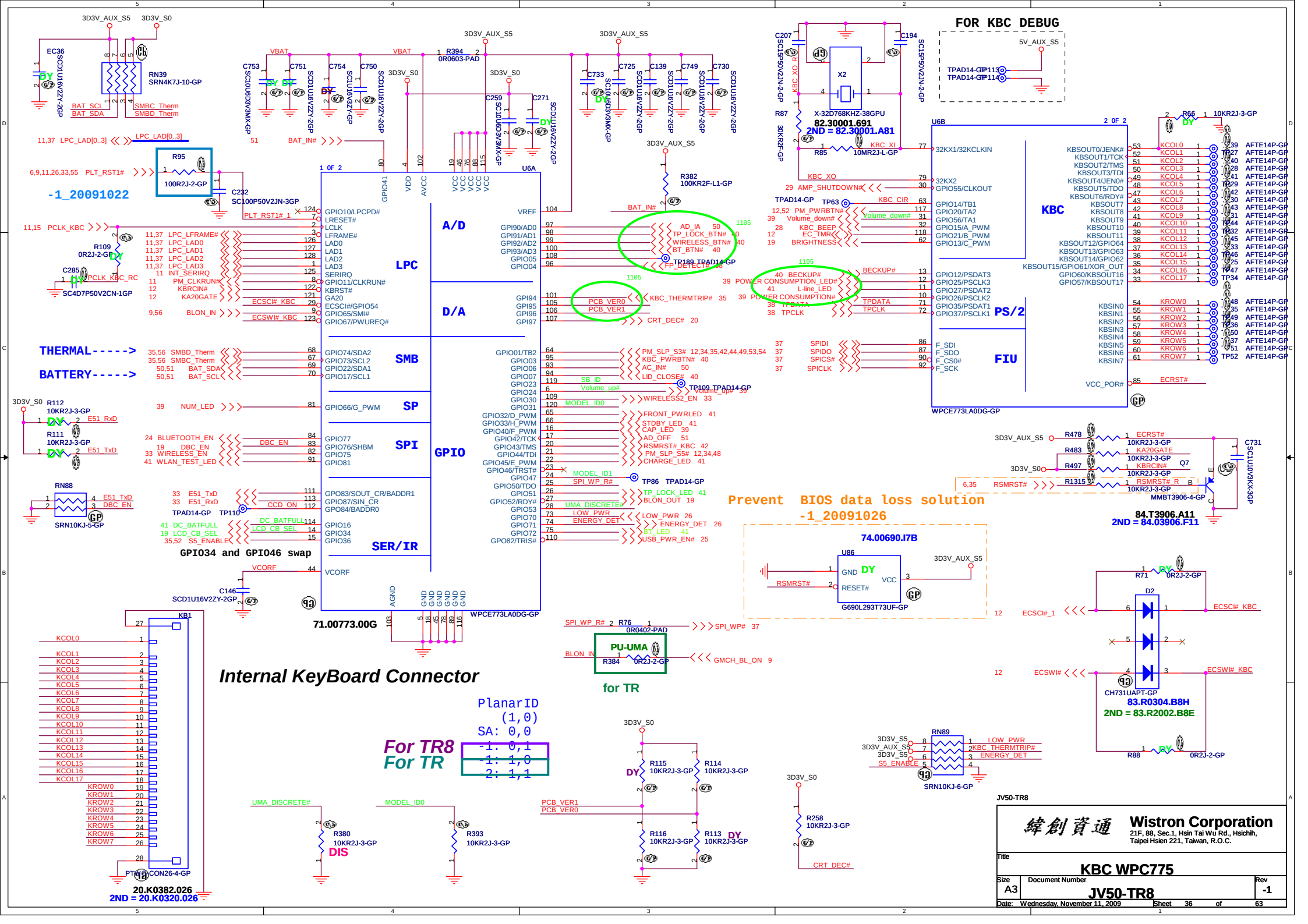
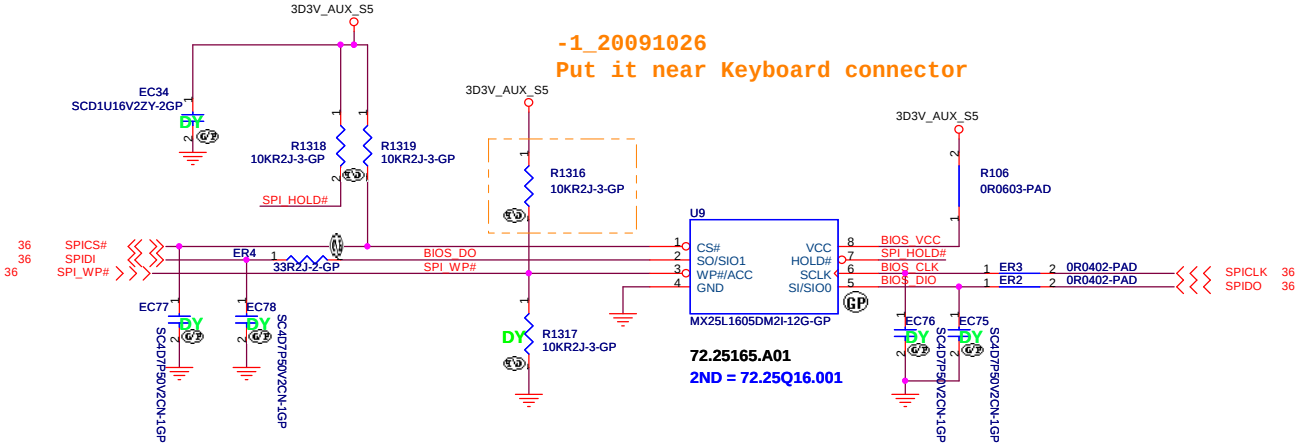
Taipei Hsien 221, Taiwan, R.O.C.

Title: G792

Size	Document Number	Rev
A3	JV50-TR8	-1

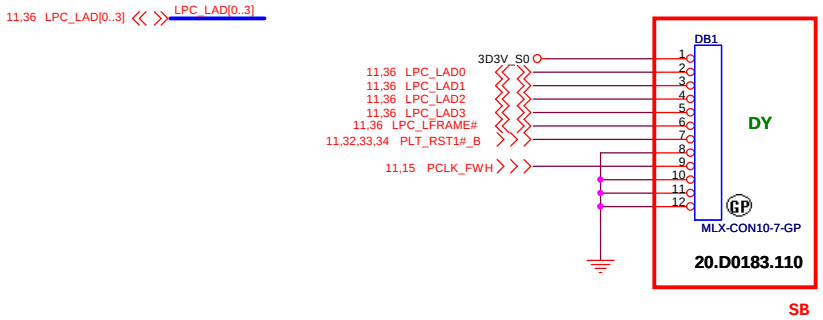
Date: Monday, October 26, 2009 Sheet 35 of 63


FOR KBC DEBUG
-1_20091022
THERMAL----->
BATTERY----->
GPIO034 and GPIO046 swap
Prevent BIOS data loss solution
-1_20091026
Internal KeyBoard Connector
for TR
PlanarID
(1,0)
SA: 0,0
-1: 0,1
-1: 1,0
2: 1,1
For TR8
For TR
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
U6A
U6B
WPCE773LA0DG-GP
71.00773.00G
82.30001.691
2ND = 82.30001.A81
74.00690.I7B
84.T3906.A11
2ND = 84.03906.F11
83.R0304.B8H
2ND = 83.R2002.B8E
20.K0382.026
2ND = 20.K0320.026
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC775
JV50-TR8
Wednesday, November 11, 2009



16M Bits
SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD



JV50-TR8

緯創資通 Wistron Corporation
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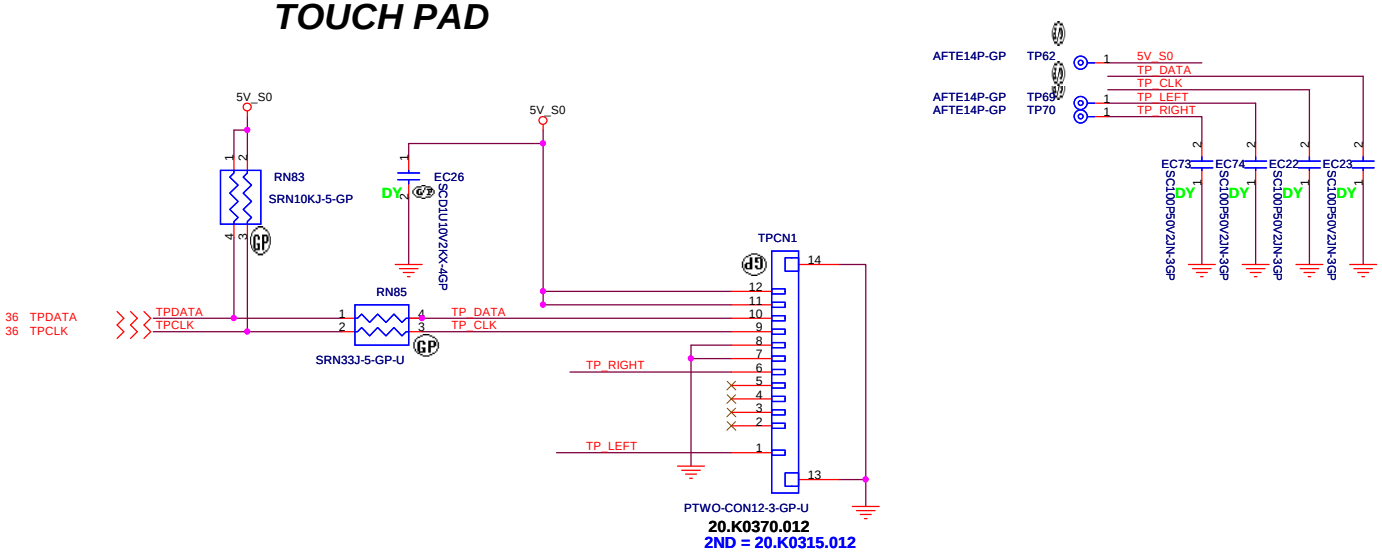
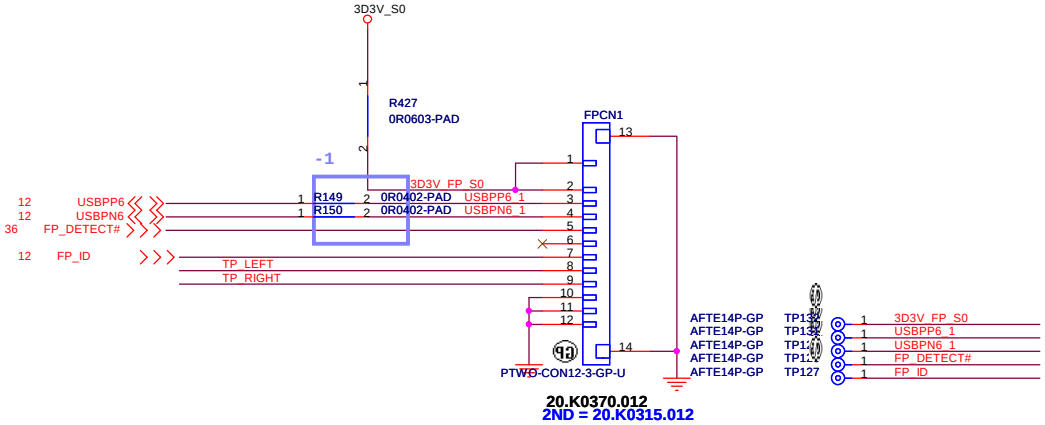
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BIOS		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Wednesday, November 11, 2009	Sheet 37 of 63	

TOUCH PAD



Finger printer



JV50-TR8

緯創資通 Wistron Corporation
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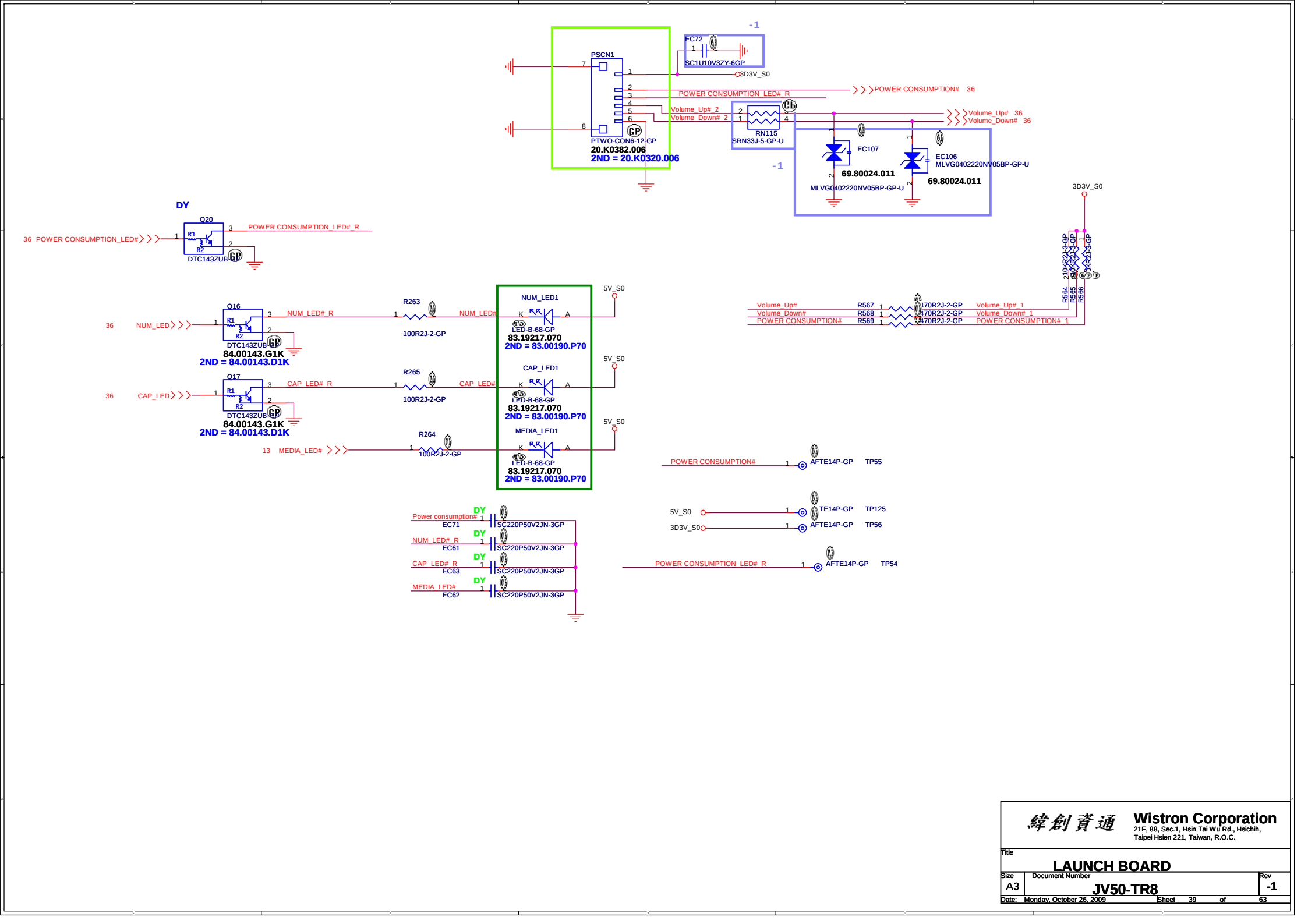
Taipei Hsien 221, Taiwan, R.O.C.

Title: Touch PAD/Finger printer

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 26, 2009 Sheet 38 of 63



Wistron Corporation		
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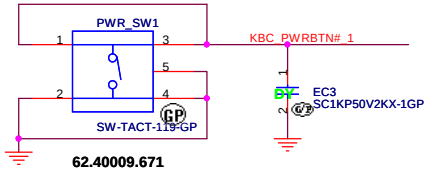
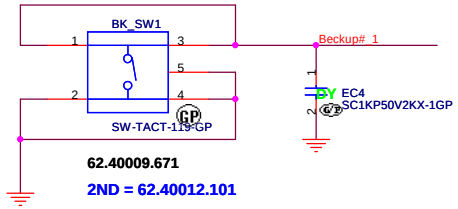
Title: LAUNCH BOARD		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 39 of 63	

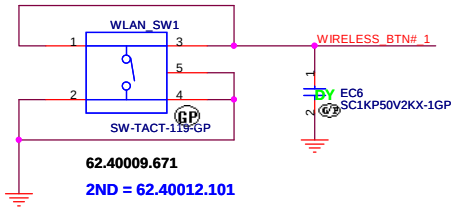
Power Button



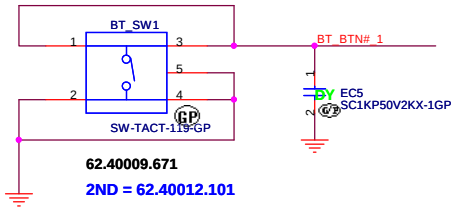
Beckup Button



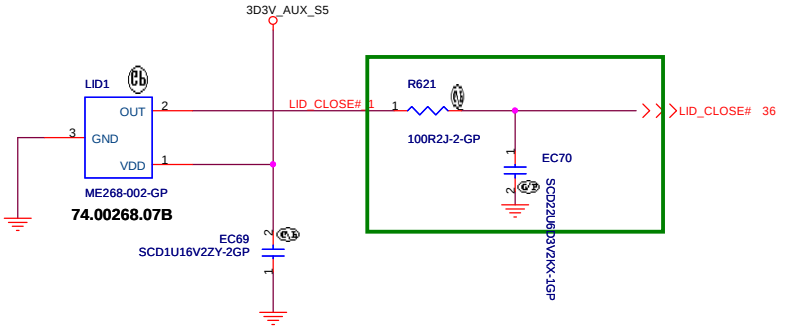
WIRELESS Button

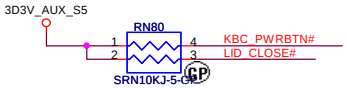


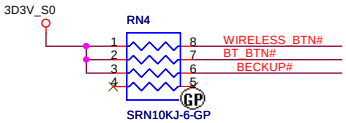
BT/3G Button

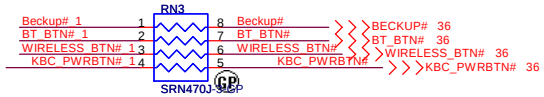


Cover Up Switch

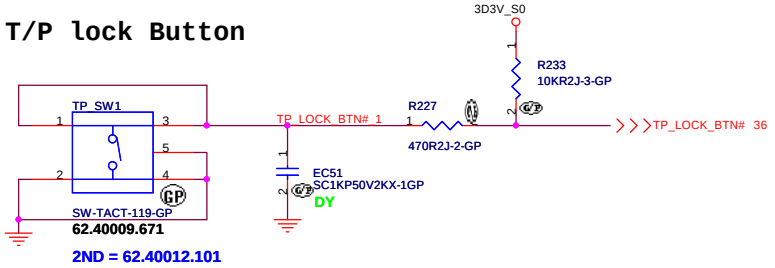




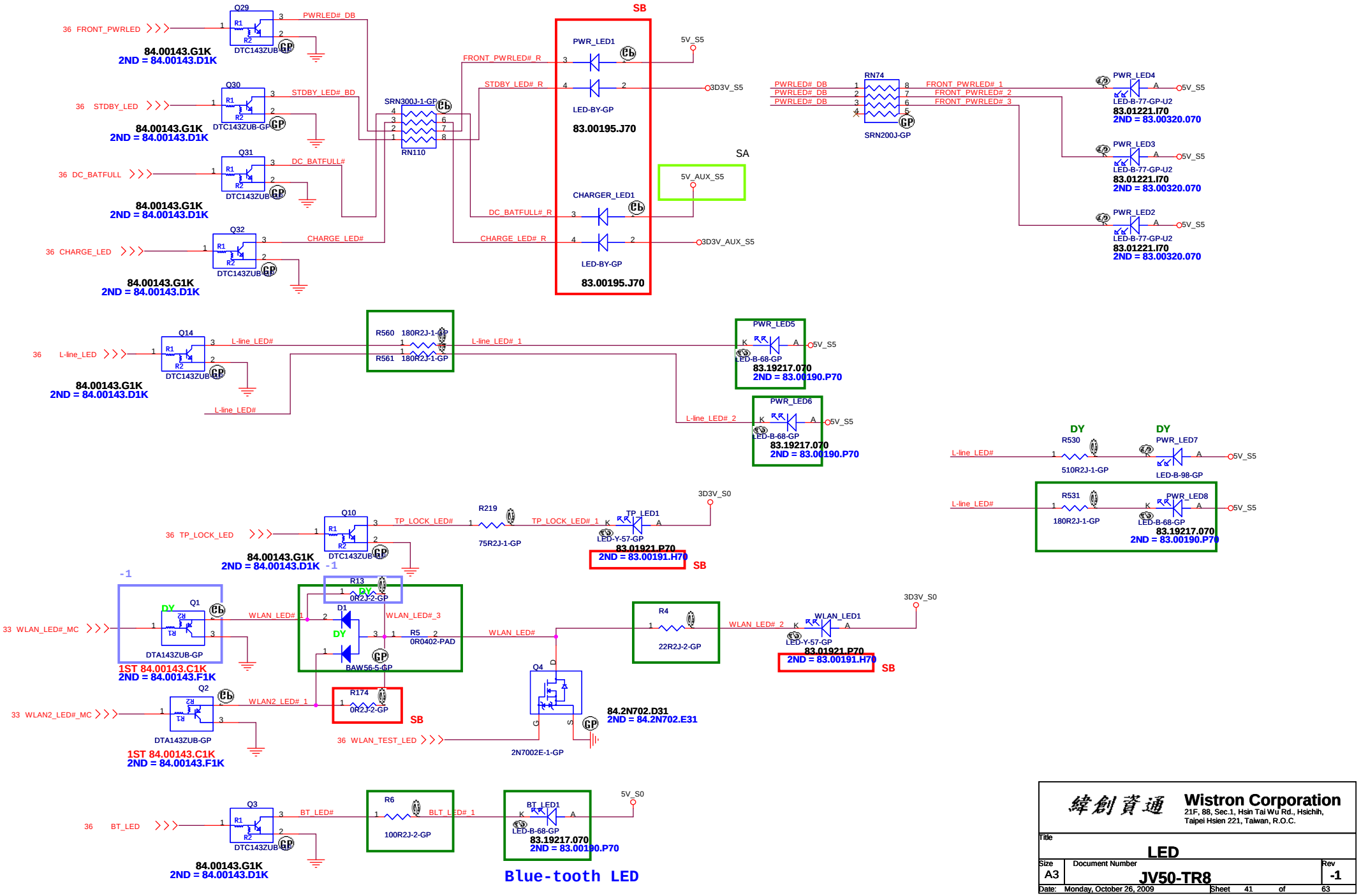




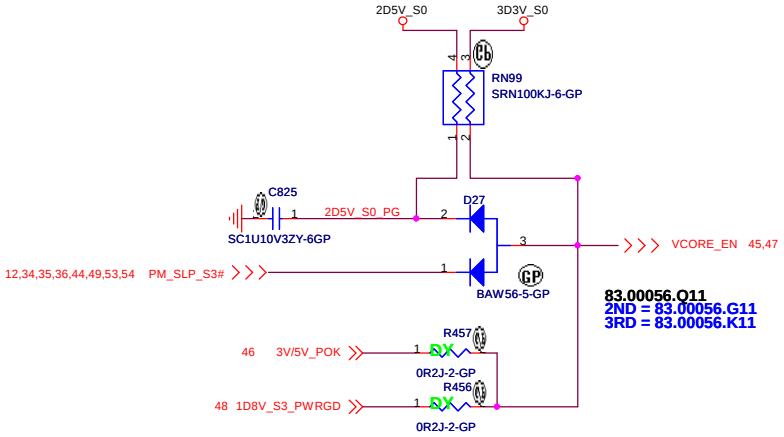
T/P lock Button

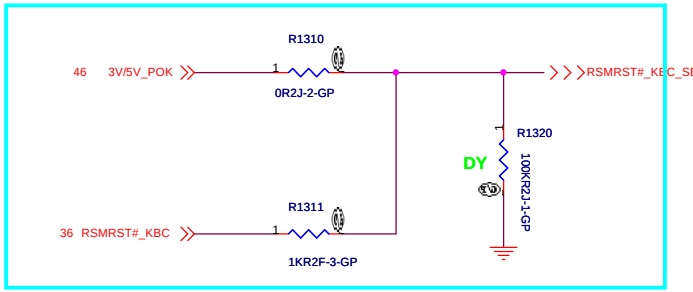


緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: SWITCH		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 40 of 63	



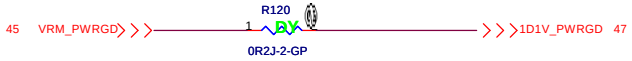
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: LED		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 41 of 63	

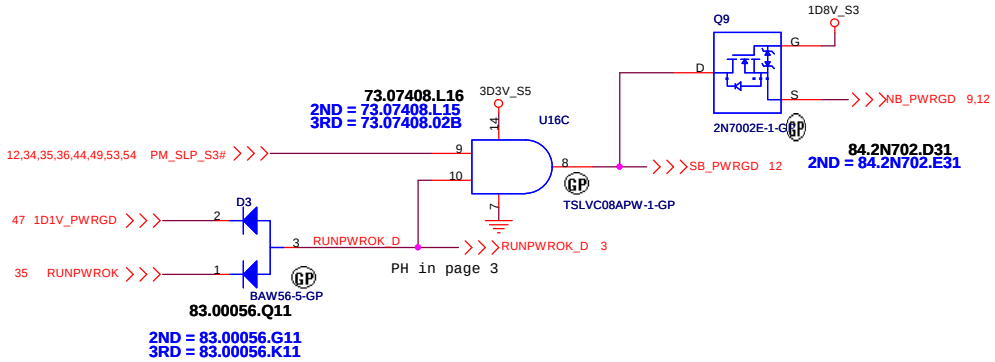




-1_20091026

P/H @ 1D8V_S3 PAGE





JV50-TR8

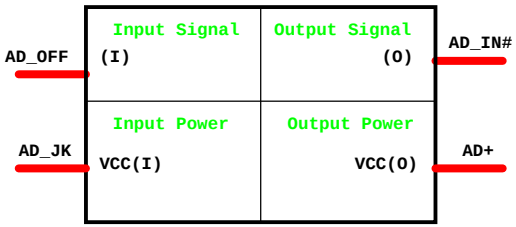
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER ON LOGIC

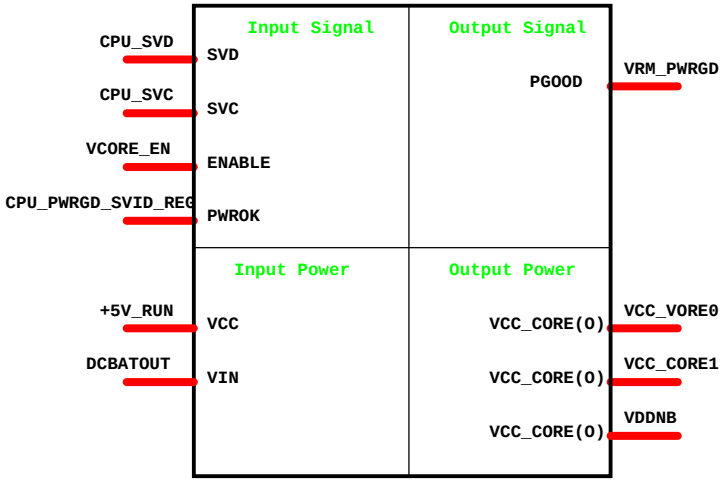
Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Wednesday, November 11, 2009 Sheet 42 of 63

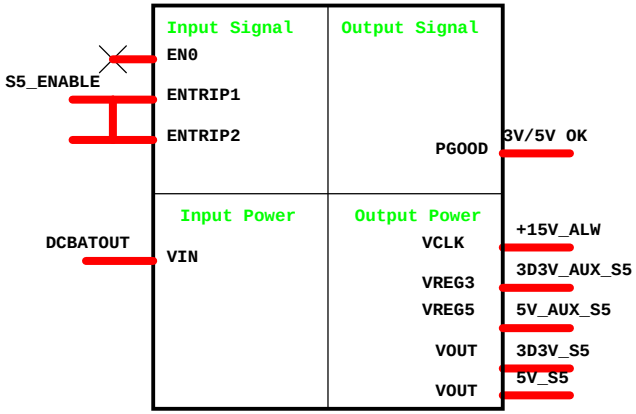
Adapter



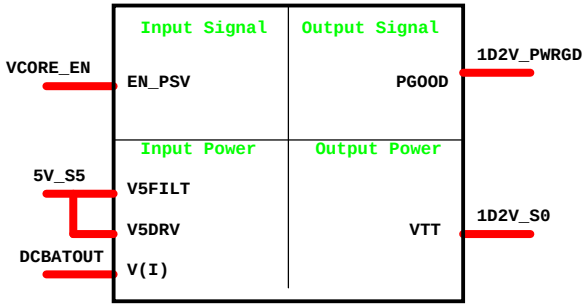
CPU_CORE
ISL6265HRTZ



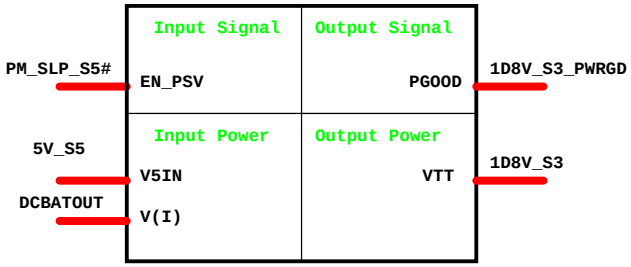
DCDC 5V/3D3V(RT8205A)



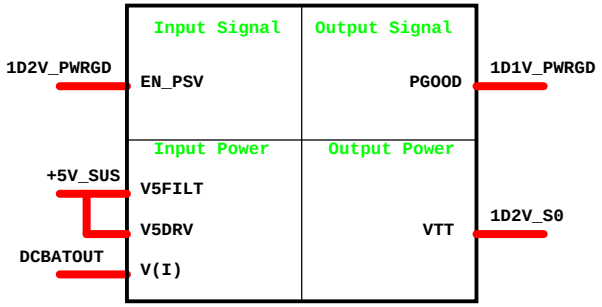
DCDC 1D2V(TPS51124)



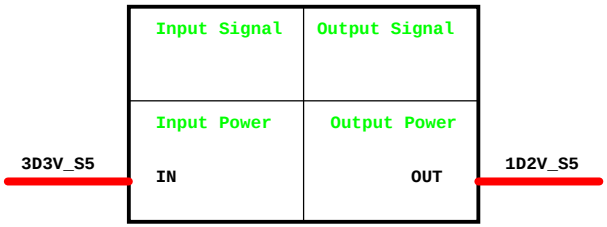
DCDC 1D8V(RT8209B)



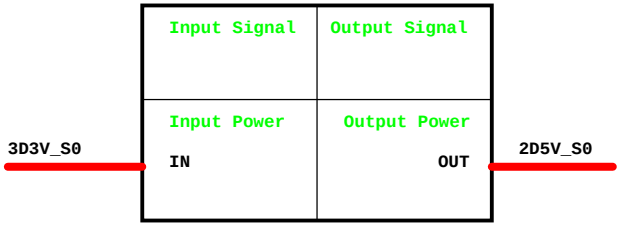
DCDC 1D1V(TPS51124)



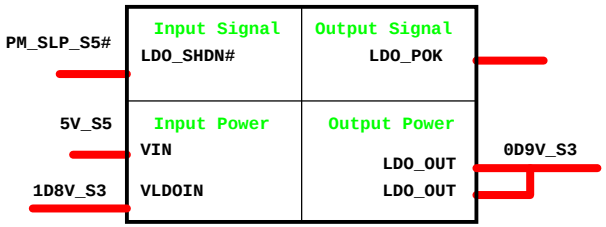
1D2V LDO G9161



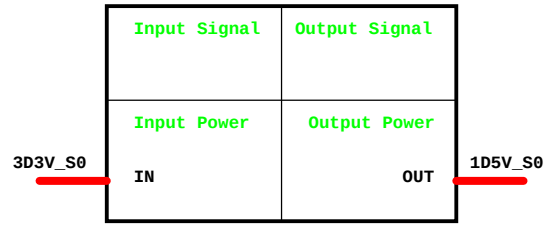
2D5V LDO R9161



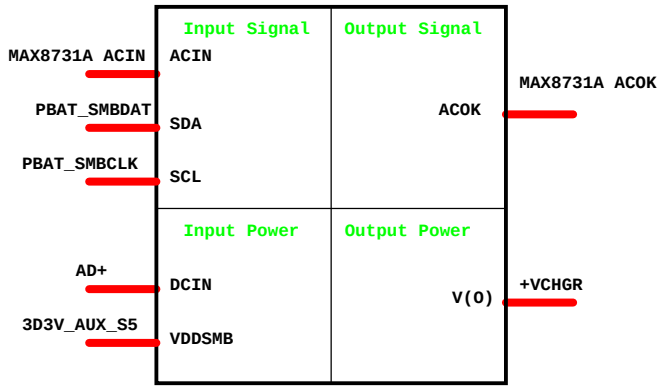
0D9V LDO RT9026



1D5V LDO G9571



CHARGER MAX8731



JV50-TR8

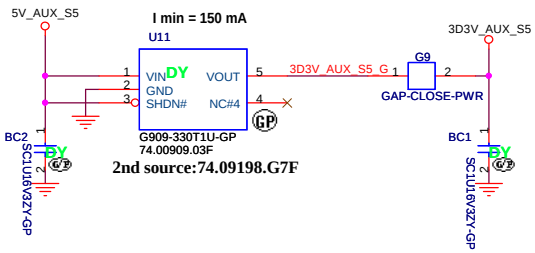
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

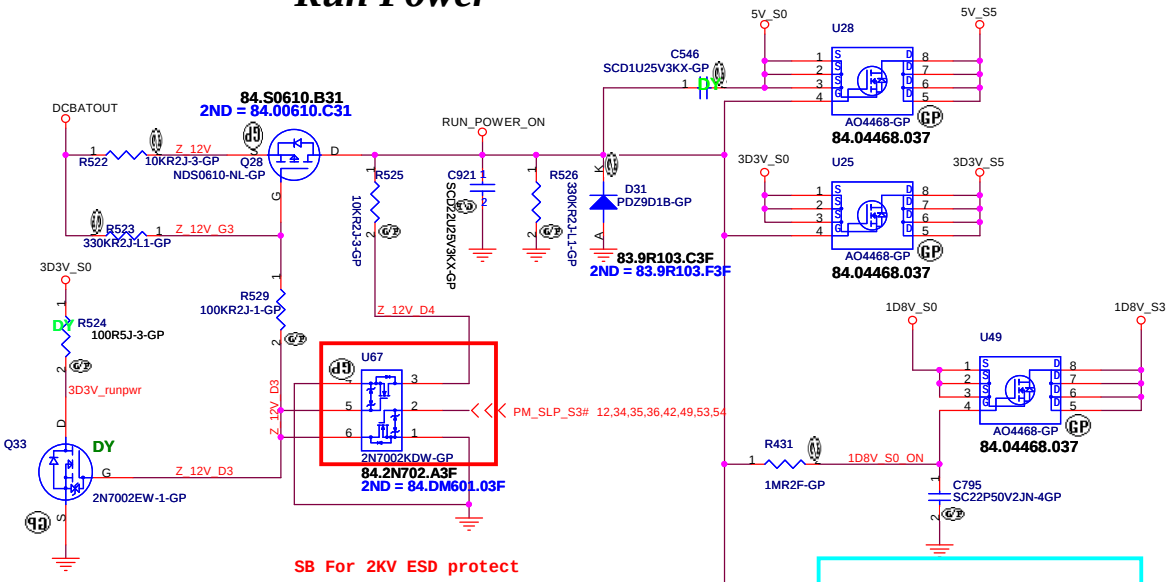
Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 05, 2009 Sheet 43 of 63

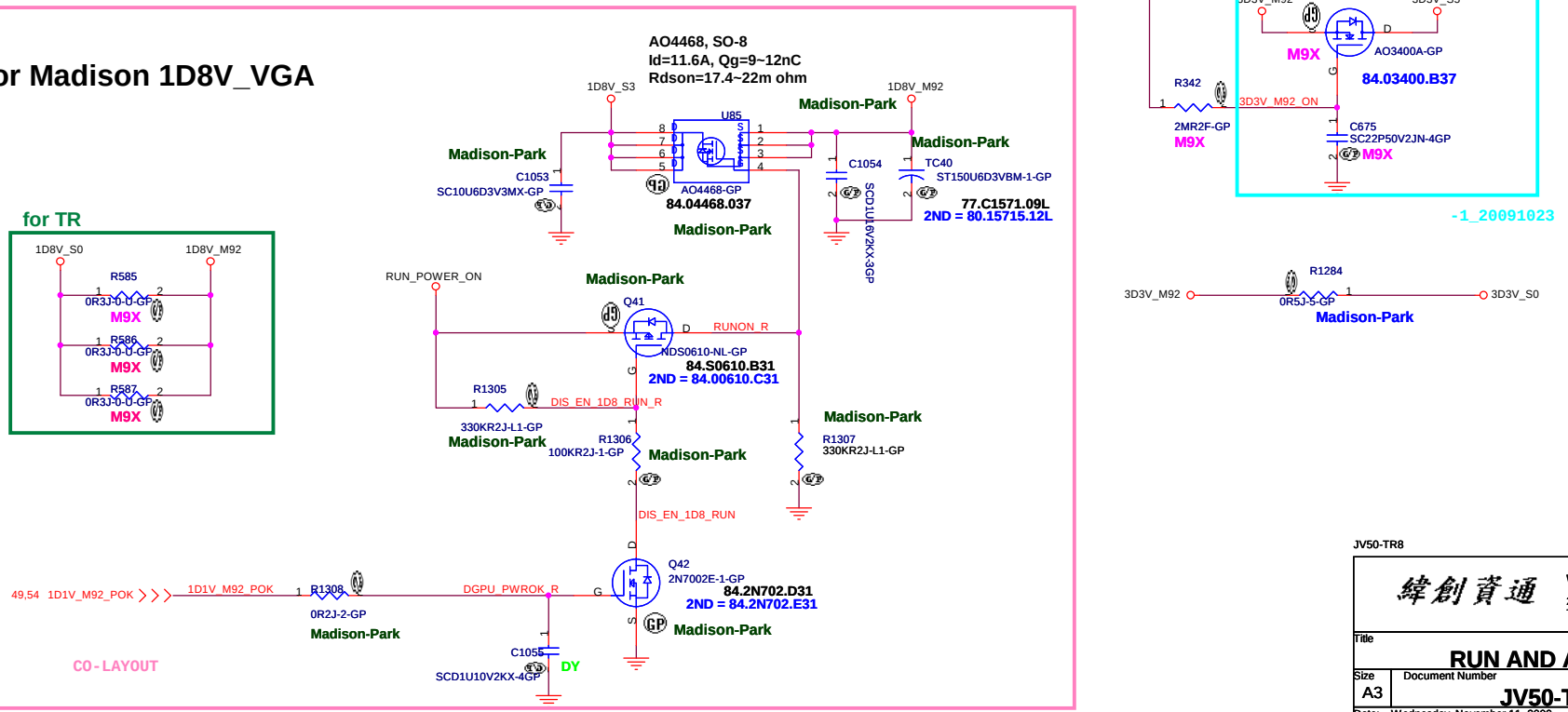
Aux Power 3D3V_AUX_S5



Run Power

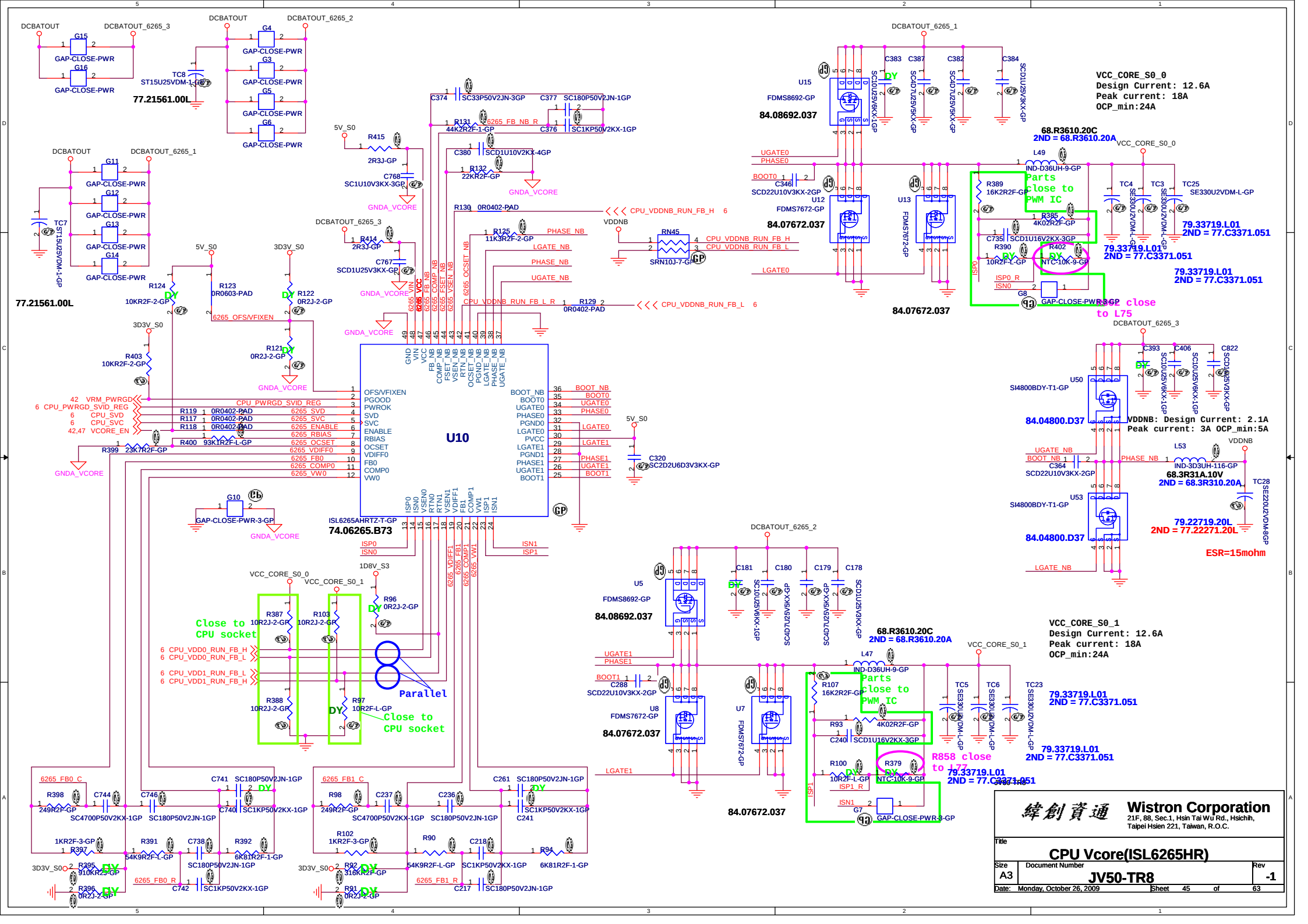


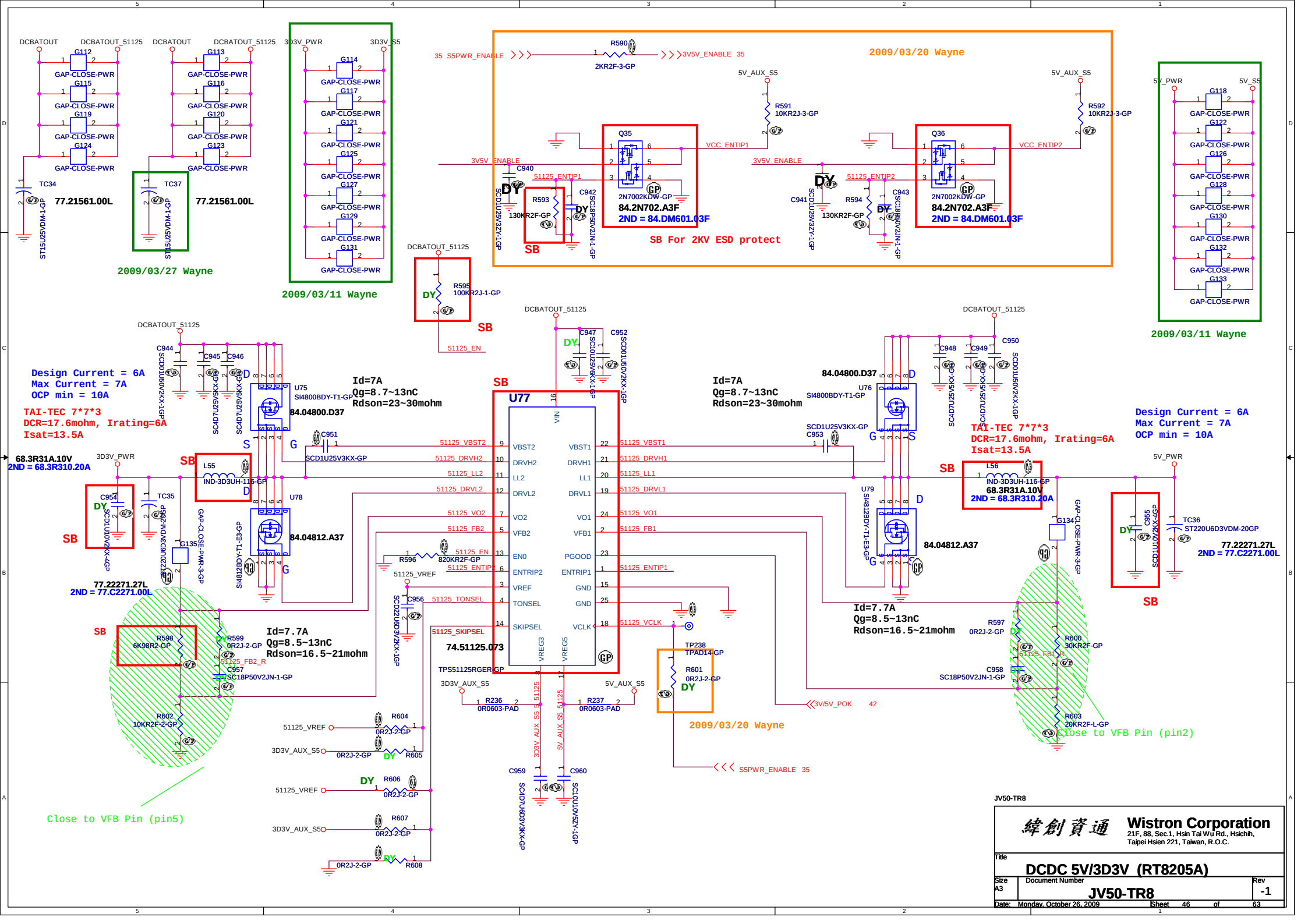
For Madison 1D8V_VGA

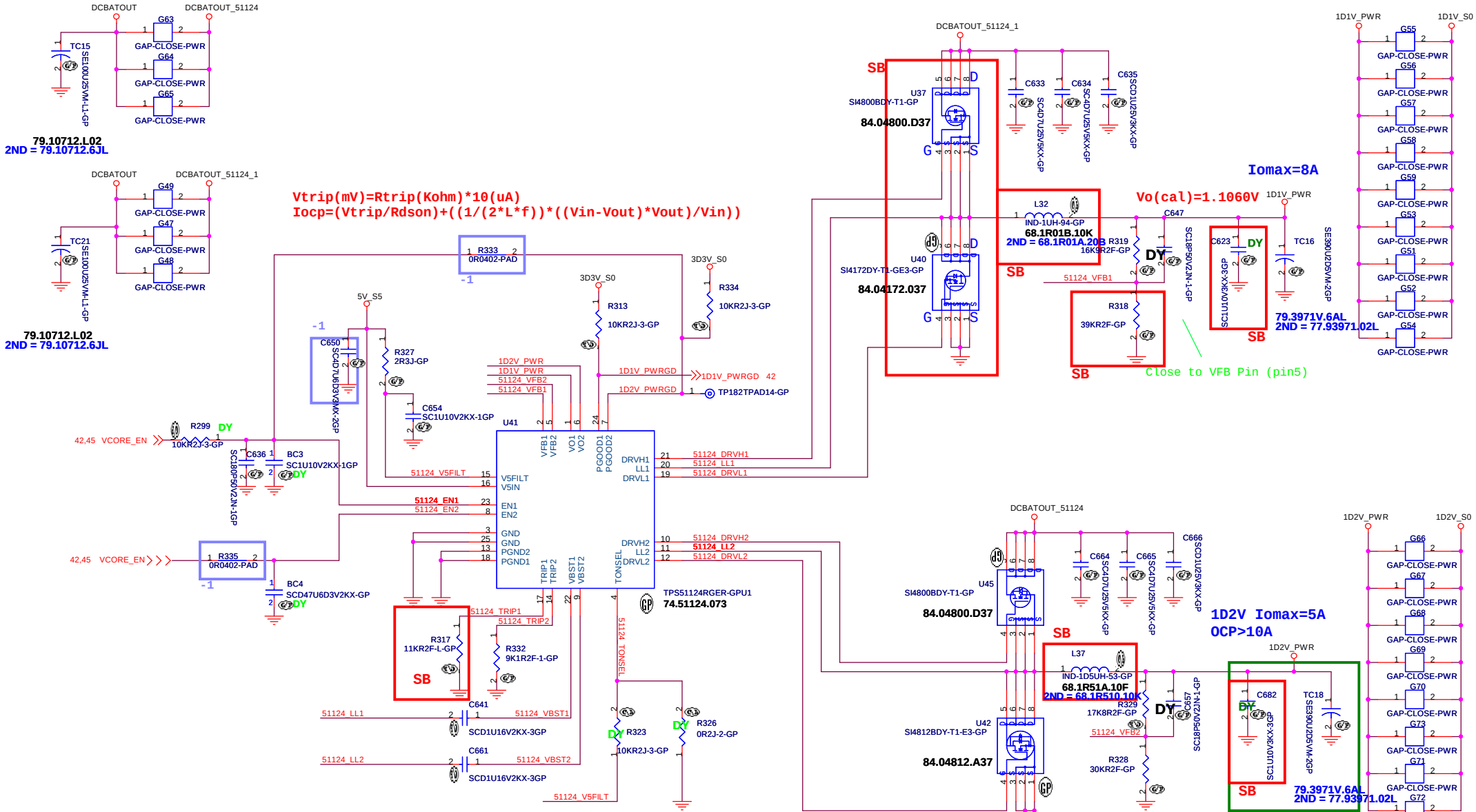


JV50-TR8

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RUN AND AUX POWER		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Wednesday, November 11, 2009	Sheet 44 of 63	


U10
ISL6265AHRTZ-T-GP
74.06265.B73
U15
FDMS8692-GP
84.08692.037
U12
FDMS7672-GP
84.07672.037
U13
U50
SI4800BDY-T1-GP
84.04800.D37
U53
U5
U8
U7
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
68.R3610.20C
2ND = 68.R3610.20A
68.3R31A.10V
2ND = 68.3R310.20A
79.33719.L01
2ND = 77.C3371.051
79.22719.20L
2ND = 77.22271.20L
ESR=15mohm
Parts close to PWM IC
R389 close to L75
R858 close to L77
Close to CPU socket
Parallel
77.21561.00L
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
JV50-TR8
Rev -1
Date: Monday, October 26, 2009
Sheet 45 of 63


DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_PWR
5V_S5
5V_AUX_S5
GAP-CLOSE-PWR
77.21561.00L
ST15U25VDM-1-GP
2009/03/27 Wayne
2009/03/11 Wayne
2009/03/20 Wayne
35 S5PWR_ENABLE
3V5V_ENABLE 35
2KR2F-3-GP
R590
R591 10KR2J-3-GP
R592 10KR2J-3-GP
Q35
Q36
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
VCC_ENTIP1
VCC_ENTIP2
3V5V_ENABLE
51125_ENTIP1
51125_ENTIP2
C940
C941
C942
C943
R593 130KR2F-GP
R594 130KR2F-GP
SCD1U25V3ZY-1GP
SCD1U25V3KX-GP
SCD18P50V2JN-1-GP
DY
SB
SB For 2KV ESD protect
R595 100KR2J-1-GP
51125_EN
Design Current = 6A
Max Current = 7A
OCP min = 10A
TAI-TEC 7*7*3
DCR=17.6mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
U75
SI4800BDY-T1-GP
84.04800.D37
U76
U77
U78
U79
SI4812BDY-T1-E3-GP
84.04812.A37
SCD1U25V3KX-GP
SCD1U10V2KX-1GP
SCD1U50V2KX-1GP
SC4D7U25V5KX-GP
SCD22U6D3V2KX-1GP
SC4D7U6D3V3KX-GP
SCD1U10V2KX-4GP
68.3R31A.10V
2ND = 68.3R310.20A
L55
L56
IND-3D3UH-116-GP
C954
C955
TC35
TC36
ST220U6D3VDM-20GP
77.22271.27L
2ND = 77.C2271.00L
G135
G134
GAP-CLOSE-PWR-3-GP
R596 820KR2F-GP
R597 0R2J-2-GP
R598 6K98R2-GP
R599 0R2J-2-GP
R600 30KR2F-GP
R601 0R2J-2-GP
R602 10KR2F-2-GP
R603 20KR2F-L-GP
C956
C957
C958
TP238 TPAD14-GP
TPS51125RGER-GP
VIN
VBST2
VBST1
DRVH2
DRVH1
LL2
LL1
DRVL2
DRVL1
VO2
VO1
VFB2
VFB1
EN0
PGOOD
ENTRIP2
ENTRIP1
VREF
GND
TONSEL
SKIPSEL
VCLK
VREG3
VREG5
51125_VBST2
51125_VBST1
51125_DRVH2
51125_DRVH1
51125_LL2
51125_LL1
51125_DRVL2
51125_DRVL1
51125_VO2
51125_VO1
51125_FB2
51125_FB1
51125_EN
51125_ENTIP2
51125_ENTIP1
51125_VREF
51125_TONSEL
51125_SKIPSEL
51125_VCLK
74.51125.073
3V/5V_POK 42
S5PWR_ENABLE 35
3D3V_AUX_S5
5V_AUX_S5
R236 0R0603-PAD
R237 0R0603-PAD
R604 0R2J-2-GP
R605 0R2J-2-GP
R606 0R2J-2-GP
R607 0R2J-2-GP
R608 0R2J-2-GP
C959
C960
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
JV50-TR8
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 5V/3D3V (RT8205A)
Size A3
Document Number
JV50-TR8
Rev -1
Date: Monday, October 26, 2009
Sheet 46 of 63



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

JV50-TR8

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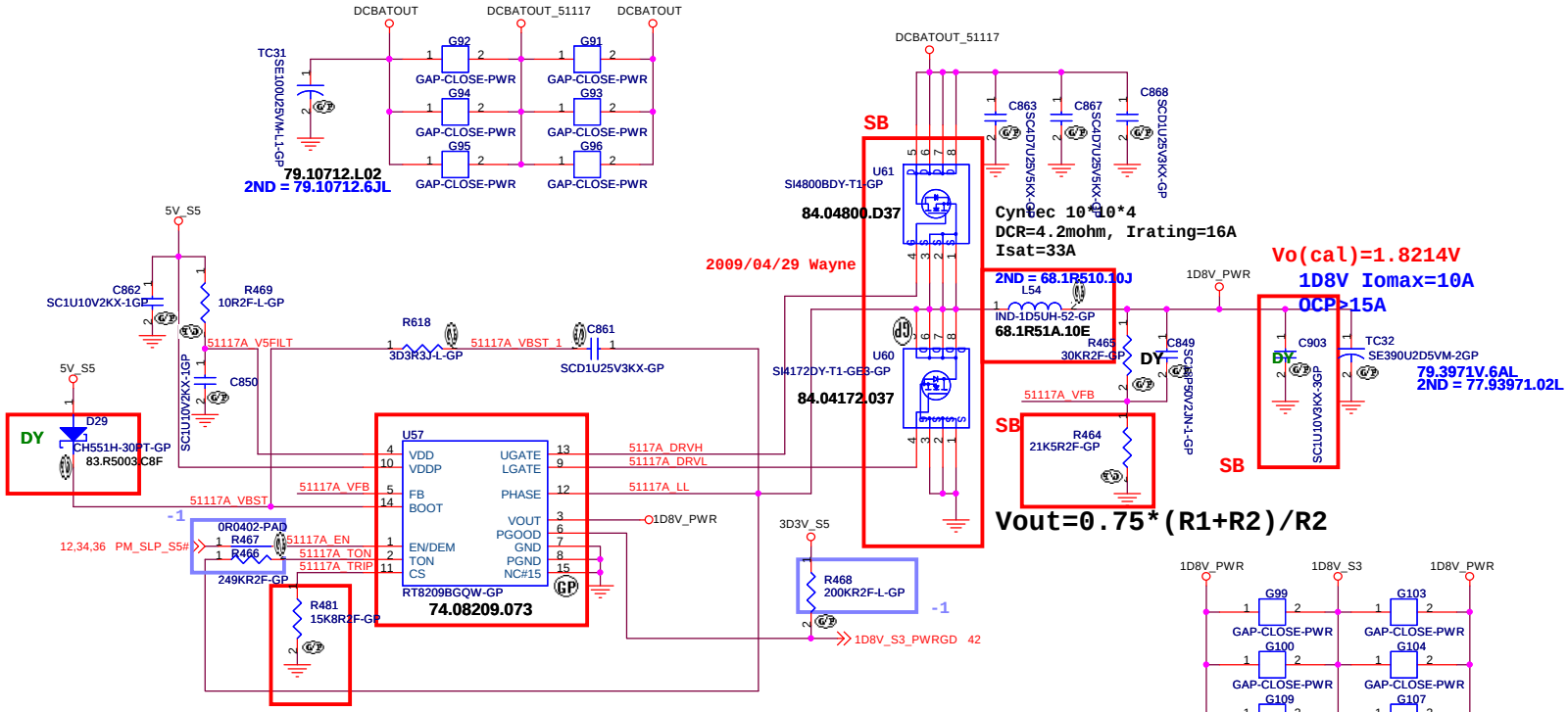
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D1V_1D2V

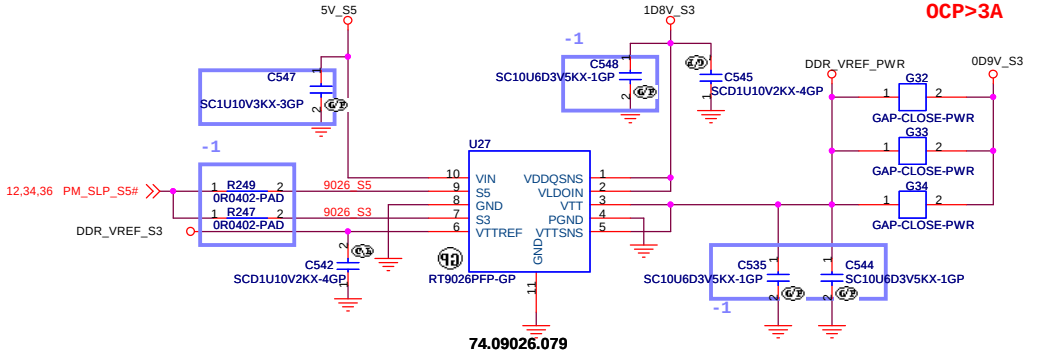
Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 26, 2009 Sheet 47 of 63



DDR_0.9V

Iomax=1.5A
OCP>3A



JV50-TR8

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

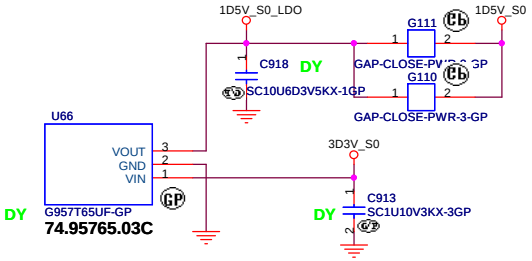
Title: DCDC_1D8V_RT8209B/LDO 0D9V

Size	Document Number	Rev
A3	JV50-TR8	-1

Date: Monday, October 26, 2009 Sheet 48 of 63

G957

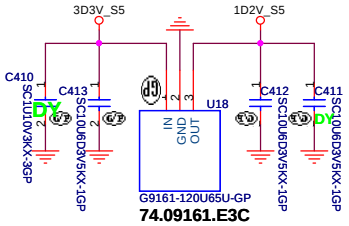
1D5V_S0
Iomax=1A



For MINI Card.NEW Card power SW

G9161

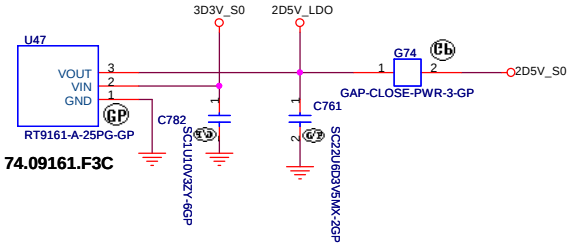
1D2V_S5
Iomax=400mA



Place near to SB710

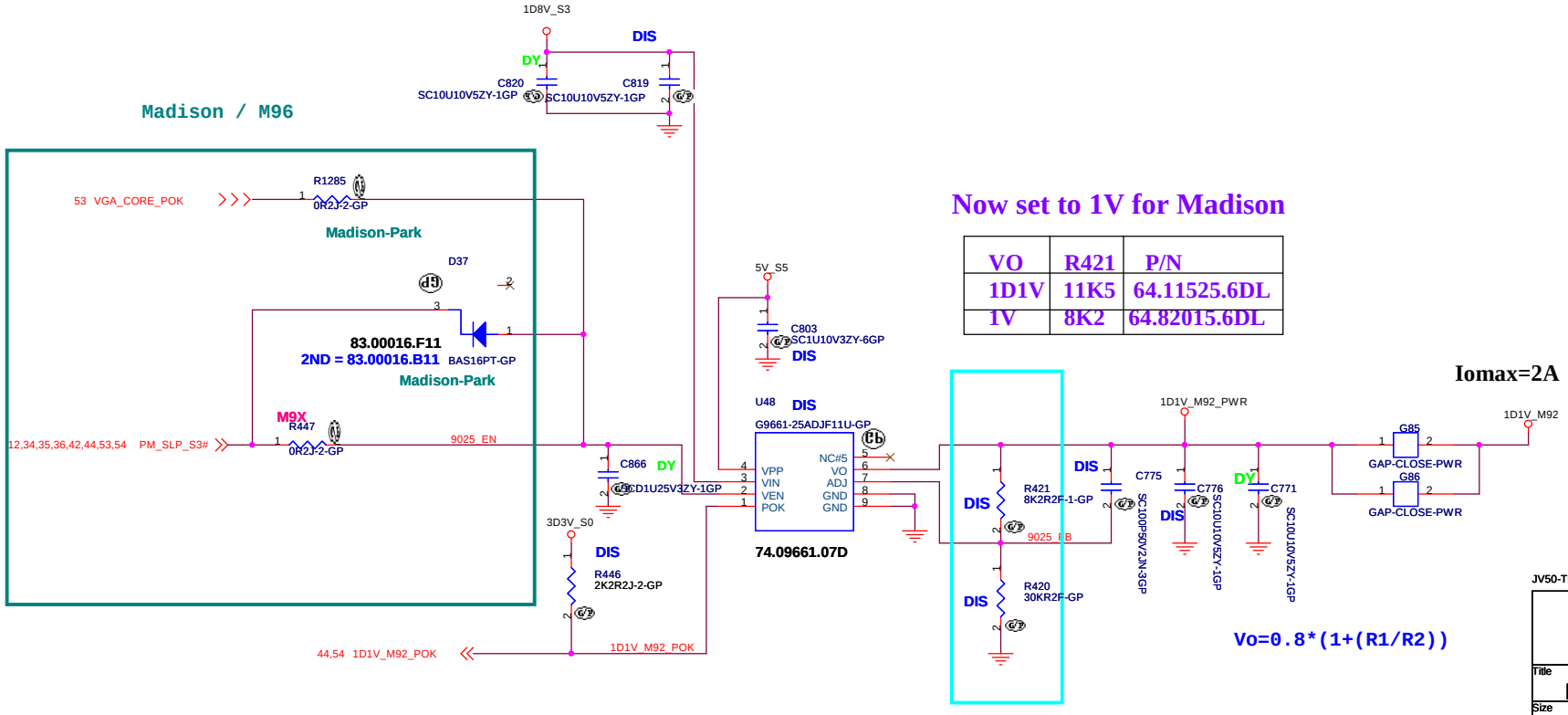
RT9161A

2D5V
Iomax=0.2A



Place near to CPU

Madison / M96



-1_20091019

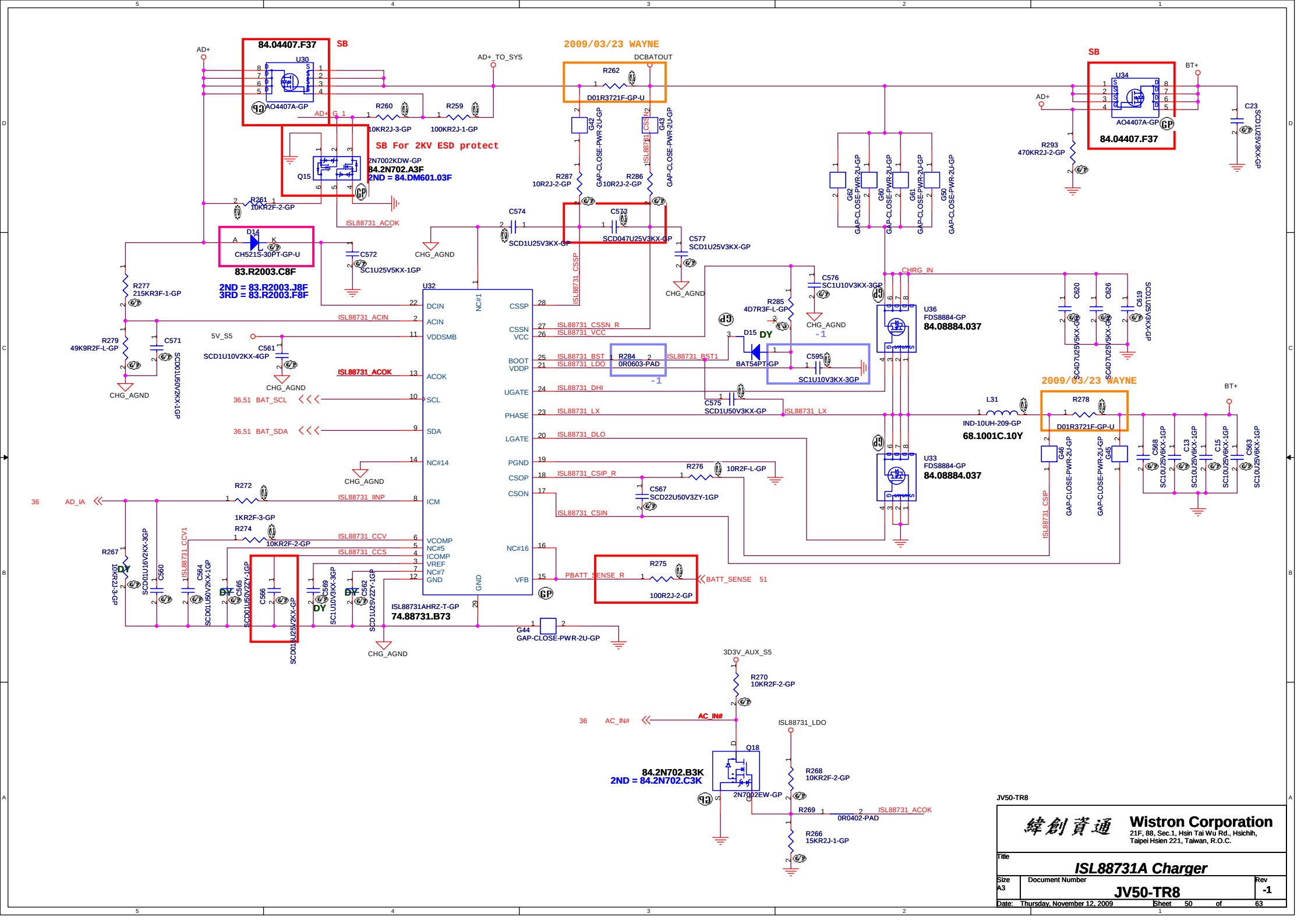
JV50-TR8

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

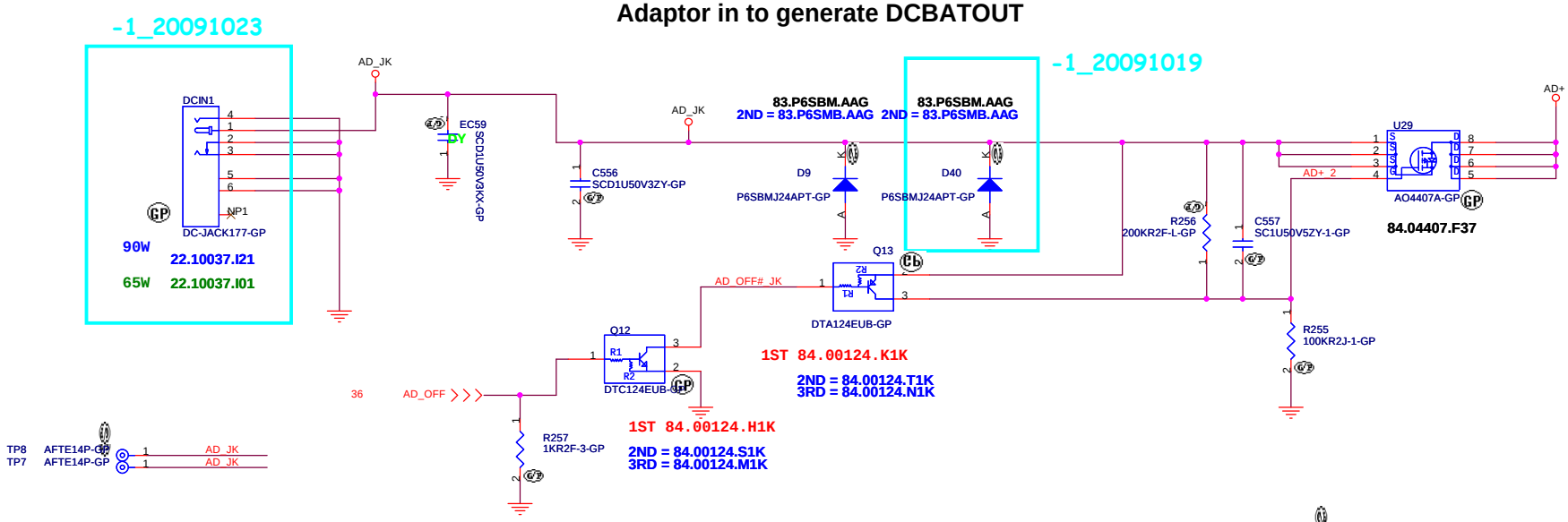
Title: LDO 2D5V/1D5V/1D2V_S5/1V_VGA

Size	Document Number	Rev
A3	JV50-TR8	-1

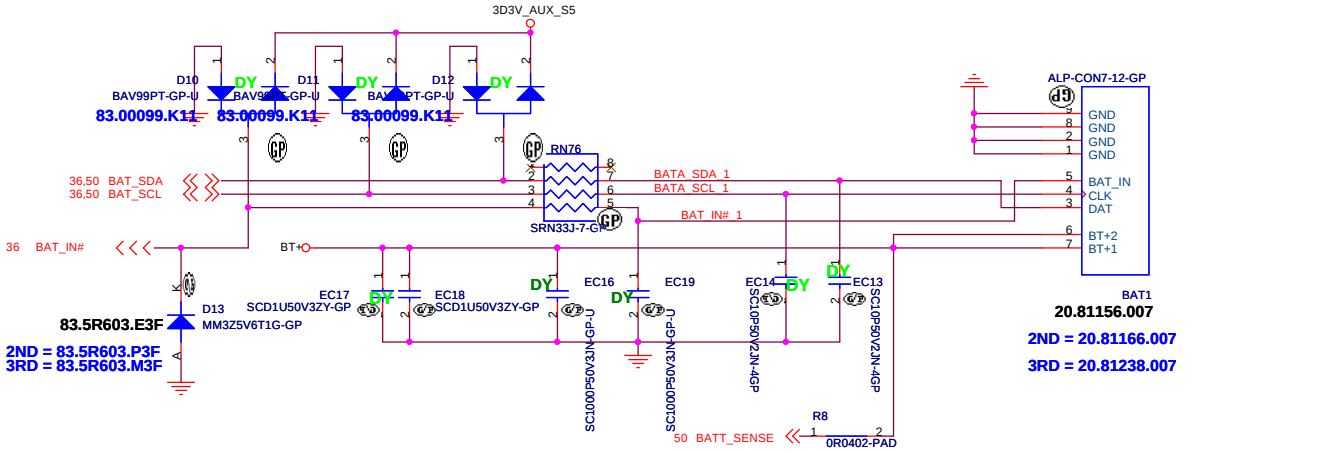
Date: Wednesday, November 11, 2009 Sheet 49 of 63


84.04407.F37
SB
U30
AO4407A-GP
AD+
AD+_TO_SYS
2009/03/23 WAYNE
DCBATOUT
R262
D01R3721F-GP-U
SB For 2KV ESD protect
Q15
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
R260
10KR2J-3-GP
R259
100KR2J-1-GP
R261
10KR2F-2-GP
ISL88731_ACOK
D14
CH521S-30PT-GP-U
83.R2003.C8F
2ND = 83.R2003.J8F
3RD = 83.R2003.F8F
C572
SC1U25V5KX-1GP
CHG_AGND
C574
SCD1U25V3KX-GP
C573
SCD047U25V3KX-GP
C577
SCD1U25V3KX-GP
R287
10R2J-2-GP
R286
10R2J-2-GP
G42
G43
GAP-CLOSE-PWR-2U-GP
ISL88731_CSSP
ISL88731_CSSN
R277
215KR3F-1-GP
R279
49K9R2F-L-GP
C571
SCD1U50V2KX-1GP
C561
SCD1U10V2KX-4GP
5V_S5
U32
ISL88731AHRZ-T-GP
74.88731.B73
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
ISL88731_ACIN
ISL88731_CSSN_R
ISL88731_VCC
ISL88731_BST
ISL88731_LDO
ISL88731_BST1
ISL88731_DHI
ISL88731_LX
ISL88731_DLO
ISL88731_CSIP_R
ISL88731_CSIN
ISL88731_IINP
ISL88731_CCV
ISL88731_CCS
ISL88731_CCV1
PBATT_SENSE_R
BATT_SENSE
36,51 BAT_SCL
36,51 BAT_SDA
R284
0R0603-PAD
R285
4D7R3F-L-GP
D15
BAT54PT-GP
C595
SC1U10V3KX-3GP
C575
SCD1U50V3KX-GP
C576
SC1U10V3KX-3GP
CHRG_IN
U36
FDS8884-GP
84.08884.037
U33
FDS8884-GP
84.08884.037
L31
IND-10UH-209-GP
68.1001C.10Y
R278
D01R3721F-GP-U
2009/03/23 WAYNE
C620
C626
C619
SCD1U25V3KX-GP
SC4D7U25V5KX-GP
C568
C13
C15
C563
SC10U25V6KX-1GP
G46
G45
GAP-CLOSE-PWR-2U-GP
R272
1KR2F-3-GP
R274
10KR2F-2-GP
R267
10KR2J-3-GP
C560
C564
C565
C566
C569
C562
SCD01U50V2KX-1GP
SCD01U50V2ZY-1GP
SC1U10V3KX-3GP
SCD1U25V2ZY-1GP
SCD01U25V2KX-GP
R276
10R2F-L-GP
C567
SCD22U50V3ZY-1GP
R275
100R2J-2-GP
G44
GAP-CLOSE-PWR-2U-GP
3D3V_AUX_S5
R270
10KR2F-2-GP
AC_IN#
Q18
2N7002EW-GP
84.2N702.B3K
2ND = 84.2N702.C3K
R268
10KR2F-2-GP
R269
0R0402-PAD
R266
15KR2J-1-GP
R293
470KR2J-2-GP
C23
SCD1U25V5KX-GP
BT+
JV50-TR8
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A Charger
Size
A3
Document Number
JV50-TR8
Rev
-1
Date: Thursday, November 12, 2009
Sheet 50 of 63

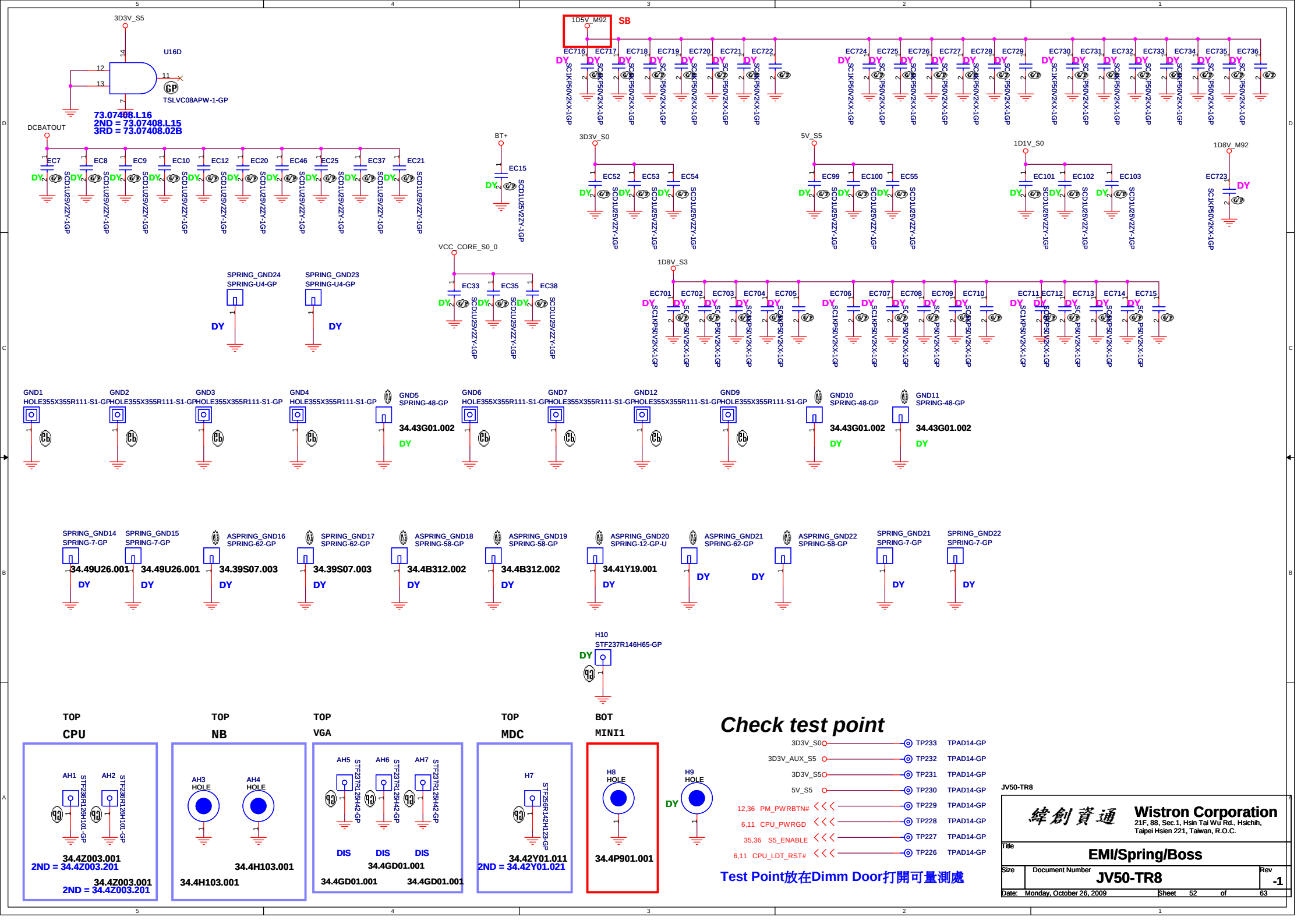
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AD/BATT CONN	
Size	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 51 of 63	



JV50-TR8

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **EMI/Spring/Boss**

Size	Document Number	Rev
	JV50-TR8	-1

Date: Monday, October 26, 2009 Sheet 52 of 63

RT8209E for VGA

Iomax=23A, OCP>40A

DCBATOUT
DCBATOUT_8209E_VGA
G136 GAP-CLOSE-PWR
G138 GAP-CLOSE-PWR
G140 GAP-CLOSE-PWR
G142 GAP-CLOSE-PWR
5V_S5
C1037 DIS SC1U10V2KX-1GP
R1286 DIS 10R2F-L-GP
C1041 DIS SC1U10V2KX-1GP
R1287 3D3R3J-L-GP DIS
8209A_R_BOOT_VGA
C1038 SCD1U16V2KX-3GP DIS
D36 B0530WS-7-F-GP DY
U81 DIS RT8209EGQW-GP
VDD VDDP UGATE LGATE PHASE BOOT FB VOUT PGOOD GND PGND EN/DEM TON CS NC#15
8209A_VDD_VGA
8209A_HGATE_VGA
8209A_LGATE_VGA
8209A_PHASE_VGA
RT8209_FB_VGA
8209A_BOOT
8209A_PGOOD_VGA
VGA_CORE_PWR
8209A_EN/DEM_VGA
8209A_TON_VGA
8209A_CS_VGA
R1288 8K2R2F-1-GP DIS
R1290 220KR2F-GP DIS
R1289 10KR2J-3-GP M9X
12,34,35,36,42,44,49,54 PM_SLP_S3#
D38
83.00016.F11
2ND = 83.00016.B11
BAS16PT-GP Madison-Park
R1293 10KR2J-3-GP Madison-Park
3D3V_M92
C1043 16KR3F-GP DIS
3D3V_S0
R1291 10KR2J-3-GP DIS
R1292 0R0402-PAD-1-GP
VGA_CORE_POK 49
C1042 SC100P50V2JN-3GP DIS
-1_20091021

U80 U82 U83 SIR474DP-T1-GE3-GP SIR460DP-T1-GE3-GP
DCBATOUT_8209E_VGA
C1039 C1040 C1056 SC1U25V5KX-GP DIS
L62 IND-D45UH-14-GP DIS
-1_20091021
VGA_CORE_PWR
TC38 TC39 SE330U2VDM-L-GP DIS
79.33719.L01

Vout=0.75*(1+Rh/Rl)

C1044 SC47P50V2JN-3GP DY
R1294 10KR2F-2-GP DIS
RT8209_FB_VGA
R1295 49K9R2F-L-GP DIS
R1296 110KR2F-L-GP DY
NV_VID1_Q
Q39 84.2N702.B3K 2ND = 84.2N702.C3K 2N7002EW-GP
R1298 10KR2J-3-GP DY
NV_VID1
PWRCNTL_1 56
C1046 SCD1U10V2KX-4GP DY
R1297 73K2R2F-GP DIS
NV_VID0_Q
Q40 2N7002EW-GP 84.2N702.B3K 2ND = 84.2N702.C3K DIS
-1_20091019
3D3V_S0
R1309 100KR2J-1-GP DIS
NV_VID0_R
Q45 MMBT2222A-3-GP
R1299 10KR2J-3-GP DIS
NV_VID0
PWRCNTL_0 56
C1045 SCD1U10V2KX-4GP DIS

M92 XT			
R1295	37.4K	R1297	30K
VGA_CORE	1.20V		

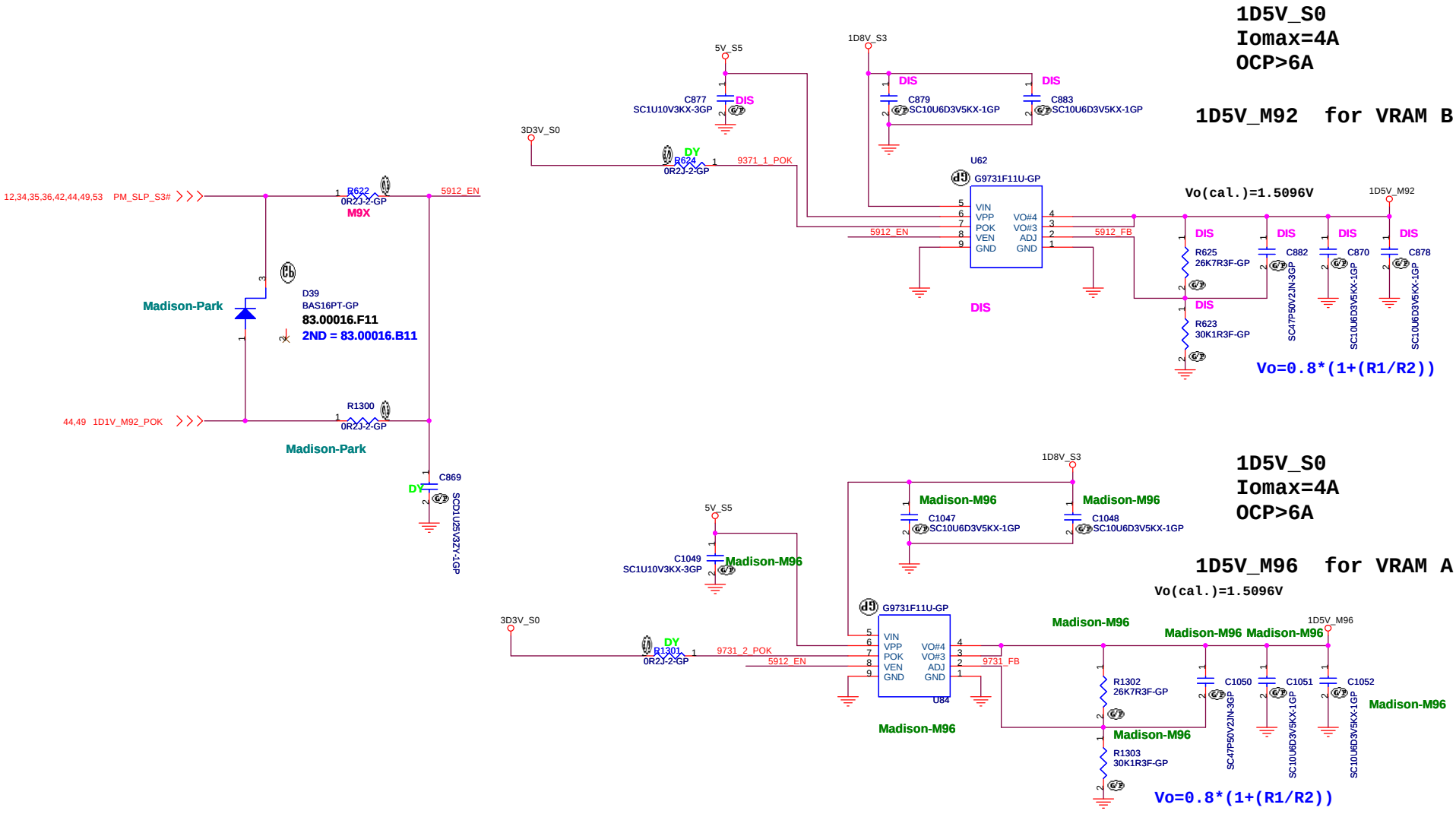
30k(64.30025.6DL)
73.2k(64.73225.6DL)
37.4k (64.37425.6DL)

	Madison Pro	Park XT	M96 Pro
R1297	73.2K	36.5K	30K
VGA_CORE	1.00V	1.12V	1.15V

	Madison Pro	Park XT	M96 Pro	M92-XT
PWRCNTL_0				
0	1.00V	1.12V	1.15V	1.20V
1	0.90V	0.90V	0.90V	0.95V

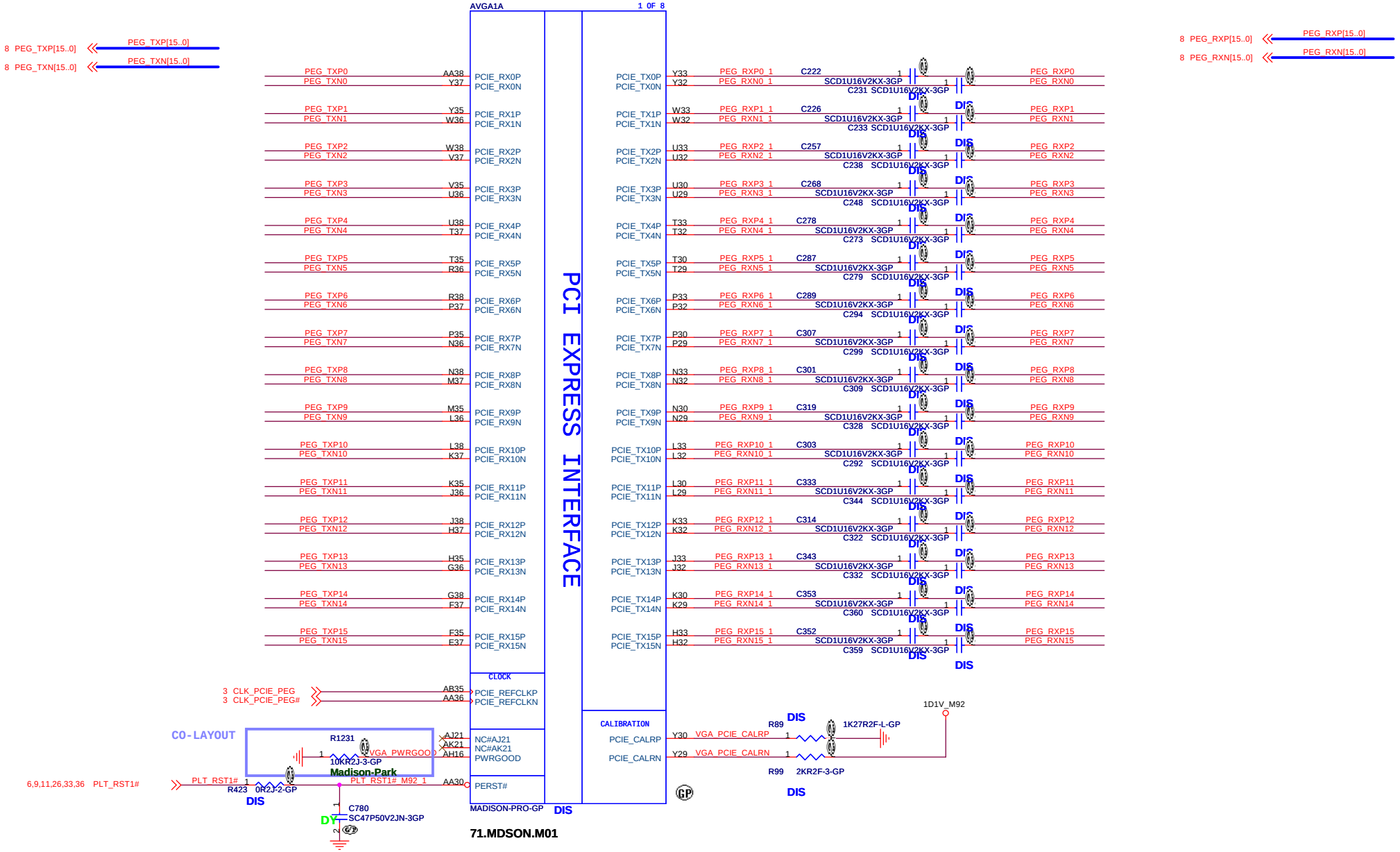
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209E VGA CORE
Size: A3 | Document Number: JV50-TR8 | Rev: -1
Date: Thursday, November 12, 2009 | Sheet 53 of 63



JV50-TR8

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: G9731_1D5V_VRAM POWER		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Wednesday, November 11, 2009	Sheet 54 of 63	



DIS / UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Madison PCIE**	
Size: A3	Document Number: **JV71-TR**	Rev: **-1**
Date: Monday, October 26, 2009	Sheet 55 of 63	

Layout notice:
It should be pleace near HDMI connector

DVPDATA [3:2:1:0] for VRAM type
selection H/W strap
Should provide VRAM Table for VBios
request

DVPDATA [3:0]
0100 1GB GDDR3 Hynix-H5TQ1G63BFR-12C (800MHz)
1000 1GB GDDR3 Samsung-K4W1G1646E-HC12 (800MHz)
1100 1GB GDDR3 ATI (800MHz)

It's strap for GDDR3-136ball
Need to Clarify

Back Bias (body bias) which minimizes
power consumption in battery modes.
PD = Disable
PU = Enable

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

For Thermal sensor

for TR

71.MDSON.M01

71.MDSON.M01

DIS / UMA

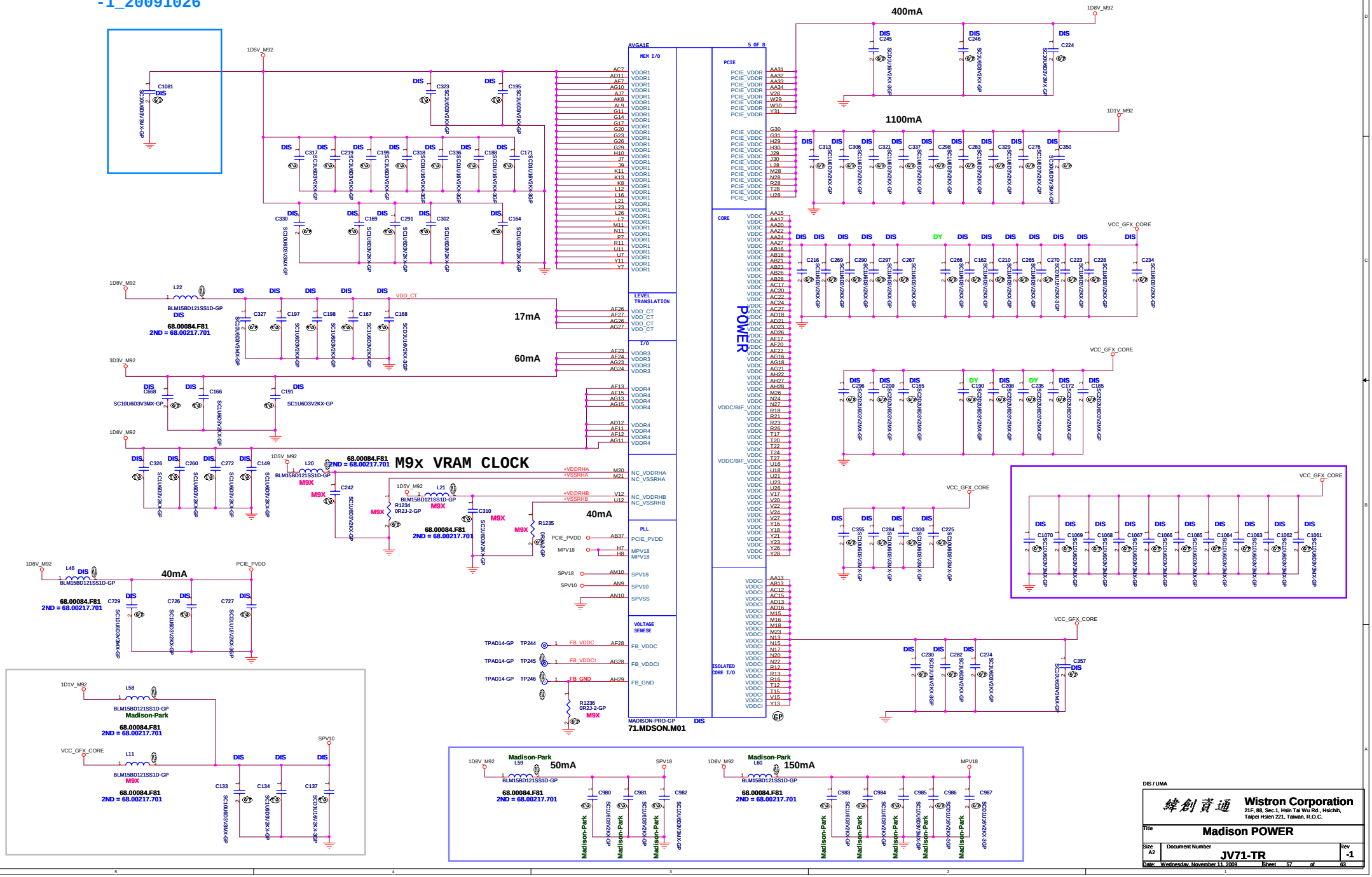
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

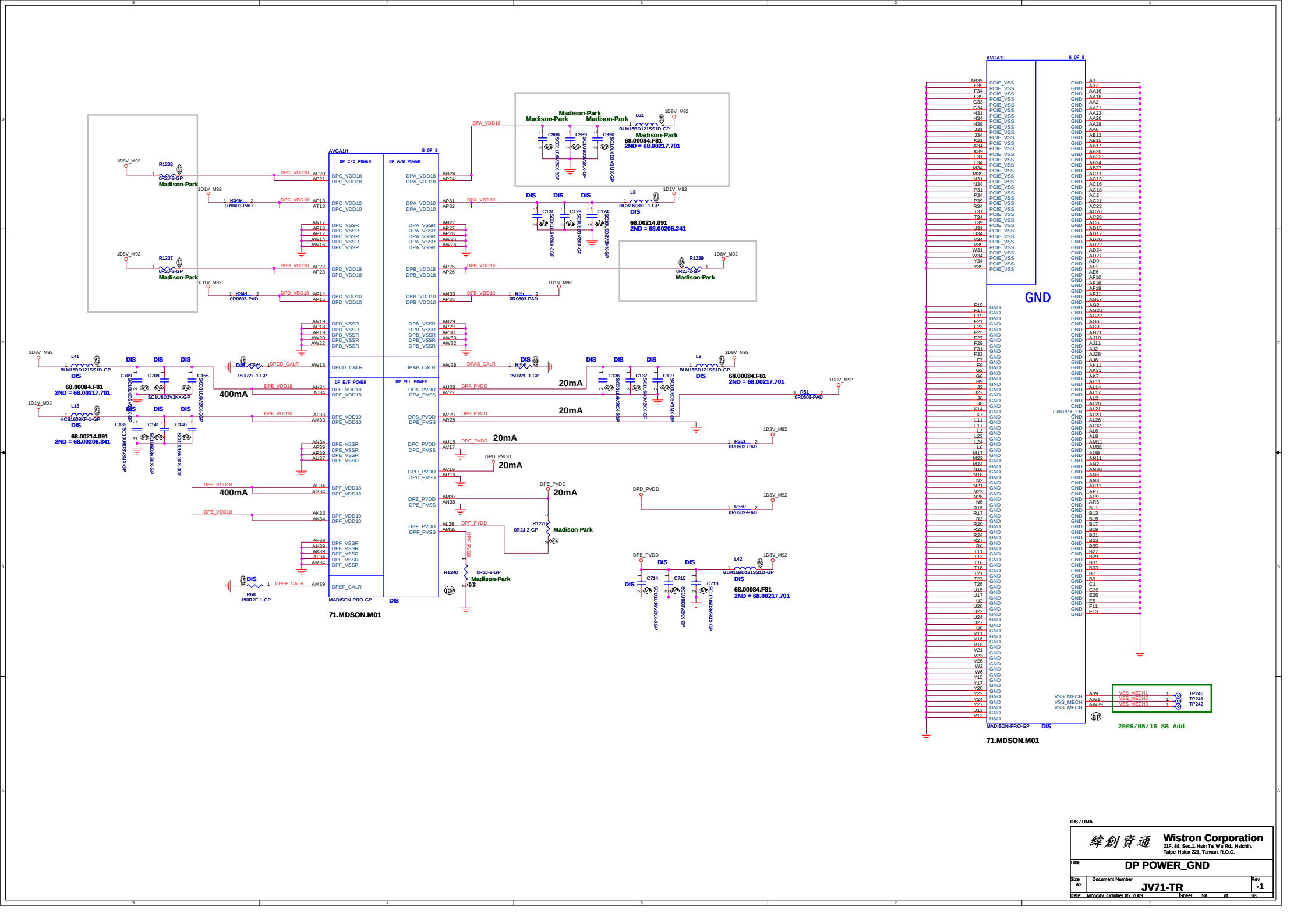
Title: Madison IO

Size: A2 | Document Number: JV71-TR | Rev: -1

Date: Wednesday, November 11, 2009 | Sheet 56 of 63

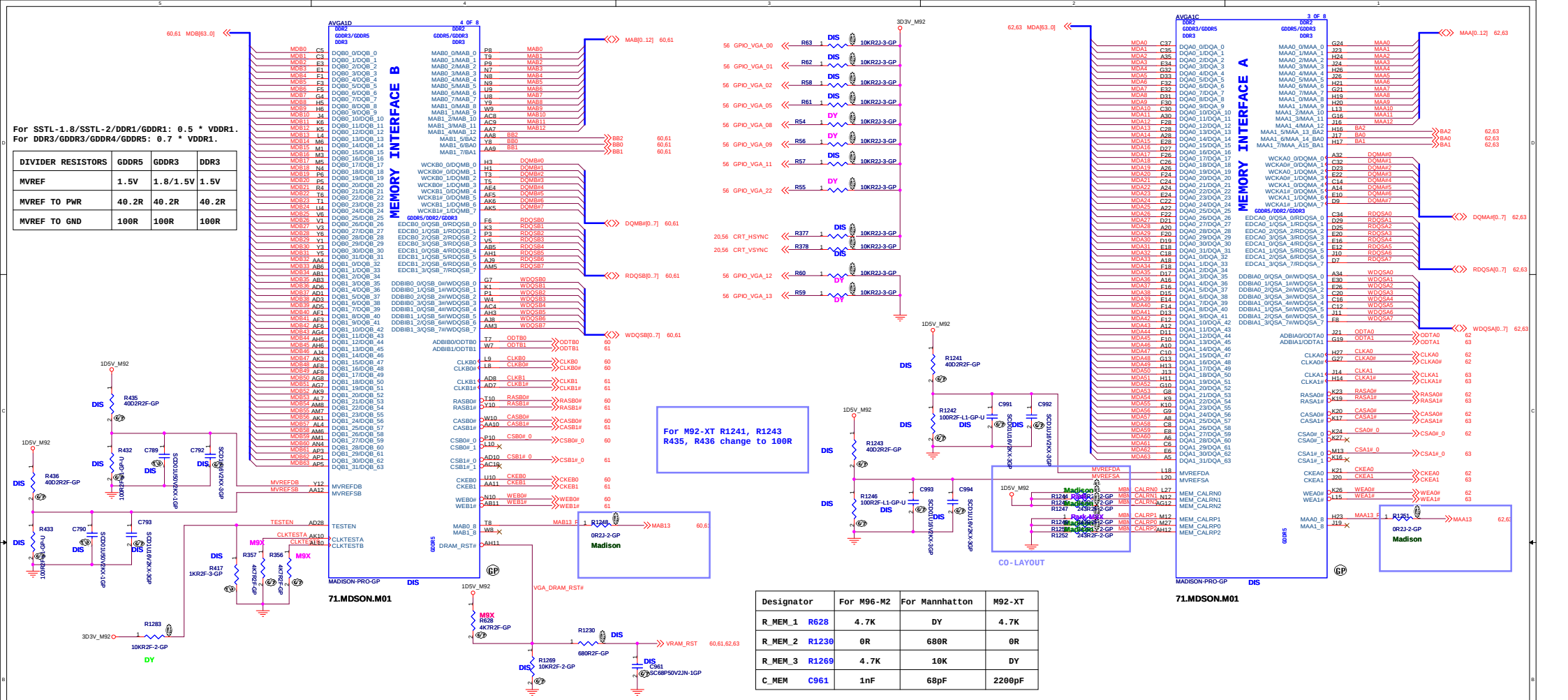
-1_20091026


400mA
1100mA
17mA
60mA
40mA
M9x VRAM CLOCK
50mA
150mA
AVGA1E
MEM I/O
PCIE
CORE
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENESE
ISOLATED CORE I/O
POWER
MADISON-PRO-GP
71.MDSON.M01
Madison-Park
68.00084.F81
2ND = 68.00217.701
BLM15BD121SS1D-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Madison POWER
JV71-TR
-1
Wednesday, November 11, 2009
57
63


AVGA1H
8 OF 8
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
MADISON-PRO-GP
DIS
71.MDSON.M01
AVGA1F
6 OF 8
GND
MADISON-PRO-GP
DIS
71.MDSON.M01
2009/05/16 SB Add
Madison-Park
68.00084.F81
2ND = 68.00217.701
68.00214.091
2ND = 68.00206.341
400mA
20mA
DIS / UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DP POWER_GND
JV71-TR
Rev -1
Monday, October 05, 2009
Sheet 58 of 63

For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R



Designator		For M96-M2	For Mannhatton	M92-XT
R_MEM_1	R628	4.7K	DY	4.7K
R_MEM_2	R1230	0R	680R	0R
R_MEM_3	R1269	4.7K	10K	DY
C_MEM	C961	1nF	68pF	2200pF

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BIF_CLK_PM_EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
PWRCNTL_[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	1
CCBYPASS	GENERICC		0

HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO , GPIO21_BB_EN

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000			
V 256MB	x001			
64MB	x010	ST Microelectronics	M25P05A	0100
32MB	x		M25P10A	0101
512MB	x		M25P20	0101
1GB	x		M25P40	0101
2GB	x		M25P80	0101
4GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
			Pm25LV010A	0101

DIS / UMA

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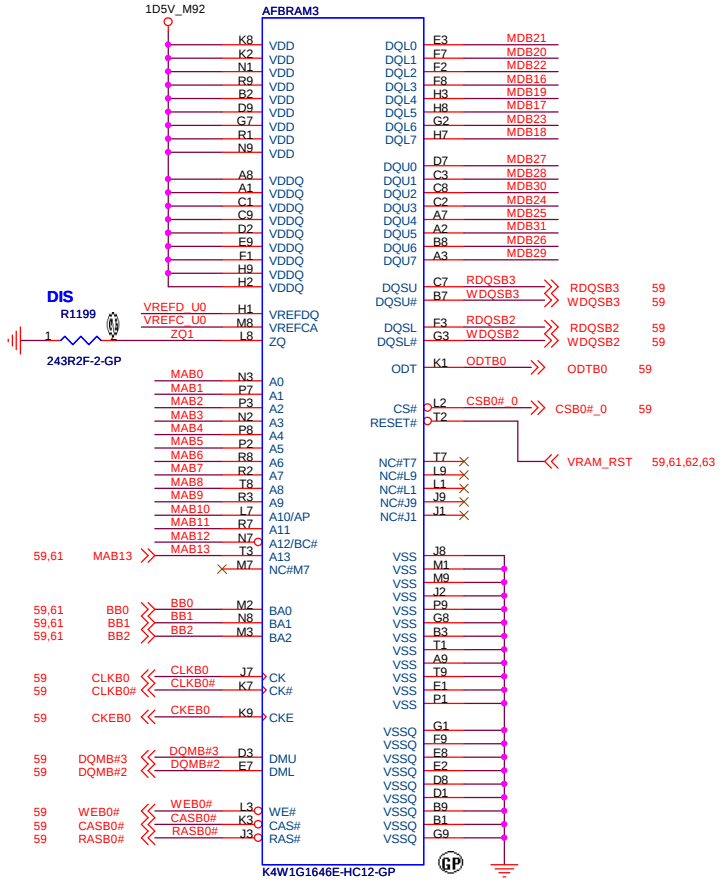
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

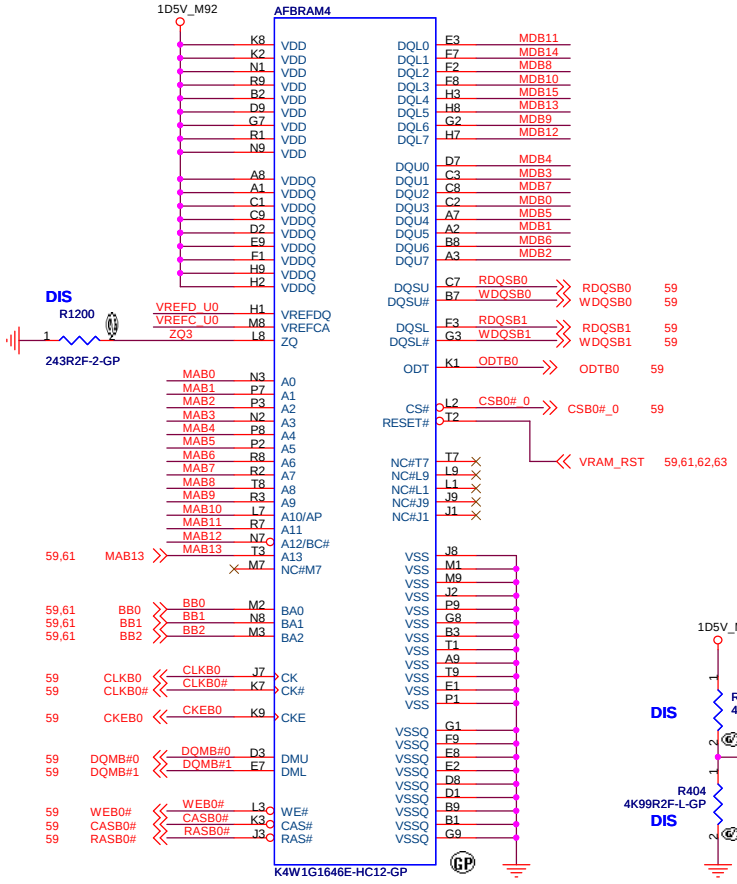
Title: Madison Memory / Straps

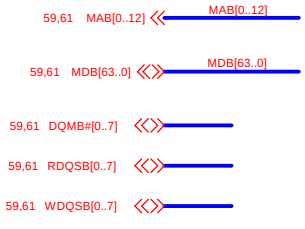
Size: A2 | Document Number: JV71-TR | Rev: -1

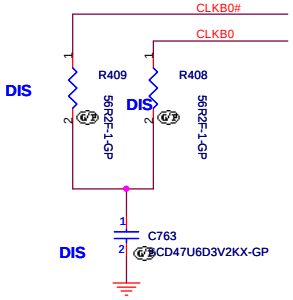
Date: Wednesday, November 11, 2009 | Sheet 59 of 63

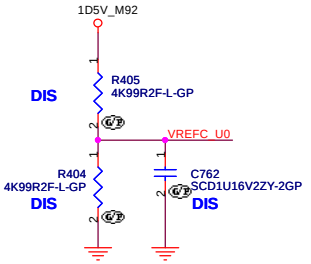
GDDR3

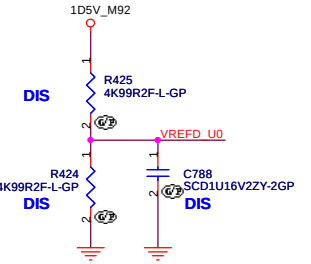












DIS

72.41164.H0U

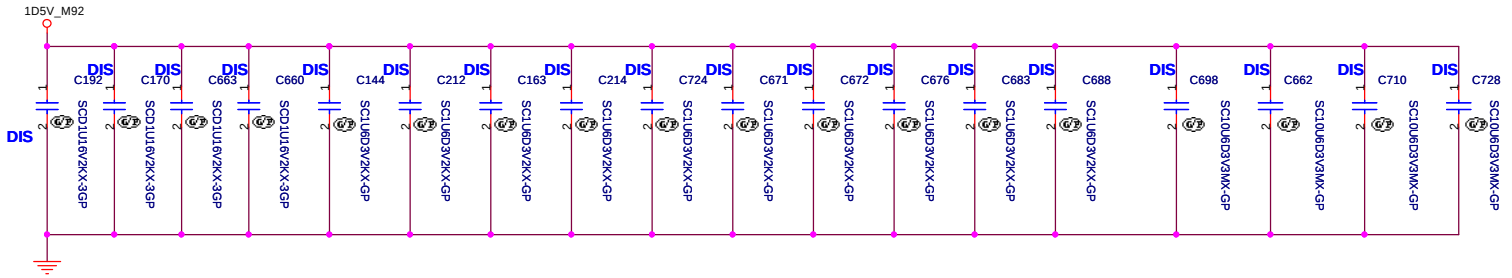
2ND = 72.51G63.C0U

SAMSUNG 1ST=72.41164.H0U
HYUNIX 2ND=72.51G63.C0U

DIS

72.41164.H0U

2ND = 72.51G63.C0U

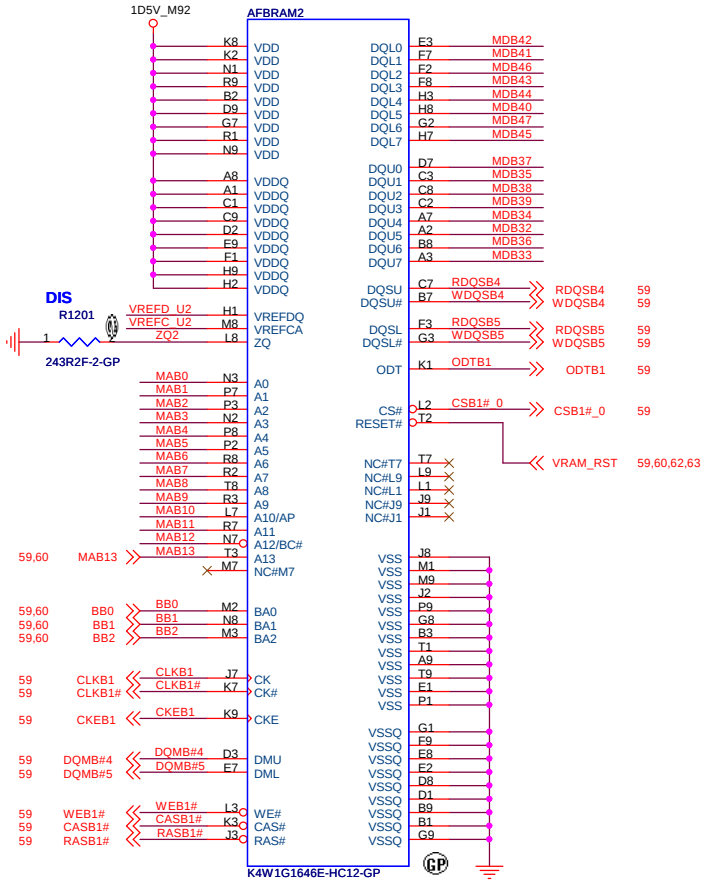


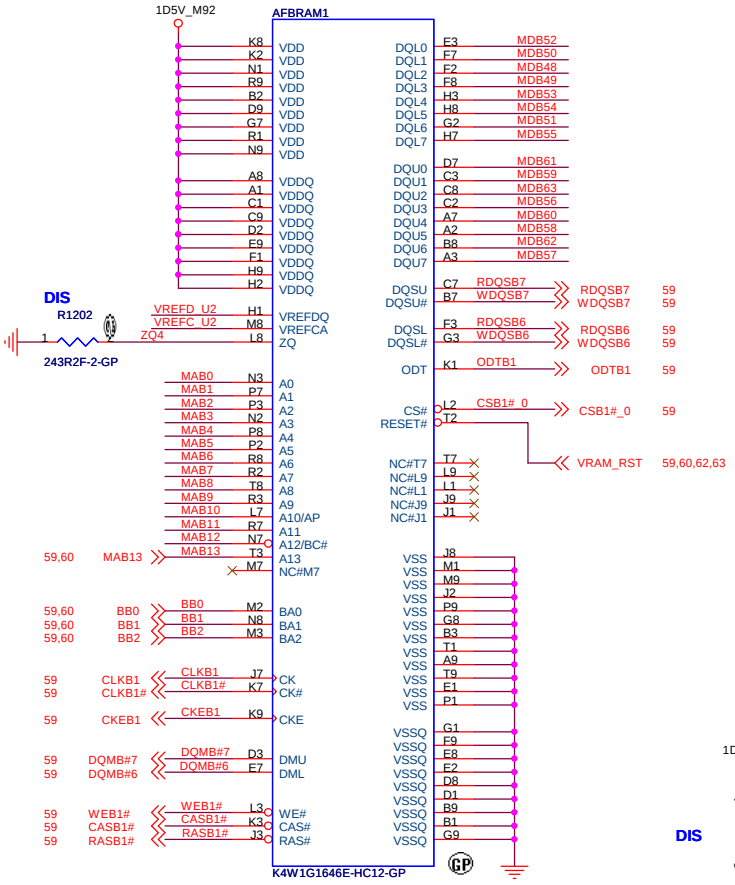
JV50-TR8

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	M92 DDR3 B0	
Size A3	Document Number JV50-TR8	Rev -1
Date: Monday, October 26, 2009	Sheet 60 of 63	

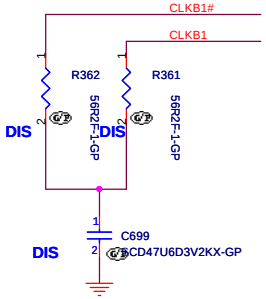
GDDR3

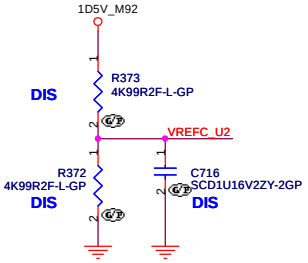


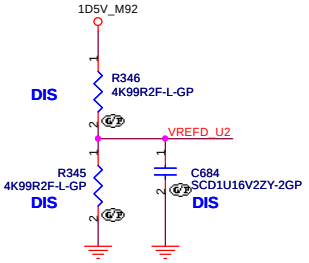


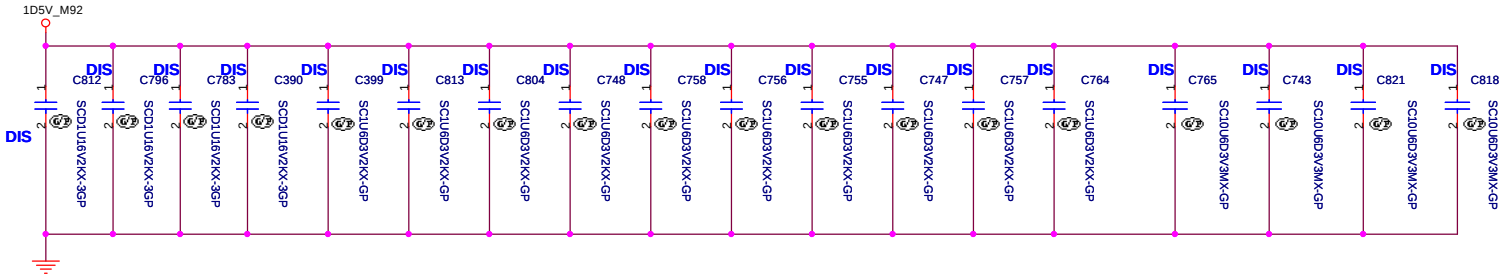
SAMSUNG 1ST=72.41164.H0U
HYUNIX 2ND=72.51G63.C0U

59,60 MAB[0..12]
59,60 MDB[63..0]
59,60 DQMB#[0..7]
59,60 RDQSB[0..7]
59,60 WDQSB[0..7]







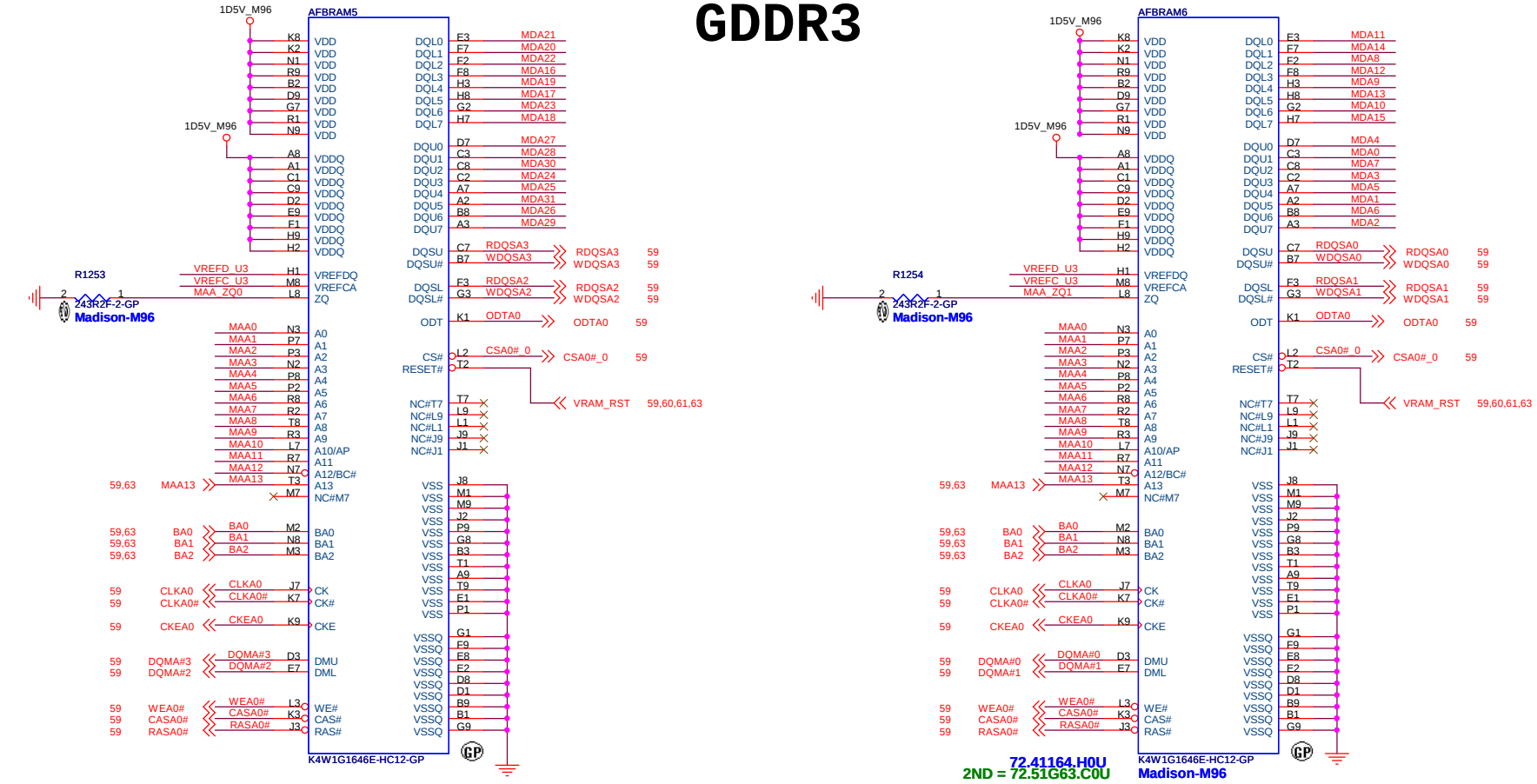


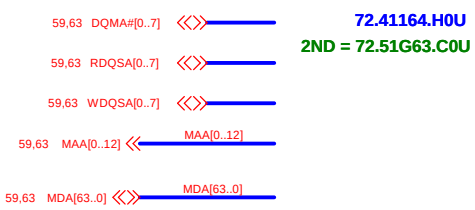
JV50-TR8

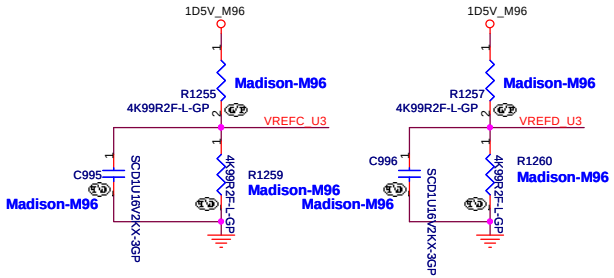
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

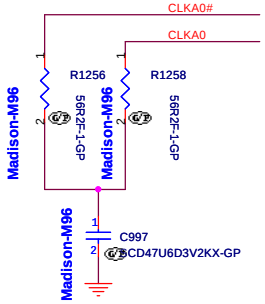
Title	M92 DDR3 B1	
Size A3	Document Number JV50-TR8	Rev -1
Date: Monday, October 26, 2009	Sheet 61 of 63	

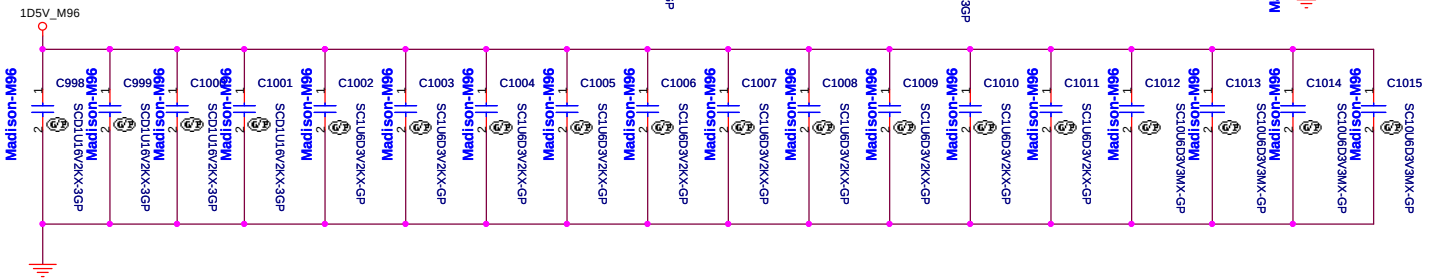
GDDR3







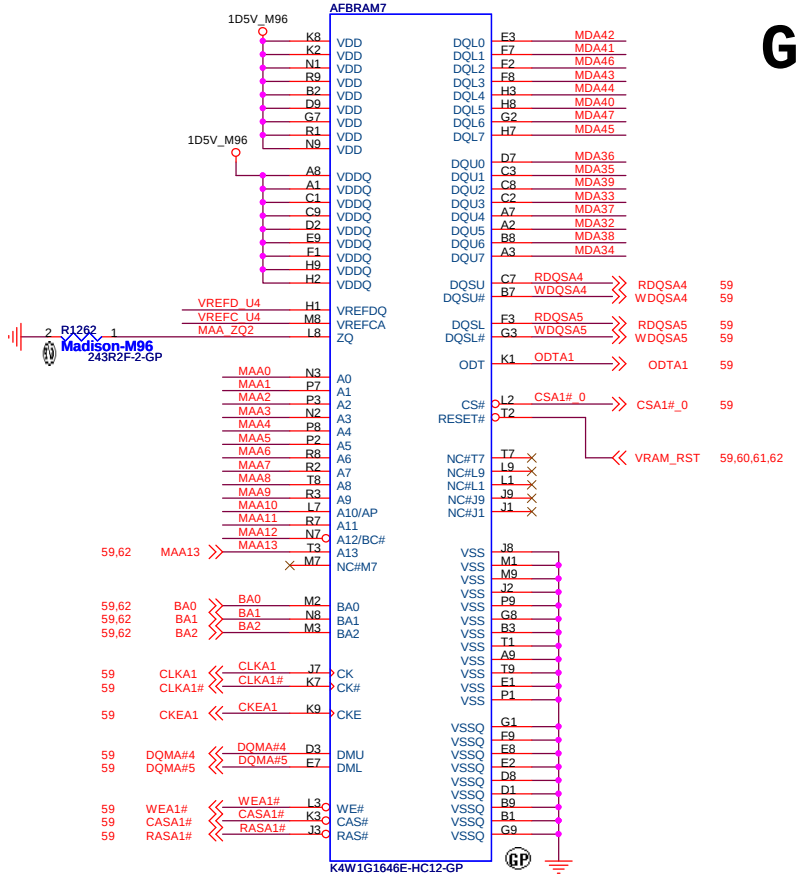


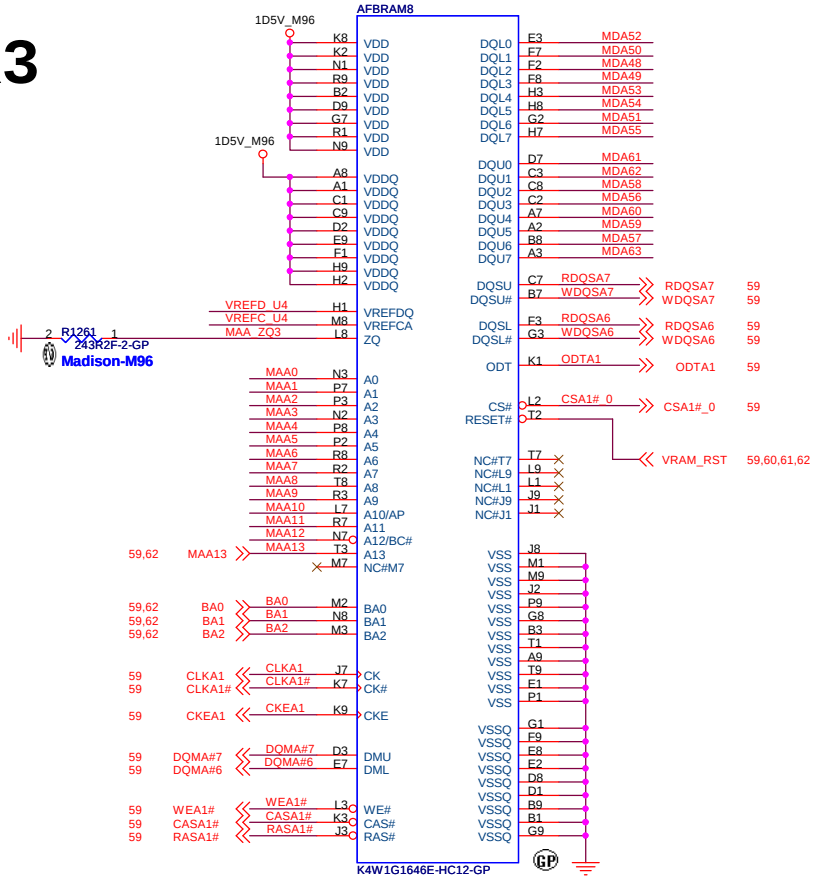


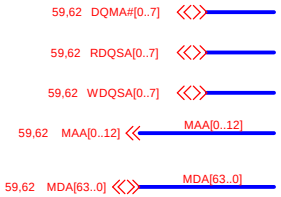
JV50-TR8

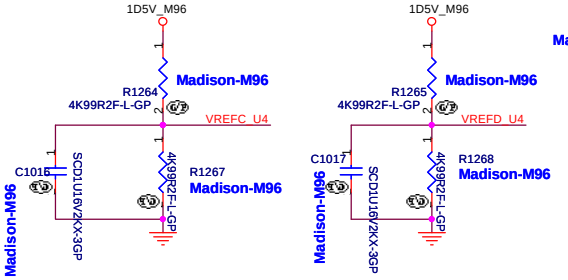
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: M92 DDR3 A0		
Size: A3	Document Number: JV50-TR8	Rev: -1
Date: Monday, October 26, 2009	Sheet 62 of 63	

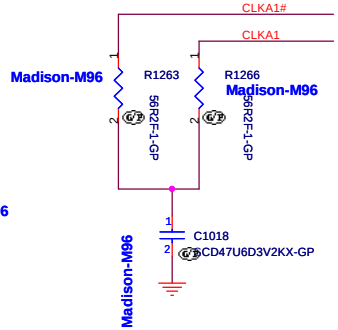
GDDR3

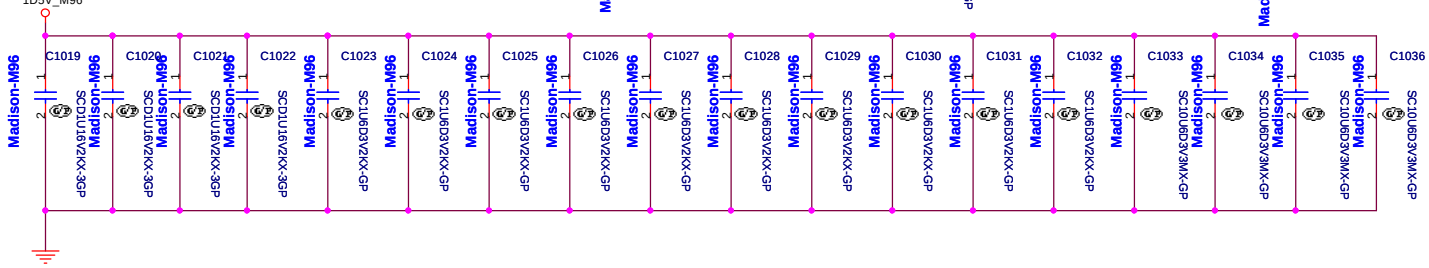












JV50-TR8

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**M92 DDR3 A1**	
Size A3	Document Number **JV50-TR8**	Rev **-1**
Date: Monday, October 26, 2009	Sheet 63 of 63	