

Compal confidential

Schematics Document

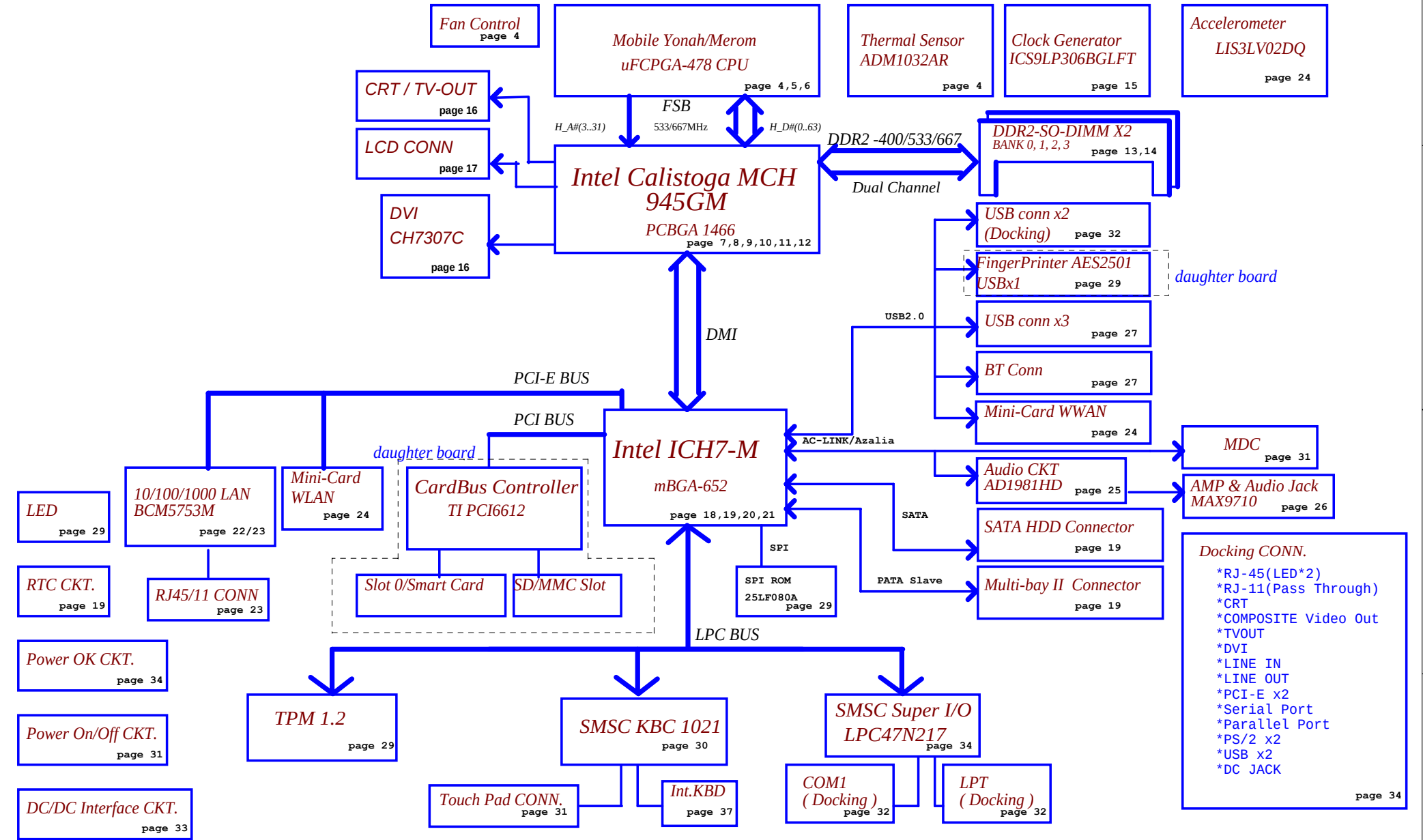
Mobile Yonah uFCPGA with Intel Calistoga_P/GM+ ICH7-M core logic

2006-04-28

REV:1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2005/05/26	Deciphered Date	2006/07/26	Title	Cover Sheet
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Caymus



Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (18.5V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V power rail for Processor I/O and MCH/ICH core power	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_VCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Internal PCI Devices

DEVICE	Bus	PCI Device ID	IDSEL #
LAN	1	D8	AD24
Azalia	0	D27	AD11
PCI-E	0	D28	AD12
USB1.1/2.0	0	D29	AD13
PCI to PCI (DMI to PCI)	0	D30	AD14
AC97 MODEM	0	D30	AD14
AC97 Audio	0	D30	AD14
PATA/SATA	0	D31	AD15
LPC I/F	0	D31	AD15
SMBUS	0	D31	AD15
CPU I/F	0	D31	AD15
DMA	0	D31	AD15
PMU	0	D31	AD15

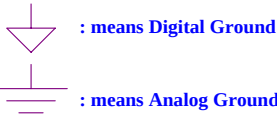
External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
CARD BUS	D6	AD22	2	C D E G

I2C / SMBUS ADDRESSING

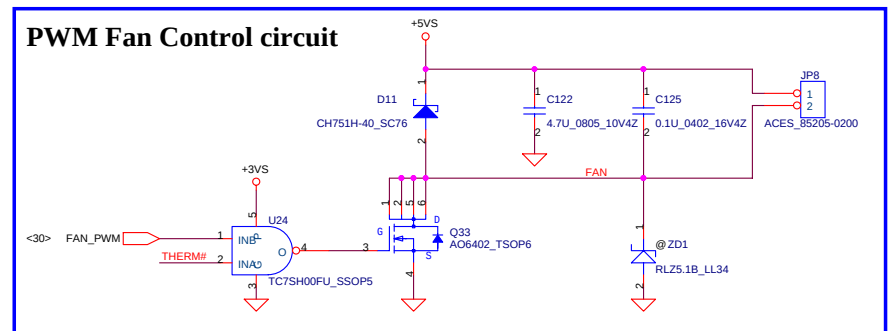
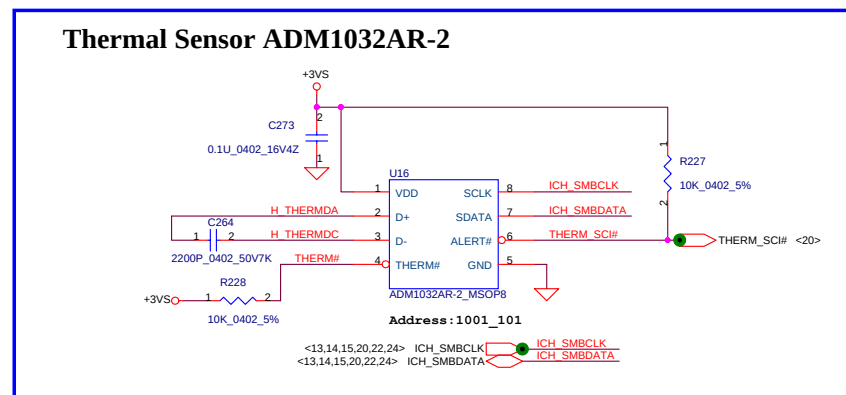
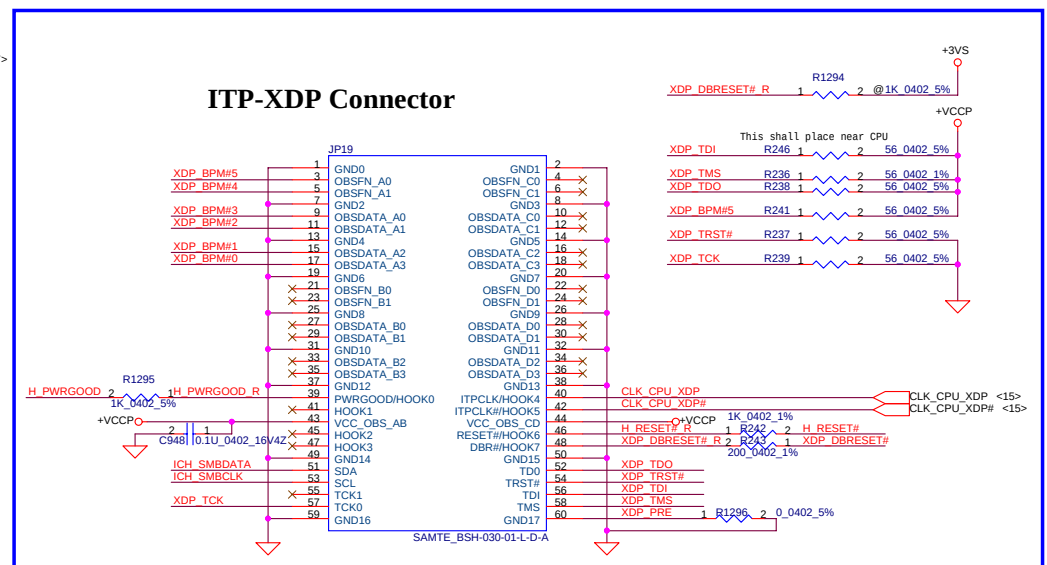
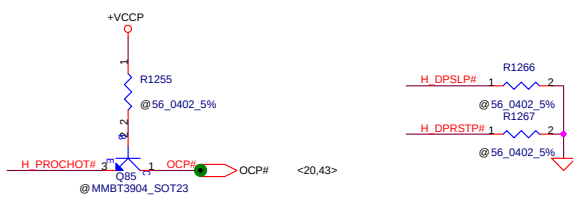
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1

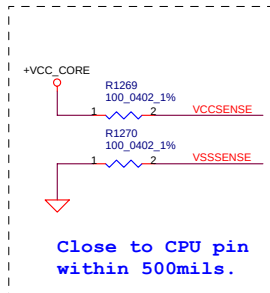
Symbol Note :



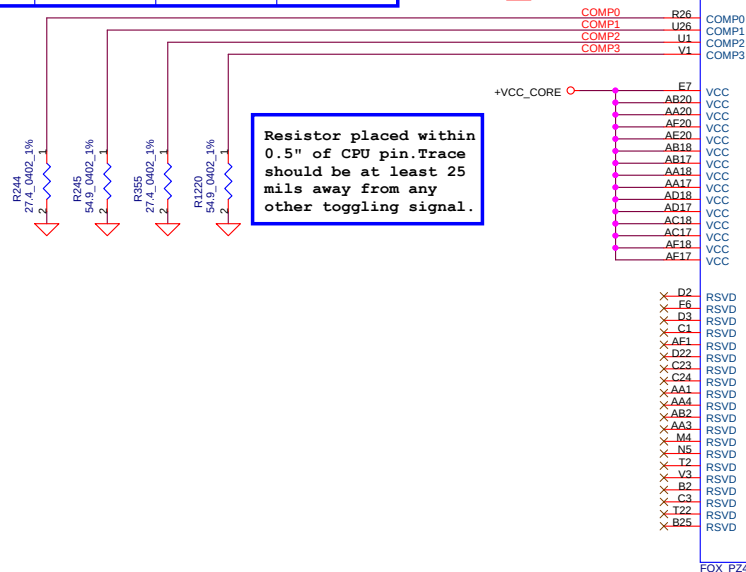
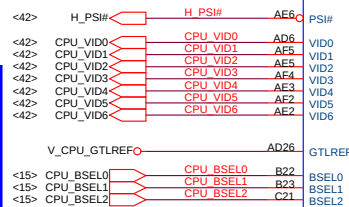
- @ : means just reserve , no build
- M52@ : means build discrete sku with ATI VGA M52 .
- UMA@ : means build UMA sku with Intel 945GM .
- SPI@ : means just build when SPI I/F BIOS function reserve.
- FWH@ : means just build when FWH I/F BIOS function reserve.
- NOXDP@ : means just build when XDP function disable.
- XDP@ : means just build when XDP function enable. When this time, docking PCI express will not work.
- 1021@ : means just build when SMC KBC1021 chip selected.
- LP@ : means just build when Low power clock gen. install
- NOLP@ : means just build when Low power clock gen. NO install

45@ : means need be mounted when 45 level assy or rework stage.

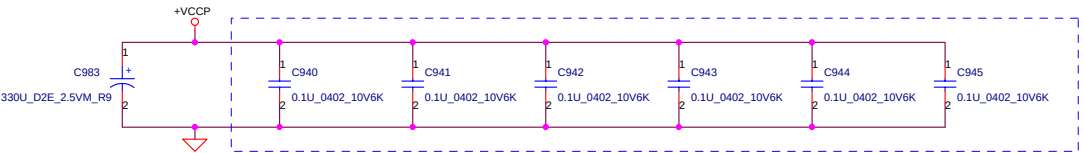
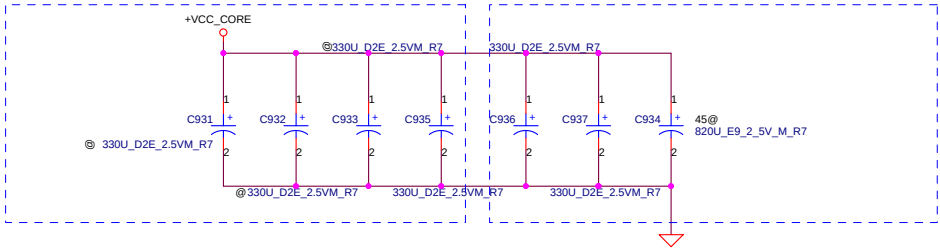
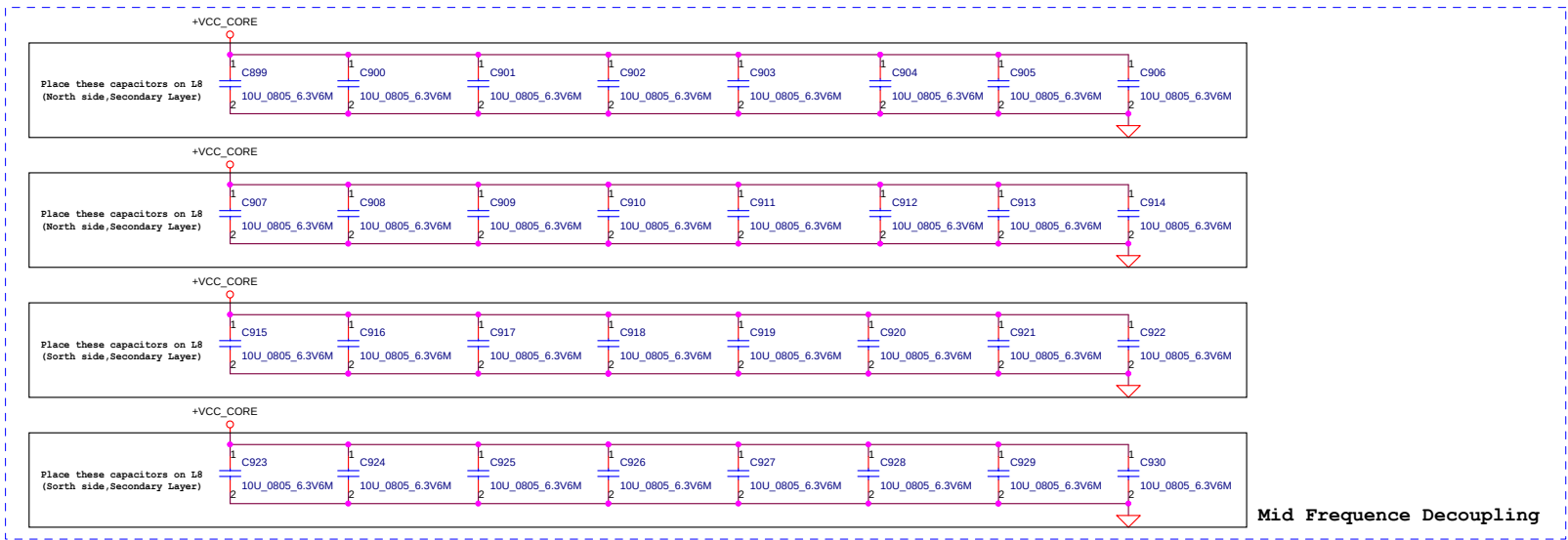


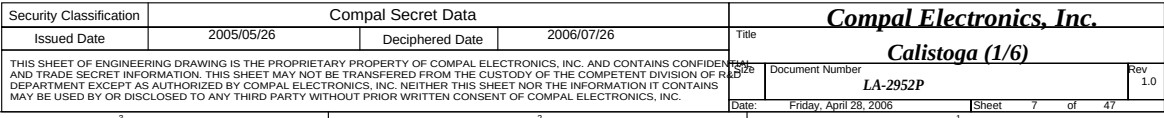


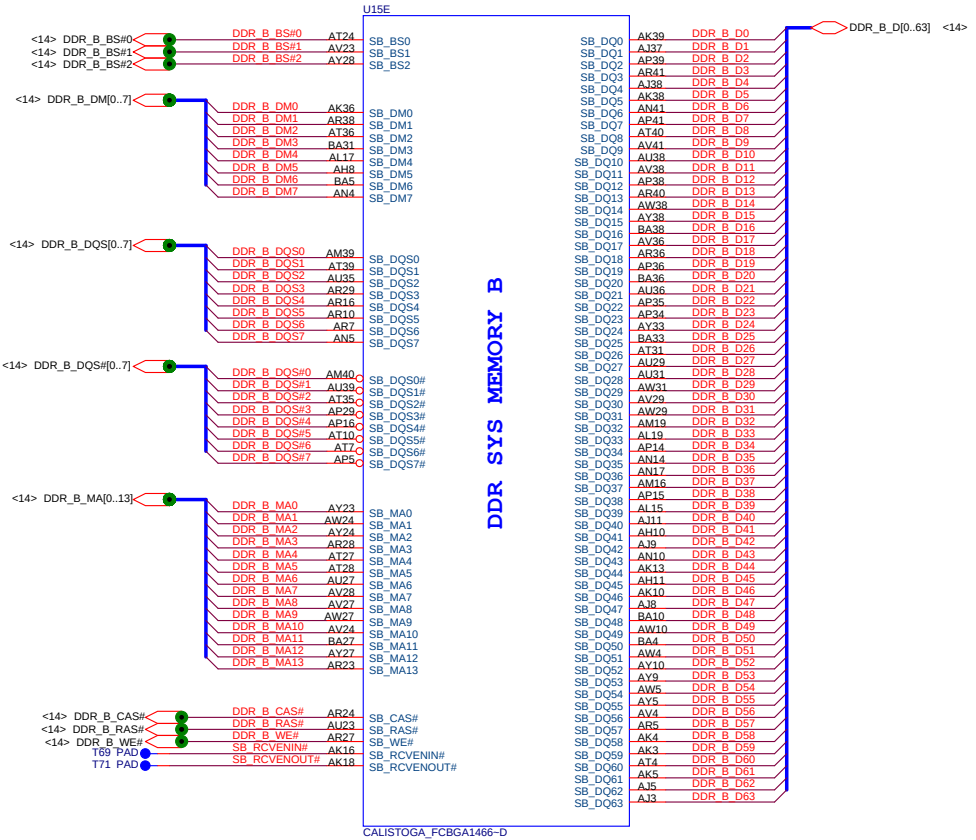
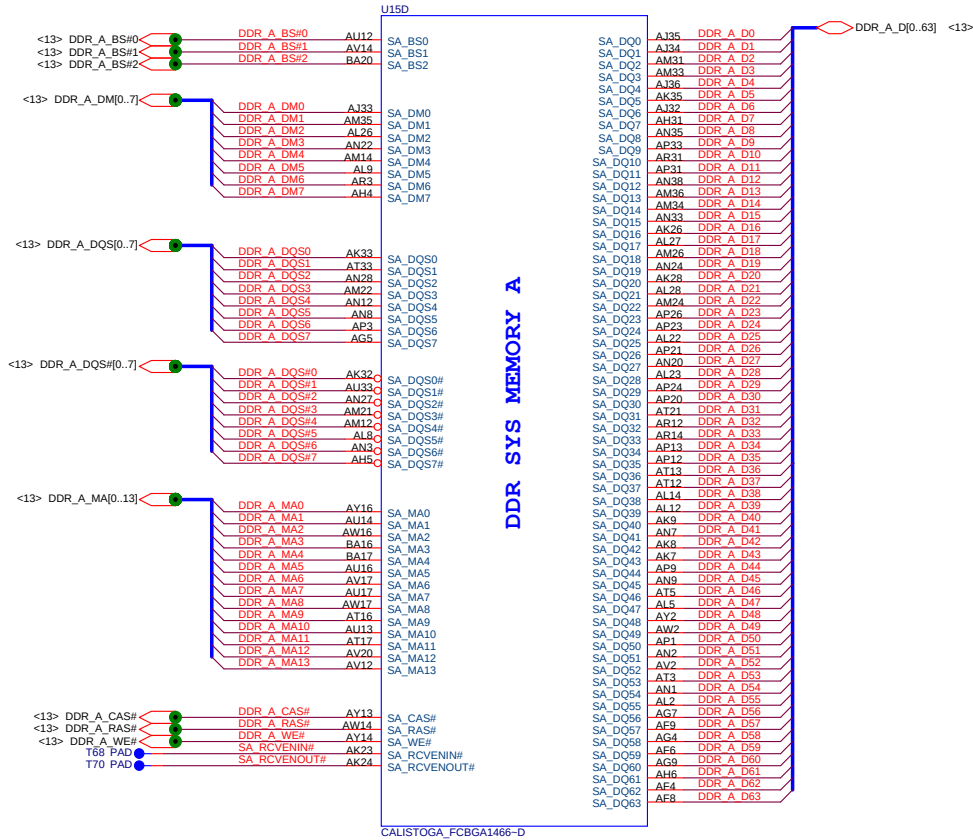
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

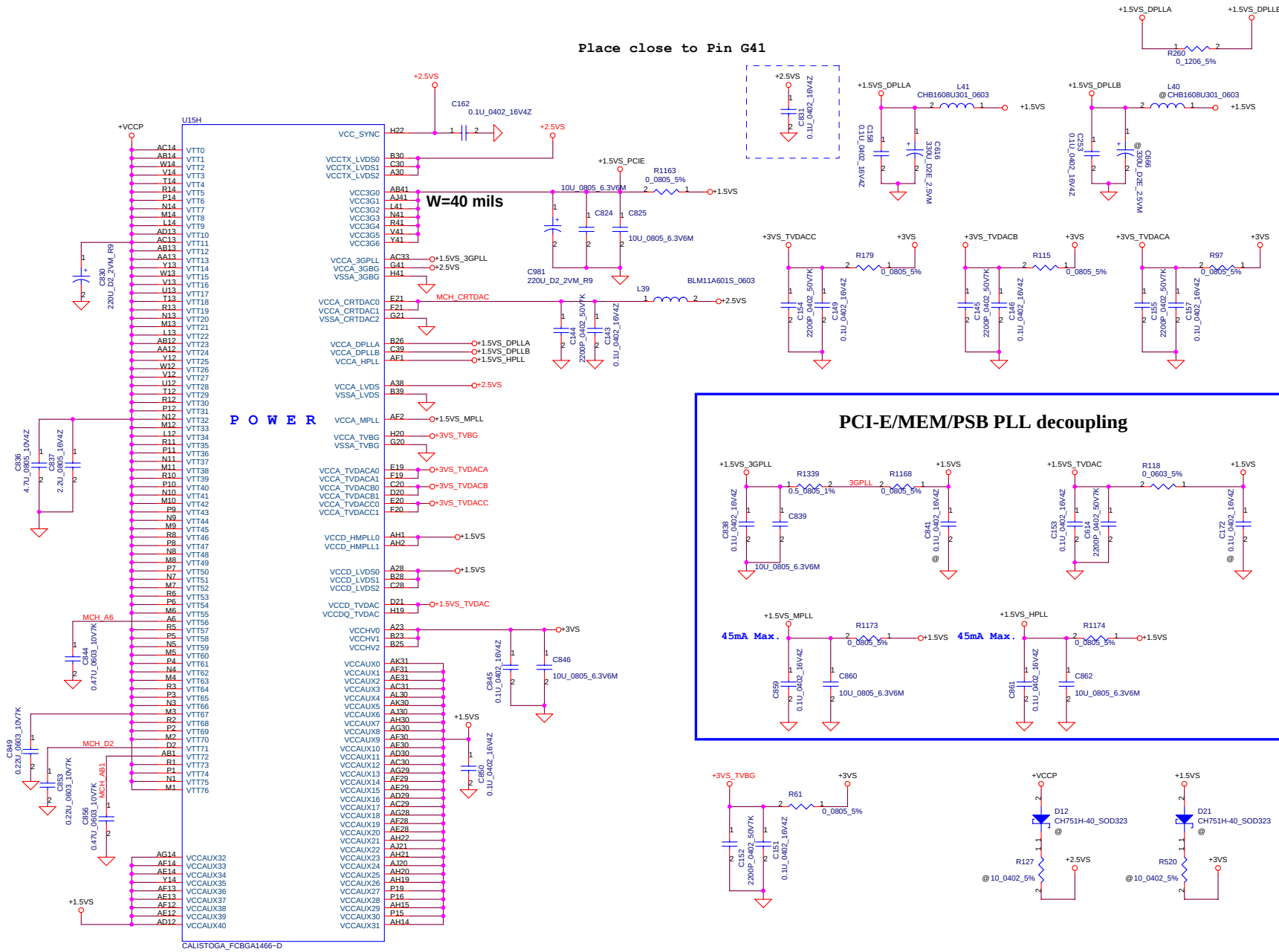


Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.









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					Calistoga (4/6)	
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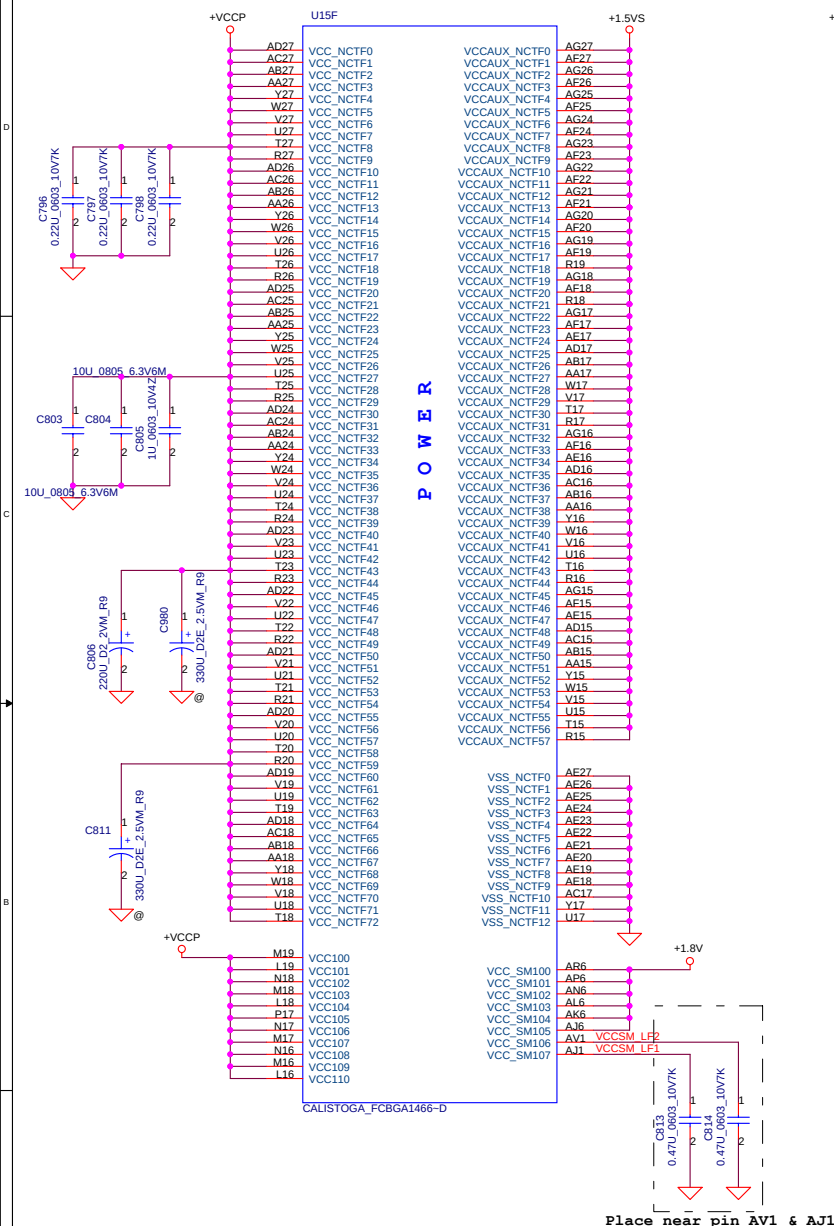
Strap Pin Table

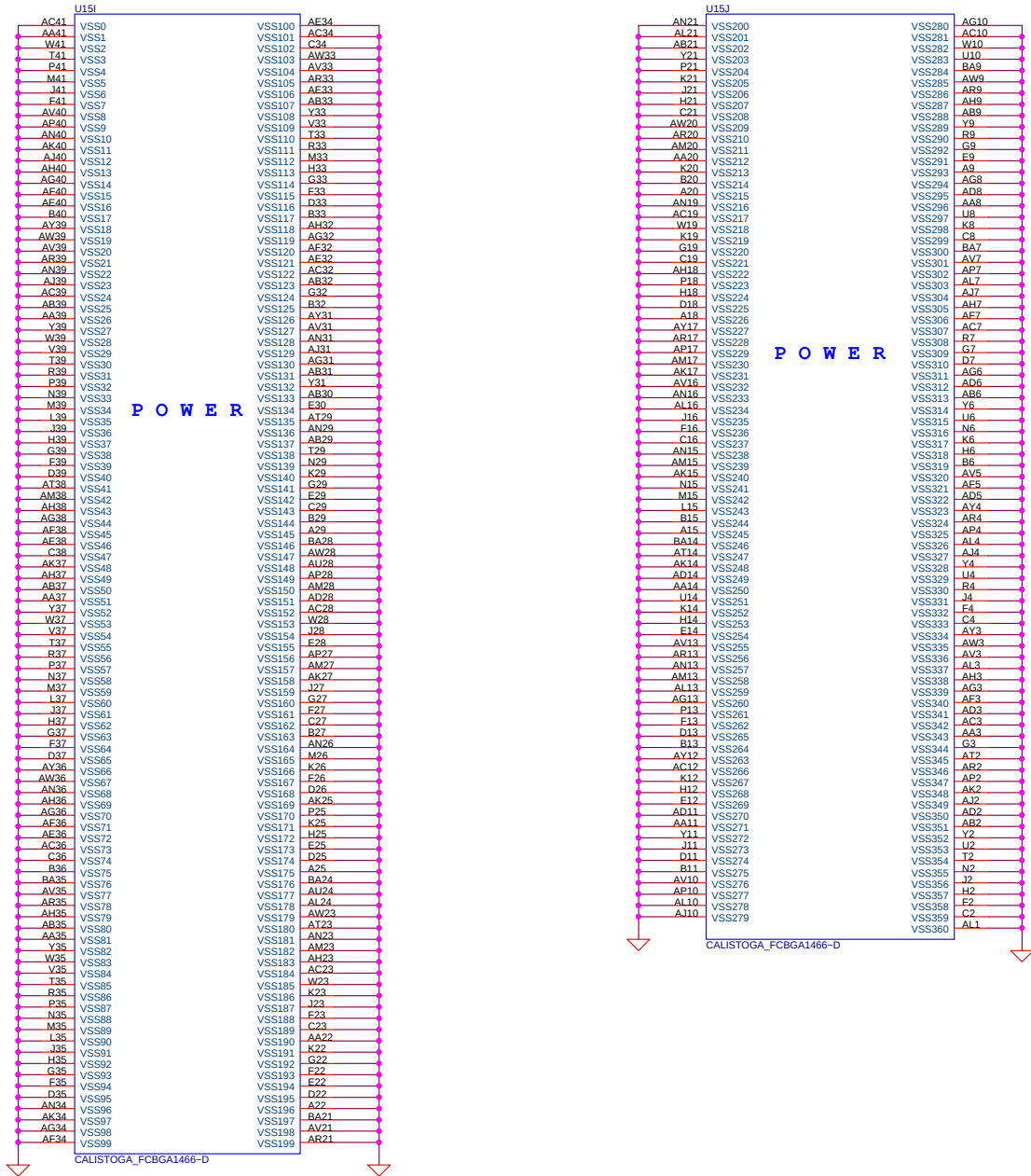
CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU * (Default)
CFG9	0 = Lane Reversal Enable * 1 = Normal Operation (Default)
CFG11	0 = Calistoga * (According to Intel Napa Schematic Checklist & CRB Rev1.301 document 2.2Kohm pull-down resistor request) 1 = Reserved
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG18	0 = 1.05V * (Default) 1 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.

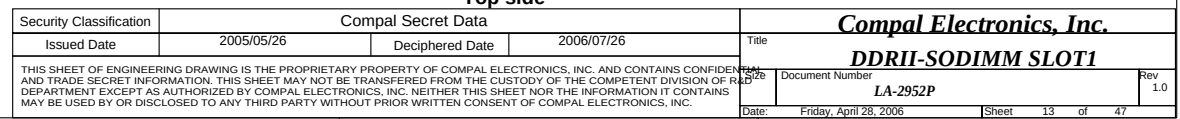
<7>	CFG5	R1151	1	2	@ 2.2K 0402 5%
<7>	CFG7	R1152	1	2	@ 2.2K 0402 5%
<7>	CFG9	R1153	1	2	@ 2.2K 0402 5%
<7>	CFG11	R1154	1	2	@ 2.2K 0402 5%
<7>	CFG12	R1155	1	2	@ 2.2K 0402 5%
<7>	CFG13	R1156	1	2	@ 2.2K 0402 5%
<7>	CFG16	R1157	1	2	@ 2.2K 0402 5%

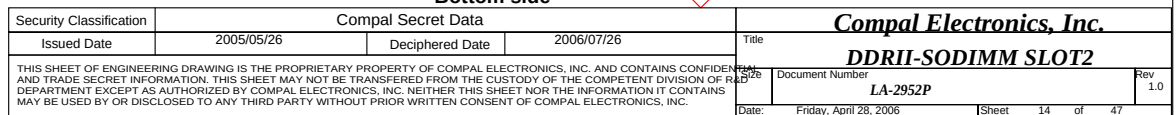
<7>	CFG18	R1158	1	2	@ 1K 0402 5%
<7>	CFG19	R1159	1	2	@ 1K 0402 5%
<7>	CFG20	R1160	1	2	@ 1K 0402 5%



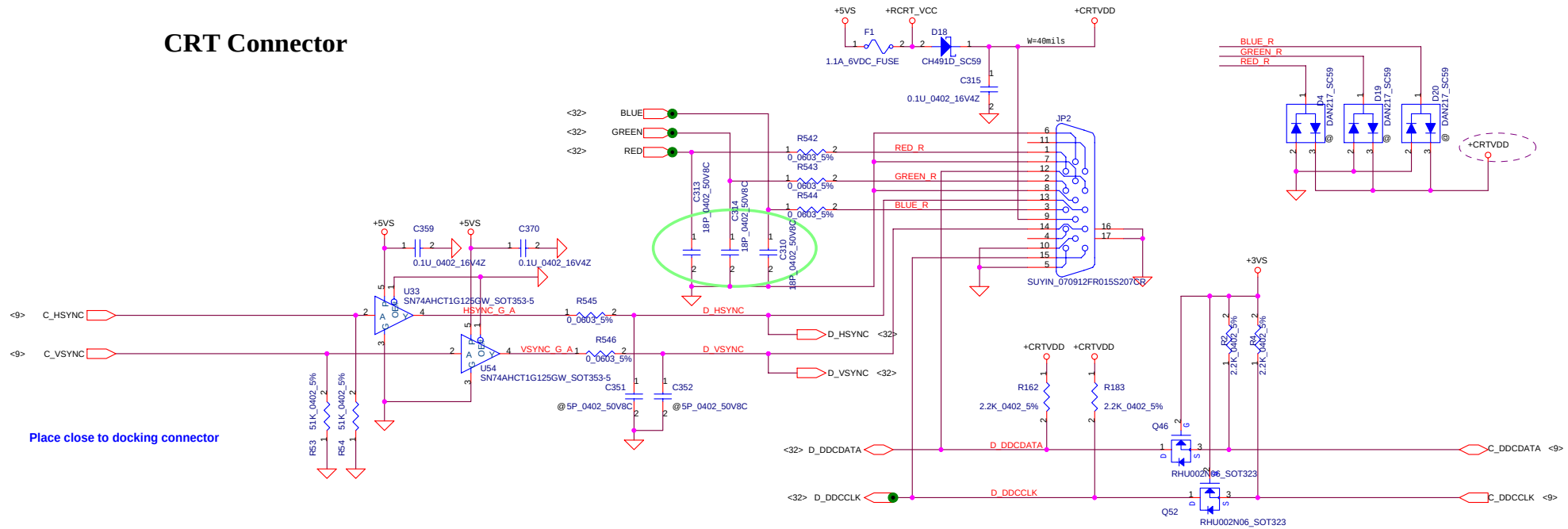


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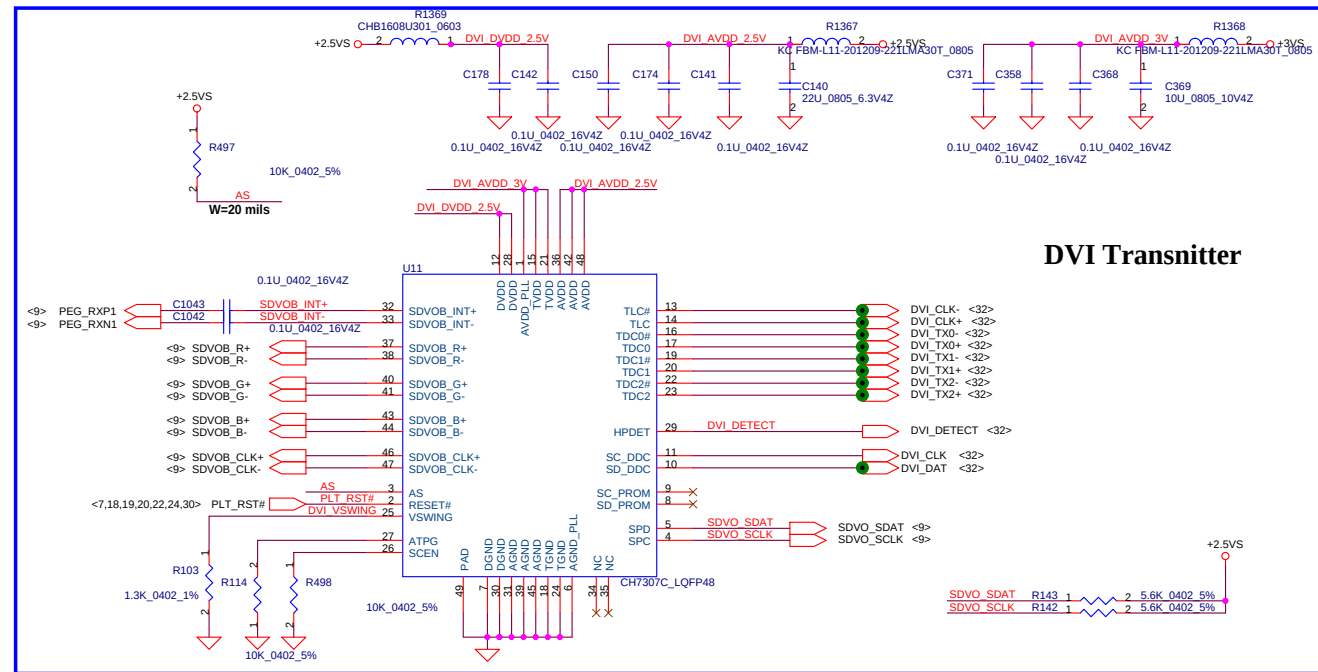
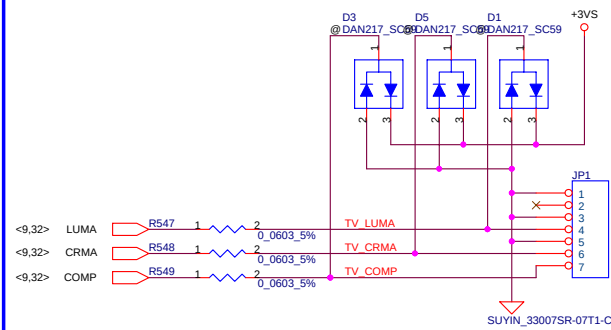




CRT Connector

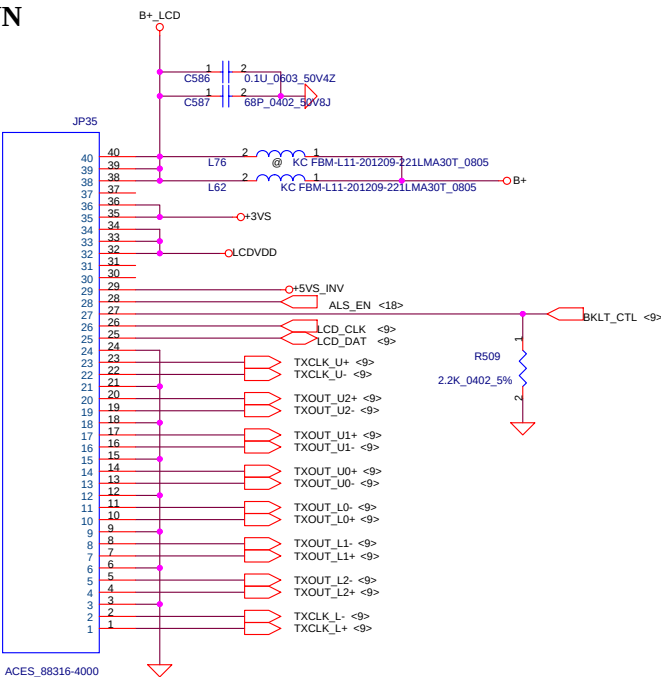


TV-Out Connector

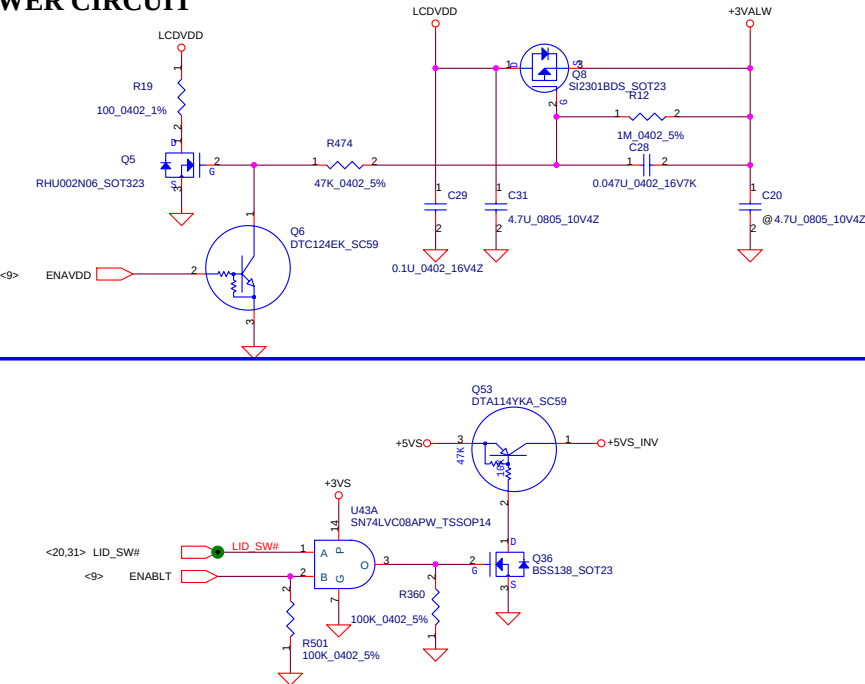


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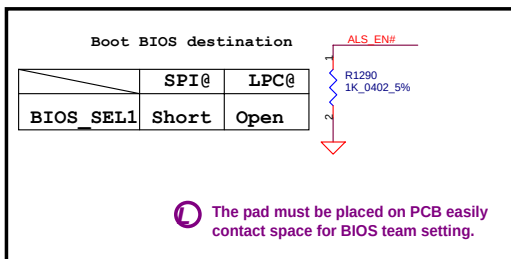
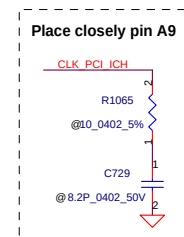
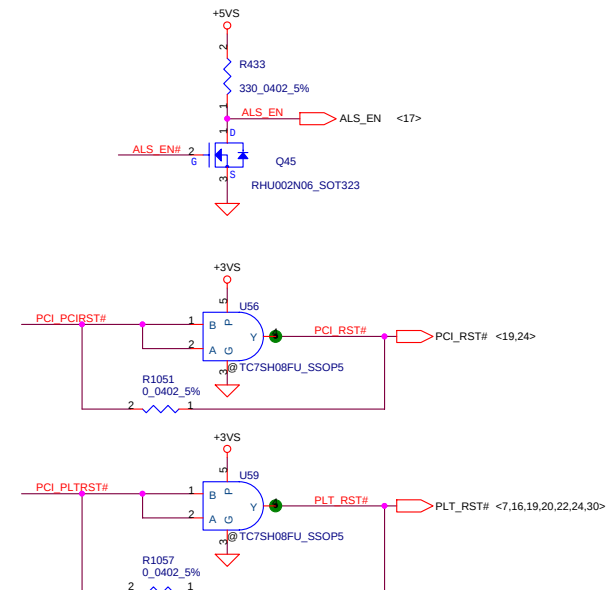
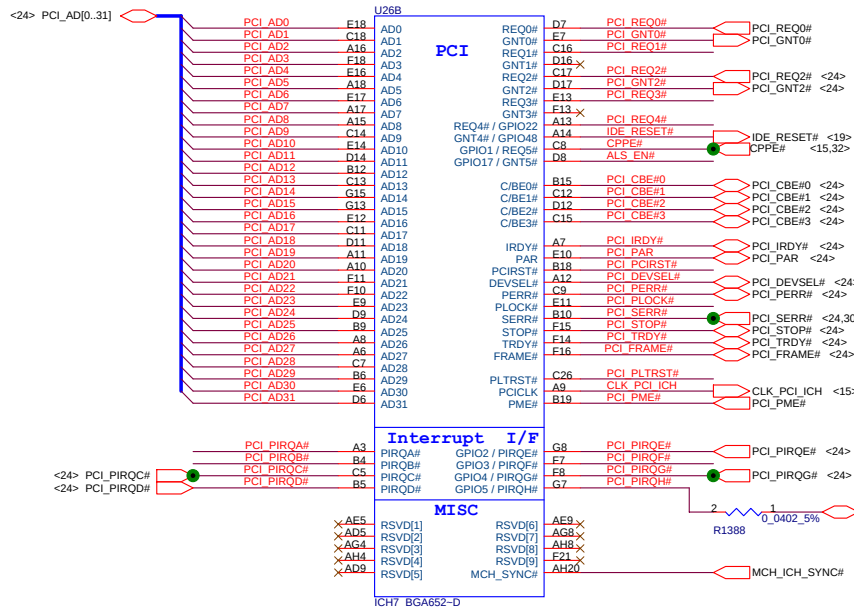
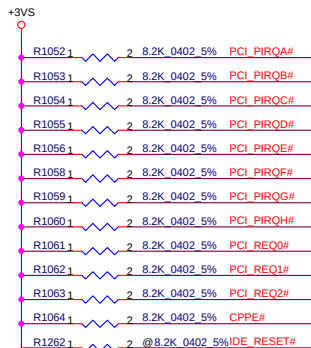
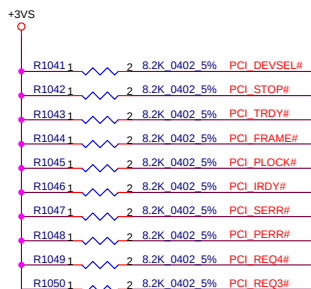
LVDS CONN

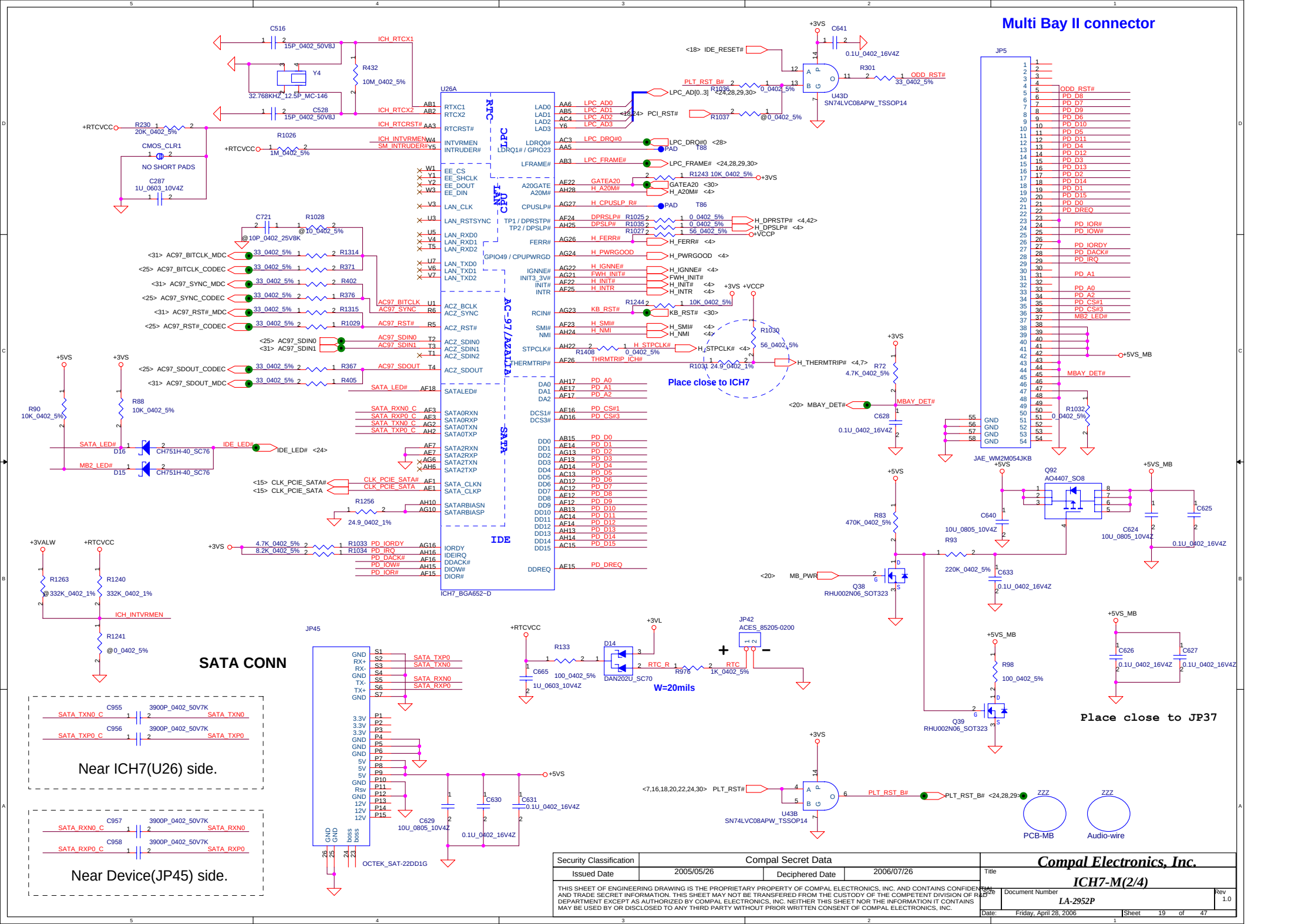


LCD POWER CIRCUIT



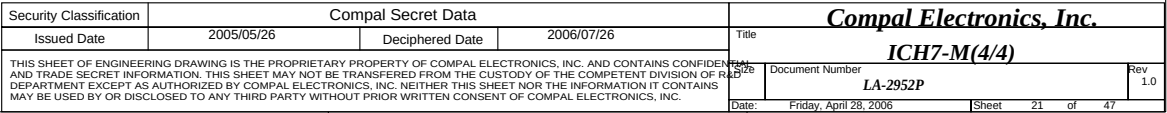
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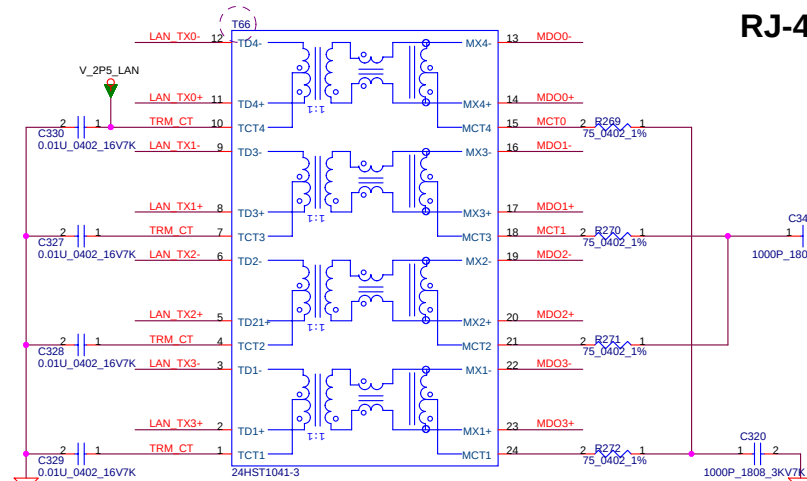


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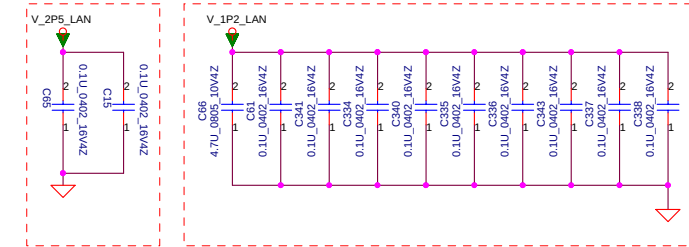


RJ-45 CONN.

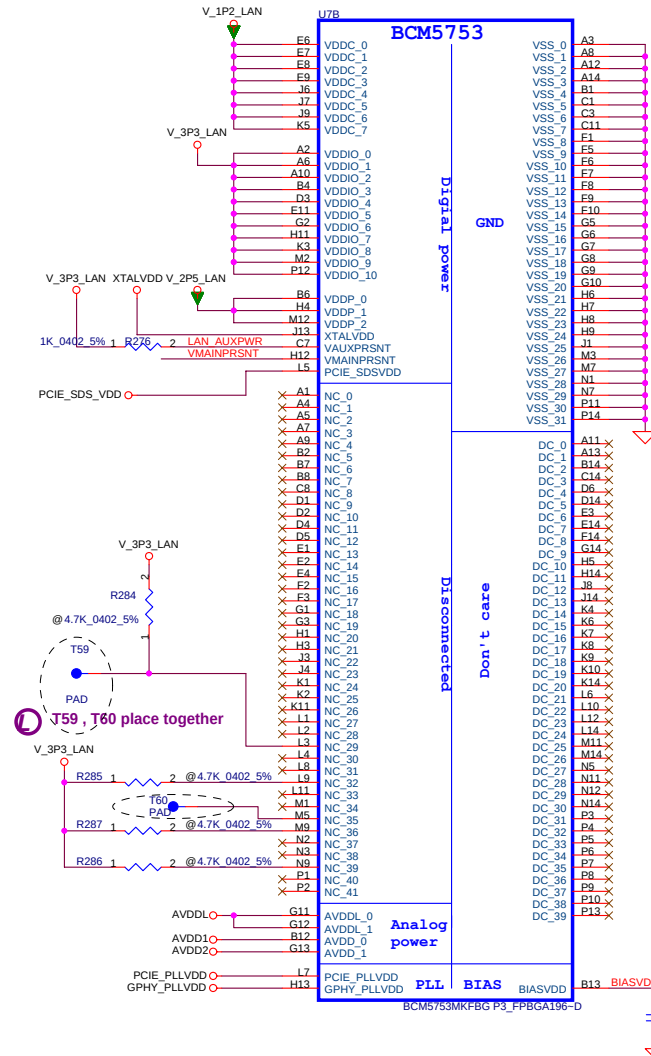
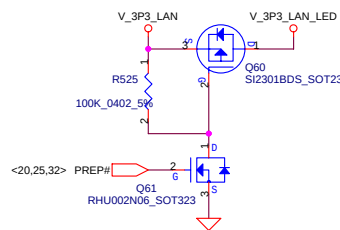
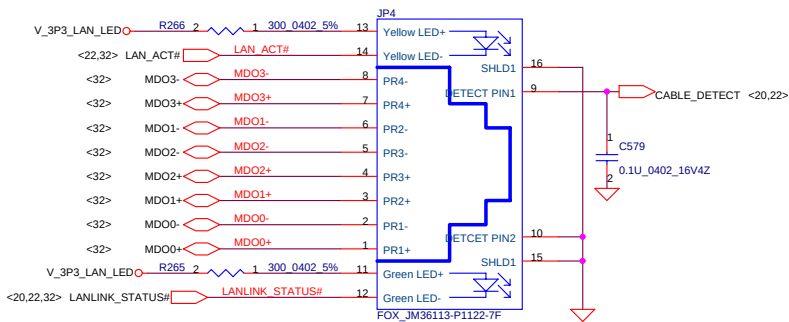
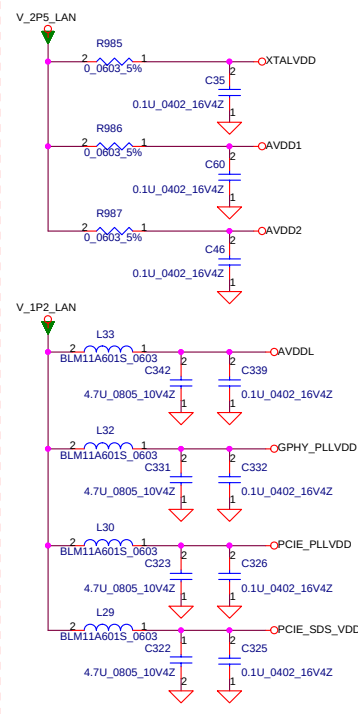
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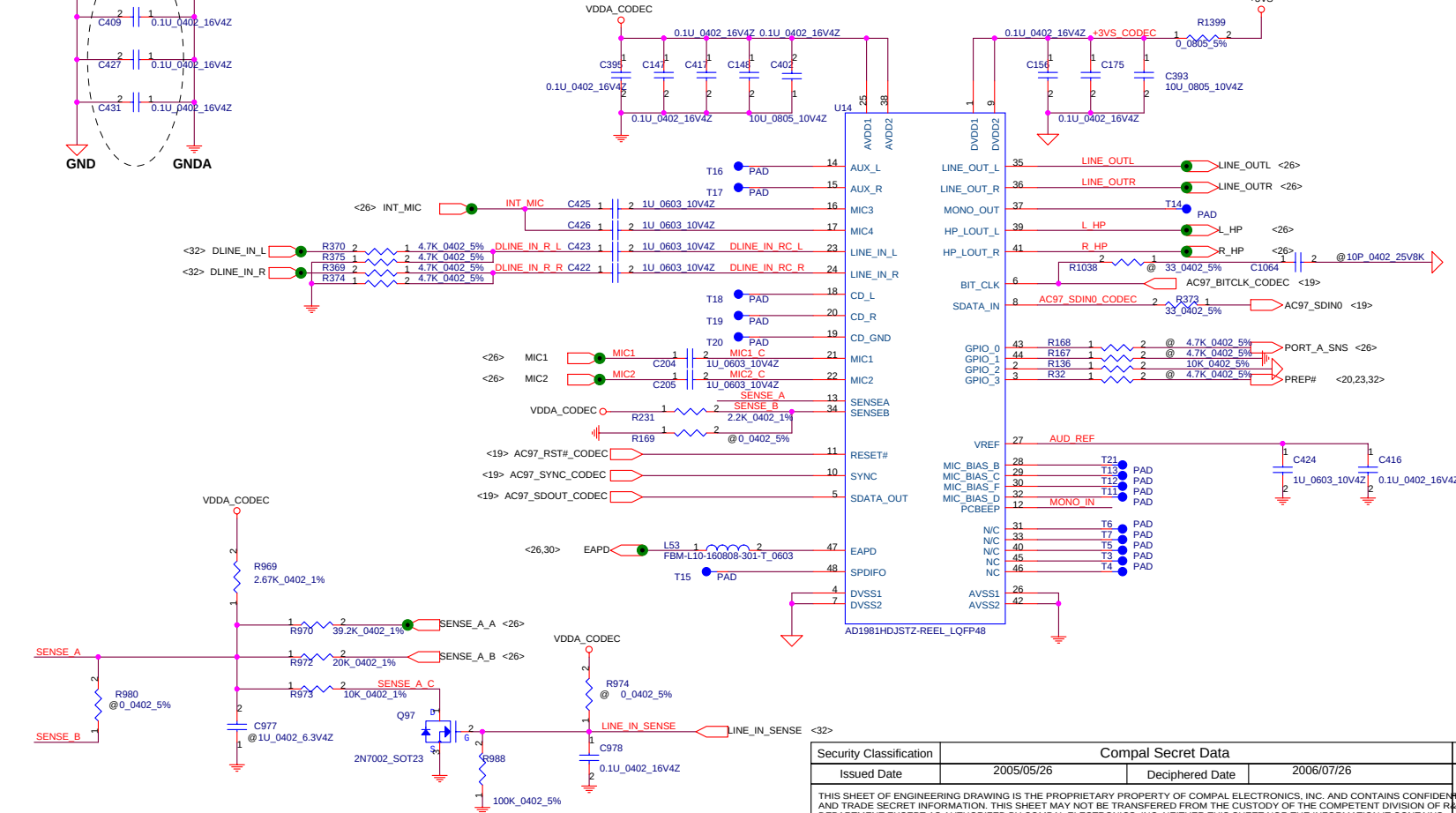
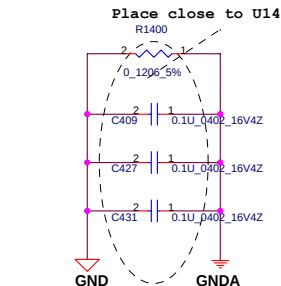
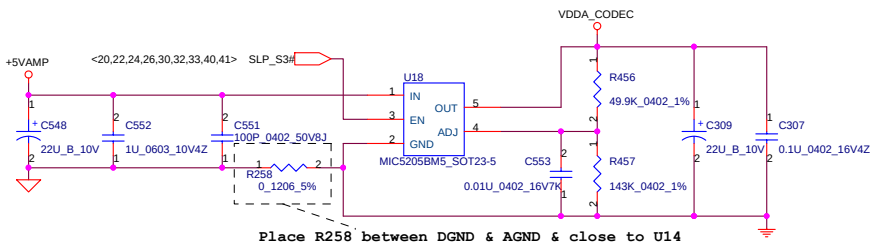
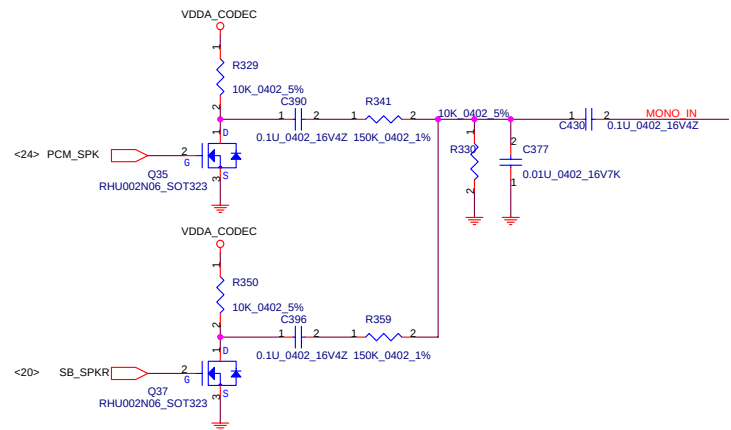
Layout Notice : Filter place as close chip as possible.



Layout Notice : Place termination as close as BCM5751M as possible

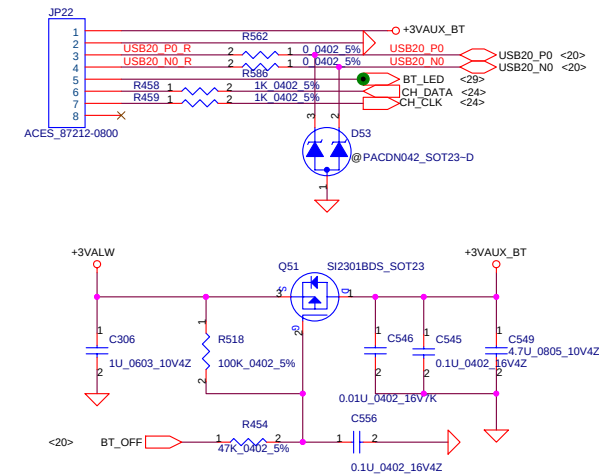
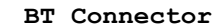
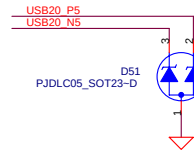
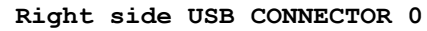


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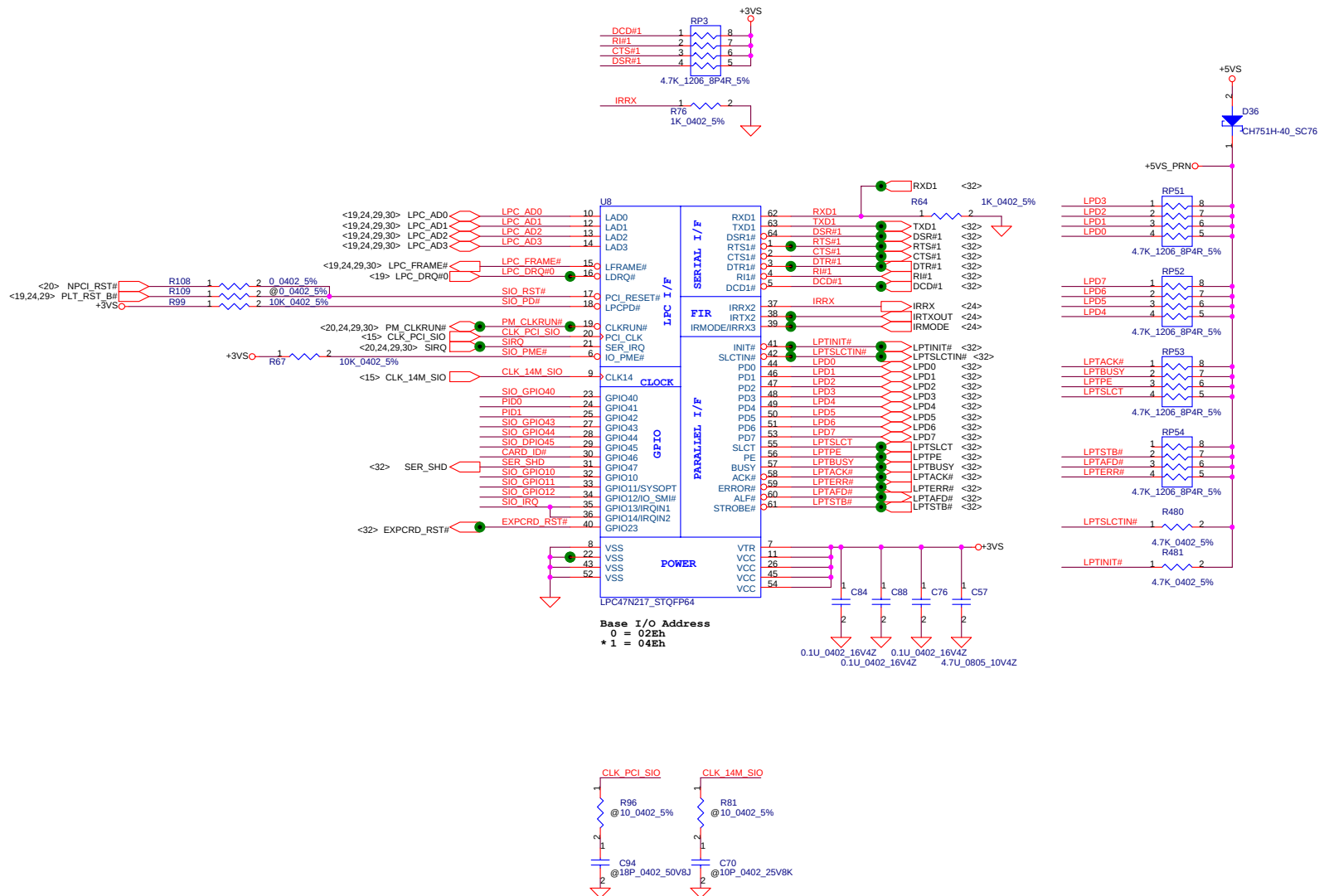


PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT, DOCK HP LO
PORT B	M/B MIC
PORT C	DOCK LI
PORT D	M/B SPK
PORT E	X
PORT F	Internal MIC

Left side USB CONNECTOR 1

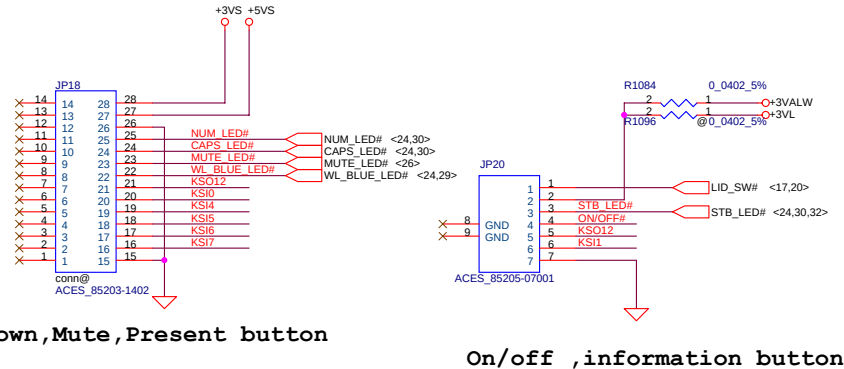


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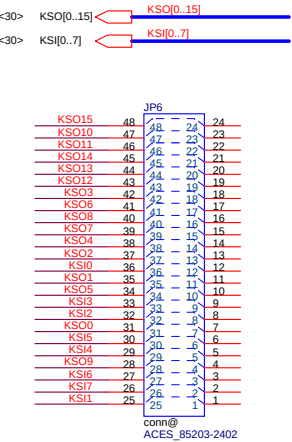


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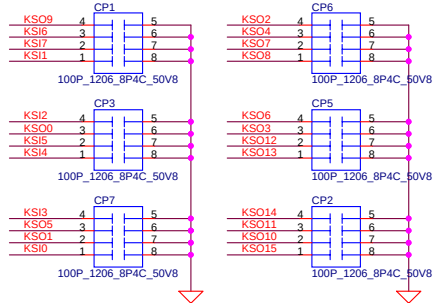
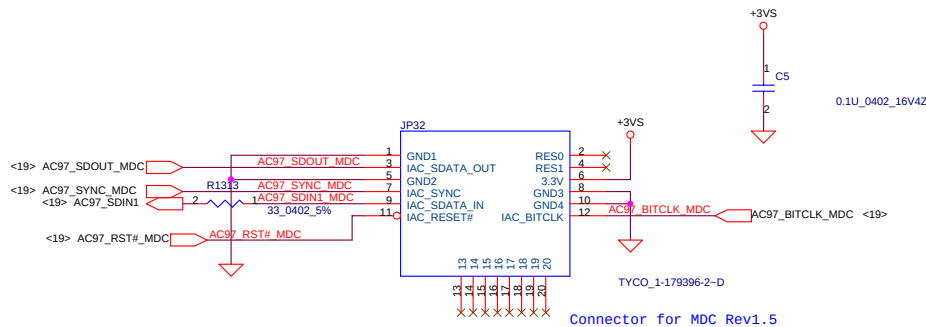
SWITCH BOARD.



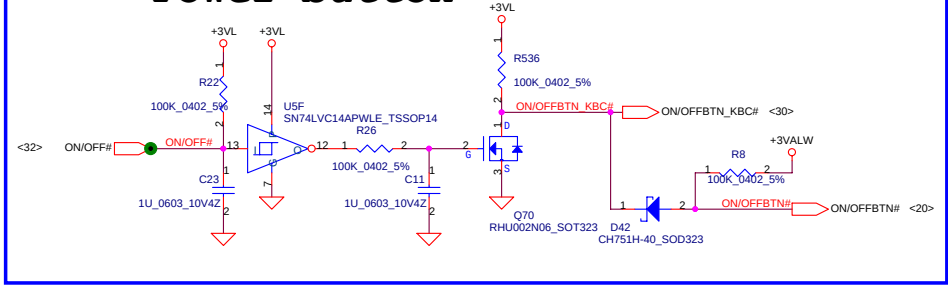
INT_KBD CONN.



MDC 1.5 Conn.

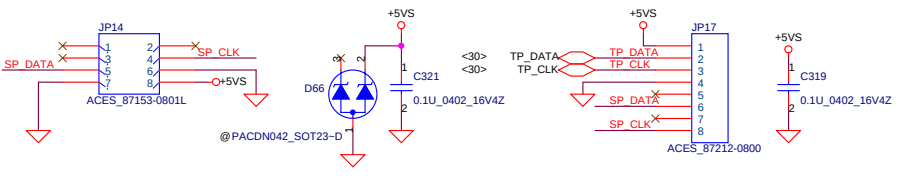


Power button



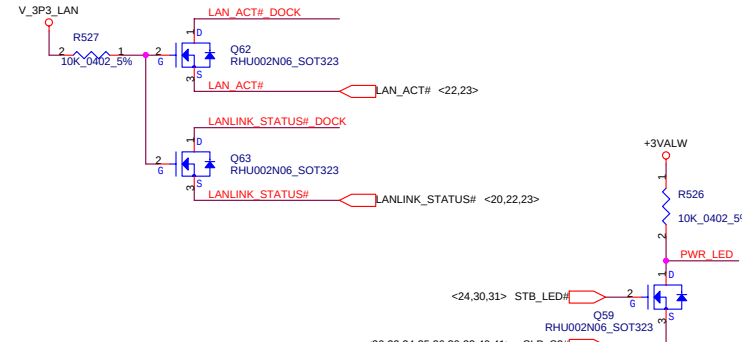
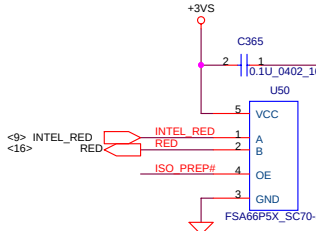
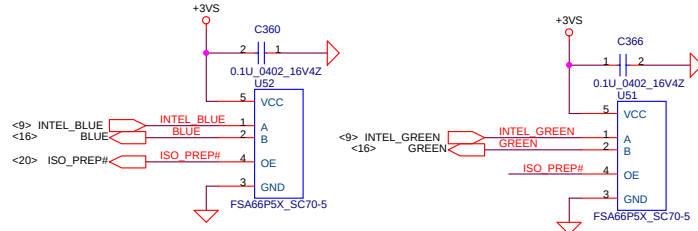
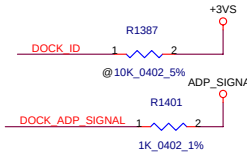
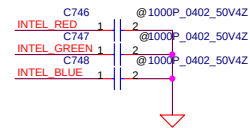
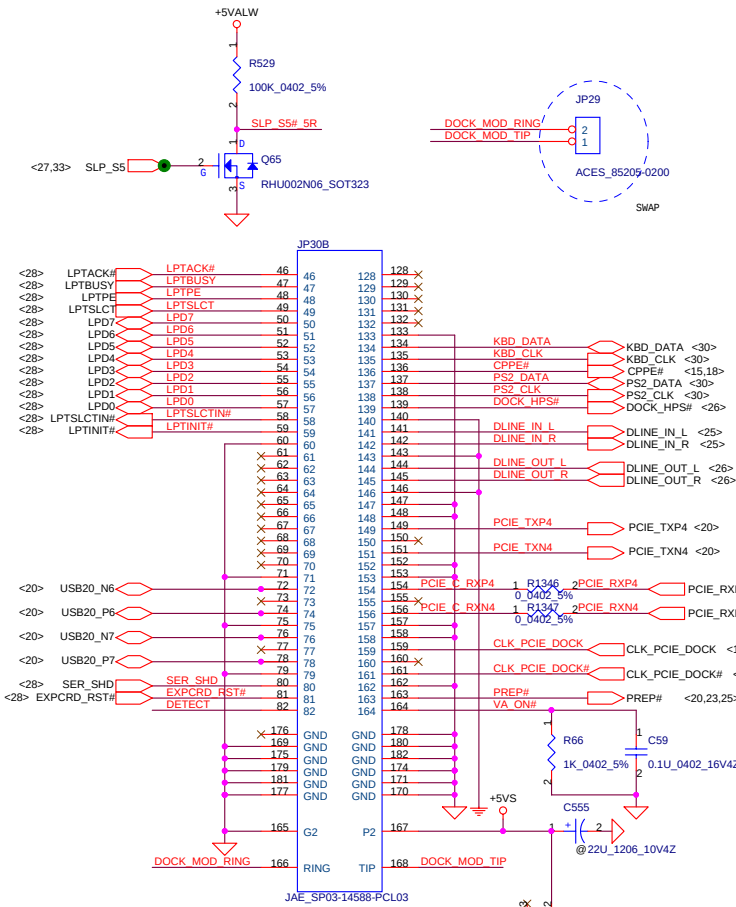
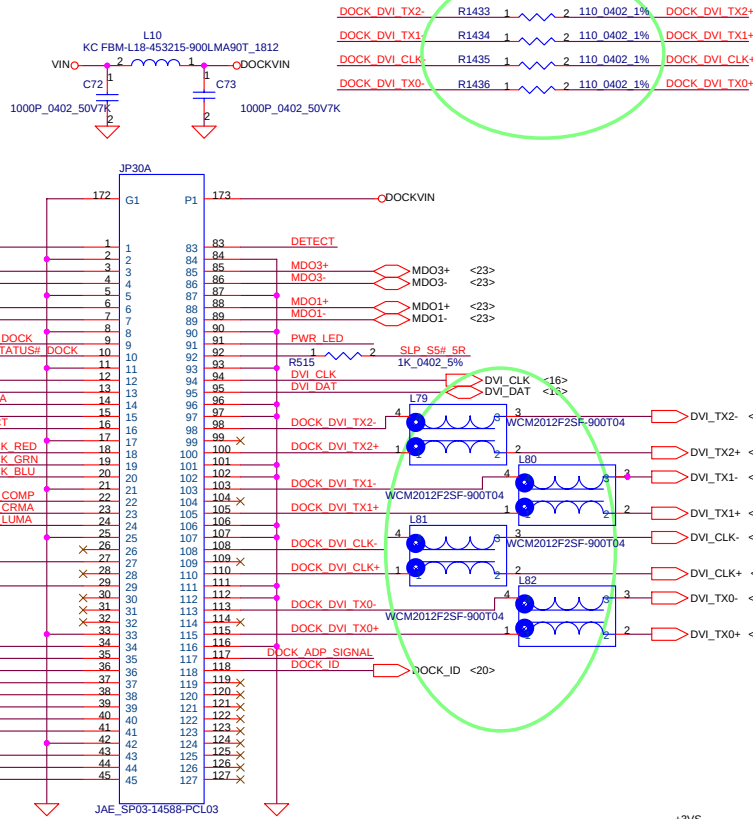
TrackPoint CONN.

T/P BOARD.



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					LA-2952P	1.0
				Date	Friday, April 28, 2006	Sheet 31 of 47

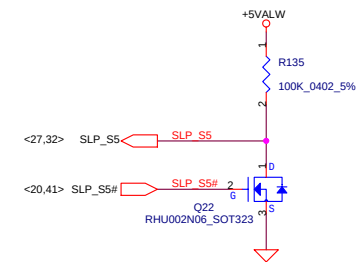
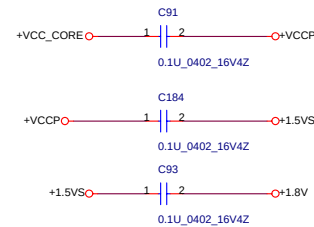
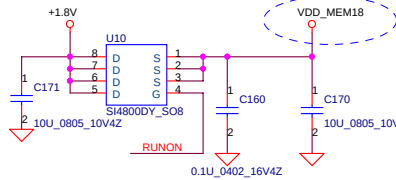
DOCK CONN. 184PIN



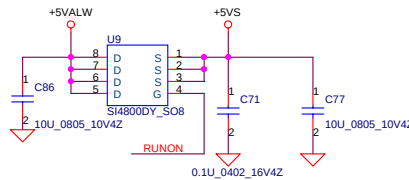
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Issued Date				2005/05/26				Deciphered Date			
2006/07/26				2006/07/26				2006/07/26			
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+1.8V to +1.8VS Transfer

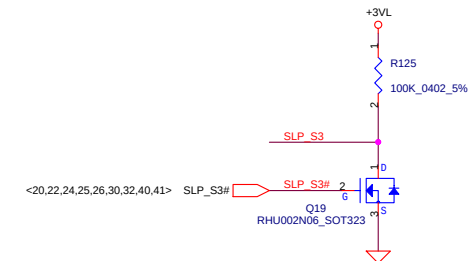
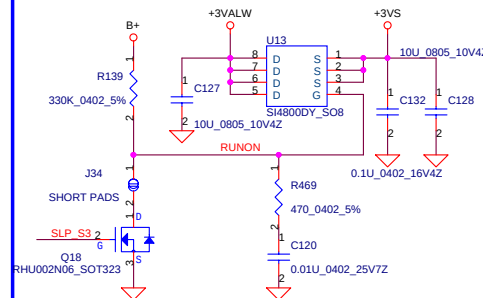
VRAM



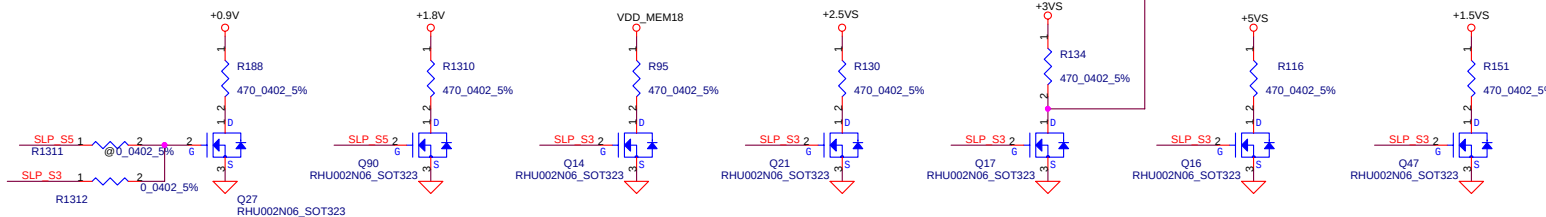
+5VALW to +5VS Transfer



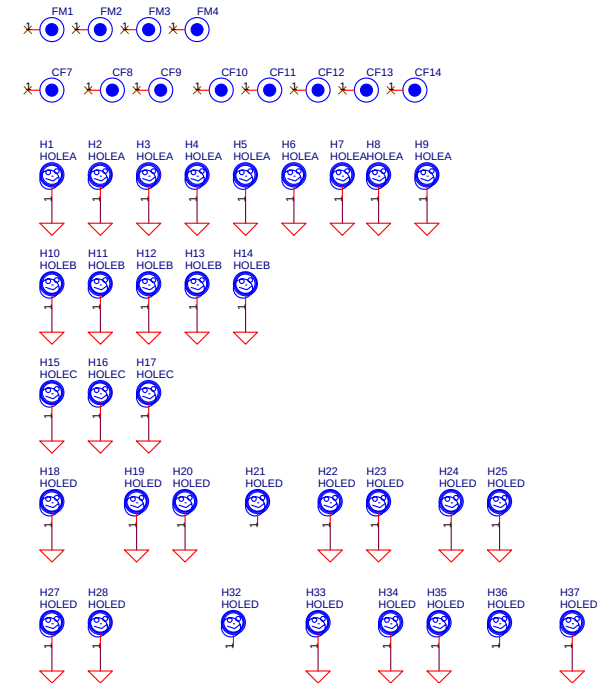
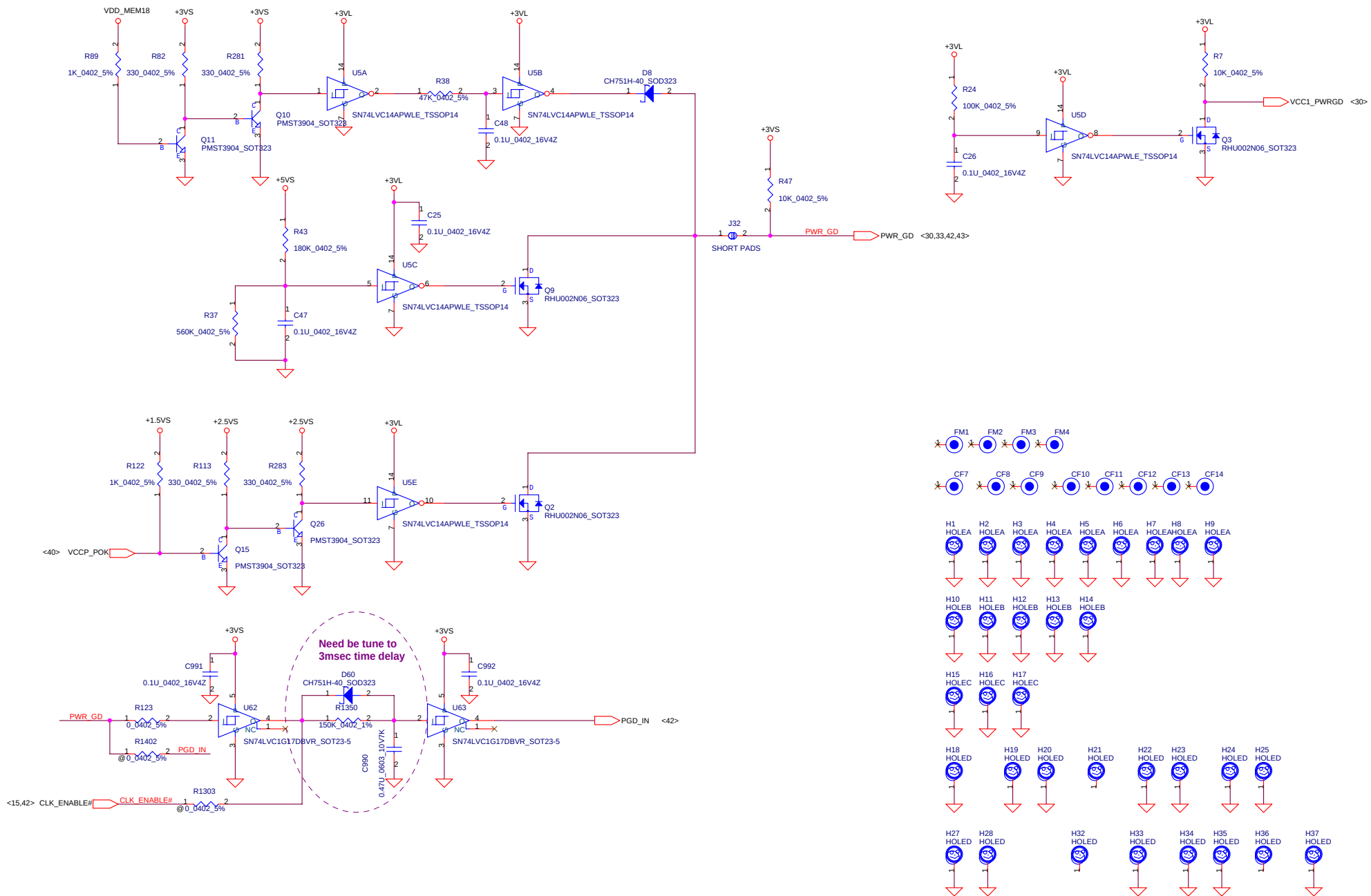
+3VALW to +3VS Transfer



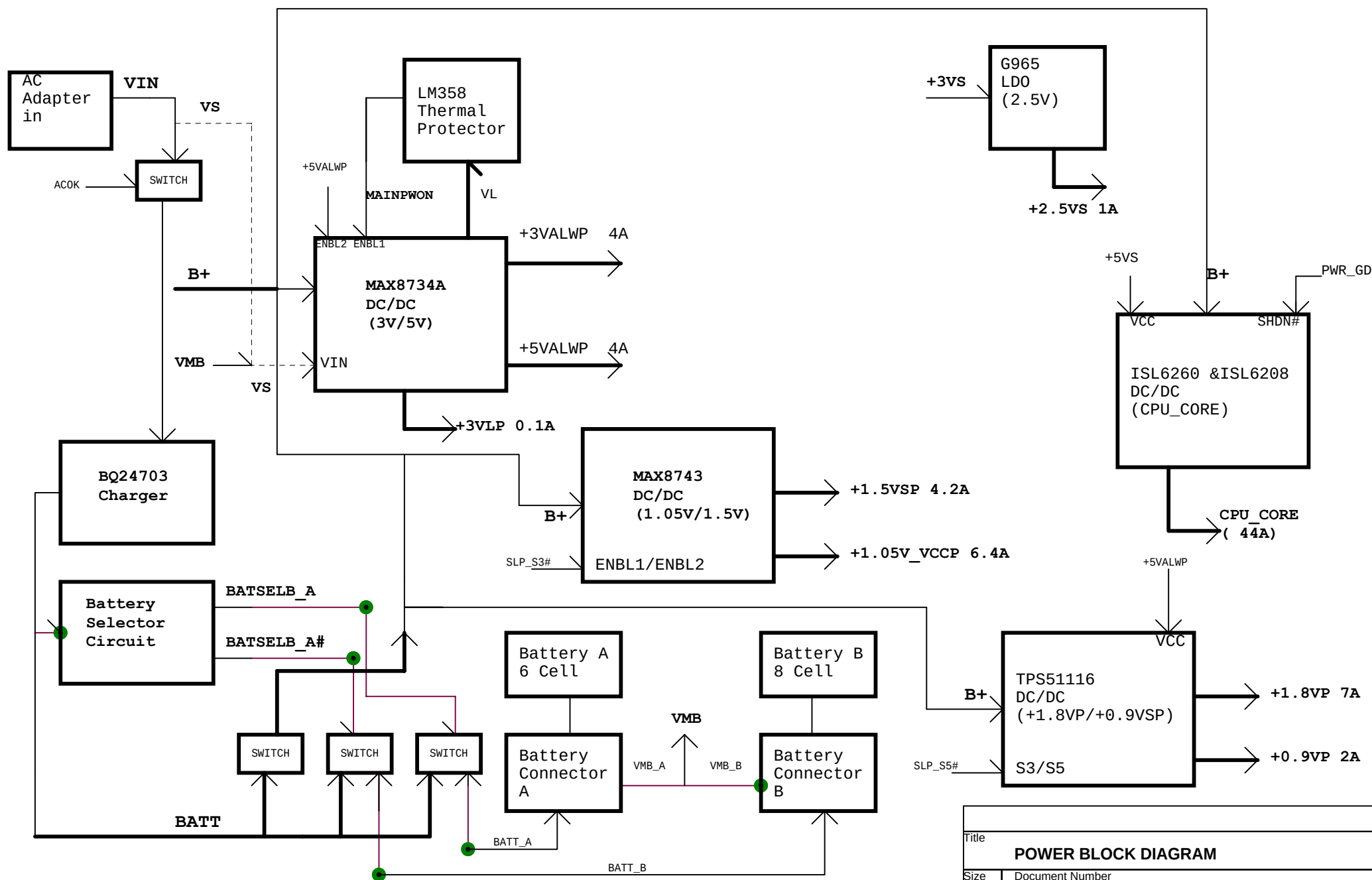
Discharge circuit



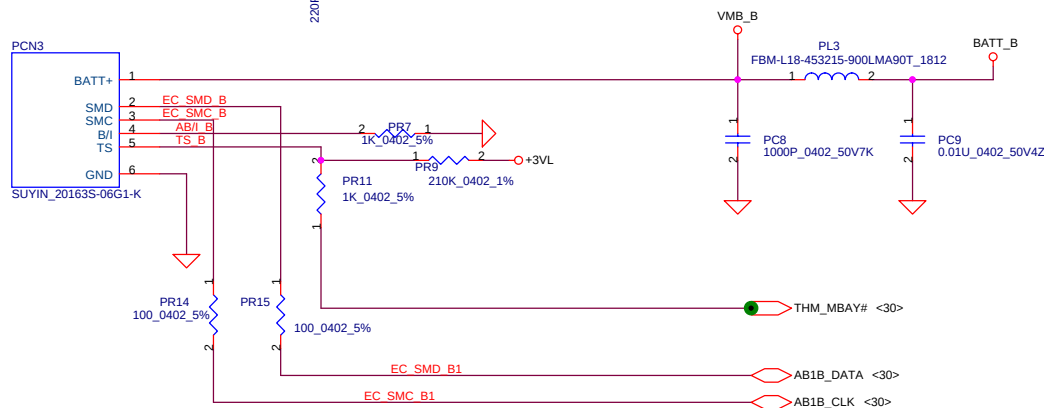
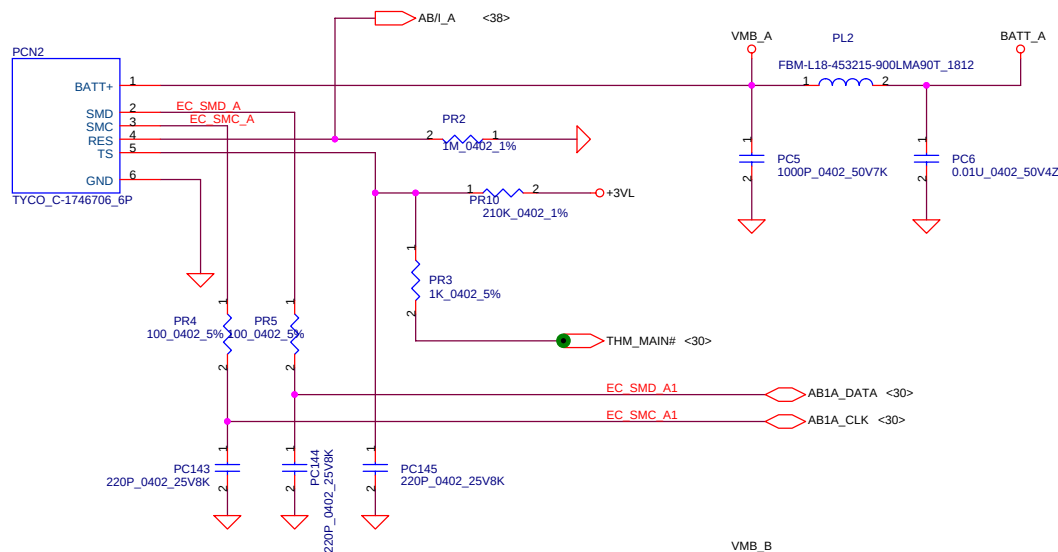
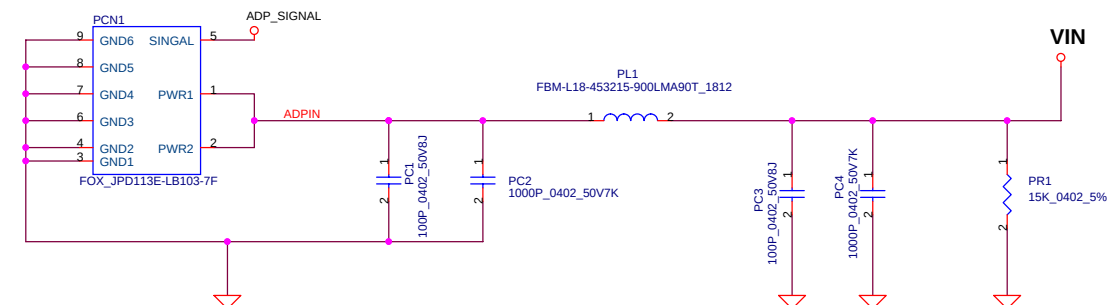
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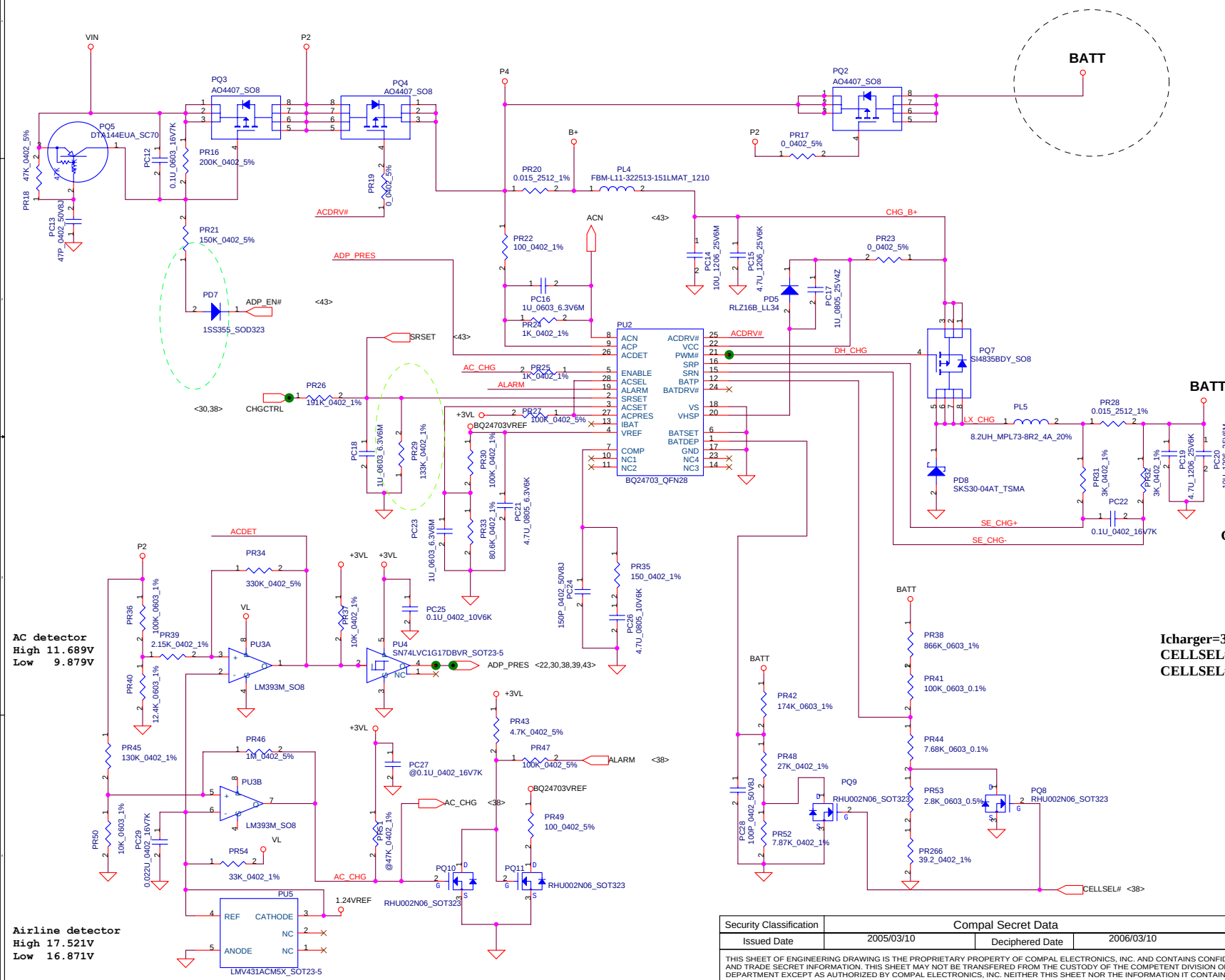
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Title		
POWER BLOCK DIAGRAM		
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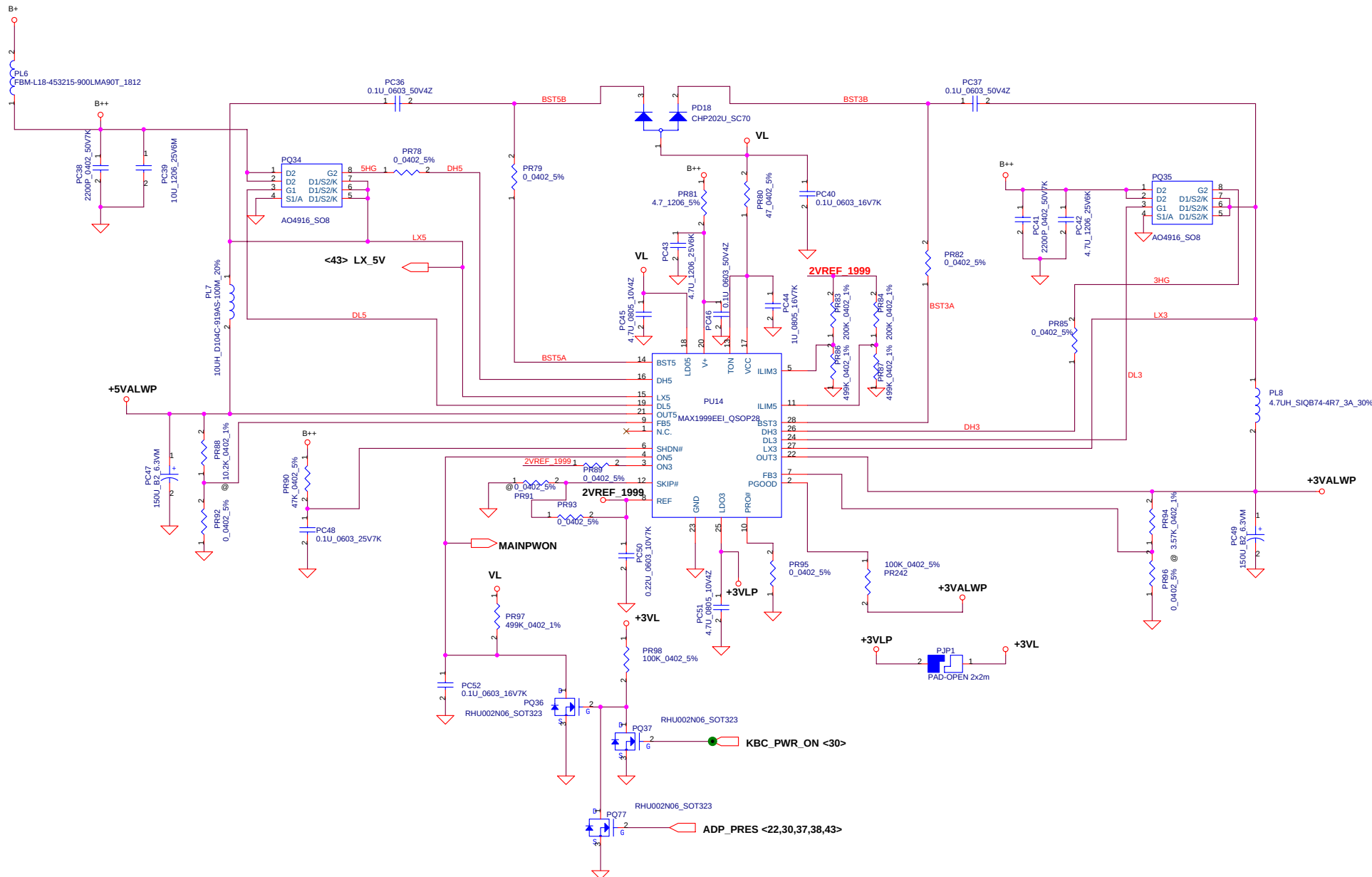
CV=12.6V(6 CELLS LI-ION)
 16.8V(8 CELL LI-ION)
 CC=3A for 2.4Ahr
 CC=3.57A for 2.55Ahr

Icharger=3A
 CELLSEL#=0,Vcharger= 12.6V
 CELLSEL#=1,Vcharger= 16.8V

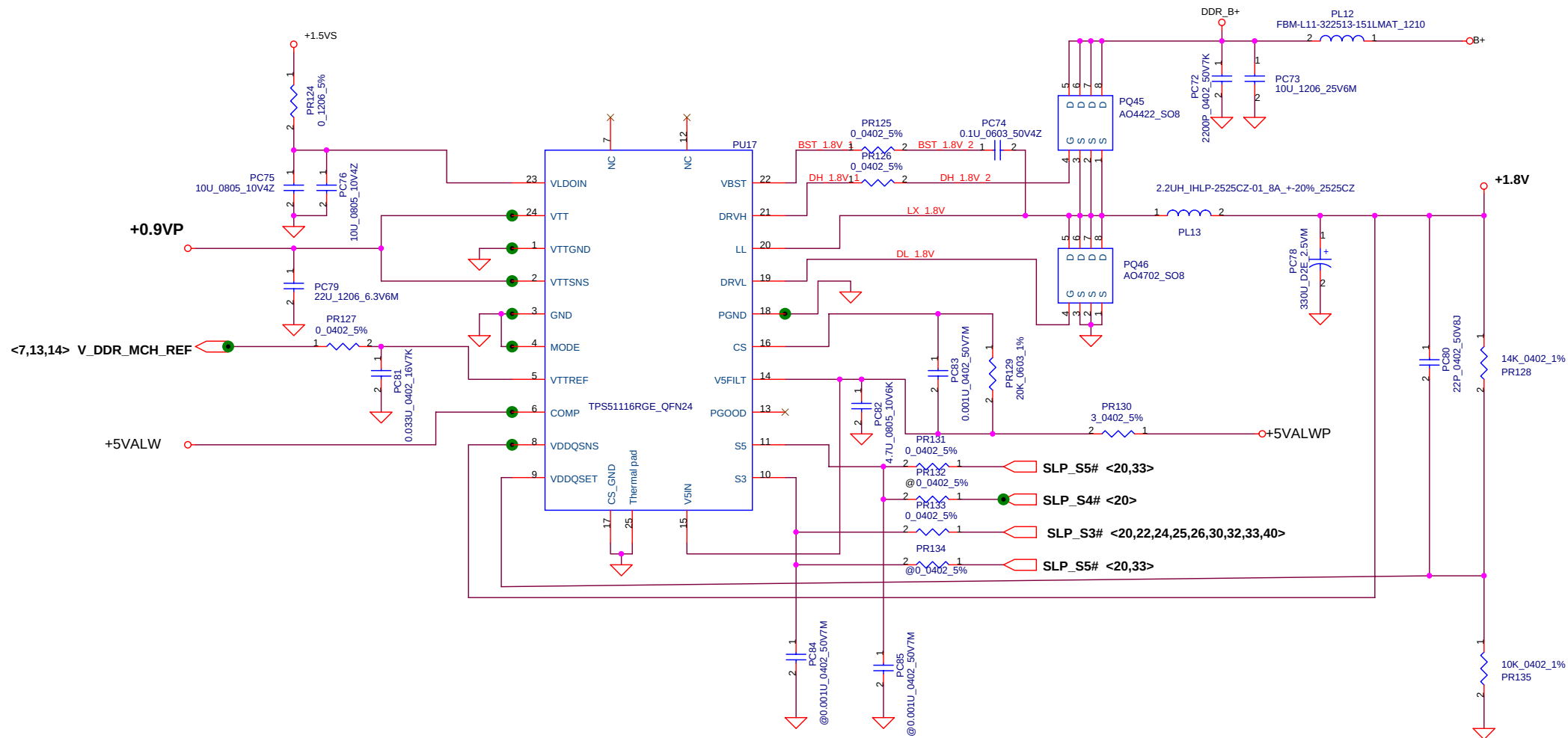
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		2005/03/10	
2005/03/10		2006/03/10		2006/03/10	
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Compal Electronics, Inc.
Charger

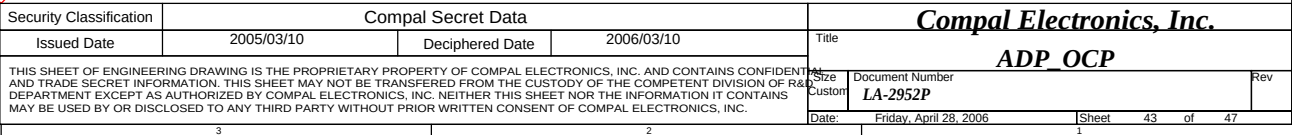
+3.3V/+5V



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EE PIR list

06/01/2005 schematics review start :

06/02/2005

Page38 : Add R58,R59,R60 ,those are removed from daughter board
Page39 : JP18 pin3 change from ground to BT_LED
Page37 : Remove JP16 & change debug port interface to JP44
Page27 : ICH7M pin R7 change to +3VS
Page32 : JP44 PLT_RST# change to PLT_RST_B# to reduce the loading
Page33 : Update audio amp to MAX9710

06/03/2005

Page10 : Add R260 to reduce one 330U cap C666

Page25 : 1. R27 change to +3VS
2..Add R1035 for H_DPSLP#

Page26 : 1.Add T80 for GPIO25
2. GPIO21 change net name to VGARST#
3. Add T88 for GPIO23
4. Add T89 for GPIO26
5. GPIO30 change net name to USB_OC#6
6. GPIO31 change net name to USB_OC#7
7. Add R1036/7 for RESET option
8. Remove the connection of USB_OC#3/4/5

Page24 : Add ALS_EN on JP35 pin24 for light sensor

Page32 : 1.JP13 change to 90 pins connector
2.Add U72 for ESD protection

06/04/2005

Page10 : A. U71 change to U43D (the fourth gate in U43)
B. Add +3VS TVBG R/C filters & voltage follower D12,D21,R127,R520
Page34 : audio change-- add R1419 ,R431,R434,R435 for BIASA/B/C

Page35 : Add JP3 for Smart card FFC connector

Page18 : 1.R1365 CHANGE TO 2K_0402_1%
2. R1366 change to 562_0402_1%
3. R1367 change to 1.47K_0402_1%

Page31 : JP4 update to RJ45 connector

Page15 :Add the connection for UMA VGA clock , & SRC0/2 SWAP
1.Add R1148/R1149 , R1129/R1132 , R1118/R1121
2.Add R1242/R1248,R1253/R1272

Page09 : Change 0 ohm resistors before filters ,
and delete the other group of filtes at page 19
Page16 : add R671~R678 ,R530,R531 for DVI

Page19 : Swap I2C bus for LVDS/Thermal sensor

06/07/2005

Page47 : PQ34 pin5/6/7 change netname to LX_5V

Page38 : Pin96: INVFWM rename to OUT9 & add T90

Page36 : Delete R500 & rename to EXPCRD_RST#

Page35 : Add JP3 for Smart card FFC connector

06/08/2005

Page7 : Delete PD resistor R1340~R1343.

Page17 : Update JP35 LVDS connector

Page26 : A. GPIO28 ==Delete R1321 & A_SD , change to VGA_RST#
B. GPIO21 ==Change to MB_PWR
C. GPIO19 ==Change to PD

06/09/2005

Page17 : Delete Q56 ,R510 ,Caymus support 3V PWM

Page25 : Update Q92 to AOS4407

Page26 : Delete R252

Page37 : Add PD RP42,R273

Delete Cardbus 6612 circuit & move to daughter board LS-2953

06/10/2005

Page17 : Add R458,R459 for ch_data,ch_clk

Page33 : Add C367 0.1U for +SC_PWR

06/11/2005

Page28: 1.Delete R15 ,due to Internal PD
2.Delete R69 ,due to Internal PD
3. Add U70,U71,R69,R92 R1297 for serial falsh support.

Page19 : Add T8/T9 for GPIO10/14

Page23 : Change L1,L2,L63,L6,L7,L9,L11-16,L65,L66 to FB

Page30 : Disconnect the I2C bus / WL_LED#/WP_LED# on JP46

Page10 : 1. Add R504/R505 for VCC_SYNC
2. Add R490/R491 for VCCTX LVDS
3. Add R494 for VCCA_CRTDAC
4. Add R492/R493 for VCCA_LVDS
5. Add R495 for +3VS_TVBG
6. Add R500 for +3VS_TVDACA
7. Add R502 for +1.5VS_TVDAC
7. Add R499 for +3VS_TVDACB
8. Add R496 for +3VS_TVDACC

Page09 : 1.Add R460,R461, R550,R552,R553 for CRT discrete/uma option
2. Add R462,R463,R464 for TV discrete/uma option

06/13/2005

Page23 : Add R6 R15,R106,R128,R129 GPIO PD

06/14/2005

Page21 : Change L1,L2,L63 to FB

Page16 : 1. Add C174,C150,C142,C371,C358 for DVI
2. R103 change to 1%

Page35 : U69 pin7 change to PD

06/15/2005

Page04 : R1265 change to 51_0402_5% & install

Page07 : Install R1344

Page28 : Delete U70 ,reserve U71 for 200 mil

Page35 : Delete U61 , resevre U66 for 200 mil

Page29 : Update U7 symbol pinB7/B8/C8

06/16/2005

Page36 : Delete R32 ,double PU

Page41 : Delete R180,Q49 , the same function for +1.8VS

Page10 : Delete C982 for Lead-free

Page20 : Add C570 for Lead free

Page32 : 1,Delete Q28 .
2. D49,D50 change to U73
3. Add C577,C581 for Lead free

Page33 : Add R163,R164,R165 for USB power switch PU

Page26 : Separate PCIE_WAKE# to NIC/Mini-card PCIE_WAKE# to avoid battery mode can't enter S3 issue

Page23 : Delete L65,C270,C269,C271 for M52-T

Page18~23 : ATI VGA controller change to M52T

06/22/2005

Page09 : Add R554 , R555 for CRT disable

Page10 : 1. Add R508,R510 for VCCD_LVDS1/1/2
2. R504,R505 chnage for +2.5VS_GMCH,&delete R490,R491,R492,R493

Page30 : Delete JP48,49 & change screw holes

06/23/2005

Page16 : Change SDVOB_INT+/- net name to PEG_RXP1/N1

Page10 : 1.R505 / R510 for M52 , R504 / R508 for UMA
2. R499,R500,R496 connect to +1.5VS for diable CRT

Page36: Delete R49 & CB_CLK

Page25: JP42 change to wire to board connector

Page19: 1.Add CRT,TV filters for M52T
2. Add DVI BOM option 0 ohm

Page16 : Move 0 ohm to TV-out connector for TV

Page38 : Move 0 ohm to docking connector for CRT

06/24/2005

Page19 : Add LVDS L-shape BOM option resistors

Page10 : Enable TV/ CRT when using 945PM

Page9 : Enable TV/ CRT when using 945PM

06/25/2005

Page33 : Delete U58, R165,C568,C1,C312,C311 FOR LAYOUT SPACE

06/27/2005

Change A11 2N7002_SOT23 to RHU002N06_SOT323 to save layout space

06/28/2005

Page40 : Change Q10,Q11,Q15,Q26 from SOT23 to SOT323
to save layout space

Page37 : 1 . Update JP20 to 6 pin connector
2. Update JP20 & JP18 pin assignments to follow Taos

06/30/2005

Page28 : Y1 update to smaller package 6x3.5

Page25 : Y4 update to smaller package 14M-J

Page15 : Y3 update to smaller package 6x3.5

07/01/2005

Page23 : Add HW strpping pin on DVPDATA20,21,22,23 for VRAM ID0,1,2,3

Page33 : U57 change to 2A current limit power switch G548

07/04/2005

Page17 : Add R131 for inverter PWM when ATI PWM issue

Page19 : 1. Add R49 , R189 for 1.2V voltage divider
2. Add Q12 for M52_therm# & change to GPIO14

Page32 : The limitation for 5 pin audio jack can't switch
headphone/docking line-out ,so add R1420,R1421,C526,R252
Delete R256,R255,C536.

Page39 : Delete C984~C988

Page33 : Delete C527

Page10 : Delete C823 reserved pad

Page25 : Add JP5 slim type ODD connector

07/12/2005

Page25 : Add C629,C630,C631 for SATA connector

Page33 : Swap JP3 samrt card pin assignment for FFC

07/14/2005

Page25 : Add R133 100 ohm to avoid RTC short

Page15 : 1. clock gen. pin 5 change to connect to +ck_vdd_dp
2. C731,C732,C733 change from 0.1u to 0.01u
3. C361,C364 change from 33p to 27p

07/19/2005

Page39 : Add C91,C93,C181 for low speed signal

07/20/2005

Page30 : Add R1422 pad for XMIT_OFF

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For DB2 Modification

08/11/2005

Page31/32 : Update Audio portion for jack sensing
Page35 : Delete LED circuit & connect to LS-2953 directly
Page11 : Change R1154 to NI
Page30 : Add C554 for UIM power
Page25 : Delete JP37 MB2 conector
Page19 : Change C611 to NI ,R662 to 0 ohm for clcok spectrum
Page15 : Add R1136 PD for clk_pcie_m52 ,R1084 change to NI
Page24 : R1388 change to Install
Page26 : R1364 change to NI
Page36 : R1354 change to NI

08/15/2005

Page30 : R1418 , R1360 change to NI

08/19/2005

Page35 : Delete FWH , SPI change to +3VALW
Page36 :Delete R538
Page10 : Delete L39
Page25 : Add D15, D16 , R90 , R88 for HDD LED

08/20/2005

Page30 : Change +3VL / Caps_LED# to Pin45/51
Page38 : Delete R551 ,R548,R549,R541
Page25 : Add D15,D16,R88,R90 for HDD_LED
Page30 : Add SW1 C986, R521 , D65,D66 for SIM power off

08/24/2005

Page15 : Add C353~C372 for clk cap

08/25/2005

Page31/32 : Add JP16 for audio cable
Page30 : Internal MIC signal change to JP13

08/26/2005

Page32 : Add R427,R429,C492 for J_MIC_REF

08/29/2005

Page32 : Add 1423,R1424 for MIC_REF , & MIC_SENSE connection
Page23 : R154 change to NI
Page29 : Add C333 for NIC

08/30/2005

Page15 : Add C373 for clk_debug_port
Page23 : Add R173 for Therm_SCI#
Page36 : R538 change to NI
Page21 : Add C140, C172 , C141 , L17 for VDDPLL

08/31/2005

Page32 : Delete R1419, R1420
Page19 : R189 change to 56_0402_1%

10/04/2005

Page26 : R251.2/C526.1 connect to DLINE_OUT_L
Page32 : PR255.1 connect to pin 29 of the docking connector.
(ACOC_P_EN#)
Page29 : Add discharge circuit for BT_LED and WL_LED(R504,R505)
(this issue occurs when there is no WLAN card)
Page20 : Delete R1323 (EAPD to ICH7)
Page22 : Add Q40,R1419, reserve R1420
Page24 : Add R996,reserve R519,Q41,Q42
Page29 : Install R1409, Make R1380 NI ; reserve R101
Page30 : Reserve R91,R102
Page27 : Change R454 to 47K , add C556
Page25 : Install R136

Page15 :Delete R1071,R1073,R1076,R1082,R1094,R1096,R1258,R1260
R1112,R1116,R1250,R1252,R1124,R1127,R1134,R1137,R1238
R1239,R1242,R1248,R1253,R1272(NOLP@)

10/04/2005

Page32 : Reserve C555

10/06/2005

Page24: NI D64 ,install R1355
Page07: NI R1202,R1203
Page22: NI R1397,U36 ; Install Q94 ; Add R1076
Page29:Reserve U61
Page24:Add R1364 ; Reserve R1363
Page30:Install R91
Page24:Add R1366 ; Reserve R1365

10/07/2005

Page24: Add R1071,R1073
Page07: NI R1209
Page22: Install R275,R289 ; NI R1396,R1398
Page20: Install R1384,R1395 ; Reserve R1385,R1427
Del Q71,R1345

Page20: Add R1040,R871 ; Reserve Q106 ; Del R1404
Page22 : Add R1091,R1082,R1088,R1085,Q105,R1023,
R1024,D63,C1042,U55,R1021,R1076 ;
Reserve Q103,Q104,R1090,
Del R601.
Page15 : Del R1084,R1136

10/08/2005

Page28 :Install Q103 ; NI R1091

10/13/2005

Page33 :Delete J33
Page18 :Delete BIOS_SEL jump

10/26/2005

Page26 :NI C526
Page32 :Add R1404,R1428,R1429,R1430,R1431,R1432,
R609,R608,R611,R610,R613,R612,R616,R615
Page31 :Install CPl-CP6

10/31/2005

Page06 :NI C933 ;Modify 330U cap from ESR9 to ESR7.

For SI2 Modification

12/06/2005

Page06 :Del C938.
Page19 :Del C646
Page24 :NI R1355 , Install D64
Page30 :Install R33 ;Change RP43,44 to 10K ohm
Page31 :exchange netname between JP18's pin 25 and pin 24
Page34 :Del U45,U48,R1306,R117,R1307,C33,C993,C87

12/07/2005

Page20 :Del R1384,R1385,R1427 ;
Connect LP_EN# to GPIO8

Page15 :Add C740,C741,C744,C745 for EMI request

12/13/2005

Page20 :Add Q43 HALT LED issue
Page31 :Add R1084 and reserve R1096

12/15/2005

Page32 :Modify R1404 ,R1428,R1429 to 0603
Add C746,C747,C748 for EMI request

12/16/2005

Page22 :Del U71,R69,R92,R1297
Page24 :UI R1364,Install R1363
Page07 :Install R1201,R1204

12/16/2005

Page16 :Add R1369,R1367,R1368
Page32 :Add D16 for EMI request
Page30 :Change C350,C349 to 18pF
Page15 :Change C361,C364 to 18pF
Page19 :Change C516,C528 to 15pF
Page31 :Add D66 for EMI request
Page15 :Change R1075,R1081,R1129,R1132,R1148
,R1149,R1111,R1115 to 22ohm

For PV Modification

01/16/2006

Page07 :UI R1201,R1204 for SI-2 shutdown issue
Page15 :Change R1148,R1149,R1070,R1072,R1075,R1081,R1129,R1132
R1093,R1095,R1257,R1259,R1144,R1145,R1123,R1126,R1133,R1111
R1115,R1143,R1249,R1251 to 24Ω for CLK GEN vendor recommend
Page24 :R996 change to SM010014500 (220ohm impedance)
for improve WLAN performance

02/07/2006

Page24 : Modify R996 to 1000ohm/100MHz bead
Modify R996's location to L78
For power noise impact WLAN performance
Page24 : Connect R1363.2 to V_3P3_LAN, INSTALL R1363 and UI R1364
For support wake on WLAN from S3.
Page15 : Install R1245 and UI R1247
Page31 : Change Num_LED# and CAPS_LED#
For LED reverse issue
Layout :Modify +3VALW power trace width for LCDVDD

02/14/2006

Page20 : Add R1437
For HALTLED turn on 100ms when power on.
Page29 : Del U61. (150mil SPI ROM)
Page15 : Add C357,C372,C373,C374,C375,C376,C378,C379
To improve WWAN performance

02/16/2006

Page32 : Add R1433~R1436 on each DVI differential pair for EMI request.

02/20/2006

Page26 : Connect JP24 and JP15's 7,8pin to DGND.
For ESD concern.

02/21/2006

Page09 : Reserve ESD diode(D67) for C_HSYNC and C_VSYNC

02/23/2006

Page27 : Add D51,D52,D61 for EMI team request

02/24/2006

Page16 : Change C140 to 22u, R103 to 1.3K to fix DVI EMI issue

03/08/2006

Page26 : Change R1405 and R1406 to 12.1K

For MVL Modification

03/24/2006

Page19 : Change Y4 to a LF part.
Page22 : Change R70 to 1.21K to improve signal amplitude

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04/06/2006

Page32 : Change R1433~R1436 to 110Ω ;

Change R609~R613,R615,R616 to L79~L82 (common mode choke 90 ohm)

For DVI EMI issue

Page16 : Change C310,C313,C314 to 18P

For CRT EMI issue

Page09 : Change L28,L35,L27 to 0 ohm ; C193,C232,C237 to 12P

Change L31,L34,L26 to 39nH inductor

For CRT EMI issue

04/28/2006

Page22 : Install R1022 and UI R1021

For clock can't shut down under DC mode

Security Classification	Compal Secret Data			Title		
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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	42,44,50		8/26/2005 (DB)	HP	To implement 4 cell main battery	Add PR2,PR259,PR261 (1M ohm) , Add PQ73,PQ74,PQ75,PQ76 (RHU002N06_SOT323) Add PR260 (39.2k)	DB
2	48		8/30/2005 (DB)	HP	To fix VDD_CORE in 1V(Only for Discrete).	Remove PQ49,PQ66	DB
3	43		10/18/2005 (SI)	HP	Changes for OCP circuit	Add PC147 3900pF capacitor across PR214 Change PR207 from 0 Ohm to 3.9K_5% Change PC131 from 0.22uF to 0.027uF Change PR203 from 649K to 604K_1% Change PR221 from 47K to 10K_5% Add a newPR265 47K_5% resistor in series with PR216-2 Add a new PC146 1uF X7R capacitor from PR216-2 to GND Change PC133 from 10uF to 0.1uF X7R Change PR228 from 10K to 21K_1% Change PR234 from 11.5K to 3.48K_1% Change PR232 from 3.3K to 21K_1%	SI
4	37		10/18/2005 (SI)	HP	sets Max charge current to 3.75A	Change PR29 from 100K to 143K_1%	SI
5	43 37		12/06/2005 (SI2)	HP	Changes for OCP circuit	PR225 is open and PR26.2 connects to PQ63.1	SI
6	43		12/12/2005 (SI2)	HP	Changes for OCP circuit for 50W adapter	Correct PR223 from 180K to 182K. Change PR258 from 29.4K to 22.6K	SI2
7	41		12/19/2005 (SI2)	compal	DDR2 issue	Change PC78 from 220u to 330u Delete PC81,PR127	SI2
8	42		12/21/2005 (SI2)	compal	OTS#181928 Electrical printed circuit assembly acoustic noise test fail	Add PC148 (68uF)	SI2
9	41		01/16/2006 (PV)	compal	For 1.8V thermal shut down issue	Add PC81,PR127	PV
10			02/08/2006 (PV)	compal	OTS#184638 SVTP_S11:PC Card Wireless Radio Interference fail on GSM 850 and GSM 900 channel.	Change PL8,PL11 to shielded inductors	PV
11	37		02/17/2006 (PV)	HP	This change will slightly increase the battery life	Change PR38 to 866_1% Ohms Change PR41 to 100K_0.1% Change PR44 to 7.68K_0.1% Change PR53 to 2.80K_0.5% Add a 39.2_1% resistor in series with PR53. Connect one end to PR53.2 and the other end to GND.	PV

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