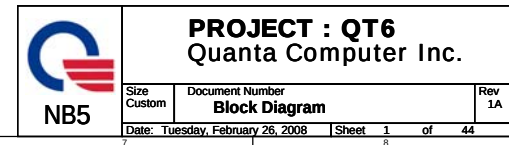
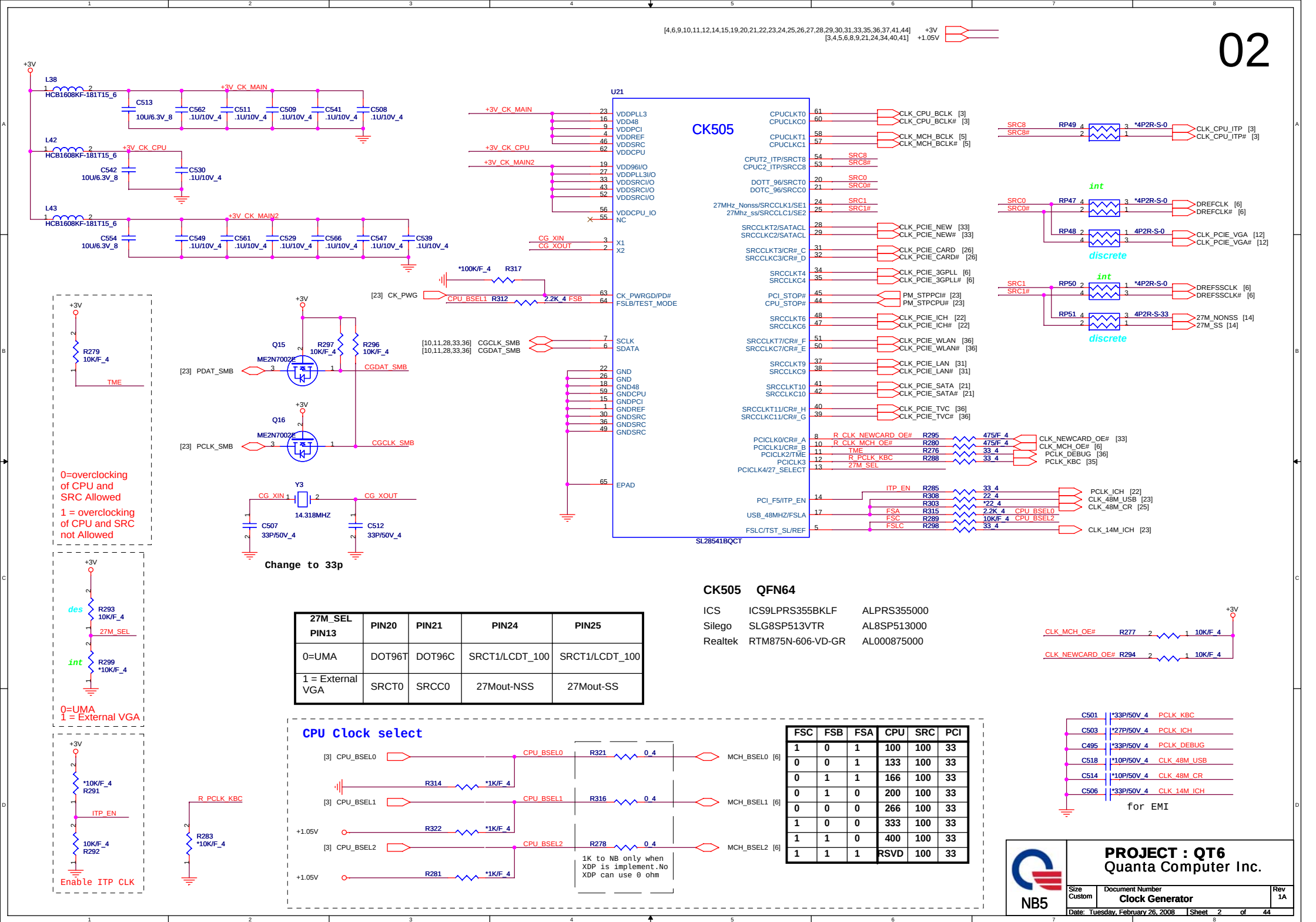
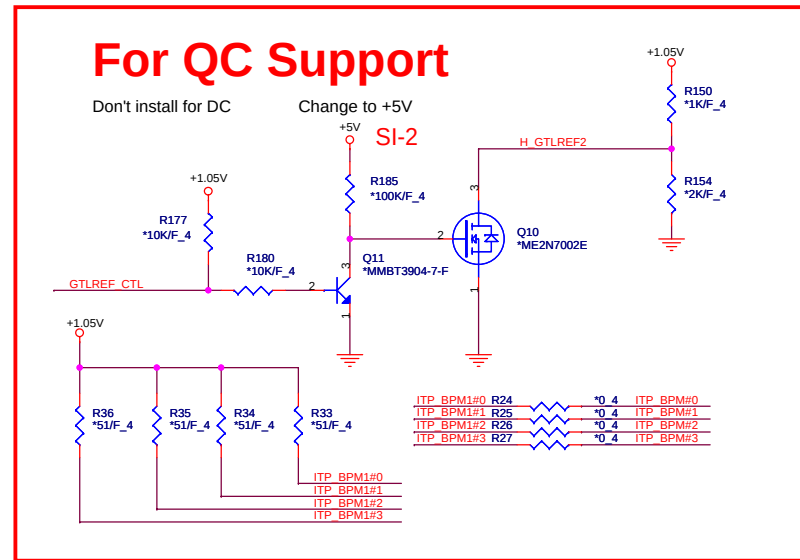
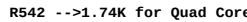


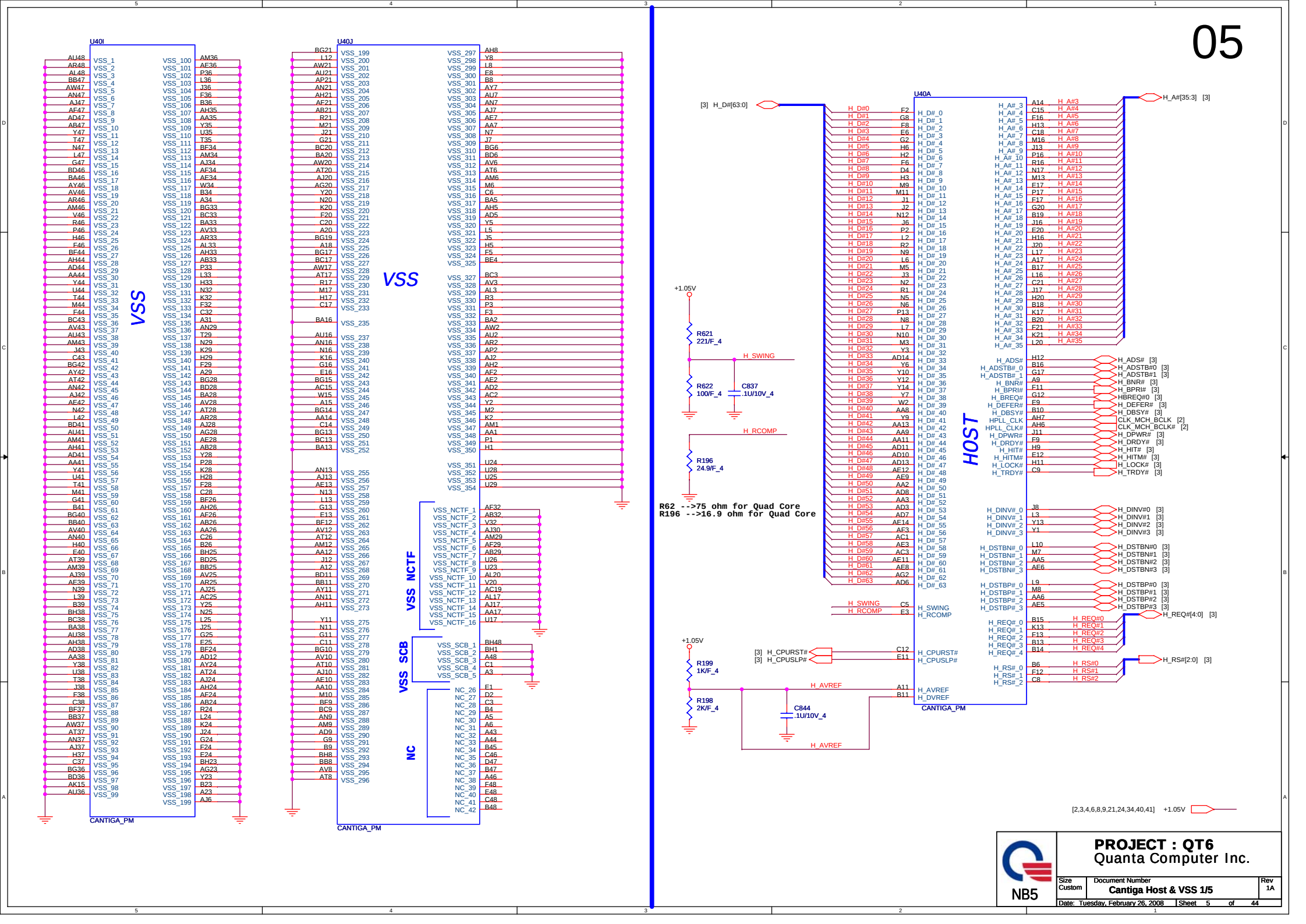
01

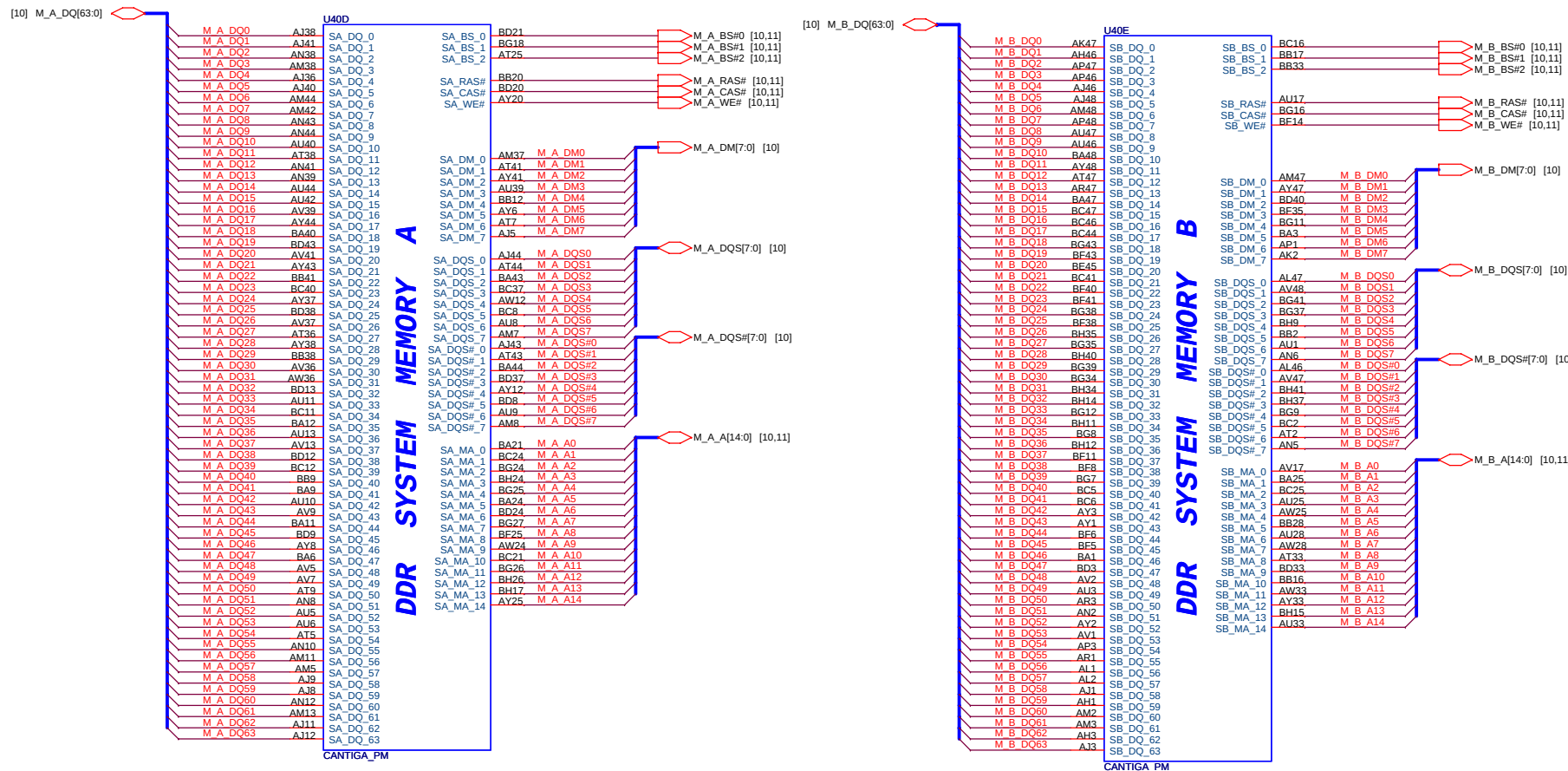






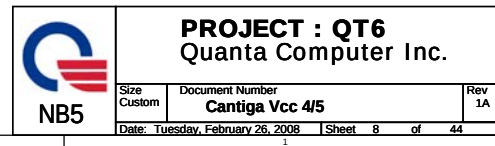


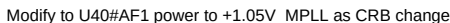


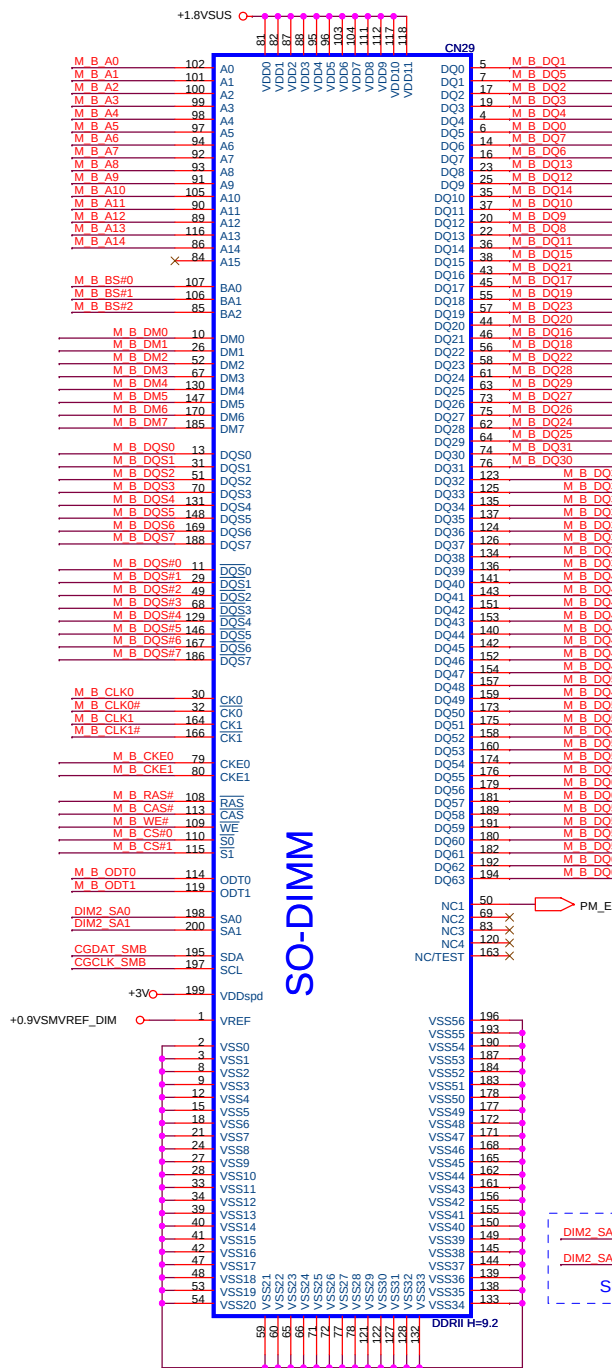


PROJECT : QT6
Quanta Computer Inc.

Size Custom	Document Number Cantiga DDR2 3/5	Rev 1A
Date: Tuesday, February 26, 2008	Sheet 7 of 44	

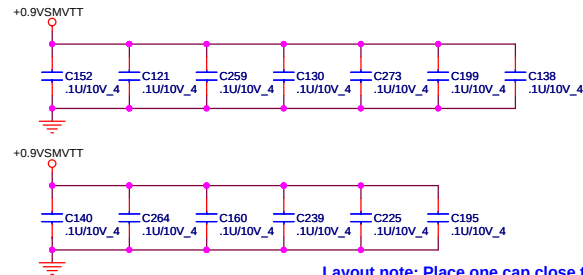






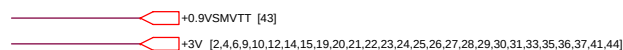
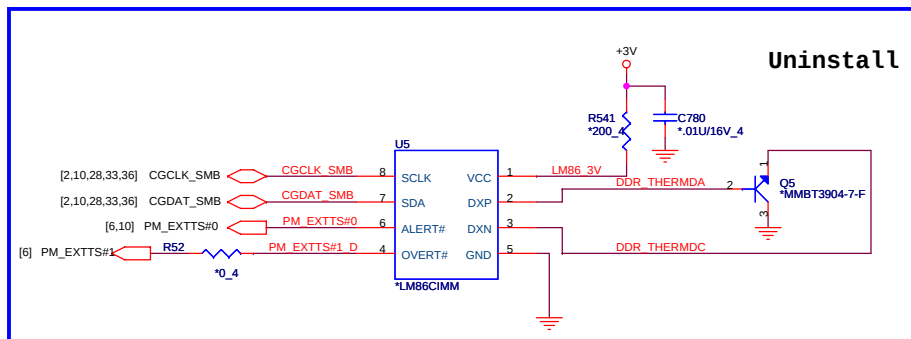
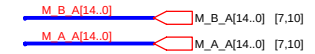
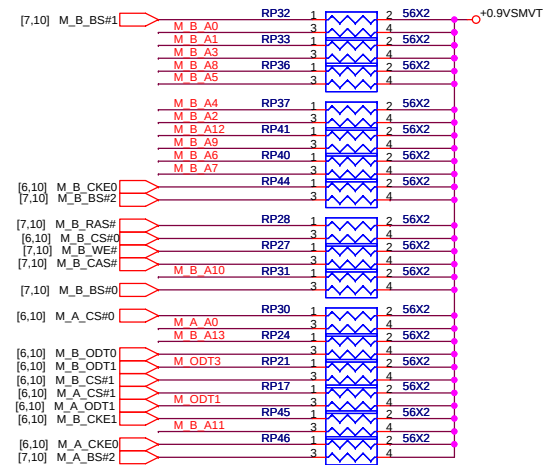
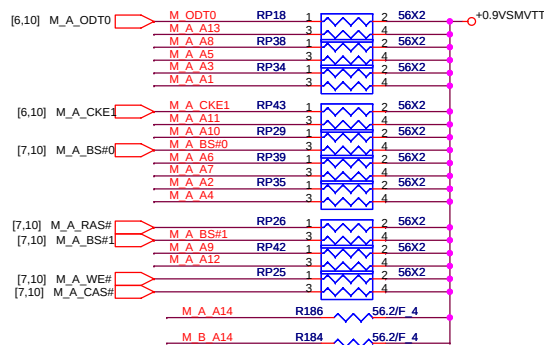
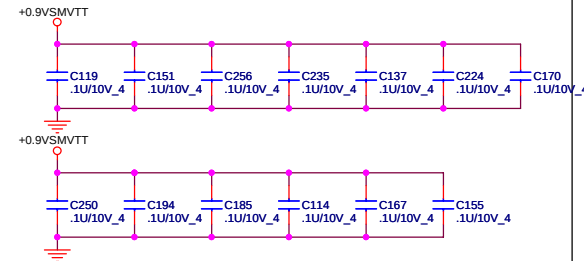
DDRII DUAL CHANNEL A, B.

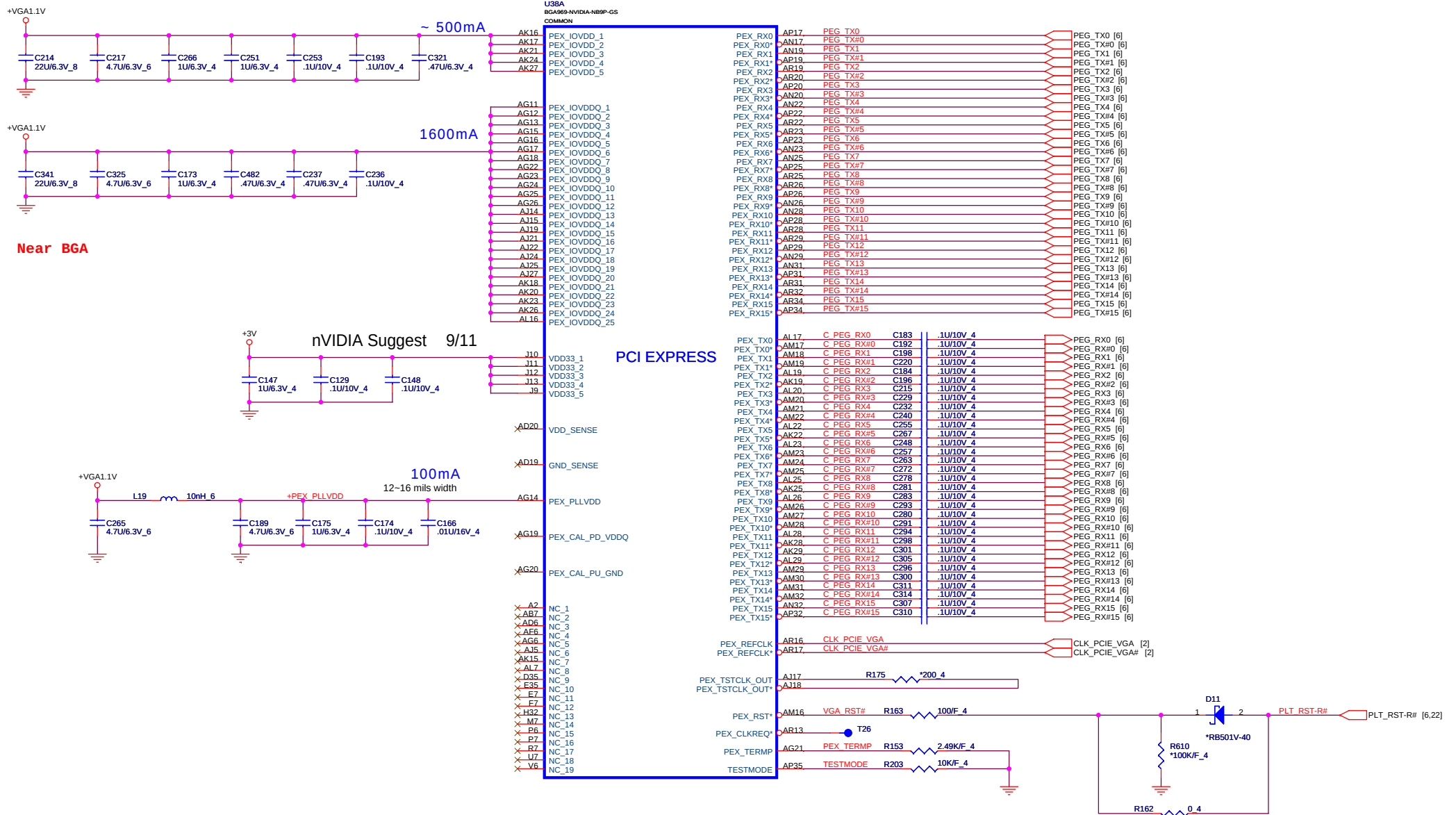
DDRII A CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

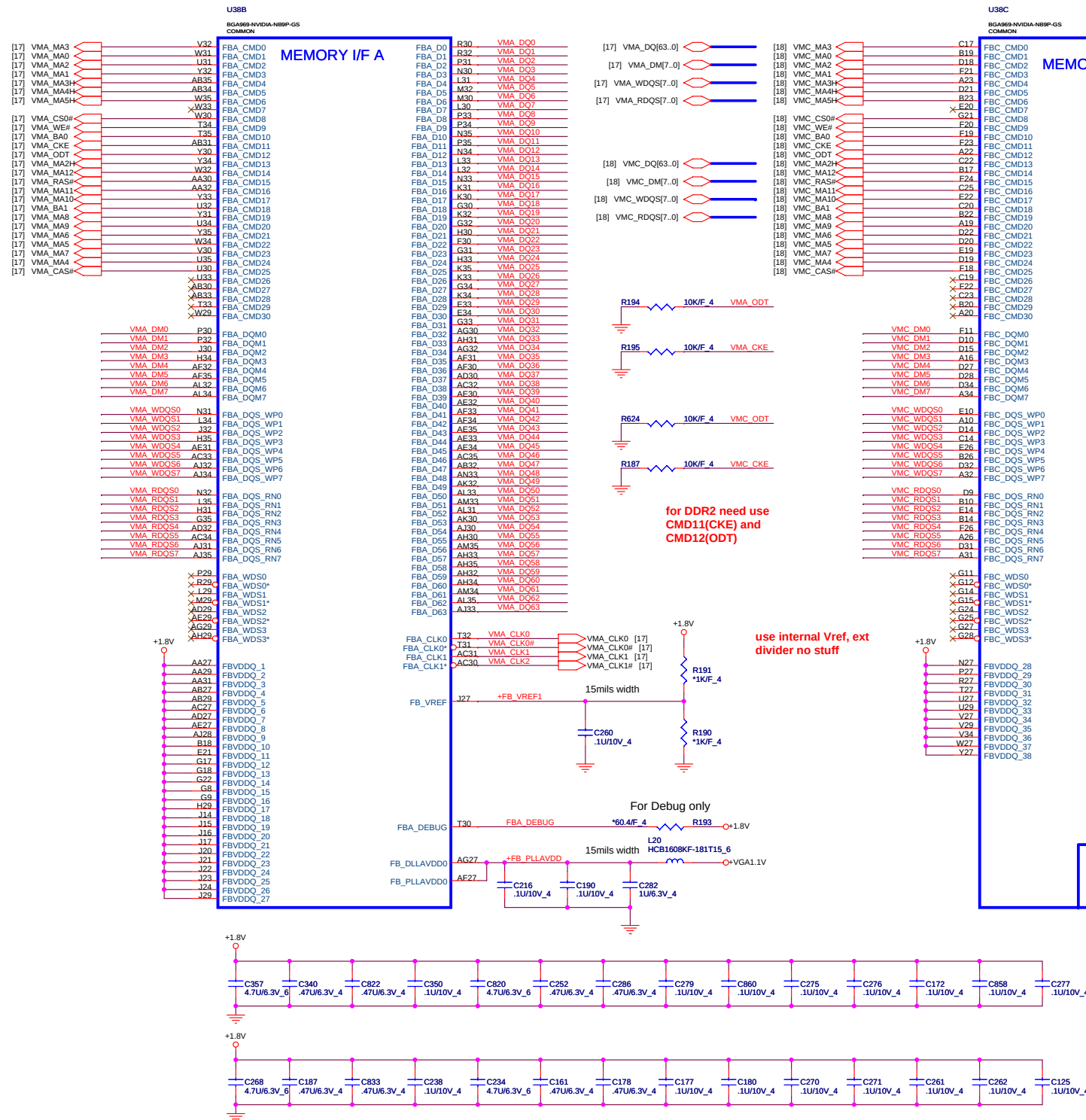
DDRII B CHANNEL

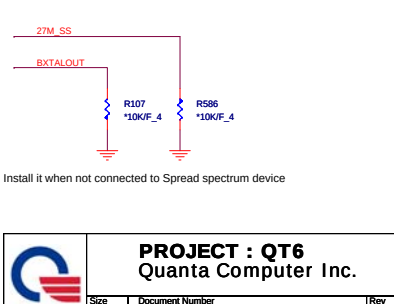
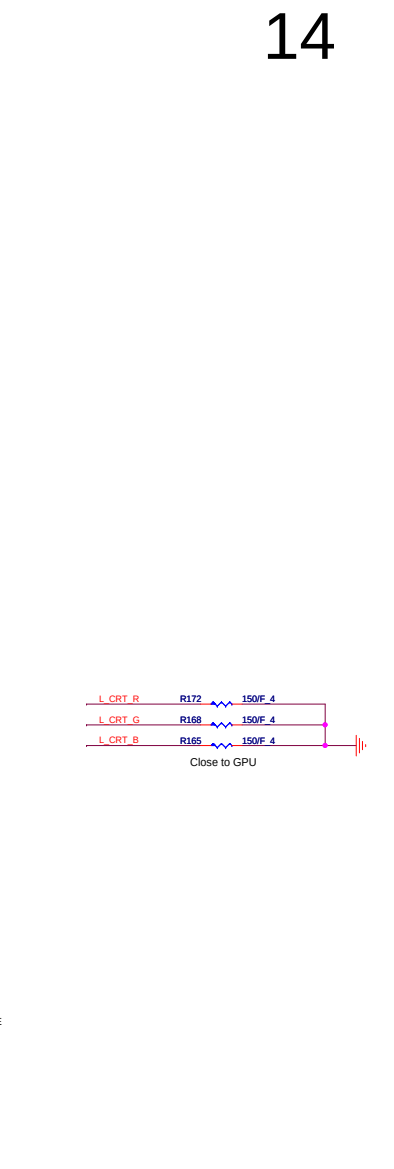




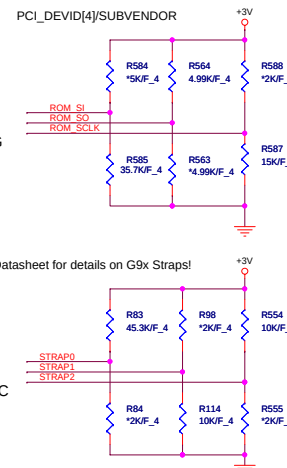
PROJECT : QT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV9X (PCIE I/F) 1/5	1A
Date: Tuesday, February 26, 2008	Sheet 12 of 44	





GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL



Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

PCI_DEVID: STRAP2 R554

NB9M-GE	0x06E 8	1000	PU	5K
NB9M-GS	0x06E 9	1001	PU	10K
NB9P-GE2	0x064 8	1000	PU	5K
NB9P-GS	0x064 9	1001	PU	10K

CS33572FB13	RES CHIP 35.7K 1/16W +-1%(0402)
CS34532FB18	RES CHIP 45.3K 1/16W +-1% (0402)

RAM ID: ROM_SI R585

SAM **0101** **PD** **30.1K**

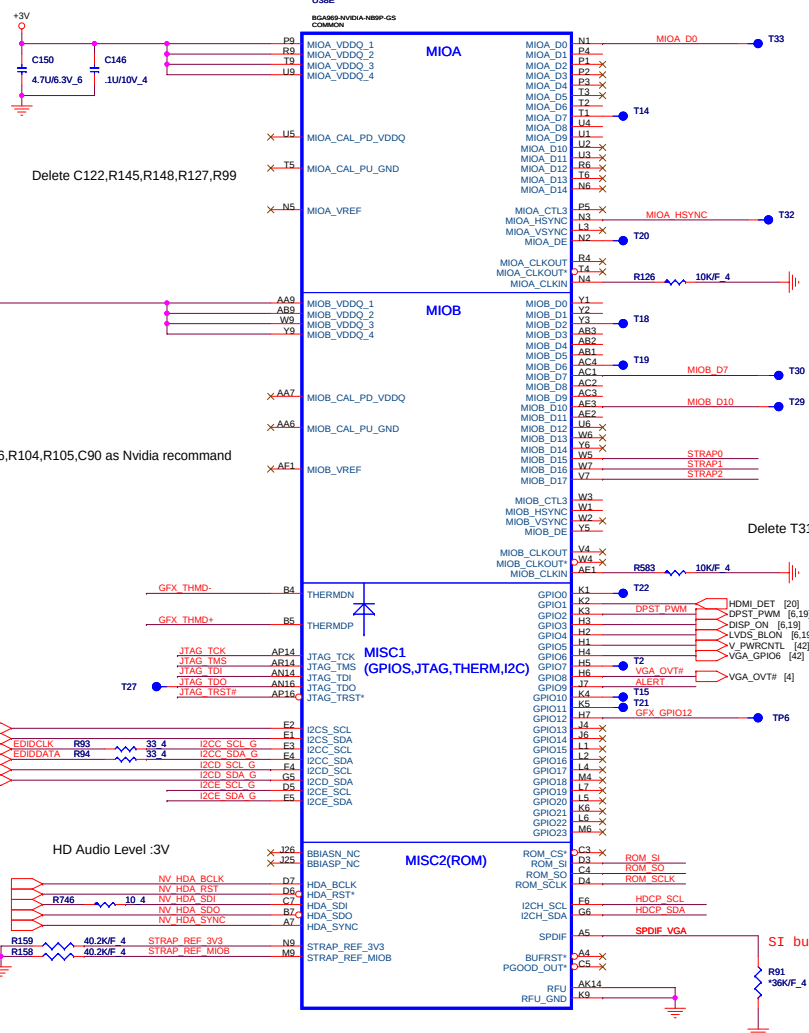
QIM 0110 PD 35.7K

HYN 0111 PD 45.3K

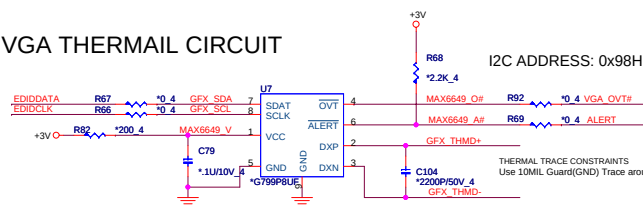


PROJECT : QT6
Quanta Computer Inc.

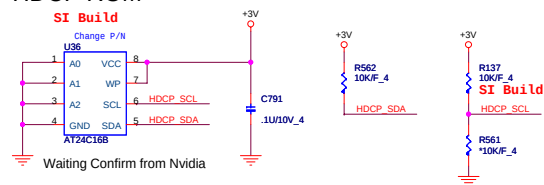
Size C	Document Number NV9X (GPIO & STRRAPS) 4/5	Re
-----------	---	----



VGA THERMAIL CIRCUIT



HDCP ROM

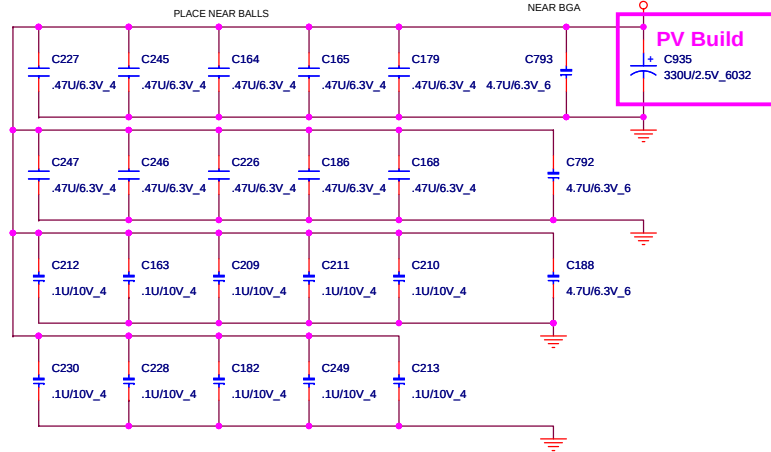
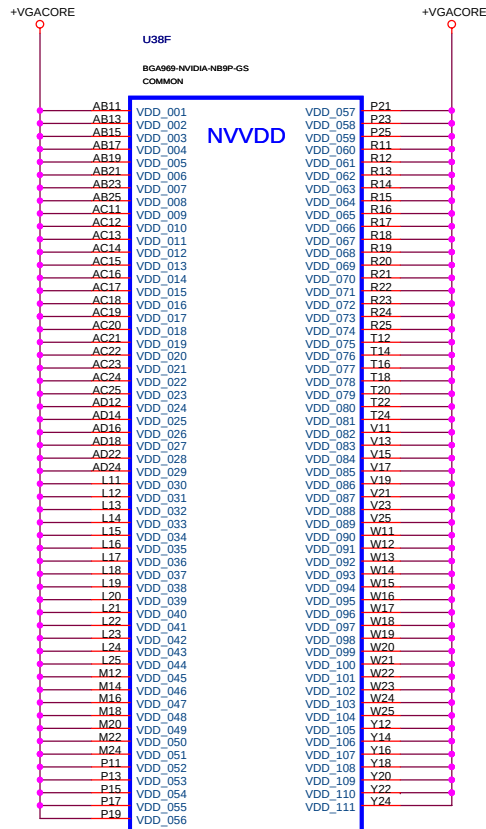


DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

NB9X VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix HY5PS121621CFP-25
0110	DDR2 32Mx16x8, 128bit, 512MB	Qimonda HYB18T512161B2F-25
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung K4N51163QE-ZC25
other	Reserved	

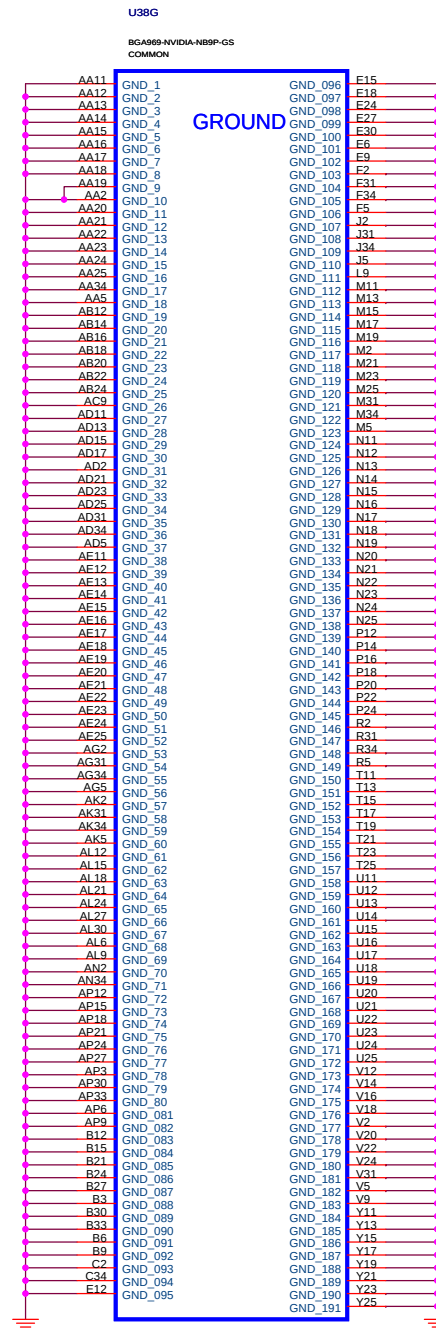
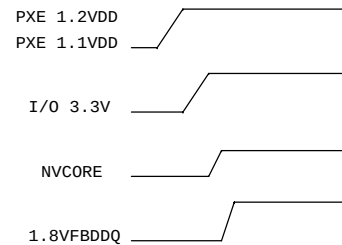
NVVDD Decoupling



Follow Design Guide DG-03276-001 4.7uFx3
and 0.47x10 uF instead of 0.1uF x10

NB9M: VGACORE +0.90V (Normal) , +1.09V

power up sequence

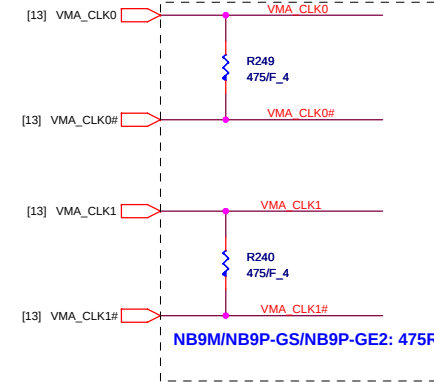
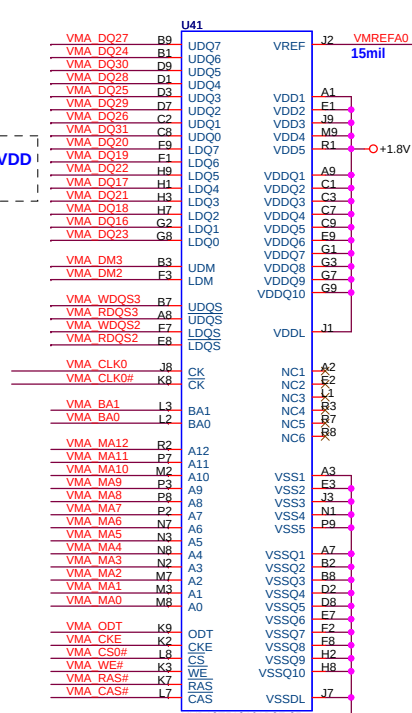


PROJECT : QT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV9X (POWER & GND) 5/5	1A
Date: Tuesday, February 26, 2008	Sheet 16 of 44	

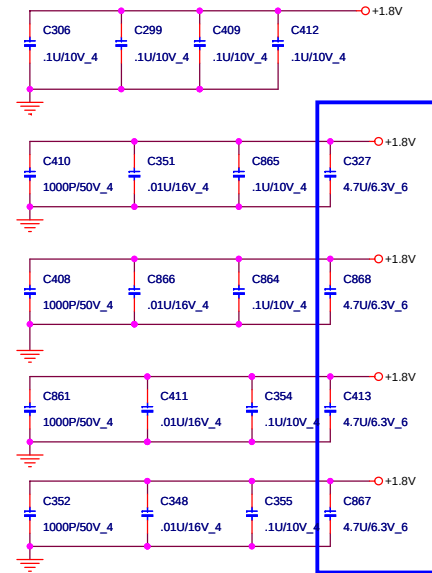


NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE: 50% , R635 (1K)



CS14752FB11 RES CHIP 475 1/16W +-1%(0402)

(By pass capacitor)

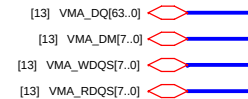


For DB:

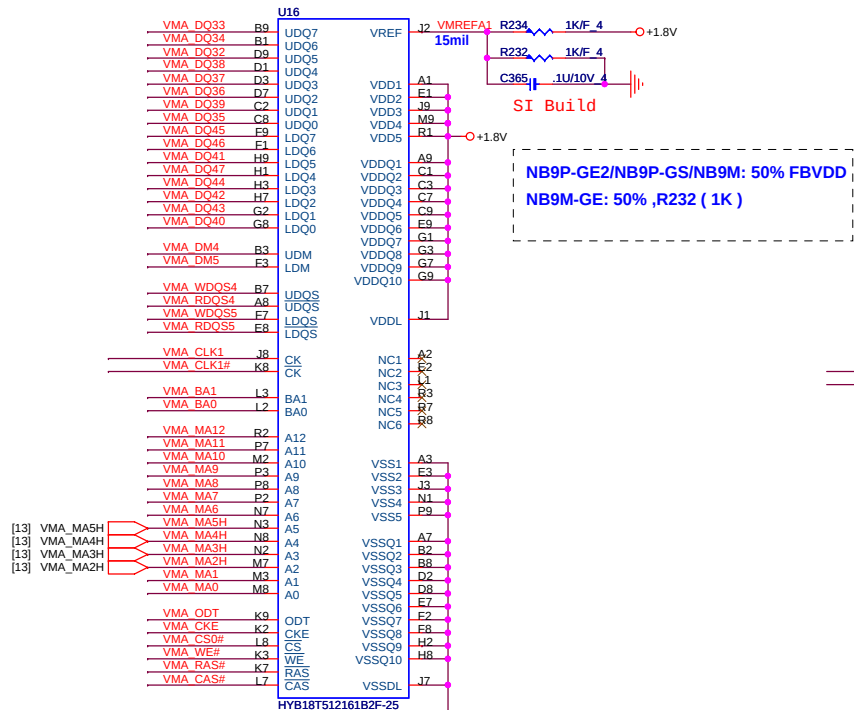
NB9P : AKD59G-T502(Samsung,32M*16)

NB9M : AKD5FG-TW31(Hynix,32M*16)

AKD5FG-T*03(Qimonda 32M*16)

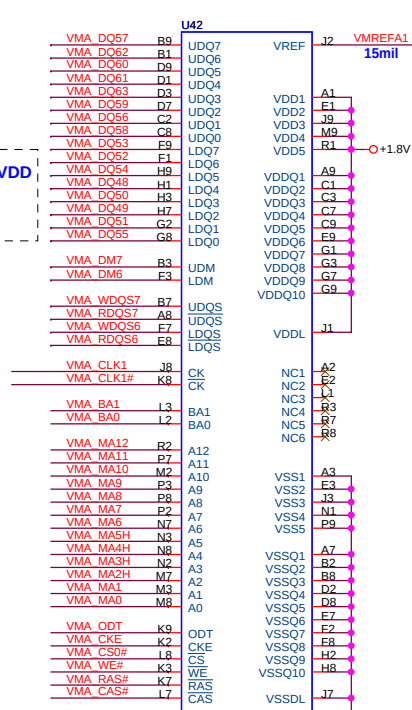


256Mb : AKD5JGAT*05
512Mb : AKD59G-T*01



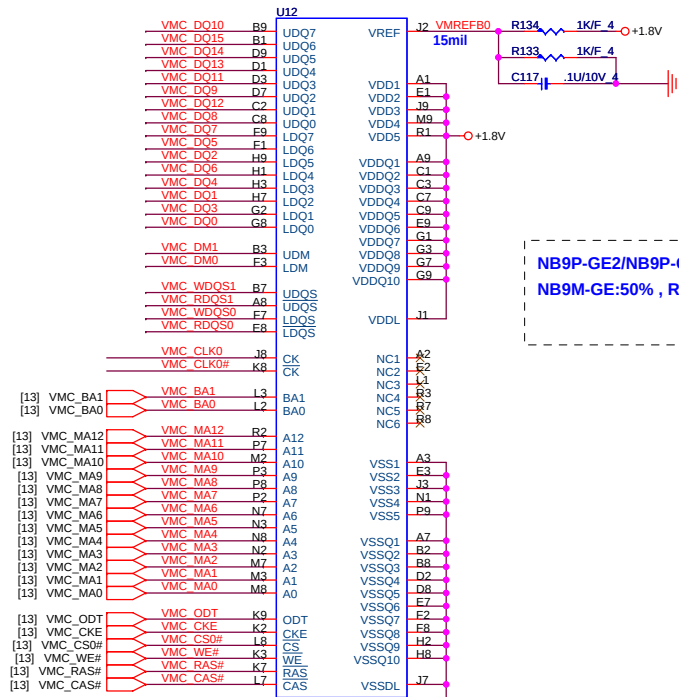
SI Build

NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE: 50% ,R232 (1K)

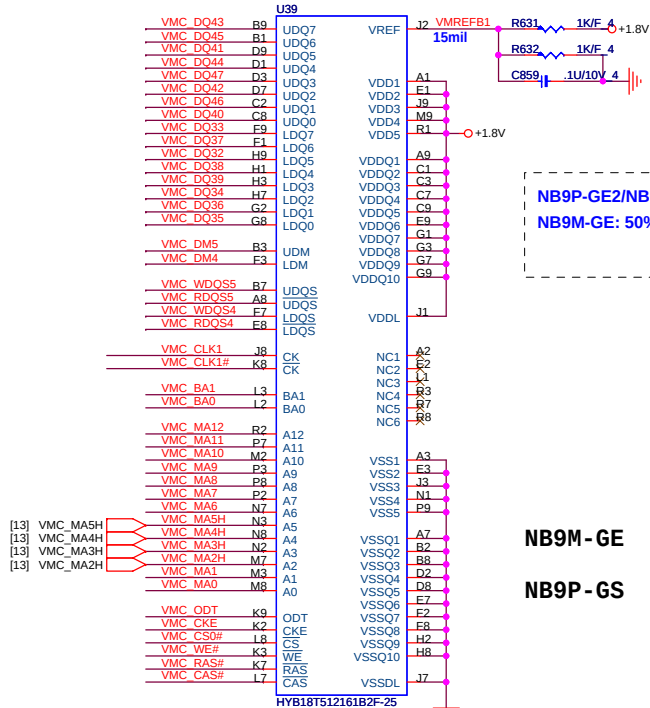


PROJECT : QT6
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	NV9X VRAM-1(GDDR2 BGA84)	
Date: Tuesday, February 26, 2008	Sheet 17 of 44	



NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE: 50%, R133(1K)

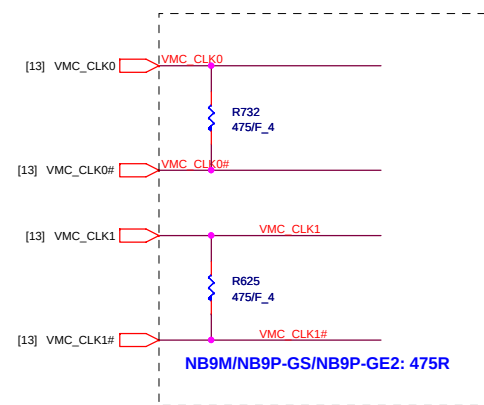
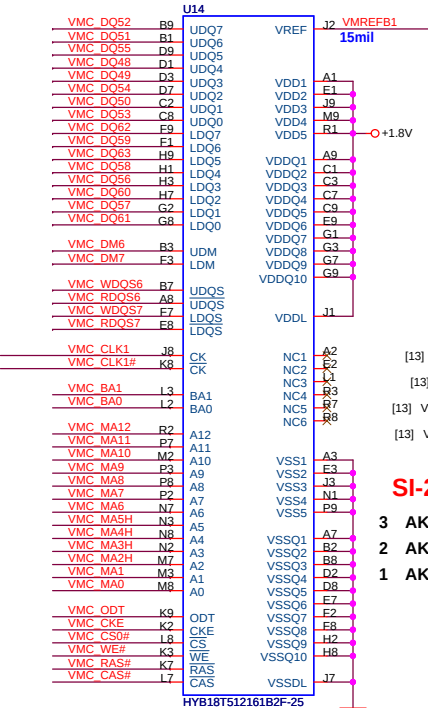
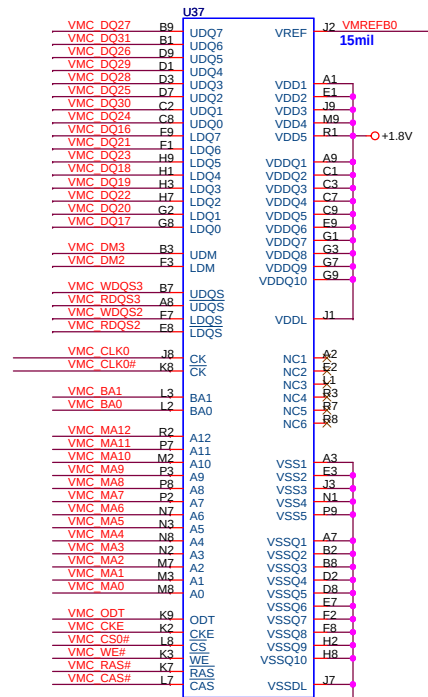


NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE: 50%, R632 (1K)

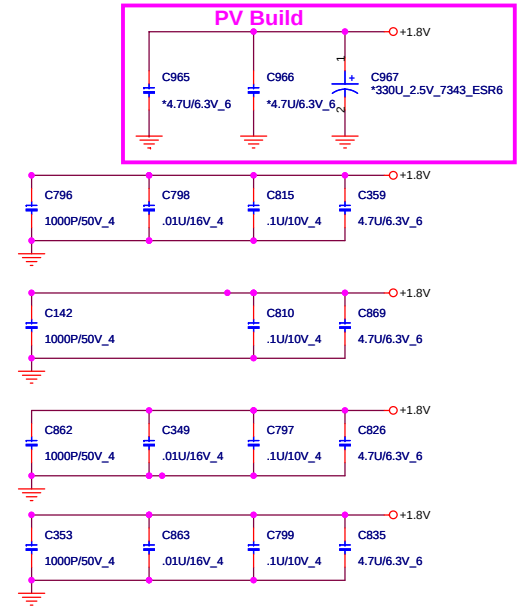
VRAM Vendor

NB9M-GE 1 3

NB9P-GS 2



CS14752FB11 RES CHIP 475 1/16W +1% (0402)



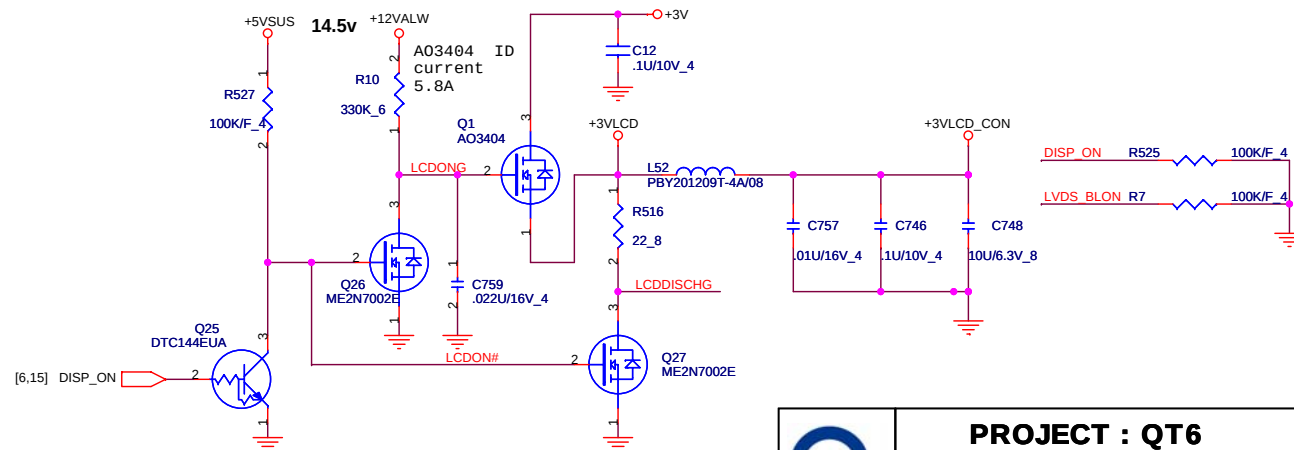
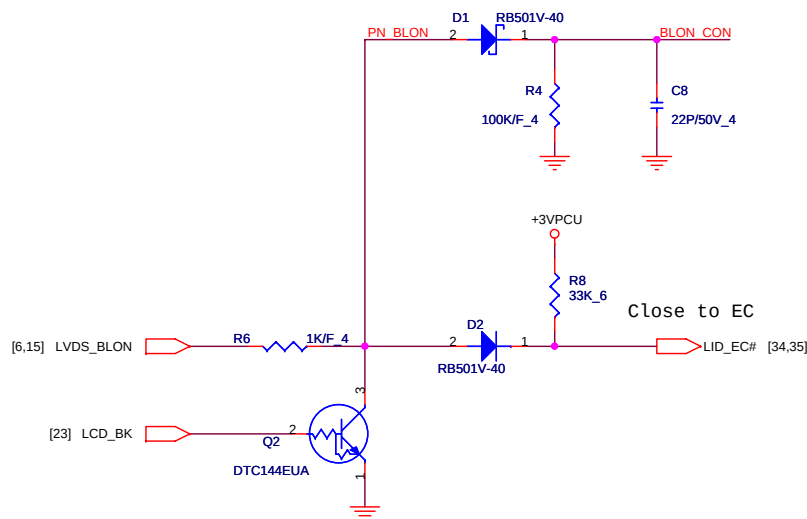
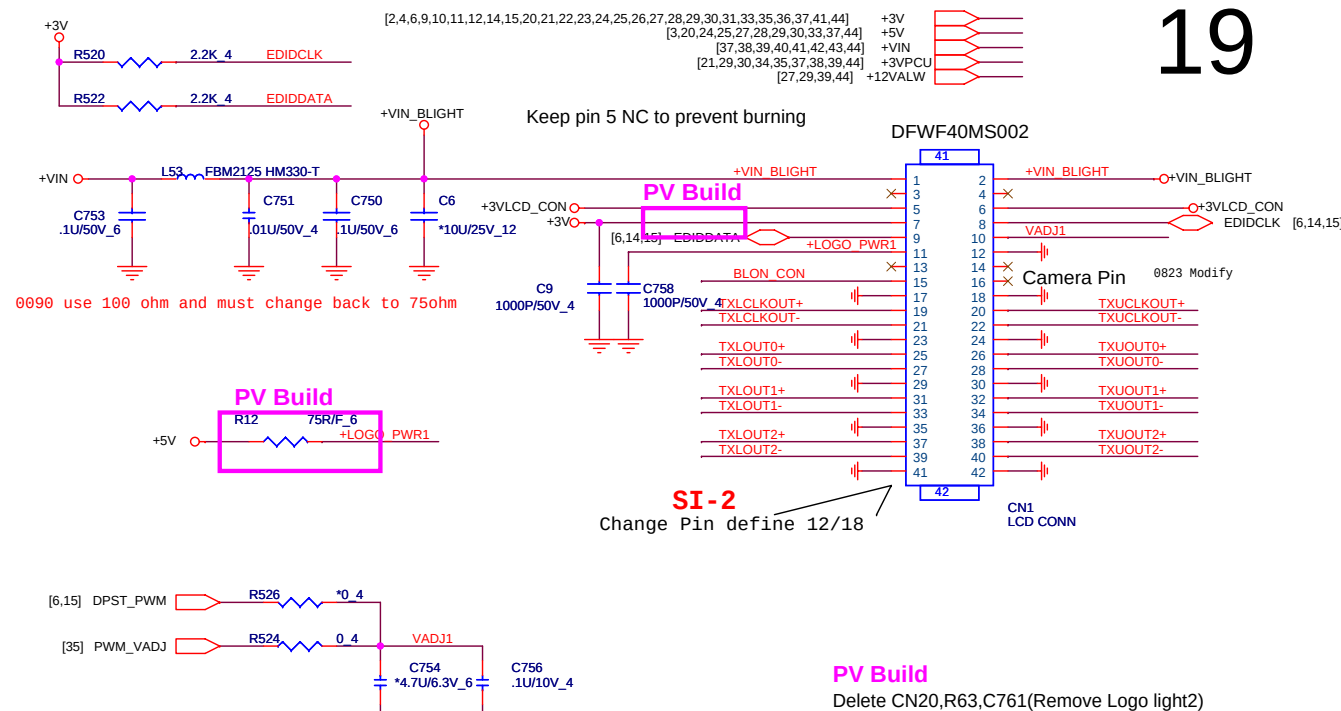
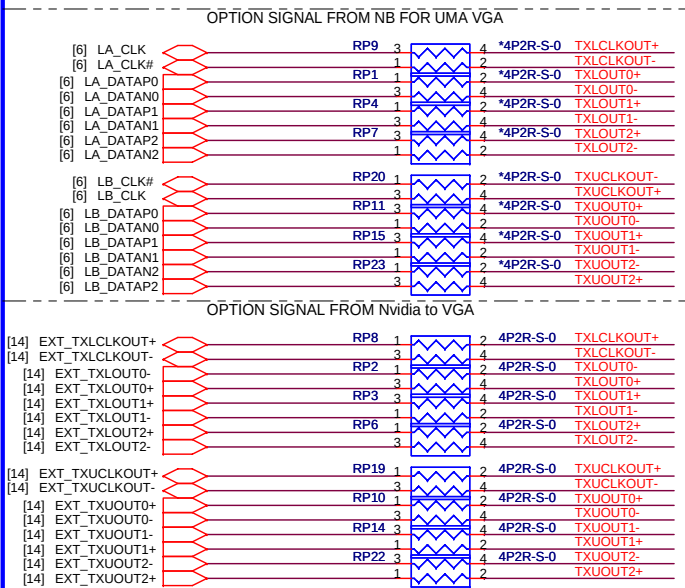
- [13] VMC_DQ[63..0]
- [13] VMC_DM[7..0]
- [13] VMC_WDQS[7..0]
- [13] VMC_RDQS[7..0]

SI-2

- | | | | |
|---|-------------|--|---------|
| 3 | AKD5FG-T501 | IC SDRAM(84P) K4N51163QG-HC25(FBGA) | Samsung |
| 2 | AKD5FG-TA03 | IC SDRAM(84P)HYB18T512161B2F-25(TFBGA) | Qimonda |
| 1 | AKD5FG-TW31 | IC SDRAM(84P) HY5PS121621CFP-25(FBGA) | Hynix |

NB5	PROJECT : QT6 Quanta Computer Inc.	
	Size Custom	Document Number NV9X VRAM-2(GDDR2 BGA84)
	Date: Tuesday, February 26, 2008	Sheet 18 of 44

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

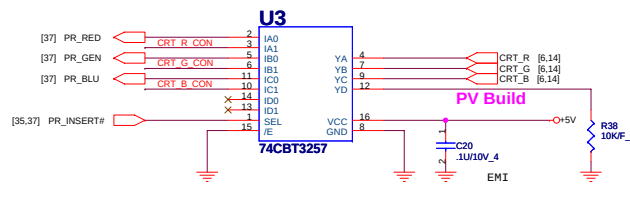


CRT PORT

PV Build
Change Layout footprint to dsub-070546fr015sx682r-15p-v

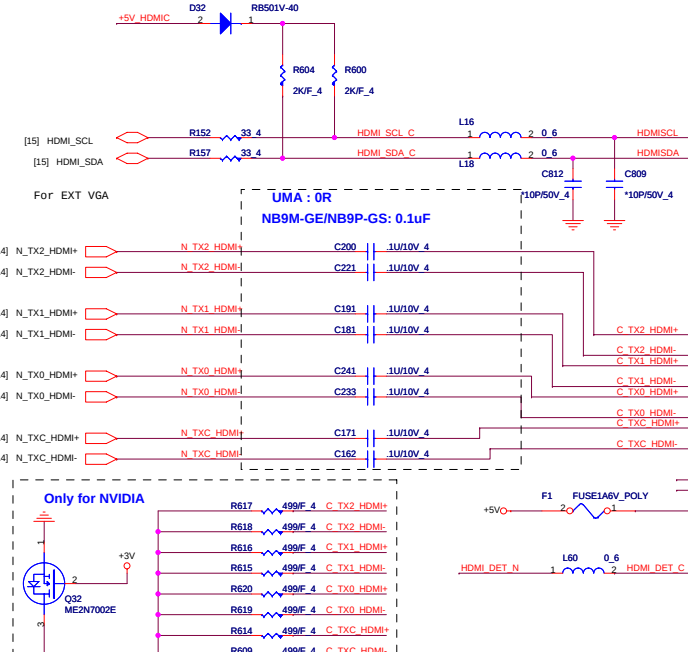
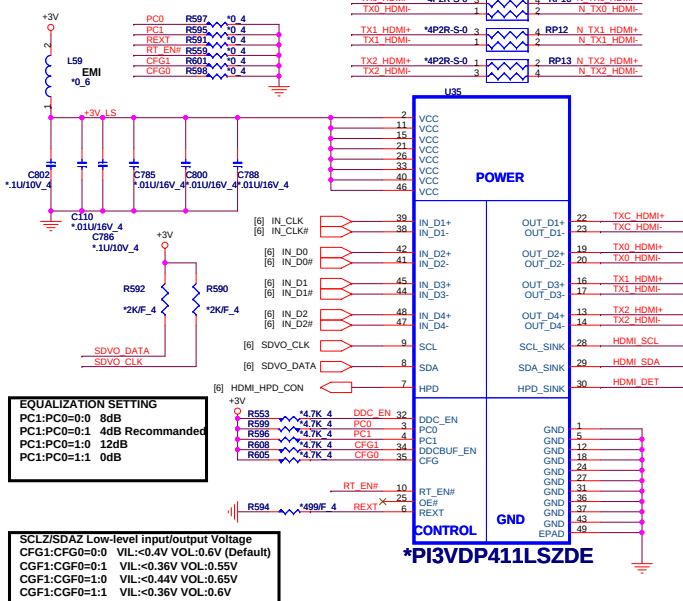
PV Build
Change ESD protection to +5V

CRT SWITCH

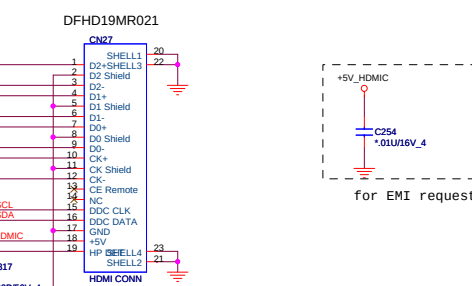


inputs	function
/E	SET
L	Y - port 0
L	Y - port 1
H	Disconnect

For UMA HDMI function



HDMI PORT





Low: Default
Hi: No reboot

SPI	0	1	(default)
PCI	1	0	
LPC	1	1	

A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default

TPM physical presence	
ICH_GPIO57	Low: Default

*1K/F 4 R391 GNT3# [22]

The diagram shows a pull-up resistor network. A +3V5 supply is connected to a resistor R704 (10K/F_4). The other end of R704 is connected to a node that is also connected to a resistor R706 (100K/F_4) and the ICH_GPIO57 pin. The other end of R706 is connected to ground.

Close to U45

For Discrete

C691 *10P/50V_4 C605 *10P/50V_4 C693 *10P/50V_4



Close to U45 C691 C605 C693
For Discrete *10P/50V_4 *10P/50V_4 *10P/50V_4

SWAP PCIE PORT6 TO PORT2 (Lan and New card swap) -->Rename the port name by function and port

[2,4,6,9,10,11,12,14,15,19,20,21,23,24,25,26,27,28,29,30,31,33,35,36,37,41,44] +1.5V
[4,9,21,24,27,29,33,36,40,44] +3V
[23,25,30,36,40,41,42,44] +3VSUS

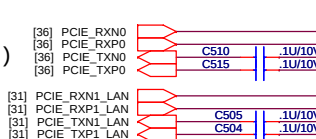


22

MINI CARD PCI-E(WLAN)

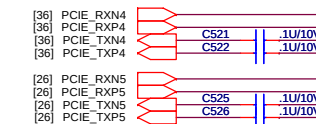
SI-2

PCIE-LAN



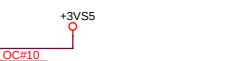
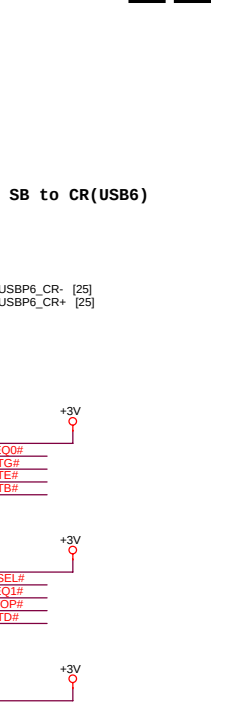
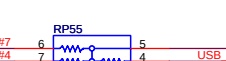
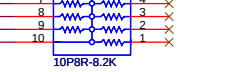
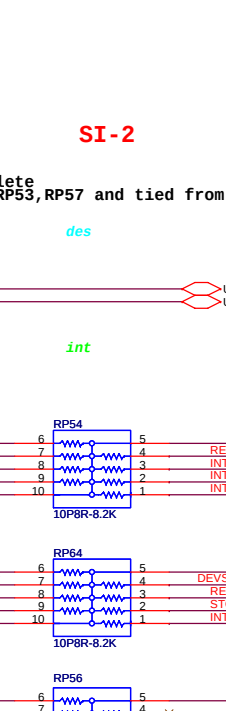
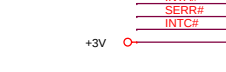
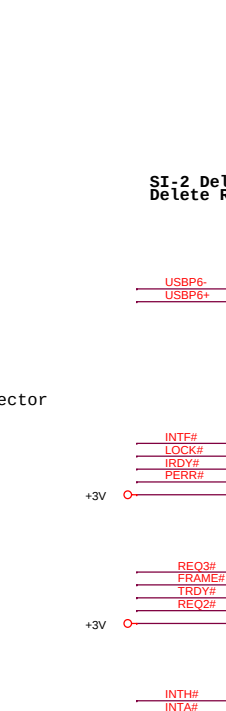
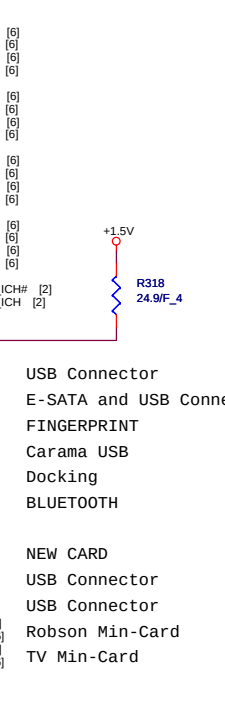
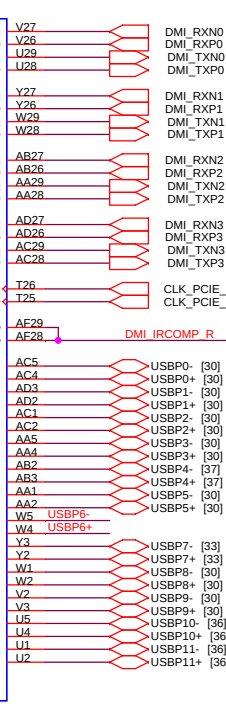
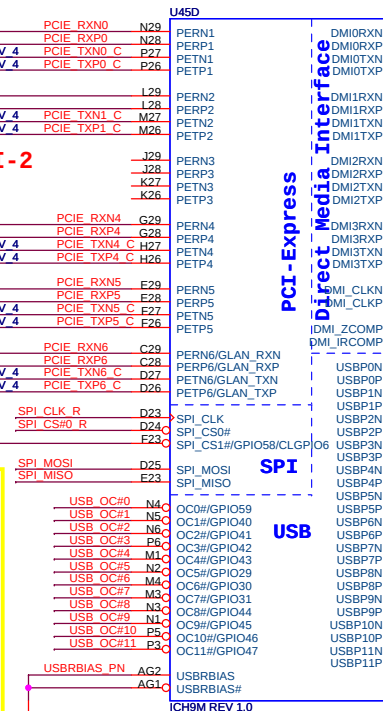
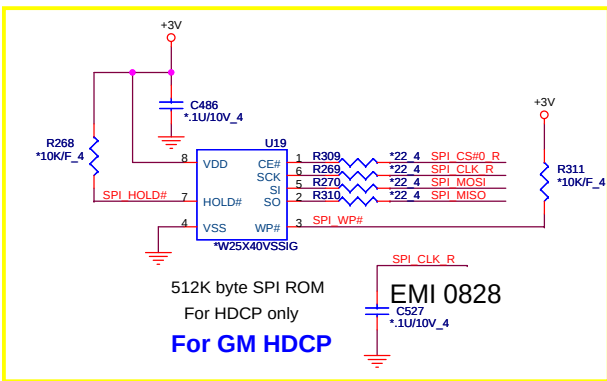
SI-2

TV CARD PCI-E

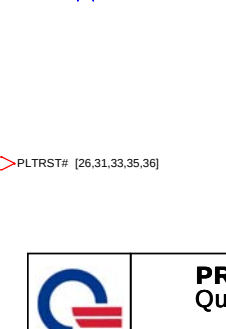
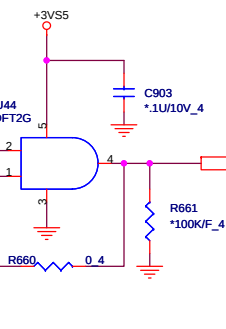
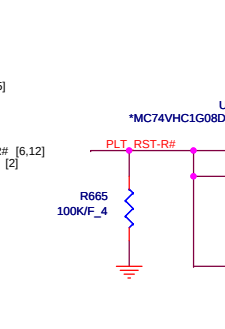
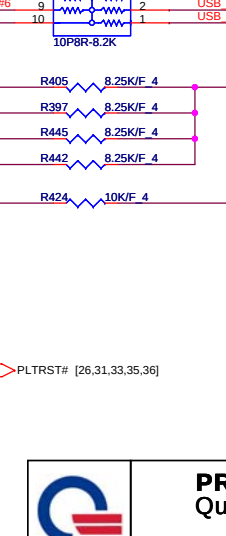
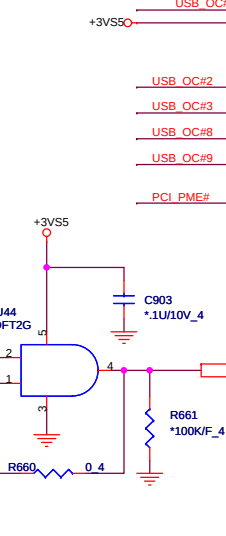
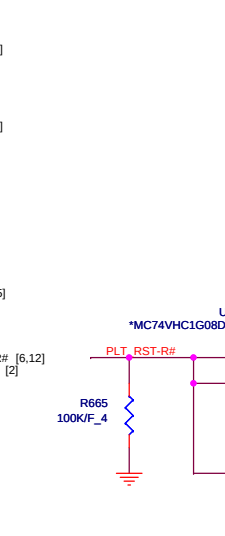
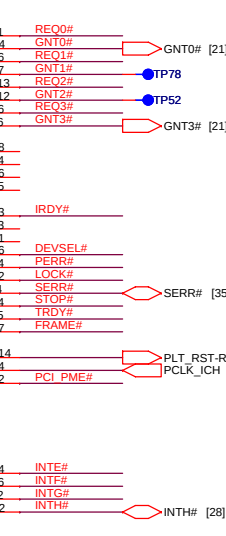
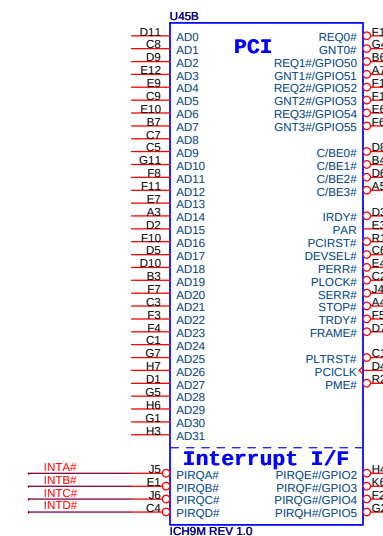
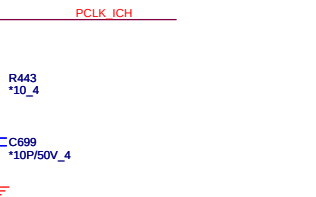


SI-2

EXPRESS CARD (NEW CARD)



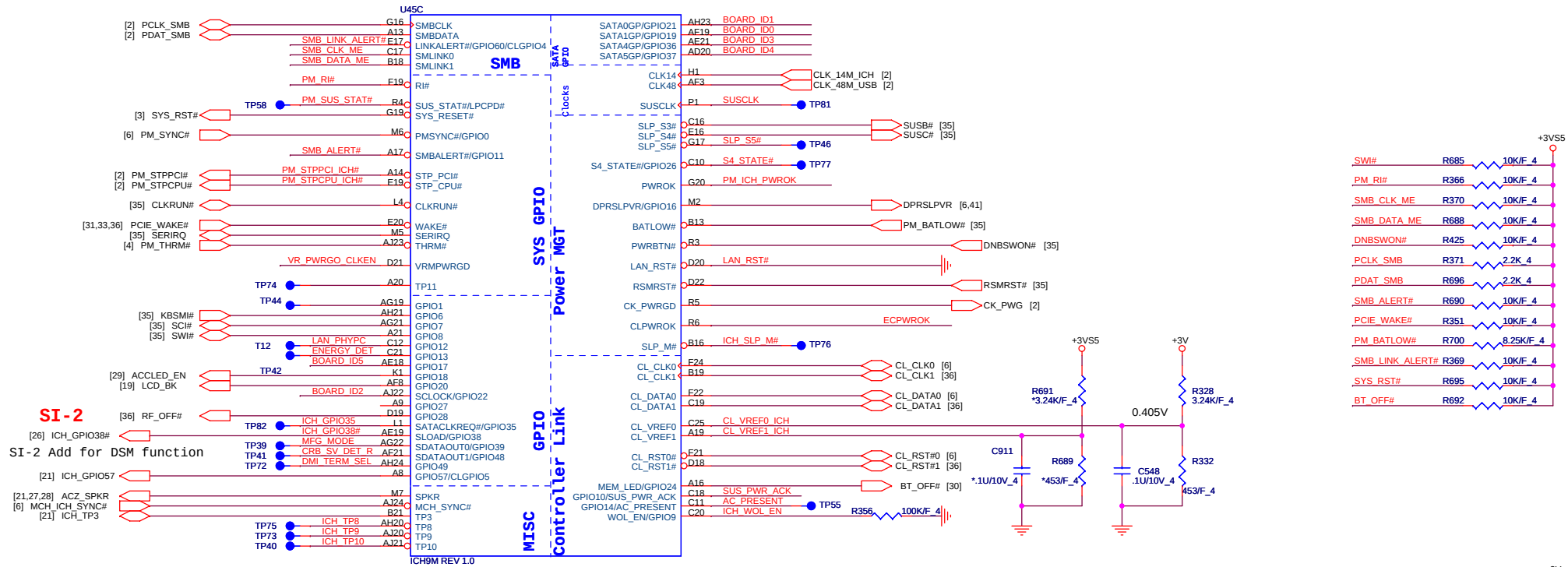
PV Build



PROJECT : QT6
Quanta Computer Inc.

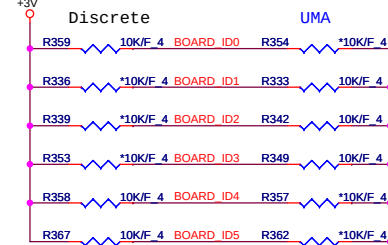
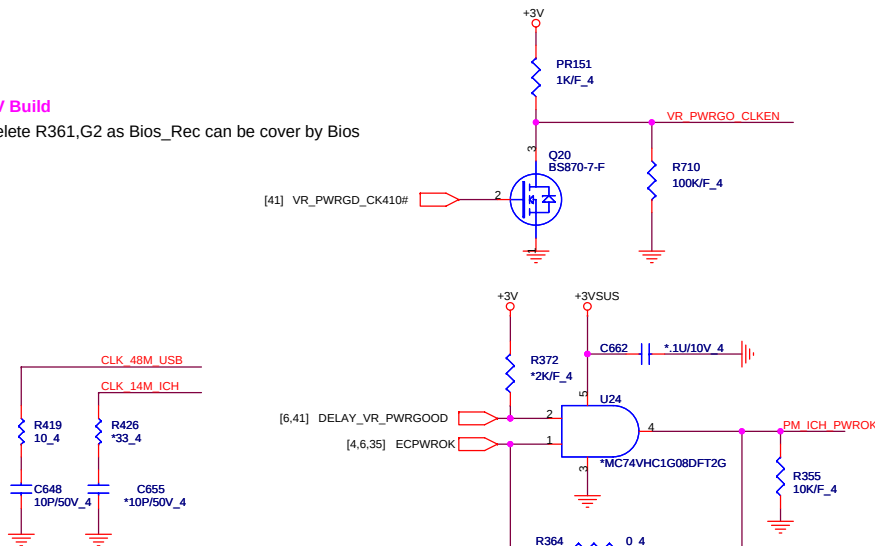
Size Custom	Document Number ICH9-M PCIE 2/4	Rev 2B
Date: Tuesday, February 26, 2008	Sheet 22	of 44

[2,4,6,9,10,11,12,14,15,19,20,21,22,24,25,26,27,28,29,30,31,33,35,36,37,41,44] +1.5V
 [21,22,24,33,44] +3V
 [25,30,36,40,41,42,44] +3VSUS



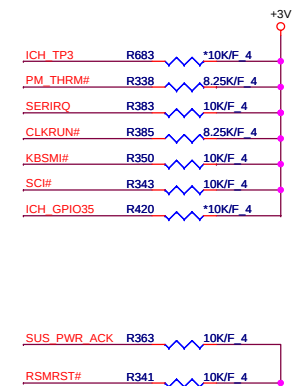
PV Build

Delete R361,G2 as Bios_Rec can be cover by Bios



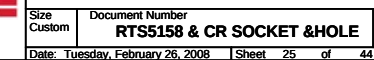
Board ID 0: 1-->Discrete , 0-->UMA

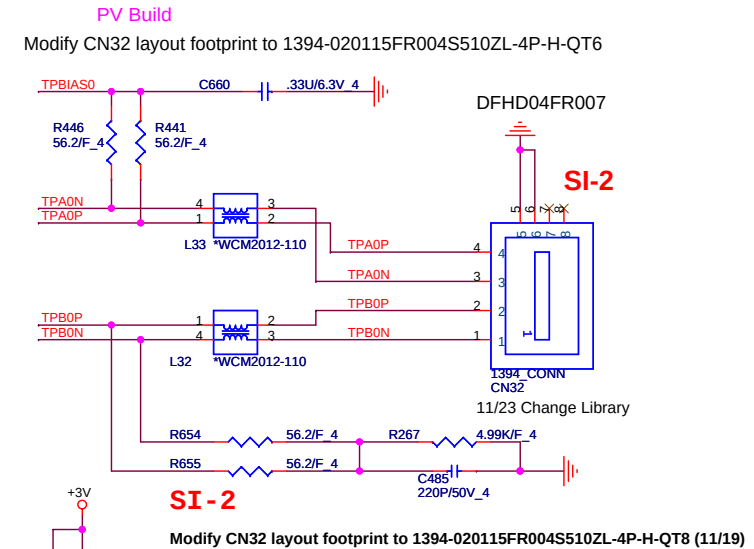
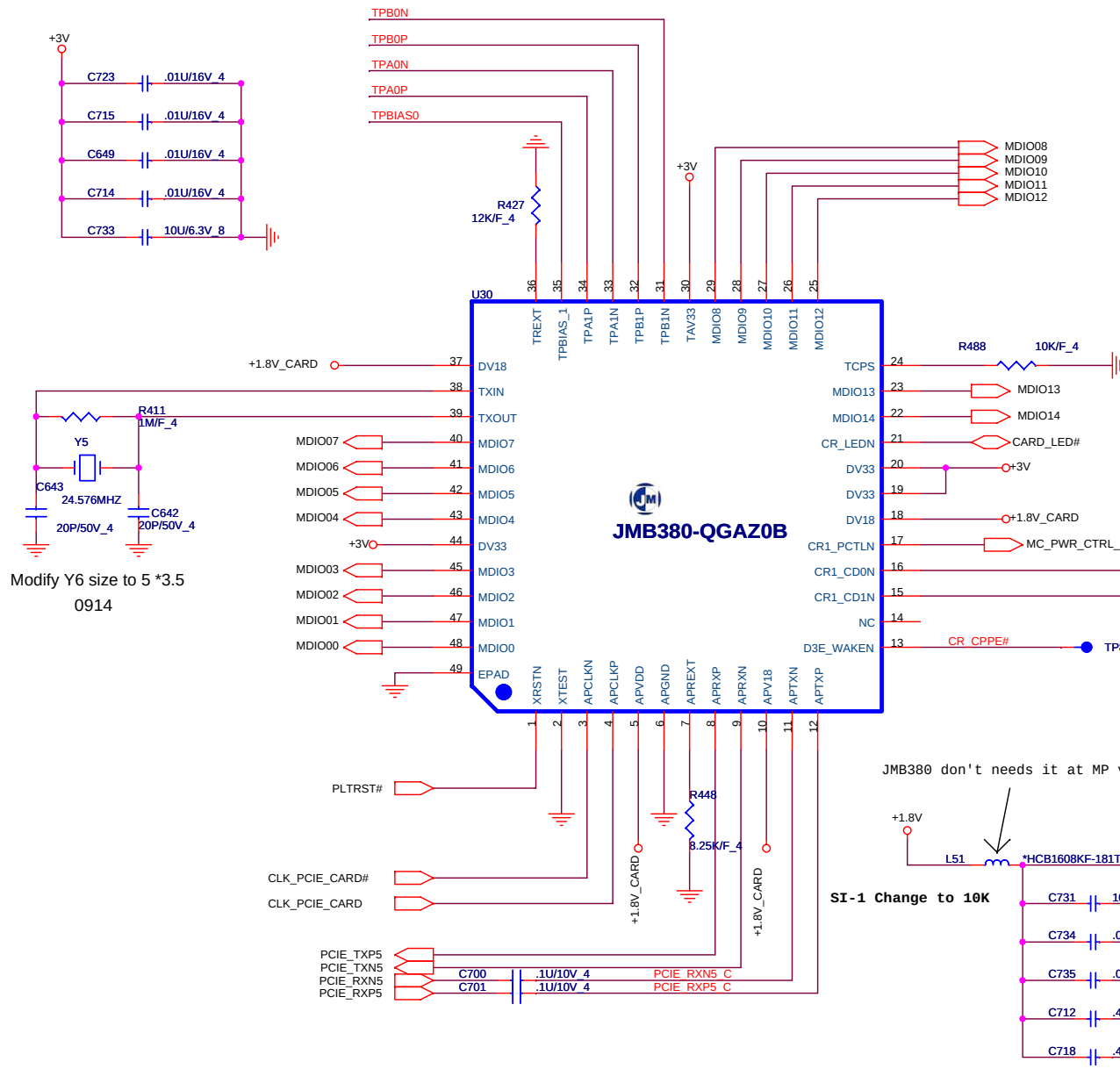
- Board ID 1
- Board ID 2
- Board ID 3
- Board ID 4
- Board ID 5



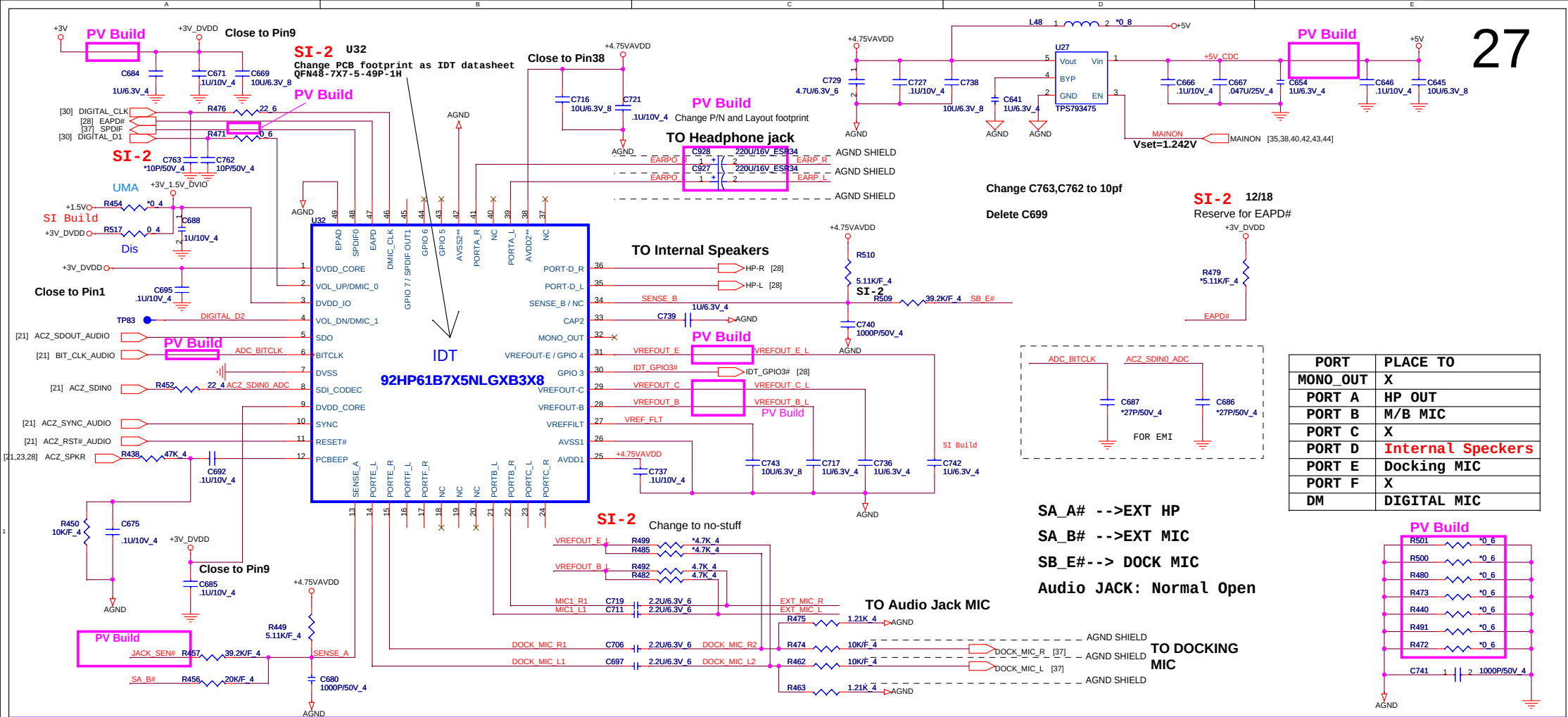
PROJECT : QT6
 Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	ICH9-M GPIO 3/4	
Date: Tuesday, February 26, 2008	Sheet 23 of 44	

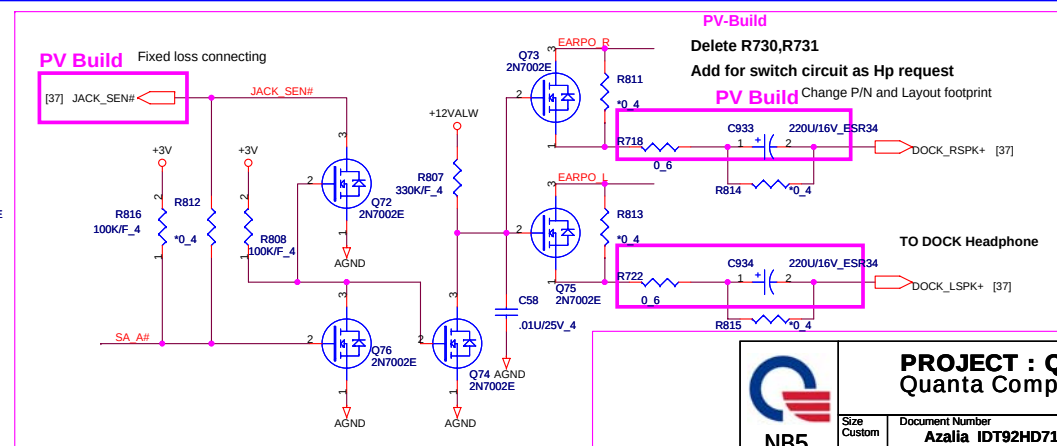
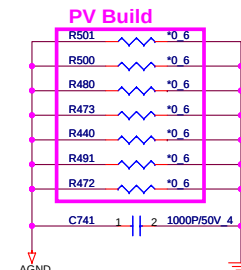




 PROJECT : QT6 Quanta Computer Inc.		
Size B	Document Number	Rev 2B
JMB380 Controller/1394		
Date: Tuesday, February 26, 2008	Sheet 26	of 44



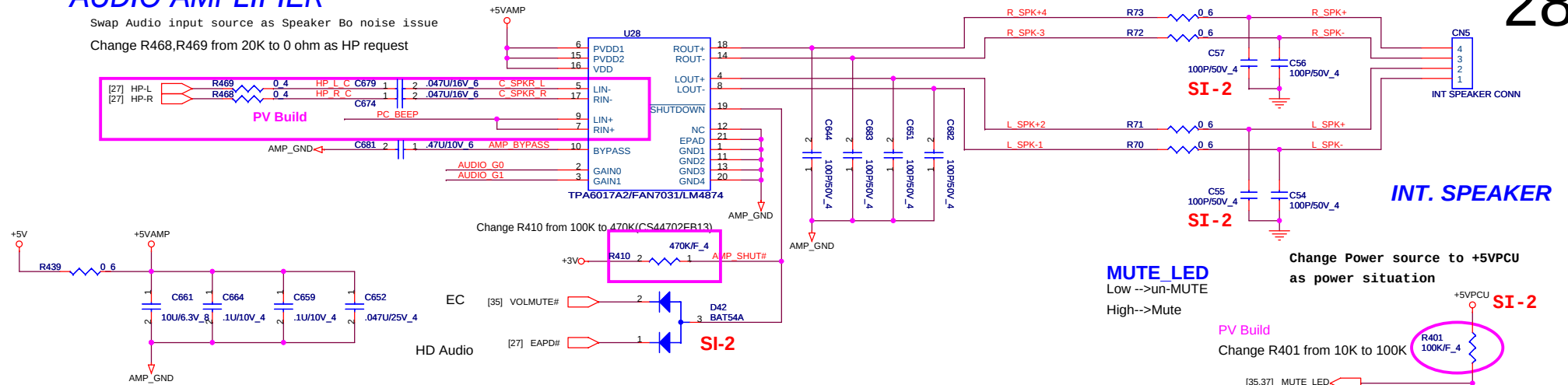
PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speckers
PORT E	Docking MIC
PORT F	X
DM	DIGITAL MIC



AUDIO AMPLIFIER

Swap Audio input source as Speaker Bo noise issue

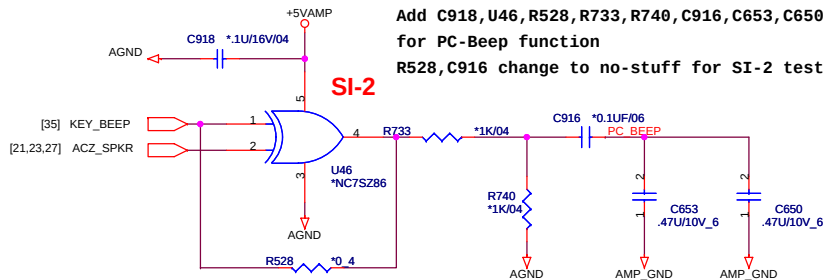
Change R468,R469 from 20K to 0 ohm as HP request



Add in SI-2

**Add C918,U46,R528,R733,R740,C916,C653,C650
for PC-Beep function**

R528,C916 change to no-stuff for SI-2 test -->12/6



6017A2 Gain Table

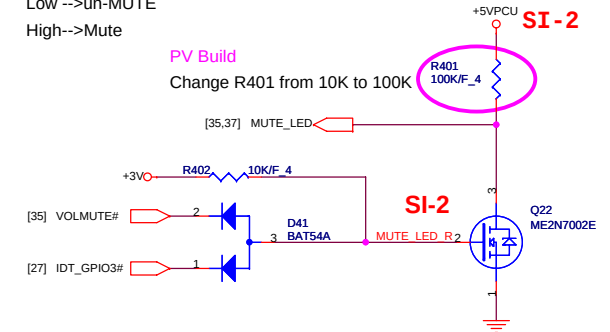
GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

MUTE_LED

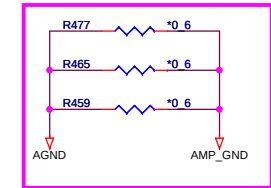
Low --> un-MUTE

High-->Mute

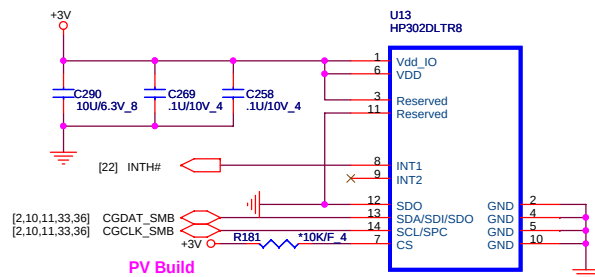
Change Power source to +5VPCU
as power situation



PV Build



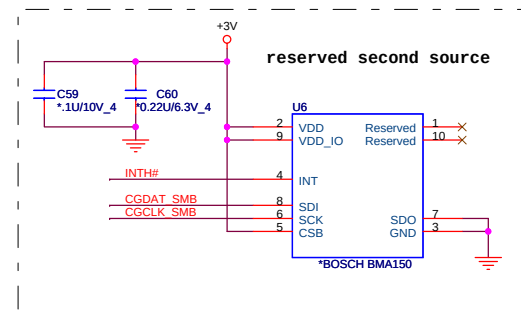
Accelerometer Sensor



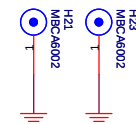
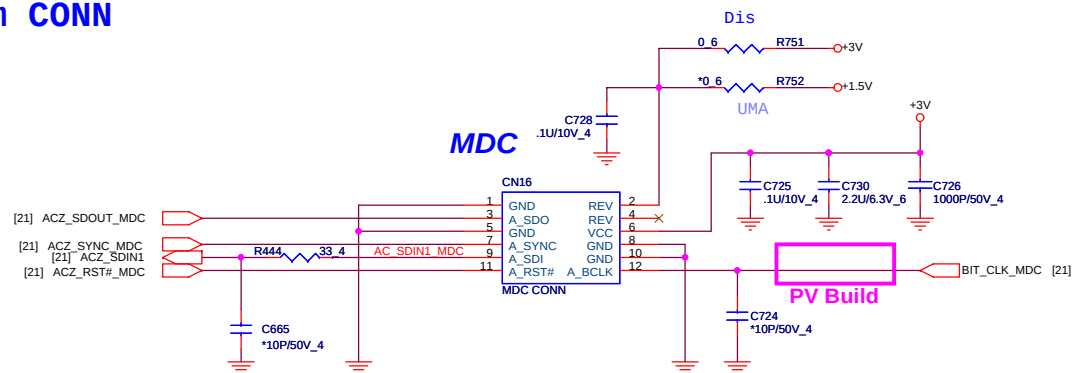
Change R181 to no stuff as internal pull high

Pin 12: Low	38hex
-------------	-------

Pin 12: unconnected/floating 3Ahex

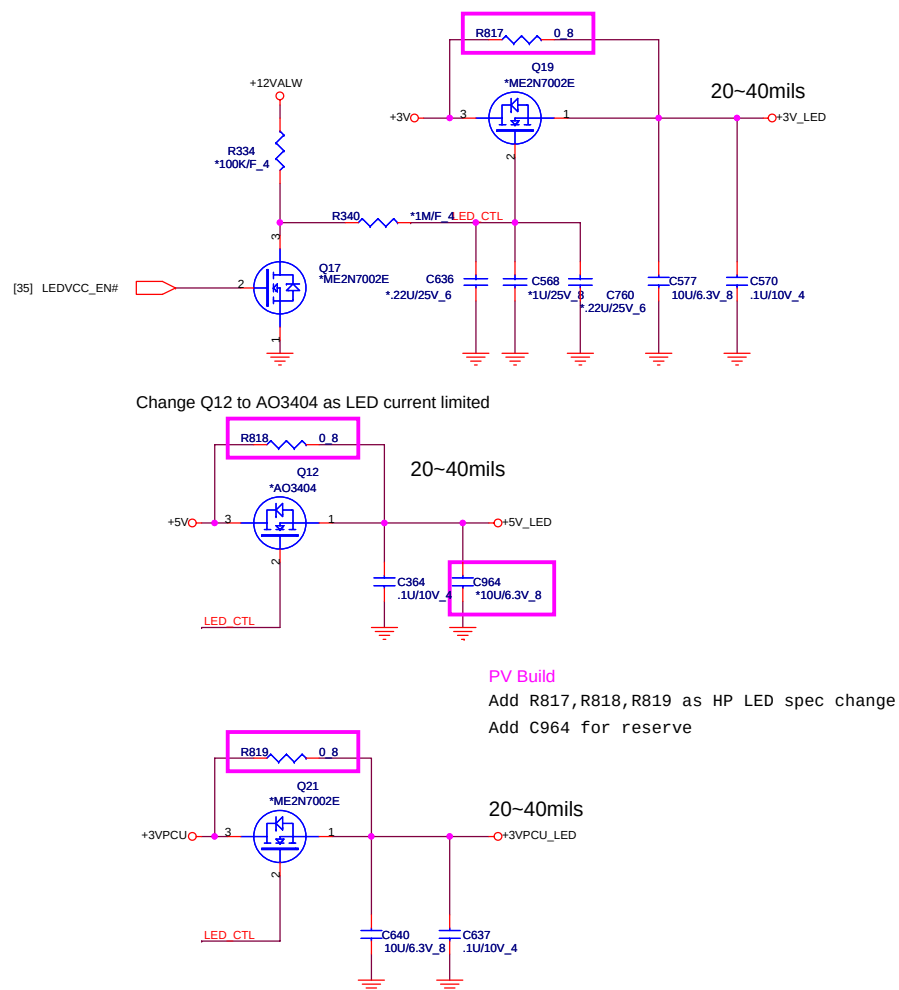


Modem CONN

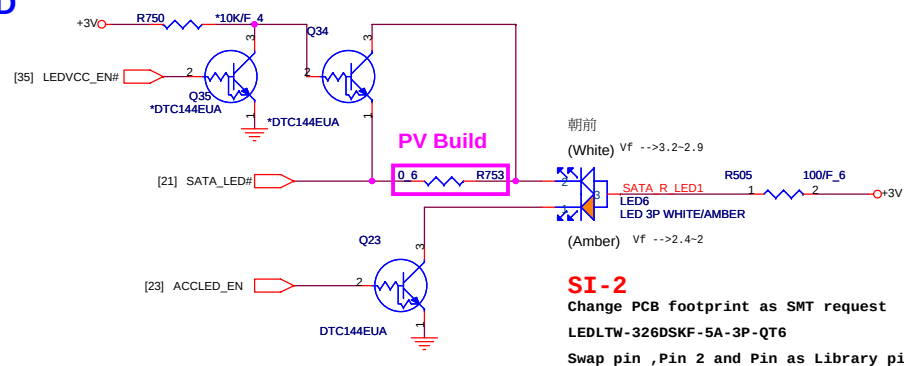


Needs to change Library as ME request

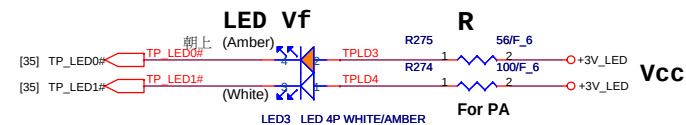
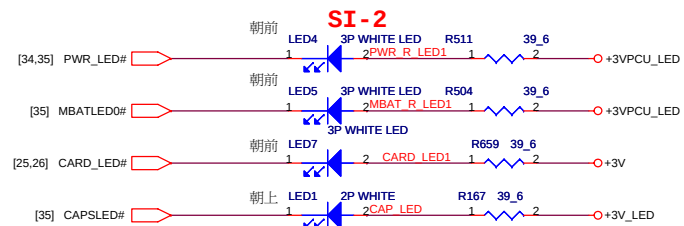
LED PWR CONTROL



LED



Modify LED4,LED5,LED7 layout footprint to ledl-s110kgct-3p-qt6 (11/19)



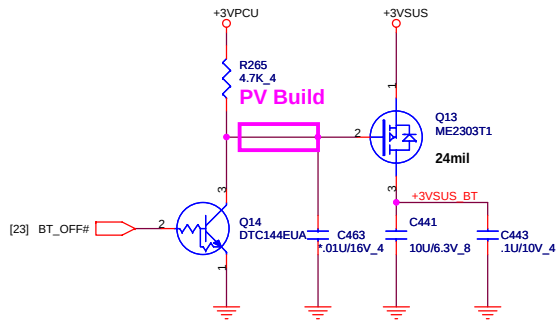
$$I = \frac{V_{cc} - V_f}{R}$$



PROJECT : QT6
Quanta Computer Inc.

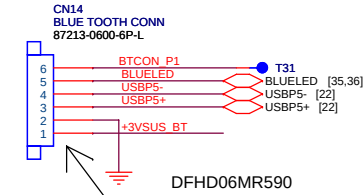
Size	Document Number	Rev
Custom	MDC/LED	3A
Date: Tuesday, February 26, 2008	Sheet 29 of 44	

BLUETOOTH



PV Build

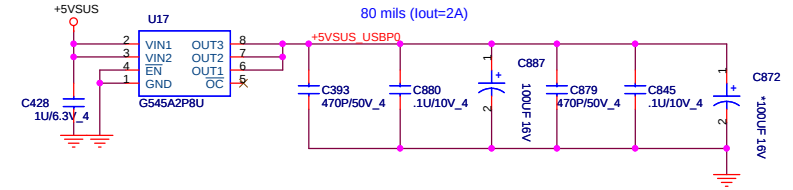
Change CN14 P/N to DFHD06MR590



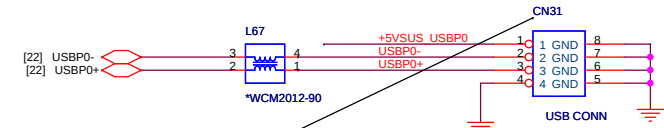
SI-2 CN14 and CN9 87213-0600-6P-L
Change footprint as ME request (pitch 1.25mm to 1.0mm)

LEFT SIDE USBX1 and E-SATA/USB COMBO

30



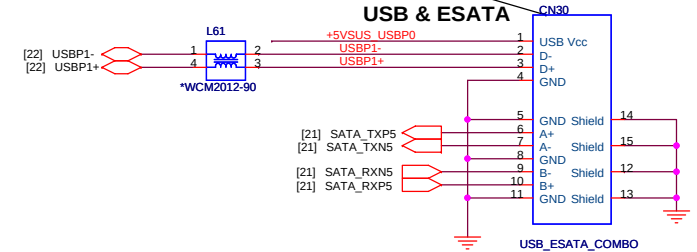
USB 0



SI-2 CN30, CN31 USB-020173MR004S51BZR-4P-R-H

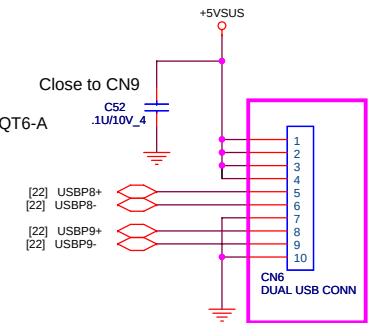
Change Connector layout type from SMD PAD to Dip as SMT request

USB & ESATA



USB-C-2006102-11P-H-QT6

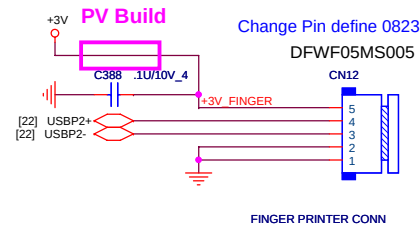
RIGHT SIDE USBX2



PV Build

Change CN6 to BL123-10R-10P-L-QT6-A

USB fingerprint CON

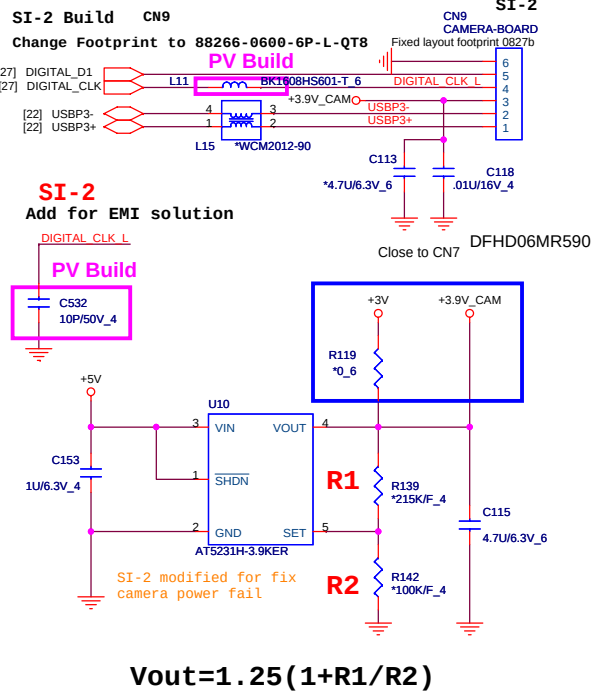


PV Build

Change CN12 to BL123-05R-5P-L-QT6-A

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

USB CAMERA /DIGITAL MIC CONNECT



T : Stuffed for RTL8111C(10/100/1000)

E : Stuffed for 8101E/8102E(10/100)

LANVCC
1.2W
364mA

PV Build

+3VLANVCC

C385
4.7U/6.3V_6

C480
.1U/10V_4

C454
.1U/10V_4

C475
.1U/10V_4

C477
.1U/10V_4

C399
.1U/10V_4

these CAP are for LAN CHIP LANVCC
pins--16, 37, 46 and 53.placement close lan
chip

PV Build

+3V_A_LAN

C401
.1U/10V_4

C434
.1U/10V_4

these CAP are for LAN CHIP LAN_A3.3
pins-- 2 and 59.placement close lan chip

8111C CV-4706MN00
8102E CS00004JA40

For Giga must change L65 to Inductor (Chipset include switch power)

+CTRL18 will become to switch power phase

**L54 for Giga lan use 4.7uH power choke
A>500mA tolerance ±15%**

placement close to lan chipset

SI Build

+CTRL18

L65
4.7UH_2016

+FB12 [31]

L63
0.8

C931
10U/6.3V_8
SI build

C930
10U/6.3V_8
SI build

C881
4.7U/6.3V_6

C876
4.7U/6.3V_6

C878
.1U/10V_4

C891
.1U/10V_4

C892
.1U/10V_4

C875
.1U/10V_4

C893
.1U/10V_4

these cap are for lan
chip LAN_A1.8
pins--5, 8, 11 and 14.
placement close chip

STUFF 100 ohm BEAD
R250 0.8

+LAN_E1.8

C421
.1U/10V_4

C422
1U/6.3V_4

these cap are for lan chip
LAN_D1.8 pins, such as 22 and 28.
placement close lan chip

SI-2

Remove R250, L63, L66 -->For 8102E

L66
0.8

Only For 8111C application

Power trace Layout 寬度> 30mil

PV Build

C422 change to 1uf

+LAN_D1.5

C474
.1U/10V_4

C479
.1U/10V_4

C459
.1U/10V_4

C456
.1U/10V_4

C472
.1U/10V_4

C461
.1U/10V_4

C476
.1U/10V_4

C415
.1U/10V_4

C478
.1U/10V_4

C400
1U/10V_4

these cap are for lan chip LAN_D1.5 pins-- 15,
21, 32, 33, 38, 41, 43, 49, 52 and 58.placement
close lan chip

Power domain chart

	RTL8111C(P) RTL8102E
LANVCC	3.3V
LAN_D1.8	1.2V
LAN_A1.8	1.2V
LAN_D1.5	1.2V



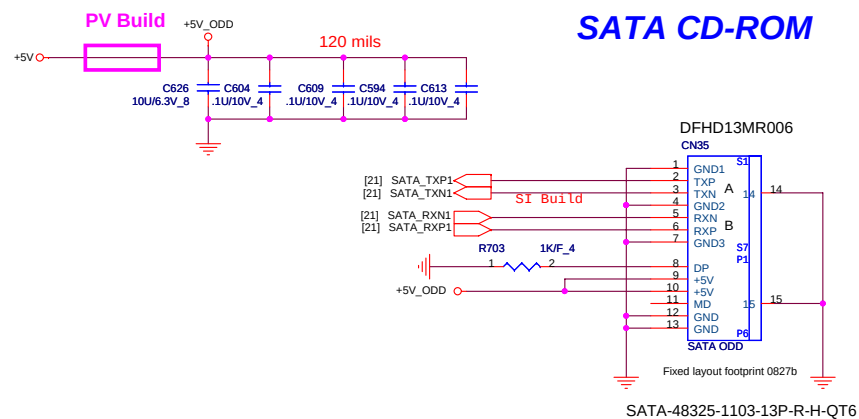
PROJECT : QT6
Quanta Computer Inc.

Size
A3

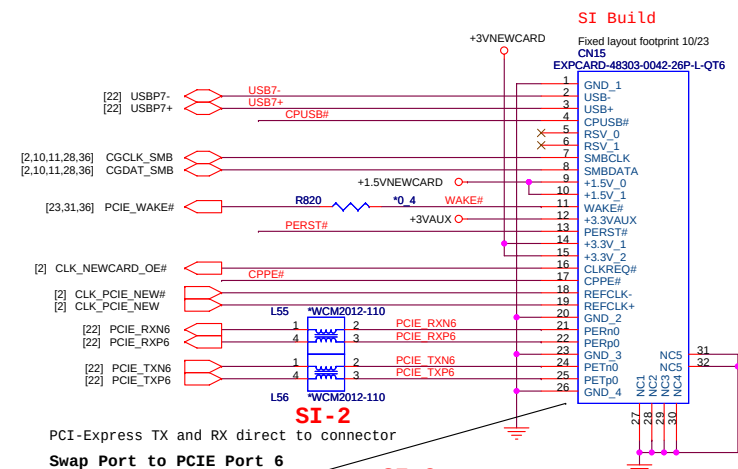
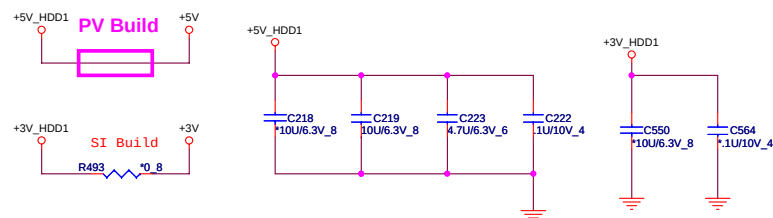
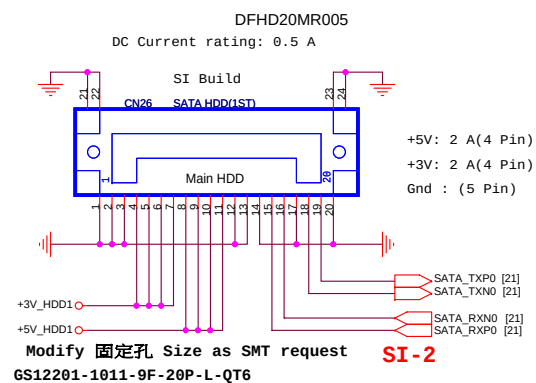
Document Number
LAN Power

Rev
1A

Date: Tuesday, February 26, 2008 Sheet 32 of 44

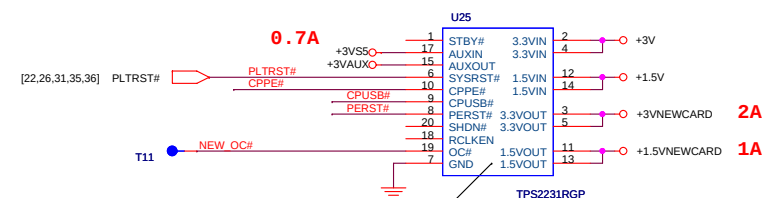


SATA HDD CONNECTOR

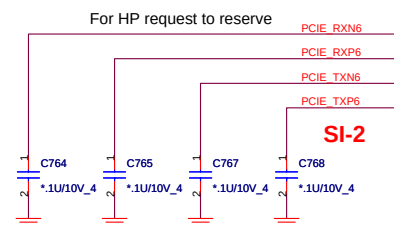
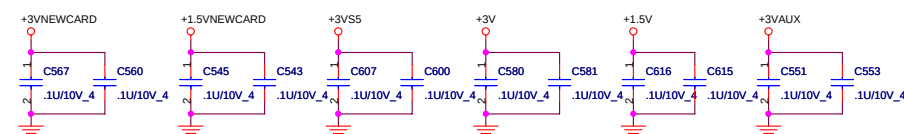


PCI-Express TX and RX direct to connector
Swap Port to PCIE Port 6

Change CN15#31,32 as ME request for Hole pad
expcard-48303-0042-26p-l-qt6 as ME modify Pad size(pin31,32)
Move CN15#29,30 Pin as ME request(Molex confirm drawing)



SI-2 add Pin 21~25 as U25 Thermal pad tied to Gnd

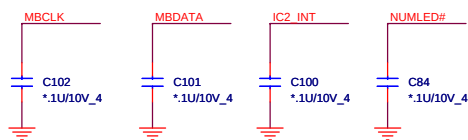


PROJECT : QT6
Quanta Computer Inc.

Size Custom	Document Number ODD/HDD/NEW CARD	Rev 2B
Date: Tuesday, February 26, 2008		Sheet 33 of 44



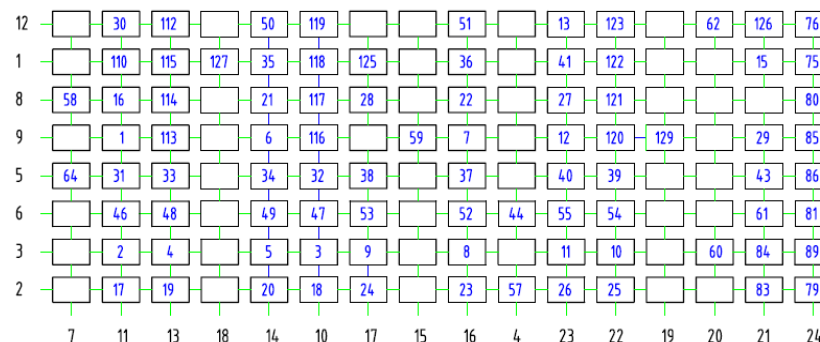
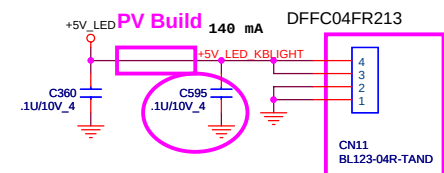
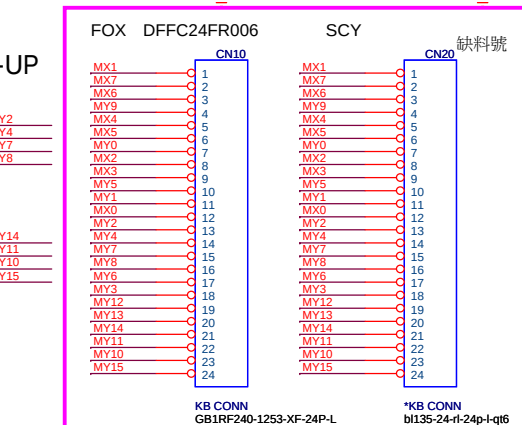
CAP SW CONNECT



Add C595 and close to CN11

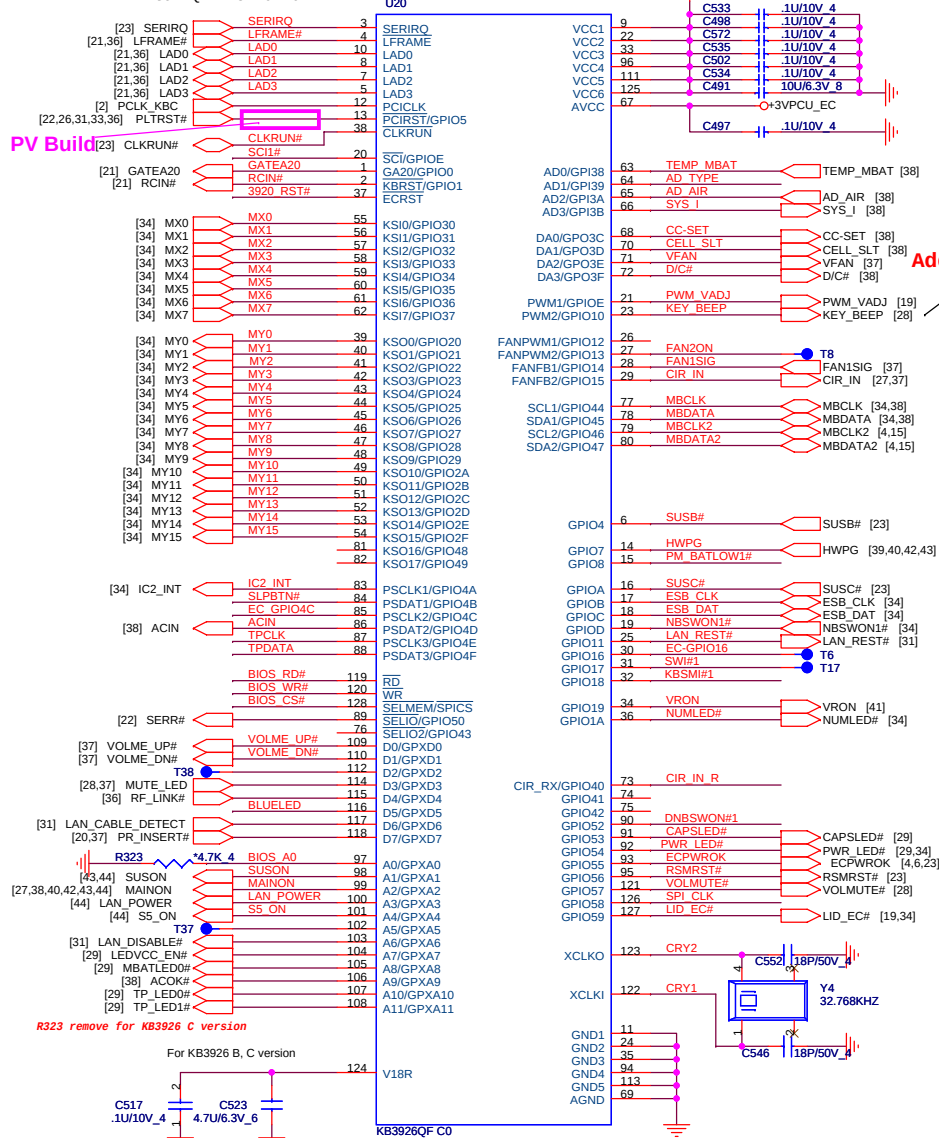
Change CN11 to BL123-04R-4P-L-OT6-A

Change CN10 to GB1RF240-1253-XF-24P-L as Foxconn drawing



Change U20 layout footprint to LQFP128-16X16-4-AA1

SI-2

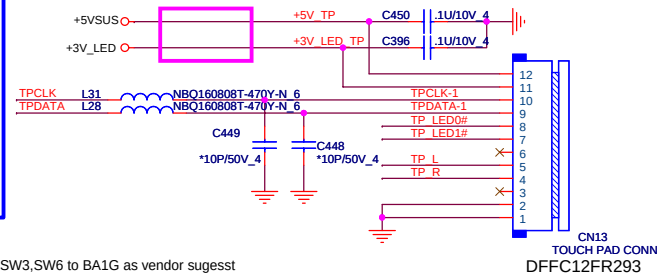


Add in SI-2

TOUCH PAD CONNECTOR

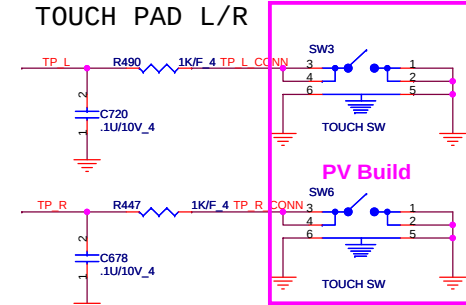
PV Build

25 mils

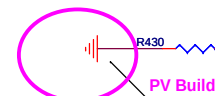
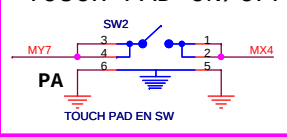


TOUCH PAD L/R

Change to SW2,SW3,SW6 to BA1G as vendor sugges



TOUCH PAD ON/OFF



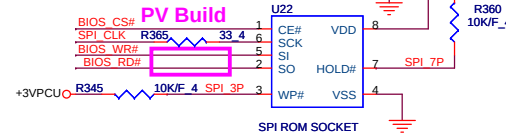
SI-2

Add R430 and tied to U20 Pin 115 and change Q18 footprint to S0T23
Delete Q18 and tied to U20#116 direction

Socket: DG008000031

MXIC AKE5GFK0Z09
WINBOND AKE3GFP0N08
PME AKE3GZP0500
EON AKE3GZP0Q00
AIT AKE3GZP0801

1M byte
SPI
BIOS

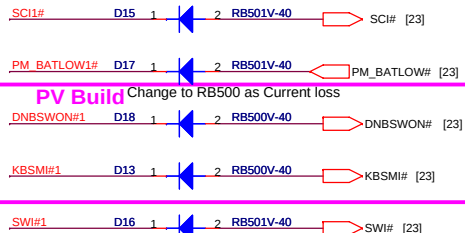


SI-2

Change Layout footprint to X6179-10XXX-8P-SOCKET(Socket)

SI-2

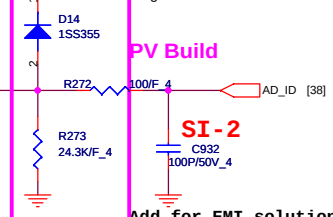
Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier
Add T37,T38,T39 for EC
Delete T10 and tie pin 117 from Lan for DSM



R273

64.9K -->65W CS36492FB17
33.2K -->90W CS33322FB13

Change to 1SS355 as Current loss



PV Build

Change to RB500 as Current loss

DNBSWON# [23]

KBSMI# [23]

SWI# [23]

SI-2

Add for Power request

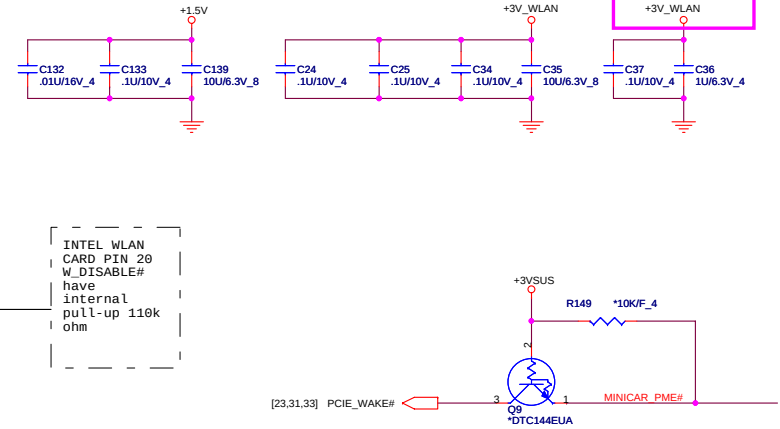
Add for EMI solution



PROJECT : QT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB3926/ROM/TP	3A
Date: Tuesday, February 26, 2008	Sheet 35 of 44	

36



Mini PCI-E Blue 3 TV Tuner

Change Library to MINICPE-P04-F3584-178-52P-QT6 12/18

Si-2 DG052000005

CN37

MINICPE H=7.0

3V_TVC

+1.5V

3V

WLAN -- have 2.8A 7W power consumption
power pin 24,39,41
GND pin 37,43
need to be careful power rail

USB11+ [22]
USB11- [22]

CGDAT SMB
CGCLK SMB

R719 0.6
R720 0.6

+3V
+3V5US

TV tuner card

	Peak	Normal
+3.3Vaux:	2750mA	1100mA
+1.5V:	500mA	375mA

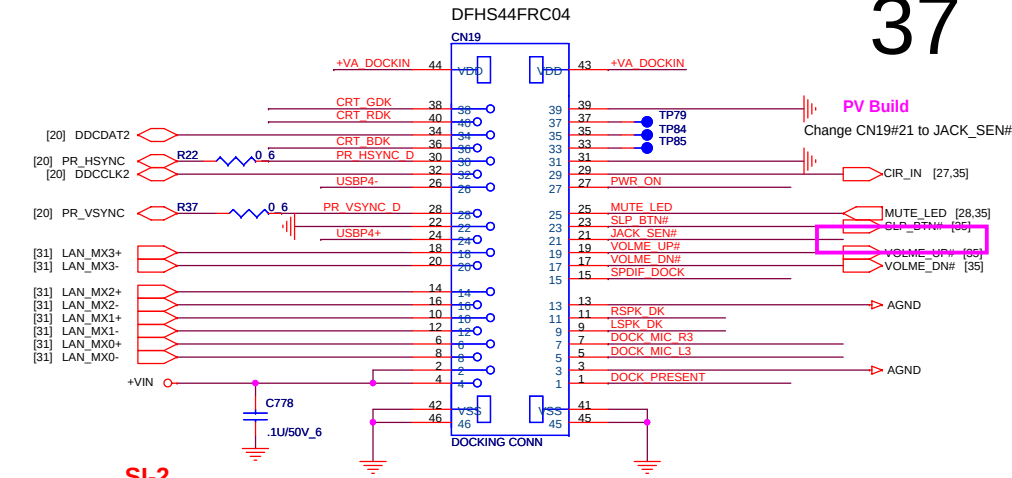
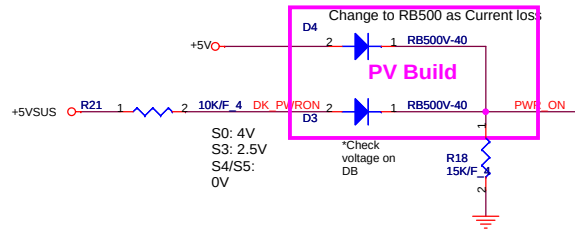
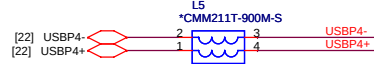
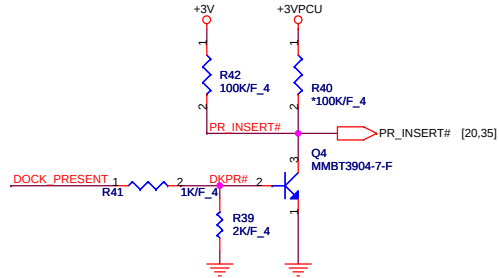
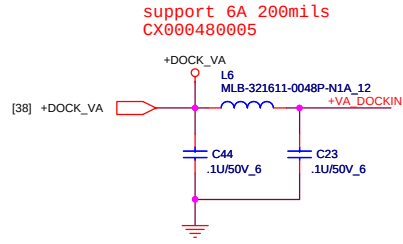
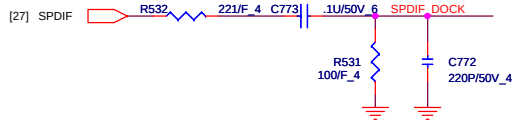
PROJECT : QT6
Quanta Computer Inc.

Size Custom
Document Number
MINI PCIE CONN X2 & HOLE

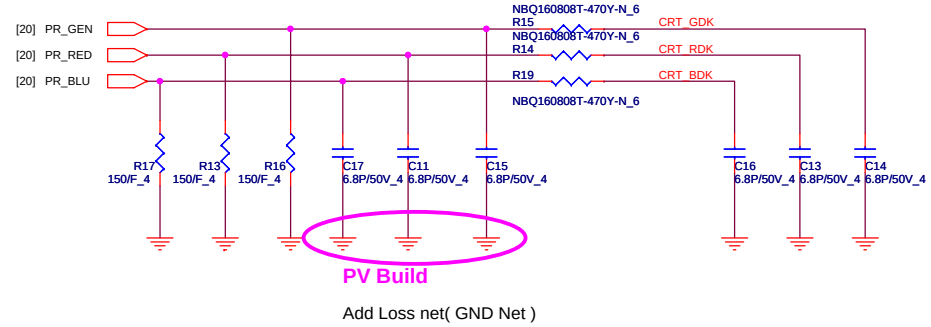
 NB5	PROJECT : QT6 Quanta Computer Inc.		
	Size Custom	Document Number MINI PCIE CONN X2 & HOLE	Rev 2B
Date: Tuesday, February 26, 2008		Sheet 36 of 44	

CABLE DOCK

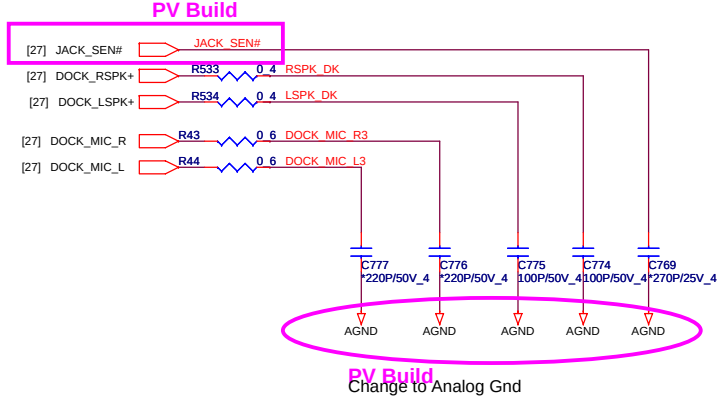
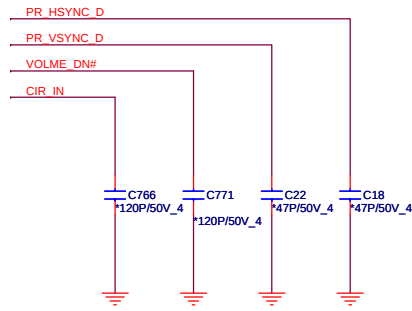
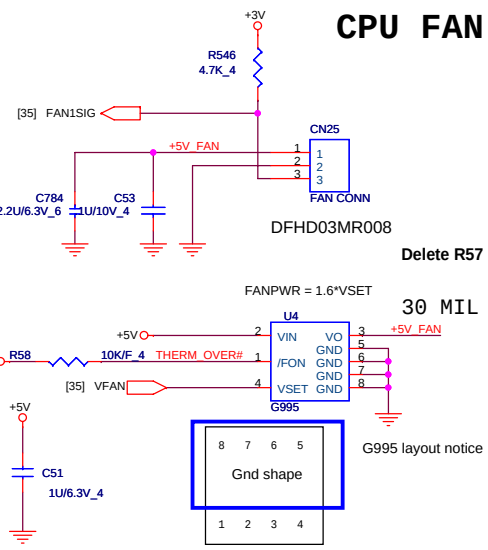
37

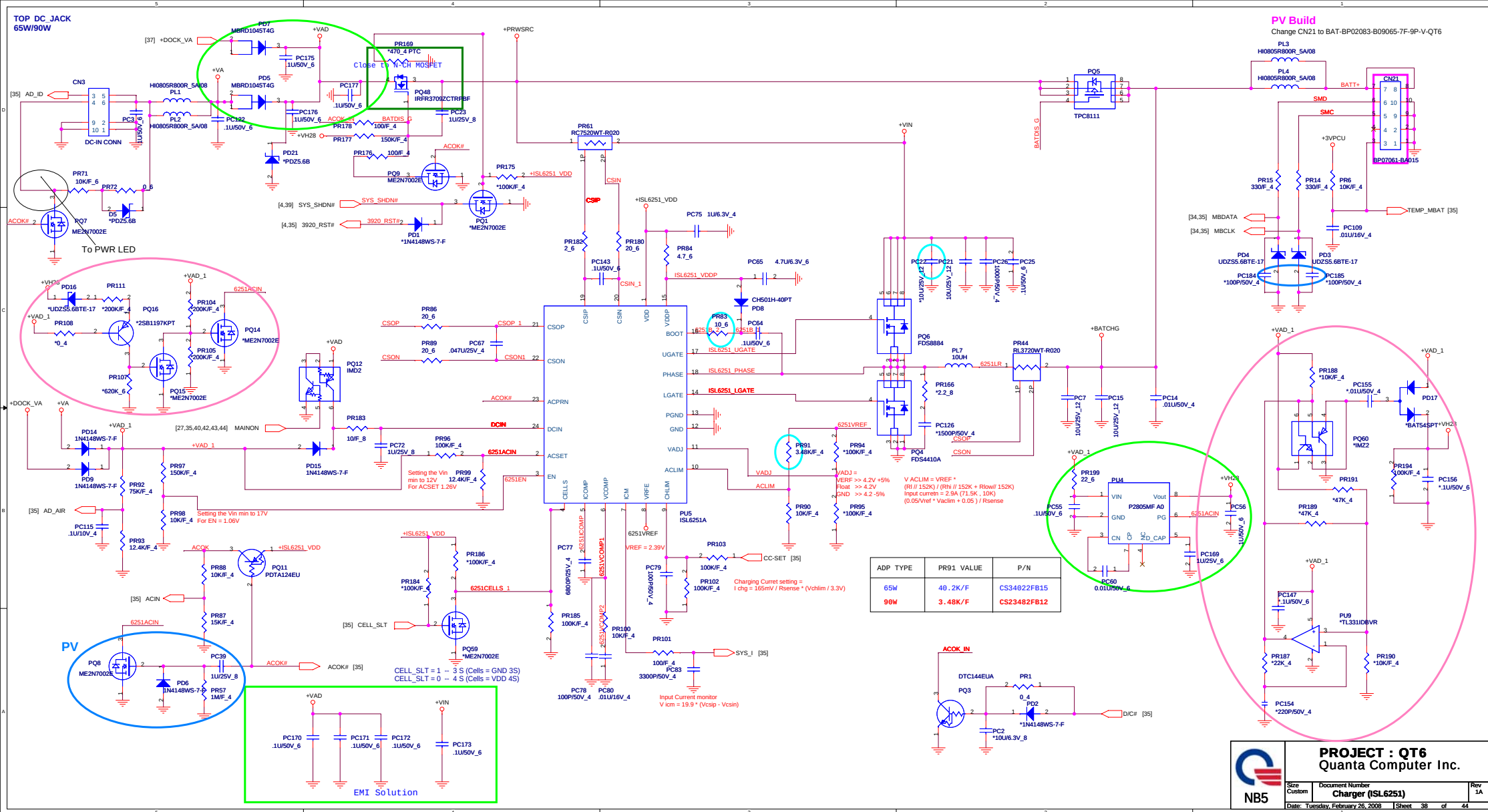


SI-2
R13,R16,R17 Change to install



CPU FAN

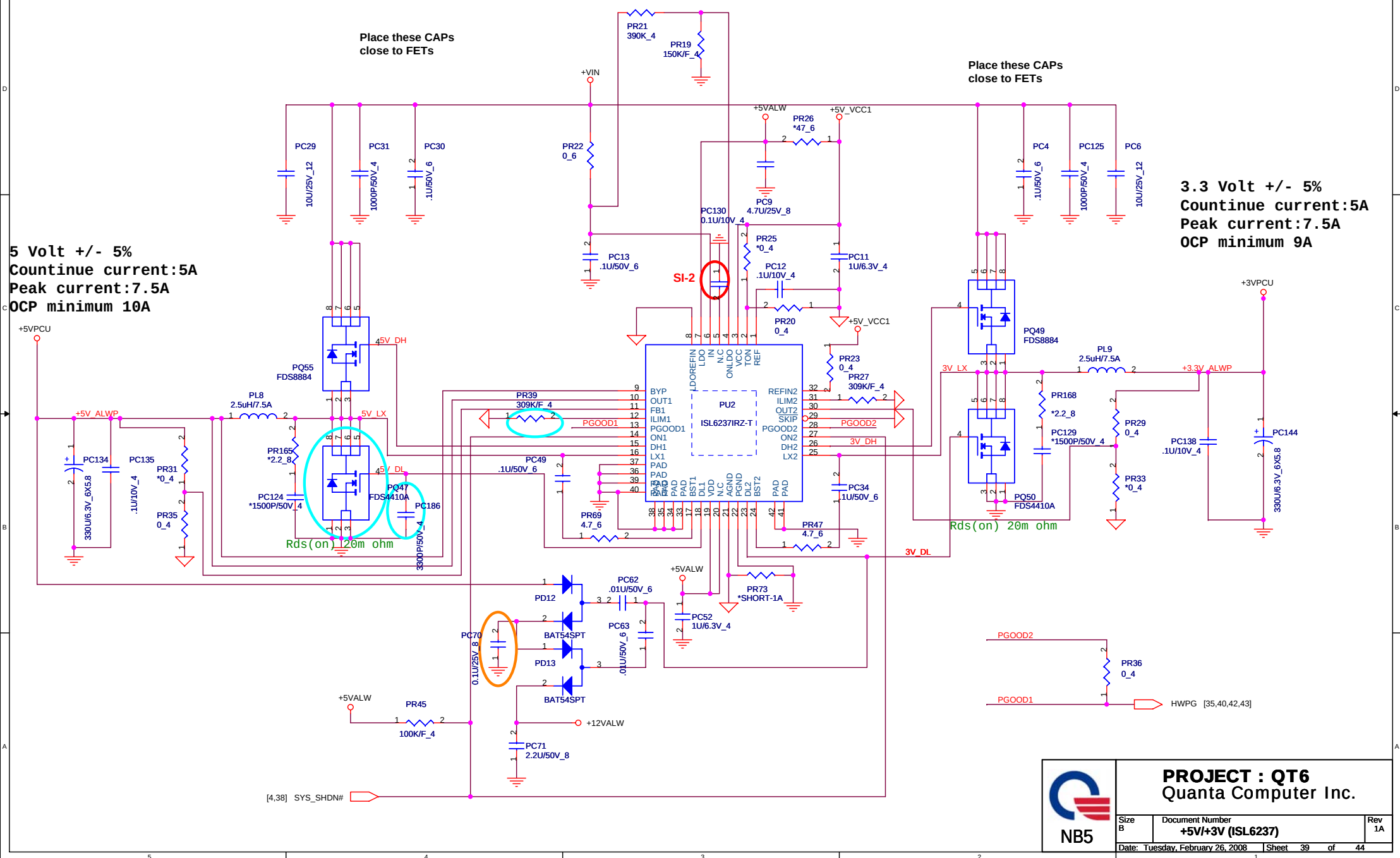




DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

5 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCp minimum 10A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCp minimum 9A



PROJECT : QT6
Quanta Computer Inc.

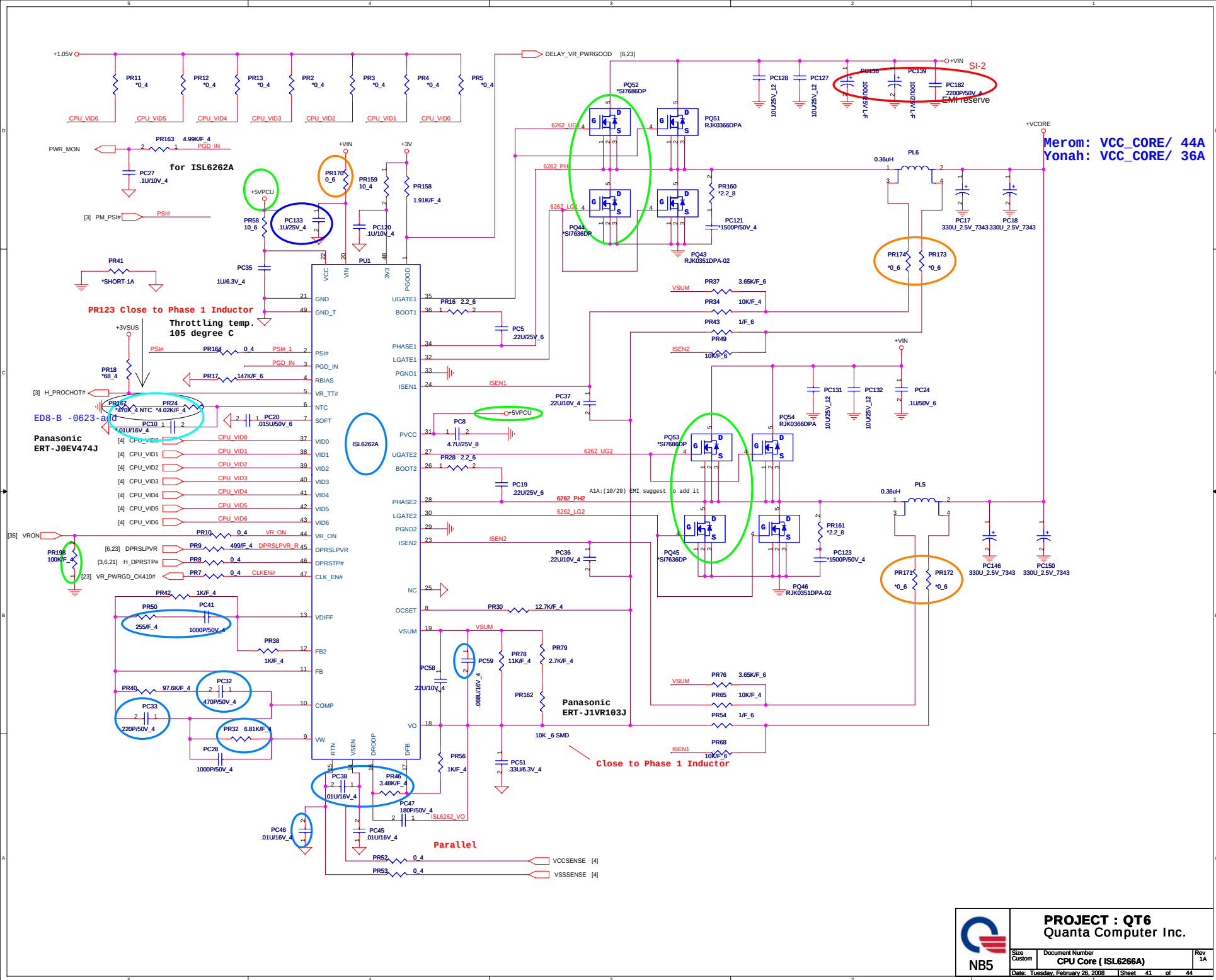
Size	Document Number	Rev
B	+5V/+3V (ISL6237)	1A
Date: Tuesday, February 26, 2008 Sheet 39 of 44		

+1.05Volt +/- 5%
Continue current:7.5A
Peak current:10A
OCP minimum 15A

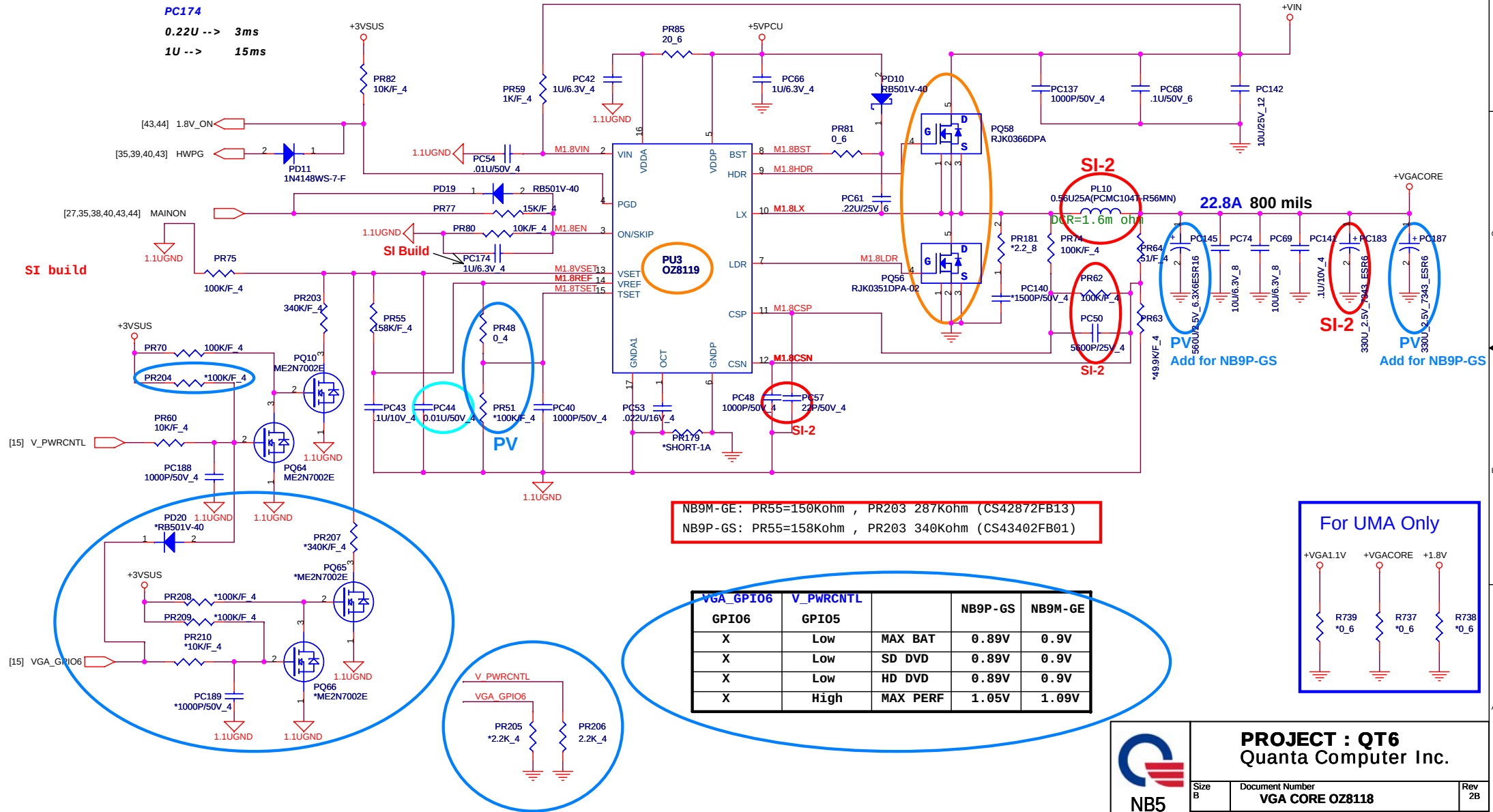


NB5

Size B	Document Number +1.05V/+1.5V (RT8204)	Rev 1A
Date: Tuesday, February 26, 2008		Sheet 40 of 44



+1.1Volt +/- 5%
Countinue current:17.54A
Peak current:22.8A
OCP minimum 23A



VGA_GPIO6	V_PWRCNTL		NB9P-GS	NB9M-GS
GPI06	GPI05			
X	Low	MAX BAT	0.89V	0.9V
X	Low	SD DVD	0.89V	0.9V
X	Low	HD DVD	0.89V	0.9V
X	High	MAX PERF	1.05V	1.09V

