

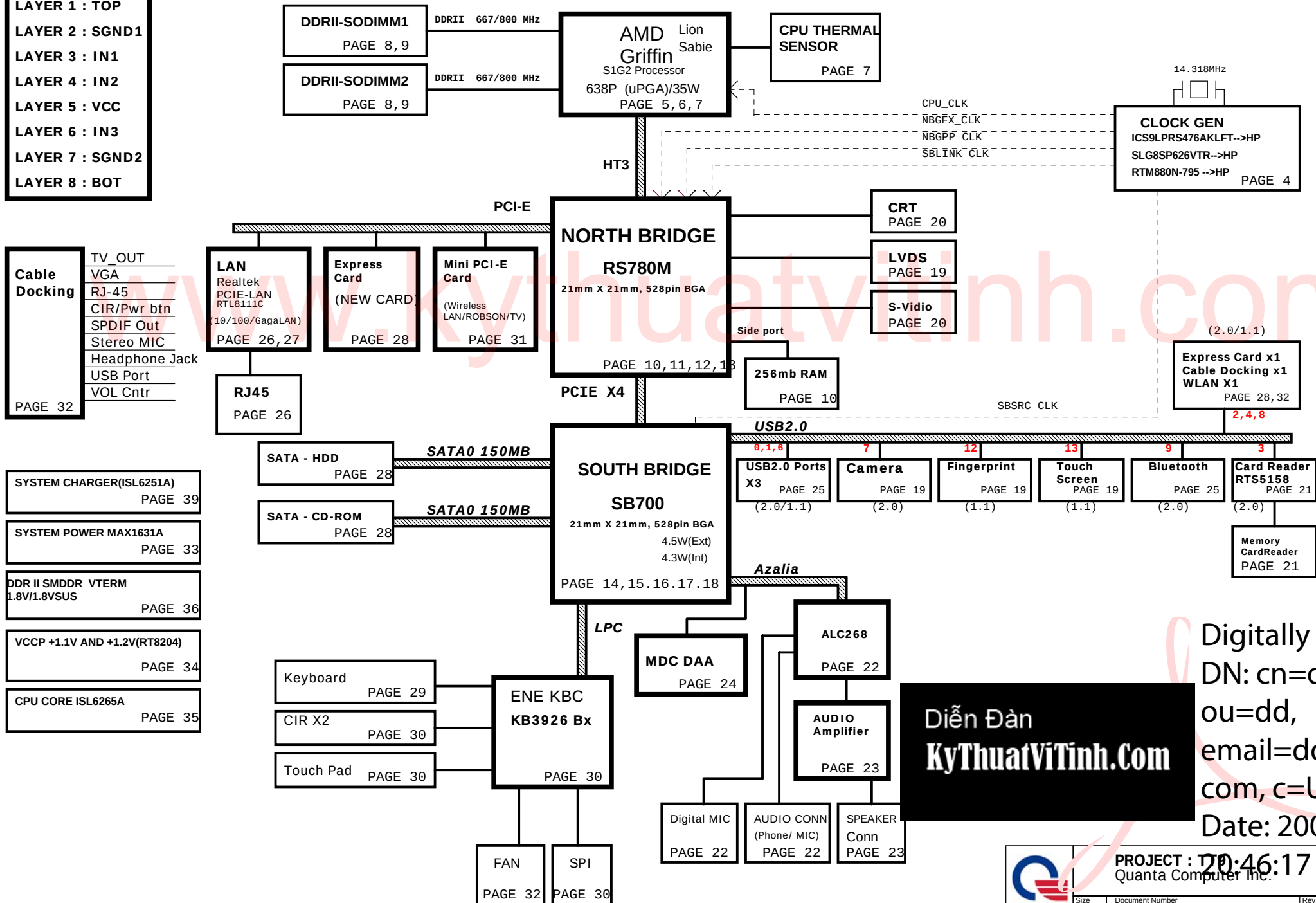
PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

Soyuz 2.0 SYSTEM DIAGRAM



01



INDEX

Pg#	Description	NOTE
1	Schematic Block Diagram	
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4	CLOCL GENERATOR	
5-7	AMD CPU S1G2 Griffin	
8-9	DDR II SO-DIMM	
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14-18	SB700	
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20	20--CRT,TV_OUT	
21	RTS5158E & CR SOCKET	
22	Azalia ALC268	
23	JACK/AMP_TPA0312	
24	Si3080 and MDC1.5 Connector	
25	Blue Tooth / USBX3 / TPM	
26	RTL8111C/RJ45	
27	LAN Power	
28	NEW CARD/SATA ODD/SATA HDD	
29	LED/KEYBOARD/SW	
30	KB3926/ROM/TP	
31	Mini CARD/Hole	
32	CABLE DOCKING/FAN	
33	3V/5V(MAX1631A)	
34	+1.2V/+1.1V (RT8204)	
35	+CPU_CORE ISL6265	
36	+1.8VSUS/+1.8V/+2.5V	
37	+1.1V/+1.2V_S5/+1.5V	
38	DISCHARGE	
39	Charger (ISL6251)	

*--> Un-stuff (ex. *1K/04)
04-- 0402 footprint
06-- 0603 footprint
08-- 0805 footprint
12-- 1206 footprint
F-- 1% tolerance

Power & Ground

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (18.5V)	
+BATT	S0, S3, S4, S5	MAIN BATTERY + (6.2V-8.4V)	
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3.3V)	
+12VALW	S0, S3, S4, S5	+12V	
+VCORE	S0	CPU CORE POWER (0.375-1.5V)	VRON
+CPUVDDNB	S0	CPU CORE POWER (1.375-1.5V)	VRON
+1.1V_NB	S0	+1.1 to +1.0 DYN	VRON
+1.1V	S0	+1.1V	VRON
+1.2VS5	S0, S3, S4, S5		S5_ON
+1.2V	S0	+1.2V	VRON
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+5V	S0		MAIND
+5VSUS	S0, S3		SUSON
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+1.5V	S0		MAIND
+1.8VSUS	S0, S3	DDR CORE POWER	SUSON
+1.8V	S0		MAINON
+2.5V	S0	CPU VDDA	VR2.5_ON
+0.9VSMVTT	S0	DDR COMMAND & CONTROL PULL UP POWER	MAINON
+0.9VSMVREF_DIMM	S0, S3	DDR REF POWER	SUSON
+AVDD	S0	AUDIO ANALOG POWER (5V)	MAINON
+3VLAVCC	S0, S3, S4, S5	LAN Power	LAN_ON
 GND	ALL PAGES	DIGITAL GROUND	
 AGND		AUDIO GND	

SMBUS	SMBUS function define
SMBCLK0 SMBDAT0	DDR / DDR THER / CLOCK GEN (+3V)
SMBCLK1 SMBDAT1	Mini Card (+3VS5)
SMBCLK2 SMBDAT2	New CARD (+3VS5)

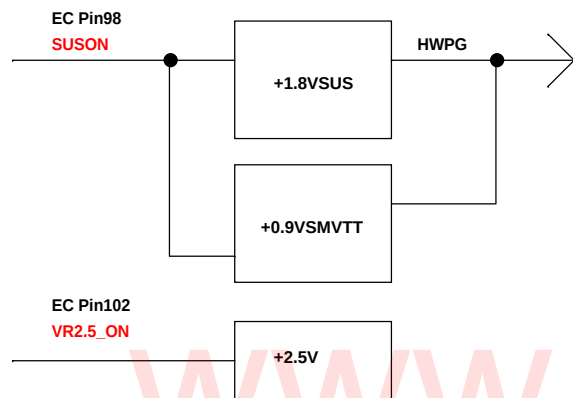


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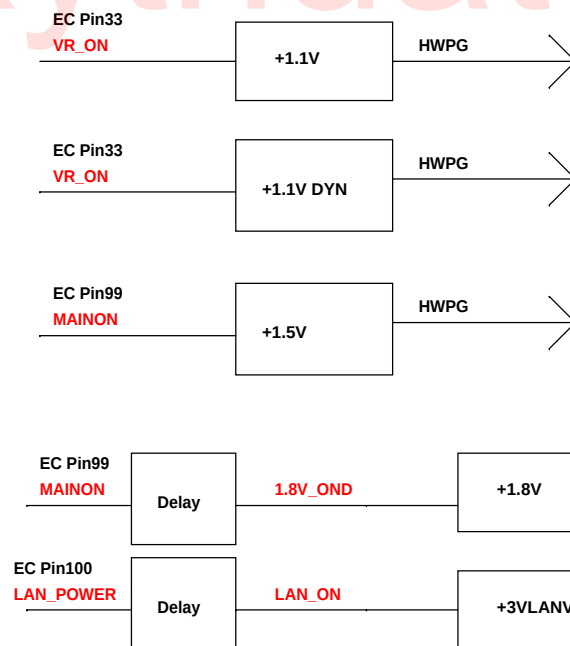
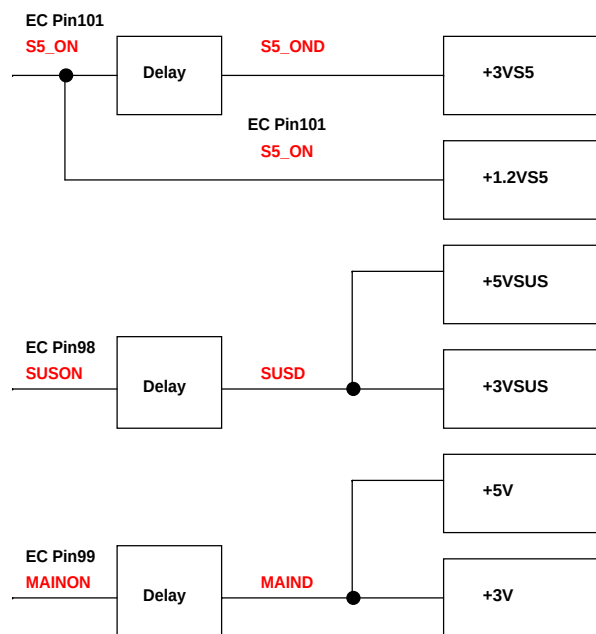
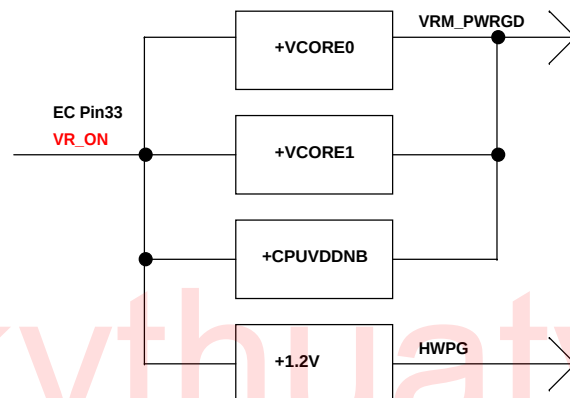
Size Custom	Document Number System Information	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 2 of 41		

02

CPU Power Group A



CPU Power Group B



3VPCU/5VPCU

NBSWON1#

DNBSWON#

S5_ON

RSMRST#

SUSC

SUSB

SUSON

MAINON

VR_ON

VR2.5_ON

HWPG

VRM_PWRGD

ECPWROK

NB_PWRGD_IN

SB_PWRGD_IN

CPU CLK IN

CPU RESET

CPU POWER OK

CPU_LDTSTOP#



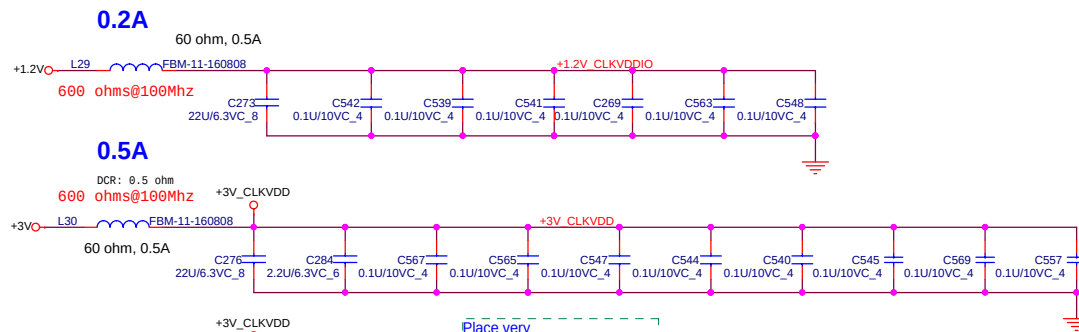
PROJECT : TT9
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Size
Custom

Document Number
Power control

Rev
1A

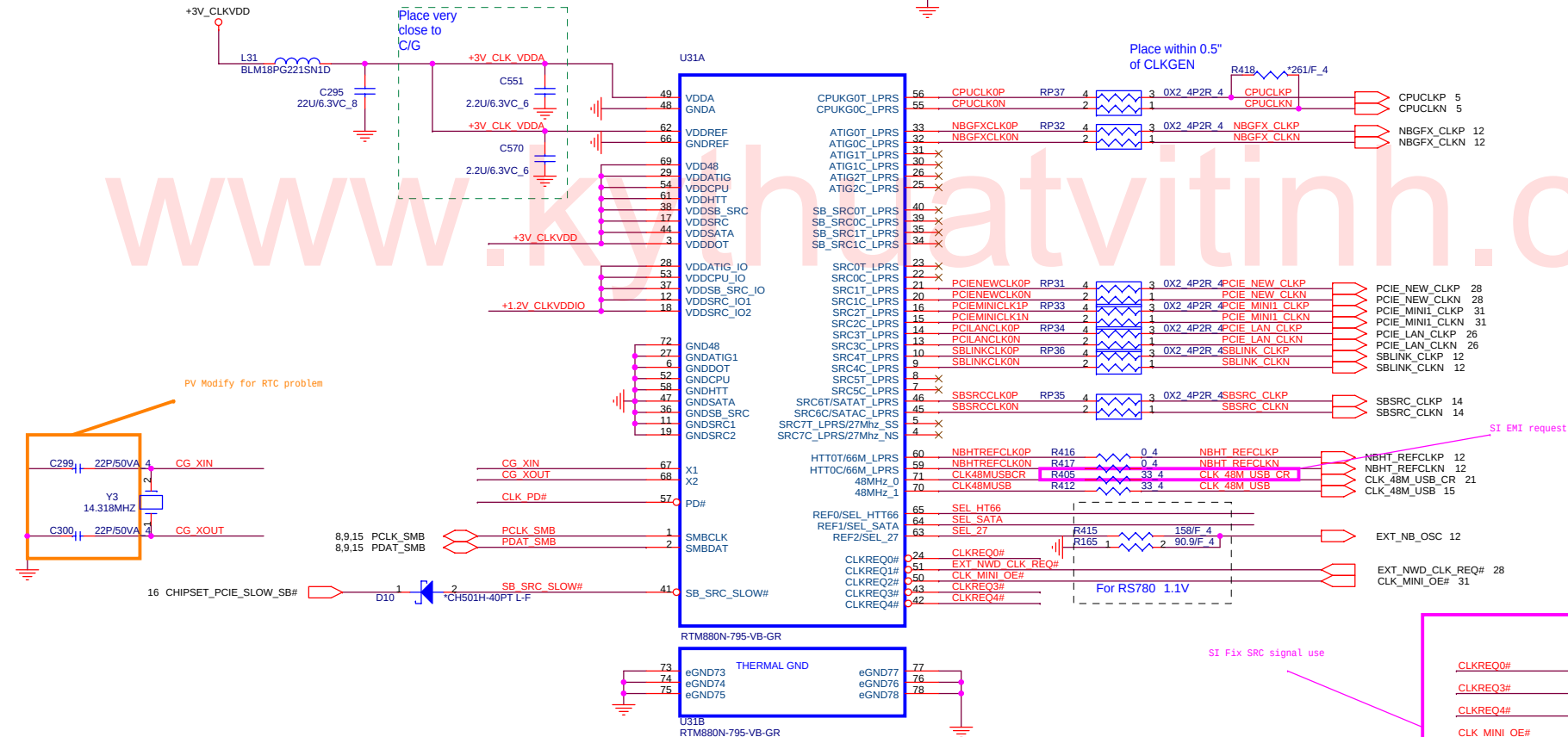
Date: Wednesday, January 23, 2008 Sheet 3 of 41



NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	vref DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

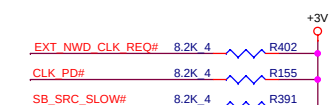
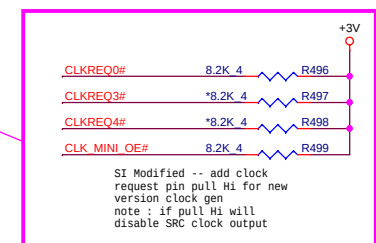
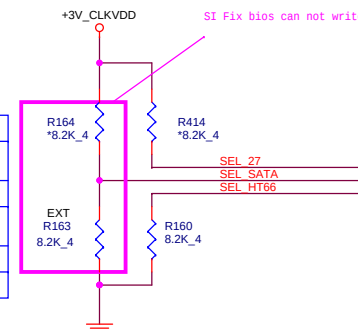
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



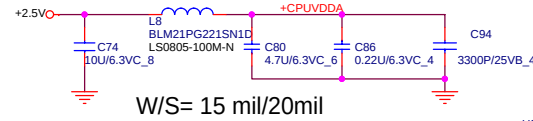
when driven low SB_SRC clocks slow only supported with
to reduced setpoint custom CG IC

* RS780 can be used as clock buffer to output two PCIE reference clocks. By default, chip will configured as input mode, BIOS can program it to output mode.

* default		
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

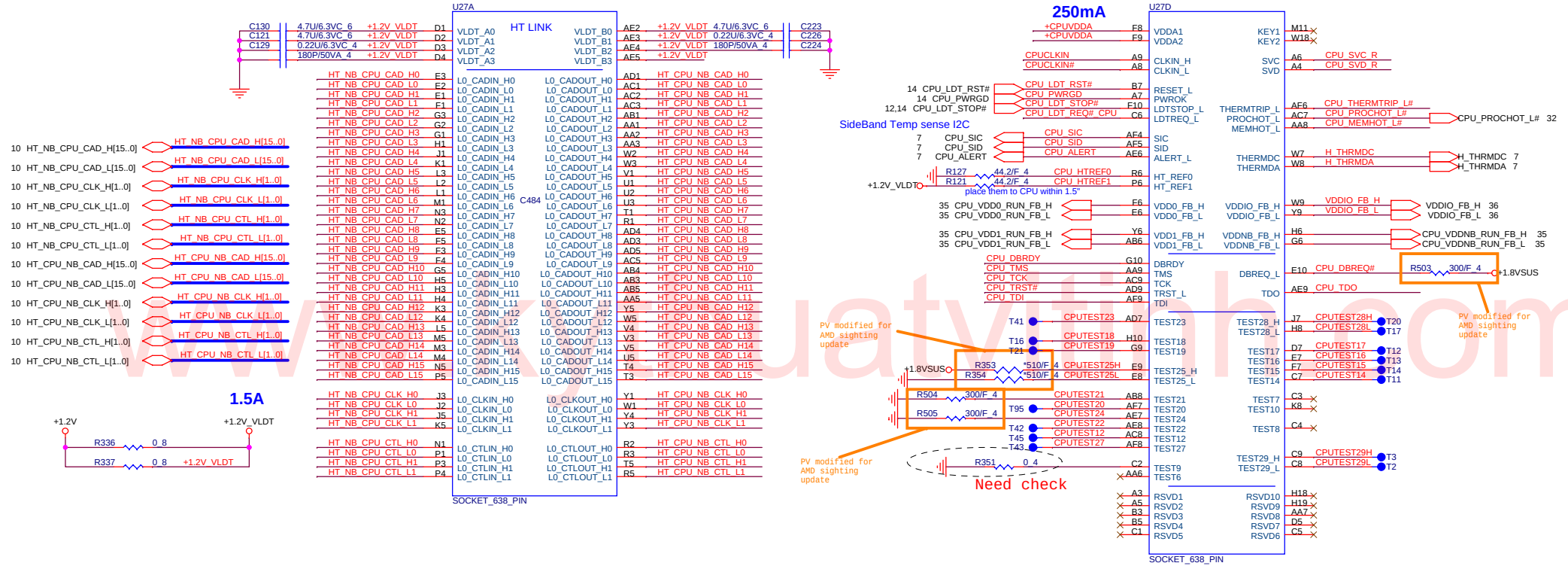


+1.2V 4,13,14,16,17,34,37
 +1.8V 10,12,13,14,15,18,36,38
 +1.8VSUS 6,7,8,9,31,35,36,37
 +2.5V 37
 +3V 4,7,8,9,12,13,14,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38

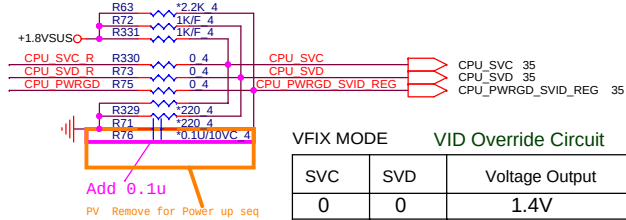


W/S= 15 mil/20mil

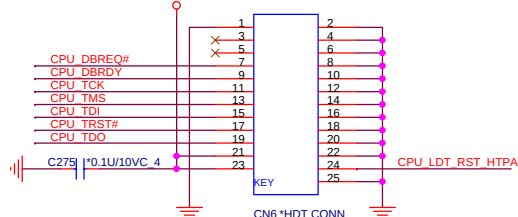
250mA



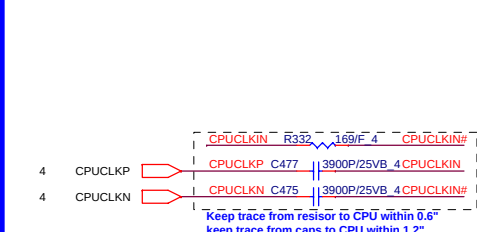
Serial VID



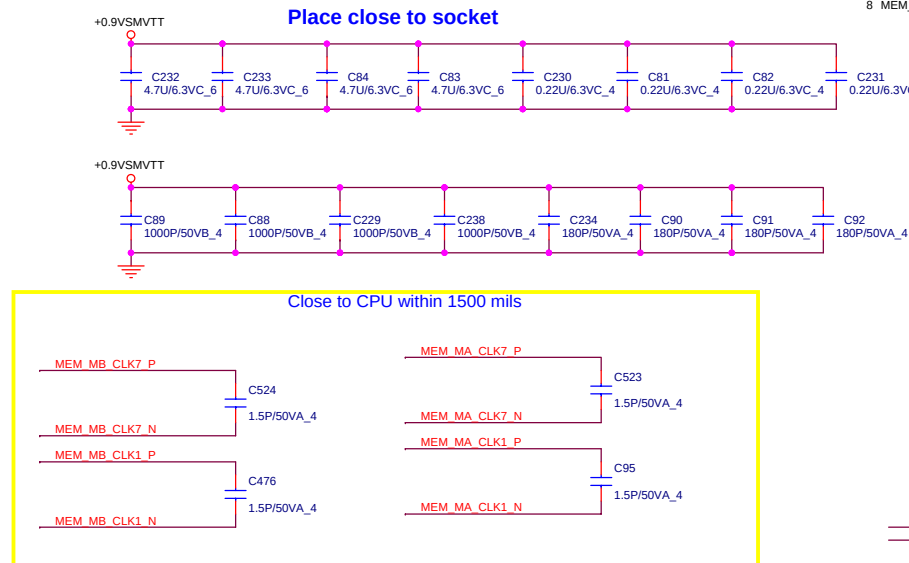
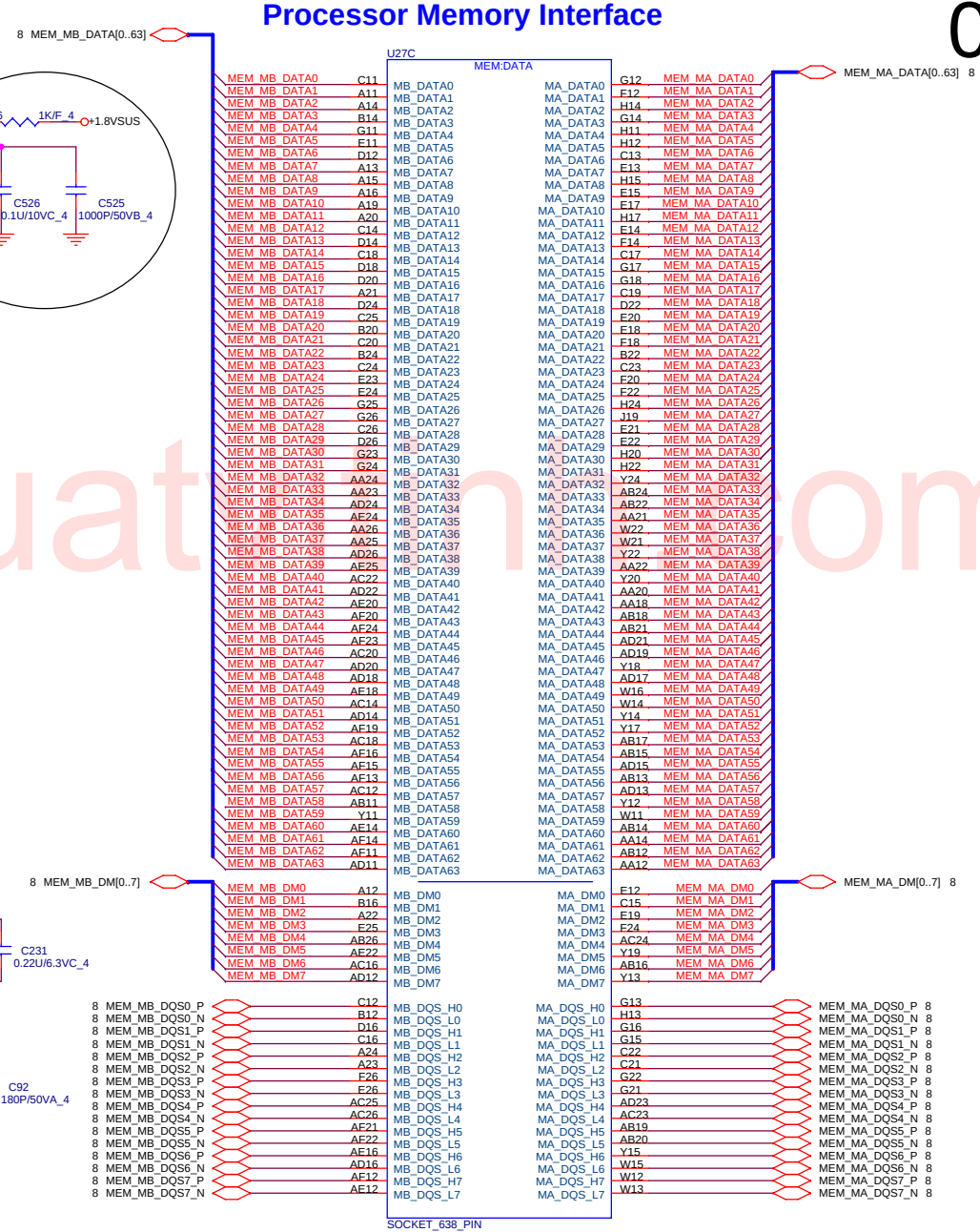
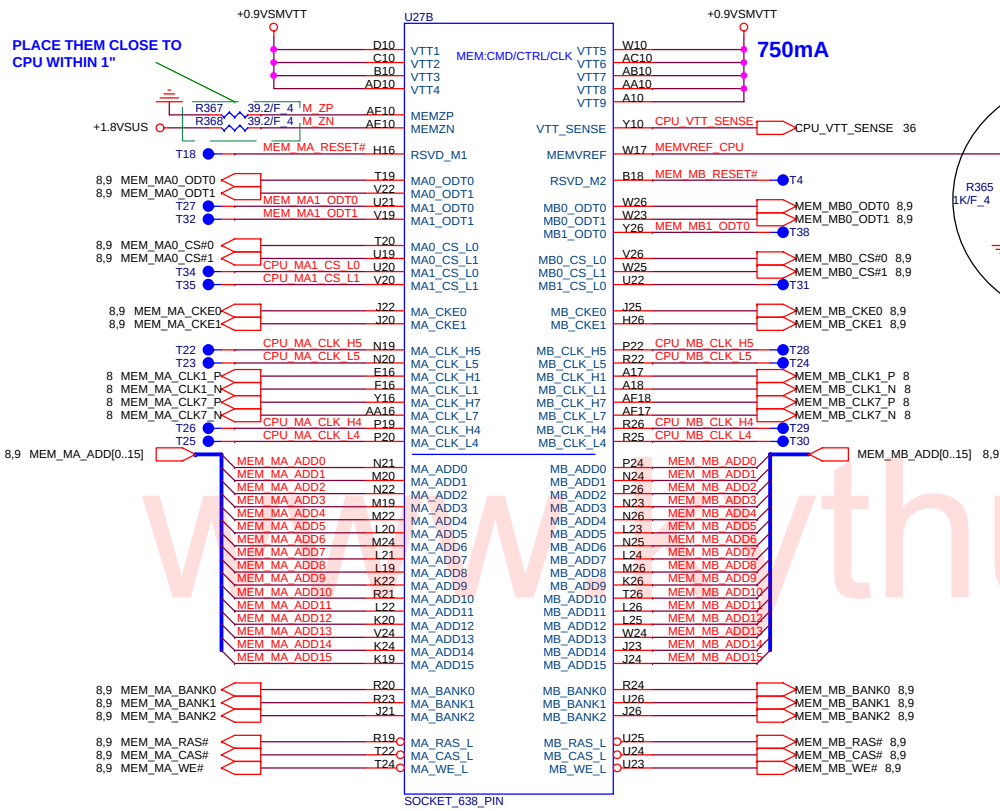
HDT Connector

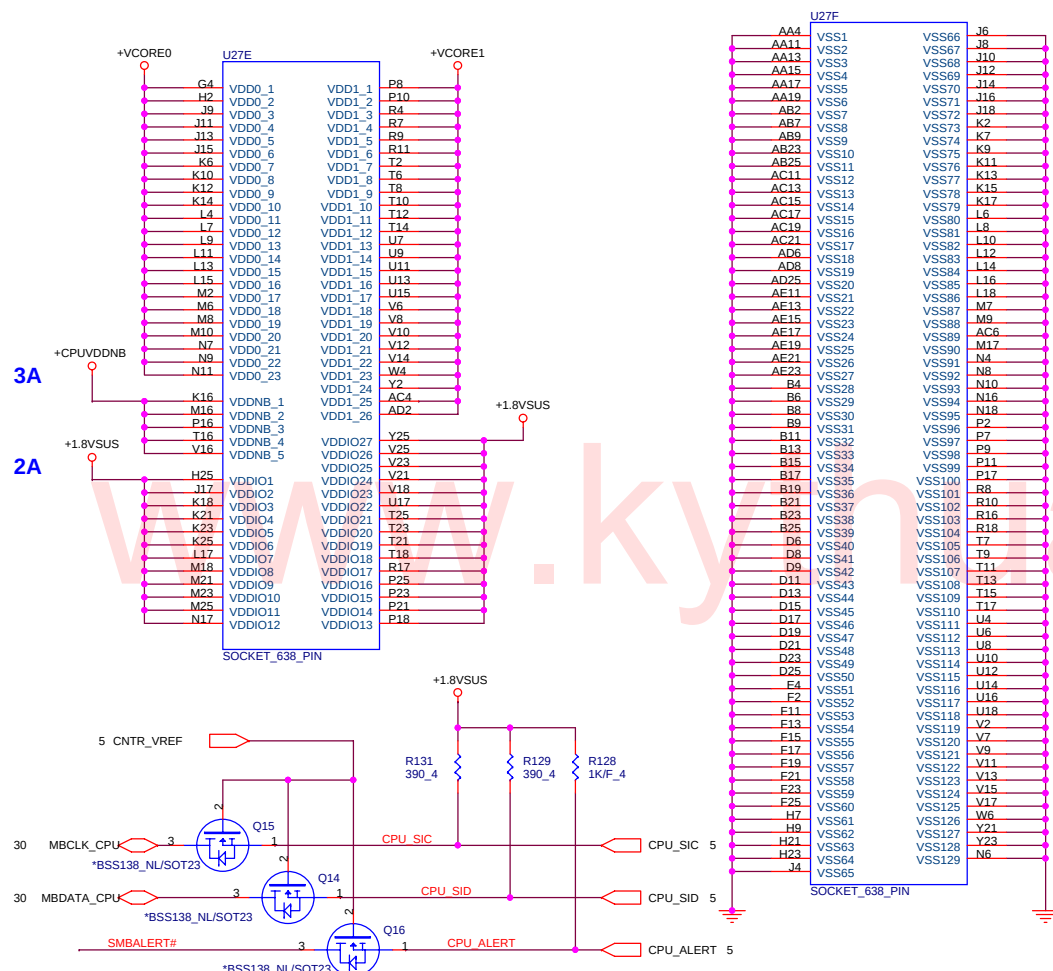


CPU CLK

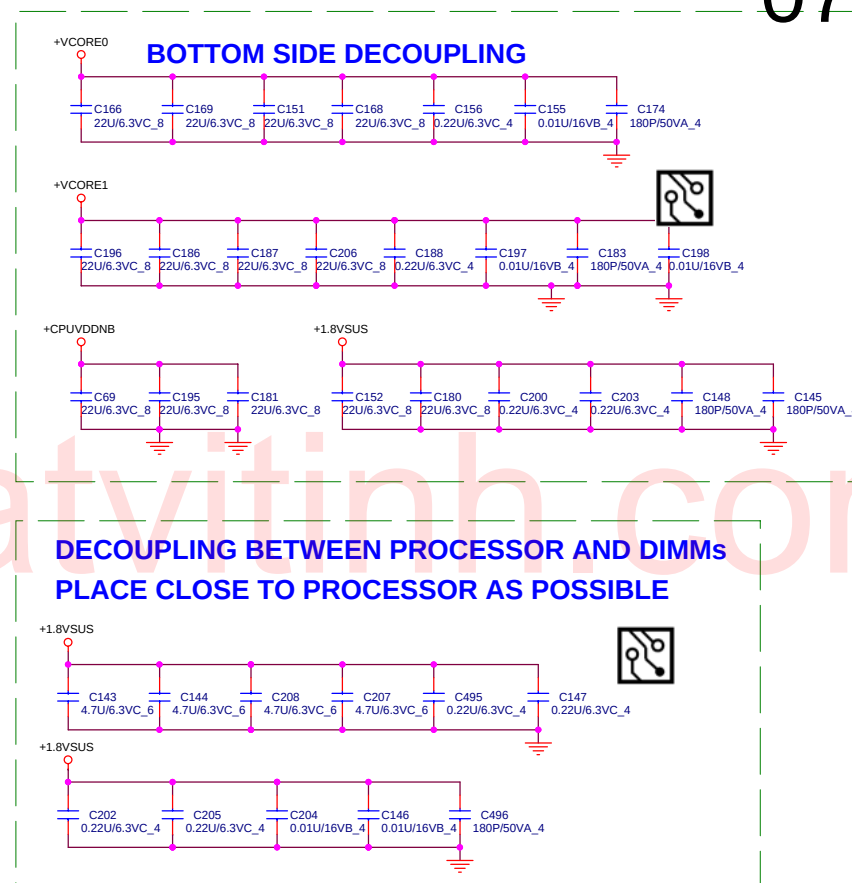
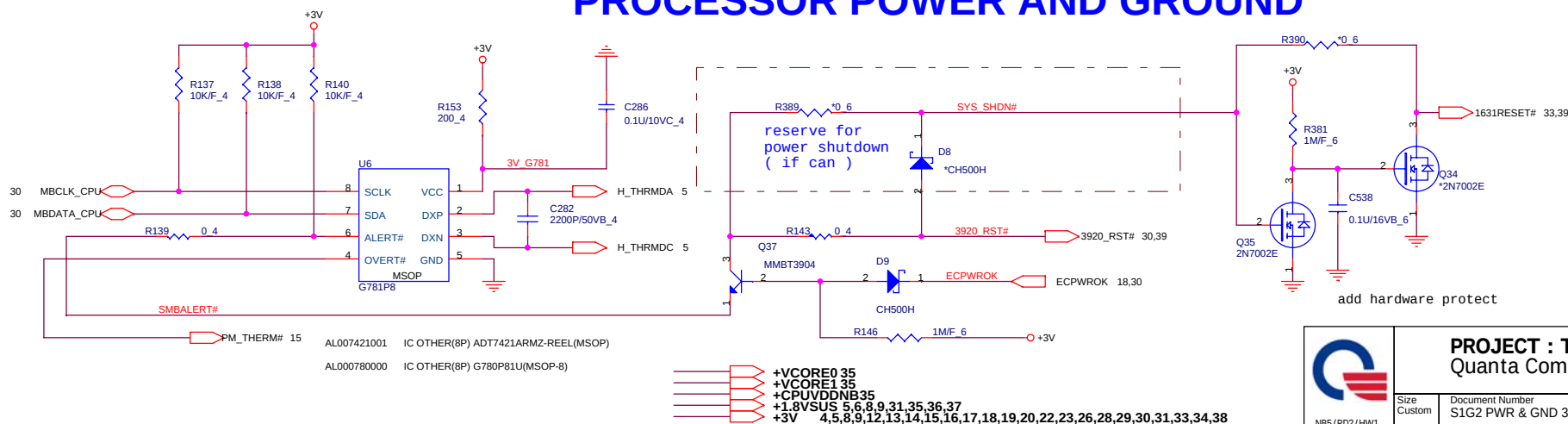


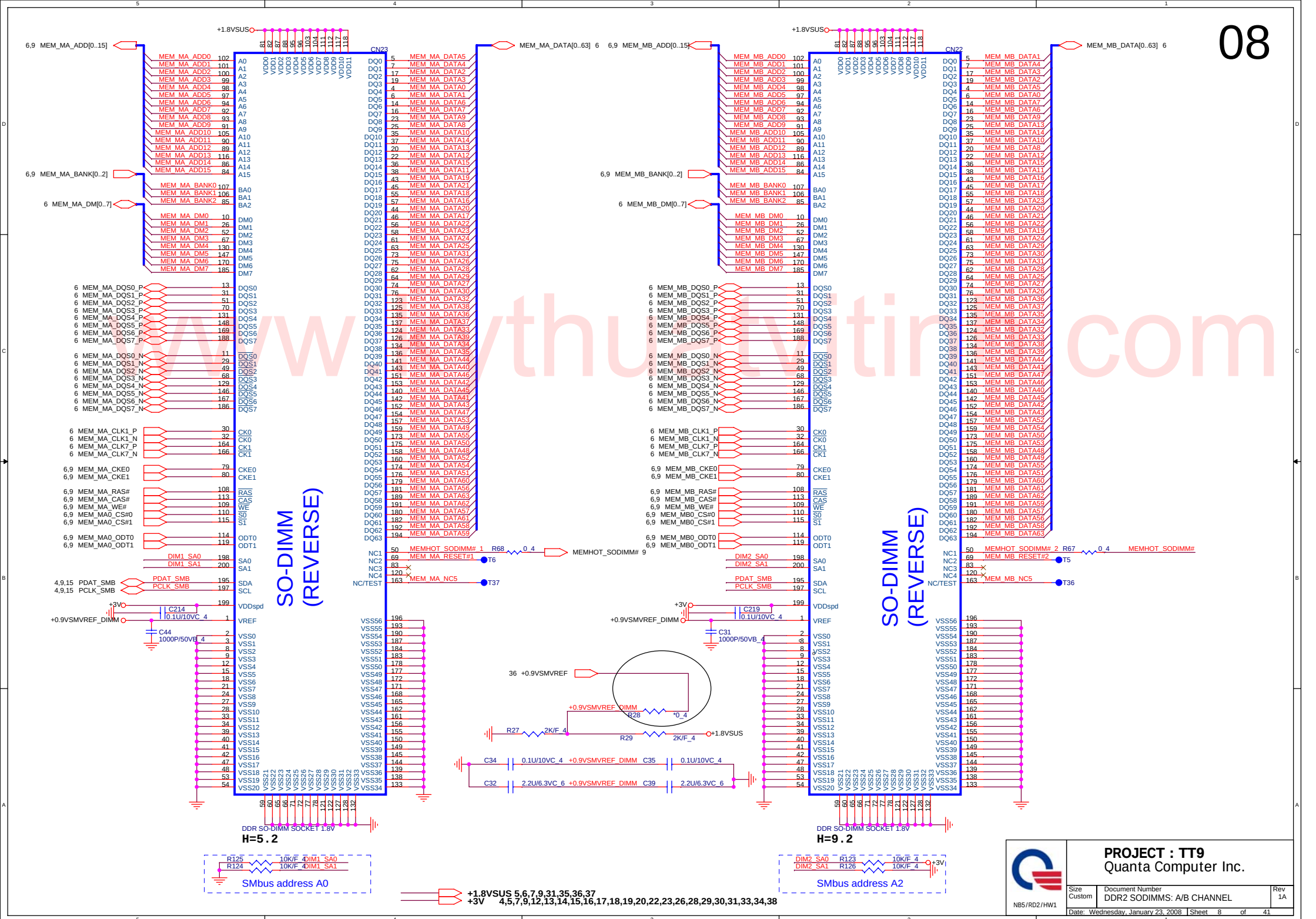
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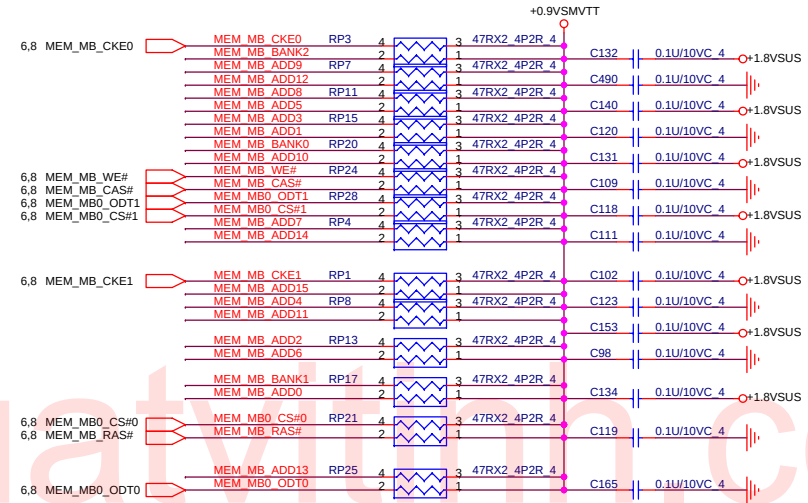
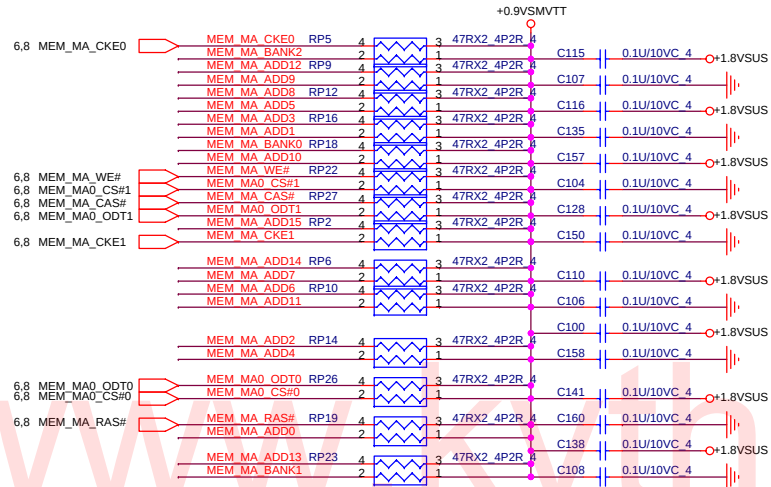
PROCESSOR POWER AND GROUND



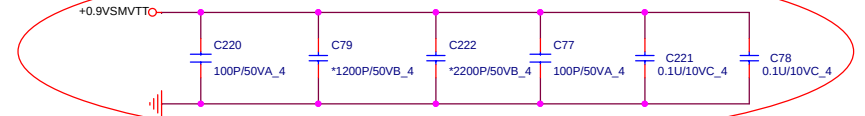


6,8 MEM_MA_ADD[0..15]  MEM_MA_ADD[0..15]
6,8 MEM_MA_BANK[0..2]  MEM_MA_BANK[0..2]

6,8 MEM_MB_ADD[0..15]  MEM_MB_ADD[0..15]
6,8 MEM_MB_BANK[0..2]  MEM_MB_BANK[0..2]



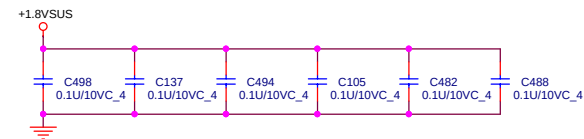
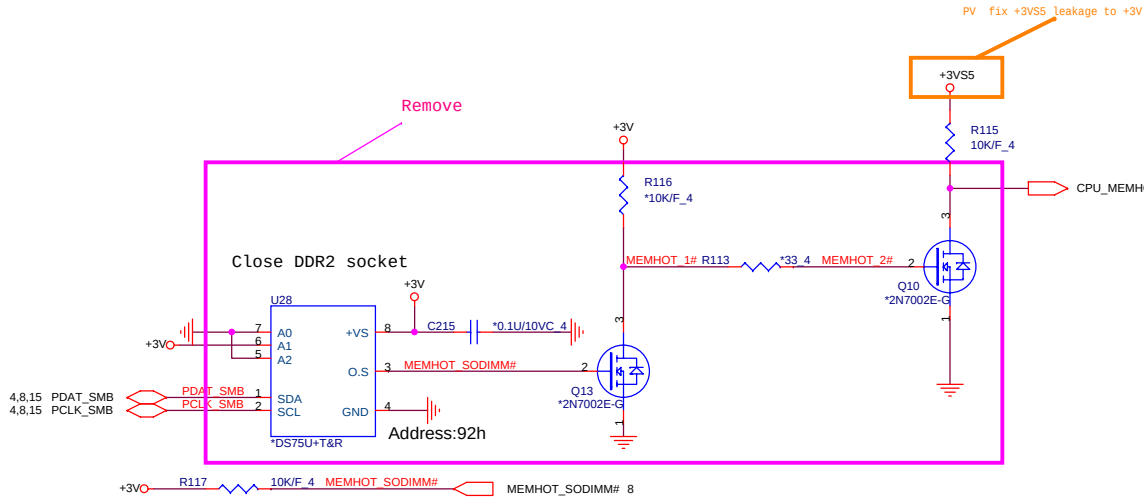
Emi request



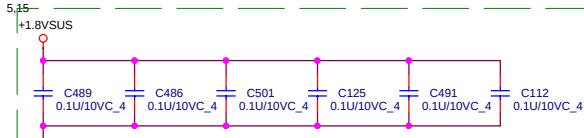
PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



PLACE CLOSE TO SOCKET(PER EMI/EMC)



PLACE CLOSE TO SOCKET(PER EMI/EMC)



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PART 1 OF 6

HYPER TRANSPORT CPU I/F

HT_CPU_NB_CAD_H0 Y25
HT_CPU_NB_CAD_L0 Y24
HT_CPU_NB_CAD_H1 V22
HT_CPU_NB_CAD_L1 V23
HT_CPU_NB_CAD_H2 V25
HT_CPU_NB_CAD_L2 V24
HT_CPU_NB_CAD_H3 U24
HT_CPU_NB_CAD_L3 U25
HT_CPU_NB_CAD_H4 T25
HT_CPU_NB_CAD_L4 T24
HT_CPU_NB_CAD_H5 P22
HT_CPU_NB_CAD_L5 P23
HT_CPU_NB_CAD_H6 P25
HT_CPU_NB_CAD_L6 P24
HT_CPU_NB_CAD_H7 N24
HT_CPU_NB_CAD_L7 N25

HT_CPU_NB_CAD_H8 AC24
HT_CPU_NB_CAD_L8 AC25
HT_CPU_NB_CAD_H9 AB25
HT_CPU_NB_CAD_L9 AB24
HT_CPU_NB_CAD_H10 AA24
HT_CPU_NB_CAD_L10 AA25
HT_CPU_NB_CAD_H11 Y22
HT_CPU_NB_CAD_L11 Y23
HT_CPU_NB_CAD_H12 W21
HT_CPU_NB_CAD_L12 W20
HT_CPU_NB_CAD_H13 V21
HT_CPU_NB_CAD_L13 V20
HT_CPU_NB_CAD_H14 U20
HT_CPU_NB_CAD_L14 U21
HT_CPU_NB_CAD_H15 U19
HT_CPU_NB_CAD_L15 U18

HT_CPU_NB_CLK_H0 T22
HT_CPU_NB_CLK_L0 T23
HT_CPU_NB_CLK_H1 AB23
HT_CPU_NB_CLK_L1 AA22

HT_CPU_NB_CTL_H0 M22
HT_CPU_NB_CTL_L0 M23
HT_CPU_NB_CTL_H1 R21
HT_CPU_NB_CTL_L1 R20

HT_RXCALP C23
HT_RXCALN A24

HT_TXCAD0P D24
HT_TXCAD0N D25
HT_TXCAD1P E24
HT_TXCAD1N E25
HT_TXCAD2P E23
HT_TXCAD2N E22
HT_TXCAD3P E23
HT_TXCAD3N E22
HT_TXCAD4P H23
HT_TXCAD4N H22
HT_TXCAD5P J25
HT_TXCAD5N J24
HT_TXCAD6P K24
HT_TXCAD6N K25
HT_TXCAD7P K23
HT_TXCAD7N K22

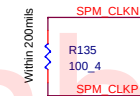
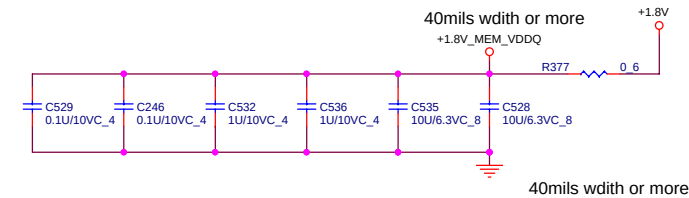
HT_TXCAD8P E21
HT_TXCAD8N G21
HT_TXCAD9P G20
HT_TXCAD9N H21
HT_TXCAD10P J21
HT_TXCAD10N J18
HT_TXCAD11P K17
HT_TXCAD11N L19
HT_TXCAD12P M19
HT_TXCAD12N L18
HT_TXCAD13P M21
HT_TXCAD13N P21
HT_TXCAD14P P18
HT_TXCAD14N M18

HT_TXCLK0P H24
HT_TXCLK0N H25
HT_TXCLK1P L21
HT_TXCLK1N L20

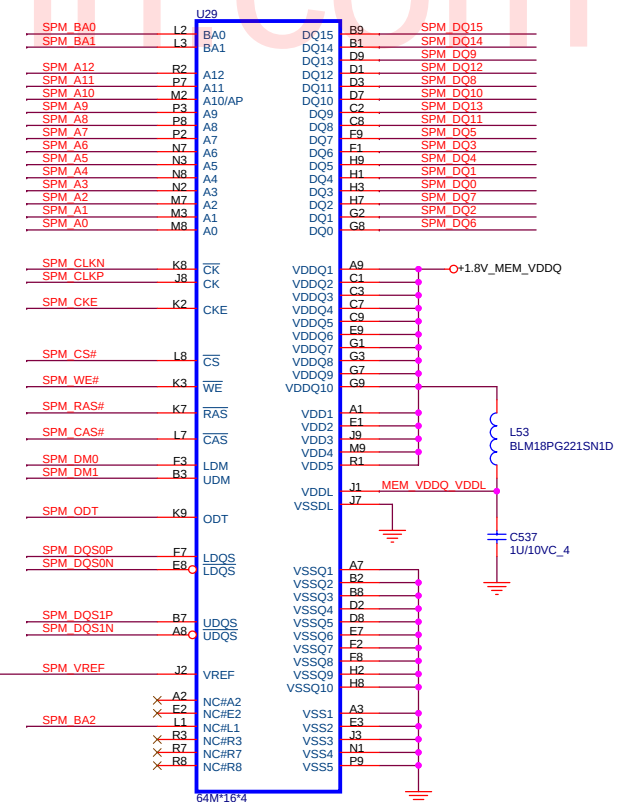
HT_TXCTL0P M24
HT_TXCTL0N M25
HT_TXCTL1P P19
HT_TXCTL1N P18

HT_TXCALP B24
HT_TXCALN B25

HT_CPU_NB_CAD_H[15..0] HT_CPU_NB_CAD_H[15..0] 5
HT_CPU_NB_CAD_L[15..0] HT_CPU_NB_CAD_L[15..0] 5
HT_CPU_NB_CLK_H[1..0] HT_CPU_NB_CLK_H[1..0] 5
HT_CPU_NB_CLK_L[1..0] HT_CPU_NB_CLK_L[1..0] 5
HT_CPU_NB_CTL_H[1..0] HT_CPU_NB_CTL_H[1..0] 5
HT_CPU_NB_CTL_L[1..0] HT_CPU_NB_CTL_L[1..0] 5
HT_NB_CPU_CAD_H[15..0] HT_NB_CPU_CAD_H[15..0] 5
HT_NB_CPU_CAD_L[15..0] HT_NB_CPU_CAD_L[15..0] 5
HT_NB_CPU_CLK_H[1..0] HT_NB_CPU_CLK_H[1..0] 5
HT_NB_CPU_CLK_L[1..0] HT_NB_CPU_CLK_L[1..0] 5
HT_NB_CPU_CTL_H[1..0] HT_NB_CPU_CTL_H[1..0] 5
HT_NB_CPU_CTL_L[1..0] HT_NB_CPU_CTL_L[1..0] 5



Close to U23



PV modified --
follow AMD
check list to
change part
number 300 ohm
to 301 ohm

PV modified --
follow AMD
check list to
change part
number 300 ohm
to 301 ohm

PAR 4 OF 6

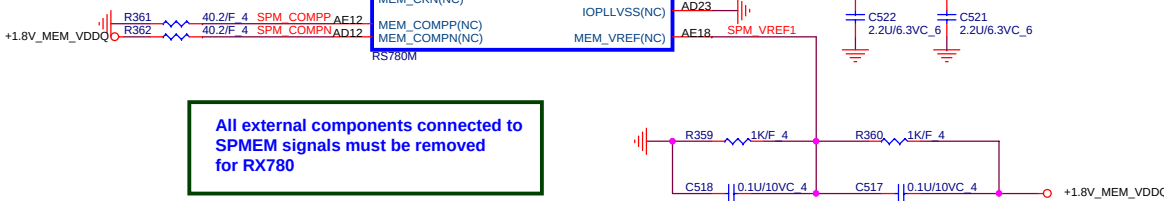
SBD_MEM/DVO_I/F

SPM_A0 AB12
SPM_A1 AE16
SPM_A2 V11
SPM_A3 AE15
SPM_A4 AE12
SPM_A5 AB16
SPM_A6 AB14
SPM_A7 AD14
SPM_A8 AD13
SPM_A9 AC15
SPM_A10 AC16
SPM_A11 AE13
SPM_A12 AC14
SPM_A13 Y14

SPM_BA0 AD16
SPM_BA1 AE17
SPM_BA2 AD17
SPM_RAS# W12
SPM_CAS# Y12
SPM_WE# AD18
SPM_CS# AB13
SPM_CKE AB18
SPM_ODT V14
SPM_CLKP W15
SPM_CLKN W14

MEM_A0(NC) MEM_DQ0/DVO_VSYNC(NC) AA18 SPM_DQ0
MEM_A1(NC) MEM_DQ1/DVO_HSYNC(NC) AA20 SPM_DQ1
MEM_A2(NC) MEM_DQ2/DVO_DE(NC) AA19 SPM_DQ2
MEM_A3(NC) MEM_DQ3/DVO_D0(NC) V19 SPM_DQ3
MEM_A4(NC) MEM_DQ4(NC) V17 SPM_DQ4
MEM_A5(NC) MEM_DQ5/DVO_D1(NC) AA17 SPM_DQ5
MEM_A6(NC) MEM_DQ6/DVO_D2(NC) AA15 SPM_DQ6
MEM_A7(NC) MEM_DQ7/DVO_D4(NC) Y15 SPM_DQ7
MEM_A8(NC) MEM_DQ8/DVO_D3(NC) AC20 SPM_DQ8
MEM_A9(NC) MEM_DQ9/DVO_D5(NC) AD19 SPM_DQ9
MEM_A10(NC) MEM_DQ10/DVO_D6(NC) AC18 SPM_DQ10
MEM_A11(NC) MEM_DQ11/DVO_D7(NC) AD22 SPM_DQ11
MEM_A12(NC) MEM_DQ12(NC) AD22 SPM_DQ12
MEM_A13(NC) MEM_DQ13/DVO_D9(NC) AD22 SPM_DQ13
MEM_BA0(NC) MEM_DQ14/DVO_D10(NC) AD22 SPM_DQ14
MEM_BA1(NC) MEM_DQ15/DVO_D11(NC) AD21 SPM_DQ15

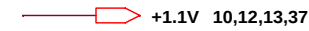
MEM_DQ0S0P/DVO_IDCKP(NC) Y17 SPM_DQ0S0P
MEM_DQ0S0N/DVO_IDCKN(NC) W18 SPM_DQ0S0N
MEM_DQ0S1P(NC) AD20 SPM_DQ0S1P
MEM_DQ0S1N(NC) AE21 SPM_DQ0S1N
MEM_DM0(NC) W17 SPM_DM0
MEM_CKE(NC) AE19 SPM_DM1
MEM_ODT(NC) AE23 +1.8V_IOPLLVDD18 NB
MEM_CKPN(NC) AE24 +1.1V_IOPLLVDD L49
MEM_CKN(NC) AD23 SPM_VREF1 C522
MEM_COMP(NC) C521
MEM_CMPN(NC) C517



+0.9VSMVTT 6,9,31,36
+1.1V 11,12,13,37
+1.8V 5,12,13,14,15,18,36,38



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Enables the Test Debug Bus using GPIO.

0 : Enable
1 : Disable
(RS780 use VSYNC#)

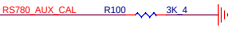


Enables Side port memory

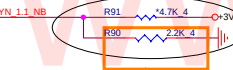
0 : Enable (RS780)
1 : Disable (RS780)
(RS780 use HSYNC#)



default values if not connected
RS780:SUS_STAT

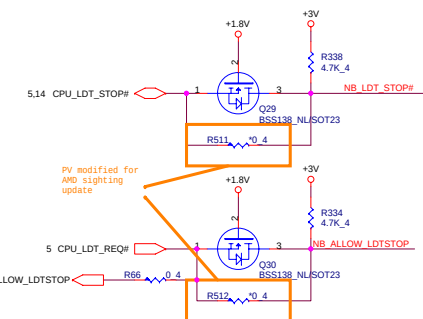
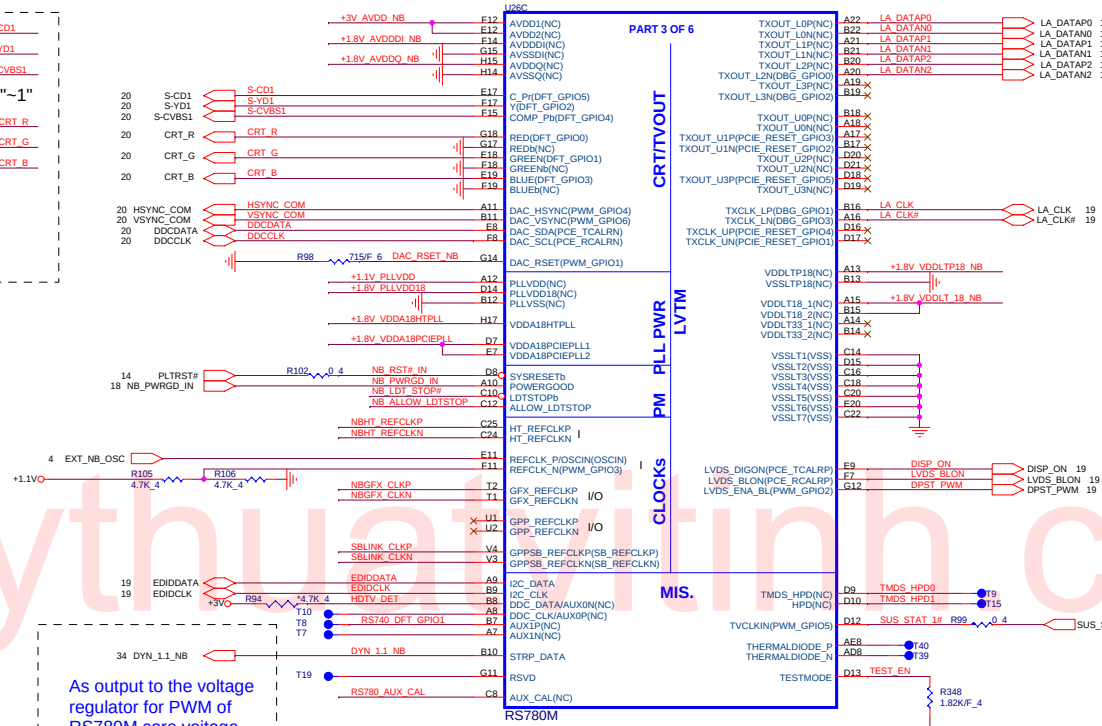


AUX CAL Value need update



PV modified for
AMD sighting
update

As output to the voltage
regulator for PWM of
RS780M core voltage.

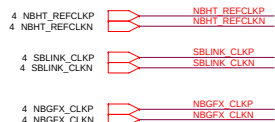


0.135A for AVDD

0.15A for PLLs 1.1V

0.1A for PLLs 1.8V

0.08A for VDDLTP18

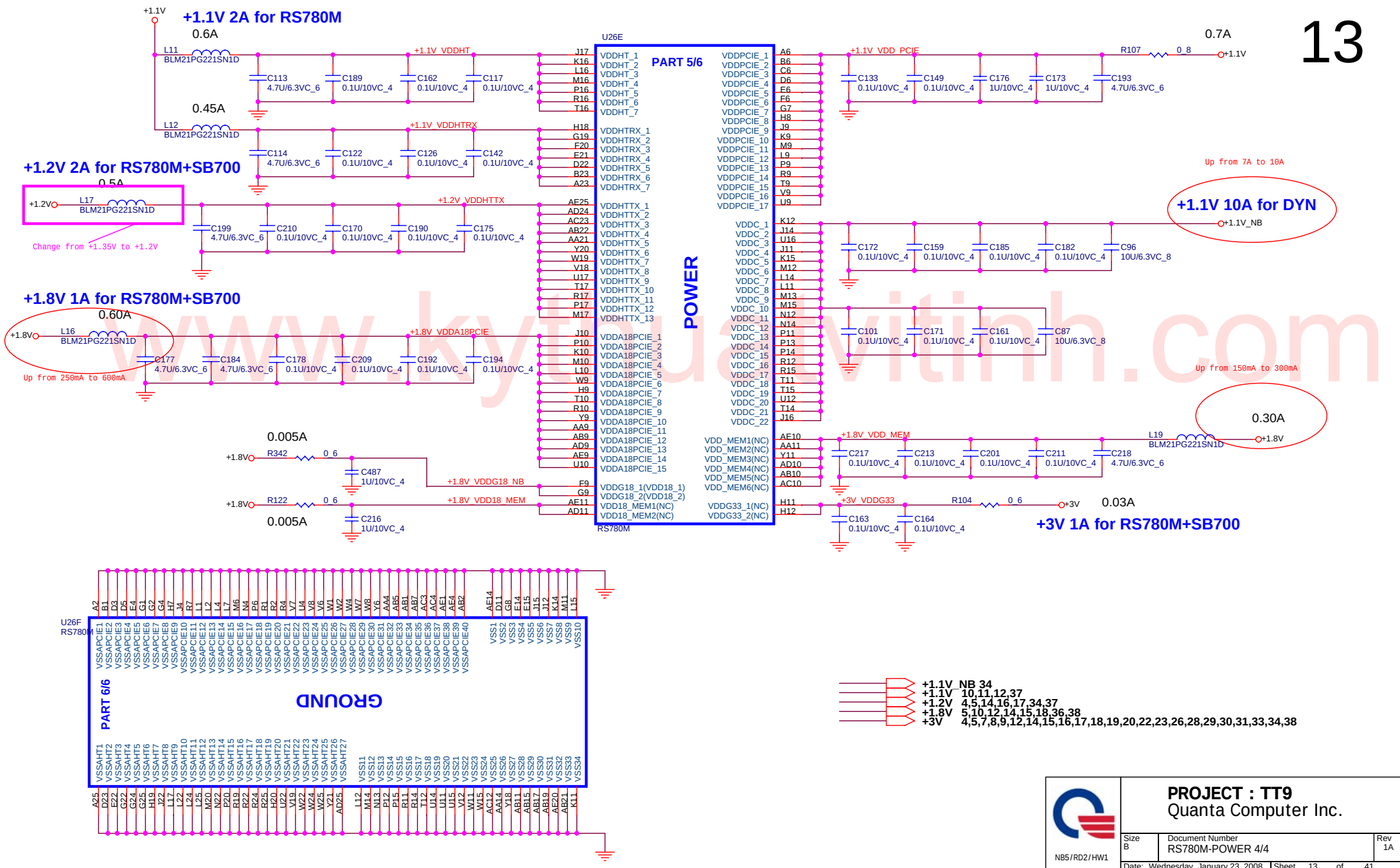


+1.1V 10,11,13,37
+1.8V 5,10,13,14,15,18,36,38
+3V 4,5,7,8,9,13,14,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38
+12VALW 19,28,31,33,38



PROJECT : TT9
Quanta Computer Inc.

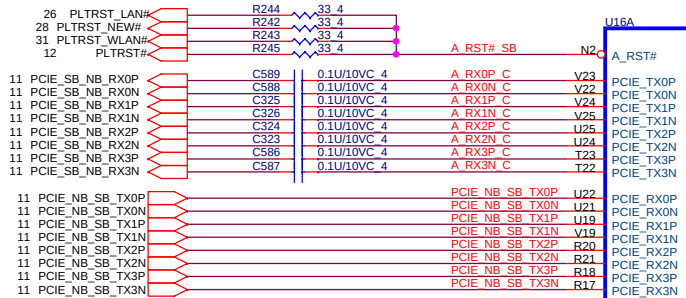
Size C Document Number RS780M-SYSTEM I/F 3/4 Rev 1A
Date: Wednesday, January 23, 2008 Sheet 12 of 41



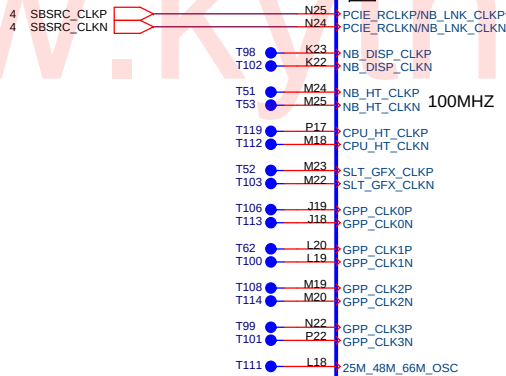
PLACE THESE
PCIe AC
COUPLING CAPS
CLOSE TO U600



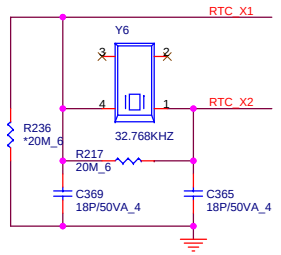
To RS780



1. PCIe Reference Clk(Ext Clk Gen)
2. A-link Clk to North Bridge(Int Clk Gen)



PV fix +3VS5 leakage to +3v



SB700

Part 1 of 5

PCI EXPRESS INTERFACE

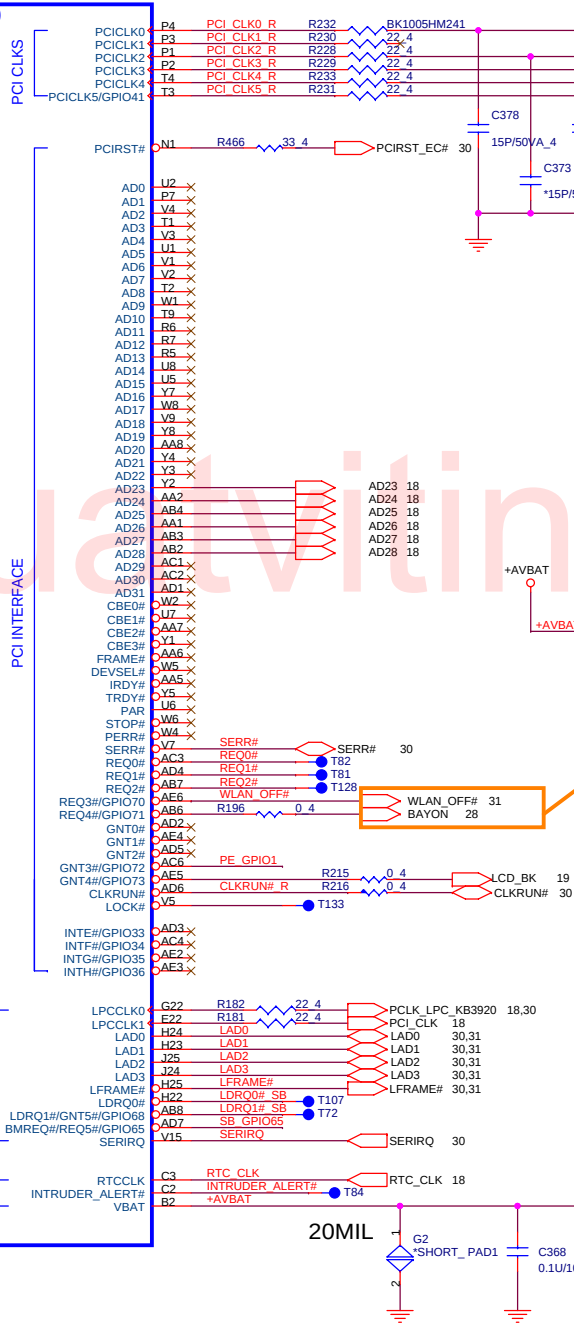
PCI INTERFACE

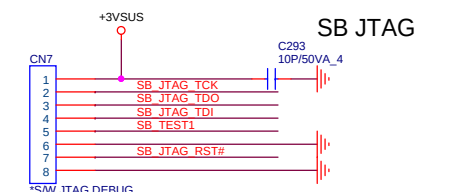
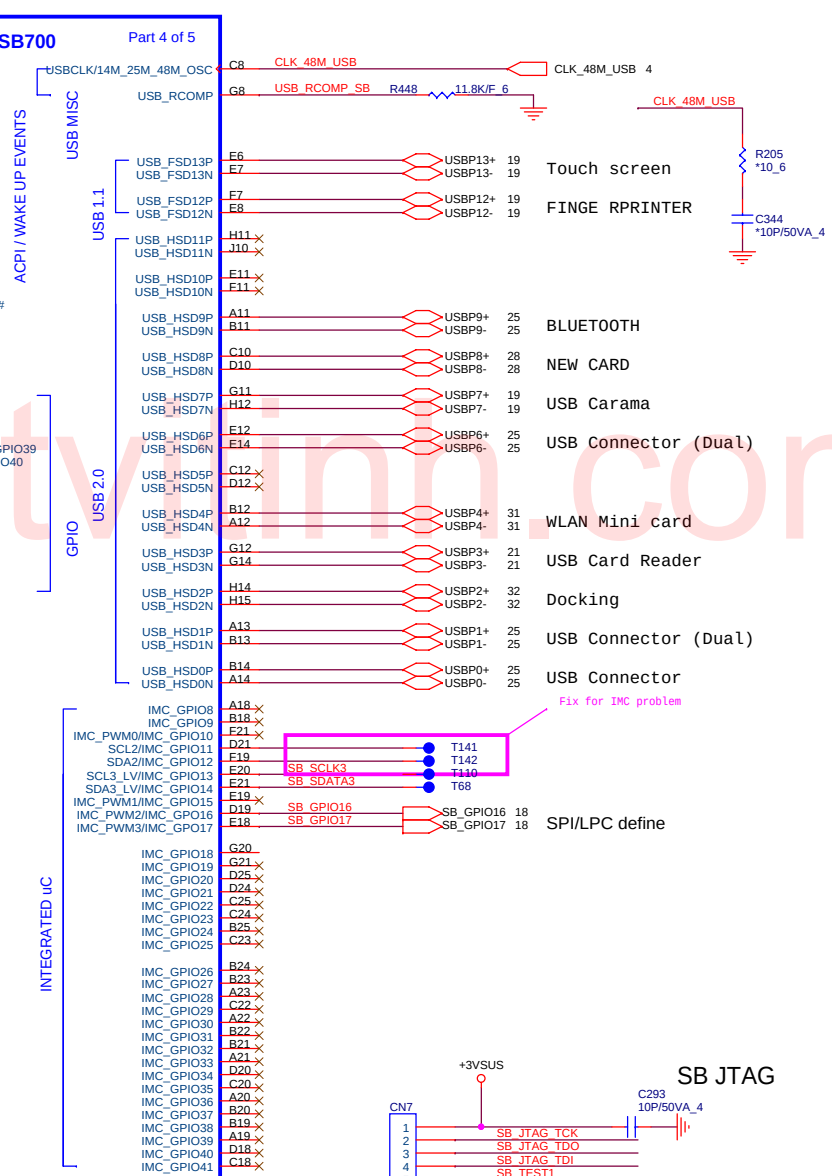
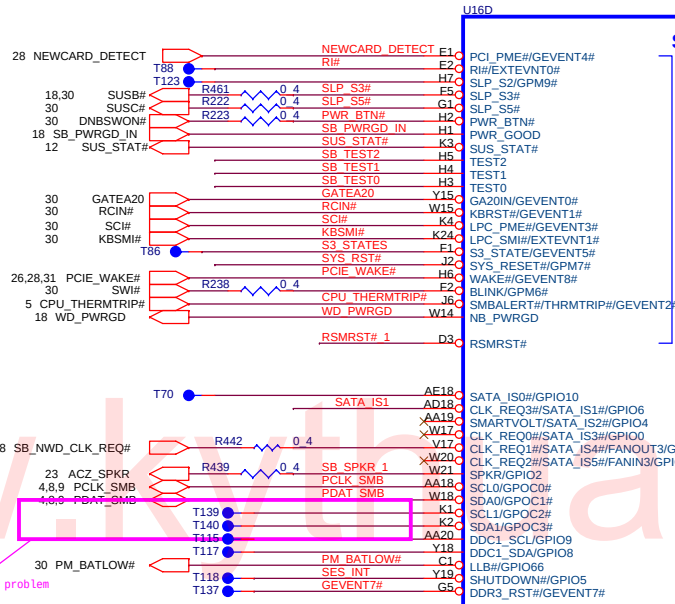
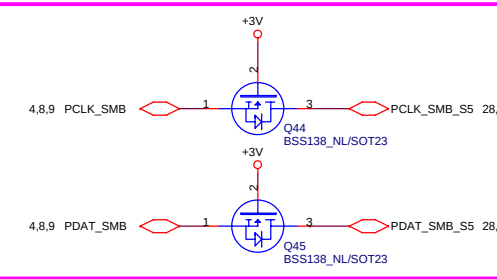
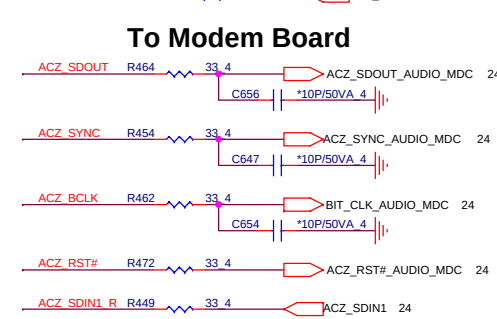
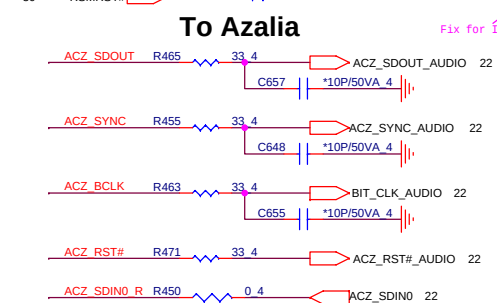
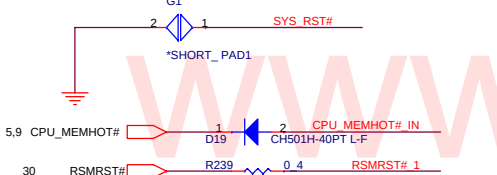
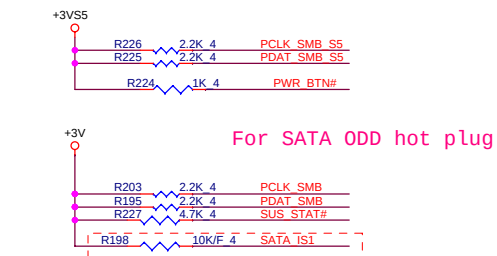
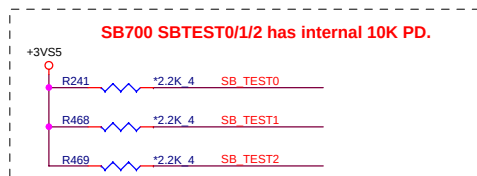
CLOCK GENERATOR

LPC

RTC

CPU





+1.8VSUS 5,6,7,8,9,31,35,36,37
 +1.8V 5,10,12,13,14,18,36,38
 +3VSUS 21,24,25,28,31,33,34,35,36,38
 +3VS5 9,14,16,17,18,28,33,38
 +3V 4,5,7,8,9,12,13,14,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38

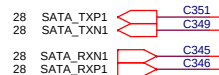


PLACE SATA AC COUPLING
CAPS CLOSE TO SB600

SATA1



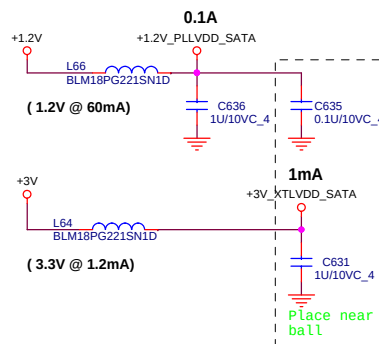
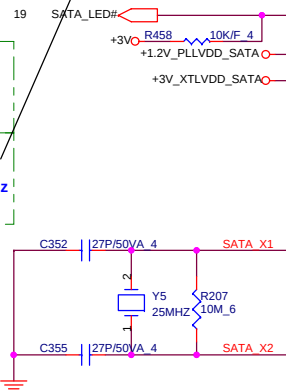
SATA ODD



PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF U600

NOTE:

R635 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK



U16B

SB700

Part 2 of 5

SERIAL ATA

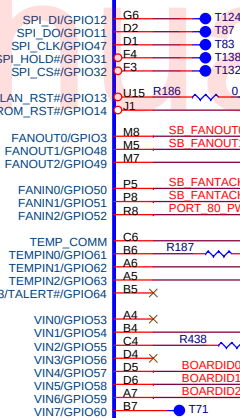
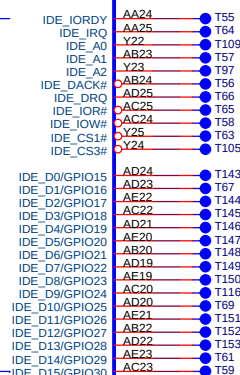
SATA PWR

HW MONITOR

ATA 66/100/133

SPI ROM

HW MONITOR

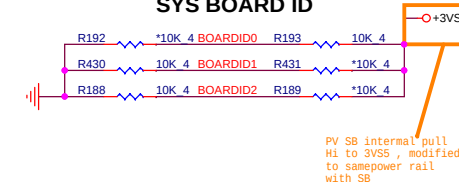


IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

Board ID	VRAM / Clock Gen	Samsung Realtek (0.0.0)	Qimonda ICS (1.0.0)	Hynix Silego (0.1.0)
BOARDID0		R192 Stuff	R193 Stuff	R192 Stuff
BOARDID1		R430 Stuff	R430 Stuff	R431 Stuff
BOARDID2		R188 Stuff	R188 Stuff	R188 Stuff

DB2 MODIFY

SYS BOARD ID



PV SB internal pull
Hi to 3V55, modified
to samepower rail
with SB

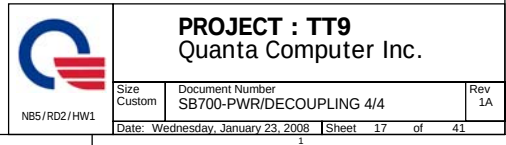
PV fix +3V55 leakage to +3V

+1.2V 4,5,13,14,17,34,37
+3V 4,5,7,8,9,12,13,14,15,17,18,19,20,22,23,26,28,29,30,31,33,34,38

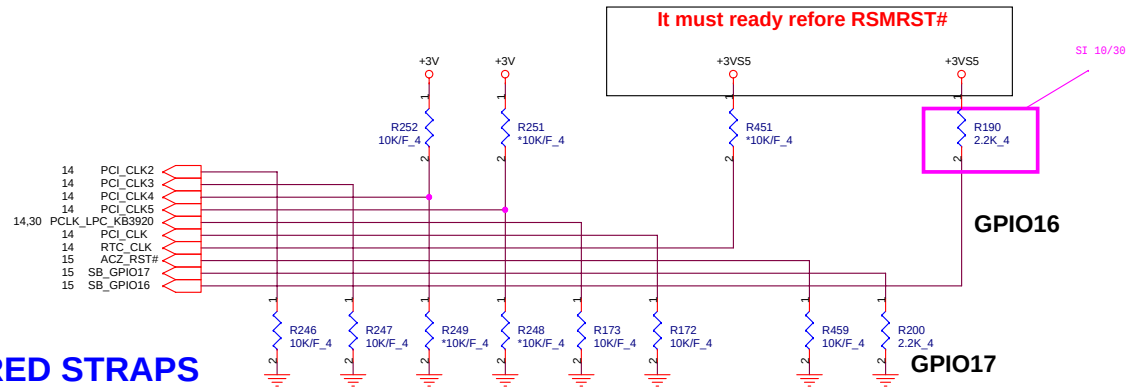


PROJECT : TT9
Quanta Computer Inc.

Size Custom	Document Number SB700-SATA/IDE/HWM/SPI 3/4	Rev 1A
NB5/RD2/HW1	Date: Wednesday, January 23, 2008	Sheet 16 of 41



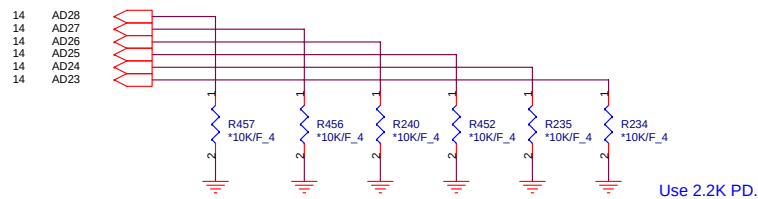
NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



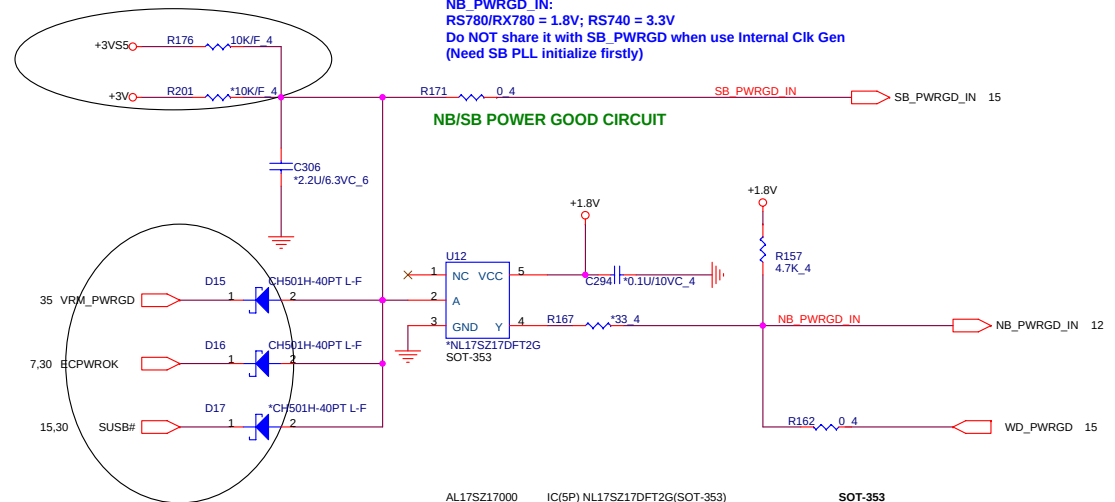
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



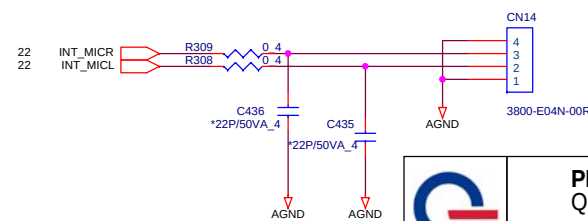
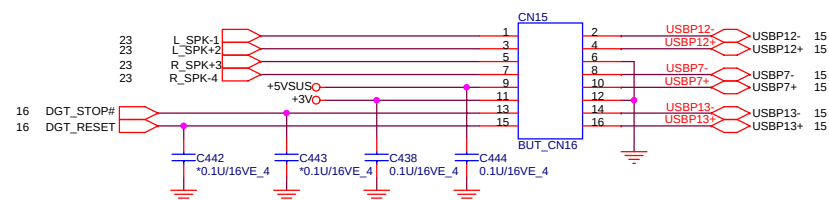
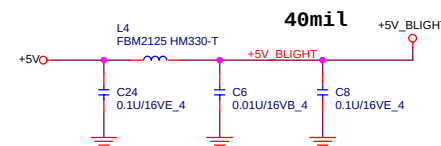
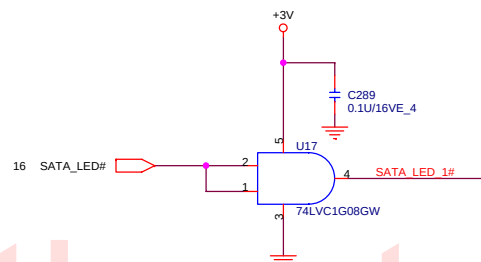
AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5



PROJECT : TT9
Quanta Computer Inc.

Size Custom Document Number SB700-STRAPS,PWRGD Rev 1A
Date: Wednesday, January 23, 2008 Sheet 18 of 41

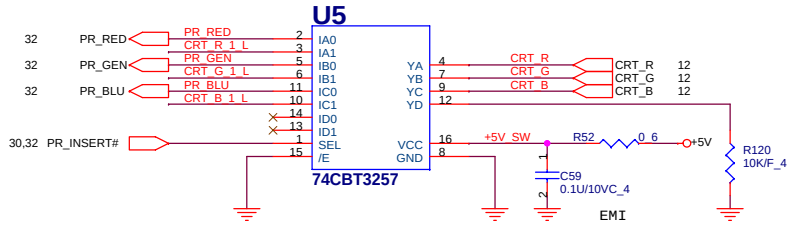
+1.8V 5,10,12,13,14,15,36,38
+3V 4,5,7,8,9,12,13,14,15,16,17,19,20,22,23,26,28,29,30,31,33,34,36
+3VS5 9,14,15,16,17,28,33,38



Speaker
+5VSUS --> Camera
+3V --> FP/Digitizer
Digitizer control signal

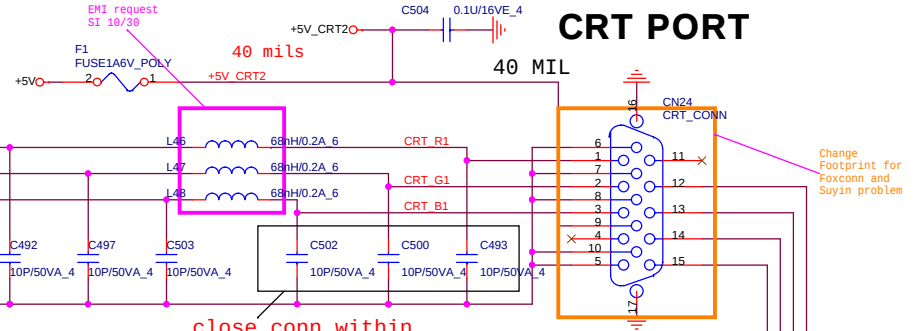

 +3VPCU 5,14,25,29,30,32,33,35,37,39
 +3V 4,5,7,8,9,12,13,14,15,16,17,18,20,22,23,26,28,29,30,31,33,34,38
 +3VSLUS 15,21,24,25,29,31,33,34,35,36,38
 +5V 17,20,22,23,28,31,32,33,37,38,39
 +12VALW 28,31,33,38

CRT SWITCH

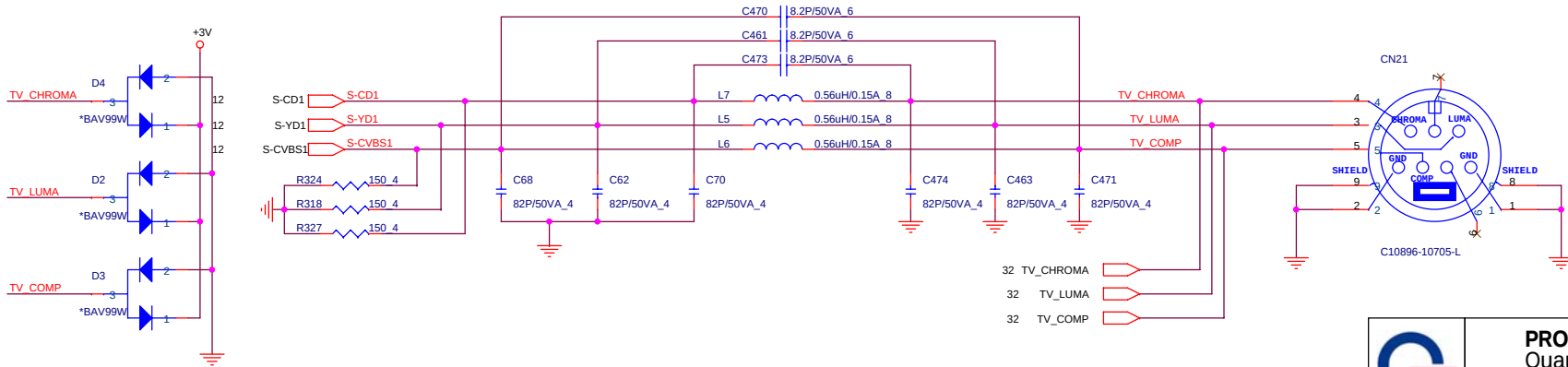
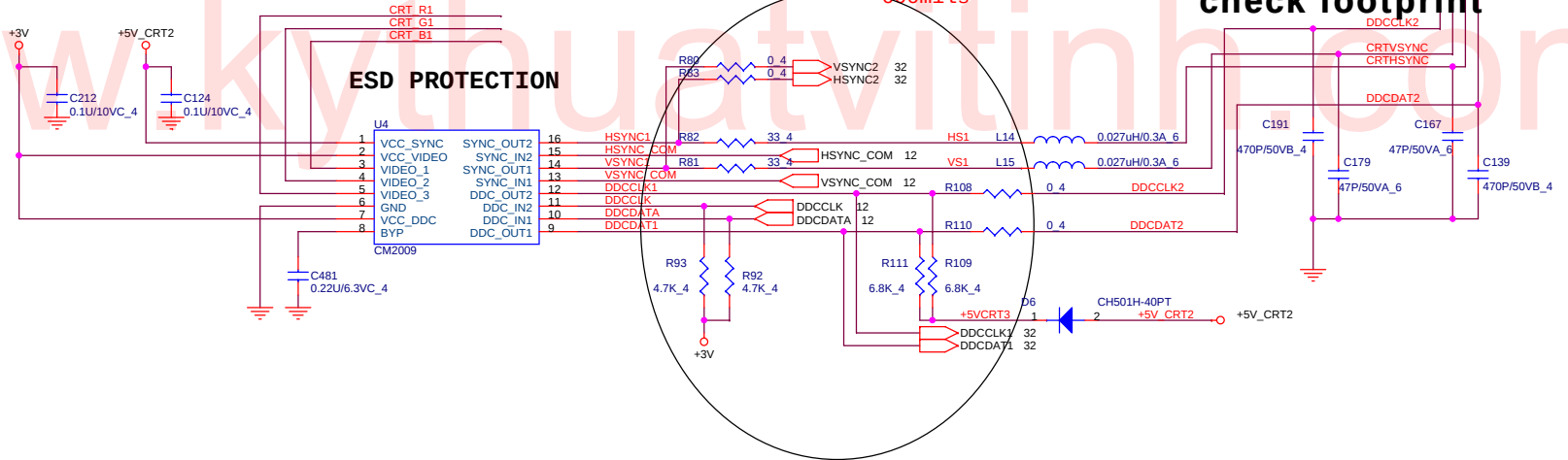


inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

CRT PORT



ESD PROTECTION



PROJECT : TT9
Quanta Computer Inc.

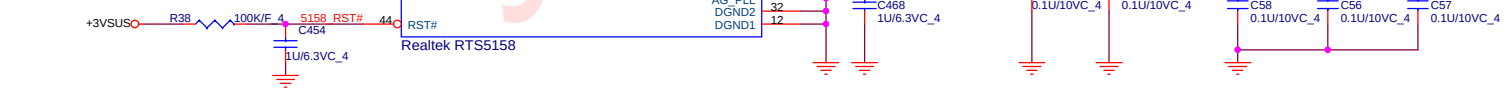
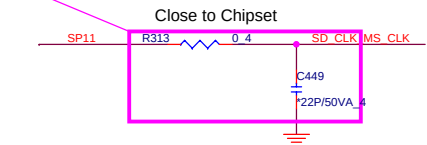
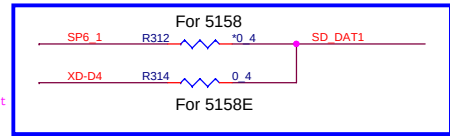
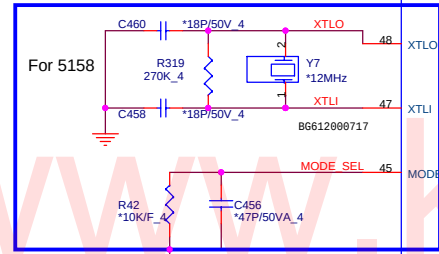
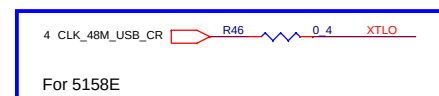
Size Custom	Document Number CRT_TV_OUT	Rev 1A
Date: Wednesday, January 23, 2008	Sheet 20 of 41	

+3V 4,5,7,8,9,12,13,14,15,16,17,18,19,22,23,26,28,29,30,31,33,34,38
+5V 17,19,22,23,28,31,32,33,37,38,39

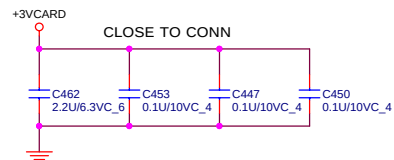
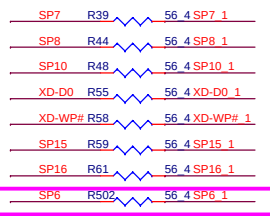
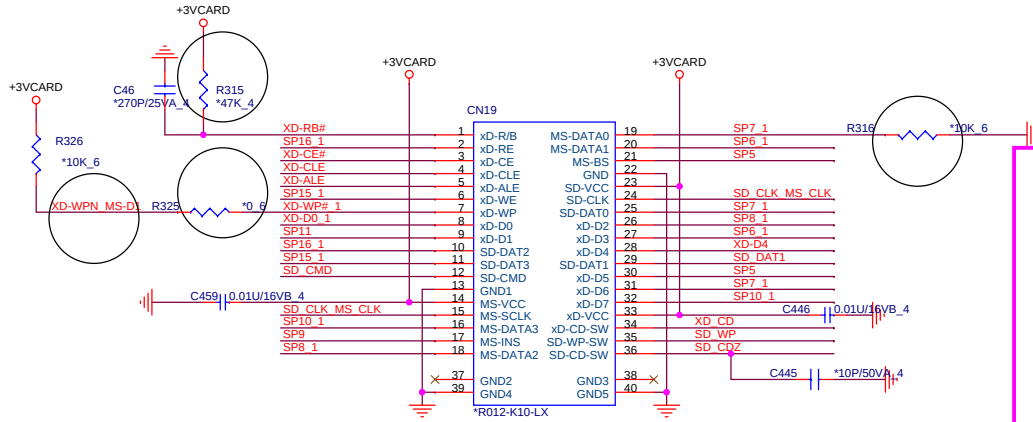
Note:

	SD/MMC	MS	XD
SP0			XD_CD#
SP1	SD_WP		XD_CD#
SP2	SD_WP		XD_CD#
SP3	SD_CD#		
SP4		XD_D4	
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14		XD_R/#	
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

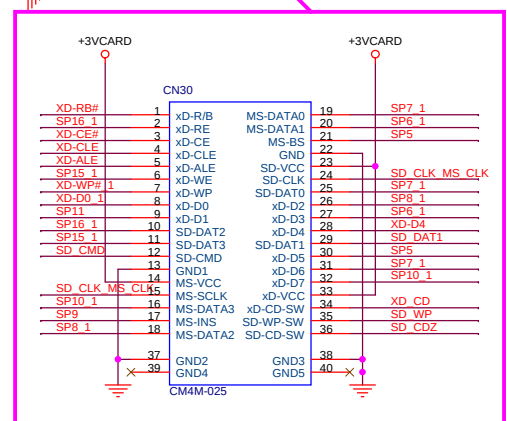
Fix card reader led problem



4 IN1 CARD READER XD, MMC/SD, MS/MSP

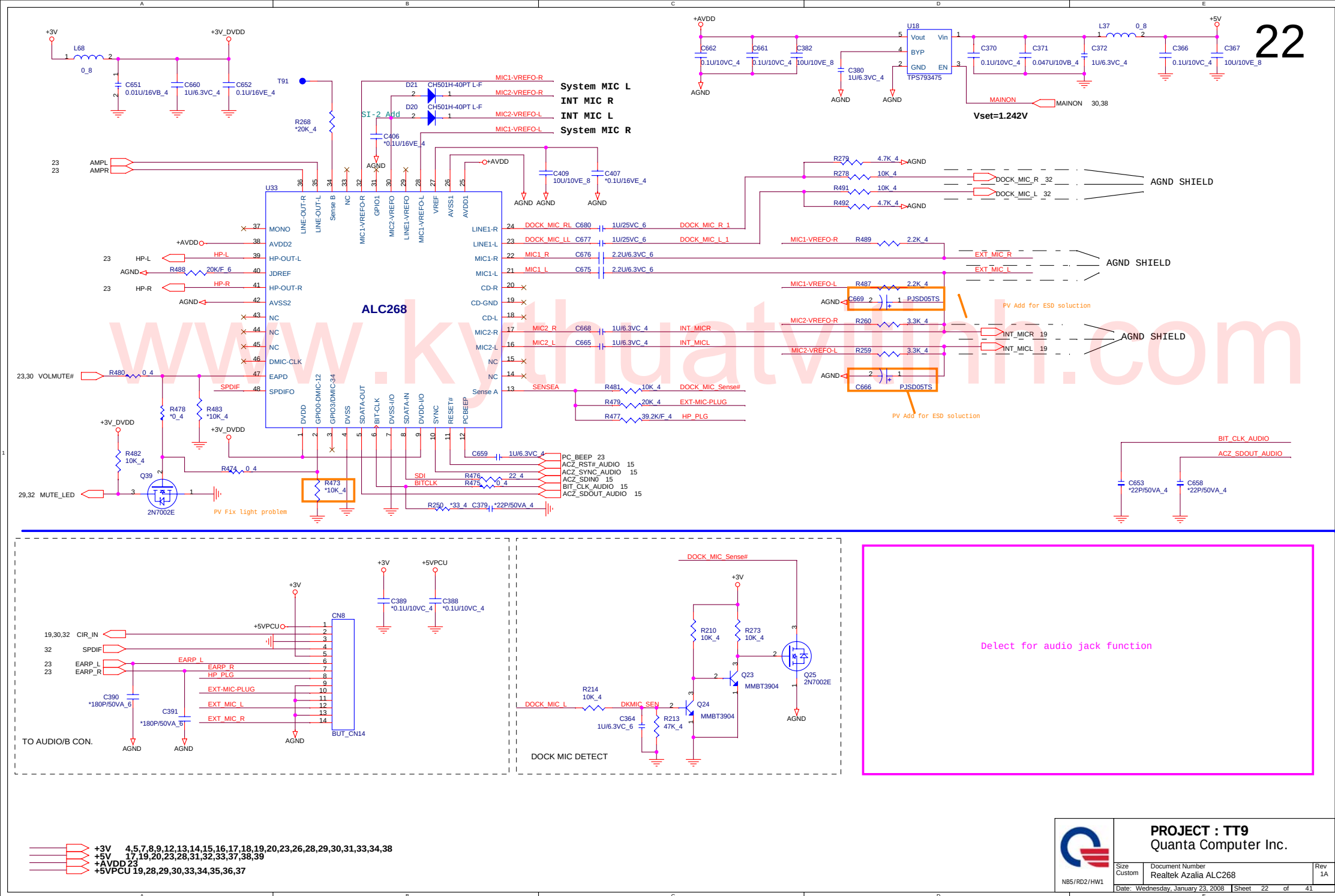


Add Connector for joint

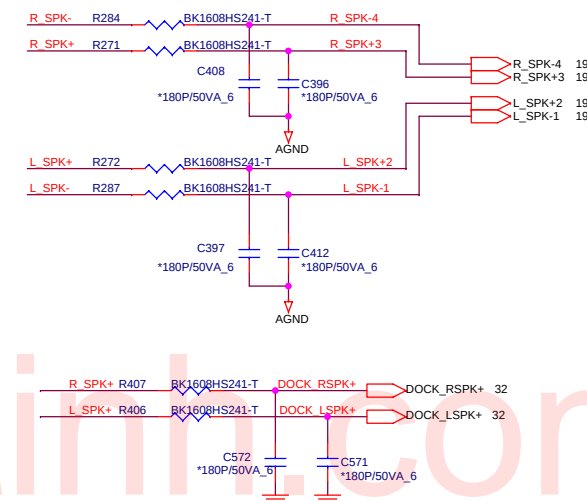


Remove Acces from HP information

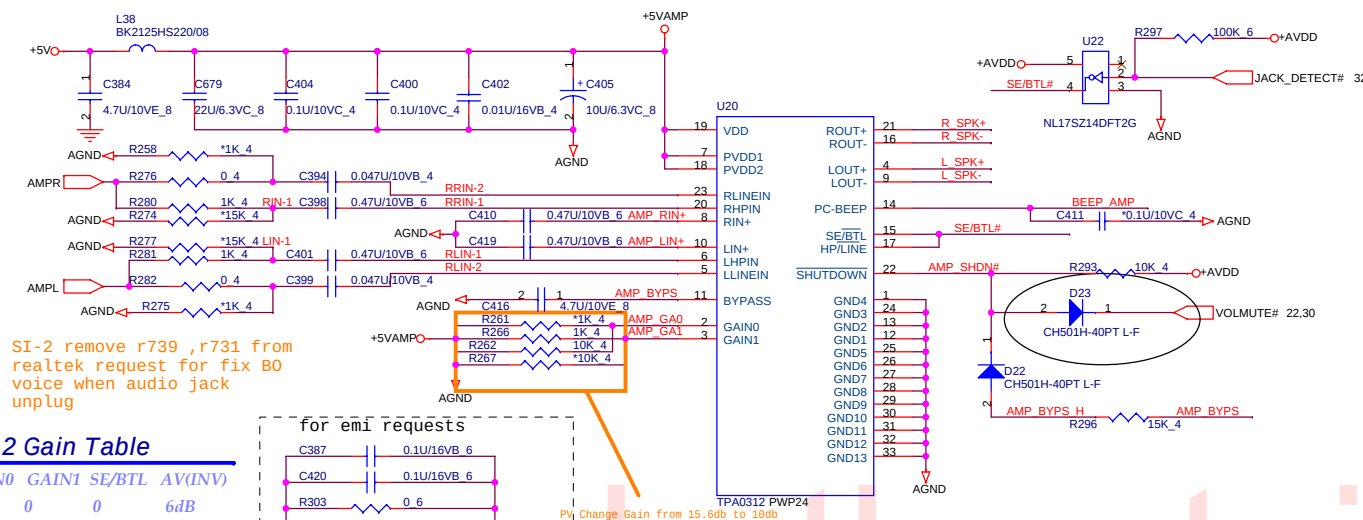
+3VSUS 15,24,25,29,31,33,34,35,36,38



INT. SPEAKER



AUDIO AMPLIFIER

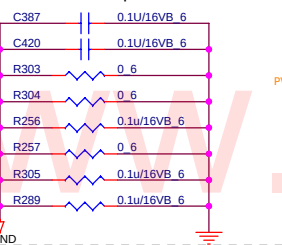


SI-2 remove r739 ,r731 from
realtek request for fix B0
voice when audio jack
unplug

0312 Gain Table

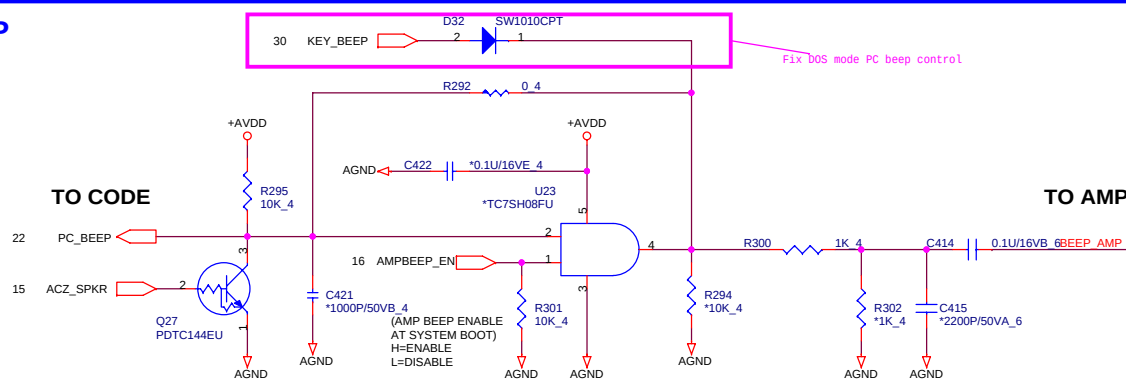
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB

for emi requests

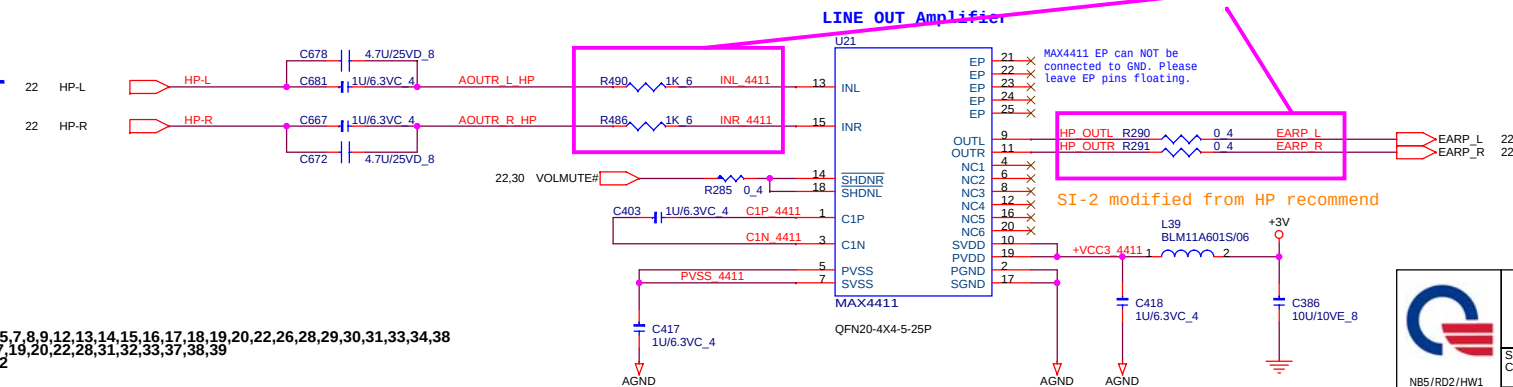


Pv Change Gain from 15.6db to 10db

PCSPK BEEP



LINE OUT Amplifier

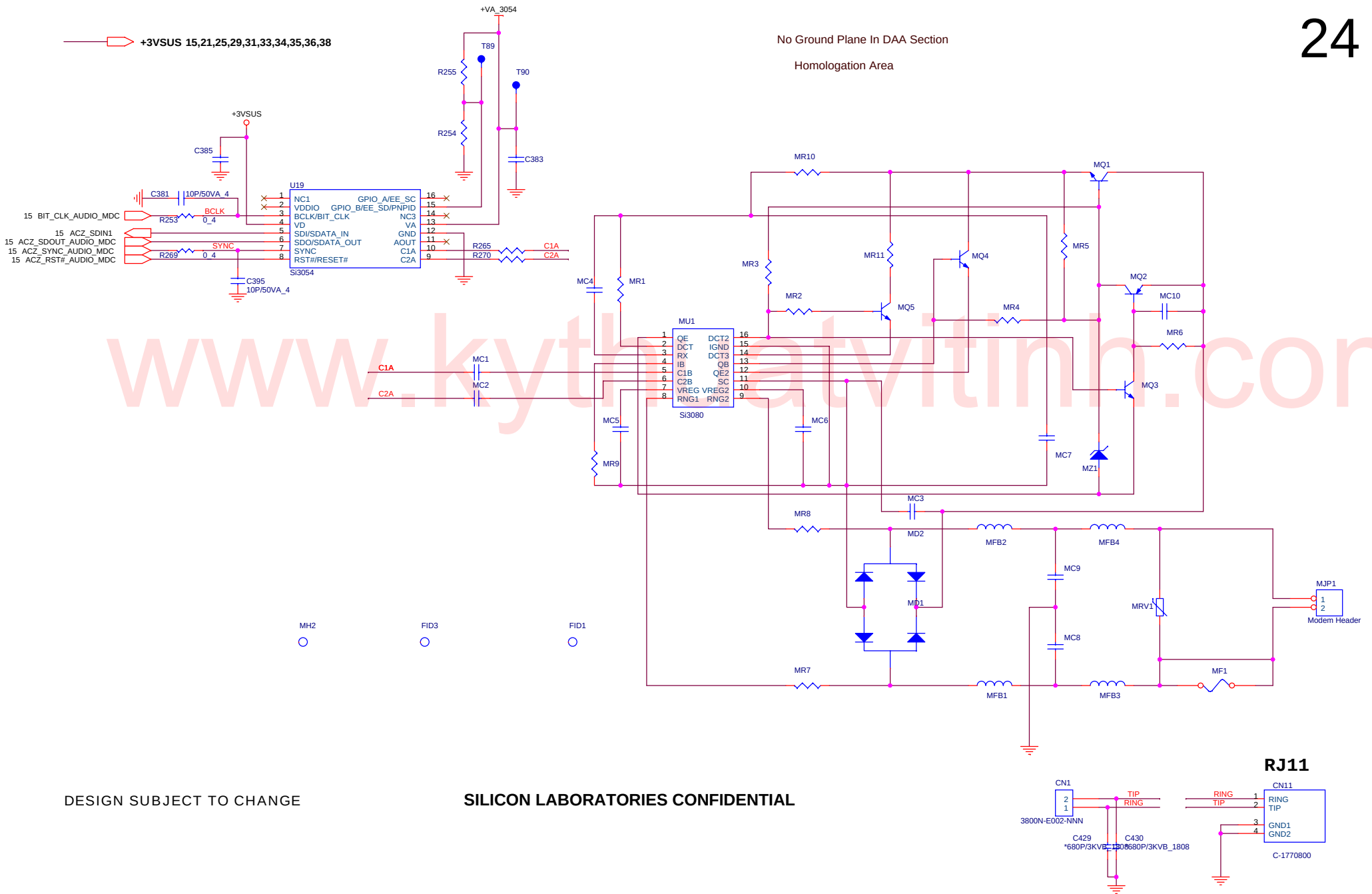


PROJECT : TT9
Quanta Computer Inc.

Size Custom	Document Number JACK/AMP_TAP0312	Rev 1A
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No Ground Plane In DAA Section

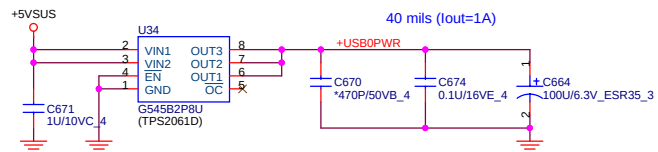
Homologation Area



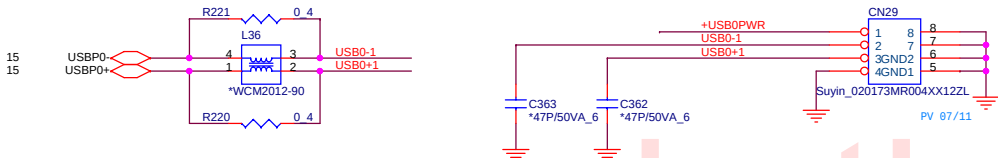
PROJECT : TT9
Quanta Computer Inc.

Size Custom	Document Number MODEM (DAA)	Rev 1A
Date: Wednesday, January 23, 2008		Sheet 24 of 41

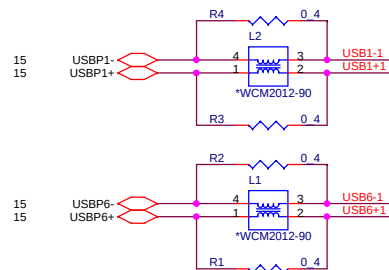
USBX1



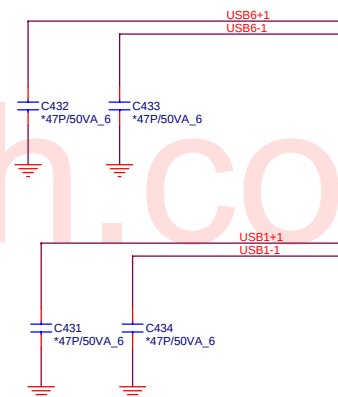
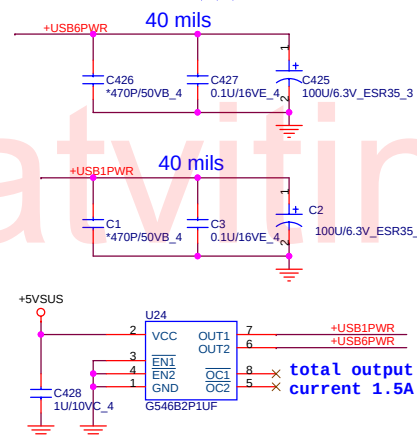
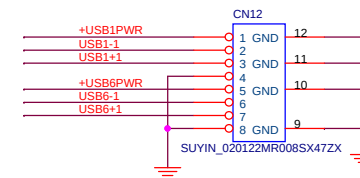
USB 0



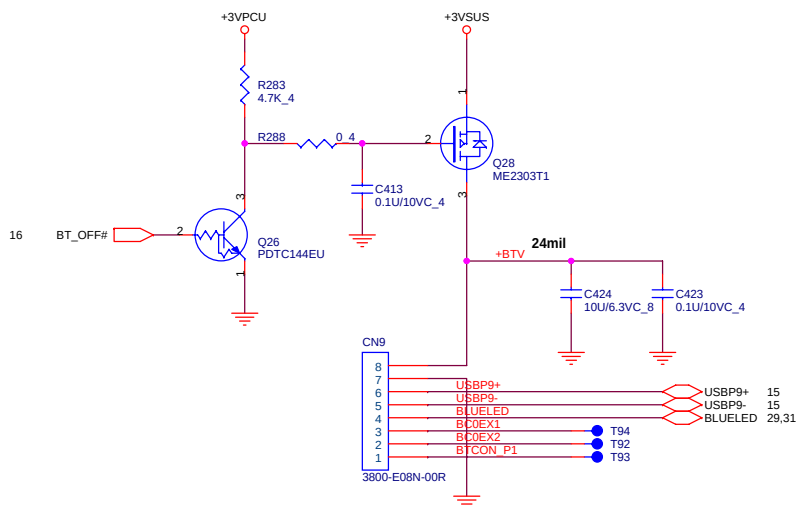
USBX2



USB 1& 6



BLUETOOTH



Select TPM function from HP information

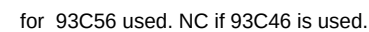
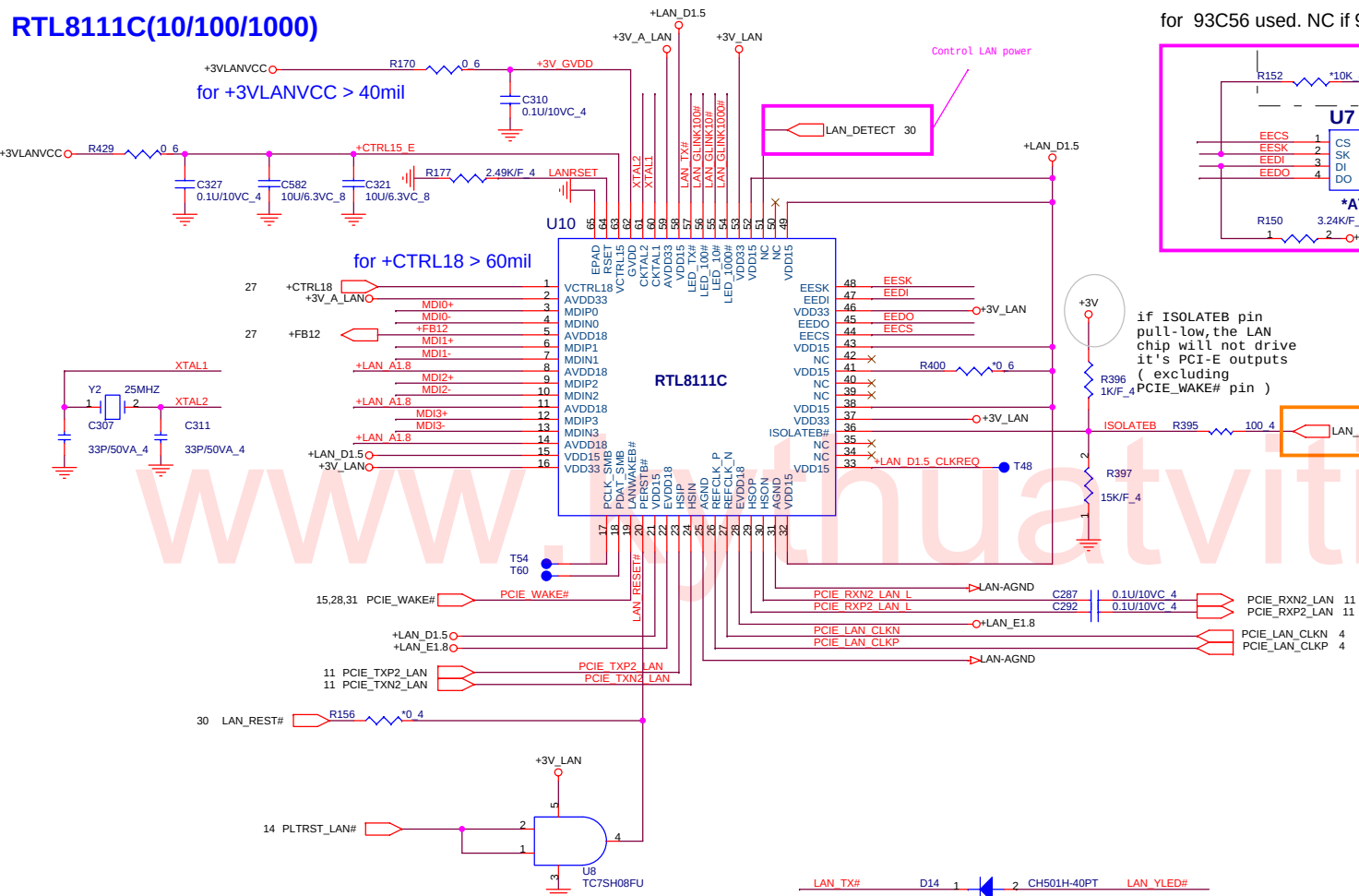
+3VPCU 5,14,19,29,30,32,33,35,37,39
+3VSUS 15,21,24,29,31,33,34,35,36,38
+5VSUS 19,30,32,33,38



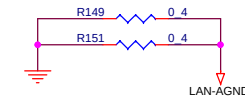
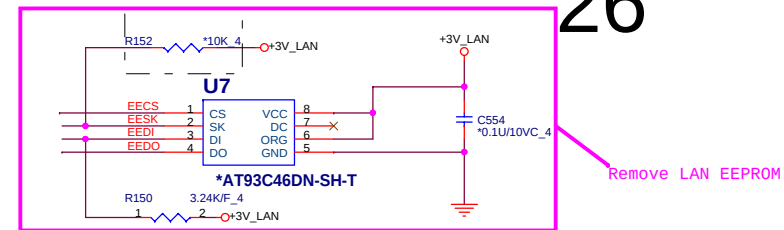
PROJECT : TT9
Quanta Computer Inc.

Size Custom	Document Number Blue Tooth/USBX3	Rev 1A
Date: Wednesday, January 23, 2008	Sheet 25 of 41	

RTL8111C(10/100/1000)

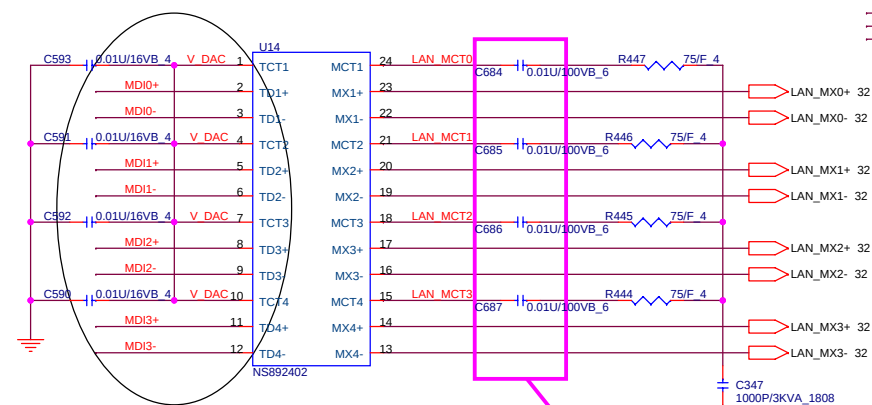


26

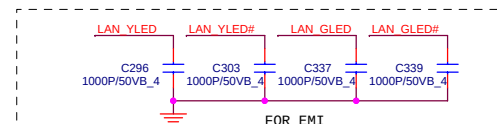
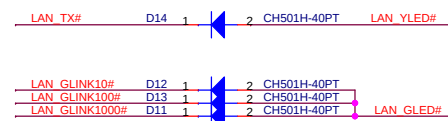


```
if ISOLATEB pin
pull-low, the LAN
chip will not drive
it's PCI-E outputs
( excluding
PCIE_WAKE# pin )
```

PV change from SB to EC control



From HP recommend

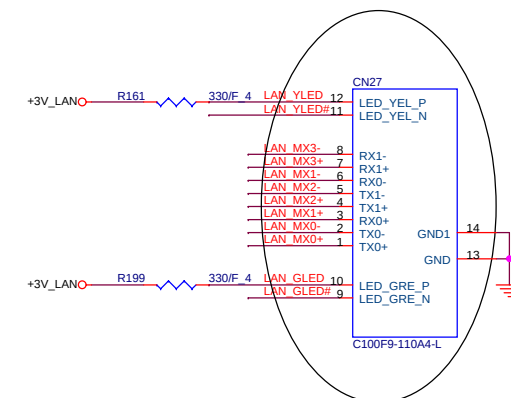


FOR EMI



Diagram showing the pin header connections for the LAN module. The connections are:

- +3V LAN 27
- +3VLANVCC 27,33,38
- LAN_D1.5 27
- LAN_A1.8 27



RJ45



NB5/RD2/HW1

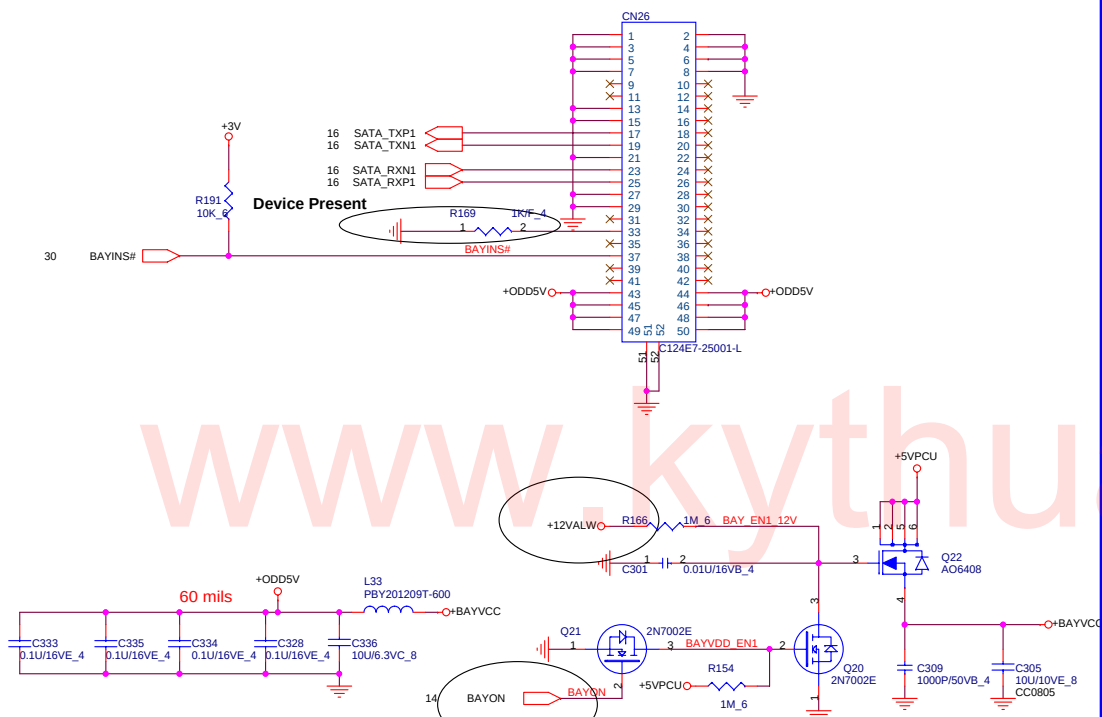
PROJECT : TT9
Quanta Computer Inc.

Size Custom	Document Number Pealtek RTL8111C	Rev 1A
Date: Wednesday, January 23, 2008	Sheet 26 of 41	

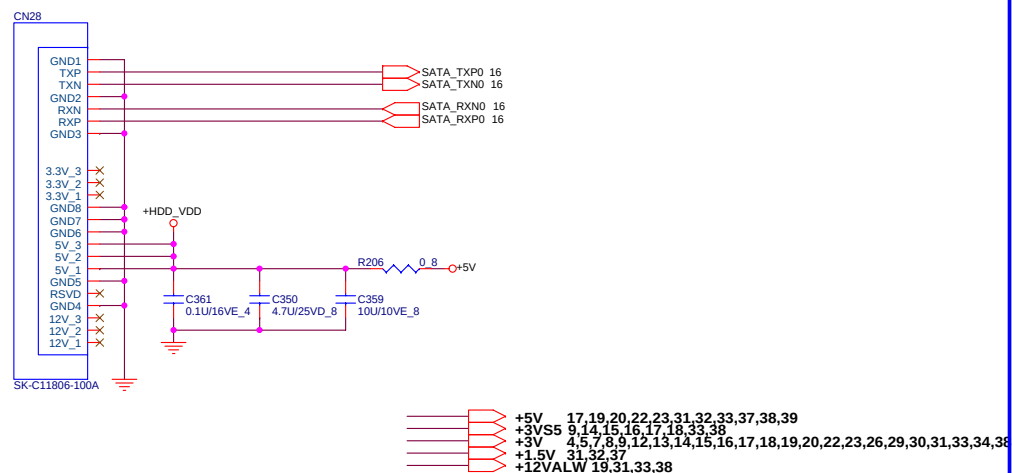


LANVCC	3.3V
LAN_D1.8	1.2V
LAN_A1.8	1.2V
LAN_D1.5	1.2V

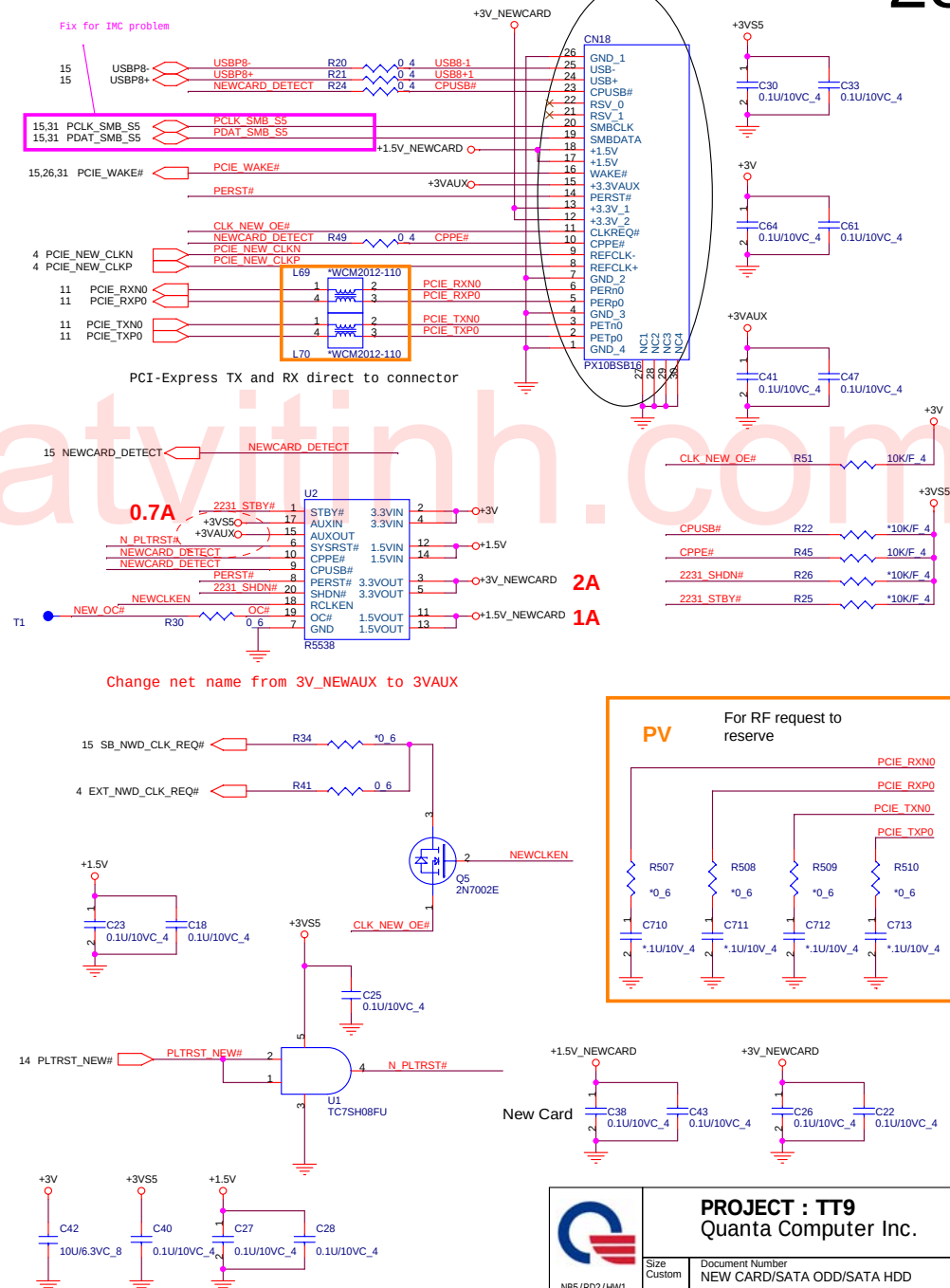
SATA ODD



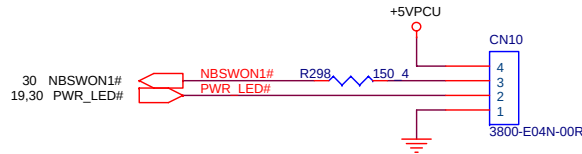
SATA CONNECTOR

**NEWCARD**

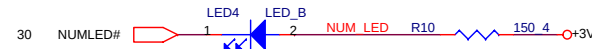
NEWCARD (PCIEXPRESS*1 + USB*1)



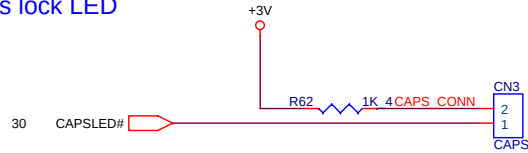
FOR POWER ON SW BOARD



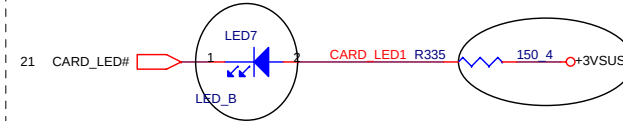
Num lock LED



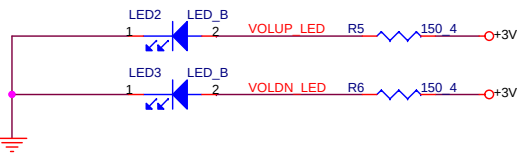
Caps lock LED



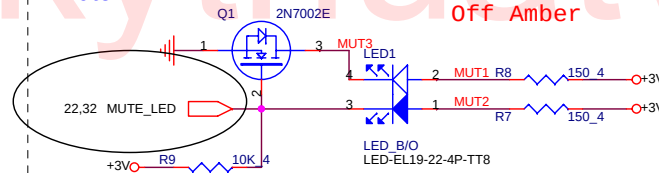
Card Reader LED



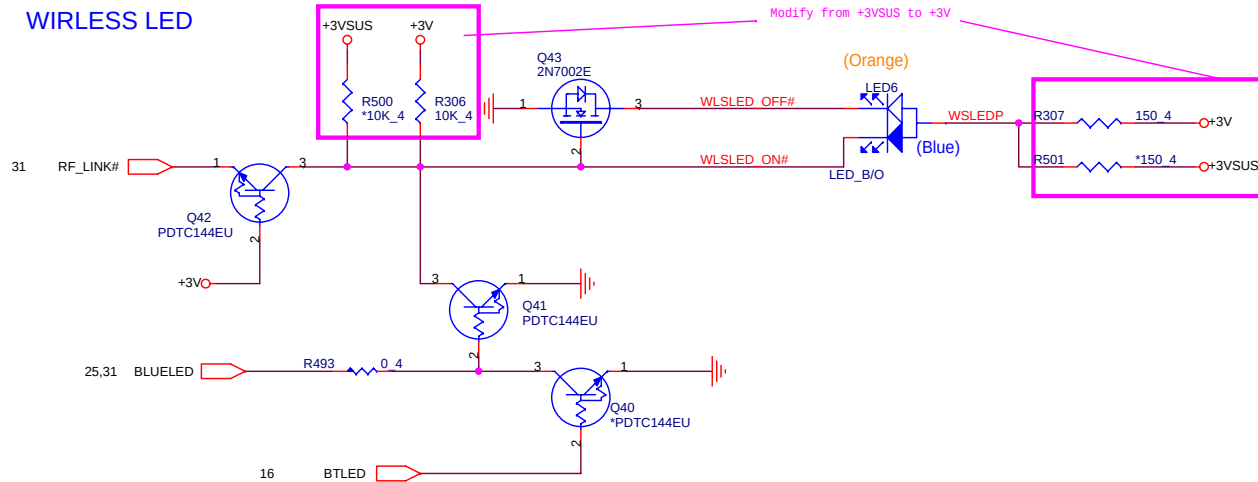
Volume up/down LED



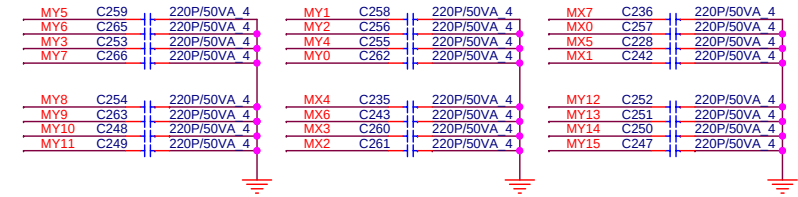
Mute LED



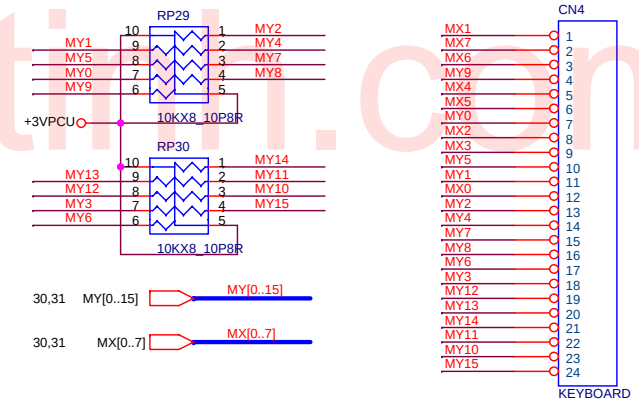
WIRELESS LED



Keyboard



KEYBOARD PULL-UP




 +5VPCU 19,22,28,30,33,34,35,36,37

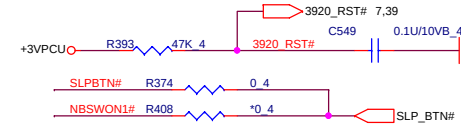
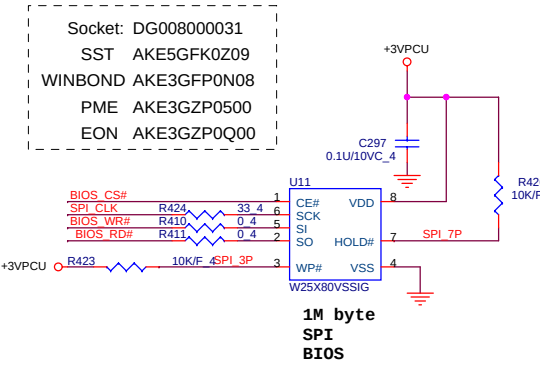
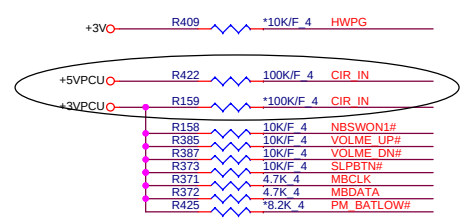
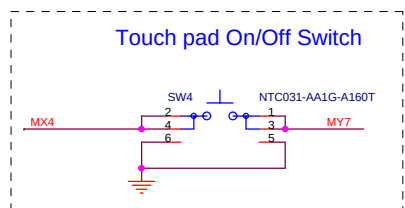
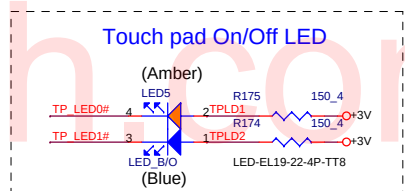
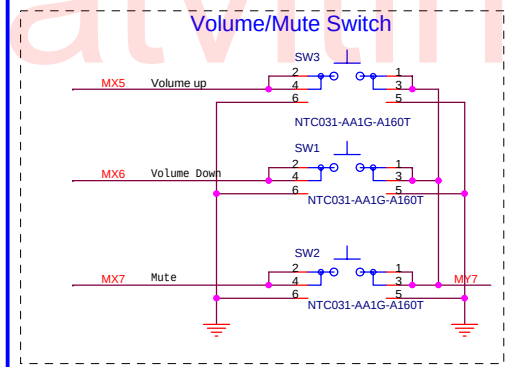
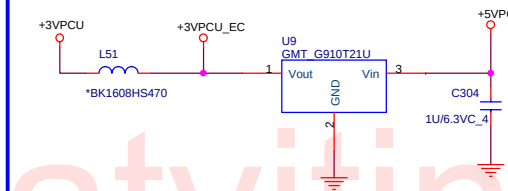
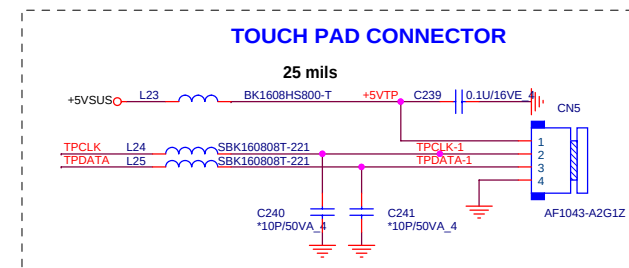
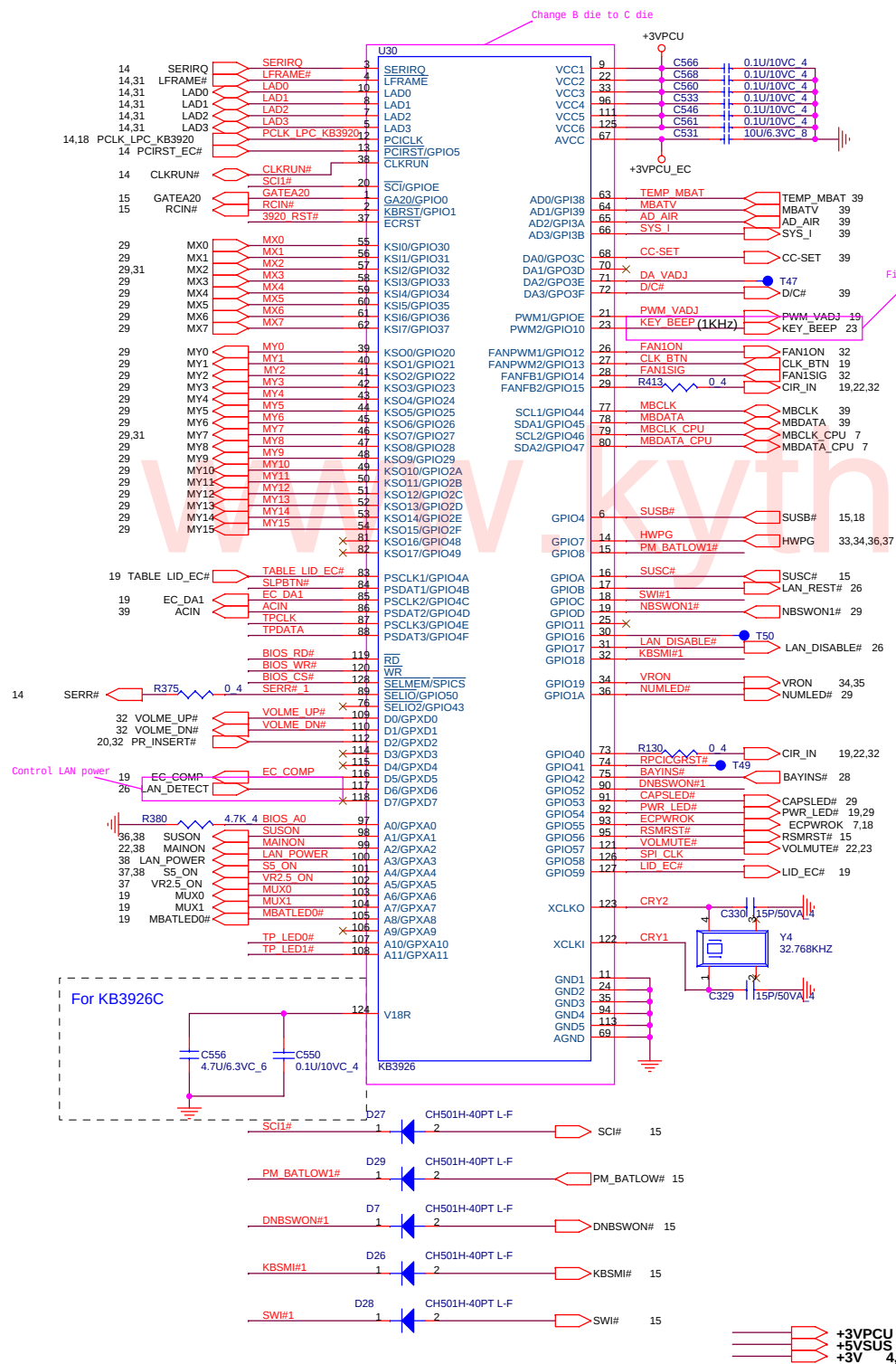
 +3V 4,5,7,8,9,12,13,14,15,16,17,18,19,20,22,23,26,28,30,31,33,34,38

 +3VSUS 15,21,24,25,31,33,34,35,36,38



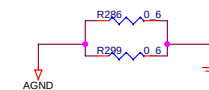
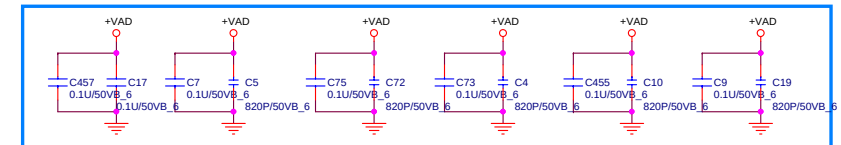
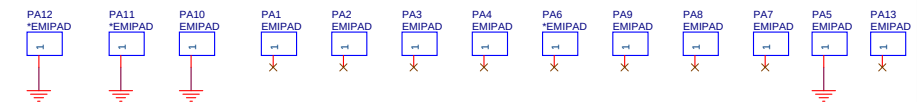
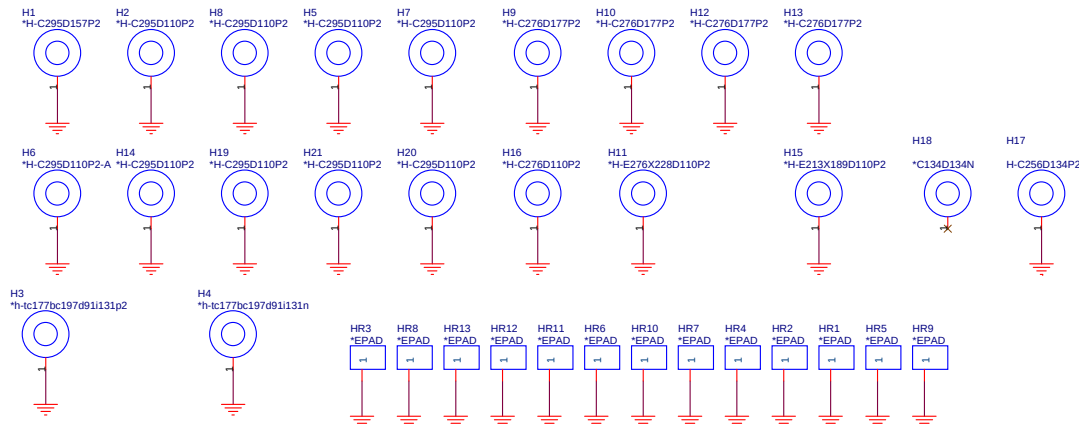
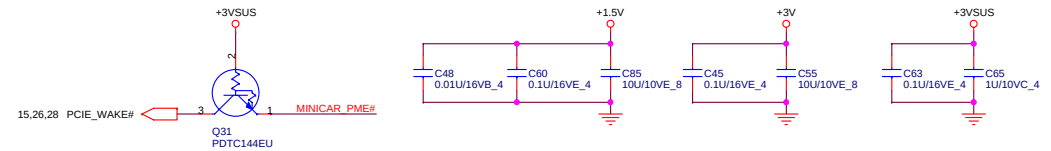
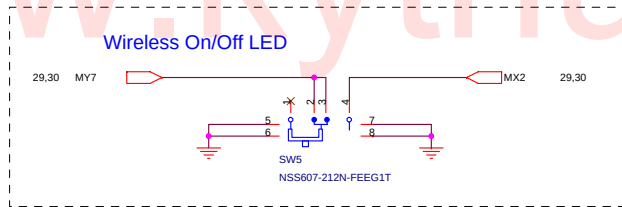
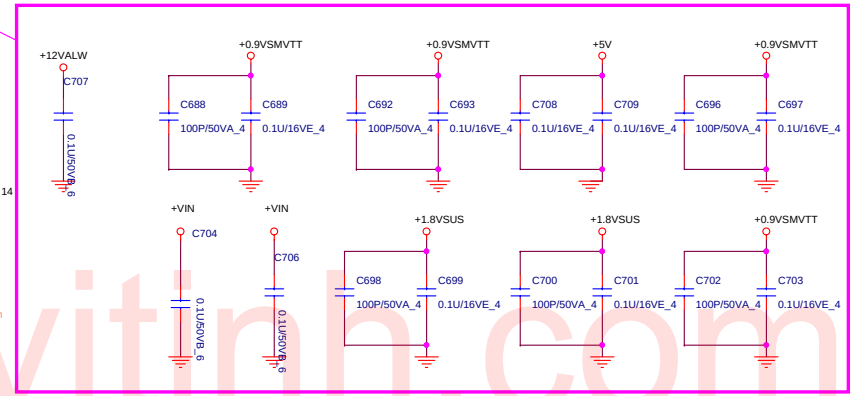
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Quanta Computer Inc.

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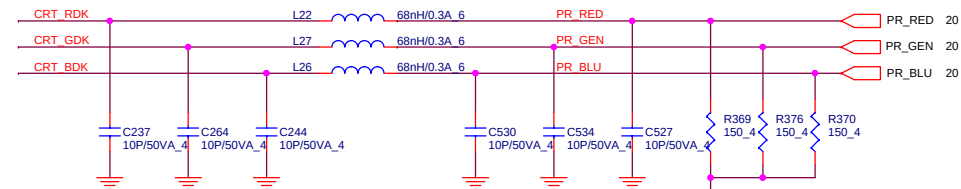
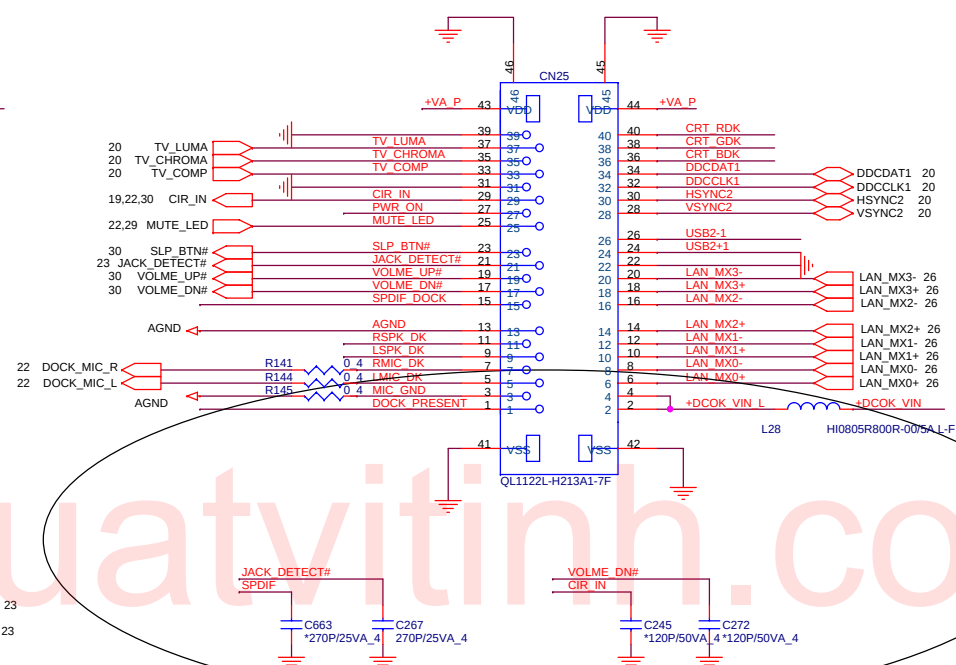
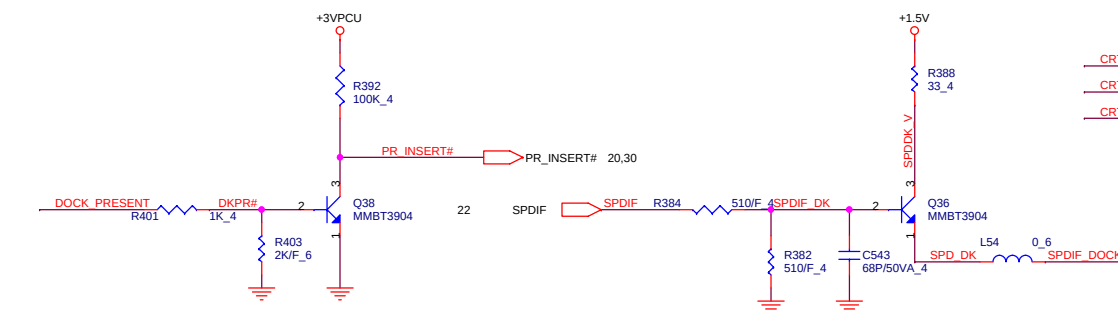
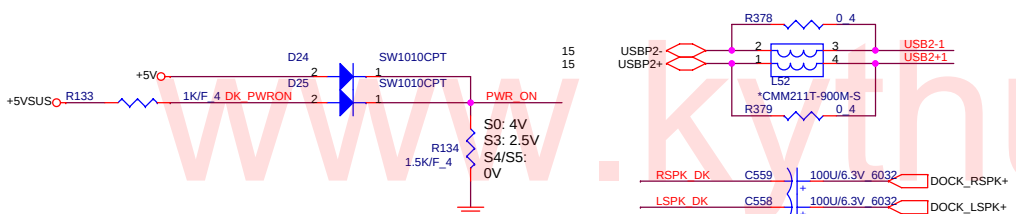
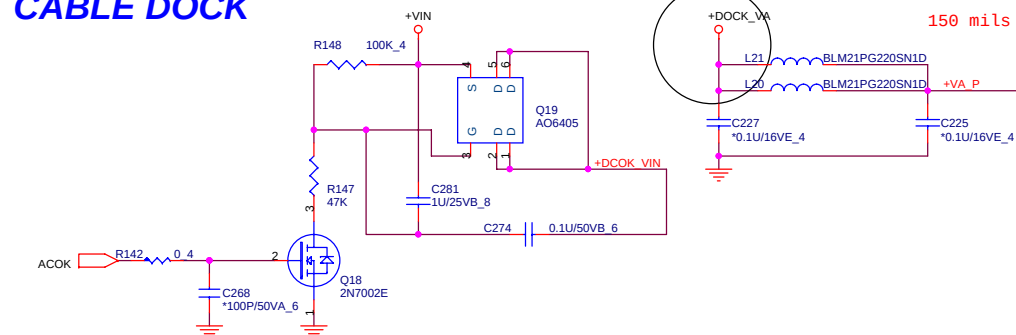
The diagrams illustrate different capacitor placement strategies for a 50V load:

- Diagram 1:** A series capacitor C52 (0.1u/50VB_6) is placed before the load C51 (820P/50VB_6).
- Diagram 2:** A shunt capacitor C21 (0.1u/50VB_6) is placed before the load C20 (820P/50VB_6).
- Diagram 3:** A shunt capacitor C54 (0.1u/50VB_6) is placed before the load C37 (820P/50VB_6).
- Diagram 4:** A shunt capacitor C451 (0.1u/50VB_6) is placed before the load C452 (820P/50VB_6).
- Diagram 5:** A shunt capacitor C36 (0.1u/50VB_6) is placed before the load C53 (820P/50VB_6).

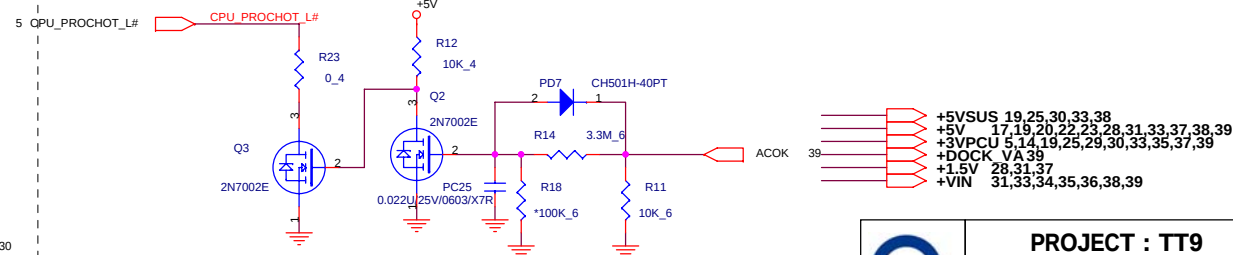
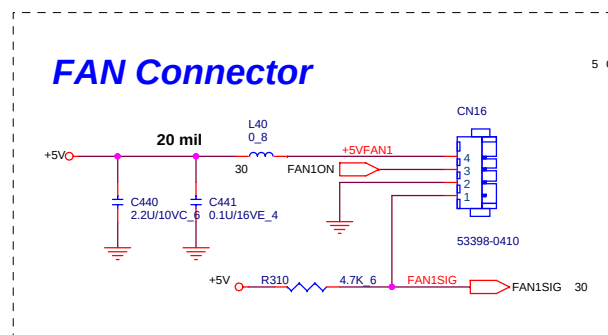


CABLE DOCK

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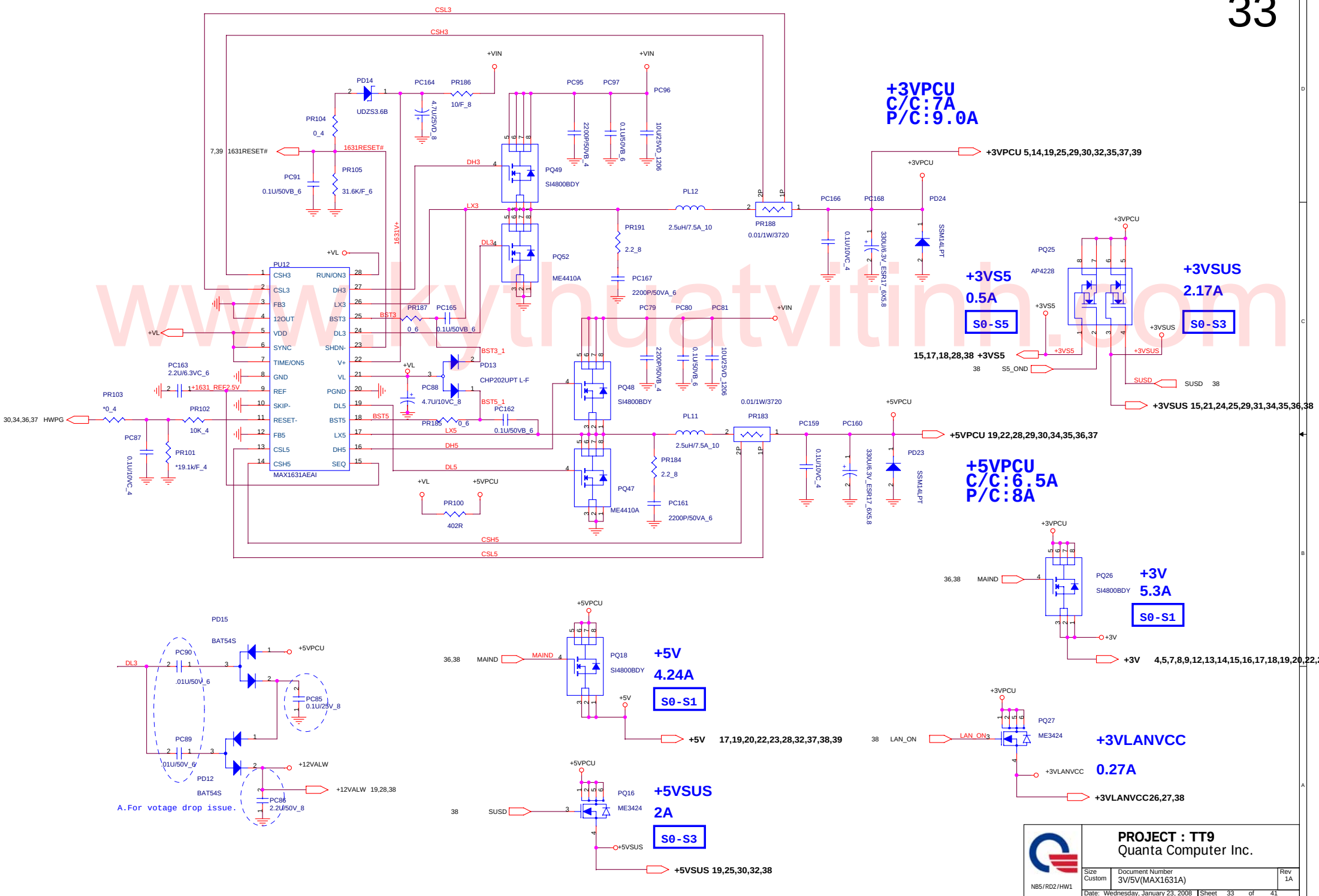
FAN Connector



NB5/RD2/HW1

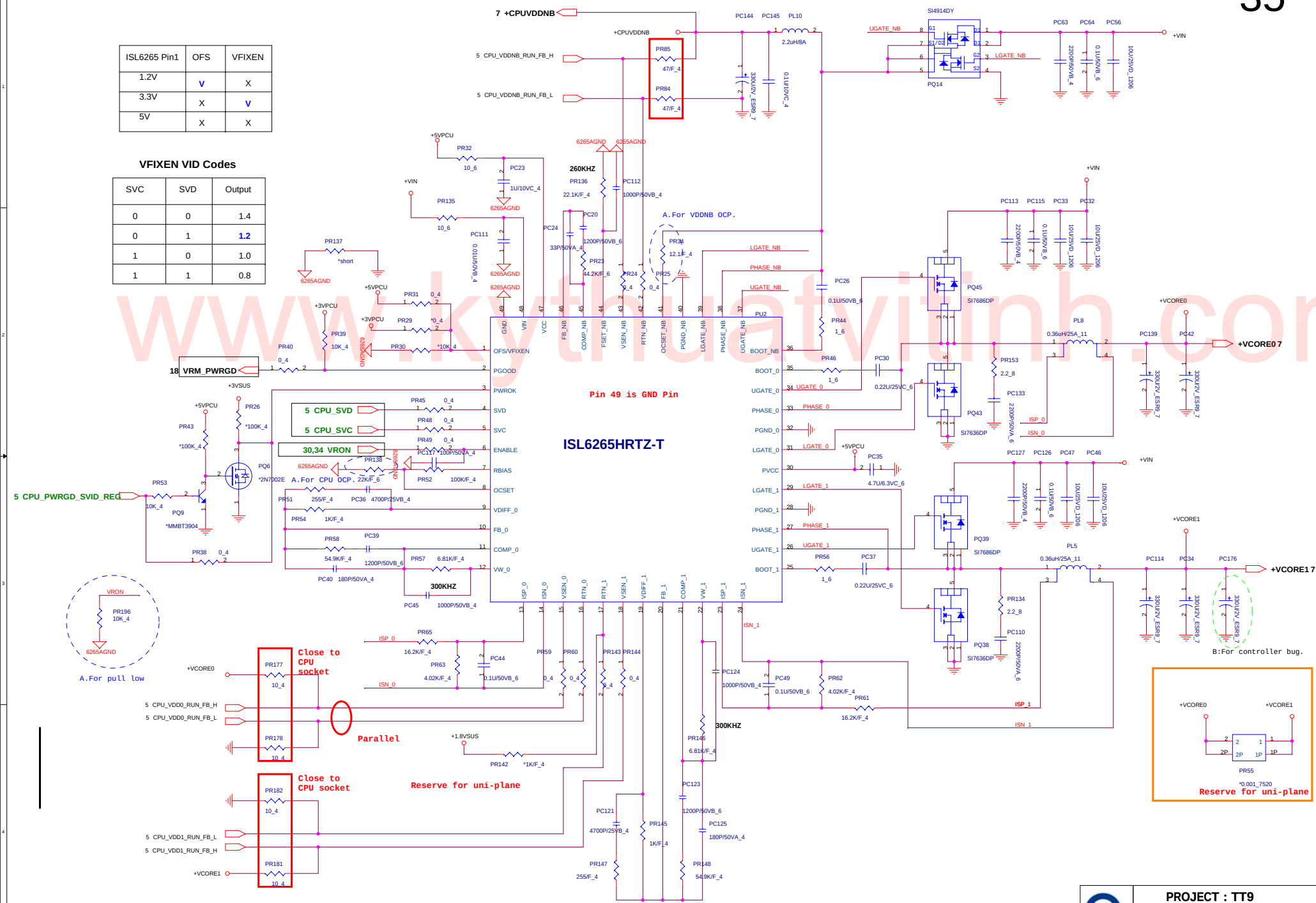
PROJECT : TT9
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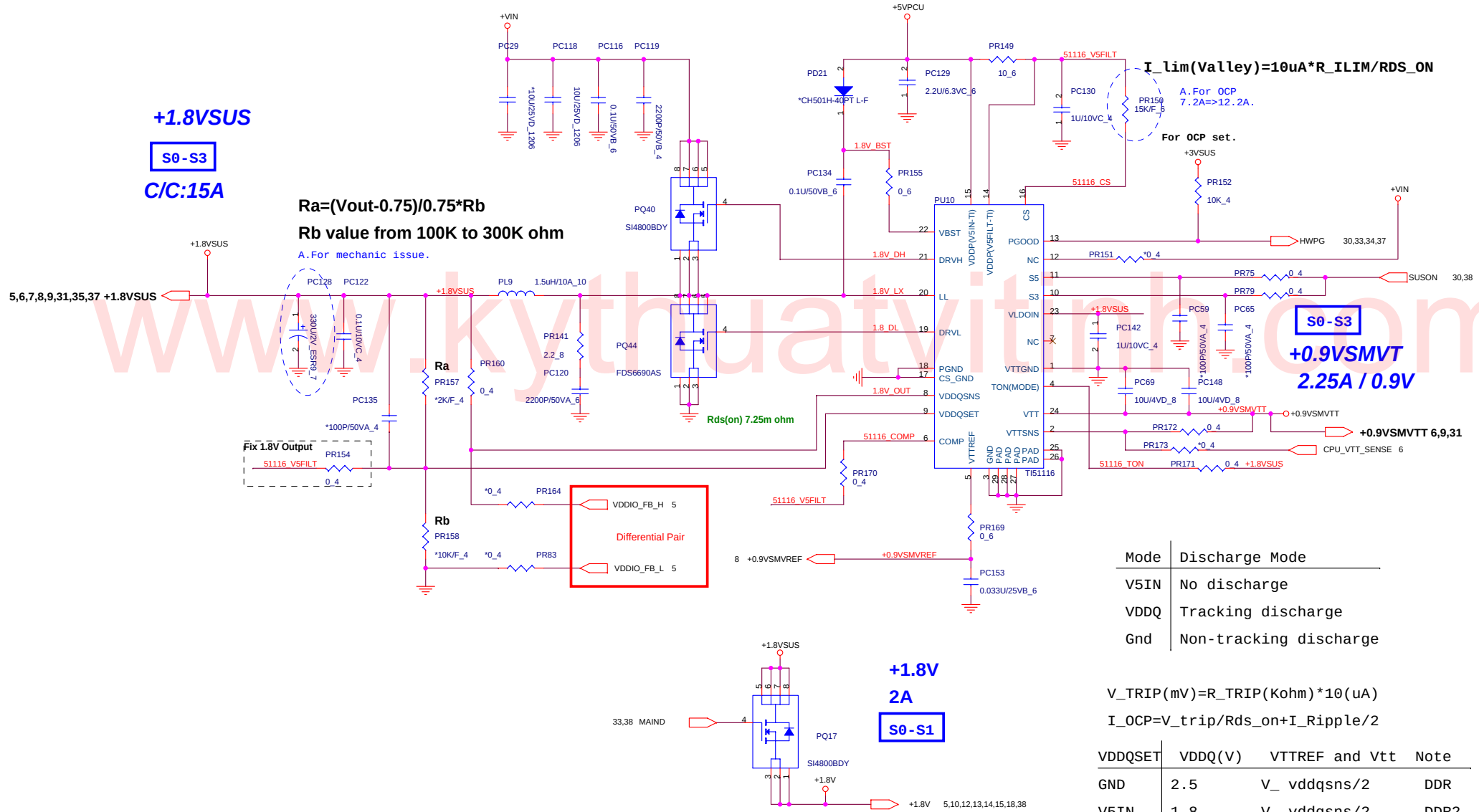
Size Custom	Document Number CABLE DOCKING	Rev 1A
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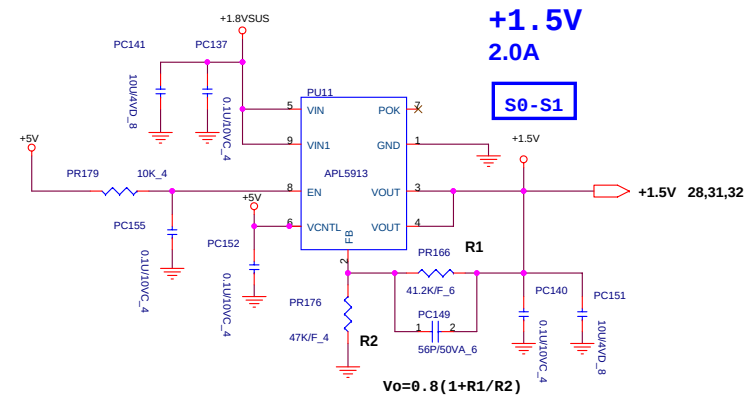
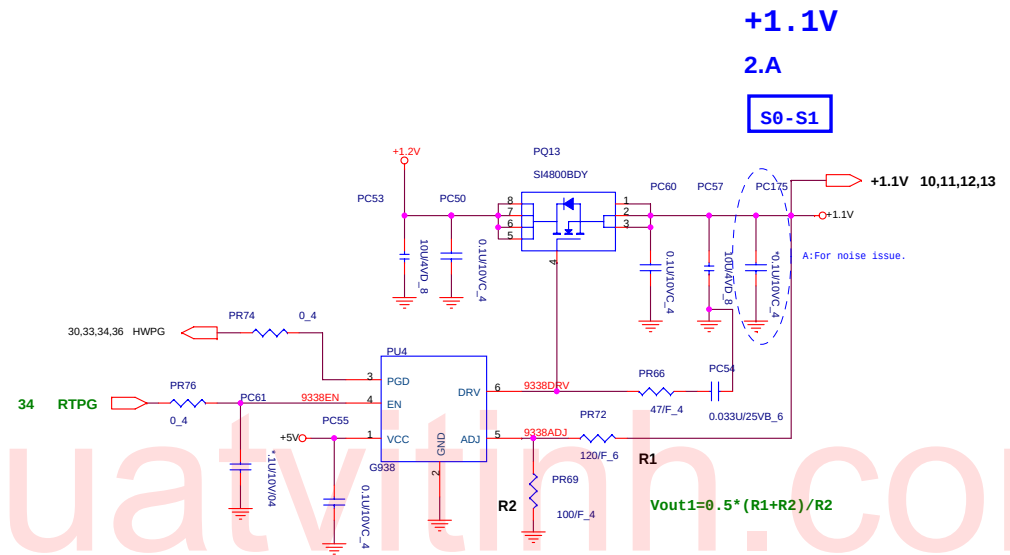
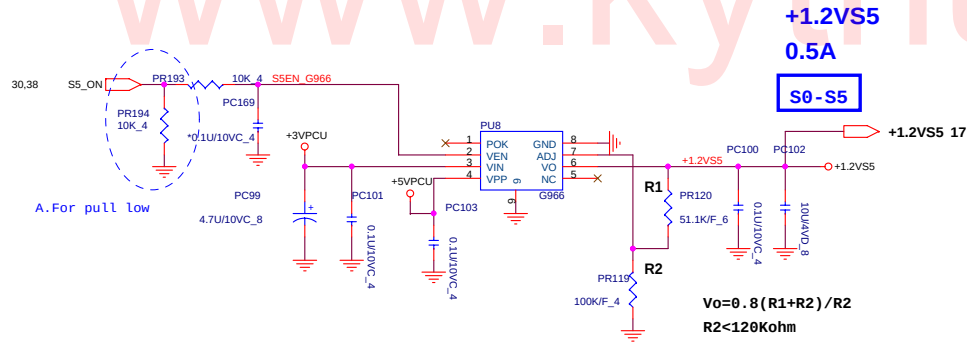
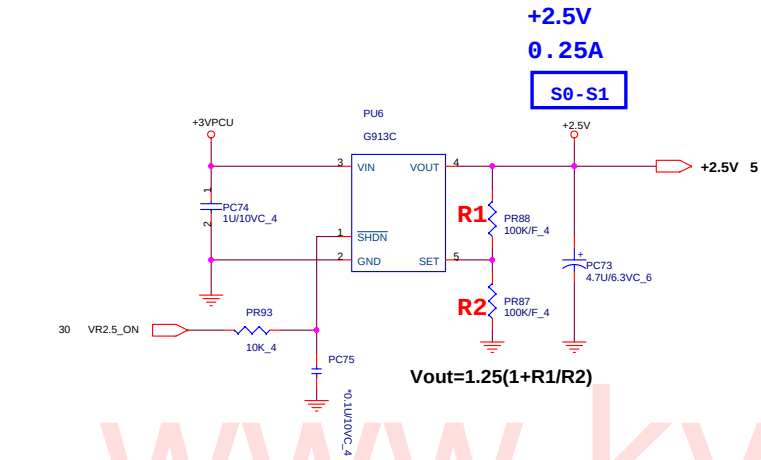




SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

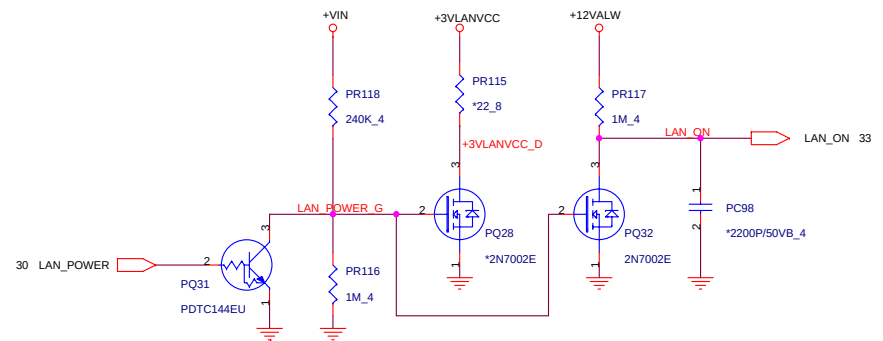
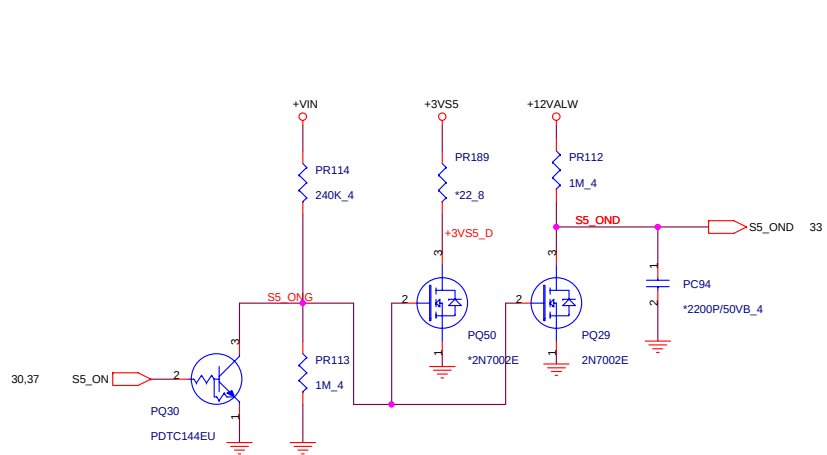
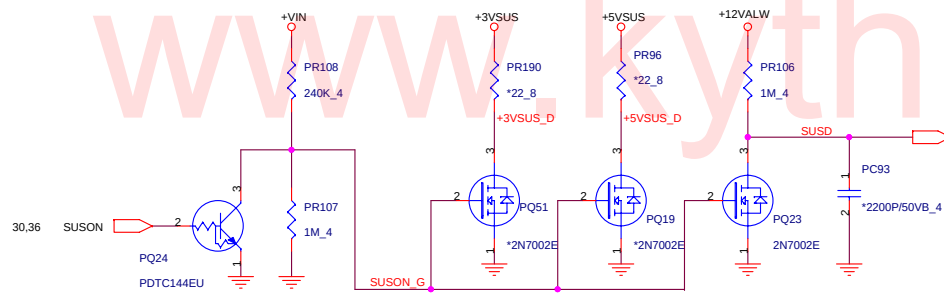
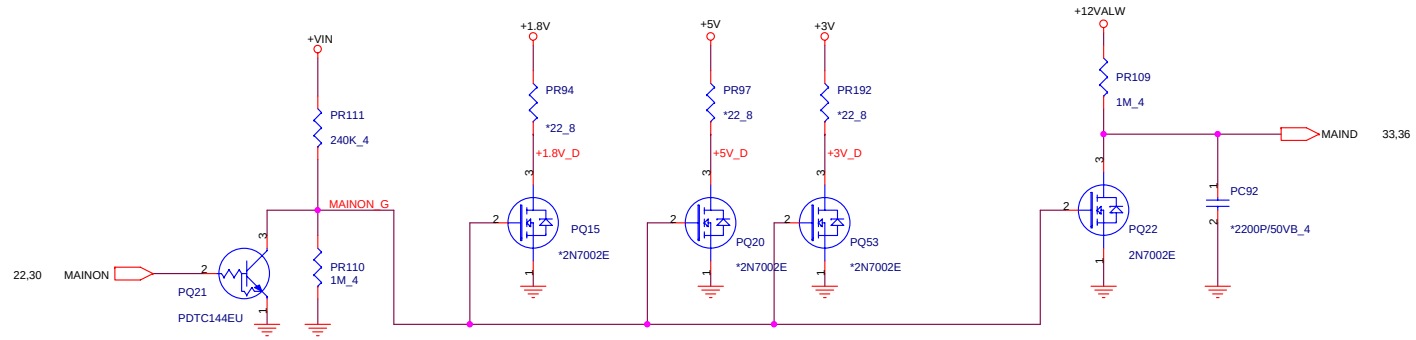






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Charge current:
4 & 6 cell =>3A
8 cell =>3.5A

