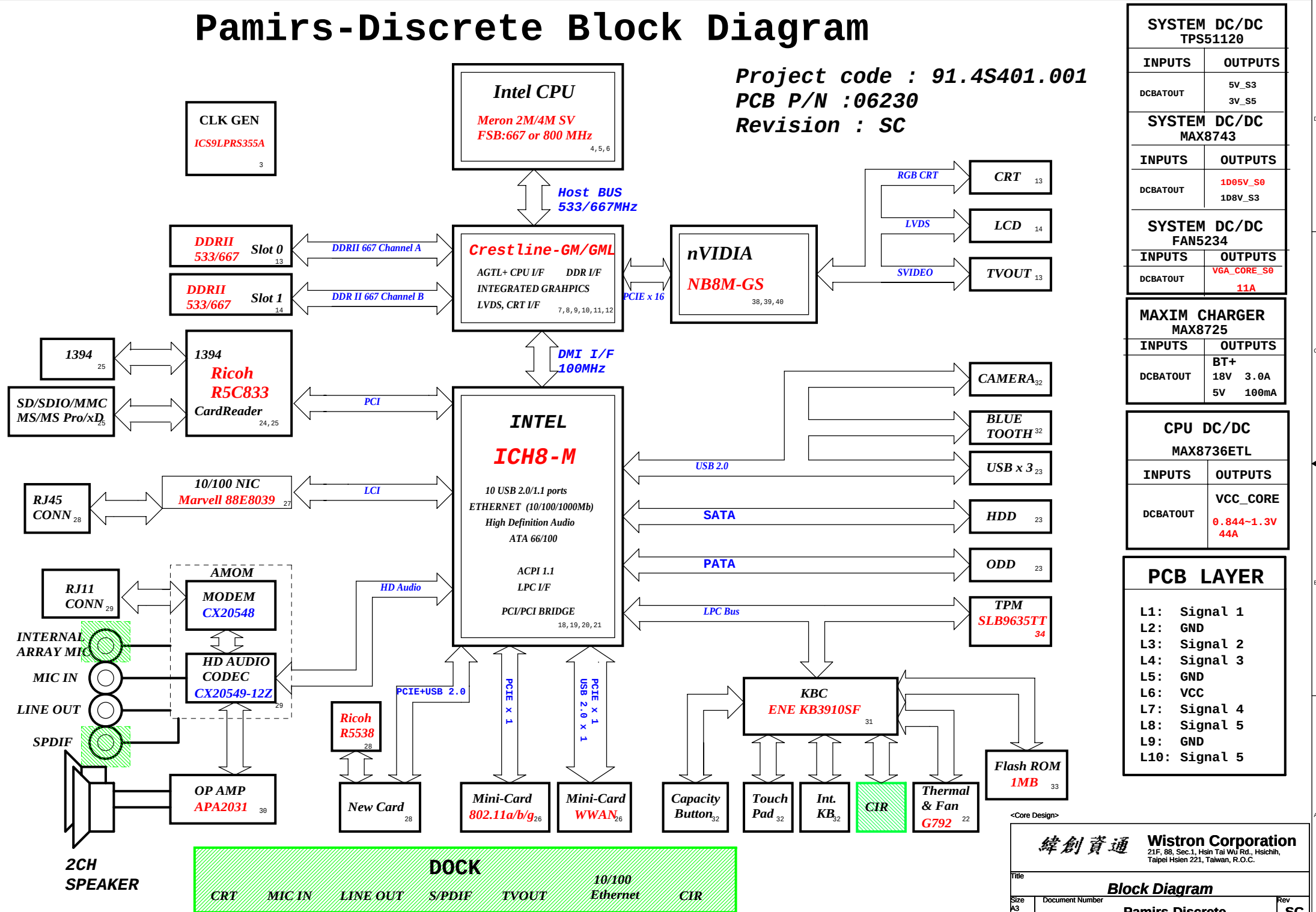


Pamirs-Discrete Block Diagram

Project code : 91.4S401.001
PCB P/N :06230
Revision : SC



SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S5
SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
SYSTEM DC/DC FAN5234	
INPUTS	OUTPUTS
DCBATOUT	V6A_CORE_S0 11A

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC	
MAX8736ETL	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	GND
L6:	VCC
L7:	Signal 4
L8:	Signal 5
L9:	GND
L10:	Signal 5

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config 1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIe Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIe Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPI020	Reserved	Weak Internal PULL-DOWN. NOTE: This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h: bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05, VccCL1_05 VRM when sampled high
SATALED#	PCIe LAN REVERSAL. Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit. (Offset: 3410h: bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPI033/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up. If sampled low, the Flash Descriptor Security will be overridden. If high, the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap			
ICH_RSVD_P3	AZ_DOUT_ICH	Description	
0	0	RSVD	
0	1	Enter XOR Chain	
1	0	Normal Operation (default)	
1	1	Set PCIe port config bit1	

A16 swap override strap	
PCT_GNT3#	low = A16 swap override enable high = default

BOOT BIOS Strap		
PCI_GNT0#	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCT
1	1	LPC (Default)

Integrated VccSus1_05, VccSus1_5, VccCL1_5	
SM_INTVRMEN	High=Enable Low=Disable
Integrated VccLAN1_05 VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

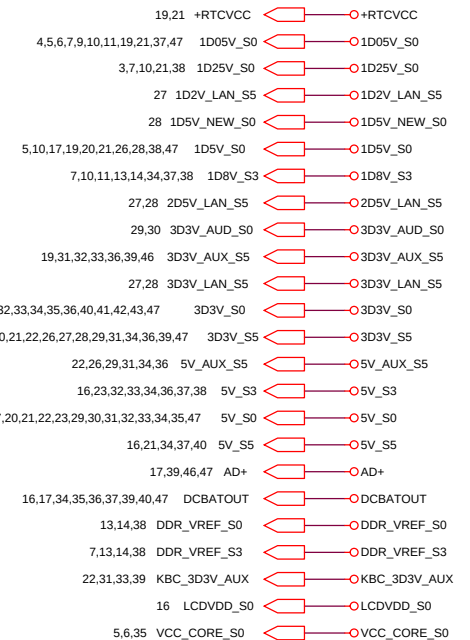
DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Default High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPI0[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPI023	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

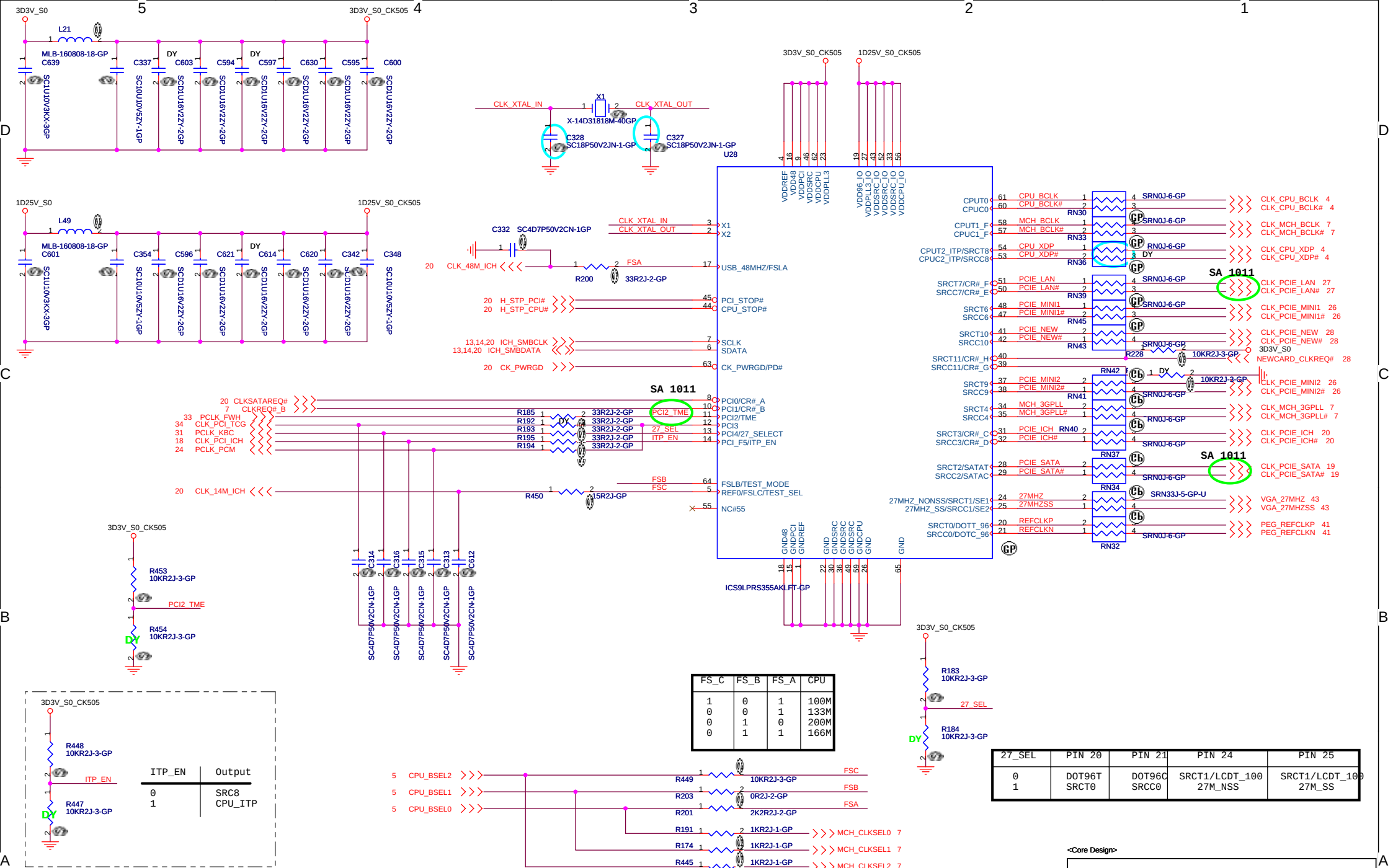


INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5		
CFG 8	DMI X 2	DMI X 4 ★
CFG 9	Low Power PCI Express	Normal ★ Low Power mode
CFG 9	PCI Express Graphics Lane Reversal	Lane Reversal
CFG 16	FSB Dynamic ODT	Disabled
CFG 19	DMI Lane Reserved	Enabled ★
CFG 20	Normal Operation ★	Reserved Lane
CFG 20	Only PCIe or SDVO is operation ★	PCIe and SDVO are operation simultaneous
SDVO_CTRL_DATA	NO SDVO Card Present ★	SDVO Card Present
CFG 12	XOR/ALL-Z	
CFG 13		
LL(00)	Reserved	
LH(01)	XOR Mode Enabled	
HL(10)	ALL Z Mode Enabled	
HH(11)	Normal Operation	

<Core Design>

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Title		
Table of Content		
Size A3	Document Number	Rev
Pamirs-Discrete		SA
Date: Wednesday, November 01, 2006	Sheet 2	of 47



Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function is enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

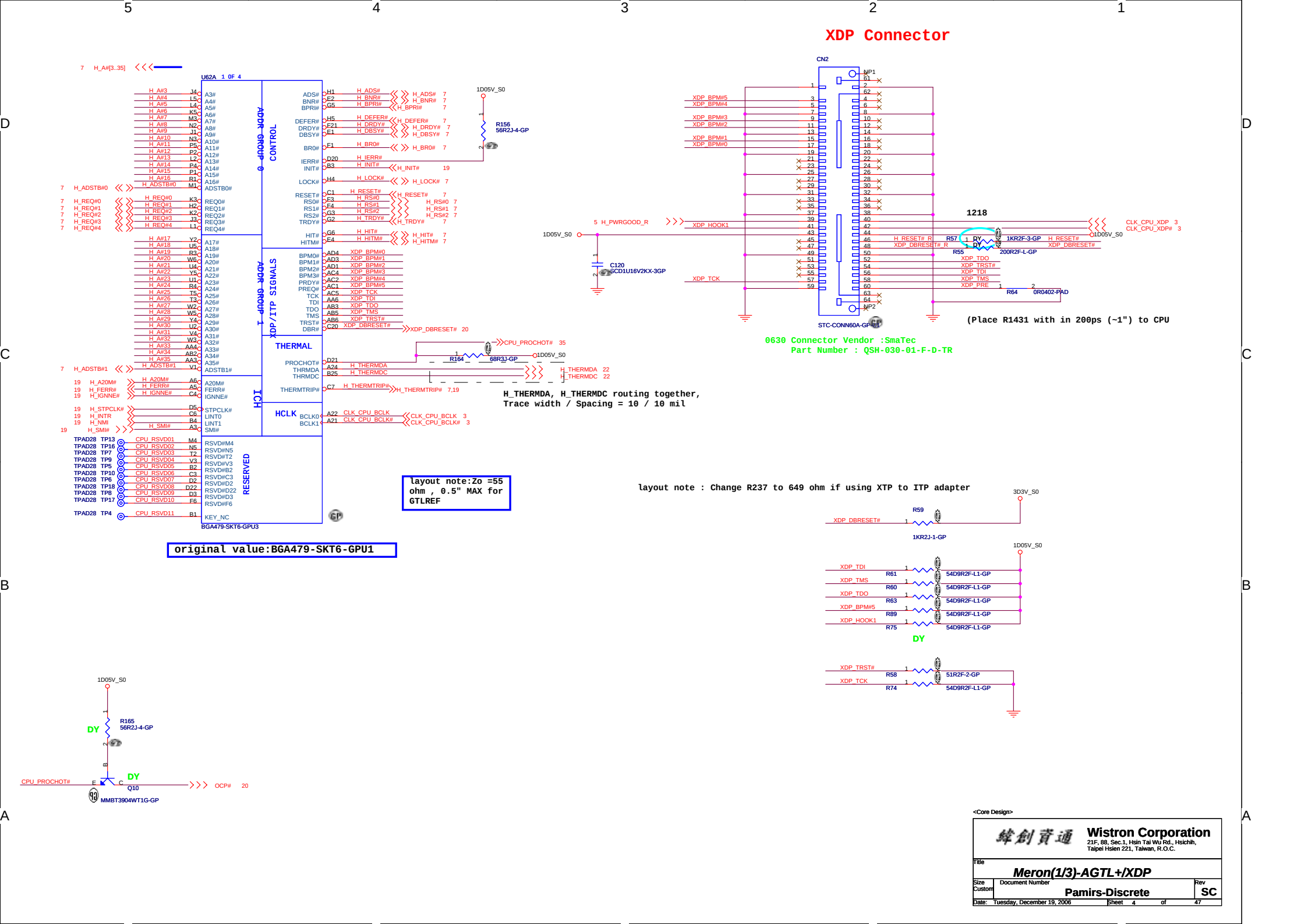
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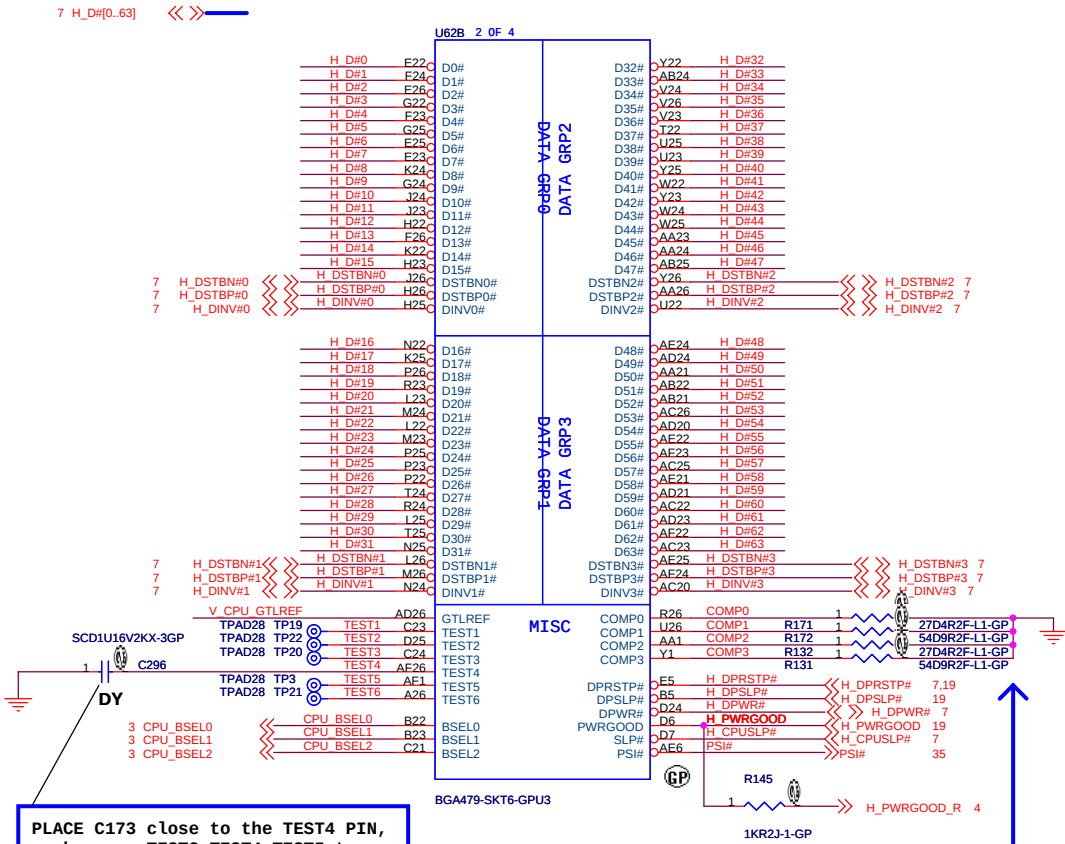
緯創資通 Wistron Corporation
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Title: **Clock generator CY28548**

Size A3	Document Number	Rev
	Pamirs-Discrete	SC

Date: Tuesday, December 19, 2006 Sheet 3 of 47



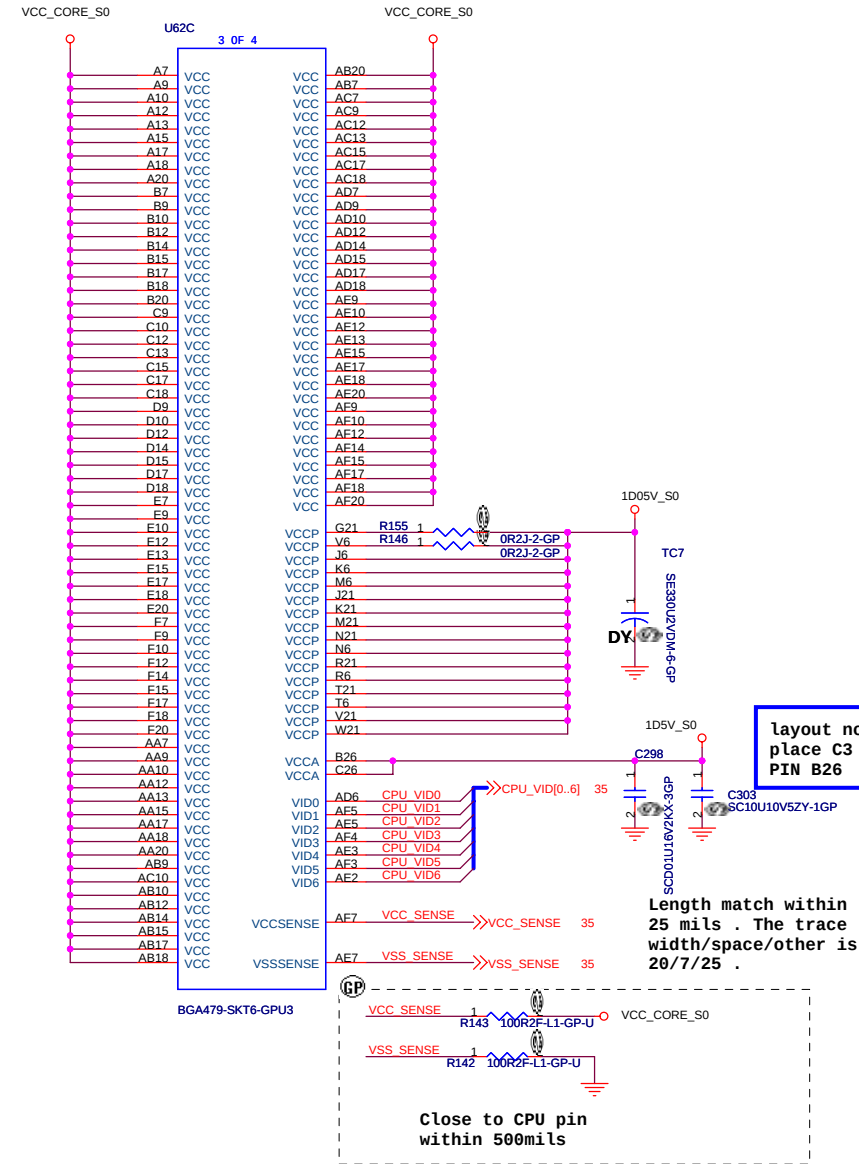
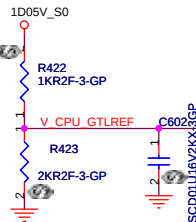


PLACE C173 close to the TEST4 PIN, make sure TEST3,TEST4,TEST5 trace routing is reference to GND and away other noisy signals

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

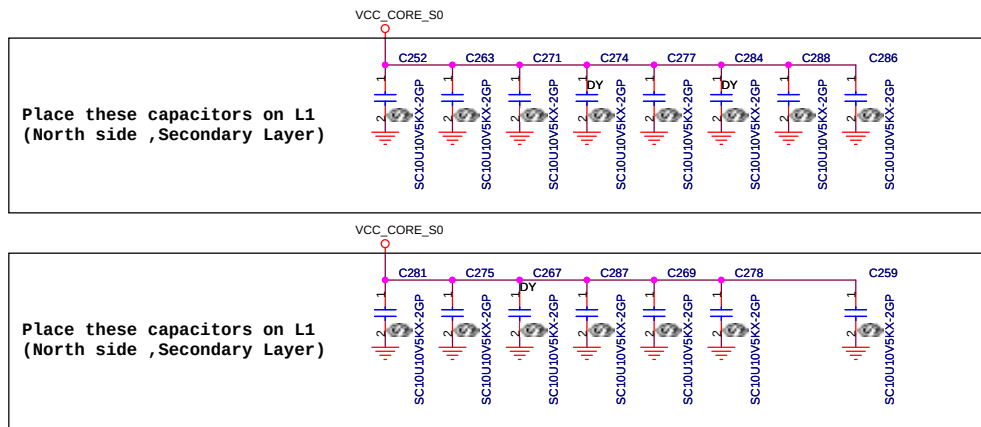
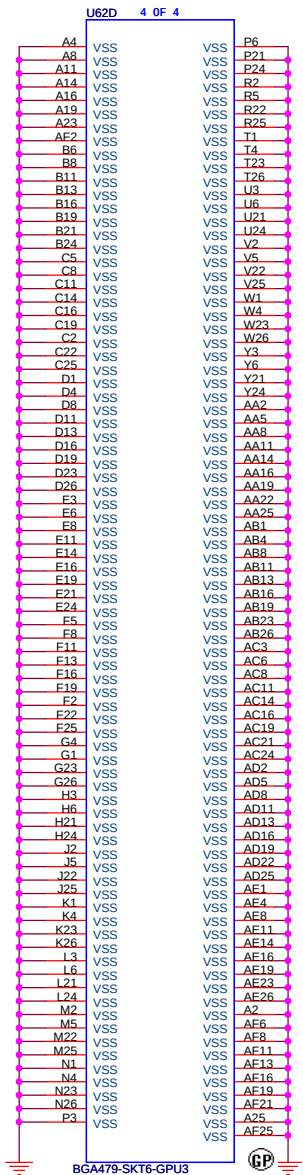
Resistor Placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Close to CPU pin AD26
Z0=55 ohm
with in 500mils.

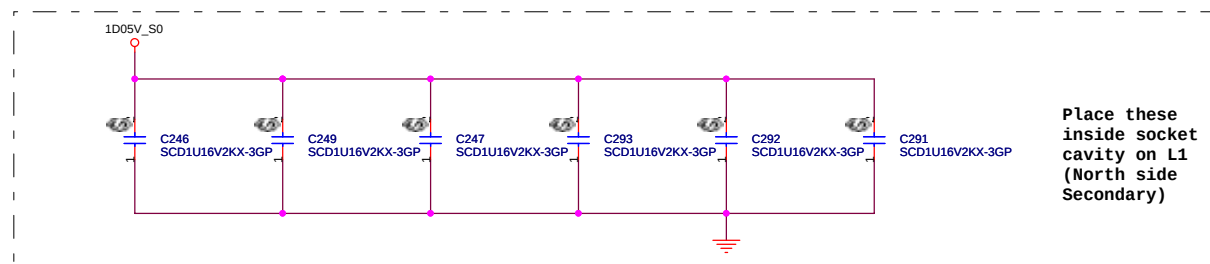


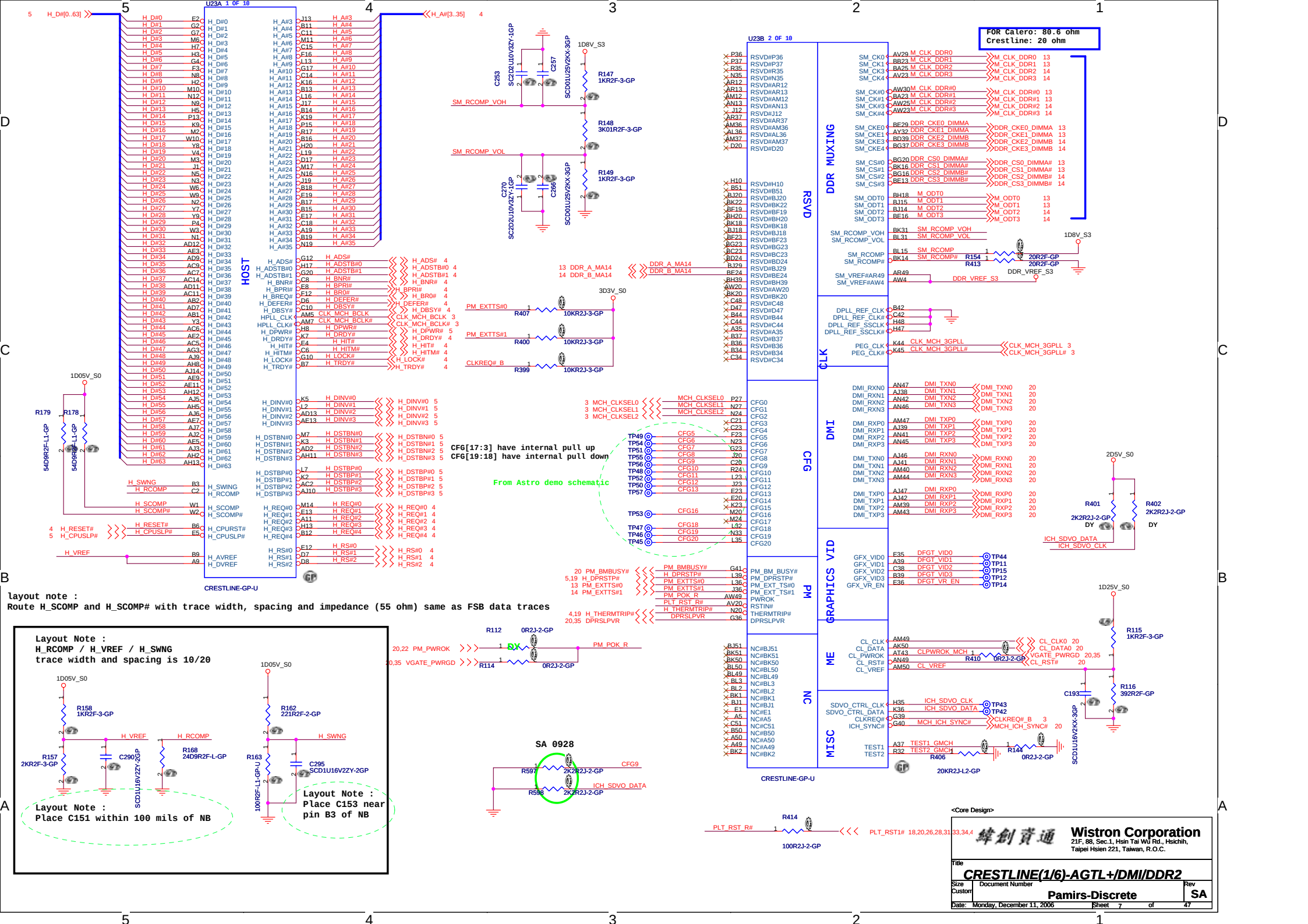
layout note:
place C3 near
PIN B26

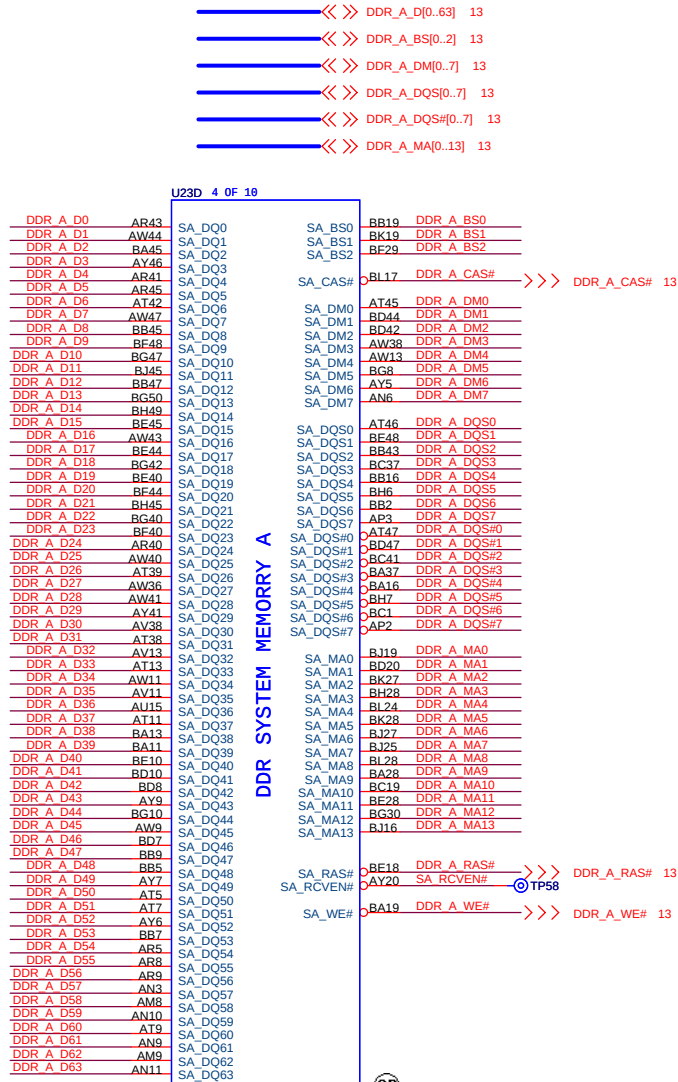
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Mid Freqencd Decoupling



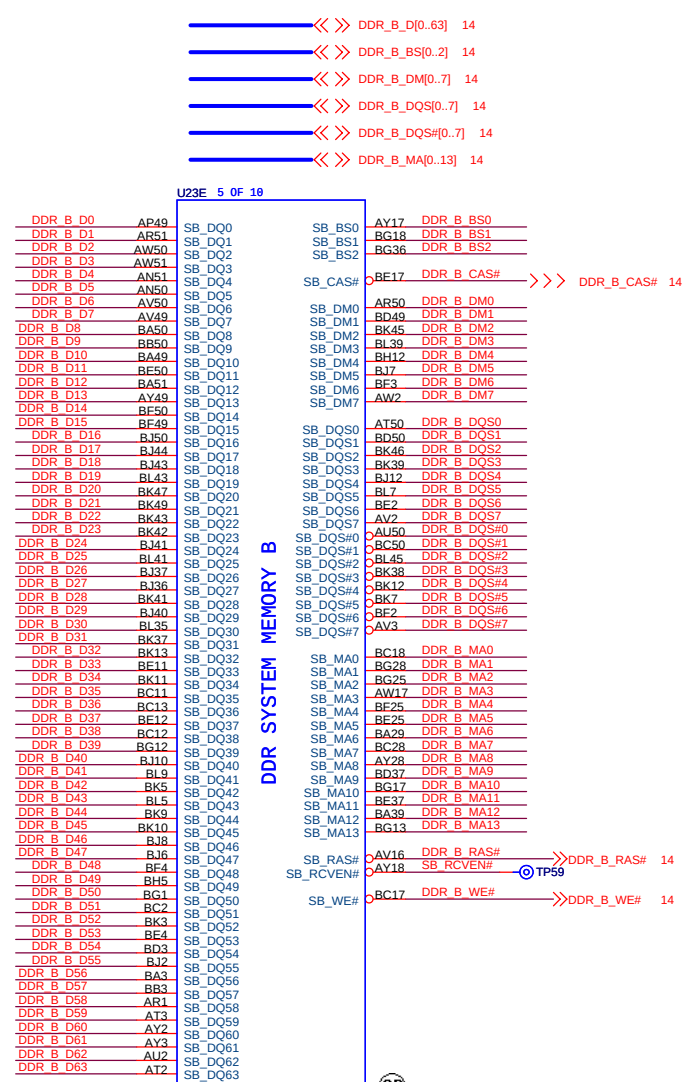




U23D 4 OF 10

DDR SYSTEM MEMORY A

CRESTLINE-GP-U

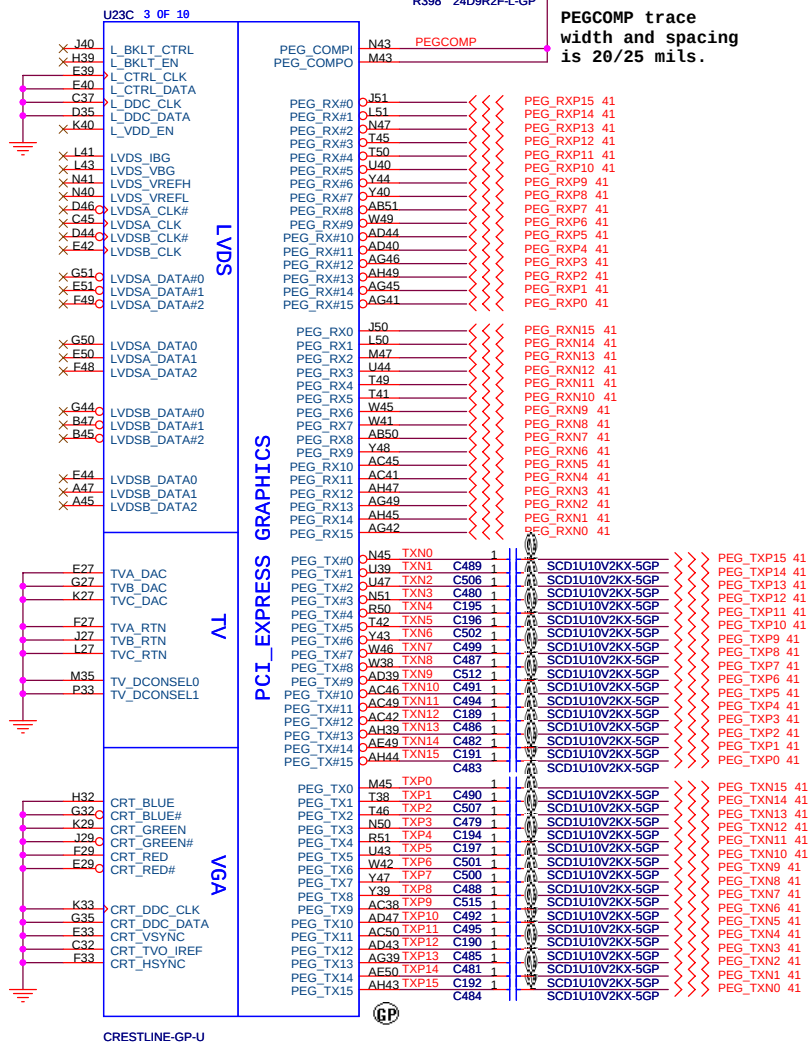


U23E 5 OF 10

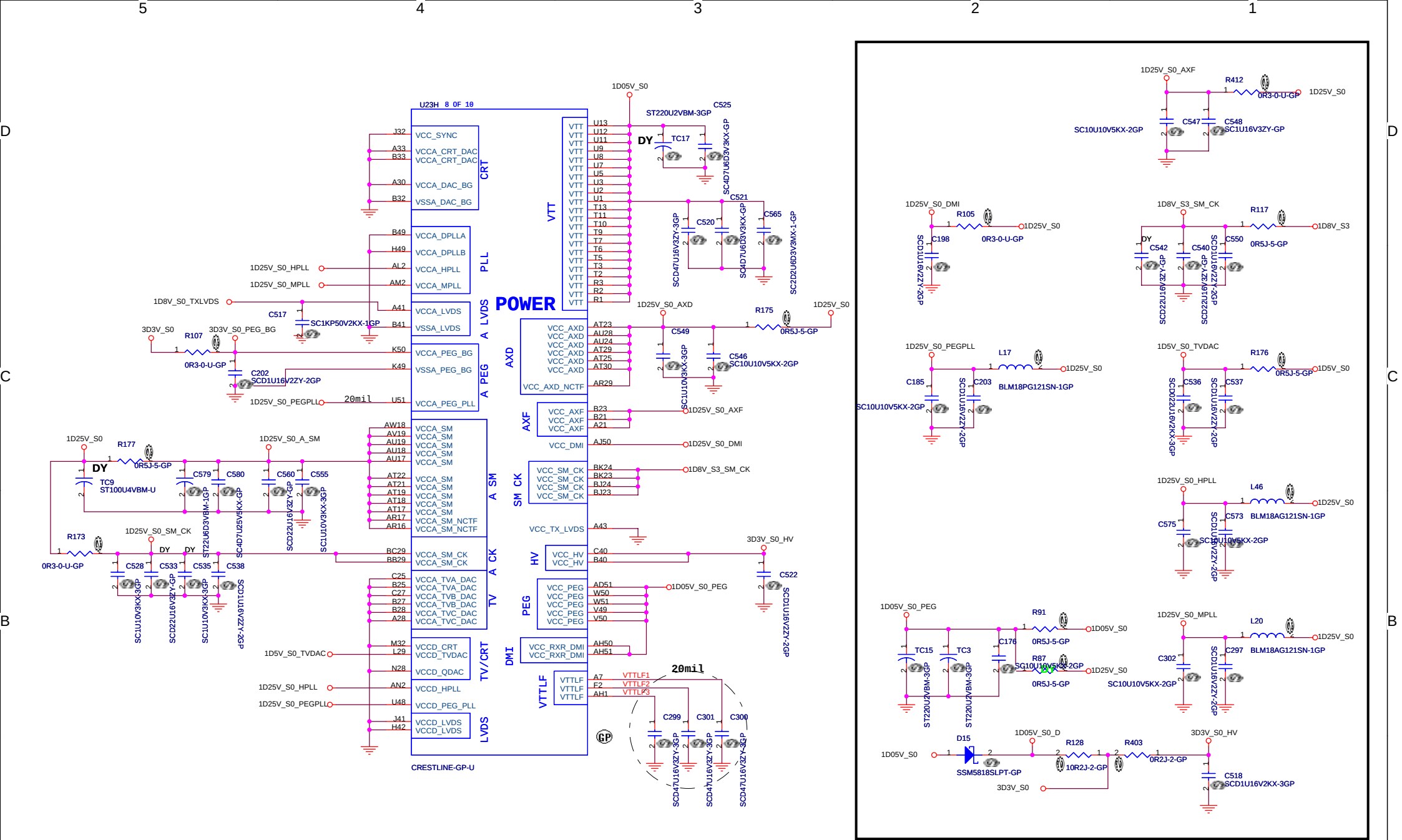
DDR SYSTEM MEMORY B

CRESTLINE-GP-U

<Core Design>



Strap Pin Table	
CFG[2:0] FSB Freq select	010 = FSB 800MHZ 011 = FSB 667MHZ Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse lane
CFG20(PCIE/SDVO consurent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.



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Title			CRESTLINE(4/6)-PWR
Size	Document Number	Rev	SA
A3			
Date: Thursday, December 14, 2006			Sheet 10 of 47

U23I 9 OF 10

A13	VSS	AW24
A15	VSS	AW29
A17	VSS	AW32
A24	VSS	AW5
AA21	VSS	AW7
AA24	VSS	AY10
AA29	VSS	AY24
AB20	VSS	AY37
AB23	VSS	AY42
AB26	VSS	AY43
AB28	VSS	AY45
AB31	VSS	AY47
AC10	VSS	AY50
AC13	VSS	B10
AC3	VSS	B20
AC39	VSS	B24
AC43	VSS	B29
AC47	VSS	B30
AD1	VSS	B35
AD21	VSS	B38
AD26	VSS	B43
AD29	VSS	B46
AD3	VSS	B5
AD41	VSS	B8
AD45	VSS	BA1
AD49	VSS	BA17
AD5	VSS	BA18
AD50	VSS	BA2
AD8	VSS	BA24
AE10	VSS	BB12
AE14	VSS	BB25
AE6	VSS	BB40
AE20	VSS	BB44
AE23	VSS	BB49
AE24	VSS	BB8
AE31	VSS	BC16
AG2	VSS	BC24
AG38	VSS	BC25
AG43	VSS	BC36
AG47	VSS	BC40
AG50	VSS	BC51
AH3	VSS	BD13
AH40	VSS	BD2
AH41	VSS	BD28
AH7	VSS	BD45
AH9	VSS	BD48
AJ11	VSS	BD5
AJ13	VSS	BE1
AJ21	VSS	BE19
AJ24	VSS	BE23
AJ29	VSS	BE30
AJ32	VSS	BE42
AJ43	VSS	BE51
AJ45	VSS	BE8
AJ49	VSS	BF12
AK20	VSS	BF16
AK21	VSS	BF36
AK26	VSS	BG19
AK28	VSS	BG2
AK31	VSS	BG24
AK51	VSS	BG29
AL1	VSS	BG39
AM11	VSS	BG48
AM13	VSS	BG5
AM3	VSS	BG51
AM4	VSS	BH17
AM41	VSS	BH30
AM45	VSS	BH44
AN1	VSS	BH46
AN38	VSS	BH8
AN39	VSS	BJ11
AN43	VSS	BJ13
AN5	VSS	BJ38
AN7	VSS	BJ4
AP4	VSS	BJ42
AP48	VSS	BJ46
AP50	VSS	BK15
AR11	VSS	BK17
AR2	VSS	BK25
AR39	VSS	BK29
AR44	VSS	BK36
AR47	VSS	BK40
AR7	VSS	BK44
AT10	VSS	BK6
AT14	VSS	BK8
AT41	VSS	BL11
AT49	VSS	BL13
AU1	VSS	BL19
AU23	VSS	BL22
AU29	VSS	BL37
AU3	VSS	BL47
AU36	VSS	C12
AU49	VSS	C16
AU51	VSS	C19
AV39	VSS	C28
AV48	VSS	C29
AW1	VSS	C33
AW12	VSS	C36
AW16	VSS	C41

CRESTLINE-GP-U

U23J 10 OF 10

C46	VSS	W11
C50	VSS	W39
C7	VSS	W43
D13	VSS	W47
D24	VSS	W5
D3	VSS	W7
D324	VSS	Y13
D39	VSS	Y2
D45	VSS	Y41
D49	VSS	Y45
E10	VSS	Y49
E16	VSS	Y5
E24	VSS	Y50
E28	VSS	Y11
E32	VSS	P29
E47	VSS	T29
F19	VSS	T31
F36	VSS	T33
F4	VSS	R28
F40	VSS	
F50	VSS	
G1	VSS	
G13	VSS	
G16	VSS	AA32
G19	VSS	AB32
G24	VSS	AD32
G28	VSS	AE28
G29	VSS	AE29
G33	VSS	AT27
G42	VSS	AV25
G45	VSS	H50
G48	VSS	
GB44	VSS	
H24	VSS	
H28	VSS	
H4	VSS	
H45	VSS	
J11	VSS	
J16	VSS	
J2	VSS	
J24	VSS	
J28	VSS	
J33	VSS	
J35	VSS	
J39	VSS	
K12	VSS	
K47	VSS	
K8	VSS	
L1	VSS	
L17	VSS	
L20	VSS	
L24	VSS	
L28	VSS	
L3	VSS	
L33	VSS	
L49	VSS	
M28	VSS	
M42	VSS	
M46	VSS	
M49	VSS	
M5	VSS	
M50	VSS	
M9	VSS	
N11	VSS	
N14	VSS	
N7	VSS	
N29	VSS	
N32	VSS	
N36	VSS	
N39	VSS	
N44	VSS	
N49	VSS	
P19	VSS	
P2	VSS	
P23	VSS	
P3	VSS	
P50	VSS	
R49	VSS	
T39	VSS	
T43	VSS	
T47	VSS	
U41	VSS	
U46	VSS	
U50	VSS	
V2	VSS	
V3	VSS	

VSS

CRESTLINE-GP-U



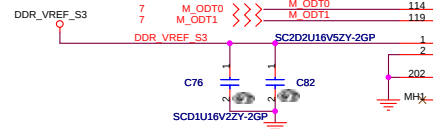
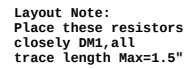
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Title		
CRESTLINE(6/6)-PWR/GND		
Size	Document Number	Rev
A3		SA
Date:	Wednesday, October 18, 2006	Sheet 12 of 47

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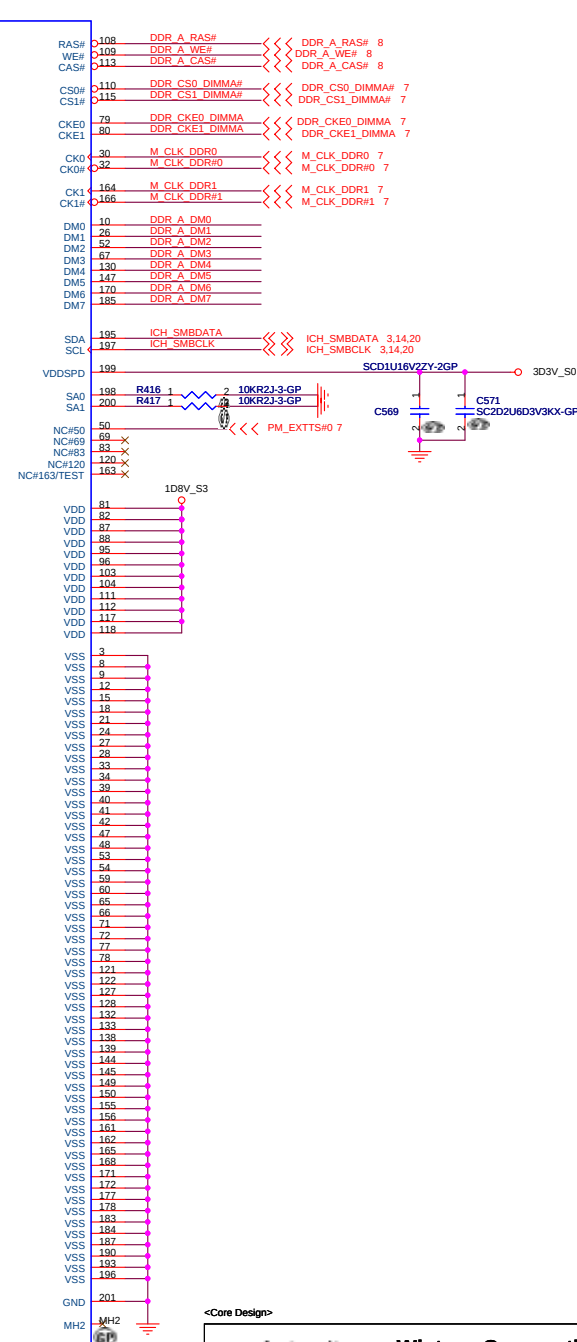
Pamirs-Discrete



		DM2
DDR A MA0	102	A0
DDR A MA1	101	A1
DDR A MA2	100	A2
DDR A MA3	99	A3
DDR A MA4	98	A4
DDR A MA5	97	A5
DDR A MA6	94	A6
DDR A MA7	93	A7
DDR A MA8	93	A8
DDR A MA9	91	A9
DDR A MA10	105	A10/AP
DDR A MA11	99	A11
DDR A MA12	99	A12
DDR A MA13	116	A13
DDR A MA14	86	A14
DDR A BS2	84	A15
	85	B16/BA2
DDR A BS0	107	BA0
DDR A BS1	106	BA1

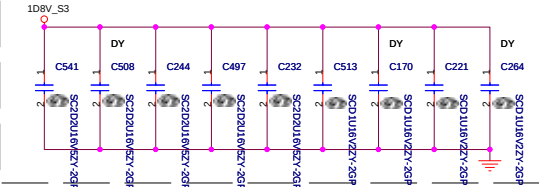
DDR A D0	5	D00
DDR A D1	17	D01
DDR A D2	17	D02
DDR A D3	19	D03
DDR A D4	19	D04
DDR A D5	14	D05
DDR A D6	16	D06
DDR A D7	16	D07
DDR A D8	23	D08
DDR A D9	25	D09
DDR A D10	25	D10
DDR A D11	37	D11
DDR A D12	37	D12
DDR A D13	22	D13
DDR A D14	36	D14
DDR A D15	36	D15
DDR A D16	43	D16
DDR A D17	47	D17
DDR A D18	55	D18
DDR A D19	57	D19
DDR A D20	46	D20
DDR A D21	61	D21
DDR A D22	61	D22
DDR A D23	58	D23
DDR A D24	61	D24
DDR A D25	63	D25
DDR A D26	63	D26
DDR A D27	75	D27
DDR A D28	62	D28
DDR A D29	64	D29
DDR A D30	76	D30
DDR A D31	76	D31
DDR A D32	123	D32
DDR A D33	125	D33
DDR A D34	133	D34
DDR A D35	137	D35
DDR A D36	124	D36
DDR A D37	138	D37
DDR A D38	134	D38
DDR A D39	136	D39
DDR A D40	141	D40
DDR A D41	141	D41
DDR A D42	151	D42
DDR A D43	153	D43
DDR A D44	142	D44
DDR A D45	142	D45
DDR A D46	152	D46
DDR A D47	154	D47
DDR A D48	154	D48
DDR A D49	159	D49
DDR A D50	173	D50
DDR A D51	173	D51
DDR A D52	158	D52
DDR A D53	160	D53
DDR A D54	174	D54
DDR A D55	174	D55
DDR A D56	179	D56
DDR A D57	181	D57
DDR A D58	181	D58
DDR A D59	191	D59
DDR A D60	180	D60
DDR A D61	182	D61
DDR A D62	182	D62
DDR A D63	194	D63

DDR A DQS#0	11	DQS#0
DDR A DQS#1	29	DQS#1
DDR A DQS#2	49	DQS#2
DDR A DQS#3	68	DQS#3
DDR A DQS#4	129	DQS#4
DDR A DQS#5	146	DQS#5
DDR A DQS#6	167	DQS#6
DDR A DQS#7	186	DQS#7
DDR A DQS0	13	DQS0
DDR A DQS1	31	DQS1
DDR A DQS2	51	DQS2
DDR A DQS3	70	DQS3
DDR A DQS4	131	DQS4
DDR A DQS5	148	DQS5
DDR A DQS6	169	DQS6
DDR A DQS7	188	DQS7

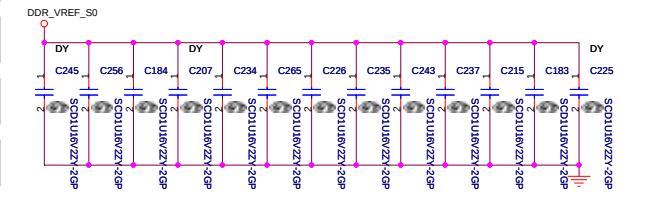


8 DDR_B_DQS#[0..7] <<>>
 8 DDR_B_DQ[0..63] <<>>
 8 DDR_B_DM[0..7] <<>>
 8 DDR_B_DQS[0..7] <<>>
 8 DDR_B_MA[0..13] <<>>
 8 DDR_B_BS[0..2] <<>>

Layout Note:
Place near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



7 DDR_B_MA14 <<>>

DM1
 DDR B MA0 102
 DDR B MA1 101
 DDR B MA2 100
 DDR B MA3 99
 DDR B MA4 98
 DDR B MA5 97
 DDR B MA6 96
 DDR B MA7 95
 DDR B MA8 94
 DDR B MA9 93
 DDR B MA10 92
 DDR B MA11 91
 DDR B MA12 90
 DDR B MA13 89
 DDR B MA14 88
 DDR B BS2 87
 DDR B BS0 86
 DDR B BS1 85
 DDR B BS2 84
 DDR B BS0 83
 DDR B BS1 82

DDR B D0 5
 DDR B D1 7
 DDR B D2 17
 DDR B D3 18
 DDR B D4 19
 DDR B D5 20
 DDR B D6 21
 DDR B D7 22
 DDR B D8 23
 DDR B D9 24
 DDR B D10 25
 DDR B D11 26
 DDR B D12 27
 DDR B D13 28
 DDR B D14 29
 DDR B D15 30
 DDR B D16 31
 DDR B D17 32
 DDR B D18 33
 DDR B D19 34
 DDR B D20 35
 DDR B D21 36
 DDR B D22 37
 DDR B D23 38
 DDR B D24 39
 DDR B D25 40
 DDR B D26 41
 DDR B D27 42
 DDR B D28 43
 DDR B D29 44
 DDR B D30 45
 DDR B D31 46
 DDR B D32 47
 DDR B D33 48
 DDR B D34 49
 DDR B D35 50
 DDR B D36 51
 DDR B D37 52
 DDR B D38 53
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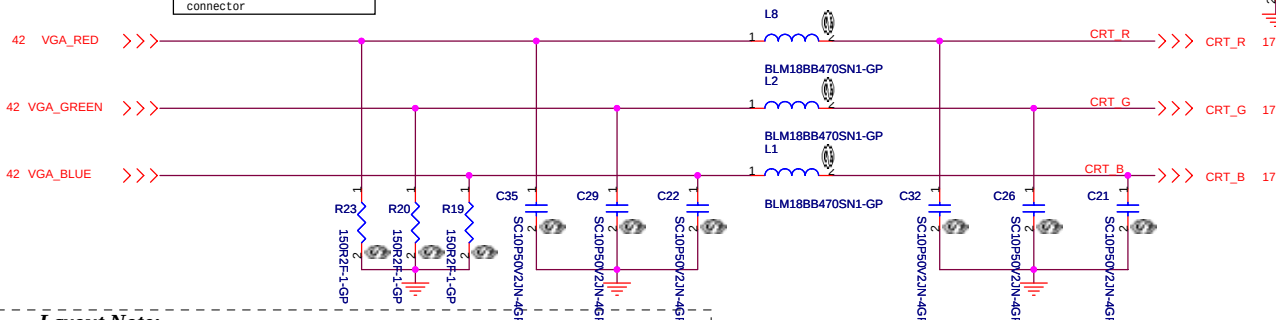
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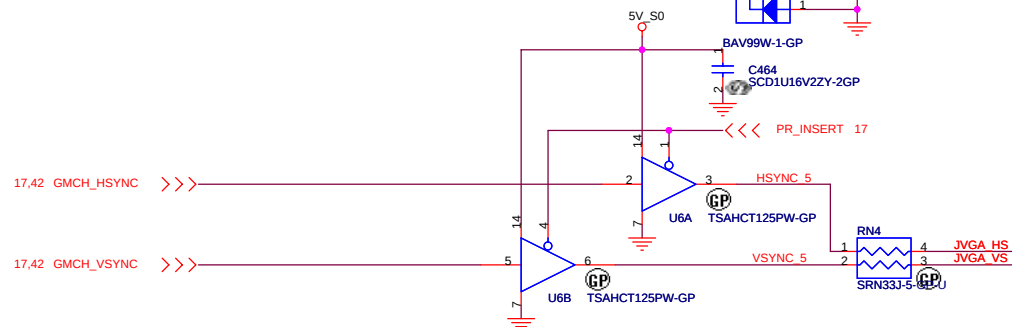
CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector



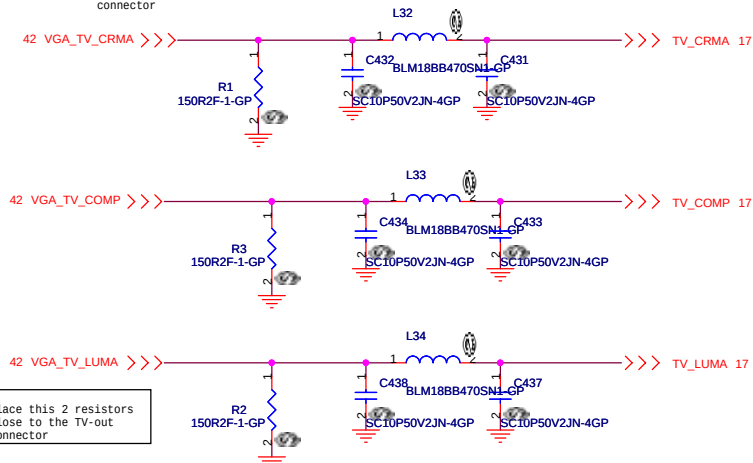
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

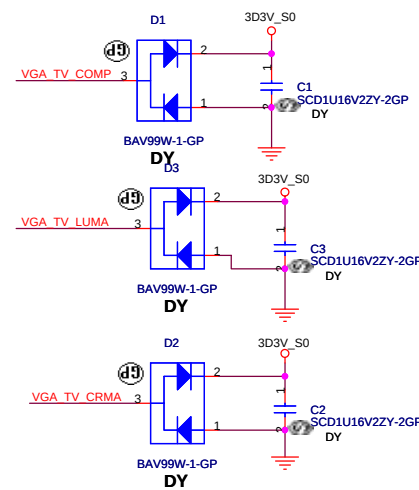
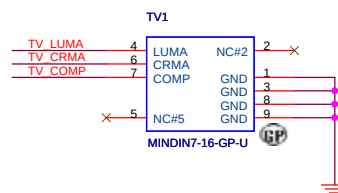


TV OUT CONN

connector



Place this 2 resistors
close to the TV-out
connector



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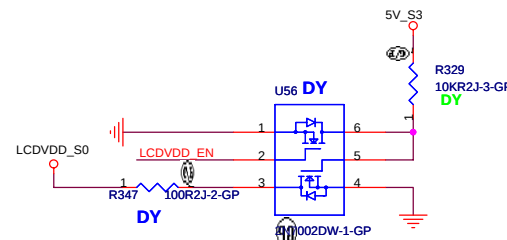
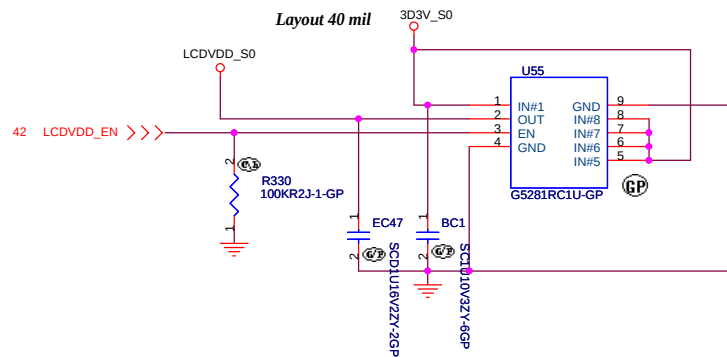
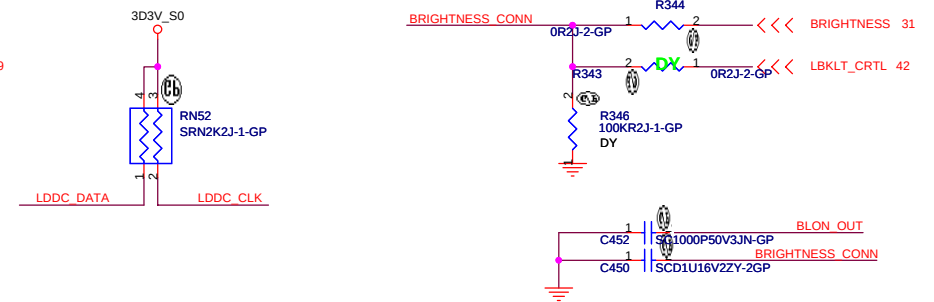
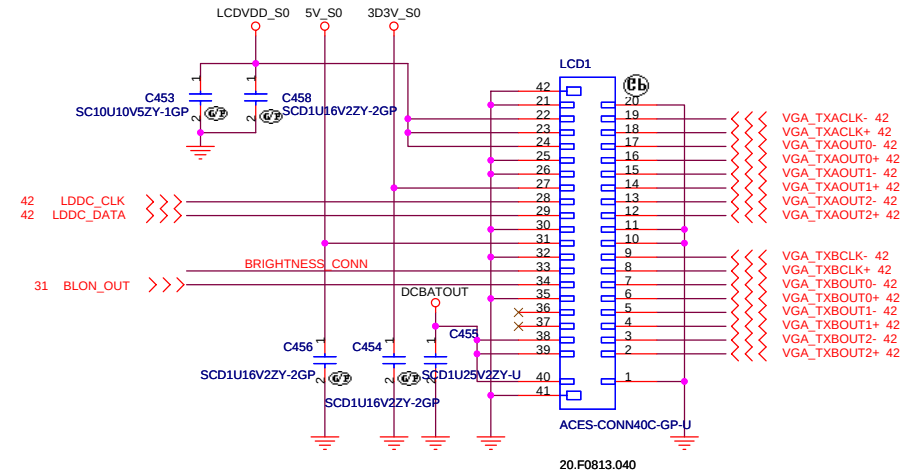
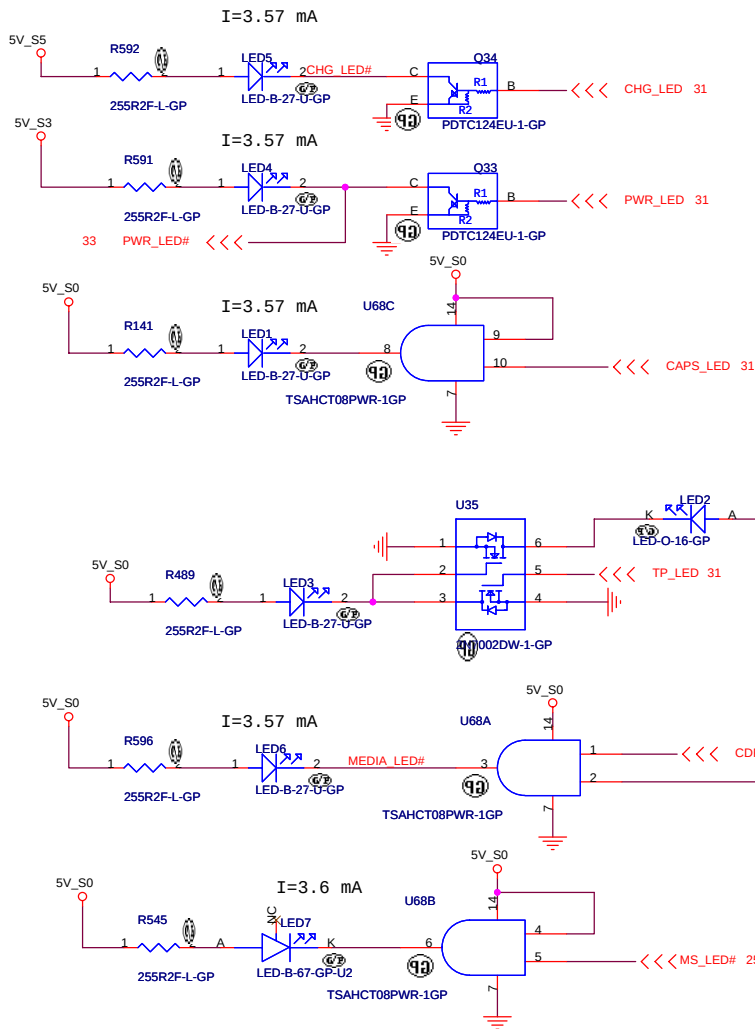
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

CRT/TV Connector		
Size A3	Document Number	Rev SA
Date: Friday, November 24, 2006	Sheet 15 of 47	

LED / INVERTER INTERFACE

LCD/INV CONN

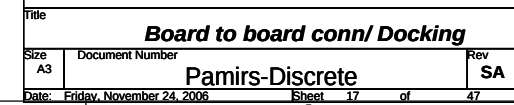


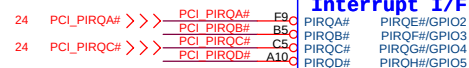
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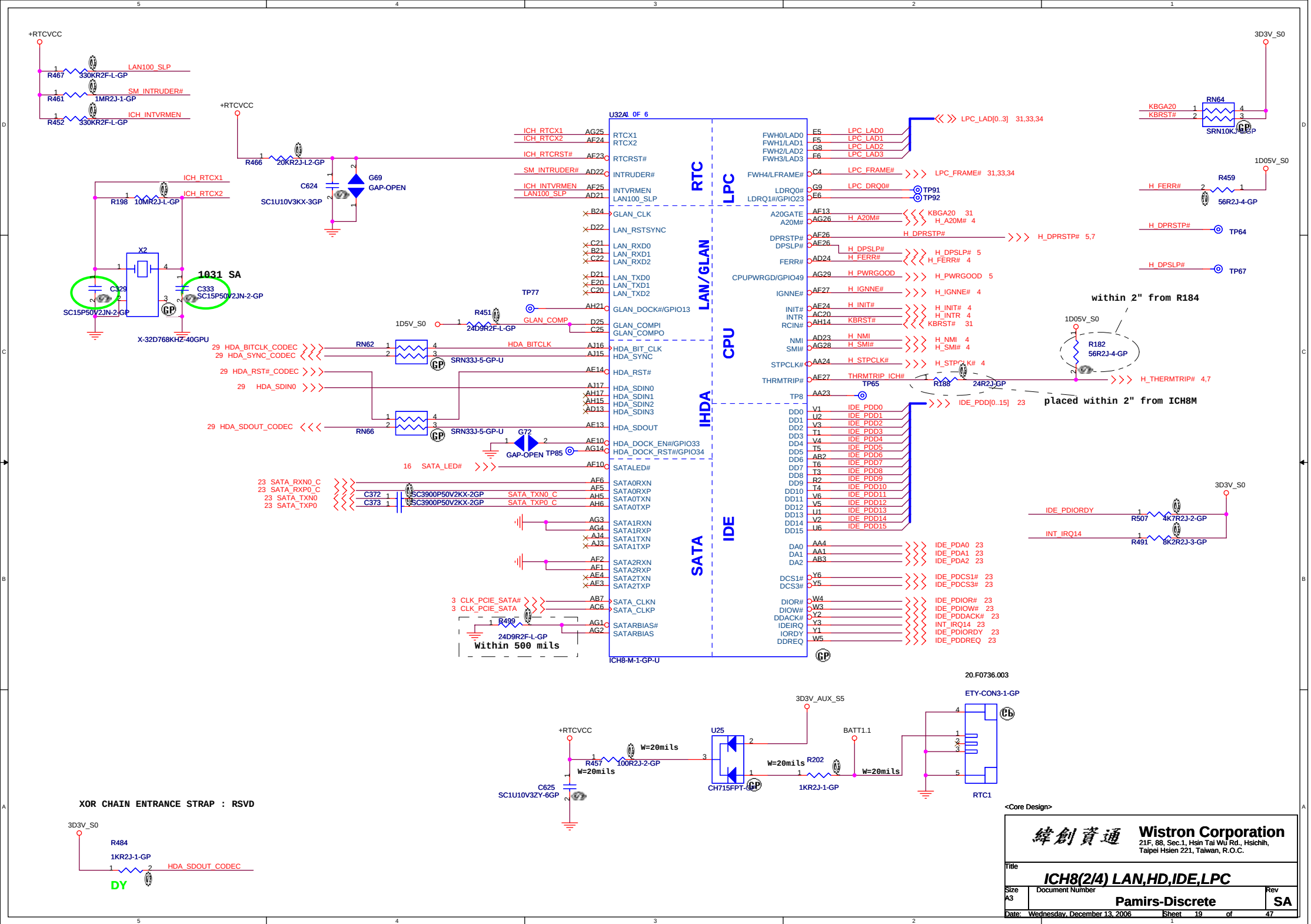
緯創資通

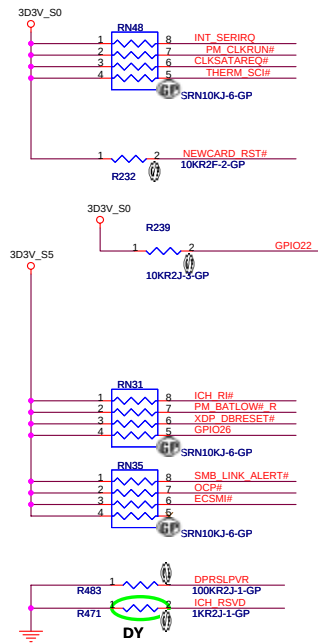
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

LCD/Inverter Connector			Rev
Size	Document Number		SA
Custom			
Date:	Tuesday, December 19, 2006	Sheet 16 of 47	

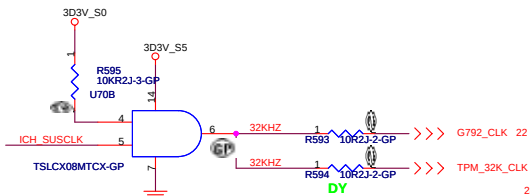








32K suspend clock output

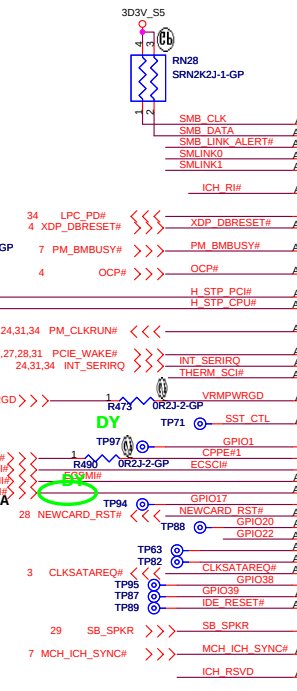
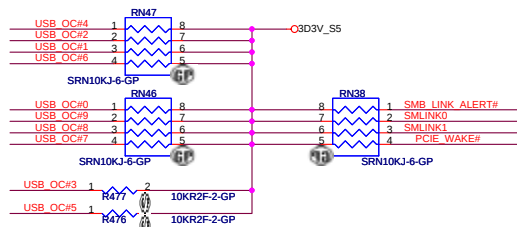


New Card

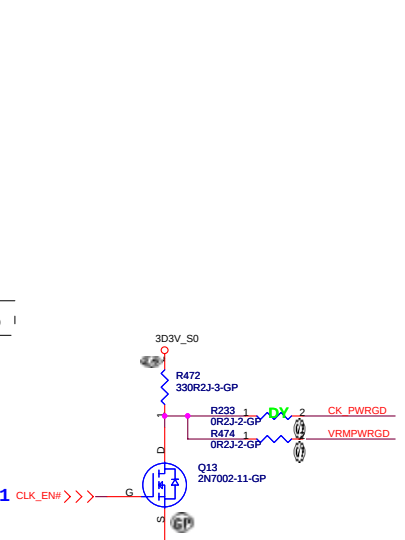
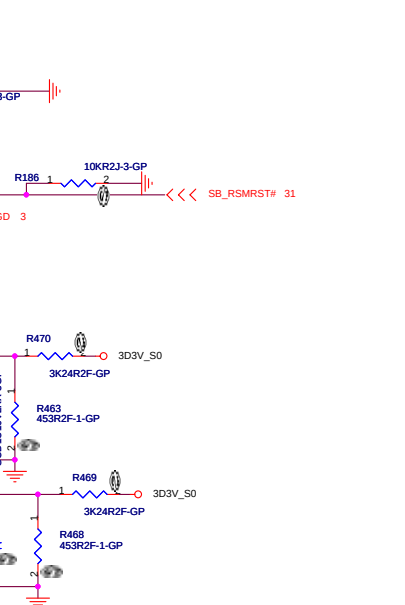
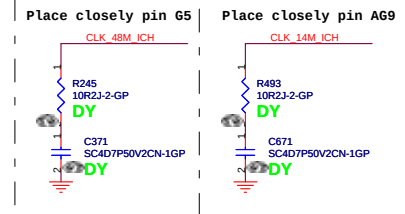
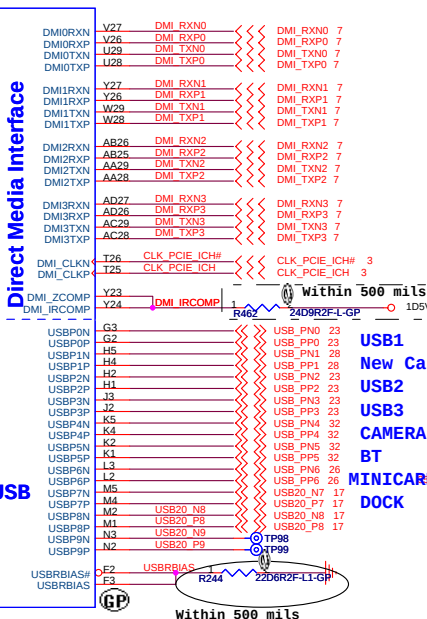
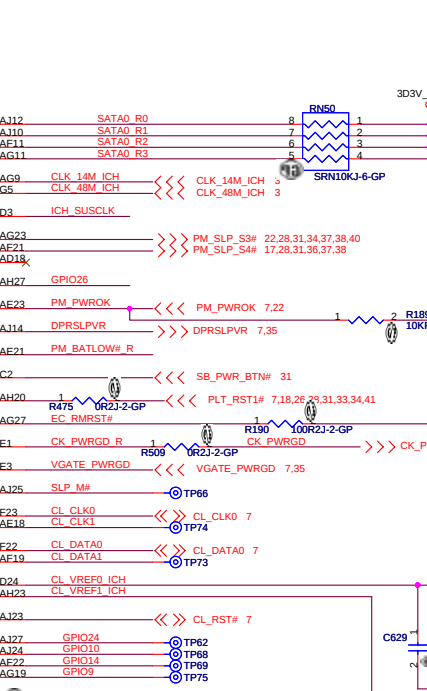
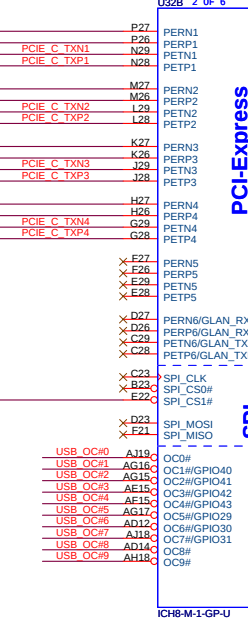
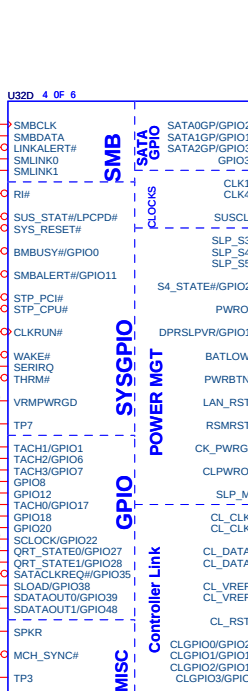
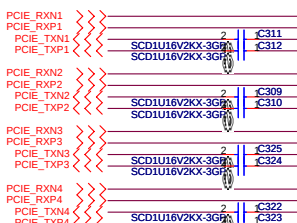
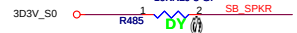
LAN

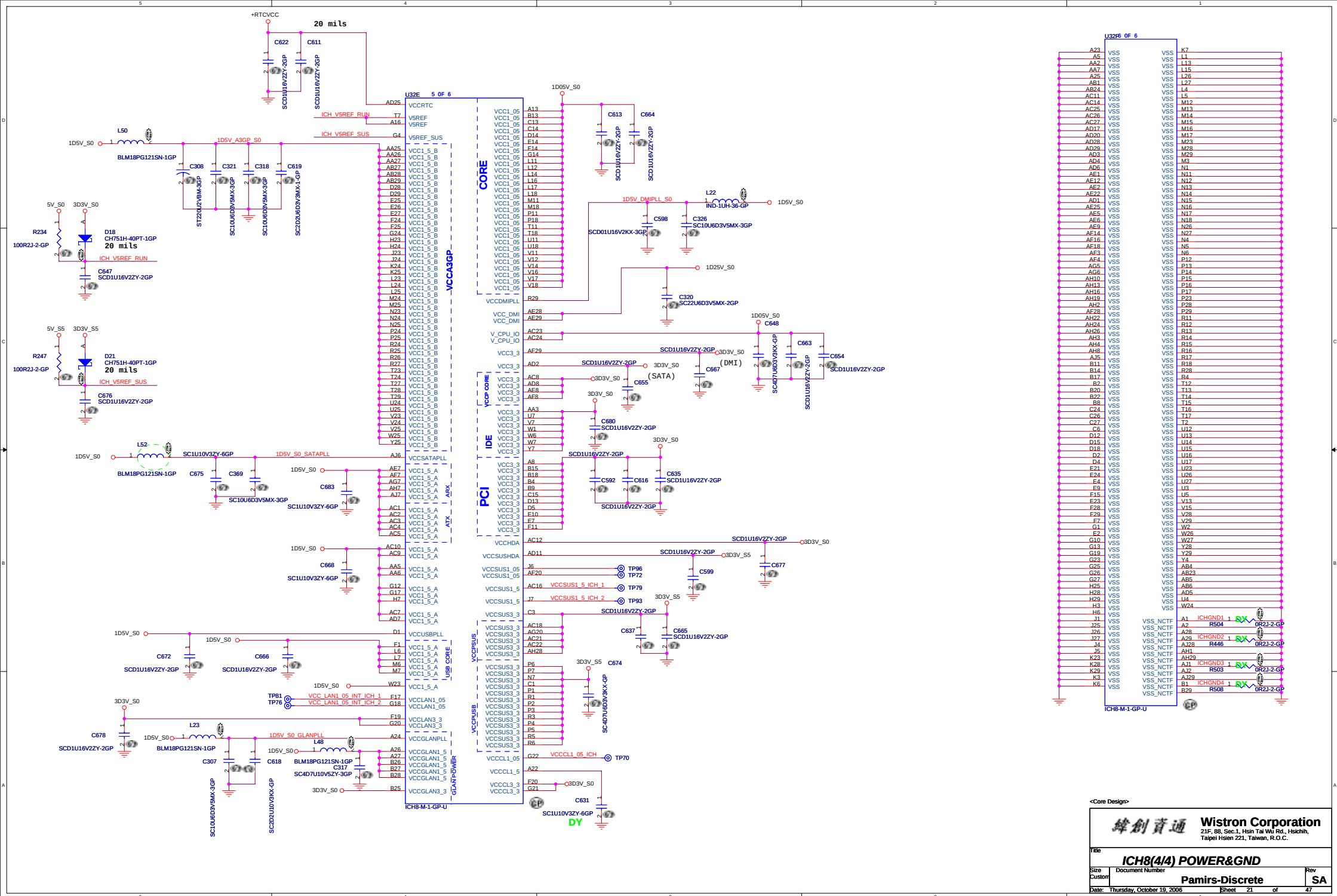
Mini Card 1

Mini Card 2

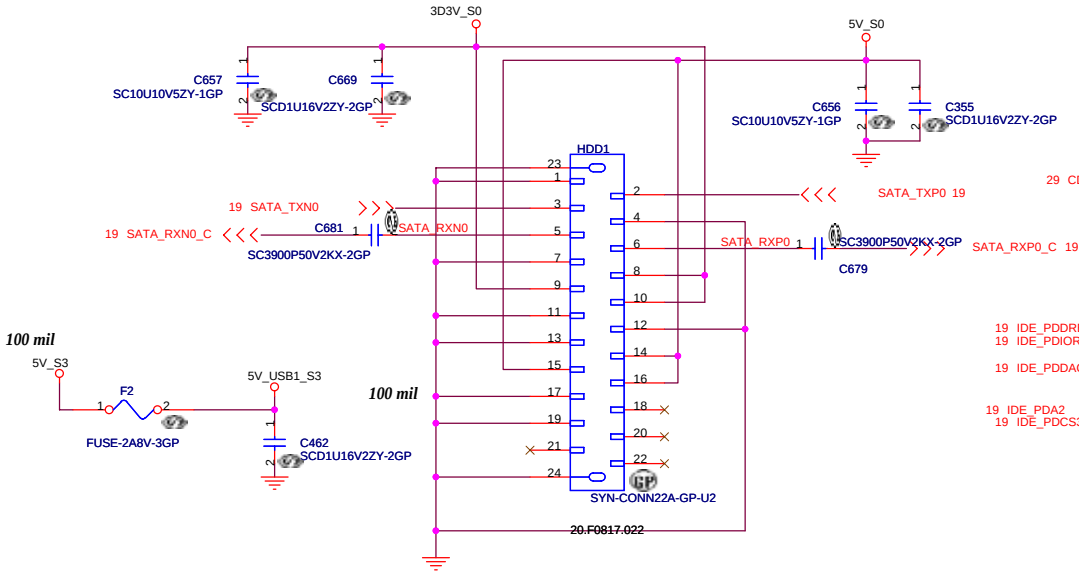


Low--> default
High--> No boot

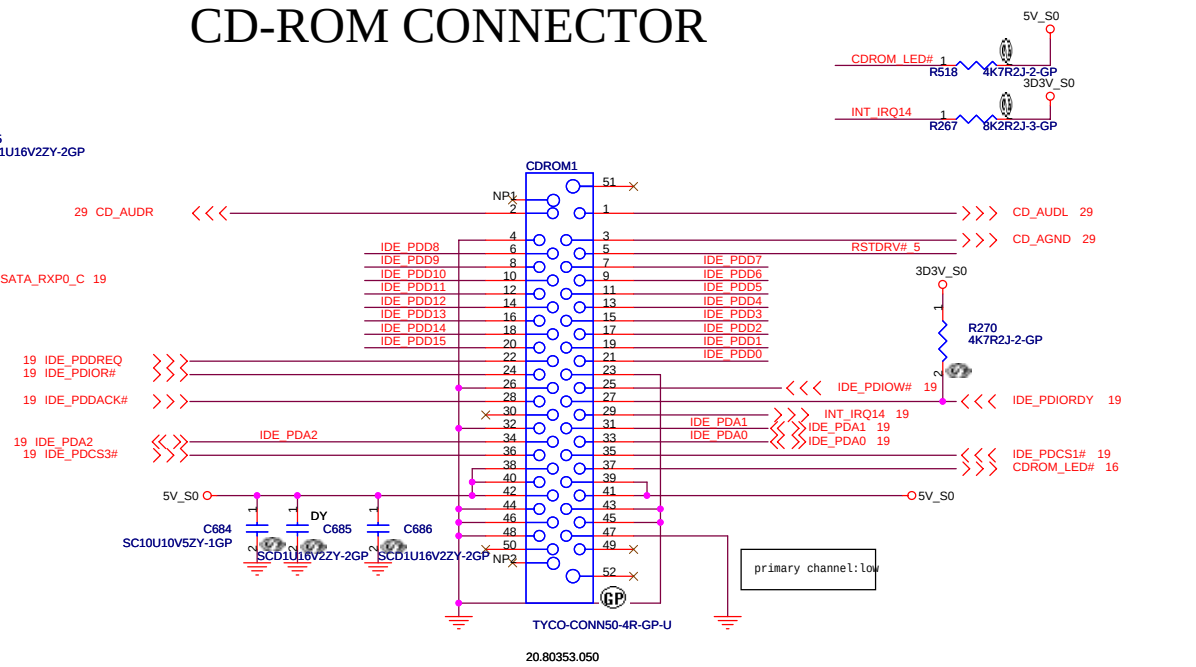




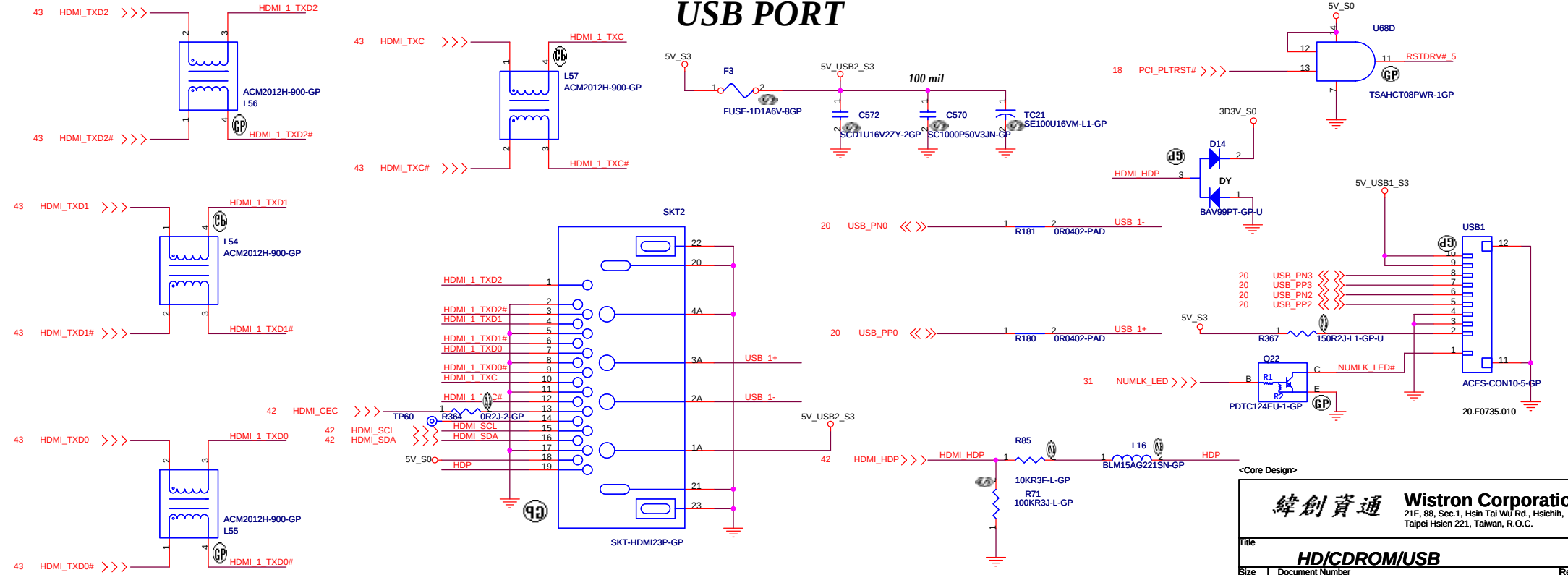
SATA HD Connector



CD-ROM CONNECTOR

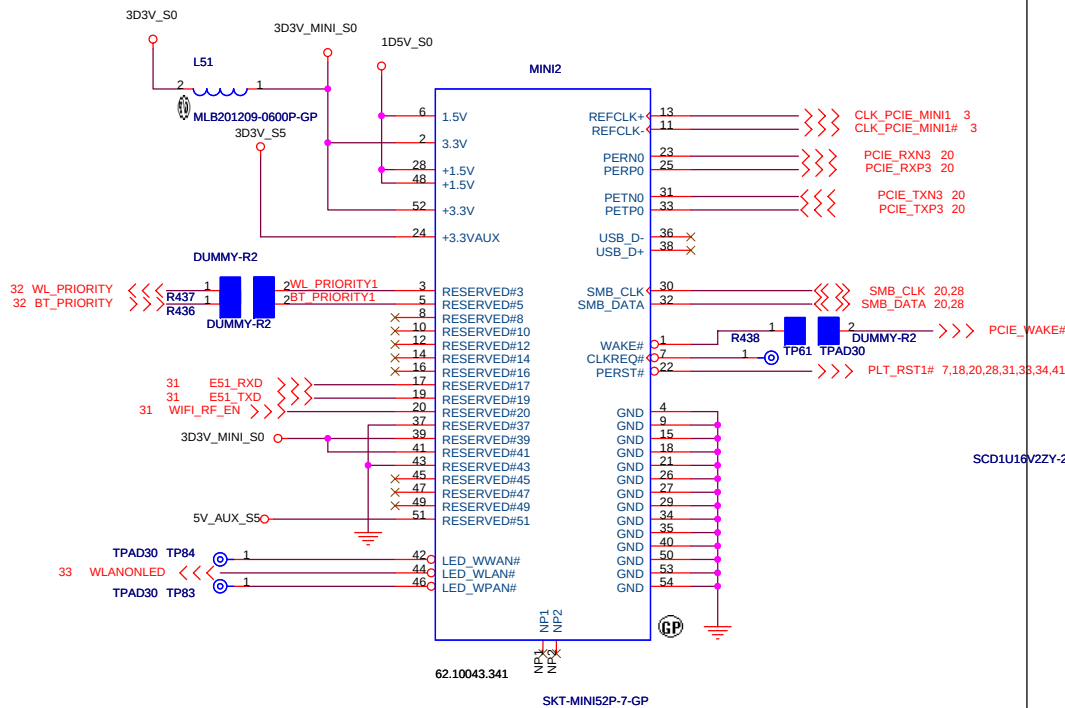


USB PORT



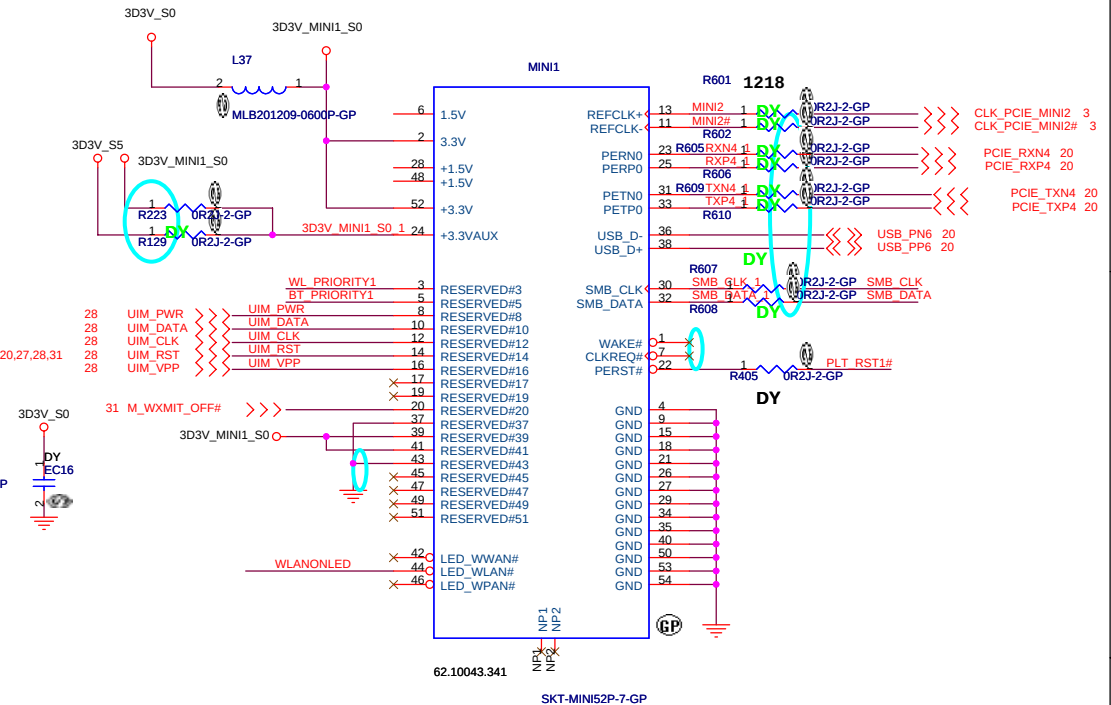
Mini Card Connector 2

Wireless card



Mini Card Connector 1

WWAN

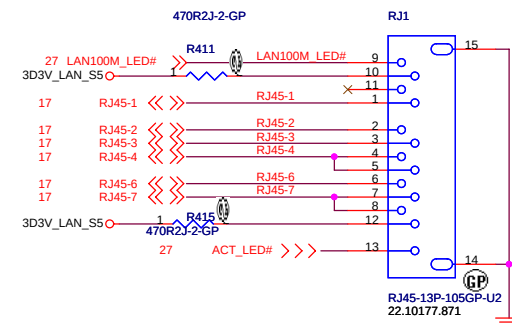
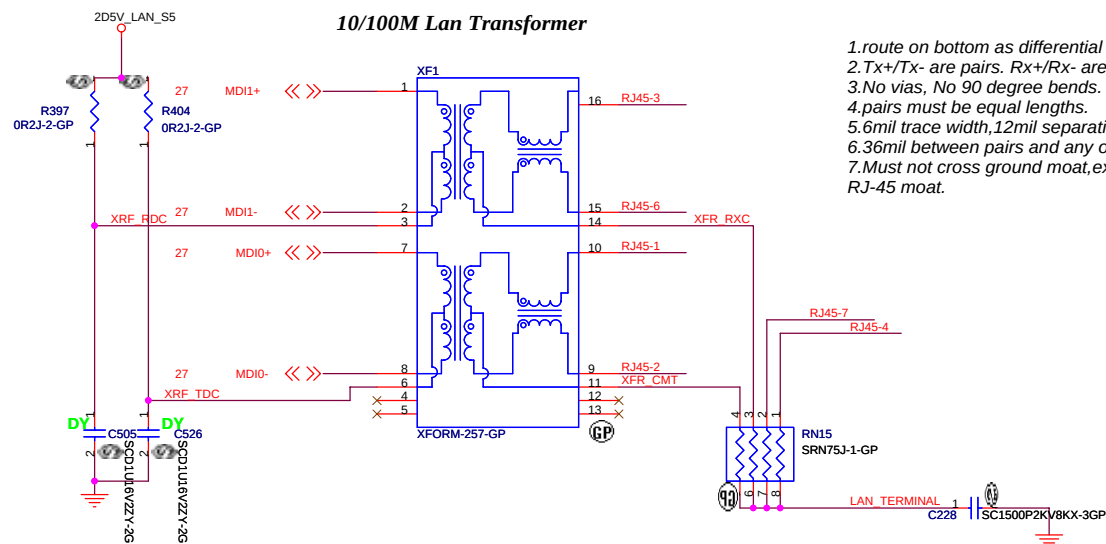


<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

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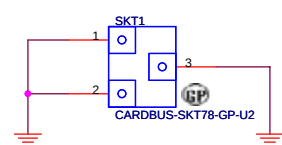
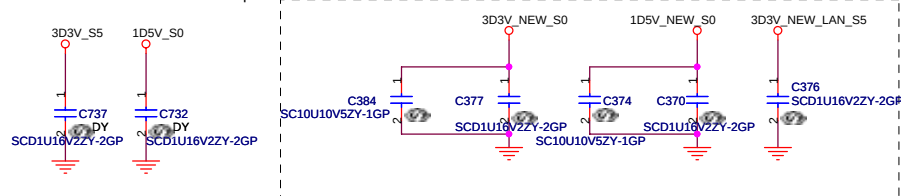
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.



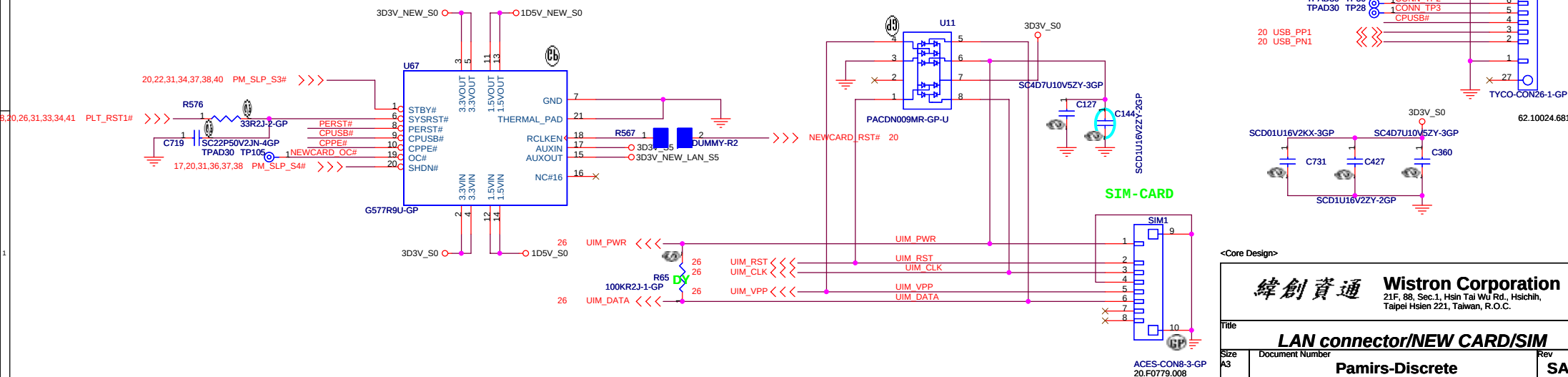
Green : Link up
Blinking : TX/RX activity

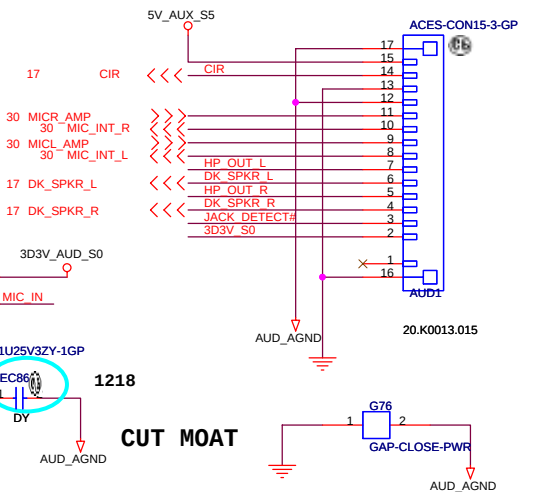
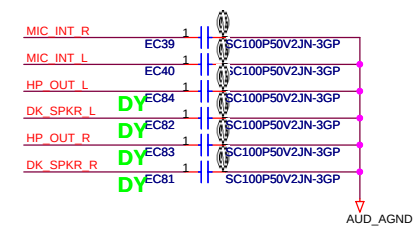
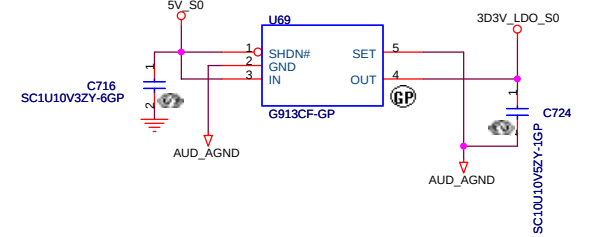
Place them Near to Connector

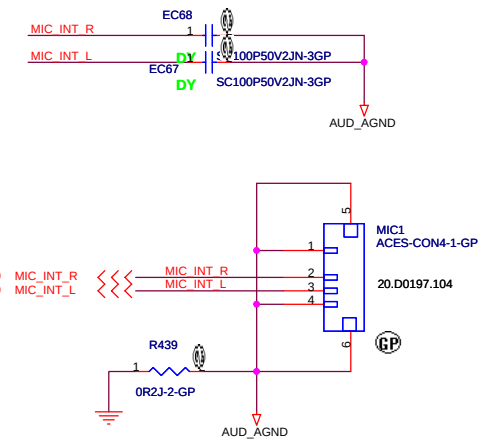
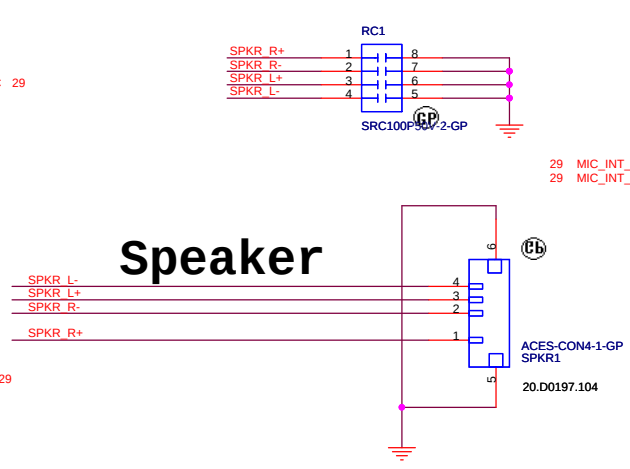
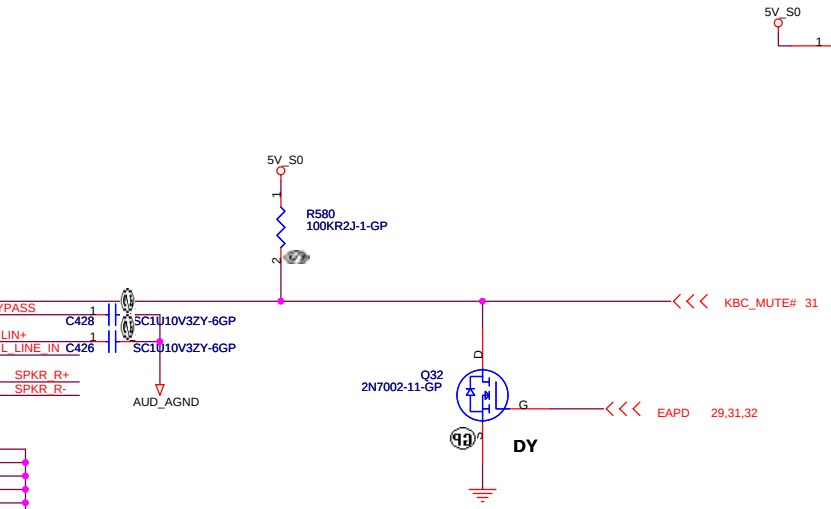
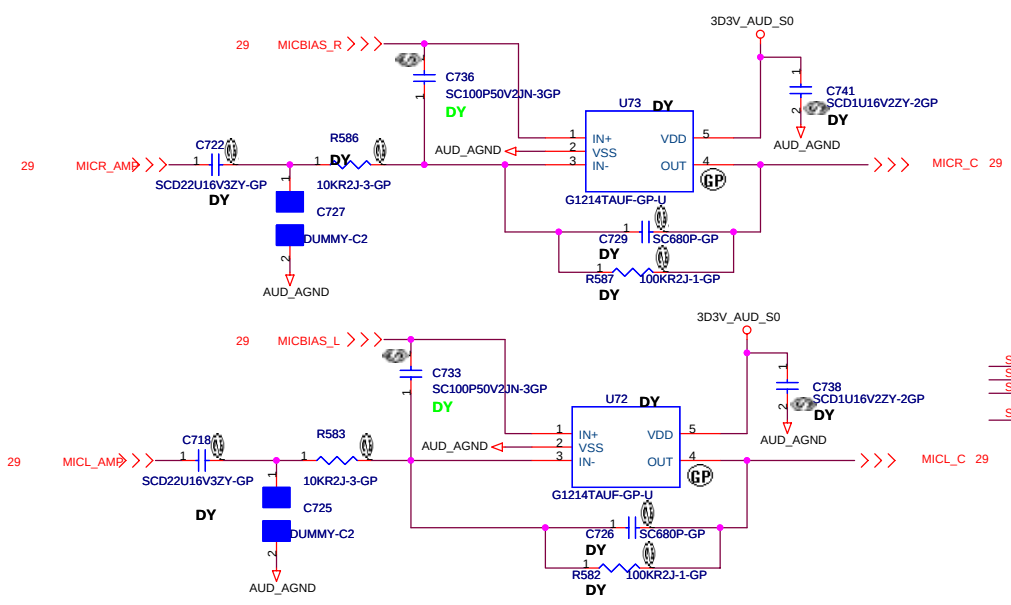
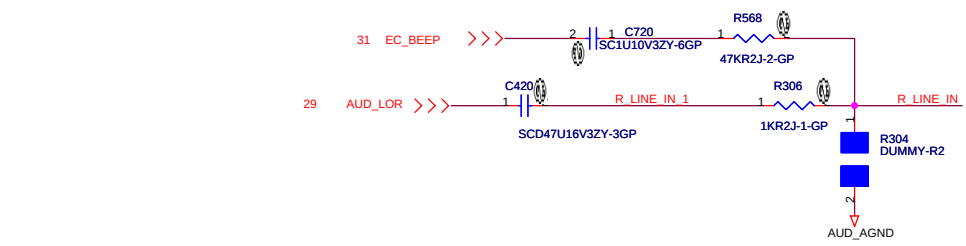
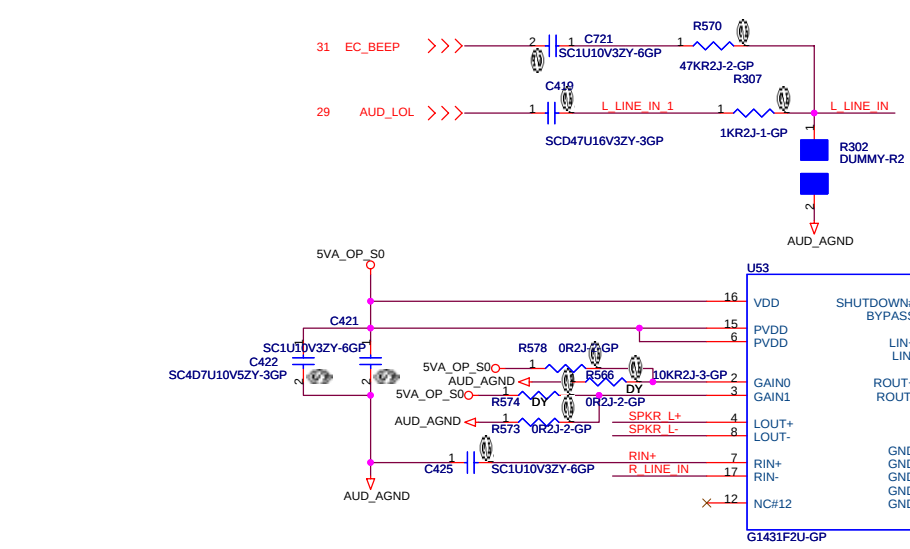
Place them Near to Chip

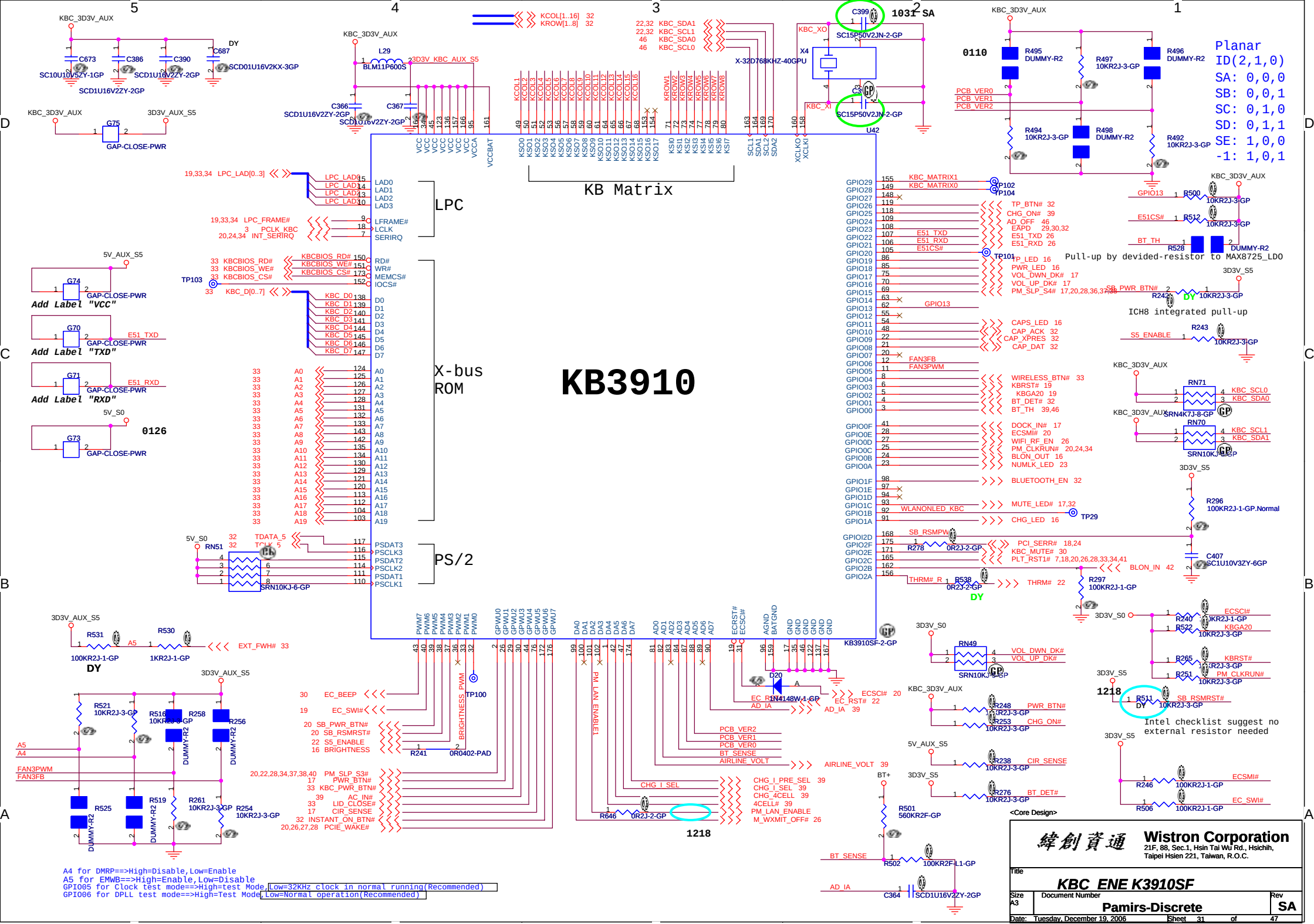


For Newcard socket









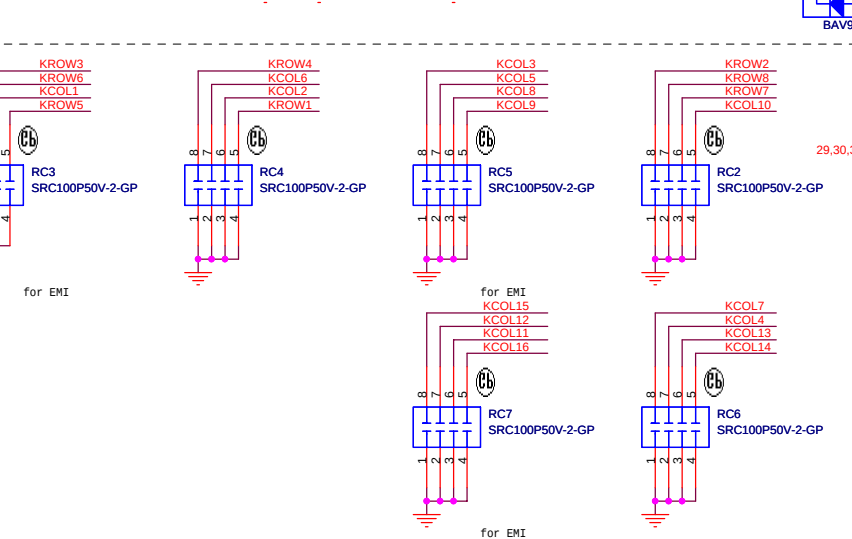
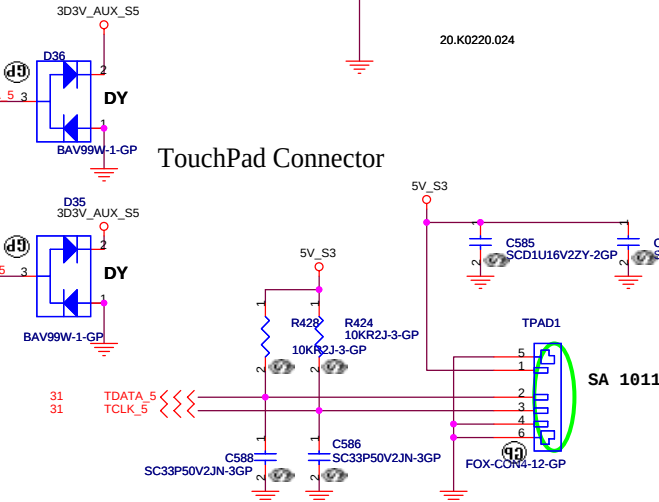
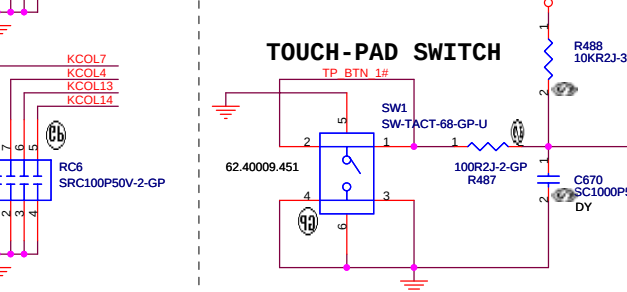
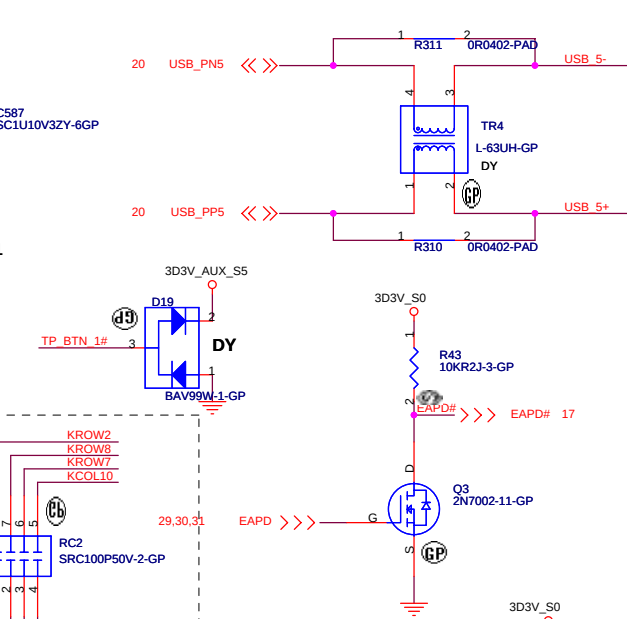
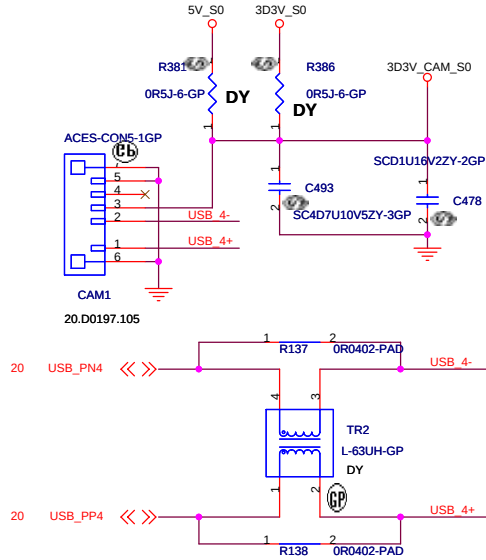
CAMERA

Internal KeyBoard Connector

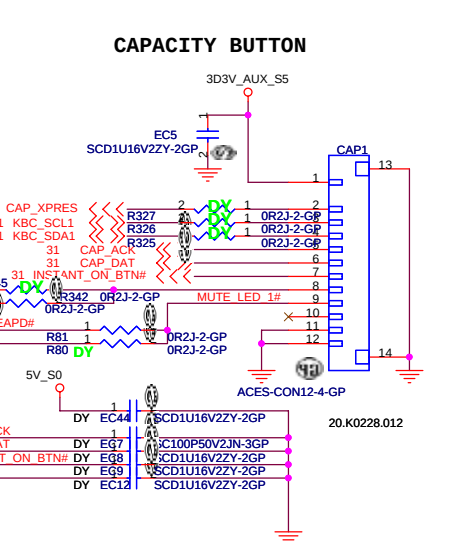
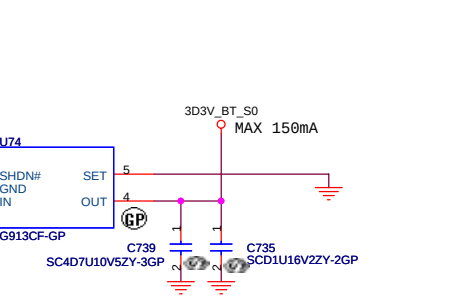
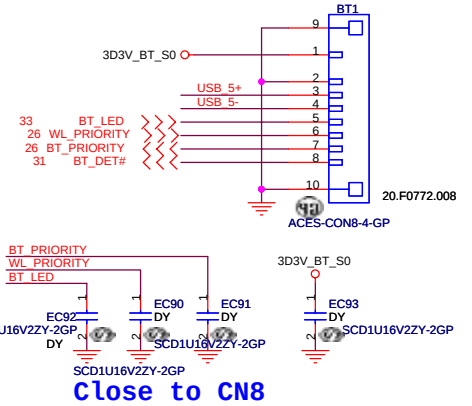
31 KROW[1..8] <<< <<<
31 KCOL[1..16] <<< <<<

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



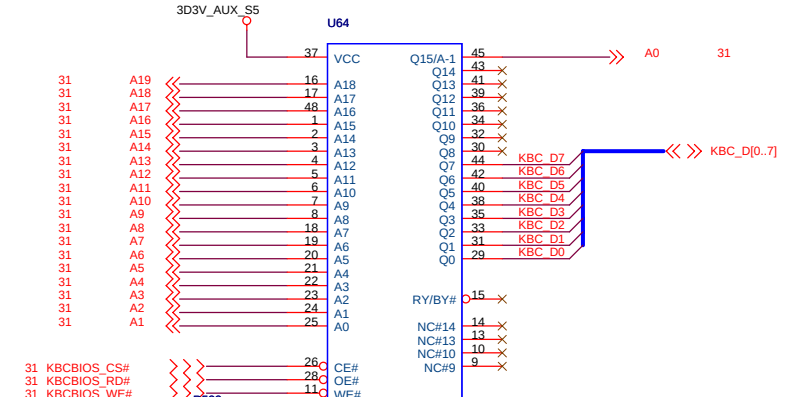
Blue thumb



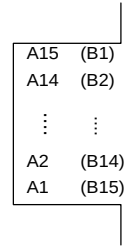
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KeyBoard-CONN

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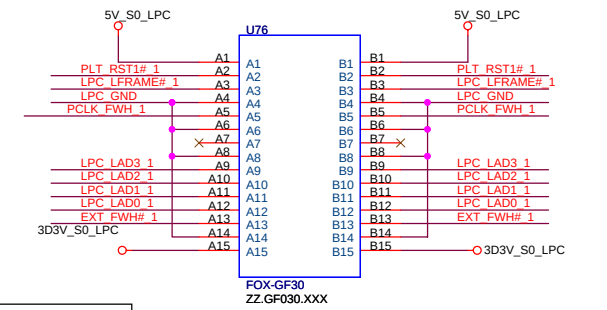
TOP VIEW



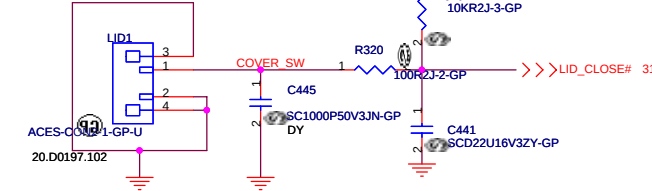
(BOTTOM VIEW)

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

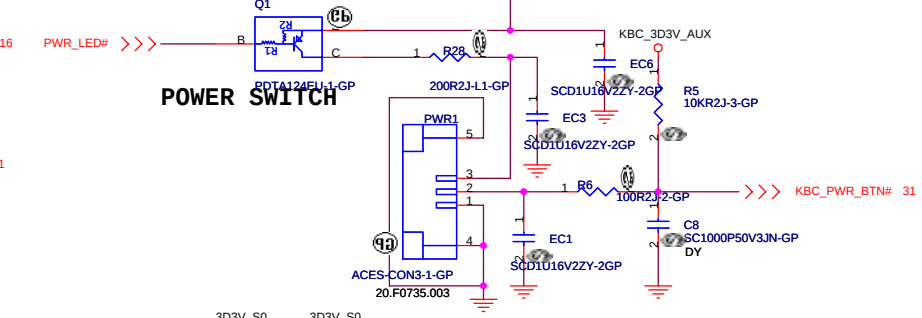
GOLDEN FINGER FOR DEBUG BOARD



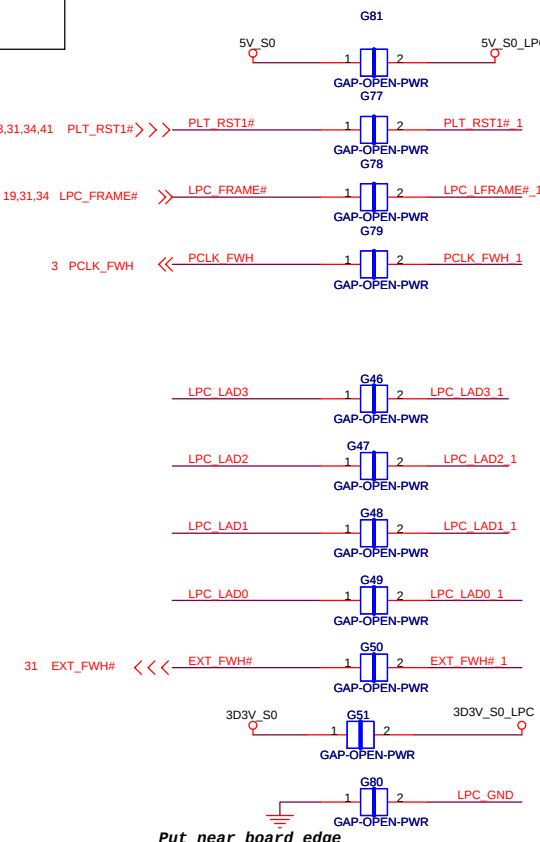
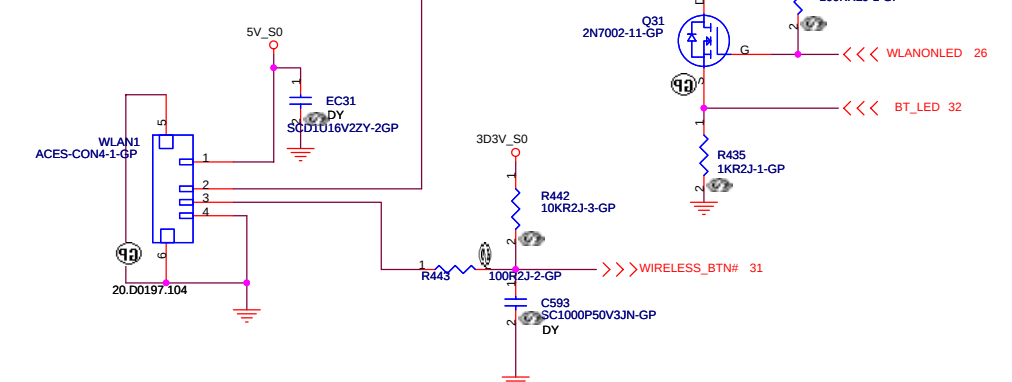
COVER SWITCH



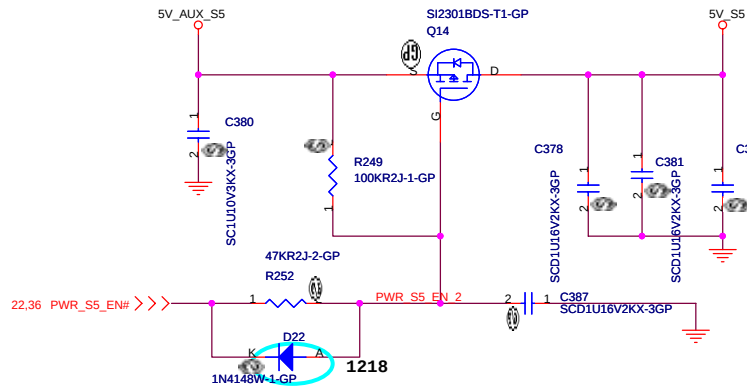
POWER SWITCH



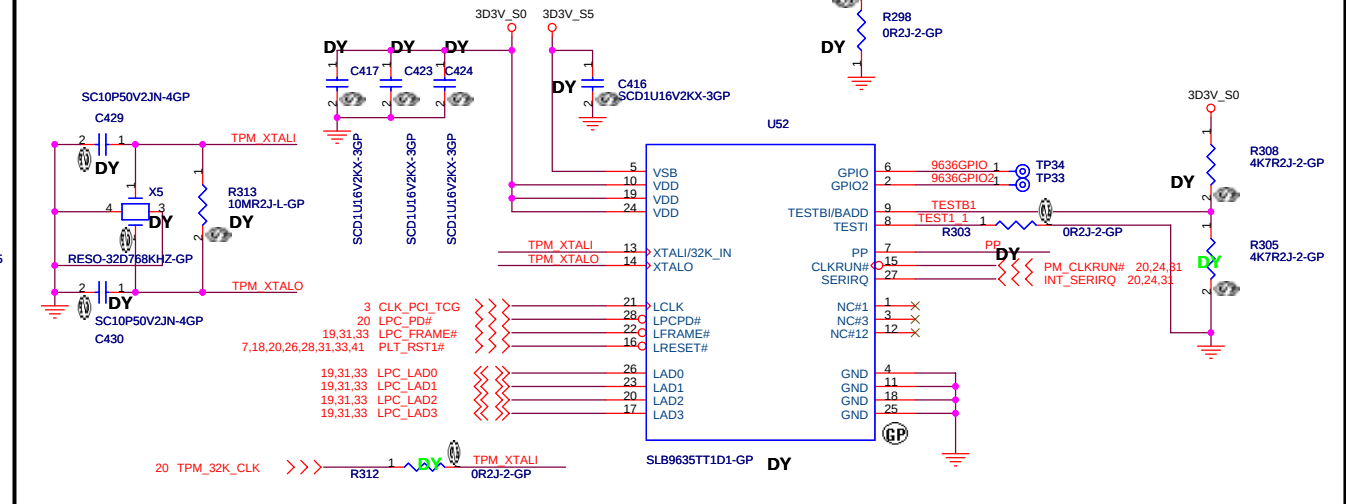
WIRELESS SWITCH



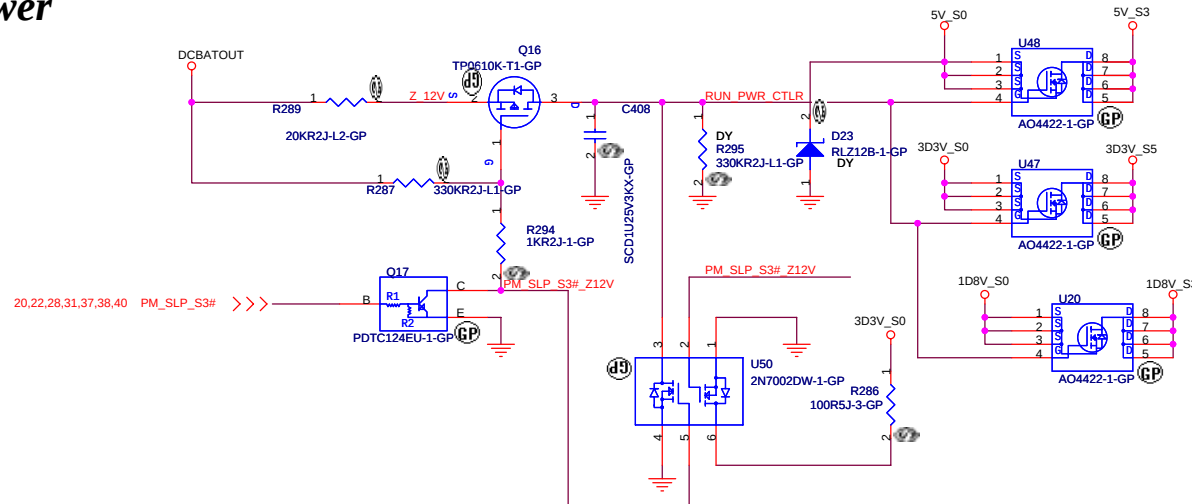
5V_AUX_S5 TO 5V_S5



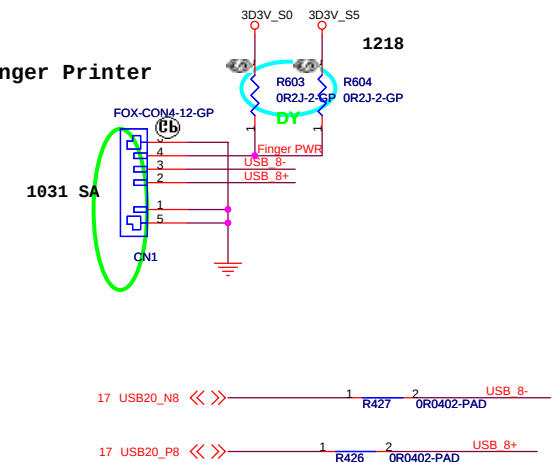
TPM 1.2



Run Power



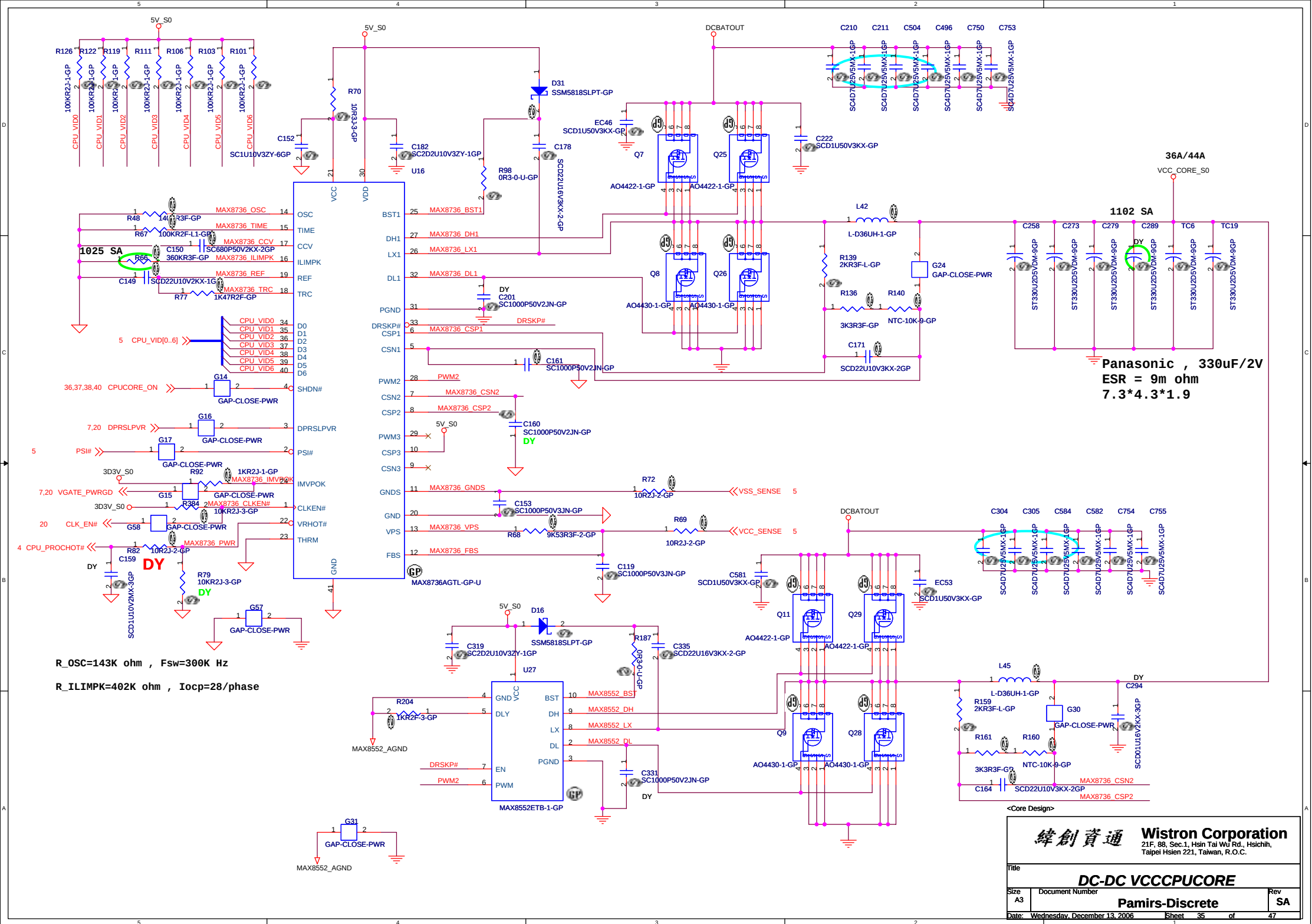
Finger Printer

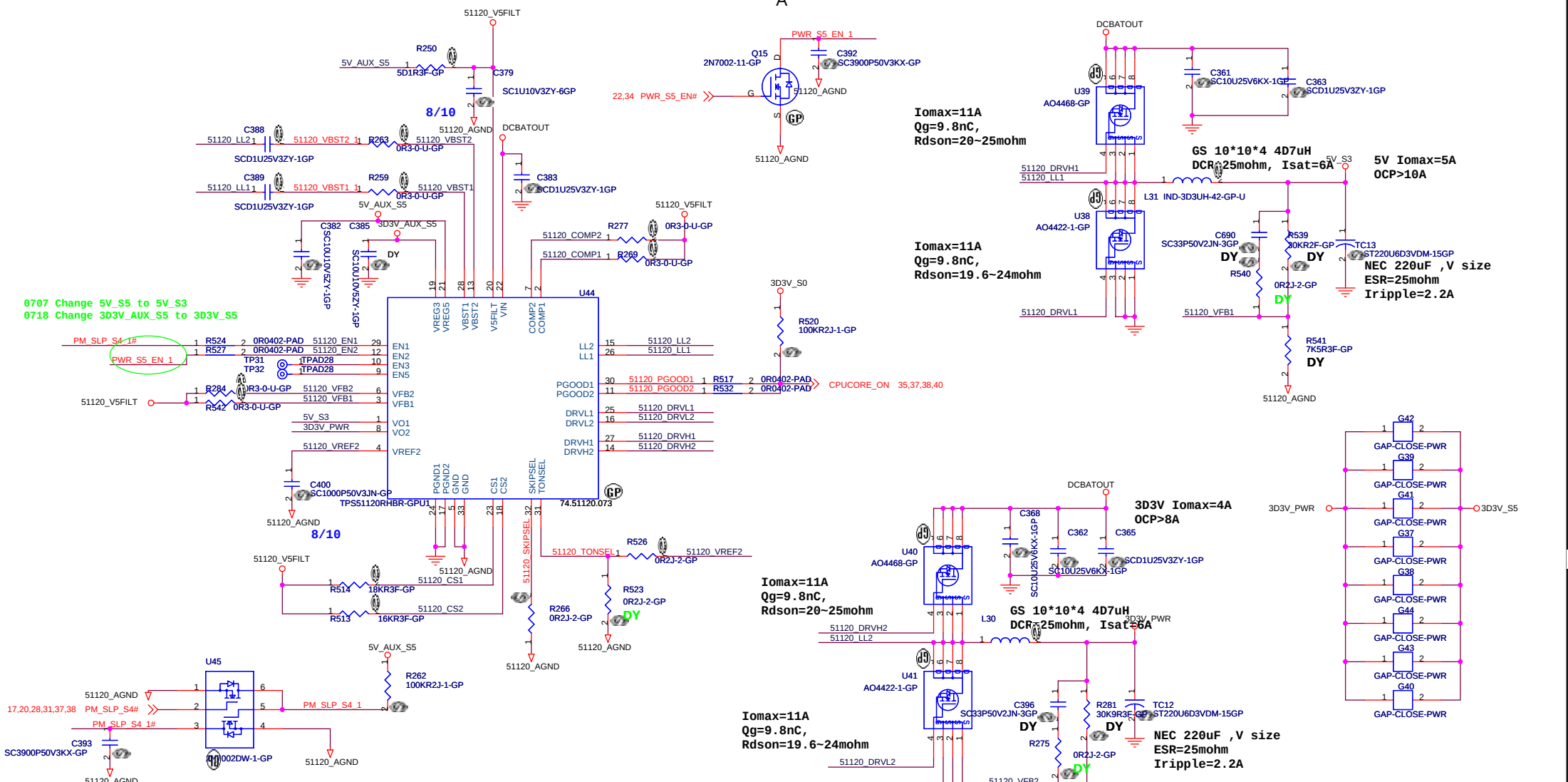


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Title			
PWRPLANE&RESETLOGIC			
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	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	switcher OFF	not use	Switchchr ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

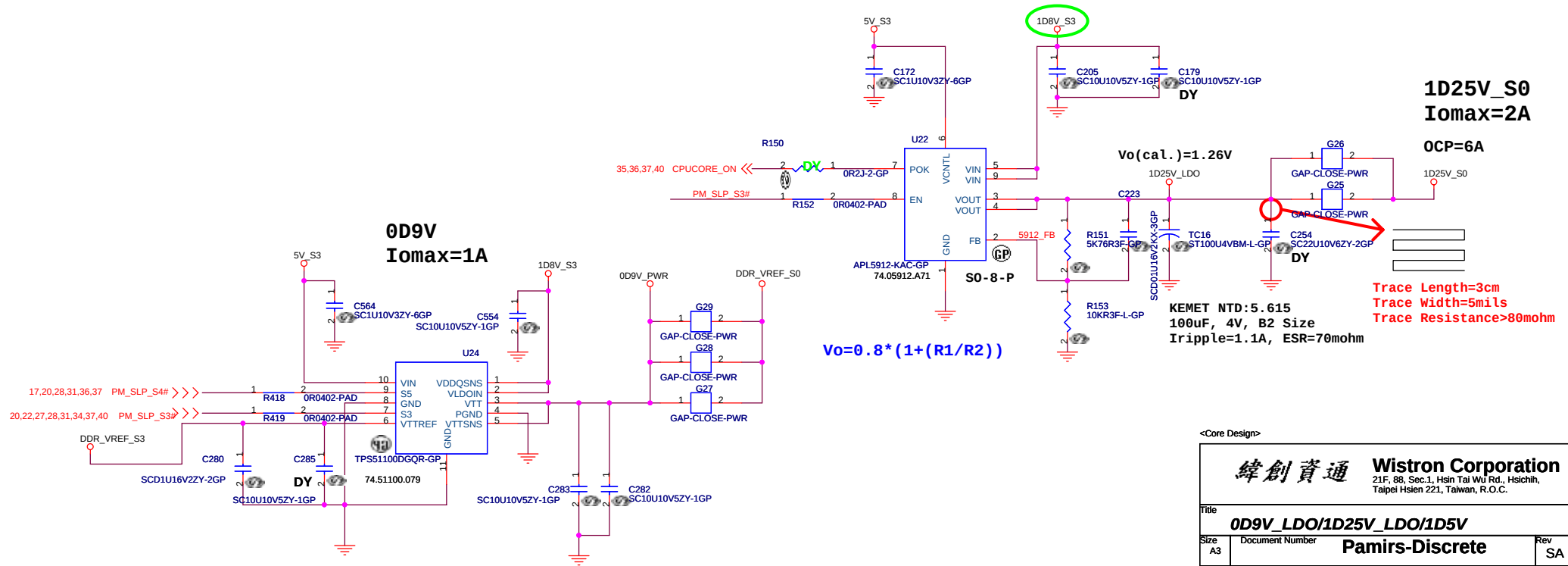
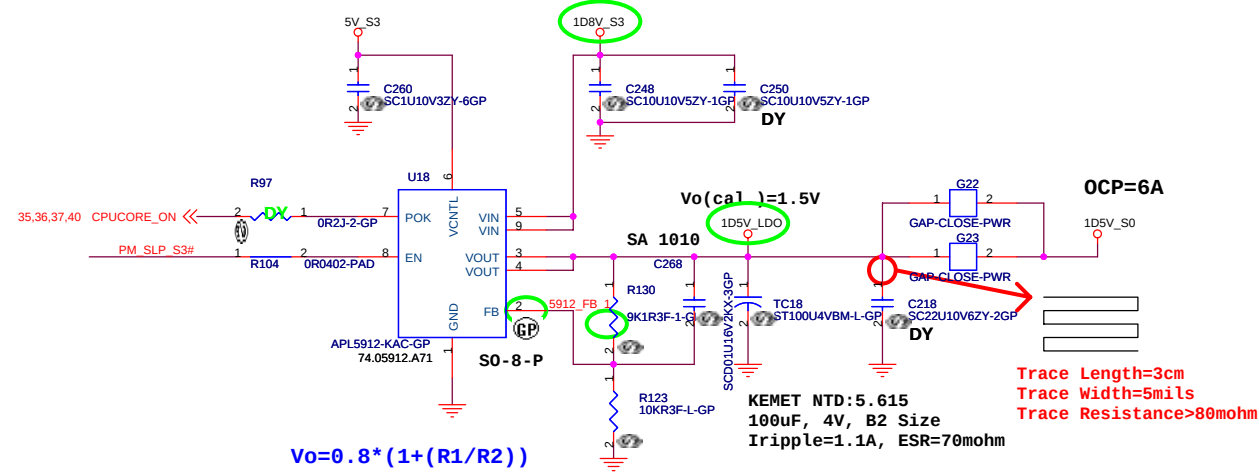
Vout=1V* (R1+R2) /R2

For TPS51120,
Vout=5V

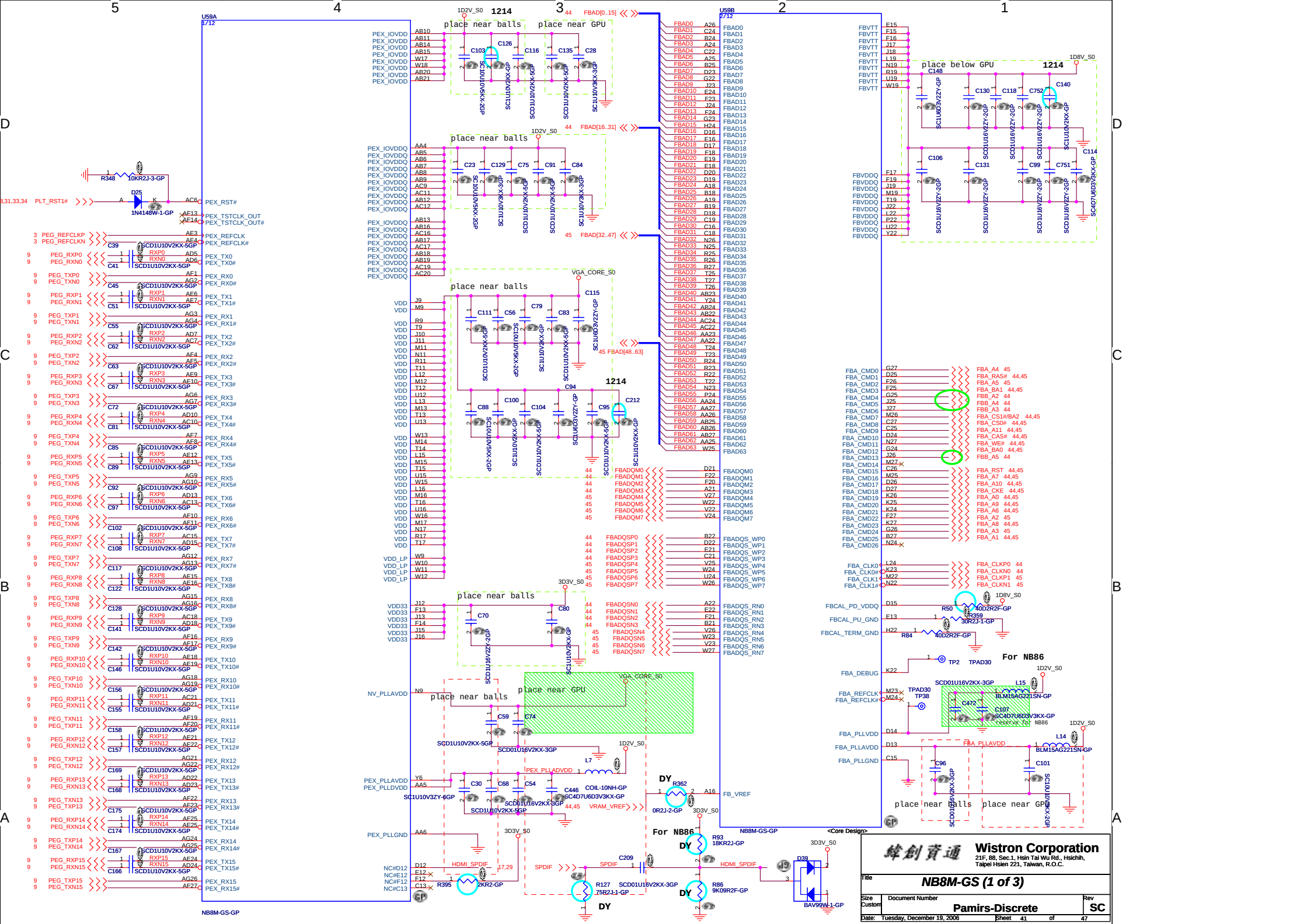
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

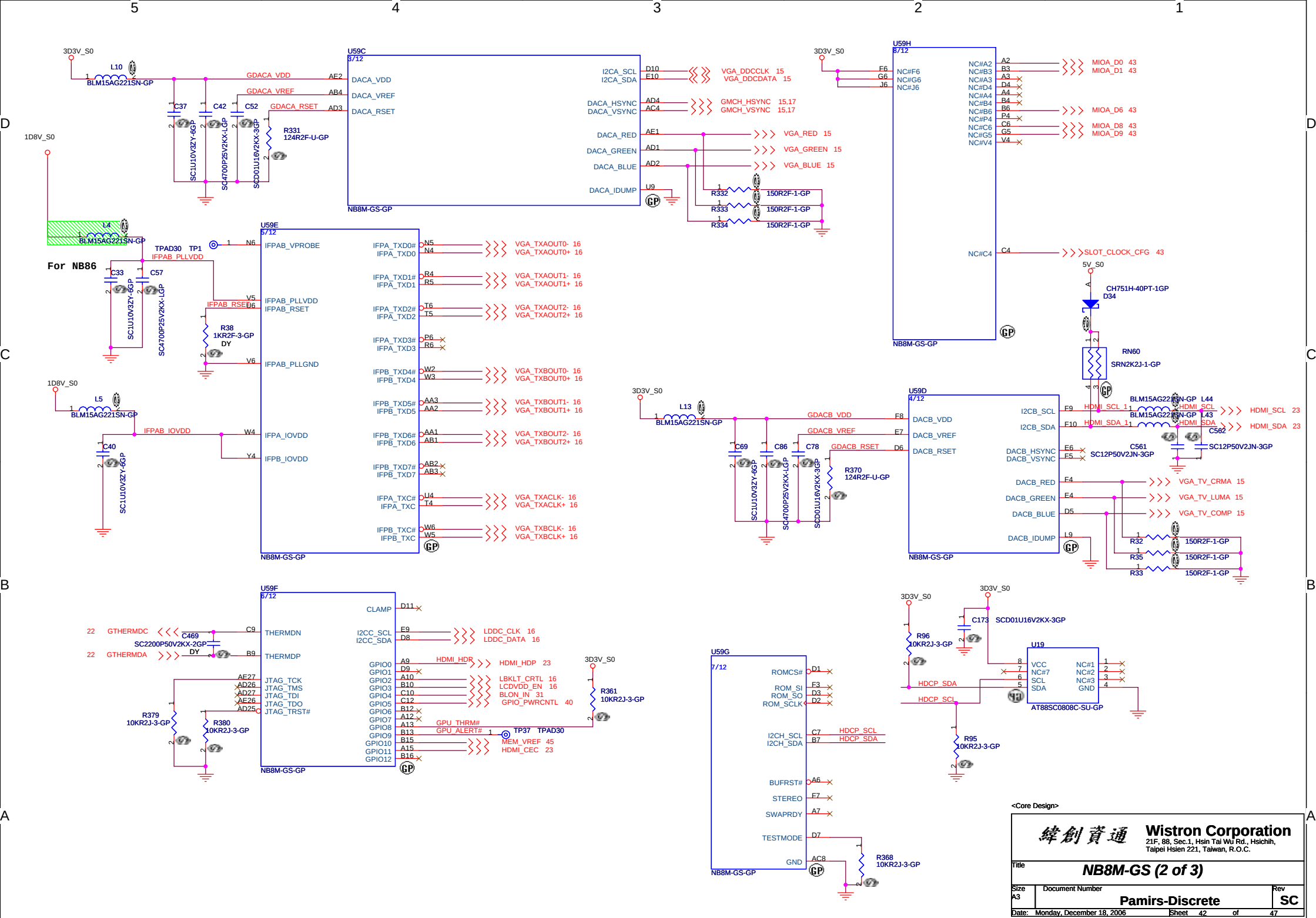
Vout=3.3V

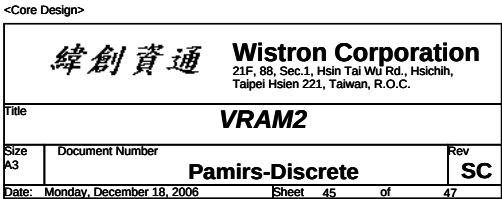
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.











[illegible]

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AD/BATT CONN			
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