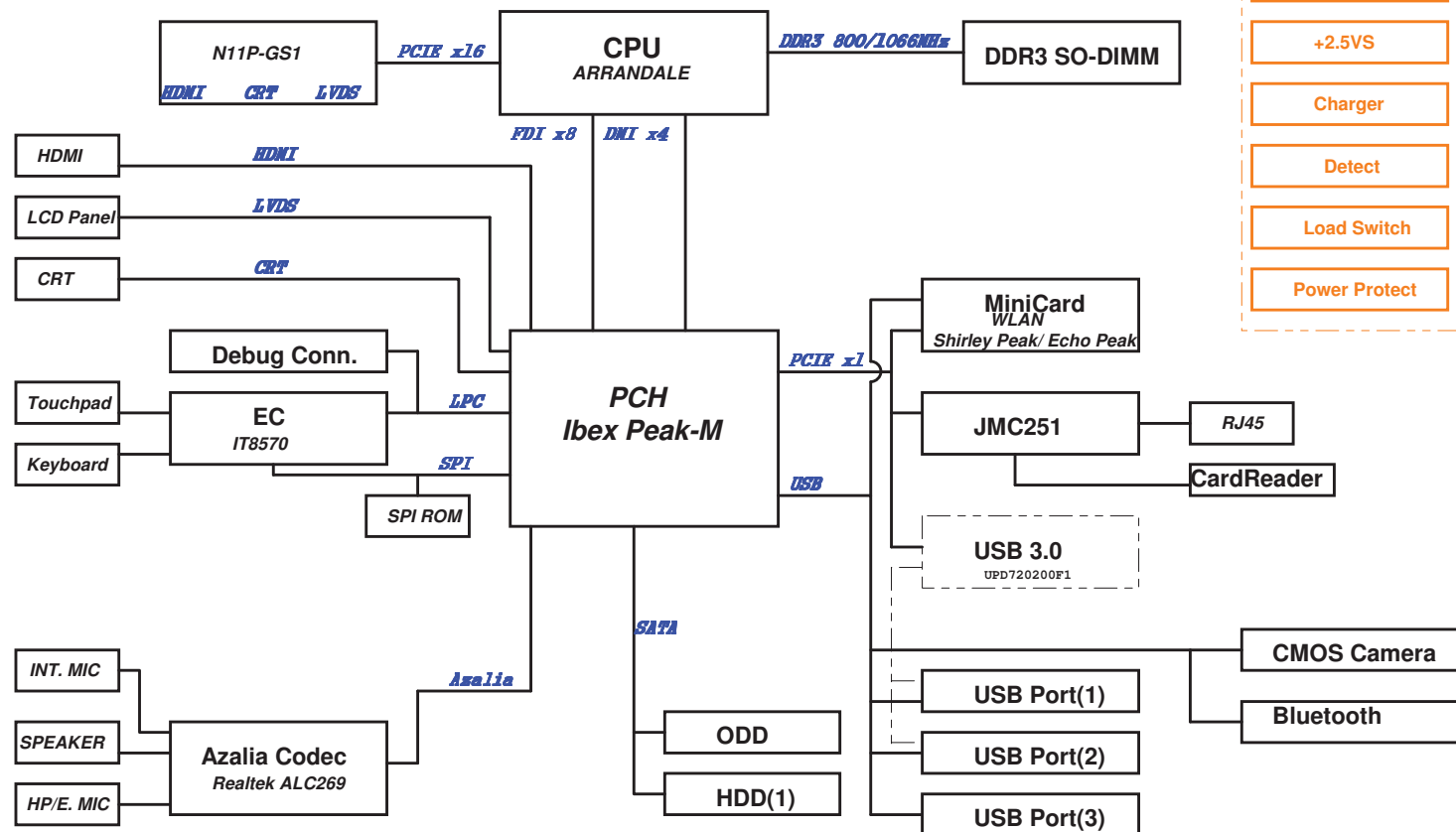


K42Jv SCHEMATIC Revision 2.0

BLOCK DIAGRAM



Power

VCORE

System

1.5VS & 1.05VS

DDR & VTT

+2.5VS

Charger

Detect

Load Switch

Power Protect

PAGE

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PCH IBEX GPIO

PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	GPO	-	-	+3VS
GPIO 01	GPO	-	INT TBD	+3VS
GPIO [2:5]	Native	-	EXT PU	+5VS
GPIO 06	GPO	-	INT TBD	+3VS
GPIO 07	GPI	USB30_SMIB	EXT PU	+3VS
GPIO 08	GPI	EC_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	OC5#	EXT PU	+3VSUS
GPIO 10	Native	OC6#	EXT PU	+3VSUS
GPIO 11	GPI	EC_SCI#	EXT PU	+3VSUS
GPIO 12	Native	-	EXT PU	+3VSUS
GPIO 13	GPO	-	-	+3VSUS
GPIO 14	Native	OC7#	EXT PU	+3VSUS
GPIO 15	GPO	-	INT PD	+3VSUS
GPIO 16	GPO	DGPU_HOLD_RST#	EXT PU	+3VS
GPIO 17	GPI	DGPU_PWRGD_PCH	EXT PD	+3VS
GPIO 18	Native	CLK_REQ1#	EXT PU	+3VS
GPIO 19	GPO	-	-	+3VS
GPIO 20	Native	CLKREQ2_WLAN#_R	EXT PD	+3VS
GPIO 21	GPO	-	-	+3VS
GPIO 22	GPO	WLAN_BT_LED	EXT PD	+3VS
GPIO 23	Native	LPC_DRQ#1	-	+3VS
GPIO 24	GPO	-	-	+3VSUS
GPIO 25	Native	CLK_REQ3#	EXT PU	+3VSUS
GPIO 26	Native	CLK_REQ4#(USB 3.0)	EXT PU	+3VSUS
GPIO 27	Native	PCH_VRM_EN	INT WEAK PU	+3VSUS
GPIO 28	GPO	WLAN_ON	-	+3VSUS
GPIO 29	GPO	-	-	+3VSUS
GPIO 30	Native	ME_SusPwrDnAck	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU	+3VSUS
GPIO 32	Native	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPI	PCH_SPI_OV_RW	INT WEAK PU	+3VS
GPIO 34	Native	STP_PCI#	EXT PU	+3VS
GPIO 35	Native	SATACLKREQ#	EXT PD	+3VS
GPIO 36	GPO	DGPU_PWR_EN#	EXT PU	+3VS
GPIO 37	GPI	DGPU_PRSENT#	EXT PD	+3VS
GPIO 38	GPI	PCB_ID0	EXT PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PD	+3VS
GPIO 40	Native	USB_OC2#	EXT PU	+3VSUS
GPIO 41	Native	OC2#	EXT PU (Not used)	+3VSUS
GPIO 42	Native	OC3#	EXT PU (Not used)	+3VSUS
GPIO 43	Native	OC4#	EXT PU (Not used)	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU (Not used)	+3VSUS
GPIO 45	Native	CLK_REQ6#	EXT PU (Not used)	+3VSUS
GPIO 46	Native	CLK_REQ7#	EXT PU (Not used)	+3VSUS
GPIO 47	Native	PECLK_REQ#	EXT PU	+3VSUS
GPIO 48	GPO	-	EXT PU	+3VS
GPIO 49	GPO	PCH_TEMP_EN	EXT PU	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU (Not used)	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS
GPIO 52	GPO	DGPU_SELECT#	EXT PU	+5VS
GPIO 53	GPO	PCI_GNT2#	INT PU	+3VS
GPIO 54	GPO	-	-	+5VS
GPIO 55	Native	PCI_GNT3#	INT PU	+3VS
GPIO 56	Native	CLKREQ2_GLAN#_R	EXT PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU(DIODE)	+3VSUS
GPIO 58	Native	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	USB_OC01#	EXT PU	+3VSUS
GPIO 60	GPO	-	-	+3VSUS
GPIO 61	Native	PM_SUS_STAT#	-	+3VSUS
GPIO 62	Native	SUS_CLK	-	+3VSUS
GPIO 63	Native	PM_SLP_S5#	-	+3VSUS
GPIO 64	Native	CLK_OUT0	INT TBD	+3VS
GPIO 65	Native	CLK_OUT1	INT TBD	+3VS
GPIO 66	Native	EDID_SELECT#	INT TBD	+3VS
GPIO 67	Native	CLK_OUT3	INT TBD	+3VS
GPIO 72	GPO	PM_BATLOW#	EXT PU (Not used)	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU (Not used)	+3VSUS
GPIO 74	GPO	-	EXT PU (Not used)	+3VSUS
GPIO 75	Native	SML1_DATA	EXT PU	+3VSUS

EC IT8570

EC GPIO	Use As	Signal Name
GPA0	O	PWR_LED#
GPA1	O	CHG_LED#
GPA2	O	CHG_FULL_LED#
GPA3	-	-
GPA4	O	LCD_BL_PWM
GPA5	O	FAN0_PWM
GPA6	-	-
GPA7	-	-
GPB0	O	BATSEL_0
GPB1	O	BATSEL_1
GPB2	O	ME_AC_PRESENT
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	O	A20GATE
GPB6	O	KB_RST#
GPB7	O	PM_RSMRST#
GPC0	O	CLK_UC
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5	O	OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	-	-
GPD0	-	-
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	O	EC_SCI#
GPD4	O	EC_SMI#
GPD5	O	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7	I	HDMI_HPD
GPE0	-	-
GPE1	-	-
GPE2	-	-
GPE3	-	-
GPE4	I	PWR_SW#
GPE5	-	-
GPE6	I	LID_SW#
GPF0	-	-
GPF1	O	VSUS_ON
GPF2	O	VTT_DRAM_PWR_SEL1
GPF3	O	VTT_DRAM_PWR_SEL2
GPF4	IO	TP_CLK
GPF5	IO	TP_DAT
GPF6	O	THRO_CPU
GPF7	O	PCH_SPI_OV
GPG0	I	ME_SusPwrDnAck_EC
PGP1	I	PM_SUSB#
PGP2	-	-
PGP6	-	-
GPH0	IO	PM_CLKRUN#
GPH1	O	VGA_DEEPIPLE (TBD)
GPH2	O	CHG_EN
GPH3	O	SUSC_EC#
GPH4	O	SUSB_EC#
GPH5	-	-
GPH6	O	CAP_LED#
GPI0	I	GPU_ALERT#
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	PCH_TEMP_ENABLE
GPI5	I	CPU_VCORE_I_SEN
GPI6	I	DGPU_VCORE_I_SEN
GPI7	-	-
GPJ0	O	CPU_VRON
GPJ1	O	PM_PWROK
GPJ2	O	VSET_EC
GPJ3	O	ISET_EC
GPJ4	O	VRM_TEMP_OV_PROT
GPJ5	O	VRM_TEMP_PROT

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	SM-Bus Address	
Clock Generator(ICS9LV53162)	1101001x (D2)	
SO-DIMM 0	1010000x (A0)	
SO-DIMM 1	1010001x (A4)	
WiFi/WiMax	N/A	
EC Master (SMB1)		
SM-Bus Device	SM-Bus Address	
VGA Thermal IC(G781-1)	1001101x (9A)	

PCIE 1		USB 0	USB Port (1)
PCIE 2	Minicard WLAN	USB 1	USB Port (2)
PCIE 3		USB 2	USB Port (3)
PCIE 4	USB 3.0	USB 3	
PCIE 5		USB 4	
PCIE 6	GLAN	USB 5	
PCIE 7		USB 6	
PCIE 8		USB 7	
		USB 8	WLAN
		USB 9	CMOS Camera
		USB 10	
		USB 11	
		USB 12	Bluetooth
		USB 13	

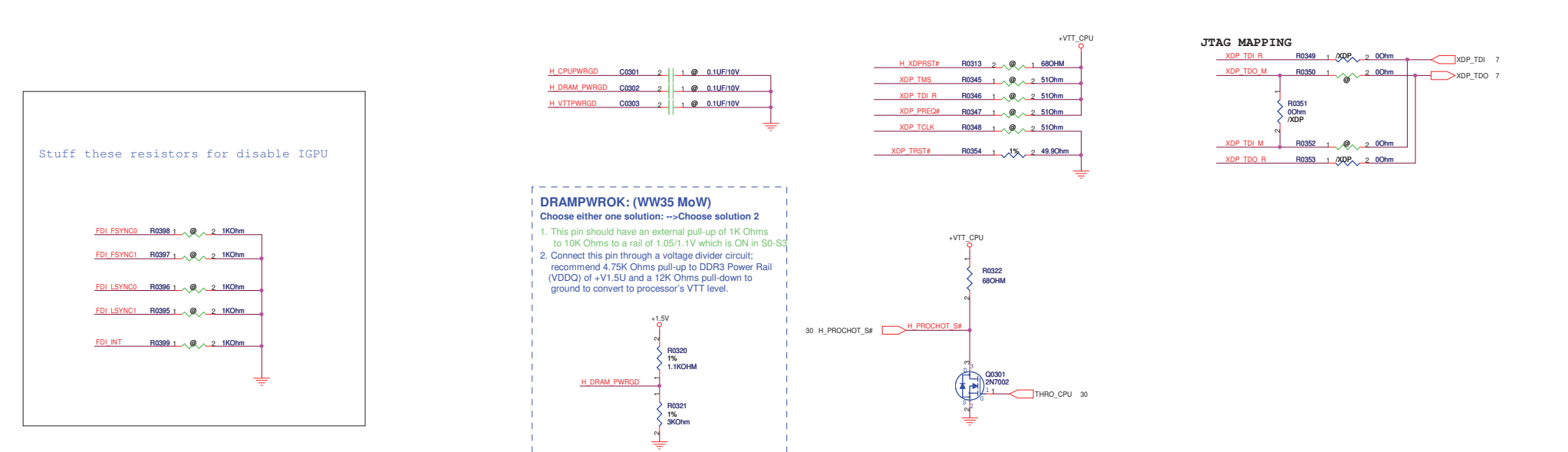
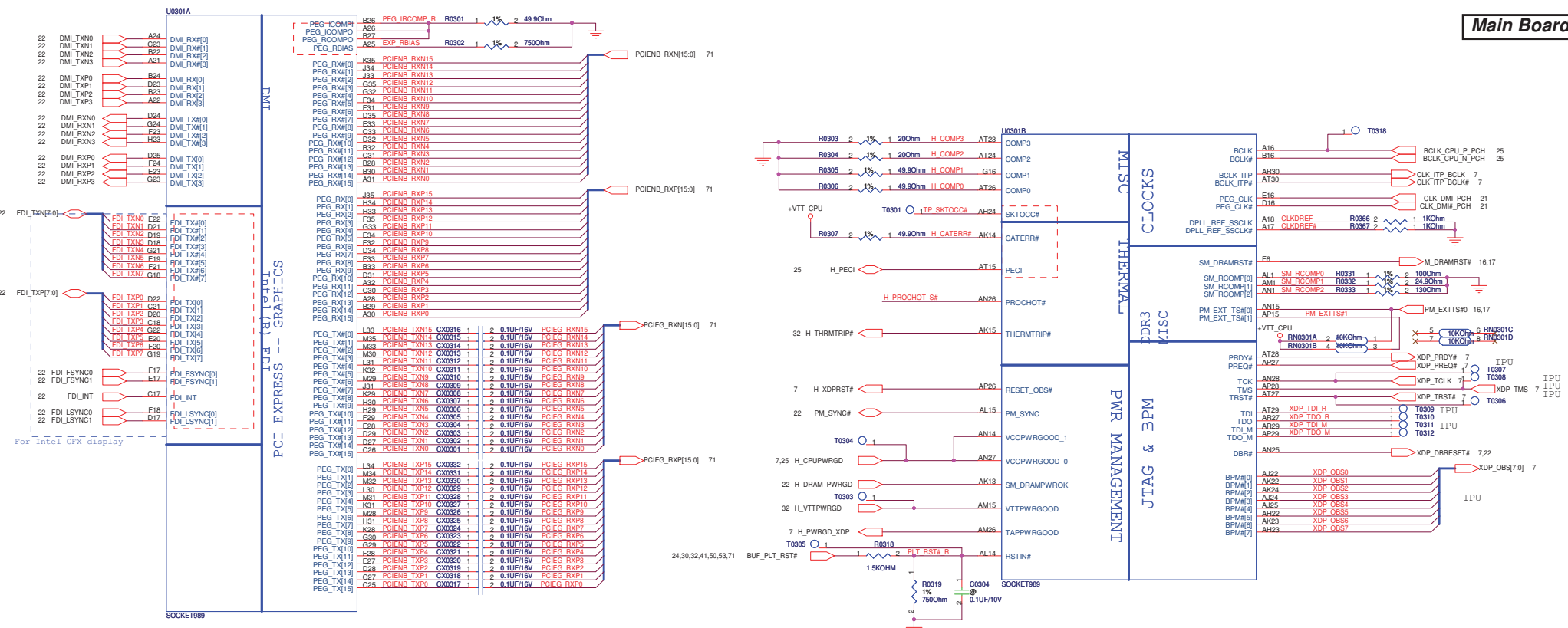
SATA 0	SATA HDD (1)
SATA1	SATA ODD

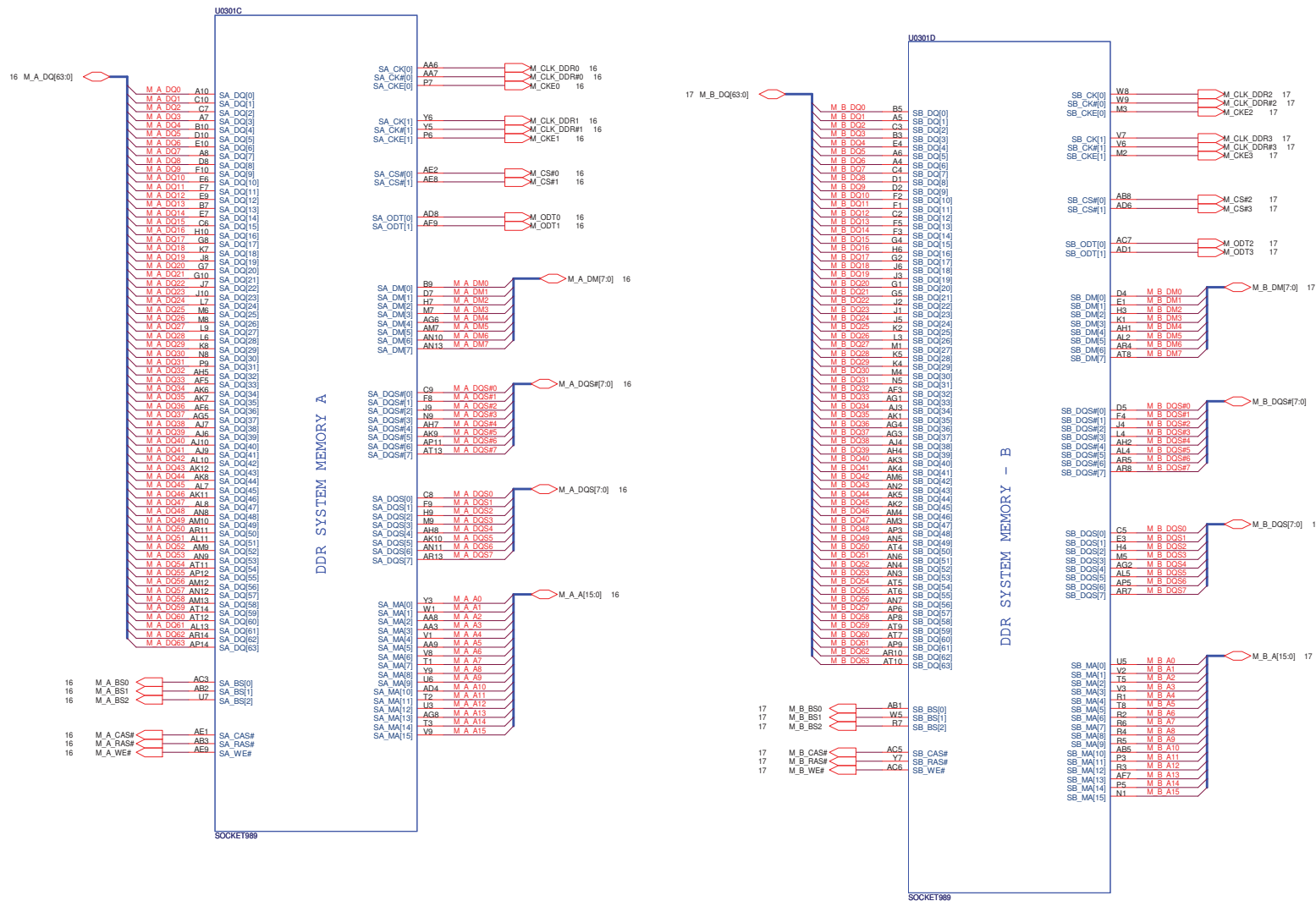


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 ASUSTek COMPUTER INC. N/A
 Engineer: JAY TSAI

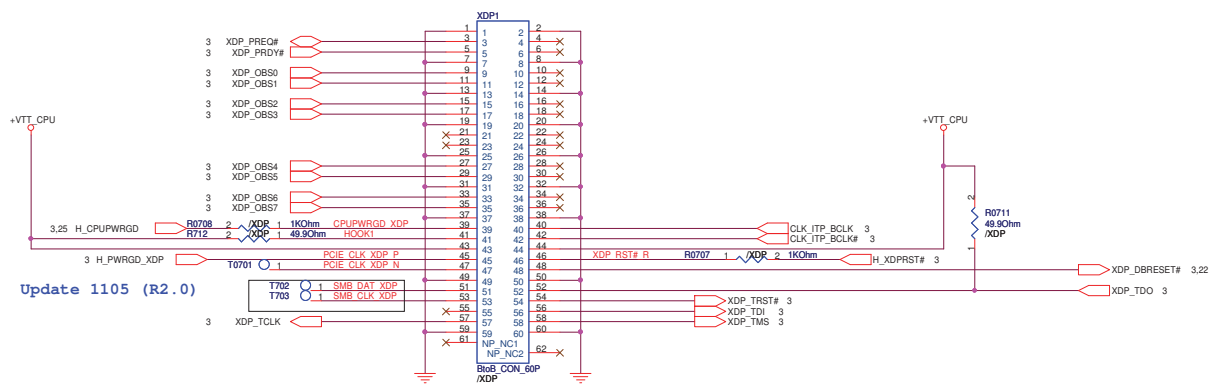
Size C	Project Name	K42Jv	Rev 1.01
Date: Thursday, February 11, 2010	Sheet	2	of 95

Main Board





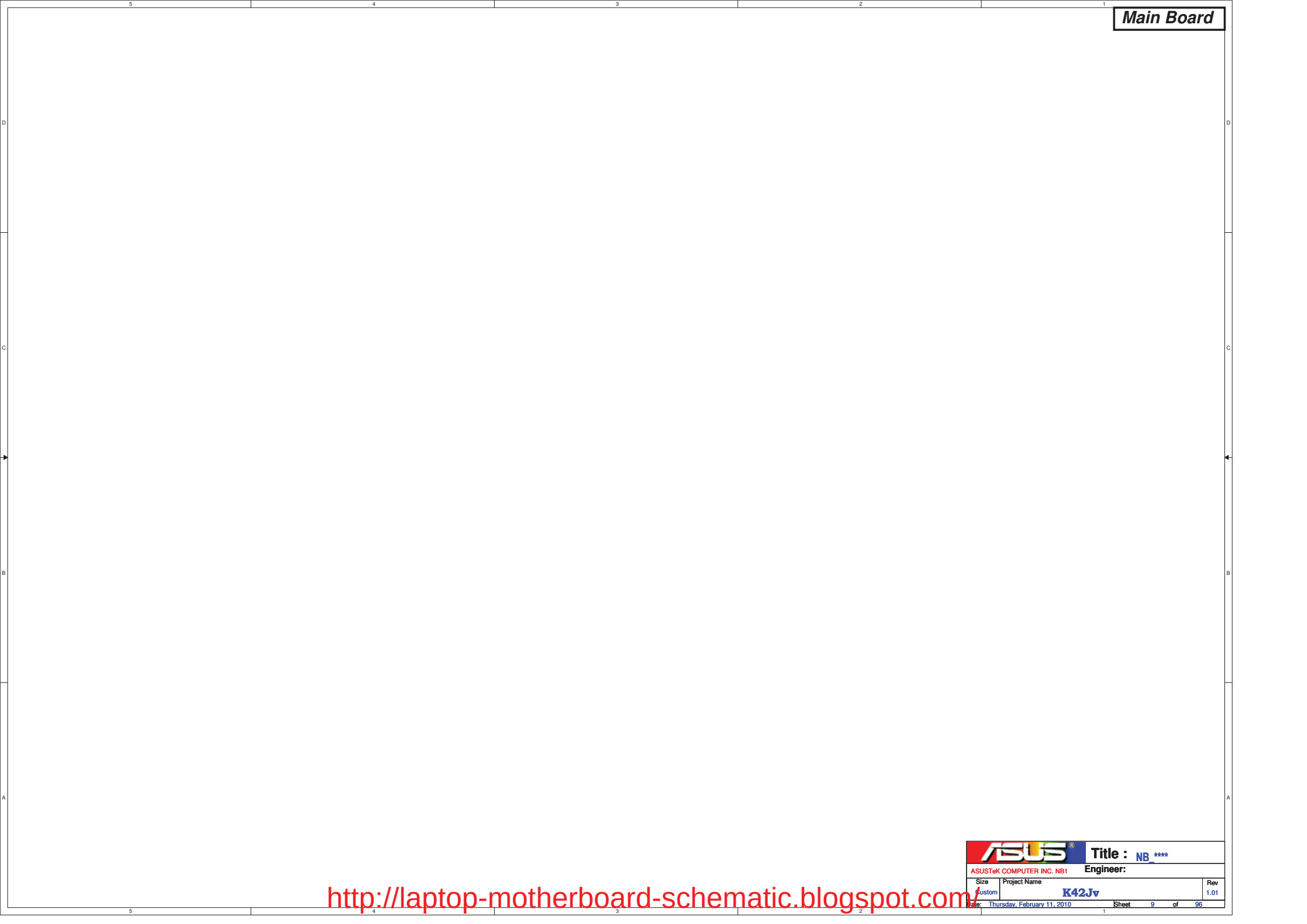
CPU XDP connector

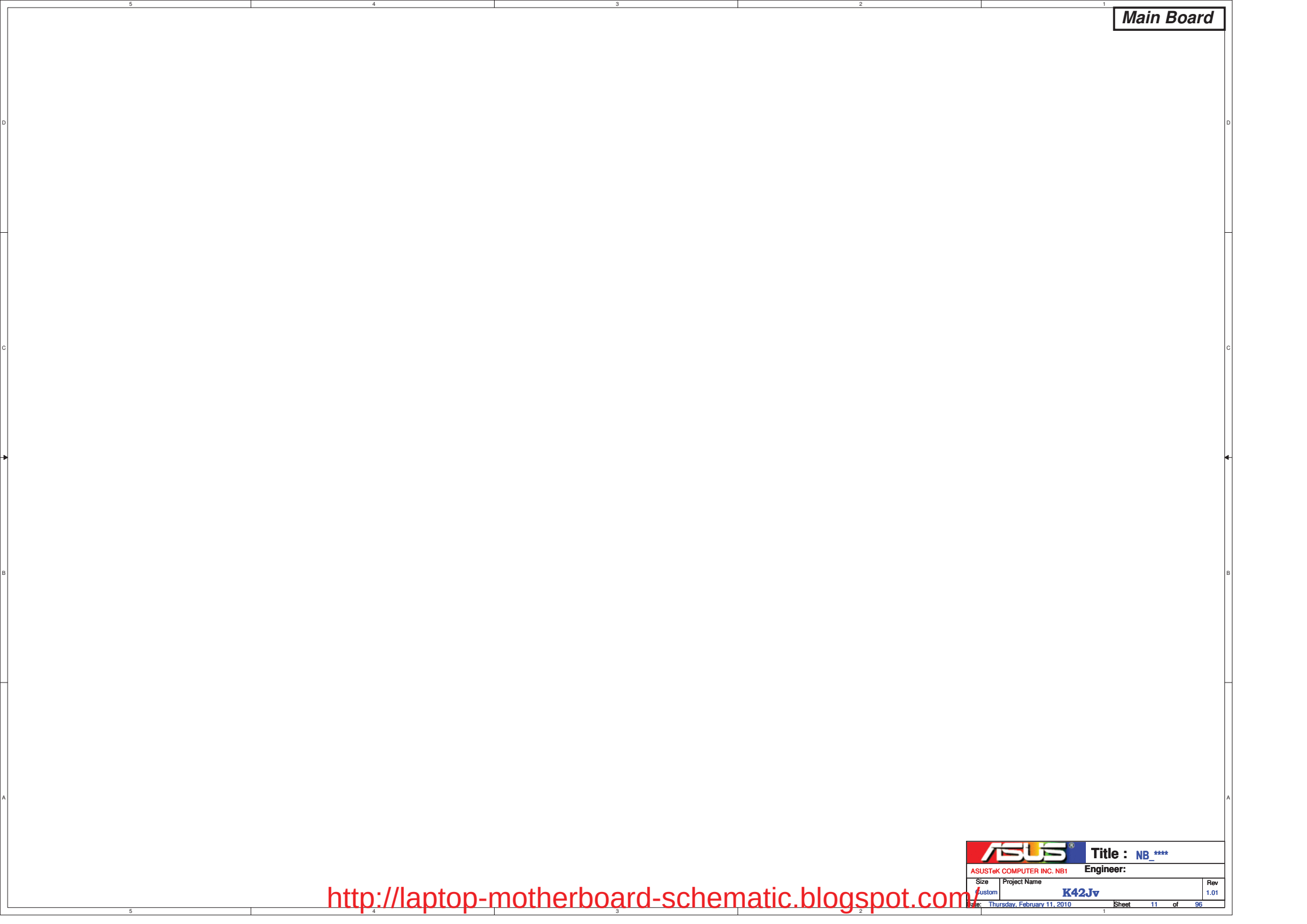


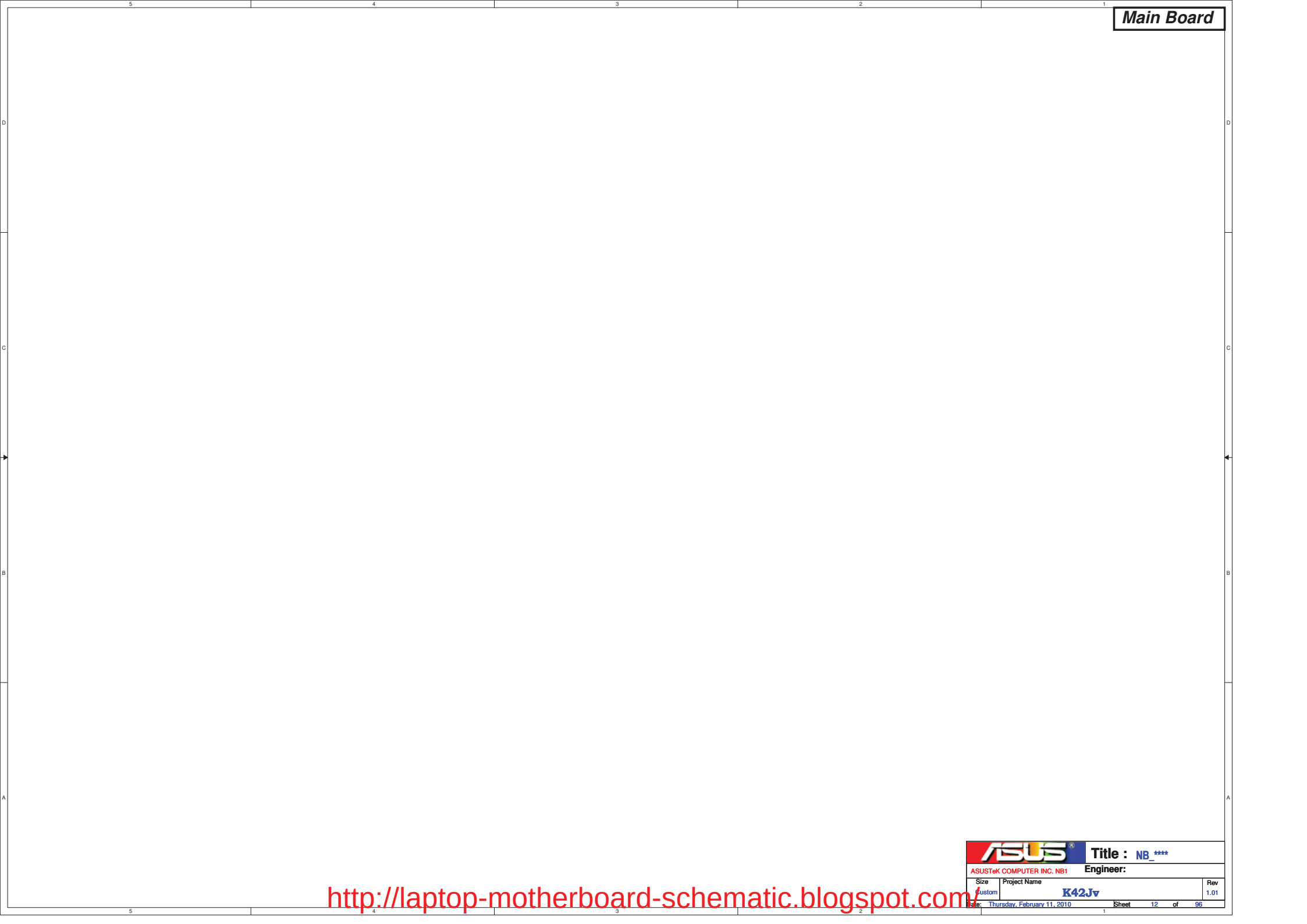
Update 1105 (R2.0)



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ASUSTeK COMPUTER INC. NB1		Engineer:	
Size	Project Name		Rev
Custom	K42Jv		1.01
Date: Thursday, February 11, 2010		Sheet	8 of 96









Title : NB ****

ASUSTeK COMPUTER INC. NB1

Engineer:

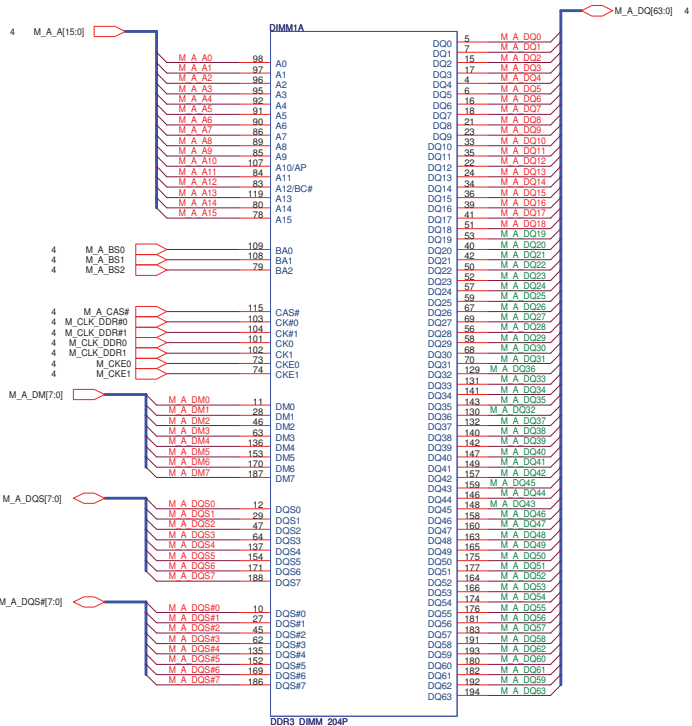
Size	Project Name	Rev
Custom	K42Jv	1.01
Date: Thursday, February 11, 2010		Sheet 12 of 96



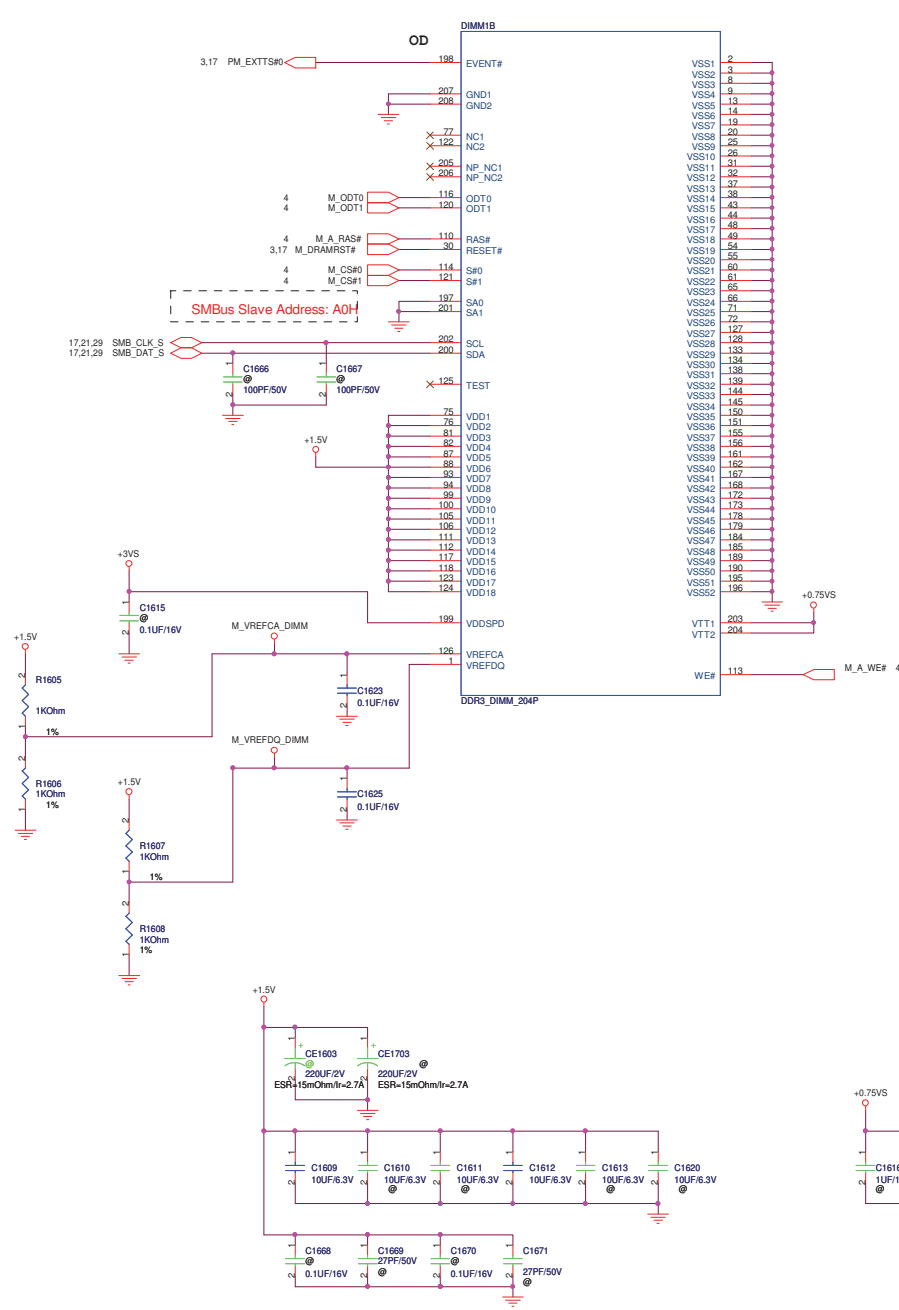
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ASUSTeK COMPUTER INC. NB6		Engineer:	
Size A	Project Name K42Jv		Rev 1.01
Date Tuesday, February 1, 2010	Sheet 14	of 96	



		Title :	
ASUSTeK COMPUTER INC. NB6		Engineer:	
Size	Project Name		Rev
A	K42Jv		1.01
Date	Tuesday, February 1, 2011		Sheet 15 of 96



REV 9.2mm



Layout Note: Place these caps near SO DIMMS

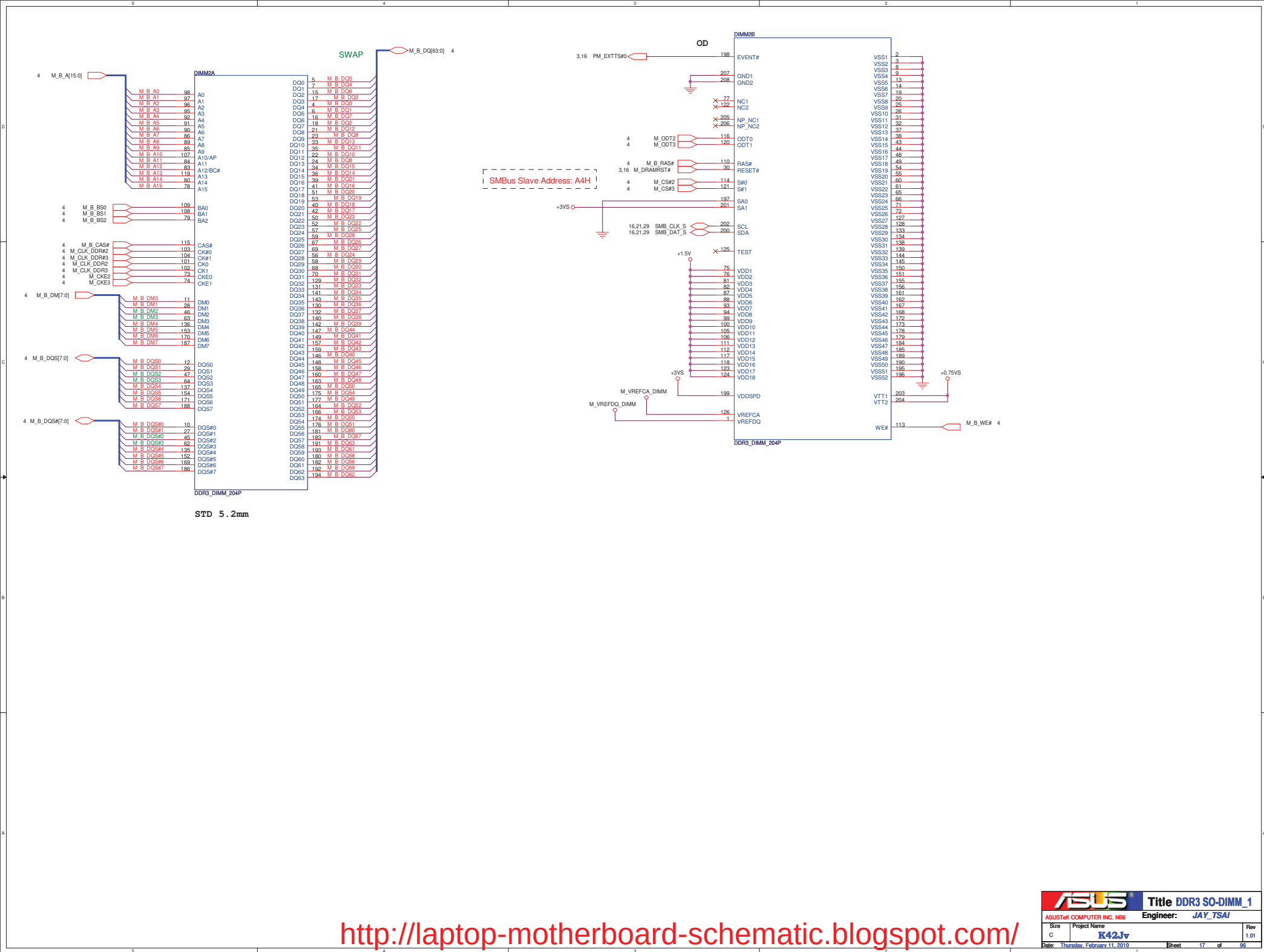


Table 2-28. Functional Strap Definitions (Sheet 1 of 5)

Signal	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PWROK	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# de-asserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (the PCH will disable the TCO Timer system reboot feature). The status of this strap is readable using the NO_REBOOT bit (Chipset Config Registers: Offset 3410h:bit 5).
INT3_V#	Reserved	Rising edge of PWROK	This signal has a weak internal pull up. Note: the internal pull-up is disabled after PLTRST# de-asserts. NOTE: This signal should not be pulled low.
GNT[3]# / GPIO[55]	Top-Block Swap Override	Rising edge of PWROK	The signal has a weak internal pull-up. Note: the internal pull-up is disabled after PCIRST# de-asserts. If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode (the PCH inverts ALG for all cycles targeting BIOS space). The status of this strap is readable using the Top Swap bit (Chipset Config Registers: Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable	Always	Integrated 1.05 V VRMs is enabled when high. NOTE: This signal should always be pulled high

Table 2-28. Functional Strap Definitions (Sheet 2 of 5)

Signal	Usage	When Sampled	Comment															
			This signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.															
GNT1# / GPIO51	Boot BIOS Strap bit [1] BBS[1]	Rising edge of PWROK	<table><tr><th>Bit11</th><th>Bit 10</th><th>Boot BIOS Destination</th></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>PCI</td></tr><tr><td>1</td><td>1</td><td>SPI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table> NOTE: If option 00 LPC is selected, BIOS may still be placed on LPC; however, all platforms with the PCH require SPI flash connected directly to the PCH SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® Management Engine or Integrated GbE LAN.	Bit11	Bit 10	Boot BIOS Destination	0	1	Reserved	1	0	PCI	1	1	SPI	0	0	LPC
Bit11	Bit 10	Boot BIOS Destination																
0	1	Reserved																
1	0	PCI																
1	1	SPI																
0	0	LPC																

Table 2-28. Functional Strap Definitions (Sheet 5 of 5)

Signal	Usage	When Sampled	Comment
SDVO_CTRLDA TA	Digital Display Port (Port B)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port B is enabled when sampled high. When sampled low Port B is Disabled.
DDPC_CTRLDA TA	Digital Display Port (Port C)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port C is enabled when sampled high. When sampled low Port C is Disabled.
DDPD_CTRLDA TA	Digital Display Port (Port D)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port D is enabled when sampled high. When sampled low Port D is Disabled.

Table 2-28. Functional Strap Definitions (Sheet 3 of 5)

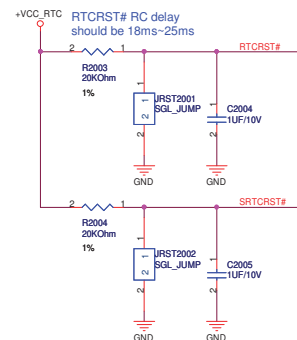
Functional Group Comments (continued)																		
Signal	Usage	When Sampled	Comment															
GNT[0]#	Boot BIOS Strap bit[0] BBS[0]	Rising edge of PWROK	This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap.															
			<table><thead><tr><th>Bit11</th><th>Bit 10</th><th>Boot BIOS Destination</th></tr></thead><tbody><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>PCI</td></tr><tr><td>1</td><td>1</td><td>SPI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	Bit11	Bit 10	Boot BIOS Destination	0	1	Reserved	1	0	PCI	1	1	SPI	0	0	LPC
			Bit11	Bit 10	Boot BIOS Destination													
			0	1	Reserved													
			1	0	PCI													
1	1	SPI																
0	0	LPC																
NOTE: If option 00 LPC is selected, BIOS may still be placed on LPC; however, all platforms with the PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot.																		
NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.																		
GNT2# / GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. Tying this strap low configures DMI for ESI compatible operation. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.															
NV_ALE	Reserved	Rising edge of PWROK	This signal has a weak internal pull down. NOTE: This signal should not be pulled high															

Table 2-28. Functional Strap Definitions (Sheet 4 of 5)

Signal	Usage	When Sampled	Comment
HDA_DOCK_EN# / GPIO[33]	Flash Descriptor Security Override/ ME Debug Mode	Rising edge of PWROK	Signal has a weak internal pull-up. If strap is sampled high, the security measures defined in the Flash Descriptor will be in effect (default). If sampled low, the Flash Descriptor Security will be overridden. This strap should only be asserted low using external pull down in manufacturing/ debug environments ONLY. NOTE: Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel® Management Engine after chipset bringup and disable runtime Intel® Management Engine features. This is a debug mode and must not be asserted after manufacturing/debug.
SPI_MOSI	TPM Functionality Disable	Rising edge of MEPWROK	This signal has a weak internal pull-down resistor. This signal must be sampled low.
NV_CLE	DMI Termination Voltage	Rising edge of PWROK	This signal has a weak internal pull-down.
HDA_SDO	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull down. NOTE: This signal should not be pulled high
GPIO8	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull up. Note that the weak internal pull-up is disabled after RSMRST# de-asserts. NOTE: This signal should not be pulled low
GPIO27	Reserved	Rising edge of RSMRST# pin	This signal should be left as a No Connect.
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	This signal has a weak internal pull down. On-Die PLL VR is supplied by 1.5 V when sampled high; 1.8 V when sampled low.
GPIO15	Reserved	Rising edge of RSMRST# pin	Low = Intel® Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel® Management Engine Crypto TLS cipher suite with confidentiality This signal has a weak internal pull down. NOTE: A strong pull up may be needed for GPIO functionality
L_DDC_DATA	LVDS	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. LVDS is enabled when sampled high. When sampled low LVDS is Disabled.

Request by CSC for CMOS
clear function

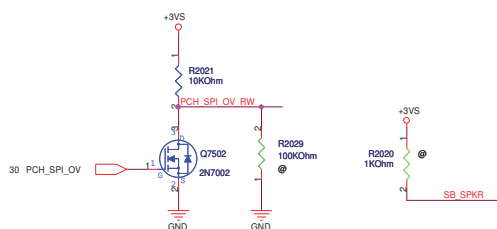
CMOS Settings		JST2001		TPM Settings		JST2002	
Clear CMOS	Shunt	Clear ME RTC Registers		Clear ME RTC Registers	Shunt	Clear ME RTC Registers	
Keep CMOS	Open (Default)	Keep ME RTC Registers		Keep ME RTC Registers	Open (Default)	Keep ME RTC Registers	



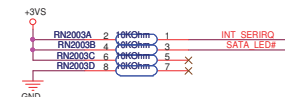
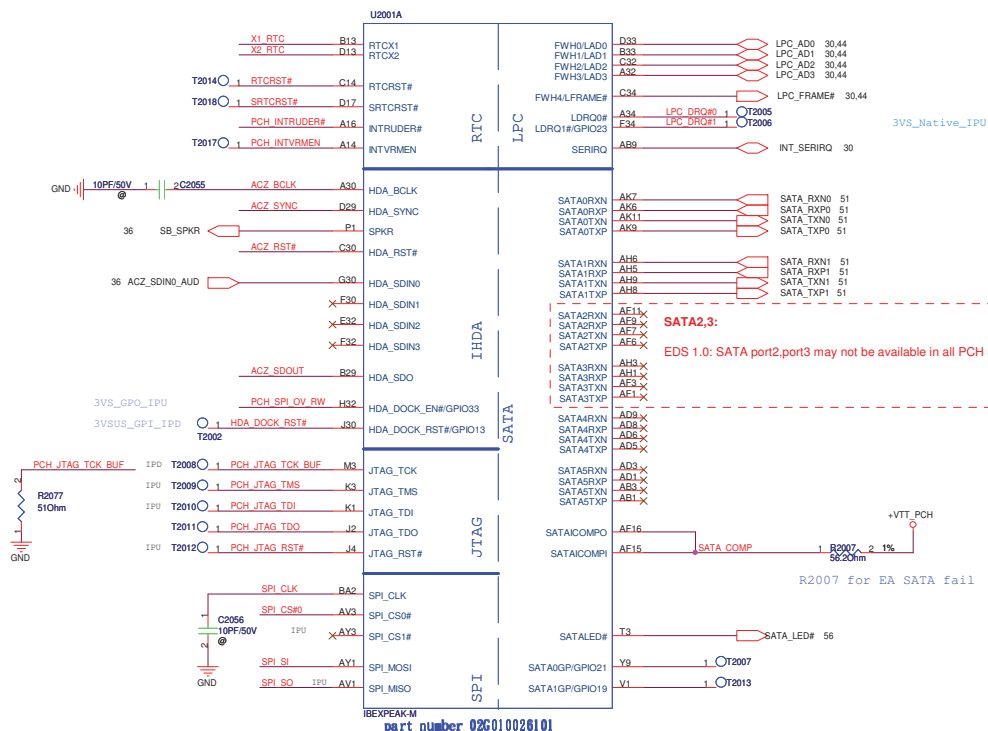
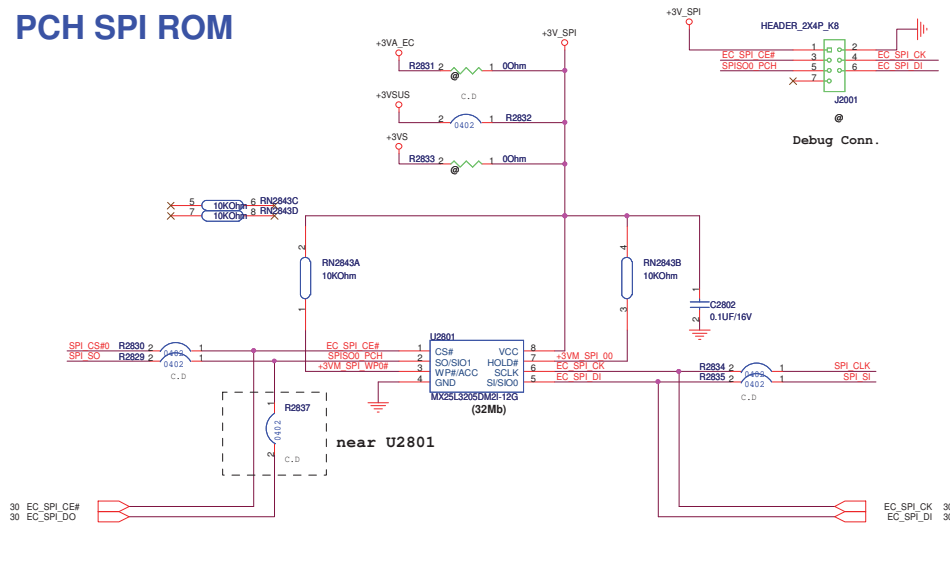
DG2.0 P297
RSTCRST# and SRTCRST# can not be shorted together

Strap information:

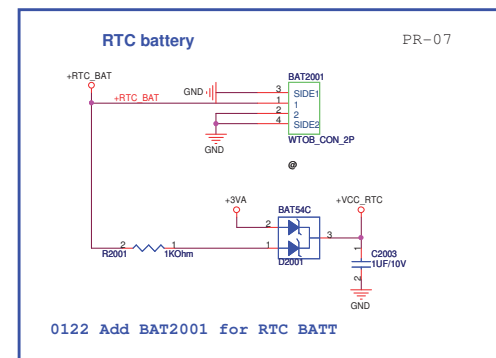
RTCRST# Select VCCVPM 1.5V or 1.8V (IPD)	1.5V	1.8V
SB_SPKR: No reboot strap (IPD)	No reboot	Disable No reboot
PCH_SPI_OV_RW: (IPU)	No Flash ME FW	Flash ME FW
SPI_S1: 1TPM strap. (IPD)	Enable	Disable
PCH_INTVPMEN Integrated 1.05 V VPM Enable /Disable	Enable	Disable



PCH SPI ROM



RTC battery



PCIE2: WLAN

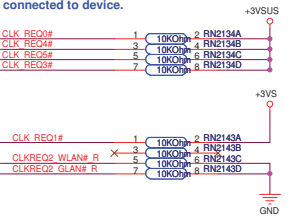
PCIE4: USB30

PCIE6: LAN

PCIE7,8:
EDS 1.0: port7,port8 may not be available in all PCH SKUs.

Note: Place these
resistors near
to PCIe Slots

PCH CLKREQ Setting:
Not connected to device.



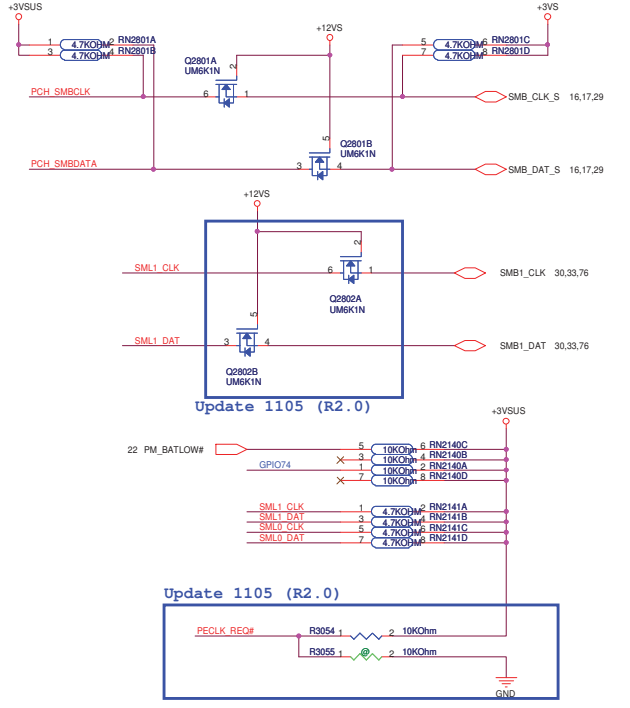
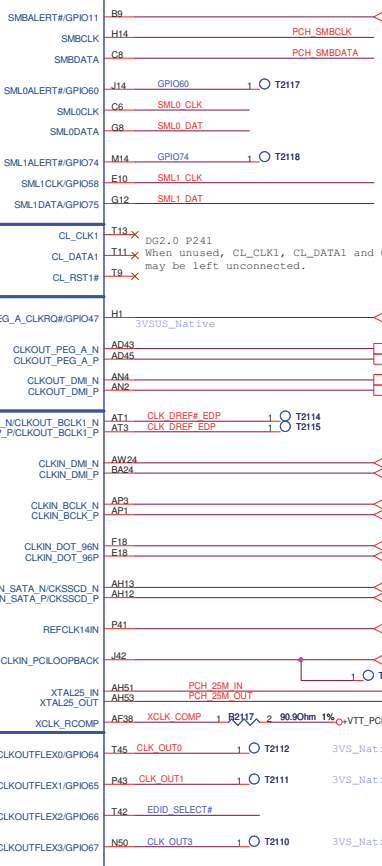
U2001B

PCIE*

Controller Link

From CLK BUFFER

Clock Flex



If not use crystal, please change C1201 to 0 Ohm

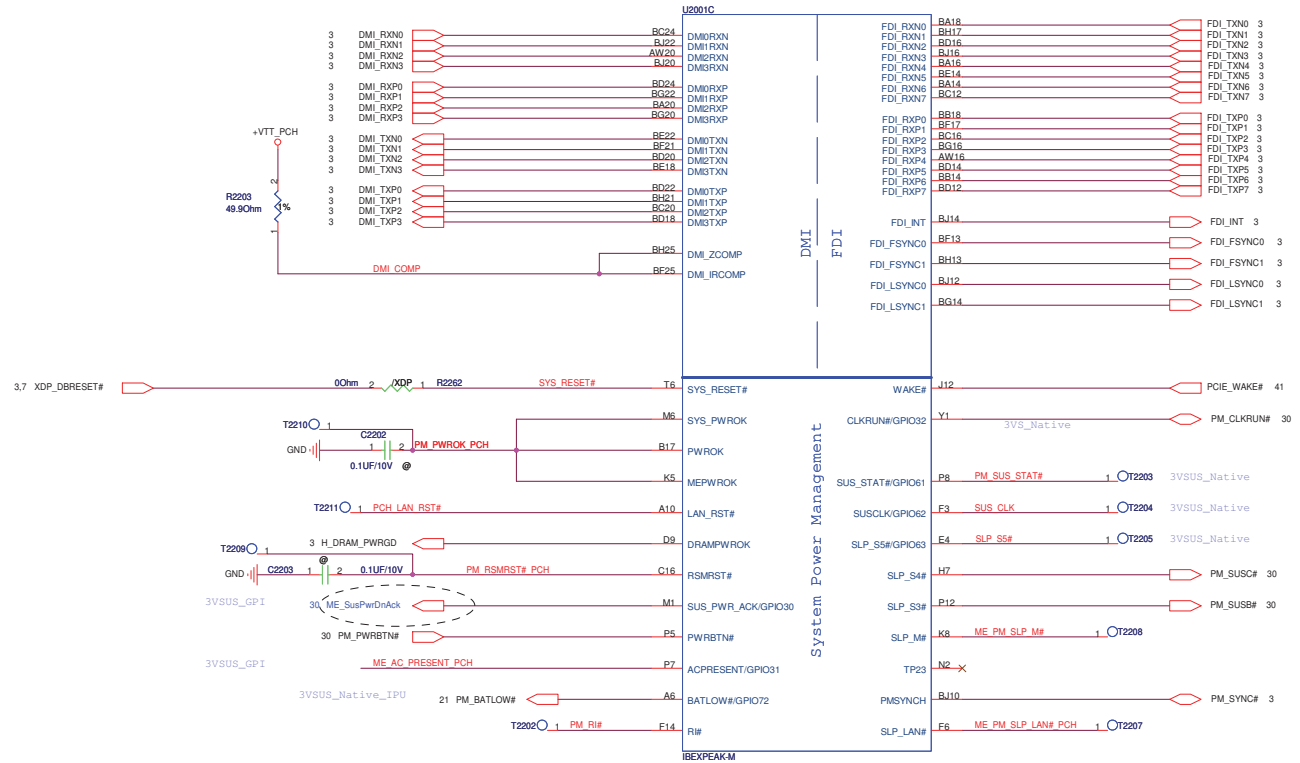
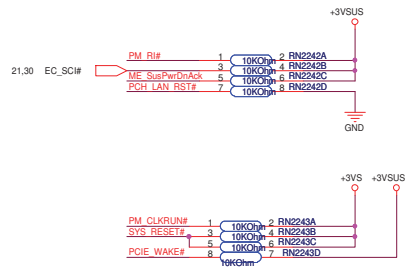
R2120: For Xtal measurement

DG2.0
Section 4.2.4.1: Added 25-MHz Crystal routing guideline.
All Mobile Intel 5 Series Chipset-based Integrated
Graphics platforms are required to use a 25-MHz crystal
on the PCH XTAL25_IN/OUT to enable the PCH to
generate the display clocks. Display Clock generation is
integrated into the PCH.

Integrated Graphics platforms that implement
DVI/DP/HDMI/e-DP are required to use Display Clock
Integration (DCI) (25M crystal to generate PCH display
clocks) to improve signal integrity and mitigate risk of
electrical compliance and associated functional failures

WW35 Update: Integrated Graphics platforms that use
only LVDS and/or VGA Displays may use Buffer Through Mode
(BTM) and leave 25-MHz crystal and RC components
unsnuffed

pre-ES1 not support
Reversal Feature



R1.1,item L15

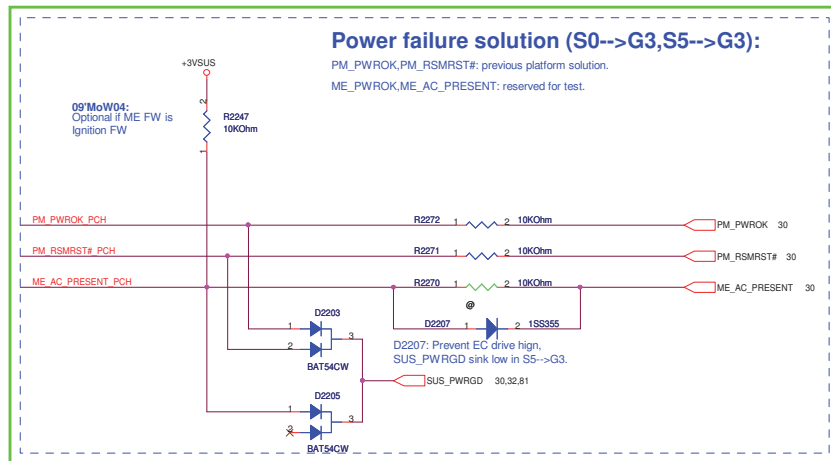
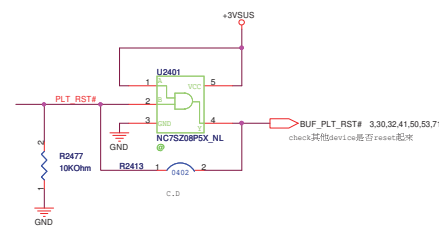


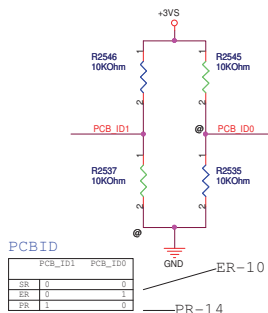
Table 112. Intel ME-EC Interaction Signal List with and without M3 Support

Signal Name	Platform with M3 Support (e.g., Intel® AMT)	Platform without M3 Support (e.g., Intel® ME Ignition Firmware)
SUS_PWR_DN_ACK (GPIO30)	Required	Required
ACPRESENT (GPIO31)	Required	Required Note: Optional if Intel ME FW is Intel® ME Ignition Firmware
SLP_M#	Required	Optional (Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_M# becomes required from Intel® ME-EC perspective.
SLP_S3#	Optional	Required Note: If SLP_M# is routed from PCH to EC, then SLP_S3# can be optional from Intel ME-EC perspective

NOTE: Optional means that these signals are optional from Intel ME-EC interaction point of view. However, they are platform critical signals and are still required to be routed on the platform.

ME Ignition Firmware is for 2MB SPI core, only PM55 can support on it.





All GPIOs are reset to the default state by CF9h reset except GPIO24.

GPIO 27=Enable VCCVRM
Low=disable.
Default internal pull up.

POWER按照提供的default值調節電壓

3VS_GPI
3VS_GPI_IPU
3VS_GPI_IPU
3VS_GPI_IPU
3VSUS_GPO_IPU
3VSUS_GPI
3VSUS_GPO_IPD
3VS_GPI
3VS_GPI_IPU
3VS_GPI_IPU
3VSUS_GPO
3VSUS_GPO_IPU
3VSUS_GPI_IPU
3VS_GPI
3VS_GPI
3VS_GPI
3VS_GPI
3VSUS_Native_IPU
3VSUS_Native
3VS_GPI
3VS_GPI
3VS_GPI
3VSUS_GPI

T2550 1 GPIO0
T2549 1 GPIO1
T2551 1
50 USB30_SMIB
30 EC_SMIB
71 DGPU_HOLD_RST#
56 WLAN_BT_LED
53 WLAN_ON
82.85 DGPU_PWR_EN#
ONE PAIZU
32 PCH_TEMP_EN
61 BT_ON

U2001F
BMBUSY#/GPIO0
TACH1#/GPIO1
TACH2#/GPIO6
TACH3#/GPIO7
GPIO8
LAN_PHY_PWR_CTRL#/GPIO12
GPIO15
SATAAGP/GPIO16
TACH0#/GPIO17
SCLOCK#/GPIO22
MEM_LED/GPIO24
GPIO27
GPIO28
STP_PCIF#/GPIO34
SATACLKREQ#/GPIO35
SATA2GP/GPIO36
SATA3GP/GPIO37
SLOAD/GPIO38
SDATAOUT0/GPIO39
PCIECLKREQ6#/GPIO45
PCIECLKREQ7#/GPIO46
SDATAOUT1/GPIO48
SATA5GP/GPIO49
GPIO57

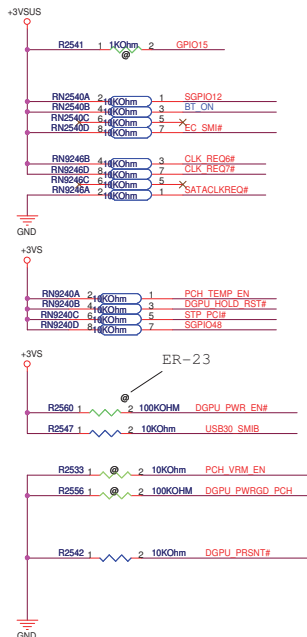
VSS_NCTF_1
VSS_NCTF_2
VSS_NCTF_3
VSS_NCTF_4
VSS_NCTF_5
VSS_NCTF_6
VSS_NCTF_7
VSS_NCTF_8
VSS_NCTF_9
VSS_NCTF_10
VSS_NCTF_11
VSS_NCTF_12
VSS_NCTF_13
VSS_NCTF_14
VSS_NCTF_15
VSS_NCTF_16
VSS_NCTF_17
VSS_NCTF_18
VSS_NCTF_19
VSS_NCTF_20
VSS_NCTF_21
VSS_NCTF_22
VSS_NCTF_23
VSS_NCTF_24
VSS_NCTF_25
VSS_NCTF_26
VSS_NCTF_27
VSS_NCTF_28
VSS_NCTF_29
VSS_NCTF_30
VSS_NCTF_31

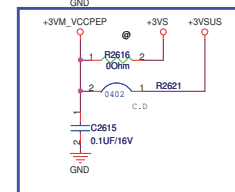
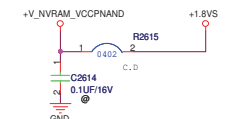
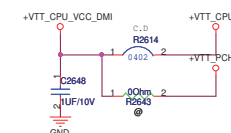
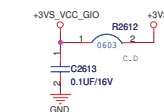
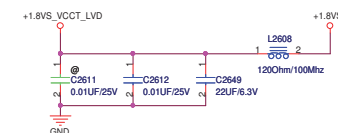
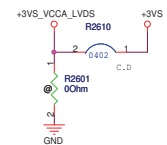
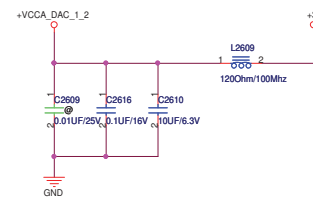
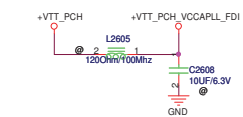
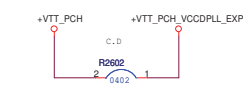
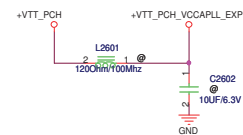
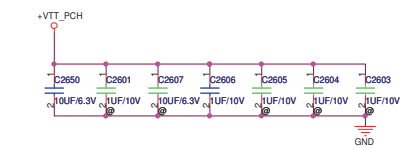
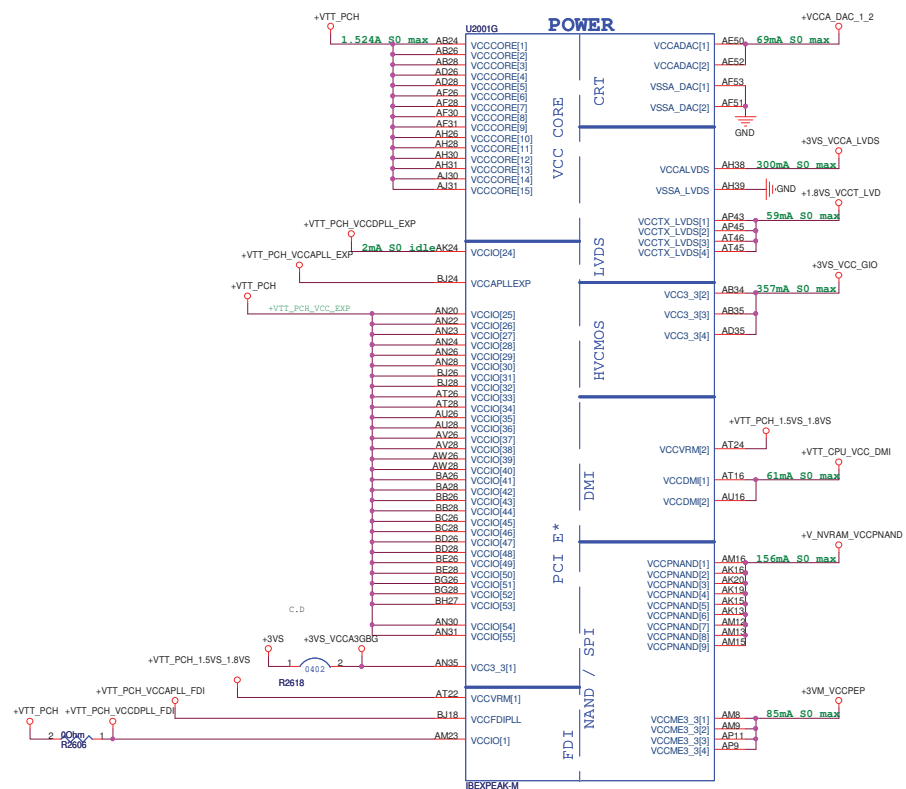
MISC
CPU
GPIO

NCTF
RSVD

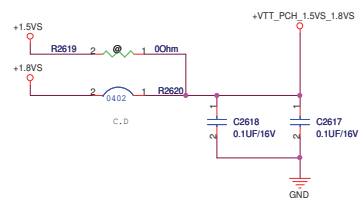
CLKOUT_PCIE6N
CLKOUT_PCIE6P
CLKOUT_PCIE7N
CLKOUT_PCIE7P
A20GATE
CLKOUT_BCLK0_N/CLKOUT_PCIE8N
CLKOUT_BCLK0_P/CLKOUT_PCIE8P
PECI
RCIN#
PROC_PWRGD
THRMTRIP#
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
TP16
TP17
TP18
TP19
NC_1
NC_2
NC_3
NC_4
NC_5
INT3_3V#
TP24

AH45
AH46
AE49
AE4X
U2
A20GATE 30
BCLK_CPU_N_PCH 3
BCLK_CPU_P_PCH 3
H_PECI 3
KB_RST# 30
H_CUP_PWRGD 3.7
PM_THRMTRIP# PCH
BA23
AW23
BB23
AY45
AY46
AV45
AV46
AE13
M18 TP9_PCH 1 T2563
N18 TP10_PCH 1 T2564
AJ24 TP11_PCH 1 T2566
AK41 TP12_PCH 1 T2580
C10



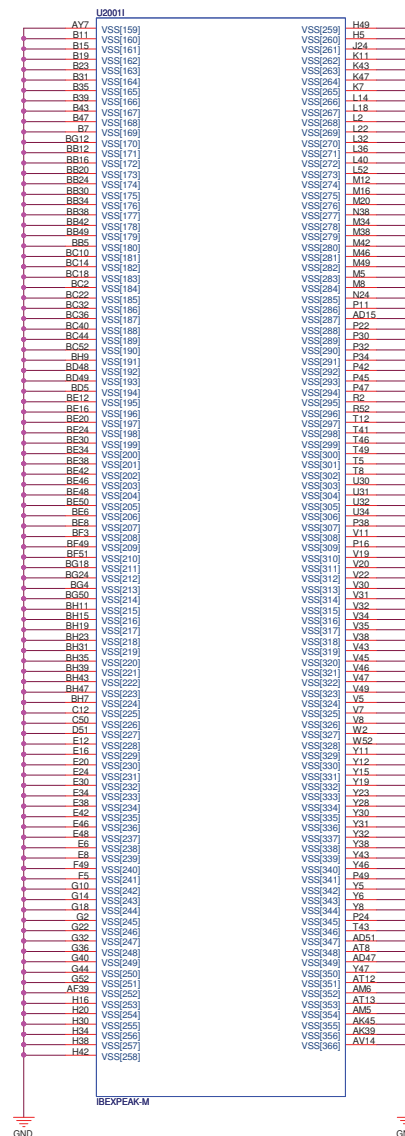


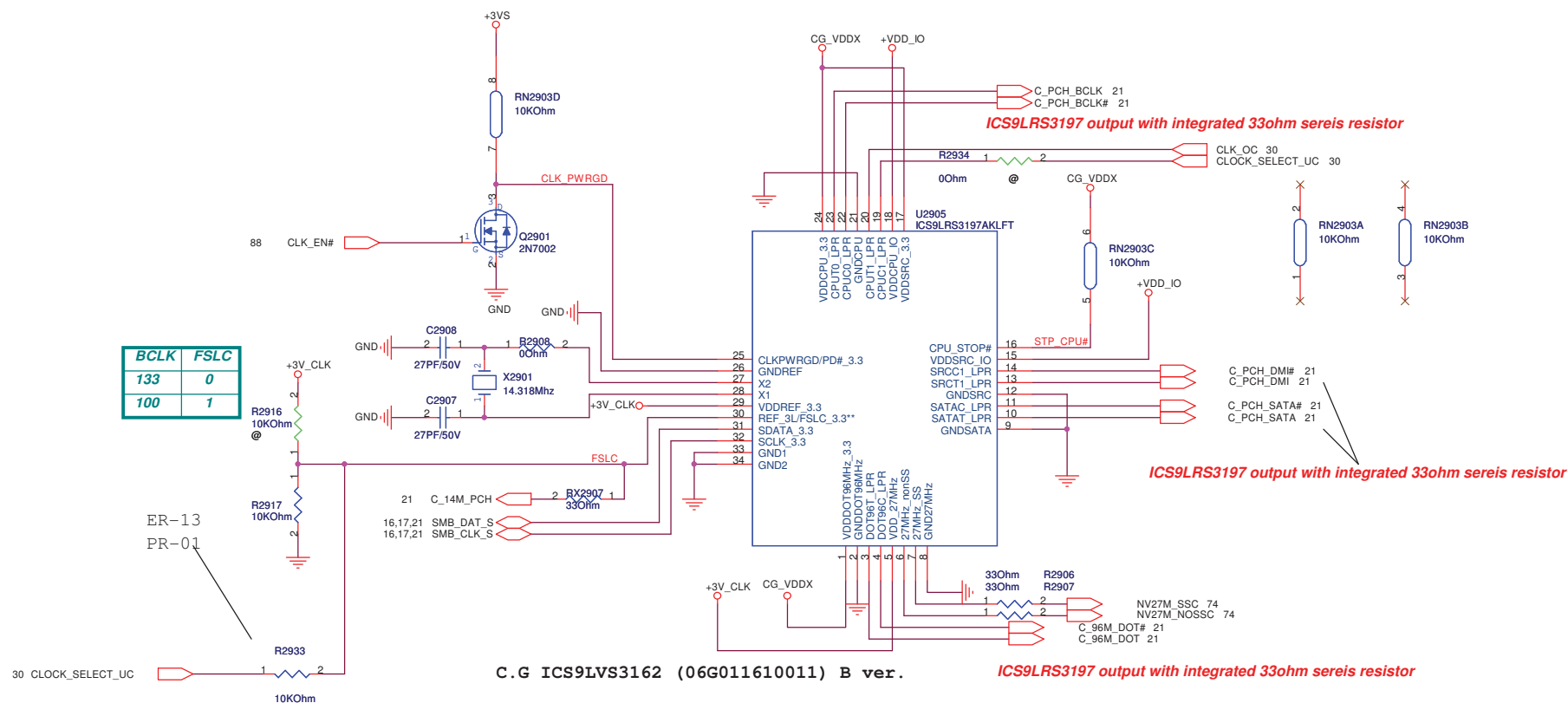
Update 1105 (R2.0)

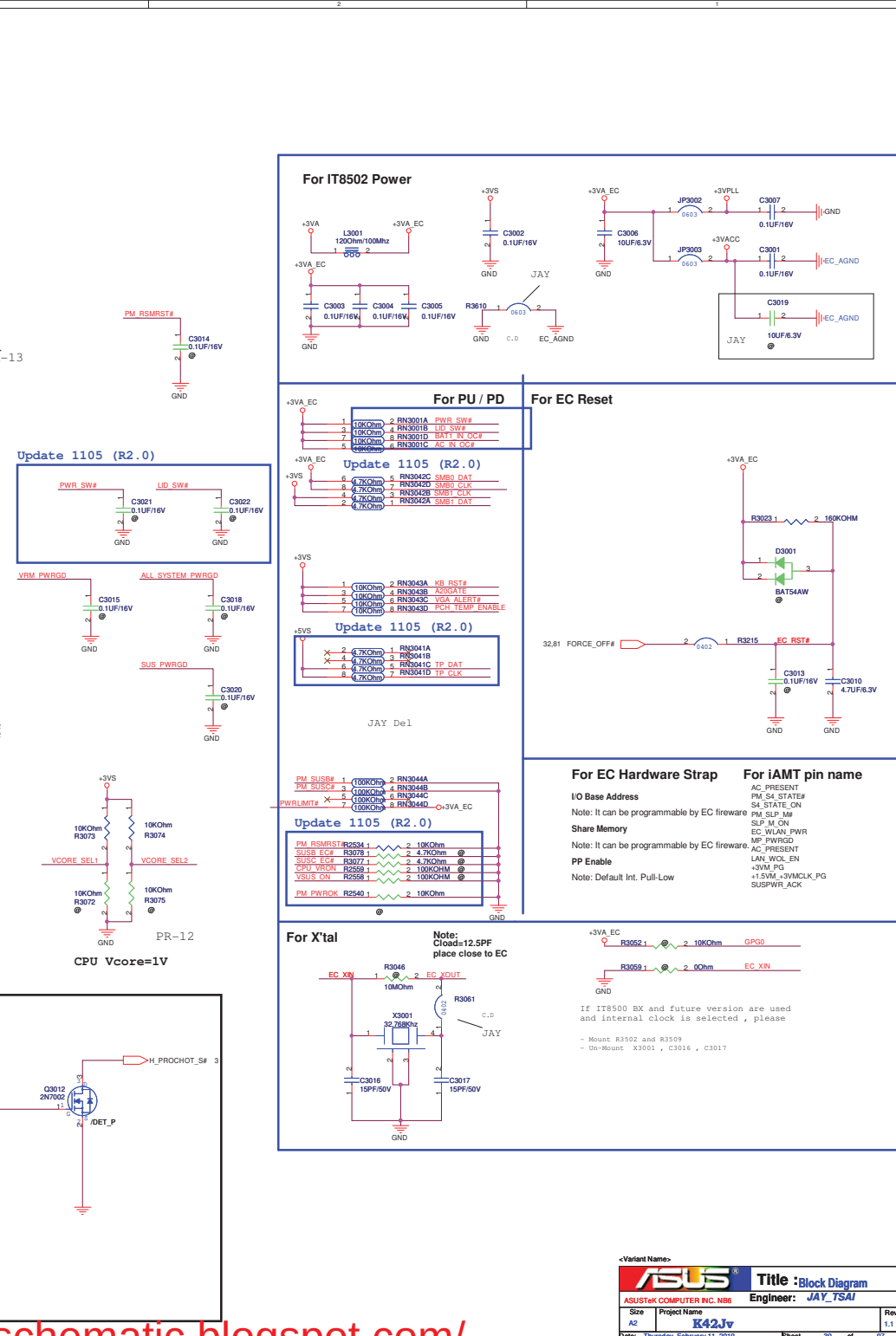


HDA_SYNC: Select VCCVRM 1.5V or 1.8V (IPD)
Low: 1.8V
High: 1.5V

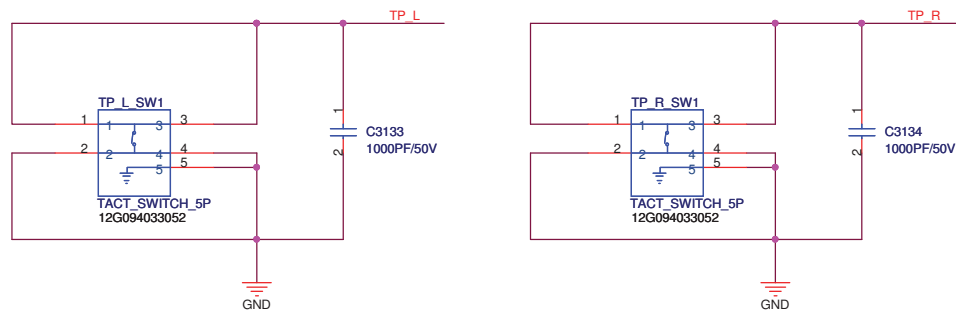
GPI027 NC:enable internal regulator for:
VccAClk VccapllEXP
VccFDIPLL VccSATAPLL



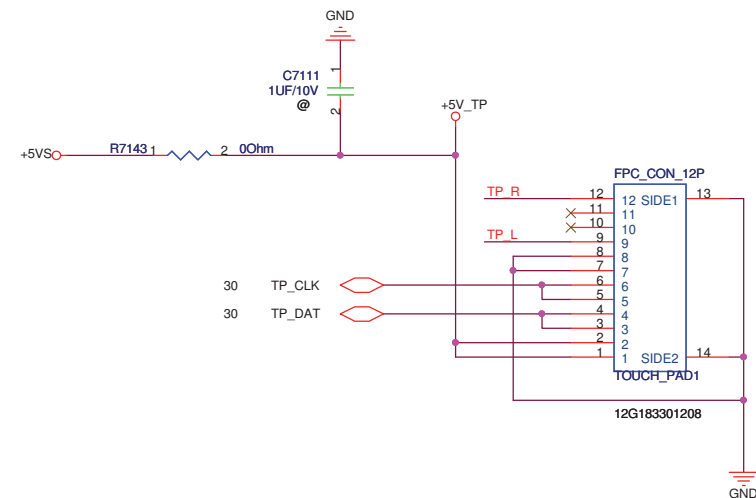




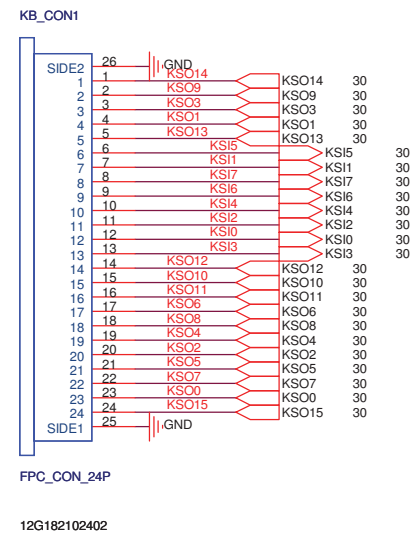
TouchPad



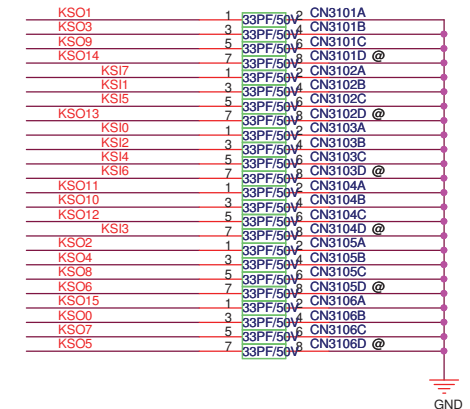
1.0 EMI test need mount C3133 and C3134



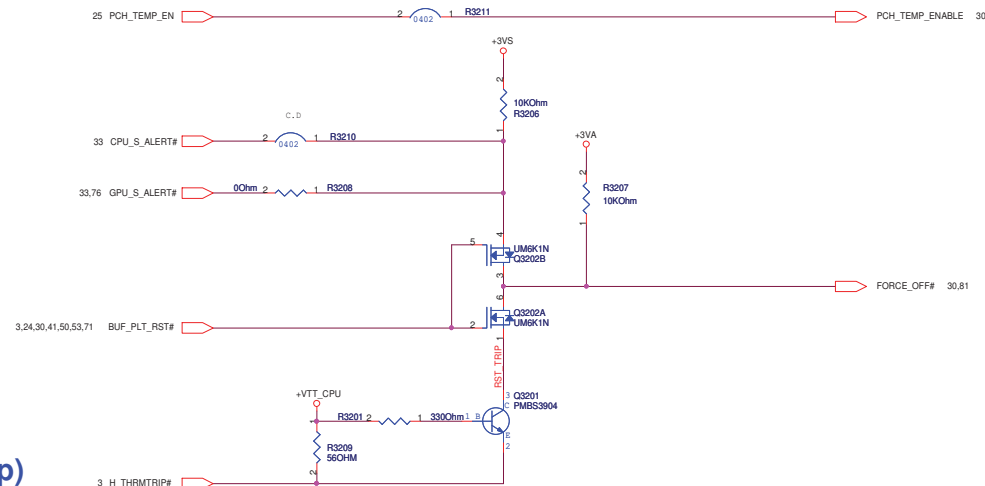
Keyboard Connector



EMI Request

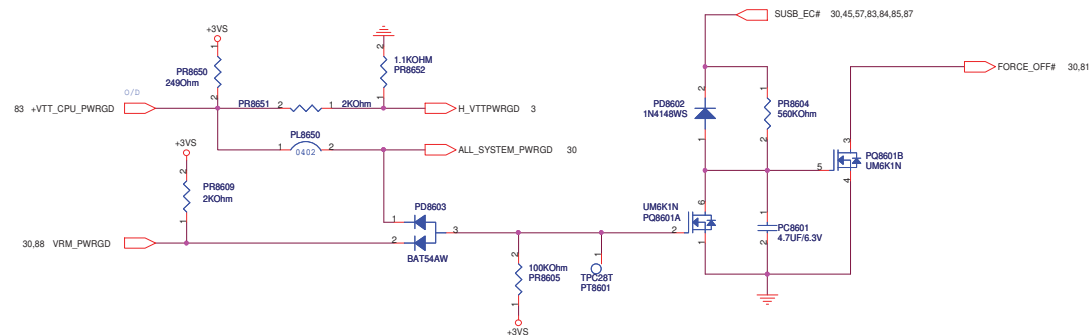
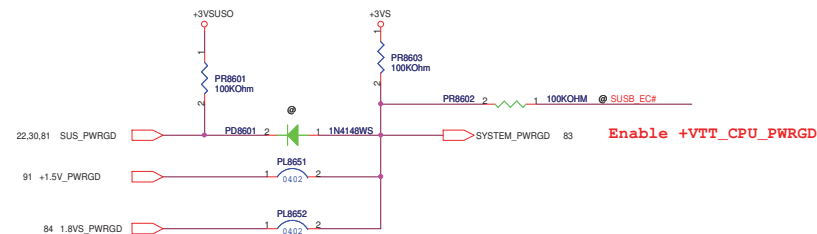


Thermal Policy

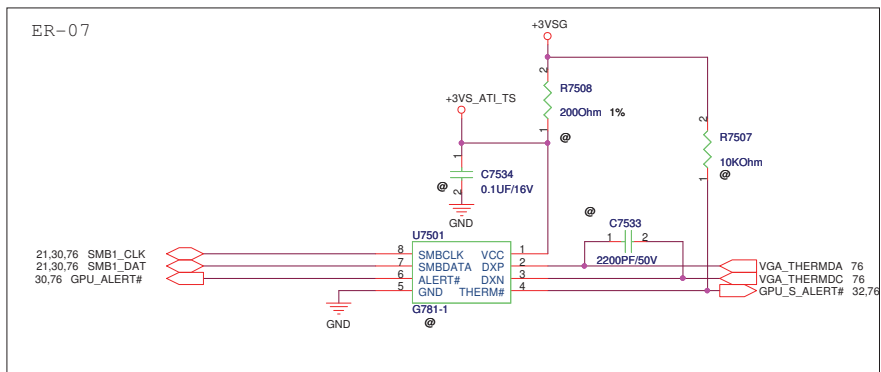


Output (shut down)

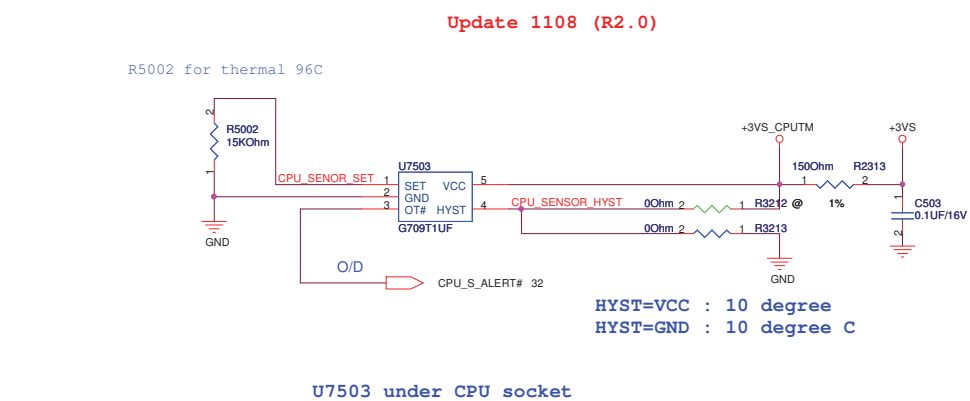
POWER GOOD DETECTOR



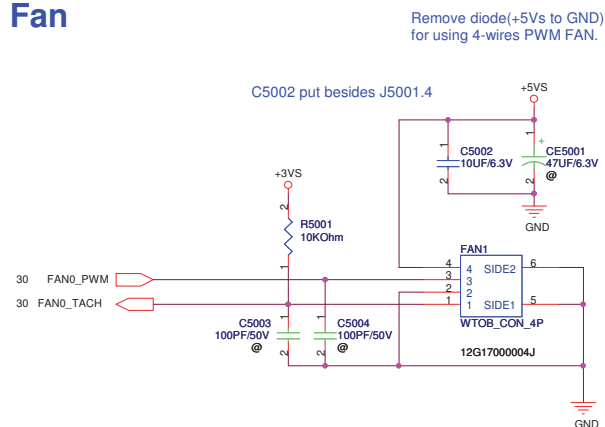
GPU Thermal Sensor



CPU Thermal Sensor

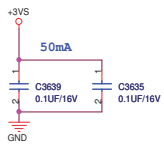


PWM Fan



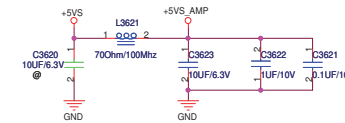
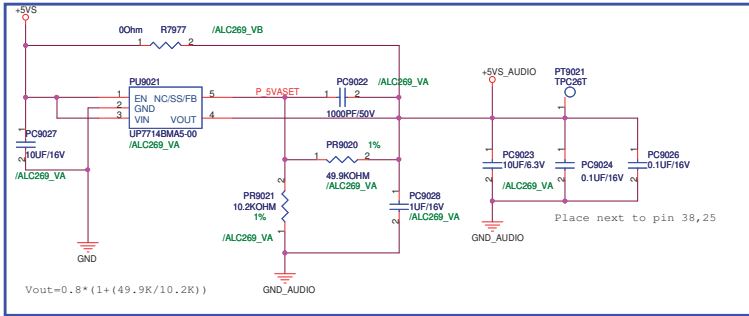
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ASUSTeK COMPUTER INC		Engineer: JAY_TSAI	
Size	Project Name		Rev
Custom	K42Jv		108
Date: Thursday, February 11, 2010		Sheet	33 of 96



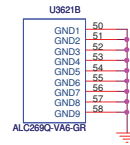


Close to pin1,9

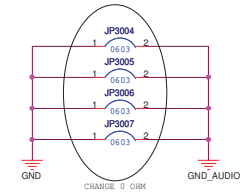
Update 11.08 (R2.0)



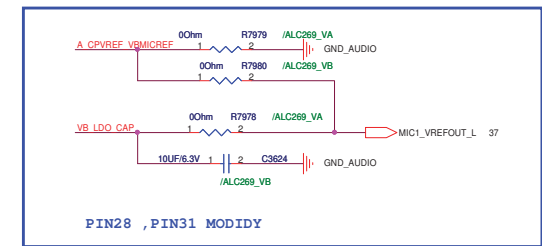
Place next to pin 39,46



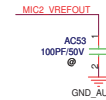
For EMI



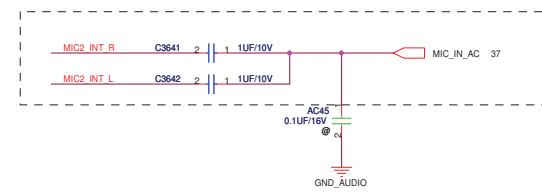
Update 11.08 (R2.0)



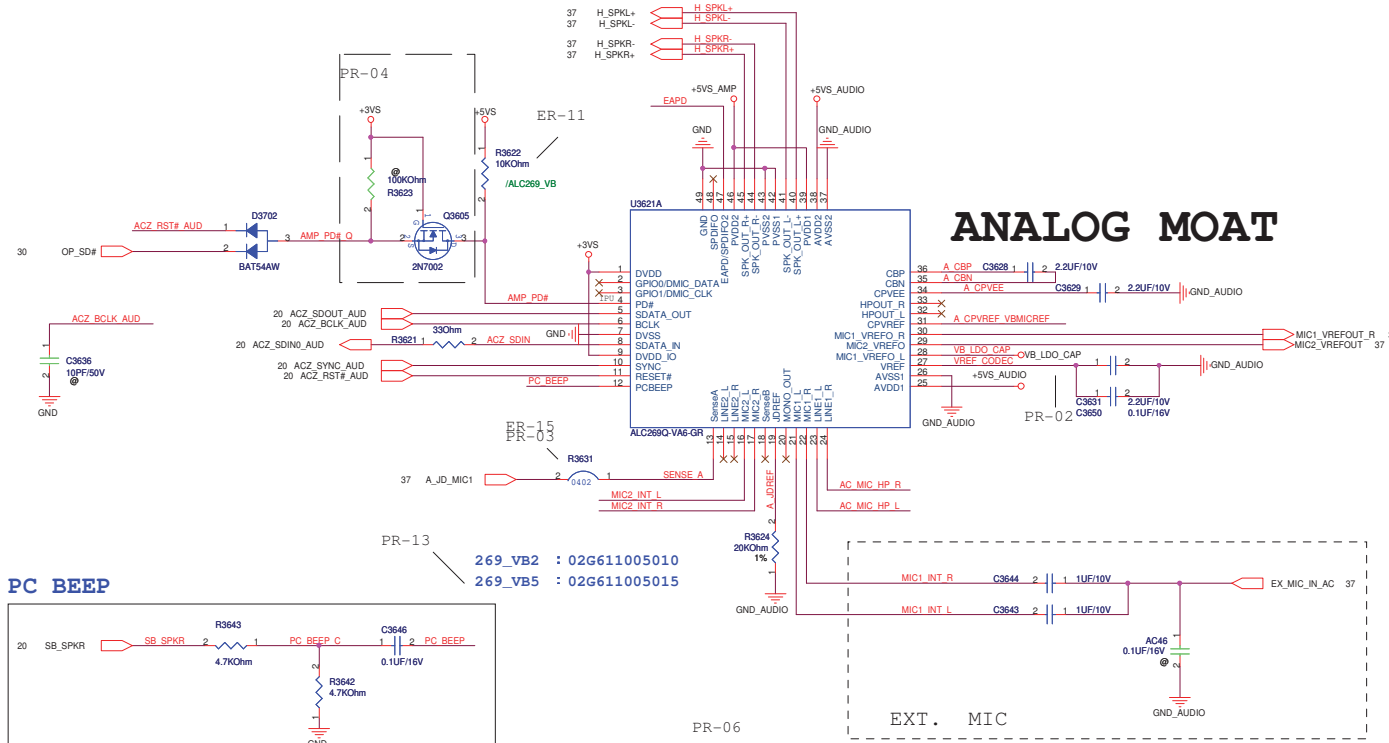
PIN28 , PIN31 MODIFY



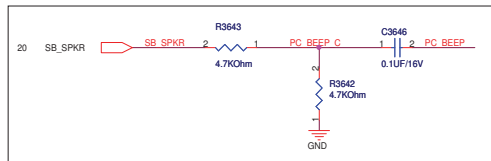
INTERNAL MIC



ANALOG MOAT



PC BEEP



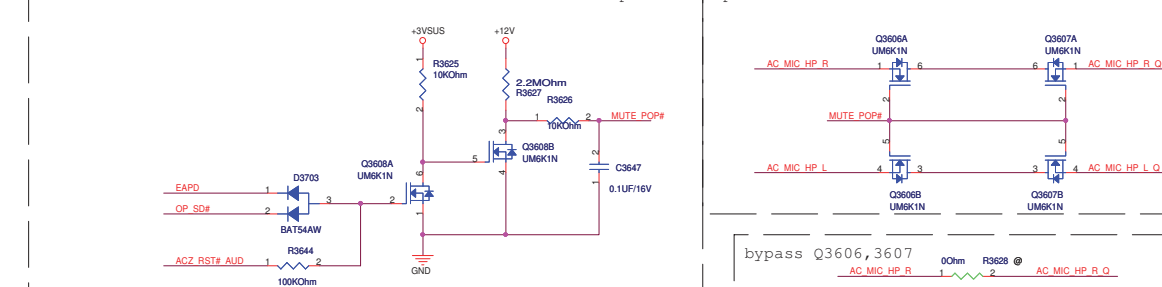
PR-06

EXT. MIC

MUTE

Option 1

Option 1

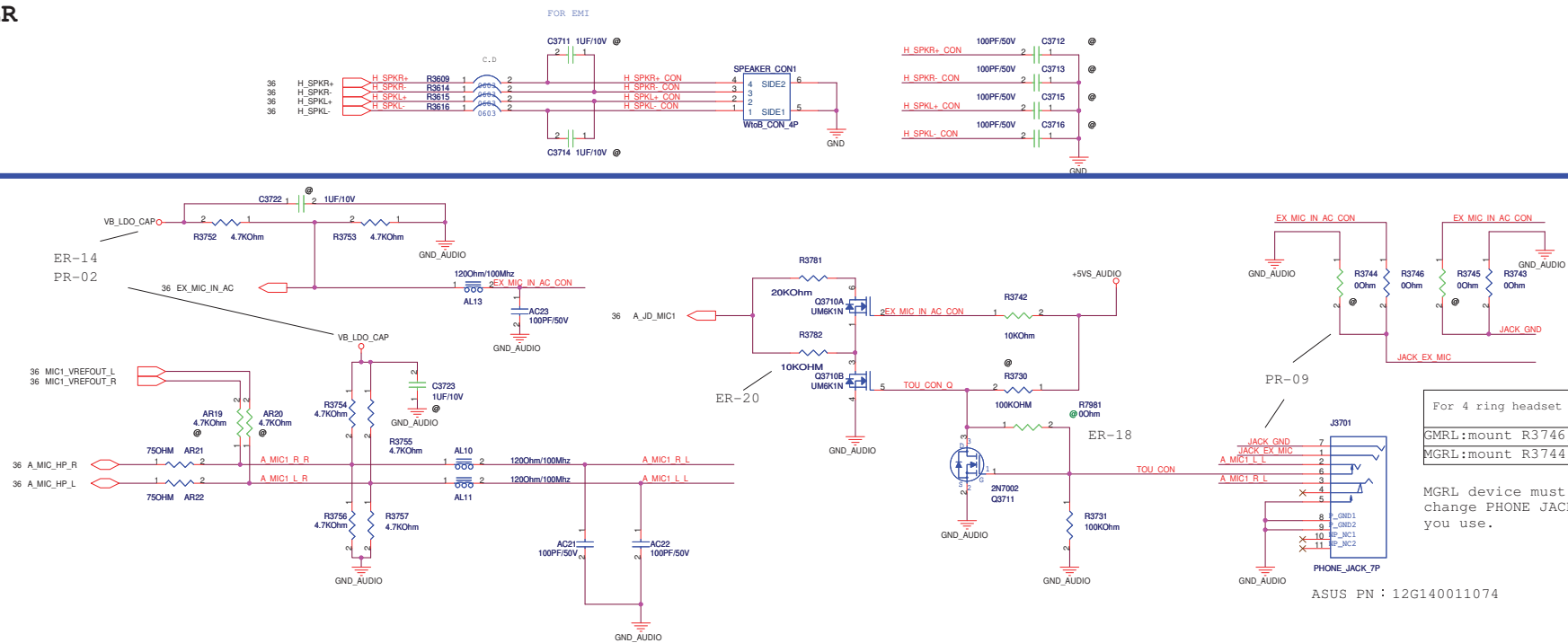


bypass Q3606, 3607



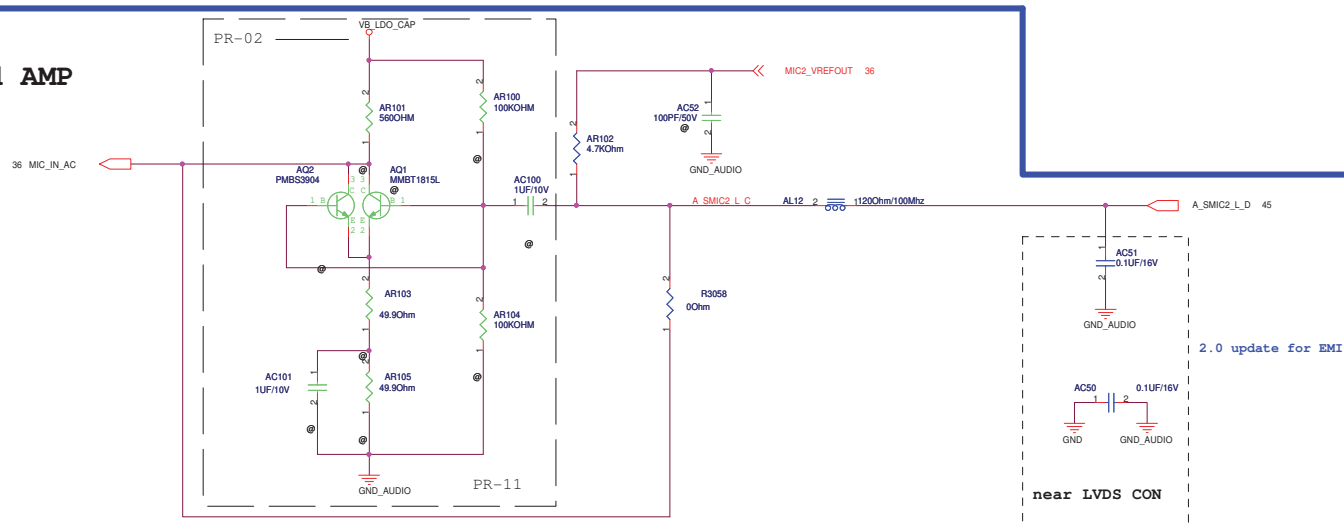
<http://laptop motherboard-schematic.blogspot.com/>

SPEAKER



HP and MIC

Internal MIC and AMP

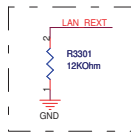




<http://laptop-motherboard-schematic.blogspot.com/>

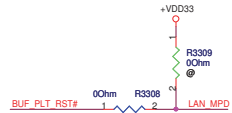
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ASUSTek Computer Inc.			Engineer: JAY_TSAI			
Size	Project Name				Rev	
A3	K42Jv				1.0G	
Date: Thursday, February 11, 2010			Sheet	40	of	96

Reference Resistance



D3E Enable/Disable

R3309	R3308	D3E
Unmount	Mount	Enable
Mount	Unmount	Disable



21 PCH_C_LAN_N
21 PCH_C_LAN_P
21 POE_TX_LAN_P
21 POE_TX_LAN_N
21 POE_RX_LAN_N
21 POE_RX_LAN_P

0.1uF/16V
0.1uF/16V
0.1uF/16V
0.1uF/16V
0.1uF/16V
0.1uF/16V

C3315
C3316
C3315
C3316
C3315
C3316

GND
GND
GND
GND
GND
GND

LAN_TXN_JMC
LAN_TXP_JMC
LAN_TXN_JMC
LAN_TXP_JMC
LAN_TXN_JMC
LAN_TXP_JMC

LAN_TXN_JMC
LAN_TXP_JMC
LAN_TXN_JMC
LAN_TXP_JMC
LAN_TXN_JMC
LAN_TXP_JMC

LAN_TXN_JMC
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LAN_TXP_JMC

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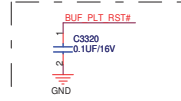
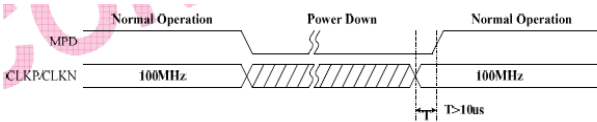
LAN_TXN_JMC
LAN_TXP_JMC
LAN_TXN_JMC
LAN_TXP_JMC
LAN_TXN_JMC
LAN_TXP_JMC

LAN_TXN_JMC
LAN_TXP_JMC
LAN_TXN_JMC
LAN_TXP_JMC
LAN_TXN_JMC
LAN_TXP_JMC

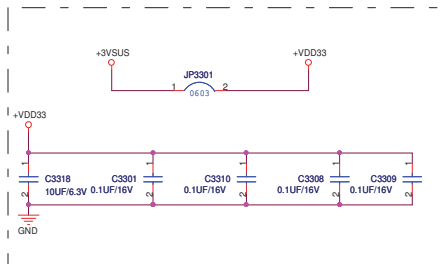
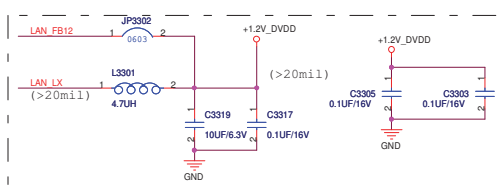
LAN_TXN_JMC
LAN_TXP_JMC
LAN_TXN_JMC
LAN_TXP_JMC
LAN_TXN_JMC
LAN_TXP_JMC

LAN_TXN_JMC
LAN_TXP_JMC
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LAN_TXP_JMC
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LAN_TXP_JMC

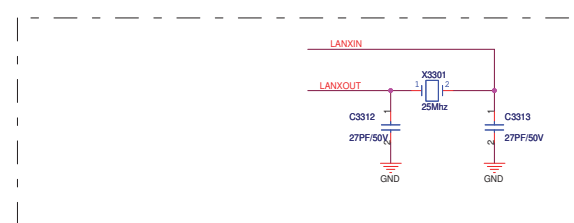
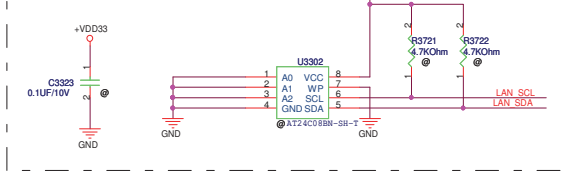
LAN_TXN_JMC
LAN_TXP_JMC
LAN_TXN_JMC
LAN_TXP_JMC
LAN_TXN_JMC
LAN_TXP_JMC



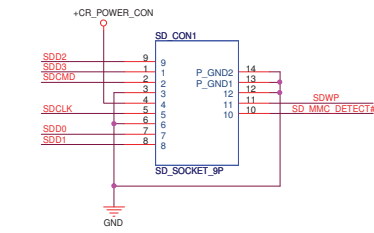
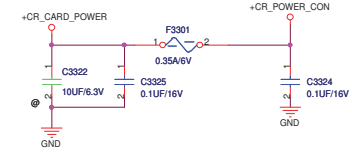
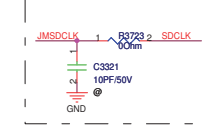
Switch Regulator



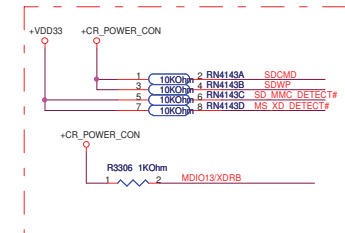
Serial EEPROM



L_TRDN3 53
L_TRDP3 53
L_TRDN2 53
L_TRDP2 53
L_TRDN1 53
L_TRDP1 53
L_TRDN0 53
L_TRDP0 53

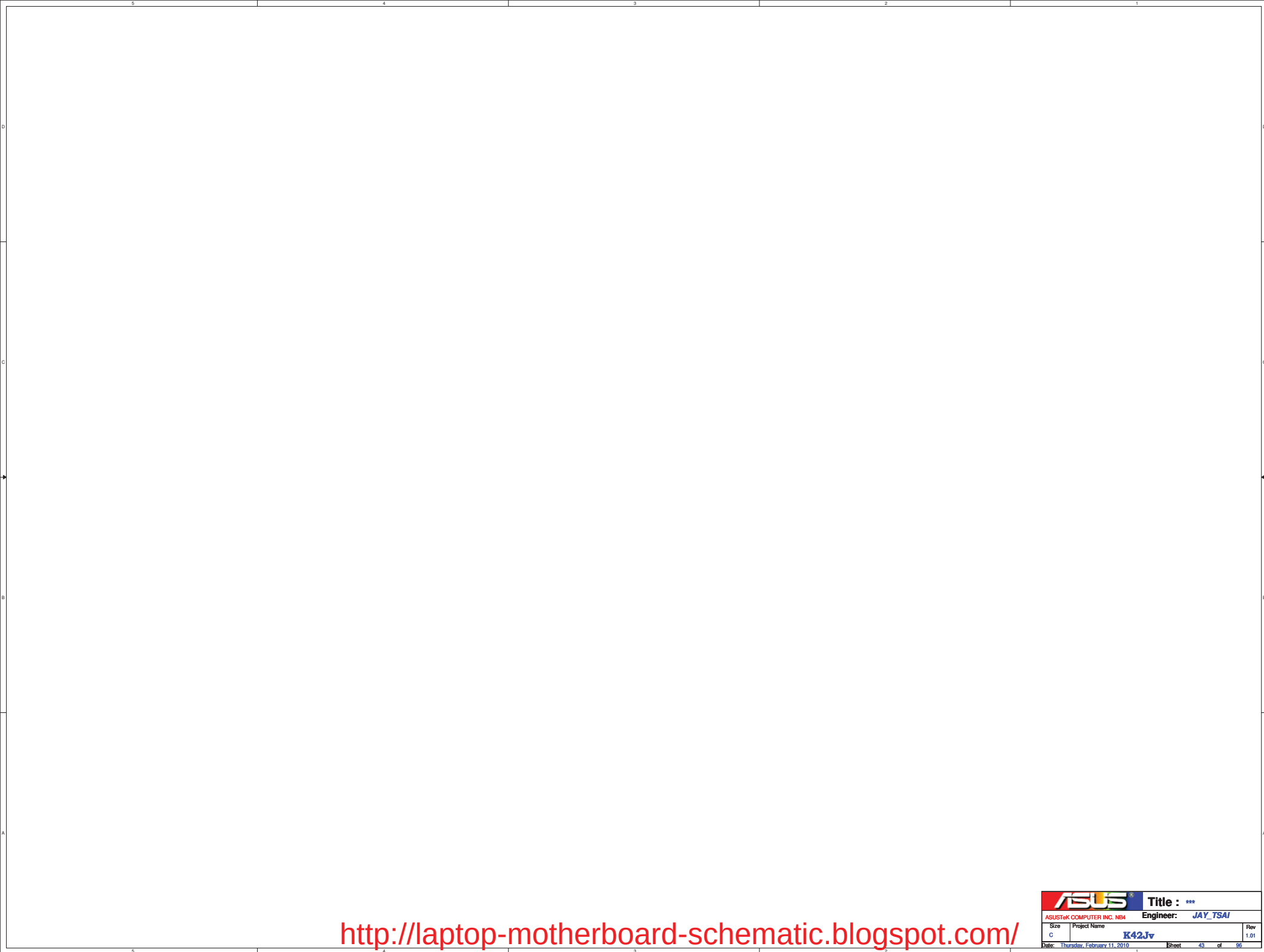


Card Insert: Pin.10 and Pin.12 are Shorted.
Card not Insert: Pin.10 and Pin.12 are Opened.
Write Protect: Pin.11 and Pin.12 are Opened.
Write Enable: Pin.11 and Pin.12 are Shorted.





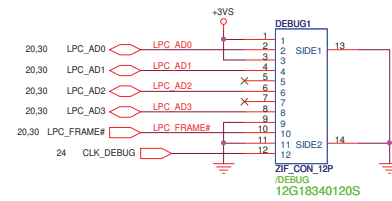
		Title : ***	
ASUSTeK COMPUTER INC. NB4		Engineer: JAY_TSAI	
Size	Project Name		Rev
Custom	K42Jv		1.3
Date	Thursday, February 11, 2010		Sheet 42 of 99

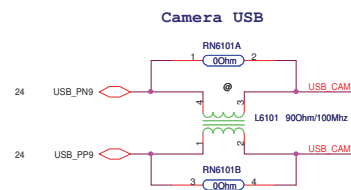
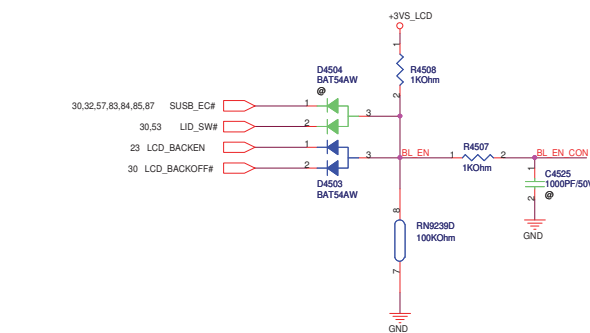
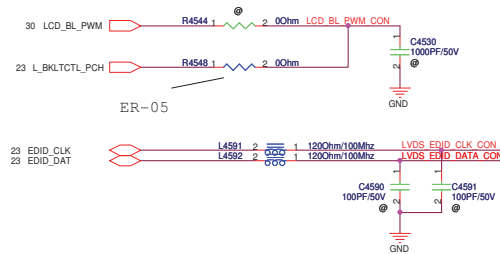
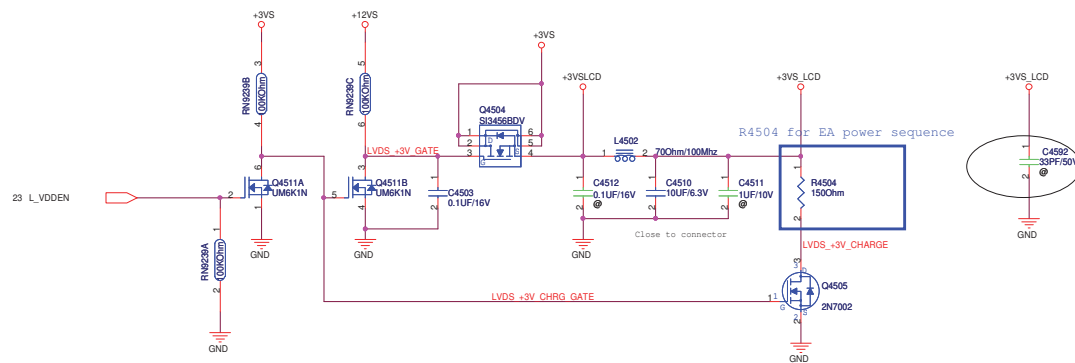


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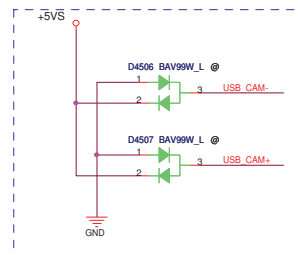
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ASUSTeK COMPUTER INC. NBD		Engineer: JAY_TSAI	
Size	Project Name		Rev
C	K42Jv		1.01
Date: Thursday, February 11, 2010		Sheet	43 of 95

LPC Debug Port

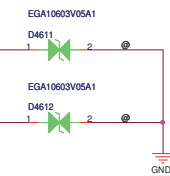
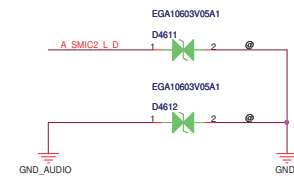
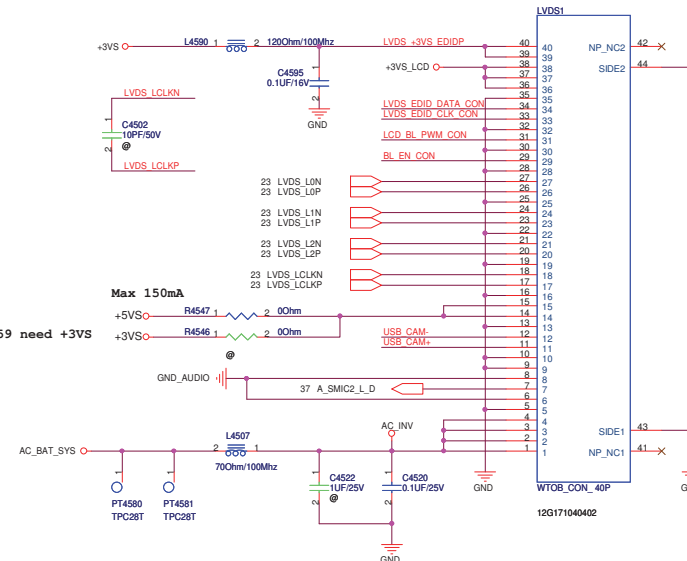




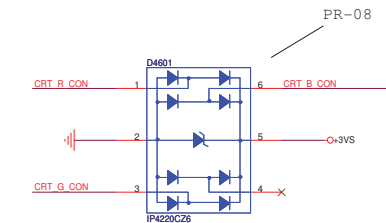
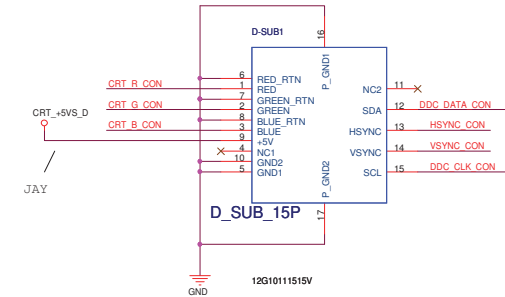
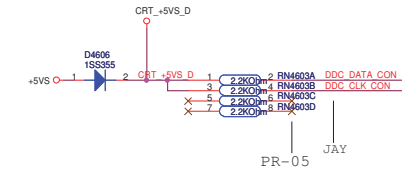
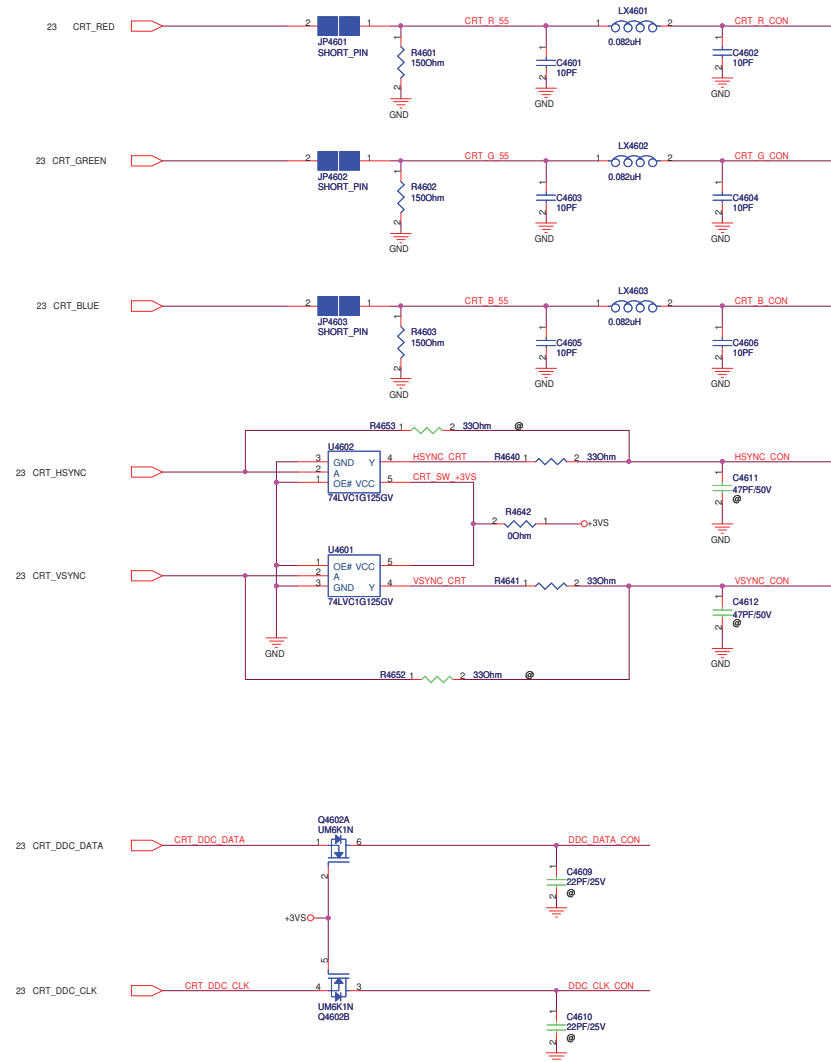
1.0 EMI test need mount D4506 and D4507



CNF9059 need +3VS



Main Board



EGA10603V05A1

D4607

D4608

D4609

D4610

D4611

D4612

D4613

D4614

D4615

D4616

D4617

D4618

D4619

D4620

D4621

D4622

D4623

D4624

D4625

D4626

D4627

D4628

D4629

D4630

D4631

D4632

D4633

D4634

D4635

D4636

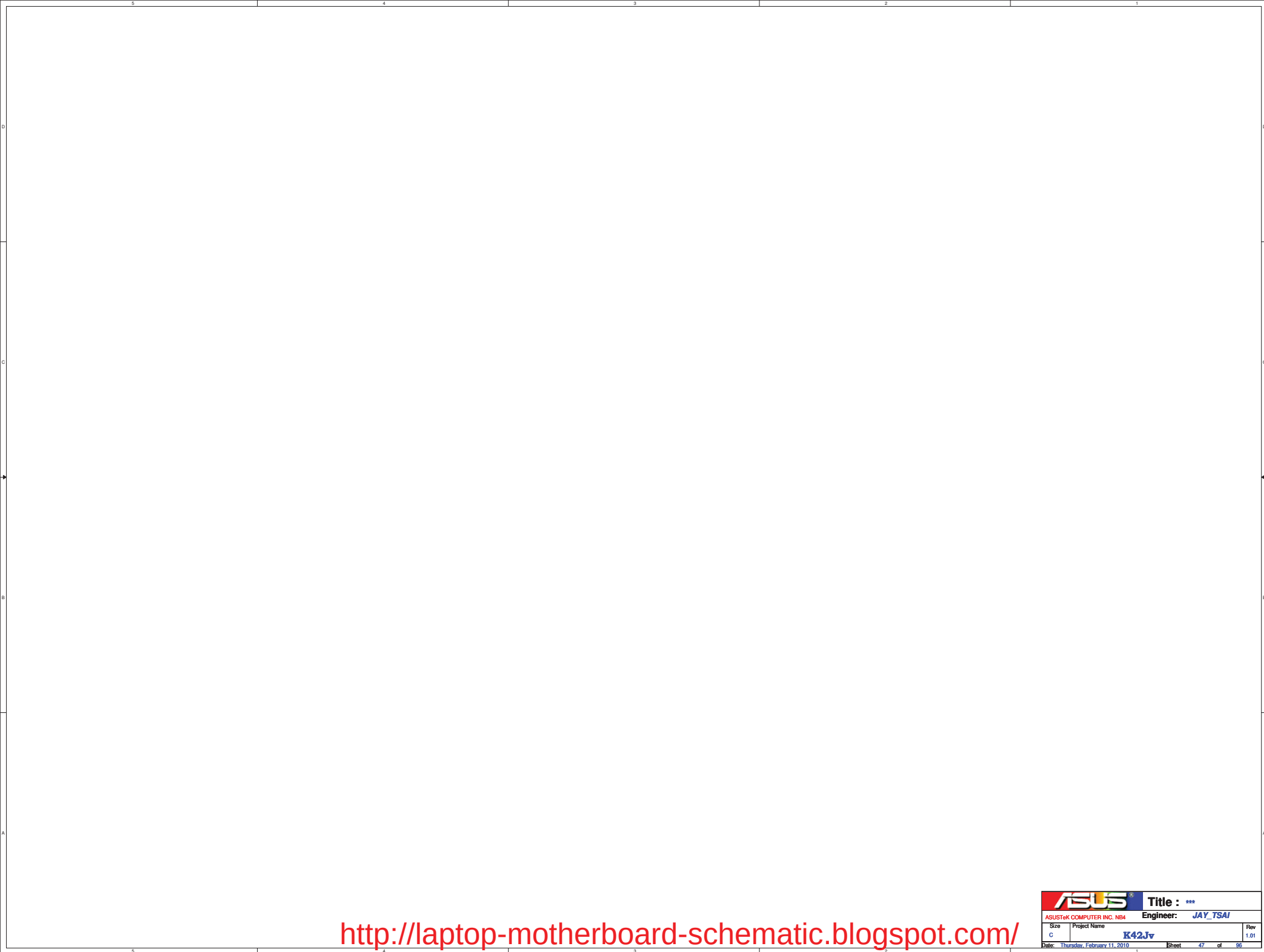
D4637

D4638

D4639

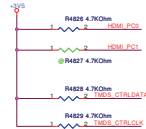
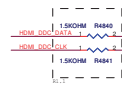
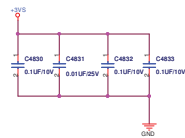
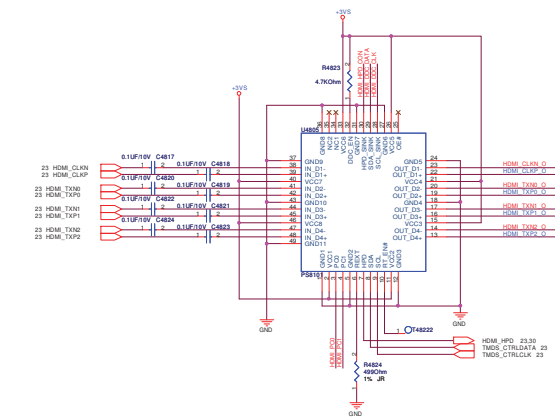
D4640

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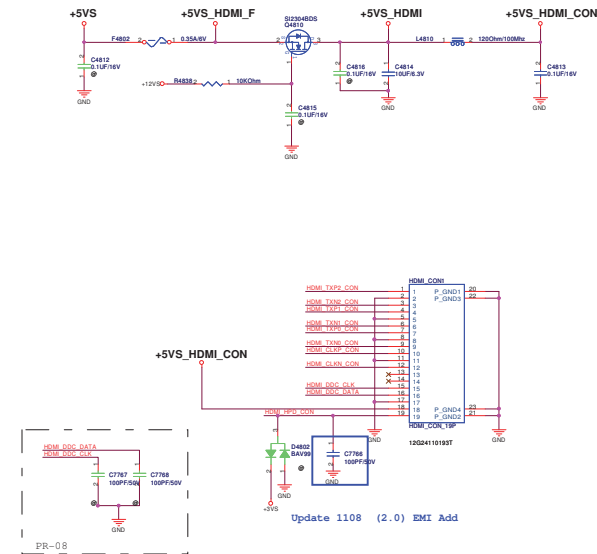
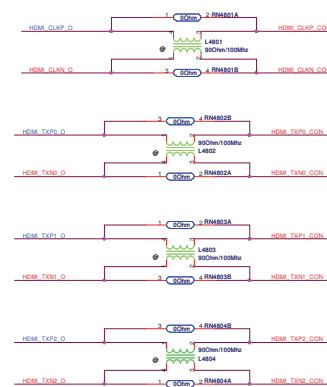


<http://laptop-motherboard-schematic.blogspot.com/>

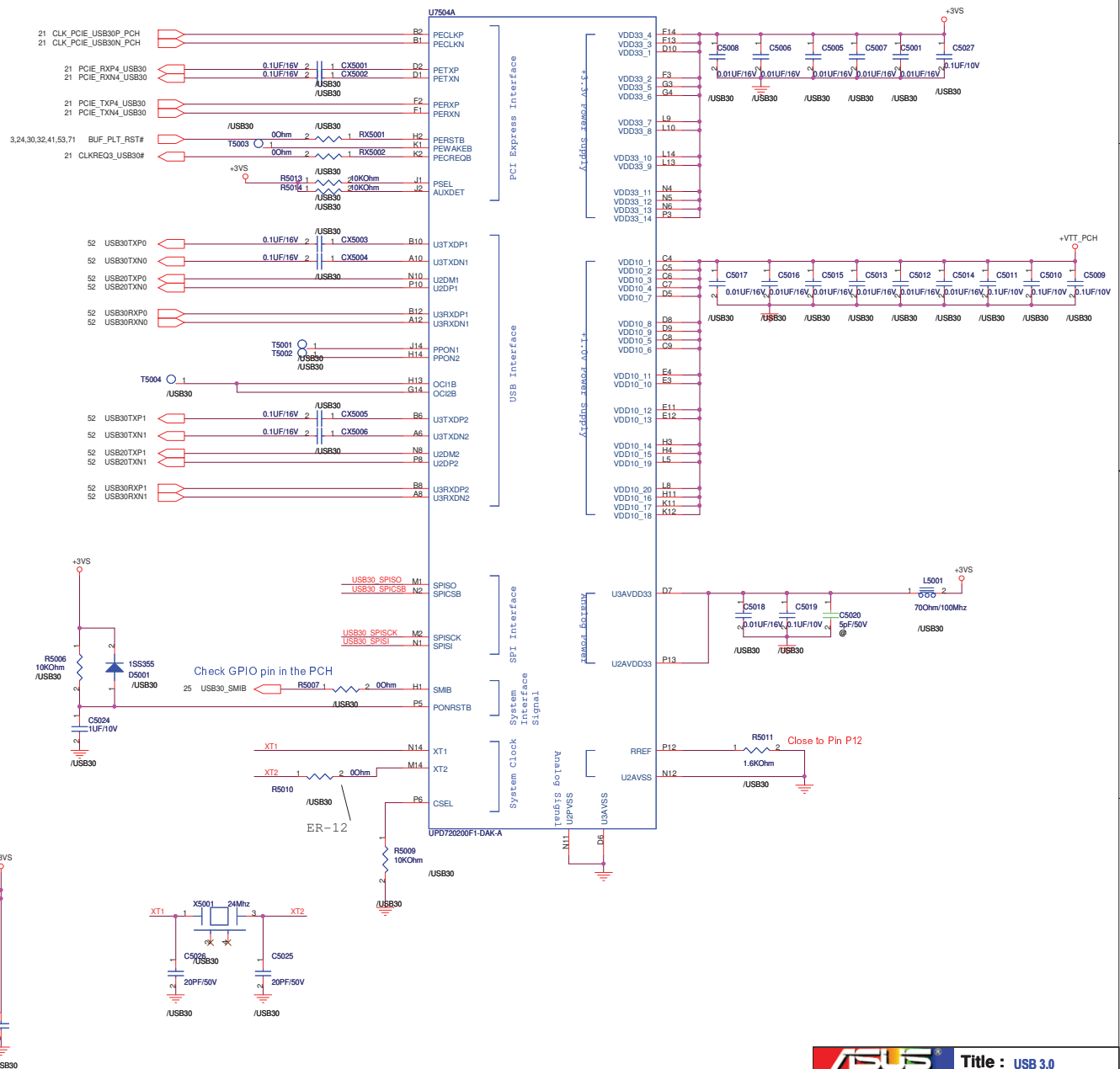
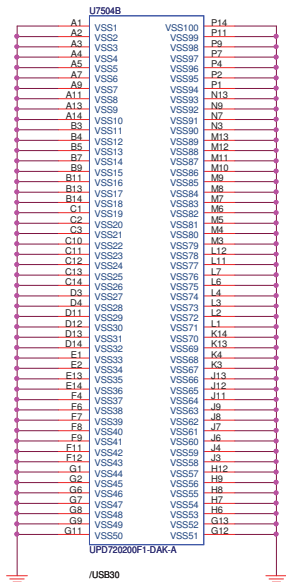
		Title : ***	
ASUSTeK COMPUTER INC. NB4		Engineer: JAY_TSAI	
Size C	Project Name K42Jv		Rev 1.01
Date: Thursday, February 11, 2010		Sheet	47 of 95



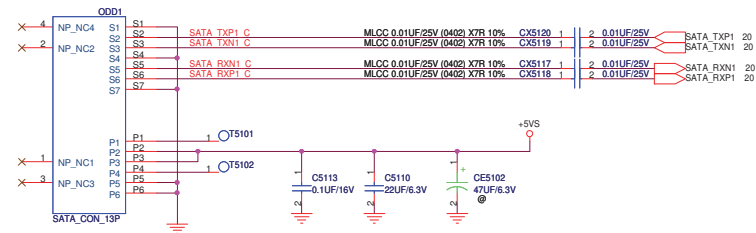
R1.1



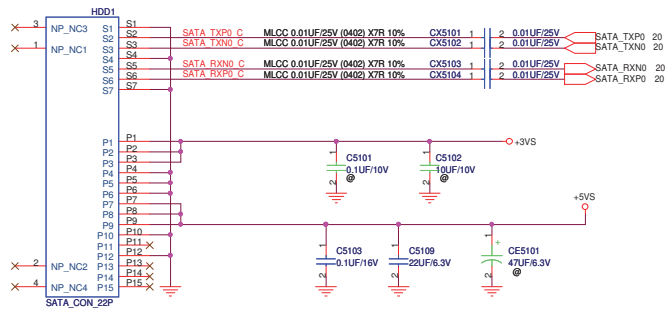
PR-08

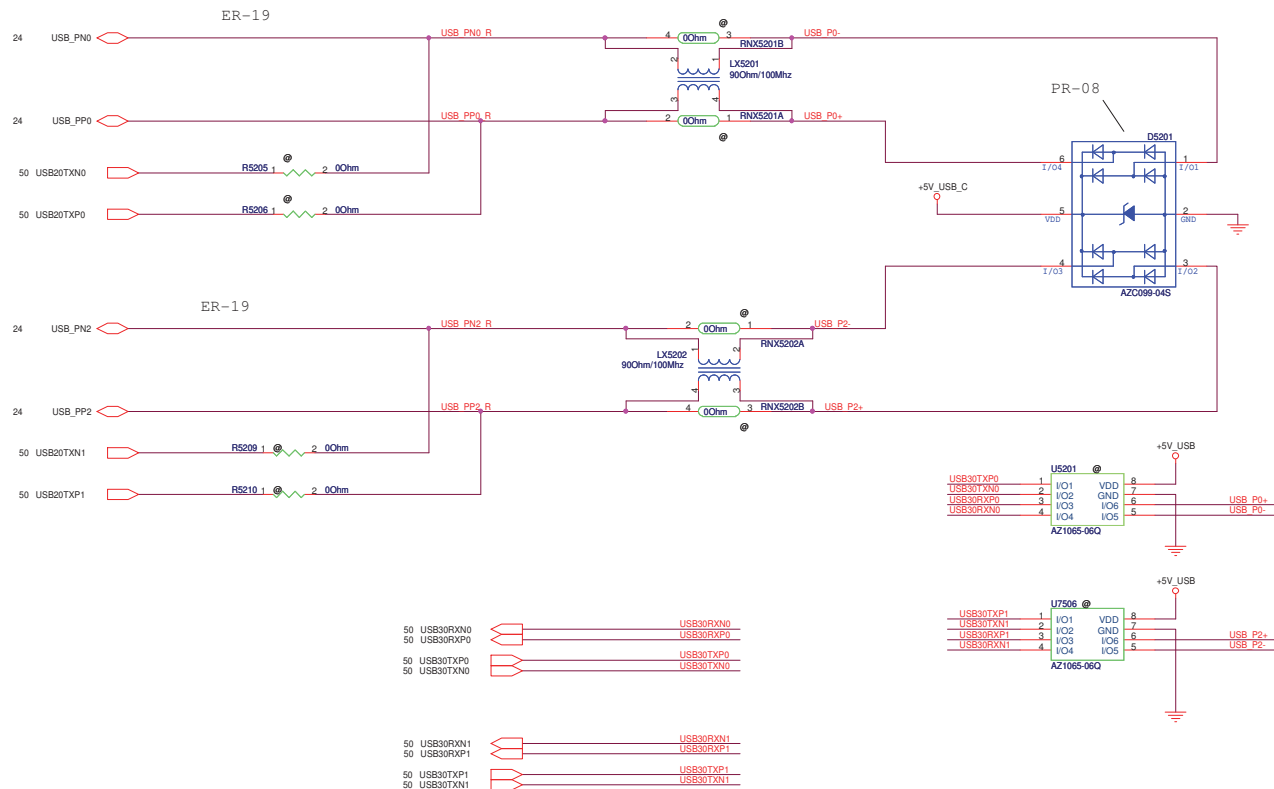
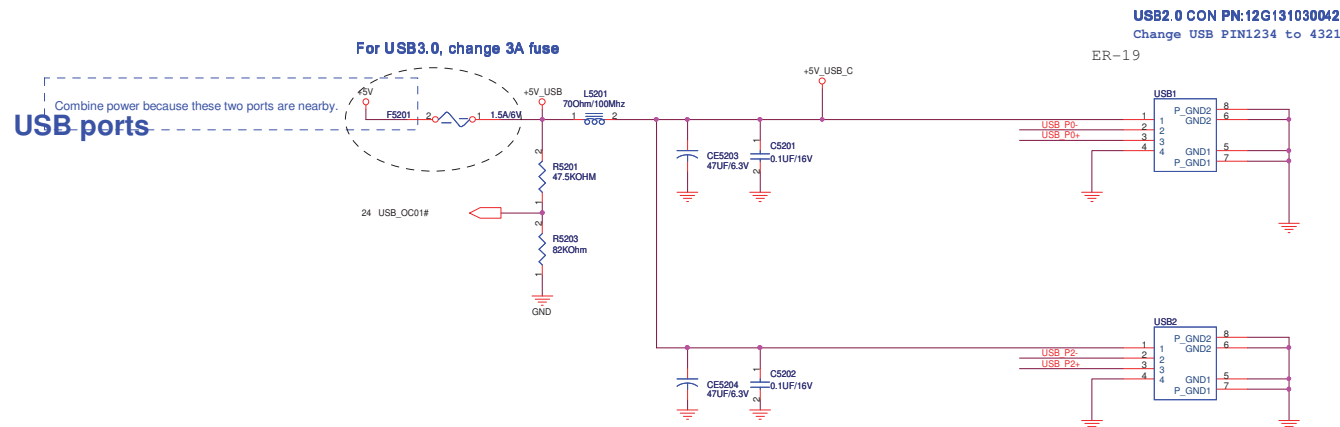


ODD



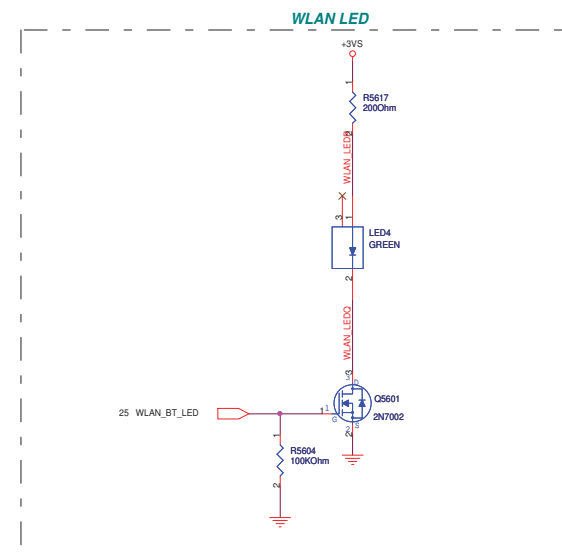
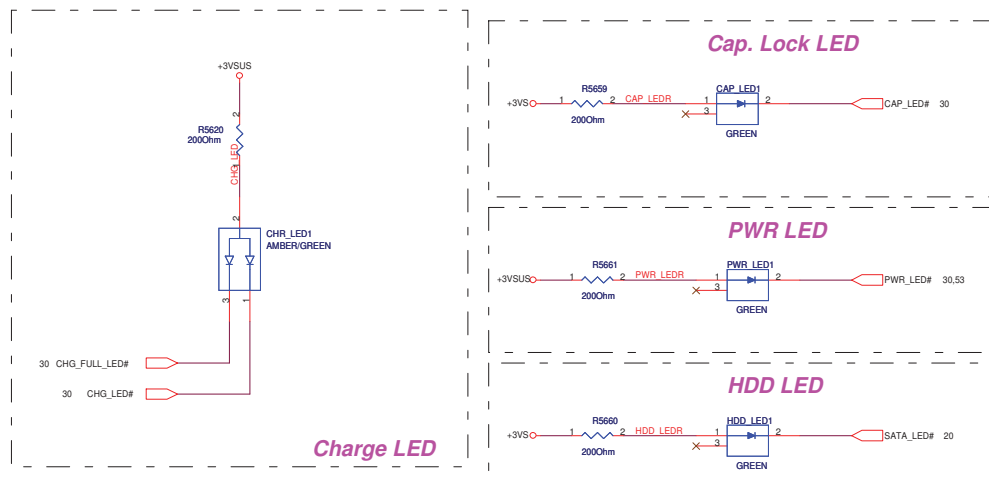
HDD (1st)





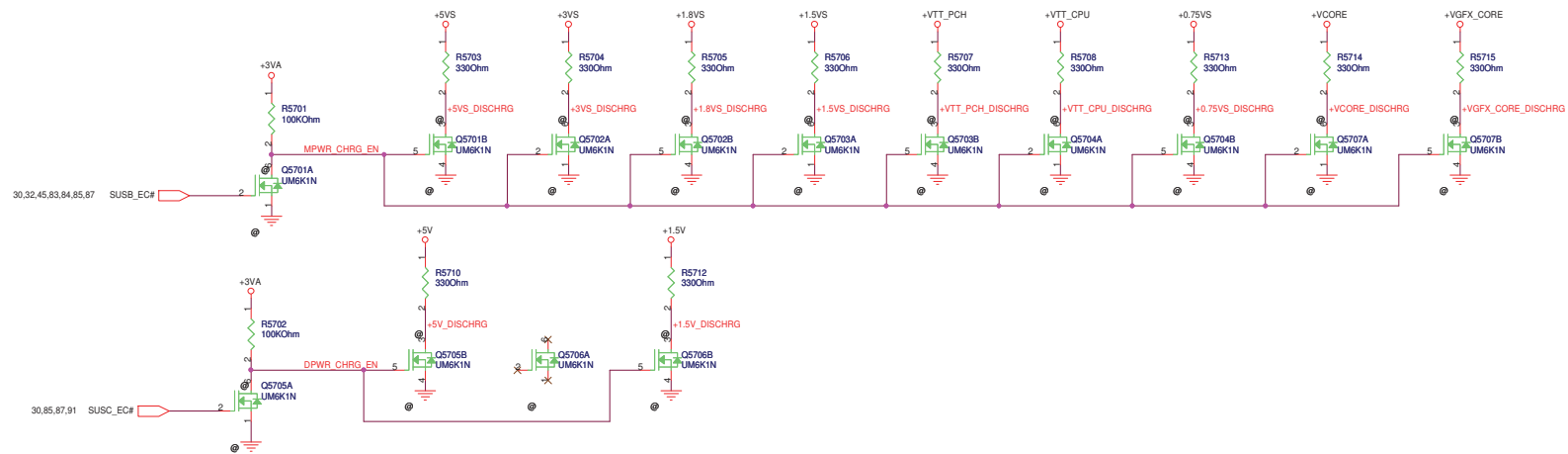
Age (years)	Percentage of people who have ever been in a romantic relationship
18	10
25	30
30	45
35	60
40	75
45	85
50	90
55	95
60	98
65	100



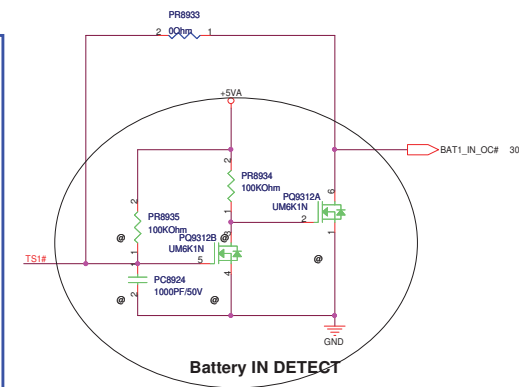
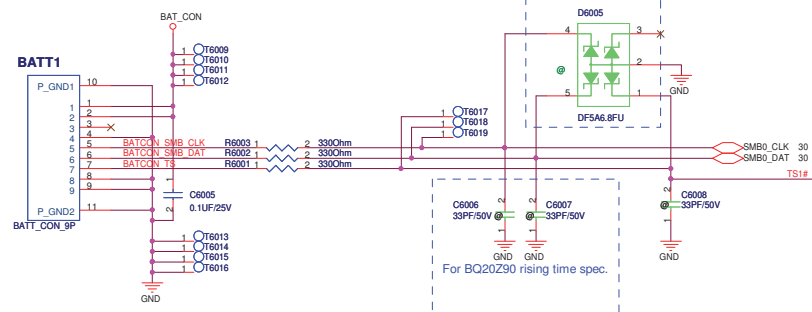


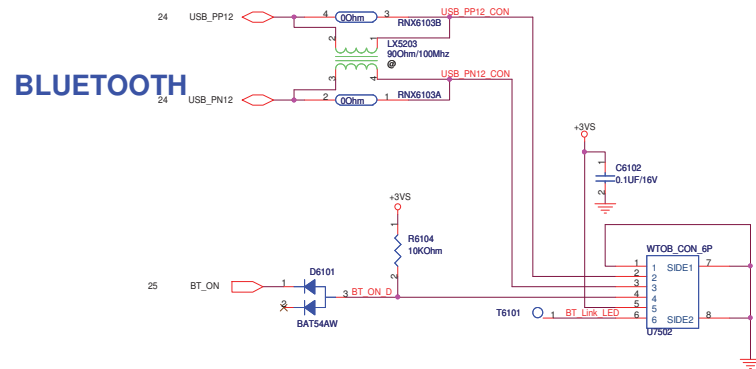
Change LED part number

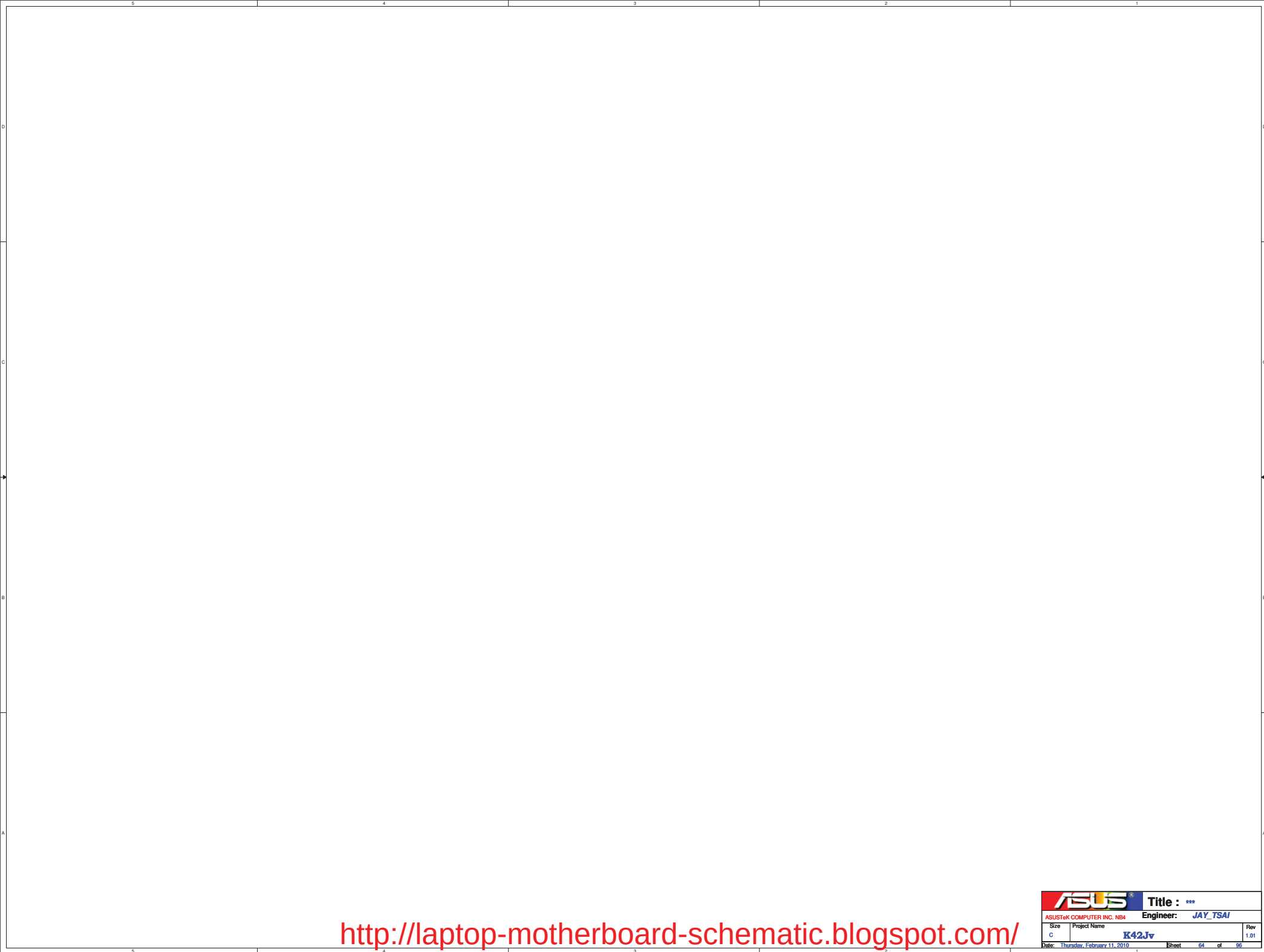
Remove +2.5Vs is for ATI GFX



Battery Connector



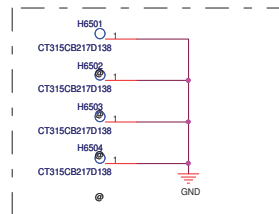




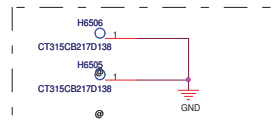
<http://laptop-motherboard-schematic.blogspot.com/>

		Title : ***	
ASUSTeK COMPUTER INC. NB4		Engineer: JAY_TSAI	
Size C	Project Name K42Jv		Rev 1.01
Date: Thursday, February 11, 2010		Sheet	64 of 95

For CPU



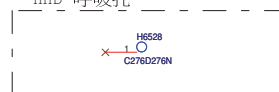
For GPU



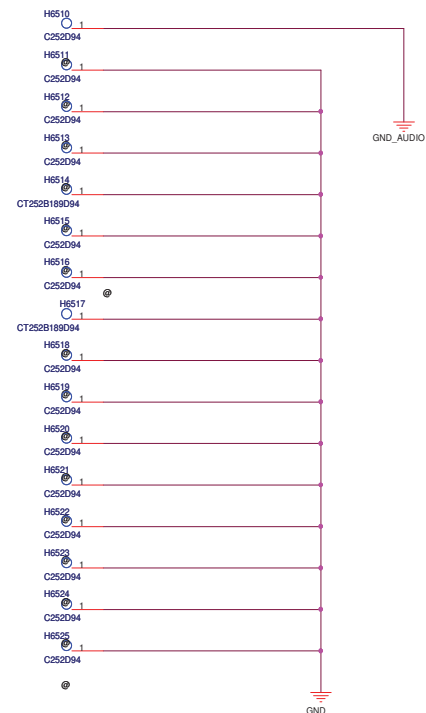
For 橢圓定位孔

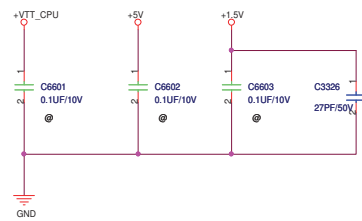


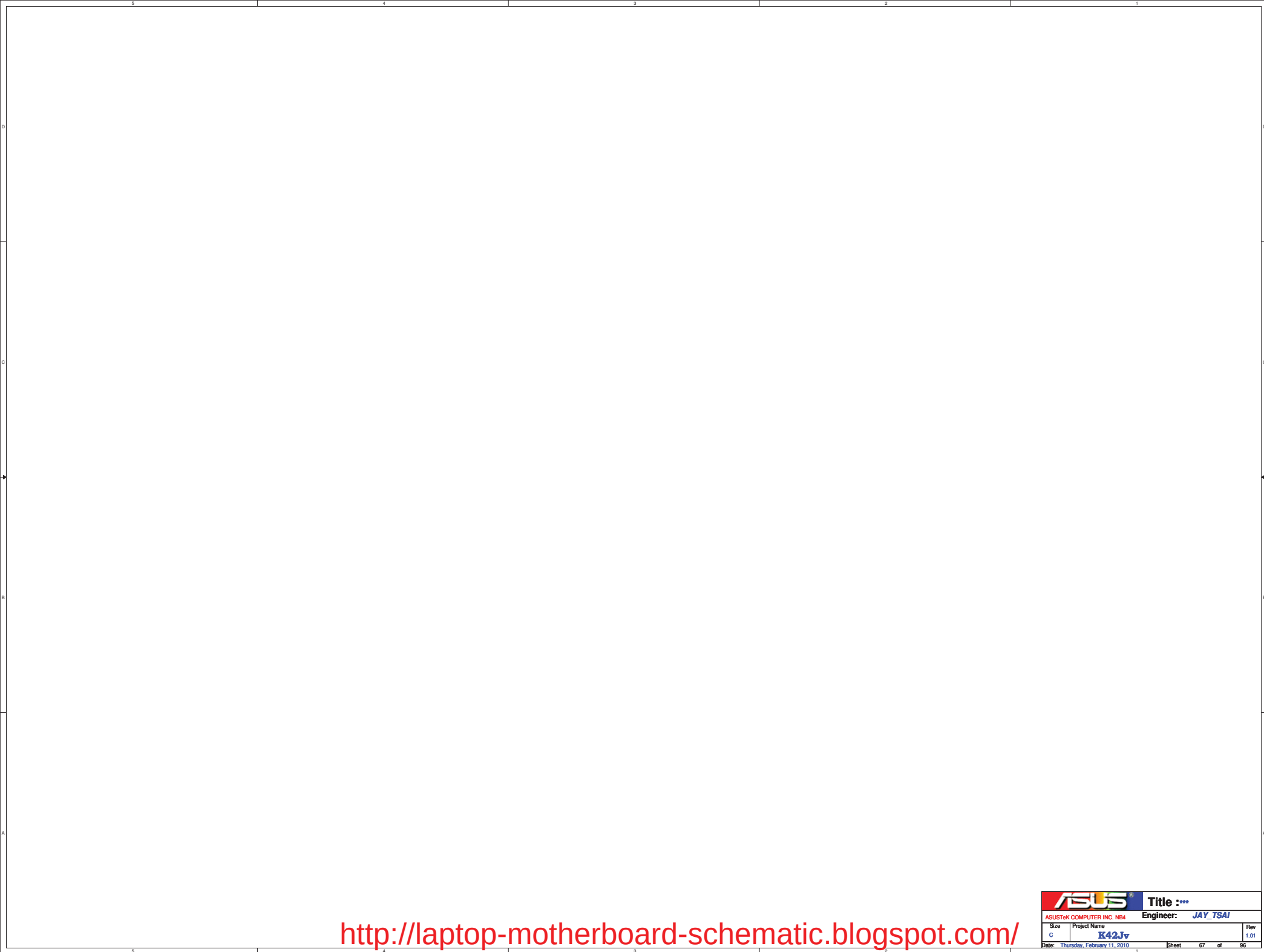
HHD 呼吸孔



Main Board

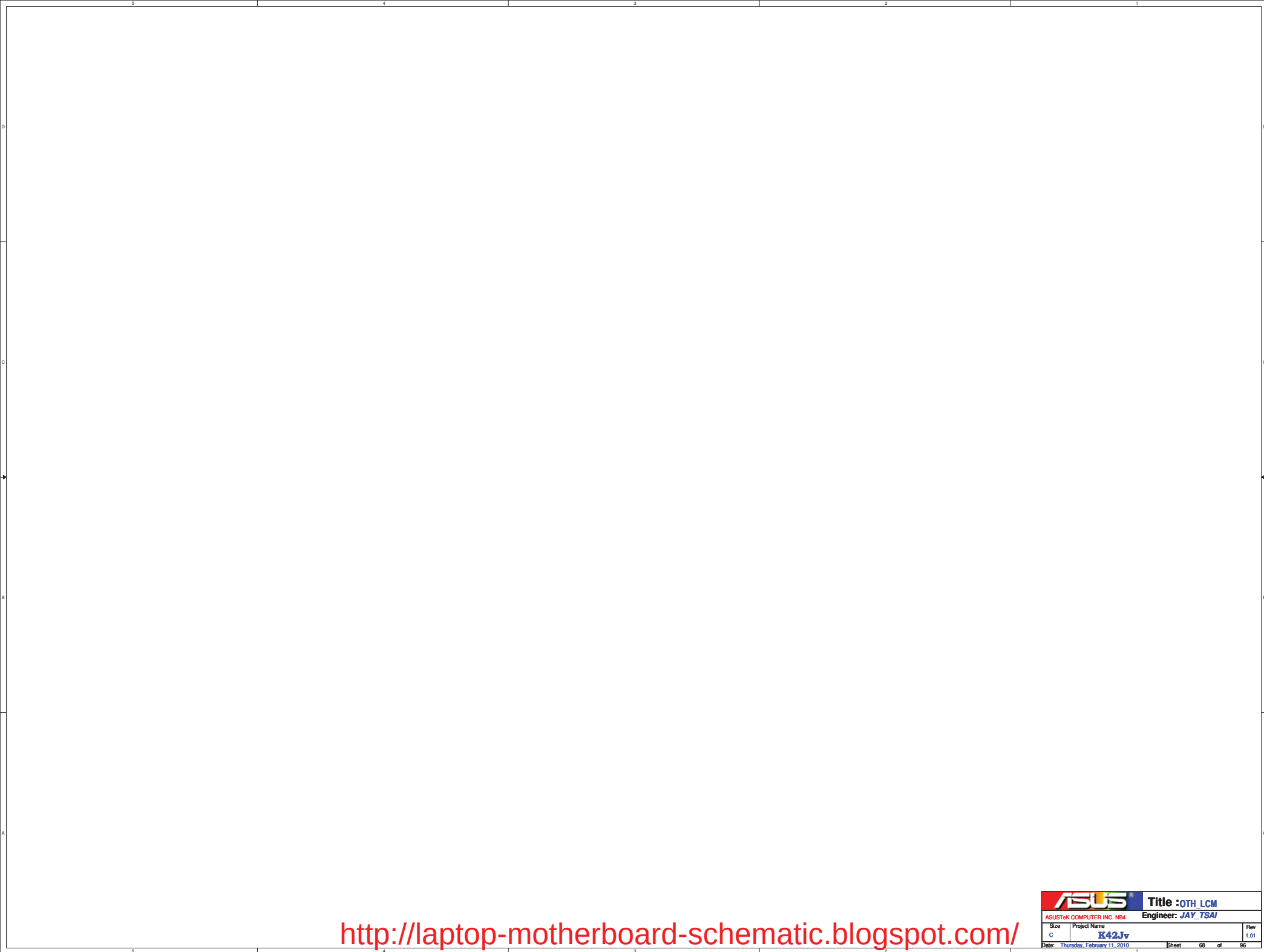






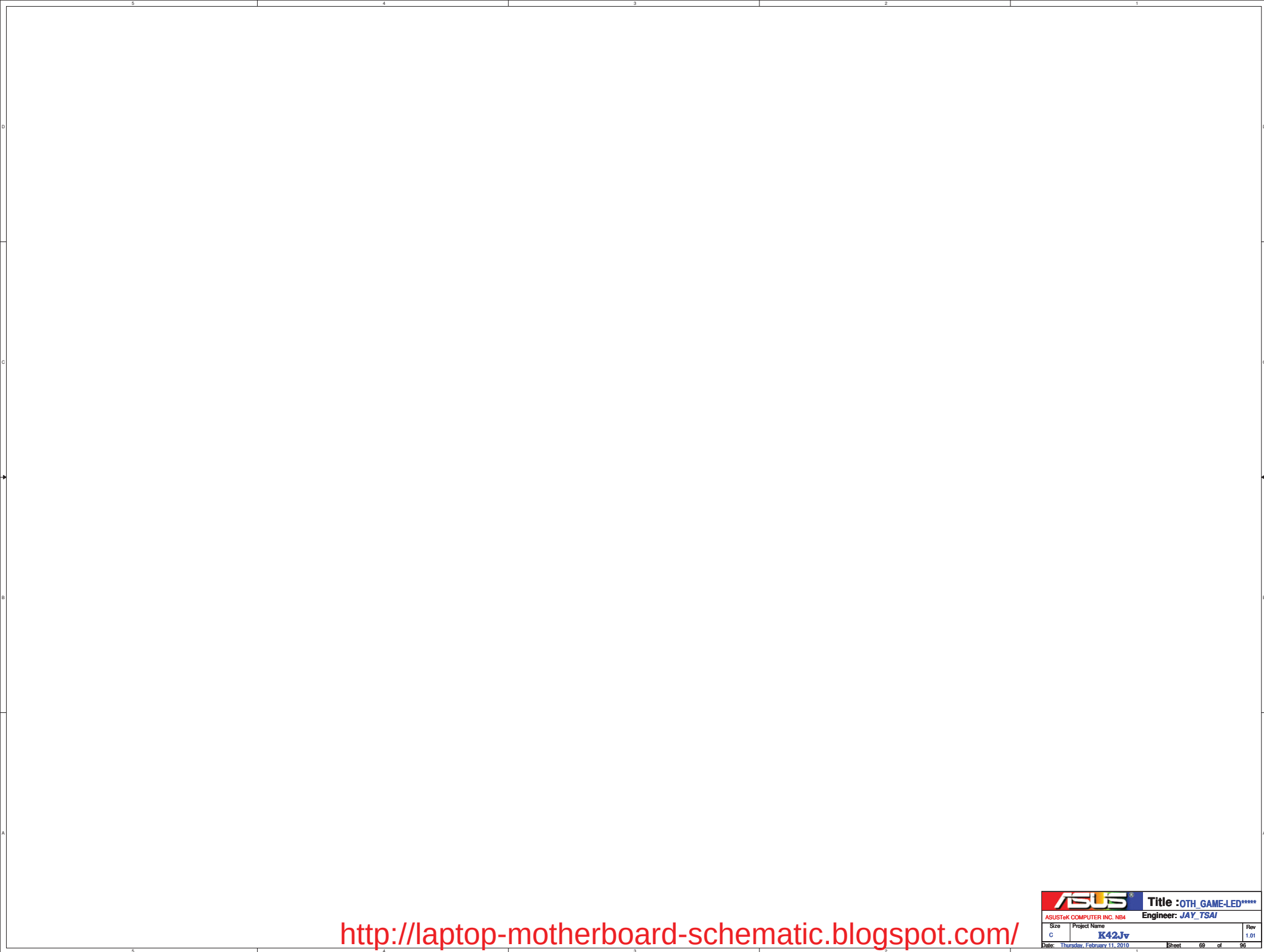
<http://laptop-motherboard-schematic.blogspot.com/>

		Title : ***	
ASUSTeK COMPUTER INC. NBD		Engineer: JAY_TSAI	
Size C	Project Name K42Jv	Rev 1.01	
Date: Thursday, February 11, 2010		Sheet 67 of 96	



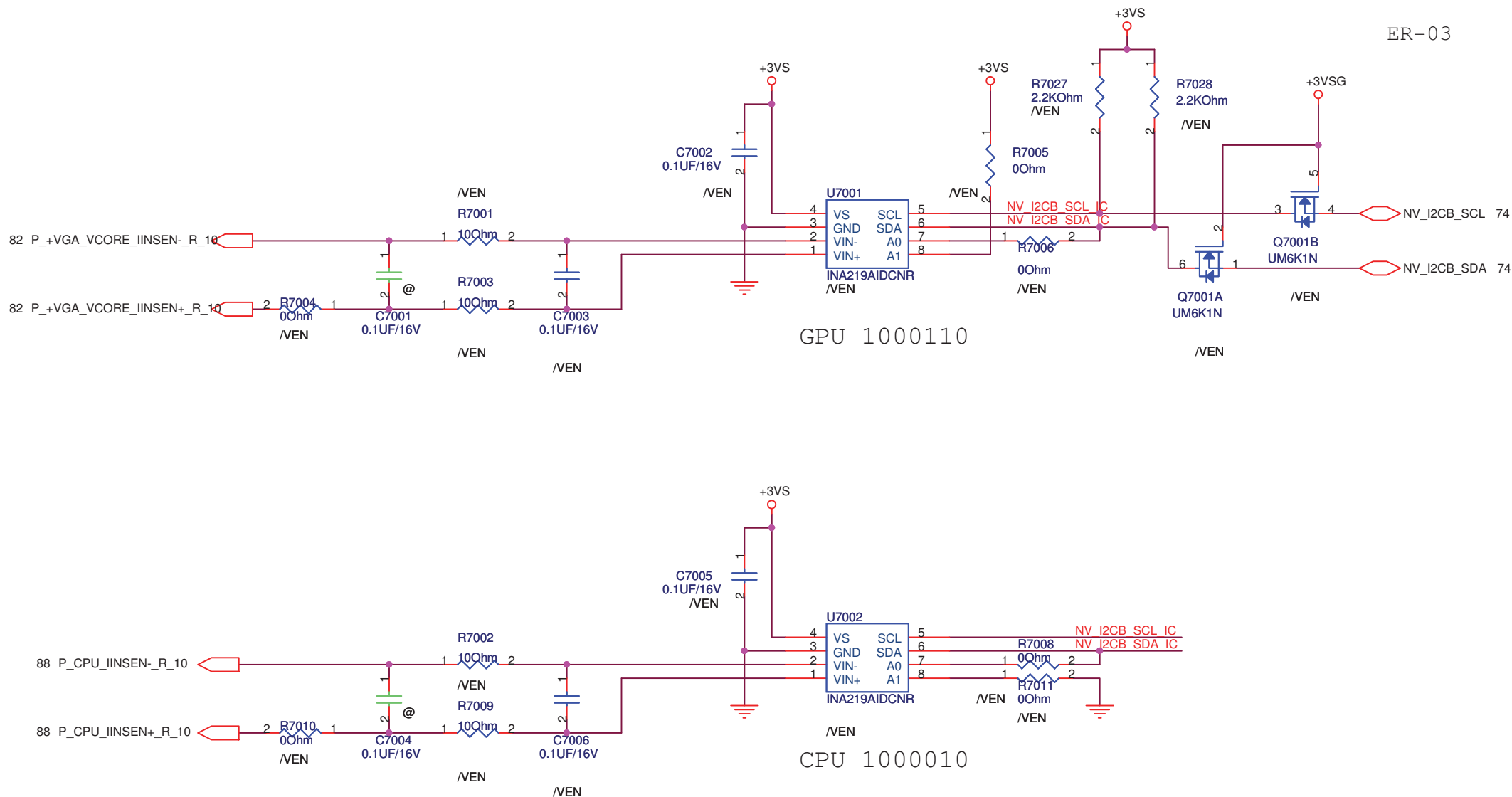
<http://laptop-motherboard-schematic.blogspot.com/>

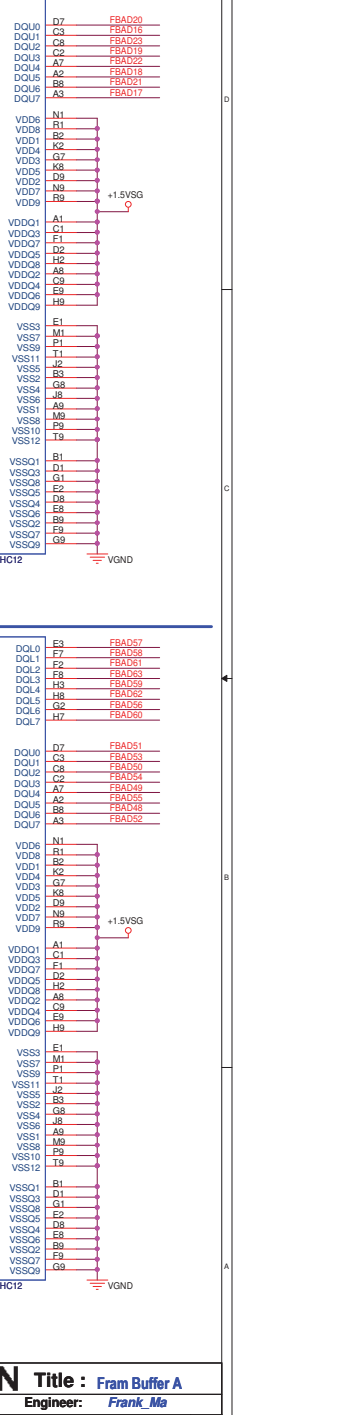
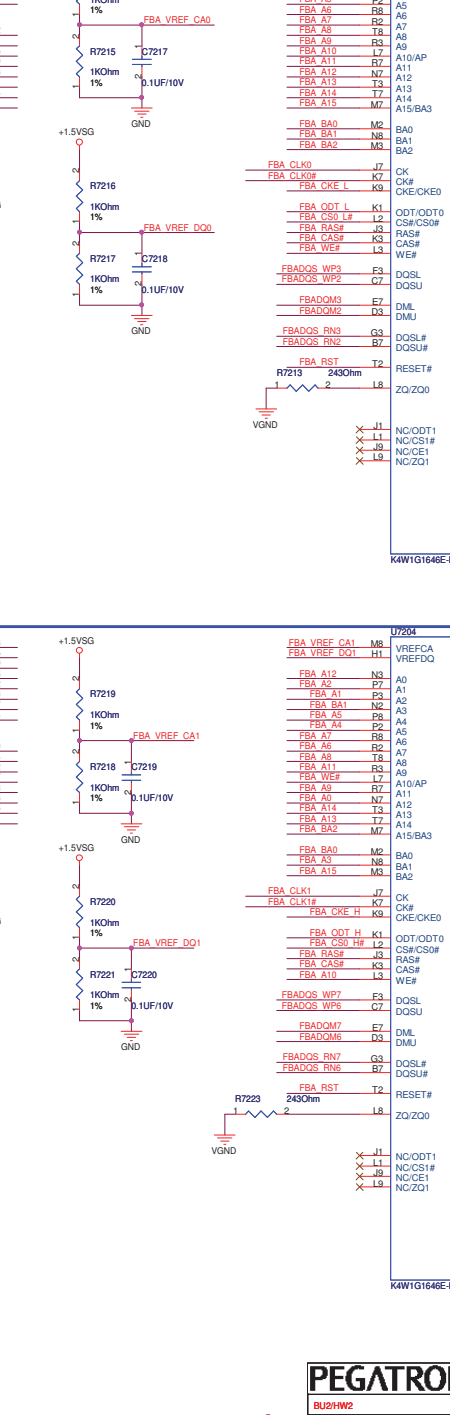
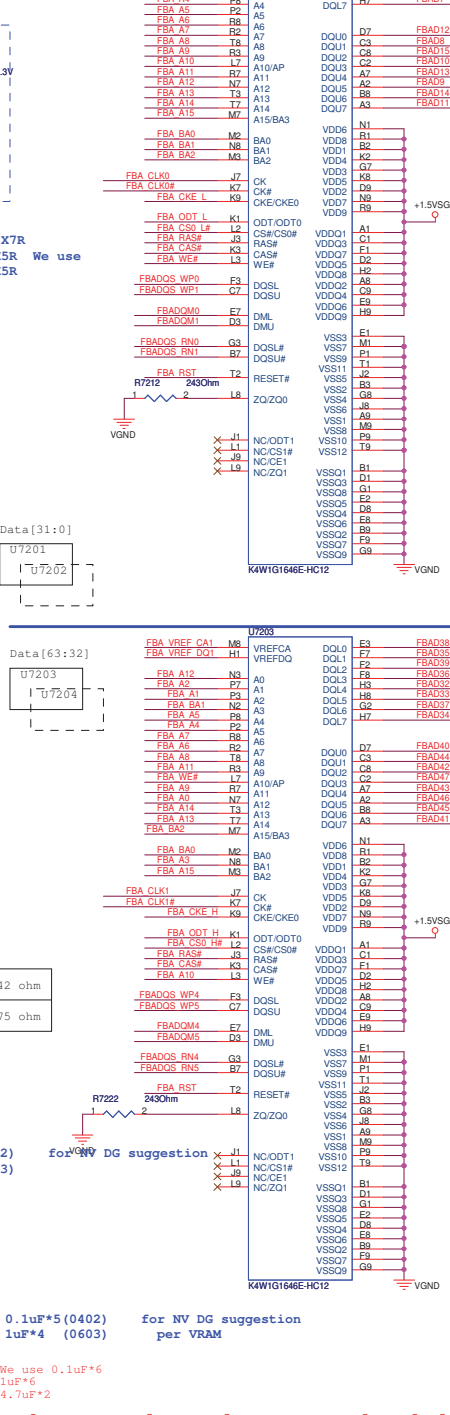
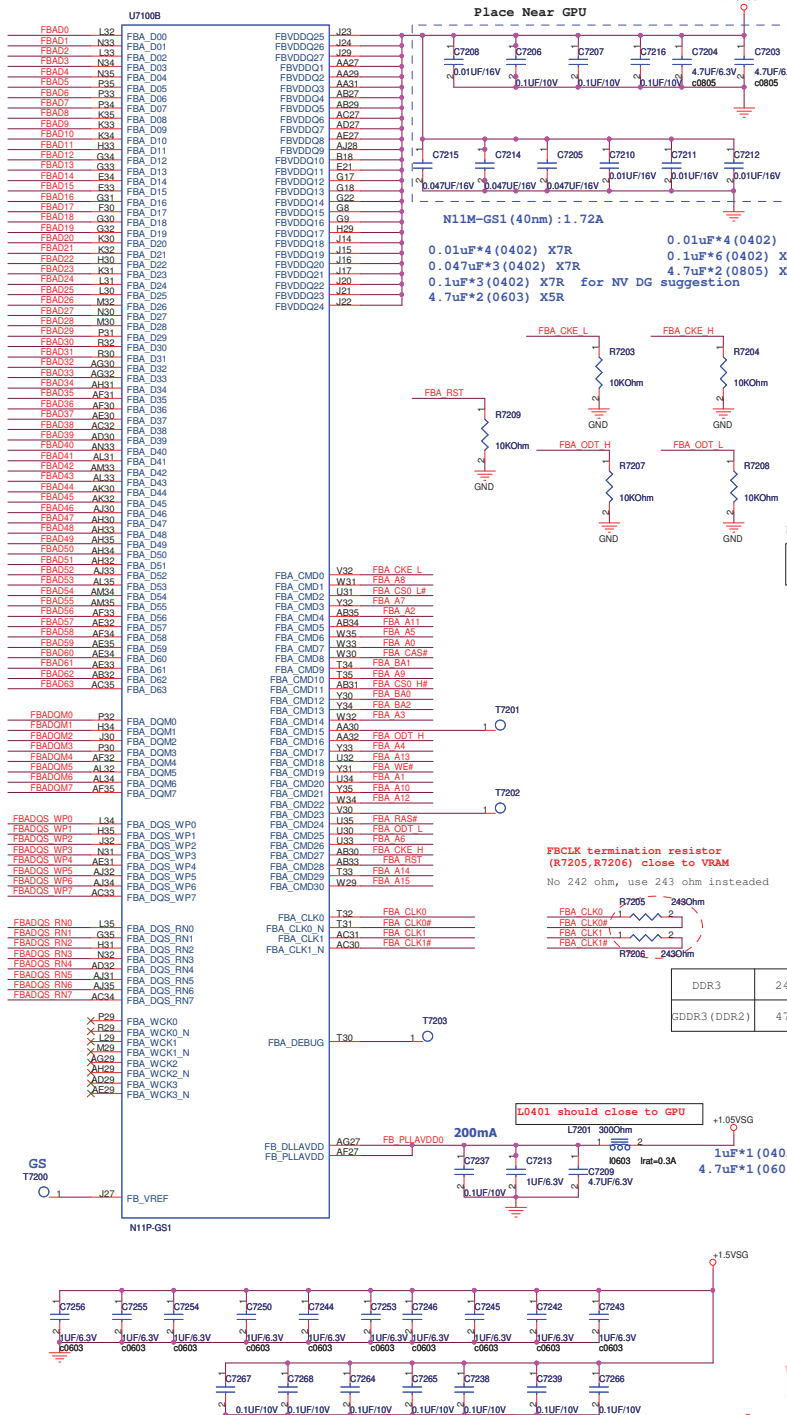
		Title : OTH_LCM	
ASUSTeK COMPUTER INC. NB4		Engineer: JAY_TSAI	
Size C	Project Name K42Jv	Rev 1.01	
Date: Thursday, February 11, 2010		Sheet 68 of 96	

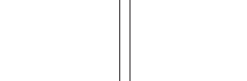


<http://laptop-motherboard-schematic.blogspot.com/>

		Title :0TH_GAME-LED*****	
ASUSTeK COMPUTER INC. NBD		Engineer: JAY_TSAI	
Size	Project Name	Rev	
C	K42Jv	1.01	
Date: Thursday, February 11, 2010		Sheet	69 of 96

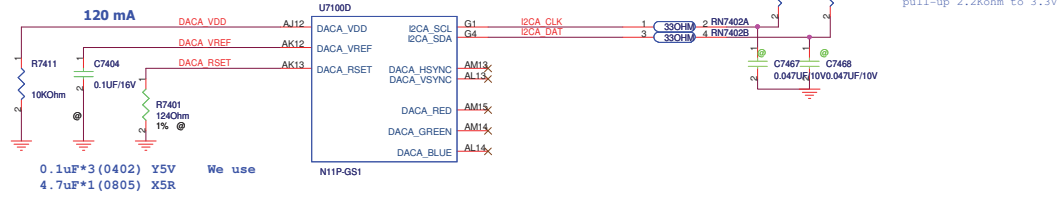




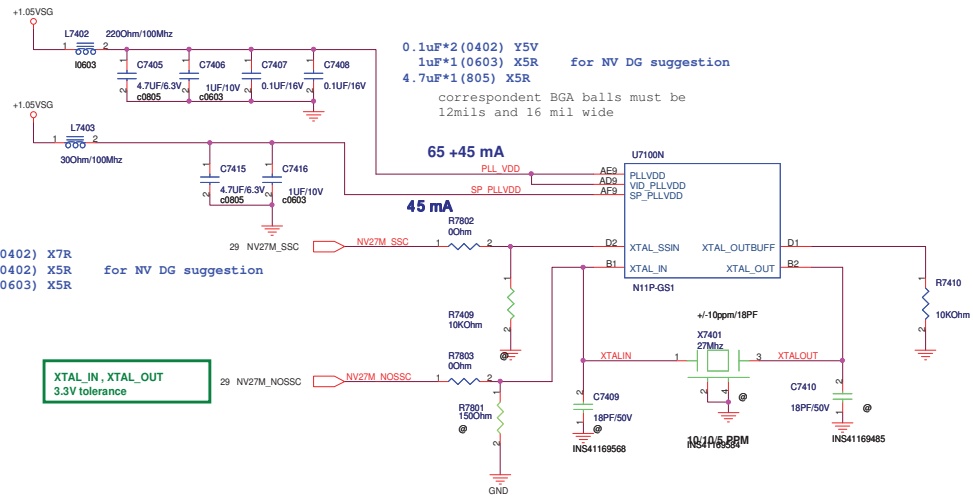
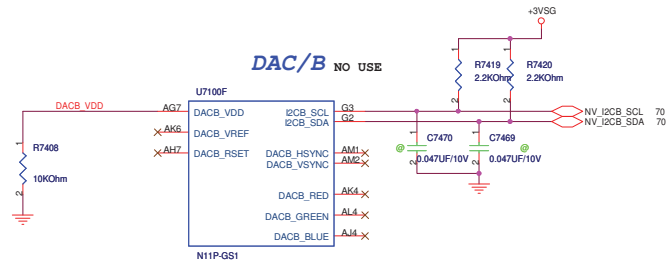


PEGATRON		Title : <i>Frame Buffer C</i>	
<i>BU2/HW2</i>		Engineer: <i>Frank_Ma</i>	
Size C	Project Name K42Jv	Rev 1.0	
Date: <i>Thursday</i> February 11 2010		Sheet 73 of 97	

CRT (DAC/A)



DAC/B NO USE

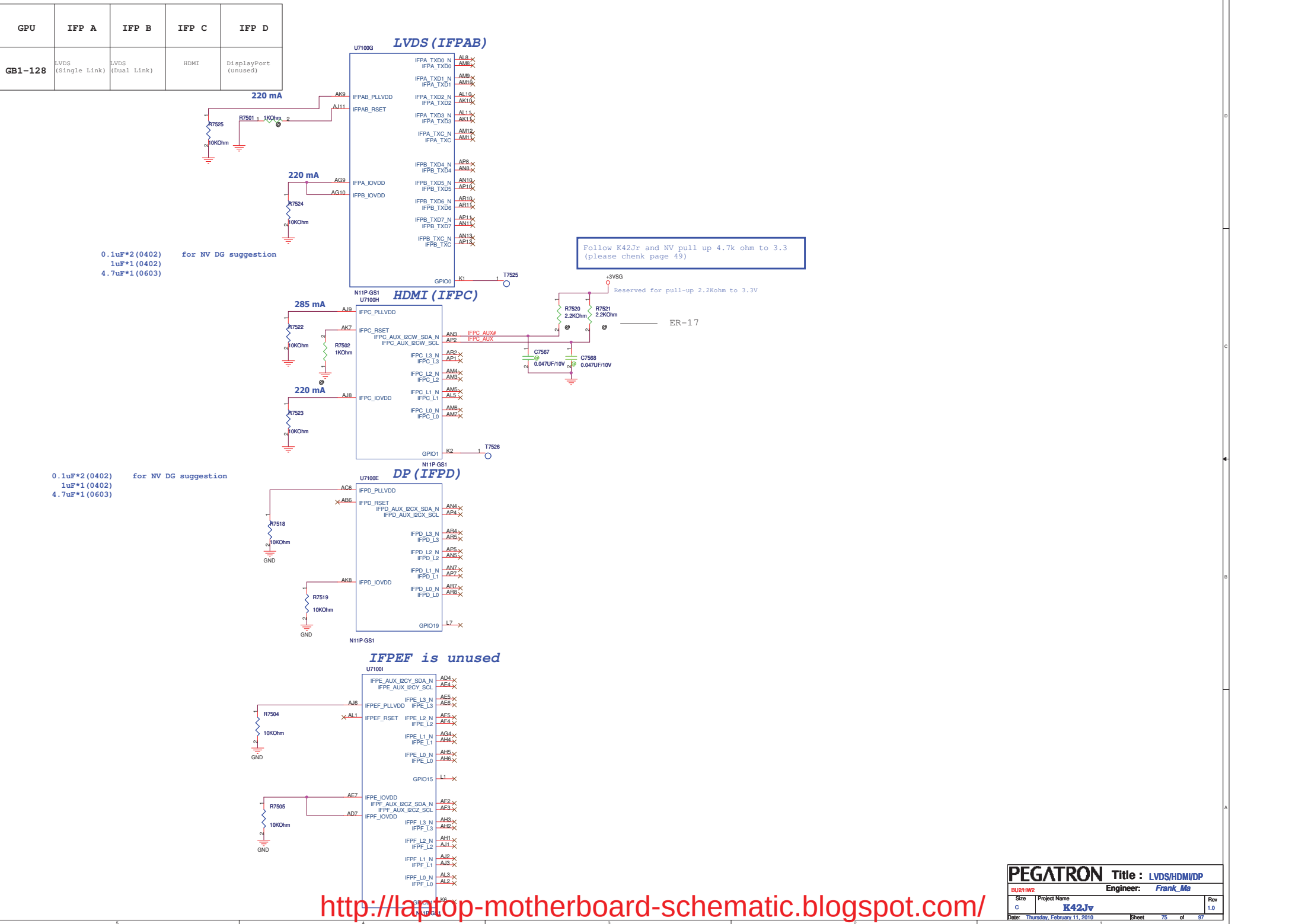


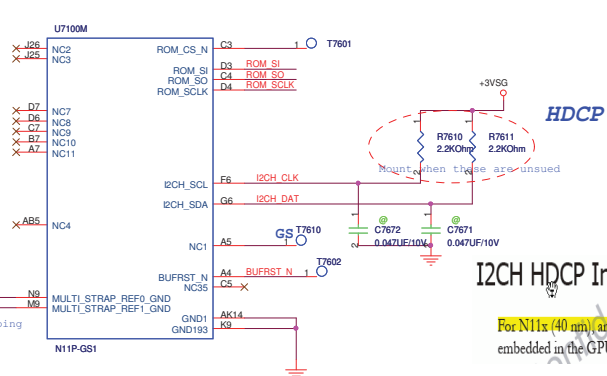
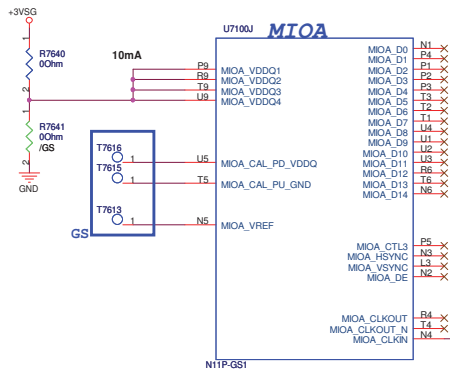
Option /SSC and /XTAL unmount

Ask to FAE if necessary or not

PEGATRON		Title : DACs, CLK GEN	
BU21HW2		Engineer: Frank Ma	
Size	Project Name	Rev	
C	K42Jv	1.0	
Date: Thursday, February 11, 2010		Sheet	74 of 97

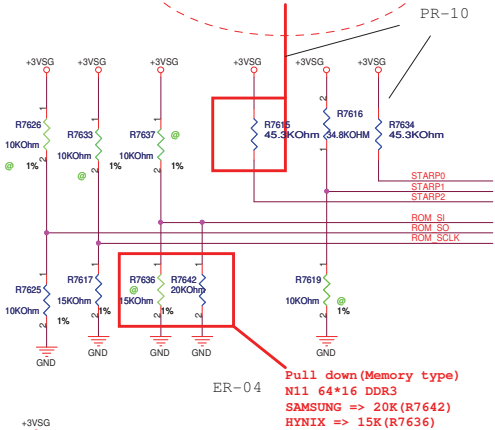
GPU	IFP A	IFP B	IFP C	IFP D
GB1-128	LVDS (Single Link)	LVDS (Dual Link)	HDMI	DisplayPort (unused)





Strap

Check with FAE
Pull up (GPU type) - R7615
N11P-GS1 (40nm) => 45.3K ohm



PR-10
ER-04
Pull down (Memory type)
N11 64*16 DDR3
SAMSUNG => 20K (R7642)
HYUNIX => 15K (R7636)

Table 13-5. Multilevel Strapping Options

Physical Strapping Pin	Power Rail	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SO	VDD33	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	VDD33	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	VDD33	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	VDD33	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	VDD33	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	VDD33	USER[3]	USER[2]	USER[1]	USER[0]

I2CH HDCP Interface

For N11s (40 nm), an external HDCP ROM is not required. HDCP functionality is embedded in the GPU. External connections are not required to support HDCP.

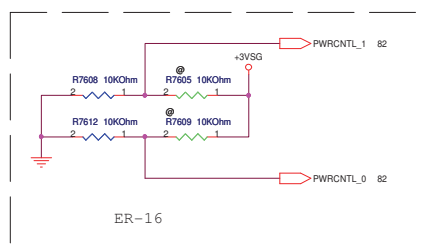
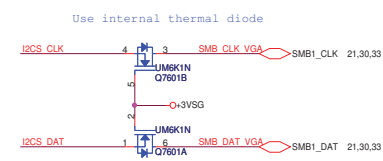
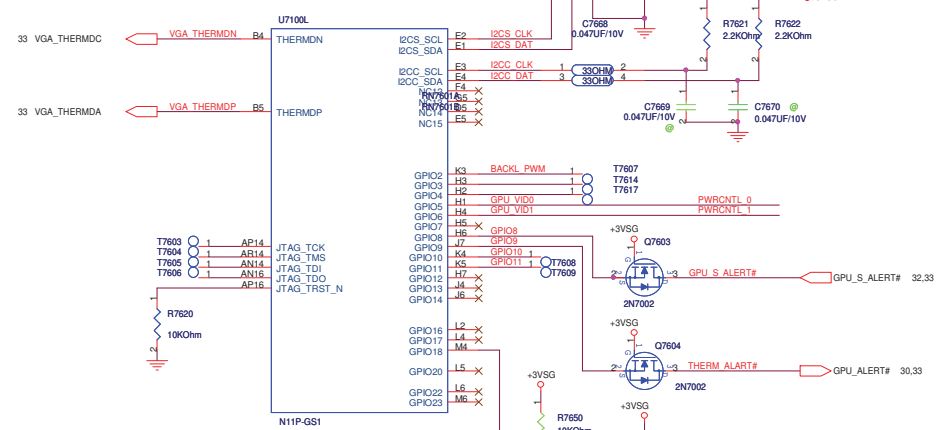
I2C ASSIGNMENTS

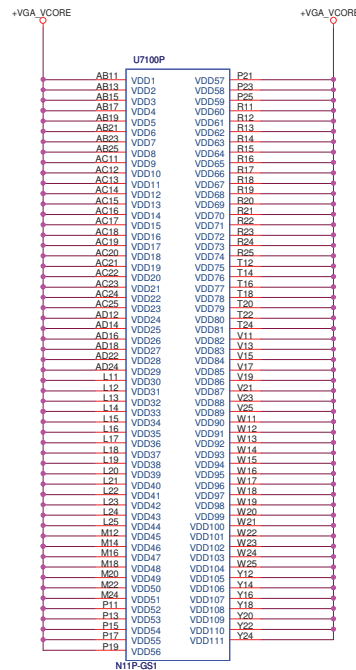
I2CA: CRT --3V
I2CB: N/A
I2CC: LVDS (EDID)
I2CS: Slave for GPU internal thermal
I2CH: HDCP
IFPC_AUX_I2CW: HDMI --3 V
IFPD_AUX_I2CX: DP --3 V
IFPE_AUX_I2CY: N/A
IFPF_AUX_I2CZ: N/A

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	n/a	-	p.75
1	IN	-	IFPC HPD-C (HDMI) p.75
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	-	NVVD0 VID 0
6	OUT	-	NVVD1 VID 1
7	OUT	-	NVVD2 VID 2
8	I/O	LOW	OVERTHERMAL ALERT
9	I/O	LOW	Memory VREF switch
10	OUT	-	SLI faster sync
11	I/O	LOW	AC DETECT
12	IN	-	IFPE HPD-E
13	OUT	-	FAN PWM
14	OUT	-	Reserved
15	IN	-	Reserved
16	IN	-	Reserved
17	IN	-	Reserved
18	IN	-	Reserved
19	IN	-	Reserved
20	IN	-	Reserved
21	IN	-	Reserved
22	IN	-	Reserved
23	I/O	-	SLI swap ready signal

GPIO





ER Modify list:

- ER-01 : For VTT Power adjustable and DRAM power fix
 - ER-02 : Exchange PIN 2 and PIN 3 connection and Power rail chagne from +3VS to +5VS.
 - ER-03 : Add /Ven lable for Ventura option.
 - ER-04 : According GPU strap define setting to P.D.
 - ER-05 : LCD backlight control change to accord DESIGN IP.
 - ER-06 : Change R2404 to 330HM for EA measurement.
 - ER-07 : Unmount External thermal sensor change to use DGPU internal thermal sensor.
 - ER-08 : According for VTT power default setting.
 - ER-09 : To change from +1.8VSG to +1.5VSG.
 - ER-10 : PCB ID change from SR to ER setting.
 - ER-11 : ALC269 ver B. must add 10K P.U for PD# pin.
 - ER-12 : Modify Crystal Rd location and add /USB30 lable.
 - ER-13 : For Smart33 Down freq. and reserve over clock design.
R2933 mount 4.7K 0603 at ER stage.
 - ER-14 : Modify power rail to +5VS_AUDIO.
 - ER-15 : R3631 change from 10K to 0R.
 - ER-16 : Setting DGPU Vcore default power to 0.8V.
 - ER-17 : Unmount R7520,R7521 from vendor suggestion.
 - ER-18 : Reserve vendor solution add 0R for bypass other circuit.
 - ER-19 : Change USB port to 2.0 connector and design only for USB 2.0.
 - ER-20 : For line-in channel ,HP jack sensor must change to 10K.
 - ER-22 : To resolve "3622146 A Voltage Spike on Graphics Core Rail (Vaxg) to 1.5V seen during system shutdown"change from 4.7K to 470 OHM.
 - ER-23 : Follow Design IP,change to P.D.
 - ER-24 : Change mount for smart 33 control Vcore power.
- For cost down and short jump ,Please search "C.D"

PR Modify list:

- PR-01 : Change R2933 to 10K 0402.
- PR-02 : Mic bias voltage change from +5VS_AUDIO to CODEC's PIN28(integreated regulator).To avoid MIC noise by drity power.
- PR-03 : Change R3631 from 0R to short jump.
- PR-04 : Add level shift circuit.
- PR-05 : Del RN9250.
- PR-06 : Add for pop and click sounds.
- PR-07 : Change for B to B re-design.(copy from K42JC schematic)
- PR-08 : EMI/ESD request.
- PR-09 : Add MGRL of headset device design.
- PR-10 : According to vendor suggestion.(45K change to 45.3K)
- PR-11 : Bypass INT. MIC amplifier.
- PR-12 : VTT,+1.5V,VCORE power set to default normal power rails.
- PR-13 : Codec IC(ALC269) change from VB2 to VB5.
- PR-14 : PCB ID change from ER to PR setting.

PWRCNTL_1	PWRCNTL_0	VGA_VCORE
0	0	0.801V
0	1	0.852V
1	0	0.901V
1	1	0.952V

Controller

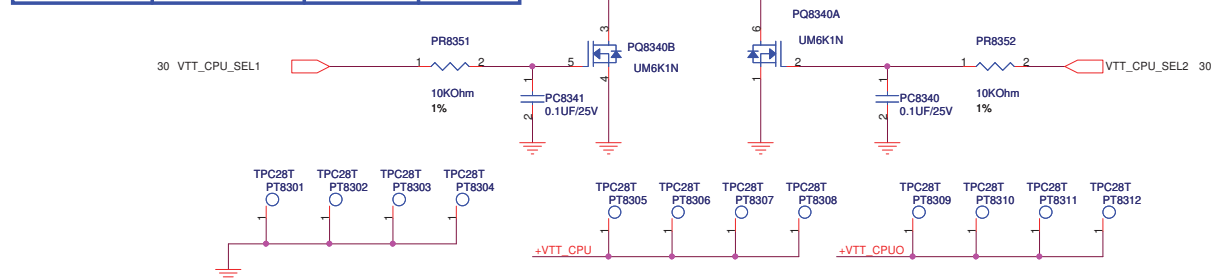
1. Voltage & Current:
+1.2VSUS: 16A
2. Frequency:
Ton=3.85p*Rt(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)=500KHZ
3. Soft start time:
Soft-Star duration is 1.35ms
5. Inrush Current:
C total =220uF
I inrush=0.163A

Power stage

1. I/P Current:
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 0.85A$
2. Ripple Current:
Ripple=3.74A
- 3.ripple voltage:
 $I_{peak} = (v_{in}-v_o) \cdot D / (L \cdot F_{sw}) = 2.07A$
DCR=3.3mohm
V=6.831mV
4. Inductor Spec: 3. OCP:
Isat=25A
Idc=15.5A
DCR=5.5mohm
5. MOSFET Spec:
H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

<Variant Name>
ASUS Title : Power_VGA_VCORE
 ASUSTeK COMPUTER INC Engineer:
 Size Project Name
 C Oemga
 Date: Thursday, February 11, 2010 Sheet 82 of 1 Rev 1.0

VTT_CPU_SEL1	VTT_CPU_SEL2	+VTT_CPU	
0	0	1.041V	DV3
0	1	1.059V	DV2
1	0	1.078V	DV1
1	1	1.097V	Normal



Controller

- Voltage & Current:**
+VCCP:1.05V@10A
- Frequency:**
Ton=3.85p*Rt(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)=500KHZ
- OCP:**
Set PR7343=18KOhm
Iocp=Rocp*20/Rds(on)=22A
- Soft start time:**
Soft-Star duration is 1.35ms
- Inrush Current:**
C total = 200 uF
I inrush= 0.16 A

Power stage

- I/P Current:**
I in = Vo*Io/(0.75 * Vin)=2.3 A
- Ripple Current:**
Iripple=2.8A
- Dynamic:**
Ipeak=1.98A
DCR=3.3mohm
V=6.534mV
- Inductor Spec:**
Isat=16A
Idc=11A
DCR=9mOhm
- MOSFET Spec:**
H-side and L-side MOSFET:RJK0355DPA-00-JO WPAK
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

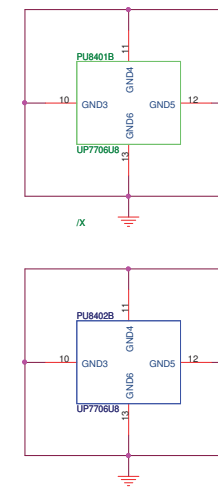
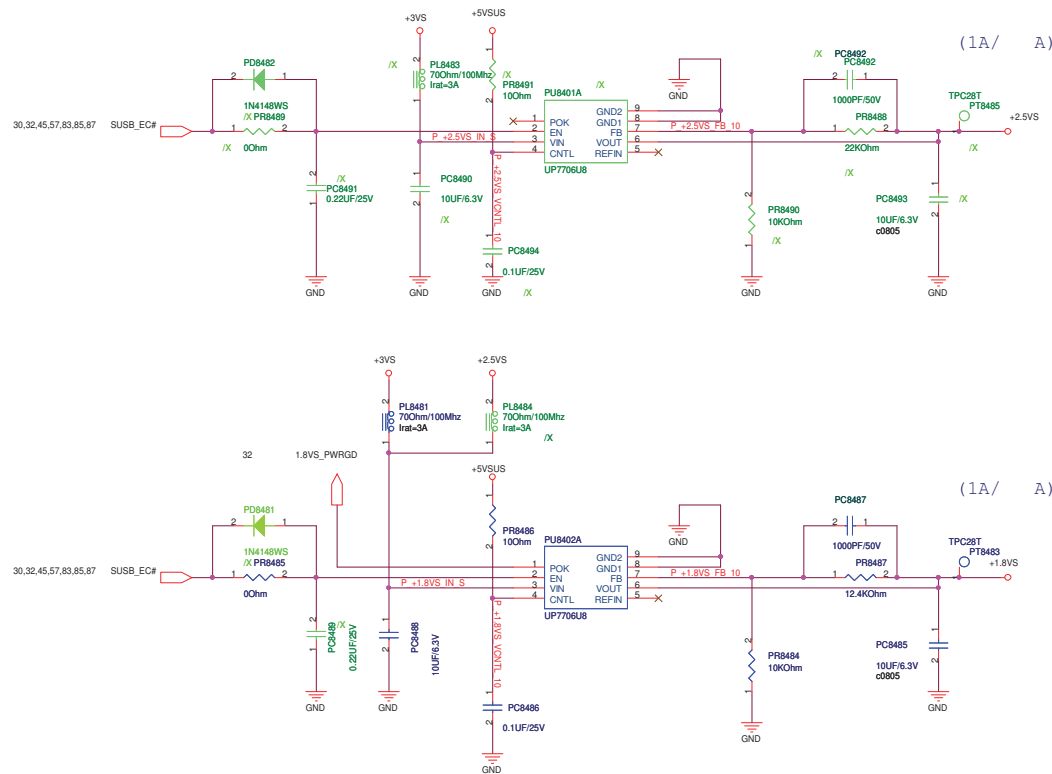
ASUSTeK COMPUTER INC

Title : Power_+VCCP

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Thursday, February 11, 2010 Sheet 83 of 1



Controller	Power stage
1. Voltage & Current: +1.8V: +1.8V & 12A 2. Frequency: $T_{on} = 3.85 \mu s \cdot R_t(on) \cdot V_o / V_{in} - 0.5$ Frequency = $V_{out} / (V_{in} \cdot T_{on})$ = 500KHZ 3. OCP: Set PR7343 = 18kohm $I_{ocp} = R_{ocp} \cdot 20 / R_{ds(on)}$ = 20 * 21.5 / 16.5 = 26A 4. Soft start time: Soft-Star duration is 1.35ms 5. Inrush Current: C total = 100uF $I_{inrush} = 0.133A$	1. I/P Current: $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 0.947A$ 2. Ripple Current: $I_{ripple} = 2.342A$ 3. Ripple Voltage: $I_{peak} = (V_{in} - V_o) \cdot D / (L \cdot F_{sw}) = 3.25A$ DCR = 3.3mohm V = 10.75mV 4. Inductor Spec: $I_{sat} = 36A$ $I_{dc} = 18A$ DCR = 3.3mohm 5. MOSFET Spec: H-side and L-side MOSFET: $R_{ds(on)} = 16.5m\Omega$ ($V_{gs} = 4.5V$) $I_{cont} = 30A$ ($T = 25$) $I_{peak} = 120A$ (Pause < 10us)

<Variant Name>

ASUS **Title : Power_+1.8V&+0.9V**

ASUSTeK COMPUTER INC. **Engineer:**

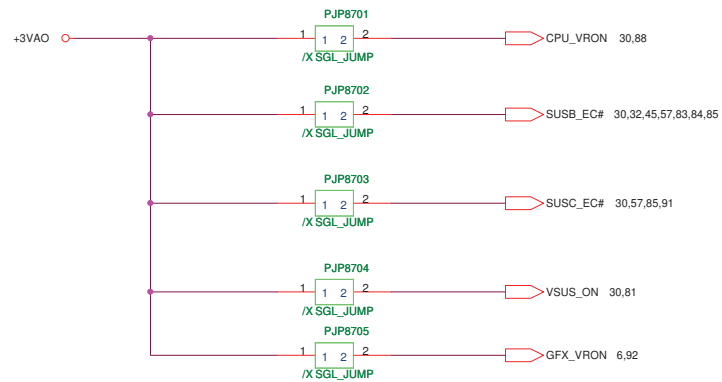
Size	Project Name	Rev
C		1.0

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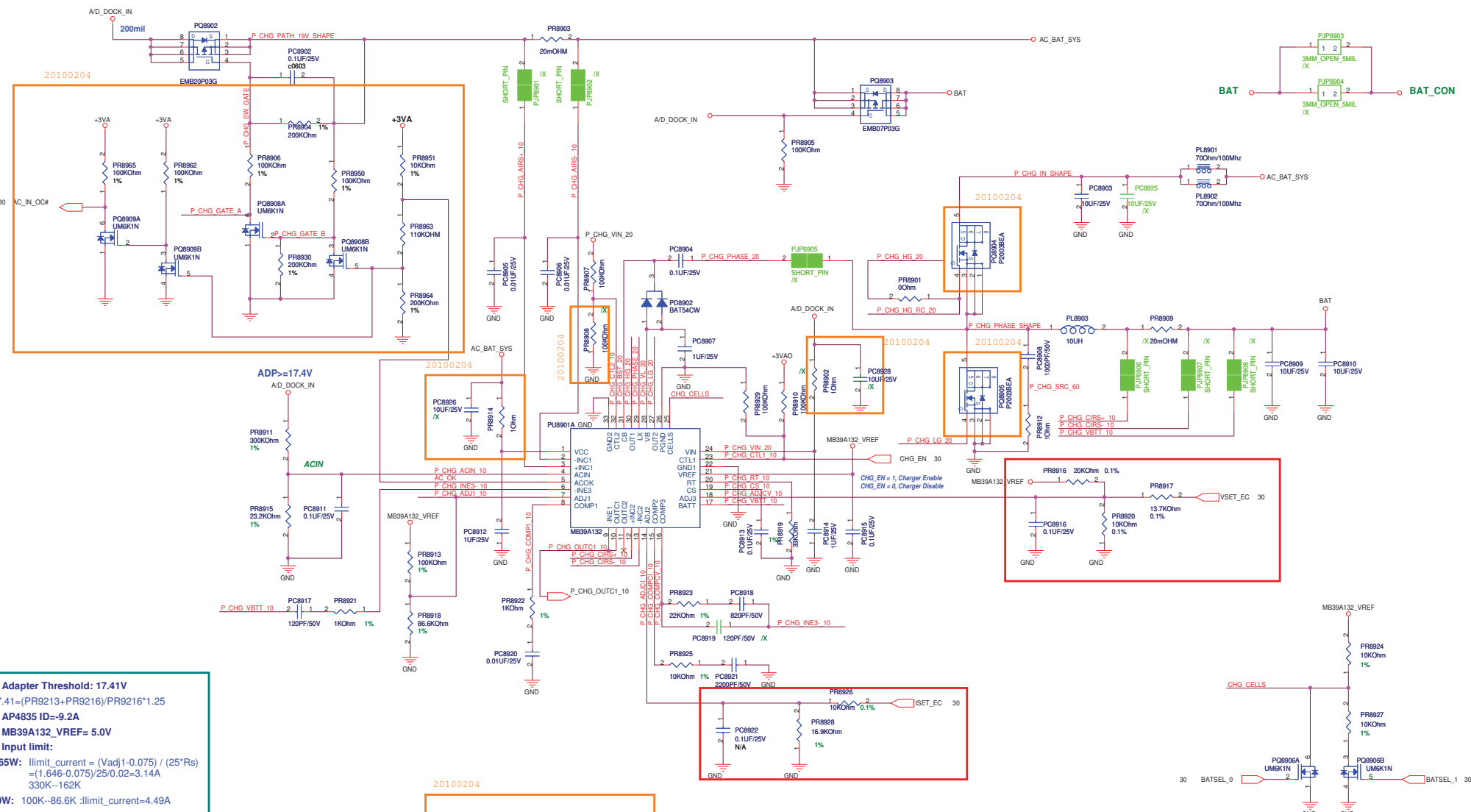
<http://laptop-motherboard-schematic.blogspot.com/>

<Variant Name>			
		Title: Power_good_detector	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom		1.0	
Date: Thursday, February 11, 2010		Sheet	86 of 1



<Variant Name>

		Title : Power_for_test	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom		1.0	
Date: Thursday, February 11, 2010		Sheet	87 of 1



- 1. Adapter Threshold: 17.41V**
 $17.41 = (PR9213 + PR9216) / PR9216 * 1.25$
- 2. AP4835 ID=9.2A**
- 3. MB39A132_VREF= 5.0V**
- 4. Input limit:**
65W: $I_{limit_current} = (V_{adj} - 1.075) / (25 * R_s) = (1.646 - 0.075) / 25 * 0.02 = 3.14A$
330K-162K
90W: 100K-86.6K : $I_{limit_current} = 4.49A$
- 5. Charging Voltage**

VSET_EC	2S	3S	4S
2.9894	3.399	12.598	16.797
- 6. Charging current**

ISET_EC	ICHG	Ps
1.3071	1492	1P
2.1094	2500	2P
3.3	3996	3P

- Controller**
- 1. Frequency:**
 $f_{osc}(KHz) = 17000 / RT (KOhm)$
 $f_{osc}(KHz) = 17000 / 33K = 515KHz$
 - 2. OCP:**
 $I_{oc} = 0.2 / R_s = 10A$
 - 3. Soft start time:**
 $t_s(s) = 0.26 * CS(uF) = 0.26 * 0.1 = 26ms$
 - 4. Inrush current(3S):**
 $I_{inrush} = C * V / t = 9.7mA$

- Power stage**
- 1. I/P Current(3S2P):**
 $I_{in} = V_o * I_o / (0.75 * V_{in}) = 2.21A$
 - 2. Ripple Current(3S2P):**
 $r_{ripple} = 1.18A$
 - 3. Inductor Spec:**
 $I_{sat} = 4.4A$
 $I_{dc} = 3.8A$
 $DCR = 35mohm$
 - 4. MOSFET Spec:**
 $I_{dc} = 6.5A / 5.0A$
 $R_{dson} = 22 / 30mohm$
 $V_{gsth} = 0.8 - 1.8V$

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EC Code: 202

ASUS		Title : Power Charger	
ASUSTek Computer INC.		Engineer: Limy Ji	
Size	Project Name	Rev	
C		1.0	
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<http://laptop-motherboard-schematic.blogspot.com/>

<Variant Name>

**ASUS**[®]

Title : Power_Charger

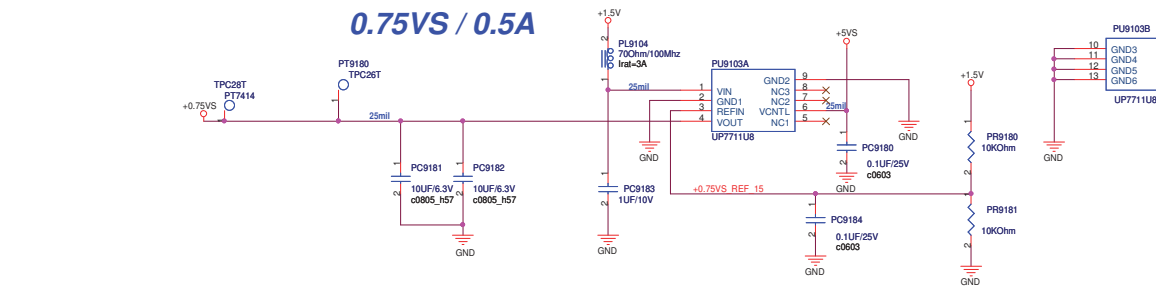
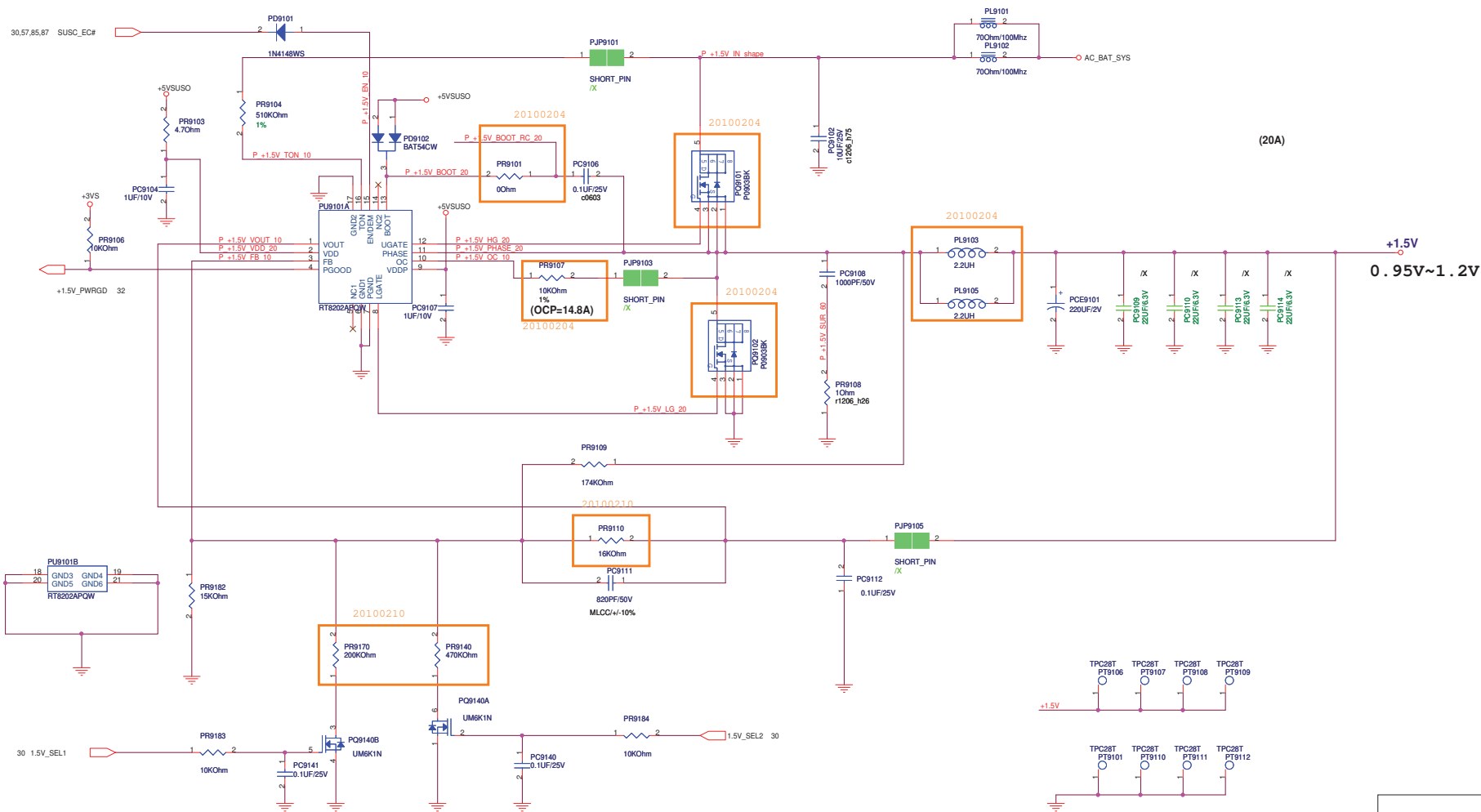
ASUSTek Computer INC.

Engineer: Limy_Ii

Size	Project Name	Rev
A3	F83T	2.1G

Date: Thursday, February 11, 2010

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1.5V_SEL1	1.5V_SEL2	+1.5V	
0	0	1.483V	DV3
0	1	1.506V	DV2
1	0	1.538V	DV1
1	1	1.561V	Normal

Controller

1. Voltage & Current:
+1.2VSUS: 16A

2. Frequency:
Ton=3.85p*Rt(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)
=500KHz

3. OCP:
Set PR8107=21.5kohm
Iocp=Rocp*(Vin-Ton)=26A

4. Soft start time:
Soft-Star duration is 1.35ms

5. Inrush Current:
C total =220uF
I inrush=0.163A

Power stage

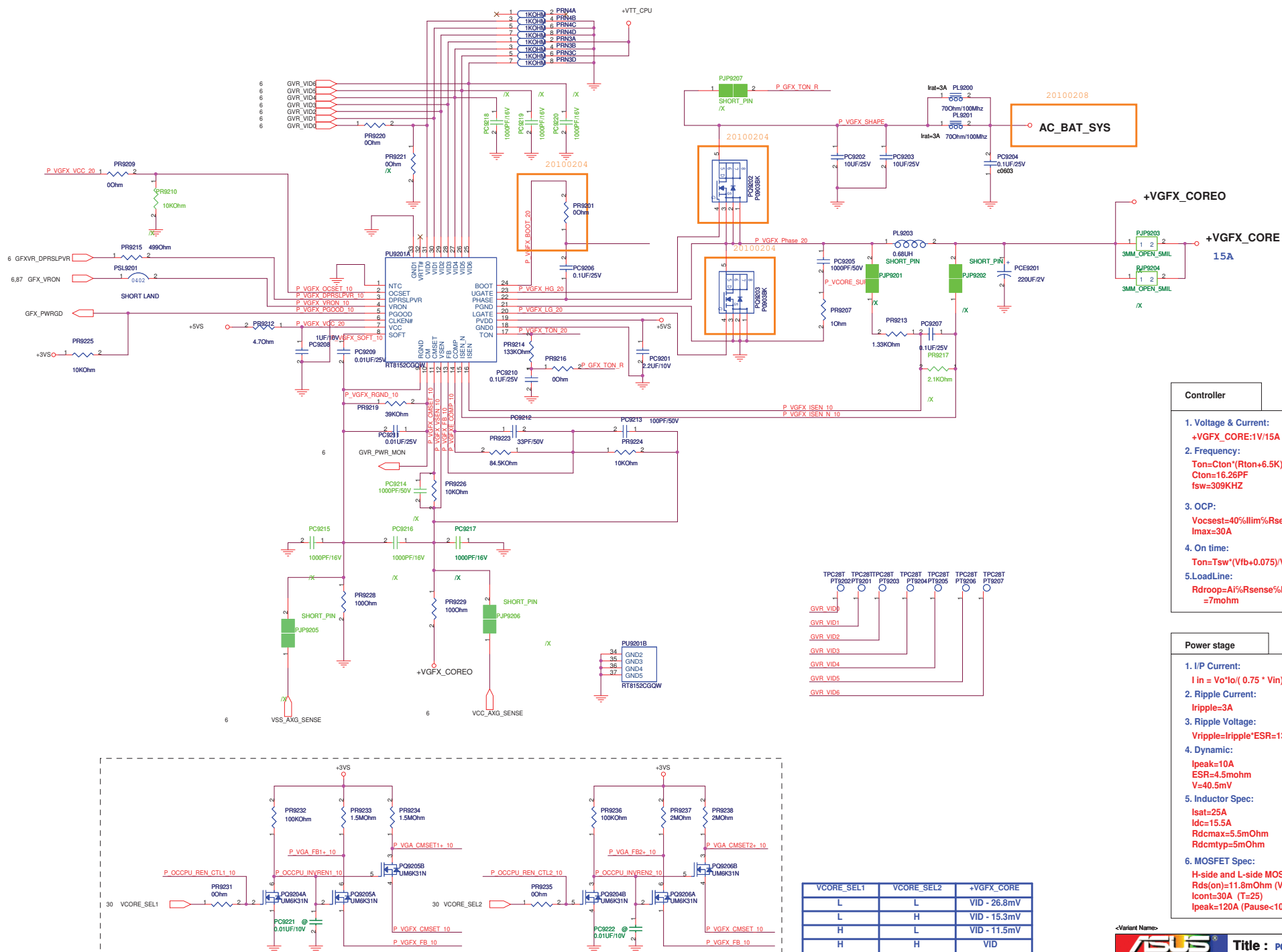
1. I/P Current:
 $I_{in} = V_o I_o / (0.75 * V_{in}) = 0.85A$

2. Ripple Current:
Iripple=3.74A

3.ripple voltage:
 $I_{peak} = (v_{in} - v_o) * D / (L * F_{sw}) = 2.07A$
DCR=3.3mohm
V=6.831mV

4. Inductor Spec:
Isat=25A
Idc=15.5A
DCR=5.5mohm

5. MOSFET Spec:
H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)



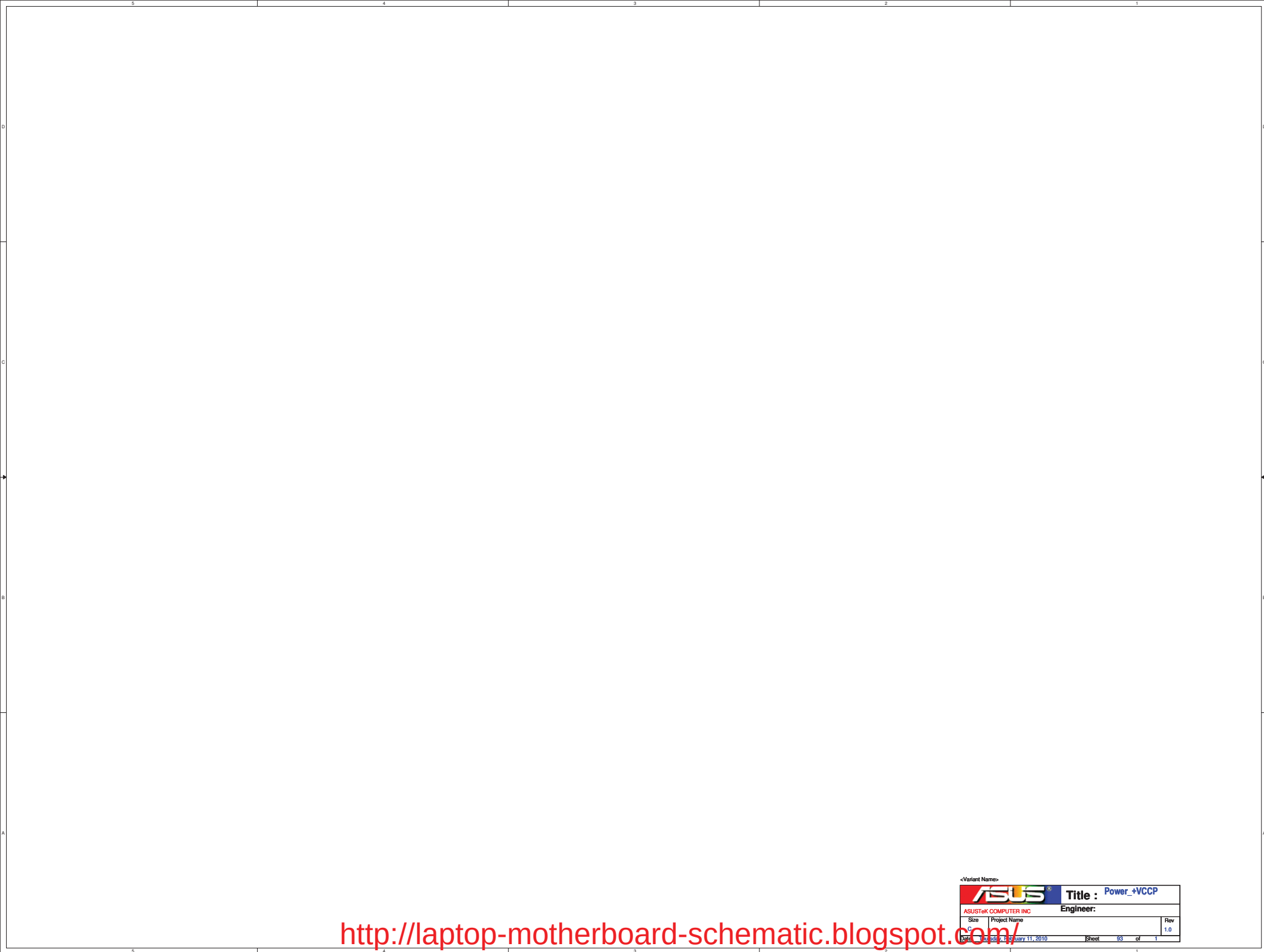
- Controller**
- Voltage & Current:**
+VGFX_CORE:1V/15A
 - Frequency:**
 $Ton = Cton \cdot (Rton + 6.5K)$
 $Cton = 16.26PF$
 $fsw = 309KHZ$
 - OC:**
 $Vocset = 40\% \cdot Ilim \cdot R_{sense}$
 $I_{max} = 30A$
 - On time:**
 $Ton = Tsw \cdot (Vfb + 0.075) / Vin = 354ns$
 - LoadLine:**
 $Rdroop = \Delta I \cdot R_{sense} \cdot R1/R2$
 $= 7mohm$

- Power stage**
- I/P Current:**
 $I_{in} = Vo \cdot Io / (0.75 \cdot Vin) = 1.33A$
 - Ripple Current:**
 $I_{ripple} = 3A$
 - Ripple Voltage:**
 $V_{ripple} = I_{ripple} \cdot ESR = 13.5mV$
 - Dynamic:**
 $I_{peak} = 10A$
 $ESR = 4.5mohm$
 $V = 40.5mV$
 - Inductor Spec:**
 $I_{sat} = 25A$
 $I_{dc} = 15.5A$
 $R_{dcmax} = 5.5mOhm$
 $R_{dcmtyp} = 5mOhm$
 - MOSFET Spec:**
H-side and L-side MOSFET: RJK0355
 $R_{ds(on)} = 11.8mOhm$ ($V_{gs} = 4.5V$)
 $I_{cont} = 30A$ ($T = 25$)
 $I_{peak} = 120A$ (Pause < 10us)

VCORE_SEL1	VCORE_SEL2	+VGFX_CORE
L	L	VID - 26.8mV
L	H	VID - 15.3mV
H	L	VID - 11.5mV
H	H	VID

ASUS
ASUSTeK COMPUTER INC. NB
Project Name: **UX21**
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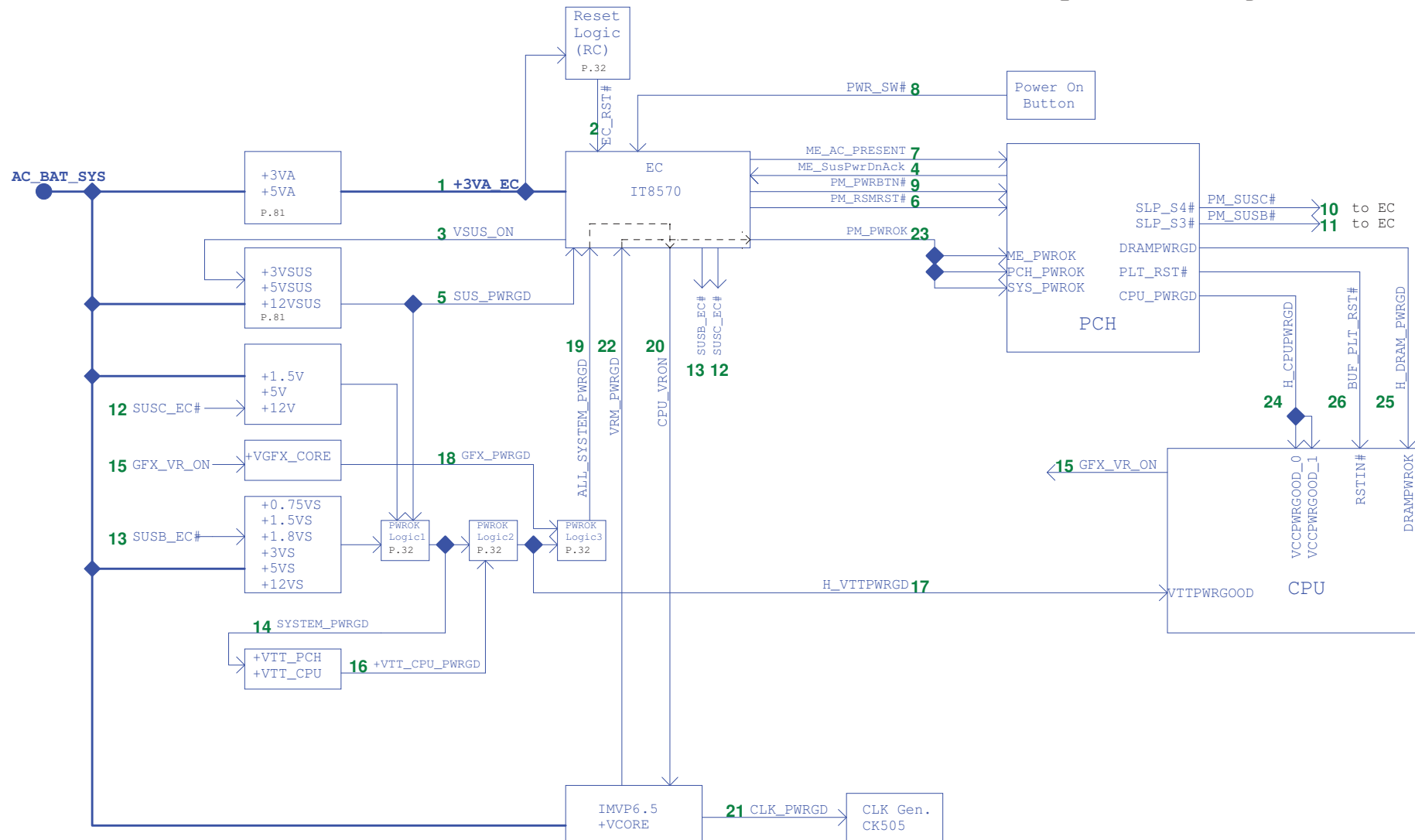
Title: POWER_VCORE
Engineer: **Limy_H**
Rev: 1.0



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<Variant Name>			
		Title : Power_+VCCP	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
C		1.0	
Date	Sheet		of
2010/02/11	93		1





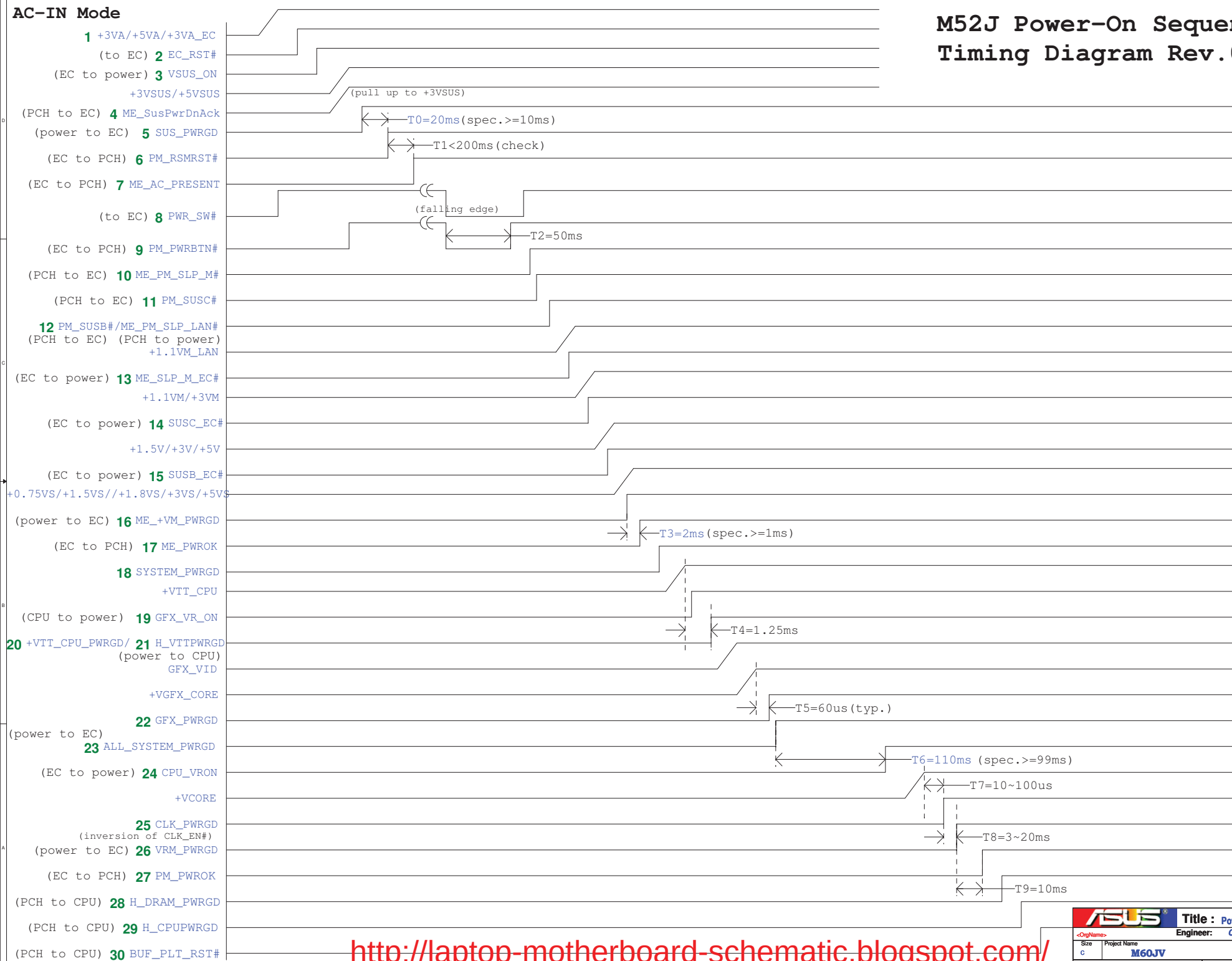
Power On Sequence

1



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M52J Power-On Sequence Timing Diagram Rev.0.31



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DC-IN Mode

M52J Power-On Sequence
Timing Diagram Rev.0.31

