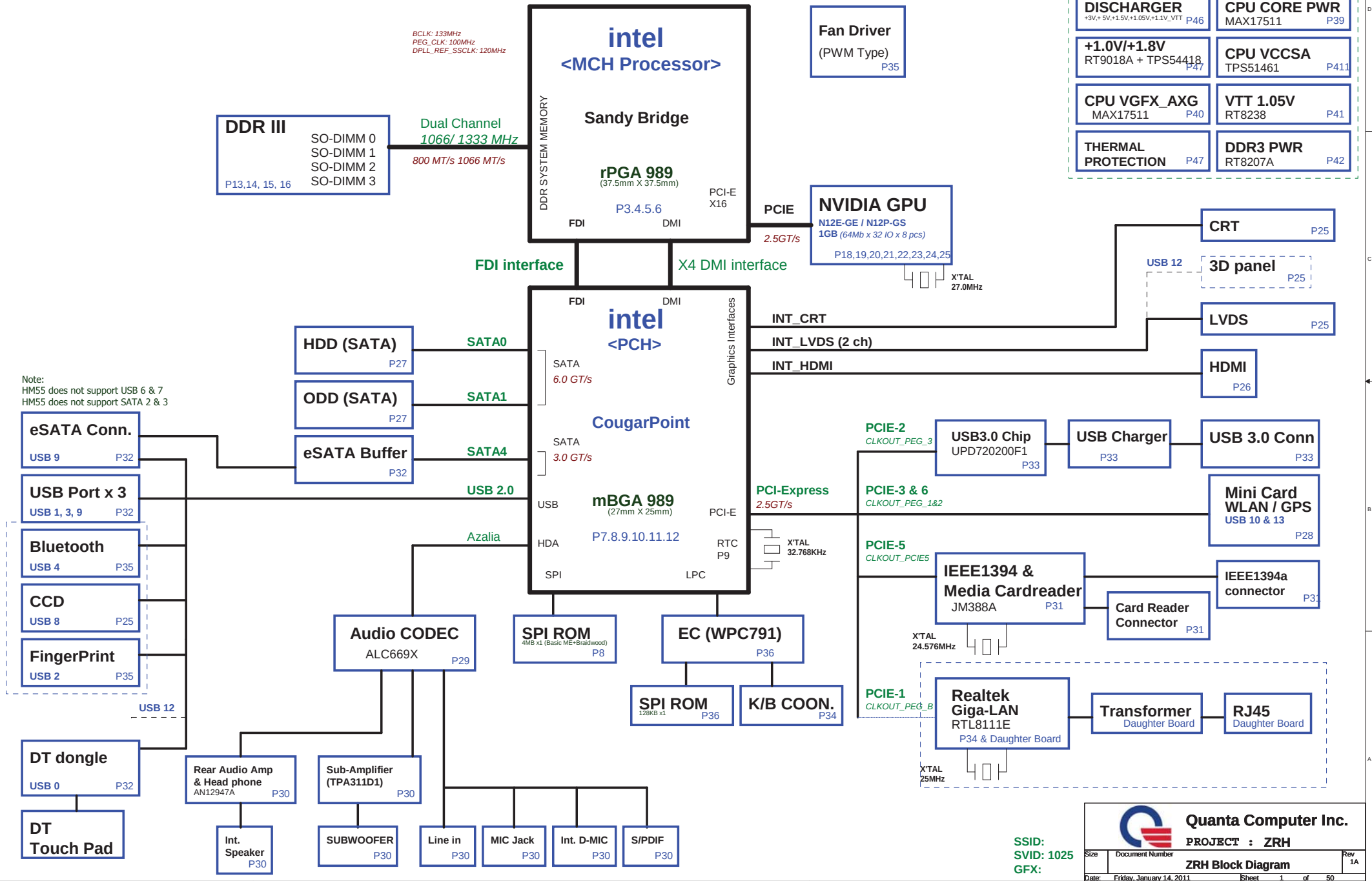
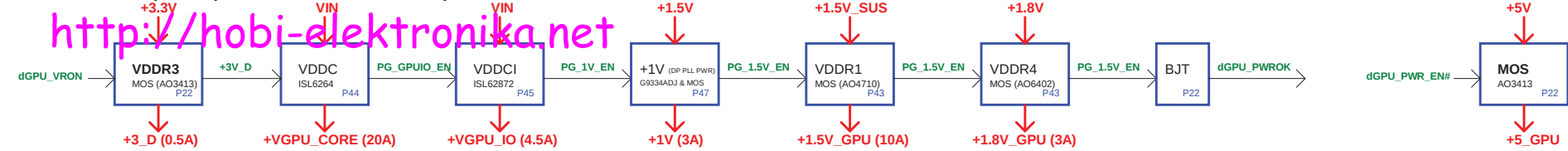


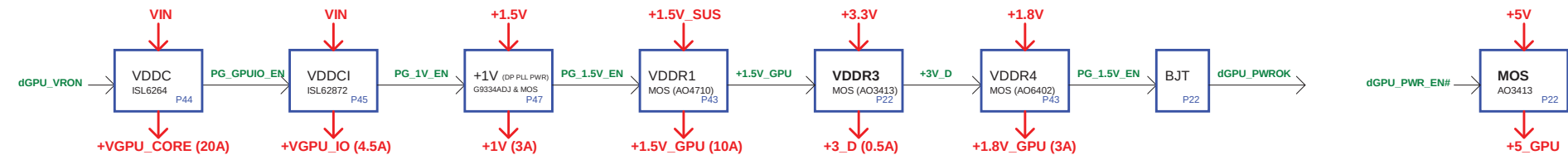
ZRH SYSTEM BLOCK DIAGRAM



GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



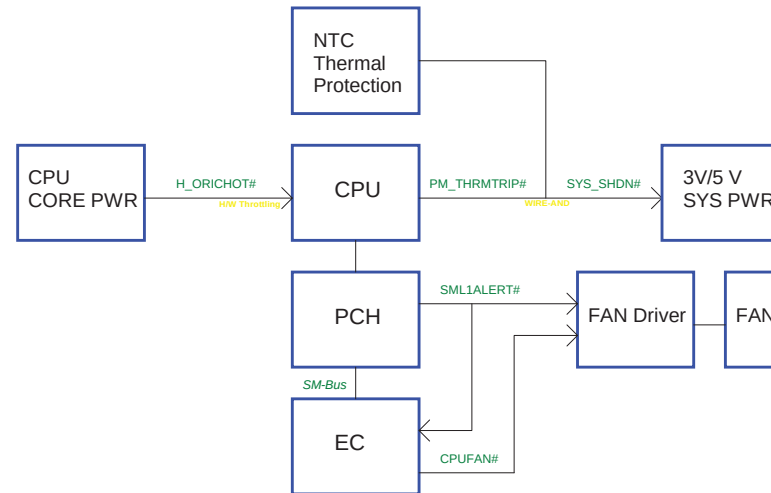
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



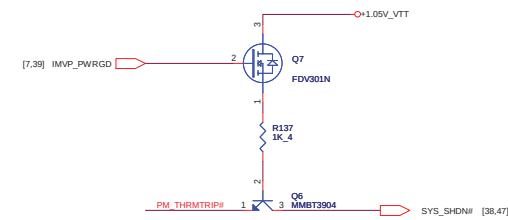
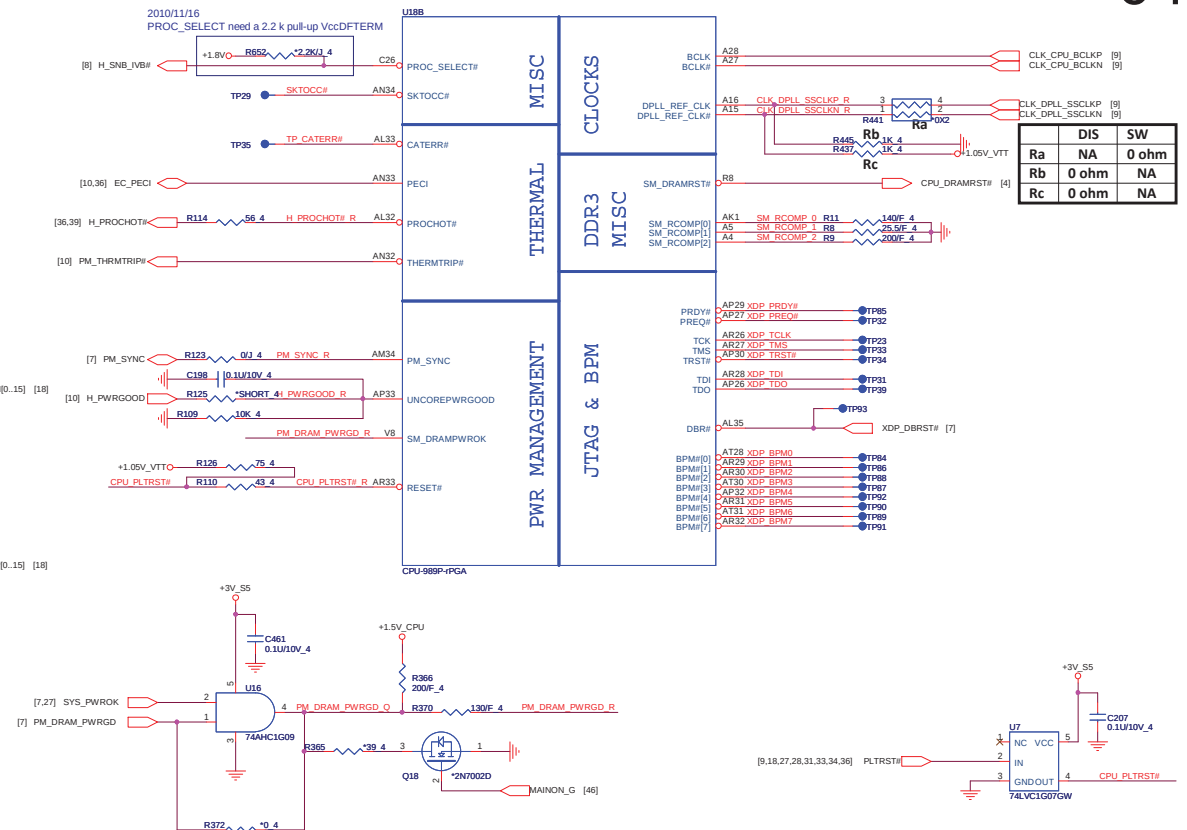
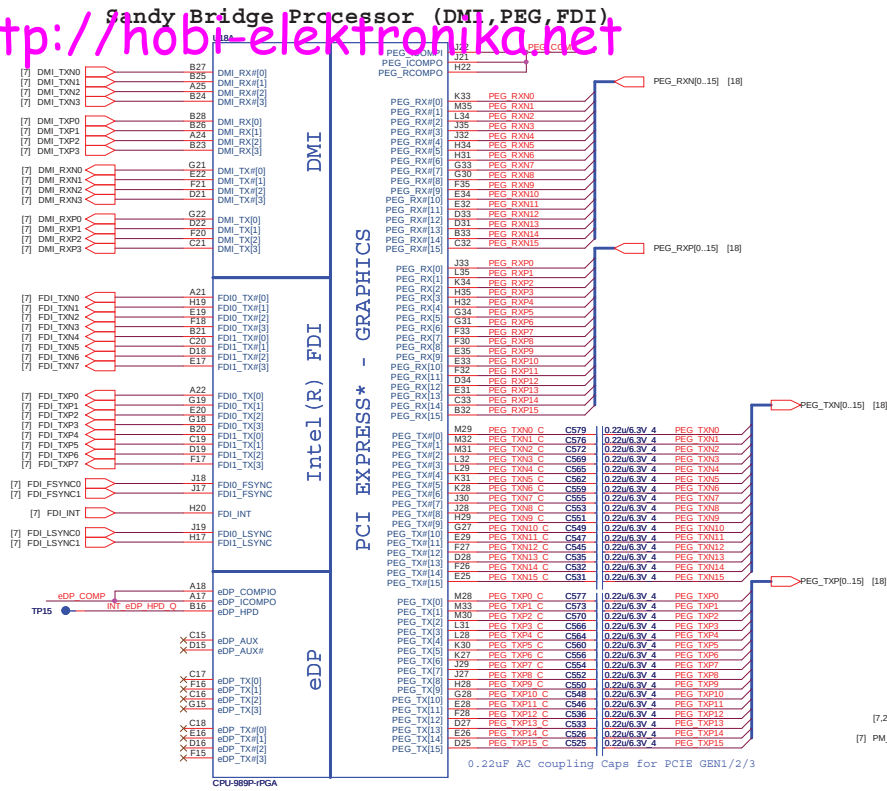
Power States

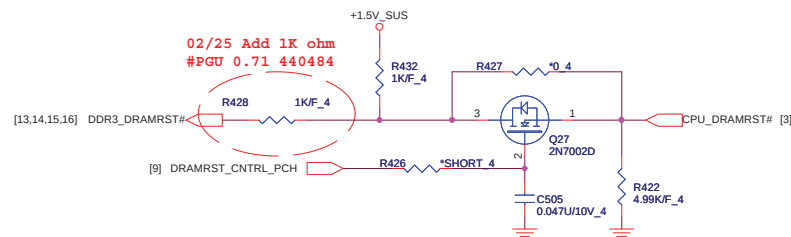
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



Sandy Bridge Processor (DMI,PEG,FDI)





Spec
330uF/6mohm x 2
22uF x 12
22uF x 7 (Non-stuff)

Real
390uF/10mohm x 1
22uF x 10
10uF x 1

Spec
470uF/4mohm x 2
22uF x 12

Real
330uF/10mohm x 1
22uF x 8
10uF x 6

POWER

GRAPHICS

1.8V RAIL

SVID CLK

SVID DATA

SVID ALERT

SENSE LINES

VREF

DDR3 - 1.5V RAILS

SA RAIL

MISC

VCCSA

VCCSA

VCCSA

VCCSA

VCCSA

VCCSA

VCCSA

VCCSA

VCCSA

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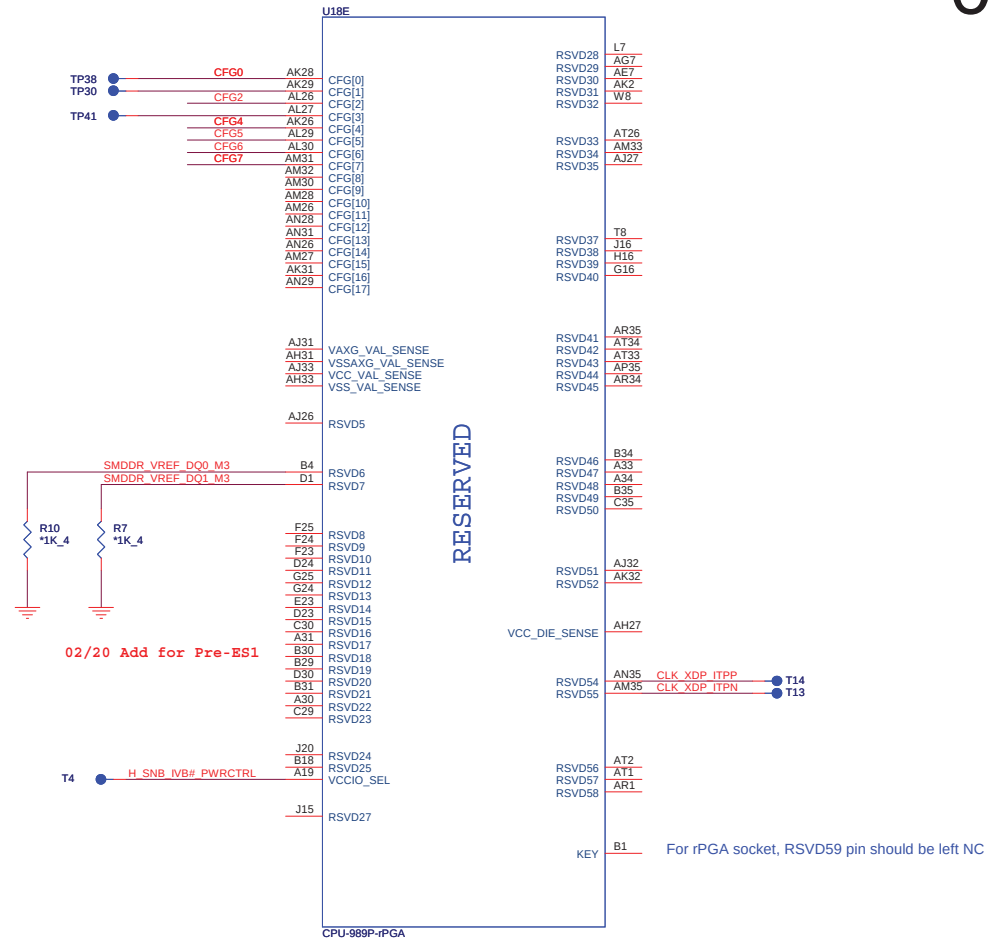
VCCSA

VCCSA

VCCSA

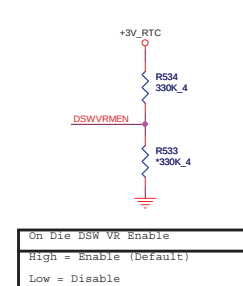
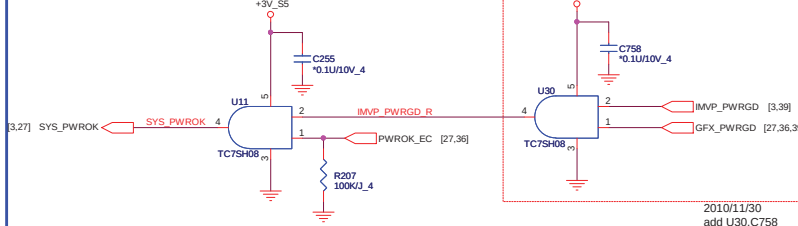
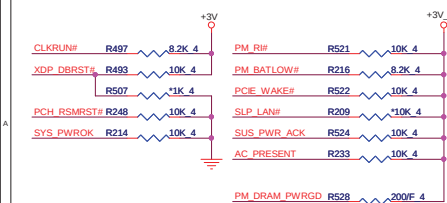
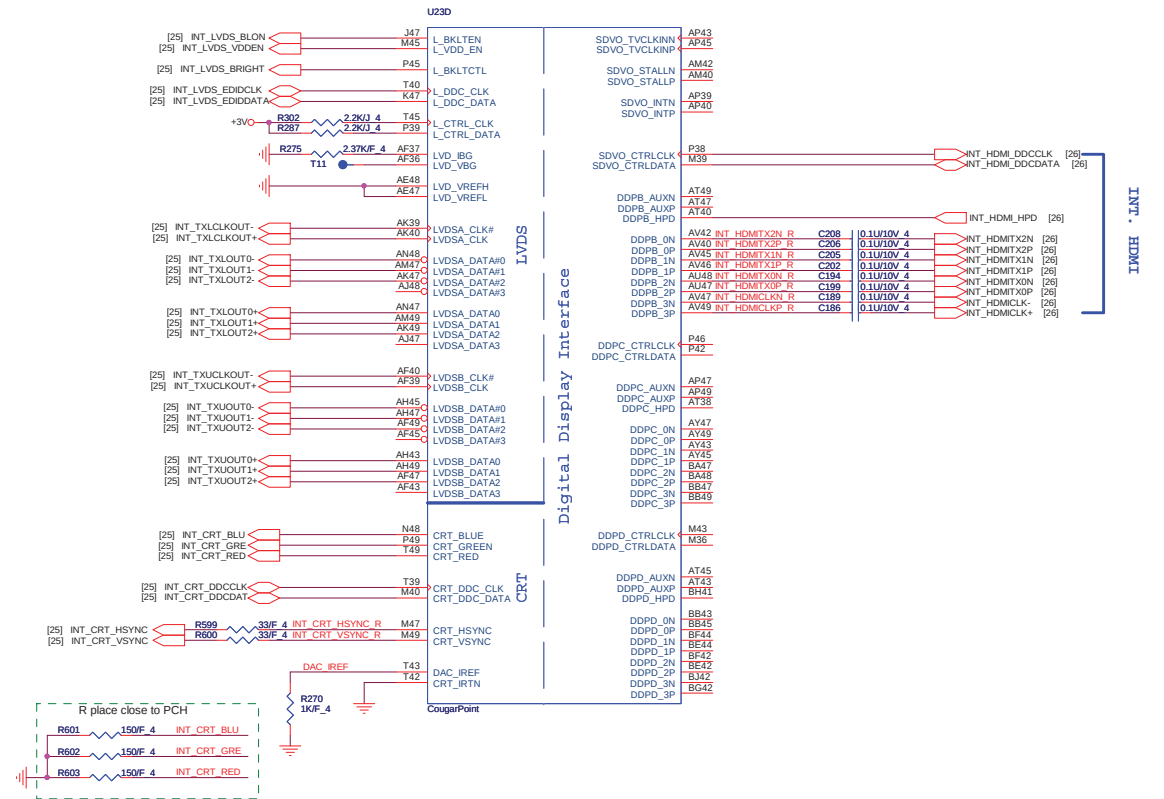
VCCSA

V

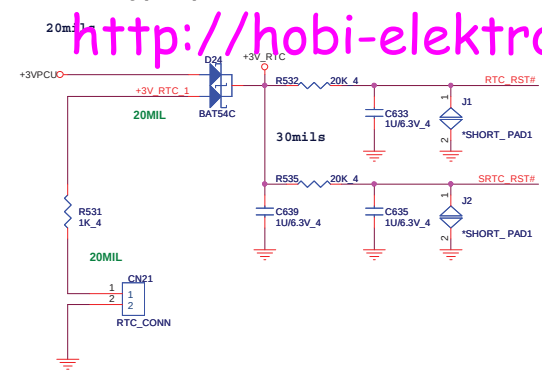


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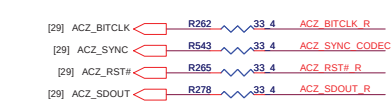
Cougar Point (DMI, FDI, PM)



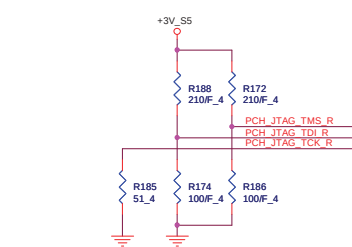
RTC Circuitry(RTC)



HDA Bus(CLG)

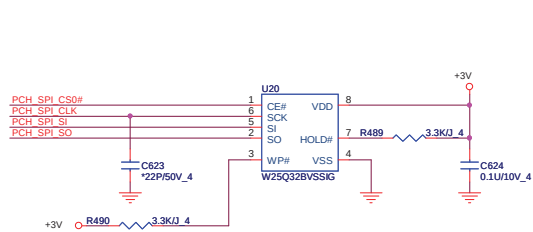


PCH JTAG Debug (CLG)

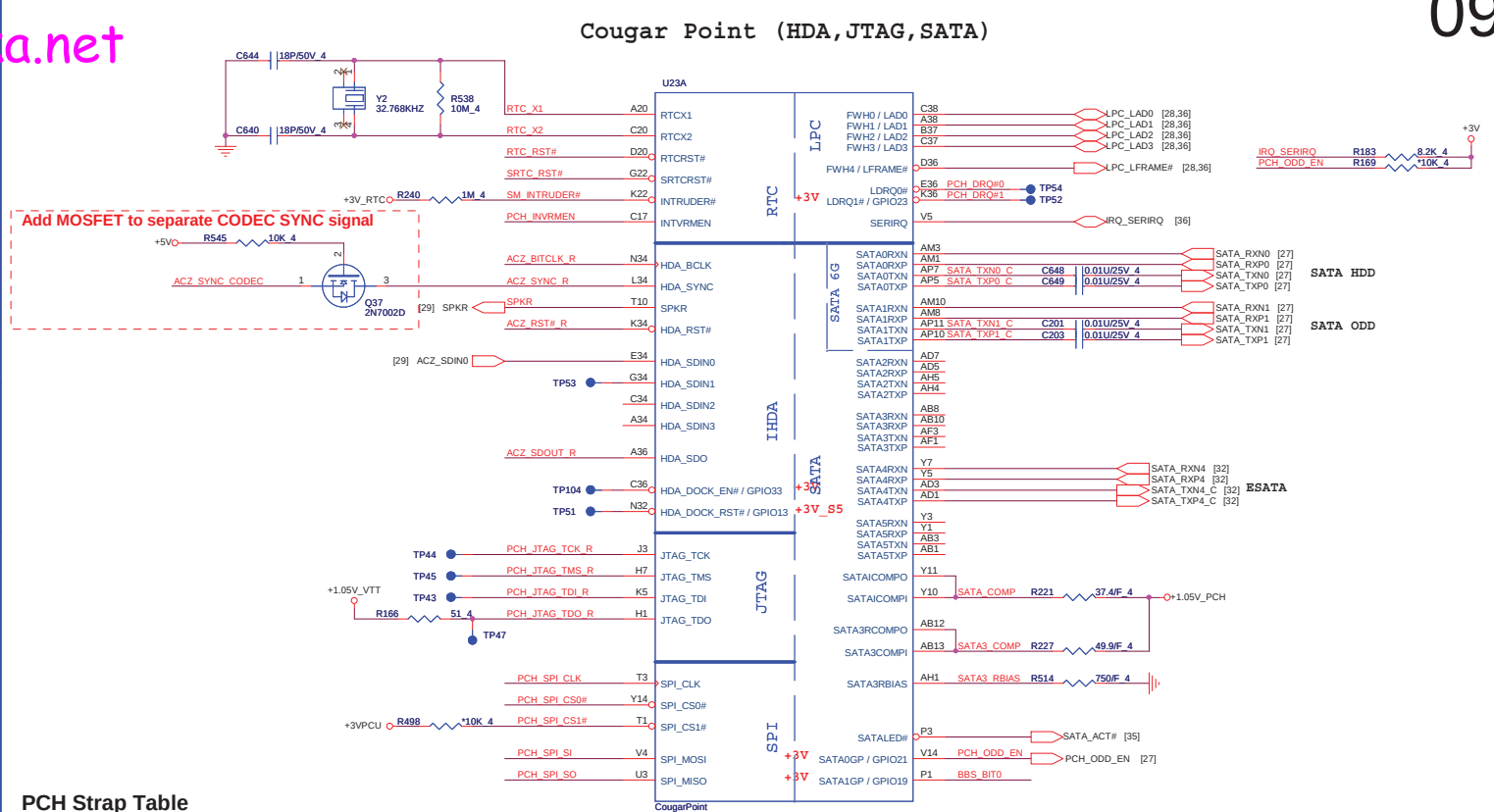


PCH Dual SPI (4M)

```
Winbond W25Q32BVSSIG AKE391P0N00
MXIC MX25L3205DM2I-12G: AKE39FP0Z00
```

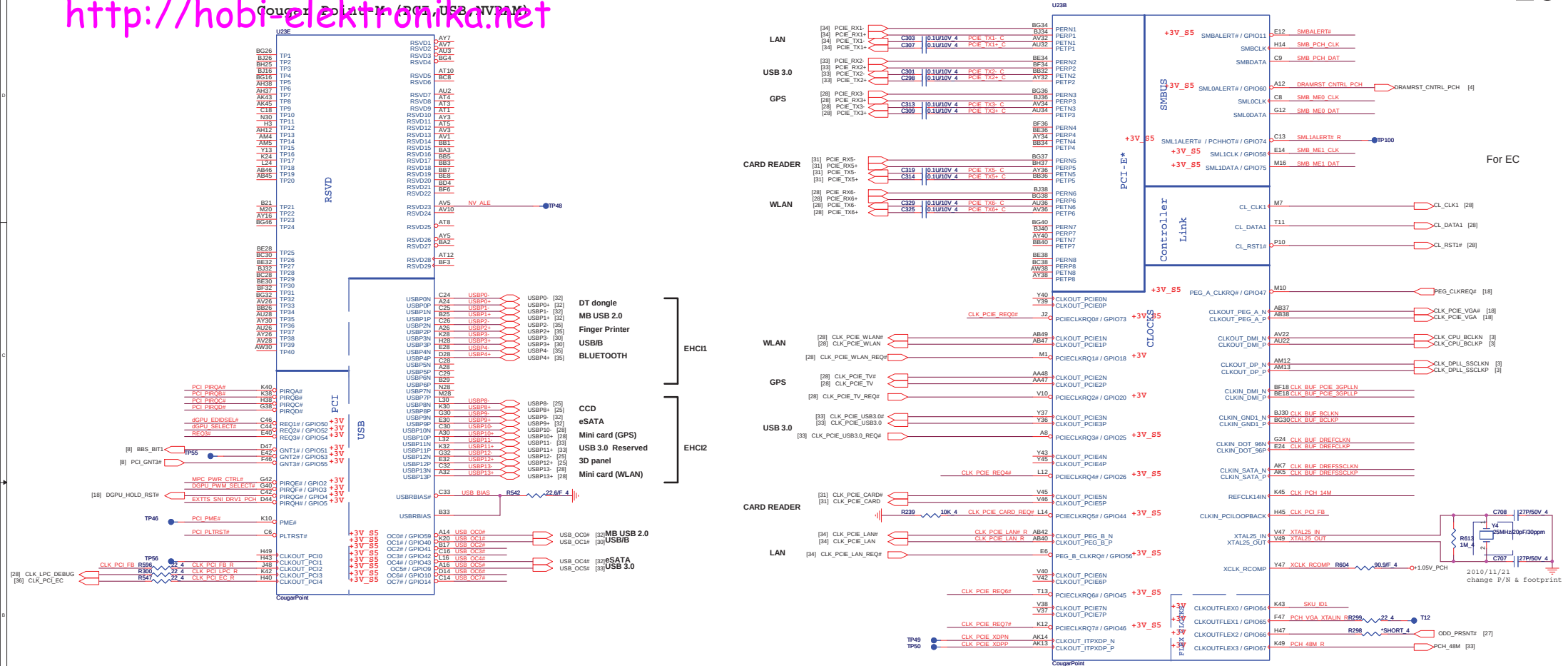


PCH2 (CLG)

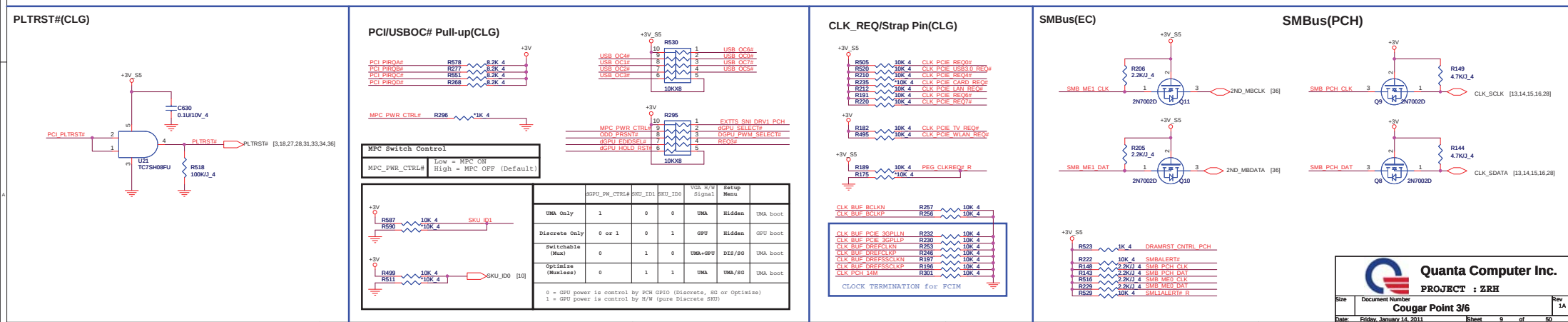


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration											
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode											
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)											
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up											
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]	
GNT1#	GNT0#	Boot Location												
1	1	SPI *												
0	0	LPC												
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK												
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)											
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)		New Add in CPT EDS Rev1.0 at 0316									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)											
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V		New Add in CPT EDS Rev1.0 at 0316									
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	Need check schematic	3/16 Remove based on CPT EDS rev1.0									
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable		3/16 Remove based on CPT EDS rev1.0									
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)		3/16 Remove based on CPT EDS rev1.0									

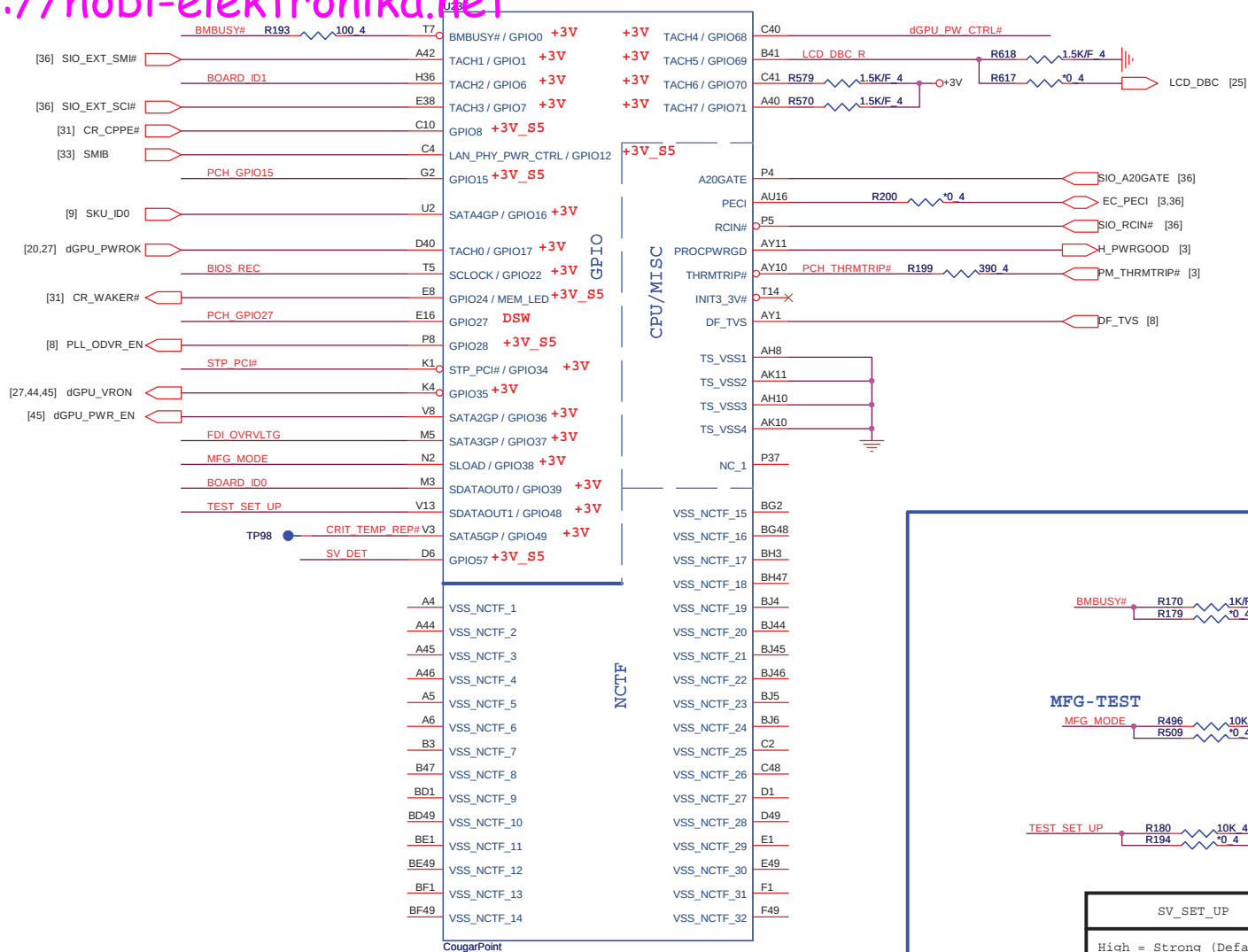


For EC

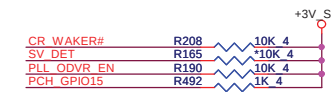


http://hobi-elektronika.net

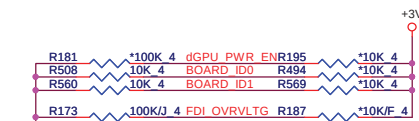
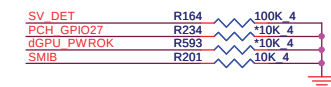
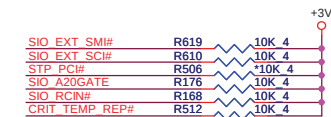
Cougar Point (GPIO,VSS NCTF,RSVD)



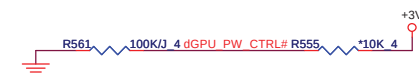
GPIO Pull-up/Pull-down(CLG)



```
GPIO15
Intel ME Crypto Transport Layer
Security (TLS) cipher suite
Low = Disable (Default)
High = Enable
```



```
FDI TERMINATIONVOLTAGE OVERRIDE
LOW - Tx, Rx terminated
to same voltage
```



high	GPU power is control by H/W (DIS only, UMA only)
low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)

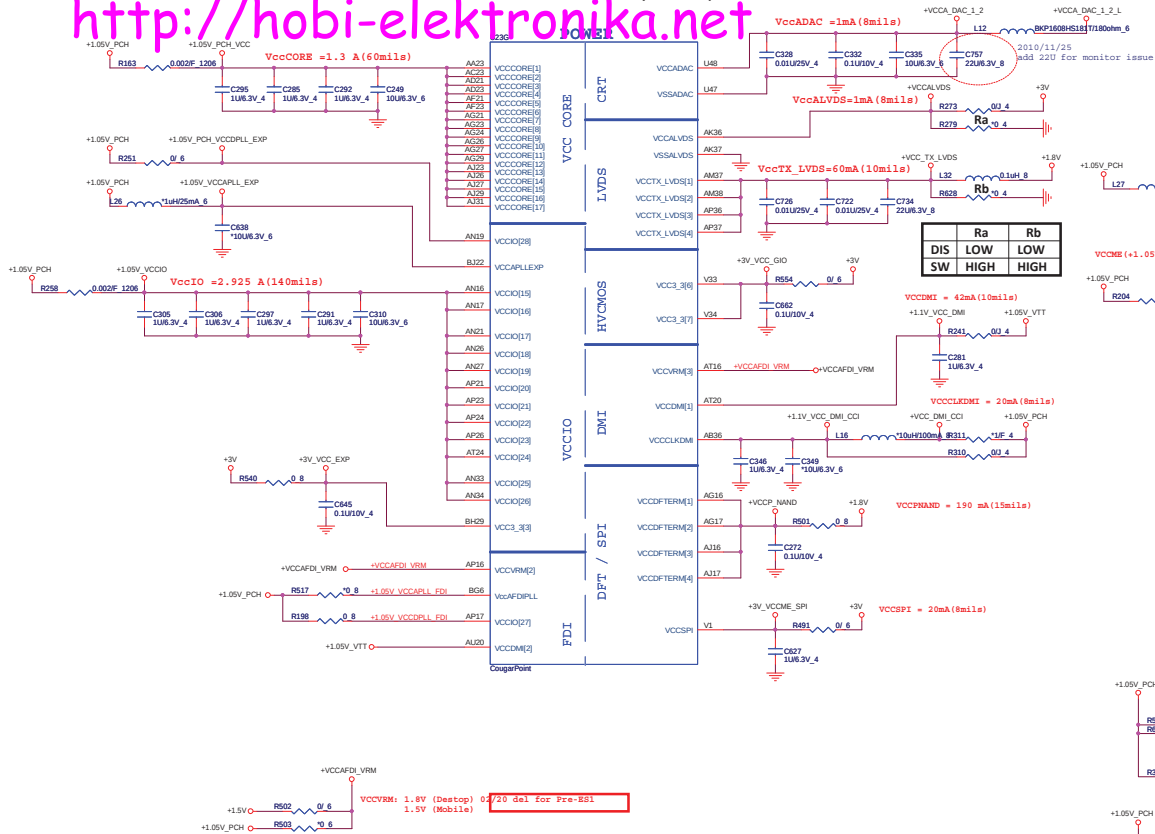


Quanta Computer Inc.

PROJECT : ZRH

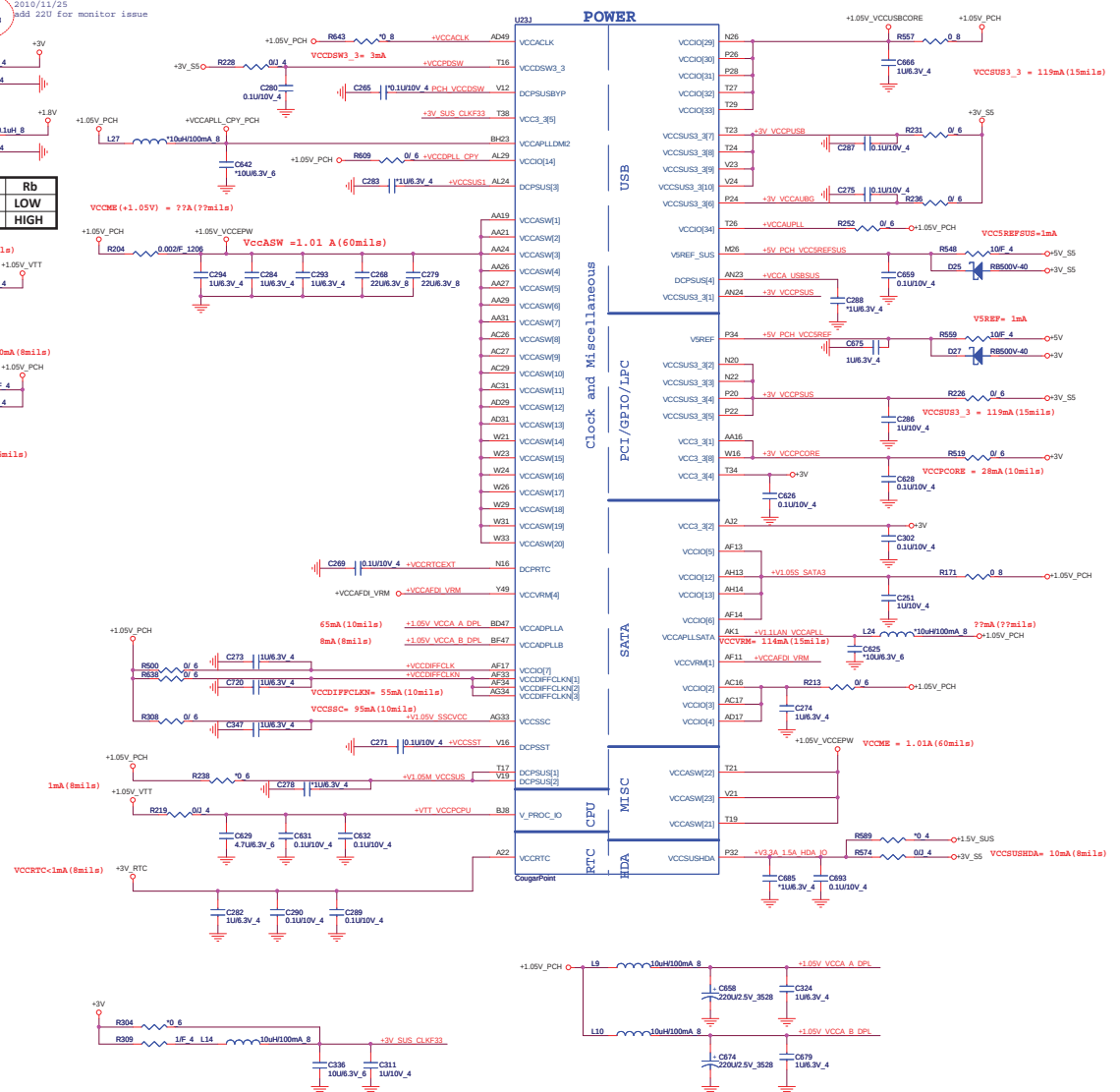
Size	Document Number	Rev
	Cougar Point 4/6	1A
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COUGAR POINT (POWER)

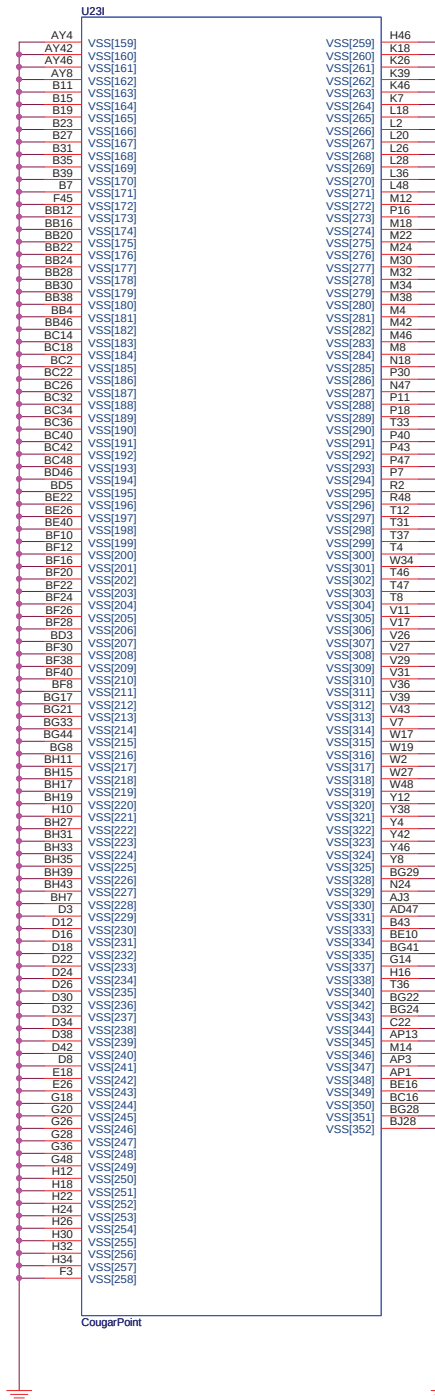
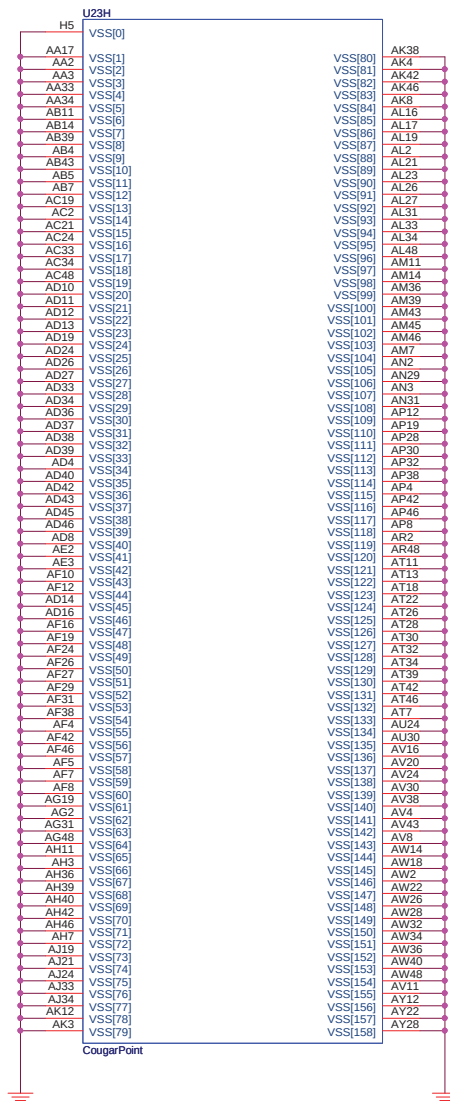
[illegible]

2011/1/11 add

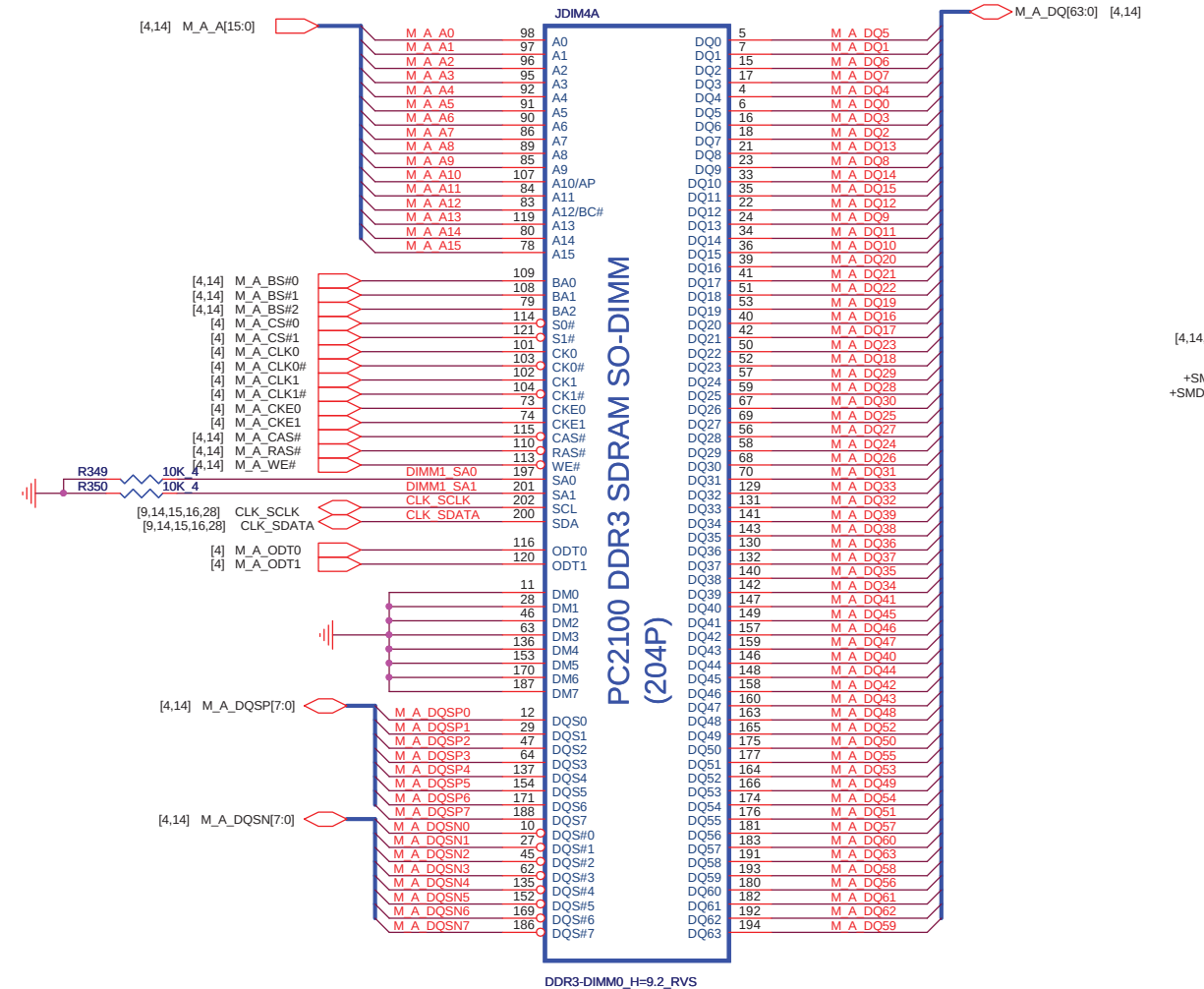
Cougar Point-M (POWER)



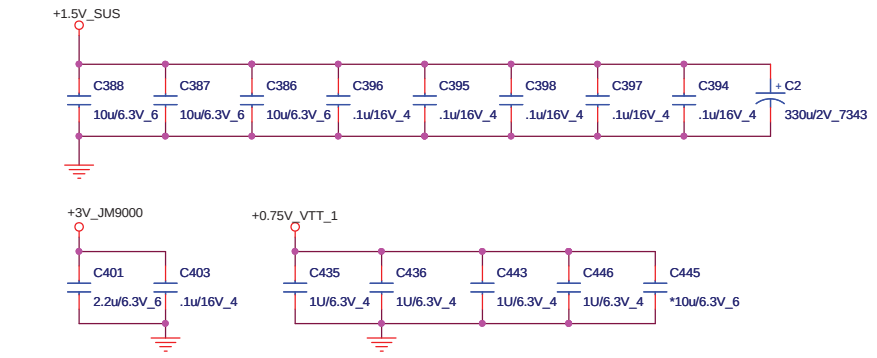
IBEX PEAK-M (GND)



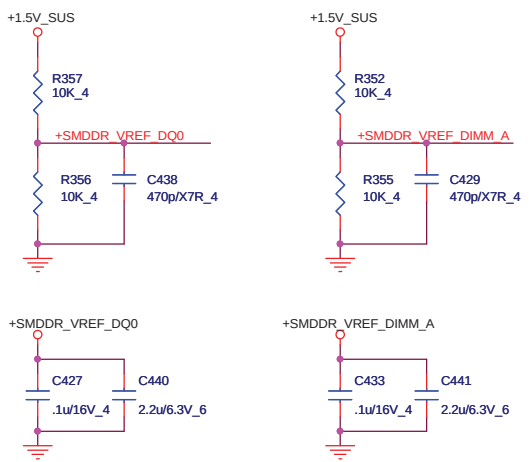
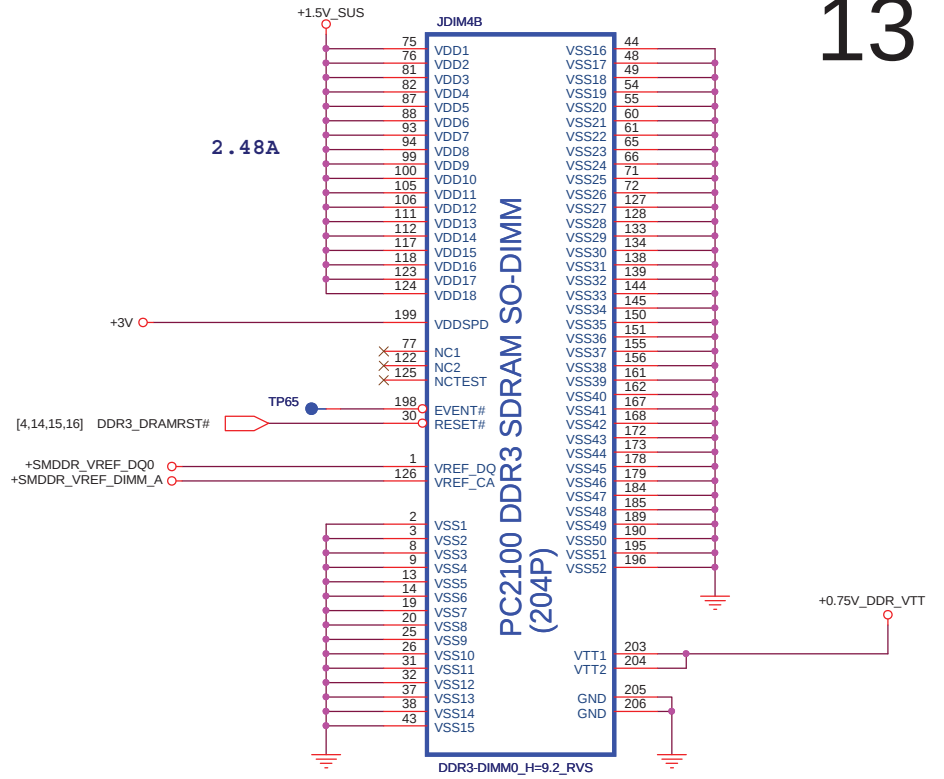
Quanta Computer Inc.
PROJECT : ZRH

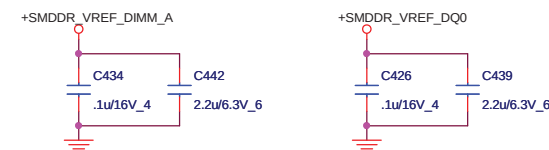
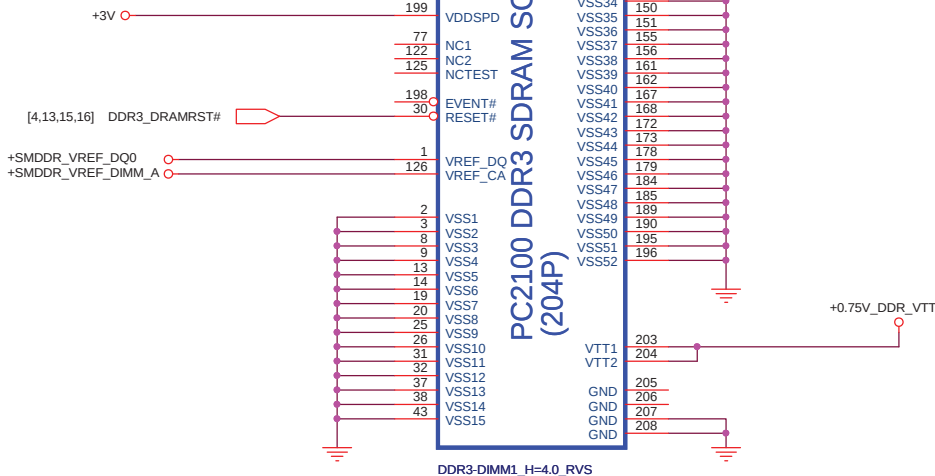


Place these Caps near So-Dimm0.



	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

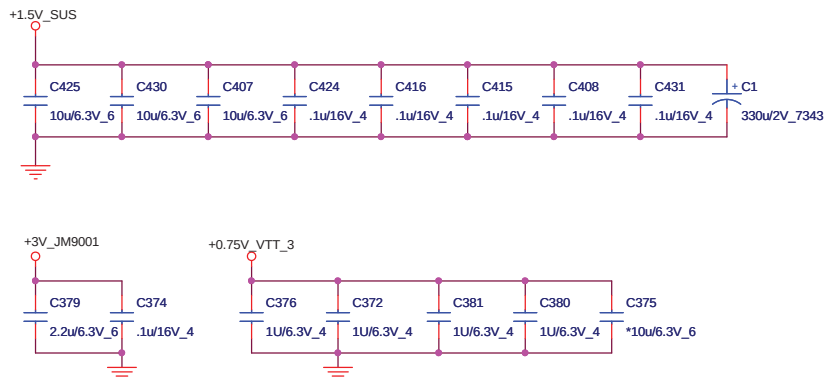
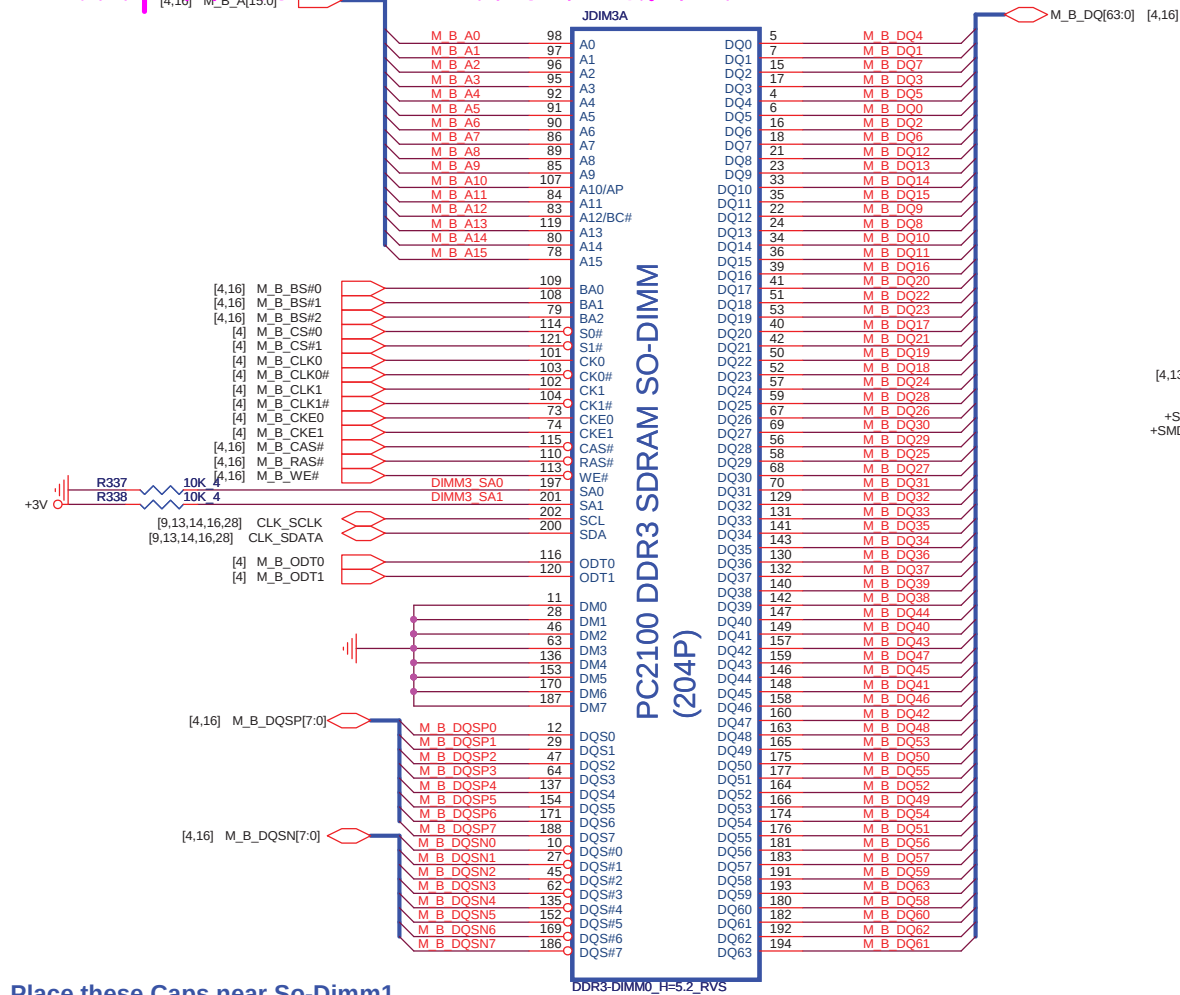




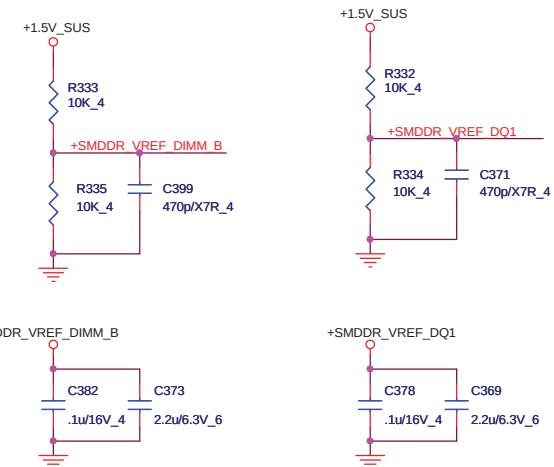
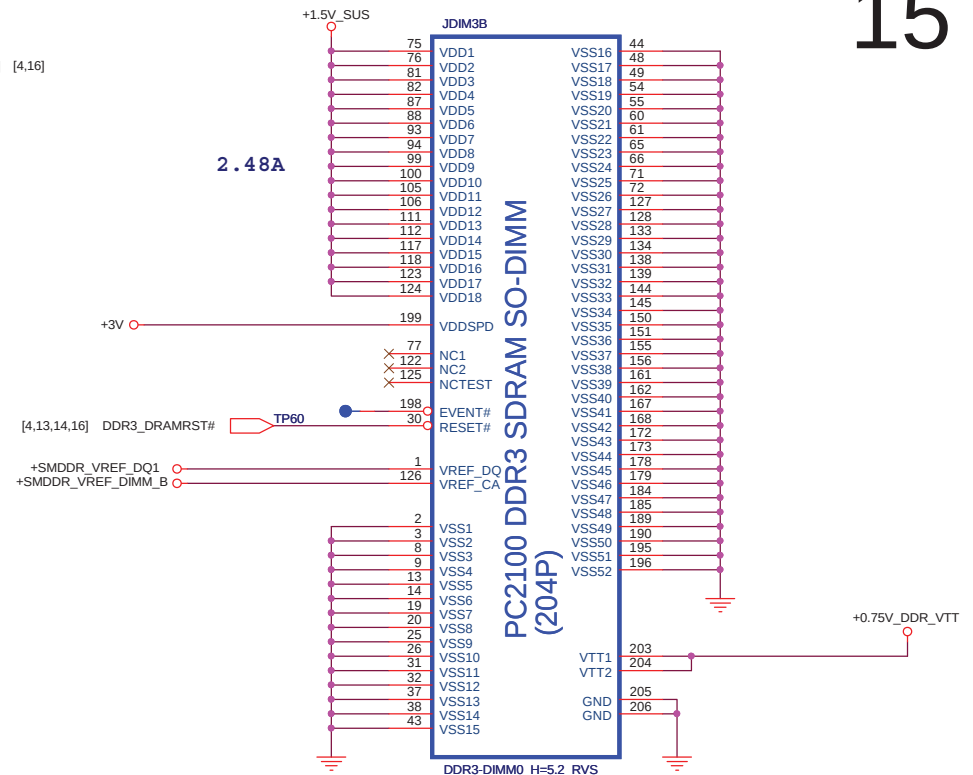
Three circuit diagrams illustrating decoupling capacitor networks for different power supplies:

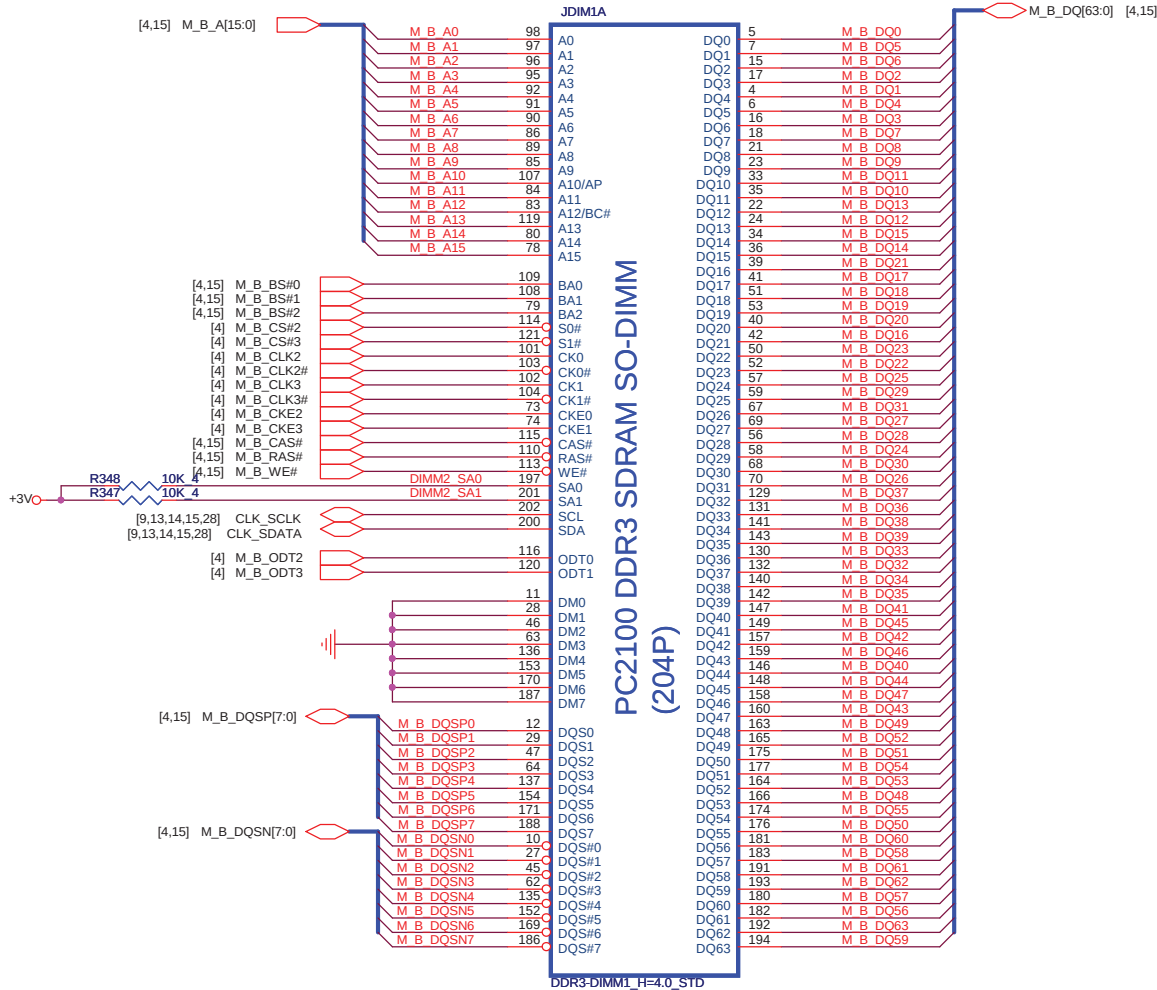
- Top Diagram:** A +1.5V_SUS supply is connected to a series chain of capacitors C383 through C444. The capacitors are connected in series between the supply and ground. The values are: C383 (10uF/6.3V_6), C384 (10uF/6.3V_6), C385 (10uF/6.3V_6), C390 (1uF/16V_4), C392 (1uF/16V_4), C391 (1uF/16V_4), C389 (.1uF/16V_4), C393 (.1uF/16V_4), and C444 (*330uF/2V_7343).
- Middle Diagram:** A +3V_3M8000 supply is connected to a parallel combination of capacitors C417 (2.2uF/6.3V_6) and C428 (.1uF/16V_4) to ground.
- Bottom Diagram:** A +0.75V_VTT_0 supply is connected to a series chain of capacitors C422 through C432. The capacitors are connected in series between the supply and ground. The values are: C422 (1uF/6.3V_4), C423 (1uF/6.3V_4), C413 (1uF/6.3V_4), C414 (1uF/6.3V_4), and C432 (*10uF/6.3V_6).

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

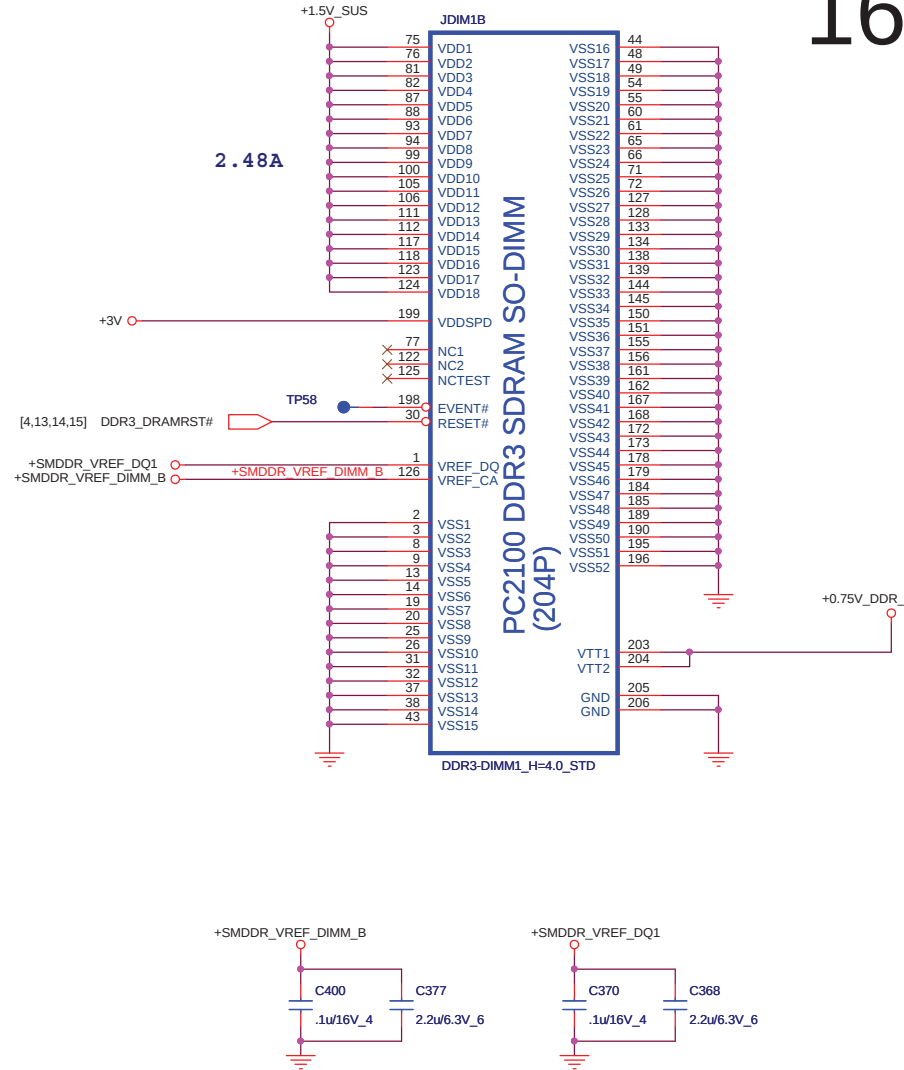
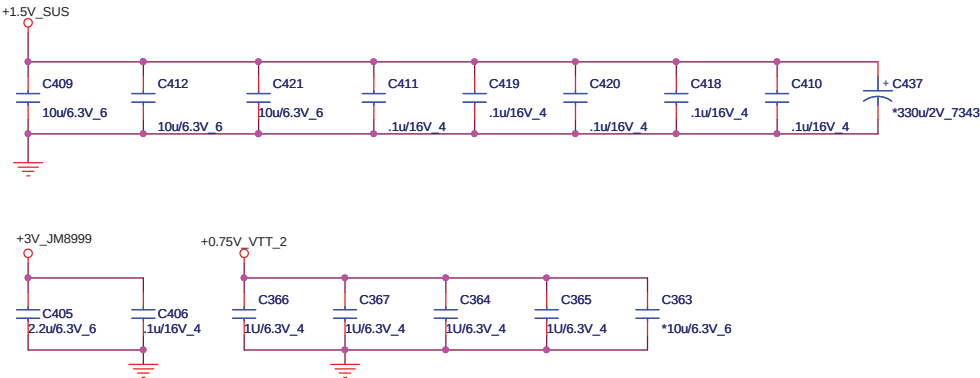


	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

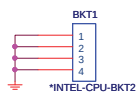
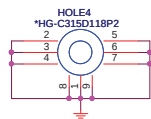
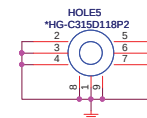
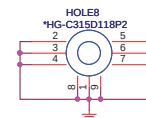
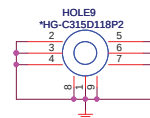
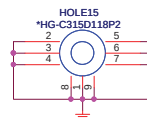
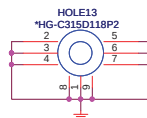
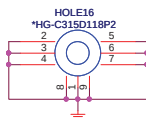
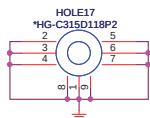
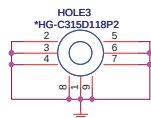




Place these Caps near So-Dimm1.



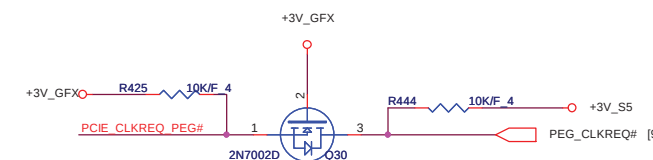
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

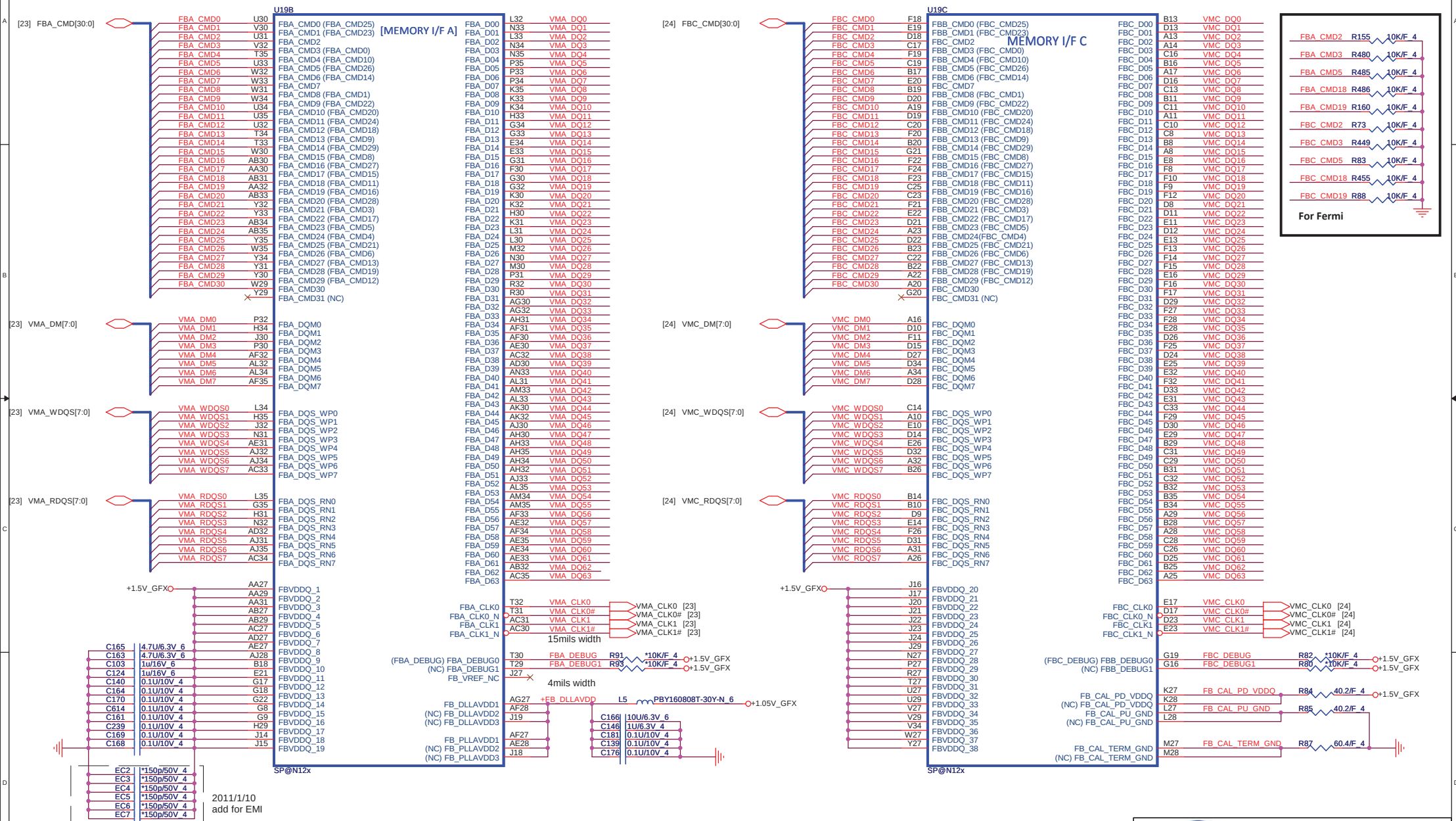


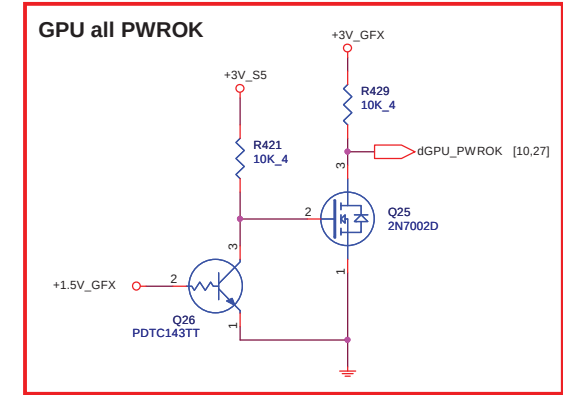
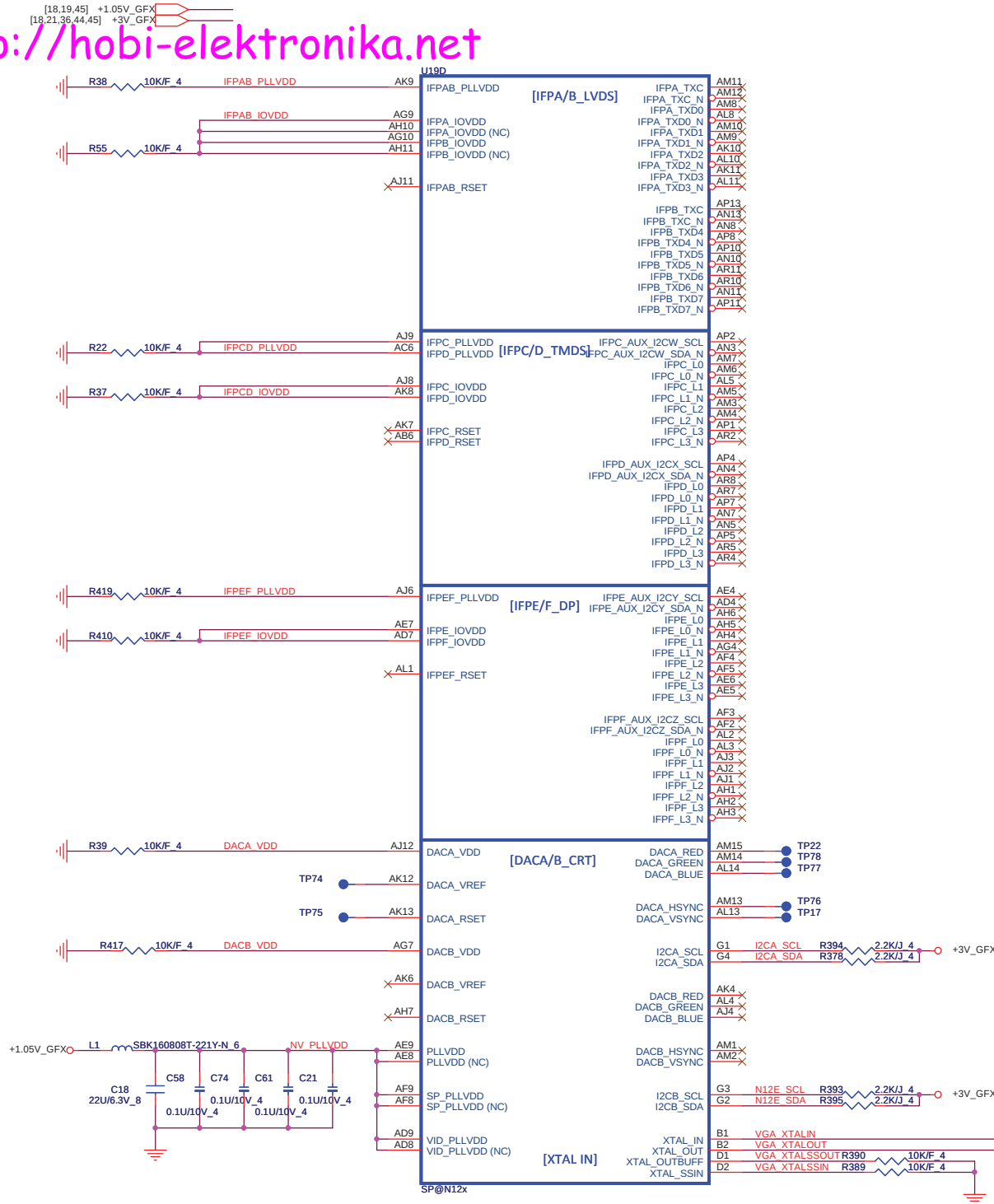
The diagram shows four digital signals over time. The signals are labeled on the left: I/O 3.3V, PXE 1.05VDD, NVCORE, and 1.5VFBDDQ. Each signal is represented by a horizontal line that transitions from low to high at a specific point in time. The transitions occur in sequence from top to bottom: I/O 3.3V transitions first, followed by PXE 1.05VDD, then NVCORE, and finally 1.5VFBDDQ.

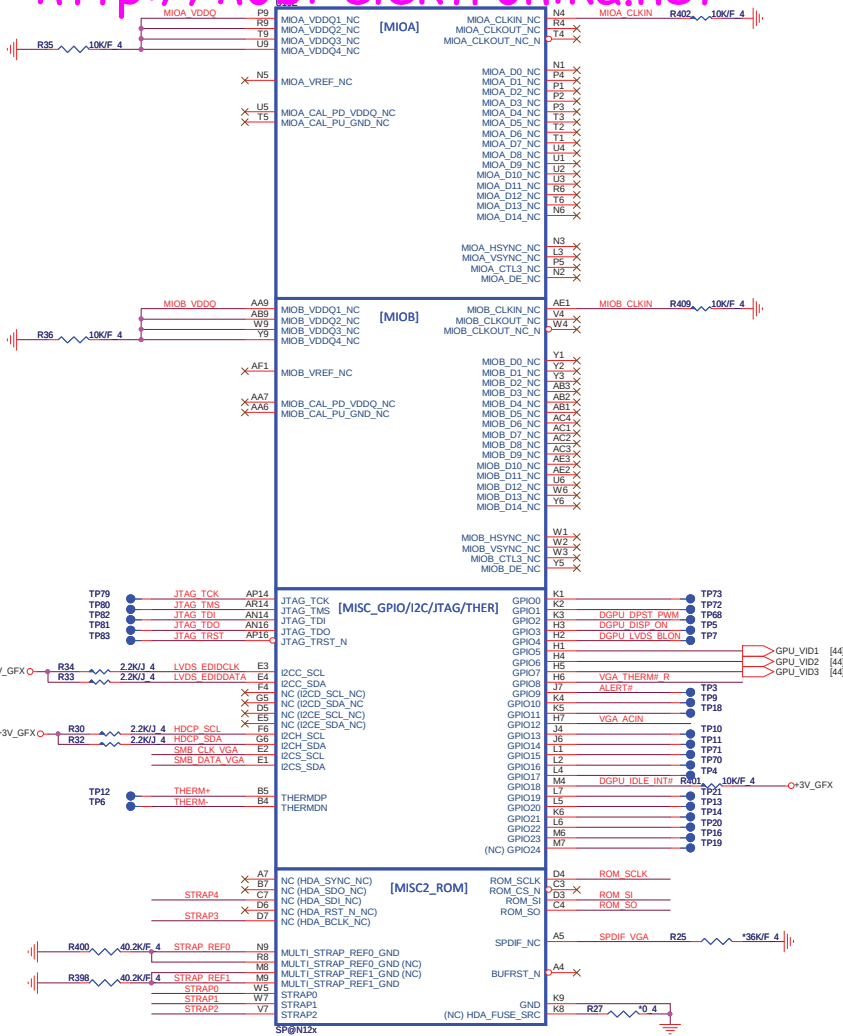
Timing diagram showing the relationship between NVDD and GPIO signals. The diagram illustrates the time interval $t_{sNVDD} \leq 192\mu s$ between the falling edge of the GPIO signal and the rising edge of the NVDD signal.

Timing diagram showing the relationship between I/O 3.3V and PEX_RST signals. The I/O 3.3V signal transitions from low to high and then back to low. The PEX_RST signal transitions from high to low and then back to high. The rising edge of I/O 3.3V is labeled $T_{rise} \geq 1\mu S$. The falling edge of PEX_RST is labeled $T_{fail} \leq 500nS$.

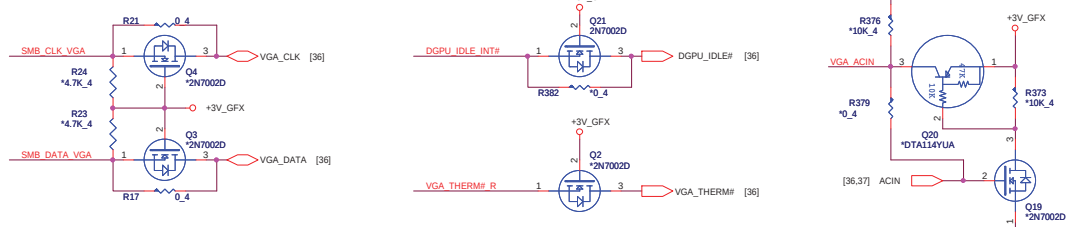






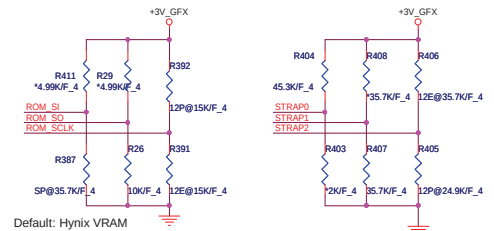


VGA Thermal



	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	N12P-GS	N12E-GE
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0XXX	0XXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0100	1110
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110	0110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111	1111

ROM_SI	DESCRIPTION	Vendor PIN	ROM_SI	Quanta P/N B/S
0010	Hynix DDR3 64Mx16x8, 1GB,900MHz	H5TQ1G63DFR-11C	PD 15K	AKD5LZWTW05
0011	Samsung DDR3 64Mx16x8, 1GB,900MHz	K4W1G1646E-HC11	PD 20K	
0110	Hynix DDR3 128Mx16x8, 2GB,900MHz	H5TQ2G63BFR-11C	PD 35K	
0111	Samsung DDR3 128Mx16x8, 2GB,900MHz	K4W2G1646C-HC11	PD 45K	



Logical Strap Bit Mapping

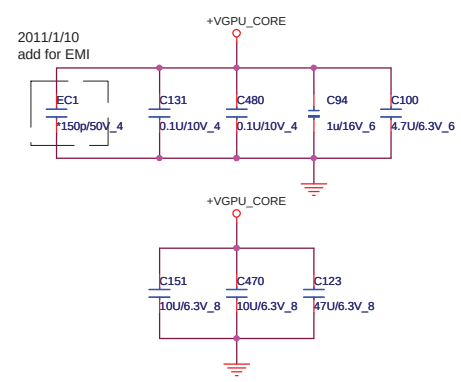
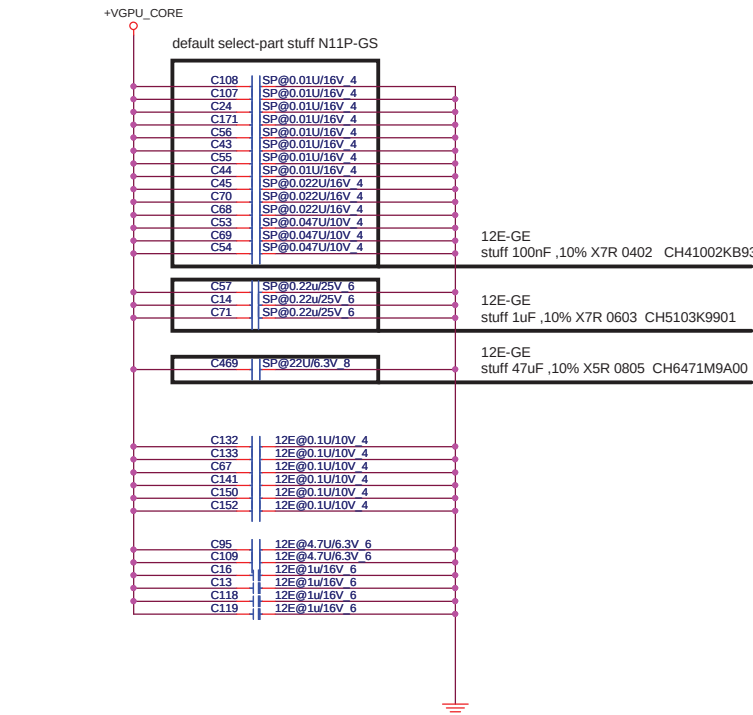
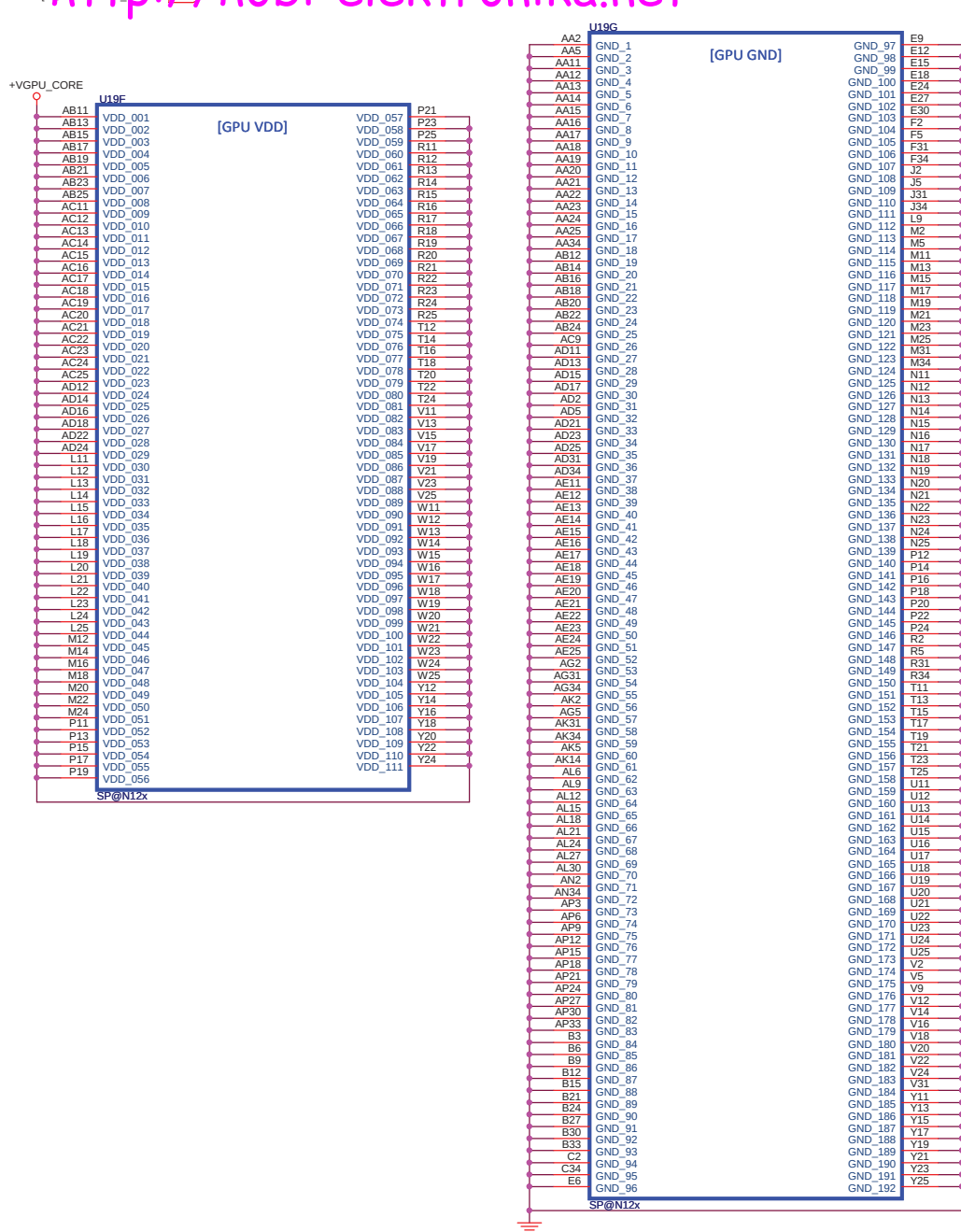
	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

CHIP	N12P-GS	N12E-GE
ROM_SCLK	PU 15K	PD 15K
STRAP2	PD 25K	PU 35K

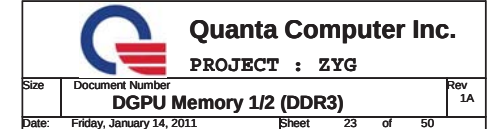
4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1%(0402)]
15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1%(0402)]
30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1%(0402)]
35.7K/F 4: CS3352FB13 [RES CHIP 35.7K 1/16W +1%(0402)]
45.3K/F 4: CS3452FB18 [RES CHIP 45.3K 1/16W +1%(0402)]
20K/F 4: CS32002FB28 RES CHIP 20K 1/16W +1%(0402)]

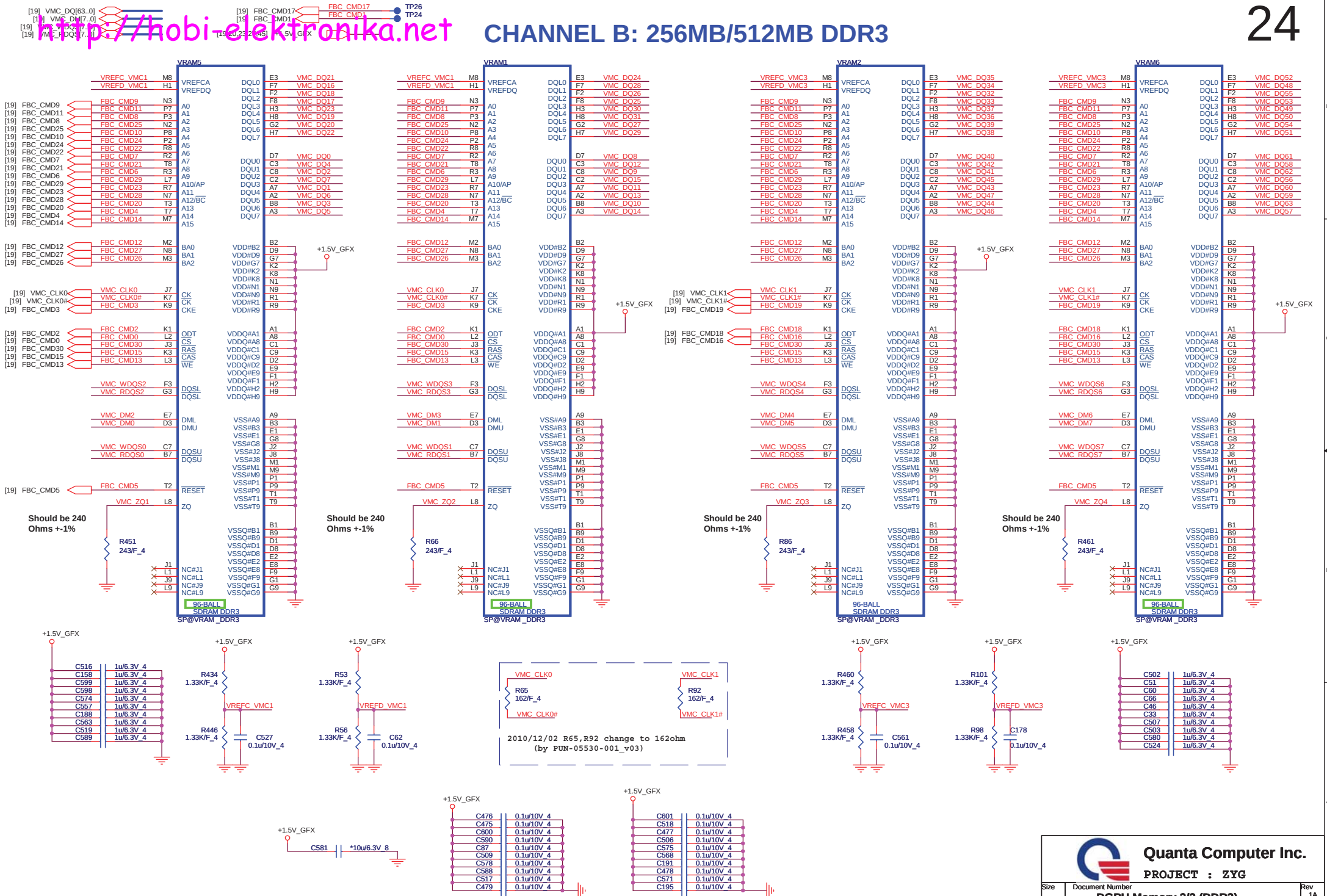
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID1
6	OUT	N/A	NVDD VID2
7	OUT	N/A	NVDD VID3
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL



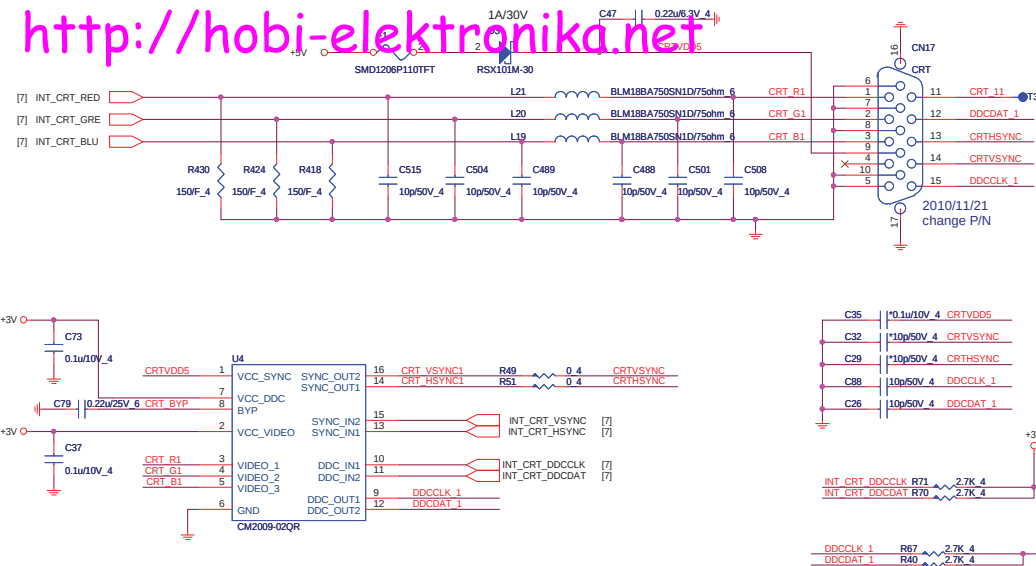
SPEC	GB2-128 12P-GS	GB3-128 12E-GE
10nF, 10% X7R 0402	8	
22nF, 10% X7R 0402	3	
47nF, 10% X7R 0402	3	
100nF, 10% X7R 0402	2	22
220nF, 10% X7R 0603	3	
1uF, 10% X7R 0603	1	8
4.7uF, 10% X5R 0603	1	3
10uF, 10% X5R 0805	2	2
22uF, 10% X5R 0805	1	
47uF, 10% X5R 0805	1	2
470uF	1	



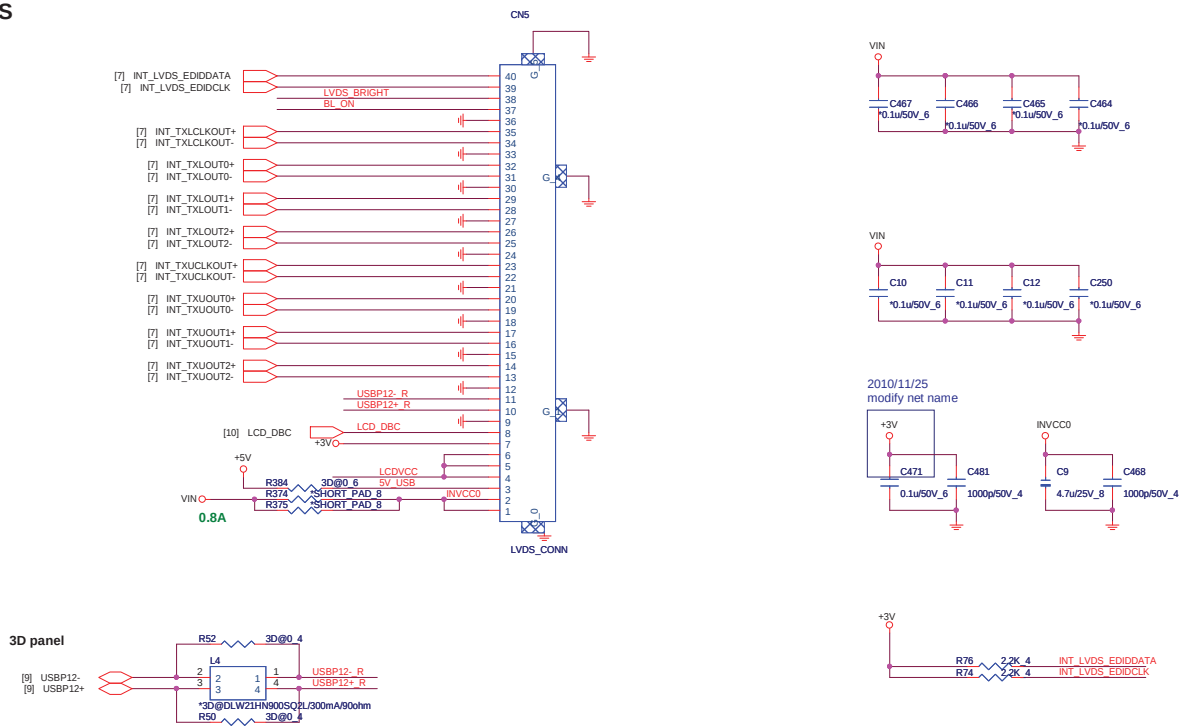


CRT

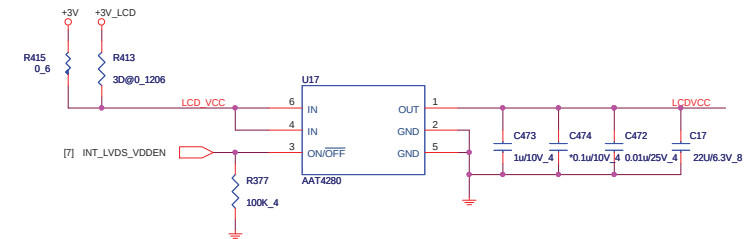
<http://hobi-elektronika.net>



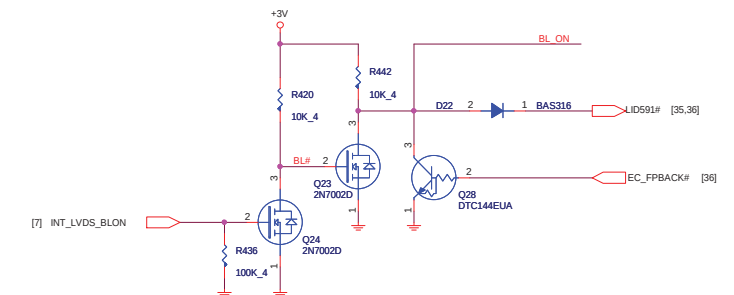
LVDS



LCD Power



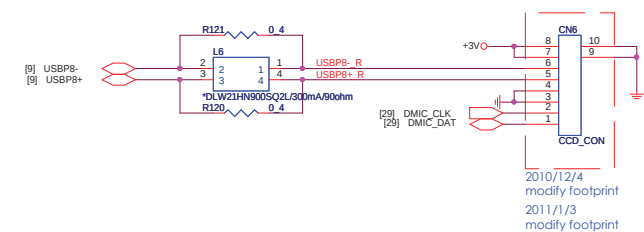
Backlight Control



Brightness Control

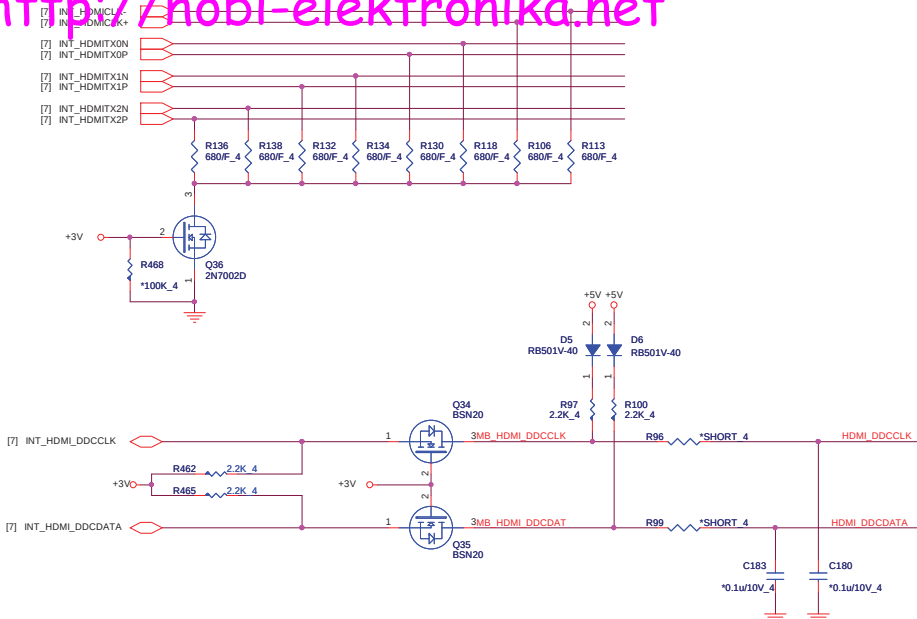


CCD & MIC

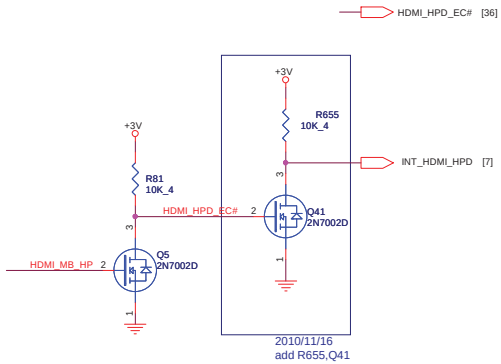


HDMI

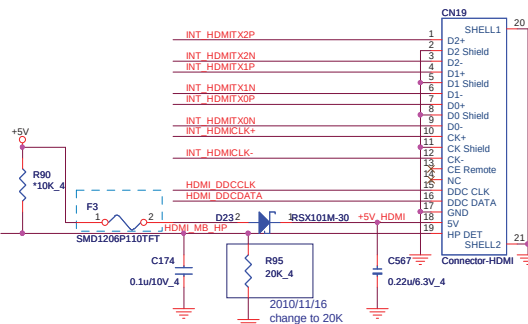
<http://hobi-elektronika.net>



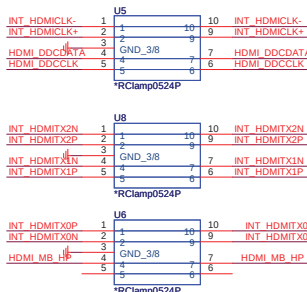
HDMI -detect



HDMI connector



ESD Protect



SATA HDD
<http://hobi-elektronika.net>

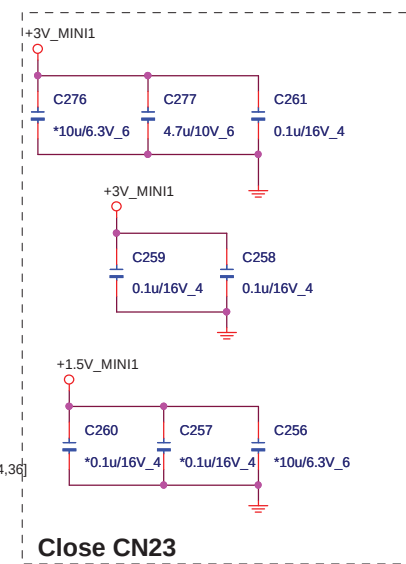
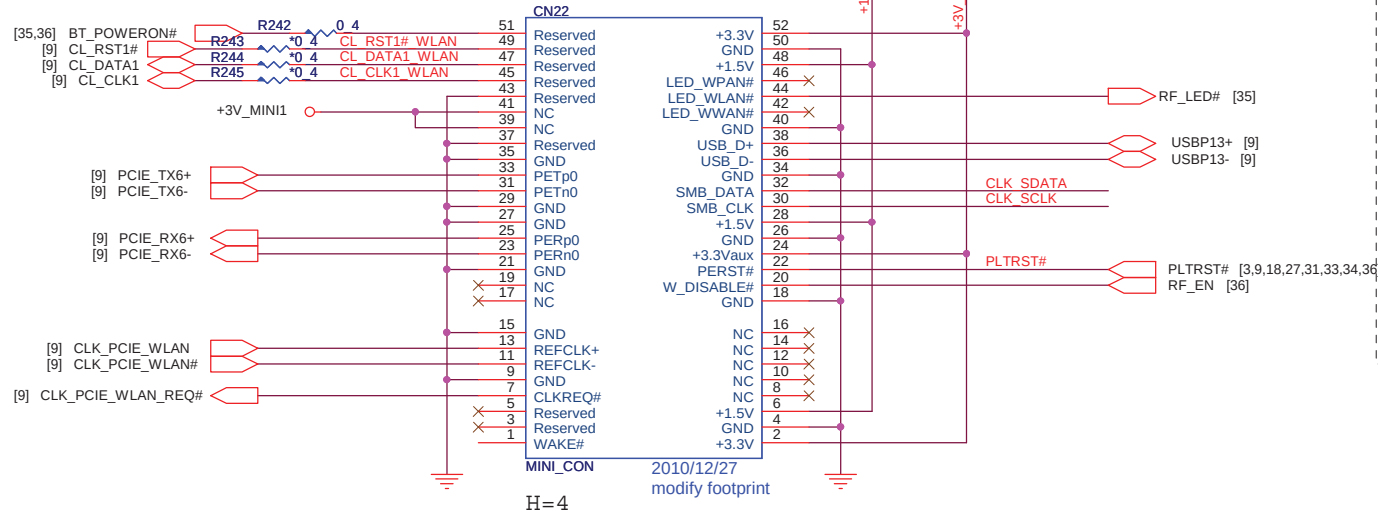


PROJECT : ZRH

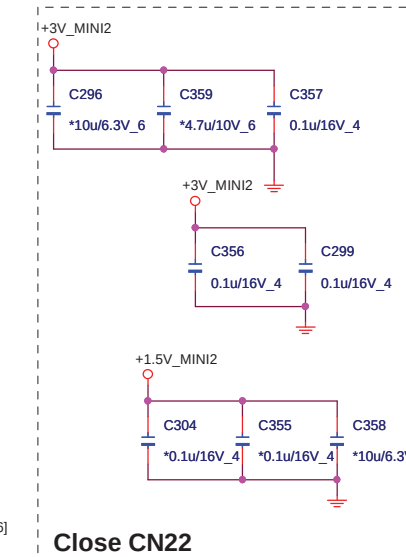
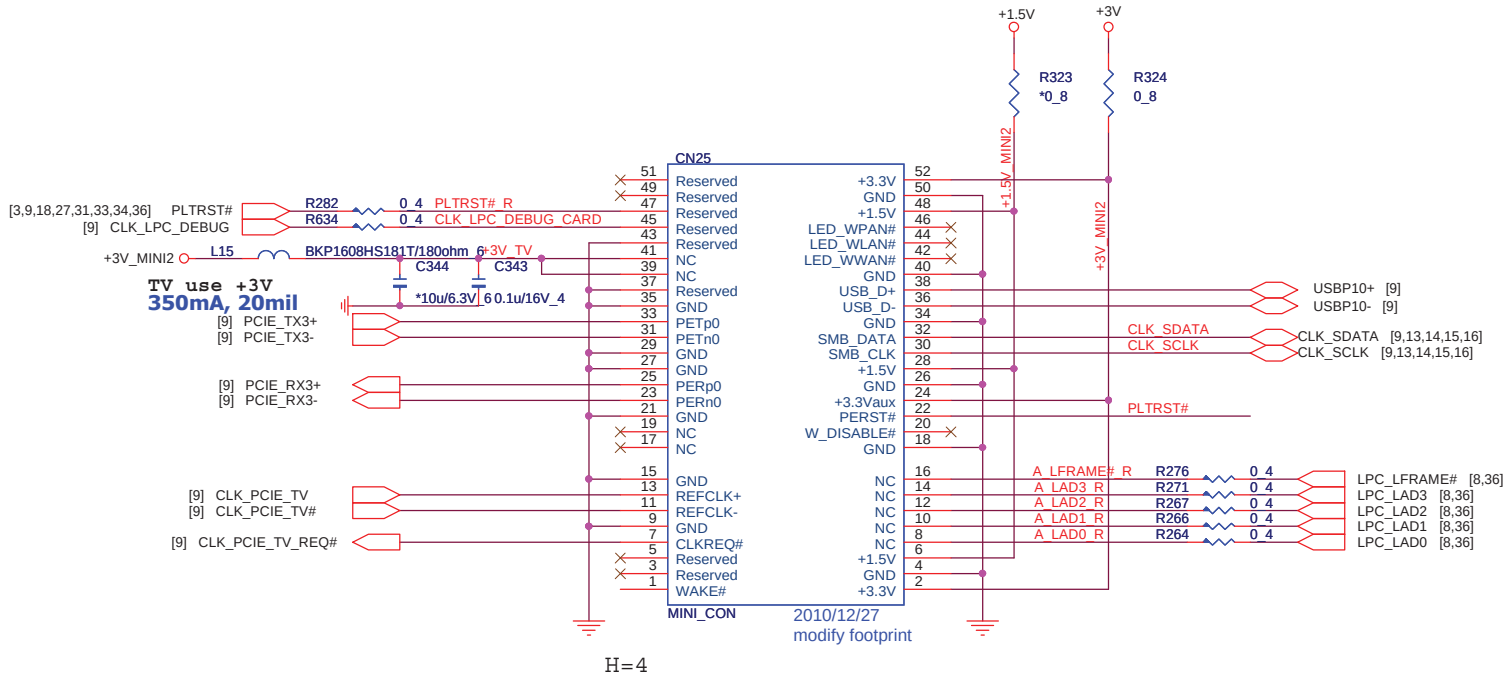
Rev
1A

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+3.3V: 2700mA
+1.5V: 500mA



TV and Debug

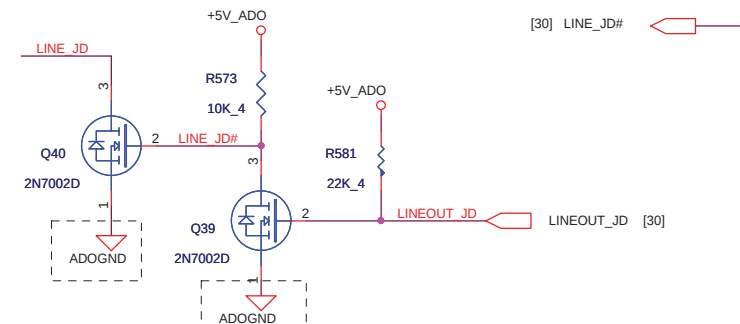
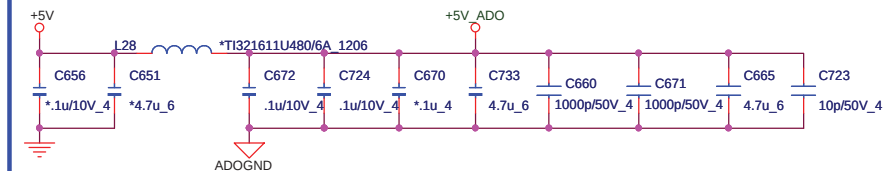


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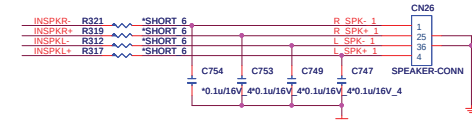
PROJECT : ZRH

MINI PCI-E card/TV

CODEC(ALC669X) <http://hobi-elektronika.net>



<http://hobi-elektronika.net>

[illegible]

SHUTDOWN	TPA3110D1
L (0V~0.8V)	SHUTDOWN
H (2V ~ VDD)	ACTIVE

Diagram illustrating the USB and audio connections for the DLW21HN6005Q2L/300mA/90ohm module.

USB Connections:

- USBP3- (Pin 3) connects to USBP3- R (Pin 5) and USBP3+ R (Pin 4).
- USBP3+ (Pin 4) connects to USBP3- R (Pin 5) and USBP3+ R (Pin 4).
- USBP3-L (Pin 5) connects to USBP3- R (Pin 5) and USBP3+ R (Pin 4).
- USBP3- (Pin 6) connects to USBP3- R (Pin 5) and USBP3+ R (Pin 4).

Audio Connections:

- HPL (Pin 21) connects to HPL (Pin 22) and HPR (Pin 20).
- HPR (Pin 20) connects to HPL (Pin 22) and HPR (Pin 20).
- LINE1-L (Pin 10) connects to LINE1-L (Pin 11) and LINE1-R (Pin 12).
- LINE1-R (Pin 12) connects to LINE1-L (Pin 11) and LINE1-R (Pin 12).
- MIC1-L2 (Pin 16) connects to MIC1-L2 (Pin 17) and MIC1-R2 (Pin 18).
- MIC1-R2 (Pin 18) connects to MIC1-L2 (Pin 17) and MIC1-R2 (Pin 18).
- LINEOUT_3D (Pin 19) connects to LINEOUT_3D (Pin 20) and SPDIF-OUT (Pin 21).
- SPDIF-OUT (Pin 21) connects to LINEOUT_3D (Pin 20) and SPDIF-OUT (Pin 21).

Power and Ground Connections:

- +3V0 (Pin 24) connects to +5VPCU (Pin 8) and USBON# (Pin 6).
- +5VPCU (Pin 8) connects to +5VPCU (Pin 8) and USBON# (Pin 6).
- USBON# (Pin 6) connects to +5VPCU (Pin 8) and USBON# (Pin 6).
- GND (Pin 7) connects to GND (Pin 7) and GND (Pin 7).

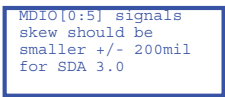
Module Identification:

DLW21HN6005Q2L/300mA/90ohm

Pin Labels:

- 24: +3V0
- 23: HPL
- 22: HPR
- 21: LINE1-L
- 20: LINE1-R
- 19: MIC1-L2
- 18: MIC1-R2
- 17: LINEOUT_3D
- 16: SPDIF-OUT
- 15: +5VPCU
- 14: USBON#
- 13: USBP3- R
- 12: USBP3+ R
- 11: USBP3-L
- 10: USBP3- (Pin 3)
- 9: USBP3+ (Pin 4)
- 8: USBP3-L (Pin 5)
- 7: USBP3- (Pin 6)
- 6: GND
- 5: GND
- 4: GND
- 3: GND
- 2: GND
- 1: GND

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The diagram shows the pinout for the CN15 connector. It is divided into two main sections: a top section for a card reader and a bottom section for other components.

Top Section (Card Reader):

- Pin 1: XD R/B
- Pin 2: XD-RE#
- Pin 3: XD CE#
- Pin 4: XD-CLE
- Pin 5: SD/XD/MS CMD
- Pin 6: XD-WE
- Pin 7: SD/XD WP#
- Pin 8: SD/XD/MS DATA0
- Pin 9: SD/XD/MS DATA1
- Pin 10: SD/XD/MS DATA2
- Pin 11: SD/XD/MS DATA3
- Pin 12: XD-WE
- Pin 13: MMIO_VCCO
- Pin 14: XD CE#
- Pin 15: SD/XD/MS DATA3
- Pin 16: MS INS#
- Pin 17: SD/XD/MS DATA2
- Pin 18: SD/XD/MS DATA0
- Pin 19: XD R/B
- Pin 20: XD-RE
- Pin 21: XD CE#
- Pin 22: XD-CLE
- Pin 23: XD-WE
- Pin 24: SD-VP
- Pin 25: SD-VP
- Pin 26: SD-VP
- Pin 27: SD-VP
- Pin 28: SD-VP
- Pin 29: SD-VP
- Pin 30: SD-VP
- Pin 31: SD-VP
- Pin 32: SD-VP
- Pin 33: SD-VP
- Pin 34: SD-VP
- Pin 35: SD-VP
- Pin 36: SD-VP

Bottom Section (Other Components):

- Pin 37: SHIELD1-GND
- Pin 38: SHIELD2-GND
- Pin 39: SHIELD3-GND
- Pin 40: SHIELD4-GND

Legend:

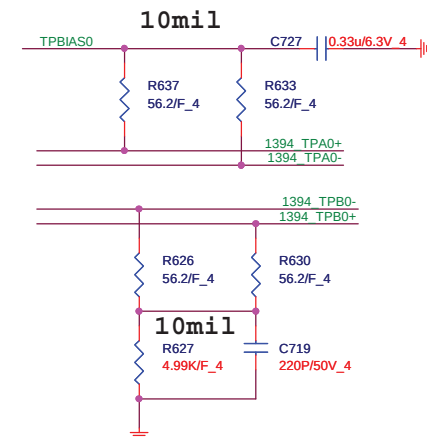
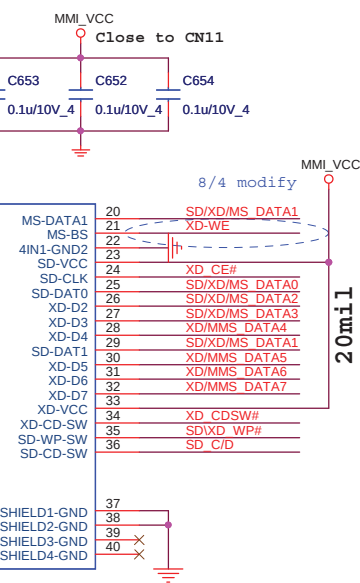
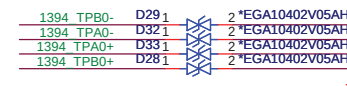
- Blue line: Card Reader
- Red line: Other

Notes:

- Pin 13 is connected to MMIO_VCCO.
- Pin 14 is connected to XD CE#.
- Pin 15 is connected to SD/XD/MS DATA3.
- Pin 16 is connected to MS INS#.
- Pin 17 is connected to SD/XD/MS DATA2.
- Pin 18 is connected to SD/XD/MS DATA0.
- Pin 19 is connected to XD R/B.
- Pin 20 is connected to XD-RE.
- Pin 21 is connected to XD CE#.
- Pin 22 is connected to XD-CLE.
- Pin 23 is connected to XD-WE.
- Pin 24 is connected to SD-VP.
- Pin 25 is connected to SD-VP.
- Pin 26 is connected to SD-VP.
- Pin 27 is connected to SD-VP.
- Pin 28 is connected to SD-VP.
- Pin 29 is connected to SD-VP.
- Pin 30 is connected to SD-VP.
- Pin 31 is connected to SD-VP.
- Pin 32 is connected to SD-VP.
- Pin 33 is connected to SD-VP.
- Pin 34 is connected to SD-VP.
- Pin 35 is connected to SD-VP.
- Pin 36 is connected to SD-VP.

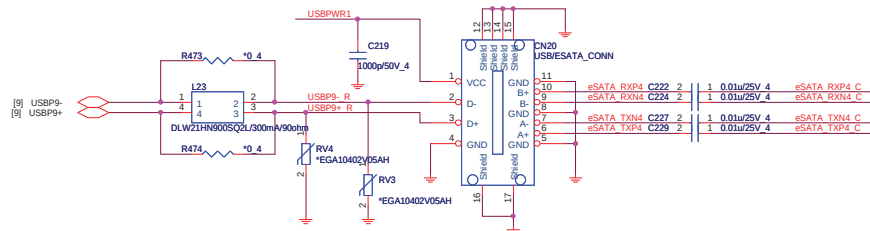
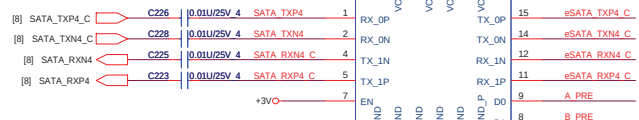
Diagram of the CN13 connector showing pin connections. Pin 1 is connected to 1394 TPB0-, Pin 2 to 1394 TPA0+, Pin 3 to 1394 TPA0-, and Pin 4 to 1394 TPB0-. Pins 5, 6, 7, and 8 are connected to a common ground.

These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Z_0) of 110ohms.

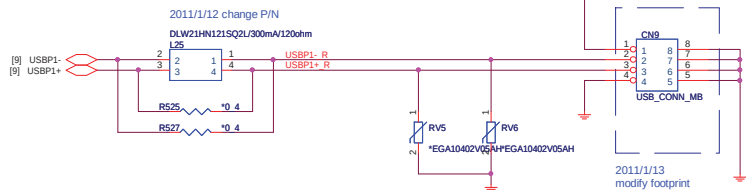


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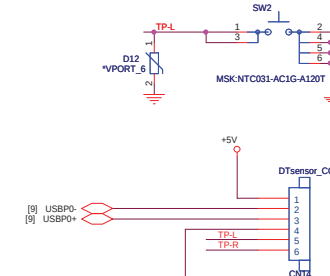
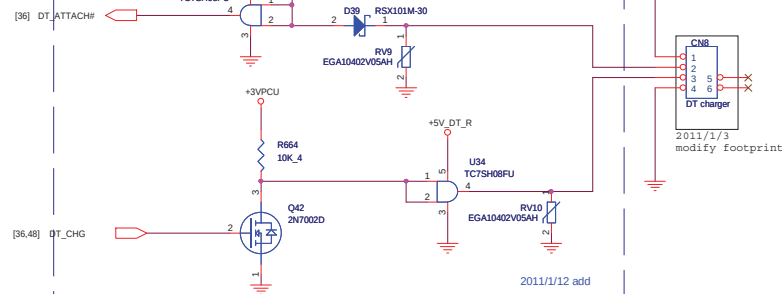
Size	Document Number Card Reader & 1394	Rev 1A
Date:	Friday, January 14, 2011	Sheet 31 of 50

AL008511001ALLVC412000

MB USB dual way

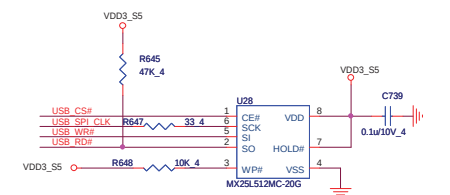


DT dongle



	DT IN	DT OUT
DT_PLUG#	LO	HIGH

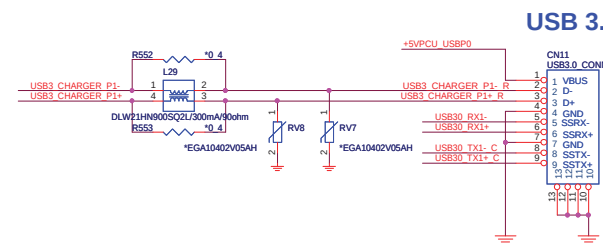
USB3.0 Chip



Clock select signal	
USB3.0_CSEL	High = External 48Mhz Low = 24MHz X'tal

Name	USB data	State	Max Current	Apple Device
SDP	YES	S0-S3	500mA	500mA
CDP	YES	S0-S3	1500mA	500mA
DCP_Auto	NO	S4-S5	1800mA	1800mA

Battery Status, EC GPO control it.
 > Hi: S0 and S3~S5 Battery over 30%
 > Lo: S3~S5/ Battery under 30%



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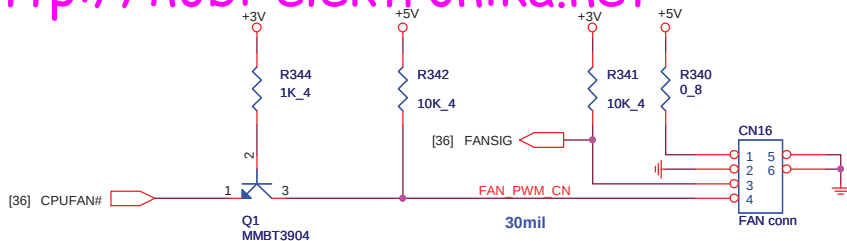
LAN_PWR/B

INT K/B

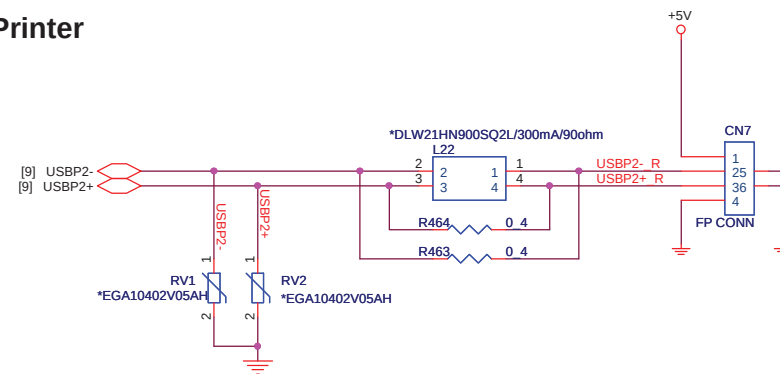
Keyboard LED control

CPU FAN

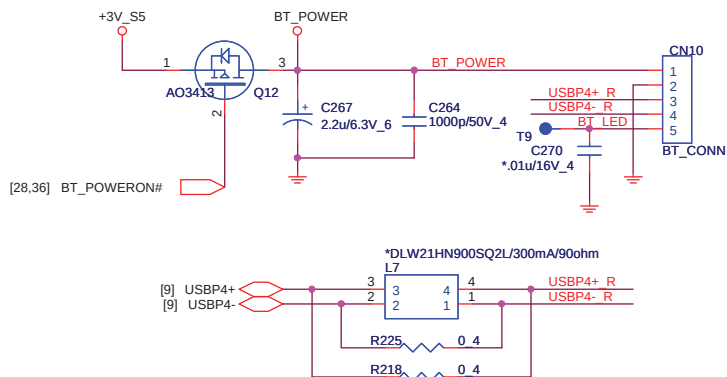
<http://hobi-elektronika.net>



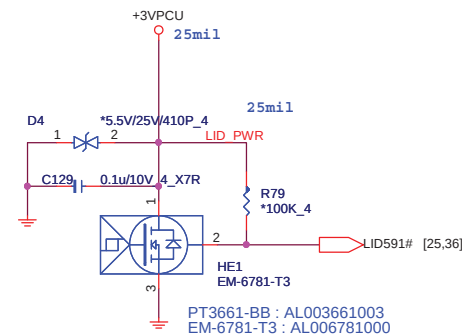
Finger Printer



BT

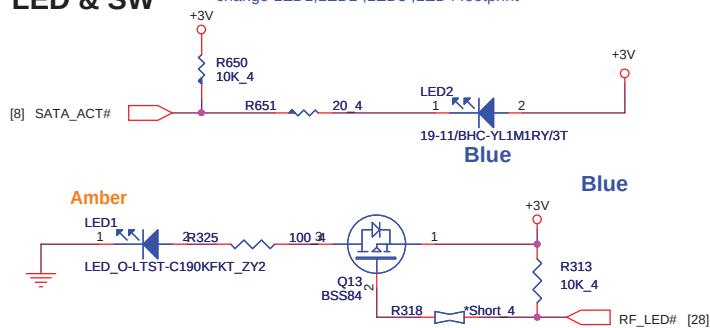


Lid Switch (Hall sensor)

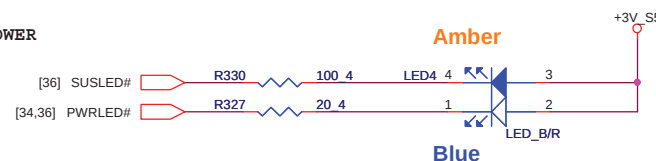


LED & SW

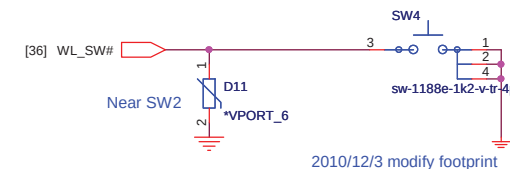
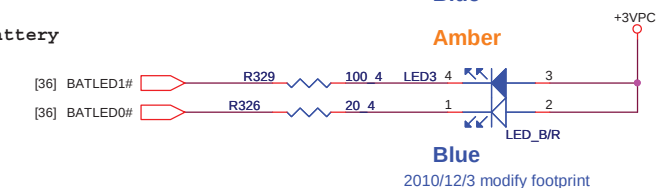
2010/11/21
change LED1,LED2 ,LED3 ,LED4 footprint

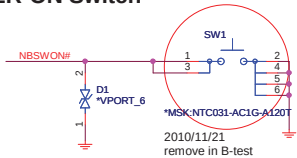


POWER



Battery





	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

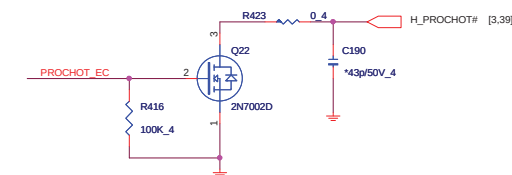


PI FLASH (128K)

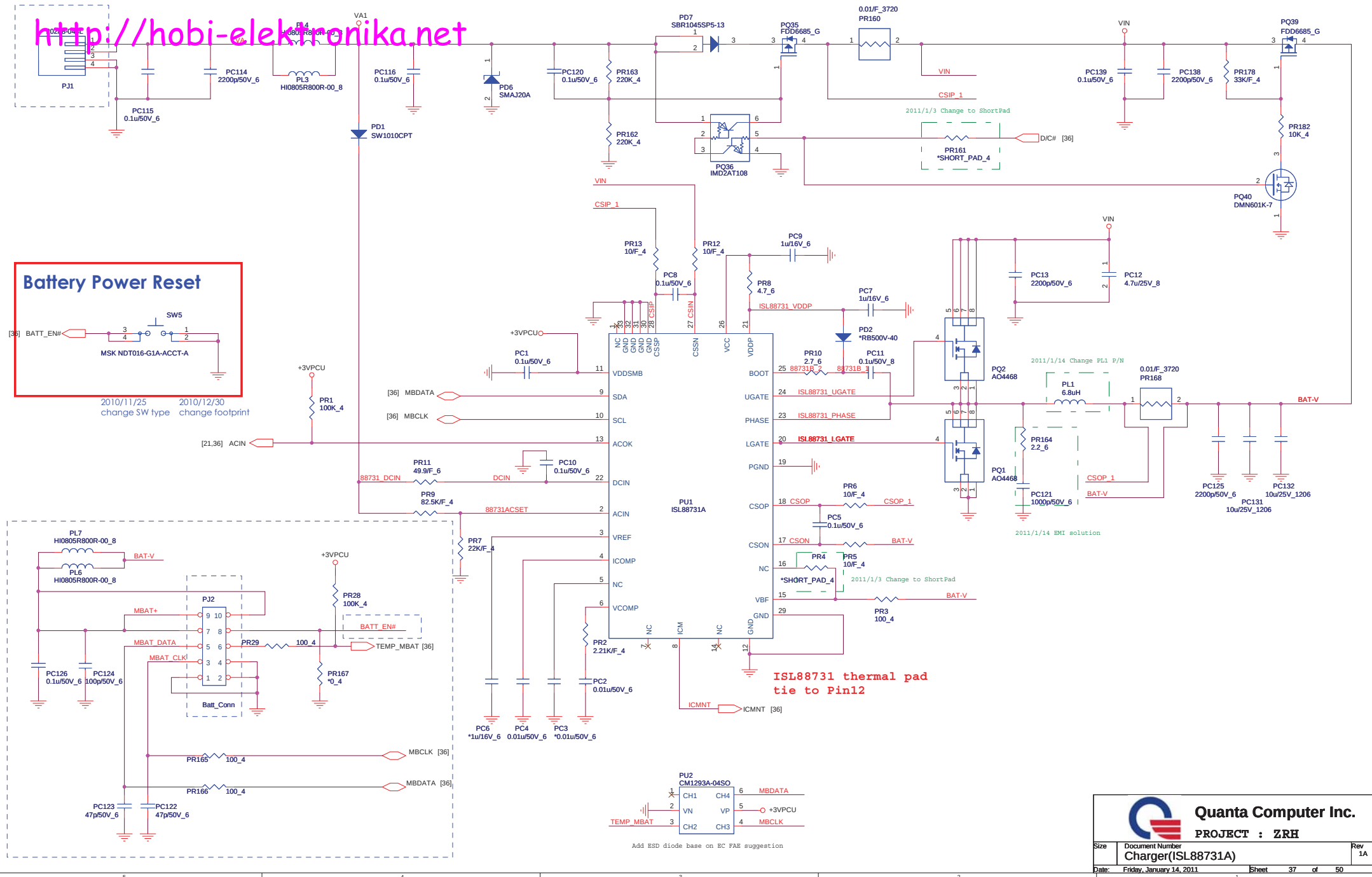
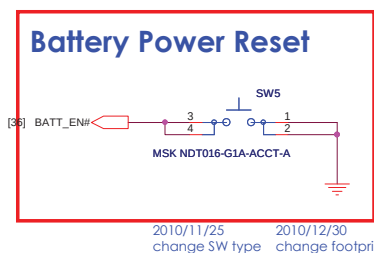
The diagram shows the connection of a W25X10BVSNIG flash chip (U3) to a microcontroller. The chip's pins are connected as follows:

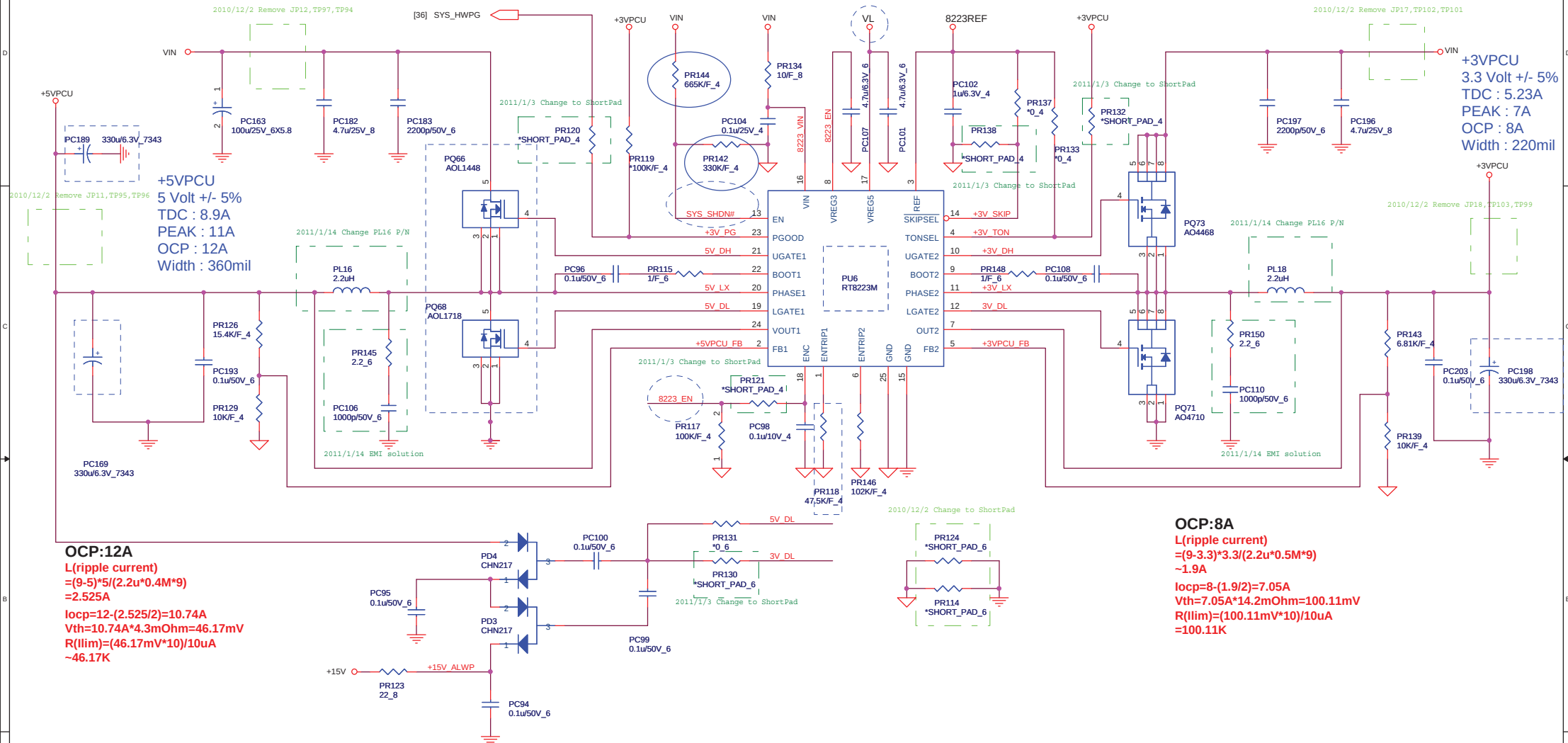
- SDI** (pin 5) to **R54** (10K 4) and **SPI SDI uR**
- SDO** (pin 6) to **R57** (100K 4) and **SPI SDO uR**
- SCK** (pin 7) to **R62** (10K 4) and **SPI SCK uR**
- CS** (pin 8) to **R62** (10K 4) and **SPI CS0W uR**
- VDD** (pin 1) to **+3VPCU**
- VSS** (pin 2) to **+3VPCU**
- W25X10BVSNIG** (pin 3) to **+3VPCU**
- W25X10BVSNIG** (pin 4) to **+3VPCU**
- W25X10BVSNIG** (pin 5) to **+3VPCU**
- W25X10BVSNIG** (pin 6) to **+3VPCU**
- W25X10BVSNIG** (pin 7) to **+3VPCU**
- W25X10BVSNIG** (pin 8) to **+3VPCU**
- W25X10BVSNIG** (pin 9) to **+3VPCU**
- W25X10BVSNIG** (pin 10) to **+3VPCU**
- W25X10BVSNIG** (pin 11) to **+3VPCU**
- W25X10BVSNIG** (pin 12) to **+3VPCU**
- W25X10BVSNIG** (pin 13) to **+3VPCU**
- W25X10BVSNIG** (pin 14) to **+3VPCU**
- W25X10BVSNIG** (pin 15) to **+3VPCU**
- W25X10BVSNIG** (pin 16) to **+3VPCU**
- W25X10BVSNIG** (pin 17) to **+3VPCU**
- W25X10BVSNIG** (pin 18) to **+3VPCU**
- W25X10BVSNIG** (pin 19) to **+3VPCU**
- W25X10BVSNIG** (pin 20) to **+3VPCU**
- W25X10BVSNIG** (pin 21) to **+3VPCU**
- W25X10BVSNIG** (pin 22) to **+3VPCU**
- W25X10BVSNIG** (pin 23) to **+3VPCU**
- W25X10BVSNIG** (pin 24) to **+3VPCU**
- W25X10BVSNIG** (pin 25) to **+3VPCU**
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- W25X10BVSNIG** (pin 92) to **+3VPCU**
- W25X10BVSNIG** (pin 93) to **+3VPCU**
- W25X10BVSNIG** (pin 94) to **+3VPCU**
- W25X10BVSNIG** (pin 95) to **+3VPCU**
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- W25X10BVSNIG** (pin 98) to **+3VPCU**
- W25X10BVSNIG** (pin 99) to **+3VPCU**
- W25X10BVSNIG** (pin 100) to **+3VPCU**
- W25X10BVSNIG** (pin 101) to **+3VPCU**
- W25X10BVSNIG** (pin 102) to **+3VPCU**
- W25X10BVSNIG** (pin 103) to **+3VPCU**
- <

Winbond W25X10BVSNIG	AKE35FN0N00
EON EN25F10-100GIP	AKE35FN0Q00
AMIC A25L010O-F	AKE35ZN0800

[illegible]

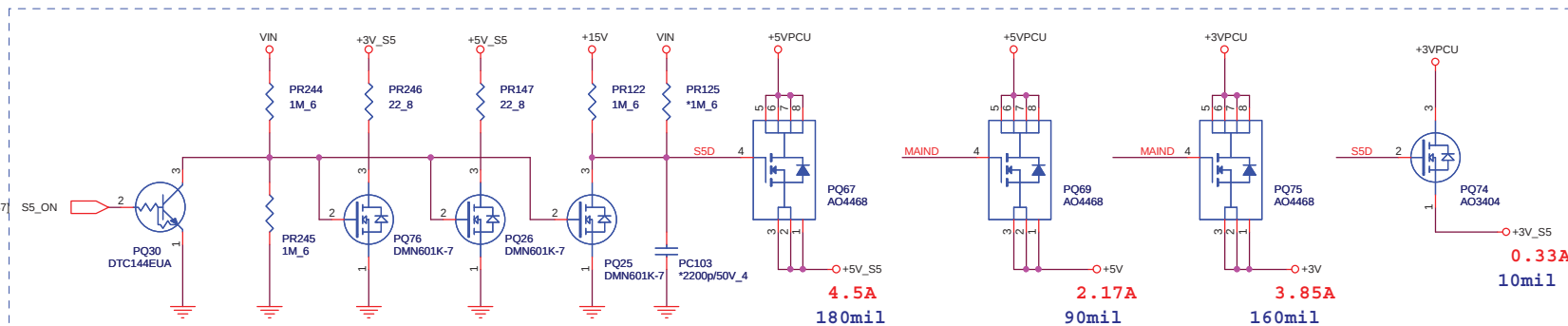
<http://hobi-elektronika.net>



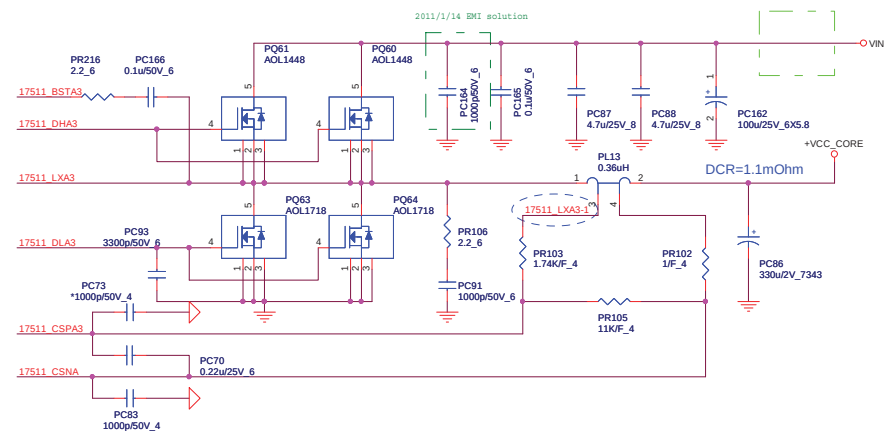
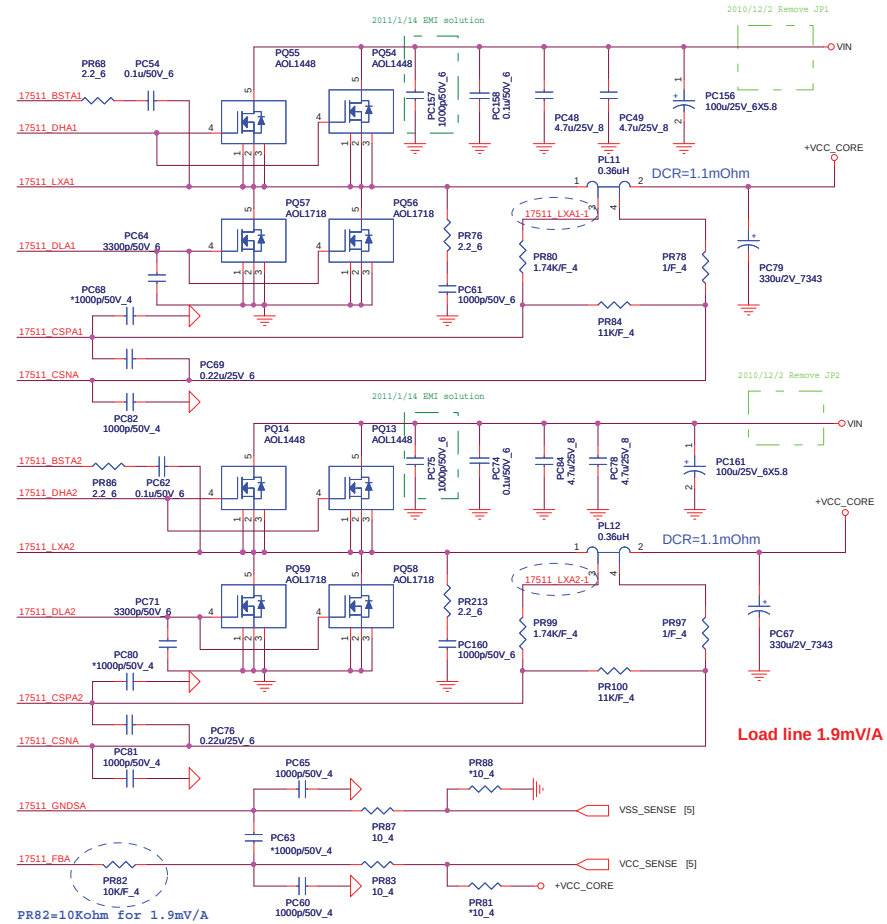
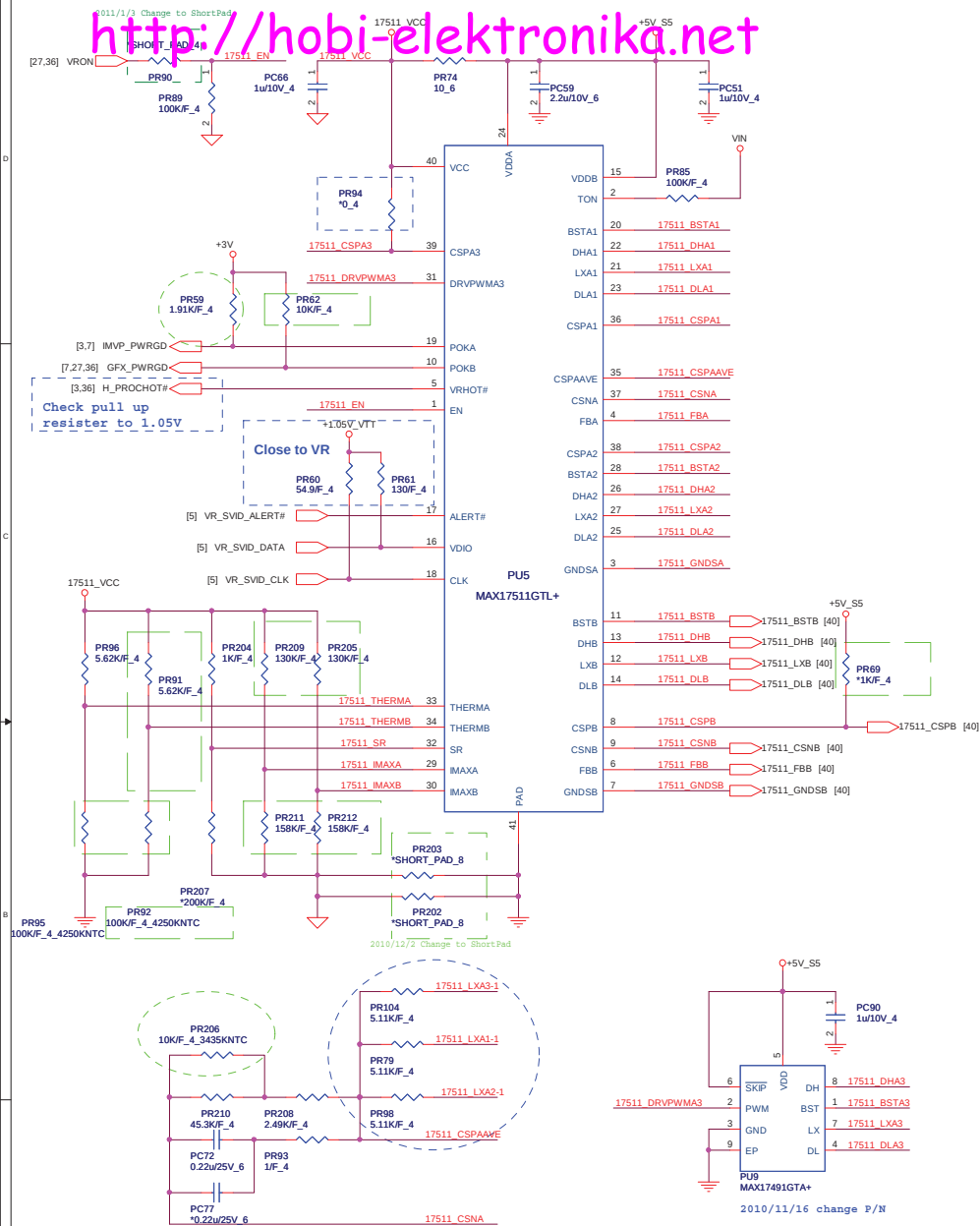


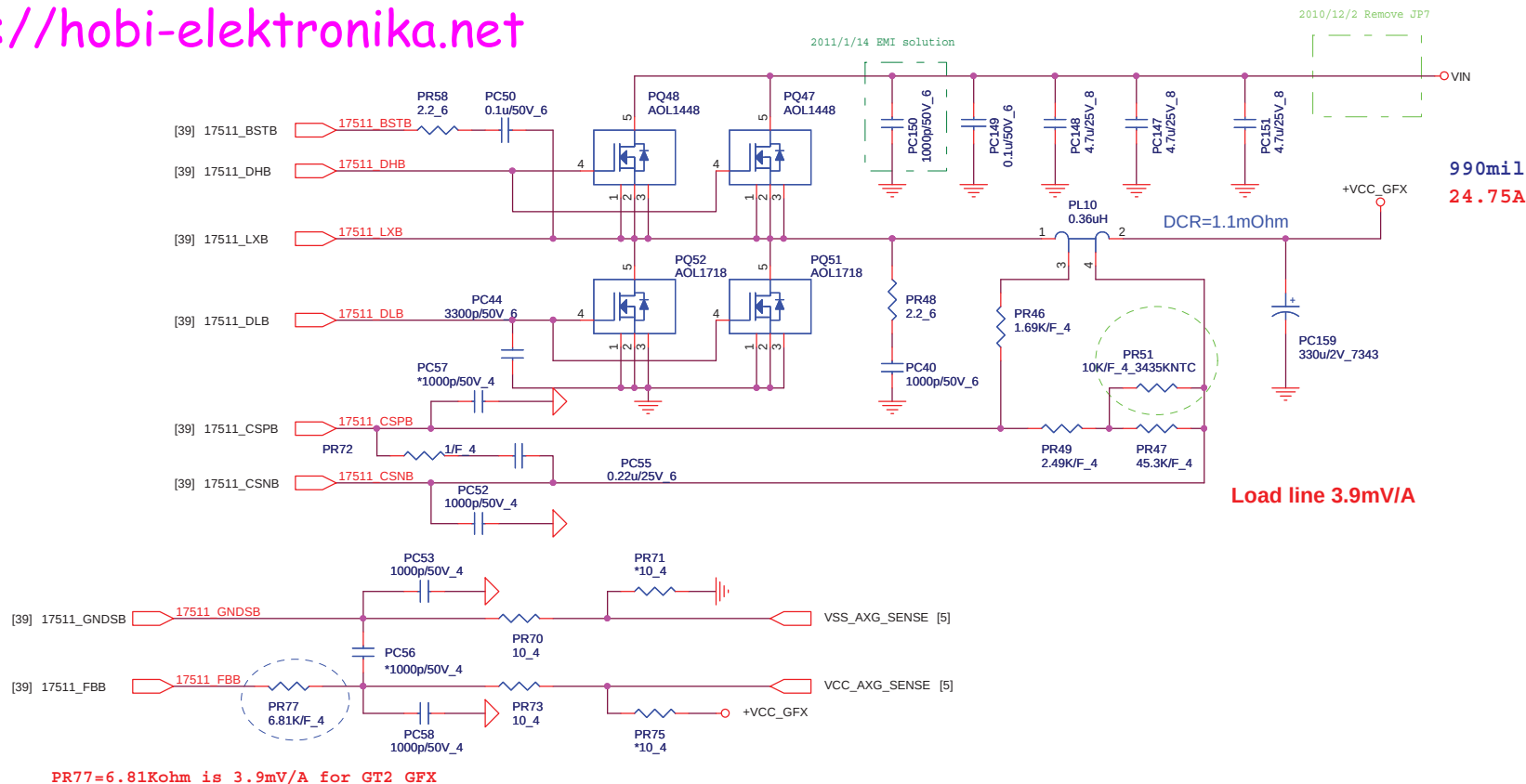
OCP:12A
L(ripple current)
 $= (9.5) \cdot 5 / (2.2 \mu \cdot 0.4 \text{M} \cdot 9)$
 $= 2.525 \text{A}$
 $\text{I}_{\text{ocp}} = 12 - (2.525/2) = 10.74 \text{A}$
 $V_{\text{th}} = 10.74 \text{A} \cdot 4.3 \text{m}\Omega = 46.17 \text{mV}$
 $R(\text{Ilim}) = (46.17 \text{mV} \cdot 10) / 10 \mu \text{A}$
 $\sim 46.17 \text{k}\Omega$

OCP:8A
L(ripple current)
 $= (9-3.3) \cdot 3.3 / (2.2 \mu \cdot 0.5 \text{M} \cdot 9)$
 $\sim 1.9 \text{A}$
 $I_{\text{ocp}} = 8 - (1.9/2) = 7.05 \text{A}$
 $V_{\text{th}} = 7.05 \text{A} \cdot 14.2 \text{m}\Omega = 100.11 \text{mV}$
 $R(\text{Ilim}) = (100.11 \text{mV} \cdot 10) / 10 \mu \text{A}$
 $= 100.11 \text{K}$



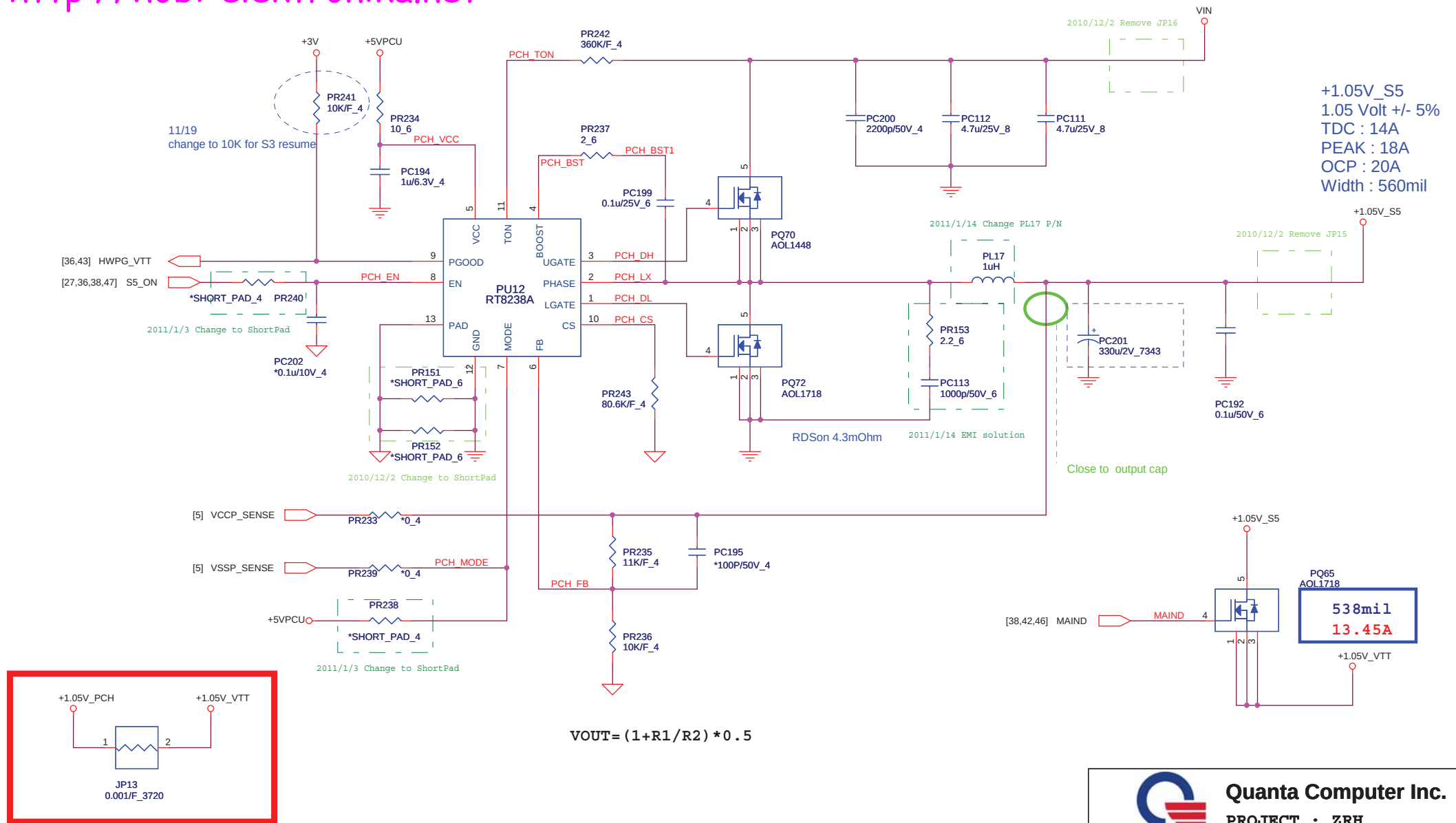
<http://hobi-elektronika.net>





	Dual Core (35W)	Quad Core (45W)
CPU Conver	2-Phase	3-Phase
PR94	Populated	NC
PR209	150K/F_4 (CS41502FB18)	130K/F_4 (CS41302FB00)
PR211	200K/F_4 (CS42002FB12)	158K/F_4 (CS41582FB14)
PR104	NC	5.11K/F_4 (CS25112FB15)
PR79	3.4K/F_4 (CS23402FB08)	5.11K/F_4 (CS25112FB15)
PR98	3.4K/F_4 (CS23402FB08)	5.11K/F_4 (CS25112FB15)

	UMA (IV@) / Muxless (MS@)	External VGA (EV@)
PR69	NC	Populated
PR85	100K/F_4 (CS41002FB28)	200K/F_4 (CS42002FB12)
PR205	130K/F_4 (CS41302FB00)	NC
PR212	158K/F_4 (CS41582FB14)	NC
PR91	5.62K/F_4 (CS25622FB18)	1K/F_4 (CS21002FB24)
PR92	Populated	NC
PR62	Populated	NC



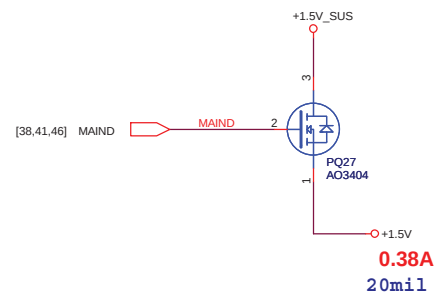


L(ripple current)

$$= (9 - 1.5) \cdot 1.5 / (0.56 \mu \cdot 400 \text{ k} \cdot 9)$$

$$\sim 5.58 \text{ A}$$

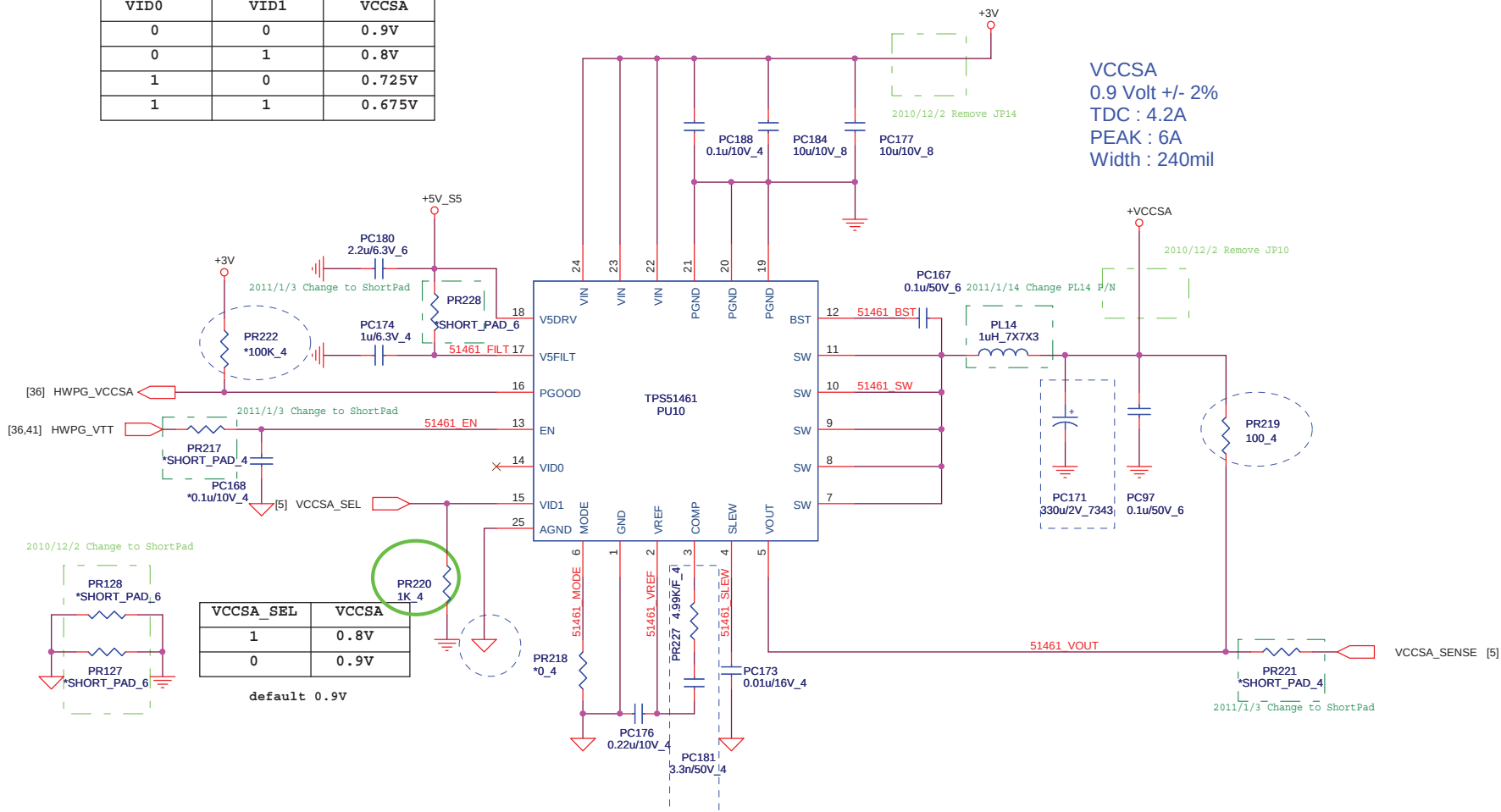
Vtrip= (22-2.79)(*4.3mohm/2)=0.0413V
RILIM=Vtrip/10uA~4.13K



	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (main on off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

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VID0	VID1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V



VCCSA
0.9 Volt +/- 2%
TDC : 4.2A
PEAK : 6A
Width : 240mil

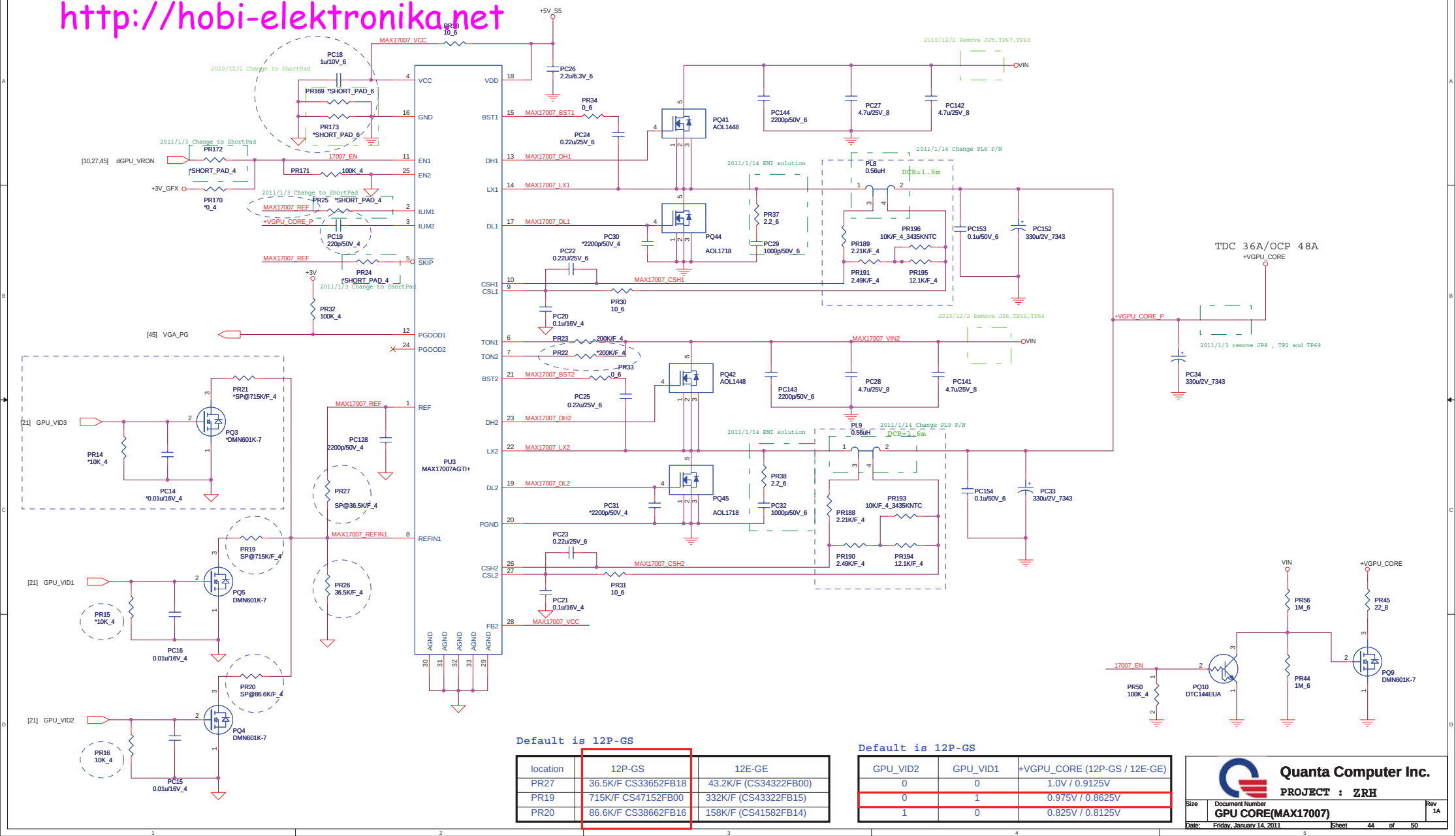
VCCSA_SEL	VCCSA
1	0.8V
0	0.9V

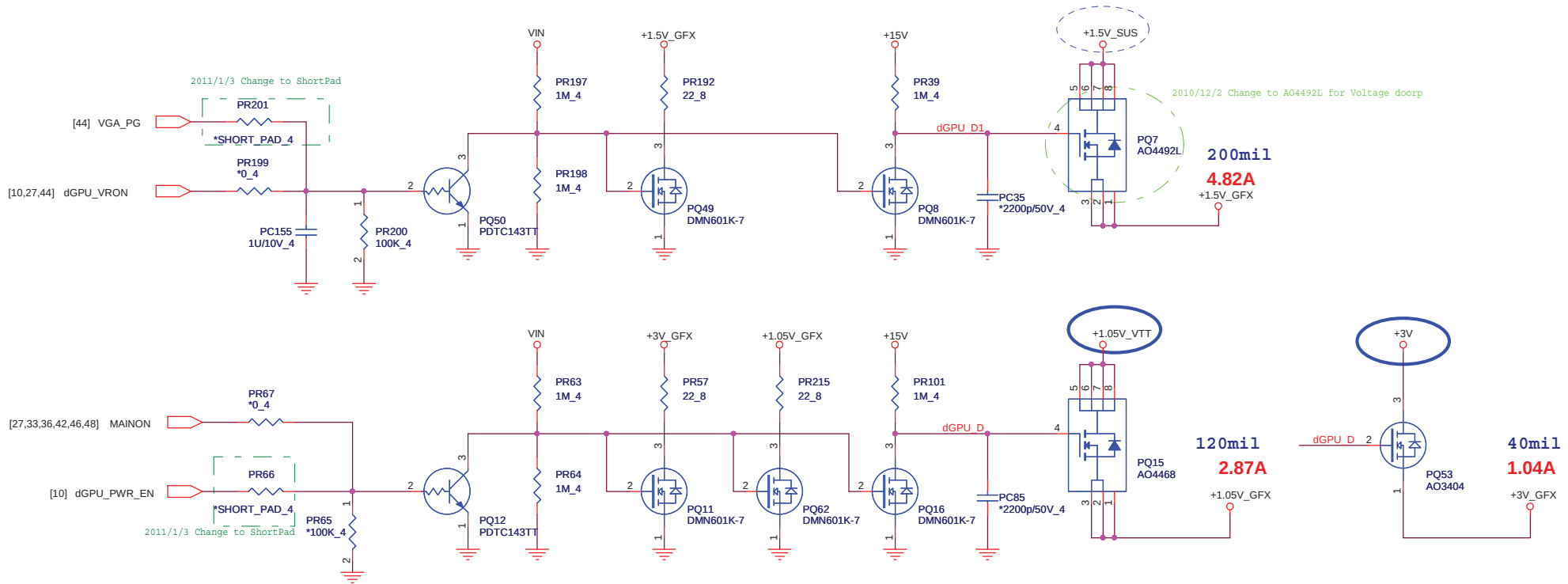
default 0.9V



Quanta Computer Inc.
PROJECT : ZRH

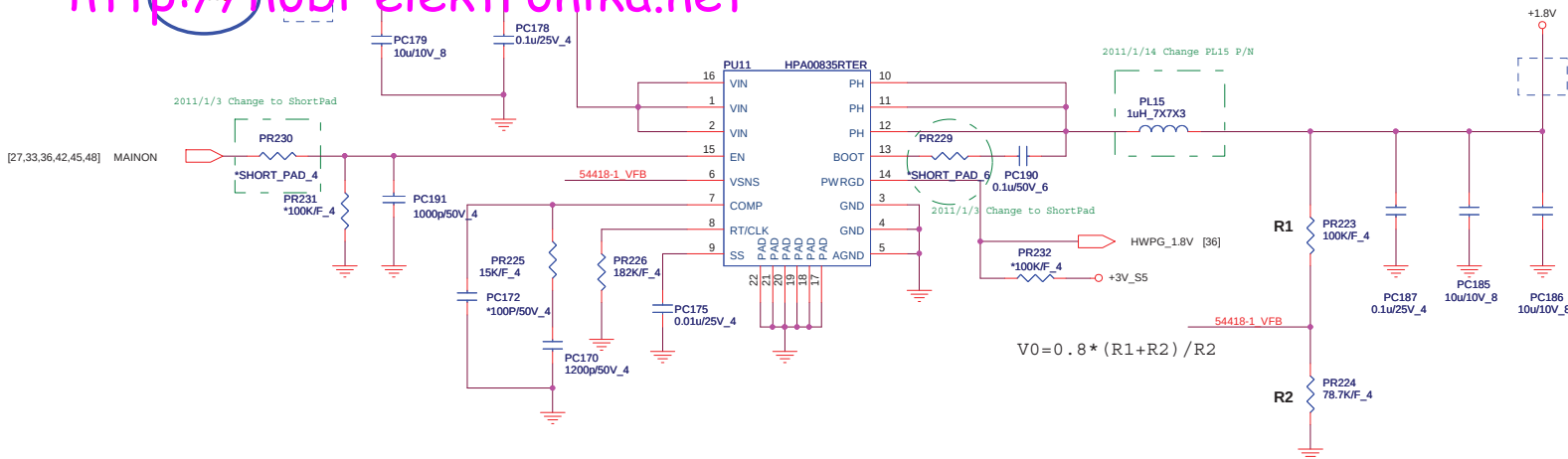
Size	Document Number	Rev
	VCCSA(TPS51461)	1A
Date:	Friday, January 14, 2011	Sheet 43 of 50



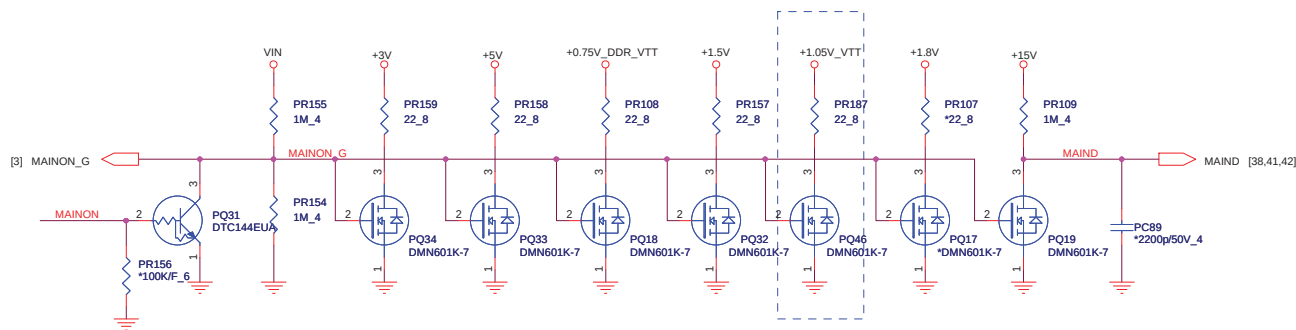
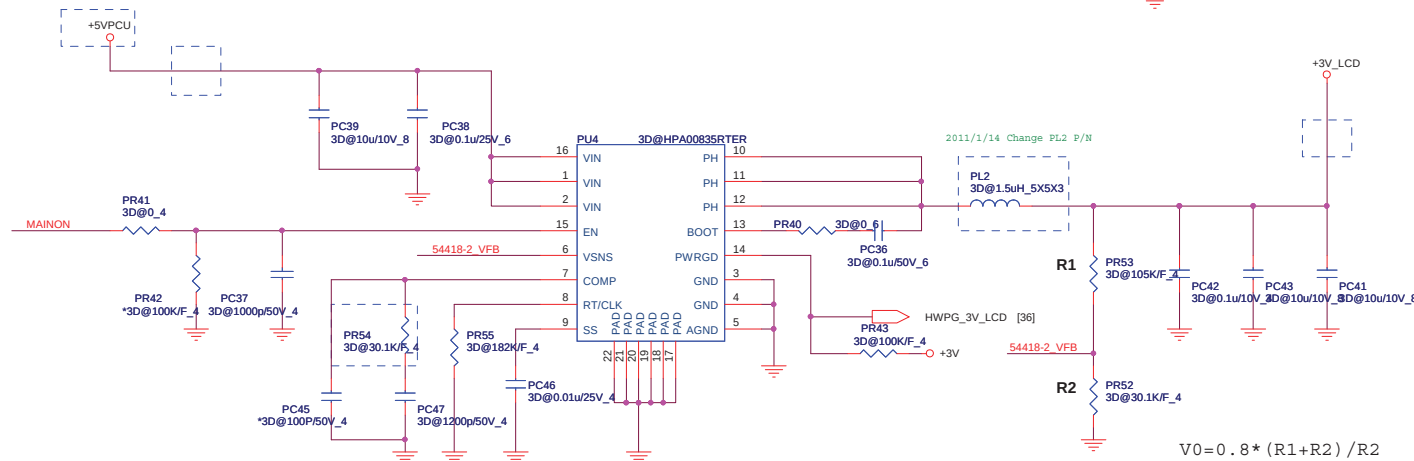


http://hobi-elektronika.net

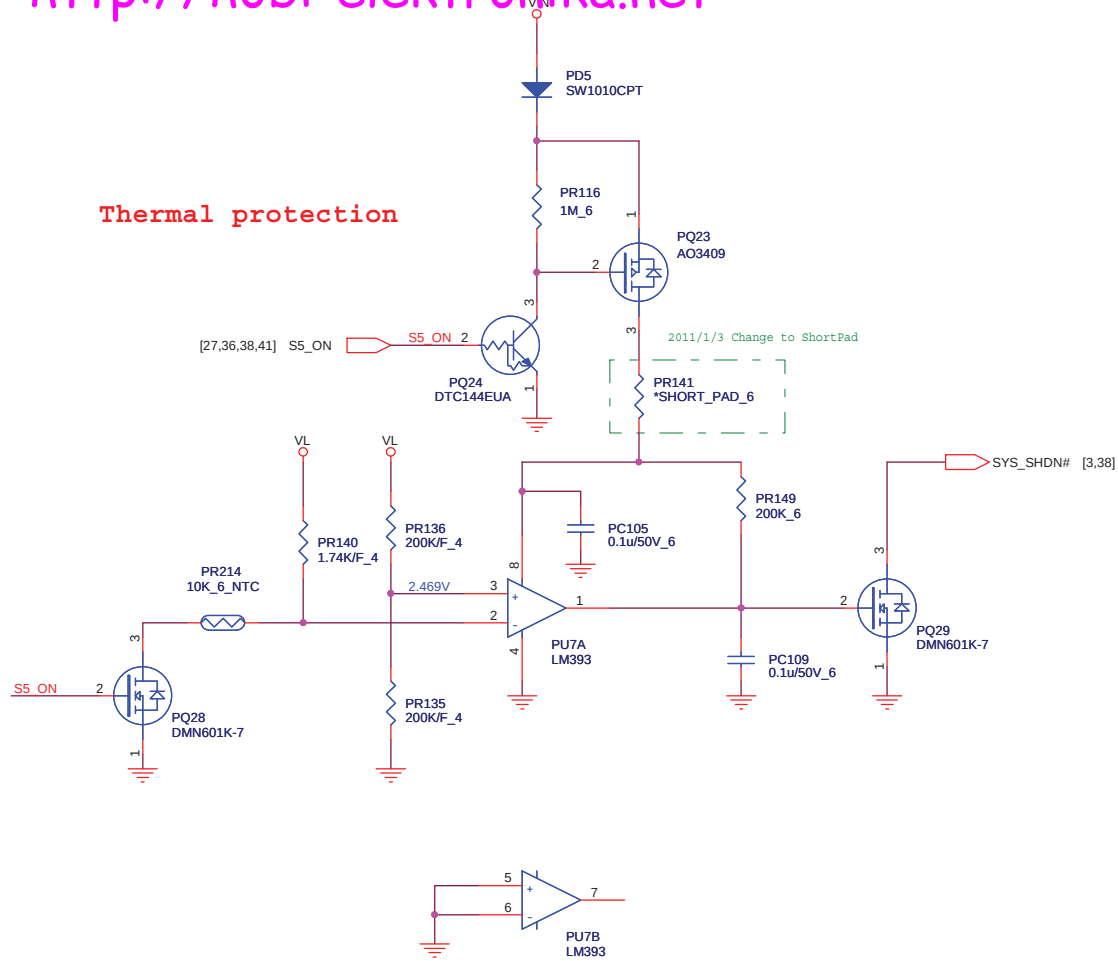
+1.8V
1.8 Volt +/- 5%
TDC : 1.54A
PEAK : 2A
Width : 60mil



+3V_LCD
3.6 Volt +/- 5%
TDC : 1.5A
PEAK : 2A
Width : 60mil



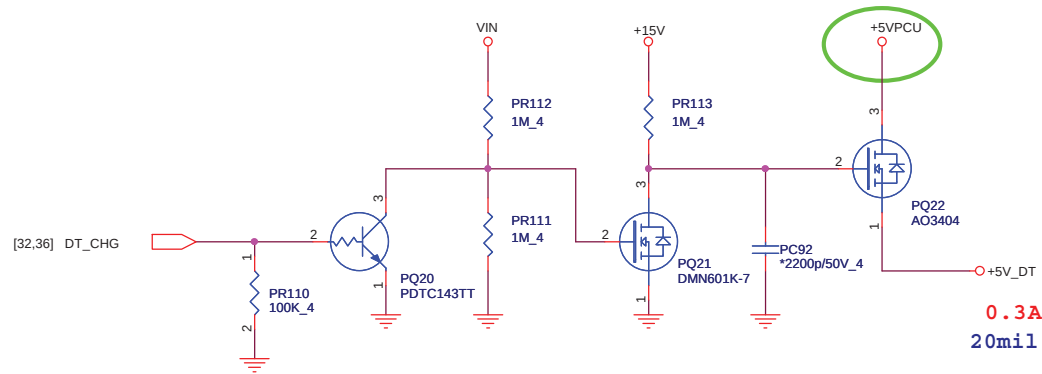
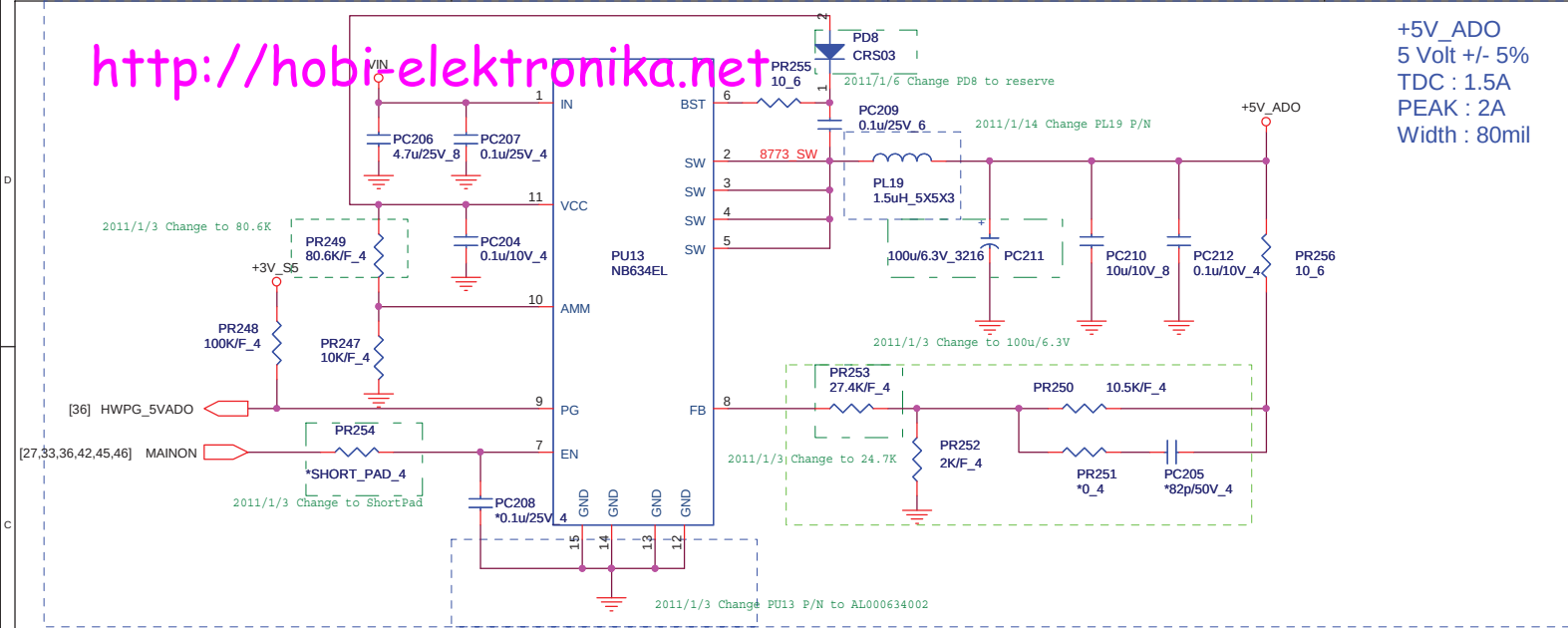
Thermal protection



For EC control thermal protection (output 3.3V)

<http://hobi-elektronika.net>

+5V_ADO
5 Volt +/- 5%
TDC : 1.5A
PEAK : 2A
Width : 80mil



Quanta Computer Inc.

PROJECT : ZRH

Size	Document Number	Rev
	+5V_ADO (MP8773)	1A
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