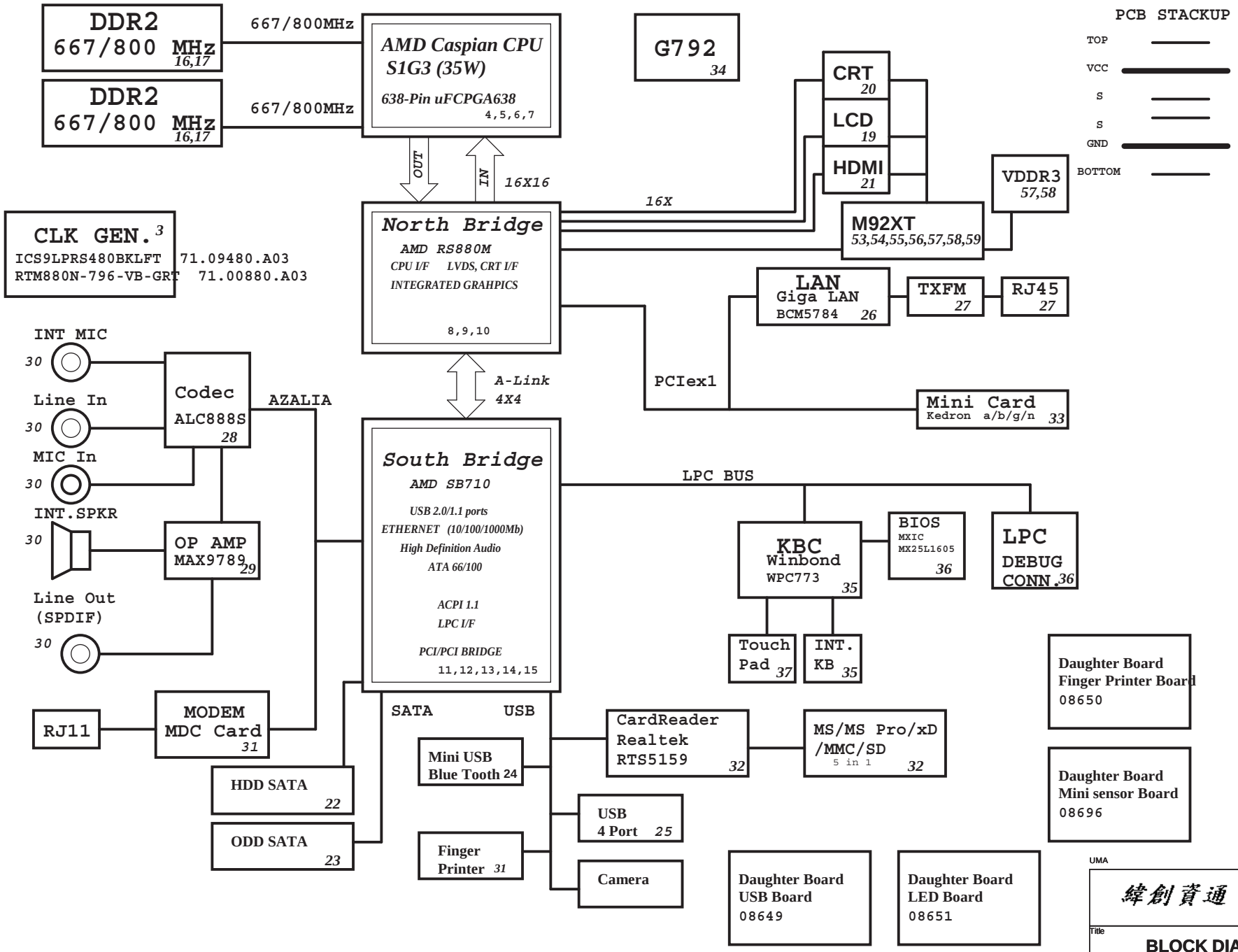
JV71-TR Block Diagram

Project code: 91.4FP01.001
PCB P/N : 48.4FP02.0SB
REVISION : 09243-SB



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC RT8205A 46

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC TPS51124 47

INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(7.5A) 1D2V_S0(4A)

SYSTEM DC/DC RT8209B 48

INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(11A)

RT9025 49

5V_S5	1D1V_M92

RT9161 49

3D3V_S0	2D5V_S0 (200mA)

G957 49

3D3V_S0	1D5V_S0 (1A)

G9161 49

3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731 50

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 45

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	JV71-TR	SB

Date: Monday, July 06, 2009 Sheet 1 of 61

UMA

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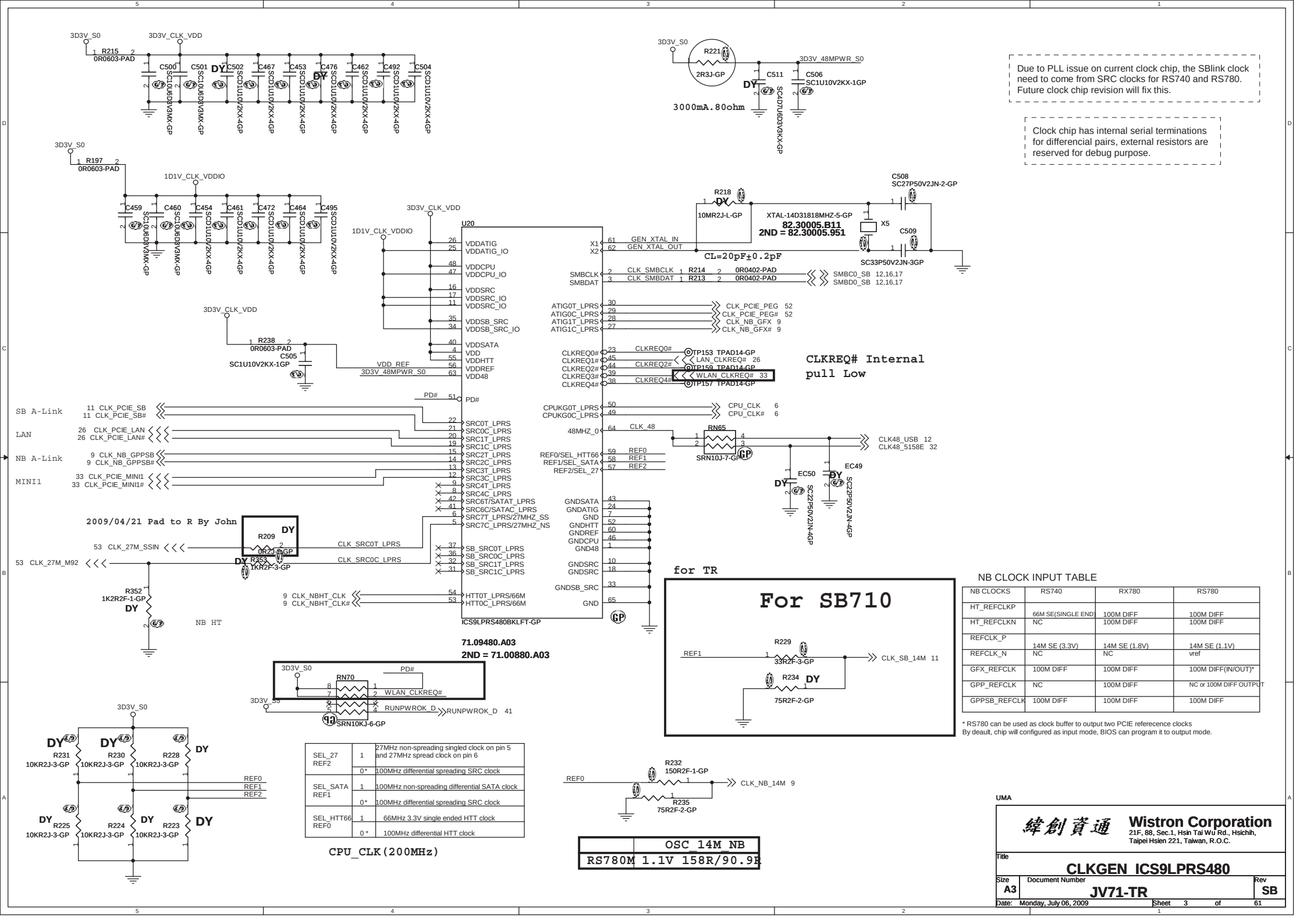
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB/PCIE Routing**

Size	Document Number	Rev
A3	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 2 of 61


3D3V_S0
3D3V_CLK_VDD
R215 0R0603-PAD
C500 SC1U06D3V3MX-GP
C501 SC1U06D3V3MX-GP
C502 SCD1U10V2KX-4GP
C467 SCD1U10V2KX-4GP
C453 SCD1U10V2KX-4GP
C476 SCD1U10V2KX-4GP
C462 SCD1U10V2KX-4GP
C492 SCD1U10V2KX-4GP
C504 SCD1U10V2KX-4GP
DY
3D3V_S0
R221 2R3J-GP
3D3V_48MPWR_S0
C511 SC4D7U6D3V3KX-GP
C506 SC1U10V2KX-1GP
3000mA.80ohm
Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.
3D3V_S0
R197 0R0603-PAD
1D1V_CLK_VDDIO
C459 C460 C454 C461 C472 C464 C495
SCD1U10V2KX-4GP
SC1U06D3V3MX-GP
3D3V_CLK_VDD
U20
1D1V_CLK_VDDIO
VDDATIG 26
VDDATIG_IO 25
VDDCPU 48
VDDCPU_IO 47
VDDSRC 16
VDDSRC_IO 17
VDDSRC_IO 11
VDDSB_SRC 35
VDDSB_SRC_IO 34
VDDSATA 40
VDD 4
VDDHTT 55
VDDREF 56
VDD48 63
R218 10MR2J-L-GP
XTAL-14D31818MHZ-5-GP
82.30005.B11
2ND = 82.30005.951
X5
C508 SC27P50V2JN-2-GP
C509 SC33P50V2JN-3GP
CL=20pF±0.2pF
X1 61 GEN_XTAL_IN
X2 62 GEN_XTAL_OUT
SMBCLK 2 CLK_SMBCLK
SMBDAT 3 CLK_SMBDAT
R214 0R0402-PAD
R213 0R0402-PAD
SMBC0_SB 12,16,17
SMBD0_SB 12,16,17
ATIG0T_LPRS 30 CLK_PCIE_PEG 52
ATIG0C_LPRS 29 CLK_PCIE_PEG# 52
ATIG1T_LPRS 28 CLK_NB_GFX 9
ATIG1C_LPRS 27 CLK_NB_GFX# 9
3D3V_CLK_VDD
R238 0R0603-PAD
C505 SC1U10V2KX-1GP
VDD_REF
3D3V_48MPWR_S0
CLKREQ0# 23 TP153 TPAD14-GP
CLKREQ1# 45 LAN_CLKREQ# 26
CLKREQ2# 44 TP159 TPAD14-GP
CLKREQ3# 39 WLAN_CLKREQ# 33
CLKREQ4# 38 TP157 TPAD14-GP
CLKREQ# Internal pull Low
PD# 51 PD#
SB A-Link 11 CLK_PCIE_SB 11 CLK_PCIE_SB#
LAN 26 CLK_PCIE_LAN 26 CLK_PCIE_LAN#
NB A-Link 9 CLK_NB_GPPSB 9 CLK_NB_GPPSB#
MINI1 33 CLK_PCIE_MINI1 33 CLK_PCIE_MINI1#
SRC0T_LPRS 22
SRC0C_LPRS 21
SRC1T_LPRS 20
SRC1C_LPRS 19
SRC2T_LPRS 15
SRC2C_LPRS 14
SRC3T_LPRS 13
SRC3C_LPRS 12
SRC4T_LPRS 9
SRC4C_LPRS 8
SRC6T/SATAT_LPRS 42
SRC6C/SATAC_LPRS 41
SRC7T_LPRS/27MHZ_SS 6
SRC7C_LPRS/27MHZ_NS 5
CPUKG0T_LPRS 50 CPU_CLK 6
CPUKG0C_LPRS 49 CPU_CLK# 6
48MHZ_0 64 CLK_48
RN65 SRN10J-7-GP
CLK48_USB 12
CLK48_5158E 32
REF0/SEL_HTT66 59 REF0
REF1/SEL_SATA 58 REF1
REF2/SEL_27 57 REF2
EC50 SC22P50V2JN-4GP
EC49 SC22P50V2JN-4GP
GNDSATA 43
GNDATIG 24
GND 7
GNDHTT 52
GNDREF 60
GNDCPU 46
GND48 1
GNDSRC 10
GNDSRC 18
GNDSB_SRC 33
GND 65
2009/04/21 Pad to R By John
R209 0R2J-2-GP
R353 1KR2F-3-GP
53 CLK_27M_SSIN
53 CLK_27M_M92
CLK_SRC0T_LPRS
CLK_SRC0C_LPRS
SB_SRC0T_LPRS 37
SB_SRC0C_LPRS 36
SB_SRC1T_LPRS 32
SB_SRC1C_LPRS 31
R352 1K2R2F-1-GP
NB HT
9 CLK_NBHT_CLK
9 CLK_NBHT_CLK#
HTT0T_LPRS/66M 54
HTT0C_LPRS/66M 53
ICS9LPRS480BKLFT-GP
71.09480.A03
2ND = 71.00880.A03
for TR
For SB710
REF1
R229 33R2F-3-GP
CLK_SB_14M 11
R234 75R2F-2-GP
3D3V_S0
RN70 SRN10KJ-6-GP
PD#
WLAN_CLKREQ#
RUNPWROK_D
RUNPWROK_D 41
3D3V_S0
R231 10KR2J-3-GP
R230 10KR2J-3-GP
R228 10KR2J-3-GP
R225 10KR2J-3-GP
R224 10KR2J-3-GP
R223 10KR2J-3-GP
REF0
REF1
REF2
SEL_27 REF2
1 27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
0* 100MHz differential spreading SRC clock
SEL_SATA REF1
1 100MHz non-spreading differential SATA clock
0* 100MHz differential spreading SRC clock
SEL_HTT66 REF0
1 66MHz 3.3V single ended HTT clock
0* 100MHz differential HTT clock
CPU_CLK(200MHz)
REF0
R232 150R2F-1-GP
R235 75R2F-2-GP
CLK_NB_14M 9
OSC_14M_NB
RS780M 1.1V 158R/90.9R
NB CLOCK INPUT TABLE
NB CLOCKS | RS740 | RX780 | RS780
HT_REFCLKP | 66M SE(SINGLE END) | 100M DIFF | 100M DIFF
HT_REFCLKN | NC | 100M DIFF | 100M DIFF
REFCLK_P | 14M SE (3.3V) | 14M SE (1.8V) | 14M SE (1.1V)
REFCLK_N | NC | NC | vref
GFX_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF(IN/OUT)*
GPP_REFCLK | NC | 100M DIFF | NC or 100M DIFF OUTPUT
GPPSB_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF
* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.
UMA
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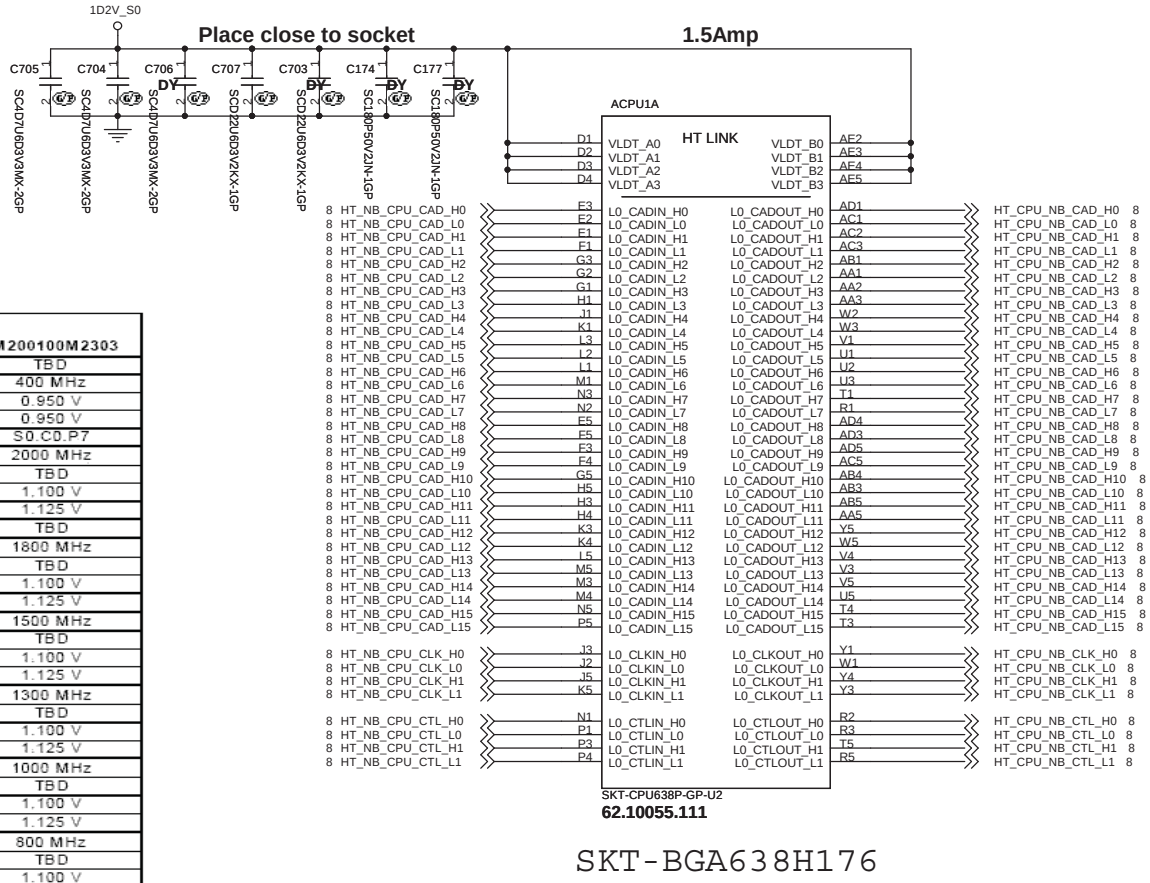
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CLKGEN_ICS9LPRS480
Size A3
Document Number JV71-TR
Rev SB
Date: Monday, July 06, 2009
Sheet 3 of 61



SKT-BGA638H176

State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

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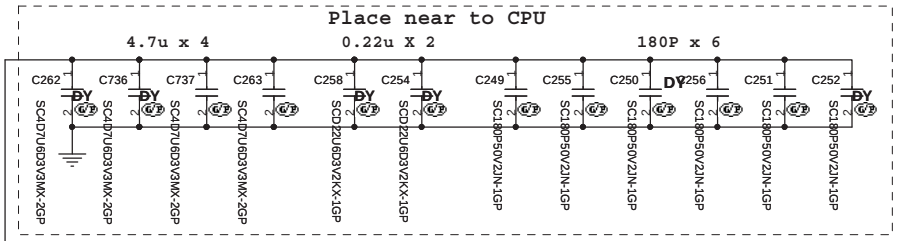
Title: CPU HT LINK I/F (1/4)

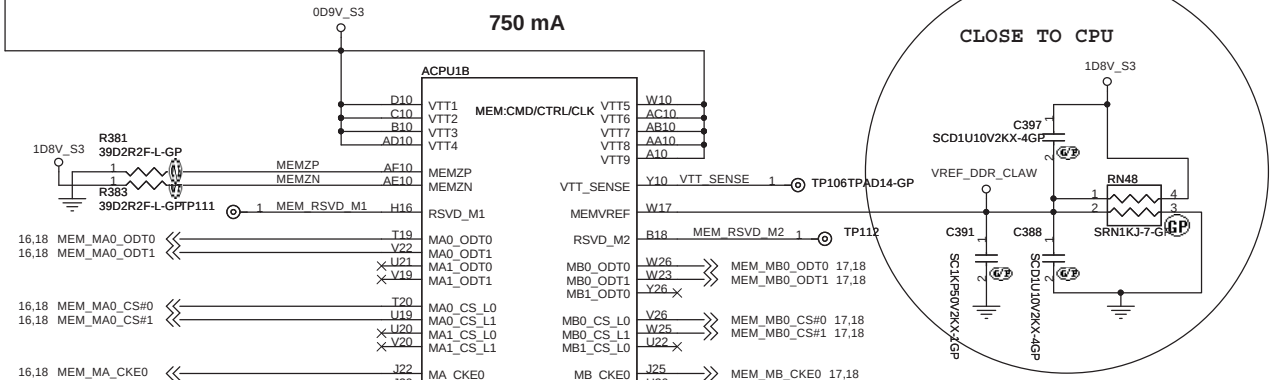
Size: A3 | Document Number: JV71-TR | Rev: SA

Date: Monday, July 06, 2009 | Sheet 4 of 61

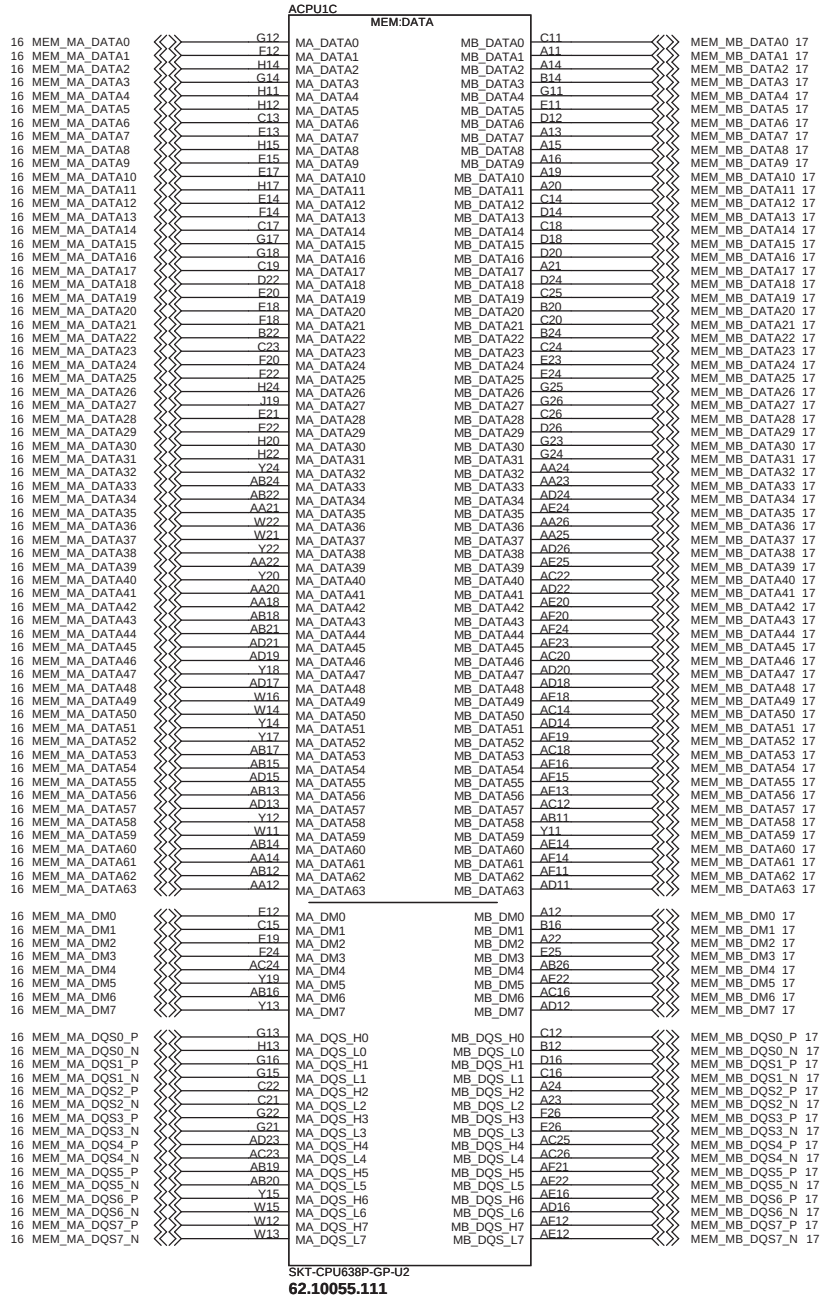


750 mA

CLOSE TO CPU



62.10055.111



62.10055.111

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Title	CPU_DDR_(2/4)	
Size: A3	Document Number: JV71-TR	Rev: SA
Date: Monday, July 06, 2009	Sheet 5 of 61	

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

Cloce To CPU

For HDT DBG

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

for TR

for TR

Near CPU PIN

84.T3904.C11
2ND = 84.03904.L06

CPU exceeds to 125℃

SKT-CPU638P-GP-U2
62.10055.111

HDT Connectors

UMA

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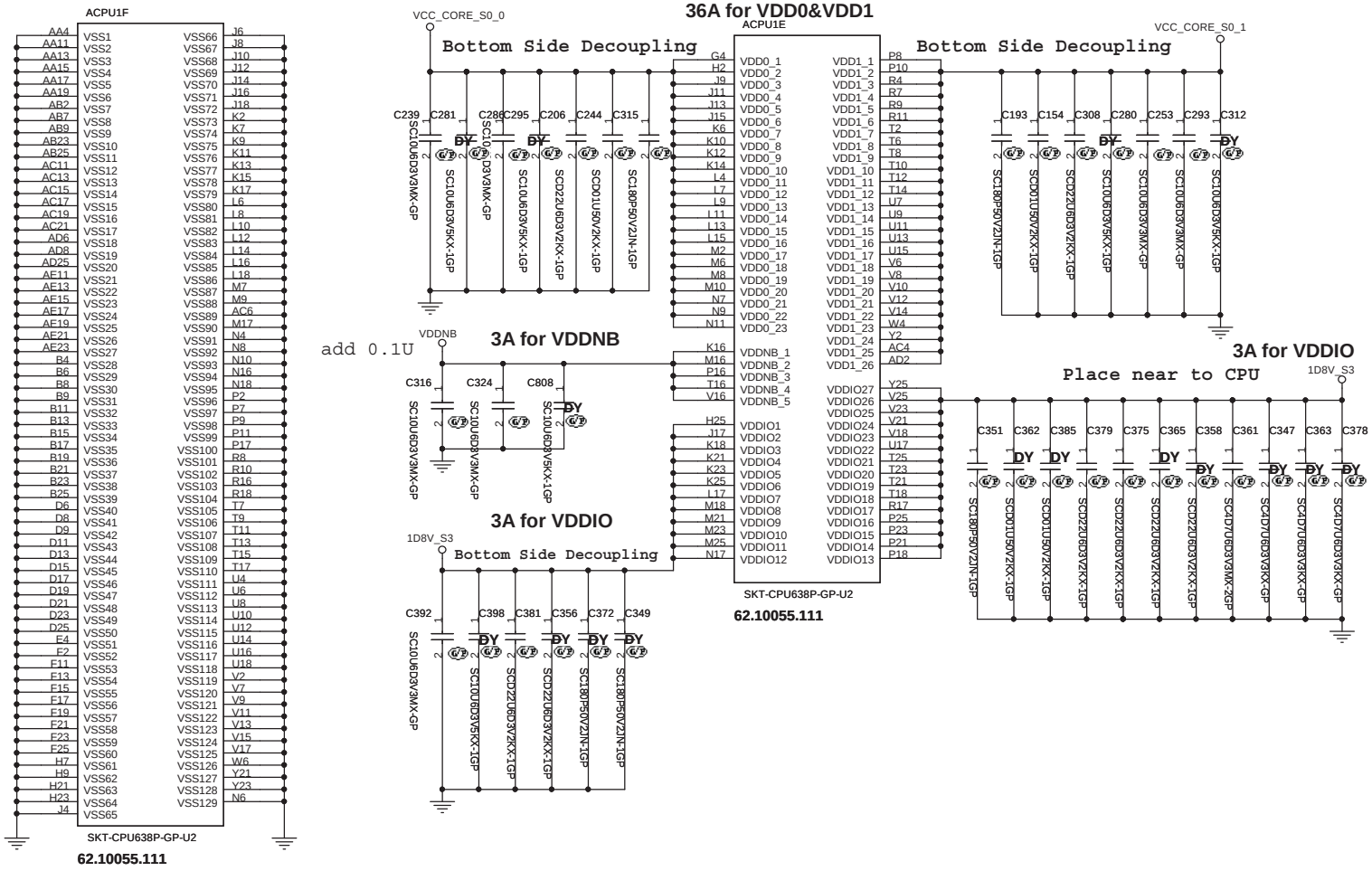
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Control&Debug_(3/4)

Size: A3 | Document Number: JV71-TR | Rev: SA

Date: Monday, July 06, 2009 | Sheet 6 of 61



UMA

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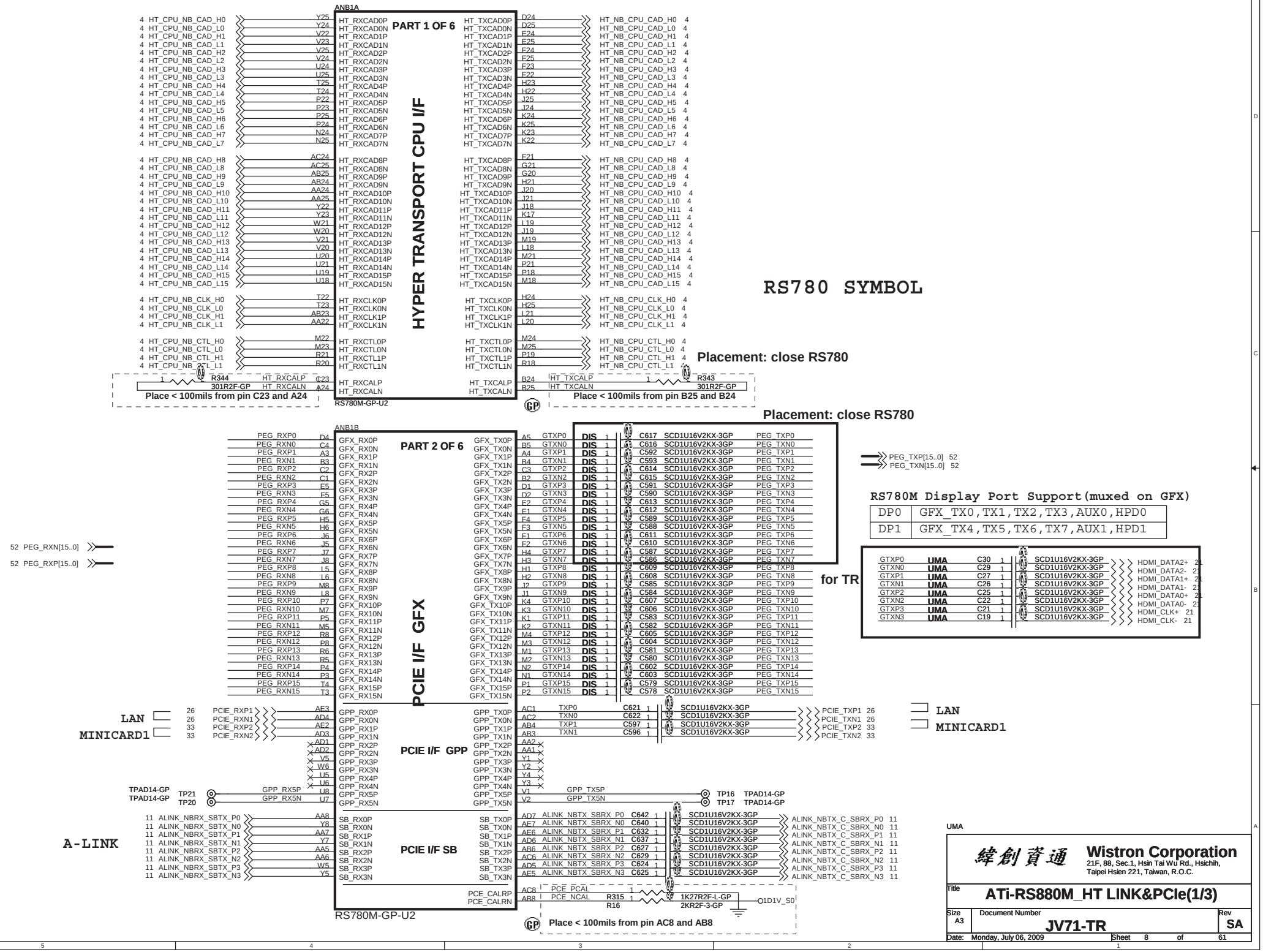
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_Power_(4/4)	
Size A3	Document Number JV71-TR	Rev SA
Date: Monday, July 06, 2009	Sheet 7 of 61	



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.				
Title	ATi-RS880M_HT LINK&PCIe(1/3)				
Size A3	Document Number JV71-TR			Rev SA	
Date: Monday, July 06, 2009	Sheet 8	of	61		

Reserve for EMI 0408

NB_PWRGD — DY EC962 SC1KP50V2KX-1GP

6 LDT_RST#_CPU — R21 0R2J-2-GP — SYSREST#
11,26,35 PLT_RST1# — R17 0R2J-2-GP
C37 SC220P50V2KX-3GP

Close to NB ball

GMCH_BLUE — R36 150R2F-1-GP
GMCH_GREEN — R37 150R2F-1-GP
GMCH_RED — R38 140R2F-GP

2009/04/22 R609 Change to 1K By John

for TR: R609 1KR2F-3-GP (1D8V_S0)

6 LDT_STP#_CPU — R14 0R0402-PAD — NB_LDT_STOP#
6 ALLOW_LDTSTOP — R24 0R2J-2-GP — NB_ALLOW_LDTSTOP
DY

for TR

1D8V_S0 — 220ohm 200mA — L4 2R3J-GP — 2009/05/26 SB Change
TC1 ST100U6D3VBM-1GP
C78 SCD1U10V2KX-1GP — DY C77 SCD1U10V2KX-4GP
DY C82 SC47U6D3V5MX-1GP

80.10715.L04
2ND = 77.C1071.081
3RD = 77.21071.09L

1D1V_S0 — L33 SBK160808T-221Y-N-GP — 220ohm 200mA — 68.00119.111
C644 SC1U10V2KX-1GP — C643 SCD1U10V2KX-4GP DY

3D3V_S0 — L3 220ohm 200mA SBK160808T-221Y-N-GP — 68.00119.111
3D3V_S0_AVDD
C70 SCD1U10V2KX-4GP DY
C71 SC1U10V2KX-1GP

1D8V_S0 — R41 0R0603-PAD — 1D8V_S0_AVDDDI
C88 SC1U10V2KX-1GP — C89 SCD1U10V2KX-4GP
68.00119.111

1D8V_S0 — 220ohm 200mA — R43 SBK160808T-221Y-N-GP
C80 SC1U10V2KX-1GP — C99 SCD1U10V2KX-4GP
TC2 ST100U6D3VBM-5GP — DY 77.C1071.081
1D8V_S0_AVDDQ

3D3V_S0 — R563 3K3R2J-3-GP — R562 3K3R2J-3-GP
GMCH_VSYNC
GMCH_HSYNC

STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable

SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

ANB1C — PART 3 OF 6

CRT/TVOUT
AVDD1 F12
AVDD2 F12
AVDDDI F14
AVSSDI G15
AVDDQ H15
AVSSQ H14
C_Pr E17
Y E17
COMP_Pb E15
RED G18
REDb G17
GREEN E18
GREENb F18
BLUE E19
BLUEb F19
DAC_HSYNC A11
DAC_VSYNC B11
DAC_SCL F8
DAC_SDA F8
DAC_RSET G14

PLL PWR LVTM
PLLVDD A12
PLLVDD18 D14
PLLVSS B12
VDDA18HTPLL H17
VDDA18PCIEPLL1 D7
VDDA18PCIEPLL2 E7
SYSRESET# D8
POWERGOOD A10
LDTSTOP# C10
ALLOW_LDTSTOP C12

CLOCKs PM
HT_REFCLKP C25
HT_REFCLKN C24
REFCLK_P/OSCIN E11
REFCLK_N F11
GFX_REFCLKP T2
GFX_REFCLKN T1
GPP_REFCLKP U1
GPP_REFCLKN U2
GPPSB_REFCLKP V4
GPPSB_REFCLKN V3

MIS.
I2C_CLK B9
I2C_DATA A9
DDC_CLK0/AUX0P B8
DDC_DATA0/AUX0N A8
DDC_CLK1/AUX1P B7
DDC_DATA1/AUX1N A7
STRP_DATA B10
RESERVED G11
AUX_CAL C8

20 GMCH_RED — 20 GMCH_GREEN — 20 GMCH_BLUE
20 GMCH_HSYNC — 20 GMCH_VSYNC — 20 GMCH_DDCCLK — 20 GMCH_DDCDATA
SYSREST# — 12,41 NB_PWRGD — NB_LDT_STOP# — 11 NB_ALLOW_LDTSTOP
3 CLK_NBHT_CLK — 3 CLK_NBHT_CLK#
3 CLK_NB_14M — NB_REFCLK_N
3 CLK_NB_GFX — 3 CLK_NB_GFX#
TPAD14-GP TP180 CLK_NBGPP_CLK — TPAD14-GP TP181 CLK_NBGPP_CLK#
3 CLK_NB_GPPSB — 3 CLK_NB_GPPSB#
19 CLK_DDC_EDID — 19 DAT_DDC_EDID
TPAD14-GP TP188 DDC_DATA0/AUX0N — TPAD14-GP TP239 DDC_CLK0/AUX0P
21 GMCH_HDMI_CLK — GMCH_HDMI_CLK
21 GMCH_HDMI_DATA — GMCH_HDMI_DATA
STRP_DATA
RS780_AUX_CAL — R294 150R2F-1-GP

RS780M-GP-U2

TXOUT_L0P A22 — GMCH_TXAOUT0+ 19
TXOUT_L0N B22 — GMCH_TXAOUT0- 19
TXOUT_L1P A21 — GMCH_TXAOUT1+ 19
TXOUT_L1N B21 — GMCH_TXAOUT1- 19
TXOUT_L2P B20 — GMCH_TXAOUT2+ 19
TXOUT_L2N A20 — GMCH_TXAOUT2- 19
TXOUT_L3P A19
TXOUT_L3N B19

TXOUT_U0P B18 — GMCH_TXBOUT0+ 19
TXOUT_U0N A18 — GMCH_TXBOUT0- 19
TXOUT_U1P A17 — GMCH_TXBOUT1+ 19
TXOUT_U1N B17 — GMCH_TXBOUT1- 19
TXOUT_U2P D20 — GMCH_TXBOUT2+ 19
TXOUT_U2N D21 — GMCH_TXBOUT2- 19
TXOUT_U3P D18
TXOUT_U3N D19

TXCLK_LP B16 — GMCH_TXACLK+ 19
TXCLK_LN A16 — GMCH_TXACLK- 19
TXCLK_UP D16 — GMCH_TXBCLK+ 19
TXCLK_UN D17 — GMCH_TXBCLK- 19

VDDLTP18 A13 — 1D8V_S0_VDDLP18 — L34 SBK160808T-221Y-N-GP — 68.00119.111
VSSLTP18 B13
C649 SC1U10V2KX-1GP DY — C648 SCD1U10V2KX-4GP
VDDLT18_1 A15
VDDLT18_2 B15
VDDLT33_1 A14
VDDLT33_2 B14
1D8V_S0_VDDLT18 — L35 PBY201209T-221Y-N-GP — 68.00206.121
VSSLT1 C14
VSSLT2 D15
VSSLT3 C16
VSSLT4 C18
VSSLT5 C20
VSSLT6 F20
VSSLT7 C22
C652 — DY C653 SCD1U10V2KX-4GP
SC4D7U6D3V3MX-2GP

LVDS_DIGON E9 — GMCH_LCDVDD_ON 19
LVDS_BLON E7 GMCH_BL_ON — GMCH_BL_ON 35
LVDS_ENA_BL G12 LVDS_ENA_BL — TP26 TPAD14-GP
RN10 SRN4K7J-10-GP — UMA

TMDS_HPD D9
HPD D10 NB_DVI_HPD — HDMI_DETECT# 21 — TP24 TPAD14-GP
SUS_STAT# D12 SUS_STAT# — R29 10KR2J-3-GP — 3D3V_S0
THERMALDIODE_P AE8 RS780_DXP3_1 — TP23 TPAD14-GP
THERMALDIODE_N AD8 RS780_DXN3_1 — TP22 TPAD14-GP
TESTMODE D13 TESTMODE_NB — R347 1K8R2F-GP

RS780 SYMBOL

ENABLE External CLK GEN
1D1V_S0 — RN11 SRN1KJ-7-GP

	GPIO MODE	
STRP_DATA	0	*1
VCC_NB	1.1V	1.0V

1D8V_S0 — L5 68.00119.111 — VDDA18HTPLL — 220ohm 200mA SBK160808T-221Y-N-GP — C86 DY SC1U10V2KX-1GP — C97 SCD1U10V2KX-4GP
1D8V_S0 — L1 68.00119.111 — VDDA18PCIEPLL — 220ohm 200mA SBK160808T-221Y-N-GP — C41 SC1U10V2KX-1GP DY — C42 SCD1U10V2KX-4GP

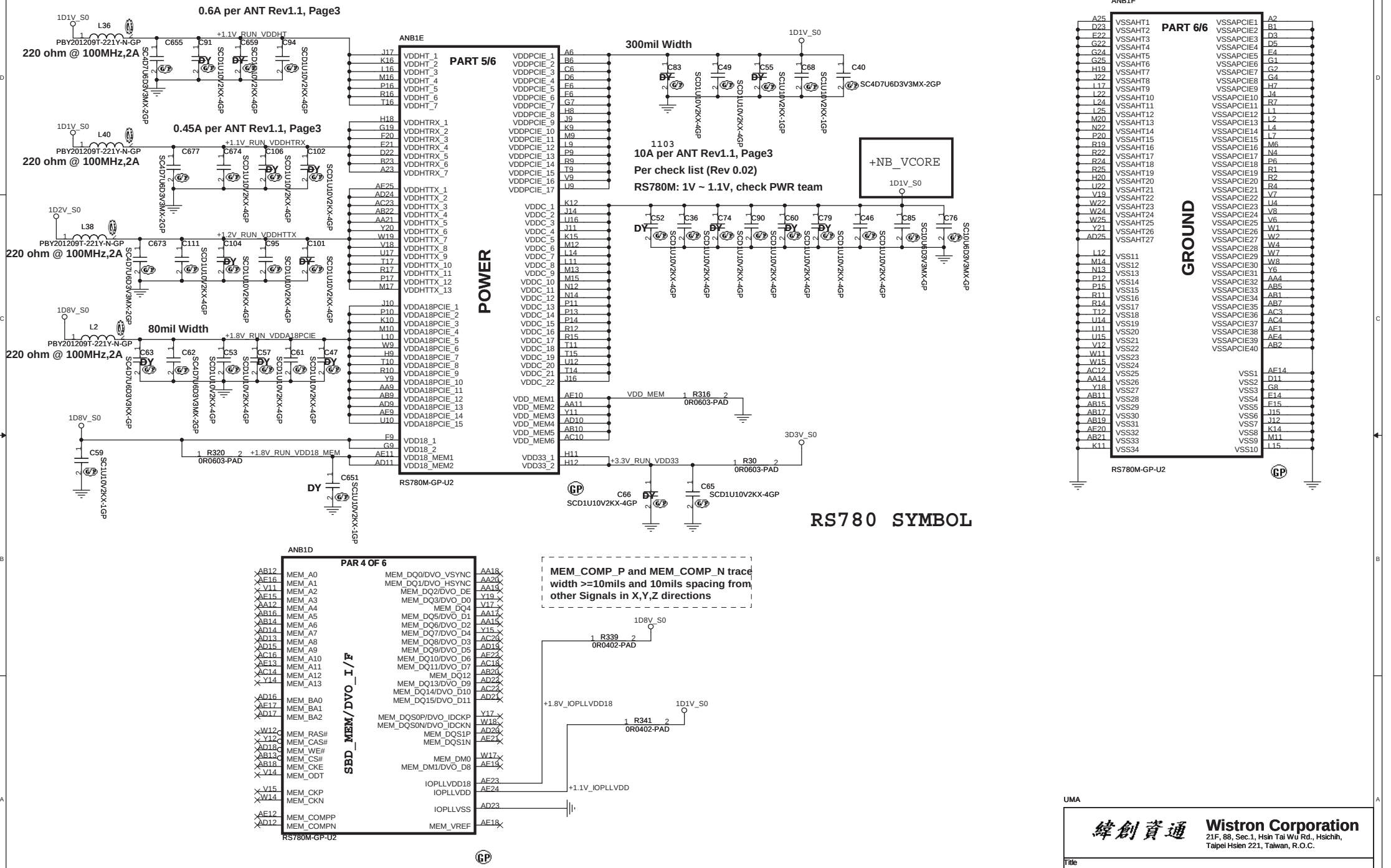
3D3V_S0 — R19 2K2R2J-2-GP DY — STRP_DATA

35,53 BLON_IN — RN64 — LVDS_ENA_BL
19,53 BRIGHTNESS_AMD — GMCH_BL_ON
SRN0J-10-GP-U — UMA
for TR

UMA

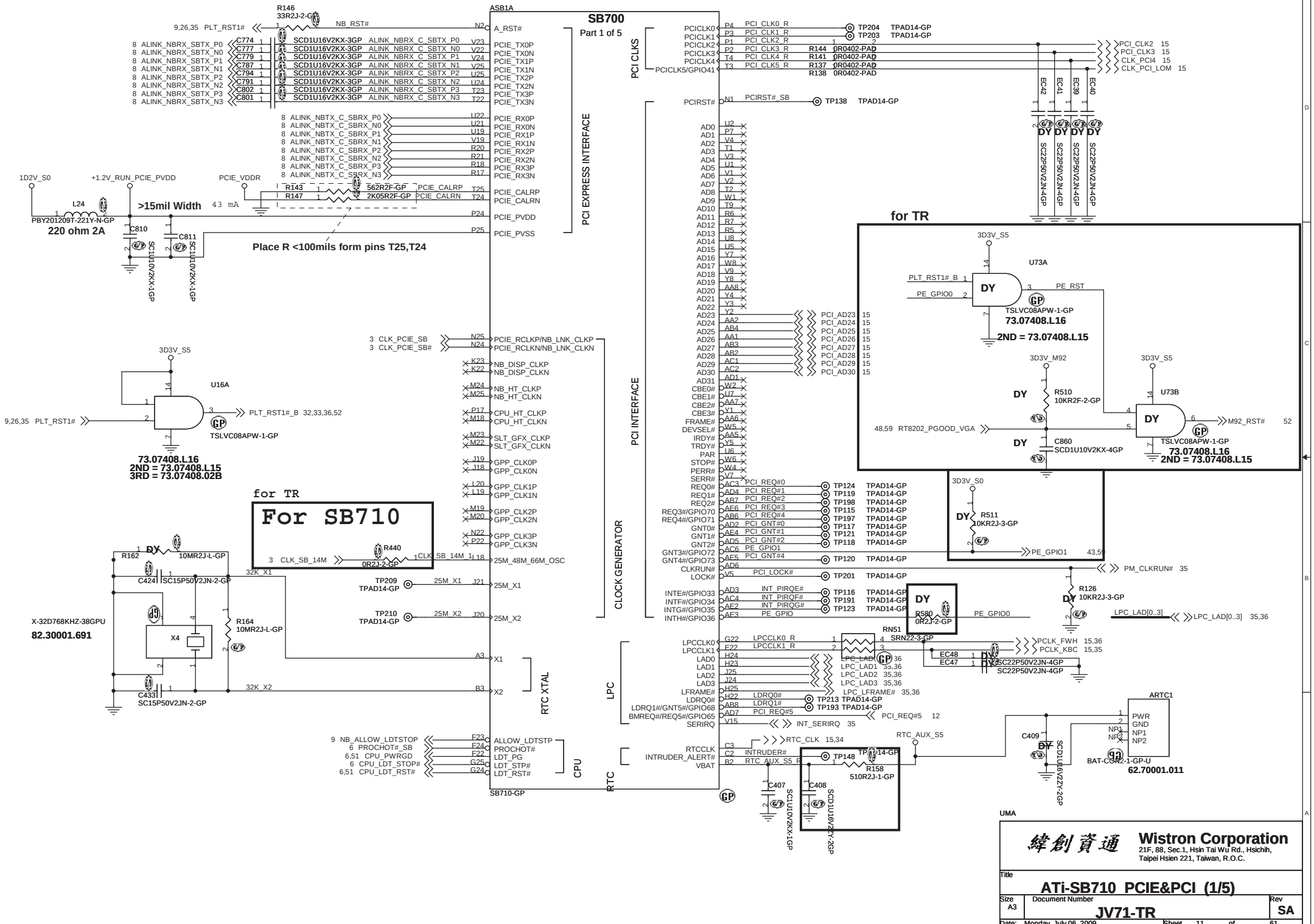
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

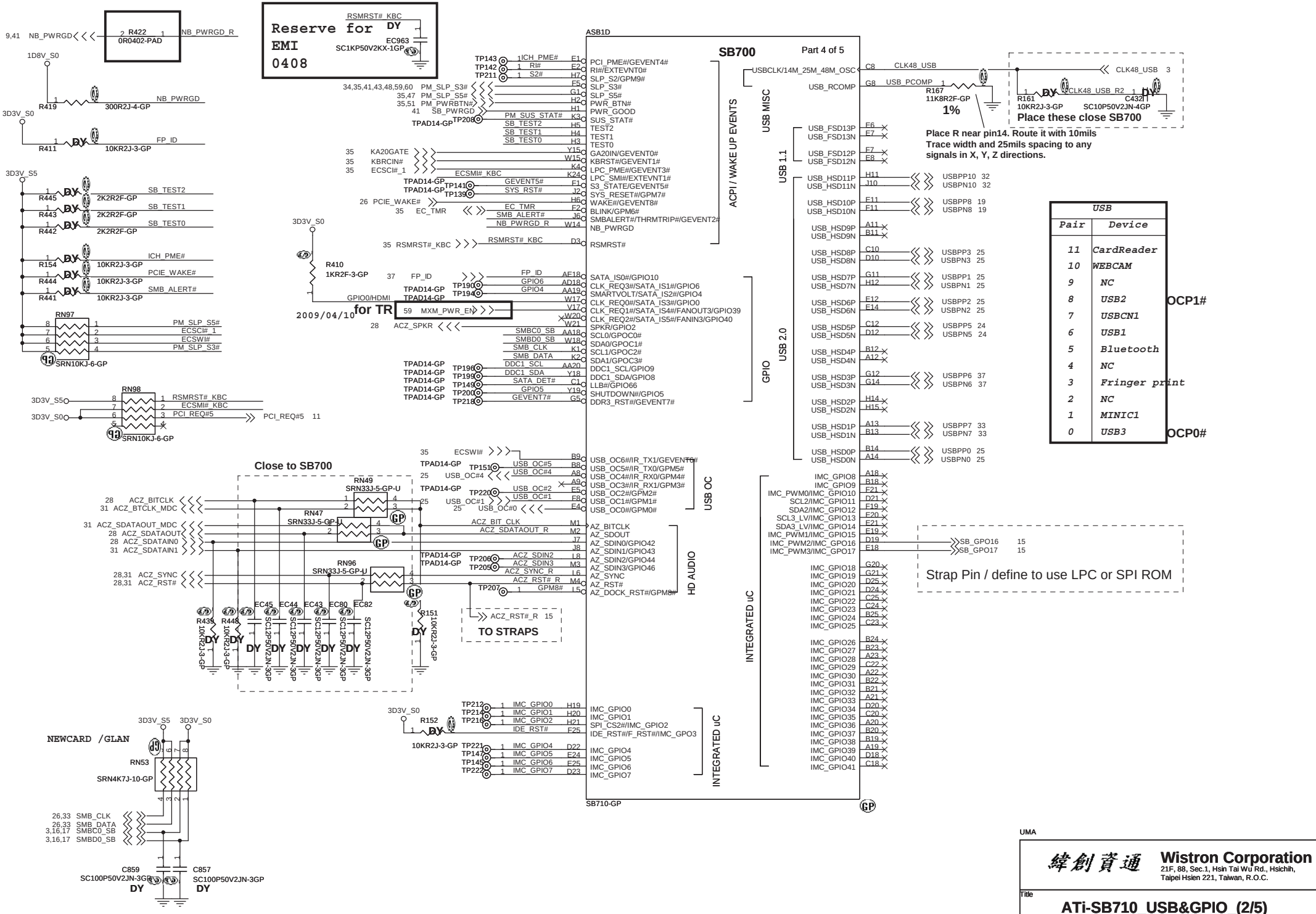
Title: ATi-RS880M LVDS&CRT (2/3)
Size: A3 | Document Number: JV71-TR | Rev: SA
Date: Monday, July 06, 2009 | Sheet 9 of 61



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**ATi-RS880M_Side Port&PWR&GND(3/3)**
Size: A3	Document Number: **JV71-TR**
Rev	**SA**
Date: Monday, July 06, 2009	Sheet 10 of 61


SB700
Part 1 of 5
ASB1A
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
SB710-GP
for TR
For SB710
for TR
U16A
U73A
U73B
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
>15mil Width
Place R <100mils form pins T25,T24
220 ohm 2A
X-32D768KHZ-38GPU
82.30001.691
62.70001.011
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-SB710 PCIE&PCI (1/5)
JV71-TR
Size A3
Rev SA
Date: Monday, July 06, 2009
Sheet 11 of 61


Reserve for EMI 0408
RSMRST# KBC
EC963 SC1KP50V2KX-1GP DY
ASB1D
SB700
Part 4 of 5
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#
SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
SB710-GP
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPIO16
IMC_PWM3/IMC_GPO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41
CLK48_USB
USB_PCOMP
R167 11K8R2F-GP 1%
Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.
CLK48_USB_R2
R161 10KR2J-3-GP DY
C432 SC10P50V2JN-4GP DY
Place these close SB700
USB
Pair | Device
11 CardReader
10 WEBCAM
9 NC
8 USB2 OCP1#
7 USBCN1
6 USB1
5 Bluetooth
4 NC
3 Fringer print
2 NC
1 MINIC1
0 USB3 OCP0#
Strap Pin / define to use LPC or SPI ROM
SB_GPO16
SB_GPO17
TO STRAPS
ACZ_RST#_R
Close to SB700
RN49 SRN33J-5-GP-U
RN47 SRN33J-5-GP-U
RN96 SRN33J-5-GP-U
EC45 EC44 EC43 EC80 EC82
R439 R448 R151 10KR2J-3-GP DY
SC12P50V2JN-3GP DY
R410 1KR2F-3-GP
2009/04/10 for TR
RN97 SRN10KJ-6-GP
RN98 SRN10KJ-6-GP
R419 300R2J-4-GP
R411 10KR2J-3-GP
R445 R443 R442 2K2R2F-GP
R154 R444 R441 10KR2J-3-GP
R152 10KR2J-3-GP DY
NEWCARD /GLAN
RN53 SRN4K7J-10-GP
C859 SC100P50V2JN-3GP DY
C857 SC100P50V2JN-3GP DY
UMA
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB710 USB&GPIO (2/5)
Size A3
Document Number JV71-TR
Rev SA
Date: Monday, July 06, 2009
Sheet 12 of 61

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700

SATA HDD
SATA ODD

SB700
Part 2 of 5

SERIAL ATA
ATA 66/100/133
SPI ROM
HW MONITOR
SATA PWR

Very Close to SB700

XTAL-25MHZ-96GP
82.30020.791
2ND = 82.30020.851

Dummy CKG select

CLK_ID (1,0)
ICS: 0,0
SEG: 0,1
RTM: 1,0

2009/04/09 ALL DY

Layout connect to Cap then GND

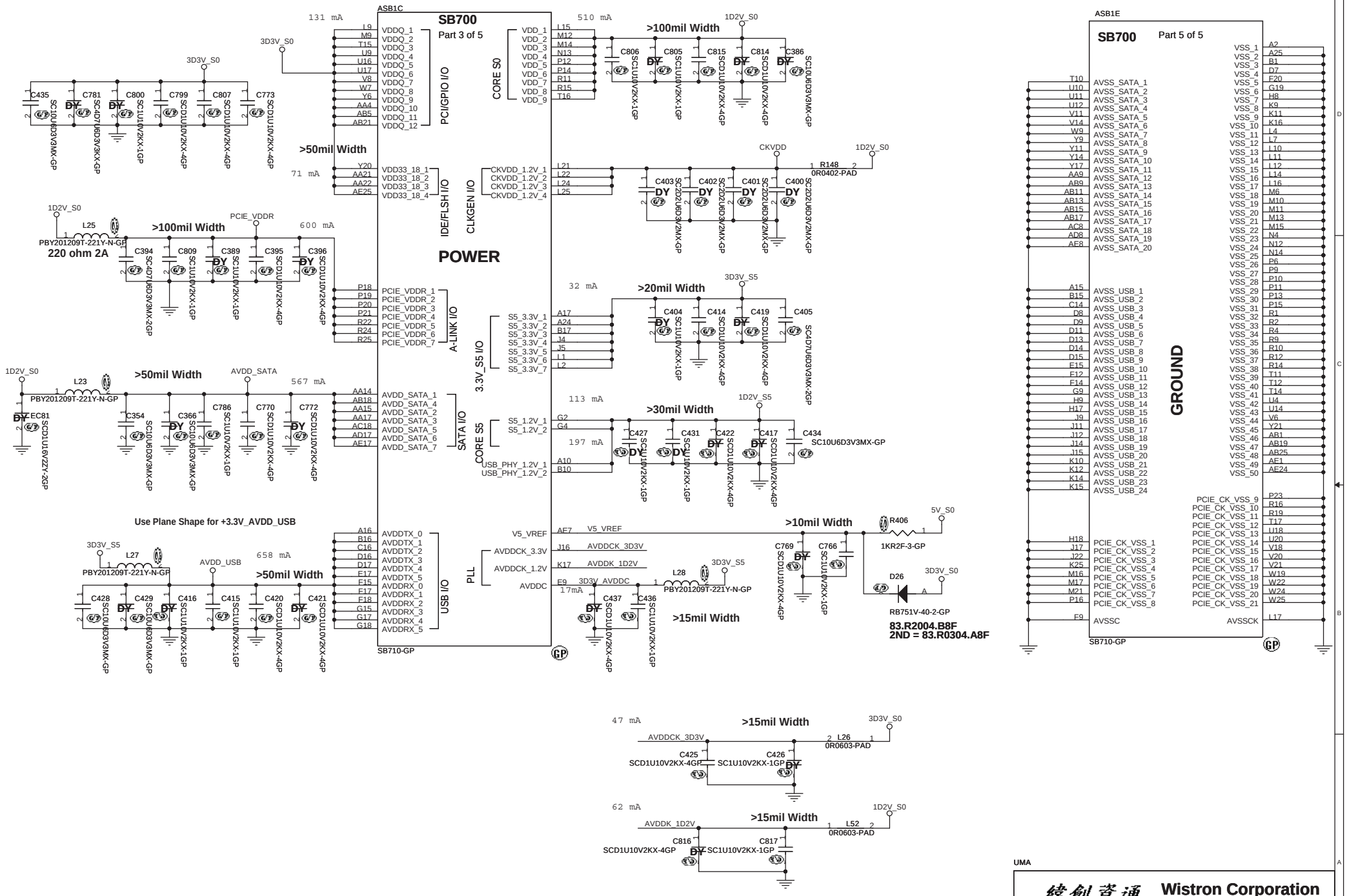
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB710 SATA-IDE (3/5)

Size: A3 | Document Number: JV71-TR | Rev: SB

Date: Monday, July 06, 2009 | Sheet 13 of 61

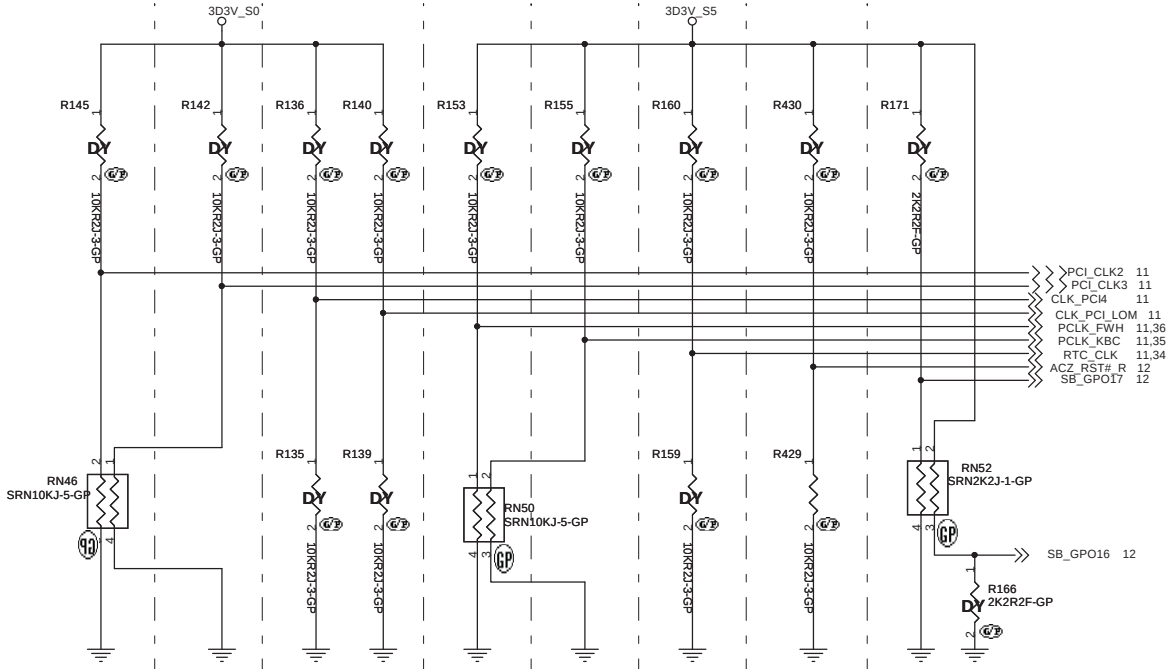


UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**ATi-SB710 POWER&GND (4/5)**
Size: A3	Document Number: JV71-TR
Rev: SB	
Date: Monday, July 06, 2009	Sheet 14 of 61

REQUIRED STRAPS

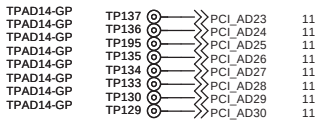
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16 ROM TYPE:
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	H, H = Reserved H, L = SPI ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM DEFAULT L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

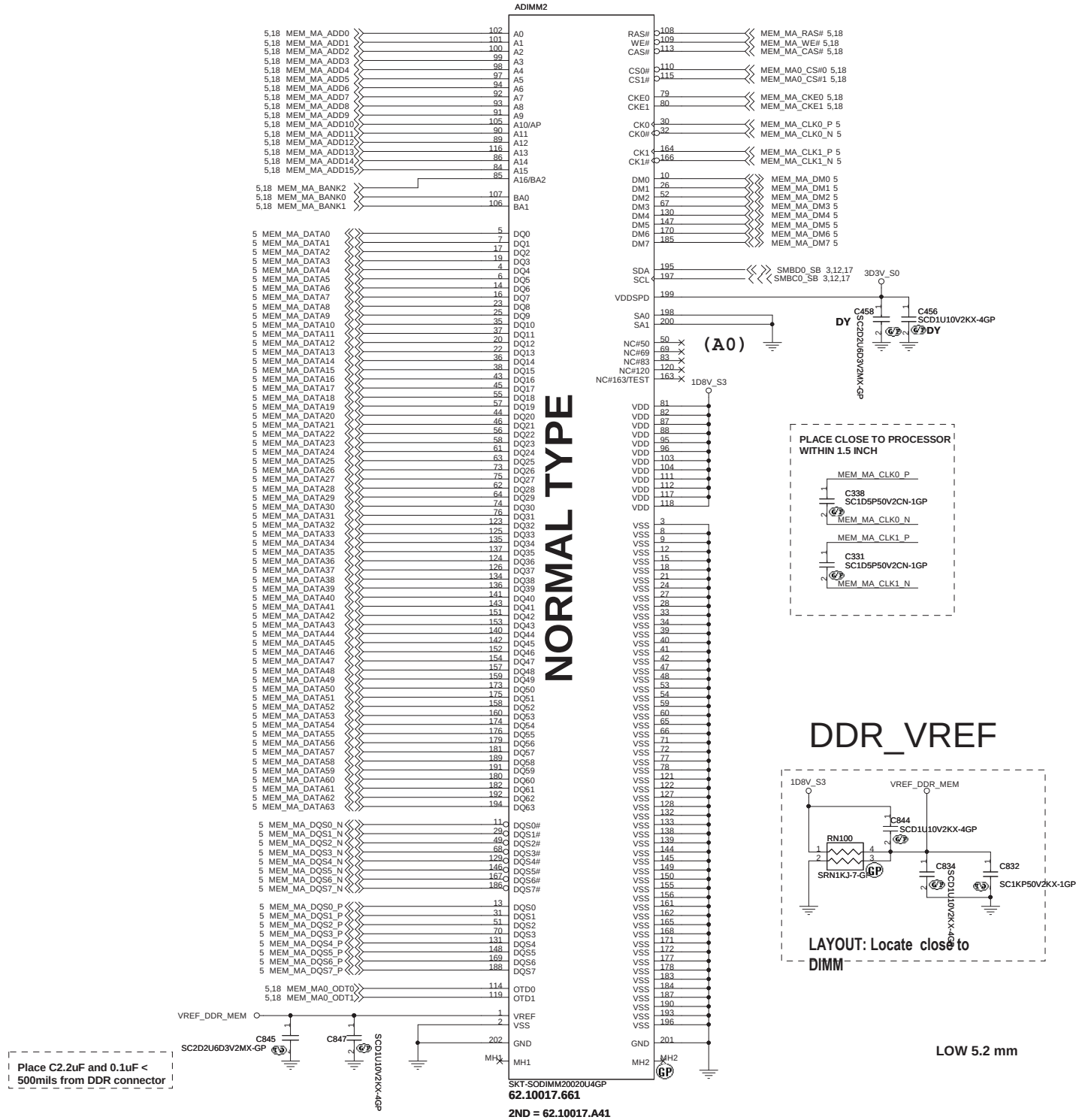
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATi-SB710 STRAPPING (5/5)**

Size	Document Number	Rev
A3	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 15 of 61



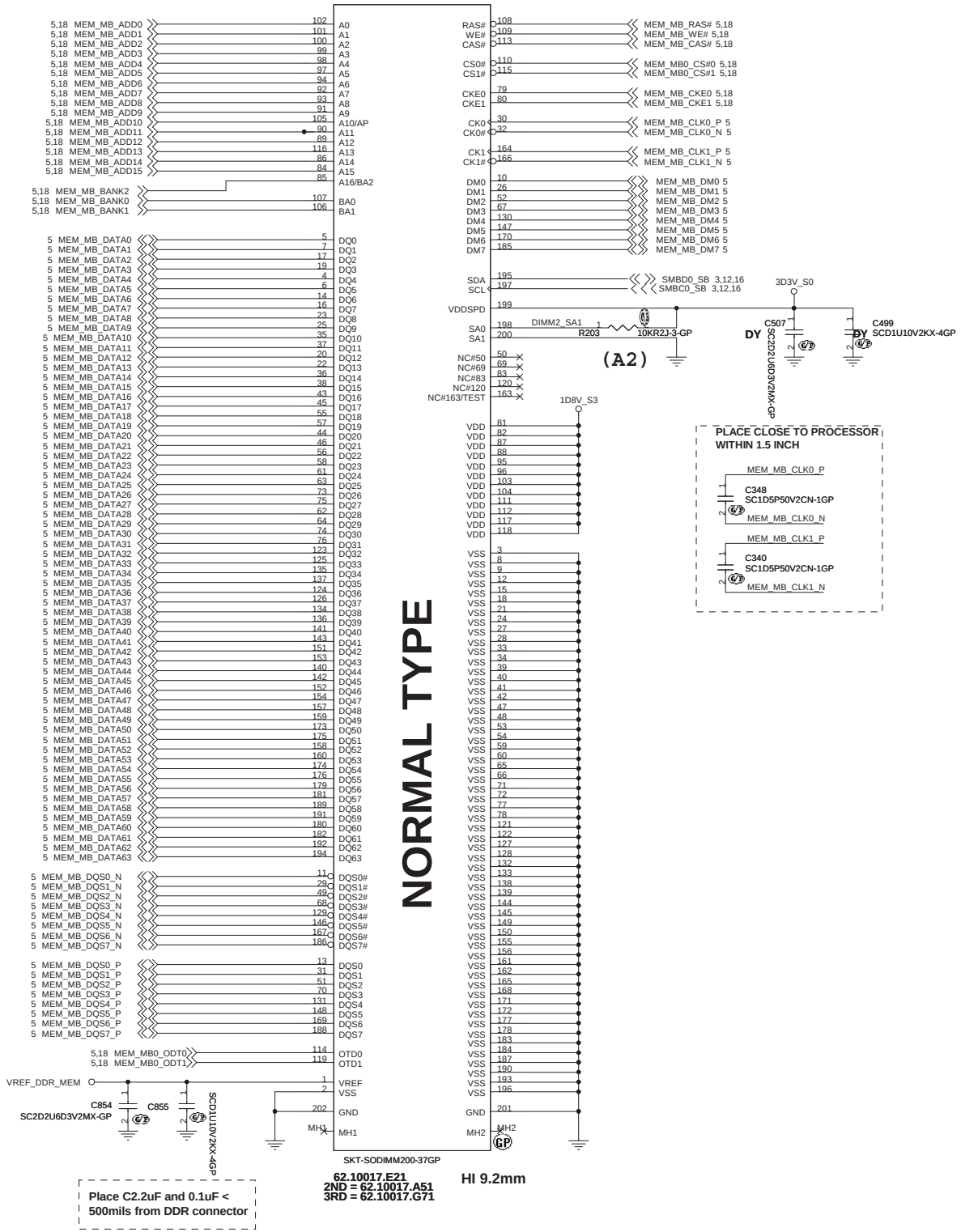
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_1

Size	Document Number	Rev
Custom	JV71-TR	SB

Date: Monday, July 06, 2009 Sheet 16 of 61

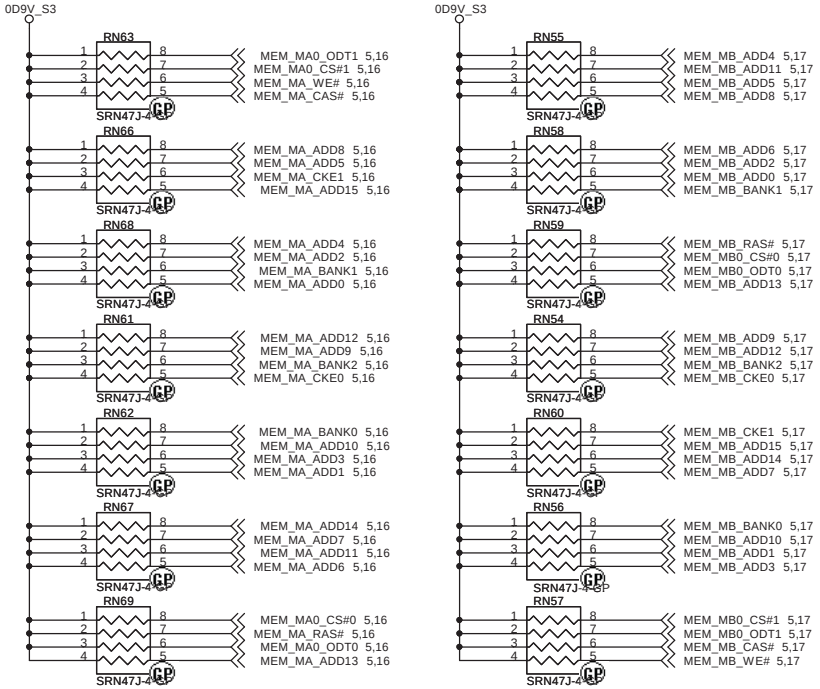


UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**DDR_SO-DIMM SKT_2**	
Size: Custom	Document Number: **JV71-TR**	Rev: **SB**
Date: Monday, July 06, 2009	Sheet 17 of 61	

PARALLEL TERMINATION

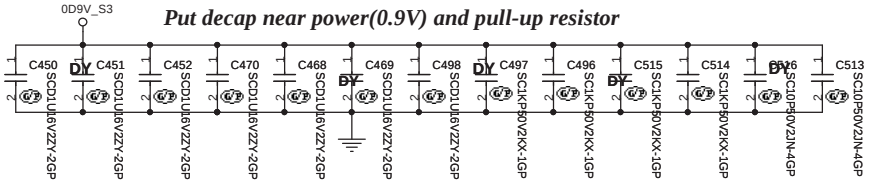
Put decap near power(0.9V) and pull-up resistor



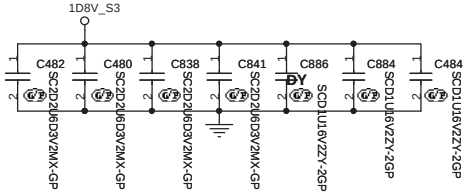
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

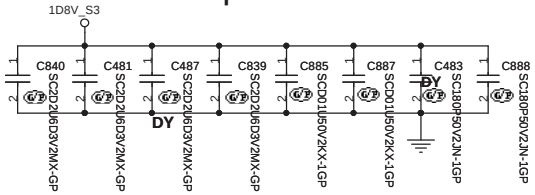


Place these Caps near DM1



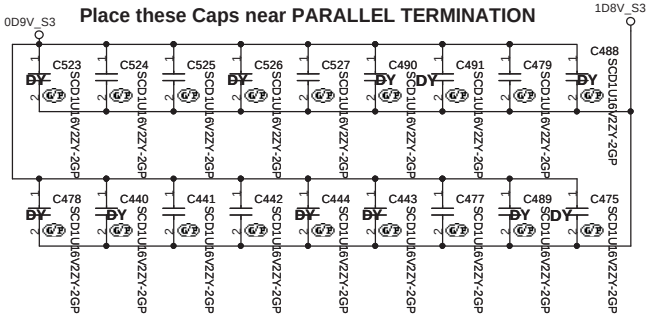
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



UMA

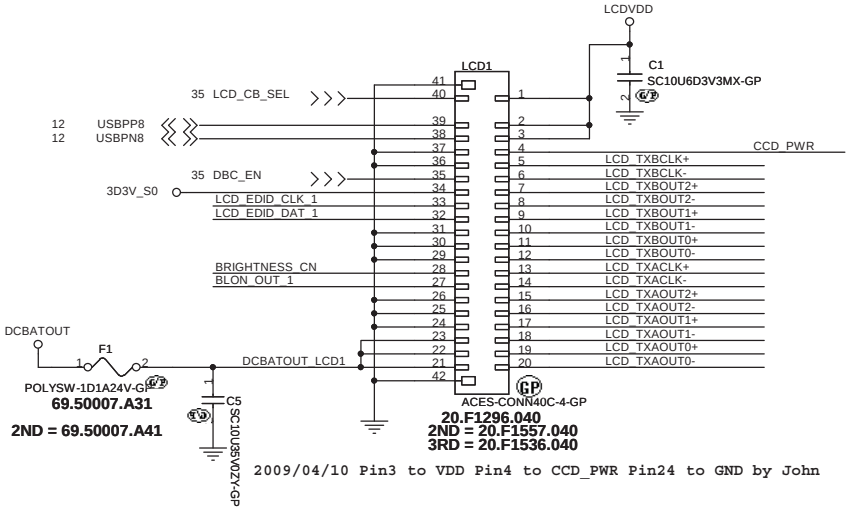
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR_DAMPING & TERMINATION**

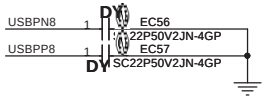
Size	Document Number	Rev
A3	JV71-TR	SB

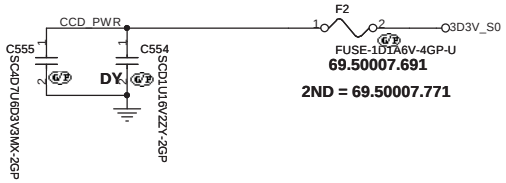
Date: Monday, July 06, 2009 Sheet 18 of 61

LCD/INVERTER/CCD CONN

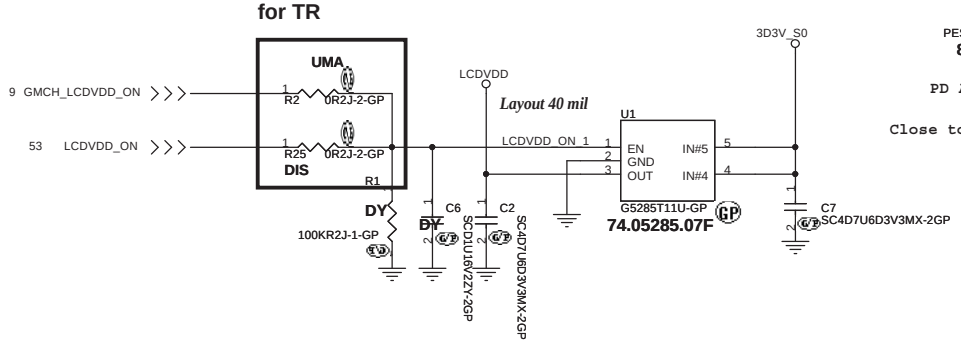


2009/04/10 Pin3 to VDD Pin4 to CCD_PWR Pin24 to GND by John

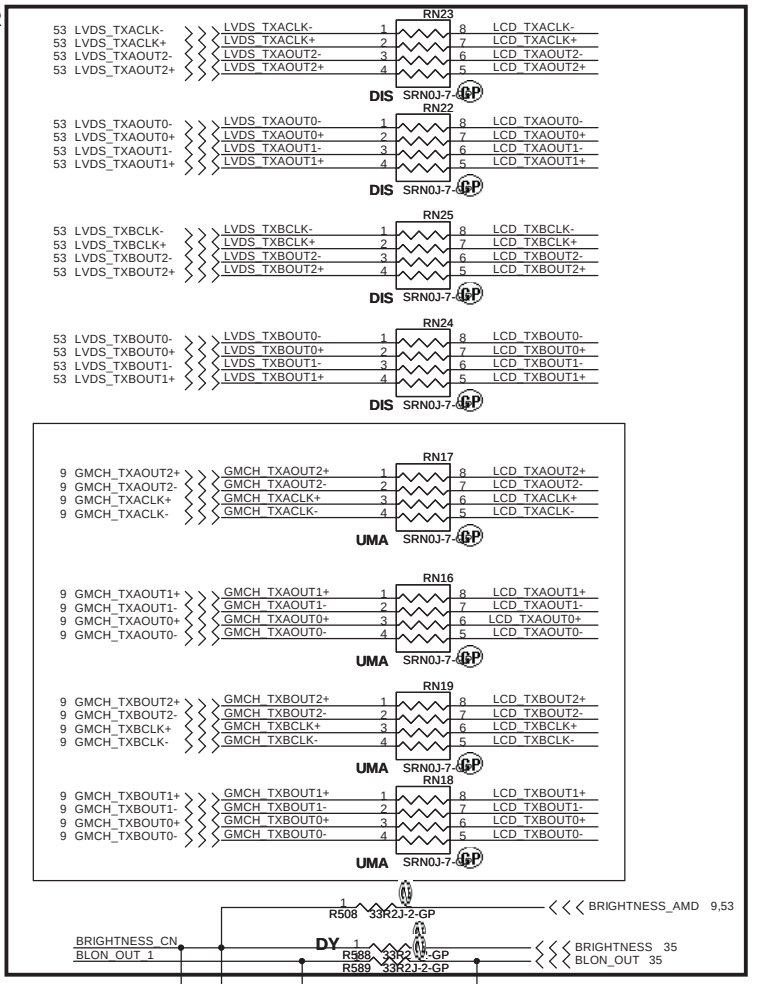


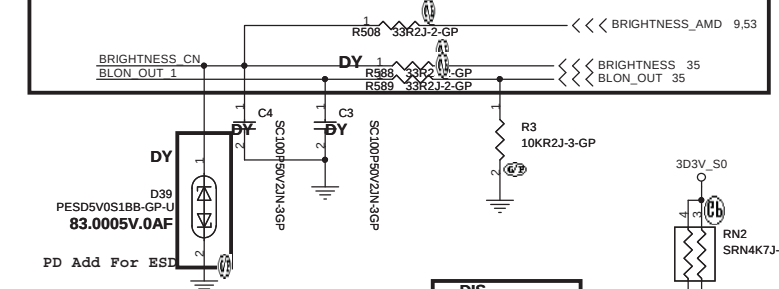


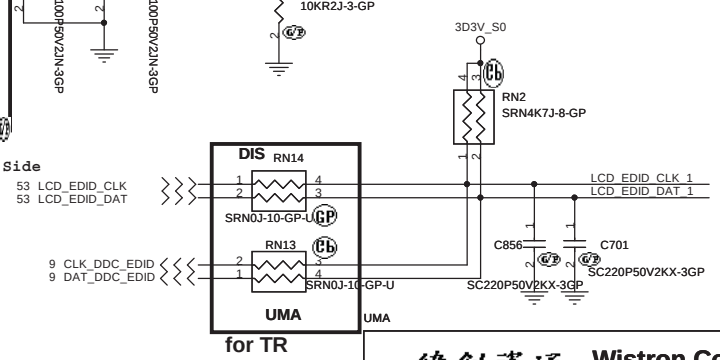
for TR



for TR







Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

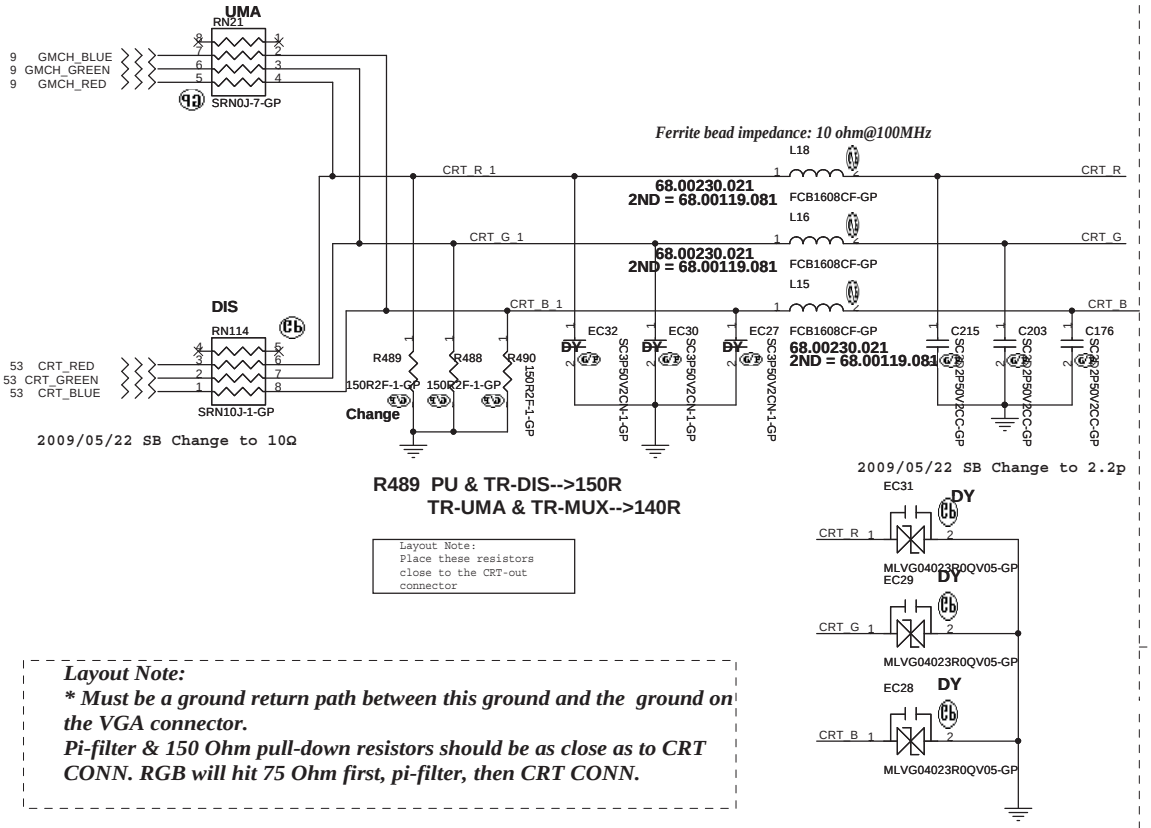
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

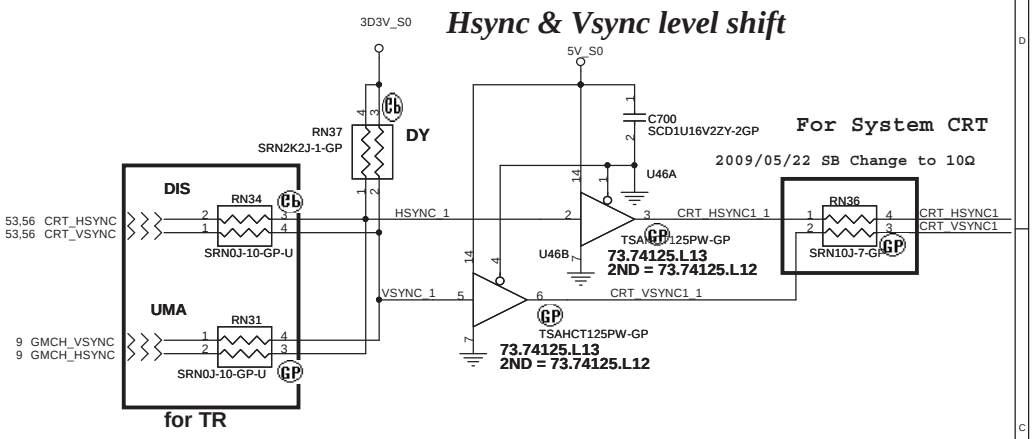
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

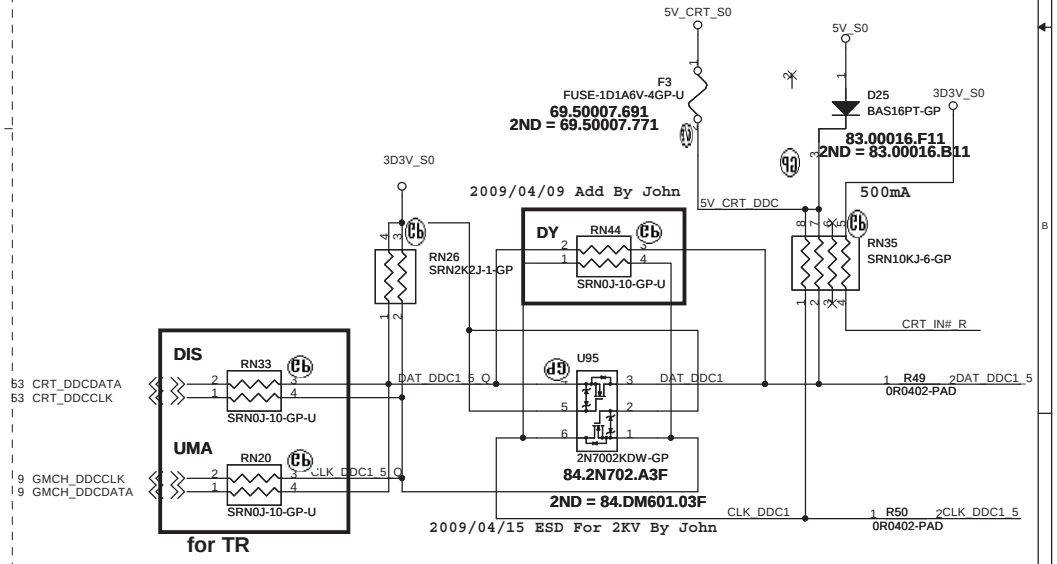
Title: **LCD CONN**

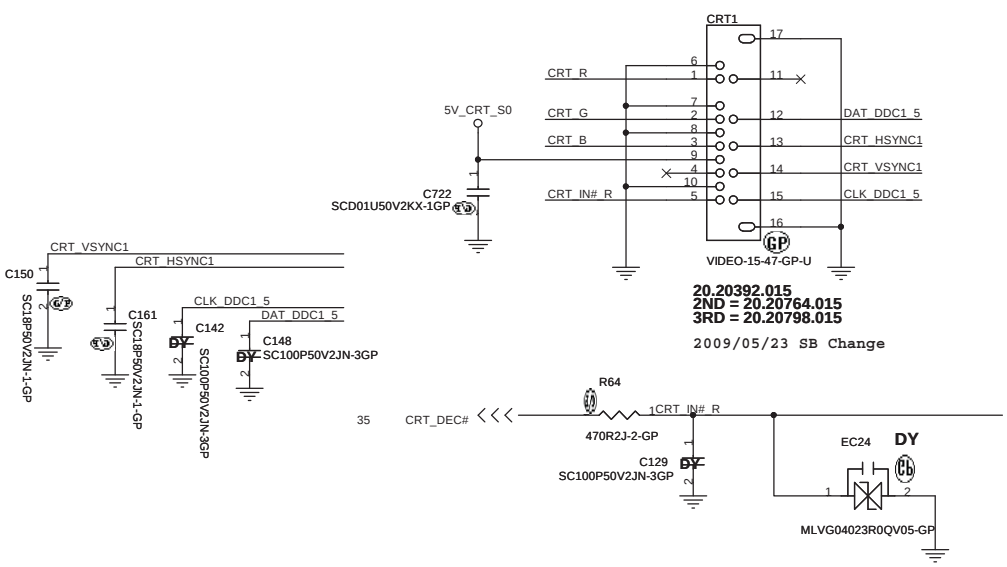
Size	Document Number	Rev
A3	JV71-TR	-1

Date: Monday, July 06, 2009 Sheet 19 of 61



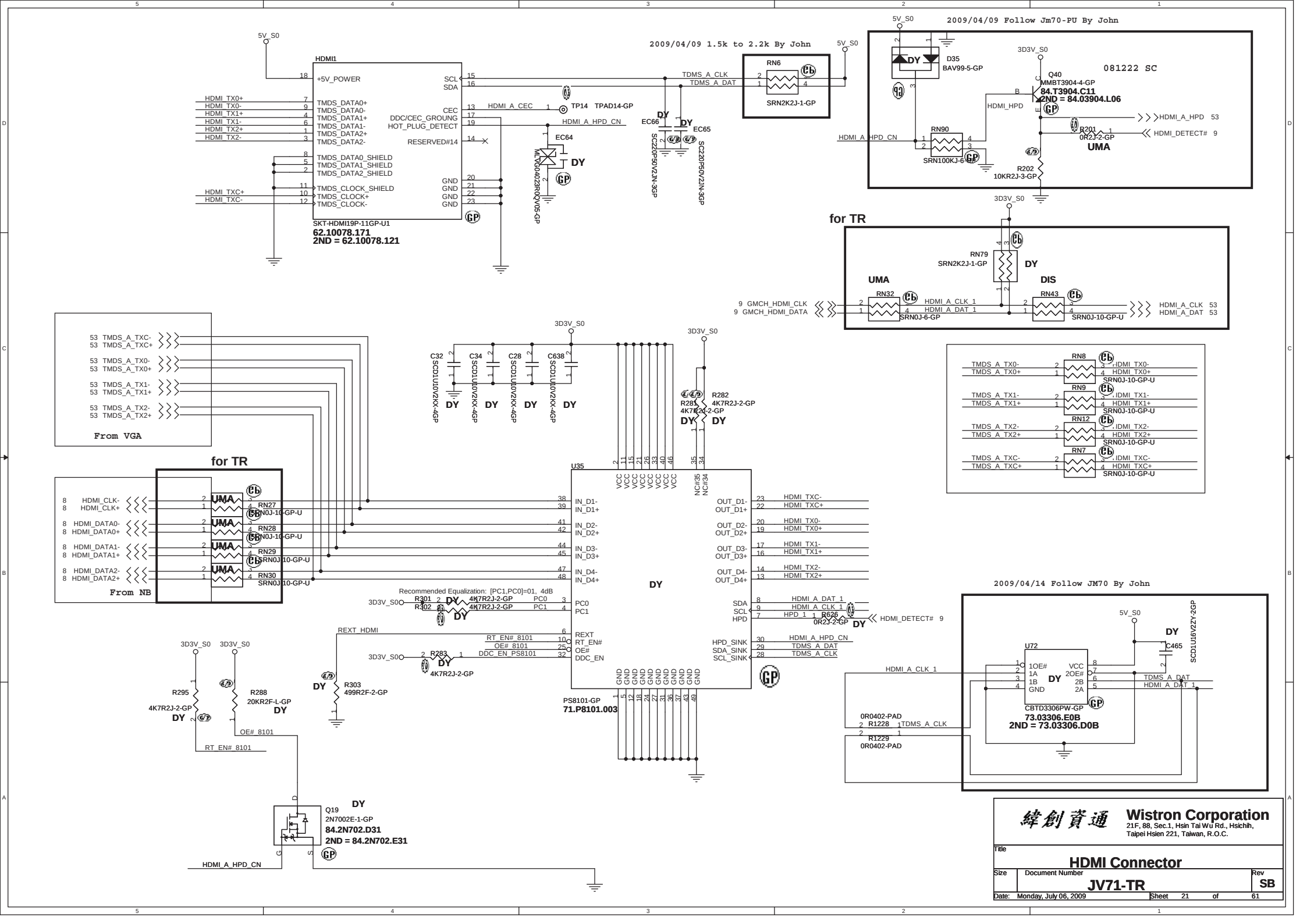




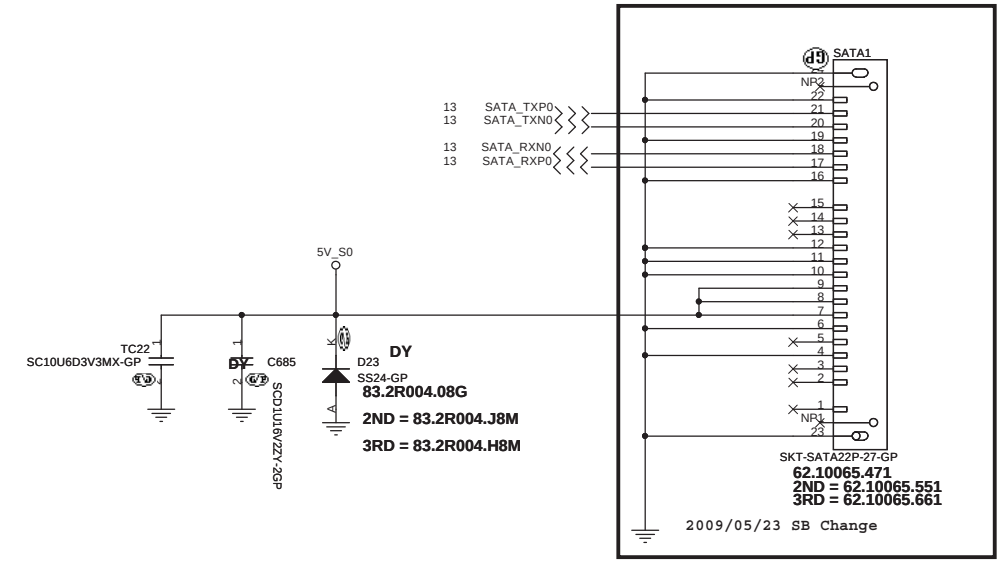


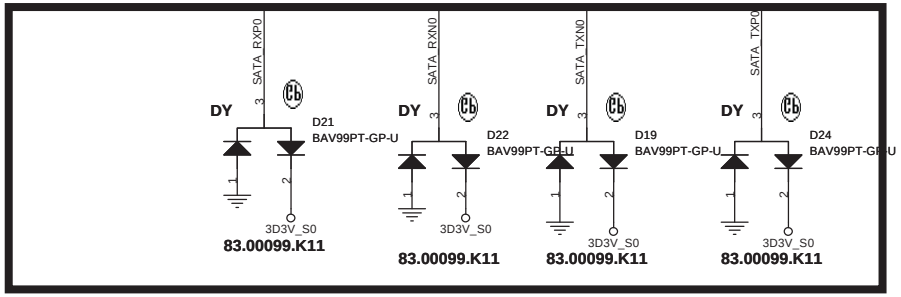
UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CRT Connector**	
Size	Document Number **JV71-TR**	Rev **SB**
Date: Monday, July 06, 2009	Sheet 20 of 61	


2009/04/09 1.5k to 2.2k By John
2009/04/09 Follow Jm70-PU By John
081222 SC
HDMI1
SKT-HDMI19P-11GP-U1
62.10078.171
2ND = 62.10078.121
RN6
SRN2K2J-1-GP
D35
BAV99-5-GP
Q40
MMBT3904-4-GP
84.T3904.C11
2ND = 84.03904.L06
RN90
SRN100KJ-6-GP
R201
0R2J-2-GP
UMA
R202
10KR2J-3-GP
for TR
RN79
SRN2K2J-1-GP
DY
UMA
DIS
RN32
RN43
SRN0J-6-GP
SRN0J-10-GP-U
From VGA
From NB
RN8
RN9
RN12
RN7
U35
PS8101-GP
71.P8101.003
Recommended Equalization: [PC1,PC0]=01, 4dB
2009/04/14 Follow JM70 By John
U72
CBTD3306PW-GP
73.03306.E0B
2ND = 73.03306.D0B
Q19
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI Connector
Size
Document Number
JV71-TR
Rev
SB
Date: Monday, July 06, 2009
Sheet 21 of 61

SATA Connector

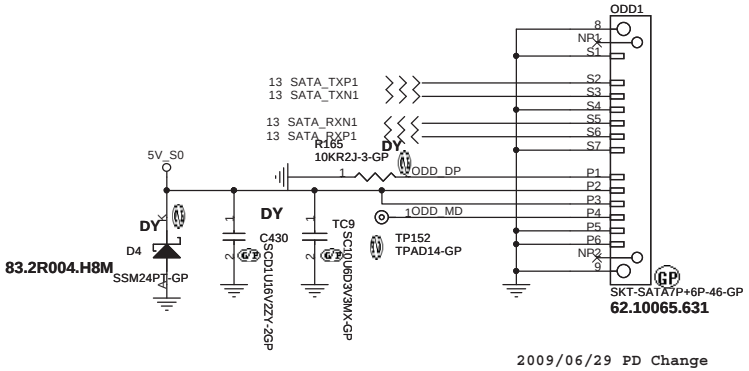


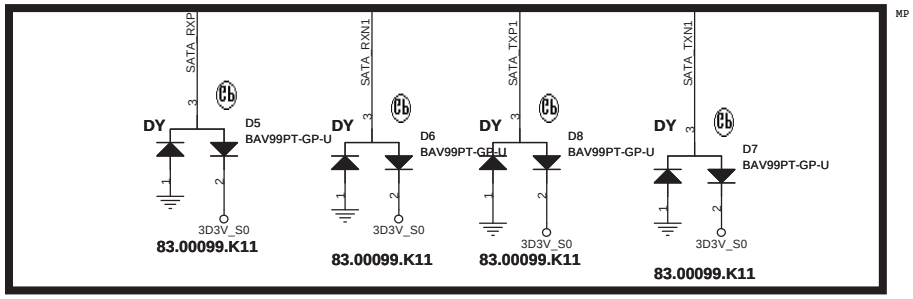


UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD		
Size	Document Number: JV71-TR	Rev: SB
Date: Monday, July 06, 2009	Sheet 22 of 61	

SATA ODD Connector



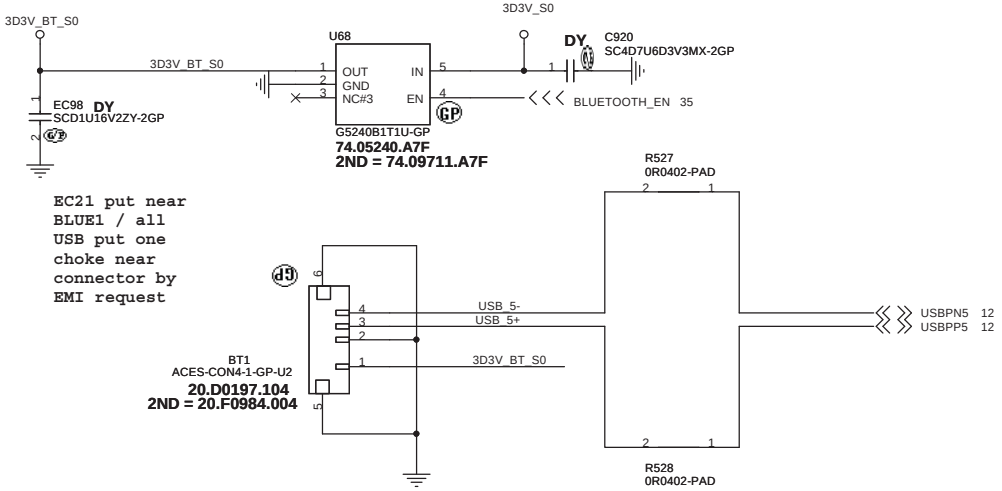


UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ODD		
Size	Document Number: JV71-TR	Rev: SB
Date: Monday, July 06, 2009	Sheet 23 of 61	

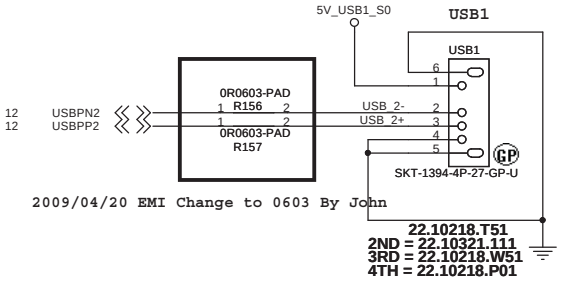
BLUETOOTH MODULE

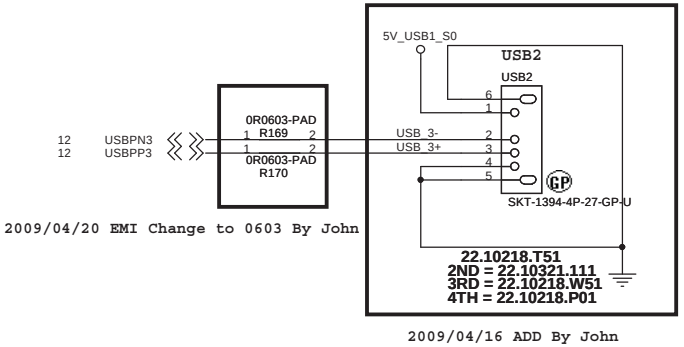
1.5A / High Active Voltage 2V

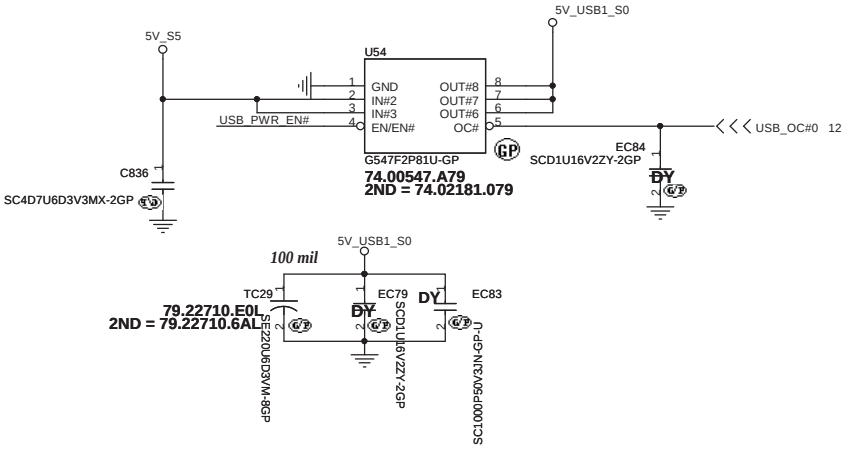


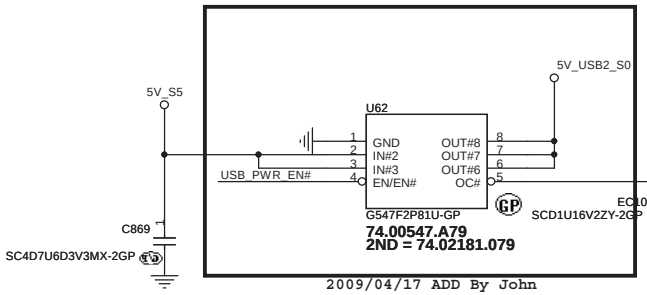
UMA

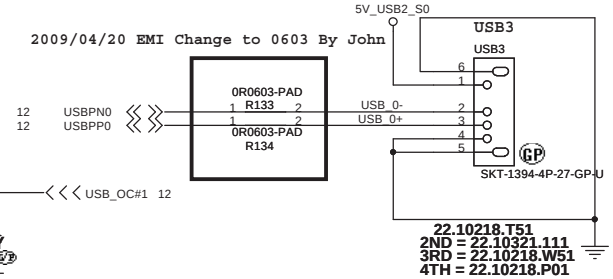
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BLUETOOTH		
Size	Document Number: JV71-TR	Rev: SA
Date: Monday, July 06, 2009	Sheet 24 of 61	

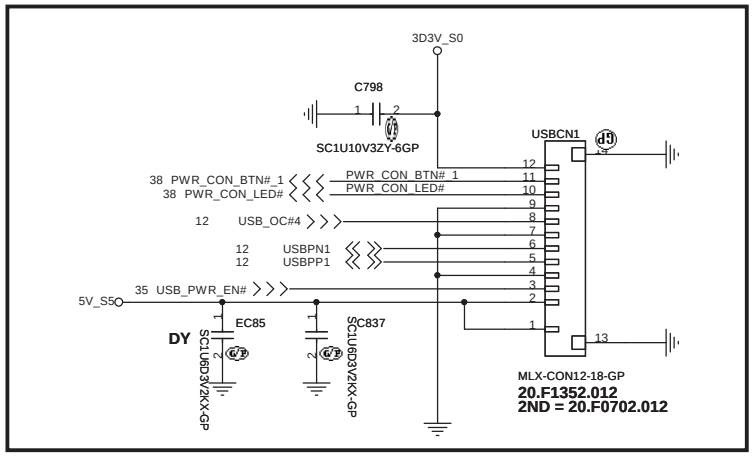


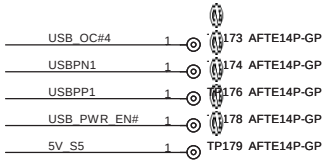


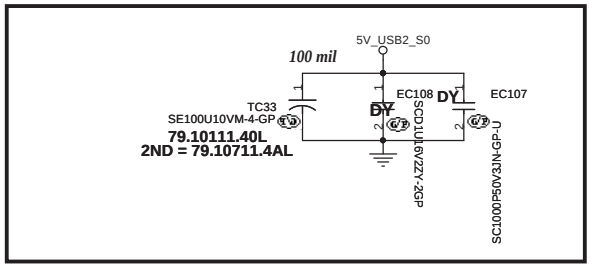












UMA

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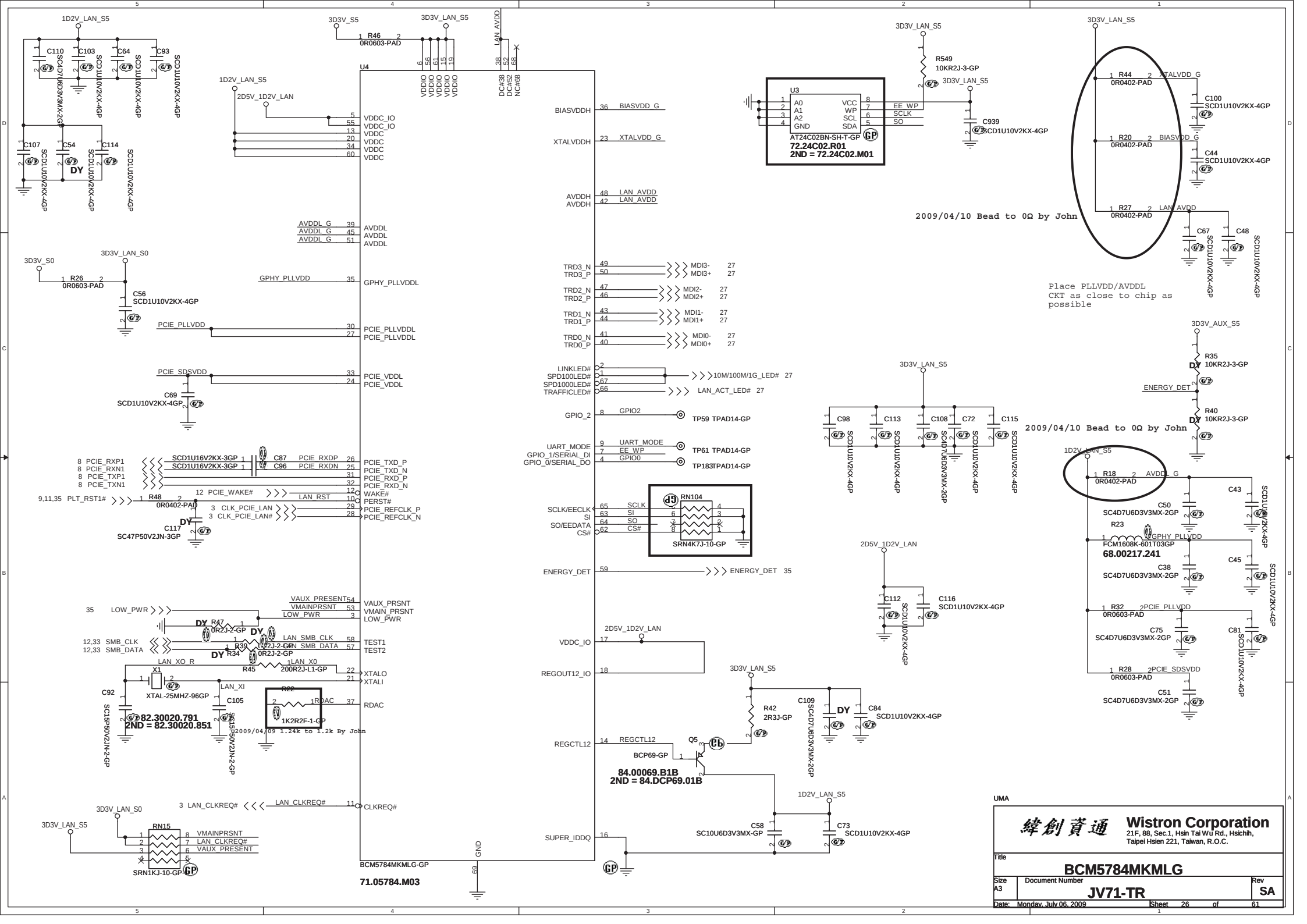
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB	
Size	Document Number: JV71-TR	Rev: SA
Date: Monday, July 06, 2009	Sheet 25 of 61	


U4
BCM5784MKMLG-GP
71.05784.M03
2009/04/10 Bead to 0Ω by John
Place PLLVDD/AVDDL CKT as close to chip as possible
2009/04/10 Bead to 0Ω by John
82.30020.791
2ND = 82.30020.851
2009/04/09 1.24k to 1.2k By John
84.00069.B1B
2ND = 84.DCP69.01B
U3
AT24C02BN-SH-T-GP
72.24C02.R01
2ND = 72.24C02.M01
RN104
SRN4K7J-10-GP
RN15
SRN1KJ-10-GP
UMA
緯創資通
Wistron Corporation
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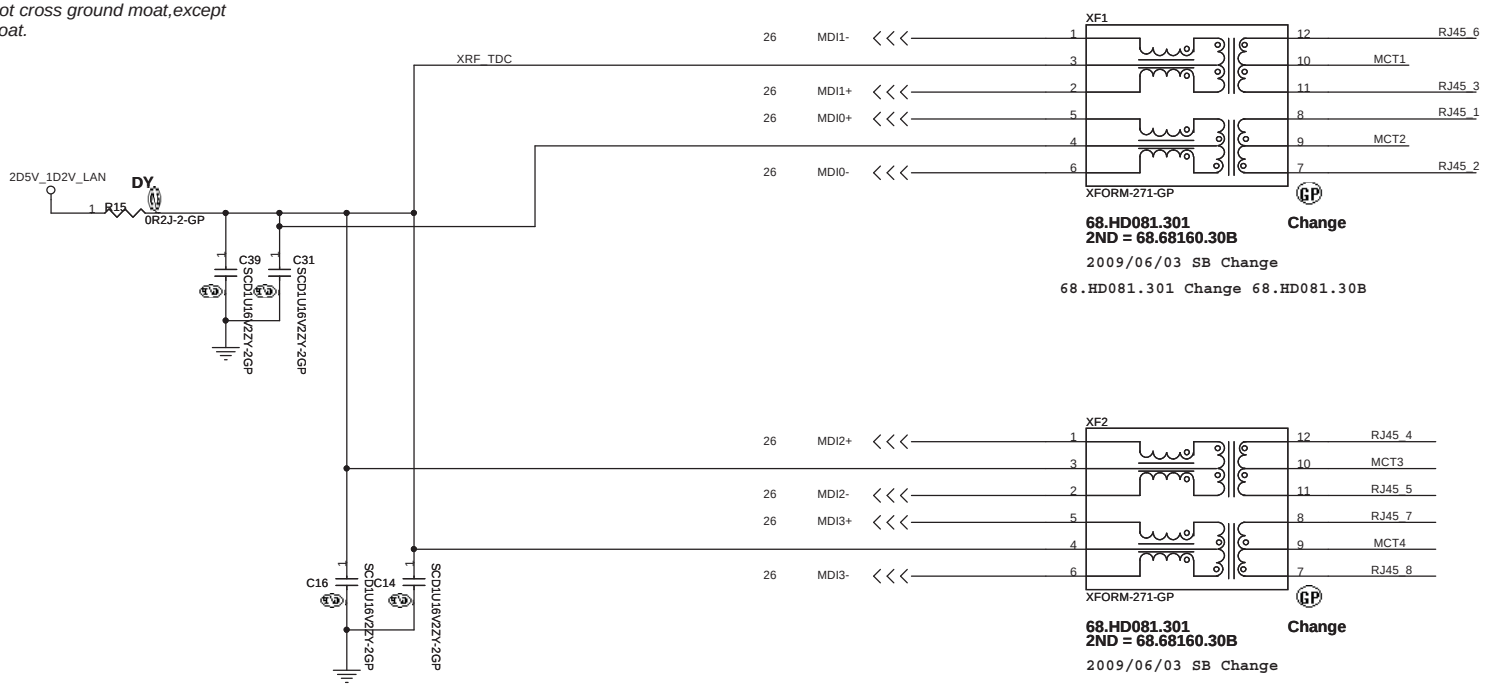
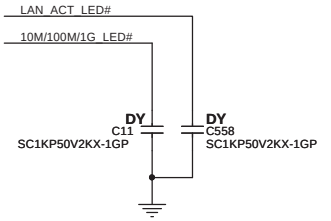
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5784MKMLG
Size A3
Document Number JV71-TR
Rev SA
Date: Monday, July 06, 2009
Sheet 26 of 61

LAN Connector

GIGA Lan Transformer

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

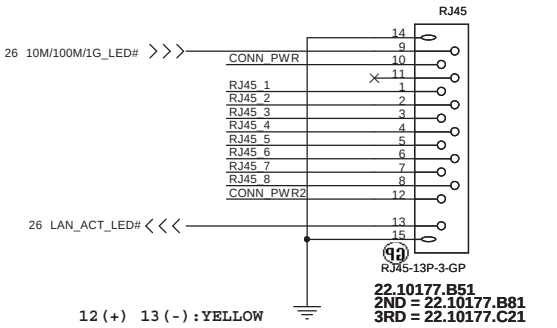




DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

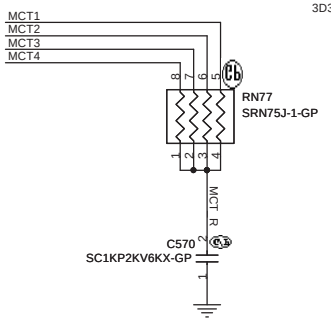
10(+) 9(-)::GREEN
10(+) 11(-):ORANGE

LAN Connector



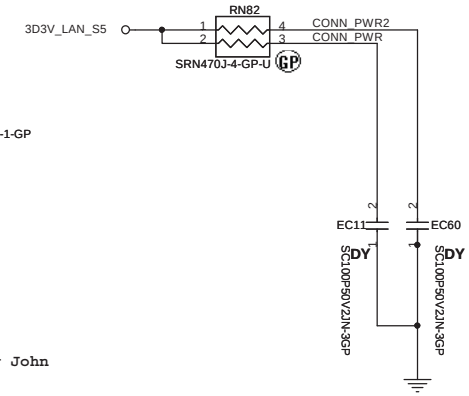
12(+) 13(-):YELLOW

2009/05/23 SB Change



2009/04/09 Follow JV70-PU By John

2009/04/09 Change 4P2R By John



UMA

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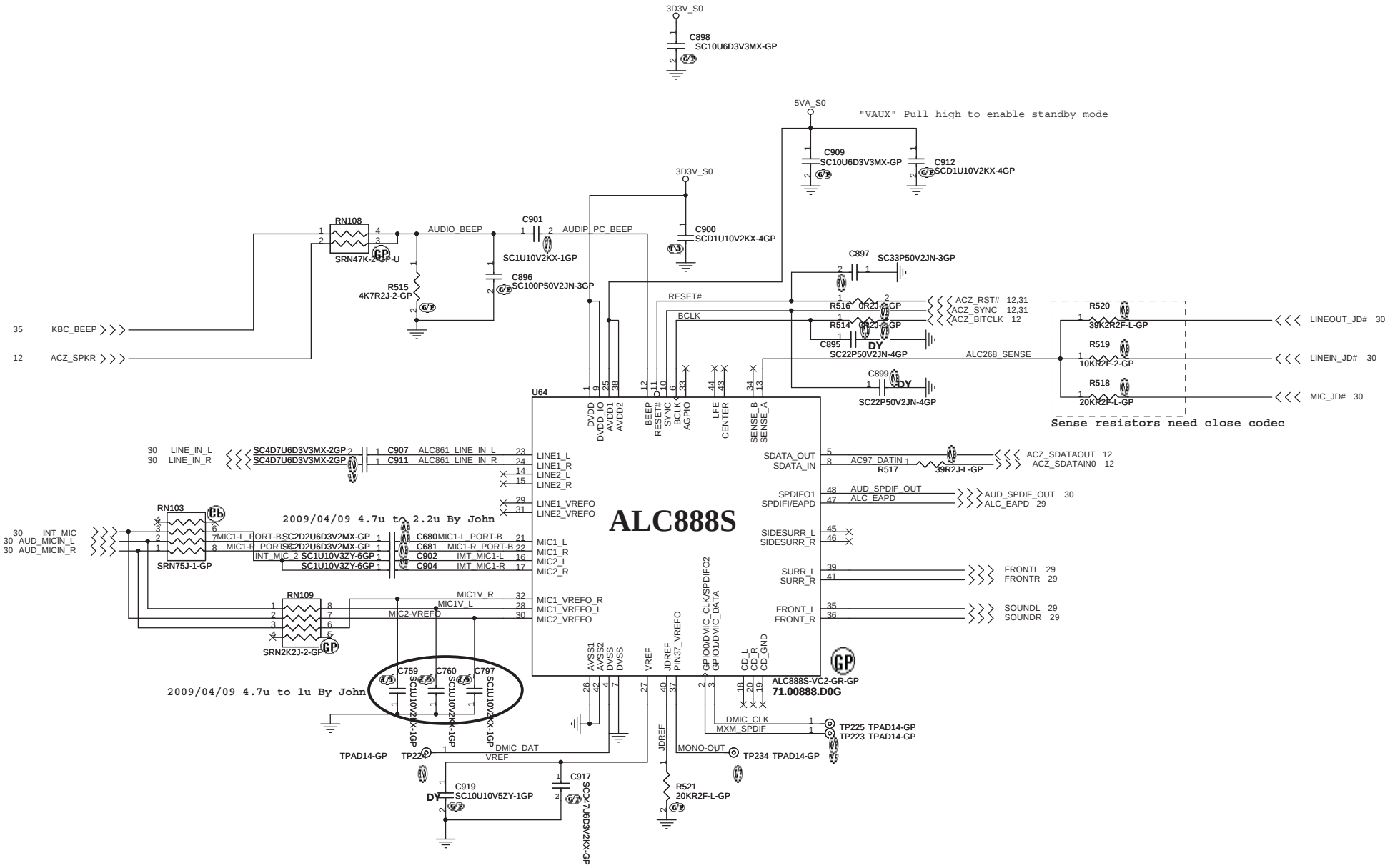
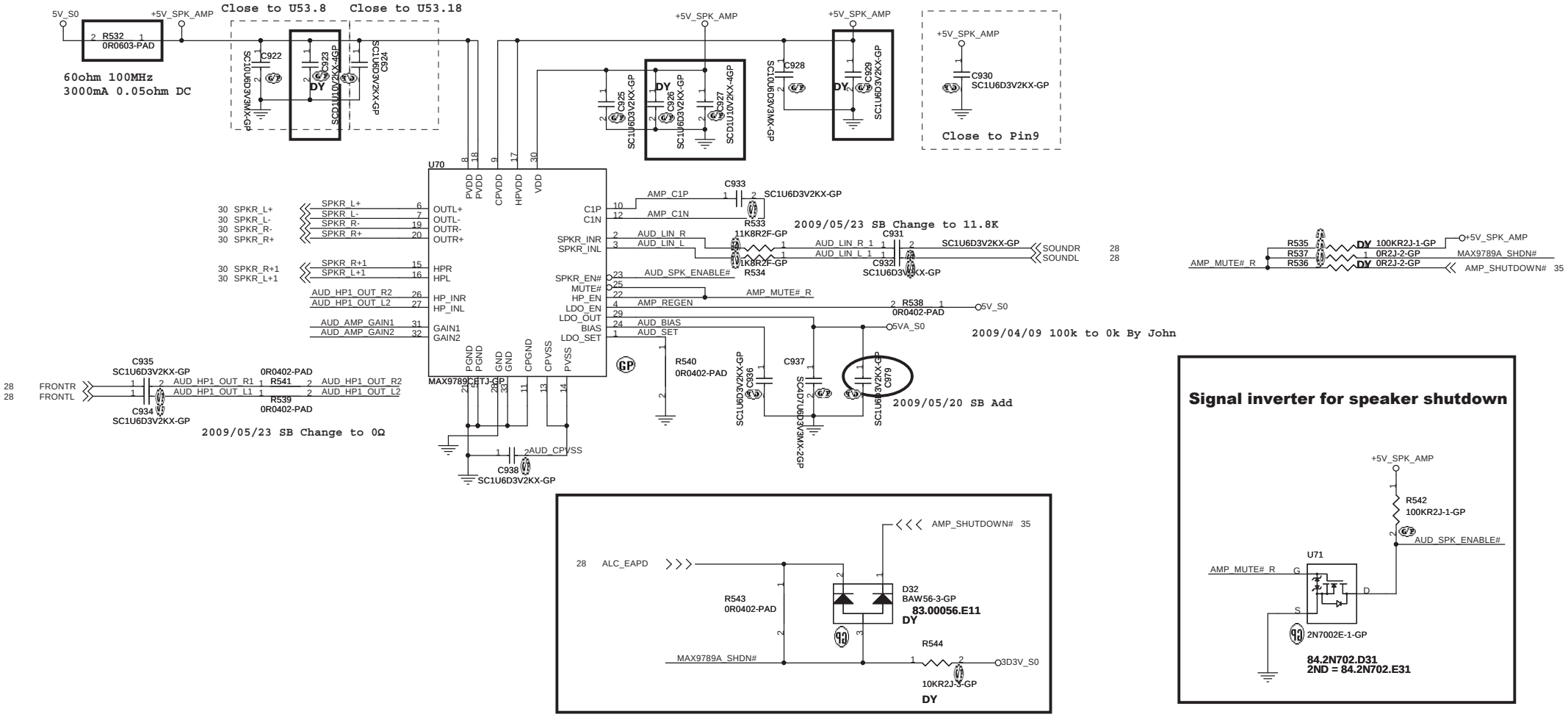
Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN CONN	
Size A3	Document Number JV71-TR	Rev SB
Date: Friday, July 10, 2009	Sheet 27 of 61	



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Azalia codec ALC888**	
Size A3	Document Number **JV71-TR**	Rev **SB**
Date: Monday, July 06, 2009	Sheet 28 of 61	



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

UMA

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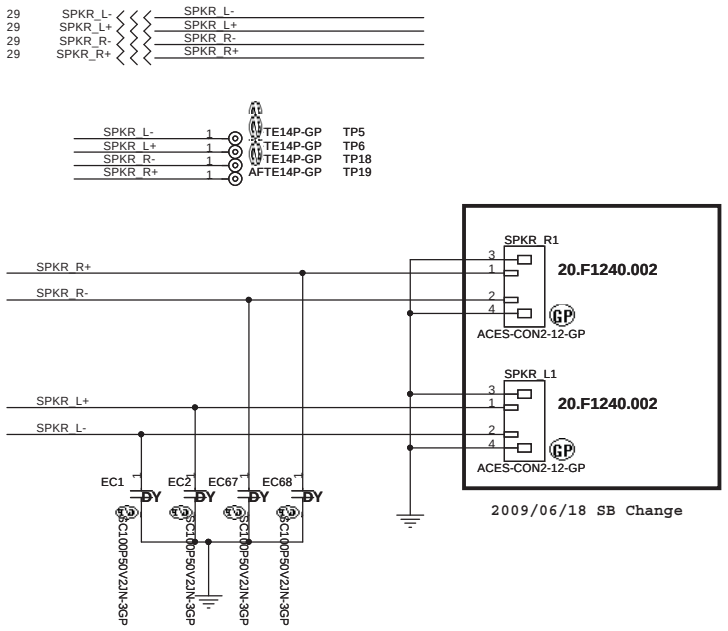
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP**

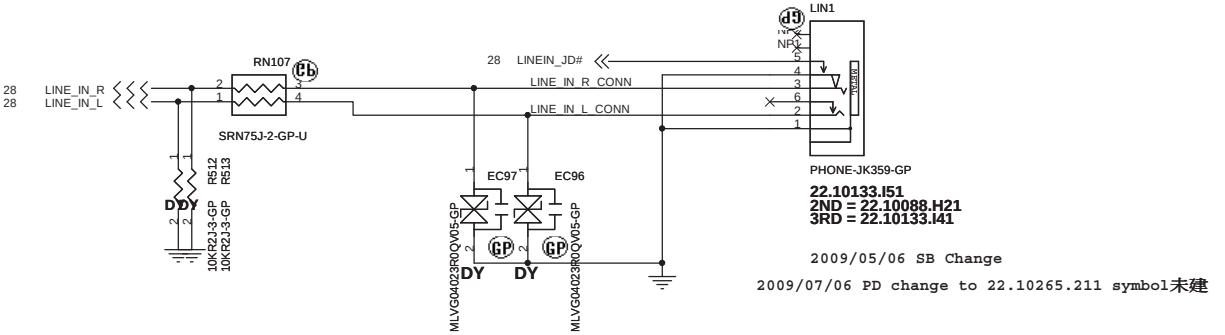
Size	Document Number	Rev
	JV71-TR	SB

Date: Monday, July 06, 2009 Sheet 29 of 61

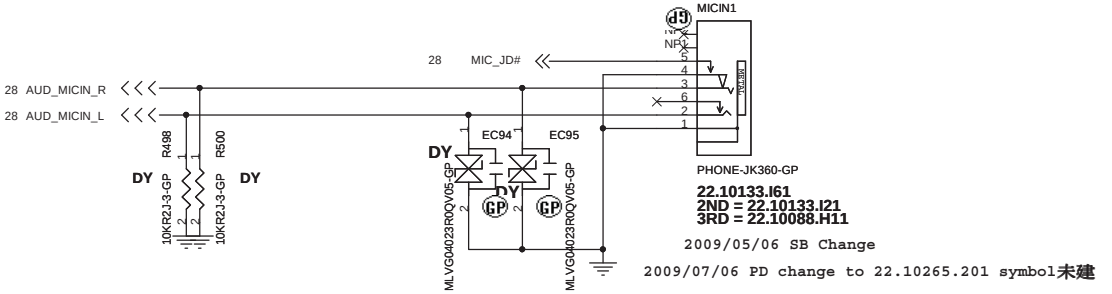
Internal Speaker



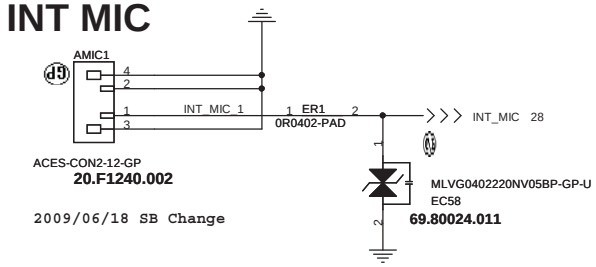
LINE IN



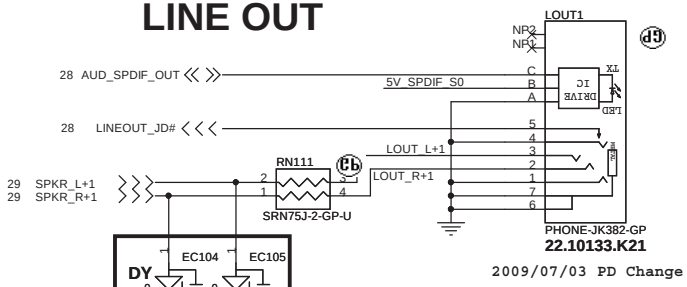
MIC IN

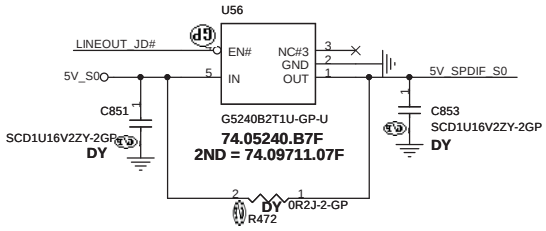


INT MIC



LINE OUT





UMA

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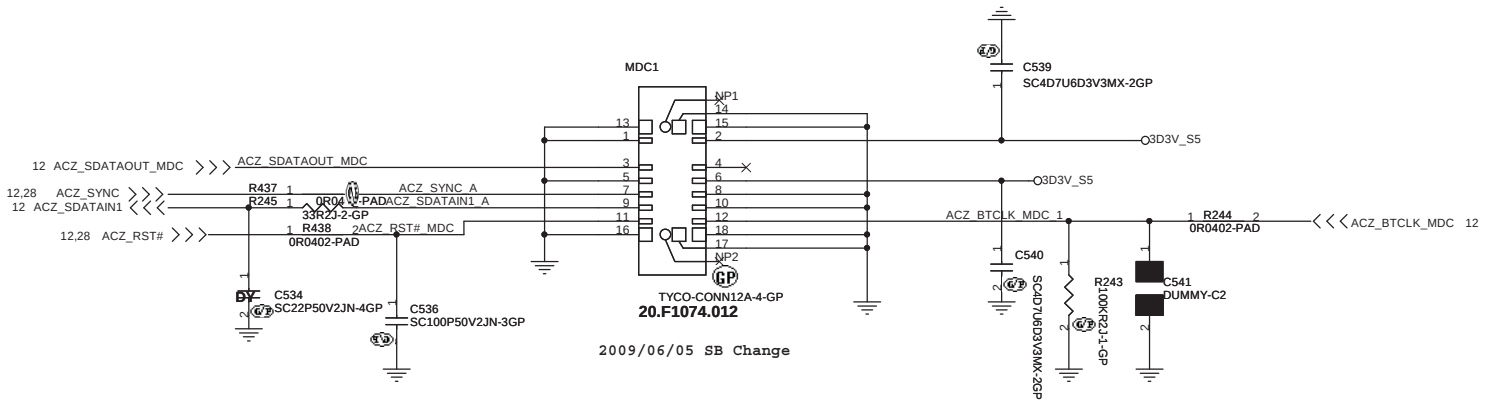
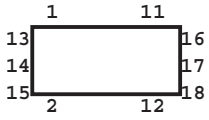
Title		
AUDIO JACK		
Size	Document Number	Rev
	JV71-TR	SB
Date: Monday, July 06, 2009	Sheet 30 of 61	

MDC 1.5 CONN





UMA

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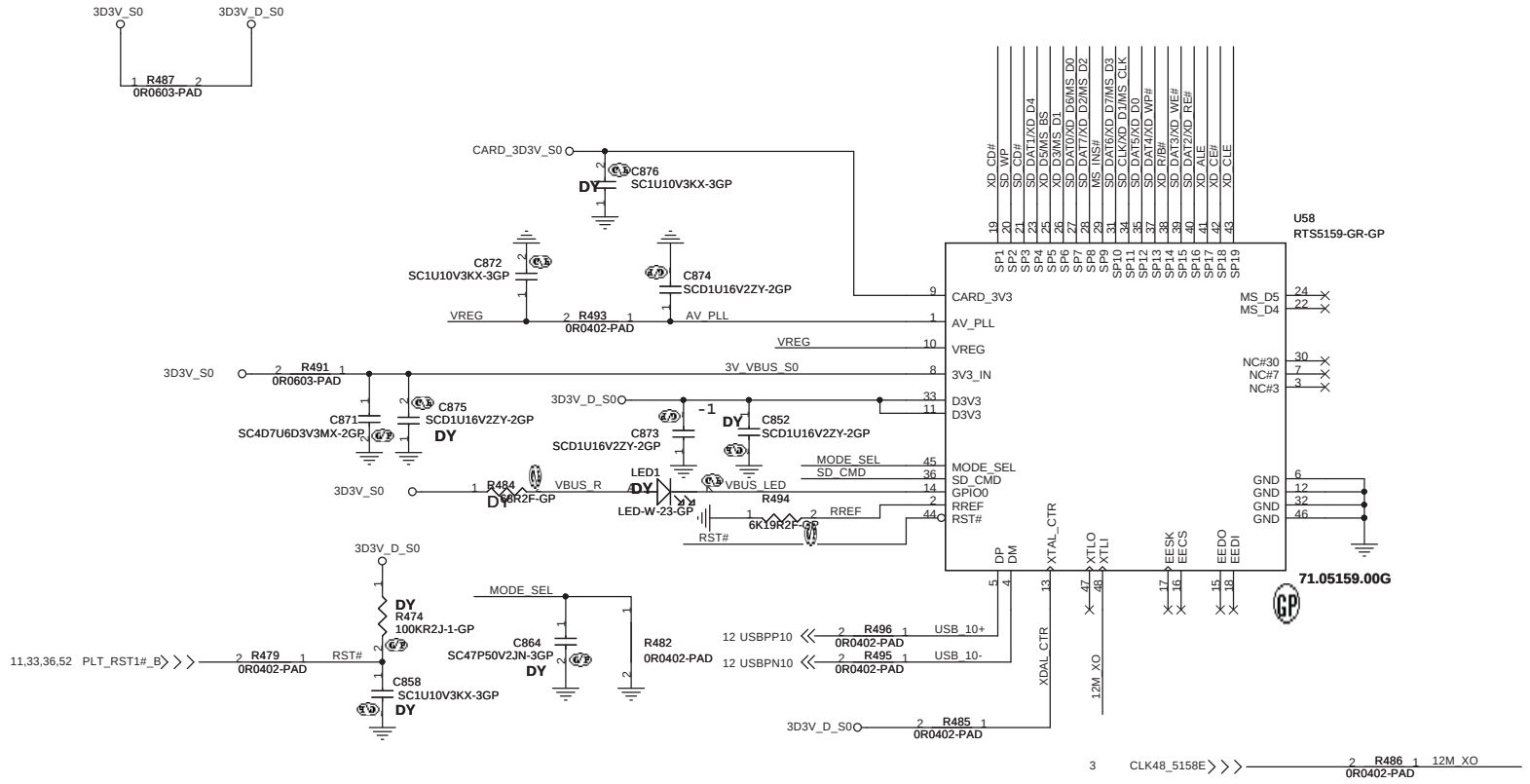
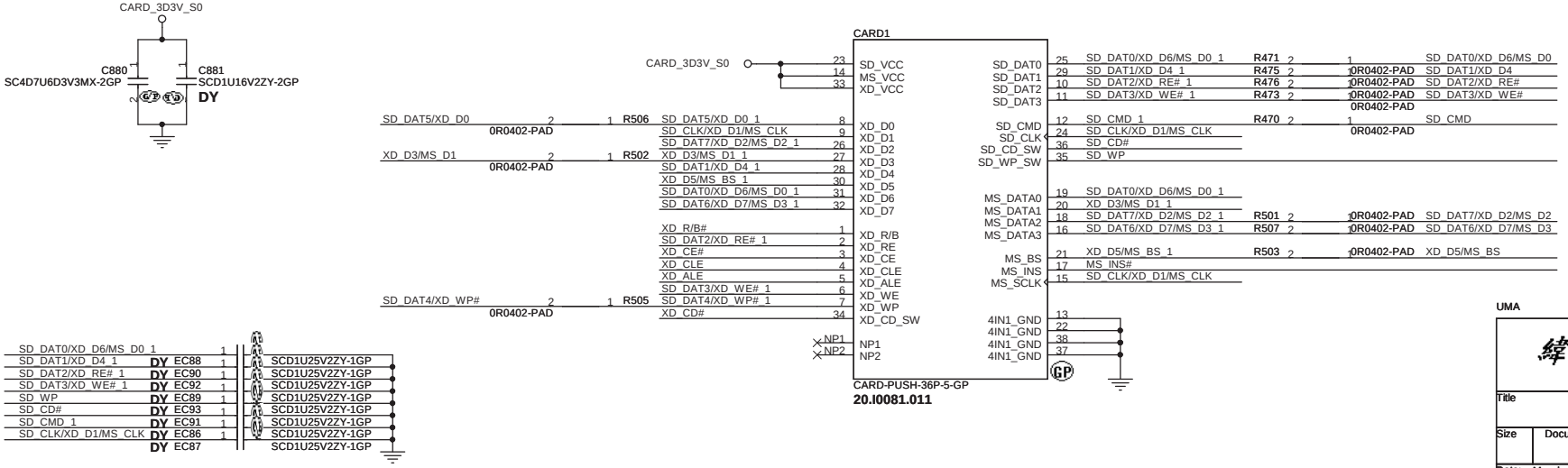
Title: MDC		
Size	Document Number: JV71-TR	Rev: SB
Date: Monday, July 06, 2009	Sheet 31 of 61	



5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



UMA

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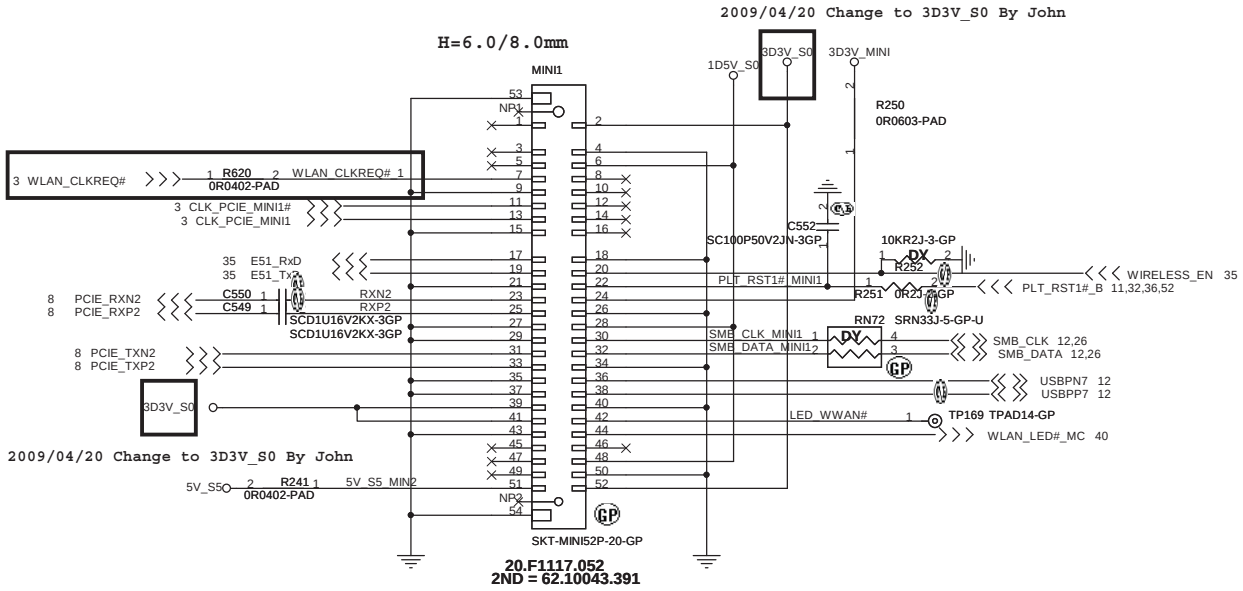
Title: CARDREADER- RTS5159

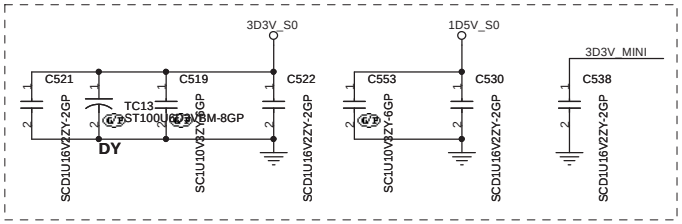
Size	Document Number	Rev
	JV71-TR	SB

Date: Monday, July 06, 2009 Sheet 32 of 61

Mini Card Connector(WLAN)



Place near MINI1



UMA

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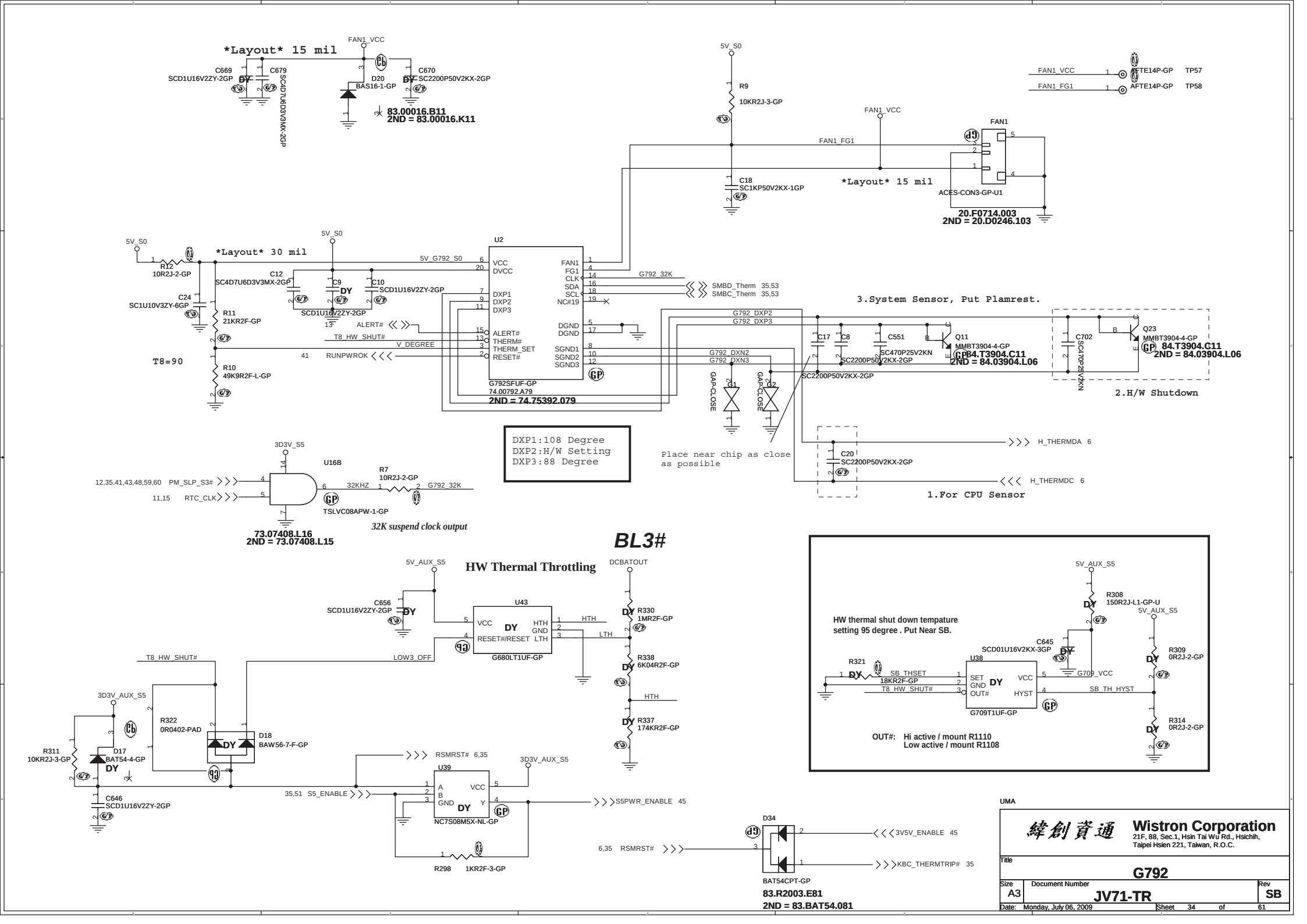
Title: MINI CARD		
Size	Document Number: JV71-TR	Rev: SA
Date: Monday, July 06, 2009	Sheet 33 of 61	



UMA

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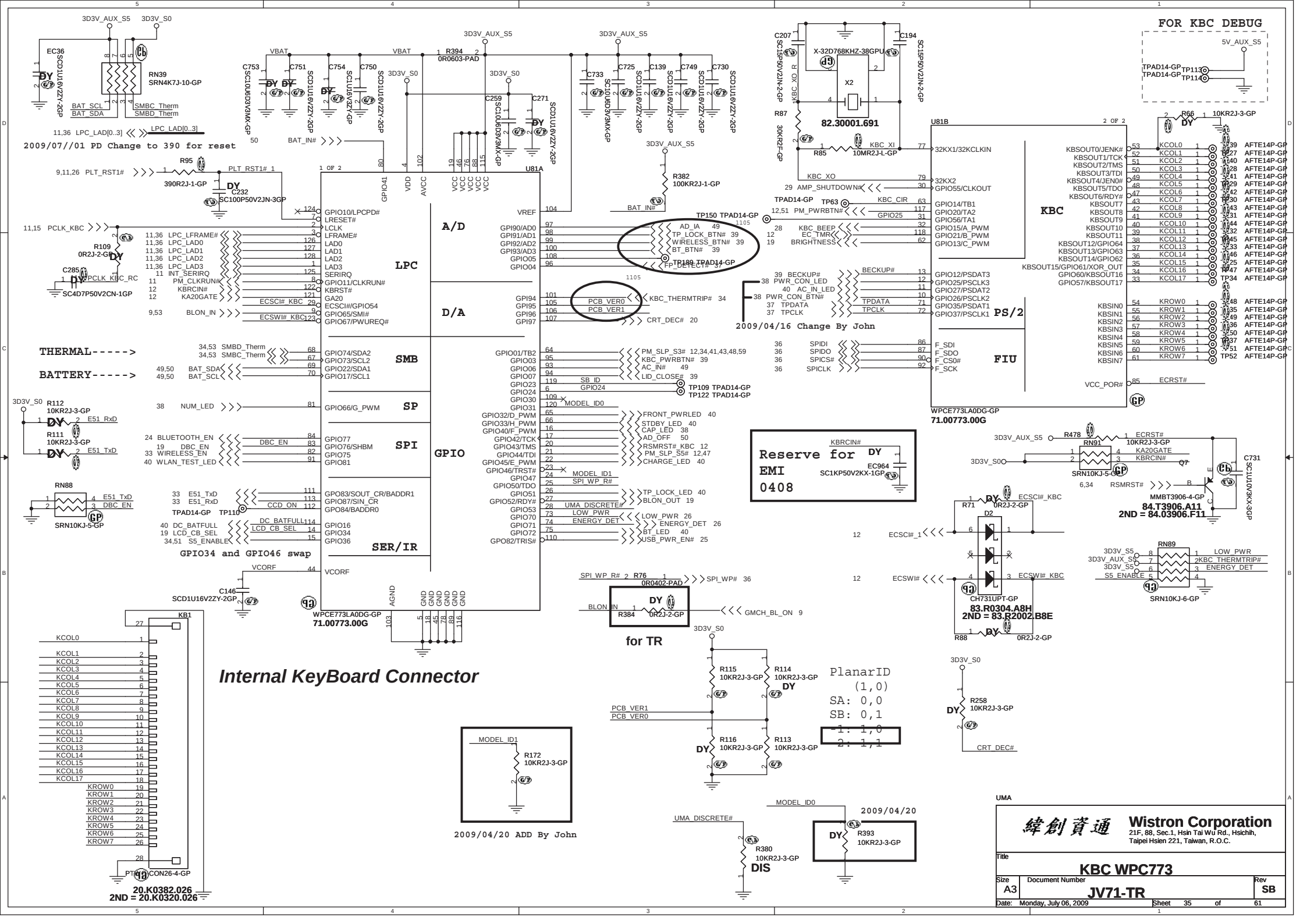
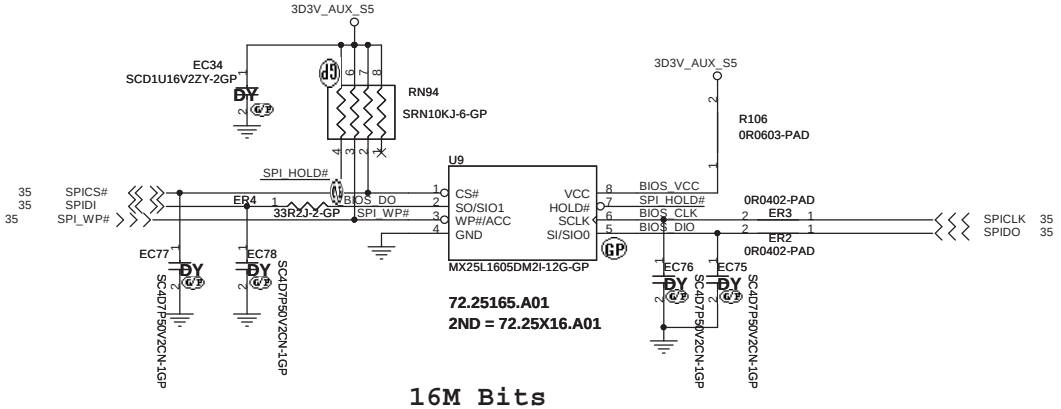
Title		
G792		
Size: A3	Document Number: JV71-TR	Rev: SB
Date: Monday, July 06, 2009	Sheet 34 of 61	

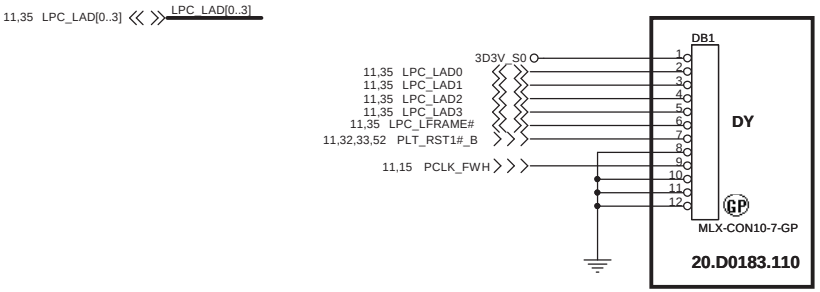

FOR KBC DEBUG
2009/07//01 PD Change to 390 for reset
2009/04/16 Change By John
THERMAL----->
BATTERY----->
GPIO34 and GPIO46 swap
Reserve for EMI 0408
for TR
2009/04/20 ADD By John
Internal KeyBoard Connector
PlanarID (1,0)
SA: 0,0
SB: 0,1
-1: 1,0
-2: 1,1
WPCE773LA0DG-GP
71.00773.00G
82.30001.691
84.T3906.A11
2ND = 84.03906.F11
83.R0304.A8H
2ND = 83.R2002.B8E
20.K0382.026
2ND = 20.K0320.026
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC773
JV71-TR
Monday, July 06, 2009



16M Bits

SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD



UMA

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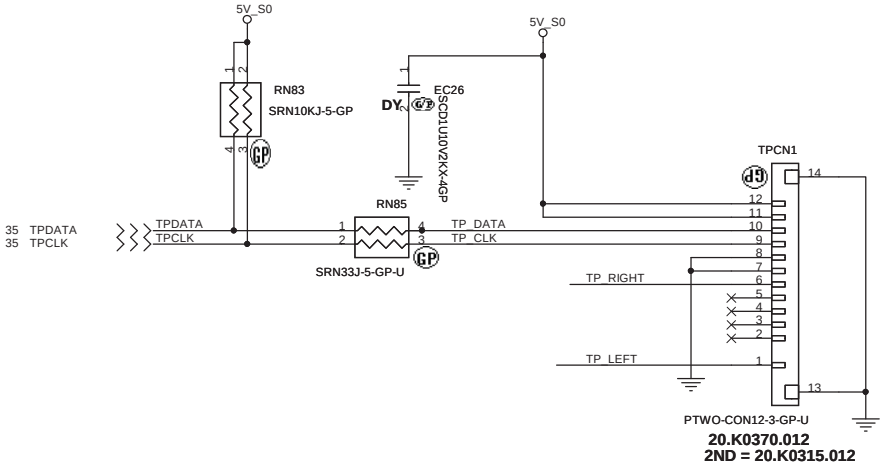
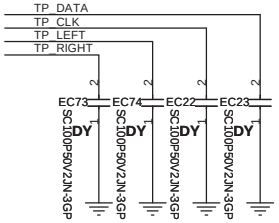
Title: **BIOS**

Size	Document Number	Rev
A3	JV71-TR	SA

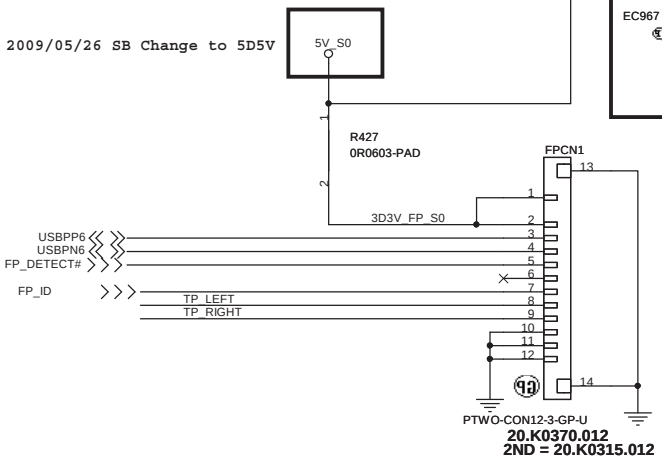
Date: Monday, July 06, 2009 Sheet 36 of 61

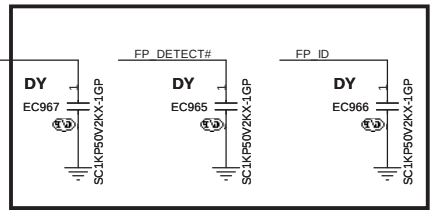
TOUCH PAD

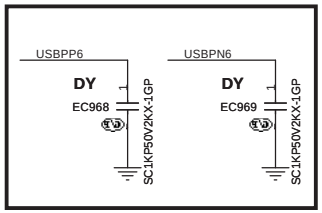




Finger printer





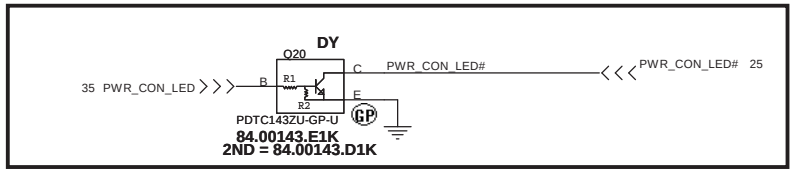


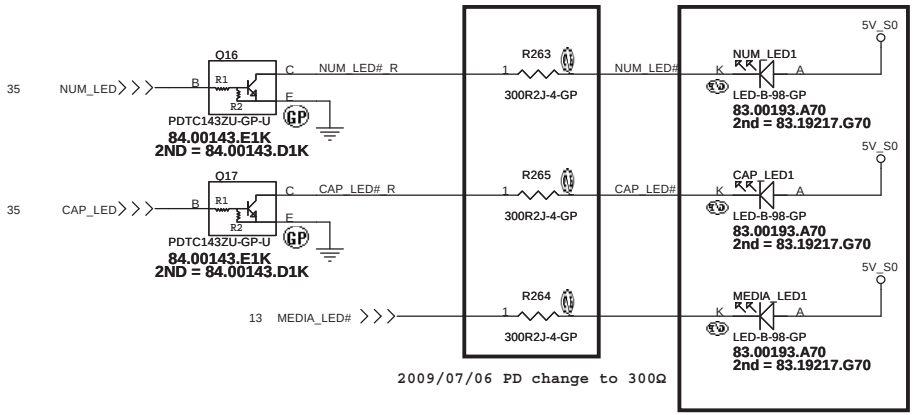
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

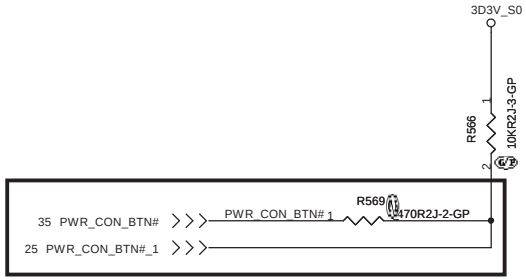
Title		
Touch PAD/Finger printer		
Size: A3	Document Number: **JV71-TR**	Rev: **SB**
Date: Monday, July 06, 2009	Sheet 37 of 61	

2009/04/16 Change By John

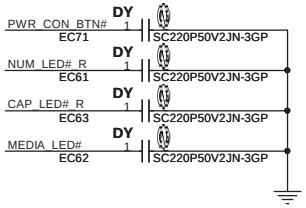




2009/07/06 PD change to 300Ω



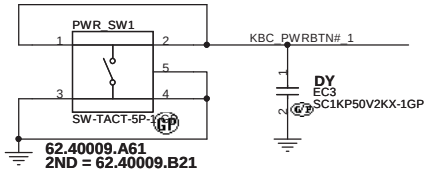
2009/04/16 Change By John



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LAUNCH BOARD		
Size: A3	Document Number: JV71-TR	Rev: SB
Date: Monday, July 06, 2009	Sheet 38 of 61	

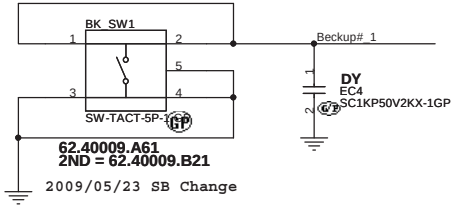
Cover Up Switch

Power Button



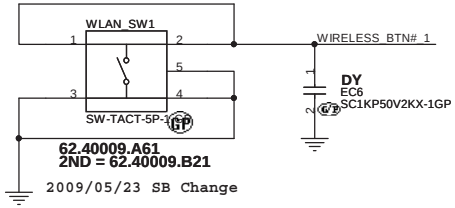
2009/05/23 SB Change

Beckup Button



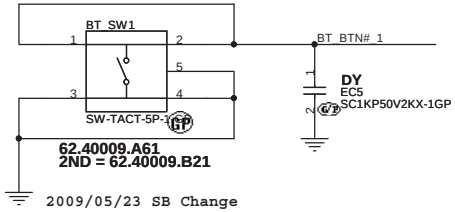
2009/05/23 SB Change

WIRELESS Button

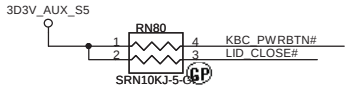


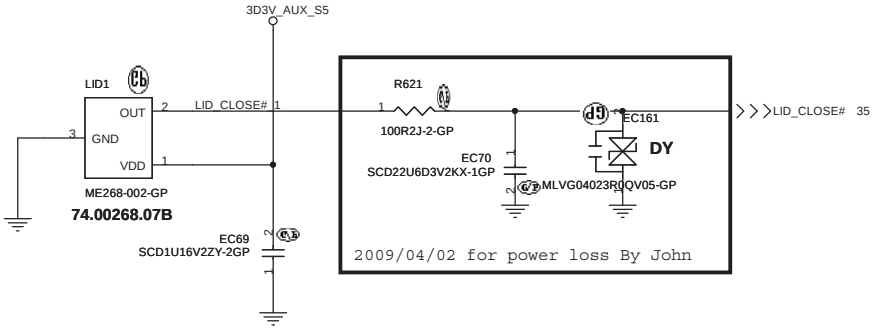
2009/05/23 SB Change

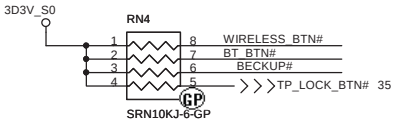
BT/3G Button

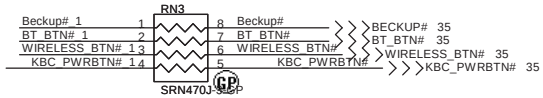


2009/05/23 SB Change

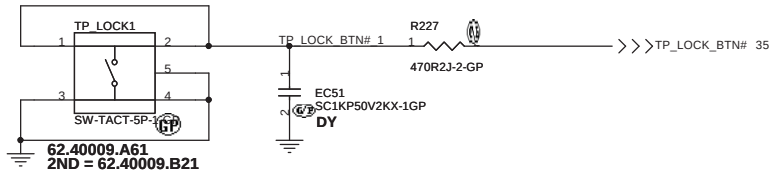






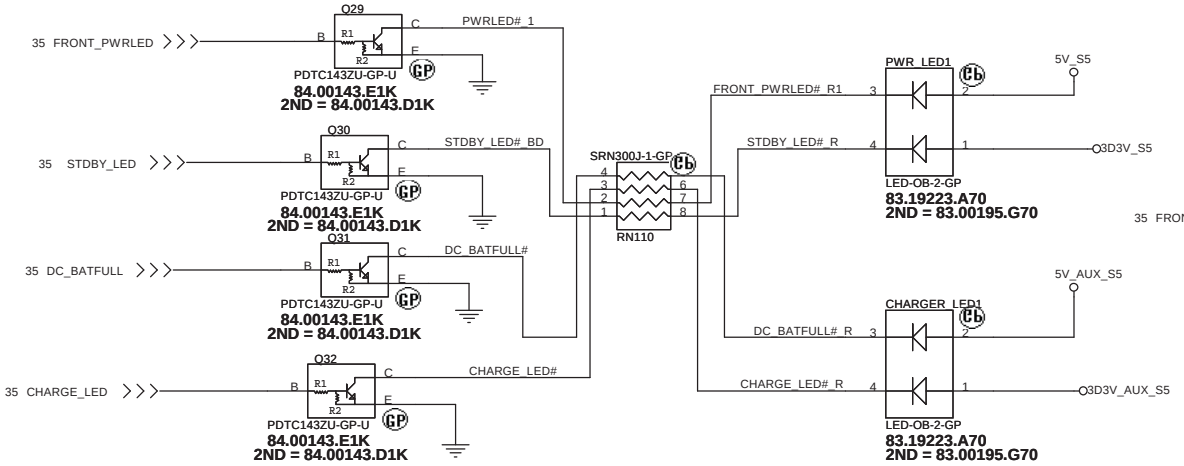


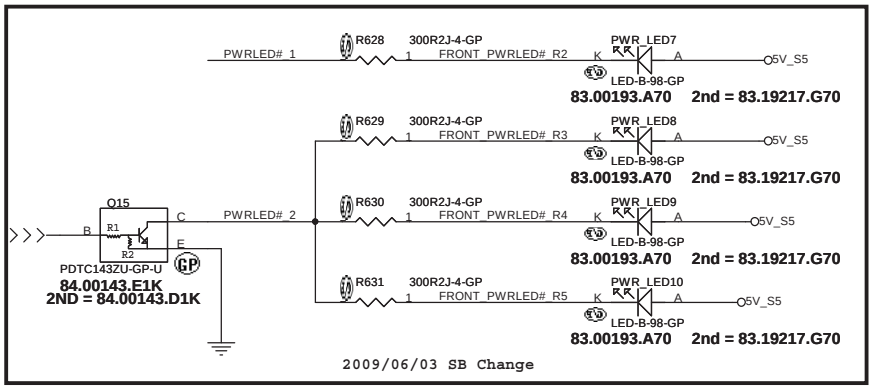
T/P lock Button

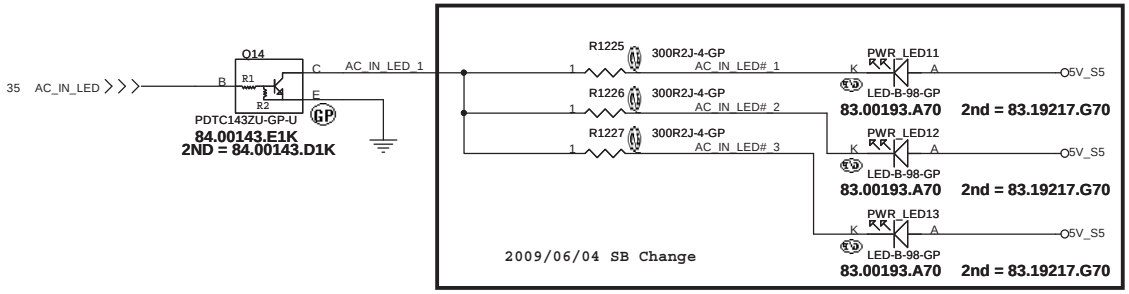


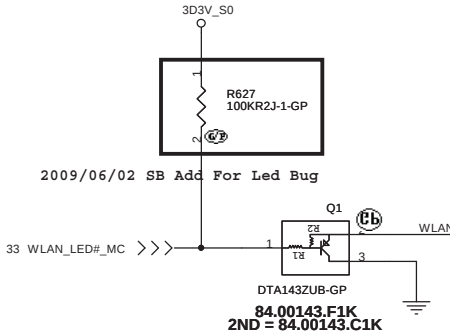
2009/05/23 SB Change

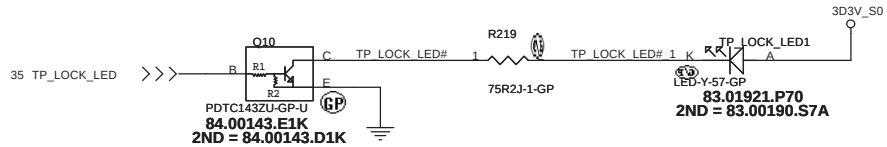
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: SWITCH		
Size: A3	Document Number: JV71-TR	Rev: SA
Date: Monday, July 06, 2009	Sheet 39 of 61	

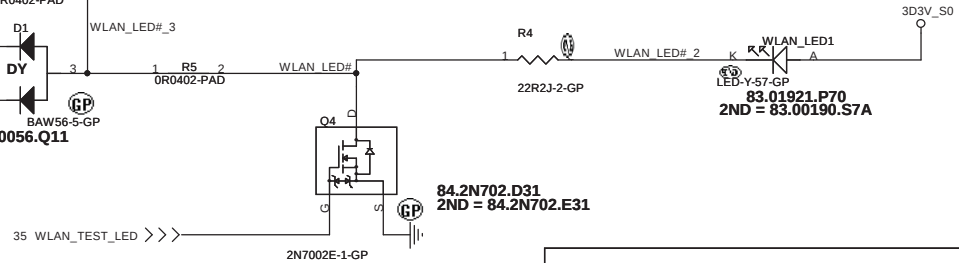


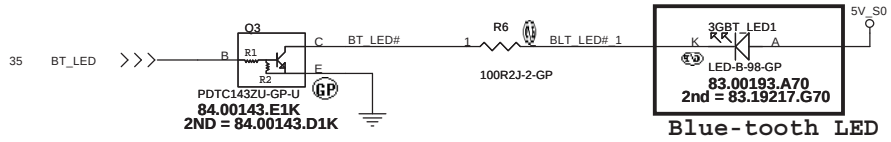












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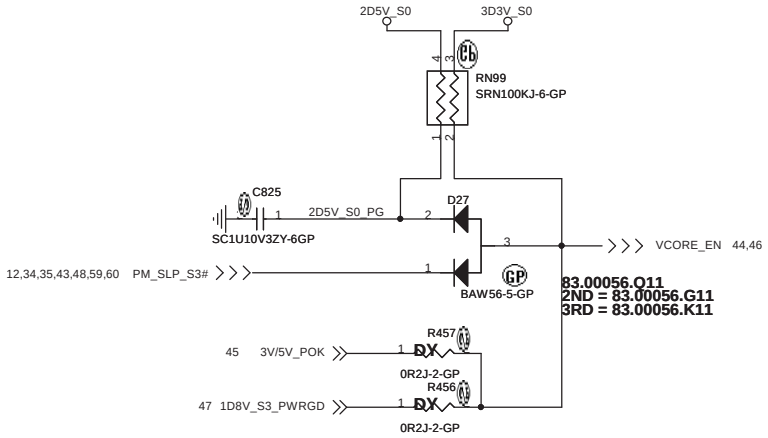
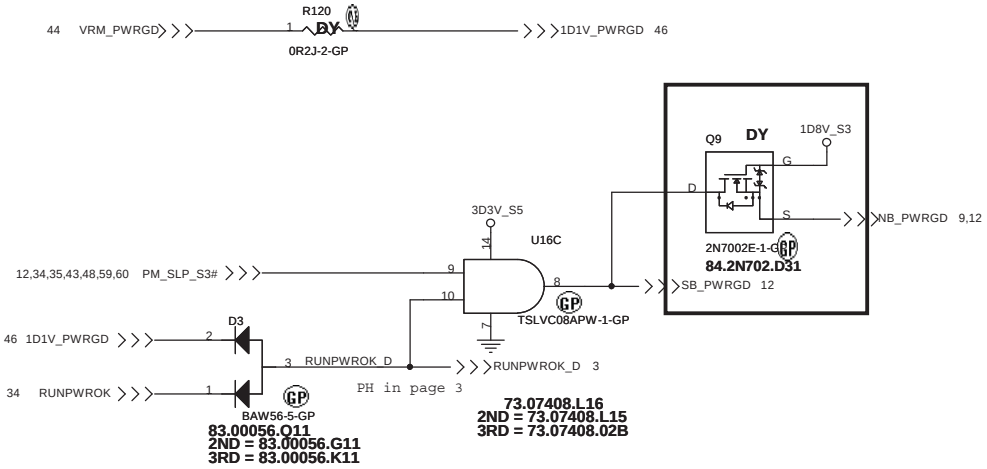
Title	**LED**	
Size: A3	Document Number: **JV71-TR**	Rev: **SB**
Date: Wednesday, July 08, 2009	Sheet 40 of 61	



P/H @ 1D8V_S3 PAGE



UMA

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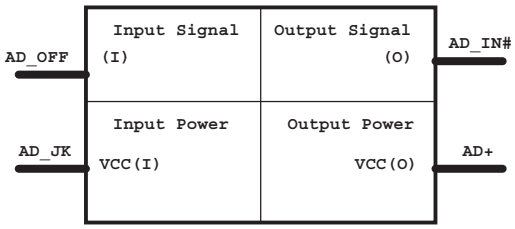
Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWER ON LOGIC**

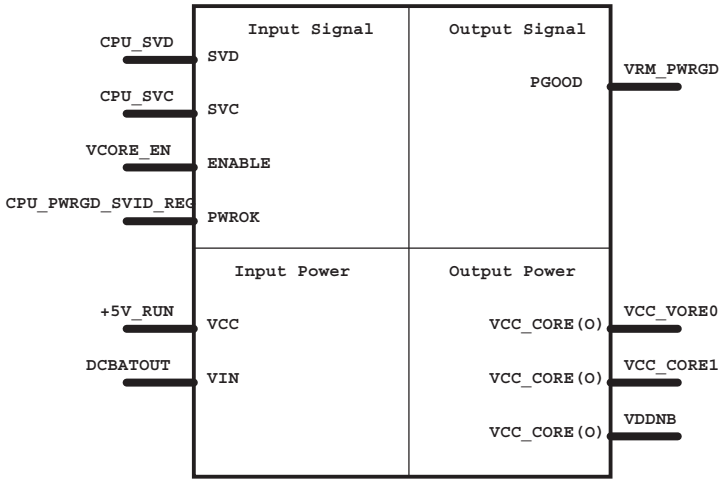
Size	Document Number	Rev
A3	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 41 of 61

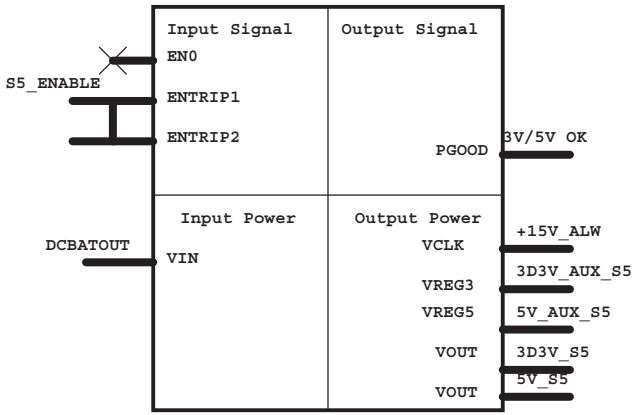
Adapter



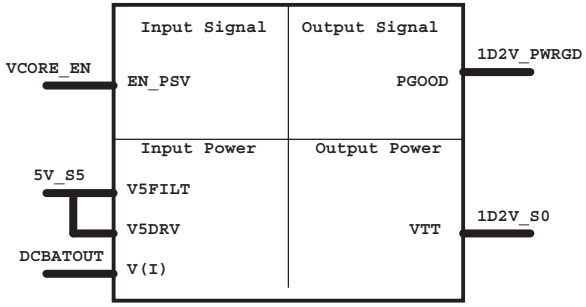
CPU_CORE
ISL6265HRTZ



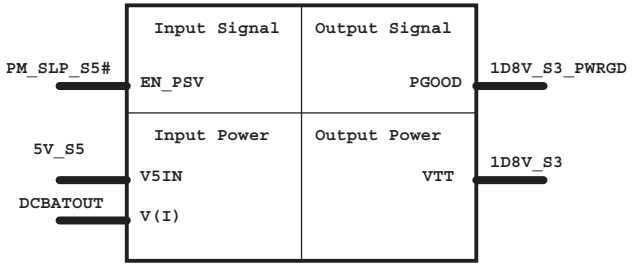
DCDC 5V/3D3V(RT8205A)



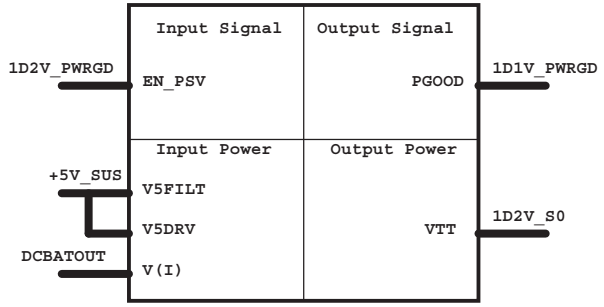
DCDC 1D2V(TPS51124)



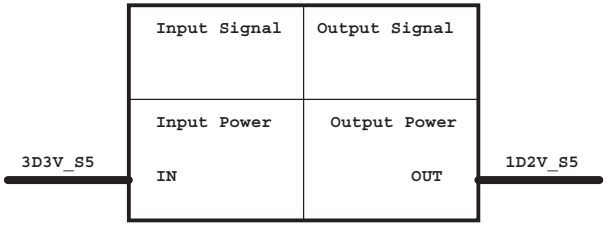
DCDC 1D8V(RT8209B)



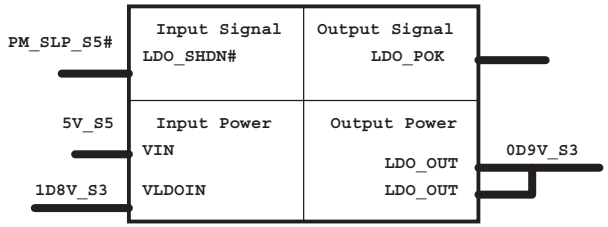
DCDC 1D1V(TPS51124)



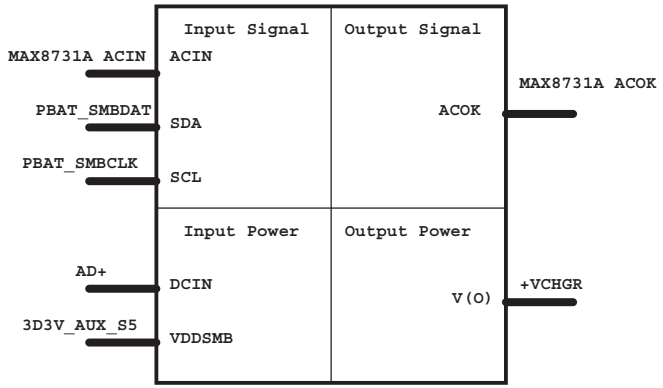
1D2V LDO G9161



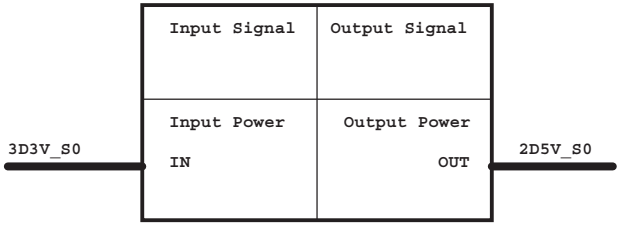
0D9V LDO RT9026



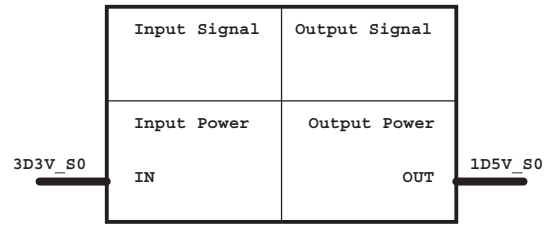
CHARGER MAX8731



2D5V LDO R9161



1D5V LDO G9571



UMA

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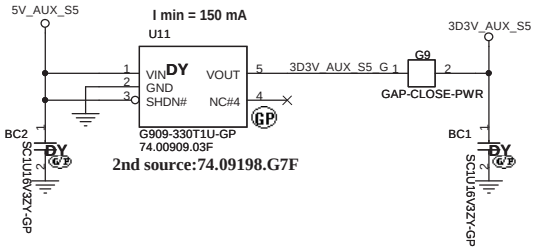
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

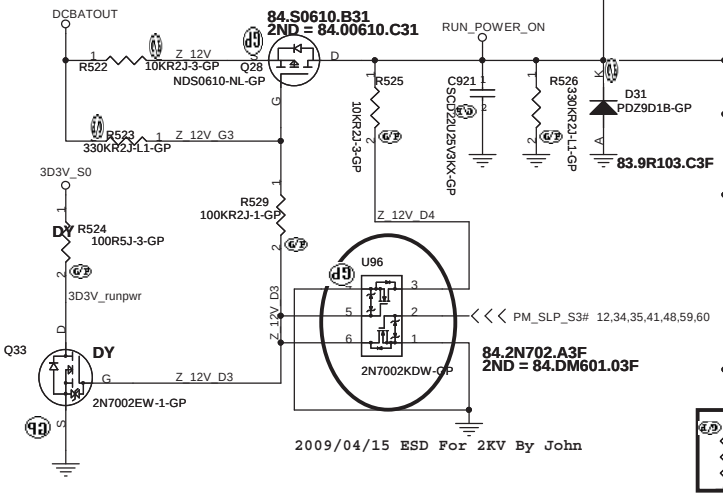
Size	Document Number	Rev
A3	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 42 of 61

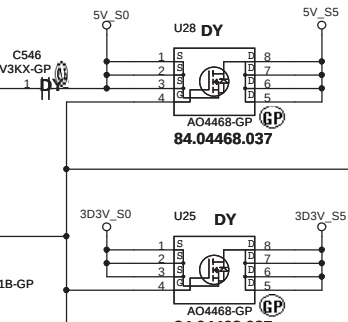
Aux Power 3D3V_AUX_S5

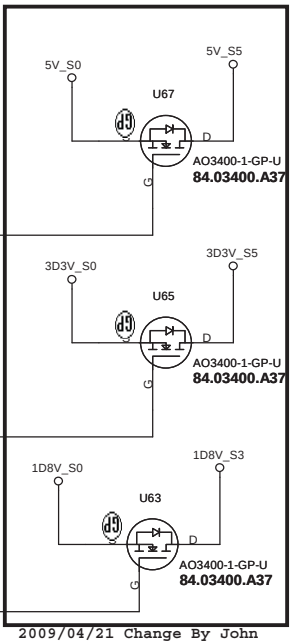


Run Power

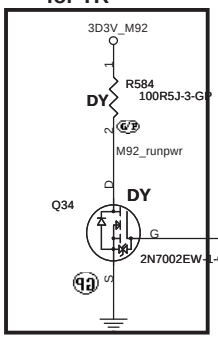


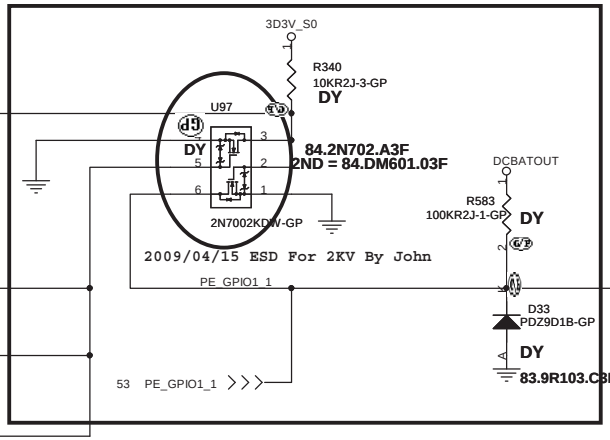
2009/04/15 ESD For 2KV By John



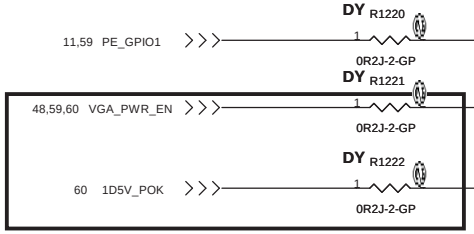


2009/04/21 Change By John

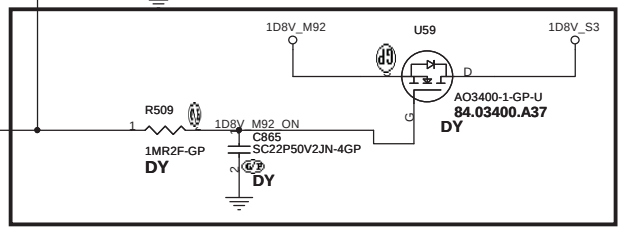


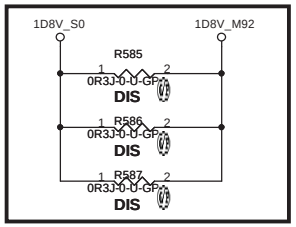


2009/04/15 ESD For 2KV By John



2009/04/21 ADD By John





R509,R342→10MΩ
C865→22pF
C675→1000pF
For VGA sequence issue

UMA

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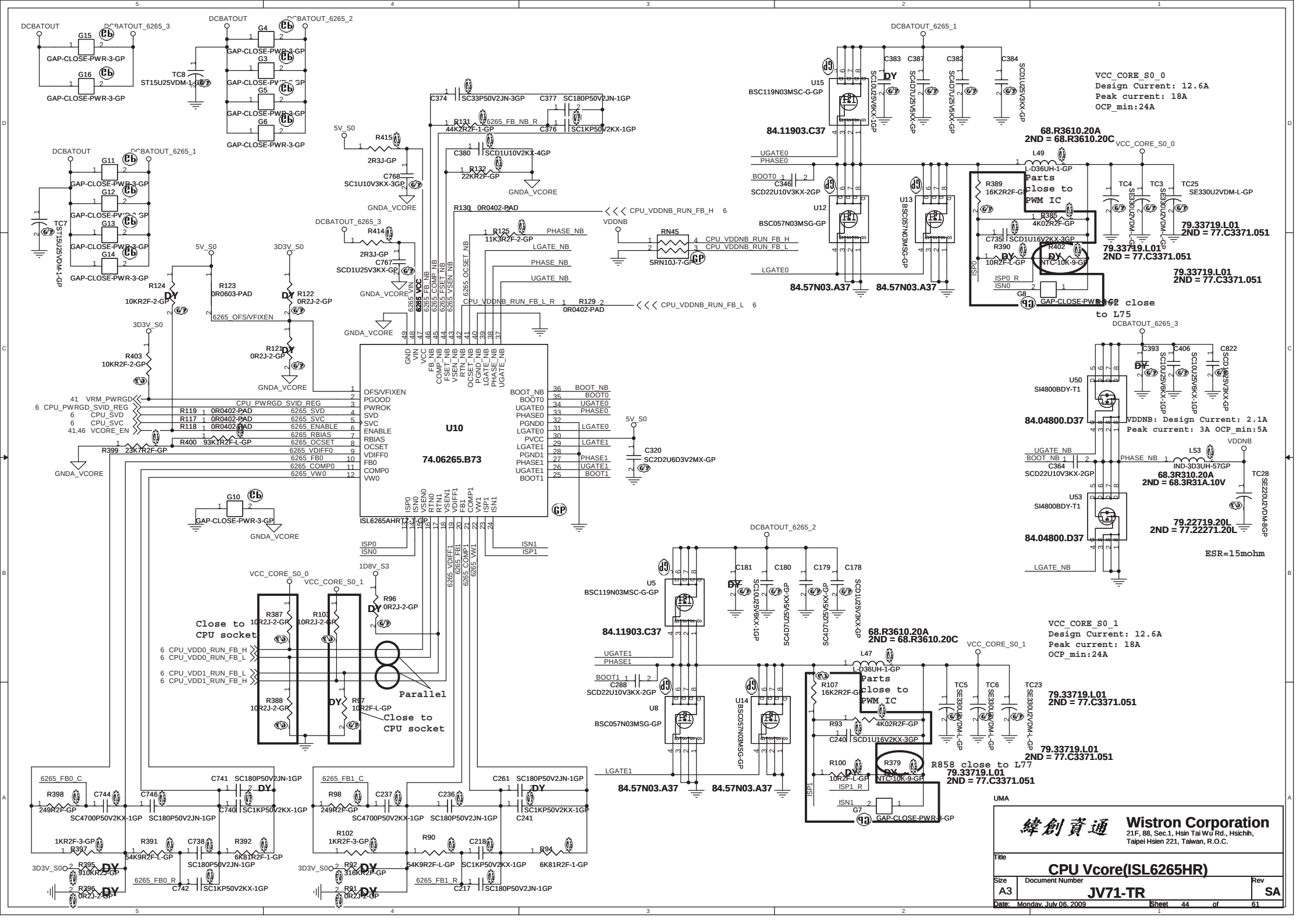
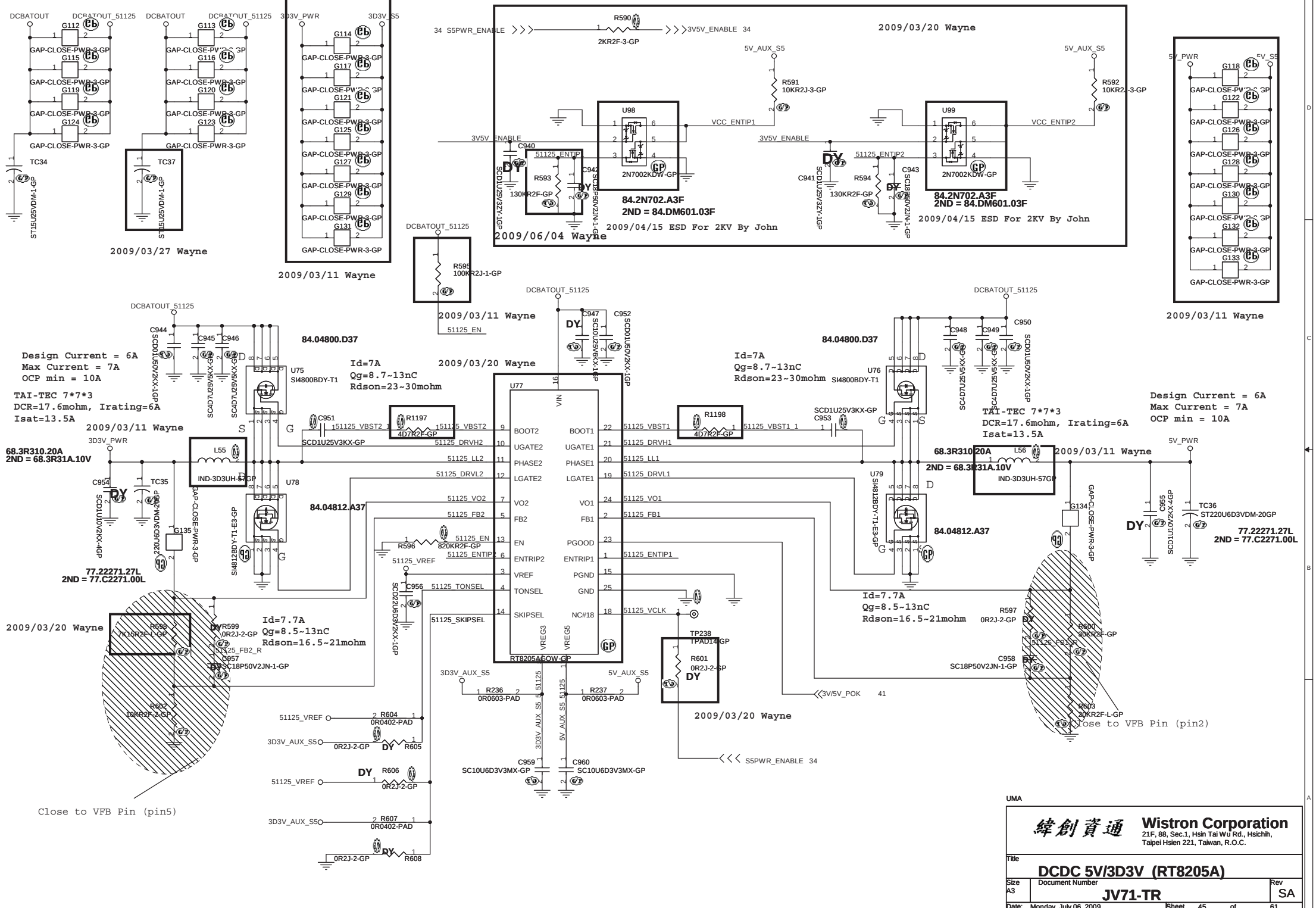
Title: **RUN AND AUX POWER**

Size	Document Number	Rev
A3	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 43 of 61


U10
74.06265.B73
ISL6265AHRTZ-T-GP
U15
BSC119N03MSC-G-GP
U12
BSC057N03MSG-GP
U13
BSC057N03MSG-GP
U50
SI4800BDY-T1
U53
SI4800BDY-T1
U5
BSC119N03MSC-G-GP
U8
BSC057N03MSG-GP
U14
BSC057N03MSG-GP
84.11903.C37
84.57N03.A37
84.04800.D37
68.R3610.20A
2ND = 68.R3610.20C
68.R310.20A
2ND = 68.3R31A.10V
79.33719.L01
2ND = 77.C3371.051
79.22719.20L
2ND = 77.22271.20L
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
ESR=15mohm
Parts close to PWM IC
R858 close to L77
Close to CPU socket
Parallel
R858 close to L75
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
JV71-TR
Size A3
Rev SA
Date: Monday, July 06, 2009
Sheet 44 of 61



UMA

緯創資通 **Wistron Corporation**
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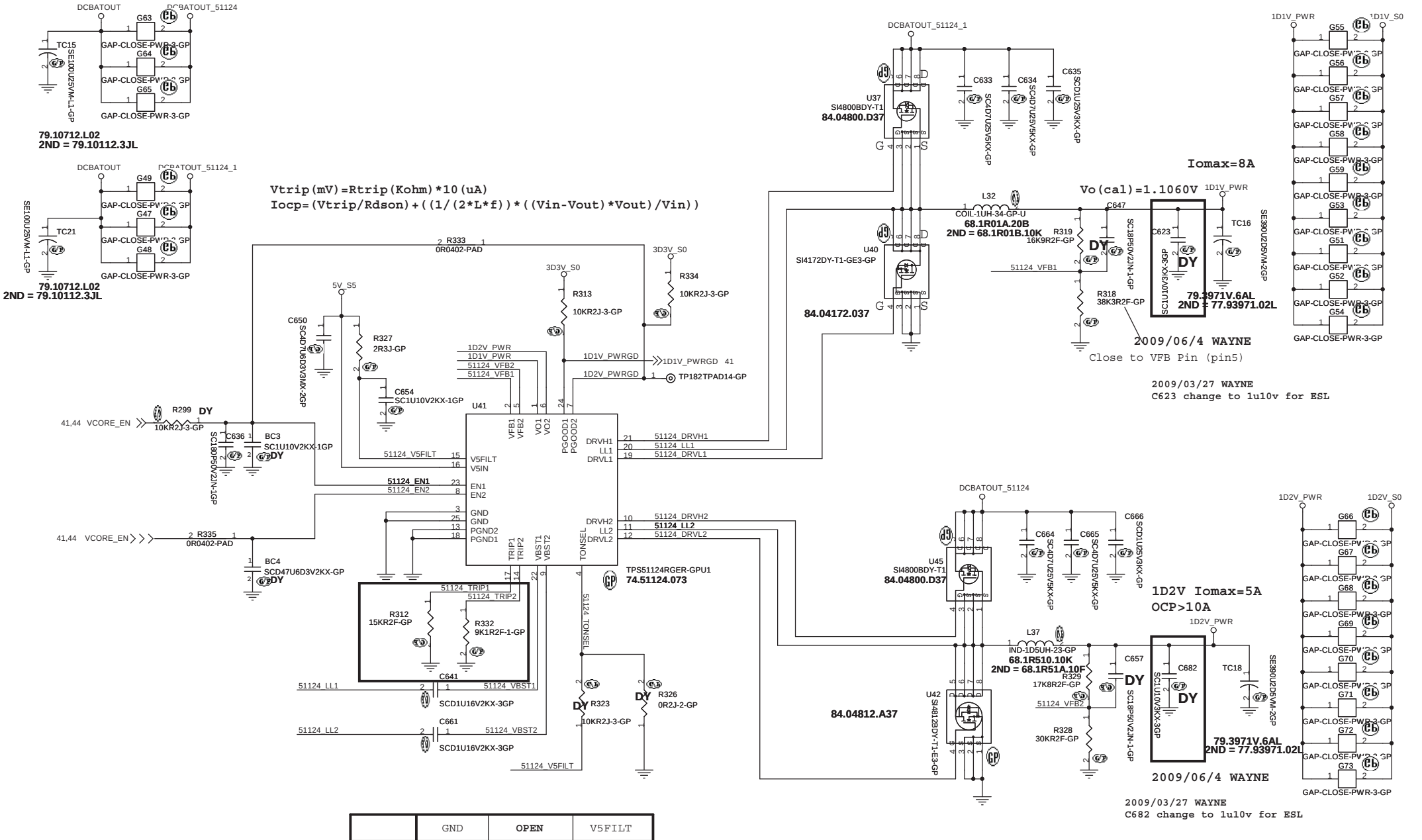
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCDC 5V/3D3V (RT8205A)**

Size	Document Number	Rev
A3	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 45 of 61



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	**300k/CH1** **360k/CH2**	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

UMA

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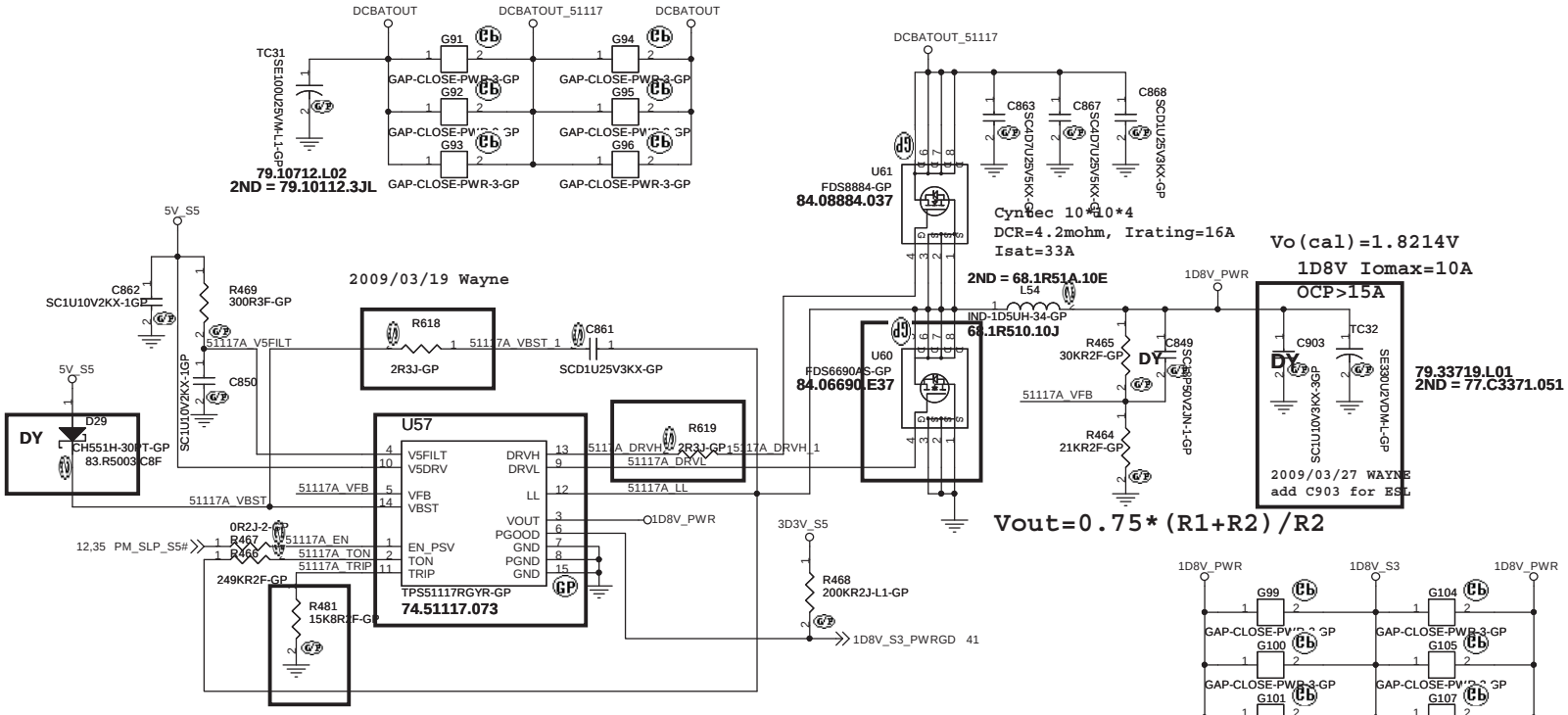
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51124_1D1V_1D2V***

Size	Document Number	Rev
A3	**JV71-TR**	**SA**

Date: Monday, July 06, 2009 Sheet 46 of 61

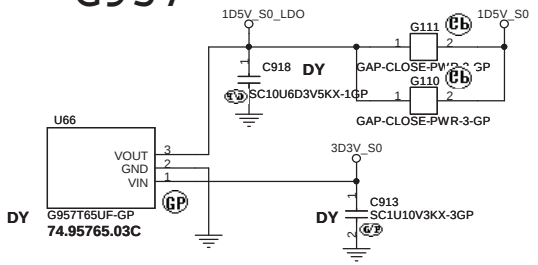


UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**DCDC_1D8V_APW7141/LDO 0D9V**	
Size: A3	Document Number: **JV71-TR**	Rev: **SA**
Date: Monday, July 06, 2009	Sheet 47 of 61	

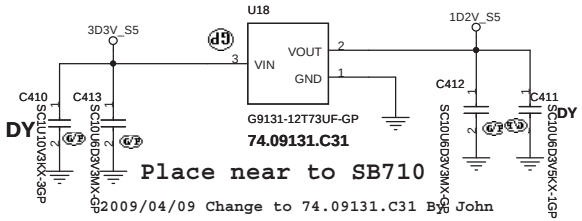
1D5V_S0
Iomax=1A

G957



For MINI Card.NEW Card power SW

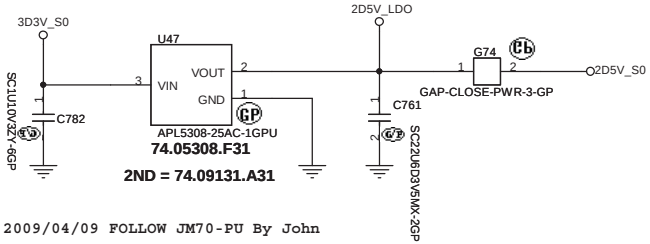
1D2V_S5
Iomax=400mA



Place near to SB710

2009/04/09 Change to 74.09131.C31 By John

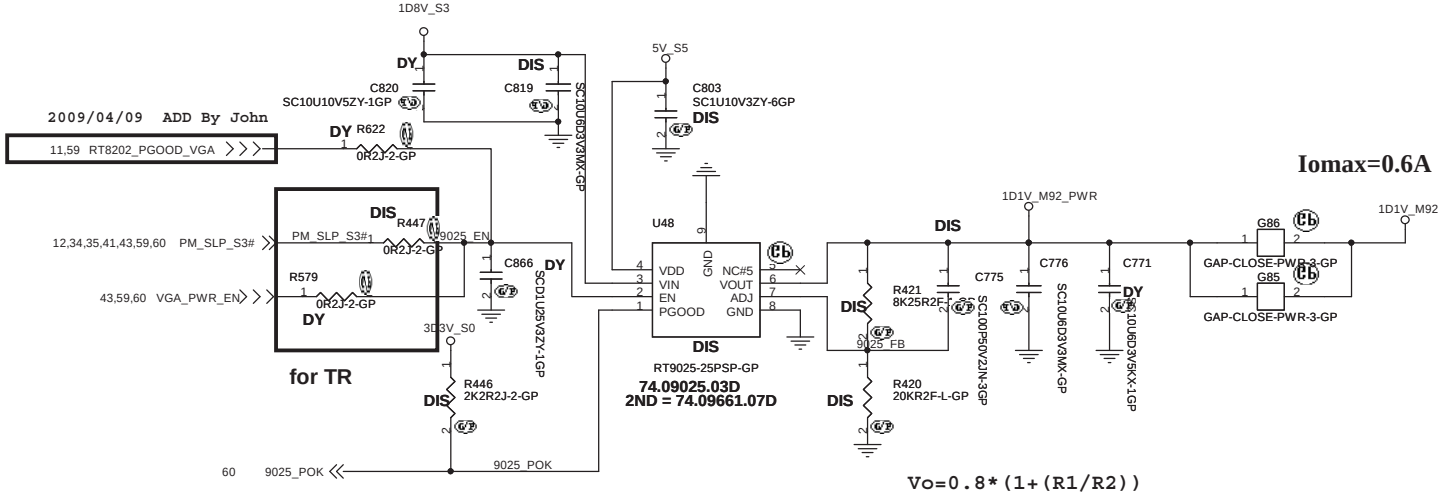
2D5V
Iomax=0.2A



2009/04/09 FOLLOW JM70-PU By John

Place near to CPU

Iomax=0.6A



Vo=0.8*(1+(R1/R2))

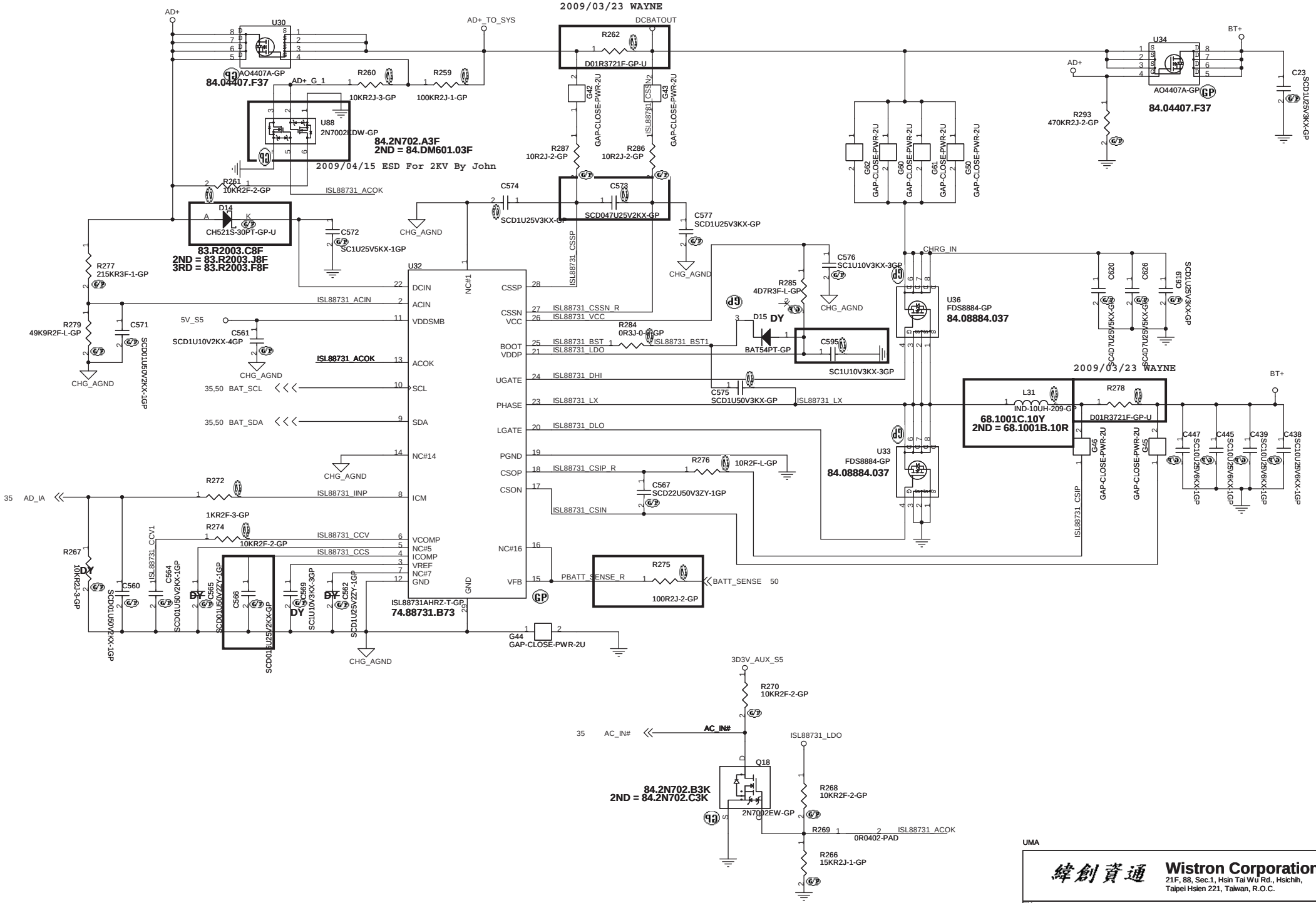
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

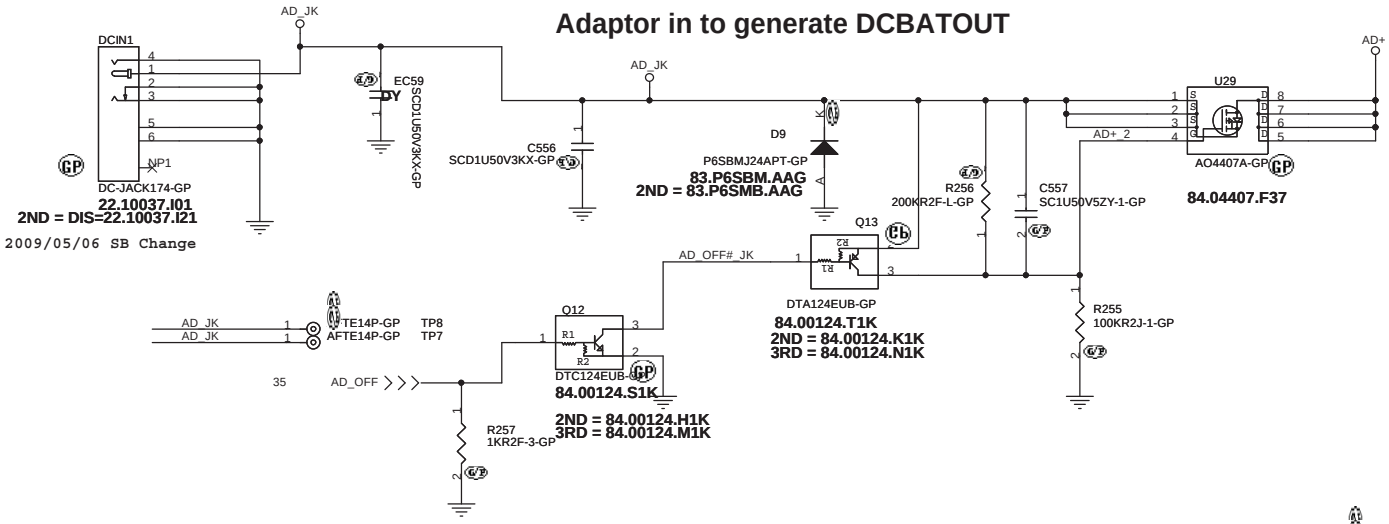
Title: LDO 2D5V/1D5V/1D2V_S5/1D1V_M92

Size	Document Number	Rev
A3	JV71-TR	SA

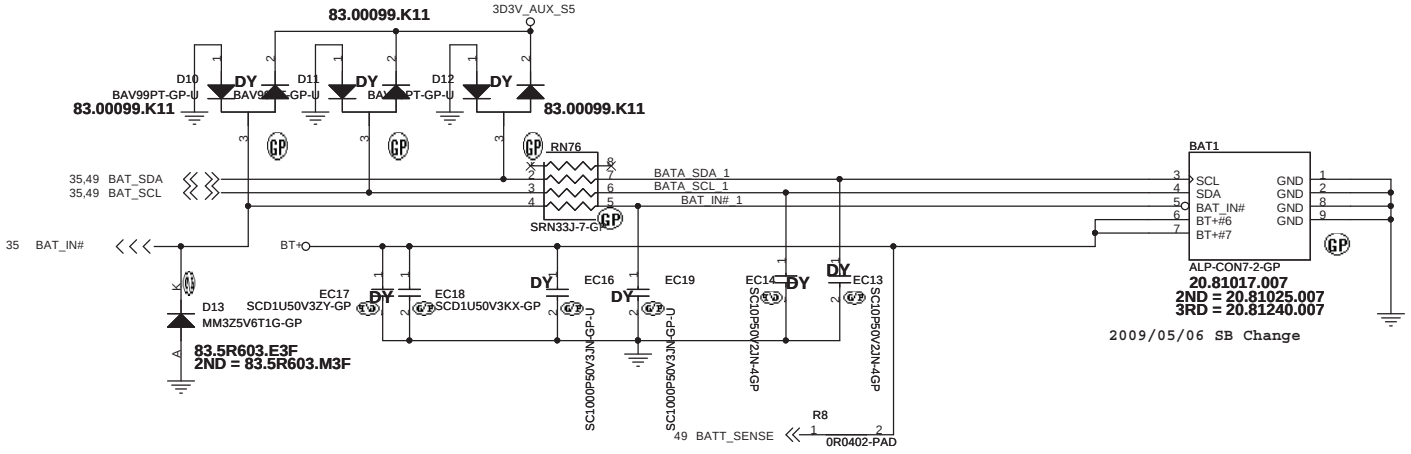
Date: Monday, July 06, 2009 Sheet 48 of 61

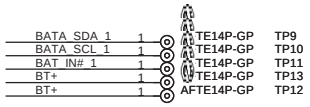

2009/03/23 WAYNE
AD+
AD+_TO_SYS
DCBATOUT
U30
AO4407A-GP
84.04407.F37
R260
10KR2J-3-GP
R259
100KR2J-1-GP
AD+_G_1
U88
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
2009/04/15 ESD For 2KV By John
R262
D01R3721F-GP-U
R287
10R2J-2-GP
R286
10R2J-2-GP
ISL88731_CSSN
ISL88731_CSSP
GAP-CLOSE-PWR-2U
R261
10KR2F-2-GP
ISL88731_ACOK
D14
CH521S-30PT-GP-U
83.R2003.C8F
2ND = 83.R2003.J8F
3RD = 83.R2003.F8F
C572
SC1U25V5KX-1GP
C574
SCD1U25V3KX-GP
C573
SCD047U25V2KX-GP
C577
SCD1U25V3KX-GP
CHG_AGND
U32
ISL88731AHRZ-T-GP
74.88731.B73
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
NC#1
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
R277
215KR3F-1-GP
R279
49K9R2F-L-GP
C571
SCD01U50V2KX-1GP
C561
SCD1U10V2KX-4GP
5V_S5
ISL88731_ACIN
35,50 BAT_SCL
35,50 BAT_SDA
R272
1KR2F-3-GP
35 AD_IA
R267
100KR2J-3-GP
DY
C560
SCD01U50V2KX-1GP
C564
SCD01U50V2KX-1GP
C565
SCD01U50V2ZY-1GP
C566
SCD01U25V2KX-GP
C569
SC1U10V3KX-3GP
C562
SCD1U25V2ZY-1GP
R274
10KR2F-2-GP
ISL88731_CCV
ISL88731_CCS
ISL88731_IINP
ISL88731_CCV1
R276
10R2F-L-GP
C567
SCD22U50V3ZY-1GP
ISL88731_CSIP_R
ISL88731_CSIN
R275
100R2J-2-GP
PBATT_SENSE_R
BATT_SENSE 50
G44
GAP-CLOSE-PWR-2U
ISL88731_DHI
ISL88731_LX
ISL88731_DLO
ISL88731_BST_1
ISL88731_LDO
ISL88731_BST1
R284
0R3J-0-GP
D15
BAT54PT-GP
C595
SC1U10V3KX-3GP
C575
SCD1U50V3KX-GP
R285
4D7R3F-L-GP
C576
SC1U10V3KX-3GP
CHRG_IN
U36
FDS8884-GP
84.08884.037
U33
FDS8884-GP
84.08884.037
L31
IND-10UH-209-GP
68.1001C.10Y
2ND = 68.1001B.10R
R278
D01R3721F-GP-U
C620
C626
C619
C4D7U25V5KX-GP
SCD1U25V3KX-GP
C447
C445
C439
C438
SC10U25V6KX-1GP
G46
G45
GAP-CLOSE-PWR-2U
ISL88731_CSIP
BT+
U34
AO4407A-GP
84.04407.F37
R293
470KR2J-2-GP
C23
SCD1U25V3KX-GP
G62
G60
G61
G50
3D3V_AUX_S5
R270
10KR2F-2-GP
35 AC_IN#
AC_IN#
ISL88731_LDO
Q18
2N7002EW-GP
84.2N702.B3K
2ND = 84.2N702.C3K
R268
10KR2F-2-GP
R269
0R0402-PAD
R266
15KR2J-1-GP
ISL88731_ACOK
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A Charger
Size
A3
Document Number
JV71-TR
Rev
SA
Date: Monday, July 06, 2009
Sheet 49 of 61

Adaptor in to generate DCBATOUT



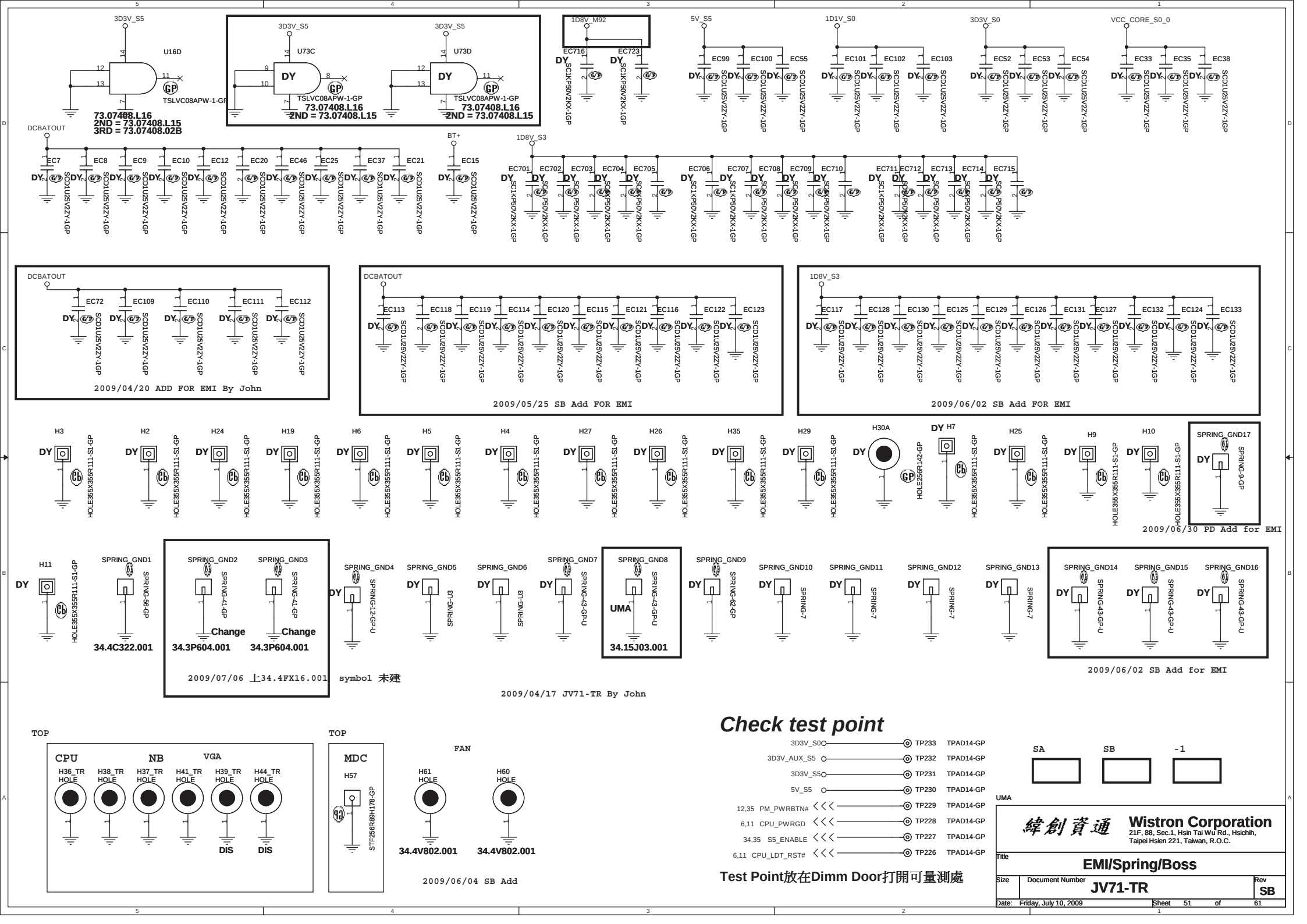
BATTERY CONNECTOR

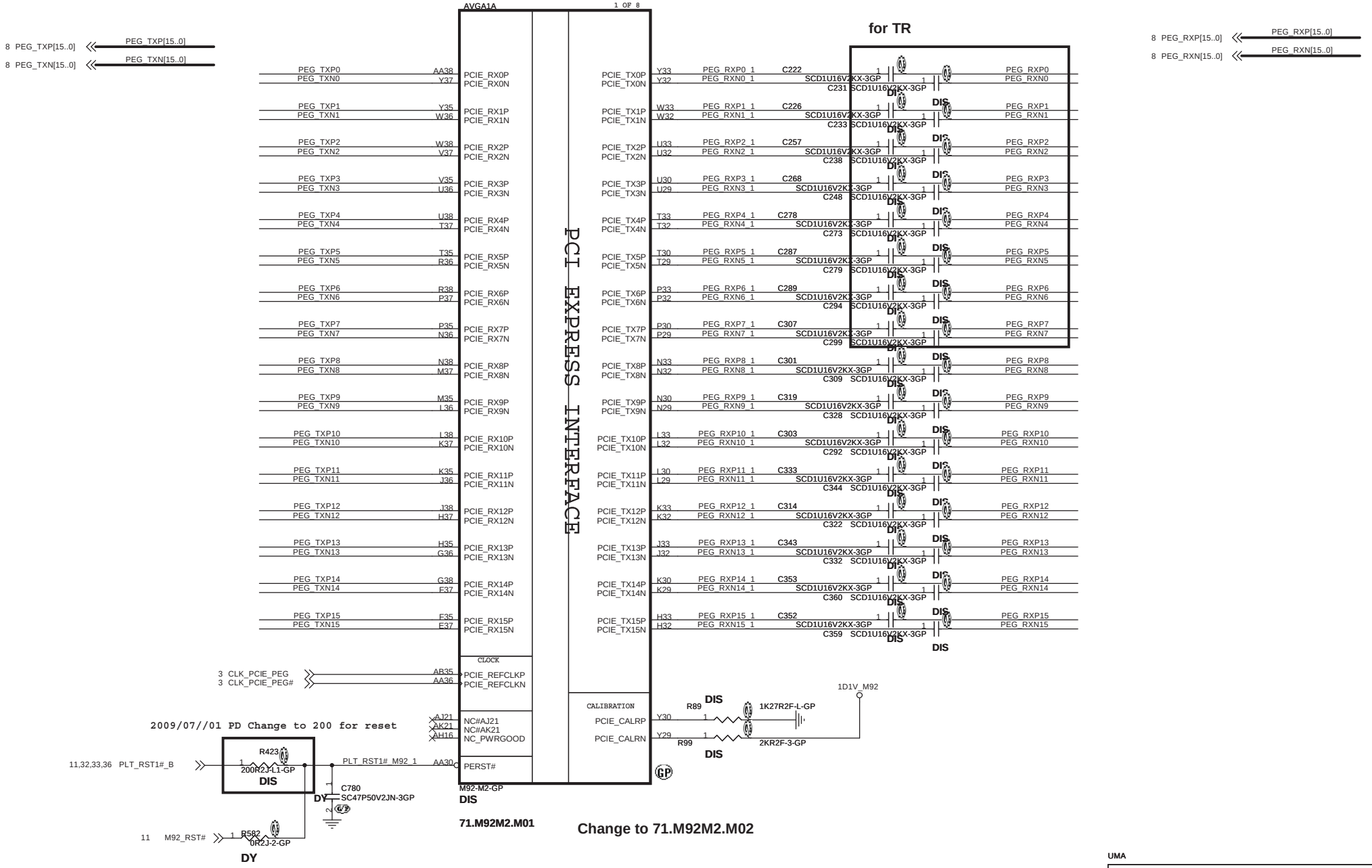




UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AD/BATT CONN		
Size	Document Number: JV71-TR	Rev: SB
Date: Monday, July 06, 2009	Sheet 50 of 61	


3D3V_S5
U16D
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
U73C
U73D
1D8V_M92
5V_S5
1D1V_S0
3D3V_S0
VCC_CORE_S0_0
DCBATOUT
BT+
1D8V_S3
2009/04/20 ADD FOR EMI By John
2009/05/25 SB Add FOR EMI
2009/06/02 SB Add FOR EMI
2009/06/30 PD Add for EMI
2009/07/06 上34.4FX16.001 symbol 未建
2009/04/17 JV71-TR By John
2009/06/02 SB Add for EMI
34.4C322.001
34.3P604.001
34.15J03.001
UMA
Check test point
3D3V_S0 TP233 TPAD14-GP
3D3V_AUX_S5 TP232 TPAD14-GP
3D3V_S5 TP231 TPAD14-GP
5V_S5 TP230 TPAD14-GP
12,35 PM_PWRBTN# TP229 TPAD14-GP
6,11 CPU_PWRGD TP228 TPAD14-GP
34,35 S5_ENABLE TP227 TPAD14-GP
6,11 CPU_LDT_RST# TP226 TPAD14-GP
Test Point放在Dimm Door打開可量測處
TOP
CPU
NB
VGA
DIS
MDC
FAN
34.4V802.001
2009/06/04 SB Add
SA
SB
-1
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
Document Number
JV71-TR
Rev
SB
Date: Friday, July 10, 2009
Sheet 51 of 61



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**M92 PCIE**	
Size A3	Document Number **JV71-TR**	Rev **SB**
Date: Monday, July 06, 2009	Sheet 52 of 61	

Layout notice:
It should be pleace near HDMI connector

DVPDATA [3:2:1:0] for VRAM type
selection H/W strap
Should provide VRAM Table for VBios
request

DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)

It's strap for GDDR3-136ball
Need to Clarify

Back Bias (body bias) which minimizes
power consumption in battery modes.
PD = Disable
PU = Enable

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

Depending on OSC used select voltage divider resist
values R25 R70 to ensure XTALIN voltage level of
1.8V

For Thermal sensor

84.2N702.B3K
2ND = 84.2N702.C3K

84.2N702.A3F
2ND = 84.DM601.03F

2009/04/15 ESD For 2KV By John

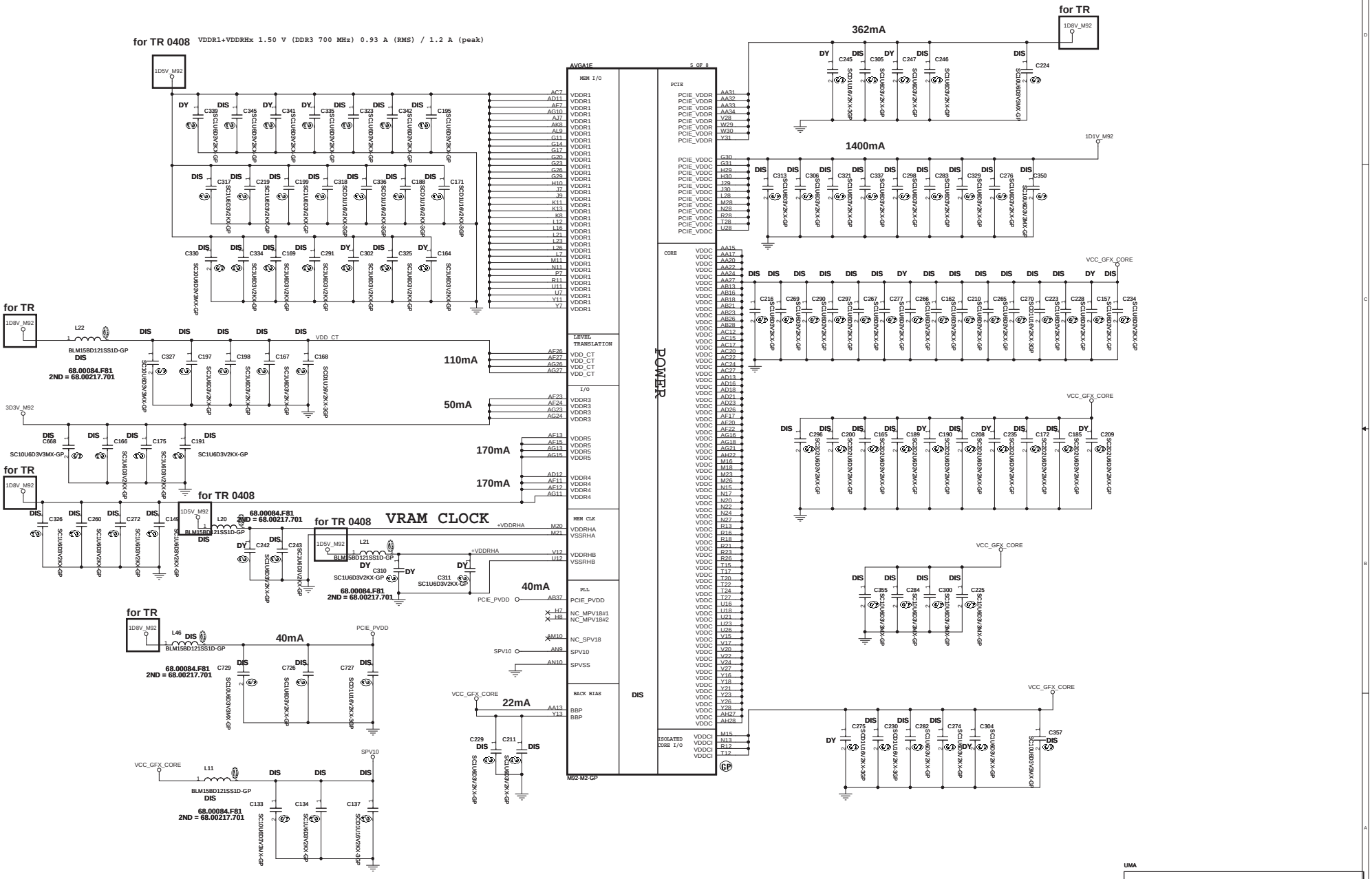
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M92 IO

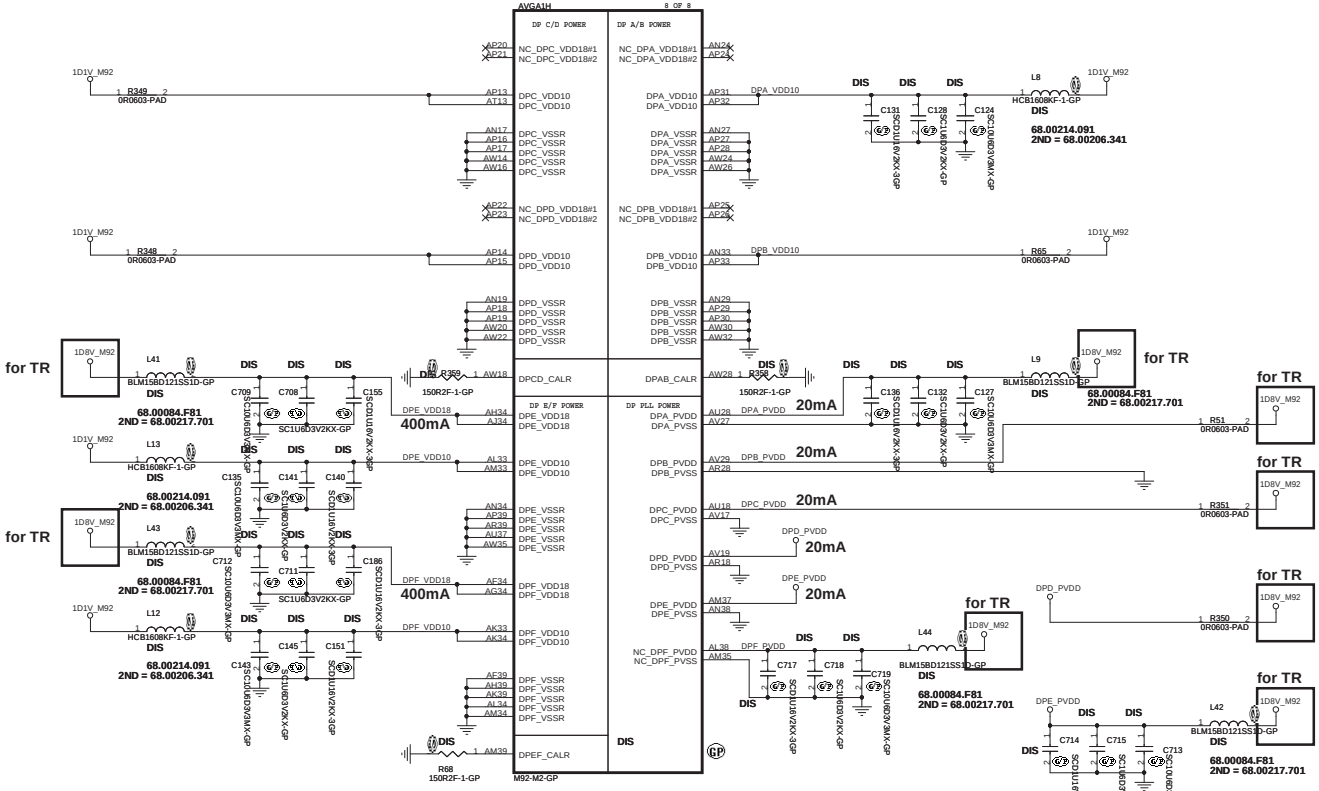
Size: A2 | Document Number: JV71-TR | Rev: SA

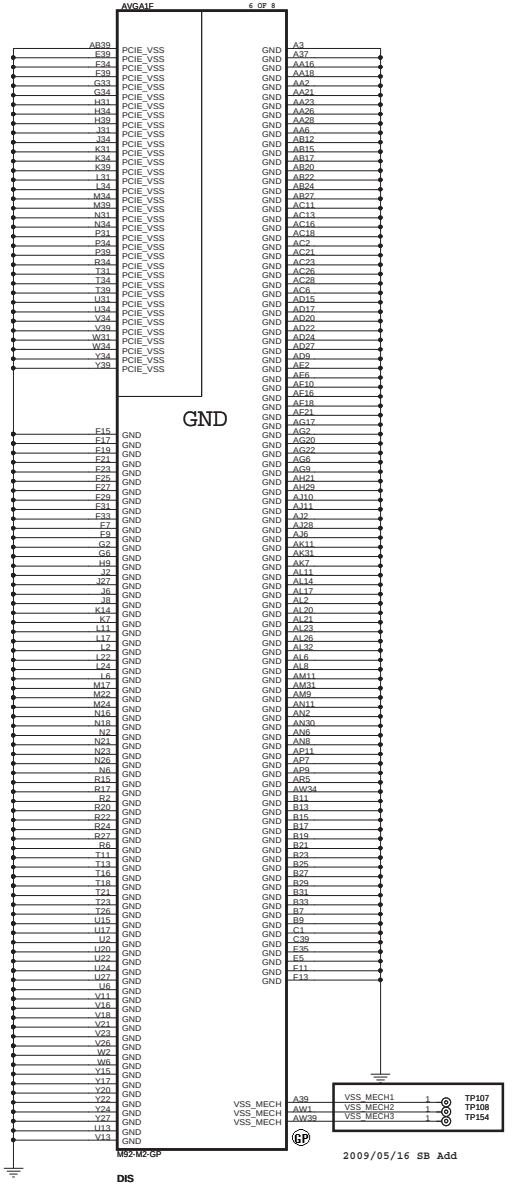
Date: Monday, July 06, 2009 | Sheet 53 of 61



UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	M92 POWER	
Size: A2	Document Number: JV71-TR	Rev: SA
Date: Monday, July 06, 2009	Sheet 54 of 61	

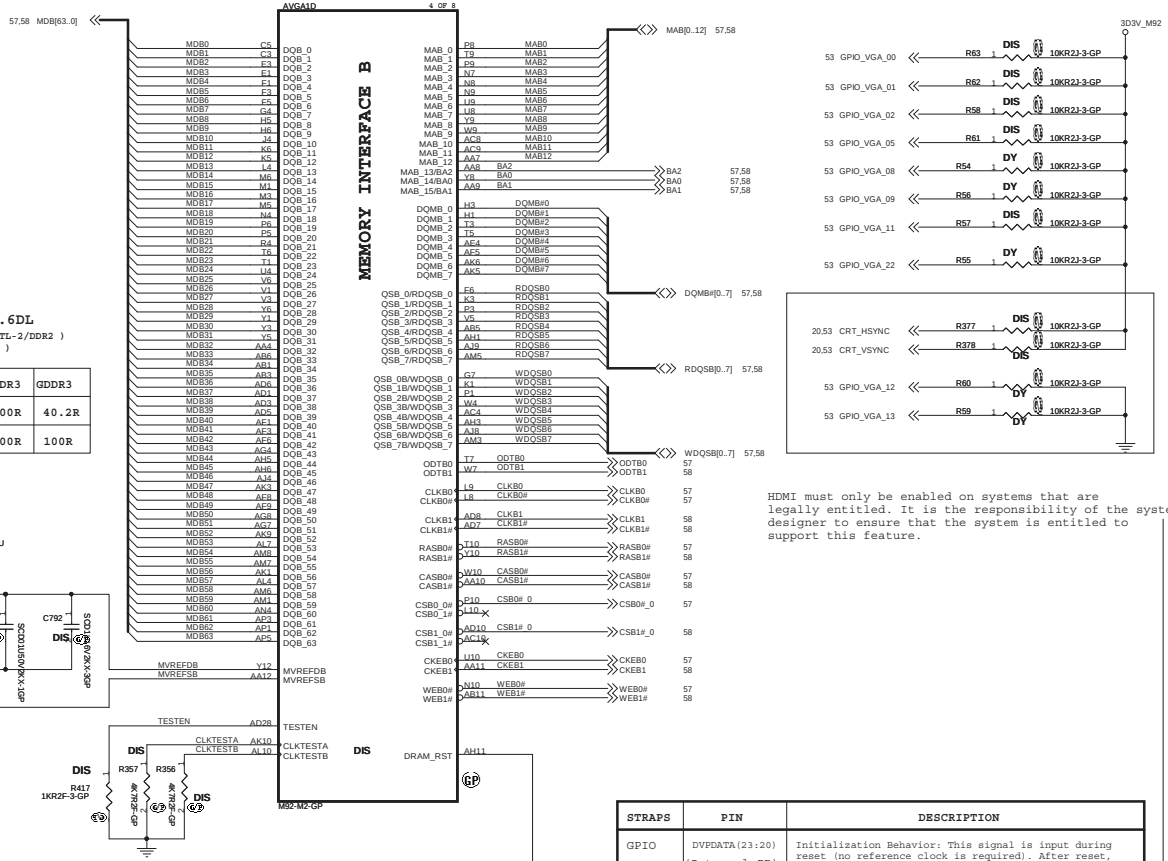




UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**DP POWER_GND**	
Size A2	Document Number **JV71-TR**	Rev **SA**
Date: Monday, July 06, 2009	Sheet 55 of 61	

M92-M2 uses memory group B only

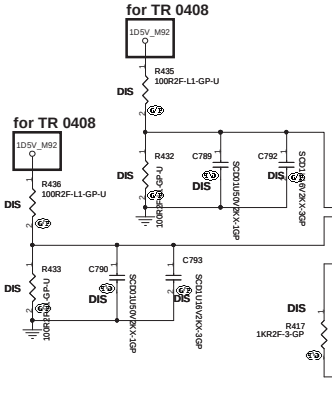


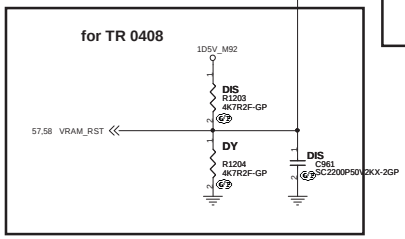
HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

40.2R PN:64.40R25.6DL

(0.5 * VDDR1) (for SSTL-1.8/SSTL-2/DDR2)
(0.7 * VDDR1) (for GDDR3/GDDR4)

DIVIDER RESISTORS	DDR2	DDR3	GDDR3
MVREF TO 1.8V	100R	100R	40.2R
MVREF TO GND	100R	100R	100R





STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.

AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET
H2SYNC, GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET
GPIO_28_TDO , GPIO21_BB_EN

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BIF_CLK_PM_EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory aperture size	X X X
PWRCNTL_[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	1
CCBYPASS	GENERICC		0

UMA

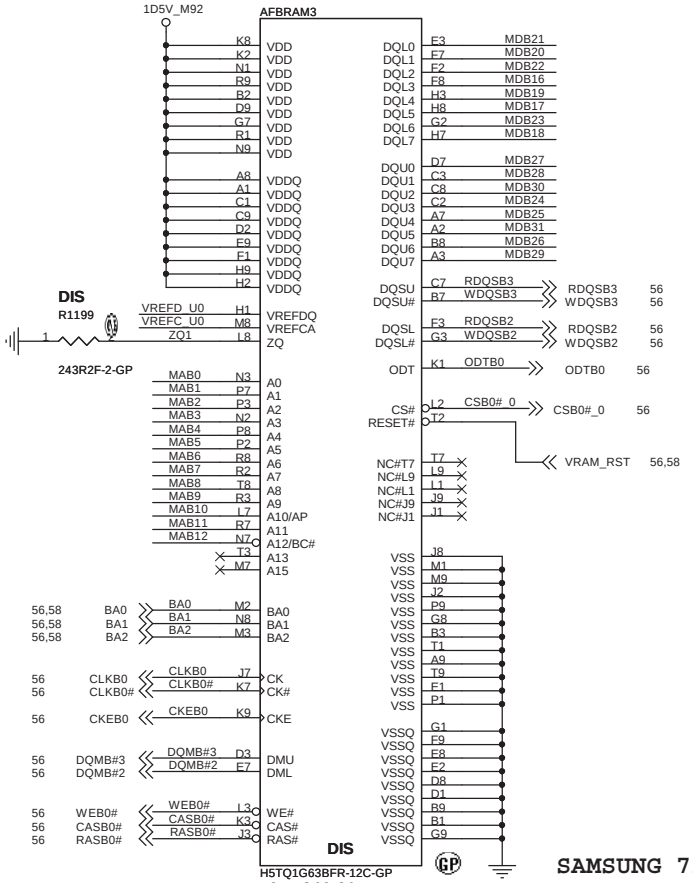
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

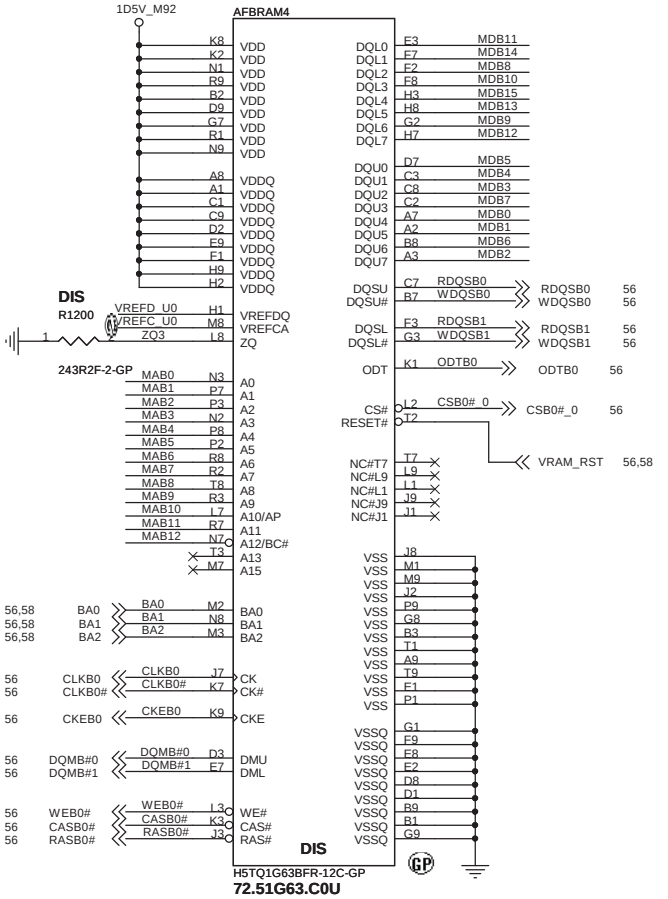
Title: Memory / Straps

Size: A2 | Document Number: JV71-TR | Rev: SA

Date: Monday, July 06, 2009 | Sheet 56 of 61

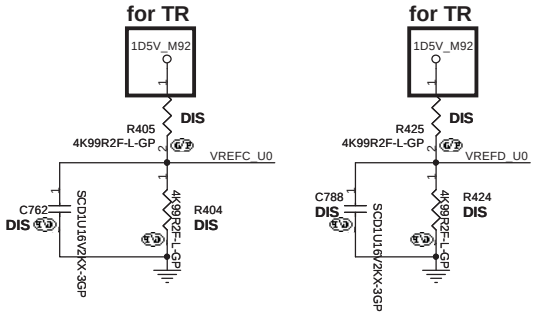
DDR3

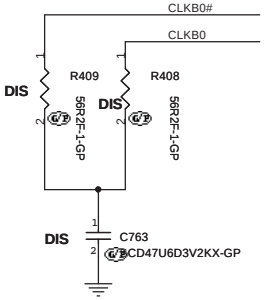


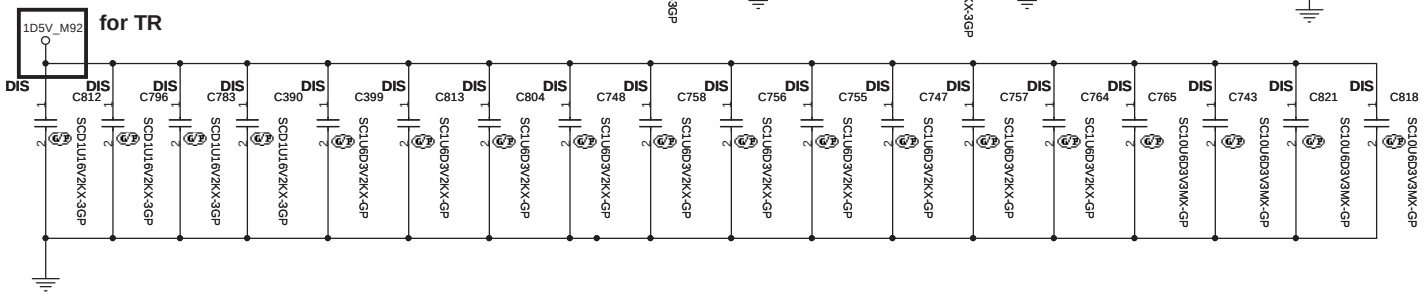


SAMSUNG 72.41164.H0U
HYUNIX 72.51G63.C0U

56,58 DQMB#[0..7]
56,58 RDQSB[0..7]
56,58 WDQSB[0..7]
56,58 MAB[0..12]
56,58 MDB[63..0]

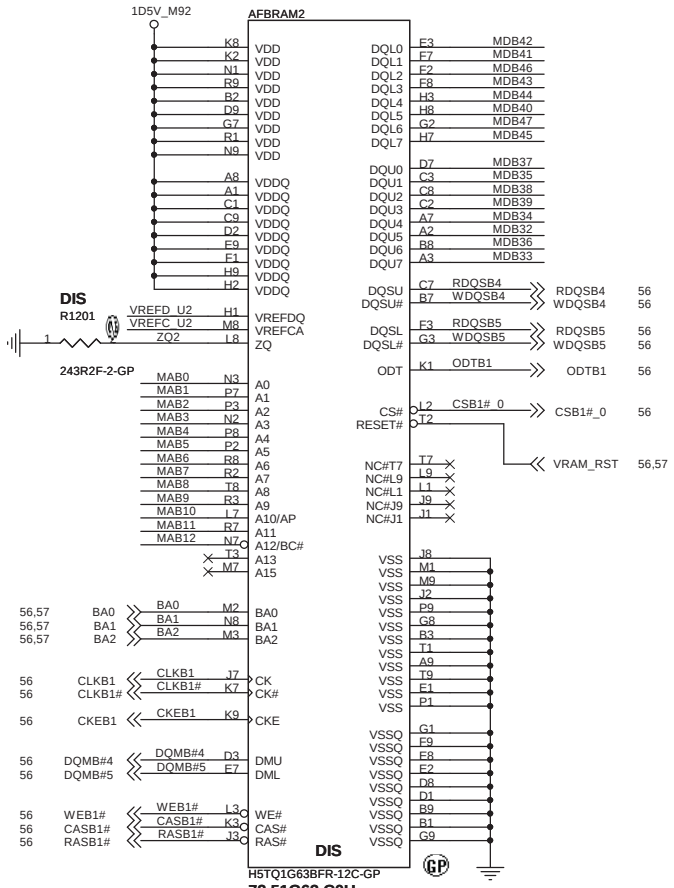


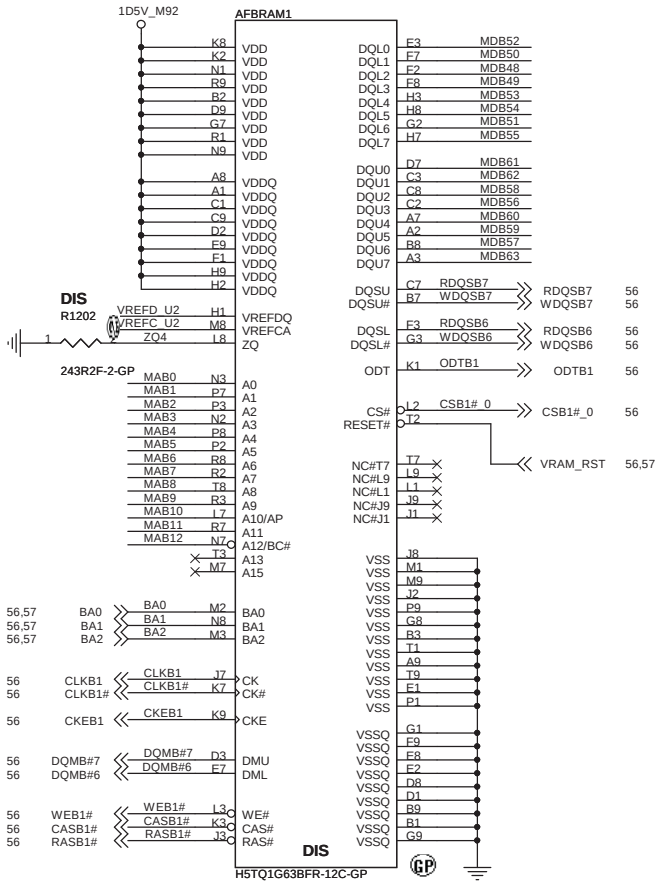




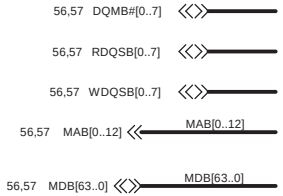
UMA

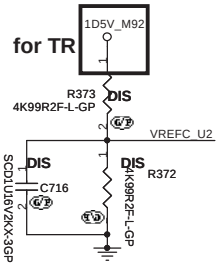
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DDR3 B0		
Size: A3	Document Number: JV71-TR	Rev: SB
Date: Monday, July 06, 2009	Sheet 57 of 61	

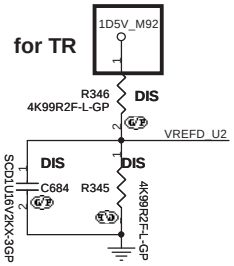


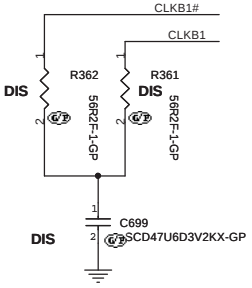


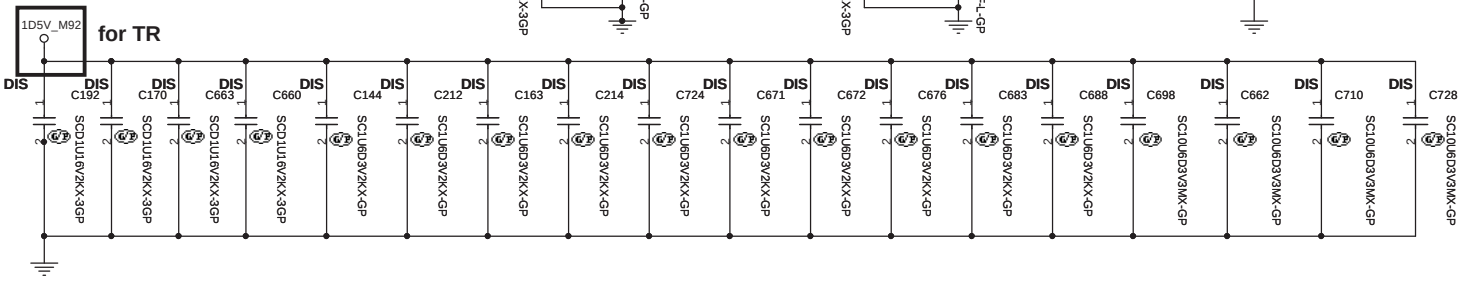
SAMSUNG 72.41164.H0U
HYUNIX 72.51G63.C0U







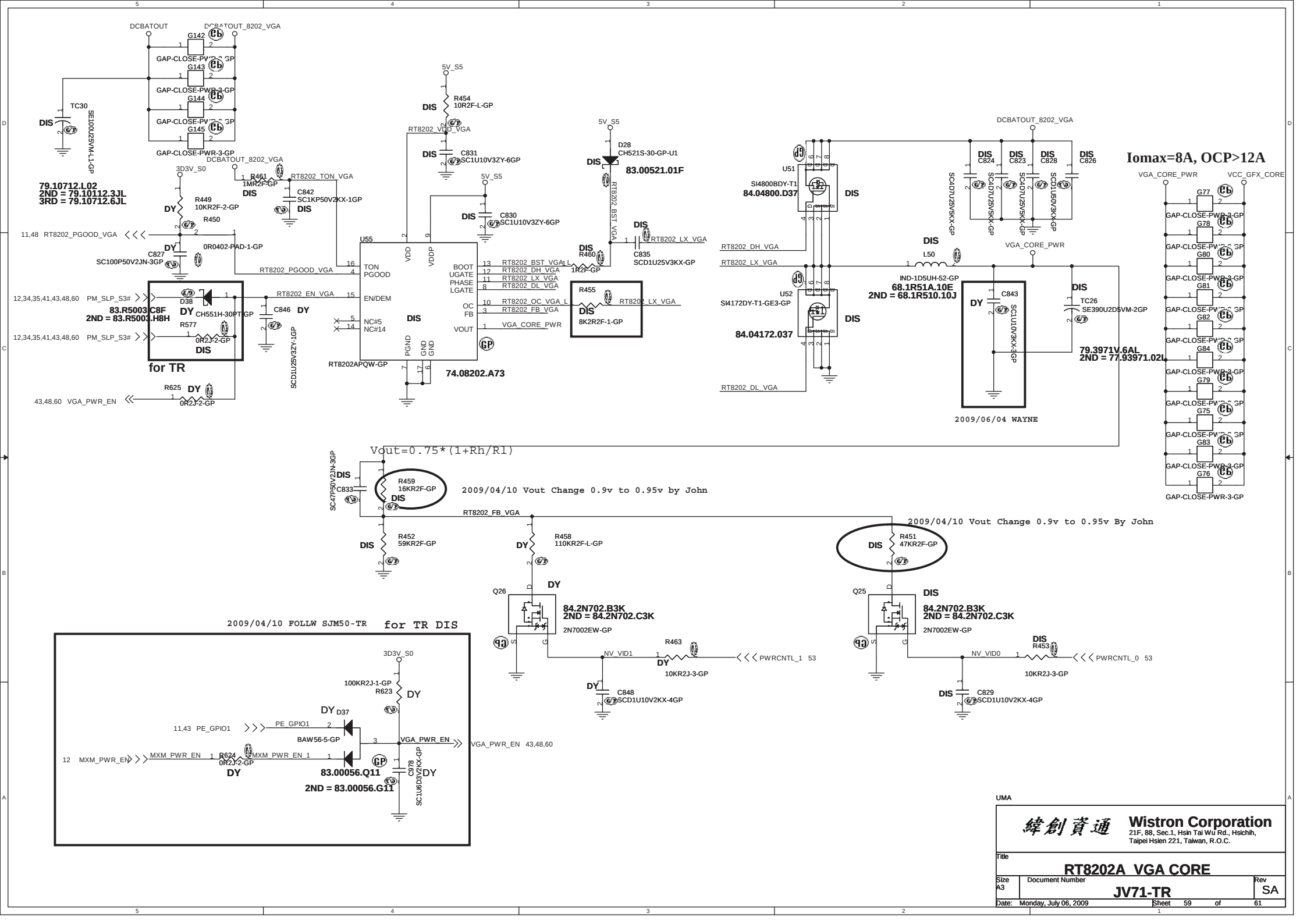




UMA

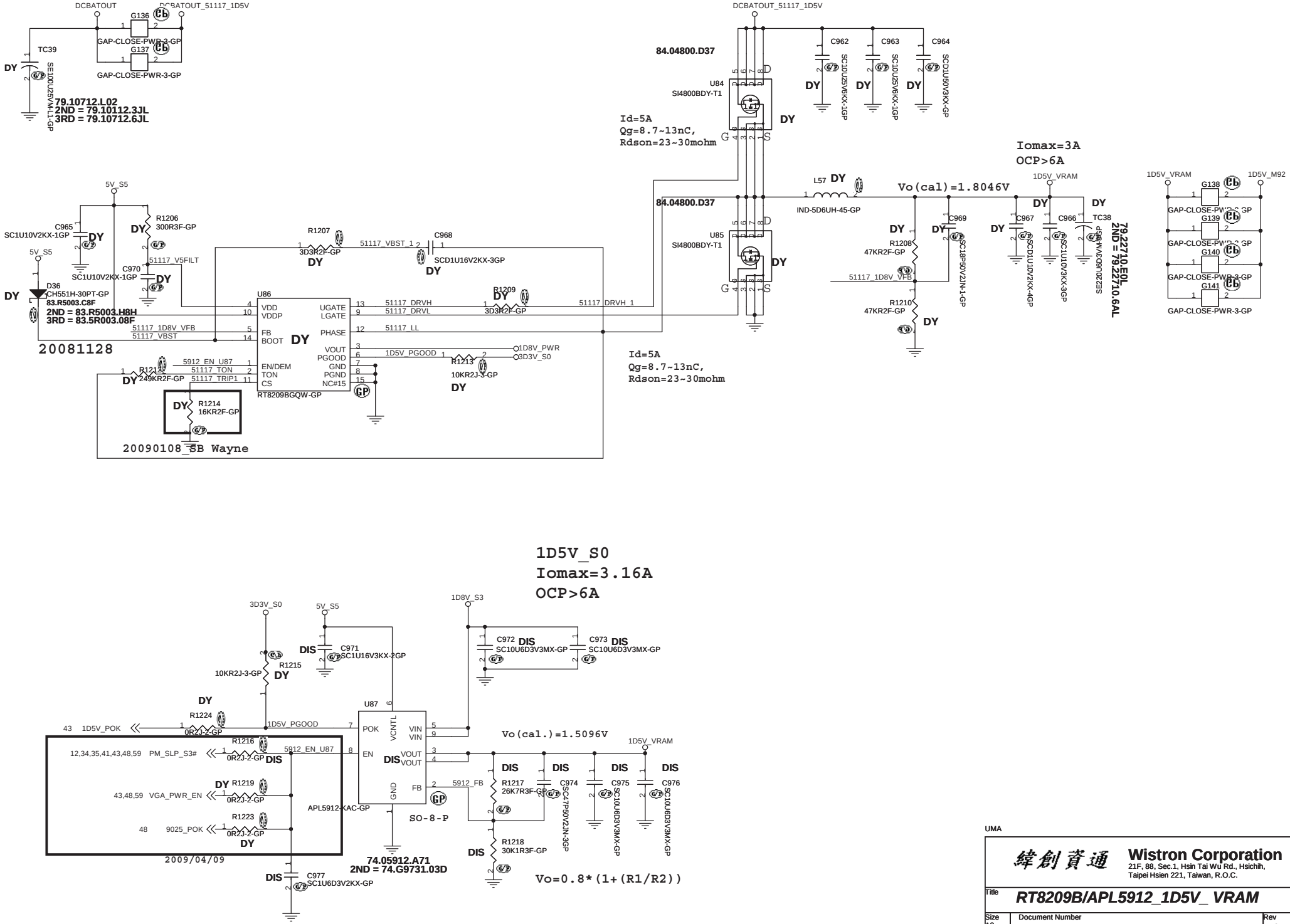
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	M92 DDR3 B1	
Size A3	Document Number JV71-TR	Rev SB
Date: Monday, July 06, 2009	Sheet 58 of 61	



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8202A VGA CORE		
Size: A3	Document Number: JV71-TR	Rev: SA
Date: Monday, July 06, 2009	Sheet 59 of 61	



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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
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Size: A3	Document Number: JV71-TR	Rev: SA
Date: Monday, July 06, 2009	Sheet 60 of 61	

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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Size	Document Number	Rev
A3	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 61 of 61