

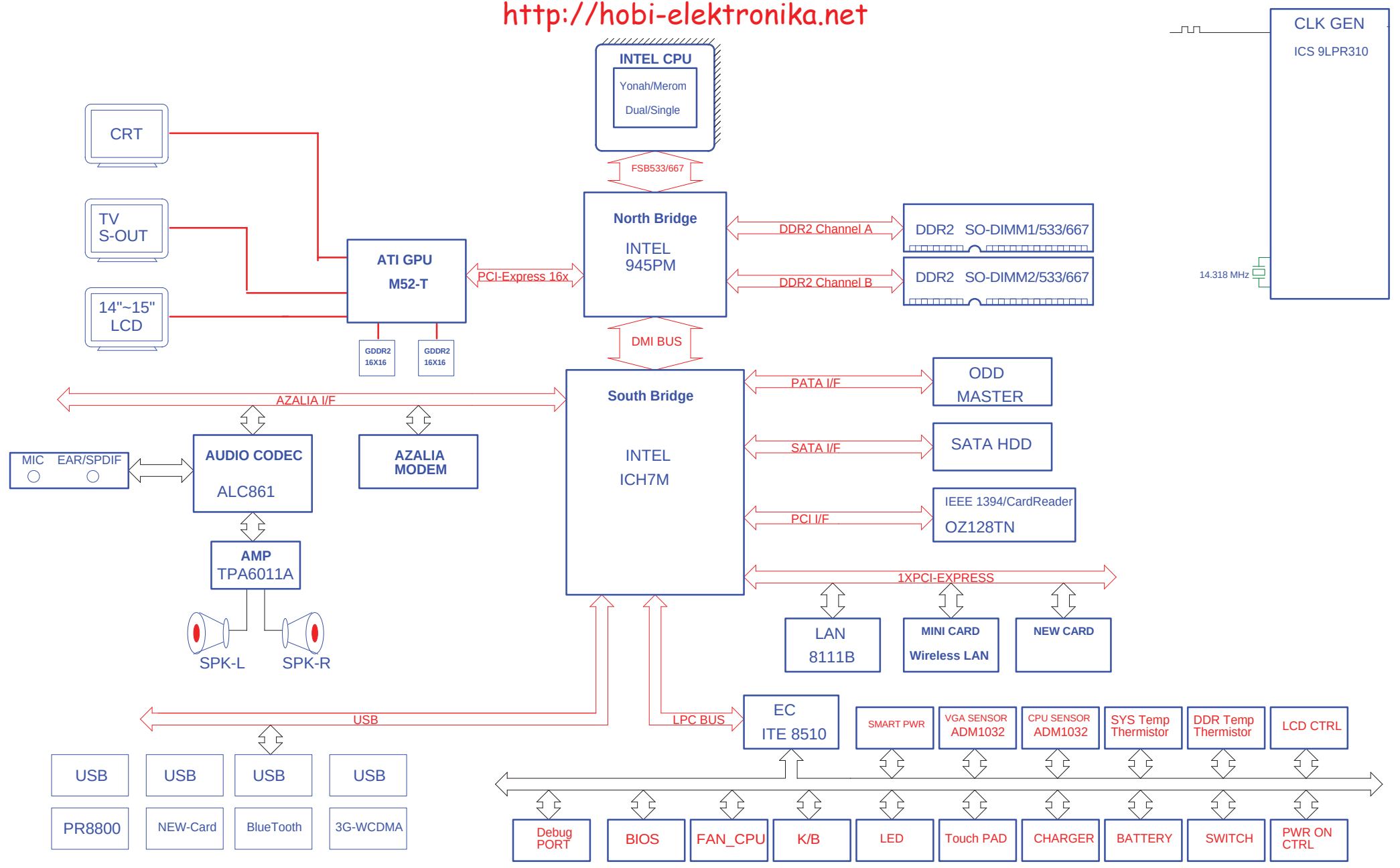
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9. NB(2)_DMI/Configuration/PM
10. NB(3)_VGA_TV_LVDS_PCIEx16* I/F
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23. FAN CTRL / SYS BIOS /SMART PWR
24. MINI CARD & NEW CARD
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26. Cardreader CONN
27. CRT CONN WITH PR8800
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29. +CPU CORE(MAX8771)
30. +1.5V&+1.8V(OZ813) & +2.5V(RT9173B)
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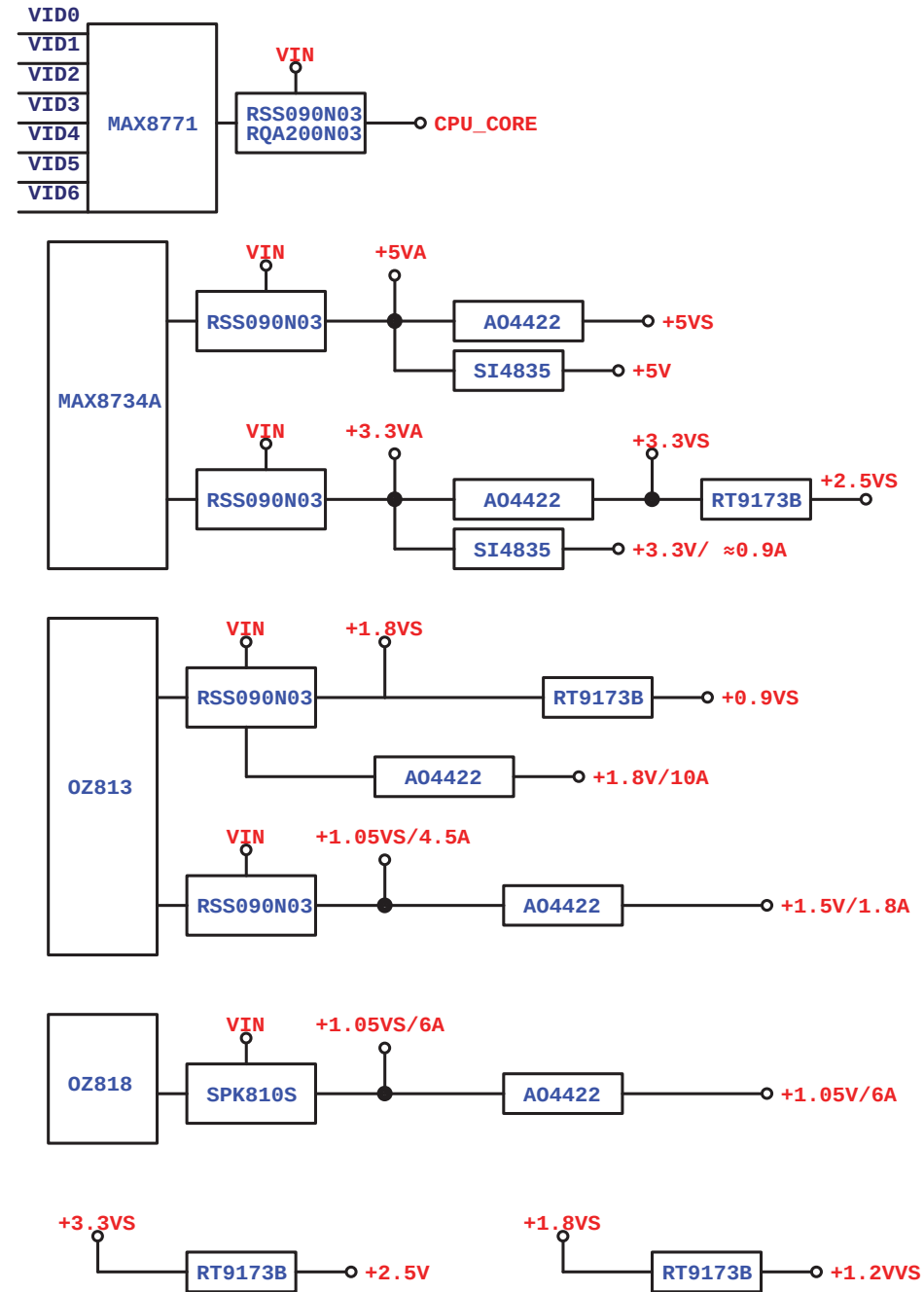
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47. AUDIO BD(3)(AMP/INTERNAL MIC)
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	PCB P/N	PCB ASSY P/N
S40II M/B	37GS50000-D0	
S50IA M/B(HYNIX)	37GS50000-D0	82GS50000-D0
S50IA M/B(SAM)	37GS50000-D0	82GS50000-??
S40 MODEM BD	35GNS4000-D0	
S50 MODEM BD	35GNS5000-D0	80GNS5000-D0
S40 SWITCH BD	35G5S5000-D0	
S50 SWITCH BD	35G5S5000-D0	80G5S5000-D0
S40 ODD BD	35GPS4000-D0	
S50 ODD BD	35GPS5000-D0	80GPS5000-D0
TOUCH PAD	35G8S5000-D0	80G8S5000-D0
AUDIO BD	35G2S5000-D0	80G2S5000-D0
3G BD	35GKS5000-D0	80GKS5000-D0

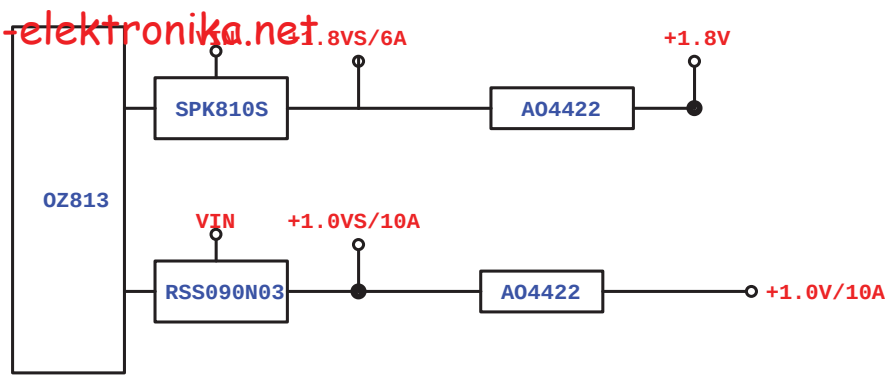
Name of Part		Cover Page	
Project	S50IA Main Board		Rev D
Date: Monday, July 10, 2006	Sheet	1 / 49	
3255	UNIWill COMPUTER CORP.		



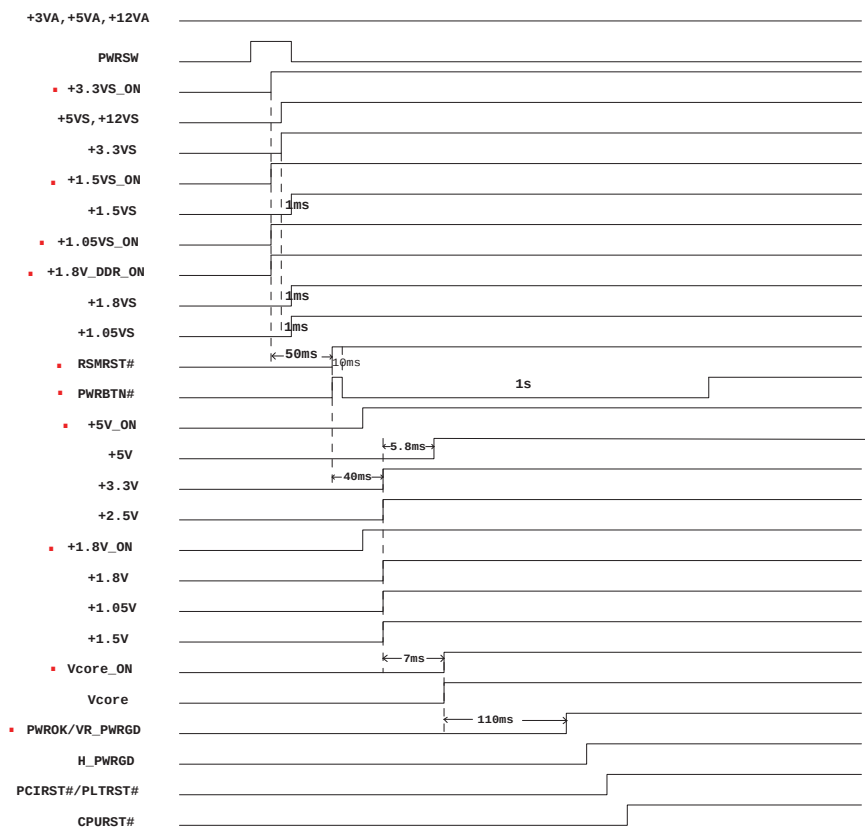
POWER BLOCK DIAGRAM



<http://hobi-elektronika.net>



POWER Sequence



POWER DIAGRAM & SEQUENCE		
Name of Project	S501A Main Board	
Project	Rev	D
Date: Monday, July 10, 2006	Sheet	3 / 49
UNIWILL COMPUTER CORP.		
3255		

ICH7-M GPIO	
GPI0	BM_BUSY#
GPI9	EC_EXTSMI#
GPI11	SMB_ALERT#
GPI12	PNLSW0
GPI13	PNLSW1
GPI14	PNLSW2
GP016	PM DPRSLPVR
GP018	PM_STPPCI#
GP020	PM_STPCPU#
GP021	
GP023	
GPI024	
GPI025	
GPI026	
GPI027	
GPI028	
GPI029	
GPI030	
GPI031	
GPI032	PM_CLKRUN#
GPI033	
GPI034	

ITE8510E GPIO	
GPCF0	RF_SW#
GPCF1	SILENT#
GPCF2	NEW_CARD_PWR_ON#
GPCF3	NA
GPCF4	TP_CLK
GPCF5	TP_DATA
GPCF6	3G_ON
GPCF7	NA
GPI0	SCROLL
GPI1	CAPS
GPI2	NUM
GPI3	CHG_R_LED#
GPI4	CHG_G_LED#
GPI5	PWRON_LED
GPI6	+1.8V_VGA_ON
GPH0	+1.8VS_ON
GPH1	+1.8V_ON
GPH2	+1.05VS_ON
GPH3	+3.3VS_ON
GPH4	+5V_ON
GPH5	SET_V
GPH6	+1.5VS_ON
GPH7	VCORE_ON
GP64	BT_ON
GP65	+VGA_CORE_ON
GP66	AMP_MUTE#
GP67	EXTTS#0
GPB0	C4_OUT
GPB1	CPPE#
GPB2	PM_RSMRST#
GPB3	BAT_SMBCLK
GPB4	BAT_SMBDAT
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	RFLED_ON
GPE0	NA
GPE1	EC_CPU_BSEL1
GPE2	NA
GPE3	NA
GPE4	EC_PWR_ON
GPE5	LID#
GPE6	NA
GPE7	PM_SLP_S3#
GPD0	ADAP_IN
GPD1	LCDSW
GPD2	PCI_RST#/PLT_RST#
GPD3	EC_EXTSMI#
GPD4	PM_SLP_S4#
GPD5	PM_THROTTLING#
GPD6	AUTO_C4#
GPD7	EC_PREST#
GPA0	BT1_BEEP
GPA1	EC_VID1
GPA2	EC_VID2
GPA3	EC_VID3
GPA4	EC_VID4
GPA5	EC_VID5
GPA6	SMP2_EN#
GPA7	PWRBTN#

ITE8510E GPIO	
GPC0	PWROK
GPC1	SMBCLK_EC
GPC2	SMBDAT_EC
GPC3	FPWROK
GPC4	BROWSER#
GPC5	C4_OUT#
GPC6	CHG_ON
GPC7	SILENT_LED
ADC0	BAT_TEMP
ADC1	ADAPTOR_I
ADC2	DDR2_TEMP
ADC3	VGA_TEMP
DA0	BRIGHTADJ
DA1	CHG_I
DA2	FAN_CTRL0
DA3	NA

CPU				
CPU CORE(V)	ICC(A)	W	TEMP()	
2.0G	1.25	36	44	69
1.5G	1.25	36	44	70
1.67G	1.25	36	44	70
1.83G	1.25	36	44	71
2.0G	1.25	36	44	72
2.16G	1.25	36	44	72
2.33G	1.25	36	44	72
2.66G	1.525	43.35	66.1	74
2.8G	1.525	44.86	68.4	75
3.06G	1.525	55.9	85.2	81

GMCH			
VCC	ICC(A)	W	TEMP()
+3.3V	0.12	0.396	70
+2.5V	0.6	1.500	
+1.8V	5.1	9.18	
+1.5V	1.544	2.316	
+VTT	0.8	0.84	
+VCC_DRCL_CORE	1.5	0.75	

ICH7-M			
VCC	ICC(A)	W	TEMP()
+5VS	0.016	0.08	70
+3.3VS	0.35	1.155	
+3.3V	1.0	3.3	
+1.5V	4.38	6.57	
+1.05V	1.5	1.575	
+3.3VA_RTC	0.003	0.00001	

ITE8510E			
VCC	ICC(mA)	W	TEMP()
+3.3V	300	1	70

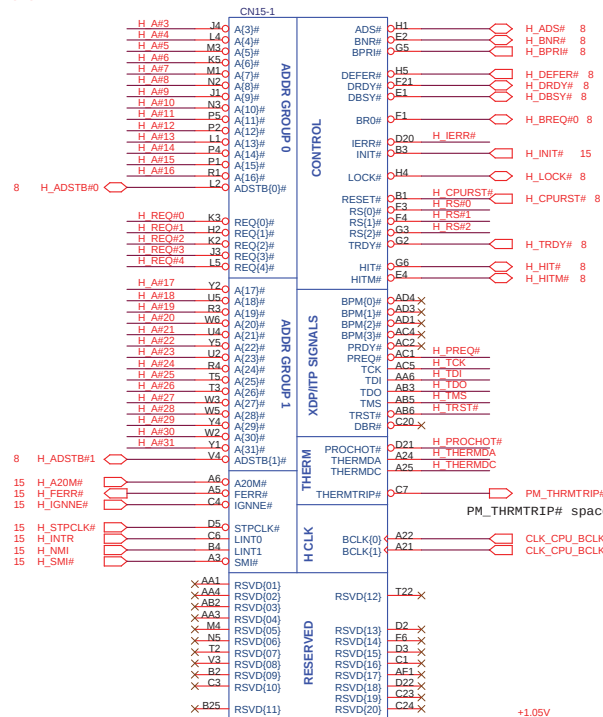
CLOCK GENERATOR			
VCC	ICC(mA)	W	TEMP()
+3.3V	180	0.594	70

ALC861			
VCC	ICC(mA)	W	TEMP()
+3.3V(DVDD)	71	0.234	70

TPA6011A4			
VCC	ICC(mA)	W	TEMP()
3.3V	30	0.099W	85

ADM1032			
VCC	ICC	W	TEMP()
+3.3V	170uA	0.56mW	150

8 H_A#13[3]
8 H_REQ#0[4:0]
8 H_RS#2[0]



Layout note: 0.5" max length.

9/23 review

9.21 CPU_BSEL1

CPU_BSEL0 B22

CPU_BSEL1 B23

CPU_BSEL2 C21

BSEL(0)

BSEL(1)

BSEL(2)

TEST1

TEST2

GTREF

AD26

H_TES1

H_TES2

D25

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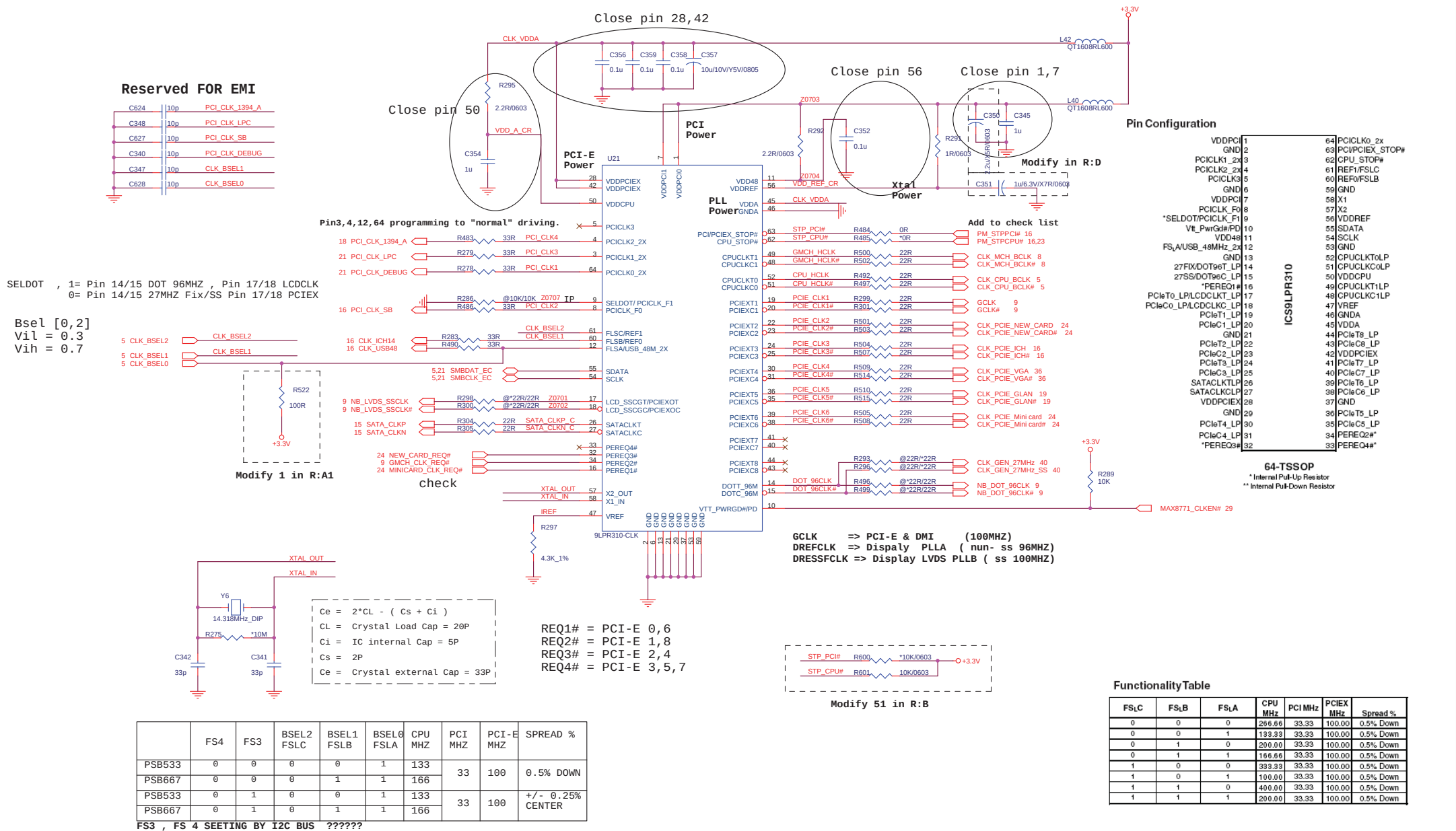
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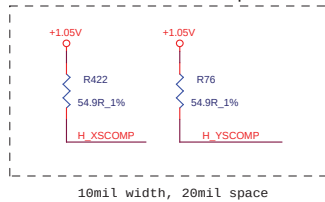
D298



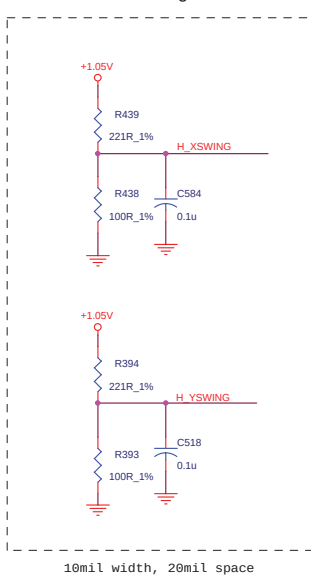
FS _L C	FS _L B	FS _L A	CPU MHz	PCI MHz	PCIEx MHz	Spread %
0	0	0	266.66	33.33	100.00	0.5% Down
0	0	1	133.33	33.33	100.00	0.5% Down
0	1	0	200.00	33.33	100.00	0.5% Down
0	1	1	166.66	33.33	100.00	0.5% Down
1	0	0	333.33	33.33	100.00	0.5% Down
1	0	1	100.00	33.33	100.00	0.5% Down
1	1	0	400.00	33.33	100.00	0.5% Down
1	1	1	200.00	33.33	100.00	0.5% Down

U11J			
AT23	VSS_180	J11	VSS_273
AN23	VSS_181	D11	VSS_274
AM23	VSS_182	B11	VSS_275
AC23	VSS_183	AV10	VSS_276
W23	VSS_185	AP10	VSS_277
K23	VSS_186	AL10	VSS_278
J23	VSS_187	AG10	VSS_279
F23	VSS_188	AC10	VSS_280
C23	VSS_189	W10	VSS_281
AA22	VSS_190	U10	VSS_282
K22	VSS_191	BA9	VSS_283
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AB9
E22	VSS_194	VSS_287	AG9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	G9
AV21	VSS_198	VSS_291	E9
AR21	VSS_199	VSS_292	AG8
AN21	VSS_200	VSS_293	AD8
AL21	VSS_201	VSS_294	AA8
AK21	VSS_202	VSS_295	VSS_296
Y21	VSS_203	VSS_297	VSS_298
K21	VSS_204	VSS_299	VSS_300
J21	VSS_205	VSS_301	VSS_302
H21	VSS_206	VSS_303	VSS_304
C21	VSS_207	VSS_305	VSS_306
AW20	VSS_208	VSS_307	VSS_308
AR20	VSS_209	VSS_309	VSS_310
AA20	VSS_210	VSS_311	VSS_312
B20	VSS_211	VSS_313	VSS_314
K20	VSS_212	VSS_315	VSS_316
A20	VSS_213	VSS_317	VSS_318
AN19	VSS_214	VSS_319	VSS_320
AC19	VSS_215	VSS_321	VSS_322
W19	VSS_216	VSS_323	VSS_324
K19	VSS_217	VSS_325	VSS_326
J19	VSS_218	VSS_327	VSS_328
G19	VSS_219	VSS_329	VSS_330
F19	VSS_220	VSS_331	VSS_332
E19	VSS_221	VSS_333	VSS_334
D19	VSS_222	VSS_335	VSS_336
C19	VSS_223	VSS_337	VSS_338
B19	VSS_224	VSS_339	VSS_340
A19	VSS_225	VSS_341	VSS_342
AY17	VSS_226	VSS_343	VSS_344
AV17	VSS_227	VSS_345	VSS_346
AM17	VSS_228	VSS_347	VSS_348
AC17	VSS_229	VSS_349	VSS_350
W17	VSS_230	VSS_351	VSS_352
K17	VSS_231	VSS_353	VSS_354
A17	VSS_232	VSS_355	VSS_356
AN16	VSS_233	VSS_357	VSS_358
AC16	VSS_234	VSS_359	VSS_360
W16	VSS_235		
K16	VSS_236		
J16	VSS_237		
F16	VSS_238		
E16	VSS_239		
D16	VSS_240		
C16	VSS_241		
B16	VSS_242		
A16	VSS_243		
AY15	VSS_244		
AV15	VSS_245		
AM15	VSS_246		
AC15	VSS_247		
W15	VSS_248		
K15	VSS_249		
J15	VSS_250		
F15	VSS_251		
E15	VSS_252		
D15	VSS_253		
C15	VSS_254		
B15	VSS_255		
A15	VSS_256		
AY14	VSS_257		
AV14	VSS_258		
AM14	VSS_259		
AC14	VSS_260		
W14	VSS_261		
K14	VSS_262		
J14	VSS_263		
F14	VSS_264		
E14	VSS_265		
D14	VSS_266		
C14	VSS_267		
B14	VSS_268		
A14	VSS_269		
AY13	VSS_270		
AV13	VSS_271		
AM13	VSS_272		
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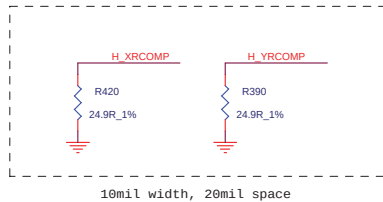
FSB I/O slew rate compensation



Reference Voltage for RCOMP



Calibration FSB I/O Buffer



H_DW0	F1	H_DW#_0	
H_DW1	J1	H_DW#_1	
H_DW2	H1	H_DW#_2	
H_DW3	D1	H_DW#_3	
H_DW4	J6	H_DW#_4	
H_DW5	K2	H_DW#_5	
H_DW6	G1	H_DW#_6	
H_DW7	C2	H_DW#_7	
H_DW8	K9	H_DW#_8	
H_DW9	K1	H_DW#_9	
H_DW10	J2	H_DW#_10	
H_DW11	K7	H_DW#_11	
H_DW12	J8	H_DW#_12	
H_DW13	J3	H_DW#_13	
H_DW14	K11	H_DW#_14	
H_DW15	G4	H_DW#_15	
H_DW16	T10	H_DW#_16	
H_DW17	W11	H_DW#_17	
H_DW18	T3	H_DW#_18	
H_DW19	U7	H_DW#_19	
H_DW20	U9	H_DW#_20	
H_DW21	U11	H_DW#_21	
H_DW22	T11	H_DW#_22	
H_DW23	W9	H_DW#_23	
H_DW24	T8	H_DW#_24	
H_DW25	T7	H_DW#_25	
H_DW26	T4	H_DW#_26	
H_DW27	W7	H_DW#_27	
H_DW28	U6	H_DW#_28	
H_DW29	T9	H_DW#_29	
H_DW30	W6	H_DW#_30	
H_DW31	T5	H_DW#_31	
H_DW32	AB7	H_DW#_32	
H_DW33	AA9	H_DW#_33	
H_DW34	WA	H_DW#_34	
H_DW35	W3	H_DW#_35	
H_DW36	Y3	H_DW#_36	
H_DW37	Y7	H_DW#_37	
H_DW38	W5	H_DW#_38	
H_DW39	Y10	H_DW#_39	
H_DW40	AB8	H_DW#_40	
H_DW41	W2	H_DW#_41	
H_DW42	AA4	H_DW#_42	
H_DW43	AA7	H_DW#_43	
H_DW44	AA2	H_DW#_44	
H_DW45	AA6	H_DW#_45	
H_DW46	AA10	H_DW#_46	
H_DW47	Y8	H_DW#_47	
H_DW48	AA1	H_DW#_48	
H_DW49	AB4	H_DW#_49	
H_DW50	AC9	H_DW#_50	
H_DW51	AB11	H_DW#_51	
H_DW52	AC11	H_DW#_52	
H_DW53	AB3	H_DW#_53	
H_DW54	AC2	H_DW#_54	
H_DW55	AD1	H_DW#_55	
H_DW56	AC9	H_DW#_56	
H_DW57	AC1	H_DW#_57	
H_DW58	AD7	H_DW#_58	
H_DW59	AC8	H_DW#_59	
H_DW60	AB5	H_DW#_60	
H_DW61	AD10	H_DW#_61	
H_DW62	AD4	H_DW#_62	
H_DW63	AC8	H_DW#_63	

H_XRCOMP	E1	H_XRCOMP	
H_XSCOMP	E2	H_XSCOMP	
H_XSWING	E4	H_XSWING	

H_YRCOMP	Y1	H_YRCOMP	
H_YSCOMP	U1	H_YSCOMP	
H_YSWING	W1	H_YSWING	

7 CLK_MCH_BCLK	AG2	H_CLKIN	
7 CLK_MCH_BCLK#	AG1	H_CLKIN#	

HOST

H_A#_3	H9	H_A#3	
H_A#_4	C9	H_A#4	
H_A#_5	E11	H_A#5	
H_A#_6	G11	H_A#6	
H_A#_7	F11	H_A#7	
H_A#_8	G12	H_A#8	
H_A#_9	F9	H_A#9	
H_A#_10	H11	H_A#10	
H_A#_11	H12	H_A#11	
H_A#_12	G14	H_A#12	
H_A#_13	D9	H_A#13	
H_A#_14	H14	H_A#14	
H_A#_15	H13	H_A#15	
H_A#_16	H15	H_A#16	
H_A#_17	F14	H_A#17	
H_A#_18	D12	H_A#18	
H_A#_19	A11	H_A#19	
H_A#_20	C11	H_A#20	
H_A#_21	A12	H_A#21	
H_A#_22	A13	H_A#22	
H_A#_23	E13	H_A#23	
H_A#_24	G13	H_A#24	
H_A#_25	F12	H_A#25	
H_A#_26	B12	H_A#26	
H_A#_27	R14	H_A#27	
H_A#_28	C12	H_A#28	
H_A#_29	A14	H_A#29	
H_A#_30	C14	H_A#30	
H_A#_31	D14	H_A#31	

H_ADS#	E8	H_ADS#_5	
H_ADSTB#_0	B9	H_ADSTB#0_5	
H_ADSTB#_1	C13	H_ADSTB#1_5	
H_VREF	I13	H_VREF	
H_BNR#	C6	H_BNR#_5	
H_BREQ#0	C7	H_BREQ#0_5	
H_CPURST#	B7	H_CPURST#_5	
H_DESY#	A7	H_DESY#_5	
H_DEFER#	C3	H_DEFER#_5	
H_DPWR#	J9	H_DPWR#_5	
H_DRDY#	H8	H_DRDY#_5	
H_VREF	K13	H_VREF	

H_DIN#_0	J7	H_DIN#0_5	
H_DIN#_1	W8	H_DIN#1_5	
H_DIN#_2	U3	H_DIN#2_5	
H_DIN#_3	AB10	H_DIN#3_5	

H_DSTBN#0	K4	H_DSTBN#0_5	
H_DSTBN#1	T7	H_DSTBN#1_5	
H_DSTBN#2	Y5	H_DSTBN#2_5	
H_DSTBN#3	AC4	H_DSTBN#3_5	

H_DSTBP#_0	K3	H_DSTBP#0_5	
H_DSTBP#_1	T6	H_DSTBP#1_5	
H_DSTBP#_2	AA5	H_DSTBP#2_5	
H_DSTBP#_3	AC5	H_DSTBP#3_5	

H_HIT#	D3	H_HIT#_5	
H_HITM#	D4	H_HITM#_5	
H_LOCK#	B3	H_LOCK#_5	

H_REQ#_0	D8	H_REQ#0_5	
H_REQ#_1	G8	H_REQ#1_5	
H_REQ#_2	B8	H_REQ#2_5	
H_REQ#_3	F8	H_REQ#3_5	
H_REQ#_4	A8	H_REQ#4_5	

H_RS#_0	B4	H_RS#0_5	
H_RS#_1	E6	H_RS#1_5	
H_RS#_2	D6	H_RS#2_5	

H_SLP#	E7	H_CPUSLP#_GMCH	
H_TRDY#	F3	H_CPUSLP#_5,15	

H_ADS#	E8	H_ADS#_5	
H_ADSTB#_0	B9	H_ADSTB#0_5	
H_ADSTB#_1	C13	H_ADSTB#1_5	
H_VREF	I13	H_VREF	
H_BNR#	C6	H_BNR#_5	
H_BREQ#0	C7	H_BREQ#0_5	
H_CPURST#	B7	H_CPURST#_5	
H_DESY#	A7	H_DESY#_5	
H_DEFER#	C3	H_DEFER#_5	
H_DPWR#	J9	H_DPWR#_5	
H_DRDY#	H8	H_DRDY#_5	
H_VREF	K13	H_VREF	

H_DIN#_0	J7	H_DIN#0_5	
H_DIN#_1	W8	H_DIN#1_5	
H_DIN#_2	U3	H_DIN#2_5	
H_DIN#_3	AB10	H_DIN#3_5	

H_DSTBN#0	K4	H_DSTBN#0_5	
H_DSTBN#1	T7	H_DSTBN#1_5	
H_DSTBN#2	Y5	H_DSTBN#2_5	
H_DSTBN#3	AC4	H_DSTBN#3_5	

H_DSTBP#_0	K3	H_DSTBP#0_5	
H_DSTBP#_1	T6	H_DSTBP#1_5	
H_DSTBP#_2	AA5	H_DSTBP#2_5	
H_DSTBP#_3	AC5	H_DSTBP#3_5	

H_HIT#	D3	H_HIT#_5	
H_HITM#	D4	H_HITM#_5	
H_LOCK#	B3	H_LOCK#_5	

H_REQ#_0	D8	H_REQ#0_5	
H_REQ#_1	G8	H_REQ#1_5	
H_REQ#_2	B8	H_REQ#2_5	
H_REQ#_3	F8	H_REQ#3_5	
H_REQ#_4	A8	H_REQ#4_5	

H_RS#_0	B4	H_RS#0_5	
H_RS#_1	E6	H_RS#1_5	
H_RS#_2	D6	H_RS#2_5	

H_SLP#	E7	H_CPUSLP#_GMCH	
H_TRDY#	F3	H_CPUSLP#_5,15	

H_ADS#	E8	H_ADS#_5	
H_ADSTB#_0	B9	H_ADSTB#0_5	
H_ADSTB#_1	C13	H_ADSTB#1_5	
H_VREF	I13	H_VREF	
H_BNR#	C6	H_BNR#_5	
H_BREQ#0	C7	H_BREQ#0_5	
H_CPURST#	B7	H_CPURST#_5	
H_DESY#	A7	H_DESY#_5	
H_DEFER#	C3	H_DEFER#_5	
H_DPWR#	J9	H_DPWR#_5	
H_DRDY#	H8	H_DRDY#_5	
H_VREF	K13	H_VREF	

H_DIN#_0	J7	H_DIN#0_5	
H_DIN#_1	W8	H_DIN#1_5	
H_DIN#_2	U3	H_DIN#2_5	
H_DIN#_3	AB10	H_DIN#3_5	

H_DSTBN#0	K4	H_DSTBN#0_5	
H_DSTBN#1	T7	H_DSTBN#1_5	
H_DSTBN#2	Y5	H_DSTBN#2_5	
H_DSTBN#3	AC4	H_DSTBN#3_5	

H_DSTBP#_0	K3	H_DSTBP#0_5	
H_DSTBP#_1	T6	H_DSTBP#1_5	
H_DSTBP#_2	AA5	H_DSTBP#2_5	
H_DSTBP#_3	AC5	H_DSTBP#3_5	

H_HIT#	D3	H_HIT#_5	
H_HITM#	D4	H_HITM#_5	
H_LOCK#	B3	H_LOCK#_5	

H_REQ#_0	D8	H_REQ#0_5	
H_REQ#_1	G8	H_REQ#1_5	
H_REQ#_2	B8	H_REQ#2_5	
H_REQ#_3	F8	H_REQ#3_5	
H_REQ#_4	A8	H_REQ#4_5	

H_RS#_0	B4	H_RS#0_5	
H_RS#_1	E6	H_RS#1_5	
H_RS#_2	D6	H_RS#2_5	

H_SLP#	E7	H_CPUSLP#_GMCH	
H_TRDY#	F3	H_CPUSLP#_5,15	

H_ADS#	E8	H_ADS#_5	
H_ADSTB#_0	B9	H_ADSTB#0_5	
H_ADSTB#_1	C13	H_ADSTB#1_5	
H_VREF	I13	H_VREF	
H_BNR#	C6	H_BNR#_5	
H_BREQ#0	C7	H_BREQ#0_5	
H_CPURST#	B7	H_CPURST#_5	
H_DESY#	A7	H_DESY#_5	
H_DEFER#	C3	H_DEFER#_5	
H_DPWR#	J9	H_DPWR#_5	
H_DRDY#	H8	H_DRDY#_5	
H_VREF	K13	H_VREF	

H_DIN#_0	J7	H_DIN#0_5	
H_DIN#_1	W8	H_DIN#1_5	
H_DIN#_2	U3	H_DIN#2_5	
H_DIN#_3	AB10	H_DIN#3_5	

H_DSTBN#0	K4	H_DSTBN#0_5	
H_DSTBN#1	T7	H_DSTBN#1_5	
H_DSTBN#2	Y5	H_DSTBN#2_5	
H_DSTBN#3	AC4	H_DSTBN#3_5	

H_DSTBP#_0	K3	H_DSTBP#0_5	
H_DSTBP#_1	T6	H_DSTBP#1_5	
H_DSTBP#_2	AA5	H_DSTBP#2_5	
H_DSTBP#_3	AC5	H_DSTBP#3_5	

H_HIT#	D3	H_HIT#_5	
H_HITM#	D4	H_HITM#_5	
H_LOCK#	B3	H_LOCK#_5	

H_REQ#_0	D8	H_REQ#0_5	
H_REQ#_1	G8	H_REQ#1_5	
H_REQ#_2	B8	H_REQ#2_5	
H_REQ#_3	F8	H_REQ#3_5	
H_REQ#_4	A8	H_REQ#4_5	

H_RS#_0	B4	H_RS#0_5	
H_RS#_1	E6	H_RS#1_5	
H_RS#_2	D6	H_RS#2_5	

H_SLP#	E7	H_CPUSLP#_GMCH	
H_TRDY#	F3	H_CPUSLP#_5,15	

H_ADS#	E8	H_ADS#_5	
H_ADSTB#_0	B9	H_ADSTB#0_5	
H_ADSTB#_1	C13	H_ADSTB#1_5	
H_VREF	I13	H_VREF	
H_BNR#	C6	H_BNR#_5	
H_BREQ#0	C7	H_BREQ#0_5	
H_CPURST#	B7	H_CPURST#_5	
H_DESY#	A7	H_DESY#_5	
H_DEFER#	C3	H_DEFER#_5	
H_DPWR#	J9	H_DPWR#_5	
H_DRDY#	H8	H_DRDY#_5	
H_VREF	K13	H_VREF	

H_DIN#_0	J7	H_DIN#0_5	
H_DIN#_1	W8	H_DIN#1_5	
H_DIN#_2	U3	H_DIN#2_5	
H_DIN#_3	AB10	H_DIN#3_5	

H_DSTBN#0	K4	H_DSTBN#0_5	
H_DSTBN#1	T7	H_DSTBN#1_5	
H_DSTBN#2	Y5	H_DSTBN#2_5	
H_DSTBN#3	AC4	H_DSTBN#3_5	

H_DSTBP#_0	K3	H_DSTBP#0_5	
H_DSTBP#_1	T6	H_DSTBP#1_5	
H_DSTBP#_2	AA5	H_DSTBP#2_5	
H_DSTBP#_3	AC5	H_DSTBP#3_5	

H_HIT#	D3	H_HIT#_5	
H_HITM#	D4	H_HITM#_5	
H_LOCK#	B3	H_LOCK#_5	

H_REQ#_0	D8	H_REQ#0_5	
H_REQ#_1	G8	H_REQ#1_5	
H_REQ#_2	B8	H_REQ#2_5	
H_REQ#_3	F8	H_REQ#3_5	
H_REQ#_4	A8	H_REQ#4_5	

H_RS#_0	B4	H_RS#0_5	
H_RS#_1	E6	H_RS#1_5	
H_RS#_2	D6	H_RS#2_5	

H_SLP#	E7	H_CPUSLP#_GMCH	
H_TRDY#	F3	H_CPUSLP#_5,15	

H_ADS#	E8	H_ADS#_5	
H_ADSTB#_0	B9	H_ADSTB#0_5	
H_ADSTB#_1	C13	H_ADSTB#1_5	
H_VREF	I13	H_VREF	
H_BNR#	C6	H_BNR#_5	
H_BREQ#0	C7	H_BREQ#0_5	
H_CPURST#	B7	H_CPURST#_5	
H_DESY#	A7	H_DESY#_5	
H_DEFER#	C3	H_DEFER#_5	
H_DPWR#	J9	H_DPWR#_5	
H_DRDY#	H8	H_DRDY#_5	
H_VREF	K13	H_VREF	

H_DIN#_0	J7	H_DIN#0_5	
H_DIN#_1	W8	H_DIN#1_5	
H_DIN#_2	U3	H_DIN#2_5	
H_DIN#_3	AB10	H_DIN#3_5	

H_DSTBN#0	K4	H_DSTBN#0_5	
H_DSTBN#1	T7	H_DSTBN#1_5	
H_DSTBN#2	Y5	H_DSTBN#2_5	
H_DSTBN#3	AC4	H_DSTBN#3_5	

H_DSTBP#_0	K3	H_DSTBP#0_5	
H_DSTBP#_1	T6	H_DSTBP#1_5	
H_DSTBP#_2	AA5	H_DSTBP#2_5	
H_DSTBP#_3	AC5	H_DSTBP#3_5	

H_HIT#	D3	H_HIT#_5	
H_HITM#	D4	H_HITM#_5	
H_LOCK#	B3	H_LOCK#_5	

H_REQ#_0	D8	H_REQ#0_5	
H_REQ#_1	G8	H_REQ#1_5	
H_REQ#_2	B8	H_REQ#2_5	
H_REQ#_3	F8	H_REQ#3_5	
H_REQ#_4	A8	H_REQ#4_5	

H_RS#_0	B4	H_RS#0_5	
H_RS#_1	E6	H_RS#1_5	
H_RS#_2	D6	H_RS#2_5	

H_SLP#	E7	H_CPUSLP#_GMCH	
H_TRDY#	F3	H_CPUSLP#_5,15	

H_ADS#	E8	H_ADS#_5	
H_ADSTB#_0	B9	H_ADSTB#0_5	
H_ADSTB#_1	C13	H_ADSTB#1_5	
H_VREF	I13	H_VREF	
H_BNR#	C6	H_BNR#_5	
H_BREQ#0	C7	H_BREQ#0_5	
H_CPURST#	B7	H_CPURST#_5	
H_DESY#	A7	H_DESY#_5	
H_DEFER#	C3	H_DEFER#_5	
H_DPWR#	J9	H_DPWR#_5	
H_DRDY#	H8	H_DRDY#_5	
H_VREF	K13	H_VREF	

H_DIN#_0	J7	H_DIN#0_5	
H_DIN#_1	W8	H_DIN#1_5	
H_DIN#_2	U3	H_DIN#2_5	
H_DIN#_3	AB10	H_DIN#3_5	

H_DSTBN#0	K4	H_DSTBN#0_5	
H_DSTBN#1	T7	H_DSTBN#1_5	
H_DSTBN#2	Y5	H_DSTBN#2_5	
H_DSTBN#3	AC4	H_DSTBN#3_5	

H_DSTBP#_0	K3	H_DSTBP#0_5	
H_DSTBP#_1	T6	H_DSTBP#1_5	
H_DSTBP#_2	AA5	H_DSTBP#2_5	
H_DSTBP#_3	AC5	H_DSTBP#3_5	

H_HIT#	D3	H_HIT#_5	
H_HITM#	D4	H_HITM#_5	
H_LOCK#	B3	H_LOCK#_5	

H_REQ#_0	D8	H_REQ#0_5	
H_REQ#_1	G8	H_REQ#1_5	
H_REQ#_2	B8	H_REQ#2_5	
H_REQ#_3	F8	H_REQ#3_5	
H_REQ#_4	A8	H_REQ#4_5	

H_RS#_0	B4	H_RS#0_5	
H_RS#_1	E6	H_RS#1_5	
H_RS#_2	D6	H_RS#2_5	

H_SLP#	E7	H_CPUSLP#_GMCH	
H_TRDY#	F3	H_CPUSLP#_5,15	

H_ADS#	E8	H_ADS#_5	
H_ADSTB#_0	B9	H_ADSTB#0_5	
H_ADSTB#_1	C13	H_ADSTB#1_5	
H_VREF	I13	H_VREF	
H_BNR#	C6	H_BNR#_5	
H_BREQ#0	C7	H_BREQ#0_5	
H_CPURST#	B7	H_CPURST#_5	
H_DESY#	A7	H_DESY#_5	
H_DEFER#	C3	H_DEFER#_5	
H_DPWR#	J9	H_DPWR#_5	
H_DRDY#	H8	H_DRDY#_5	
H_VREF	K13	H_VREF	

H_DIN#_0	J7	H_DIN#0_5	
H_DIN#_1	W8	H_DIN#1_5	
H_DIN#_2	U3	H_DIN#2_5	
H_DIN#_3	AB10	H_DIN#3_5	

H_DSTBN#0	K4	H_DSTBN#0_5	
H_DSTBN#1	T7	H_DSTBN#1_5	
H_DSTBN#2	Y5	H_DSTBN#2_5	
H_DSTBN#3	AC4	H_DSTBN#3_5	

H_DSTBP#_0	K3	H_DSTBP#0_5	
H_DSTBP#_1	T6	H_DSTBP#1_5	
H_DSTBP#_2	AA5	H_DSTBP#2_5	
H_DSTBP#_3	AC5	H_DSTBP#3_5	

H_HIT#	D3	H_HIT#_5	
H_HITM#	D4	H_HITM#_5	
H_LOCK#	B3	H_LOCK#_5	

H_REQ#_0	D8	H_REQ#0_5	
H_REQ#_1	G8	H_REQ#1_5	
H_REQ#_2	B8	H_REQ#2_5	
H_REQ#_3	F8	H_REQ#3_5	
H_REQ#_4	A8	H_REQ#4_5	

H_RS#_0	B4	H_RS#0_5	
H_RS#_1	E6	H_RS#1_5	
H_RS#_2	D6	H_RS#2_5	

H_SLP#	E7	H_CPUSLP#_GMCH	
H_TRDY#	F3	H_CPUSLP#_5,15	

H_ADS#	E8	H_ADS#_5	
H_ADSTB#_0	B9	H_ADSTB#0_5	
H_ADSTB#_1	C13	H_ADSTB#1_5	
H_VREF	I13	H_VREF	
H_BNR#	C6	H_BNR#_5	
H_BREQ#0	C7	H_BREQ#0_5	
H_CPURST#	B7	H_CPURST#_5	
H_DESY#	A7	H_DESY#_5	
H_DEFER#	C3	H_DEFER#_5	
H_DPWR#	J9	H_DPWR#_5	
H_DRDY#	H8	H_DRDY#_5	
H_VREF	K13	H_VREF	

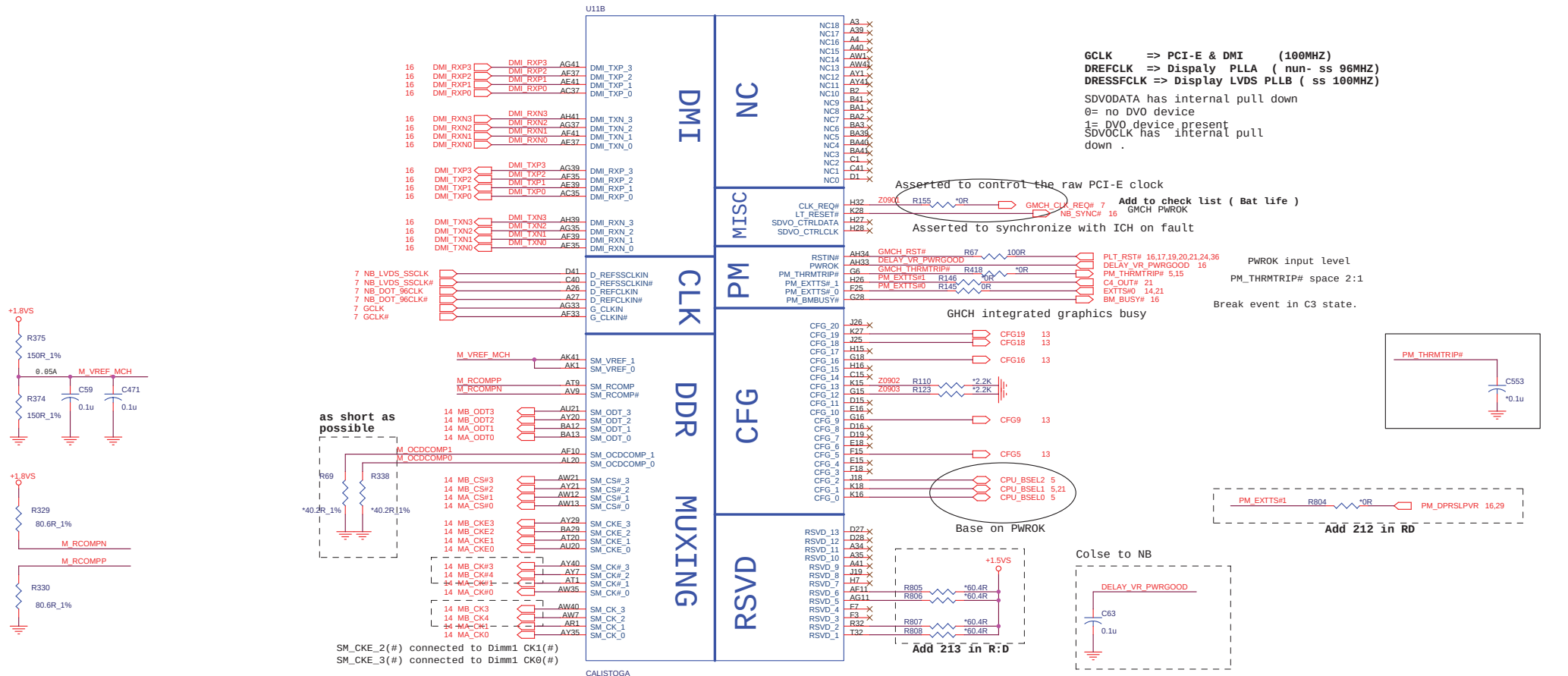
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H_DIN#_1	W8	H_DIN#1_5	
H_DIN#_2	U3	H_DIN#2_5	
H_DIN#_3	AB10	H_DIN#3_5	

H_DSTBN#0	K4	H_DSTBN#0_5	
H_DSTBN#1	T7	H_DSTBN#1_5	
H_DSTBN#2	Y5	H_DSTBN#2_5	
H_DSTBN#3	AC4	H_DSTBN#3_5	

H_DSTBP#_0	K3	H_DSTBP#0_5	
H_DSTBP#_1	T6	H_DSTBP#1_5	
H_DSTBP#_2	AA5	H_DSTBP#2_5	
H_DSTBP#_3	AC5	H_DSTBP#3_5	

H_HIT#	D3	H_HIT#_5	
H_HITM#	D4	H_HITM#_5	
H_LOCK#	B3	H_LOCK#_5	

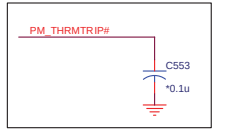
H_REQ#_0	D8	H_REQ#0_5	
H_REQ#_1	G8	H_REQ#1_5	
H_REQ#_2	B8	H_REQ#2_5	
H_REQ#_3	F8	H_REQ#3_5	
H_REQ#_4</			



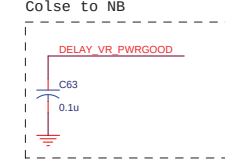
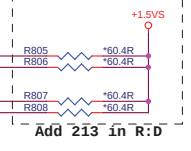
GCLK => PCI-E & DMI (100MHZ)
 DREFCLK => Display PLLA (nun- ss 96MHZ)
 DRESSFCLK => Display LVDS PLLB (ss 100MHZ)
 SDVODATA has internal pull down
 0= no DVO device
 1= DVO device present
 SDVOCLOCK has internal pull down .

Asserted to control the raw PCI-E clock
 Add to check list (Bat life)
 Asserted to synchronize with ICH on fault

PWROK input level
 PM_THRMTRIP# space 2:1
 Break event in C3 state.



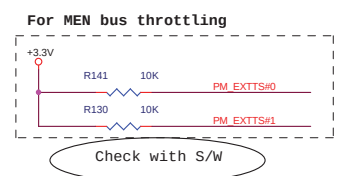
PM_EXTTS#1 R804 *0R PM_DPRSPLVR 16.29
 Add 212 in RD



Only Base on Discreted VGA

VCCA_DPLLA , VCCA_DPLL B => NC
 DREF_CLKP / DREF_SSCLKP = GND
 DREF_CLKN / DREF_SSCLKN = GND

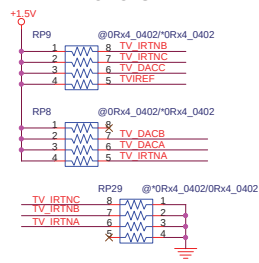
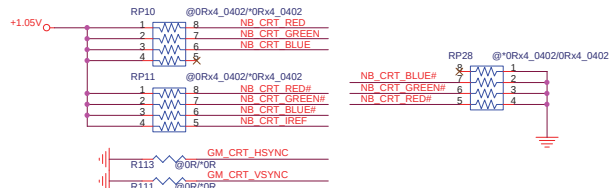
VCCA_DPLLA , VCCA_DPLL B =>1.5V
 DREF_CLKP / DREF_SSCLKP = 1.5V
 DREF_CLKN / DREF_SSCLKN = GND



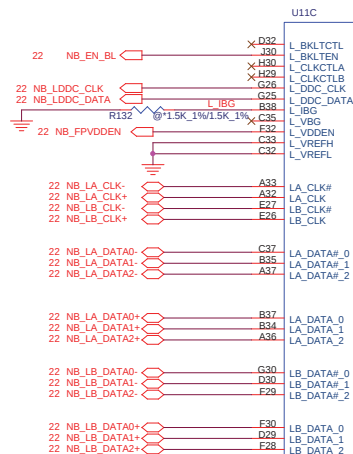
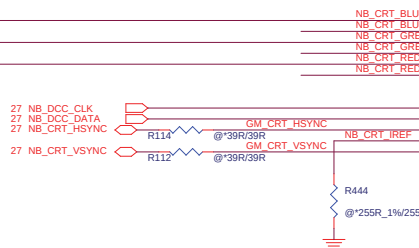
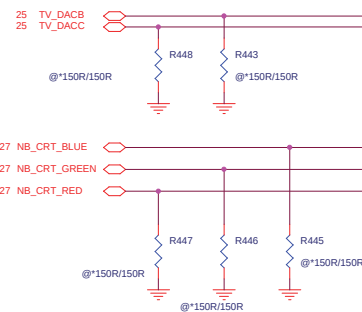
CFG0	CFG1	CFG2	Host Clock frequency
1	0	0	133
1	1	0	166

CFG7 (IPU) => 1= Mobility CPU
 0 = Reverse

Name of Part NB(2)_DMI/VGA/MICS
 Project S501A Main Board Rev D
 Date: Monday, July 10, 2006 Sheet 9 / 49
 3255 UNIWILL COMPUTER CORP.



CRT FUNC.
DISable.
ALL DAC
PORT

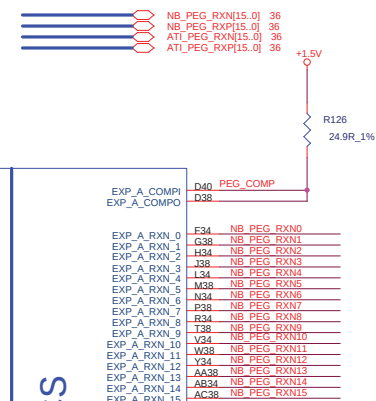


LVDS

TV

VGA

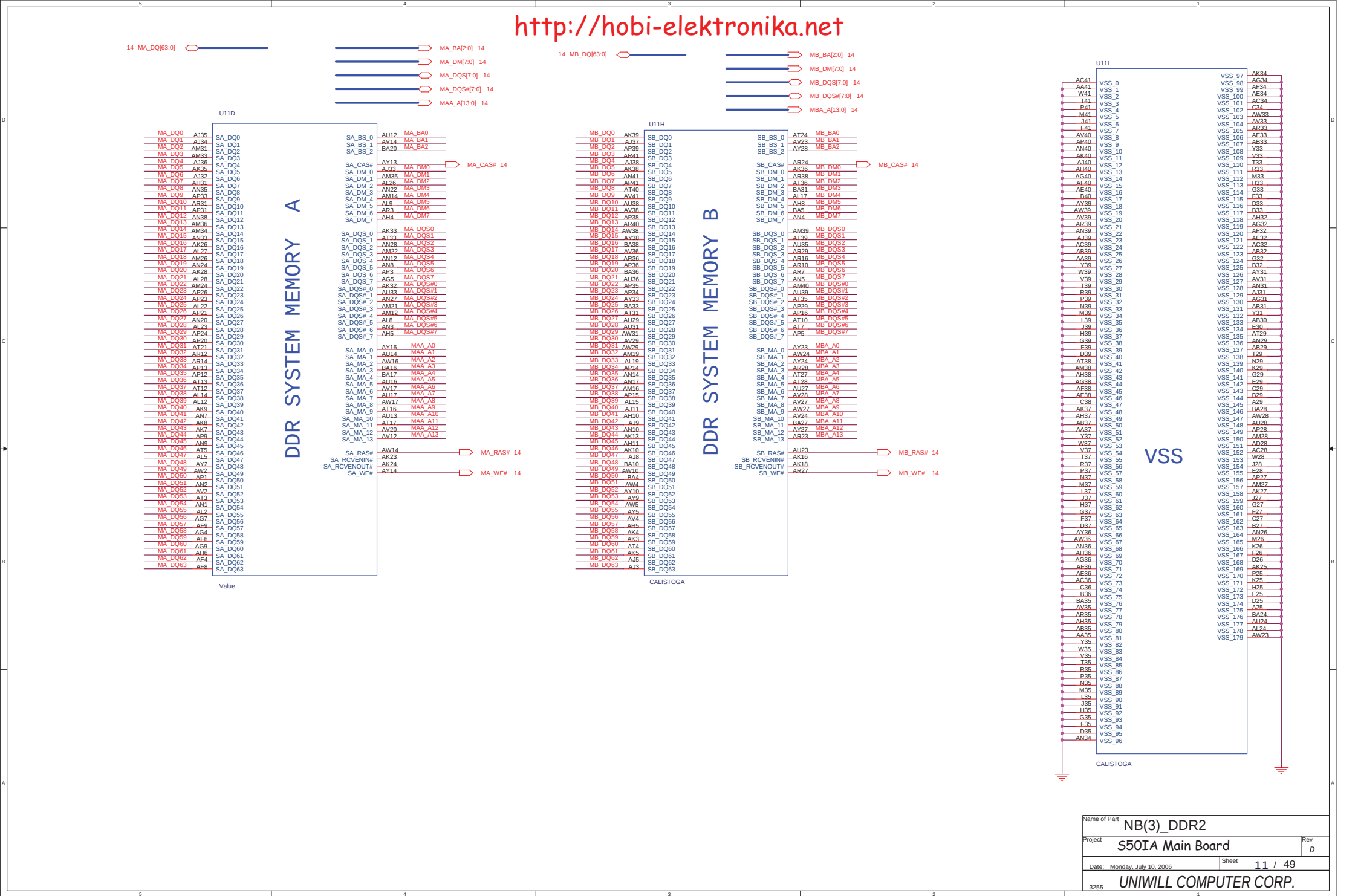
CALISTOGA

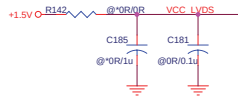
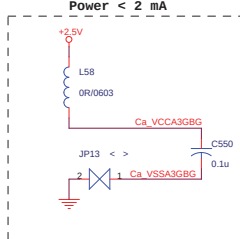


EXP_A_RXP_0	D34	NB	PEG RXP0		
EXP_A_RXP_1	F34	NB	PEG RXP1		
EXP_A_RXP_2	G34	NB	PEG RXP2		
EXP_A_RXP_3	H34	NB	PEG RXP3		
EXP_A_RXP_4	J34	NB	PEG RXP4		
EXP_A_RXP_5	L38	NB	PEG RXP5		
EXP_A_RXP_6	M34	NB	PEG RXP6		
EXP_A_RXP_7	N38	NB	PEG RXP7		
EXP_A_RXP_8	P34	NB	PEG RXP8		
EXP_A_RXP_9	R34	NB	PEG RXP9		
EXP_A_RXP_10	T34	NB	PEG RXP10		
EXP_A_RXP_11	V38	NB	PEG RXP11		
EXP_A_RXP_12	W34	NB	PEG RXP12		
EXP_A_RXP_13	Y38	NB	PEG RXP13		
EXP_A_RXP_14	AA34	NB	PEG RXP14		
EXP_A_RXP_15	AB38	NB	PEG RXP15		
EXP_A_TXN_0	F36	NB	PEG TXN0 C157	2	0.0
EXP_A_TXN_1	G40	NB	PEG TXN1 C165	1	0.0
EXP_A_TXN_2	H36	NB	PEG TXN2 C138	1	0.0
EXP_A_TXN_3	J40	NB	PEG TXN3 C547	2	0.0
EXP_A_TXN_4	L36	NB	PEG TXN4 C123	2	0.0
EXP_A_TXN_5	M36	NB	PEG TXN5 C542	1	0.0
EXP_A_TXN_6	N40	NB	PEG TXN6 C111	2	0.0
EXP_A_TXN_7	P40	NB	PEG TXN7 C540	2	0.0
EXP_A_TXN_8	R36	NB	PEG TXN8 C96	2	0.0
EXP_A_TXN_9	T40	NB	PEG TXN9 C330	2	0.0
EXP_A_TXN_10	W40	NB	PEG TXN10 C93	2	0.0
EXP_A_TXN_11	V36	NB	PEG TXN11 C524	1	0.0
EXP_A_TXN_12	Y36	NB	PEG TXN12 C84	2	0.0
EXP_A_TXN_13	AA40	NB	PEG TXN13 C514	2	0.0
EXP_A_TXN_14	AB36	NB	PEG TXN14 C73	2	0.0
EXP_A_TXN_15	AC40	NB	PEG TXN15 C503	2	0.0
				ATI	PEG RXN0
				ATI	PEG RXN1
				ATI	PEG RXN2
				ATI	PEG RXN3
				ATI	PEG RXN4
				ATI	PEG RXN5
				ATI	PEG RXN6
				ATI	PEG RXN7
				ATI	PEG RXN8
				ATI	PEG RXN9
				ATI	PEG RXN10
				ATI	PEG RXN11
				ATI	PEG RXN12
				ATI	PEG RXN13
				ATI	PEG RXN14
				ATI	PEG RXN15

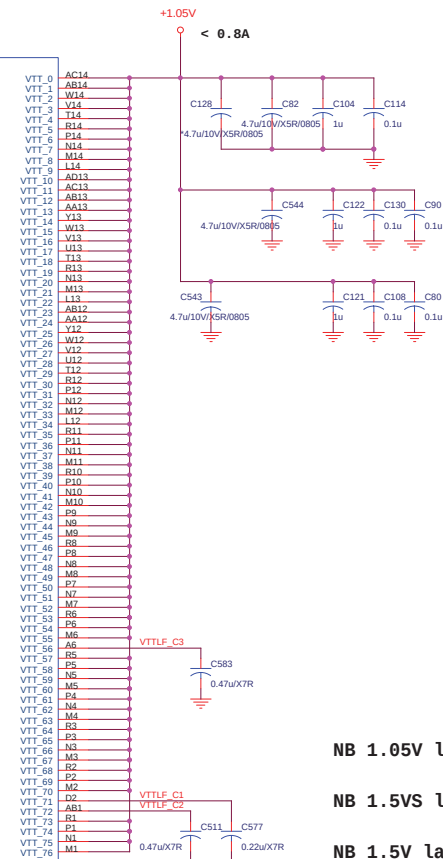
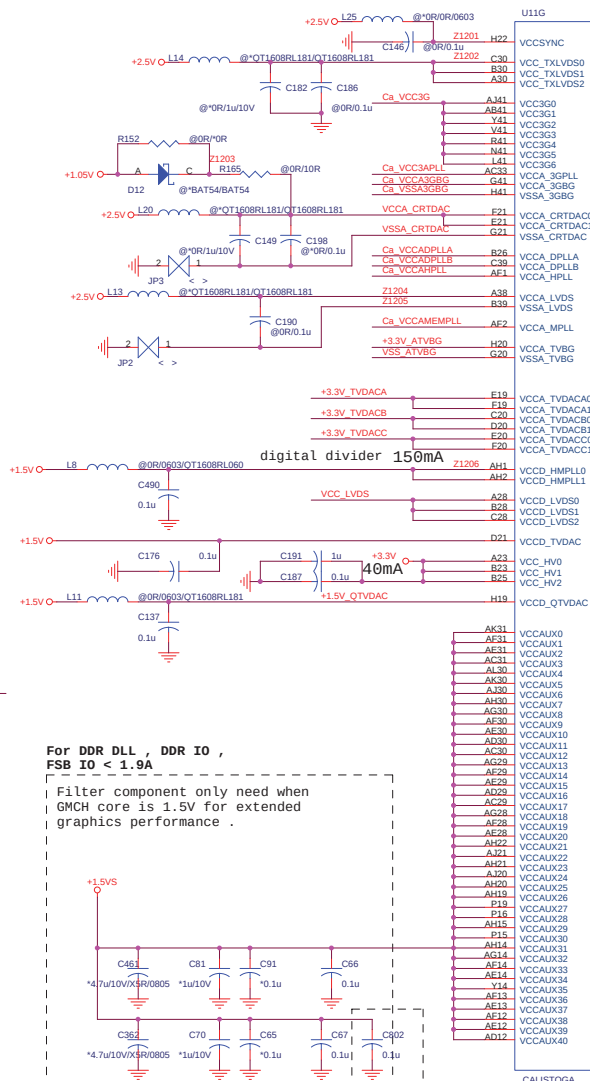
EXP_A_TXP_0	D40	NB	PEG_TXP0	C550	2	0.1u	ATI_PEG_RXP0
EXP_A_TXP_1	F40	NB	PEG_TXP1	C1581	1	2.0u	ATI_PEG_RXP1
EXP_A_TXP_2	G36	NB	PEG_TXP2	C135	2	0.1u	ATI_PEG_RXP2
EXP_A_TXP_3	H40	NB	PEG_TXP3	C549	2	0.1u	ATI_PEG_RXP3
EXP_A_TXP_4	I36	NB	PEG_TXP4	C141	2	0.1u	ATI_PEG_RXP4
EXP_A_TXP_5	L40	NB	PEG_TXP5	C545	2	0.1u	ATI_PEG_RXP5
EXP_A_TXP_6	M36	NB	PEG_TXP6	C511	2	0.1u	ATI_PEG_RXP6
EXP_A_TXP_7	N40	NB	PEG_TXP7	C541	2	0.1u	ATI_PEG_RXP7
EXP_A_TXP_8	P36	NB	PEG_TXP8	C107	2	0.1u	ATI_PEG_RXP8
EXP_A_TXP_9	R40	NB	PEG_TXP9	C539	2	0.1u	ATI_PEG_RXP9
EXP_A_TXP_10	S40	NB	PEG_TXP10	C36	2	0.1u	ATI_PEG_RXP10
EXP_A_TXP_11	V40	NB	PEG_TXP11	C529	2	0.1u	ATI_PEG_RXP11
EXP_A_TXP_12	W36	NB	PEG_TXP12	C88	2	0.1u	ATI_PEG_RXP12
EXP_A_TXP_13	X40	NB	PEG_TXP13	C517	2	0.1u	ATI_PEG_RXP13
EXP_A_TXP_14	Y40	NB	PEG_TXP14	C570	2	0.1u	ATI_PEG_RXP14
EXP_A_TXP_15	A436	NB	PEG_TXP15	C619	2	0.1u	ATI_PEG_RXP15
EXP_A_TXP_16	AB40	NB	PEG_TXP16	C511	2	0.1u	ATI_PEG_RXP16

Name of Part		NB(3)_VGA_TV_LVDS	
Project		S50IA Main Board	Rev D
Date: Monday, July 10, 2006		Sheet	10 / 49
3255 UNIWILL COMPUTER CORP.			

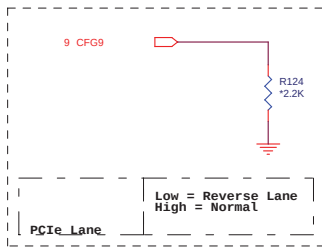
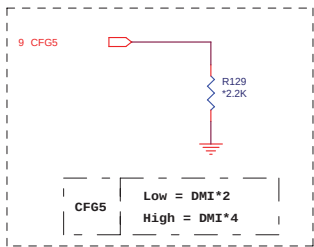
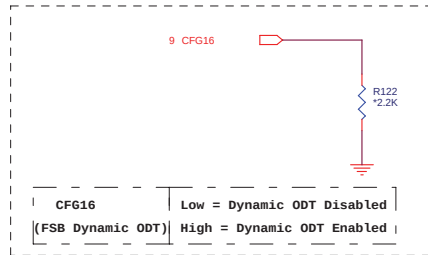




Filter component only need when
GMCH core is 1.5V for extended
graphics performance .

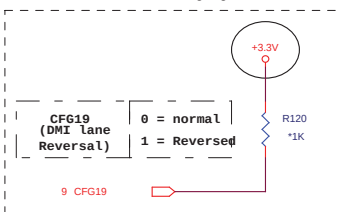
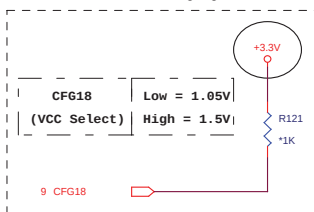


ND 110VS layout 4 01.2A

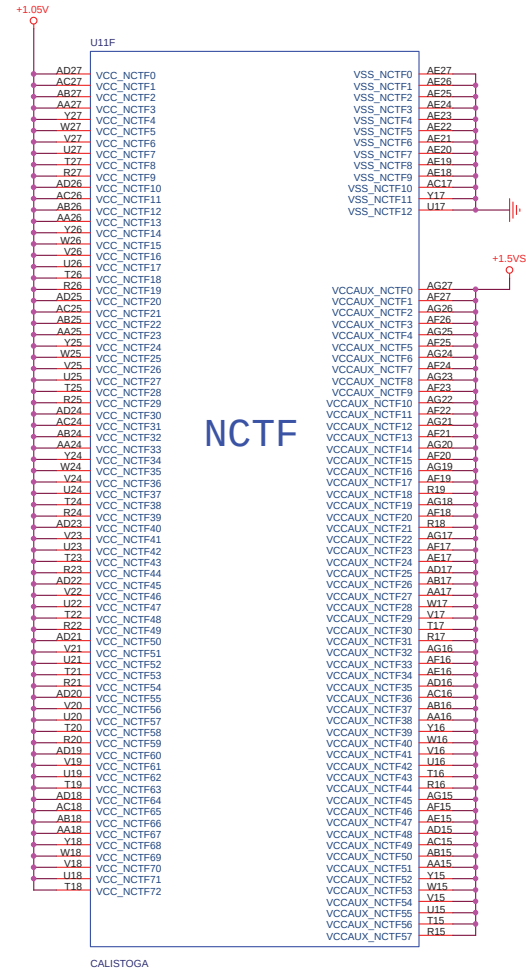
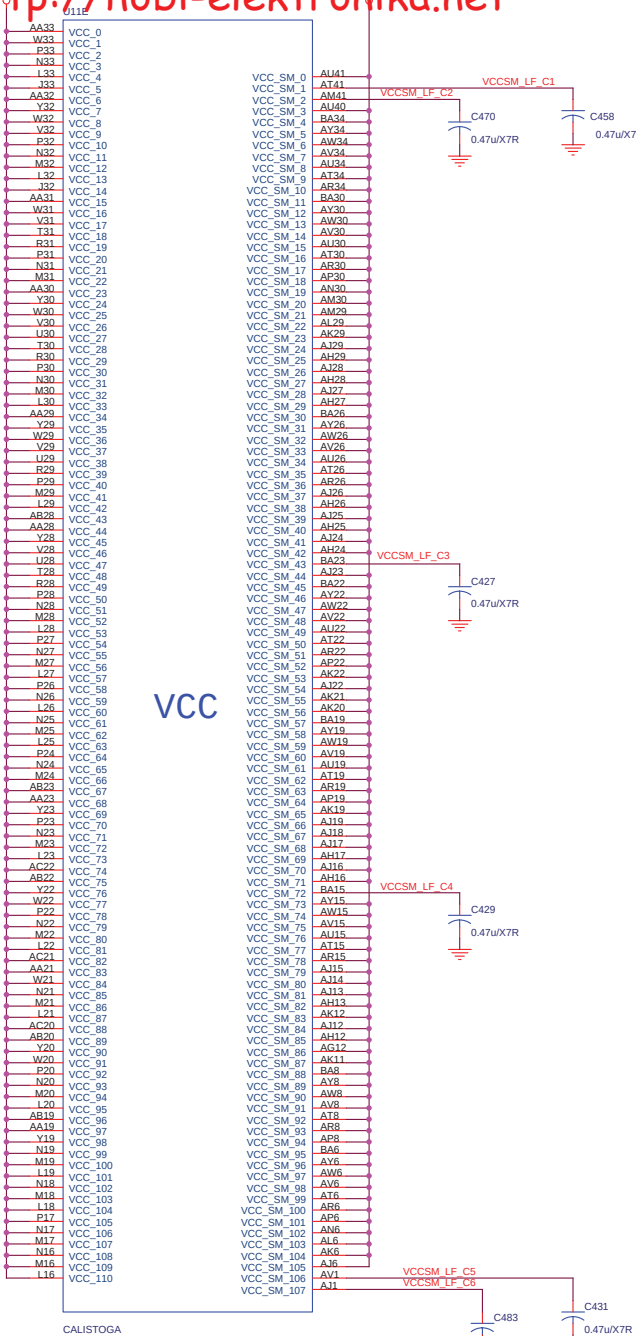
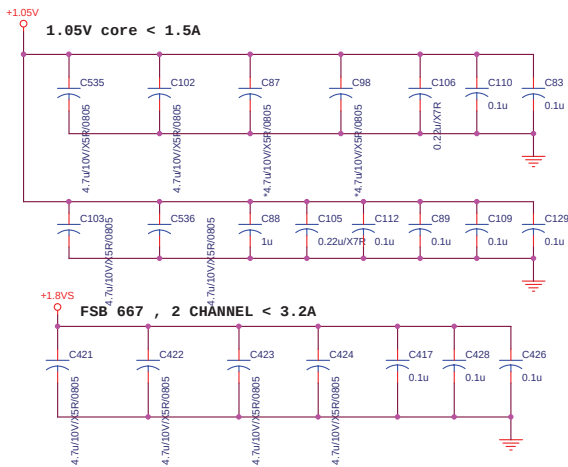


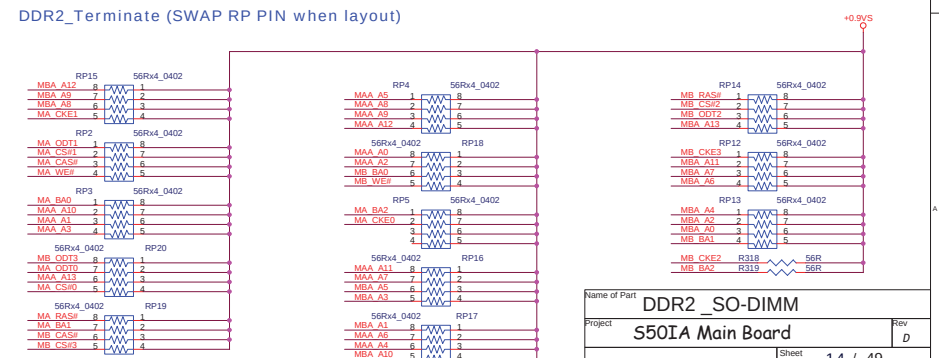
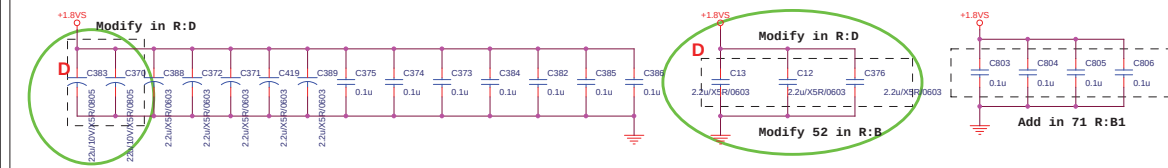
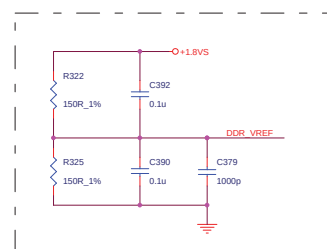
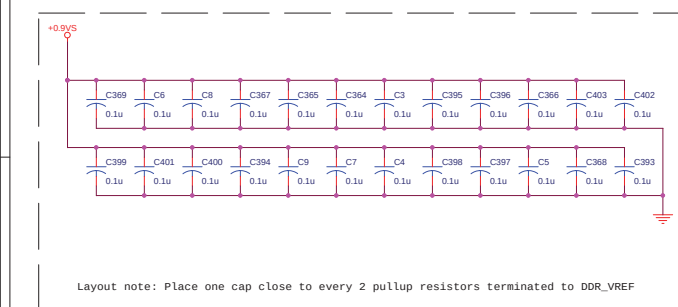
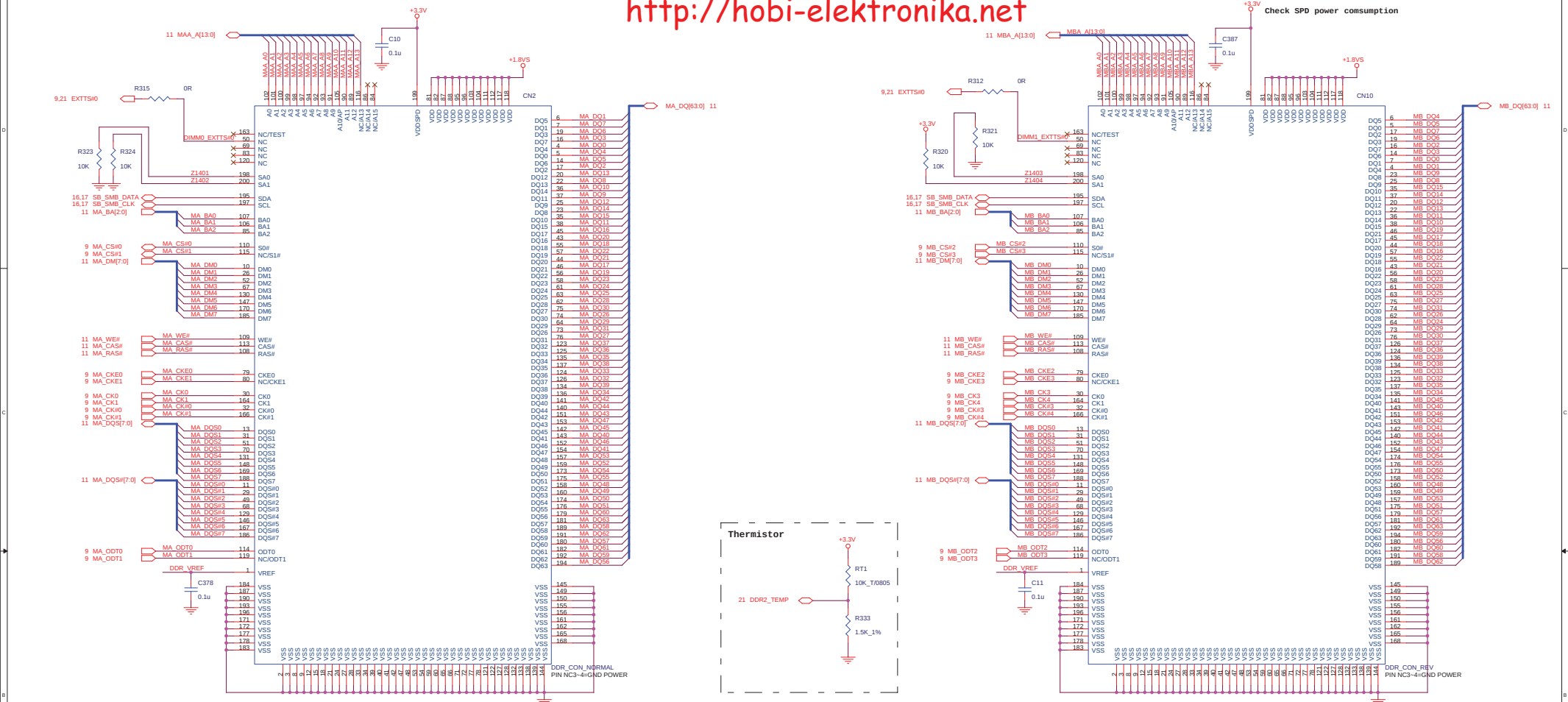
Design guide use 2.5V

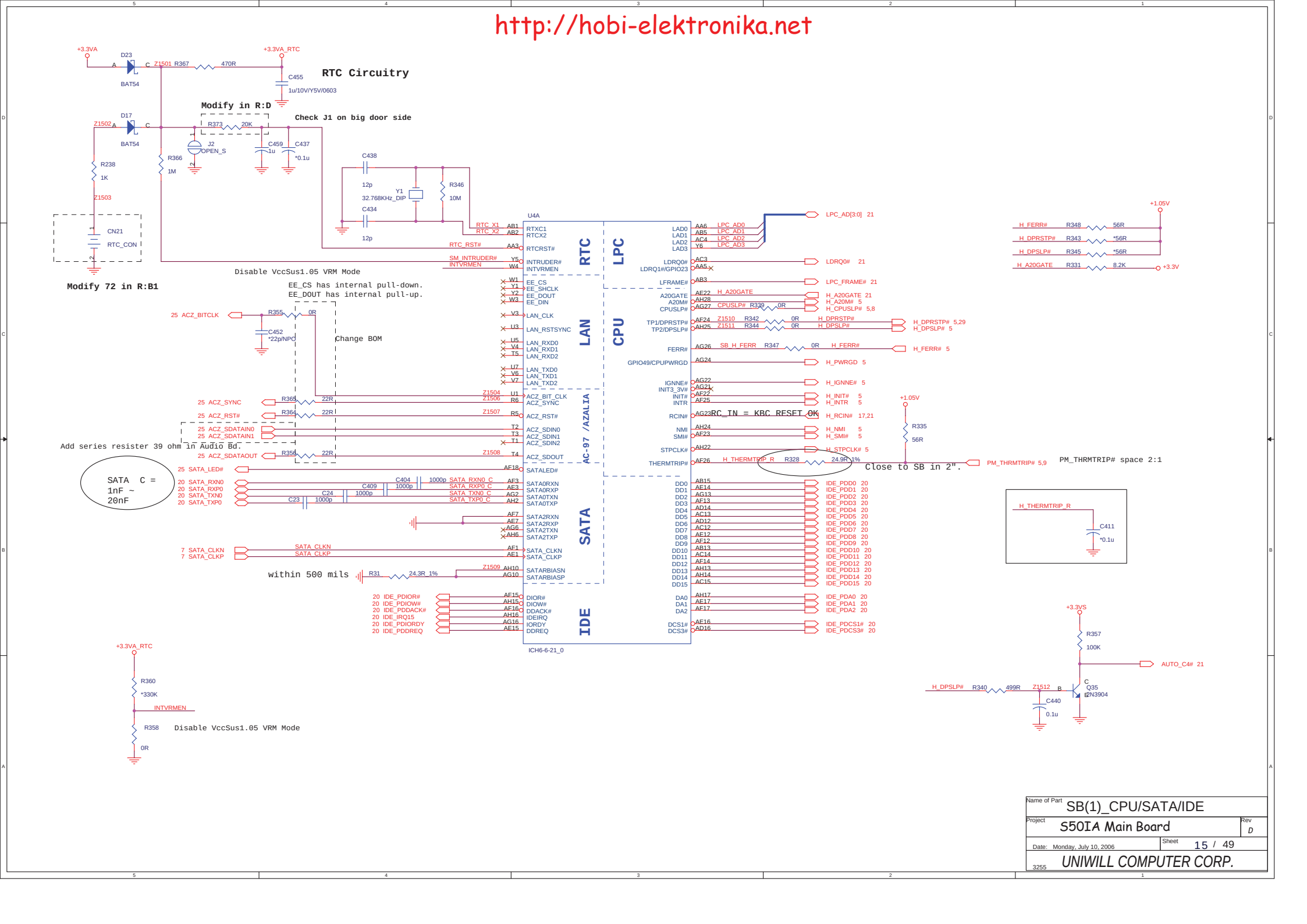
CFG[17:3] have internal pullup resistors.

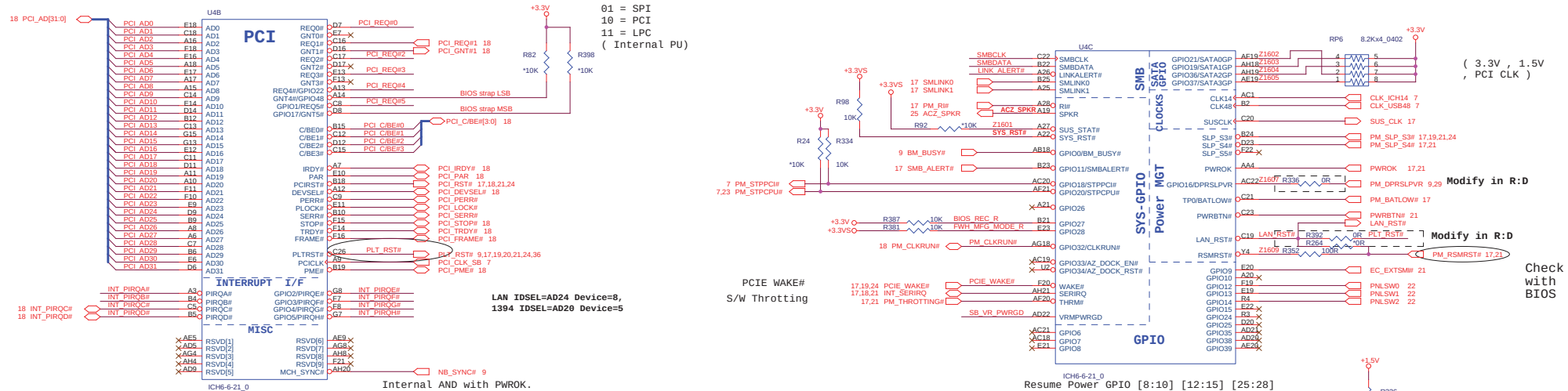


CFG[20:18] have internal pulldown resistors.

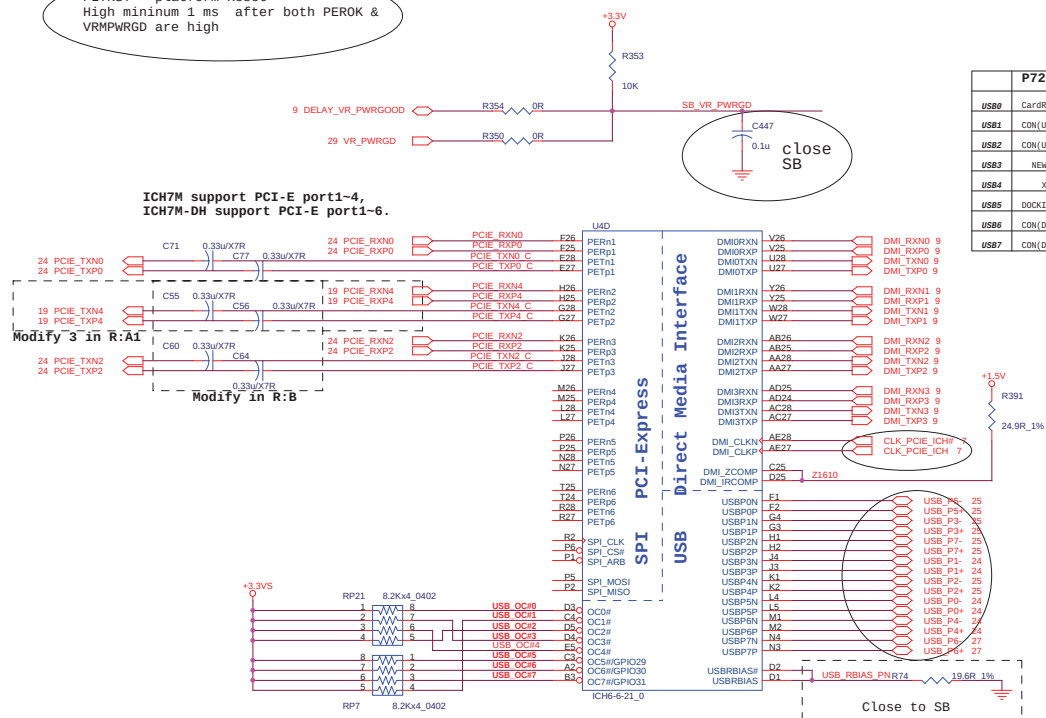




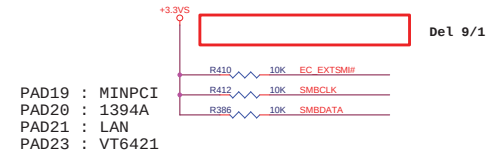
[illegible]



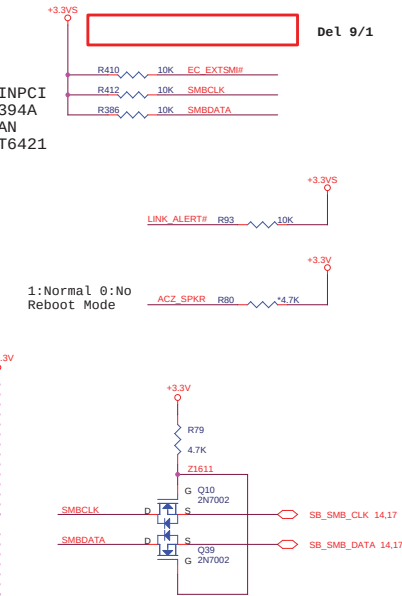
PLTRST = platform Reset
High minimum 1 ms after
VRMPWRGD are high



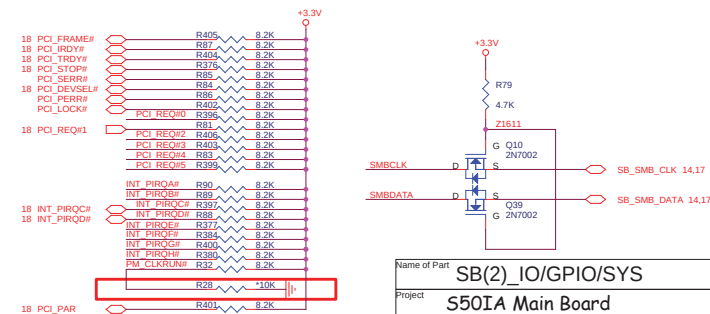
	P72	S50
USB0	CardReader	USB (M/B)
USB1	CON(USB BD)	USB (Audio)
USB2	CON(USB BD)	USB (HDC)
USB3	NEW CARD	NEW CARD
USB4	X	USB (Audio)
USB5	DOCKING	3G Module
USB6	CON(DC BD)	Bluetooth
USB7	CON(DC BD)	PR88

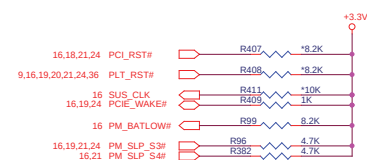
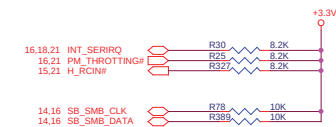
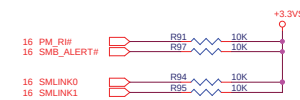


```
PAD19 : MINPCI
PAD20 : 1394A
PAD21 : LAN
PAD23 : VT6421
```

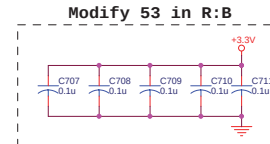


```
1:Normal 0:No
Reboot Mode
```



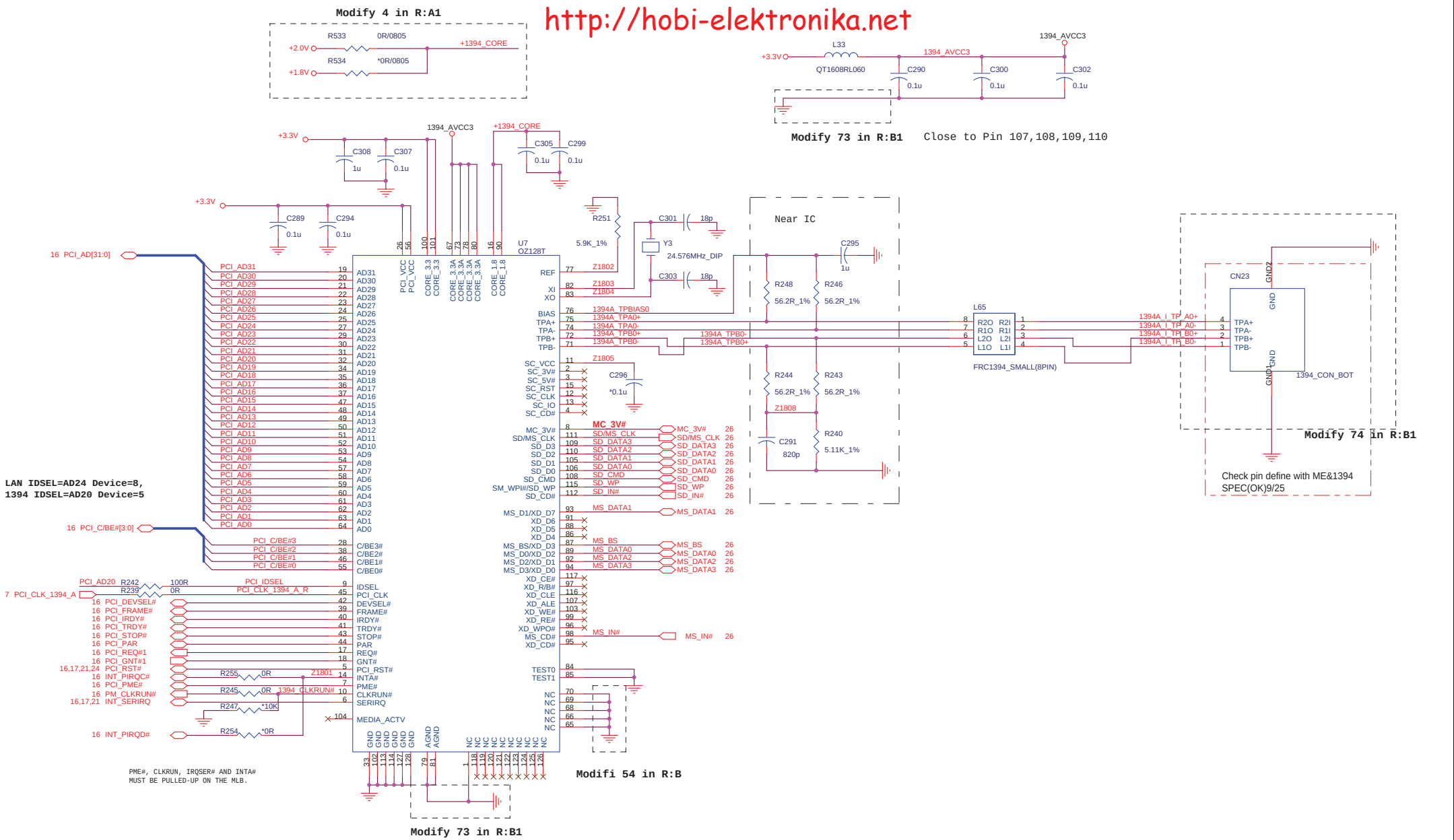


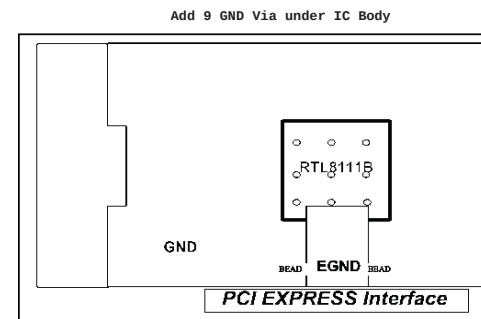
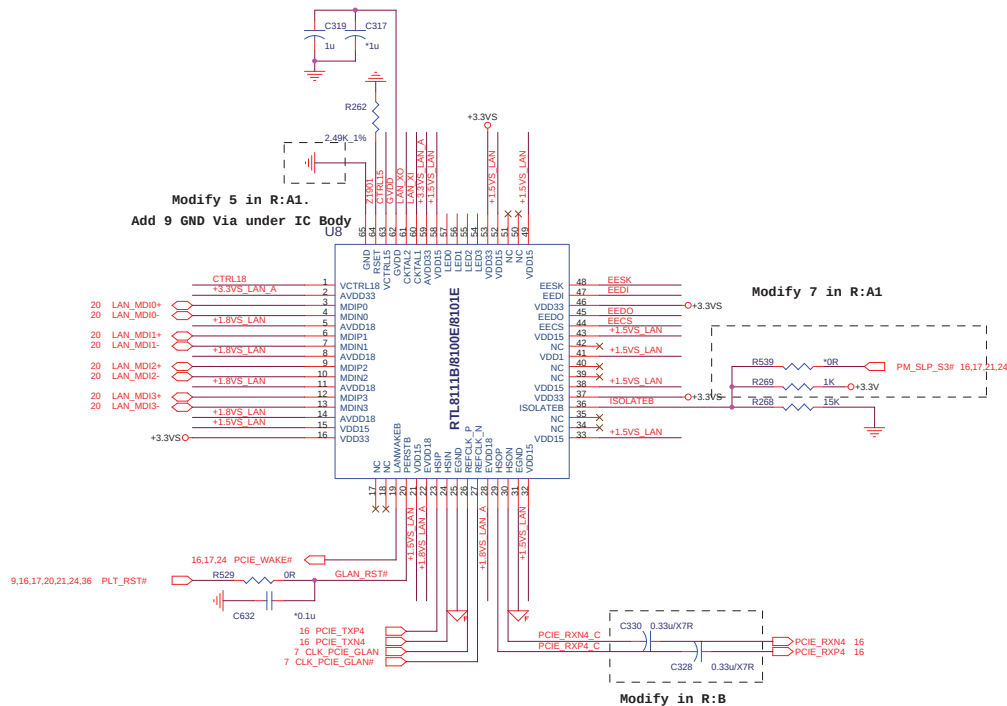
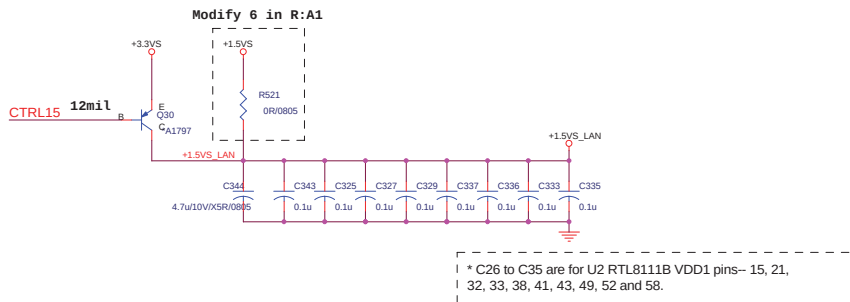
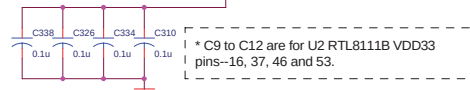
Could be generated
internal by strap
for LAN logic



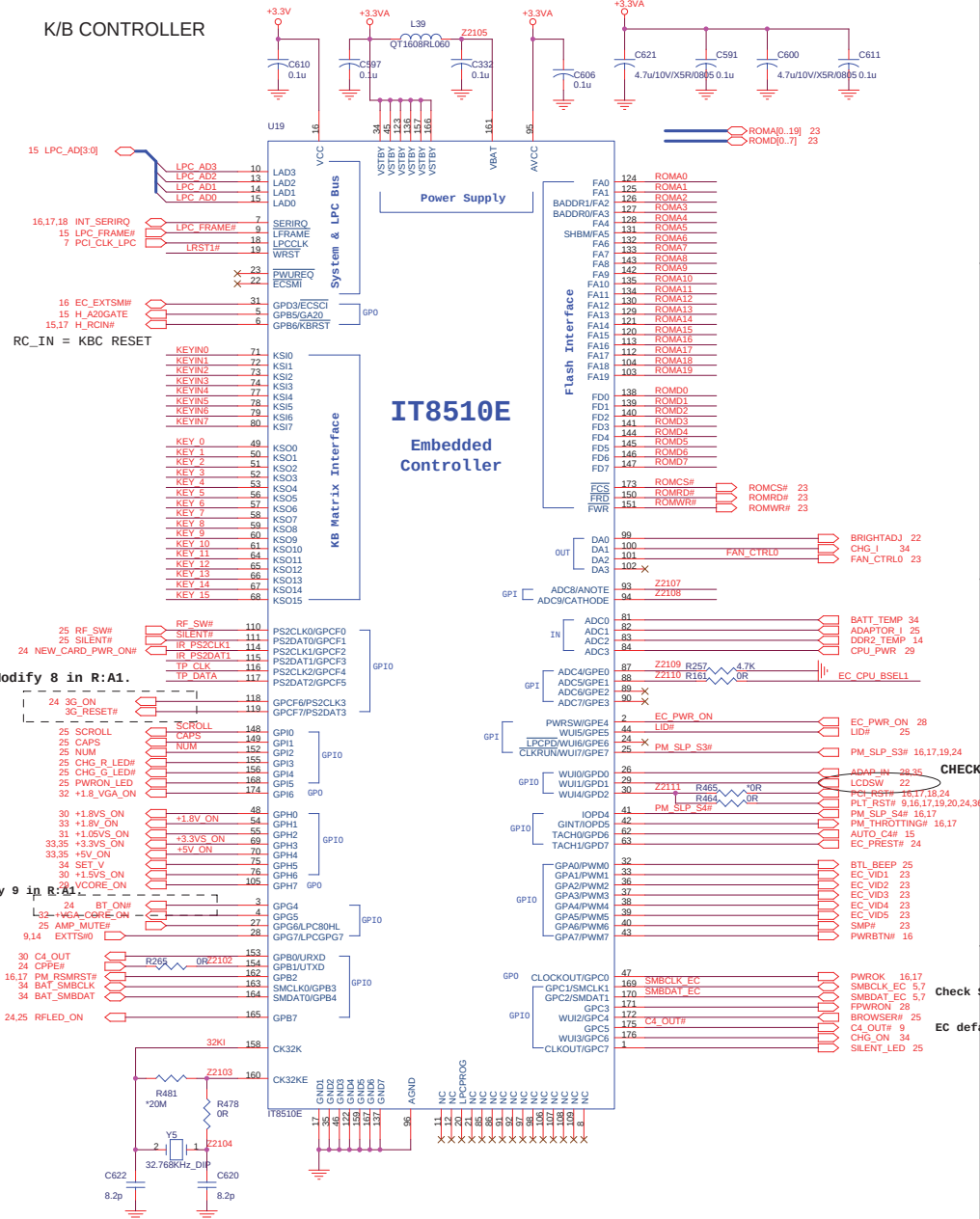
Add C700~C711 for S/B bypass C



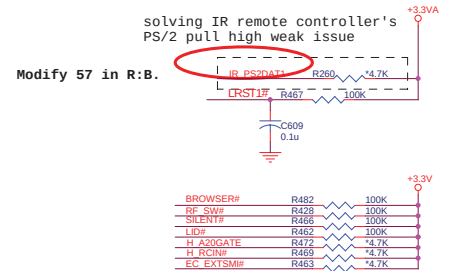
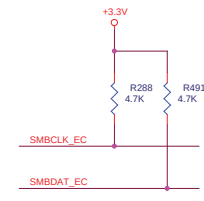




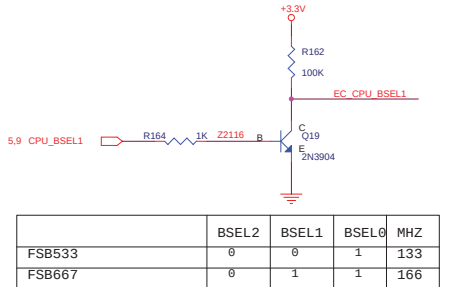
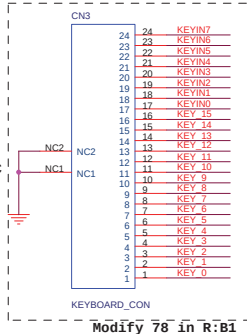
K/B CONTROLLER



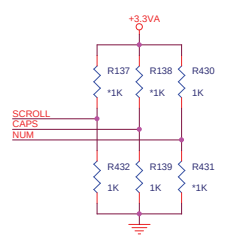
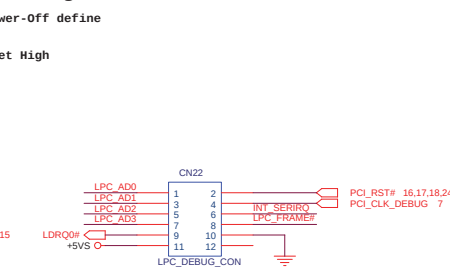
EC SMBUS



Keyboard CONN



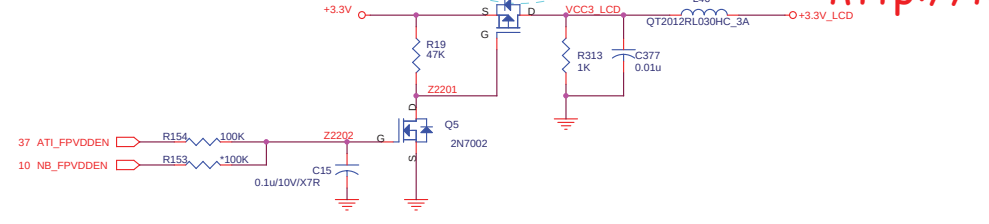
LPC Debug CONN



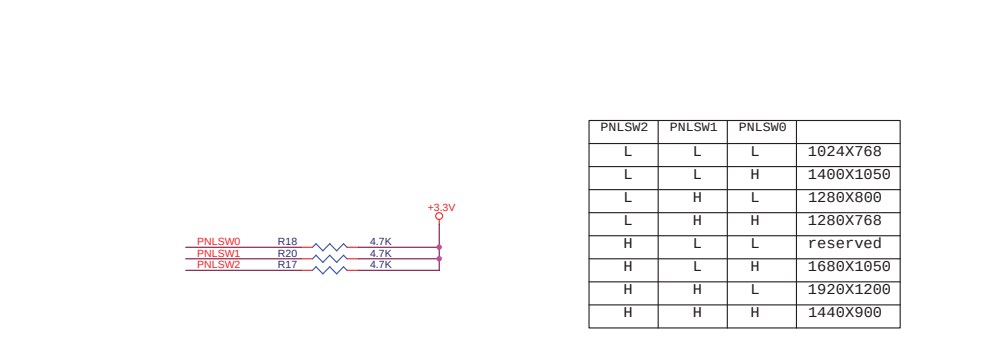
(ID2) NUMLED#	(ID1) CAPLED#	(ID0) SCROLED#	ID MODEL
0	0	0	223
0	0	1	245
0	1	0	255
0	1	1	259
1	0	0	P71EN0
1	0	1	P50EN0
1	1	0	XXX
1	1	1	XXX

Name of Part	EC IT8510E / BIOS / TP CONN	
Project	S50IA Main Board	Rev D
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3255 UNIWILL COMPUTER CORP.		

LCD POWER SW



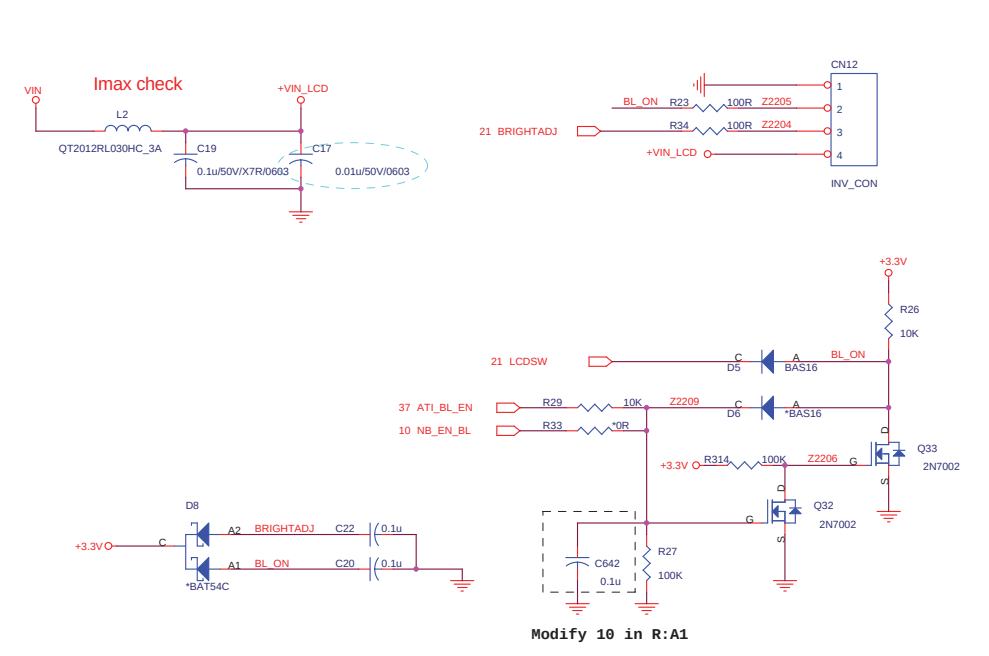
LCD CONN



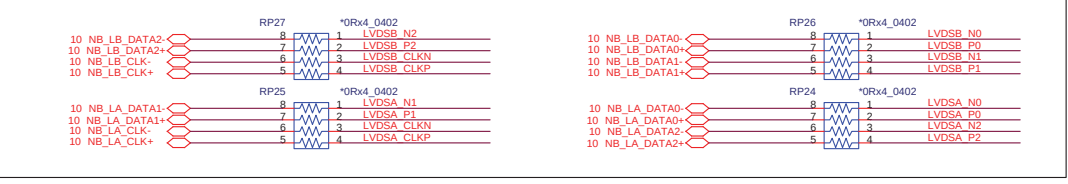
PANNEL ID SELECT

PNLSW2	PNLSW1	PNLSW0	
L	L	L	1024X768
L	L	H	1400X1050
L	H	L	1280X800
L	H	H	1280X768
H	L	L	reserved
H	L	H	1680X1050
H	H	L	1920X1200
H	H	H	1440X900

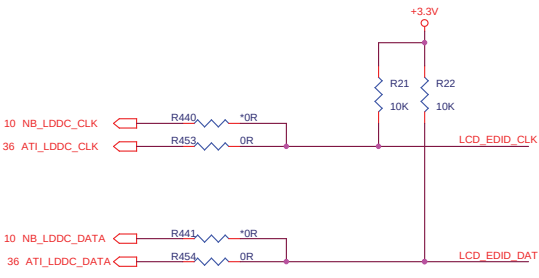
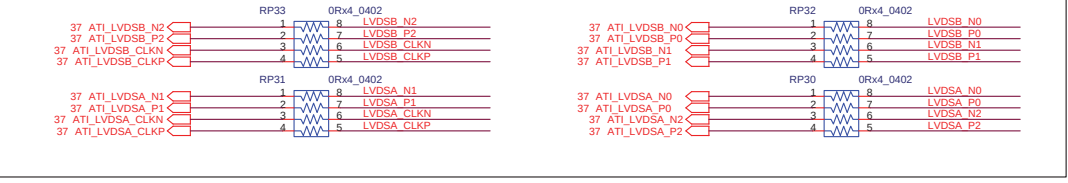
INVERTER CONN



For 945GM

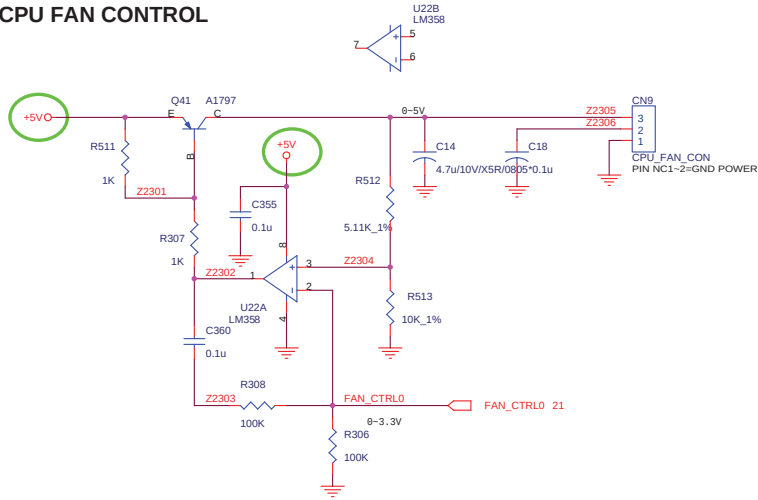


For ATI



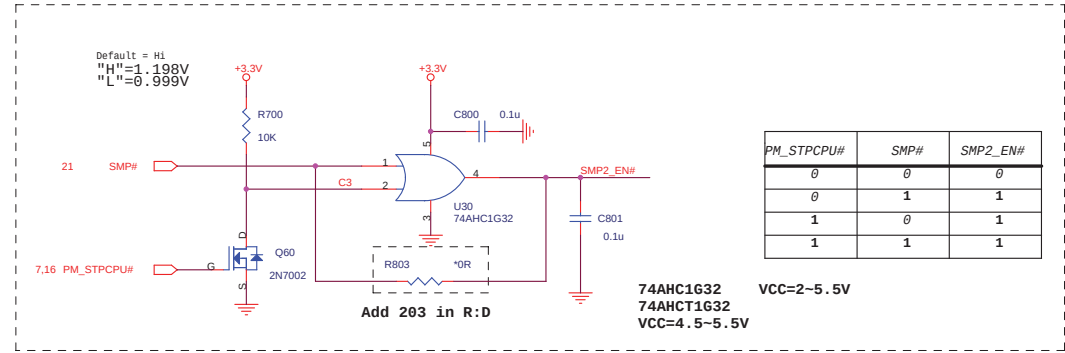
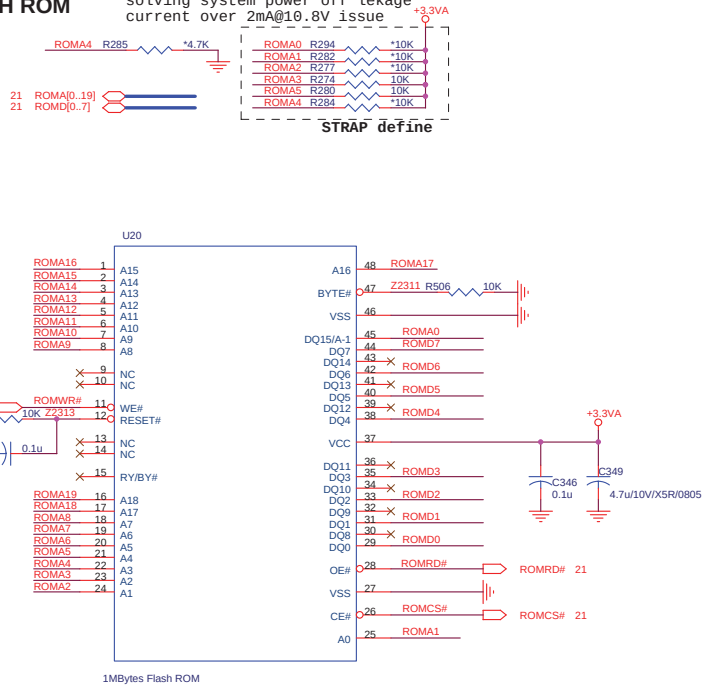
945PM/GM Co-Layout

CPU FAN CONTROL

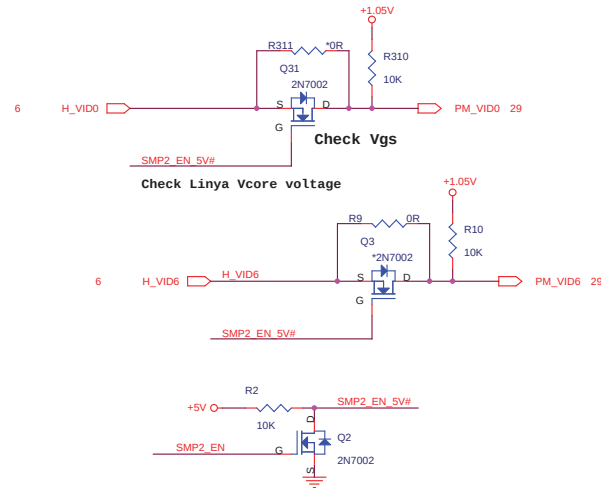


FLASH ROM

solving system power off leakage current over 2mA@10.8V issue

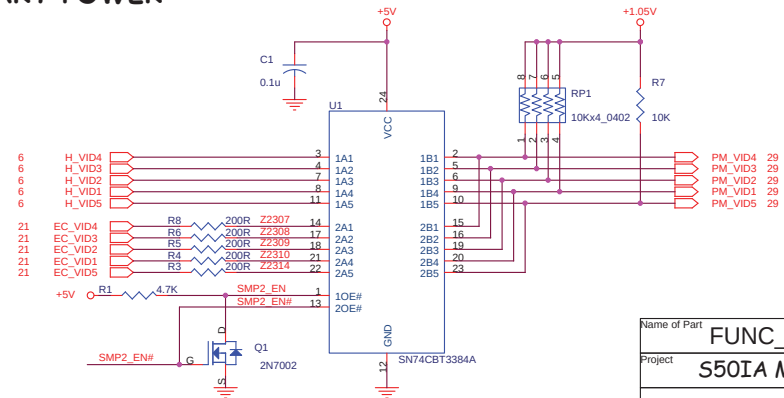


PM_STPCPU#	SMP#	SMP2_EN#
0	0	0
0	1	1
1	0	1
1	1	1



VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE	+_mV
0	0	0	0	0	0	0	1.5000	-0mV
0	0	0	0	0	0	1	1.4875	-2.5mV
0	0	0	0	0	1	0	1.4750	-5mV
0	0	0	0	1	0	0	1.4500	-50mV
0	0	0	1	0	0	0	1.4000	-100mV
0	0	1	0	0	0	0	1.3000	-200mV
0	1	0	0	0	0	0	1.1000	-400mV
1	0	0	0	0	0	0	0.7000	-800mV
0	0	1	1	0	1	1	1.1625	
0	0	1	0	0	0	1		
0	0	1	0	0	1	0		
0	0	1	0	1	0	0		
0	0	1	0	1	1	0		
0	0	1	1	0	0	1		
0	0	1	1	0	1	0		

SMART POWER

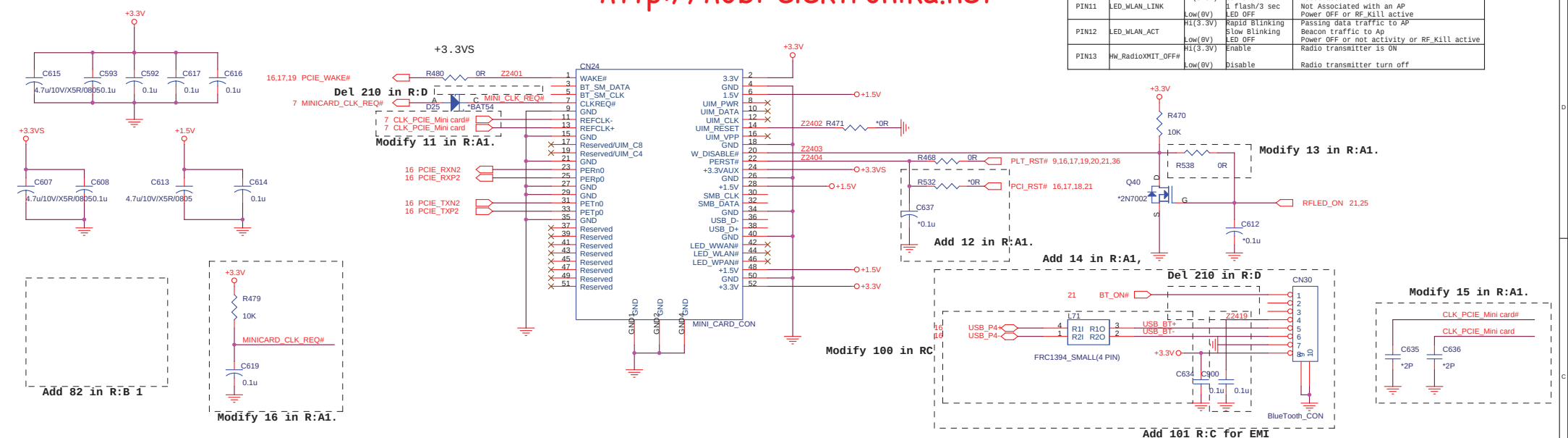


Name of Part	FUNC_CTRL
Project	S50IA Main Board
Date: Monday, July 10, 2006	Sheet 23 / 49
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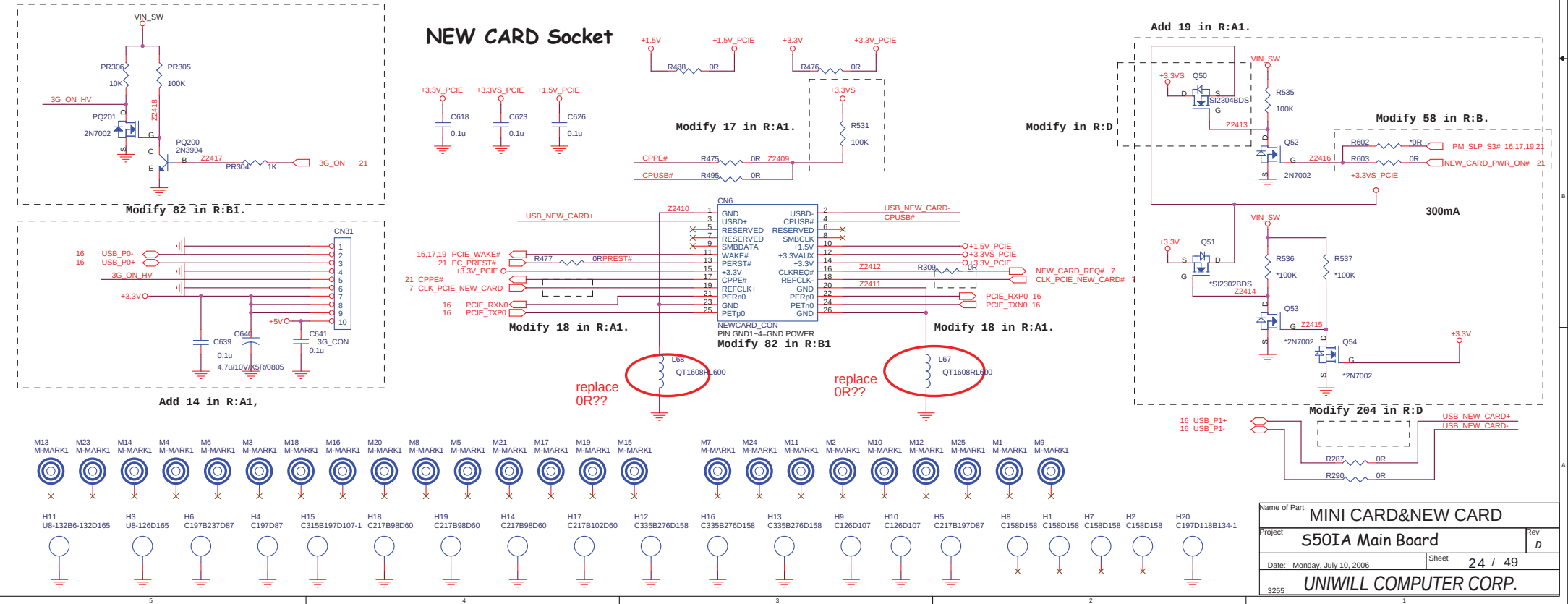
MINI CARD Socket

<http://hobi-elektronika.net>

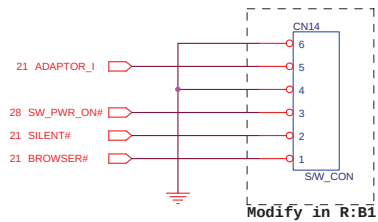
Intel PRO/Wireless 2100 LAN			
PN1N1	LED_WLAN_LINK	Hi(3.3V) Low(0V)	SOLID ON 5 Flash/3 sec LED OFF
PN1N2	LED_WLAN_ACT	Hi(3.3V) Low(0V)	Associated AP Not Associated with an AP Power OFF or RF Kill active
PN1N3	HW_RADIOMITT_OFF#	Hi(3.3V) Low(0V)	Passing data traffic to AP Beacon traffic to AP Power OFF or not activity or RF Kill active
PN1N4	HW_RADIOMITT_ON#	Hi(3.3V) Low(0V)	Radio transmitter is ON
PN1N5	HW_RADIOMITT_DISABLE#	Hi(3.3V) Low(0V)	Radio transmitter turn off



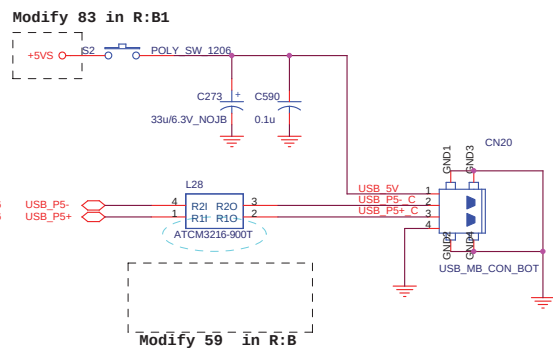
NEW CARD Socket



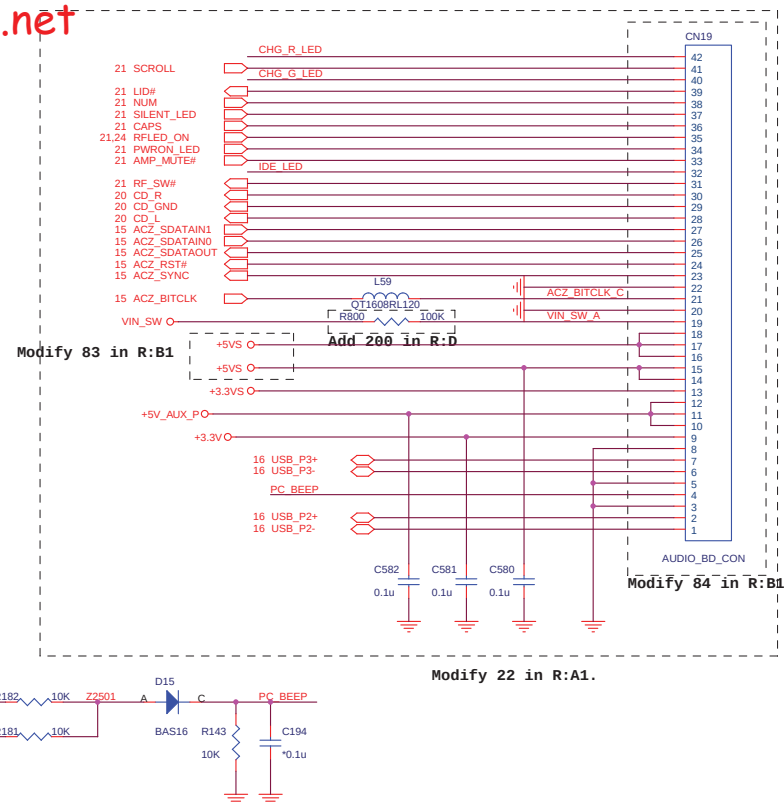
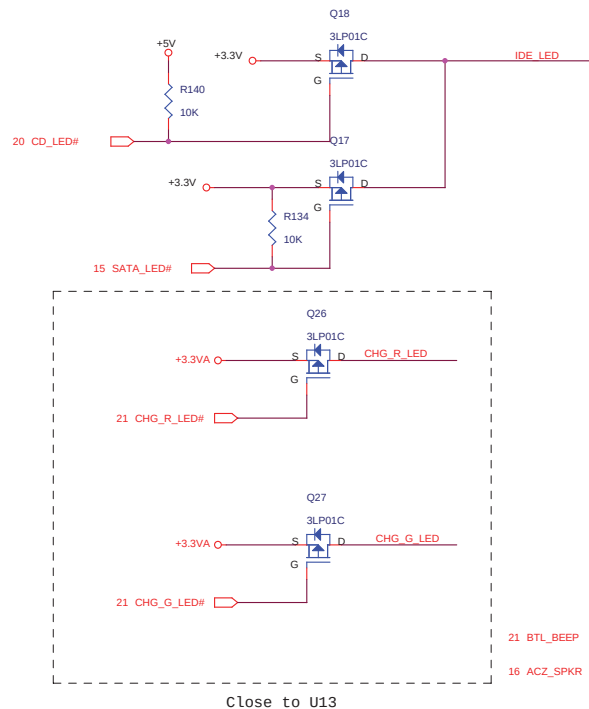
SWITCH BD CONN



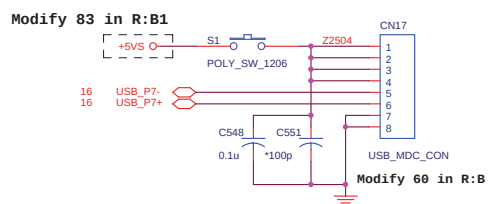
ON BOARD USB



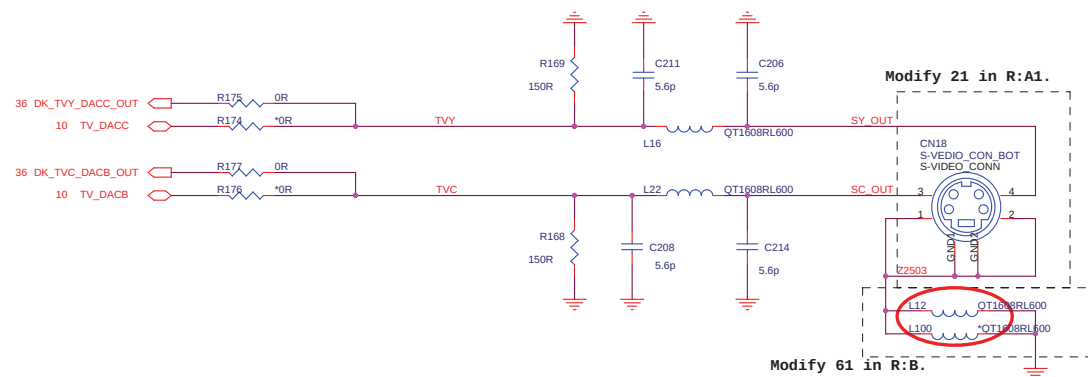
AUDIO & LED BD CONN



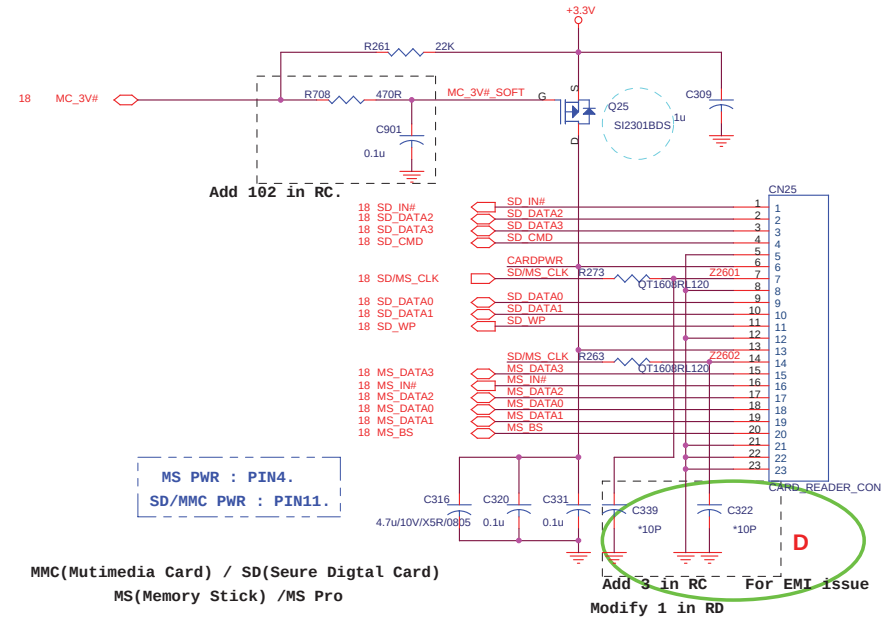
MDC BD's USB Conn

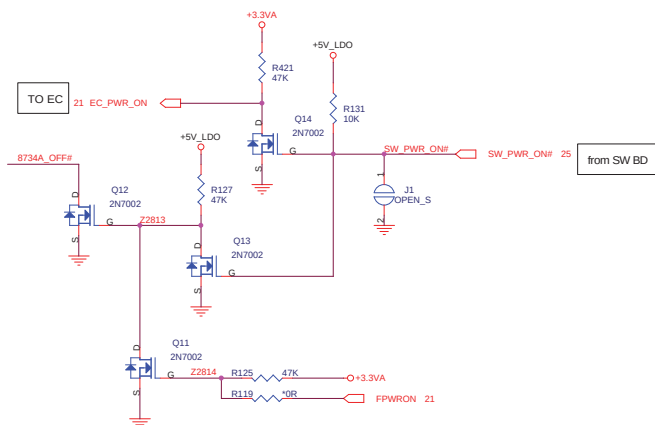
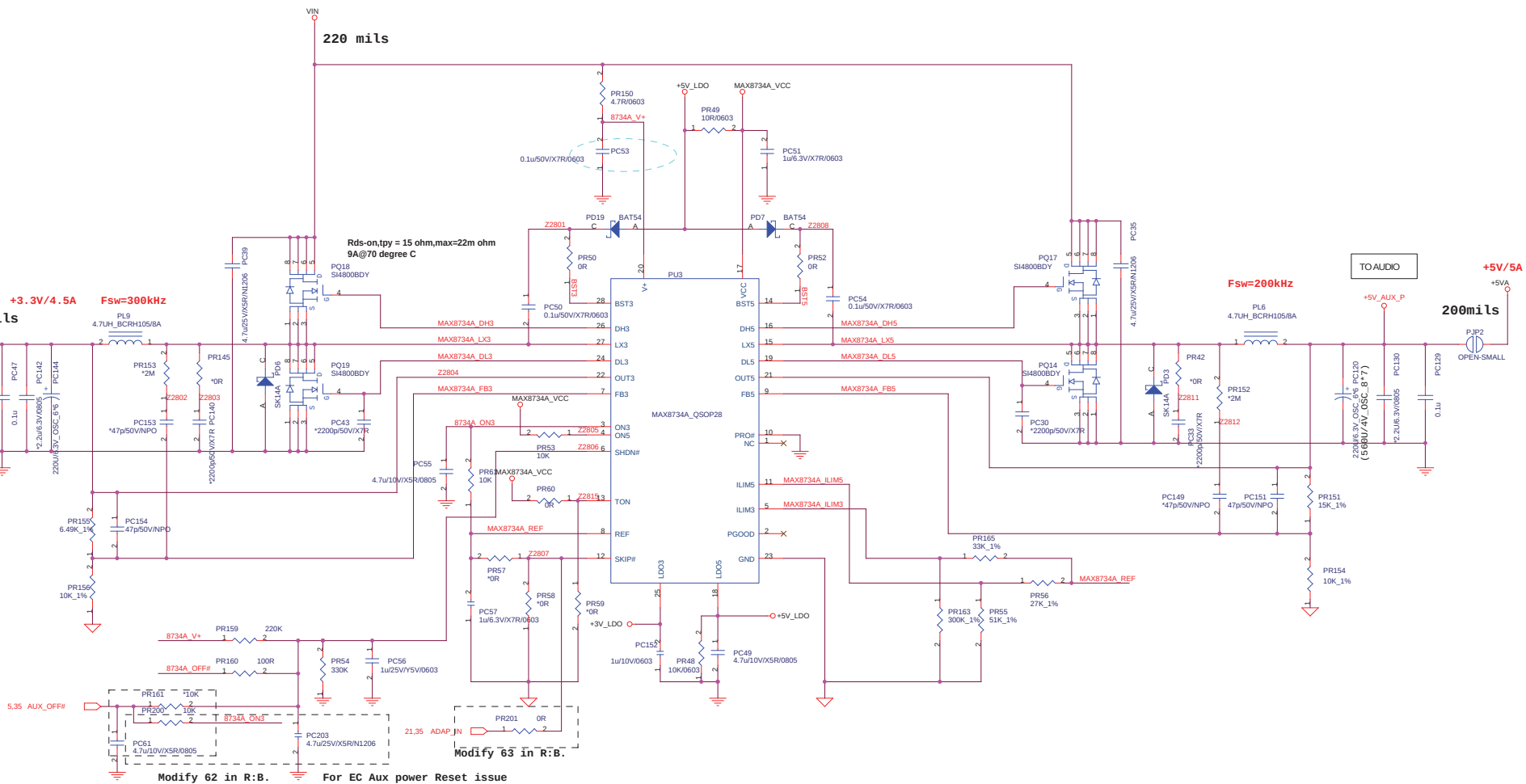


S-Vedio CONN



Name of Part	Daughter BD CONN	
Project	S50IA Main Board	Rev D
Date: Monday, July 10, 2006	Sheet	25 / 49
UNIWILL COMPUTER CORP.		





N.C.	1	 MAXIM <i>MAX8734A</i>	28	BST3
PGOOD	2		27	LX3
ON3	3		26	DH3
ON5	4		25	LD03
ILIM3	5		24	DL3
SHEIN	6		23	GND
FB3	7		22	OUT3
REF	8		21	OUT5
FB5	9		20	V+
PRO	10		19	DL5
ILIM5	11		18	LD05
SKIP	12		17	Vcc
TON	13		16	DH5
BST5	14		15	LX5

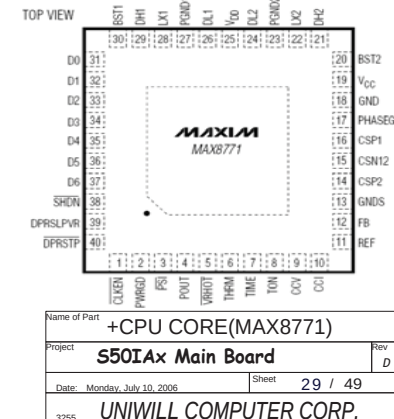
QSOP

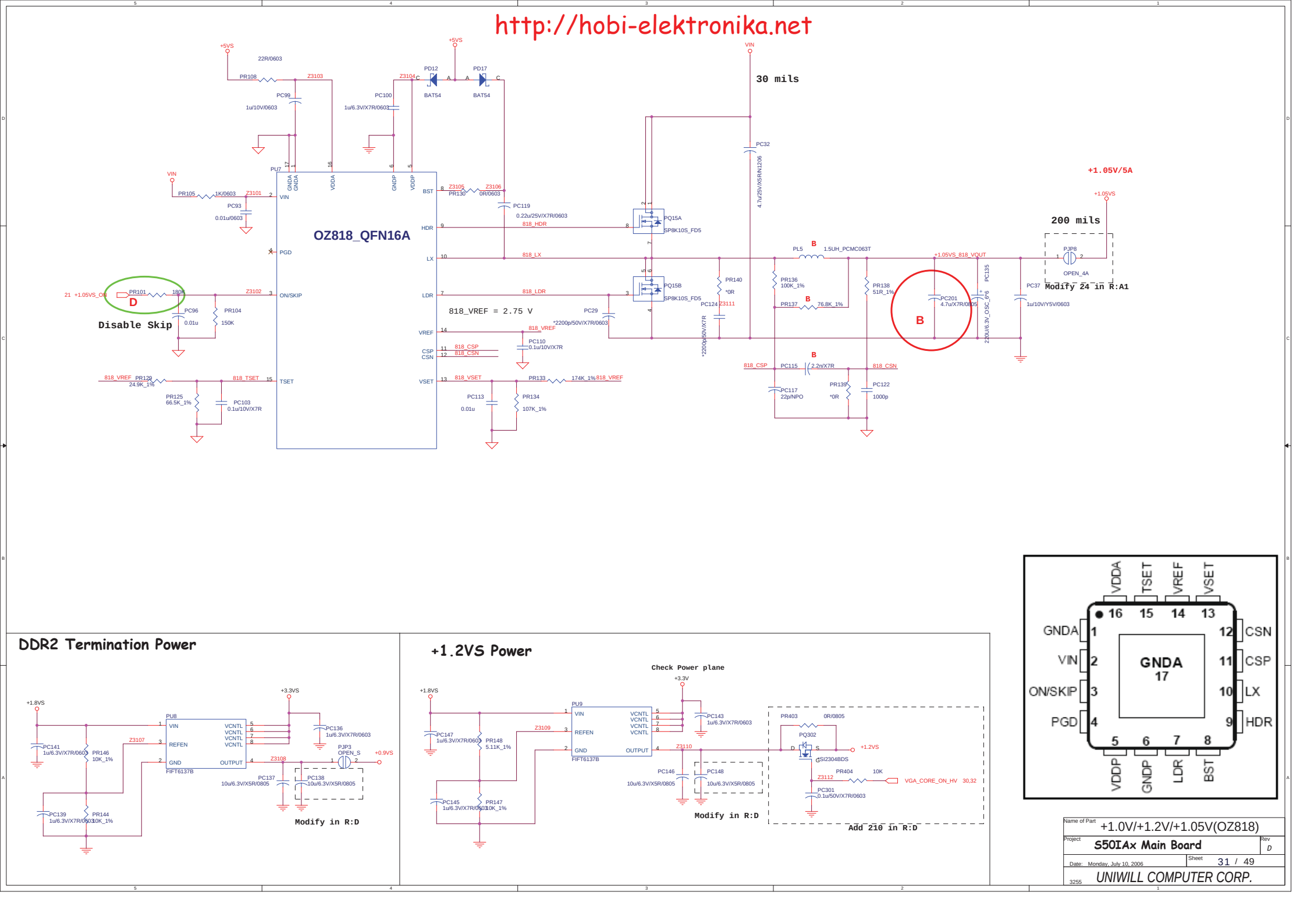
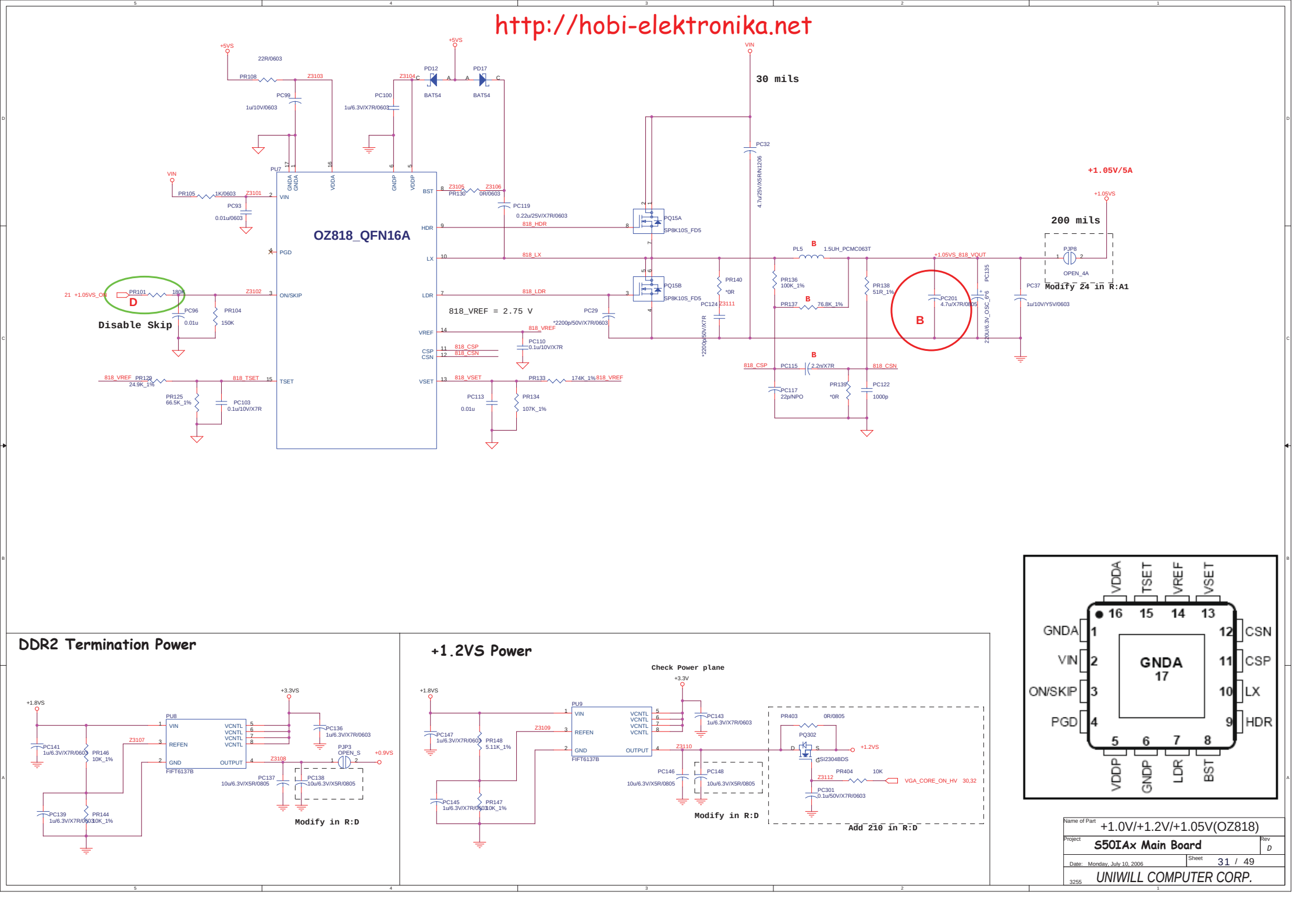
PR231	PR232	+3.3VA	+5VA
0R	NC	300KHz	200KHz
NC	0R	500KHz	400KHz

Name of Part		+5V&+3V(MAX8734A)	
Project	S501Ax Main Board		Rev D
Date	Monday, July 10, 2006	Sheet	28 / 49
3255 UNIWILL COMPUTER CORP.			

- 1.High side MOS change to RQA130N03*3PCS
- 2.Add output CAP PC42 (220uF/SPCAP/9mohm) Option
- 3.PR45 change to 3.3kohm
- 4.PR44 change to 1.8kohm
- 5.PC40 change to 0.22U/10V/X7R/0603
- 6.Add input CAP PC200 (4.7UF/1206)
- 7.PR117 change to 4.87kohm

6	5	4	3	2	1	0	Vcore	Status
0	0	1	0	0	0	1	1.2875	Yonah(HFM)
0	0	1	1	0	0	0	1.2000	Boat Vout
0	0	1	1	1	0	0	1.1500	Merom(HFM)
0	1	1	0	1	0	1	0.8375	Y&M(LFM)
0	1	1	1	0	1	1	0.7625	Y&M(Deeper Sleep)
1	1	1	1	1	1	1	0.0000	Shut down



[illegible][illegible][illegible]

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30 mils

200 mils

+1.05V/5A

+1.05V

+1.2VS

+0.9VS

+1.0V/+1.2V/+1.05V(OZ818)

S50IAx Main Board

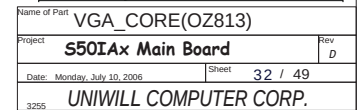
Date: Monday, July 10, 2006

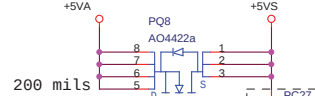
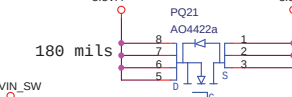
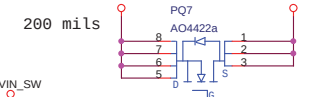
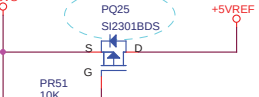
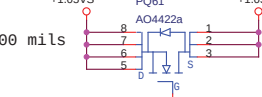
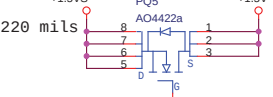
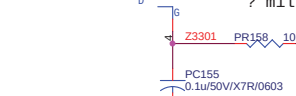
Sheet 31 / 49

UNIWILL COMPUTER CORP.

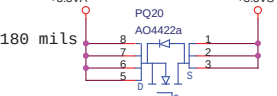
3255

[illegible]





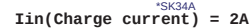
0603 Add 0.1U
between
U25 Pin3
and Pin4
for +5VS
drop
issue



Name of Part		VCC SW/Discharger	
Project	S50IAx Main Board		Rev D
Date:	Monday, July 10, 2006	Sheet	33 / 49
3255		UNIWILL COMPUTER CORP.	



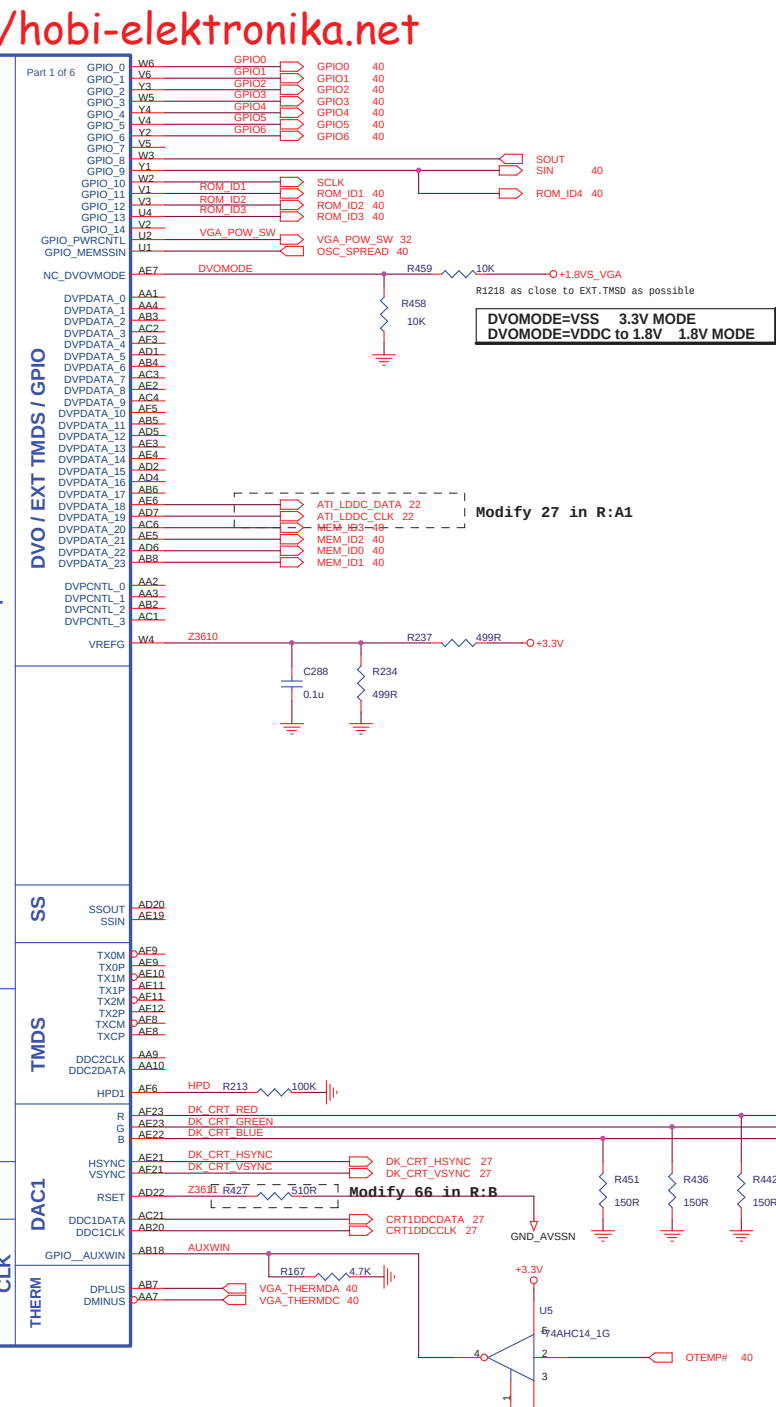
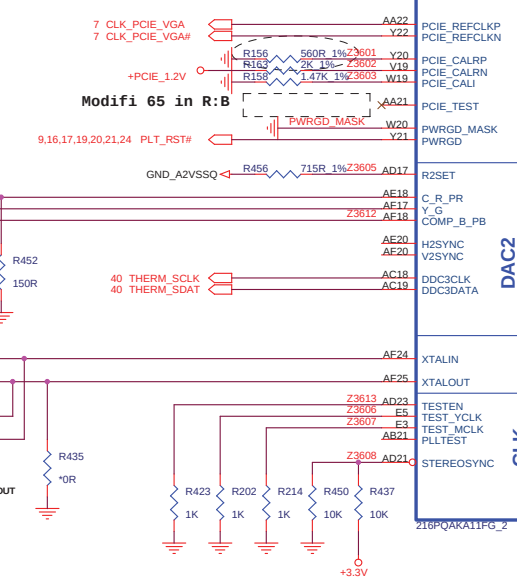
Slow Charge(Power On)



All designs with M5x (M58, M56, M54, M52) must populate the configuration pin strap on GPIO5. That is - add a 10K resistor to 3.3V on GPIO5. This pin strap sets the desired PCIE PLL bandwidth for M5x parts. The databooks and references schematics will be updated with this change.

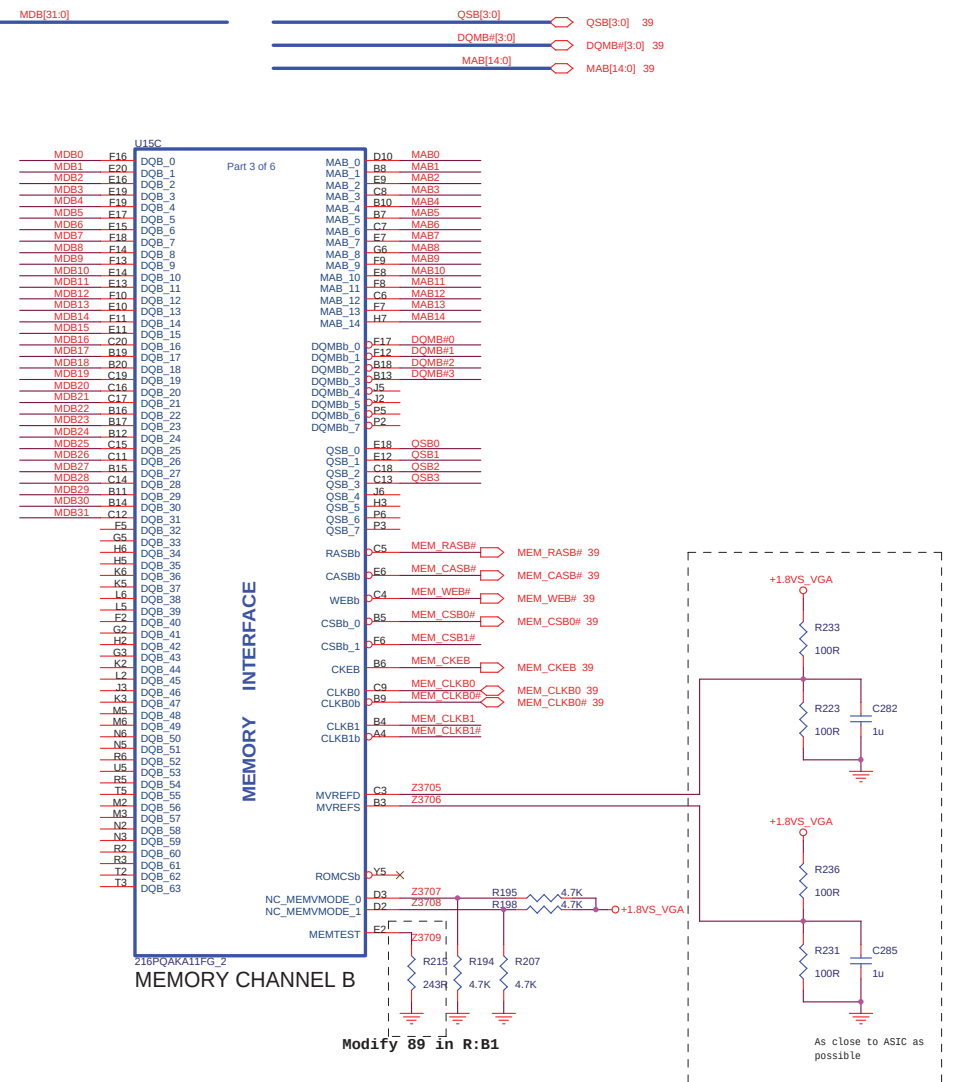
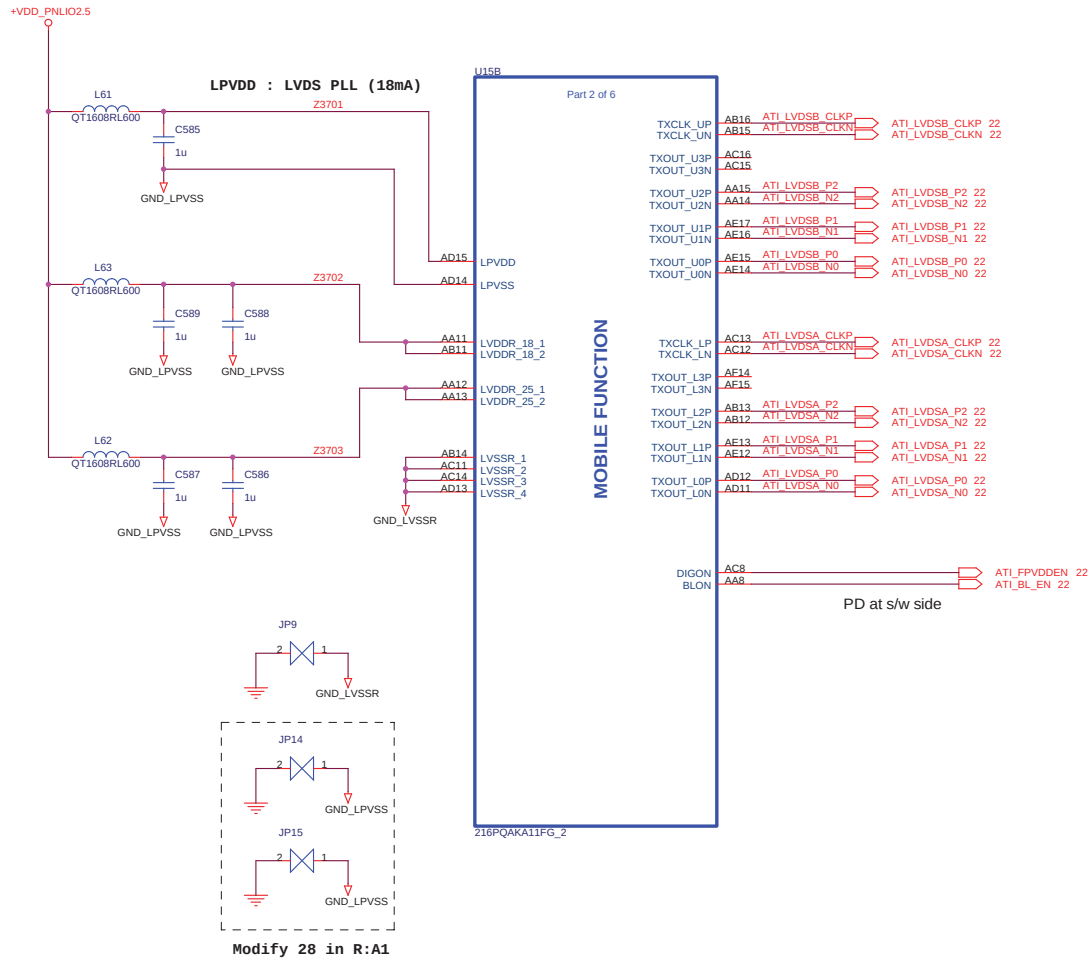
NB_PEG_RXN[15..0]	10	ATI_PEG_RXP0	AE26
NB_PEG_RXP[15..0]	10	ATI_PEG_RXN0	AD26
ATI_PEG_RXN[15..0]	10	ATI_PEG_RXP1	AB26
ATI_PEG_RXP[15..0]	10	ATI_PEG_RXN1	AA26
		ATI_PEG_RXP2	AA25
		ATI_PEG_RXN2	Y25
		ATI_PEG_RXP3	V25
		ATI_PEG_RXN3	V26
		ATI_PEG_RXP4	V25
		ATI_PEG_RXN4	U25
		ATI_PEG_RXP5	R25
		ATI_PEG_RXN5	T25
		ATI_PEG_RXP6	R25
		ATI_PEG_RXN6	P25
		ATI_PEG_RXP7	V25
		ATI_PEG_RXN7	M25
		ATI_PEG_RXP8	M25
		ATI_PEG_RXN8	L25
		ATI_PEG_RXP9	K25
		ATI_PEG_RXN9	J25
		ATI_PEG_RXP10	J25
		ATI_PEG_RXN10	G25
		ATI_PEG_RXP11	H25
		ATI_PEG_RXN11	F25
		ATI_PEG_RXP12	F25
		ATI_PEG_RXN12	D25
		ATI_PEG_RXP13	D25
		ATI_PEG_RXN13	C25
		ATI_PEG_RXP14	C25
		ATI_PEG_RXN14	B25
		ATI_PEG_RXP15	B25
		ATI_PEG_RXN15	A25

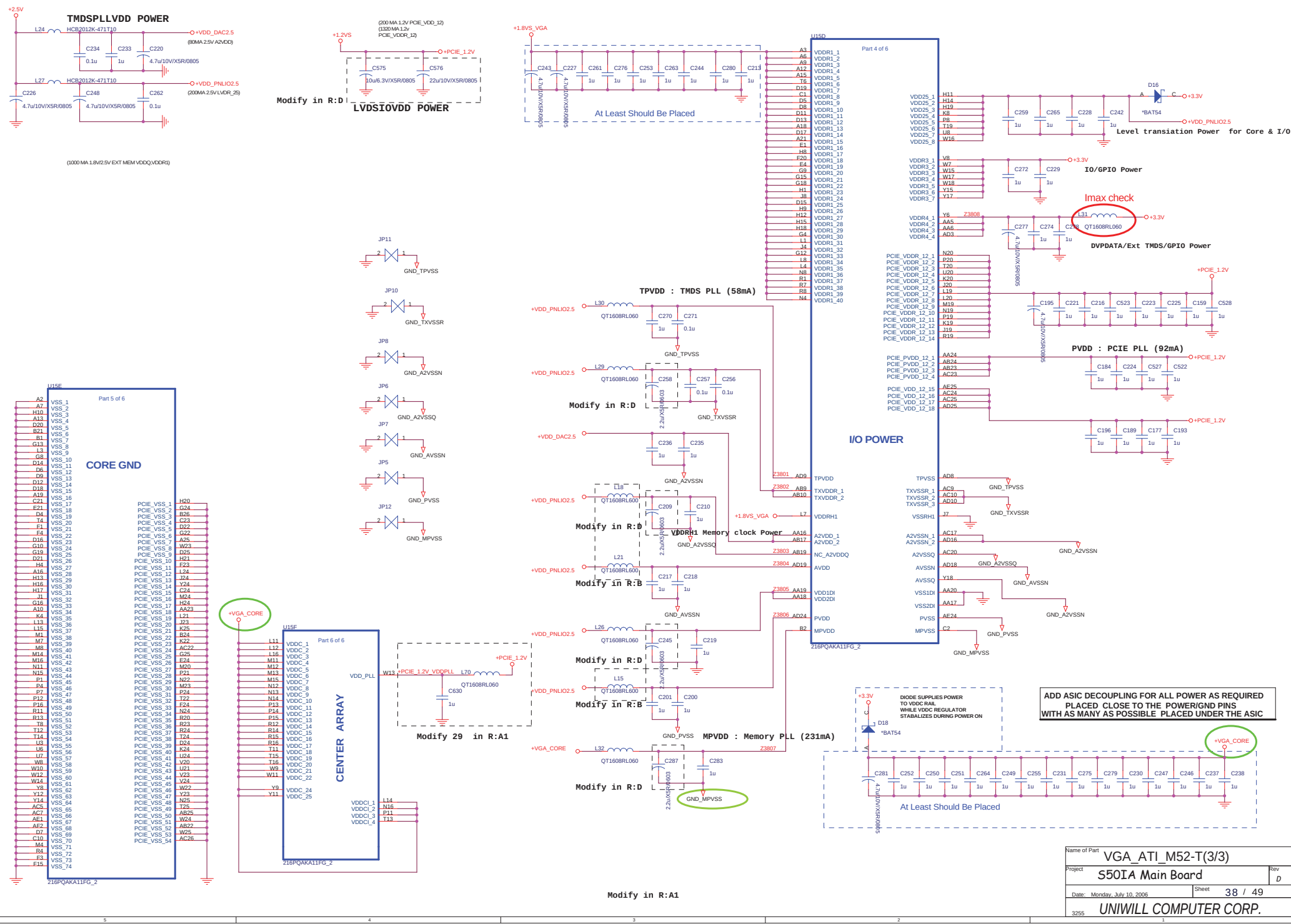
NB_PEG_RXP0	C574	1	2	0.1u	ATI_PEG_TXP0	W21
NB_PEG_RXN0	C573	1	2	0.1u	ATI_PEG_TXN0	V21
NB_PEG_RXP1	C160	1	2	0.1u	ATI_PEG_TXP1	U22
NB_PEG_RXN1	C161	1	2	0.1u	ATI_PEG_TXN1	U22
NB_PEG_RXP2	C572	1	2	0.1u	ATI_PEG_TXP2	U23
NB_PEG_RXN2	C571	1	2	0.1u	ATI_PEG_TXN2	T23
NB_PEG_RXP3	C162	1	2	0.1u	ATI_PEG_TXP3	T23
NB_PEG_RXN3	C163	1	2	0.1u	ATI_PEG_TXN3	R21
NB_PEG_RXP4	C570	1	2	0.1u	ATI_PEG_TXP4	R22
NB_PEG_RXN4	C569	1	2	0.1u	ATI_PEG_TXN4	E22
NB_PEG_RXP5	C164	1	2	0.1u	ATI_PEG_TXP5	E23
NB_PEG_RXN5	C165	1	2	0.1u	ATI_PEG_TXN5	N23
NB_PEG_RXP6	C568	1	2	0.1u	ATI_PEG_TXP6	N21
NB_PEG_RXN6	C567	1	2	0.1u	ATI_PEG_TXN6	M21
NB_PEG_RXP7	C166	1	2	0.1u	ATI_PEG_TXP7	M22
NB_PEG_RXN7	C167	1	2	0.1u	ATI_PEG_TXN7	L22
NB_PEG_RXP8	C566	1	2	0.1u	ATI_PEG_TXP8	K23
NB_PEG_RXN8	C565	1	2	0.1u	ATI_PEG_TXN8	K23
NB_PEG_RXP9	C168	1	2	0.1u	ATI_PEG_TXP9	K21
NB_PEG_RXN9	C169	1	2	0.1u	ATI_PEG_TXN9	J21
NB_PEG_RXP10	C564	1	2	0.1u	ATI_PEG_TXP10	J22
NB_PEG_RXN10	C563	1	2	0.1u	ATI_PEG_TXN10	H22
NB_PEG_RXP11	C170	1	2	0.1u	ATI_PEG_TXP11	H23
NB_PEG_RXN11	C171	1	2	0.1u	ATI_PEG_TXN11	G23
NB_PEG_RXP12	C562	1	2	0.1u	ATI_PEG_TXP12	G21
NB_PEG_RXN12	C561	1	2	0.1u	ATI_PEG_TXN12	F21
NB_PEG_RXP13	C172	1	2	0.1u	ATI_PEG_TXP13	F22
NB_PEG_RXN13	C173	1	2	0.1u	ATI_PEG_TXN13	E23
NB_PEG_RXP14	C560	1	2	0.1u	ATI_PEG_TXP14	E22
NB_PEG_RXN14	C559	1	2	0.1u	ATI_PEG_TXN14	D23
NB_PEG_RXP15	C174	1	2	0.1u	ATI_PEG_TXP15	C22
NB_PEG_RXN15	C175	1	2	0.1u	ATI_PEG_TXN15	B22

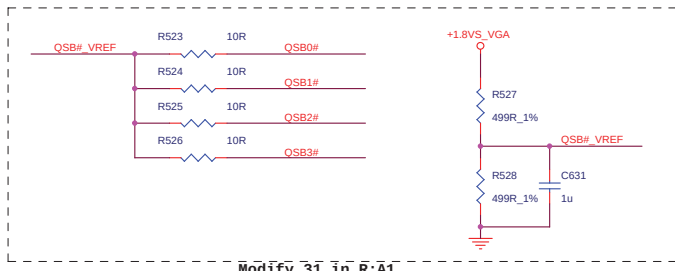
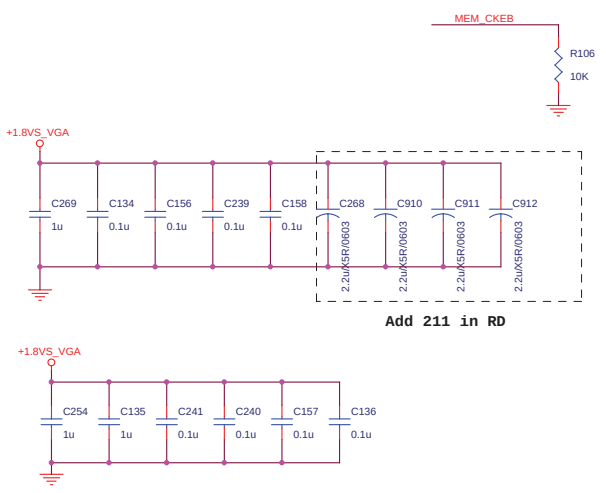
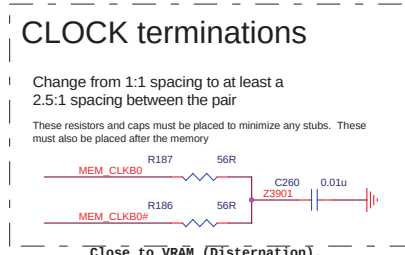
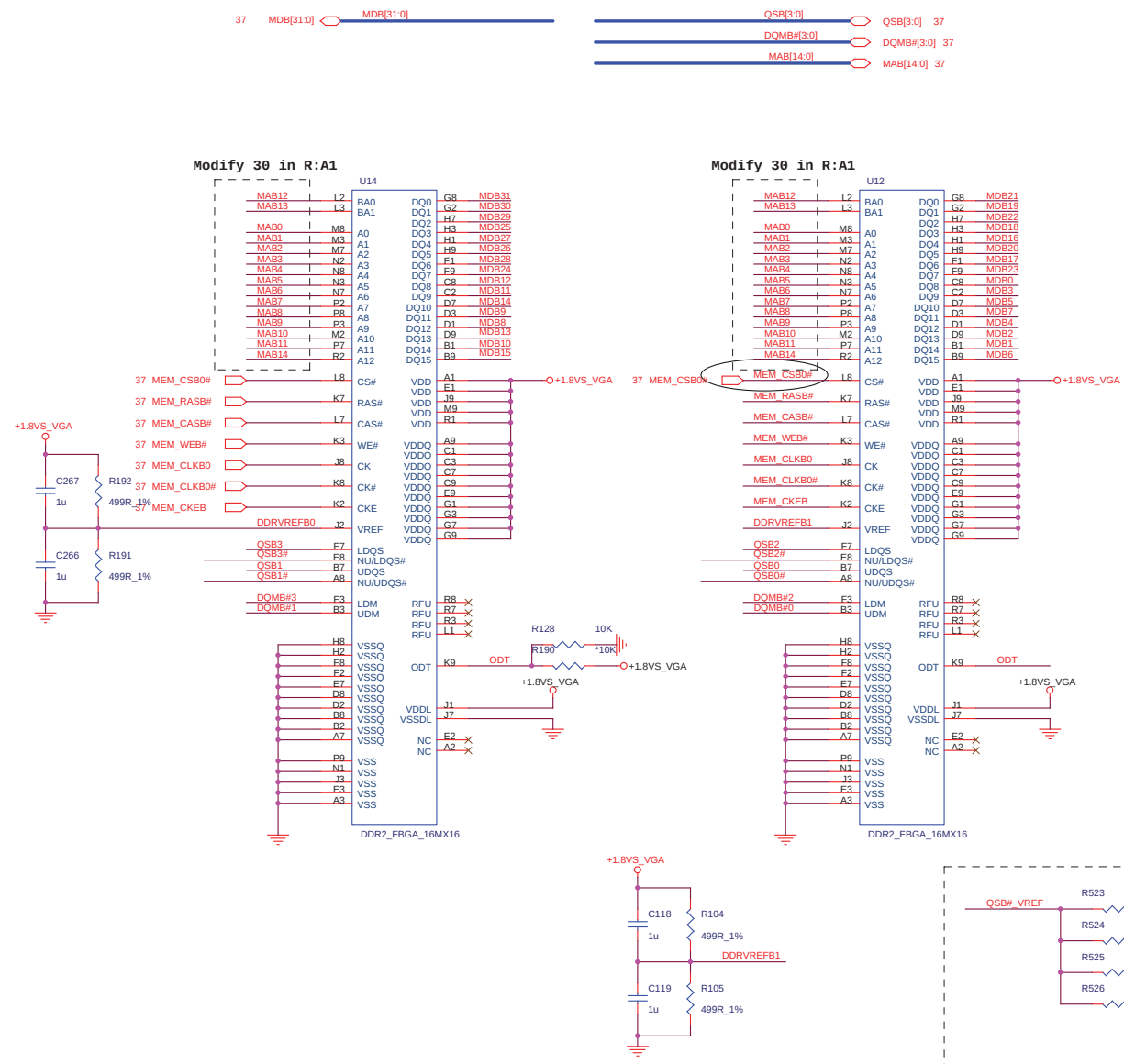


TC Modify 0914

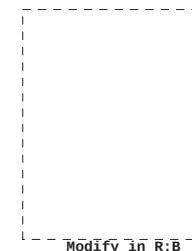
Name of Part	VGA_ATI_M52-T(1/3)	Rev	D
Project	S50IA Main Board	Date:	Monday, July 10, 2006
Sheet	36 / 49	3255	UNIWILL COMPUTER CORP.



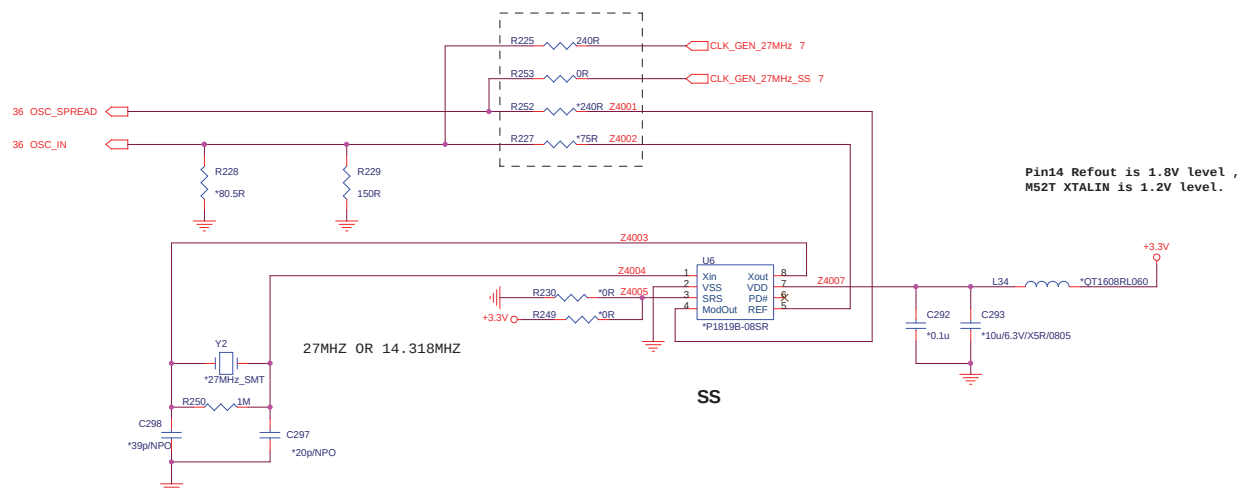




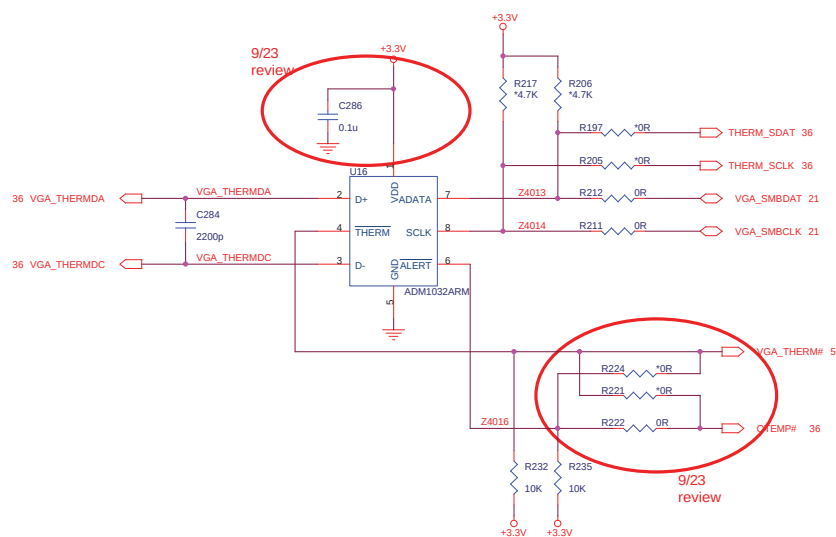
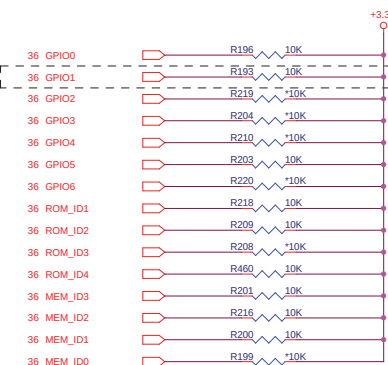
Name of Part			VGA_GDDR2
Project	S50IA Main Board	Rev	D
Date:	Monday, July 10, 2006	Sheet	39 / 49
3255			UNIWILL COMPUTER CORP.



- Modify in R:B



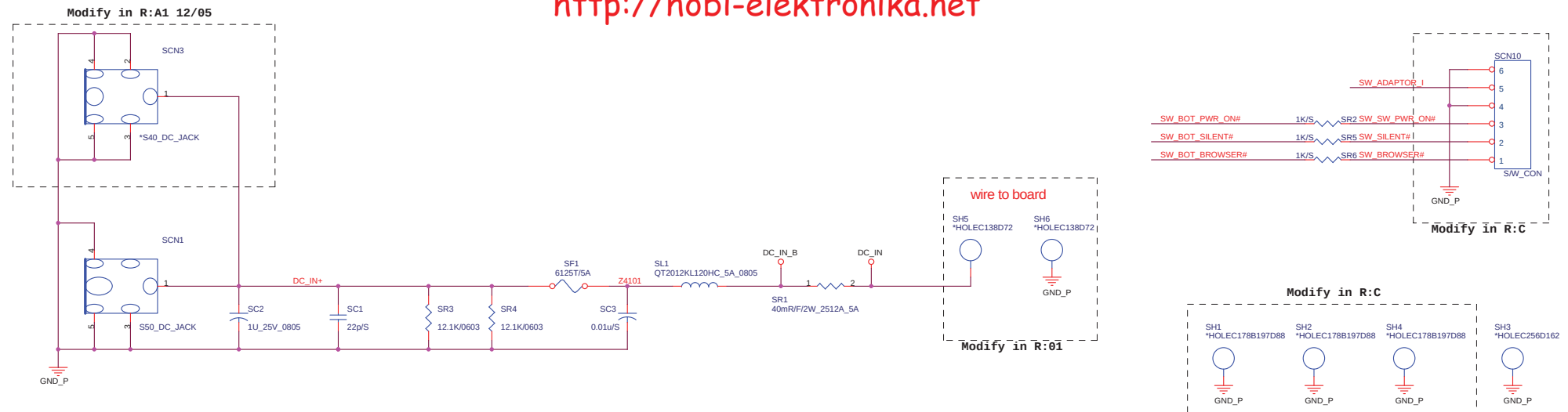
Add in R:B1



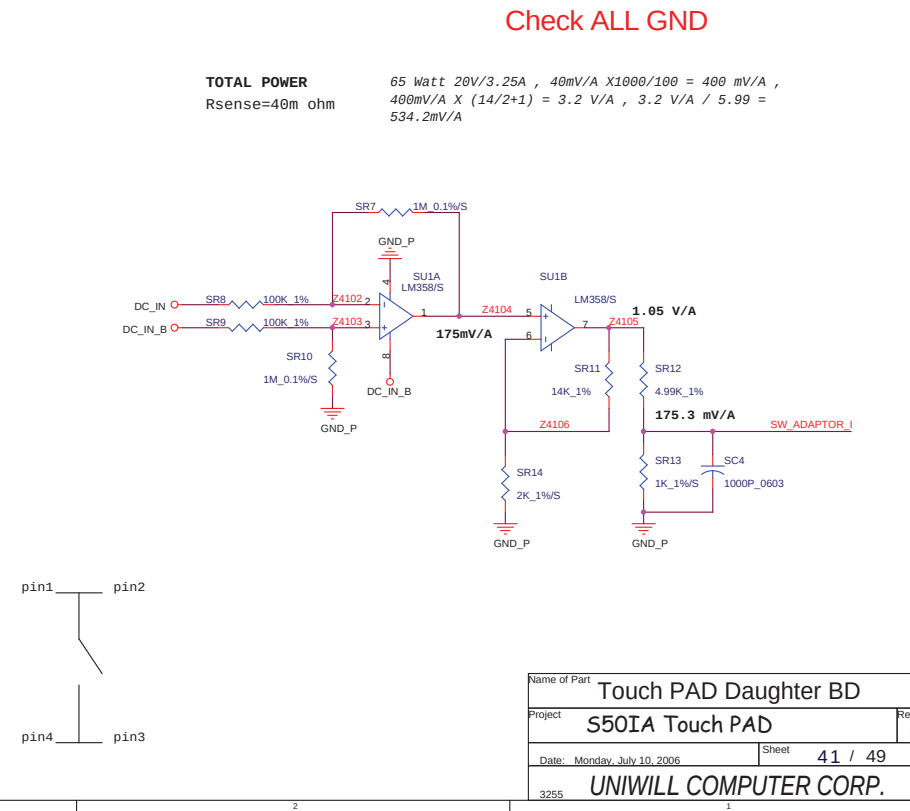
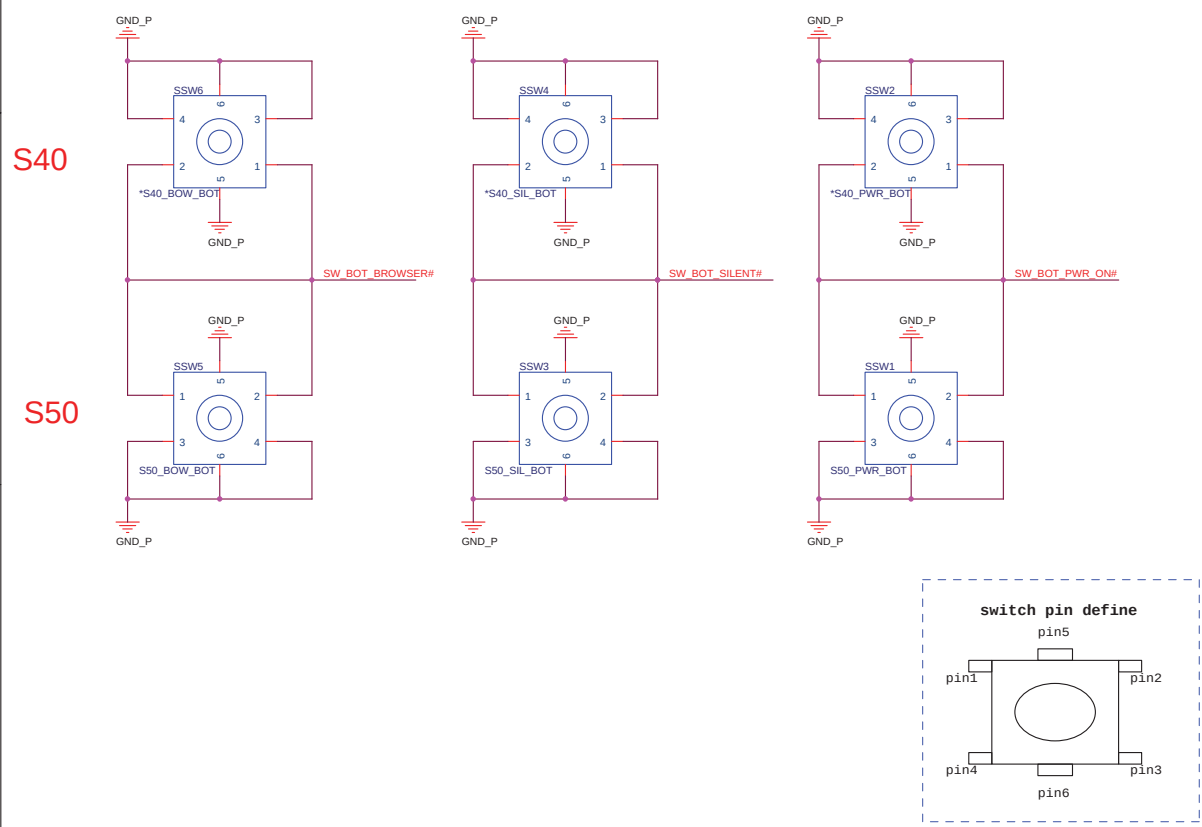
VRAM Type	MEM_ID[3,2,1,0]
DDR2 16MX16 HYPSS561621A1P-25 FBGA Hynix	[1,1,1,0]
DDR2 16MX16 84P K4N56163QF-ZC25 FBGA Samsung	[0,0,1,0]
DDR2 16MX16 84P K4N56163QF-ZC25 FBGA Samsung	[0,0,1,0]
DDR2 16MX16 HYB18T256161AFL-25 FBGA Infenion	[1,1,0,0]

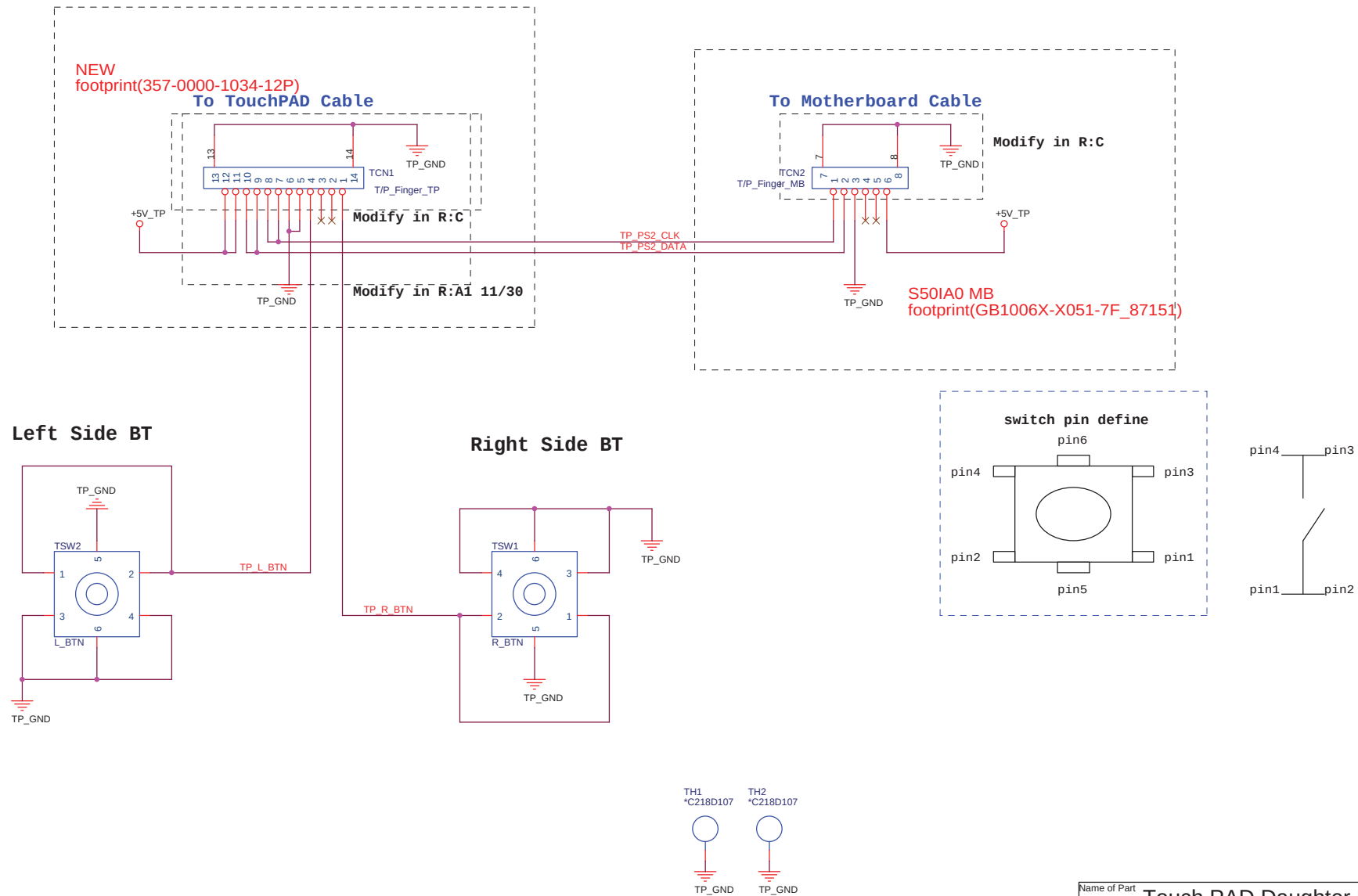
STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PRX_IDLE_MODE	PCI_TEST	PHY RECEIVER IDLE DETECTOR - NORMAL	DO NOT INSTALL 10K RESISTOR
STRAP_B_PTX_PWRS_ENB	GPIO0	Full swing	10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE - TX DE-EMPHASIS DISABLED FOR MOBILE	DO NOT INSTALL 10K RESISTOR
STRAP_PCIE_MODE	GPIO(3,2)	PCI-EXPRESS 1.0A MODE	DO NOT INSTALL 10K RESISTORS
STRAP_B_PTX_EXT	GPIO4	TRANSMITTER EXTRA CURRENT - NORMAL MODE	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE	GPIO5	DO NOT FORCE COMPLIANCE STATE QUICKLY	DO NOT INSTALL 10K RESISTORS
STRAP_B_PLLL_BW	GPIO6	PLL BANDWIDTH - FULL BANDWIDTH	DO NOT INSTALL 10K RESISTORS
RQIMDCFG(30)	ROMID (43)	SERIAL FLASH ROM TYPE SELECT - SERIAL MSP10 ROM	1011
MEM_TYPE	MEMID (30)	MEMORY TYPE AND SPEED SELECT - HYNIX 128MB	1100

Name of Part		VGA_SPRIC & ROM& STRAPS	
Project	S50IA Main Board	Rev	D
Date:	Monday, July 10, 2006	Sheet	40 / 49
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Rating button Func. TEXT





Name of Part	Touch PAD Daughter BD	
Project	S50IA Touch PAD	Rev D
Date: Monday, July 10, 2006	Sheet	42 / 49
3255	UNIWILL COMPUTER CORP.	

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S40 Modem RJ11 CONN

The diagram illustrates the S40 Modem RJ11 connection. It features an RJ11 connector (MMC3) on the left, connected to a modem chip (MMRV1) via two pins. The modem chip is connected to an RJ11 connector (MMC4) on the right via two pins. The modem chip has two ground connections (MMH1 and MMH2) and two signal lines (MODEM TX+ and MODEM RX+) connected to ground. The signal lines are also connected to the modem chip via capacitors (MMC4 and MMC5).

NEW footprint(PJS-02FC3G000A)

NEW footprint(307-0000-1066-02P)

MMH1 *HOLEC237D99

MMH2 *HOLEC178D87

MMDC_GND

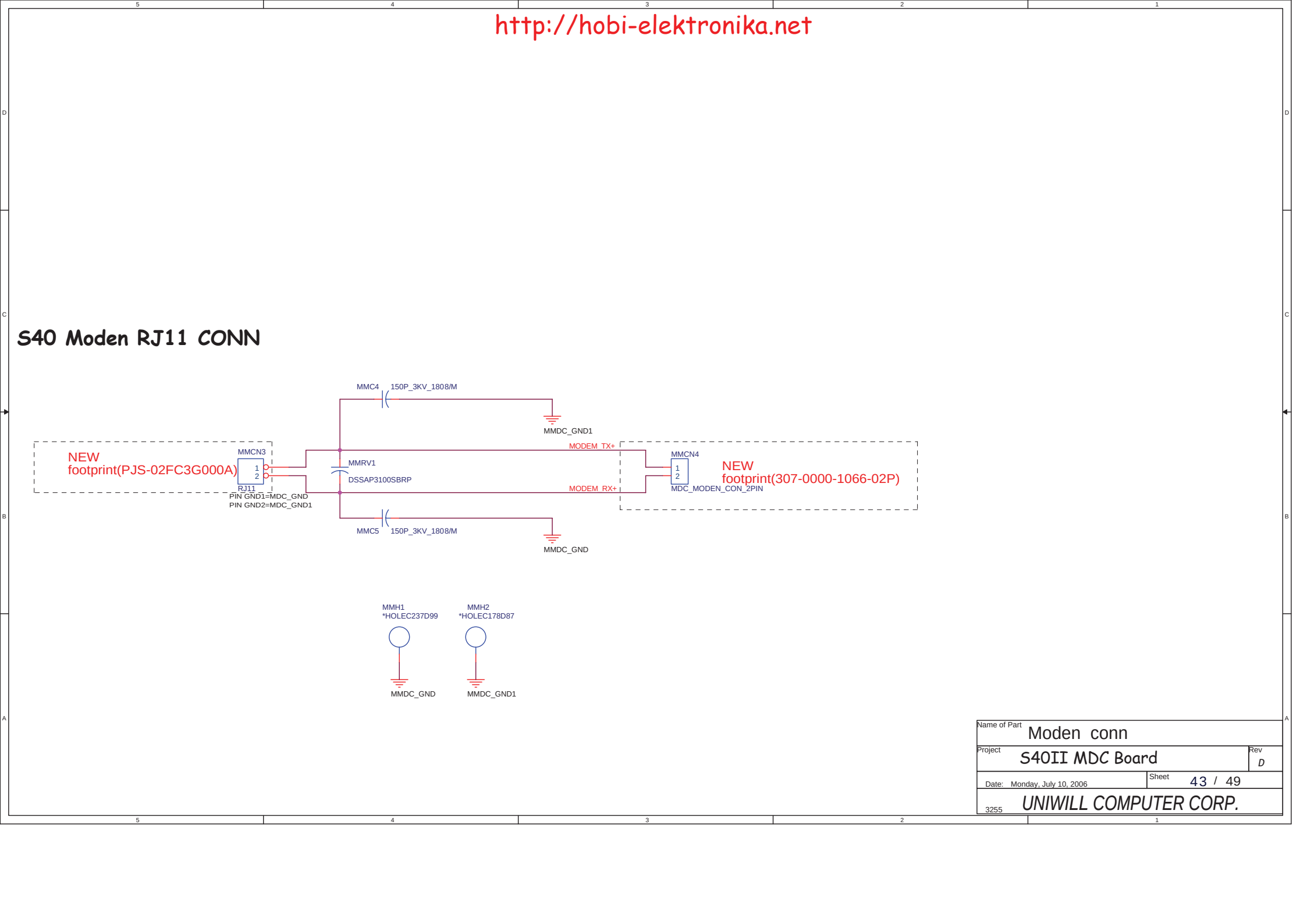
MMDC_GND1

MODEM TX+

MODEM RX+

MMDC_GND

Name of Part	Modem conn	
Project	S40II MDC Board	Rev D
Date: Monday, July 10, 2006	Sheet	43 / 49
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S40 Modem RJ11 CONN

NEW footprint(PJS-02FC3G000A)

MMC3
RJ11
PIN GND1=MDC_GND
PIN GND2=MDC_GND1

MMC4
150P_3KV_1808/M

MMRV1
DSSAP3100SBRP

MODEM TX+

MODEM RX+

MMC5
150P_3KV_1808/M

MMDC_GND1

MMDC_GND

MMH1
*HOLEC237D99

MMH2
*HOLEC178D87

MMDC_GND1

NEW footprint(307-0000-1066-02P)

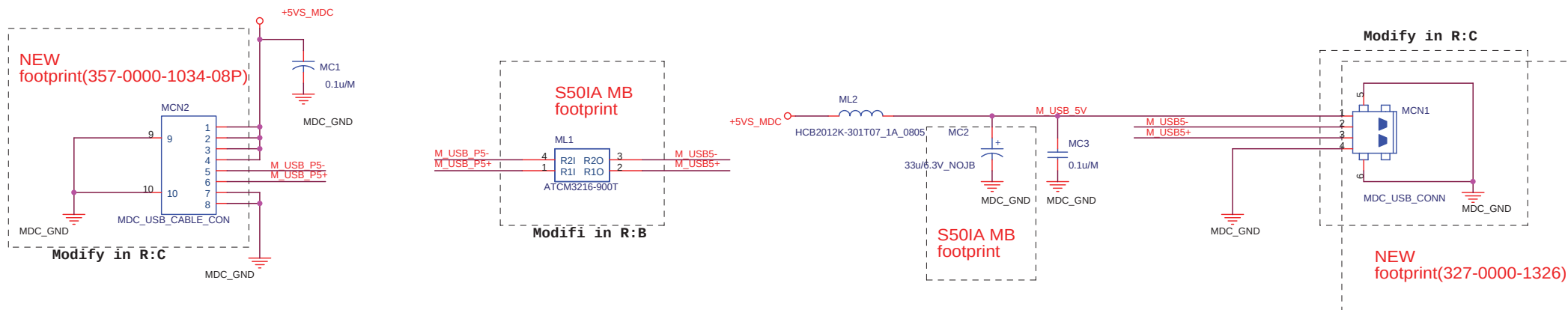
MMC4
1
2
MDC_MODEN_CON_2PIN

Name of Part		Modem conn	
Project		S40II MDC Board	
Date: Monday, July 10, 2006		Sheet	43 / 49
3255		UNIWILL COMPUTER CORP.	

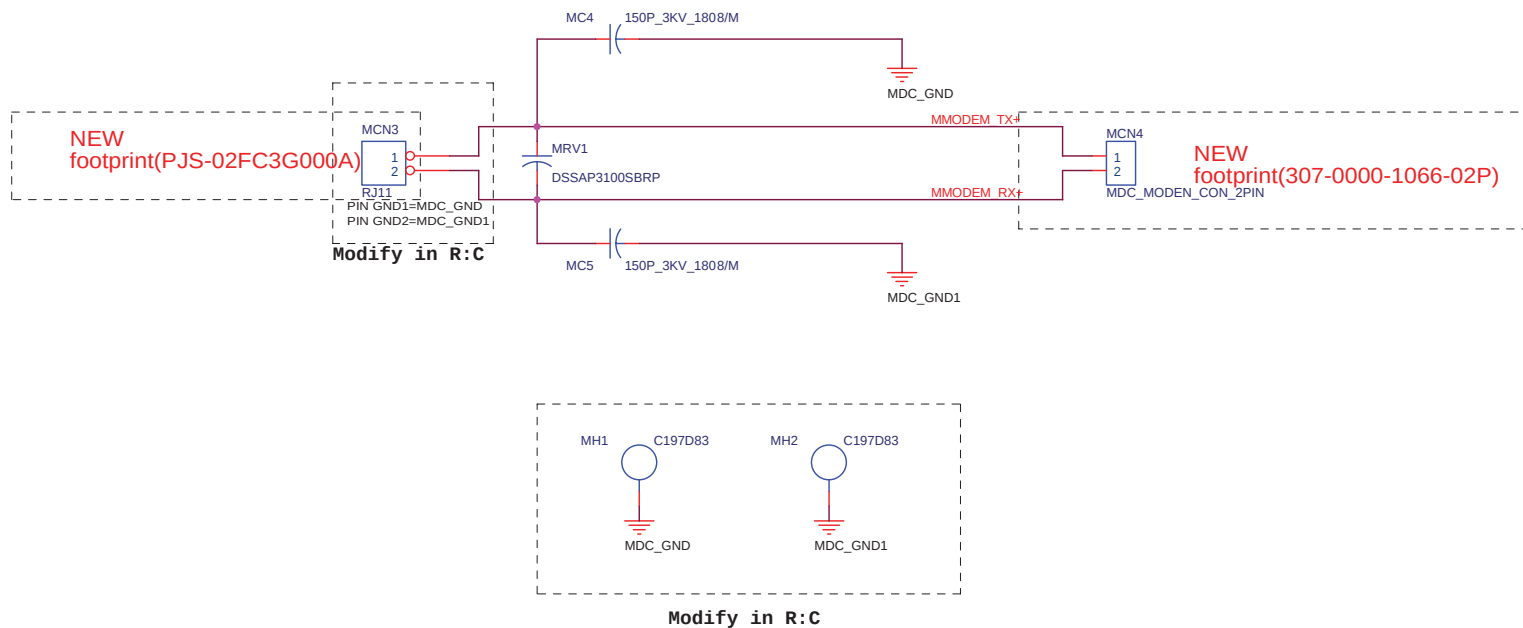
MDC USB CONN

<http://hobi-elektronika.net>

RE-Check ALL GND



Moden RJ11 CONN

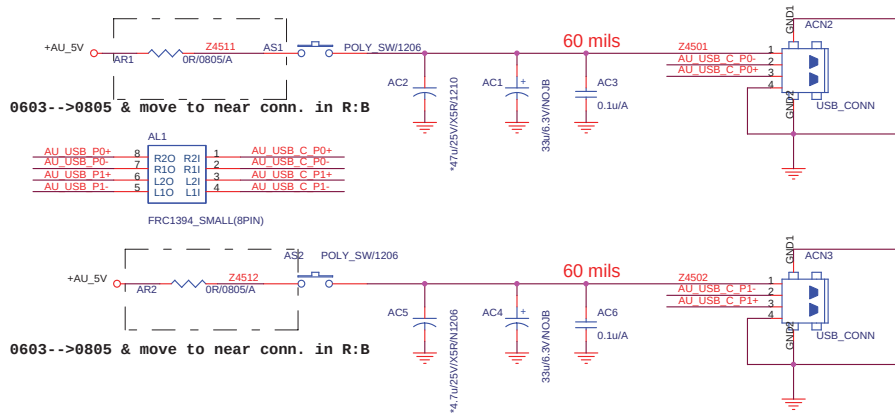


Name of Part	Moden & USB conn	
Project	S50IA MDC Board	Rev D
Date:	Monday, July 10, 2006	Sheet 44 / 49
3255	UNIWILL COMPUTER CORP.	

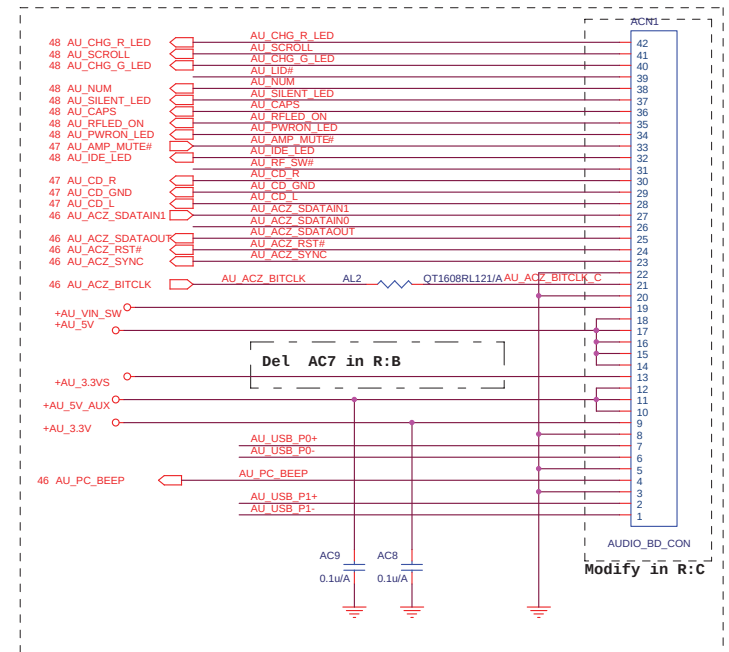
TWO PORT CONN

<http://hobi-elektronika.net>

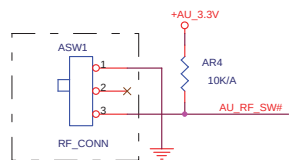
FROM MB BD CONN



Modify in R:A1 12/07



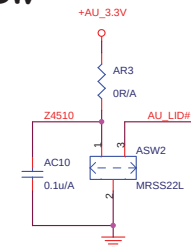
RF SW



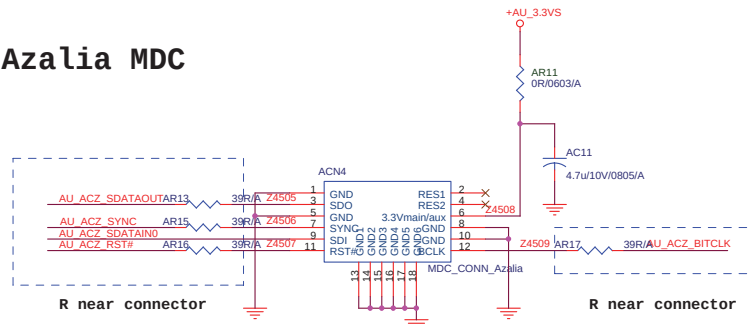
Modify in R:B & chage package for SMT issue

RF_OFF# -->Default is low.
SW Up-->pin1 & pin3 connection(RF ON).
SW Down-->pin2 & pin3 connection(RF OFF).
RF_OFF# from low to high-->EC pin is input type.

LID SW

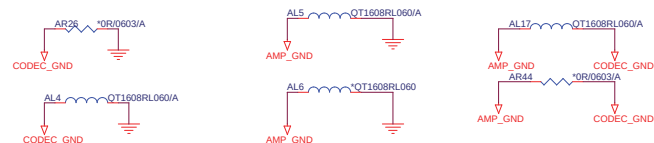
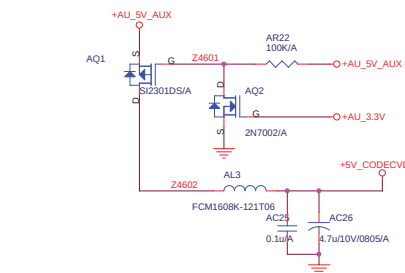


Azalia MDC

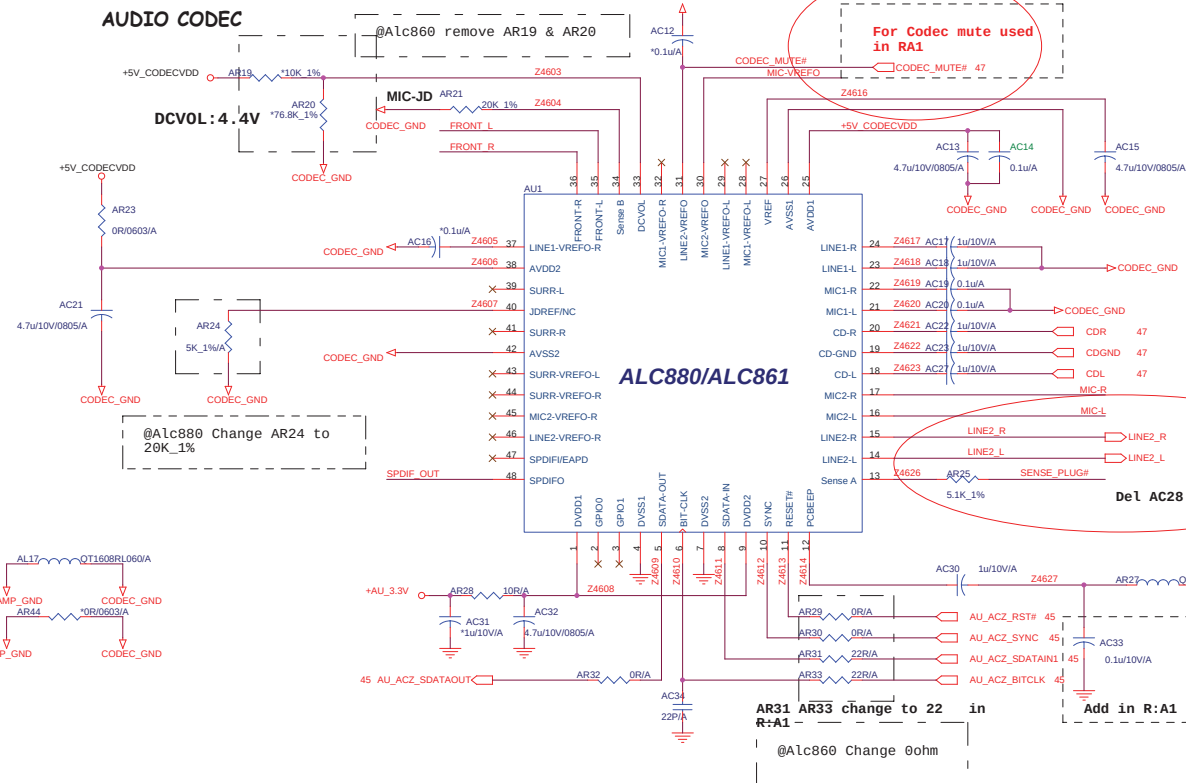


Name of Part	USB & FPC CONN	
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UNIWILL COMPUTER CORP.		

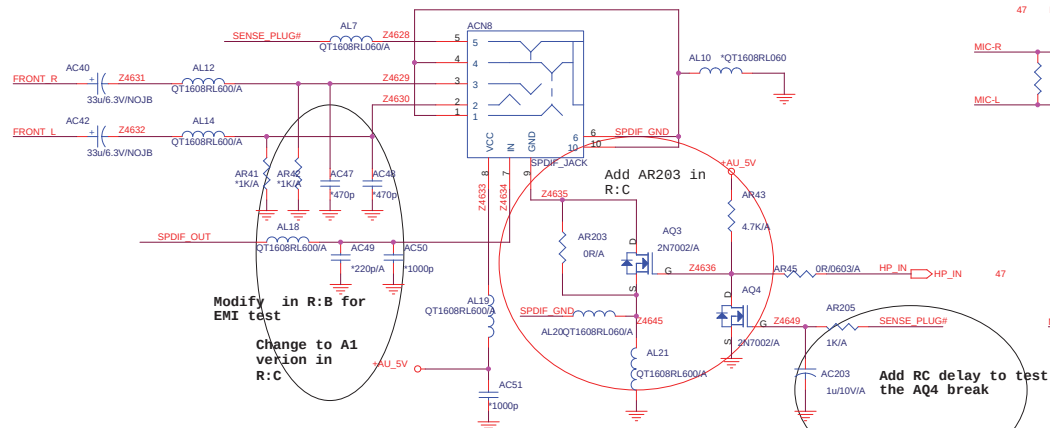
CODEC VDD



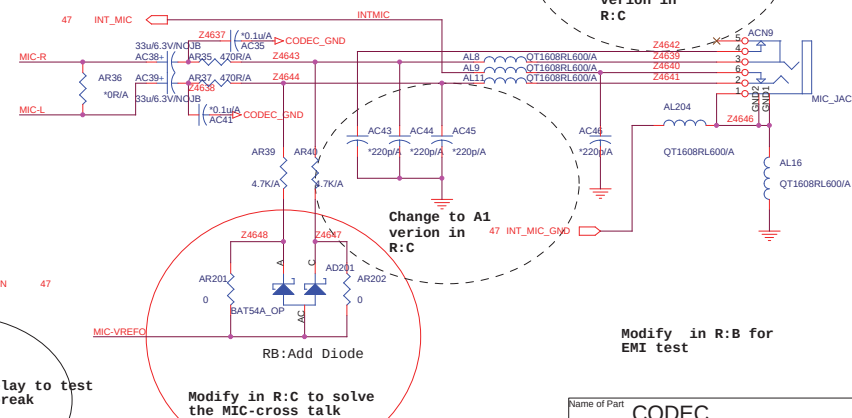
AUDIO CODEC



ERA/SPDIF JACK



MIC JACK

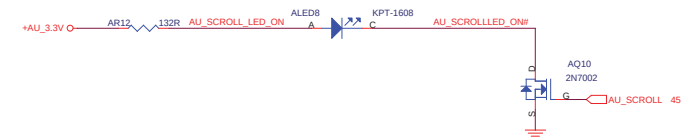
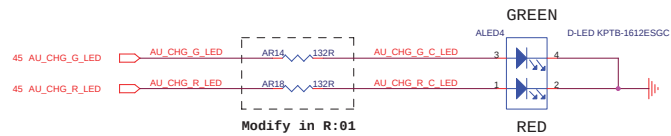
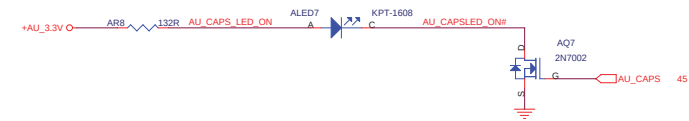
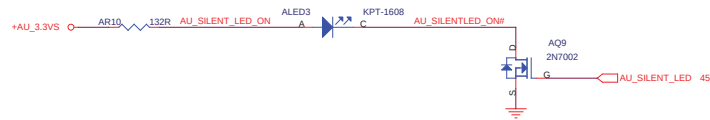
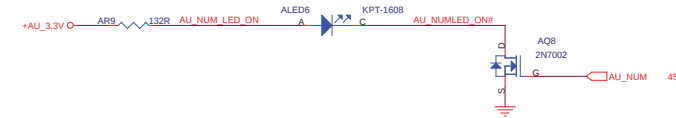
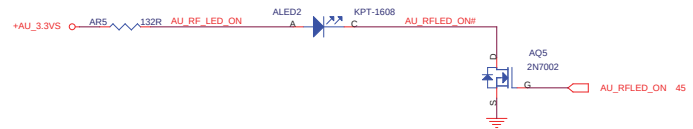
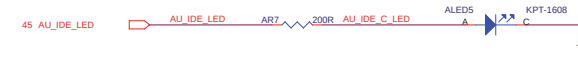
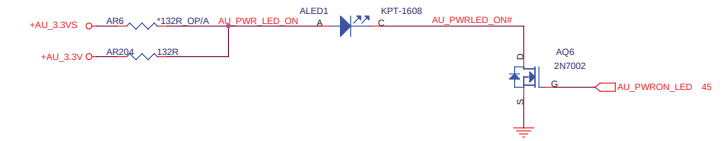


Name of Part		CODEC	
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3255	UNIWILL COMPUTER CORP.		

Rating LED indicate
Func. silkscreen

Change 3LP01->2N7002 in R:A1

LED



Name of Part	LED	
Project	S50IA AUDIO Board	Rev D
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3255	UNIWILL COMPUTER CORP.	

Chnage Note: R:A to R:A1

http://hobi-elektronika.net

Chnage Note: R:A1 to R:B

Layout:

1. page7 :Add R522 100ohm for CPU frequence Setting
2. page15:Change C438,C434 18P to 12P for RTC.
3. page16:Change Giga Lan PCI-E port in S/B, from port 4 to prot1.
4. page18:Add R533,R534 for OZ128TN core voltage 1.95V.
5. page19:Add 9 GND via under U8 body-pad for body GND.
6. page19:Add R520,R521 for U8 +1.5VS & +1.8VS.
7. page19:Reserve RS39 for S3 wake-up on LAN.
8. page21:Add 36_0N in EC for 3G module.
9. page21:Add BT_0N in EC for Bluetooth module.
10. page22: Add C642 for Invert can't tuon on.
11. page24:Exchahnge CLK_PCIE_Mini_Card(#!) for EMI.
12. page24:Reserve PCI_RST# for Mini Card.
13. page24:Add R538 for RFLED_ON.
14. page24:Add Cn30,L71,C731 for Bluetooth Module.
15. page24:Add C635,C636 in CLK_PIE_Mini_Card(#!) for EMI.
16. page24:Add R479,C619 for disable MiniCard CLK REQ#
17. page24:Change R531 power plane from +3.3VS_PCIE to +3.3VS.
18. page24:Del R302,R303.
19. page24:Add R535-R537,Q50-Q54 for New Card S3 issue.
20. page24:Add C639-C641,CN31 for 3G module.
21. page25:Exchange CN18 pin3,pin4 for pindefine error.
22. page25:Change CN19 from 40pin to 42pin.
23. page30:Change PU5 +3.3v to +5V for LDO Drop.
24. page31:Add PJP8 for +1.0VS.
25. page34:Add PR100 for CHG_ON floatong.
26. page35:Add R530,PQ100 for VIN_SW power off discharge.
27. page36:Exchange ATI_LDDC_DATA & CLK.
28. page37:Add JP14,JP15 for GND_LPVSS.
29. page38:Add L70,C630 for VDD_PLL.
30. page39:Change VRAM address pindefine.
31. page39:Add R523-R528,C631 for VRAM Vref.

BOM:

1. page7 :Add R522 10K.
2. page14:Change C438,C434 18P to 12P for RTC.
3. page18:Add R534 0 ohm 0805.
4. page19:Add R520,R521 0_0805 for U8 +1.5VS & +1.8VS.
5. page22:Add C642 0.1U for Invert can't turn on.
6. page24:Add R538 0 ohm,Del C612,Q40.
7. page24:Add R479 10K,C619 0.1U for disable MINICARD_LK_REQ#
8. page24:DelR302,R303 0 ohm 0803 for CLK_PCIE_NEW_CARD(#!).
9. page24:Add R535 100K,Q50 SI2302, Q51 2N7002 for New Card S3 issue.
10. page34:Add PR100 100K for CHG_ON floating.
11. page35:Add R530 100R_0603,PQ100 2N7002 for VIN_SW discharge.
12. page38:Add L70,C630 1U for VDD_PLL.
13. page39:Add R523-R526 10 ohm,R527-R528 499_1%,C631 1U for VRAM Vref.

Layout:

51. page 7:Add R600,R601 for PCI/CPU STOP# Pull high.
52. page14:Change C12,C13,C376 0402 to 0603.
53. page17:Add C700-C711 for S/B power Bypass C.
54. page18:Change U7 pin 65,66,68-70 from NC to GND.
55. page20:Reserve +3.3V on ODD con pin49.
56. page20:Modify HDD con package for SMT.
57. page21:Del R259 for NEW_CARD_Pwr_ON#.
58. page24:Add R602,R603 for New Card S3 issue.
59. page25:Del R188,R189 for SMT.
60. page25:Modify CN17 package.
61. page25:Add L100 for S-Vedio quality.
62. page28:Add PR200,PC203 for EC Aux power reset issue.
63. page28:Add PR201 for 3/5V skip mode.
64. page29:Del PC60.
65. page38:Del R170.
66. page38:Change R427.
67. page38:Change L15,L18,L21 for TV quality.
68. page40:Del U17.

BOM:

1. page 7:Add R601 10K/0603 for PCI STOP# pull-high.
2. page14:Change C12,C13,C376 0.1U_0402 to 0.1U_0603
3. page16:Change C56,C56,C60,C64,C71,C77 0.1u to 0.33u for WLAN.
4. page17:Add C700-C711 0.1u for S/B bypass C.
5. page19:Change C328,C330 0.1u to 0.33u for Giga Lan.
6. page24:Add R603 0 ohm for New Card S3 issue.
7. page28:Add PR200 10K,PC203 4.7U_25V_0805 for AUX reset issue.
8. page28:Add PR201 0 ohm for 3/5V skip mode.
9. page36:Change R427 from 499 to 510 for EMI.
10. page38:Change L15,L18,L21 from QT1608RL060 to QT1608RL600 for TV quality.
11. page40:Del U17.

Chnage Note: R:B to R:B1

Layout:

71. page14:Add C803-C806 for N/B +1.8VS
72. page15:Change CN21 RTC Con package.
73. page18:Change U18 AGND to GND.
74. page18:Del R241,R258 0 ohm.
75. page20:Modify HDD con package for SMT.
76. page20:Del C363.
77. page21:Modify T/P con package for SMT.
78. page21:Modify K/B con package for SMT.
79. page23:Add C800,801,Q60,R700,U30 for SmartPower.
80. page24:Add R701,R702 for BlueTooth SMB pull-up.
81. page24:AddR304-R306 PQ200,PQ201 for 3G power on.
82. page24:Modify CN6 package.
83. page25:Change all USB power from +5V to +5VS for S3 wake-up.
84. page25:Modify CN19 package.
85. page30:Add PR302,PR303 for Auto C4 adjust voltage.
86. page30:Change PU10 pindefined.
87. page32:Add PR300,PR301 for VGA power-play.
88. page35:Del D4,D21,R11.
89. page37:Change R215.

BOM:

1. page14:Add C803-C806 0.1U
2. page14:Change C12,C13,C376 0.1U_0402 to 0.1U_0603
3. page18:Del L25.
4. page18:Del R241,R258 0 ohm.
5. page23:Add C800-C801 0.1U,Q60 2N7002,R700 10K,U30 74AHC1G32.
6. page24:Add R304 1K,R305 100K,R306 10K,PQ200 2N3904,PQ201 2N7002 for 3G power on.
7. page30:Add PR302-PR303 100K for Auto C4.
8. page32:Add PR300-PR301 0 ohm for VGA power-play.
9. page37:Change R215 From 47 to 243 for ATI recommend.
10. page40:Add R193 10K for VGA Lanes switch issue.
11. page16:Del R264,add R392 0 ohm for S3 resume issue.

Chnage Note: R:D to R:01

BOM:

1. page35:Add R361 100,PQ60 2N7002 for power-off disachrgre.

Chnage Note: R:B1 to R:C

Layout:

100. page24:Add R706,R707 for cost down.
101. page24:Add C900 for EMI.
102. page26:Add R708,C901 for CardReader power Soft start.
103. page27:Add R704,R705 for Projector ghost issue.
104. page30:Change PR181 package from 0402 to 0805 for voltage drop.

BOM:

1. page24:Add C900 0.1U for EMI.
2. page26:Add R708 470,C901 0.1U for power soft start.
3. page26:Add C322,C339 10P for EMI.
4. page27:Add R704-R705 0 ohm for Projector ghost issue.
5. page:Change PR181 from 10_0402 to 10_0805 for voltage drop.

Chnage Note: R:C to R:D

Layout:

200. page25:Add R800 for D14 burned-out issue.
201. page27:Add R801,R802 for CDT signal.
202. page35:Del D14 for SMT.
203. page23:Add R803 for Smart Power.
204. page24:Del L41 for SMT.
205. page20:Modify CN16 package for SMT.
206. page20:Modify CN5 package for SMT.
207. page27:Modify CN6 package for SMT.
208. page32:Add PR400,PR405,PQ300,PQ303 for S3 power sequence.
209. page30:Add PR401,PR402,PC300,PQ301 for S3 power sequence.
210. page31:Add PR403,PR404,PC301,PQ302 for S3 power sequence.
211. page30:Add C260,C916-C912 for VRAM 1.8V bypass C.
212. page09:Add R804 for CAE function.
213. page09:Add R805-808 for N/B reserved function.

BOM:

1. page25:Add R800 100K for D14 burned-out issue.
2. page26:Del C322,C339 10P for CardReader can't be detected issue.
3. page24:Change Q60 from SI2302 to SI2304 for Vgs issue.
4. page30:Change PR6 160K 1% for 1.5V level.
5. page30:Change PR92,PR97 180K for disable skip mode.
6. page31:Change PR101 180K for disable skip mode.
7. page32:Change PR75,PR78 180K for disable mode.
8. page30:Add PR402 10K,PC300 0.1U_0603,PQ301 SI2304 for S3 sequence.
9. page31:Add PR404 10K PC301 0.1U_0603,SI2304 for S3 sequence.
10. page32:Add PR400 10K,PR405 100K,PQ300,PQ303 2N7002 for S3 sequence.
11. page05:Del R102 150 ohm for STPCLK#.
12. page16:Change R336 from 499 to 0 ohm for CAE.
13. page29:Change PR22 from 0 to 499 ohm for CAE.
14. page38:Change C209,C245,C258,C287 from 1u_0402 to 2.2U_0603_X5R for VGA PLL.
15. page07:Change C350,C351 to 0603 size,Add C357.
16. page14:Change C12,C13,C376 to 2.2U,C370,C383 to 22U for 3D restart issue.
17. page31:Add PC138,PC148 10U for 3D Blue Screen issue.
18. page38:Change C576 to 22U,C575 to 10U for 3D Blue Screen issue.
19. page15:Change R373 to 20K for RTC_RST# rise time.

Name of Part		CHANGE NOTE	
Project	S501Ax Main Board		Rev D
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3255	UNIWILL COMPUTER CORP.		