

02版基板

Version History

[illegible][illegible]

PCI BUS NUMBER = #8		
IDSEL	Dev.Number	Device
AD24	08h	PCIC / IEEE1394 /MSSD
AD25	09h	
AD26	0Ah	
AD27	0Bh	
AD28	0Ch	

SMBus

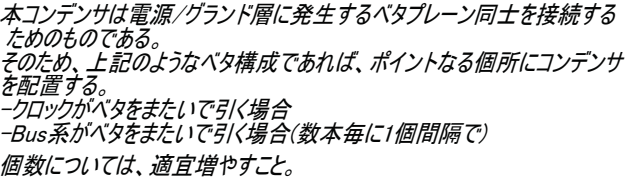
address	Device
A0h	LCD
A2h	DIMM1
A4h	DIMM2
5Eh	Thermal IC
D2h	PLL
32h	PMU

									TITLE	
									VB313AA	
									DRAW. No.	CAST
									C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	1 / 93		

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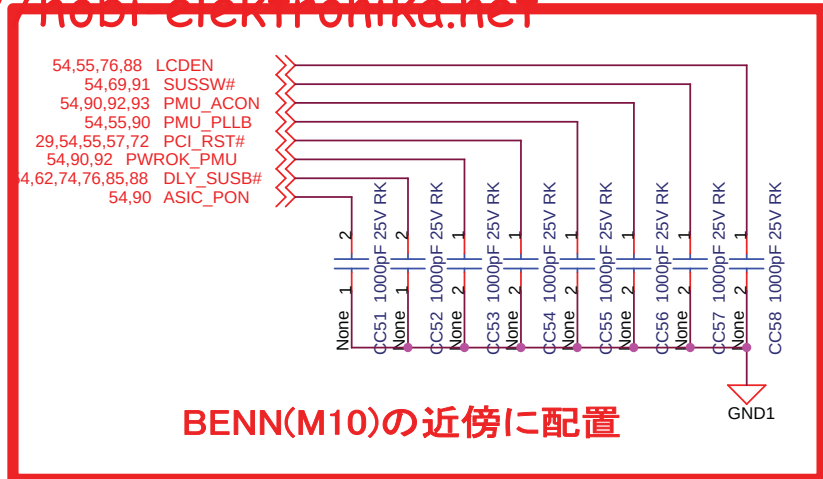


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									DRAW. No.	CAST
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Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	3 / 93		

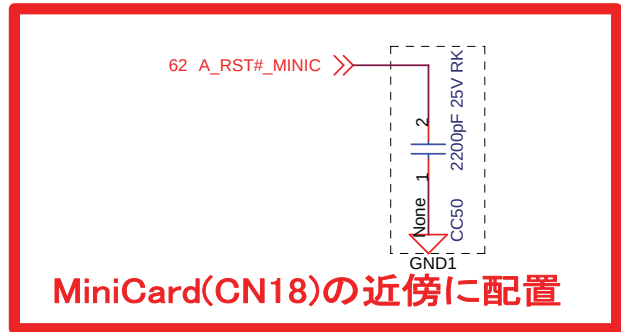
<http://hobi-elektronika.net>



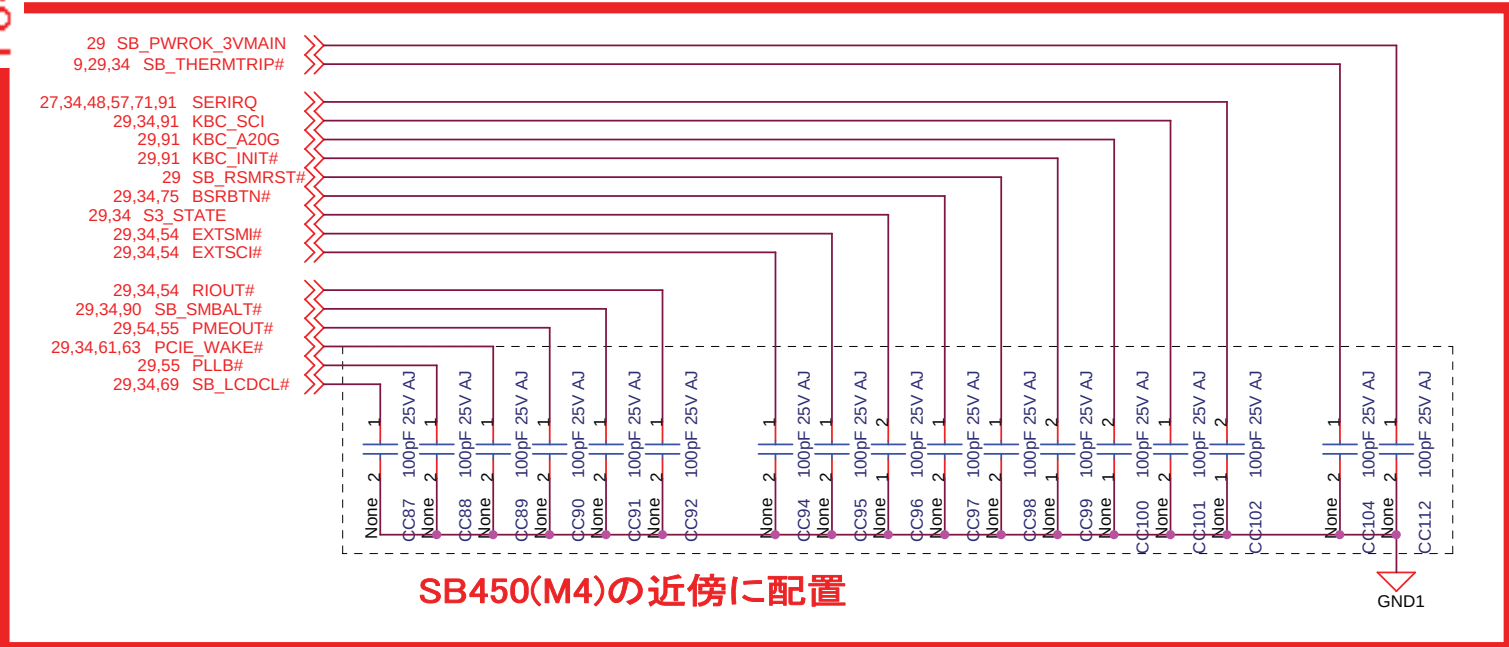
CPU(CN1)の近傍に配置



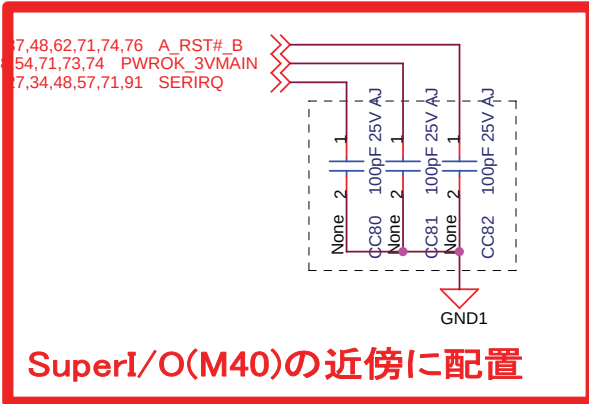
BENN(M10)の近傍に配置



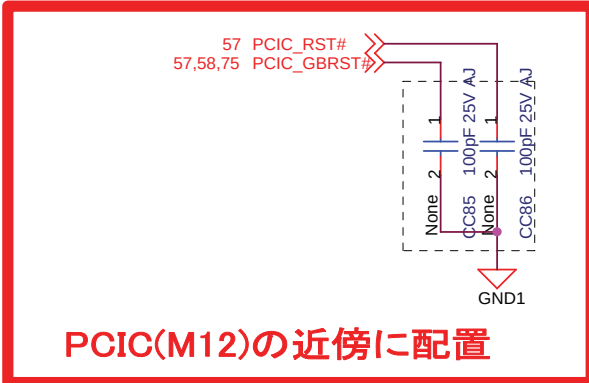
MiniCard(CN18)の近傍に配置



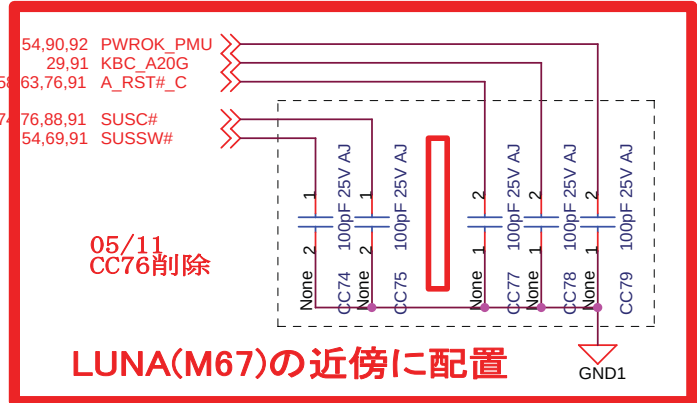
SB450(M4)の近傍に配置



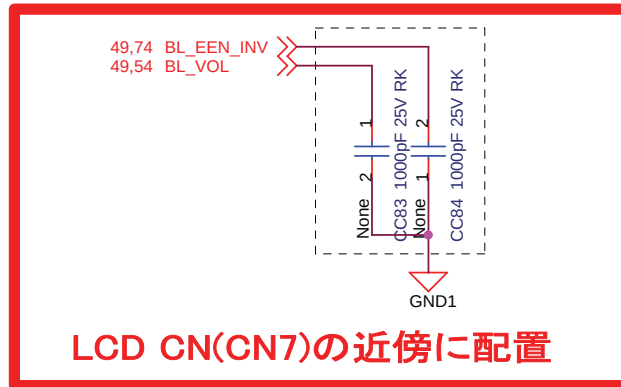
SuperI/O(M40)の近傍に配置



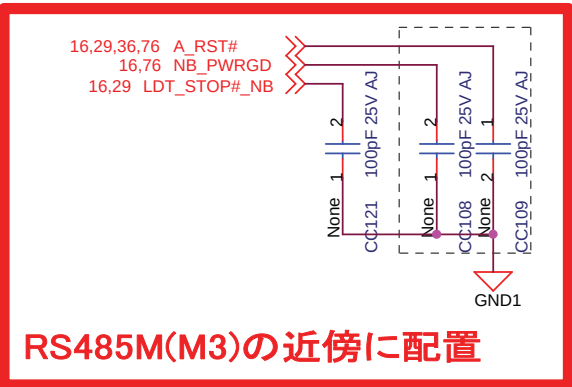
PCIC(M12)の近傍に配置



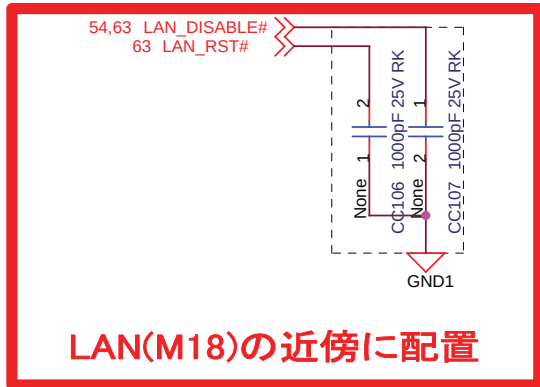
LUNA(M67)の近傍に配置



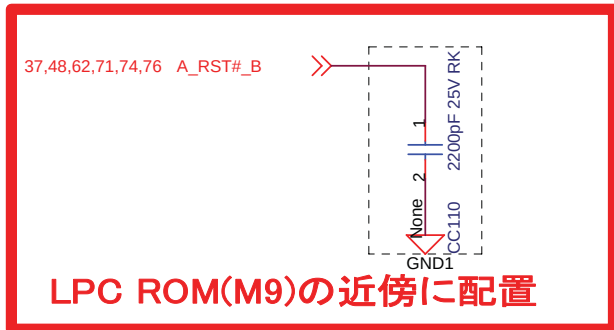
LCD CN(CN7)の近傍に配置



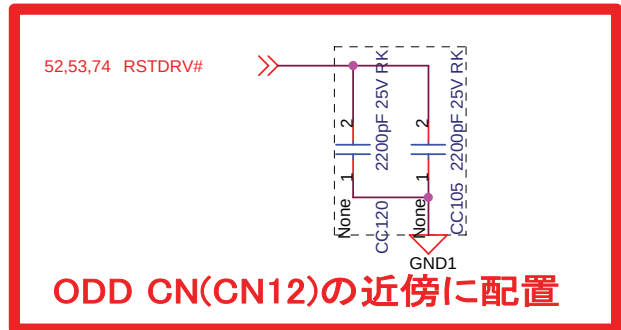
RS485M(M3)の近傍に配置



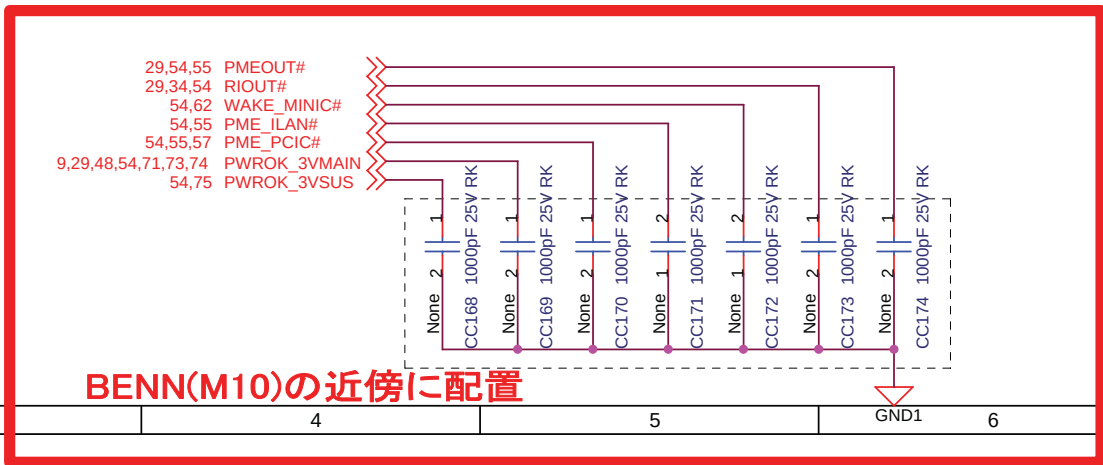
LAN(M18)の近傍に配置



LPC ROM(M9)の近傍に配置



ODD CN(CN12)の近傍に配置



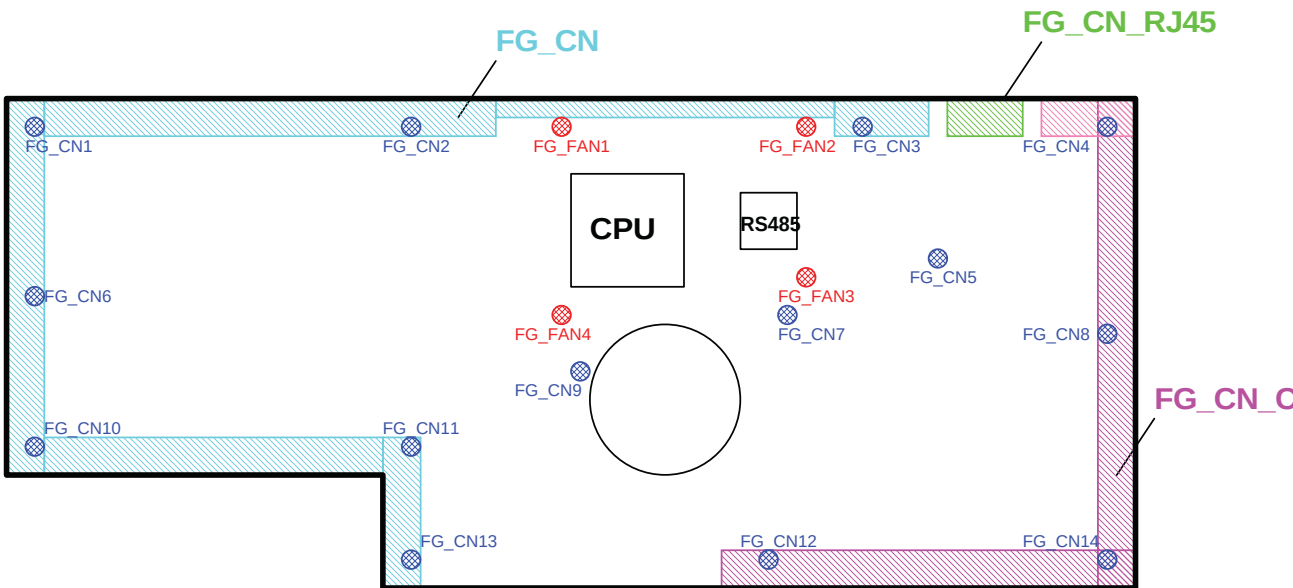
BENN(M10)の近傍に配置

R-C for ESD

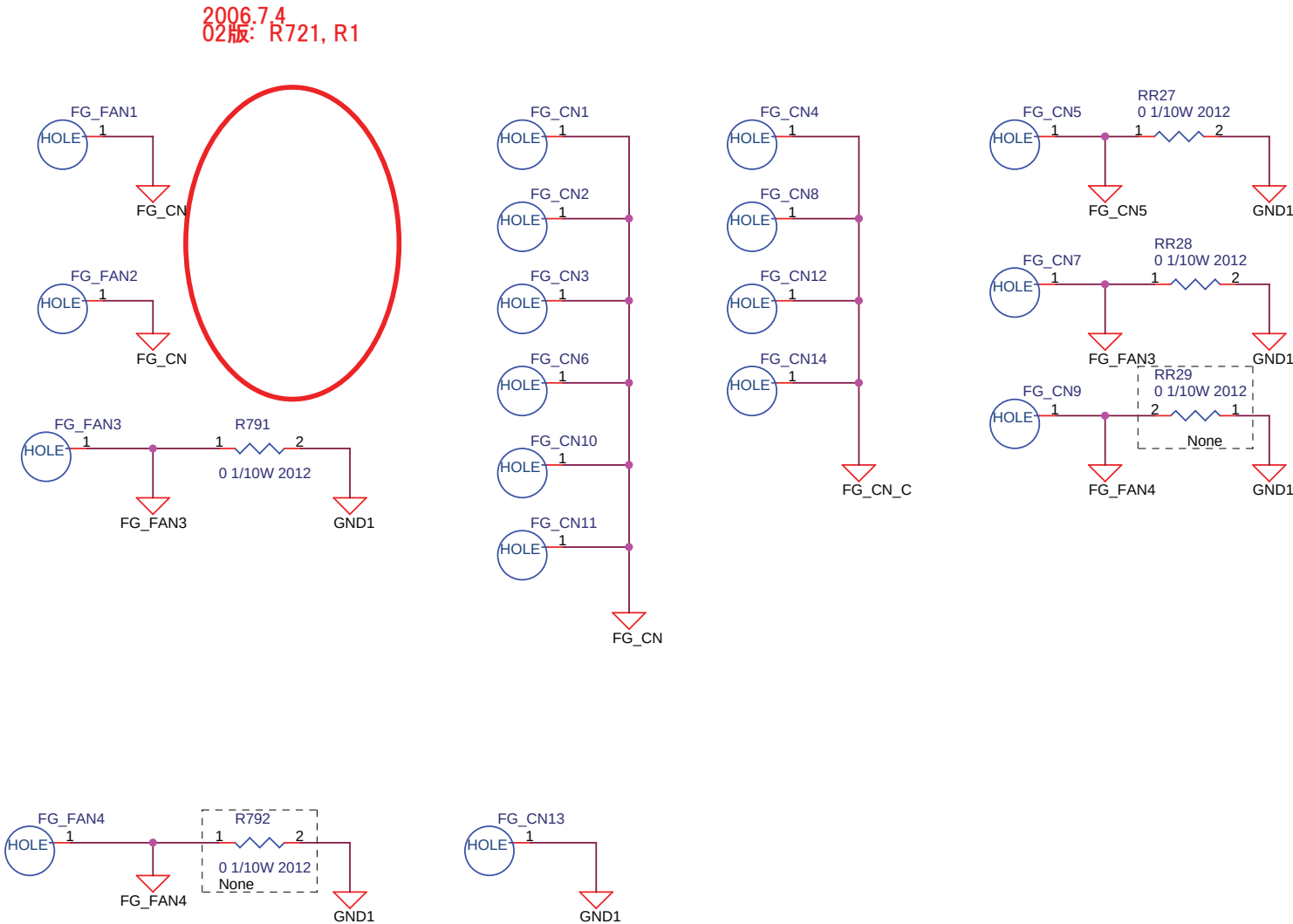
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						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		
Design	06/07/04	Mizukami	Check	Urita				
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						Appr. Hasegawa		

EMC対策

基板外周はFGグランド「FG_CN」、「FG_CN_C」、「FG_CN_RJ45」としてGND1から分離する。



このFG_CNについては、全層で可能な限り接続する。
FG_CNとGND1とは1mmのギャップを取る。
また、FG_CNについては信号線のGNDガードには使用せず、
その他信号についてもFG_CNから1.5mm以上離して配線すること。
(通す場合は相談すること。信号の種類によって判断する。)



FG-CN

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$\frac{1}{2} \times \frac{1}{2} = \frac{1}{4}$ $\frac{1}{4} \times \frac{1}{4} = \frac{1}{16}$ $\frac{1}{16} \times \frac{1}{16} = \frac{1}{256}$ $\frac{1}{256} \times \frac{1}{256} = \frac{1}{65,536}$ $\frac{1}{65,536} \times \frac{1}{65,536} = \frac{1}{4,294,967,296}$ $\frac{1}{4,294,967,296} \times \frac{1}{4,294,967,296} = \frac{1}{18,446,744,073,709,551,616}$	$\frac{1}{2} \times \frac{1}{2} = \frac{1}{4}$ $\frac{1}{4} \times \frac{1}{4} = \frac{1}{16}$ $\frac{1}{16} \times \frac{1}{16} = \frac{1}{256}$ $\frac{1}{256} \times \frac{1}{256} = \frac{1}{65,536}$ $\frac{1}{65,536} \times \frac{1}{65,536} = \frac{1}{4,294,967,296}$ $\frac{1}{4,294,967,296} \times \frac{1}{4,294,967,296} = \frac{1}{18,446,744,073,709,551,616}$
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A

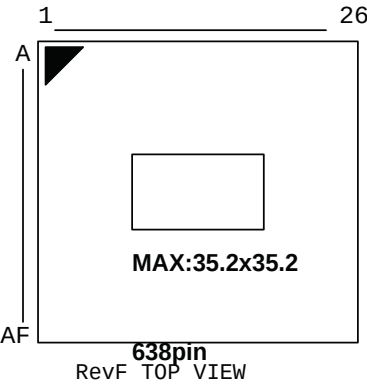
C1508-C1515は、電源Pin1pinについてひとつずつ配置すること。

G

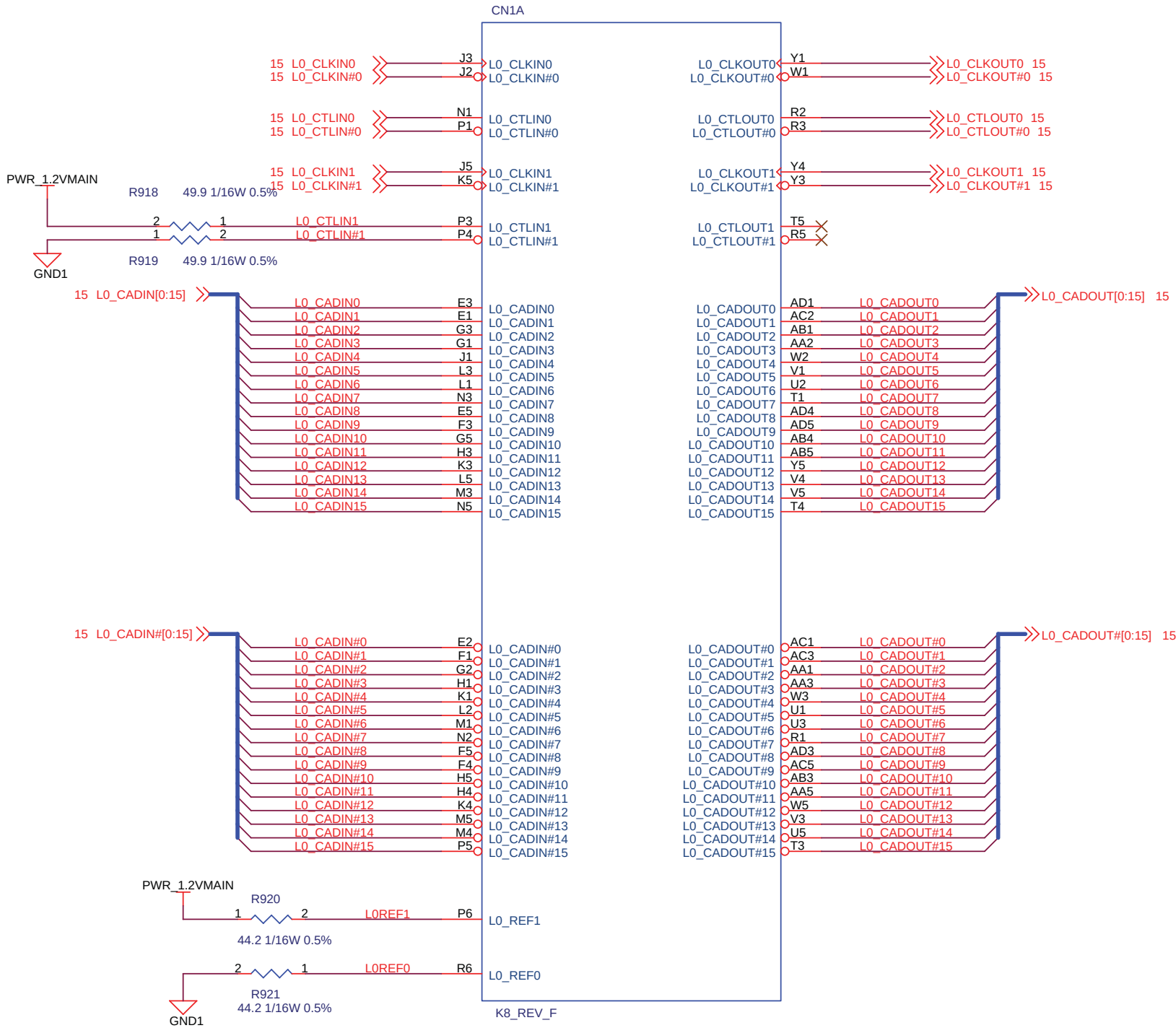
PLL

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L0REF0,L0REF1は0.127mmの線幅にて配線し、
他の信号から0.254mm以上離すこと。
R920,R921は25.4mm以内に配置すること。

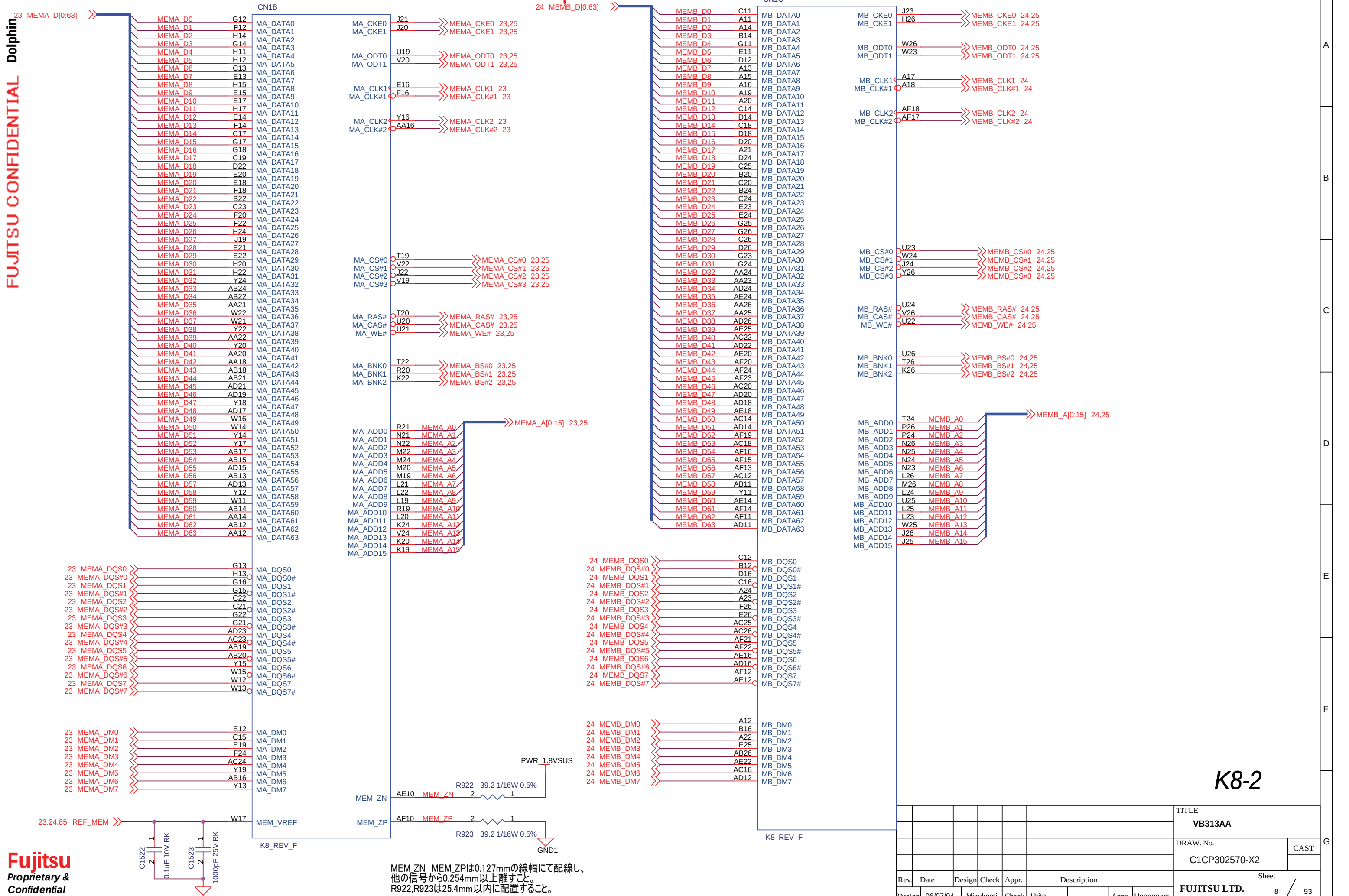
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K8-1

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Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	

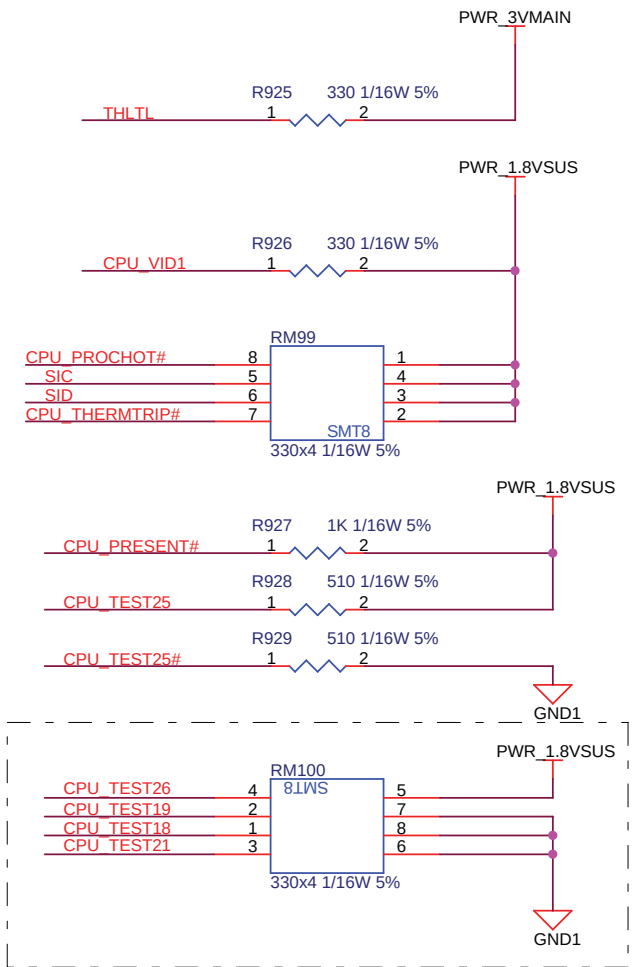
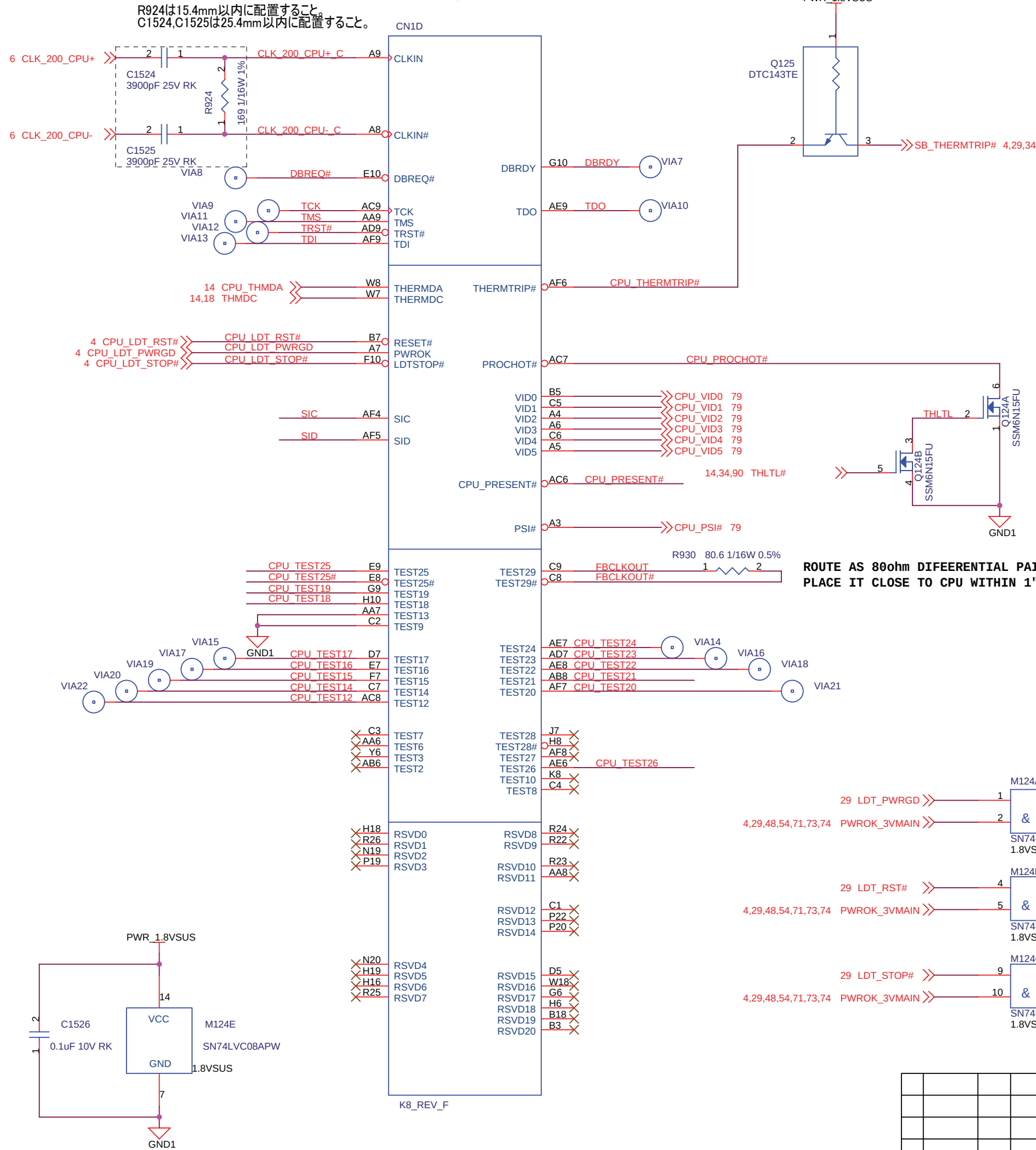
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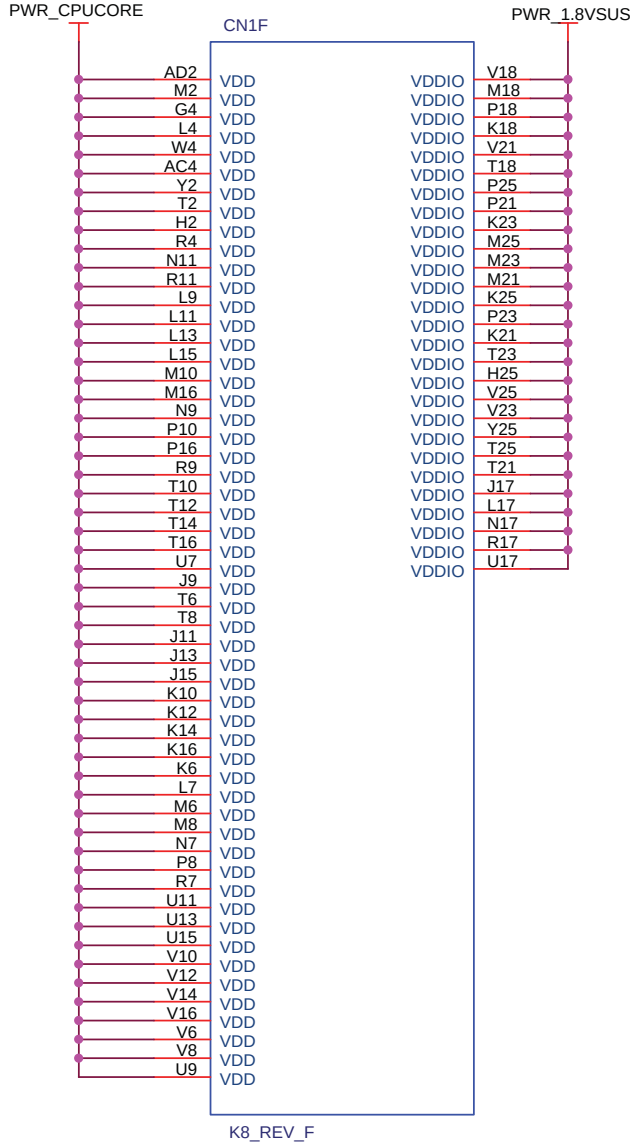
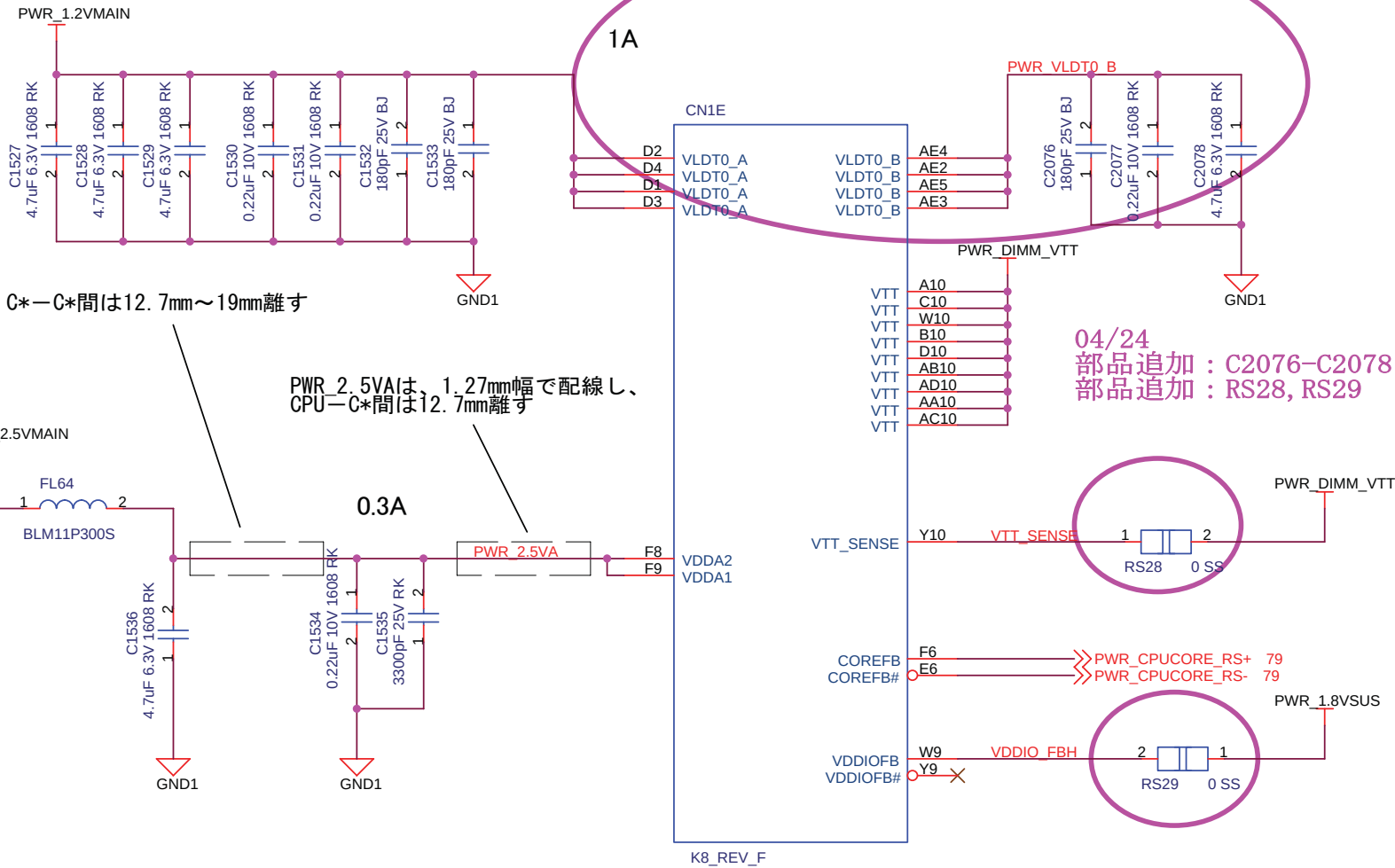
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Rev.	Date	Design	Check	Appr.	Description			Sheet 8 / 93
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Revision Guide Errata
Number133適用

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Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	9 / 93

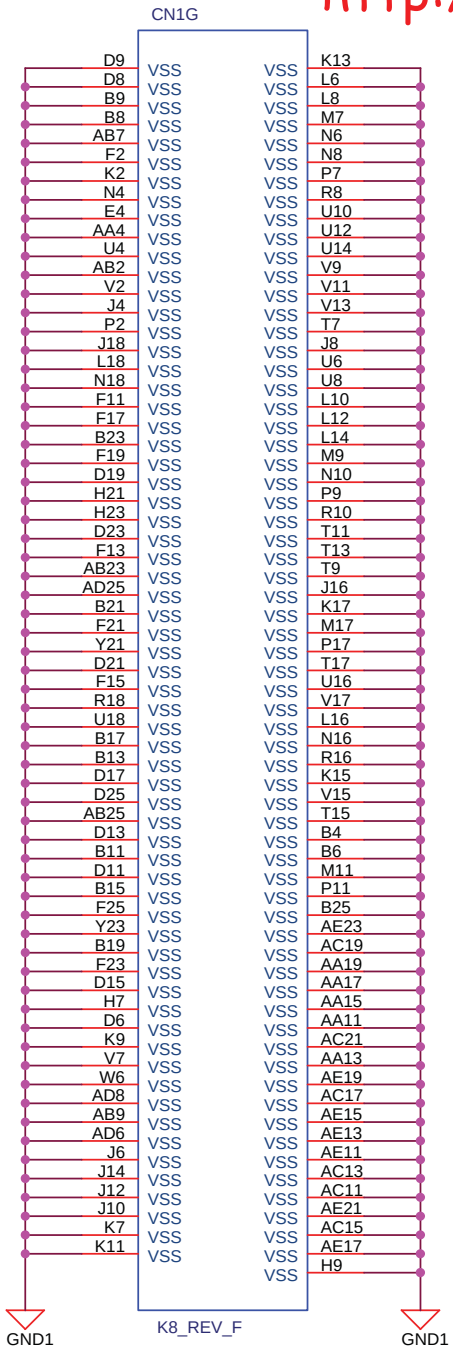


04/24
部品追加 : C2076-C2078
部品追加 : RS28, RS29

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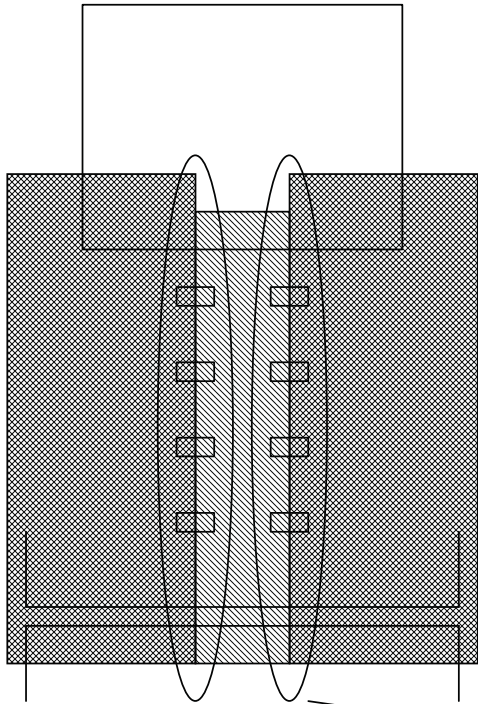
http://hobi-elektronika.net



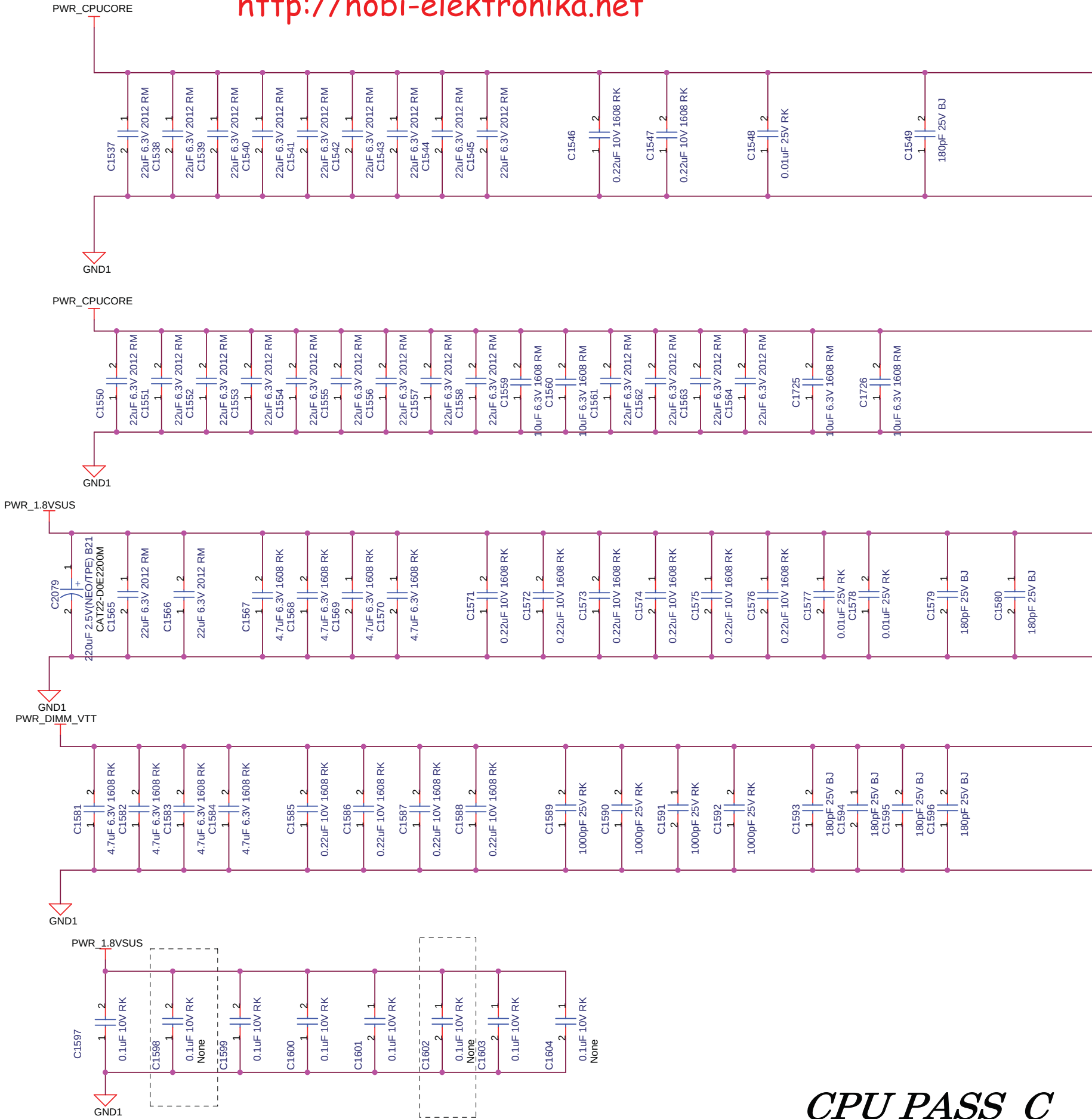
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K8-5

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Rev.	Date	Design	Check	Appr.	Description			Sheet
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これらのコンデンサC1597～C1604は、図のように
PWR_1.8VSUS, GND1のプレーンの間に
約1インチ間隔で配置すること。



K8_CPU

CPU PASS_C

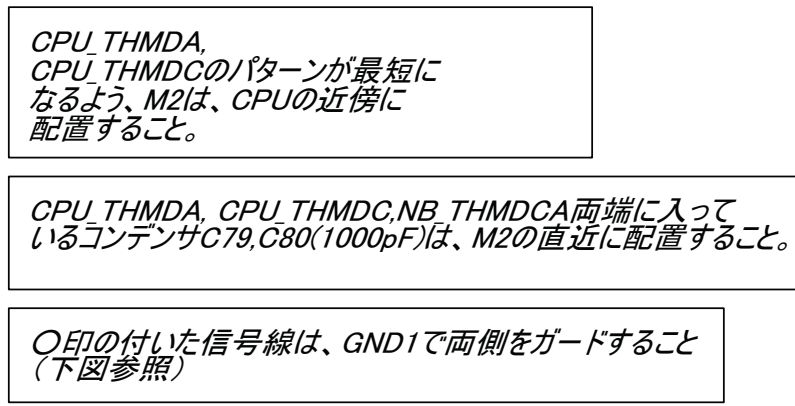
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Design	06/07/04	Mizukami	Check	Urita				
						Sheet		12 / 93

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A		http://hobi-elektronika.net														A	
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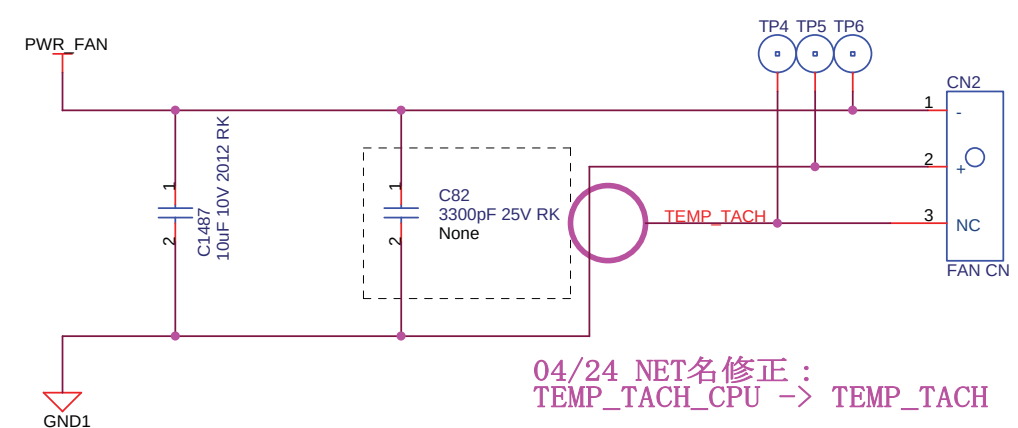
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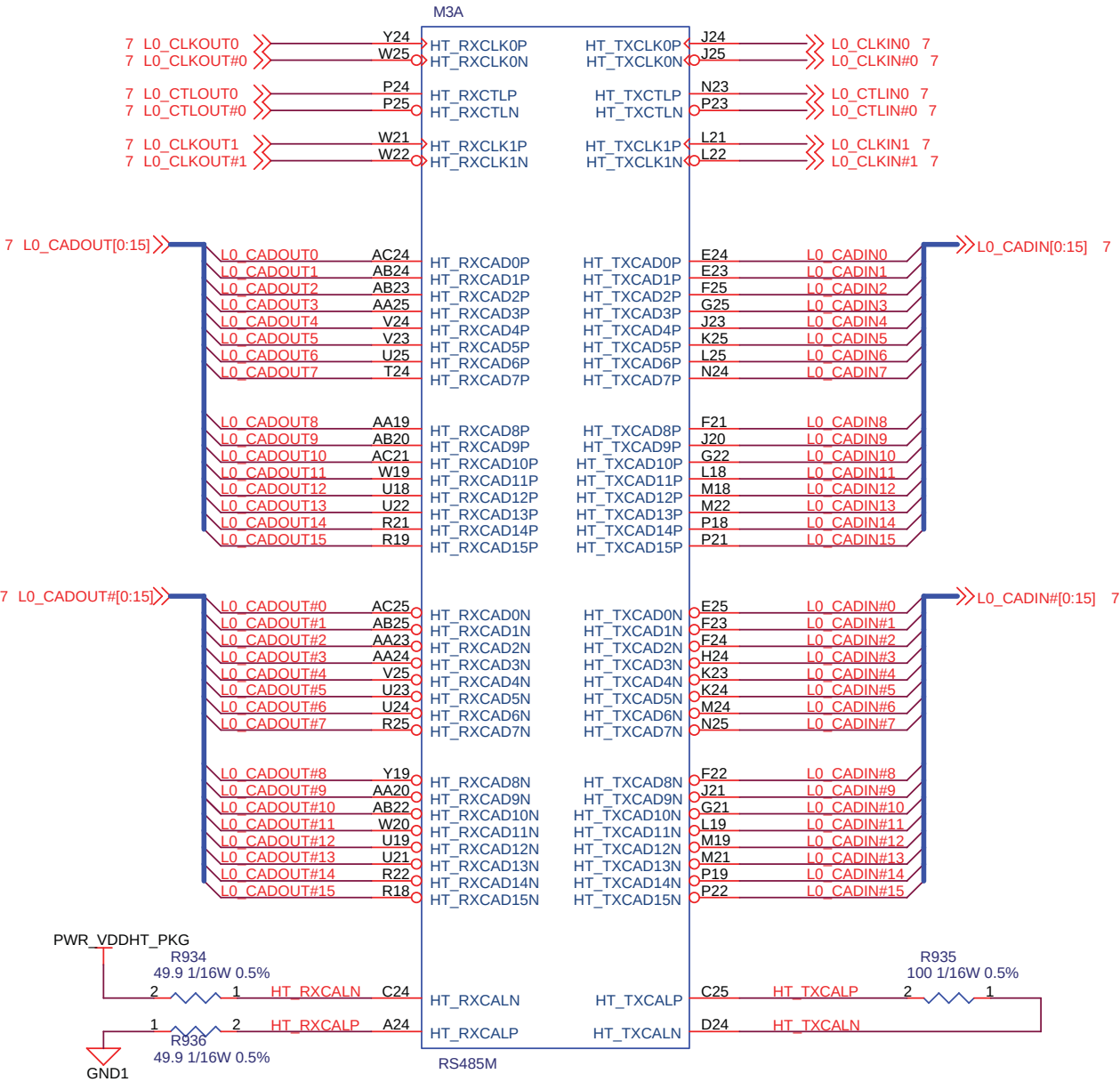
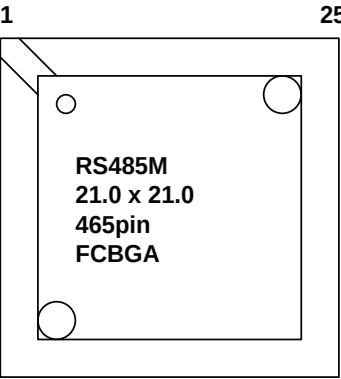
MAX6640
SMBAddress:01011110[5E固定]

The schematic diagram illustrates the PWR_FAN control circuit. It features a PWR_5VSTD supply connected to a network of resistors (R871, R872, R875, R876, R877, R878, R879) and transistors (Q121, Q123, Q122). The PWR_FAN output is connected to the drain of Q121. The PWR_MASK input is connected to the base of Q123. The PWR_5VMAIN supply is connected to the emitter of Q122. The PWMOUT output is connected to the collector of Q122. The circuit is connected to GND1 and includes a THERM_OVRIDE# input and a PWR_MASK input.



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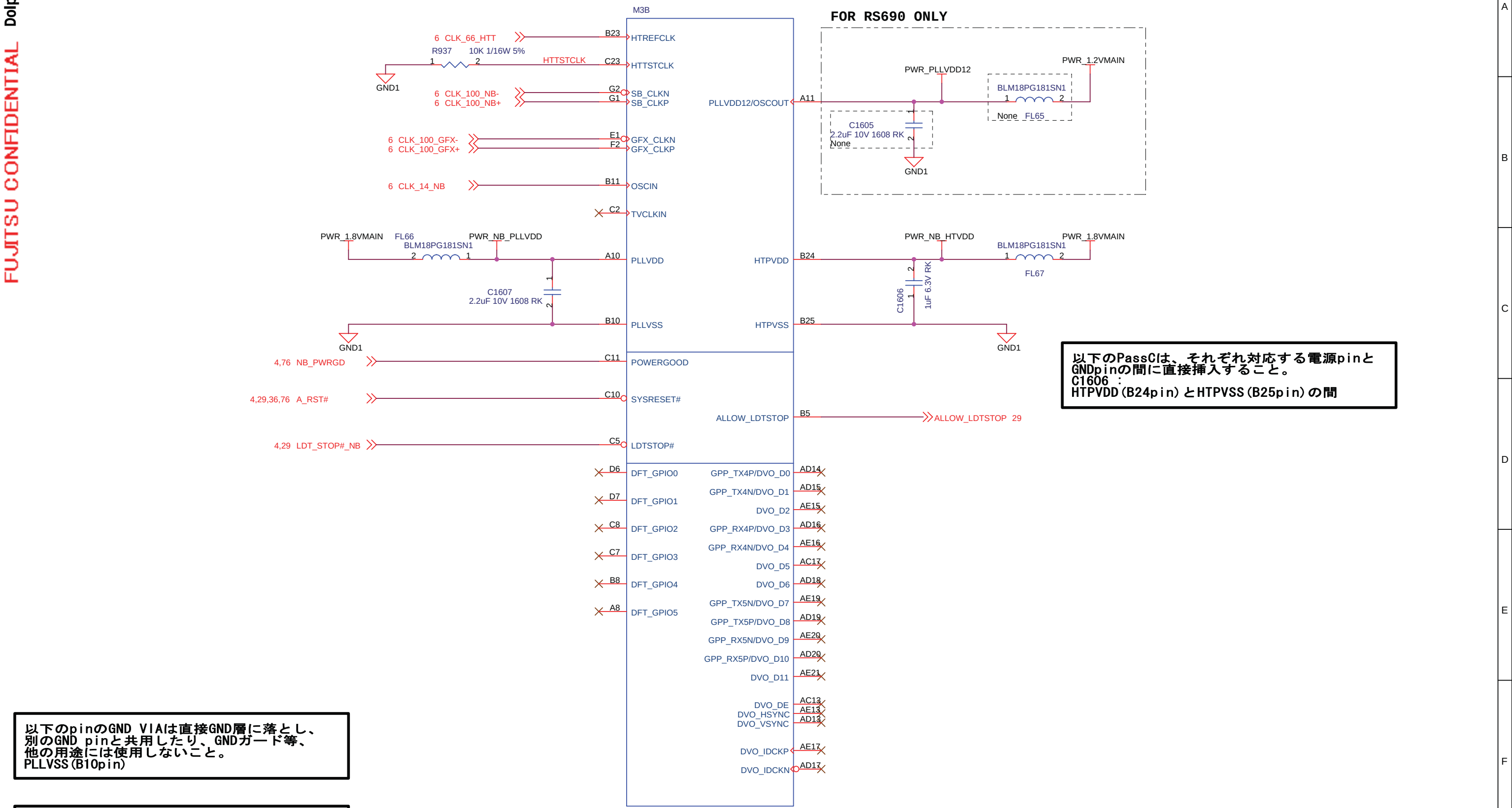


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以下のpinのGND VIAは直接GND層に落とし、別のGND pinと共用したり、GNDガード等、他の用途には使用しないこと。
PLLVSS (B10pin)

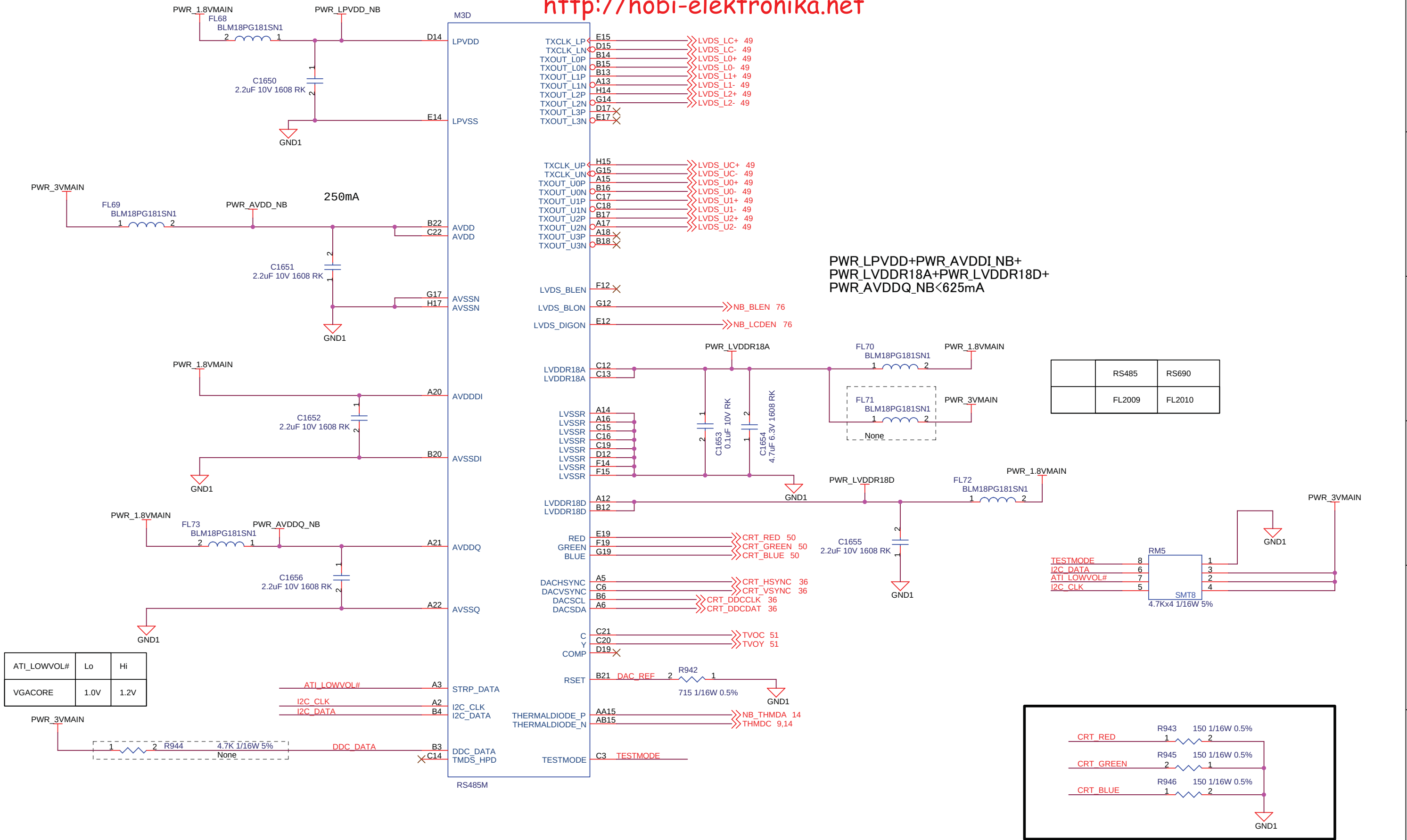
以下のPassCは、それぞれ対応する電源pinとGNDpinの間に直接挿入すること。
C1607 : PLLVDD (A10pin) とPLLVSS (B10pin) の間

以下のPassCは、それぞれ対応する電源pinとGNDpinの間に直接挿入すること。
C1606 : HTPVDD (B24pin) とHTPVSS (B25pin) の間

						TITLE		
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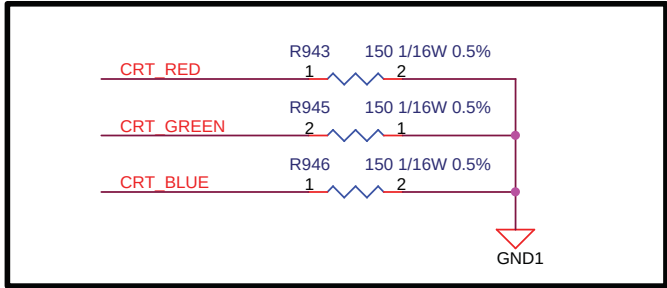
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ATI_LOWVOL#	Lo	Hi
VGACORE	1.0V	1.2V

	RS485	RS690
	FL2009	FL2010

TESTMODE	8	1
I2C_DATA	6	3
ATI_LOWVOL#	7	2
I2C_CLK	5	4



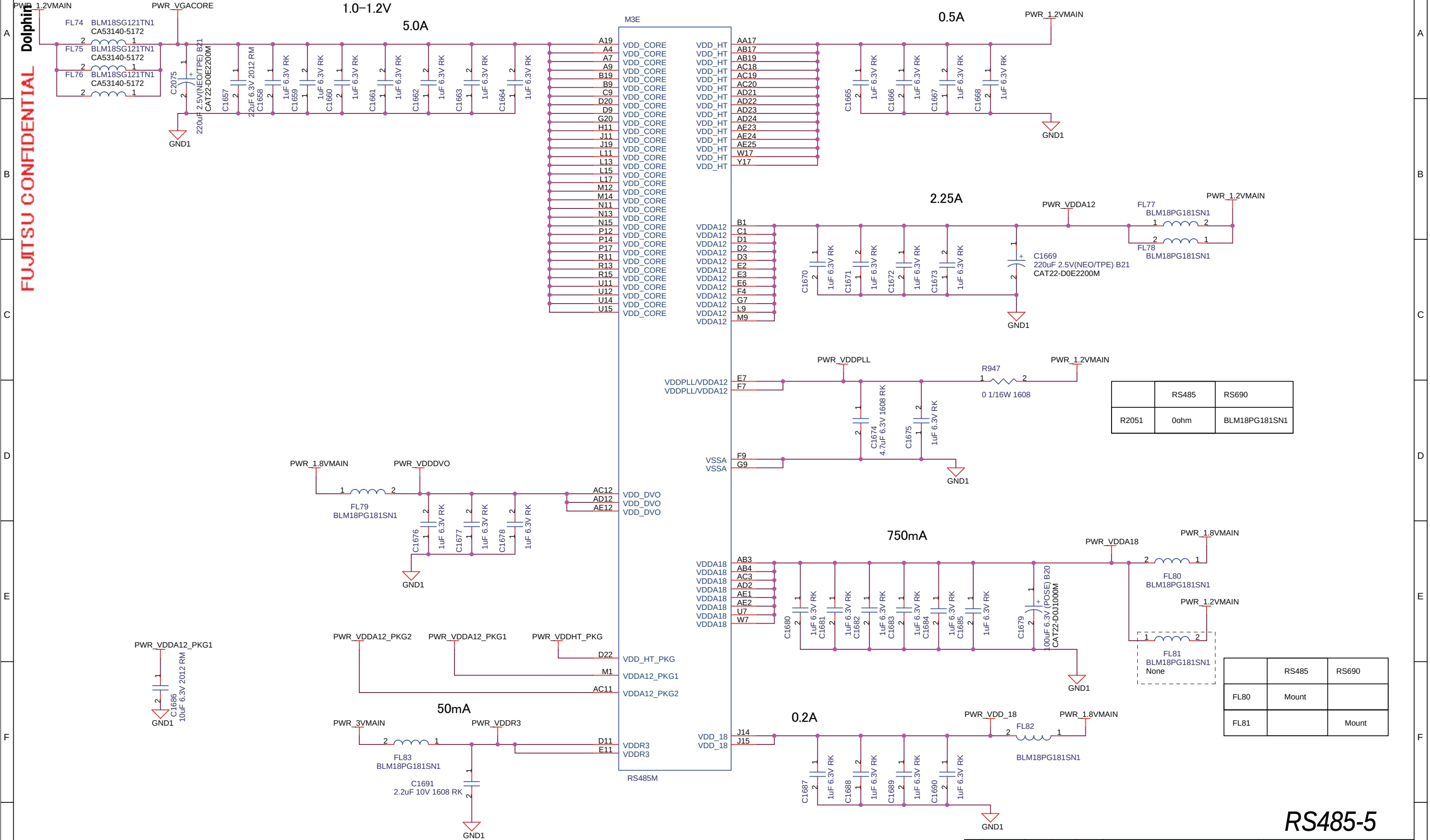
以下のpinのGND VIAは直接GND層に落とし、別のGND pinと共用したり、GNDガード等、他の用途には使用しないこと。
LPVSS(E14pin)
LVSSR(A14,A16,C15,C16,C19,D12,F14,F15pin)
AVSSN(G17,H17pin)
AVSSDI(B20pin)
AVSSQ(A22pin)

以下のPassCは、それぞれ対応する電源pinとGNDpinの間に直接挿入すること。
C1650 : LPVDD(D14pin)とLPVSS(E14pin)の間
C1653, C1654 : LVDDR18A(C12,C13pin)とLVSSR(A14,A16,C15,C16,C19,D12,F14,F15pin)の間
C1651 : AVDD(B22,C22pin)とAVSSN(G17,H17pin)の間
C1652 : AVDDI(A20pin)とAVSSDI(B20pin)の間
C1656 : AVDDQ(A21pin)とAVSSQ(A22pin)の間

R943,R945,R946は、M3(RS485M)の直近に配置すること

RS485-4

						TITLE		
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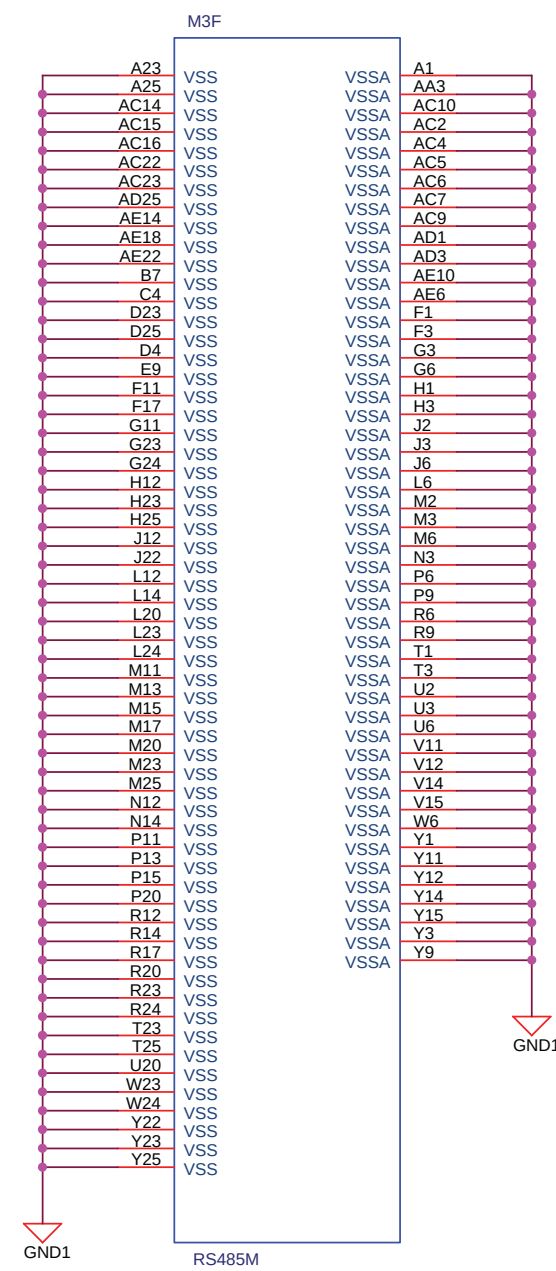


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RS485-5

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RS485-6

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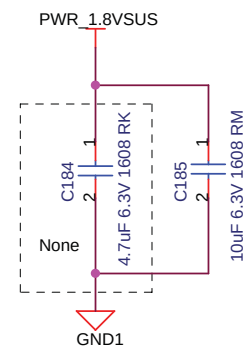
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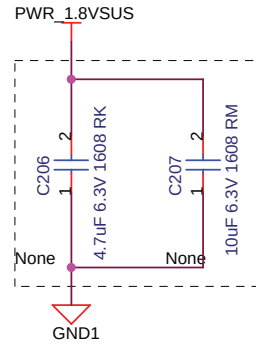
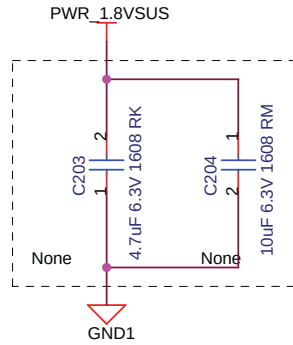
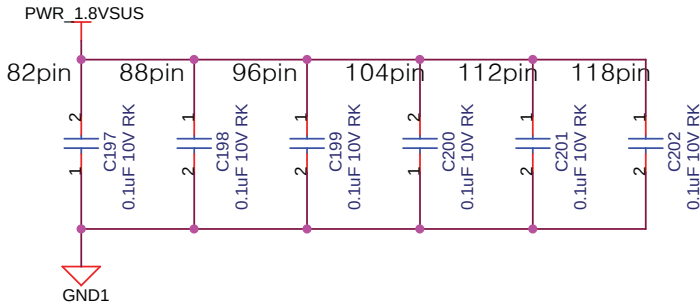
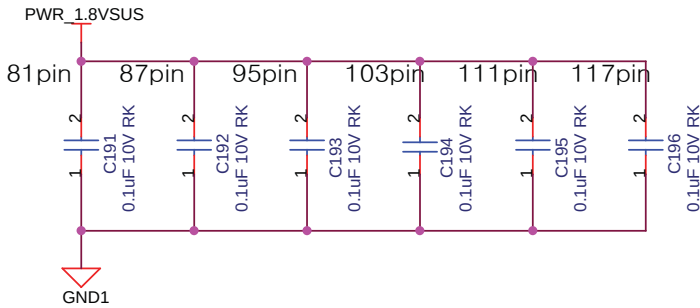
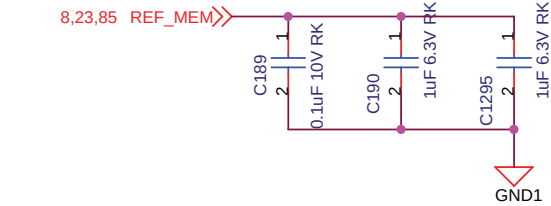
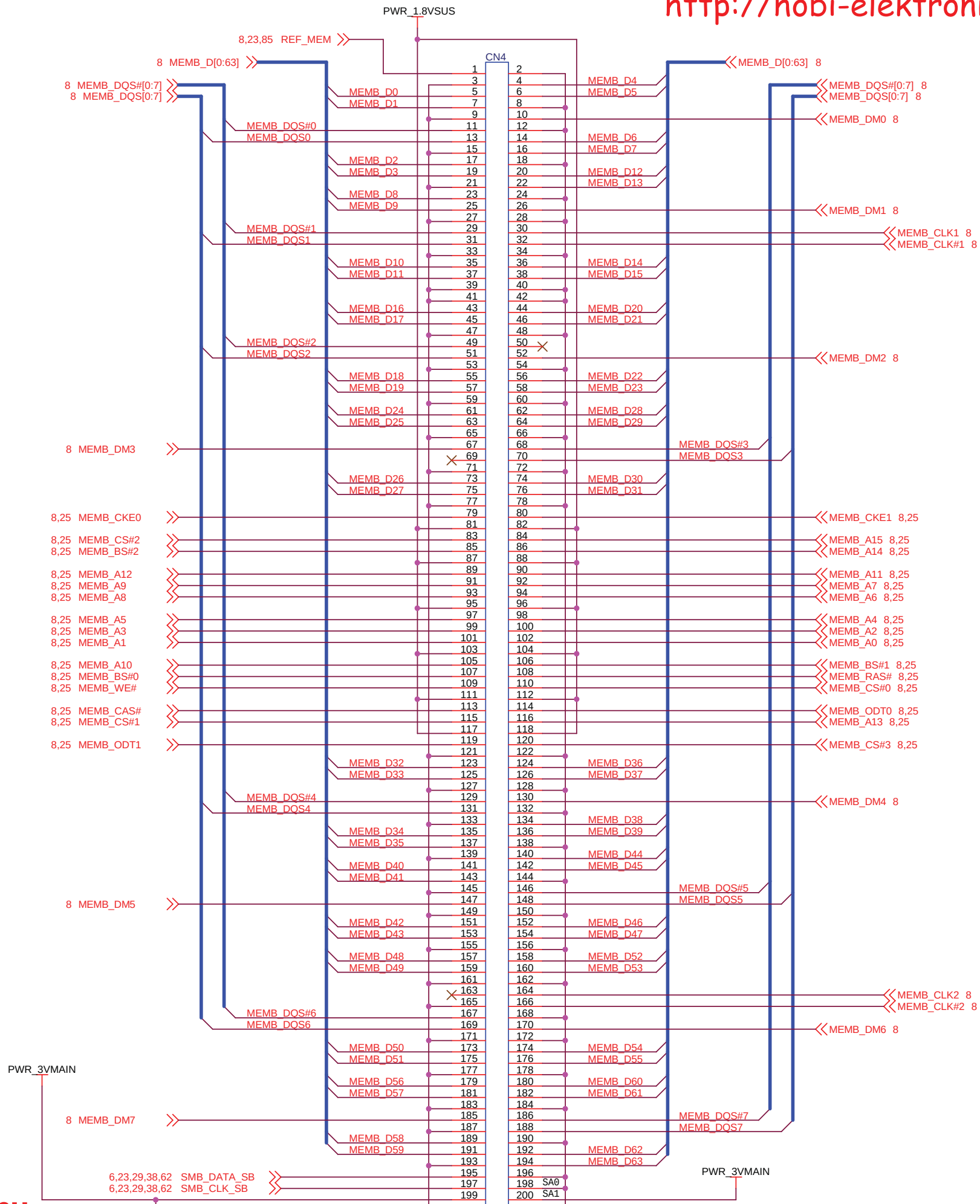
Dolphin



Memory Slot1

									TITLE		G
									VB313AA		
									DRAW. No.		
									C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.		Sheet 23 / 93
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa			



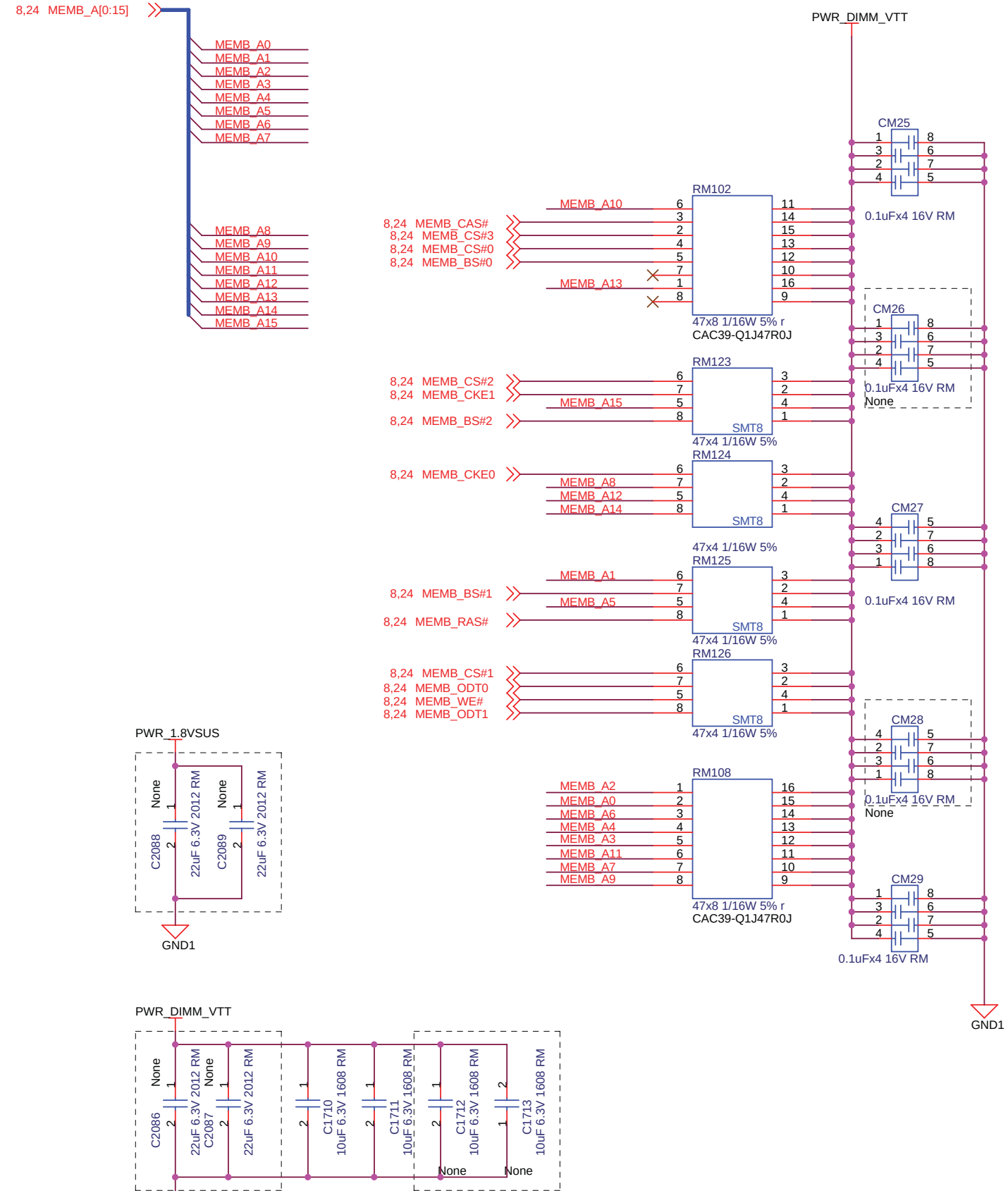
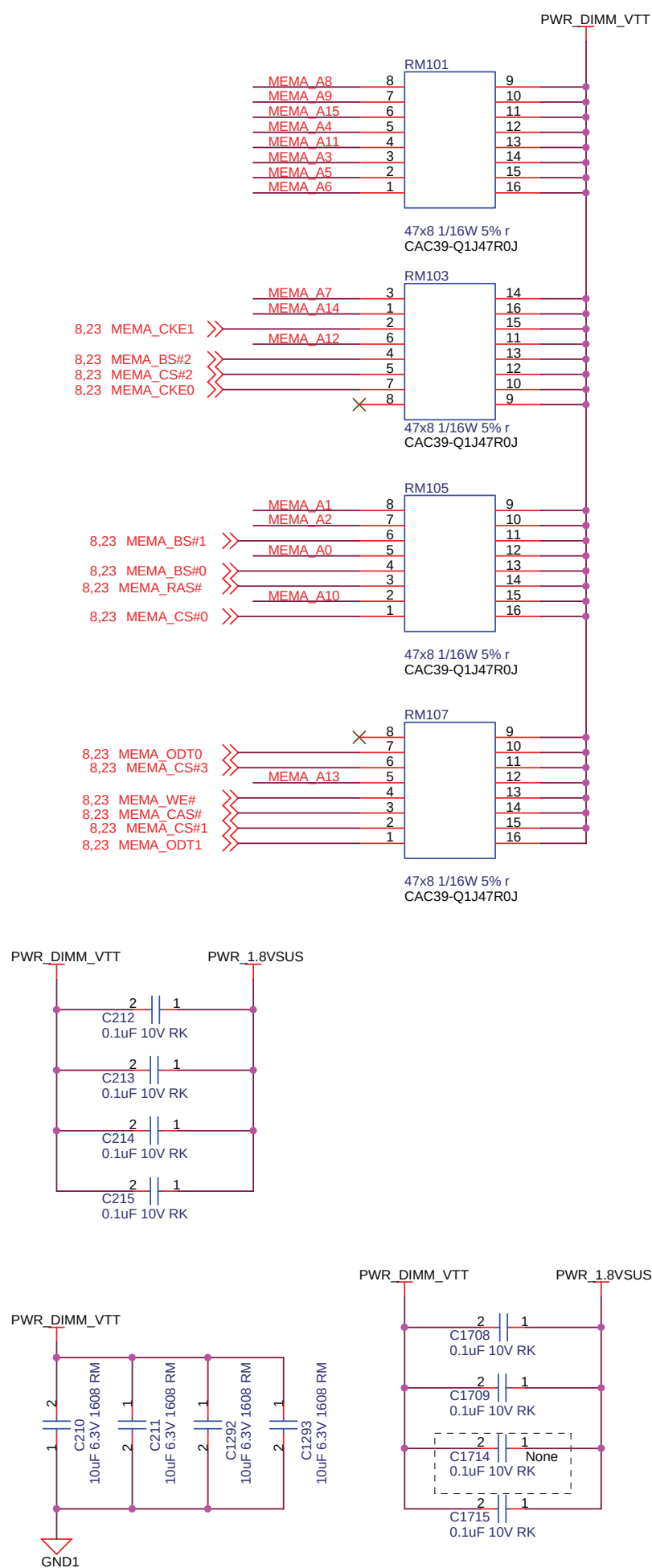


Memory Slot2

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						VB313AA		
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Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		
Design	06/07/04	Mizukami	Check	Urita				
						Sheet		
						24 / 93		

FGにはGND1を接続すること。
Connect FG to GND1

Fujitsu
Proprietary & Confidential

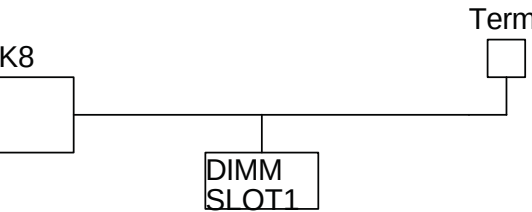


Memory Termination

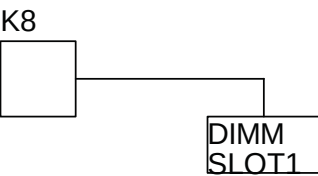
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						DRAW. No.			CAST	
						C1CP302570-X2				
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa			25 / 93

Channel A

DIMM Address/Command Topology

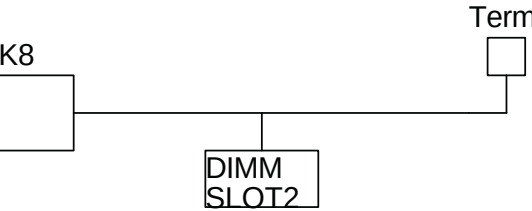


DIMM Data Bus Topology

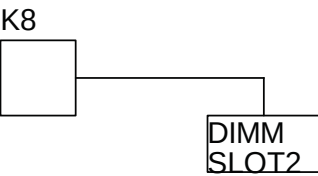


Channel B

DIMM Address/Command Topology



DIMM Data Bus Topology



Topology

						TITLE		
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						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD. 26 / 93

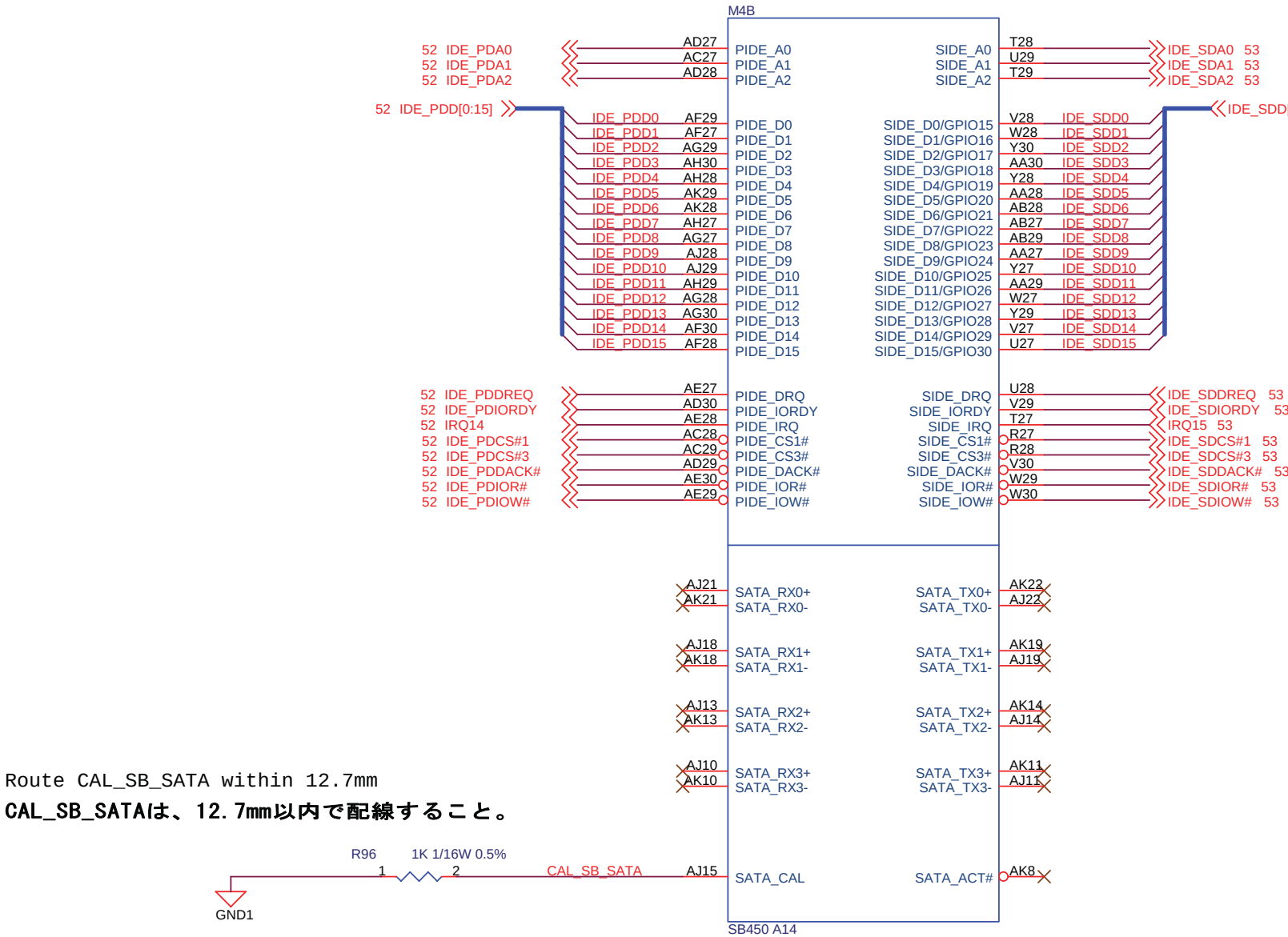


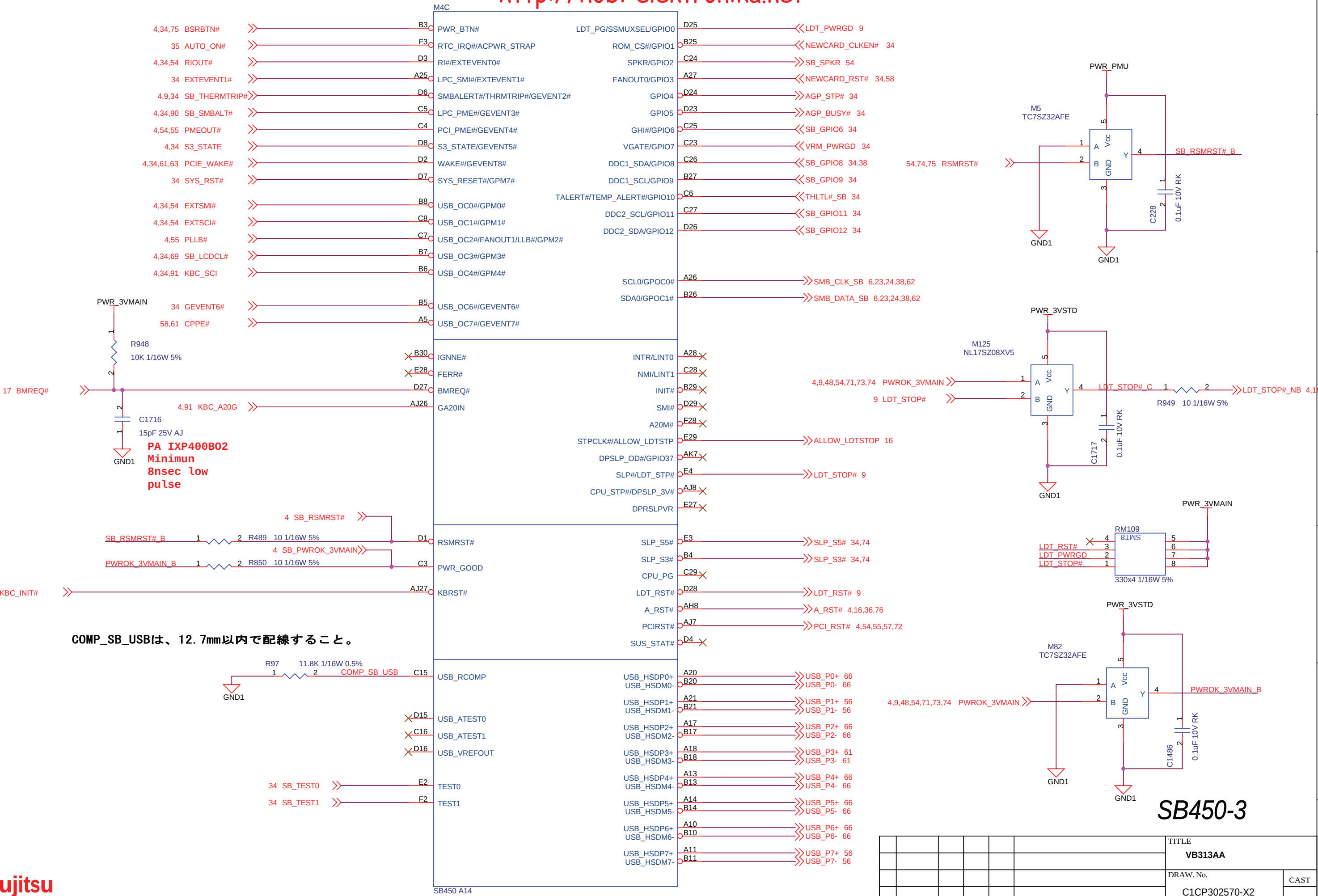
FUJITSU CONFIDENTIAL

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FUJITSU CONFIDENTIAL

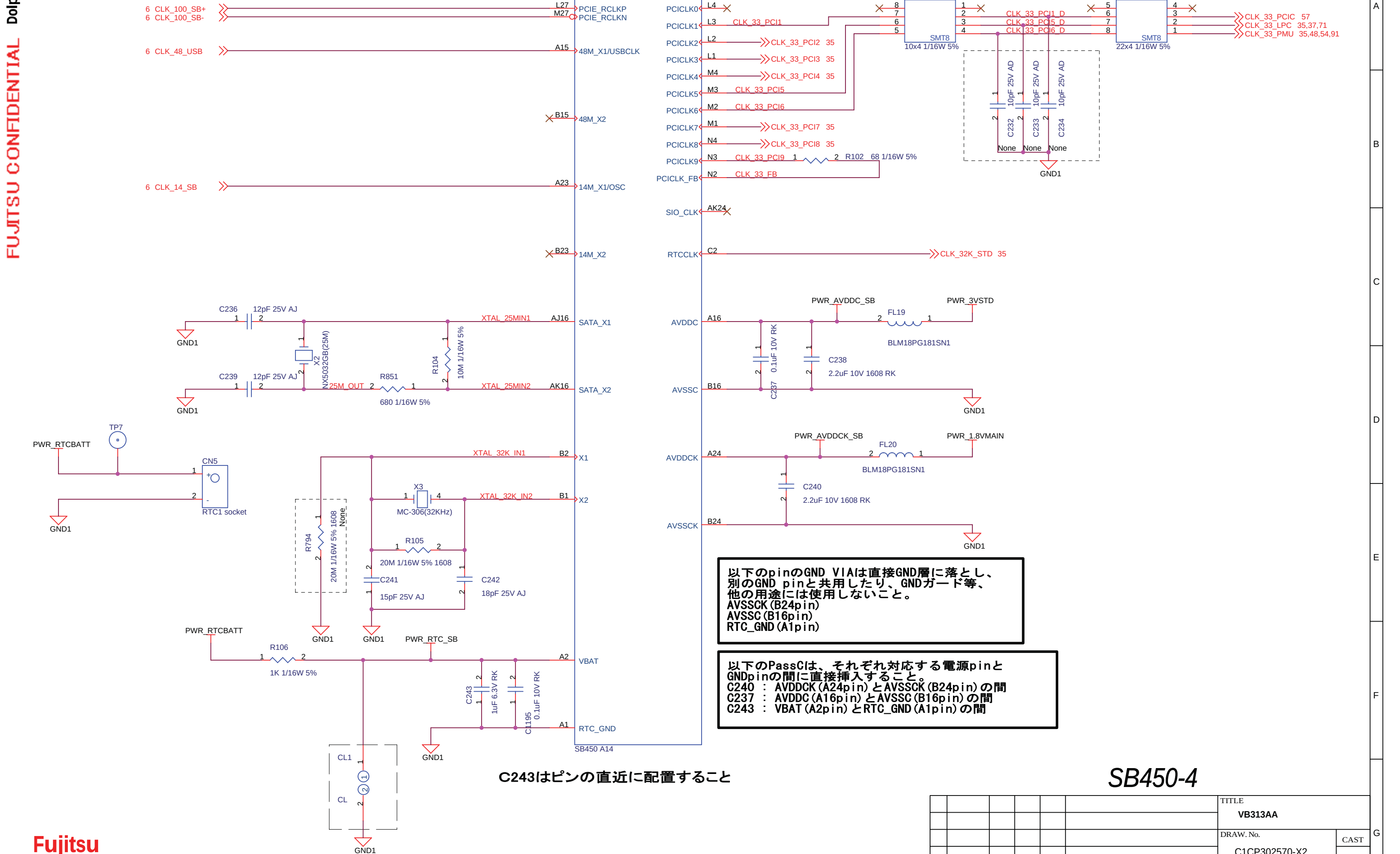




COMP_SB_USBは、12.7mm以内で配線すること。

SB450-3

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						VB313AA		
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						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	Sheet		
Design	06/07/04	Mizukami	Check	Urita		Fujitsu LTD.		29 / 93



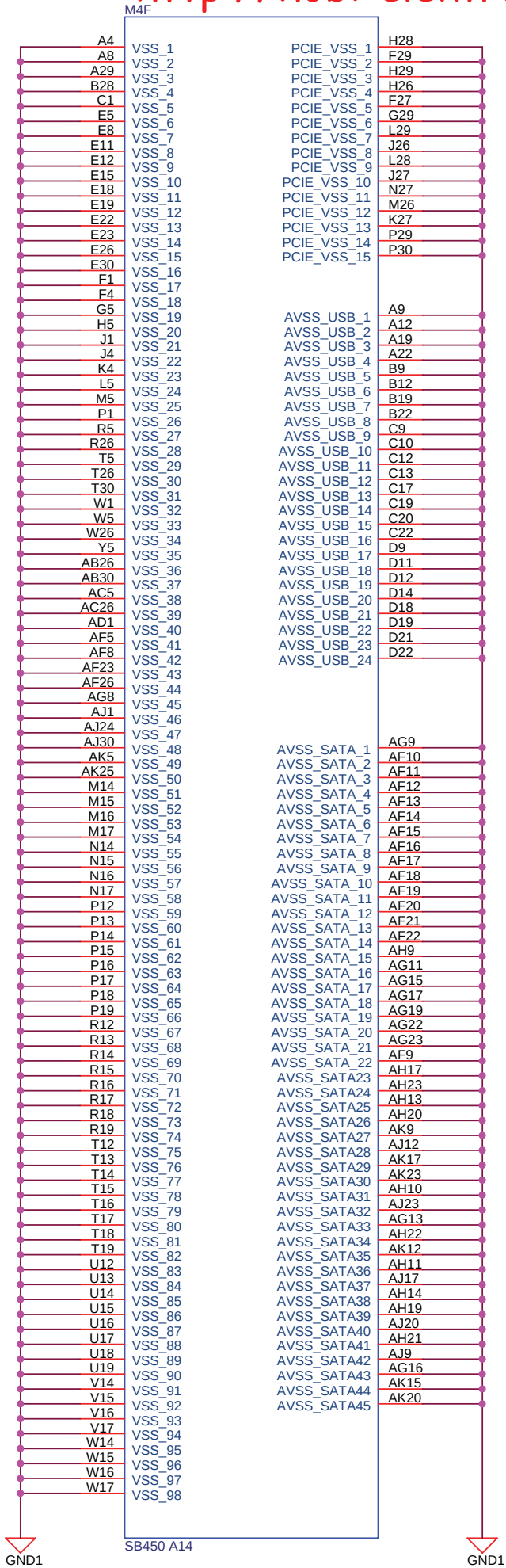
C243はピンの直近に配置すること

SB450-4

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Rev.	Date	Design	Check	Appr.	Description	Sheet		
Design	06/07/04	Mizukami	Check	Urita		Fujitsu LTD.		30 / 93

Dolphin
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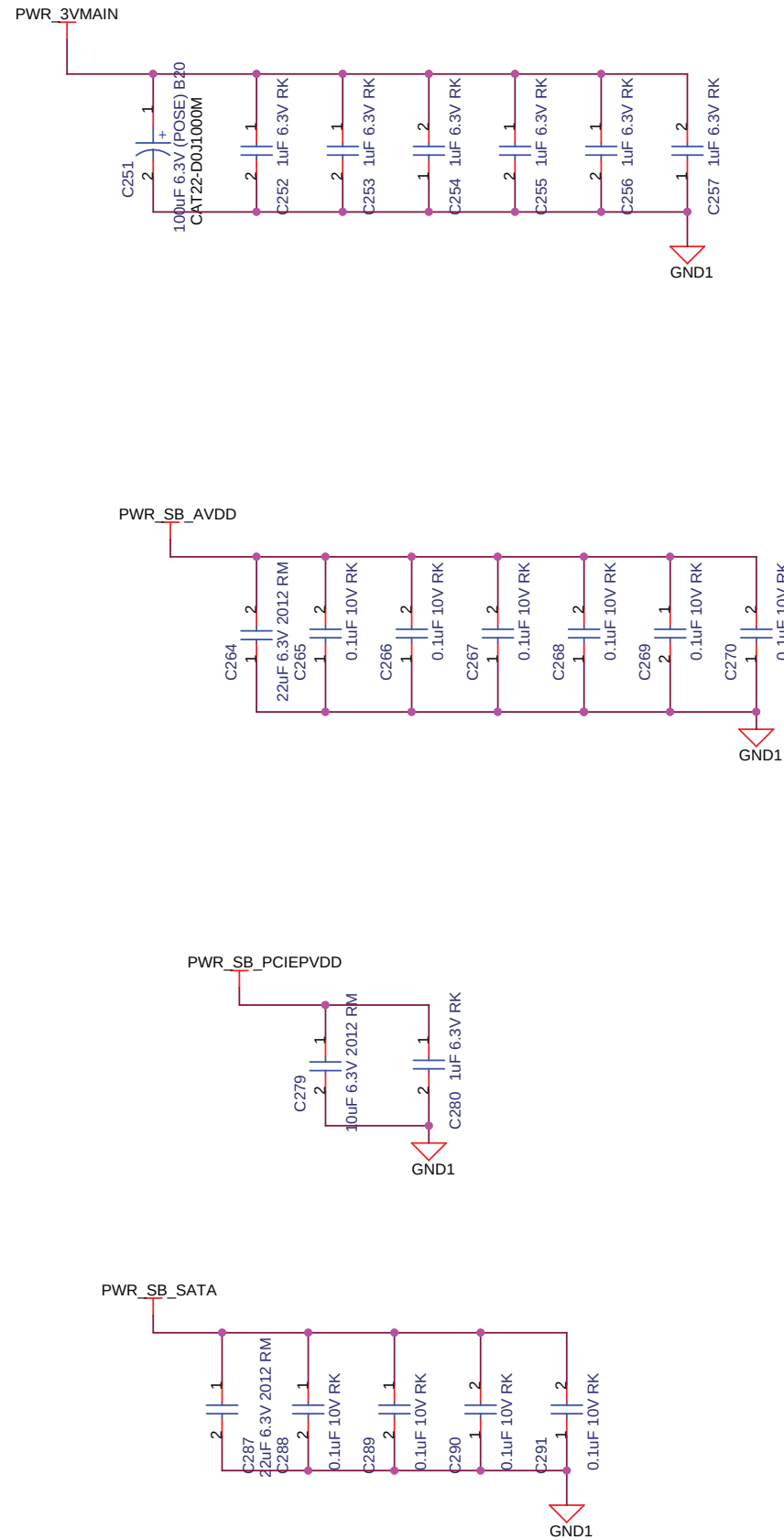
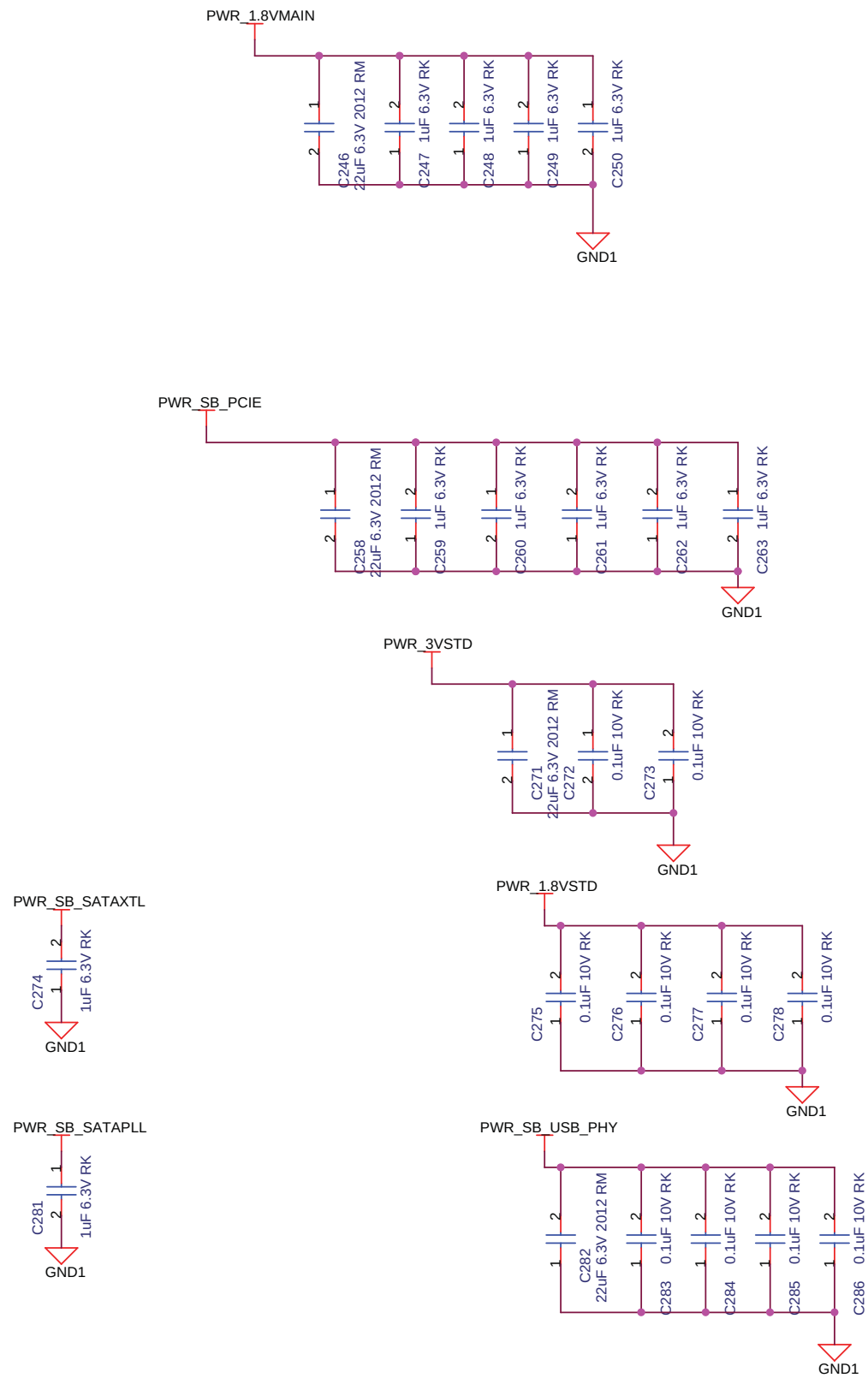


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Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD. 32 / 93

これらのパソコンはSB450近傍、可能な限りピンの直近に配置願います

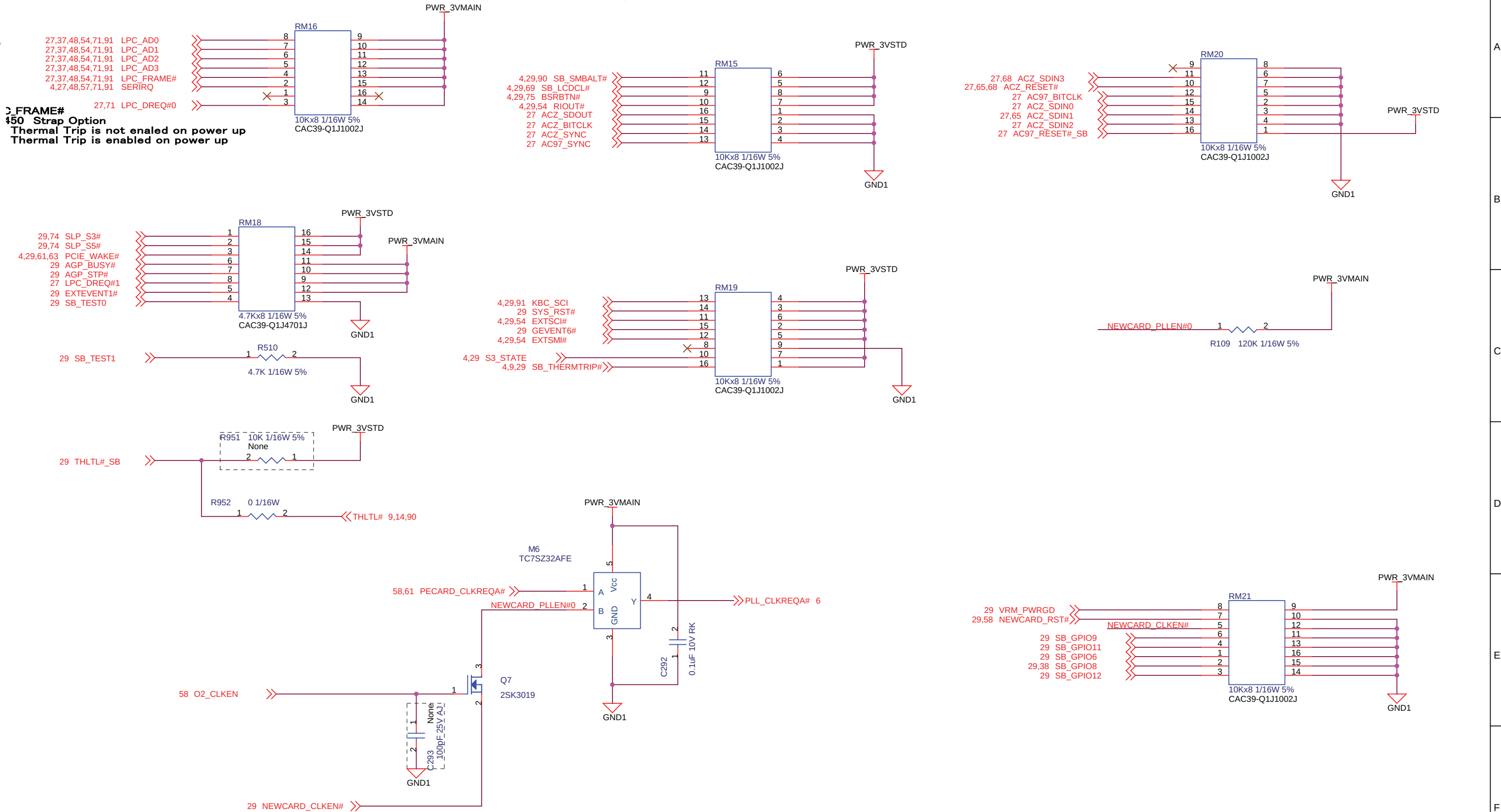
SB450-7

									TITLE VB313AA	
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Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet 33 / 93
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa		



FUJITSU CONFIDENTIAL

Dolphin



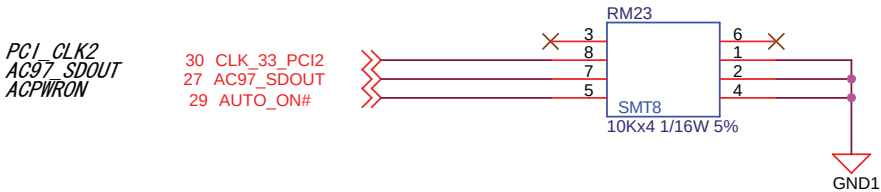
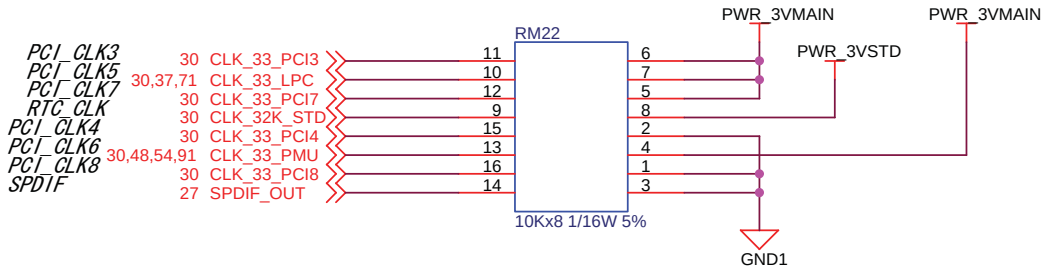
04/28
部品削除 : R494, R495, R787, R788

SB450
Pull Up/Down

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									TITLE
									VB313AA
									DRAW. No.
									C1CP302570-X2
									CAST
Rev.	Date	Design	Check	Appr.	Description			Sheet	
Design	06/07/04	Mizukami	Check	Urita			Appr. Hasegawa	34 / 93	FUJITSU LTD.

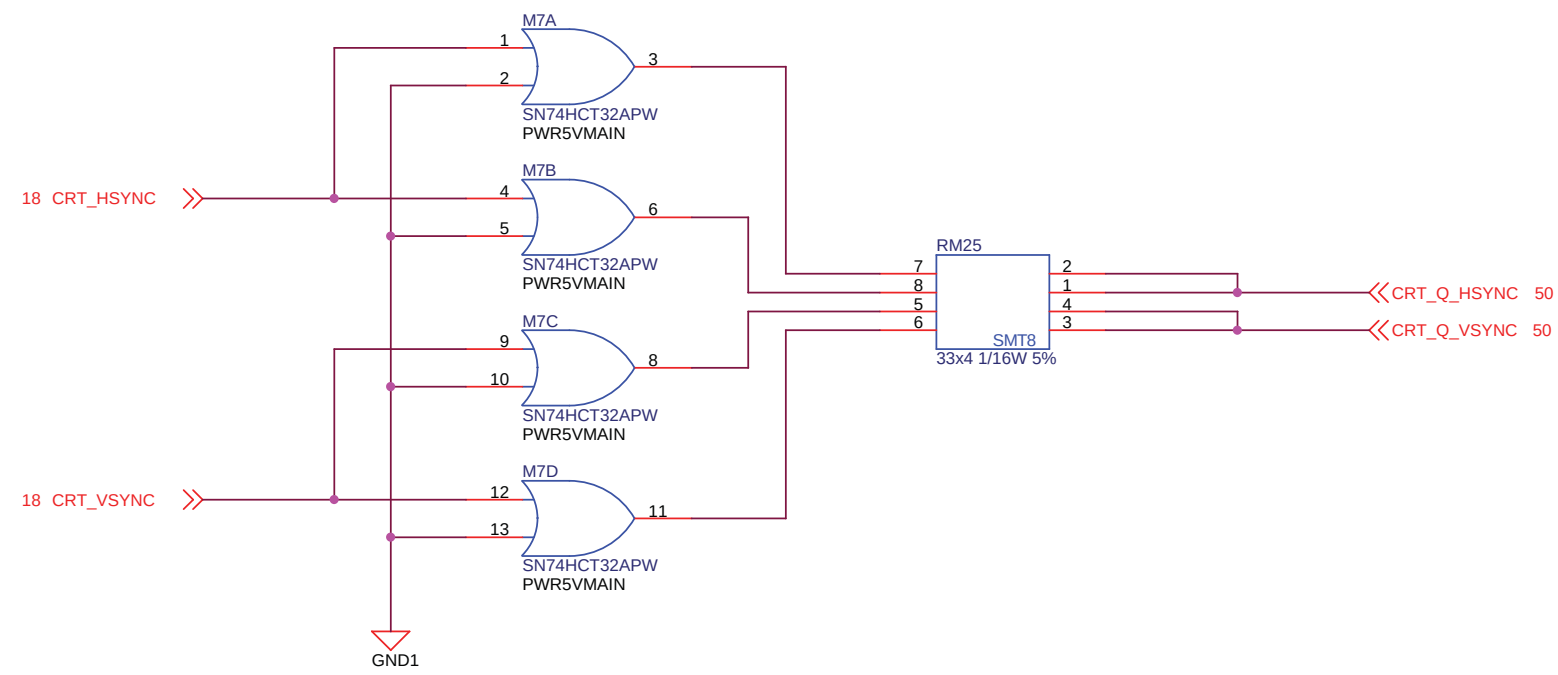
FUJITSU CONFIDENTIAL Dolphin



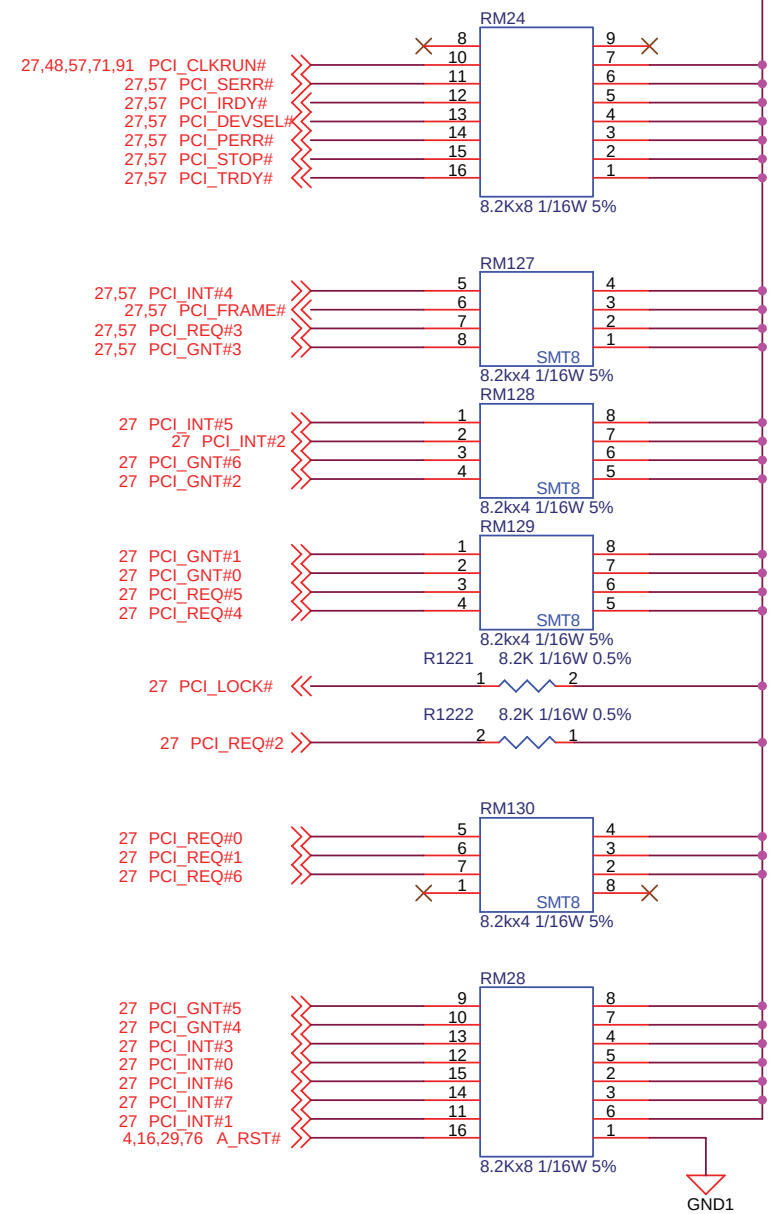
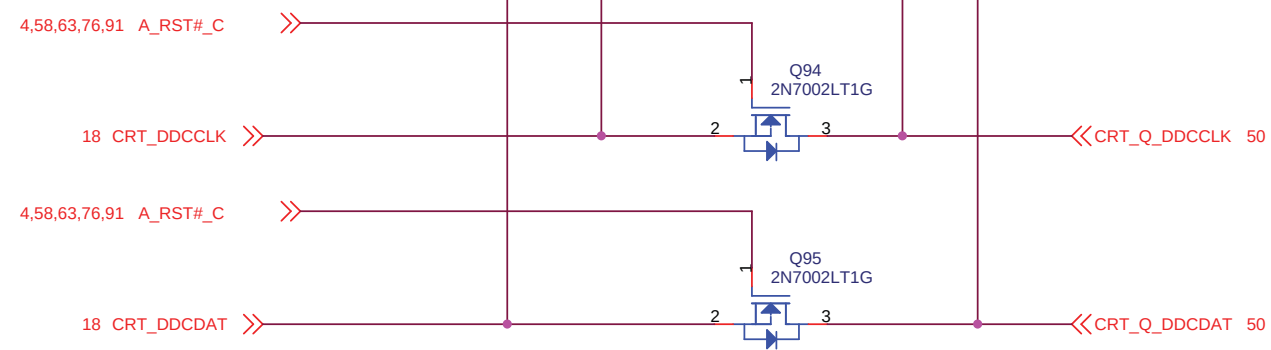
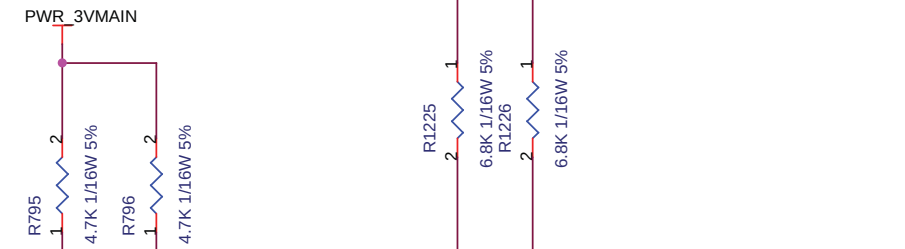
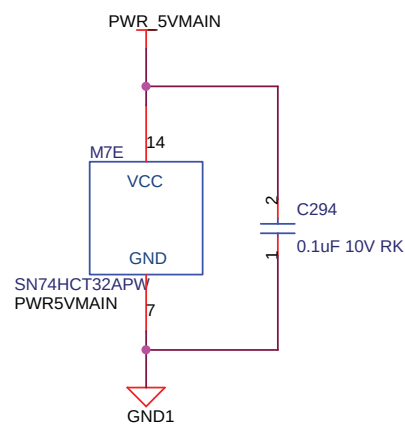
Pin Name	Description					Post-Beira Setting
ACPWRON	Active Manual Power On. 0 : Automatic Power On 1 : Manual Power On					0
AC97SDOUT	Enable/Disable additional straps for Debugging. 0 : Use Hardcoded defaults for Debug straps 1 : Enable additional Debug Strap					0
SPDIF	Select Speed for Super I/O. 0 : SIO Speed is 48MHz 1 : SIO Speed is 24MHz					0
PCICLK7 PCICLK8	ROM Type Select					1
	PCICLK7	1	1	0	0	
	PCICLK8	0	1	0	1	0
		ROM Type	LPC ROM (256K)	BIOS ROM (X-bus)	FWH	LPC ROM (512K/1M)
PCICLK6	Define Type of CPU 0 : Intel Processors 1 : AMD K8					1
PCICLK5	48MHz Clock Pad Select 0 : Ctystal Pad 1 : Clock Input Buffer					1
PCICLK4	Bypsd USB PLL 0 : use external 48MHz 1 : use internal USB					0
PCICLK3	USB PLL Down 0 : Enable 1 : Disable					1
PCICLK2	48MHz Clock Pad Select 0 : Clock Input Buffer 1 : Ctystal Pad					0
RTC_CLK	RTC Select 0 : External RTC 1 : Internal RTC					1
LFRAME#	Thermal Trip Strap 0 : Thermal Trip is not enabled on power up 1 : Thermal Trip is enabled on power up (default)					1

Pin Name	Description	
IDEPDack	Generate Short Reset 0 : Use Short Reset 1 : Use Long Reset	
PCI_AD31 PCI_AD30	Charge Pump control Bit	
PCI_AD29 PCI_AD28	PLL VCO control bits	
PCI_AD27	Bypass PCI PLL 0 : Use internal IDE PLL. Generated PCI CLK 1 : Bypass internal PCI PLL	
PCI_AD26	Bypass ACPI BCLK 0 : Use internal ACPI_BCLK 1 : Bypass ACPI_BCLK	
PCI_AD25	Bypass IDE Clock 0 : Use Internal IDE CLK 1 : Bypass Internal IDE	
PCI_AD24	BLK core strap from I2ROM enable 0 : Use default Value 1 : getting the value from I2C	
PCI_AD23	EPROM Reserved	

FUJITSU CONFIDENTIAL Dolphin



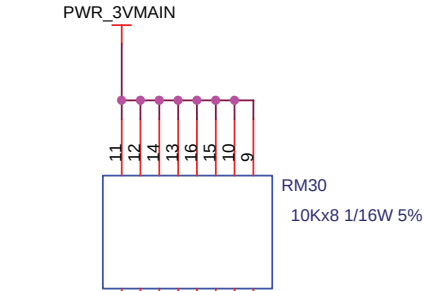
多連部品RM29については
配線しやすいようにピンスワップ可能。



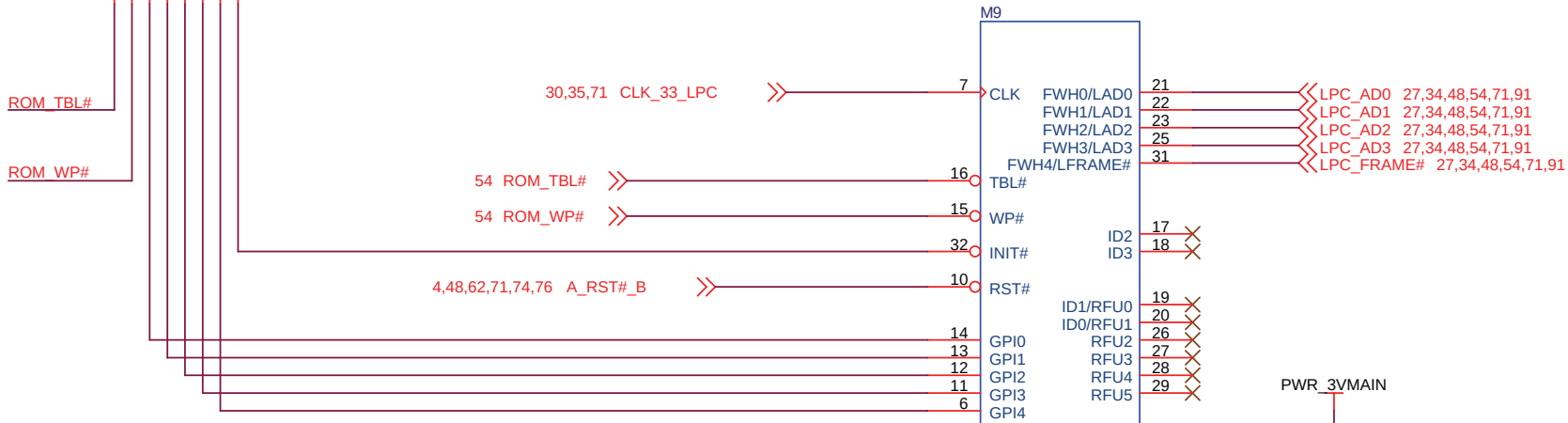
上記多連部品(8.2Kx4)については
配線しやすいようにピンスワップ可能。

Pullup for
AGP,PCI,LPC

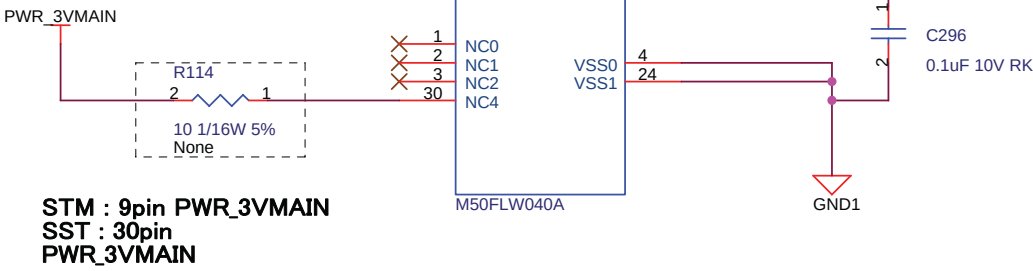
									TITLE
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								DRAW. No.	CAST
								C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita			Appr. Hasegawa	36 / 93	



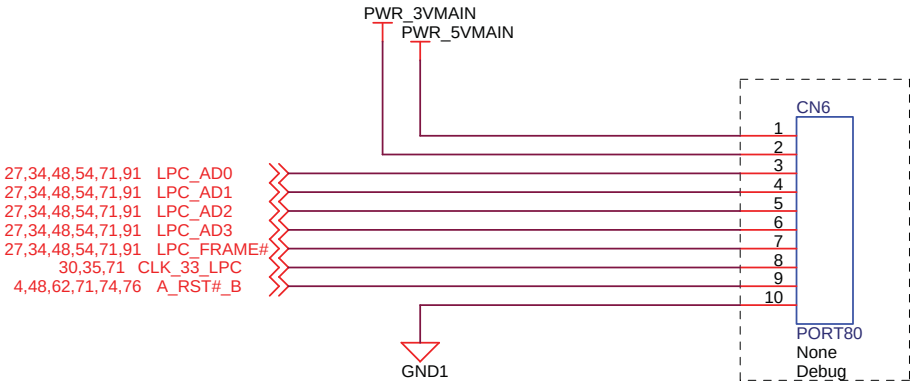
Socket for LPC ROM.
※LPC ROMはソケットを実装可能なパターンにすること。



M050FLW040 2pin has internal Pull-down

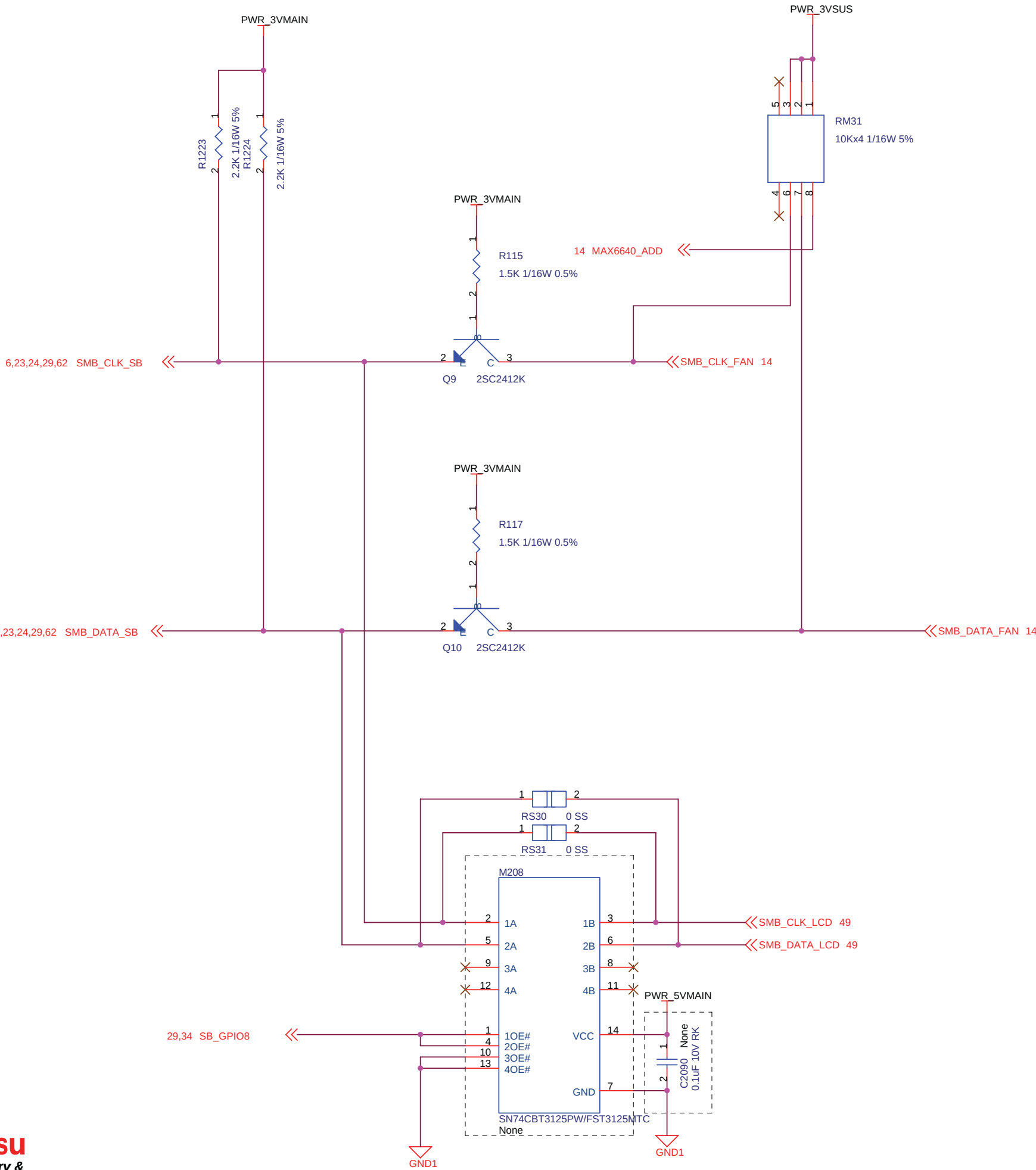


STM : 9pin PWR_3VMAIN
SST : 30pin PWR_3VMAIN



LPC ROM

						TITLE		
						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	37 / 93



Device	Hex	Address
MAX6640	5Eh	0101 111x b
MEM slot0	A2h	1010 001x b
MEM slot1	A4h	1010 010x b
PMU	32h	0011 001x b
LCD(SPWG)	A0h	1010 000x b

BUS	Device	address
	DIMM1	A2h
	DIMM2	A4h
	MAX6640	5Eh
	LCD	A0h
PLL	PLL	D2h
PMU	PMU	32h

SMBus

						TITLE		
						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	38 / 93

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E									E																																																					
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Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	39 / 93																																																						
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A		http://hobi-elektronika.net														A	
B																B	
C																C	
D																D	
E																E	
F																F	
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Fujitsu Proprietary & Confidential																Reserve	
Rev.		Date		Design		Check		Appr.		Description				TITLE			
Design		06/07/04		Mizukami		Check		Urita				Appr.		Hasegawa		VB313AA	
														DRAW. No.		CAST	
														C1CP302570-X2			
														FUJITSU LTD.		Sheet 41 / 93	

123456789									
A	http://hobi-elektronika.net								A
B									B
C									C
D									D
E									E
F									F
G							Reserve		G

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A		http://hobi-elektronika.net														A	
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F																F	
G																G	
Fujitsu Proprietary & Confidential																Reserve	
Rev.		Date		Design		Check		Appr.		Description				TITLE			
Design		06/07/04		Mizukami		Check		Urita				Appr.		Hasegawa		VB313AA	
														DRAW. No.		CAST	
														C1CP302570-X2			
														FUJITSU LTD.		Sheet 43 / 93	

1		2		3		4		5		6		7		8		9	
http://hobi-elektronika.net																	

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http://hobi-elektronika.net																			
A		Dolphin																A	
B		FUJITSU CONFIDENTIAL																B	
C																		C	
D																		D	
E																		E	
F																		F	
G		Reserve																G	
Rev.		Date		Design		Check		Appr.		Description								TITLE	
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																		DRAW. No.	
																		C1CP302570-X2	
																		CAST	
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http://hobi-elektronika.net																	

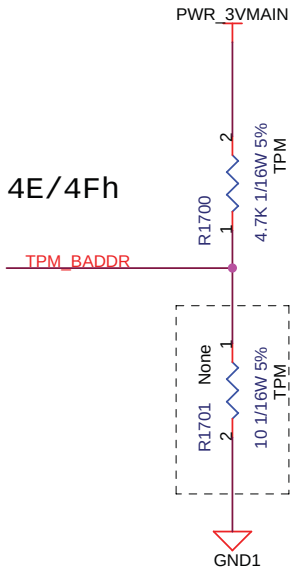
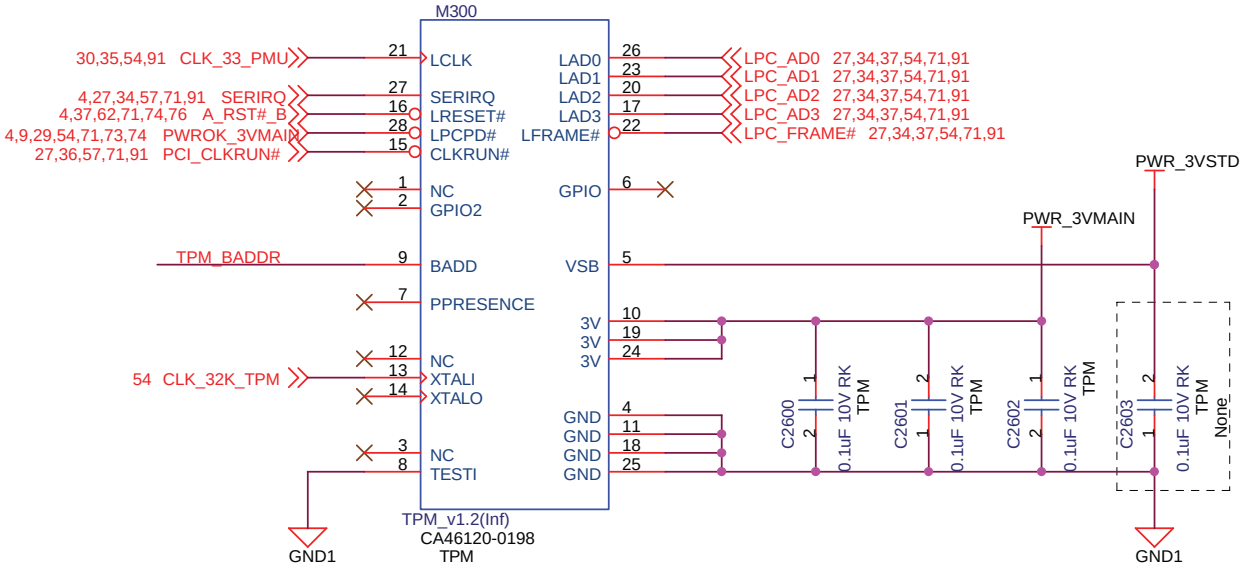
FUJITSU CONFIDENTIAL

Dolphin

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Confidential

TPM Configuration

	High	Low
TPM_BADDR	4E/4Fh	2E/2Fh



TPM

										TITLE	
										VB313AA	
										DRAW. No.	CAST
										C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description					FUJITSU LTD.	Sheet
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									TITLE	
									VB313AA	
									DRAW. No.	CAST
									C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.		Sheet 49 / 93
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa			

これらのコンデンサは可能な限りCN8直近に配置し、
GNDパターンは引き回さず、VIAでGND層に落とすこと。

これらのESD対策コンデンサは、
可能な限りDiodeの直近に配置すること

R119,120,121はCN7近傍に配置

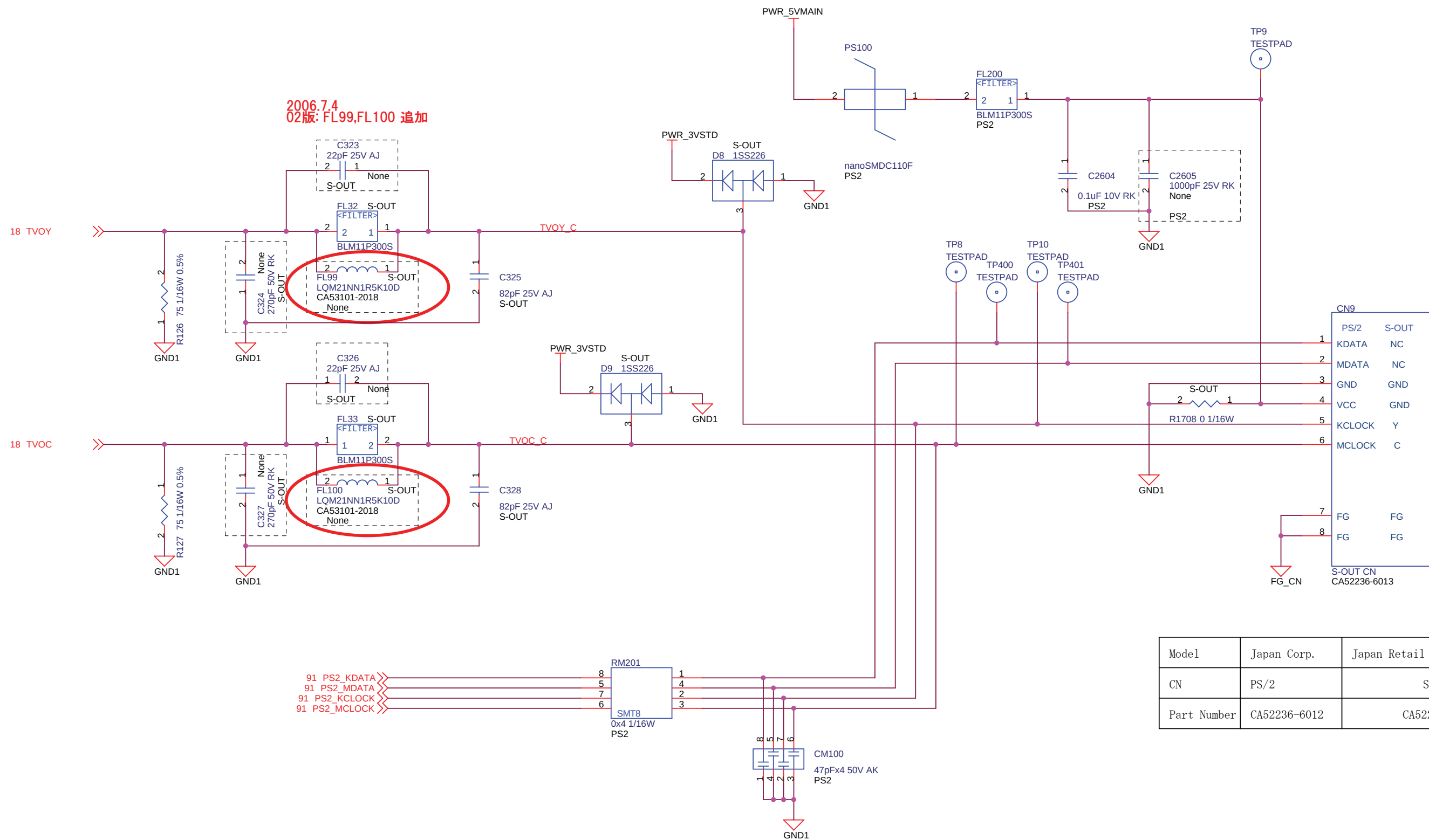
本ページに記載されている部品は
CRTコネクタの近くに配置すること。

CRT

					TITLE			
					VB313AA			
					DRAW. No.		CAST	
					C1CP302570-X2			
Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD. 50 / 93

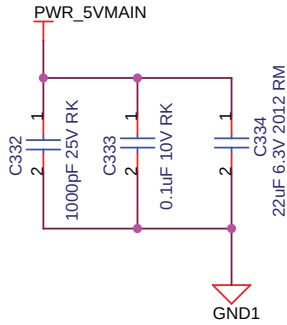
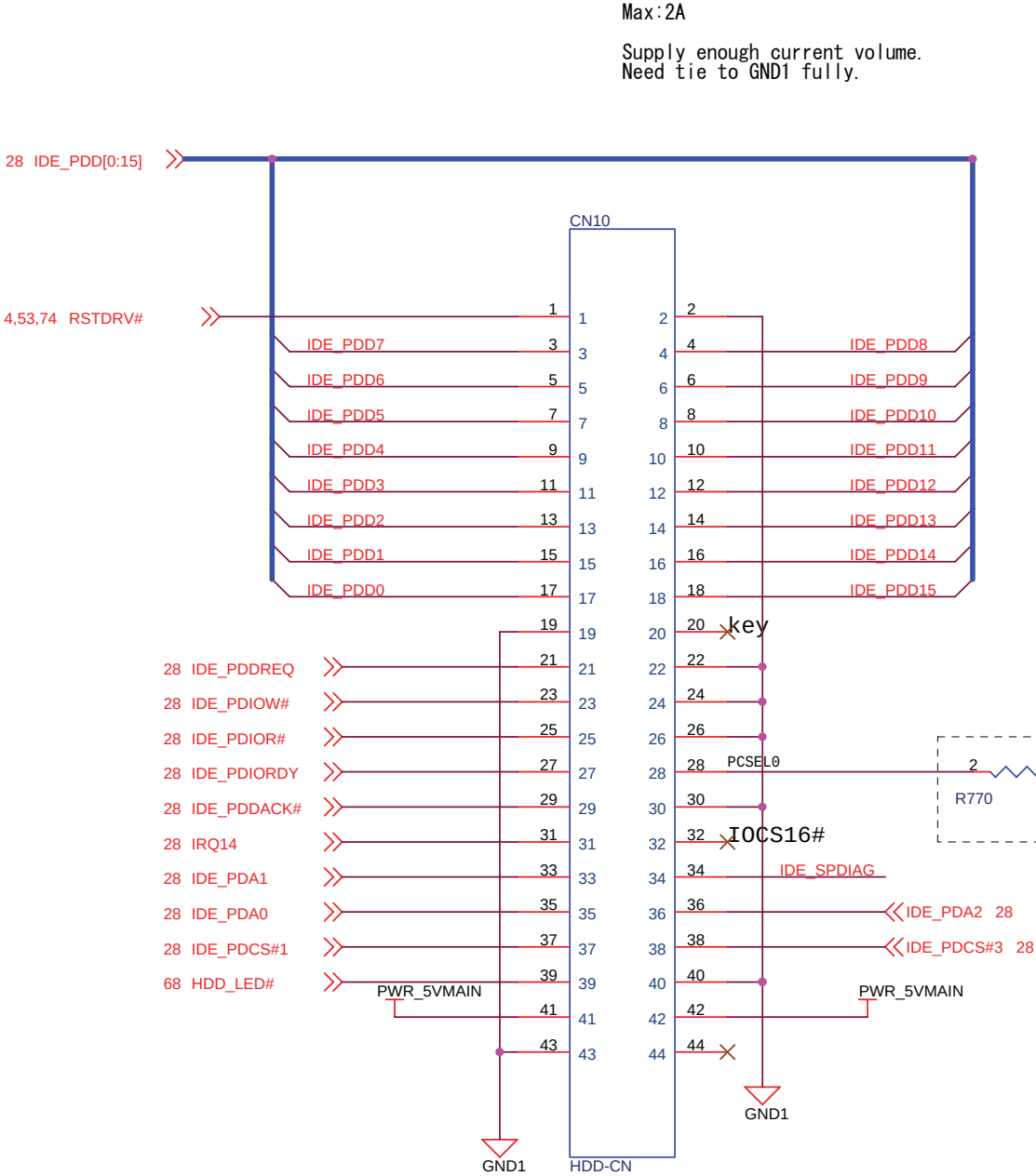
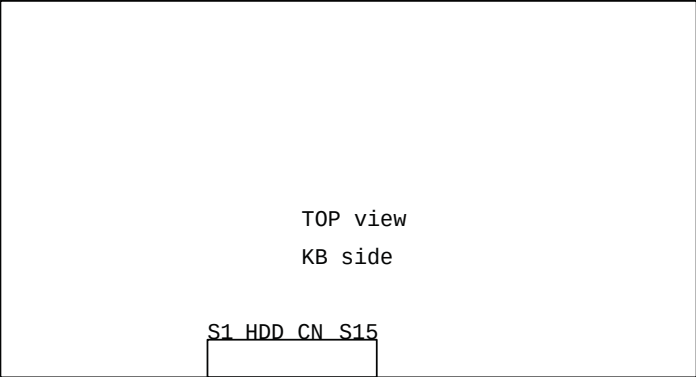
S-OUT/PS2

									TITLE	
									VB313AA	
									DRAW. No.	CAST
									C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa		51 / 93



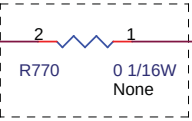
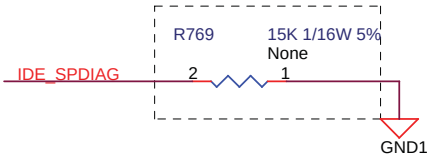
Model	Japan Corp.	Japan Retail Oversea
CN	PS/2	S-OUT
Part Number	CA52236-6012	CA52236-6013

FUJITSU CONFIDENTIAL Dolphin



Place the capacitors near power pin of HDD CN

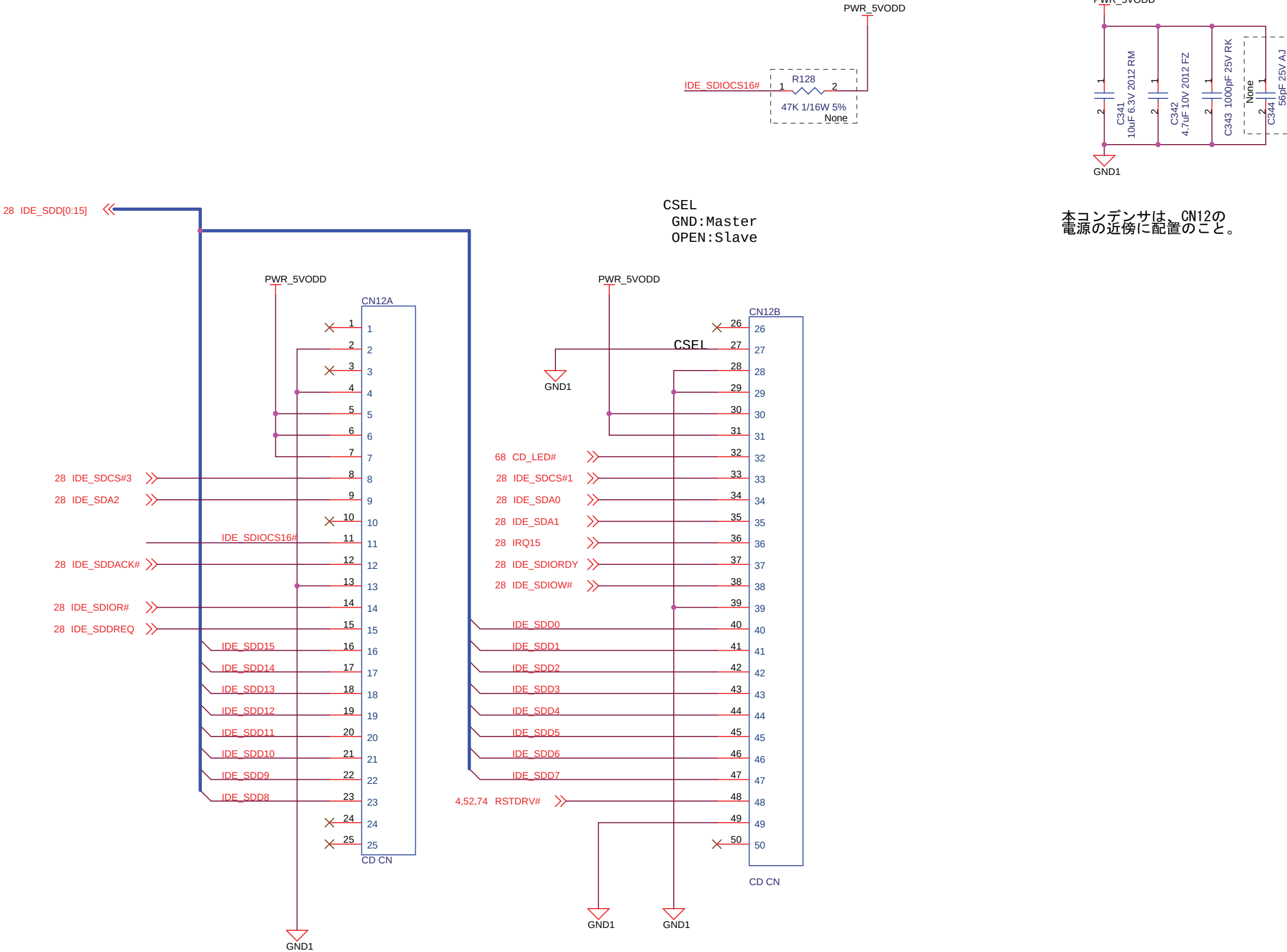
容量の小さいコンデンサを優先的にHDD-CNの電源PINの近くに配置すること。



1st HDD CN

						TITLE	
						VB313AA	
						DRAW. No.	CAST
						C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description	Sheet	
Design	06/07/04	Mizukami	Check	Urita		FUJITSU LTD.	52 / 93

FUJITSU CONFIDENTIAL Dolphin



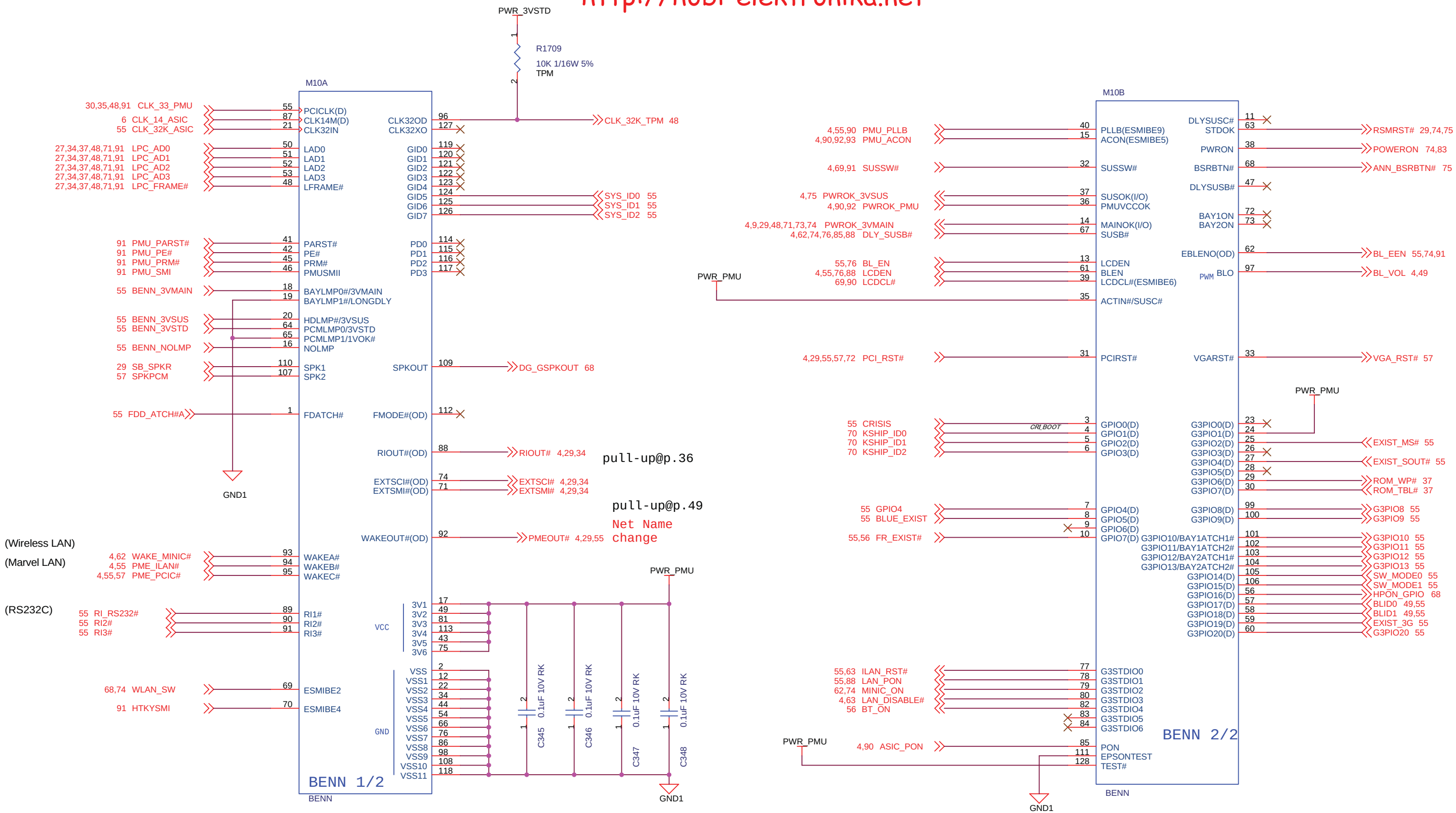
本コンデンサは、CN12の電源の近傍に配置のこと。

						TITLE	
						VB313AA	
						DRAW. No.	CAST
						C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.	
Design	06/07/04	Mizukami	Check	Urita		Sheet	53 / 93

Dolphin

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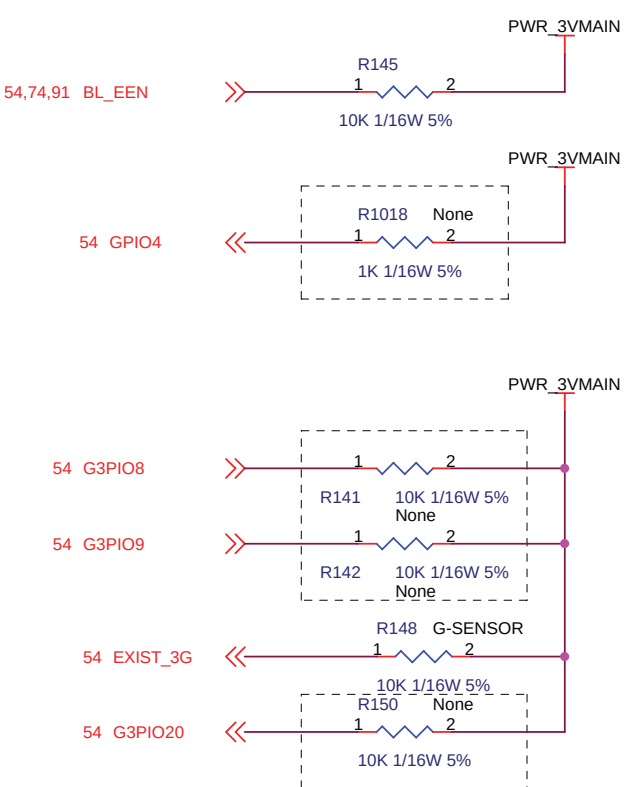
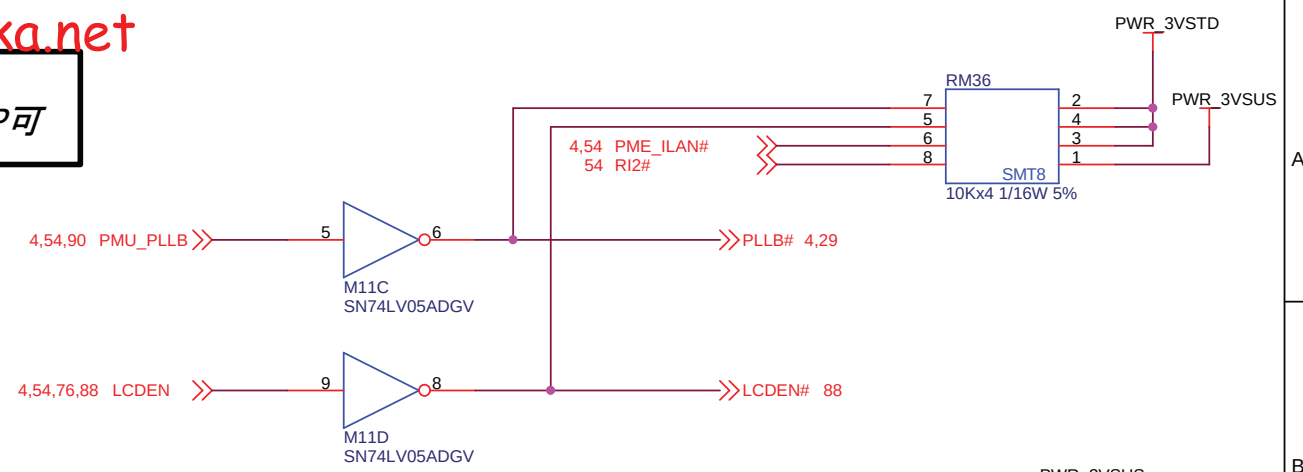
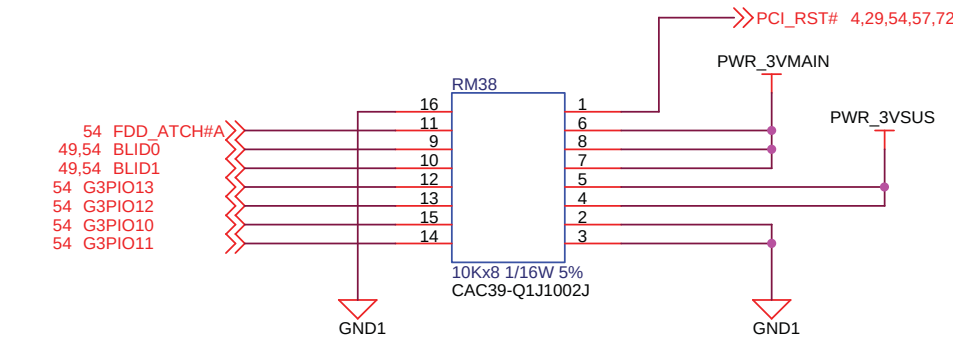


BENN

						TITLE VB313AA			
						DRAW. No.			CAST
						C1CP302570-X2			
Rev.	Date	Design	Check	Appr.	Description				Sheet 54 / 93
Design	06/07/04	Mizukami		Check	Urita		Appr.	Hasegawa	
					FUJITSU LTD.				

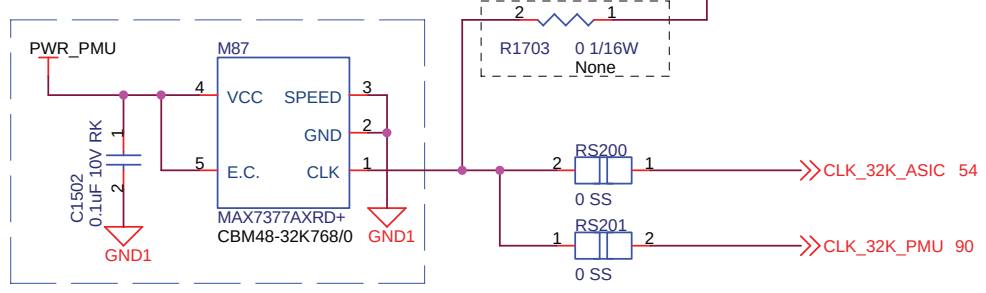
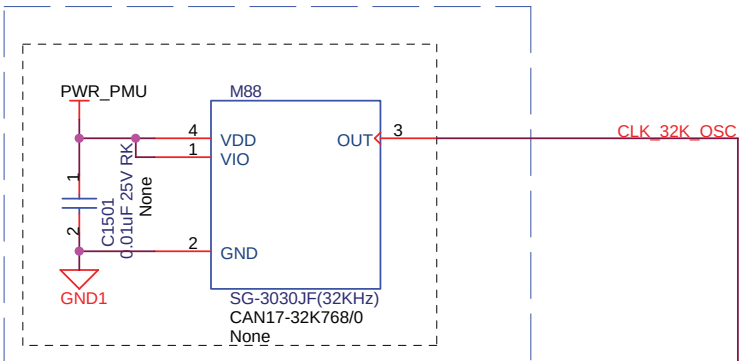
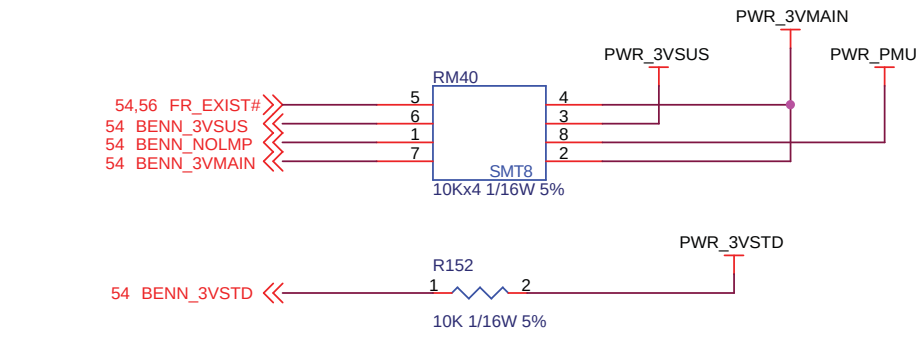
http://hobi-elektronika.net

本ページ内の集合抵抗については、
同じ容量のものについては部品間PINSWAP可



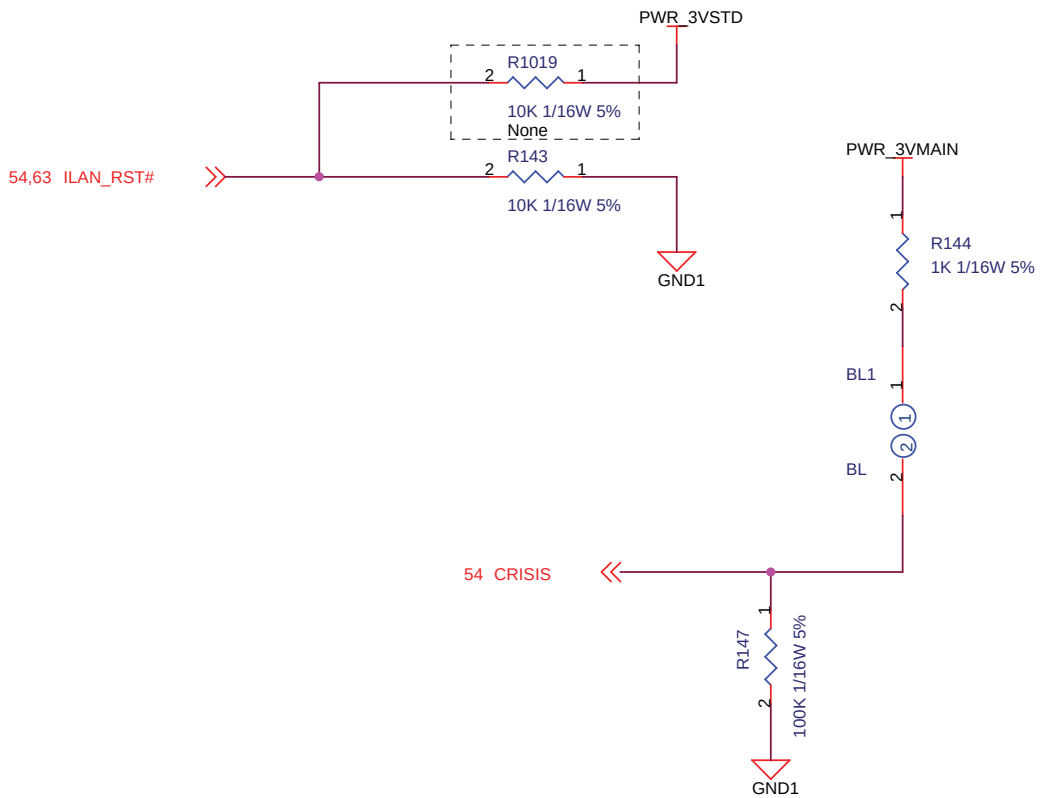
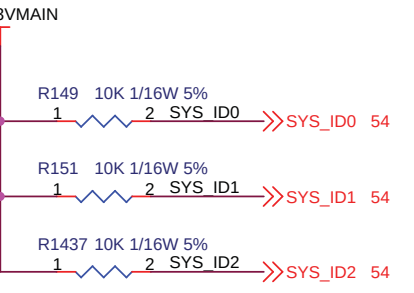
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[Appli], [Appli], [VolumeDown], [VolumeUp]
01 : 4ボタンモデル(FKL/FPC)
[Appli], [Appli], [Appli], [Appli]
10 : クラサバモデル
(T.B.D)
11 : 6ボタンモデル(仕向け先は未定。06秋冬はなし)
[Internet], [Mail], [A], [B], [VolumeDown], [VolumeUp]

※本IC/CAPの外周、及びその直下層はGND1とする。
2個以上の貫通VIAでGND層へと接続すること。



SYS_ID[2:0]
000 : 国内店頭
001 : 海外
010 : クラサバ
011 - 111 : Reserve

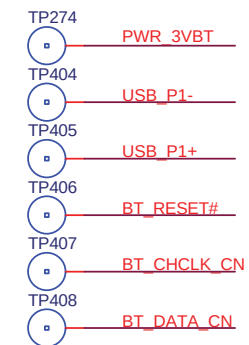
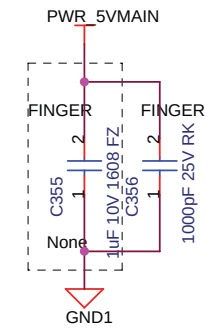
※本IC/CAPの外周、及びその直下層はGND1とする。
2個以上の貫通VIAでGND層へと接続すること。



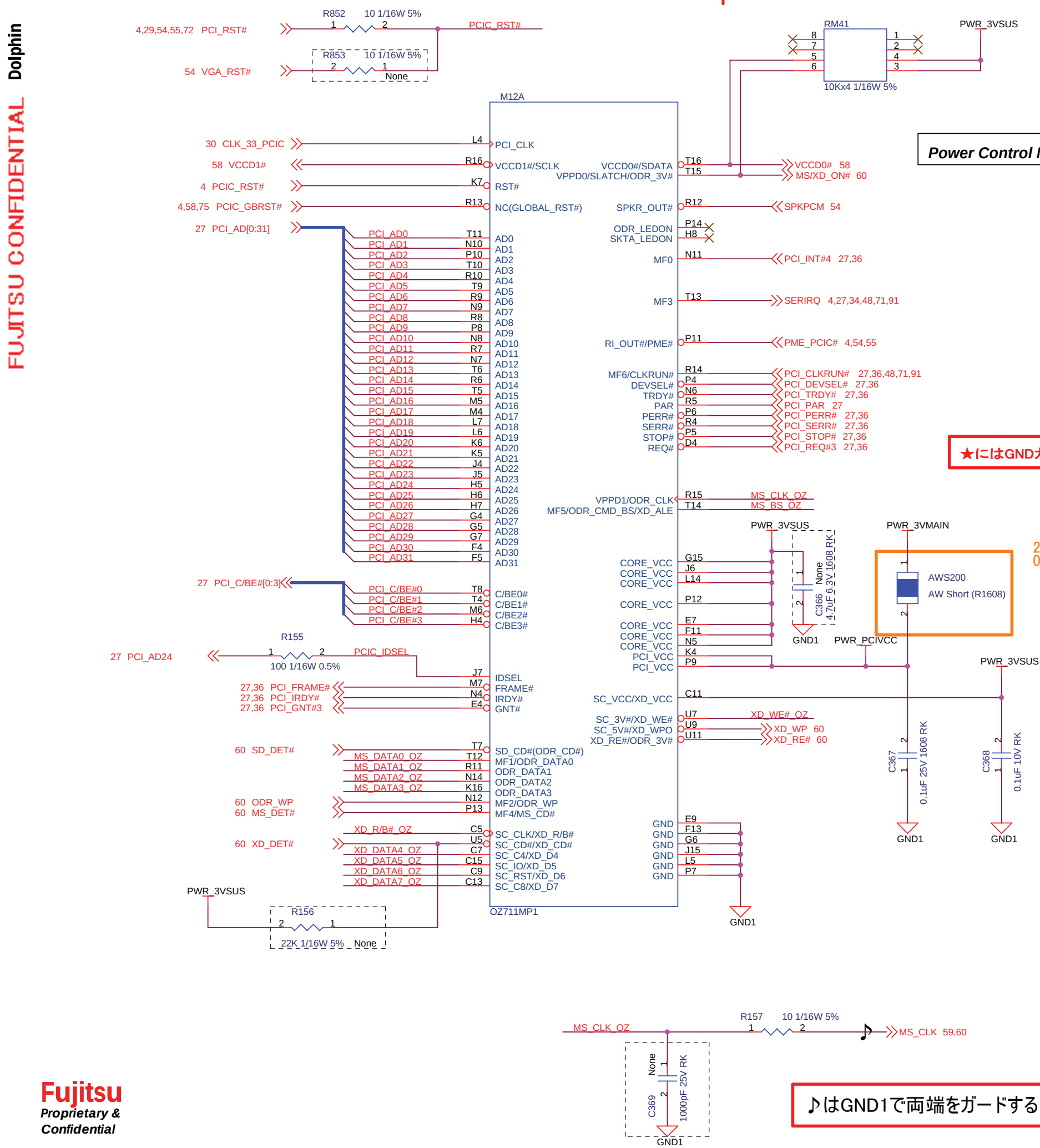
Pullup/down
for BENN

本ページ内の集合抵抗については、
特に指定の無い限りBENNの近傍に配置すること。

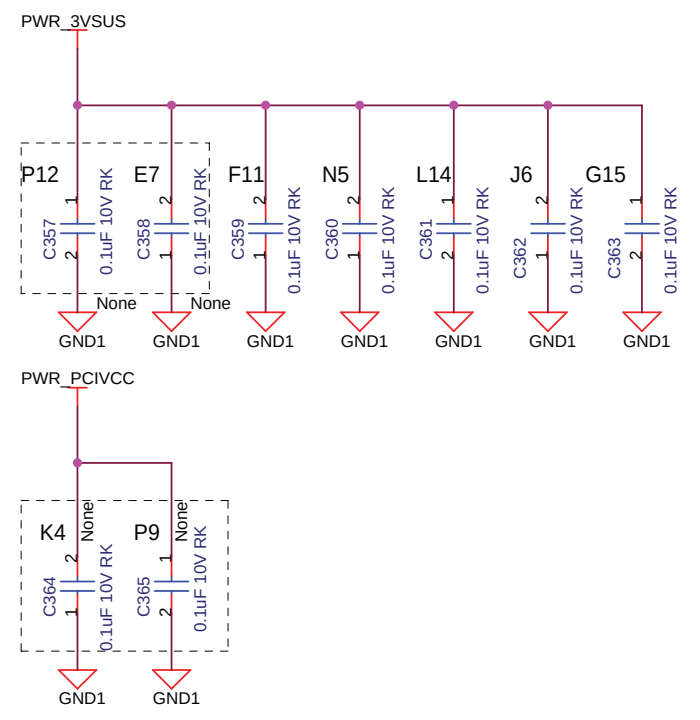
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						DRAW. No.	CAST
						C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description	Sheet	
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa	55 / 93	
						FUJITSU LTD.	



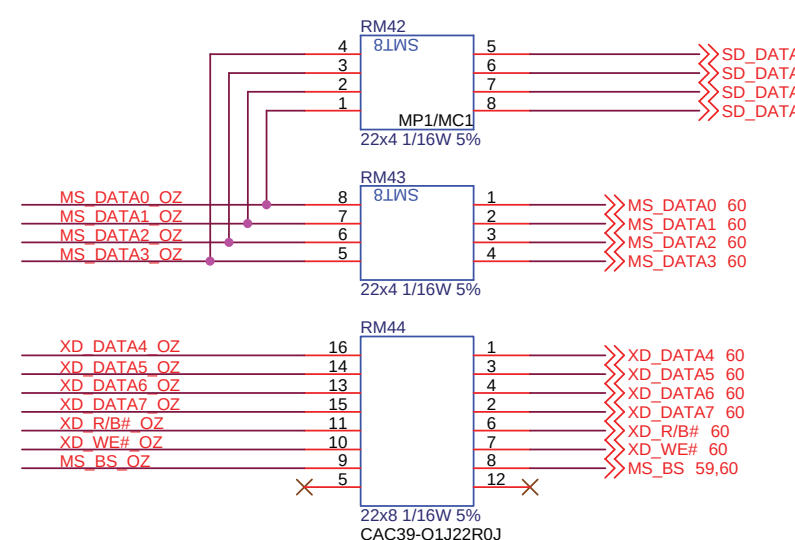
FINGER_CN



下記コンデンサは各電源PINの直近に配置すること。



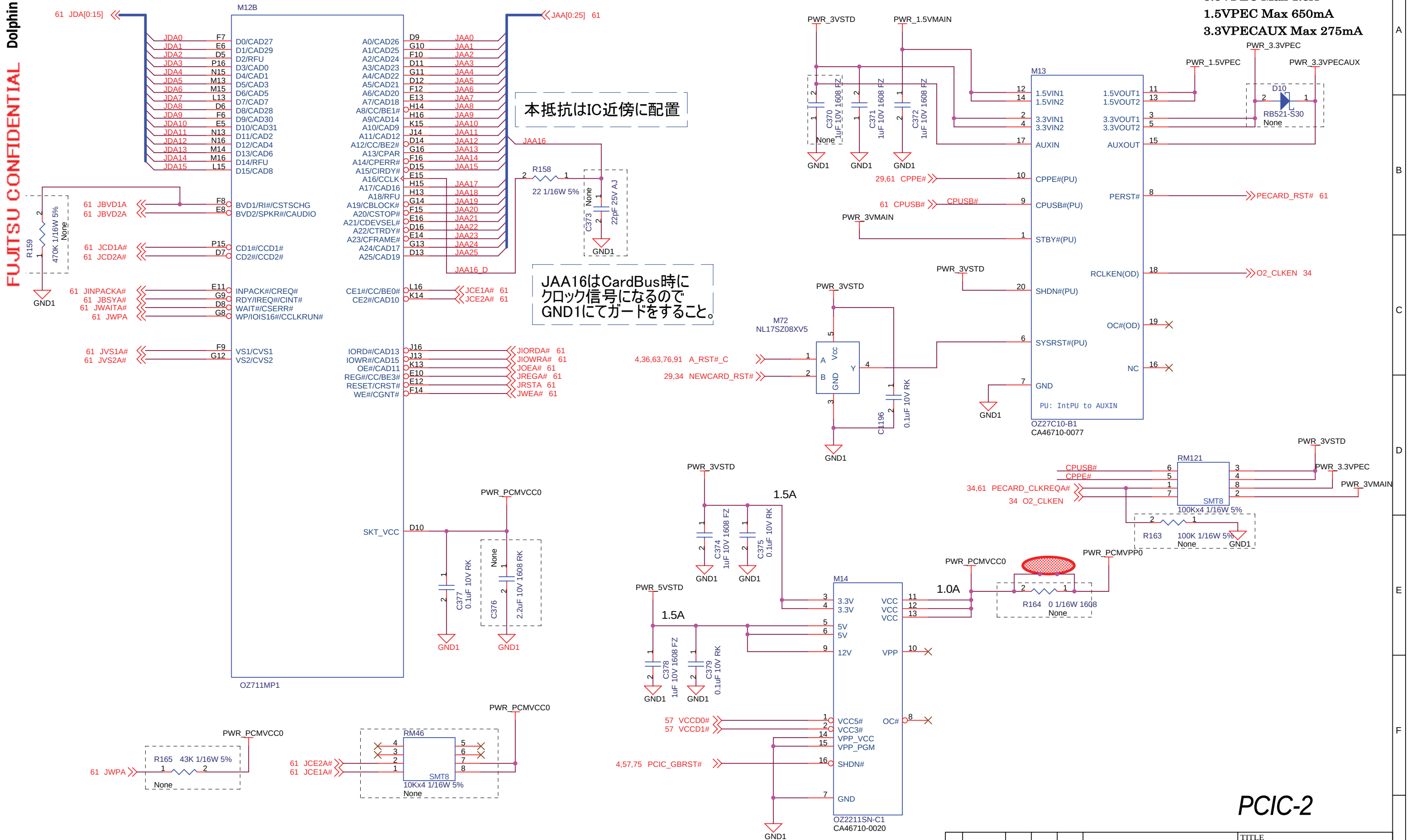
2006.6.26
02版: AWS200追加
PWR_PCIVCCの浮きを修正



PCIC-1

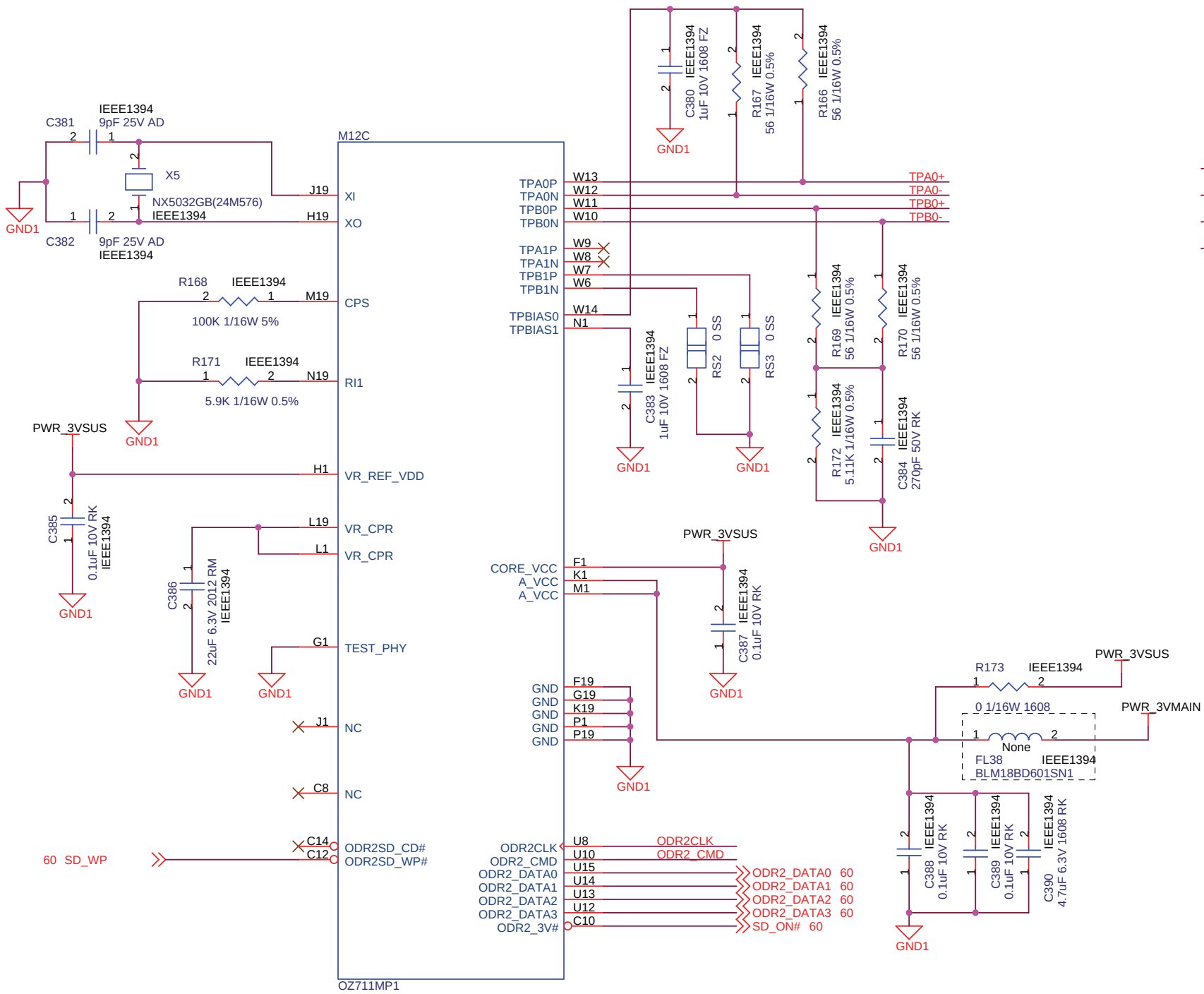
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						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa			
						Sheet		57 / 93

♪はGND1で両端をガードすること

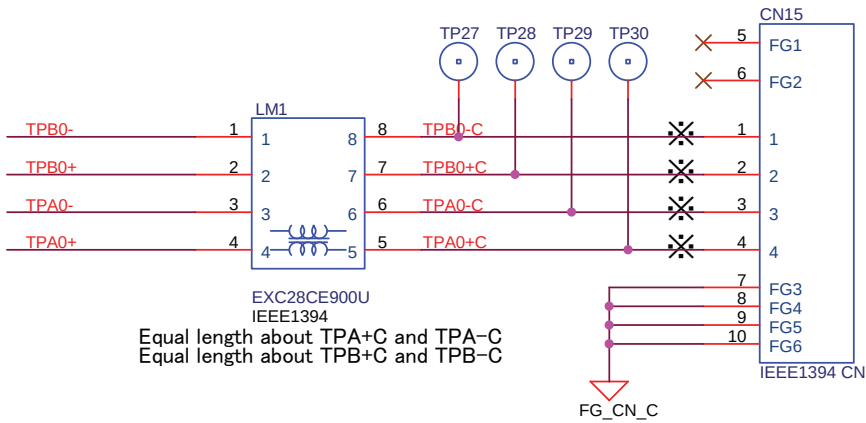


注 In case of using cardbus card, JAA16 are clock signal, these clock need have GND1 guard.
Place this clock dumping register near PCIC.

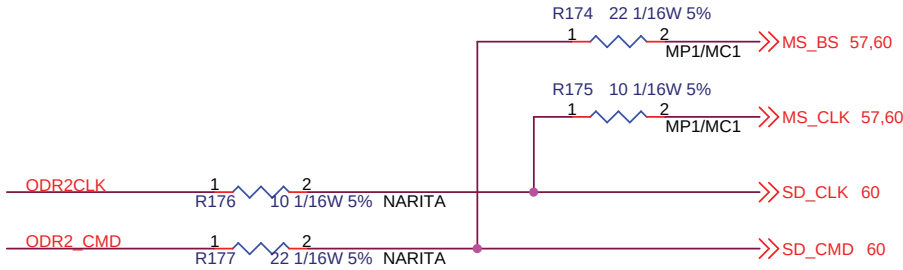
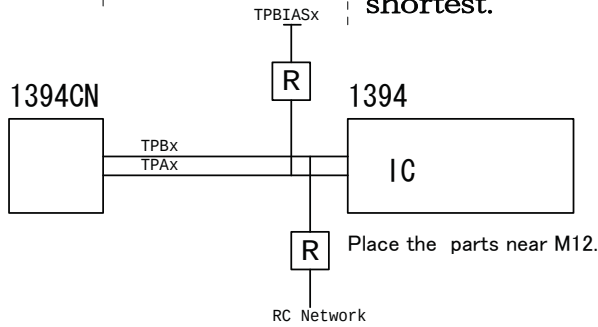
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						VB313AA		
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Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr. Hasegawa		58 / 93



Place Testpad for IEEE1394 without stab.



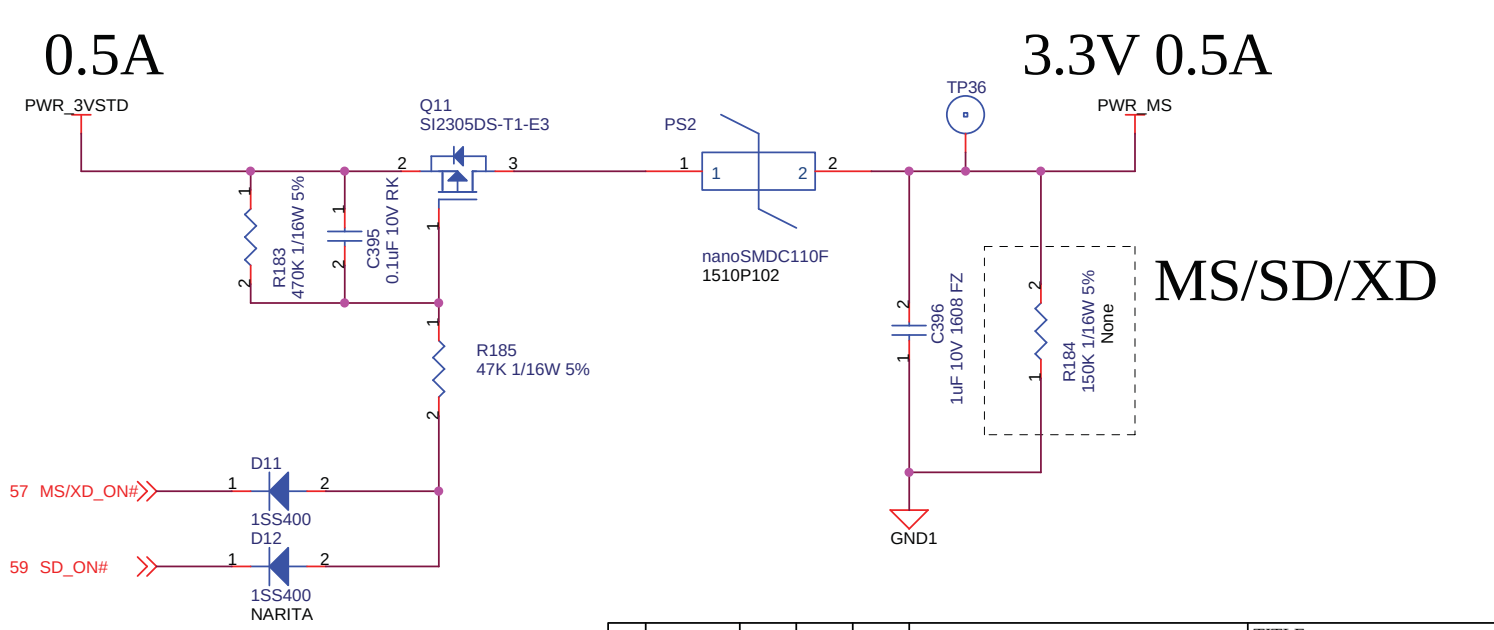
Minimize The interval of 1394 connector and M12 is shortest.



IEEE1394 CN

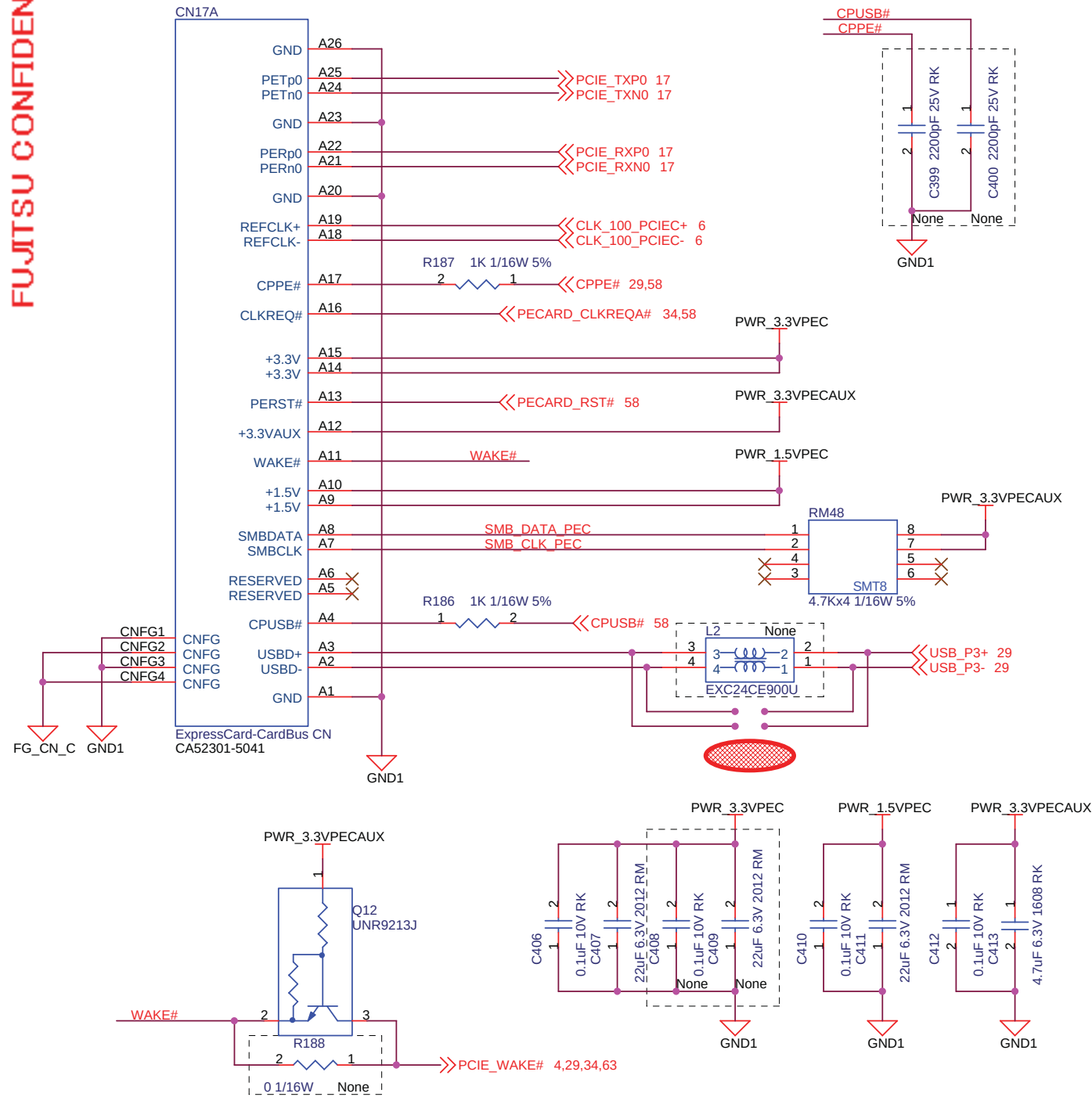
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Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr. Hasegawa	FUJITSU LTD.	
							59 / 93	

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						TITLE VB313AA					
									DRAW. No. C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description			Sheet 60 / 93			
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa				
					FUJITSU LTD.						

SLOT #1



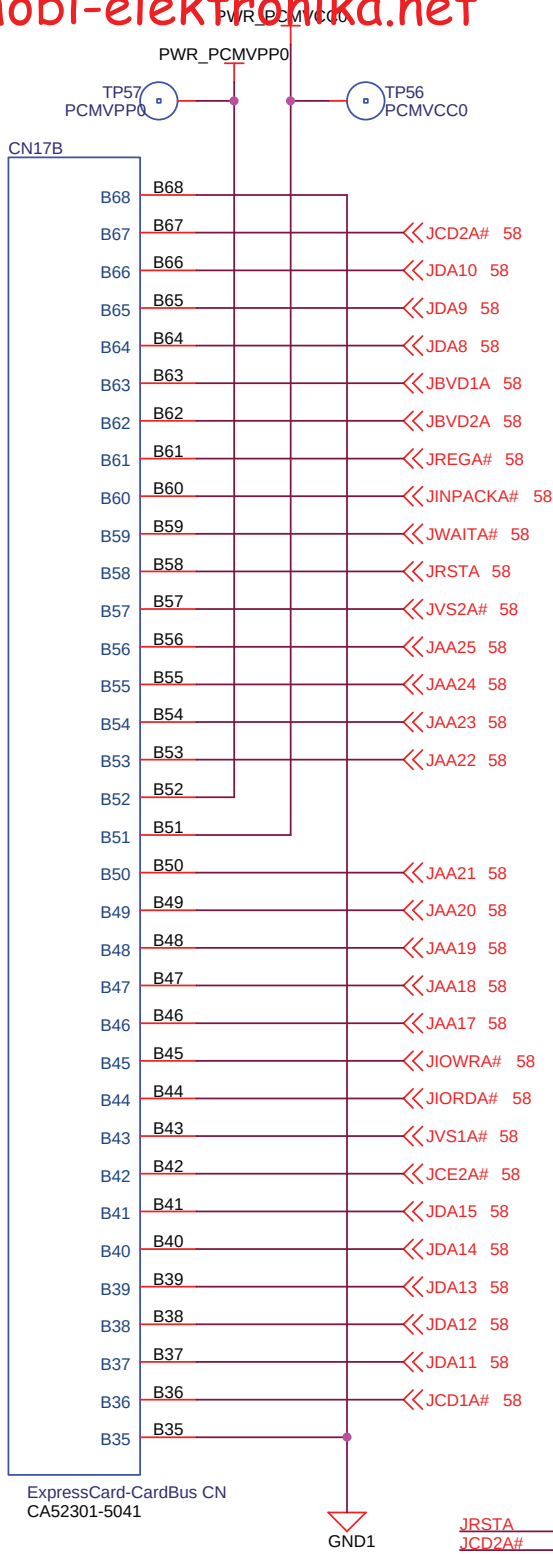
05/11
部品変更
Q12 : DTC144EE (CA47001-0312) -->
DTC144EETL (CA471005016)

Fujitsu
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Confidential

FGはGND1に接続してください。

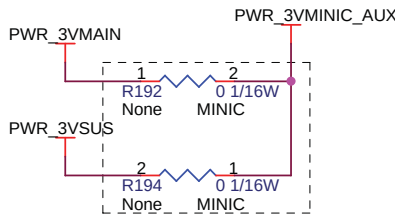
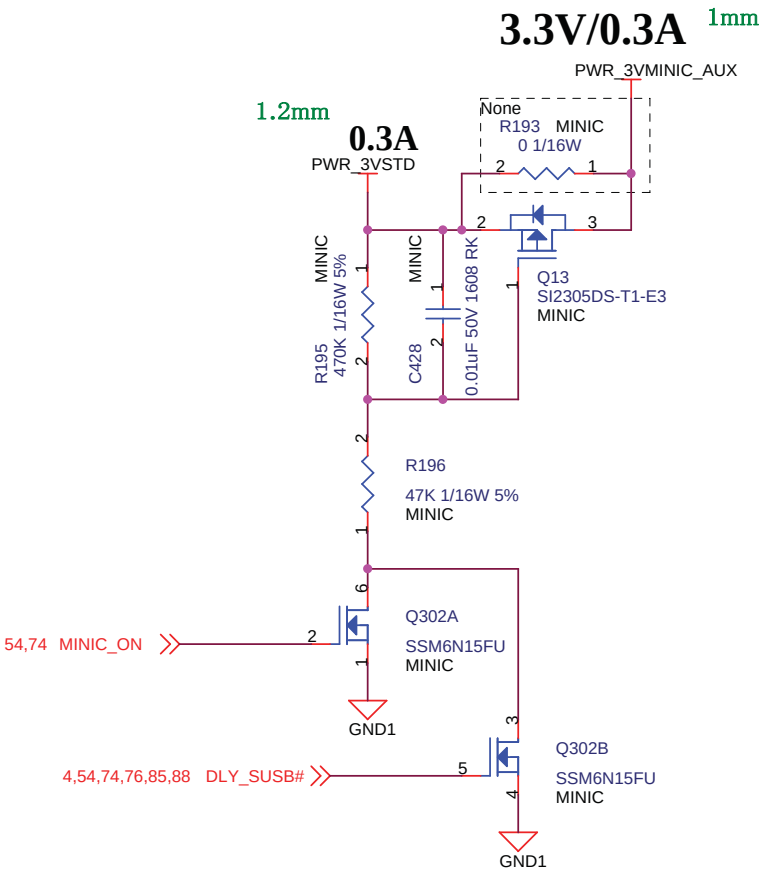
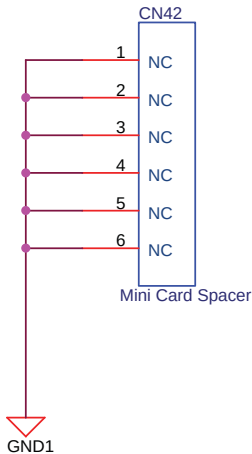
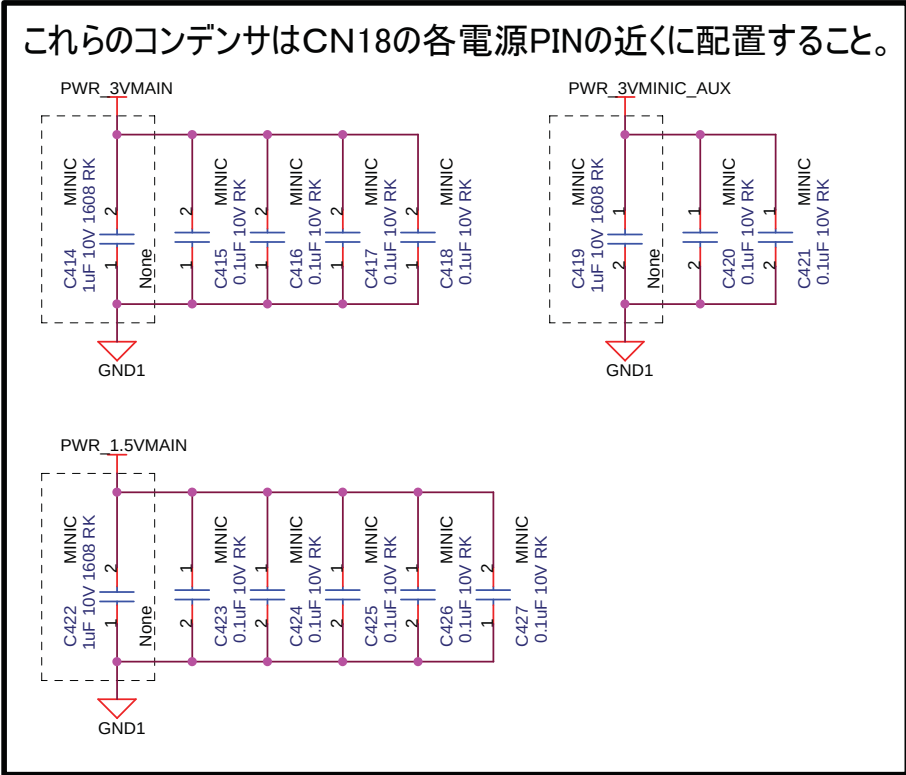
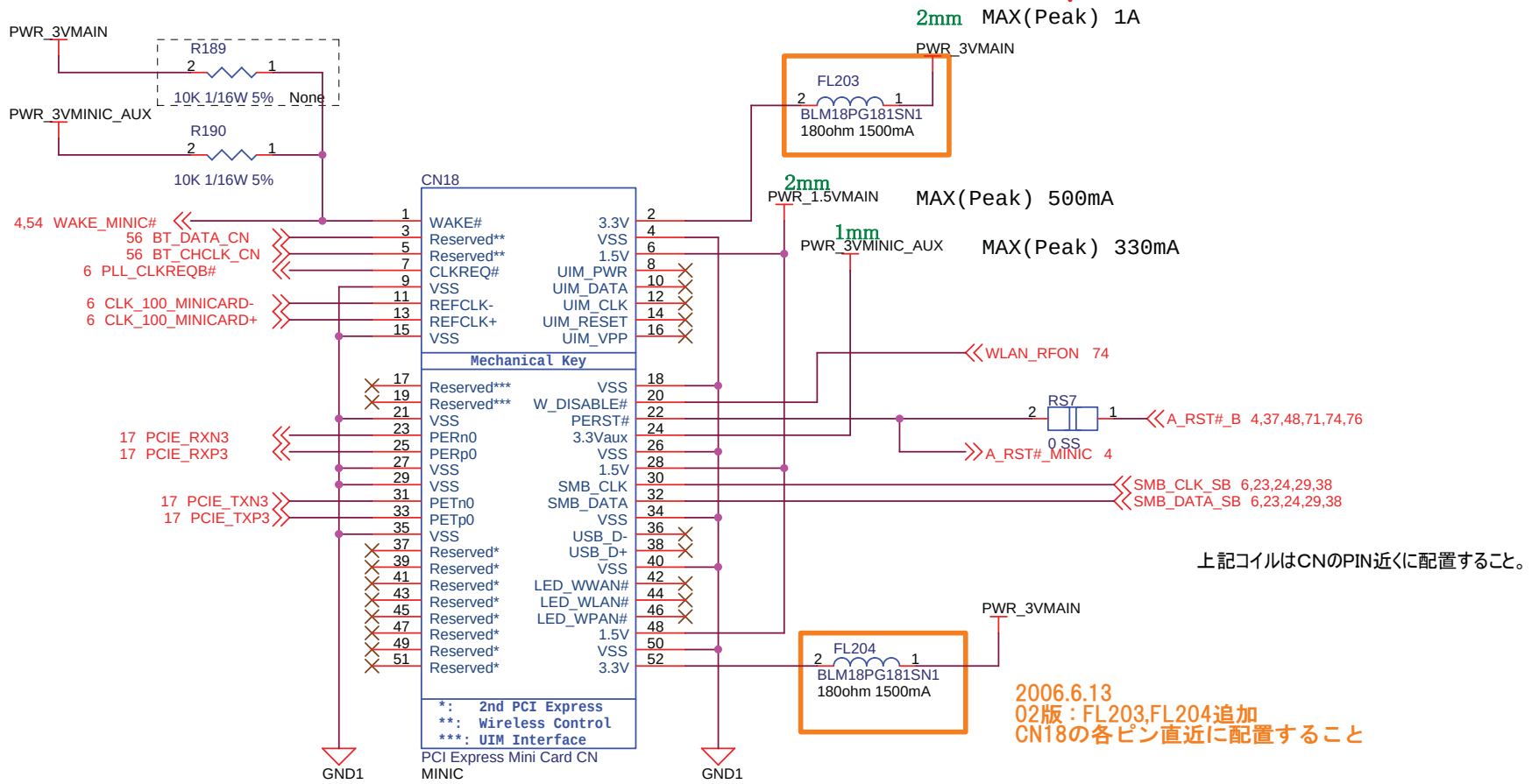
A・Bスロットとも JCE1x#, JCE2x#, JOEx#, JWEx#は、データベースとの平行配線とならないように配線すること。

SLOT #0



PCMCIA SLOT

								TITLE	
								VB313AA	
								DRAW. No.	CAST
								C1CP302570-X2	
								Sheet	
								61 / 93	
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa		



MiniCard CN

					TITLE			
					VB313AA			
					DRAW. No.		CAST	
					C1CP302570-X2			
Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa
					FUJITSU LTD.		62 / 93	

FUJITSU CONFIDENTIAL

Dolphin

B

C

D

E

F

G

A

B

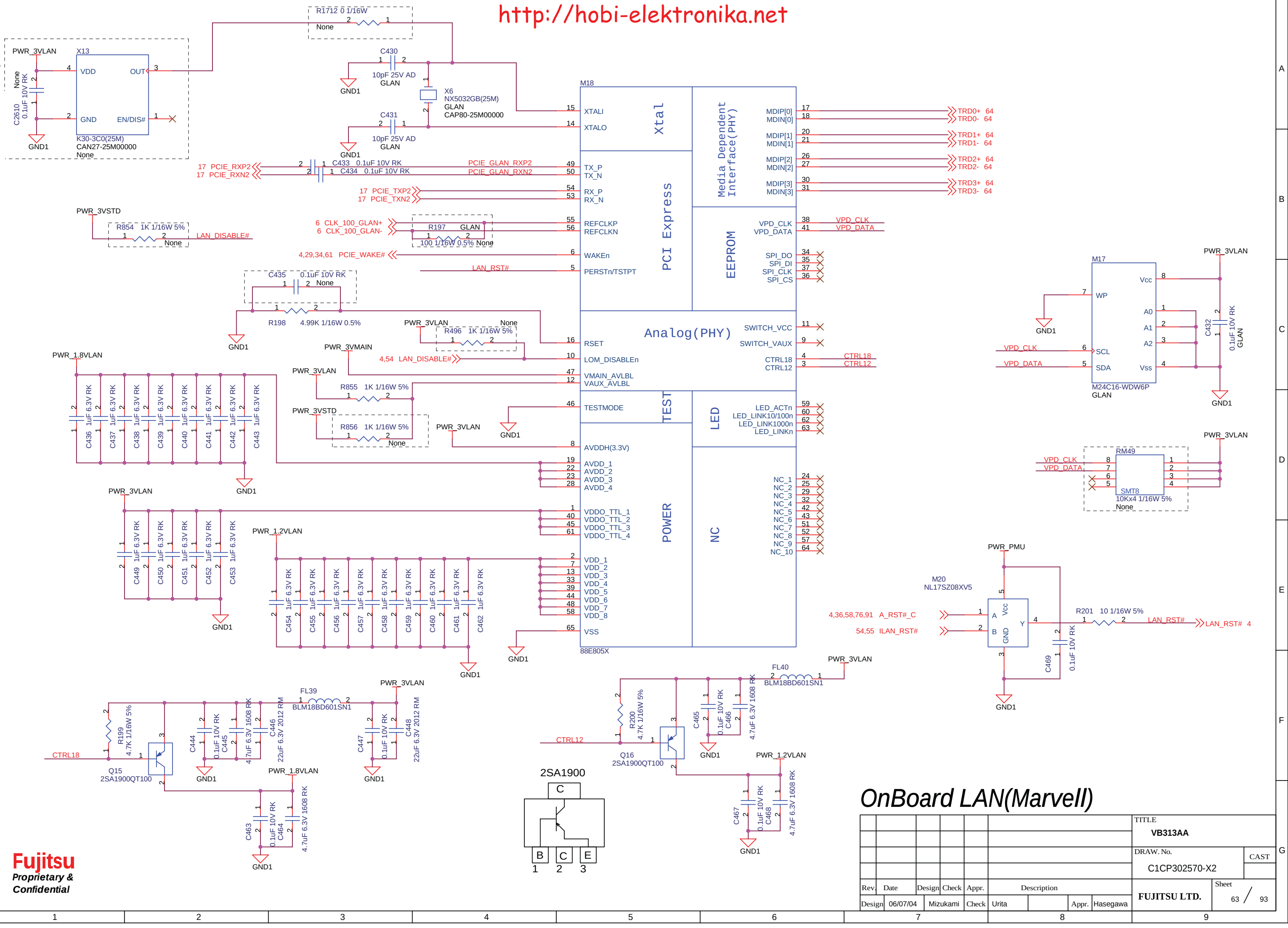
C

D

E

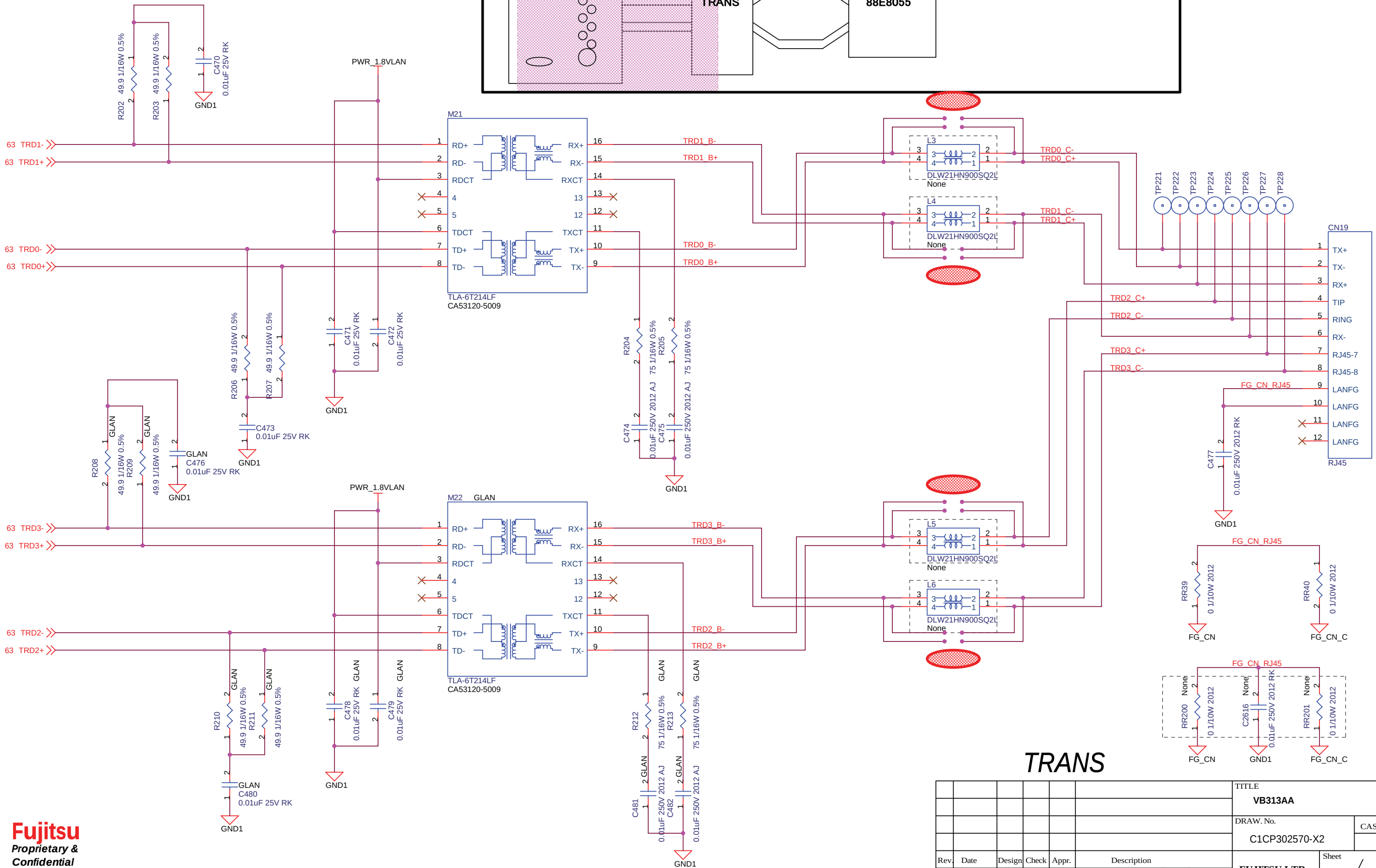
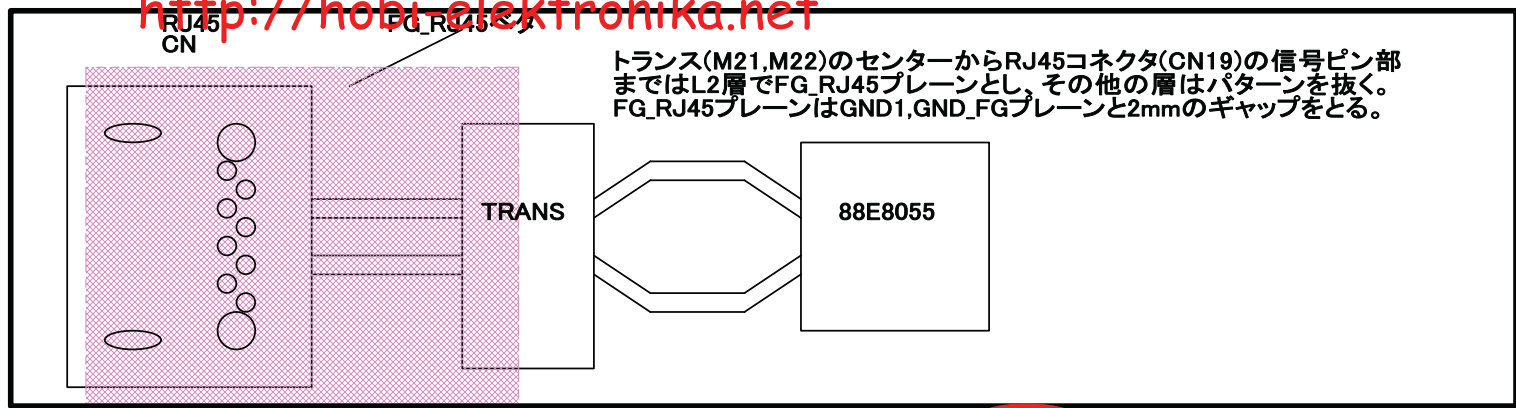
F

G



OnBoard LAN(Marvell)

						TITLE		
						VB313AA		
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						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	Sheet		
Design	06/07/04	Mizukami	Check	Urita		63 / 93		
						Fujitsu LTD.		



TRANS

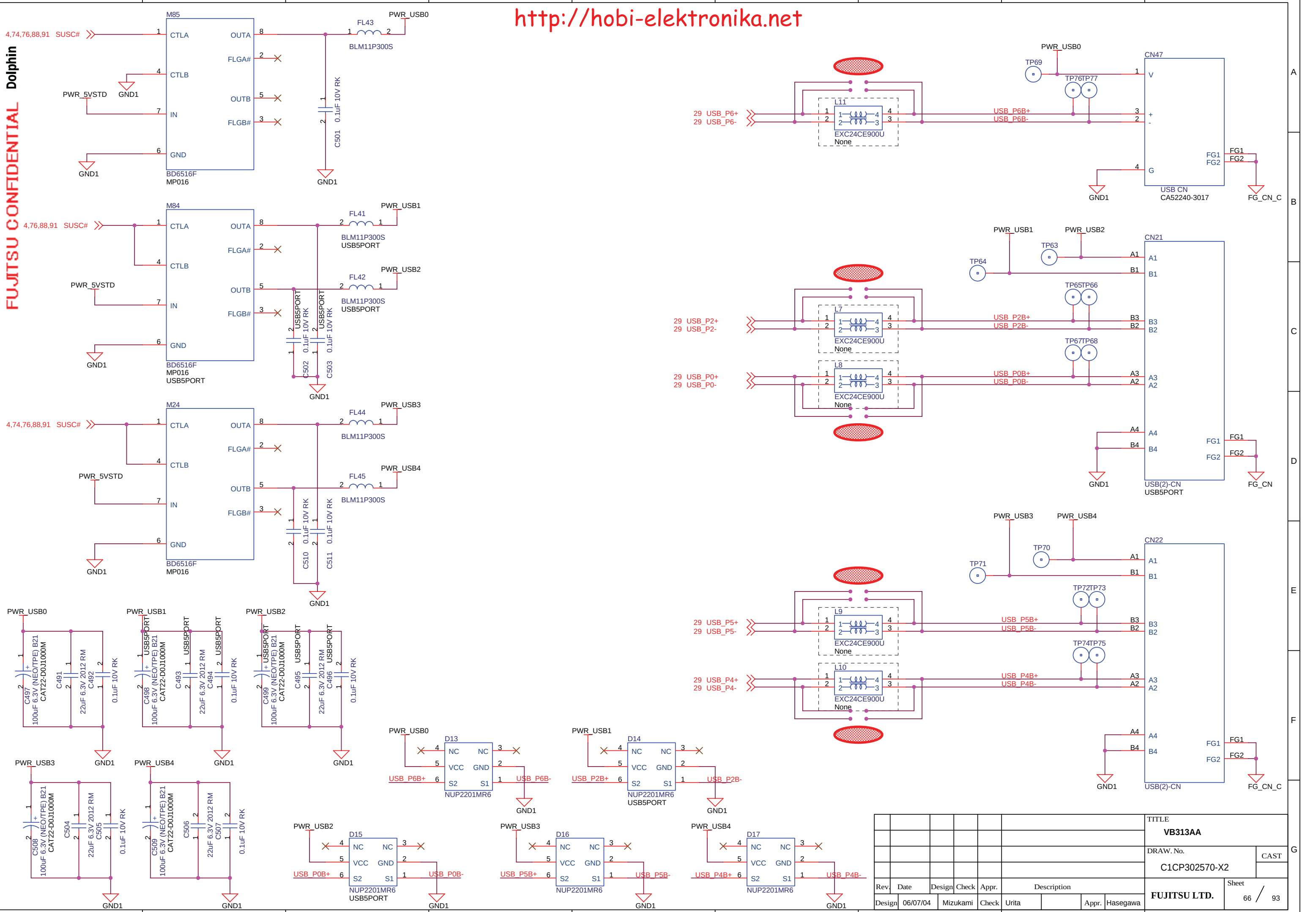
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Rev.	Date	Design	Check	Appr.	Description				Sheet	
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa	FUJITSU LTD. 64 / 93	

モジュールの固定用ネジ穴はGND1に接続する。

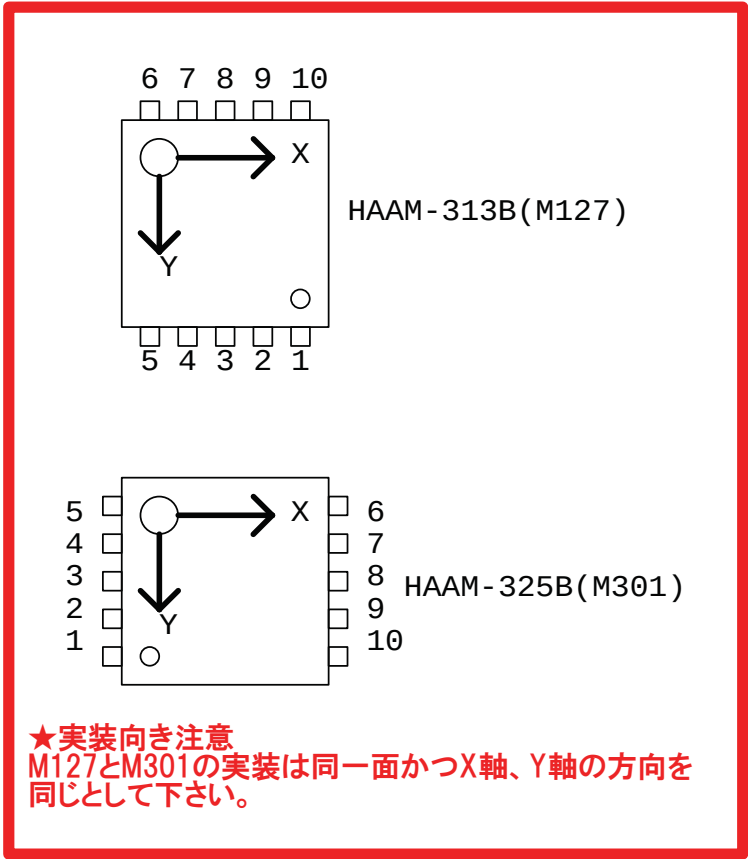
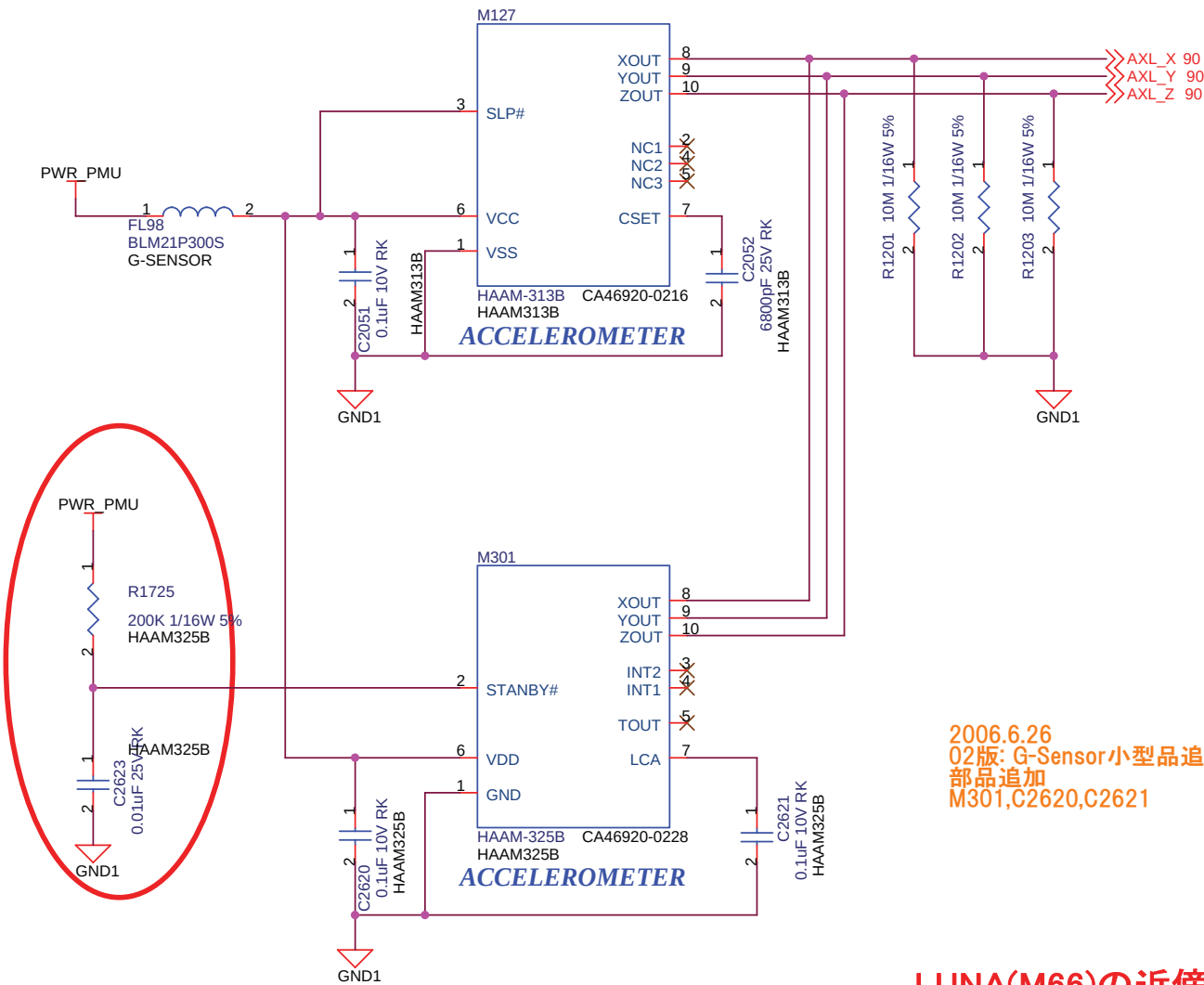


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Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD. Sheet 65 / 93
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa		

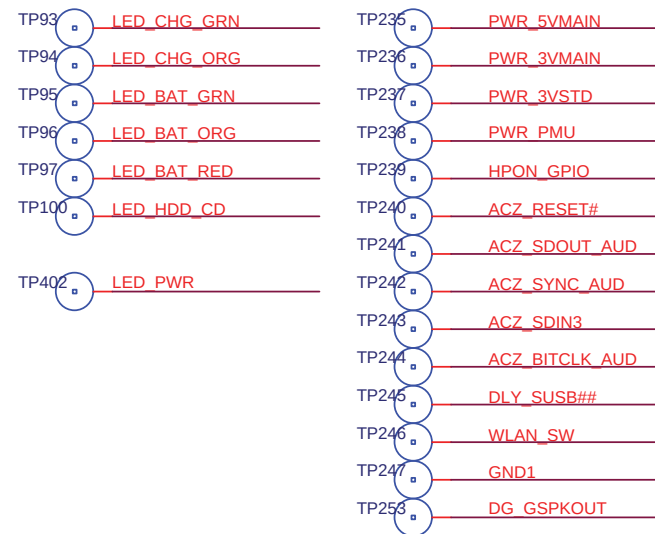
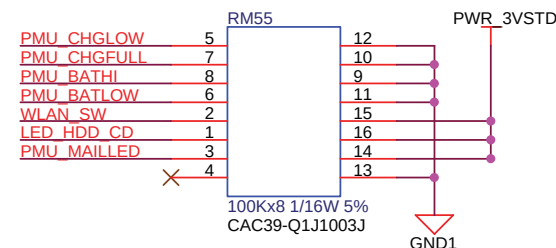
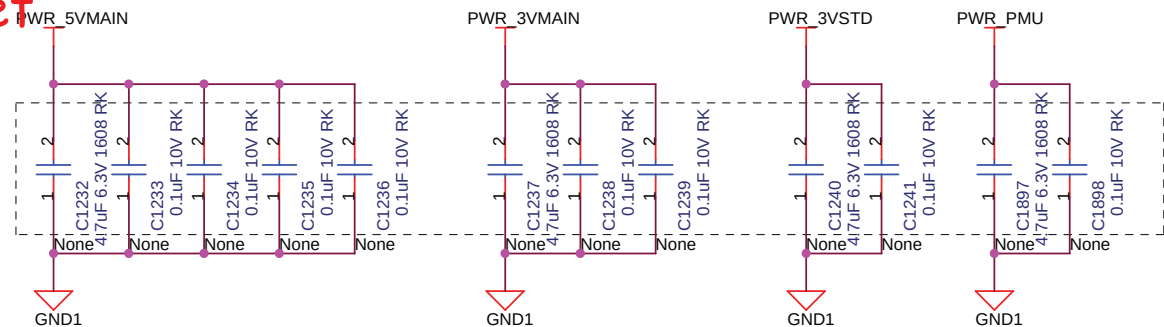
FUJITSU CONFIDENTIAL
Dolphin



						TITLE		
						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
						FUJITSU LTD.		Sheet 66 / 93
Rev.	Date	Design	Check	Appr.	Description			
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	

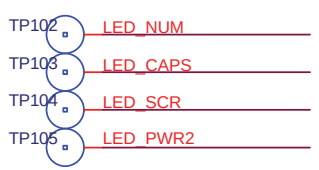
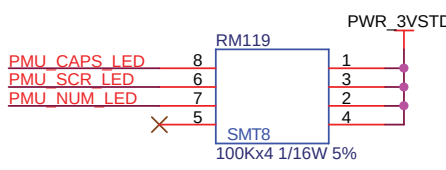
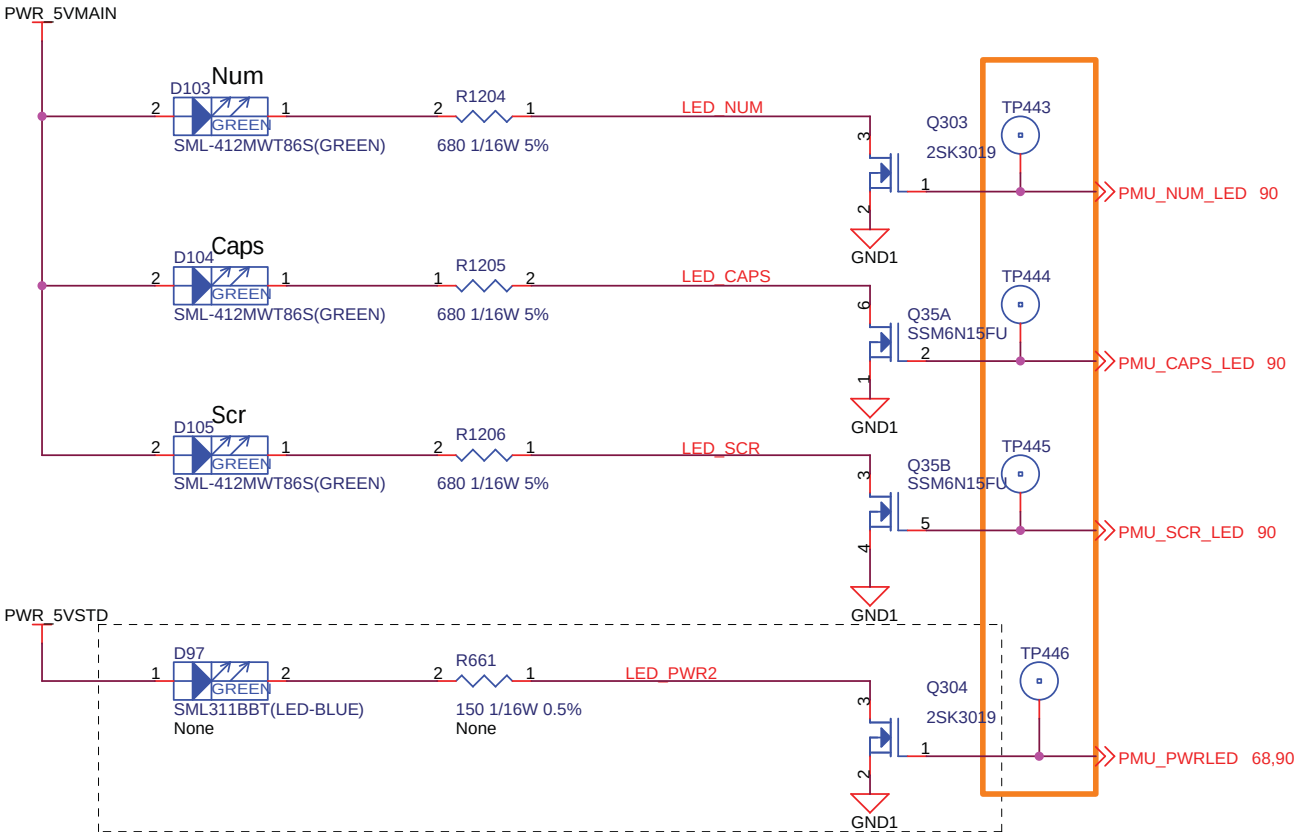


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						DRAW. No.		CAST
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Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	67 / 93



Audio/Statsu CN

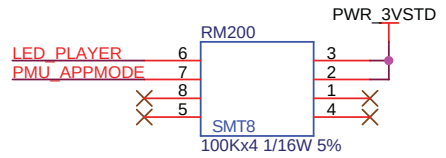
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									DRAW. No.	
									C1CP302570-X2	
									CAST	
Rev.	Date	Design	Check	Appr.	Description					
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa	FUJITSU LTD.	
									Sheet 68 / 93	



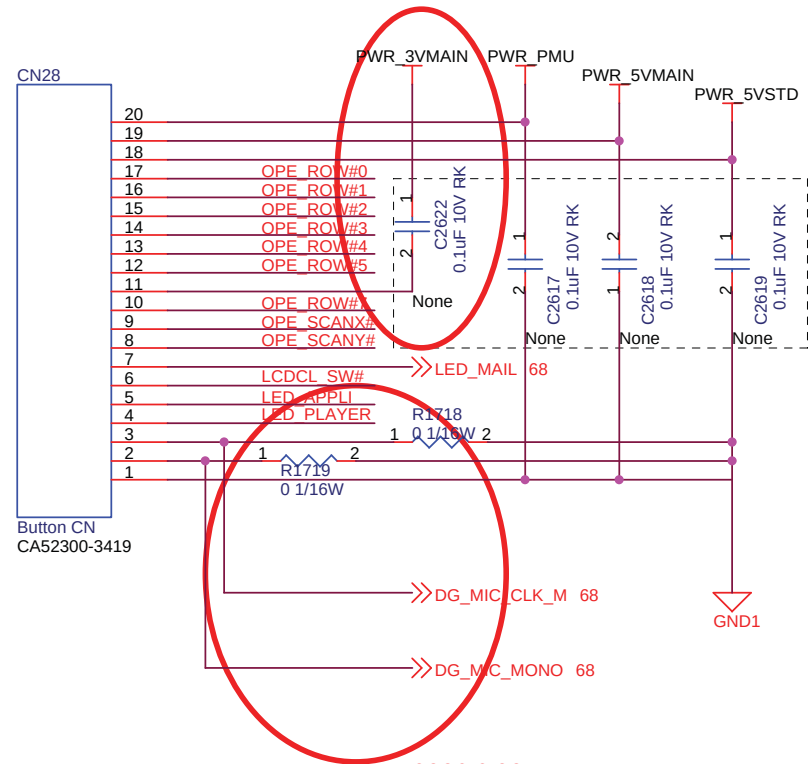
2006.6.26
02版: 電源ボタンにTP追加
(Fennecと配置の共通化をお願いします)

2006.6.26
02版: 電源ボタン変更
CA49001-5370 -> CA49001-5119

2006.6.26
02版:
LEDにTP追加。TP443,TP444,TP445,TP446
(Fennecと配置の共通化をお願いします)

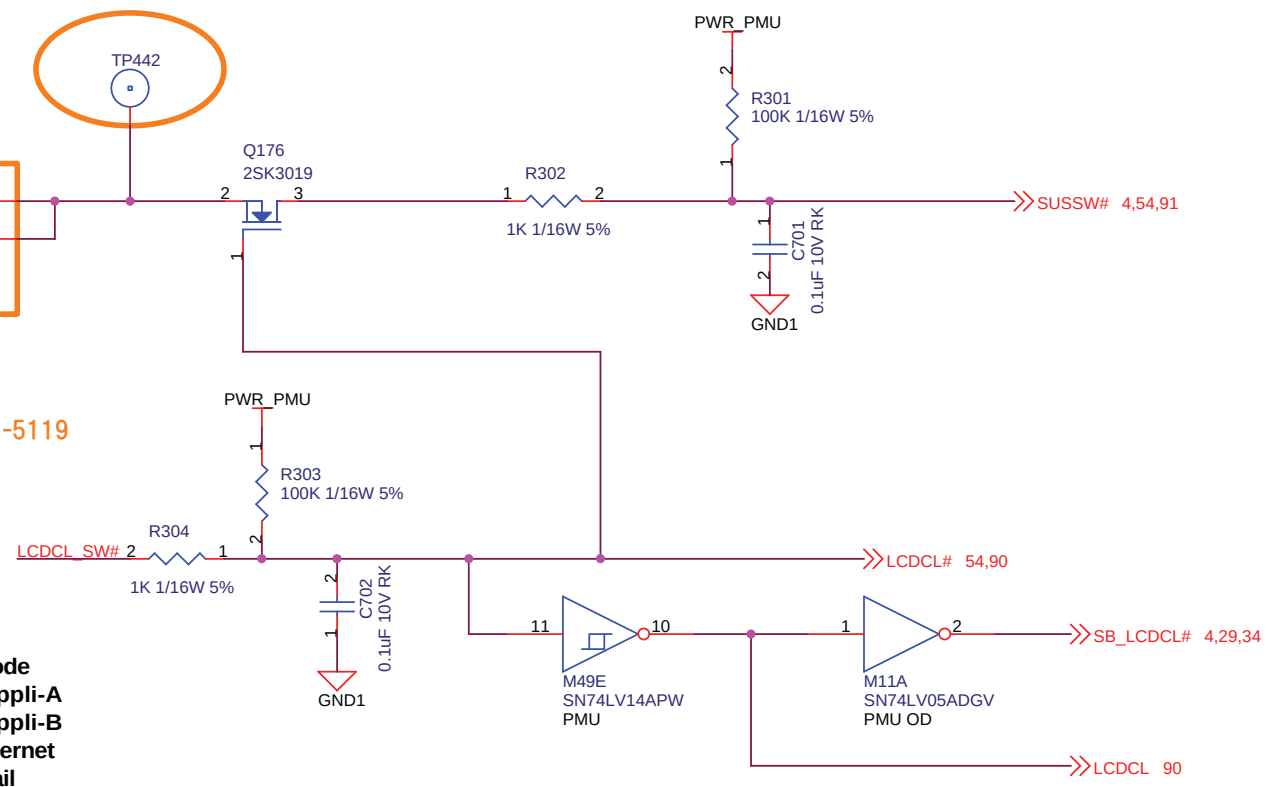
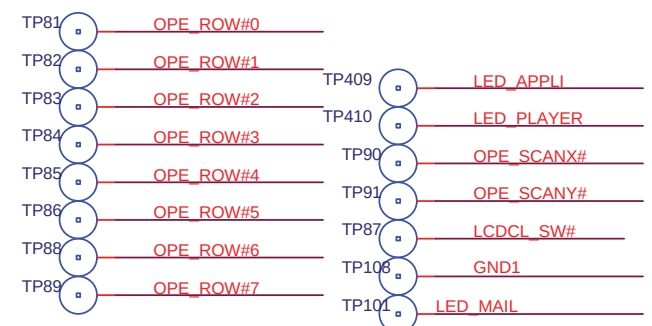
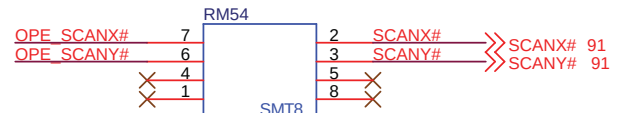
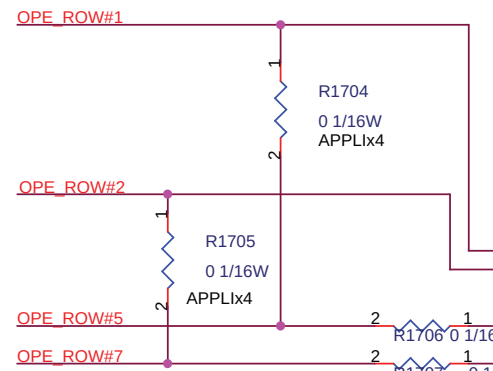


- ROW#0 SW_Mode
- ROW#1 SW_Appli-A
- ROW#2 SW_Appli-B
- ROW#3 SW_Internet
- ROW#4 SW_Mail
- ROW#5 SW_Vol_Down
- ROW#6 Unused
- ROW#7 SW_Vol_up



2006.6.30
02版: R1718-1721,C2622追加

2006.7.04
R1720,R1721をMainボードからAudioボードへ移動



[Button CN]

						TITLE		
						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
						FUJITSU LTD.		Sheet
						69 / 93		
Rev.	Date	Design	Check	Appr.	Description			
Design	06/07/04	Mizukami	Check	Urita				

Dolphin

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C

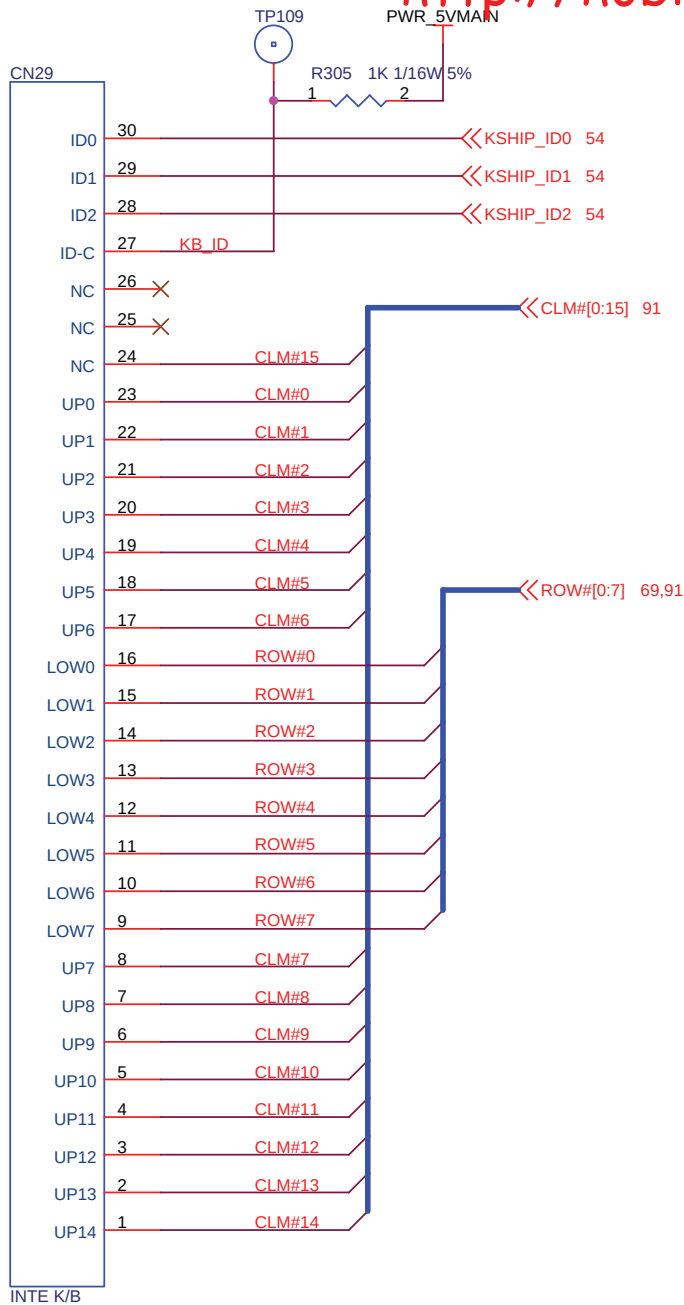
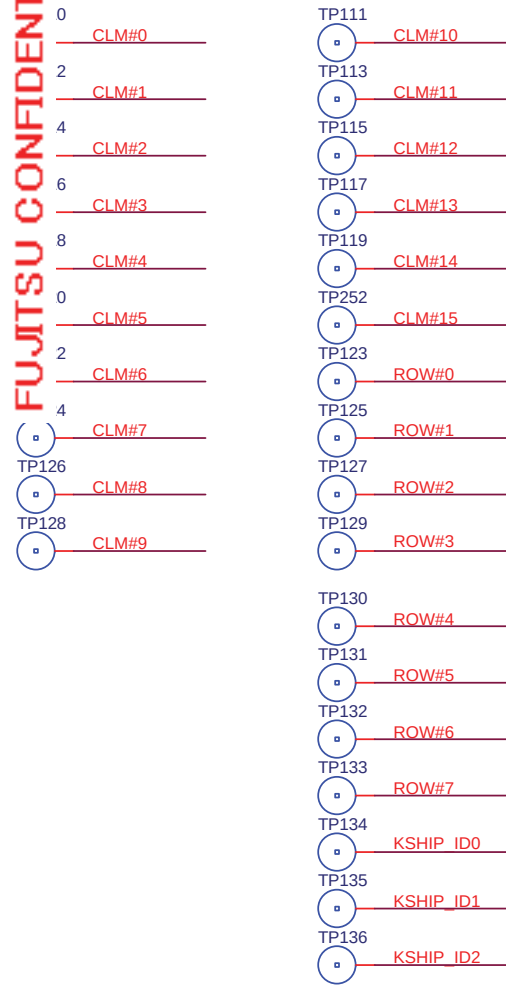
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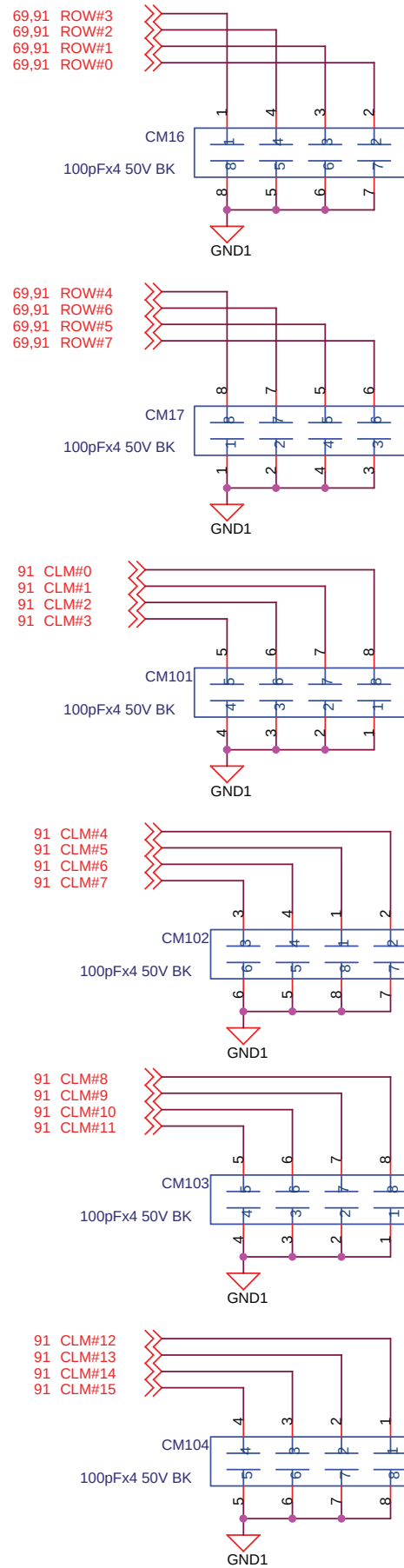
G

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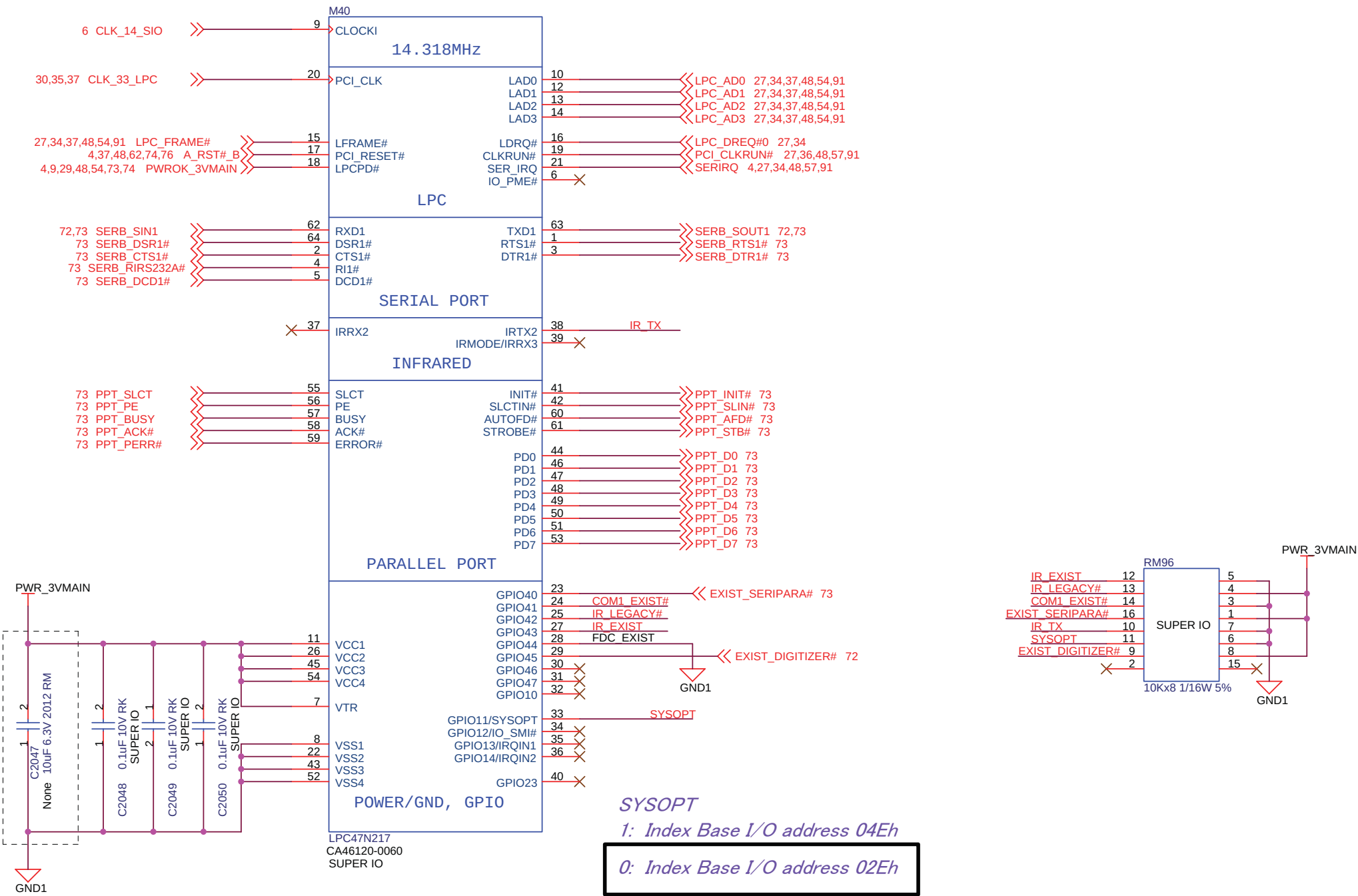
<http://hobi-elektronika.net>

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	ID0	ID1	ID2
OYA	0	0	0
UK	0	0	1
US	0	1	0
JP	0	1	1



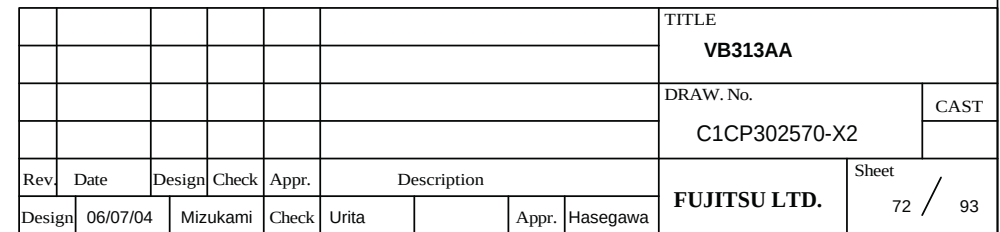
KB/Pointing-CN

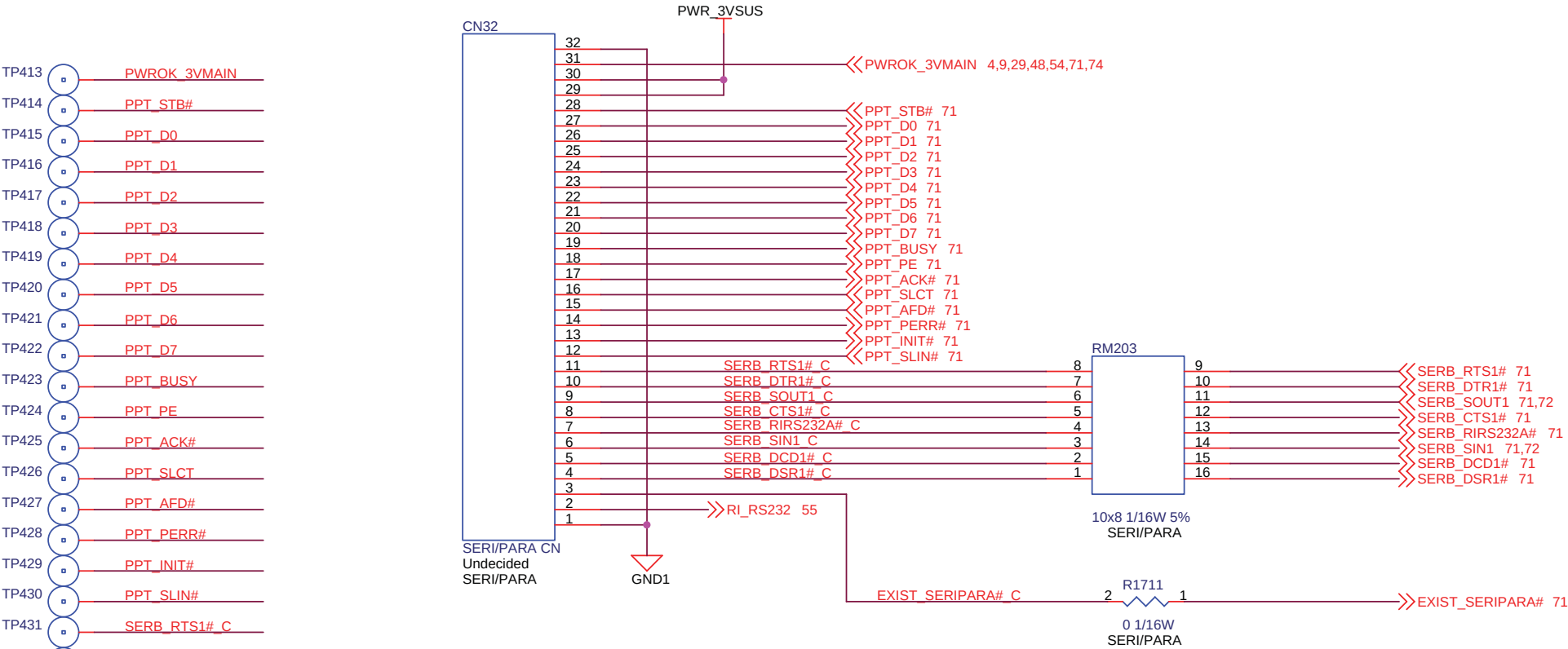
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								VB313AA		
								DRAW. No.	CAST	
								C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet / 93
Design	06/07/04		Mizukami	Check	Urita		Appr.	Hasegawa	70 / 93	



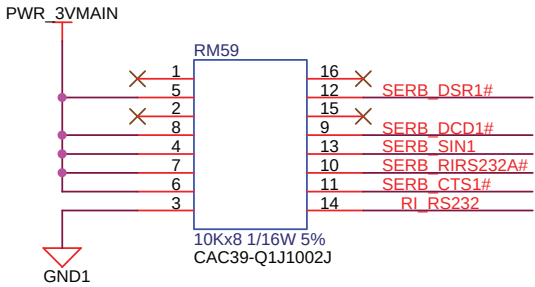
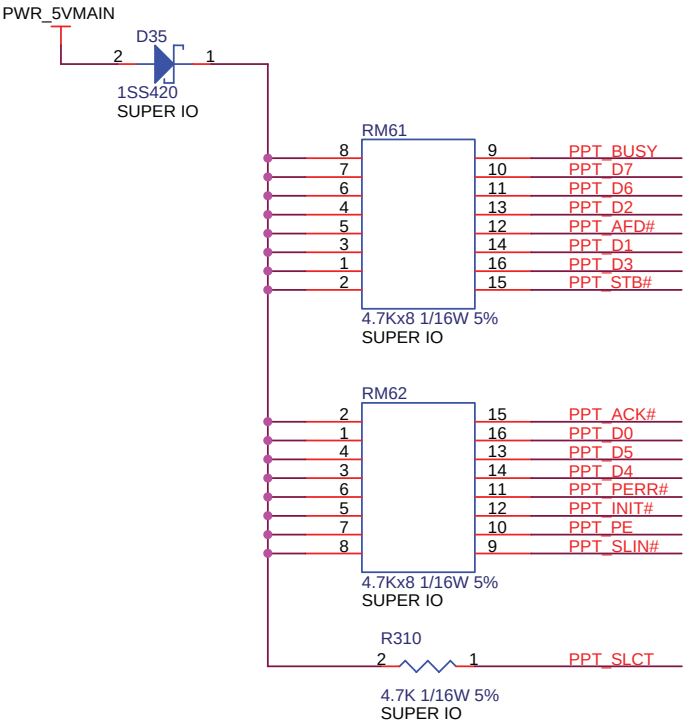
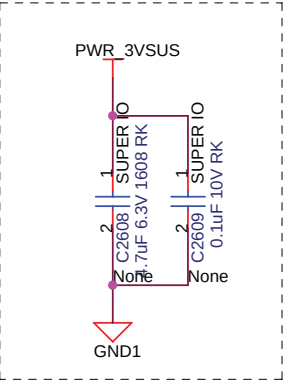
本ページの抵抗・コンデンサはKONA付近に配置すること。

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Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	71 / 93





- TP413 PWROK_3VMAIN
- TP414 PPT_STB#
- TP415 PPT_D0
- TP416 PPT_D1
- TP417 PPT_D2
- TP418 PPT_D3
- TP419 PPT_D4
- TP420 PPT_D5
- TP421 PPT_D6
- TP422 PPT_D7
- TP423 PPT_BUSY
- TP424 PPT_PE
- TP425 PPT_ACK#
- TP426 PPT_SLCT
- TP427 PPT_AFD#
- TP428 PPT_PERR#
- TP429 PPT_INIT#
- TP430 PPT_SLIN#
- TP431 SERB_RTS1#_C
- TP432 SERB_DTR1#_C
- TP433 SERB_SOUT1_C
- TP434 SERB_CTS1#_C
- TP435 SERB_RIRS232A#_C
- TP436 SERB_SIN1_C
- TP437 SERB_DCD1#_C
- TP438 SERB_DSR1#_C
- TP439 EXIST_SERIPARA#_C
- TP440 RI_RS232
- TP441 PWR_3VSUS

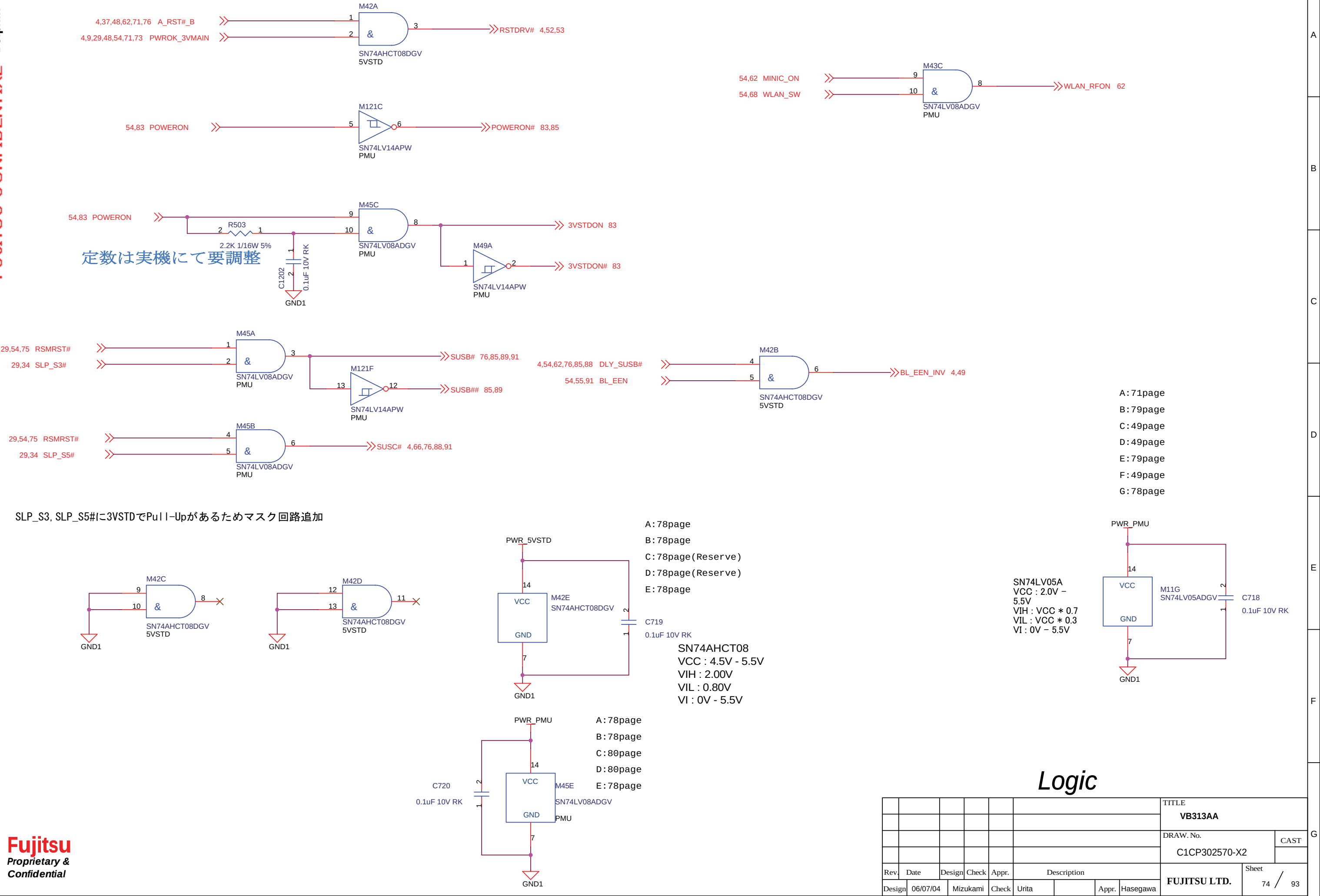


本ページの部品は、I/O-CNの近くに配置すること

04/28
部品追加 : C2608, C2609

PARALLEL/SERIAL CN

					TITLE			
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					DRAW. No.			CASE
					C1CP302570-X2			
Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	73 / 93



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Dolphin

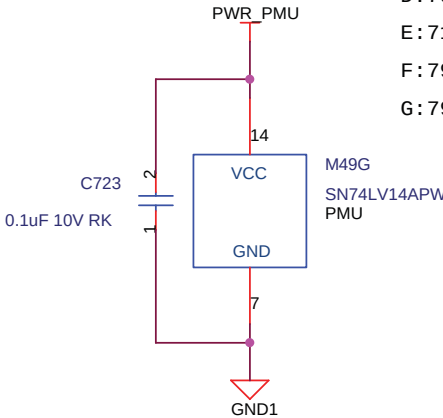
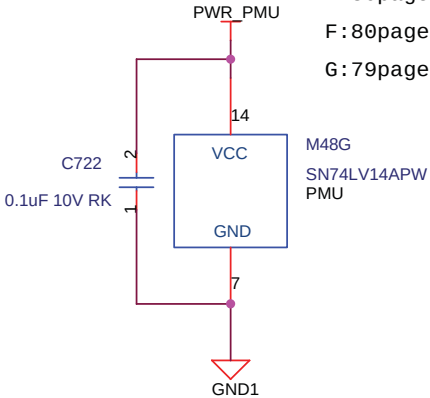
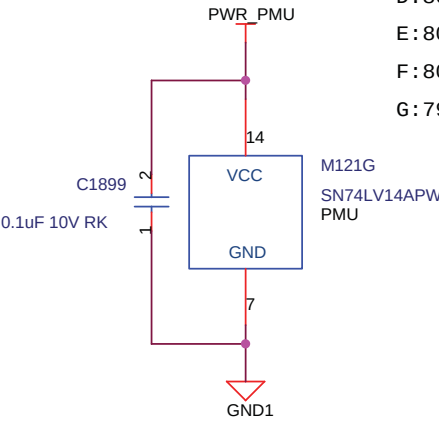
PWR_3VSUS to BENN_SUSOK
Default 50ms

PWR_3VMAIN to BENN_MAINOK
Default 170ms

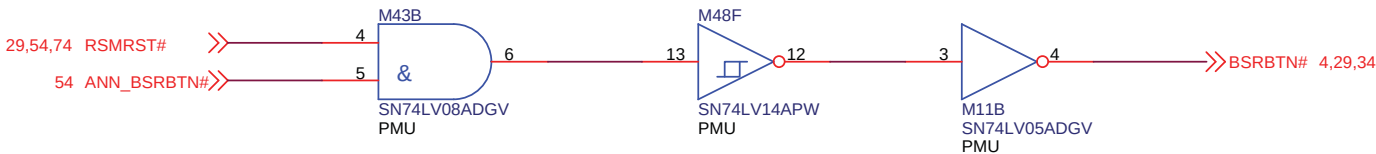
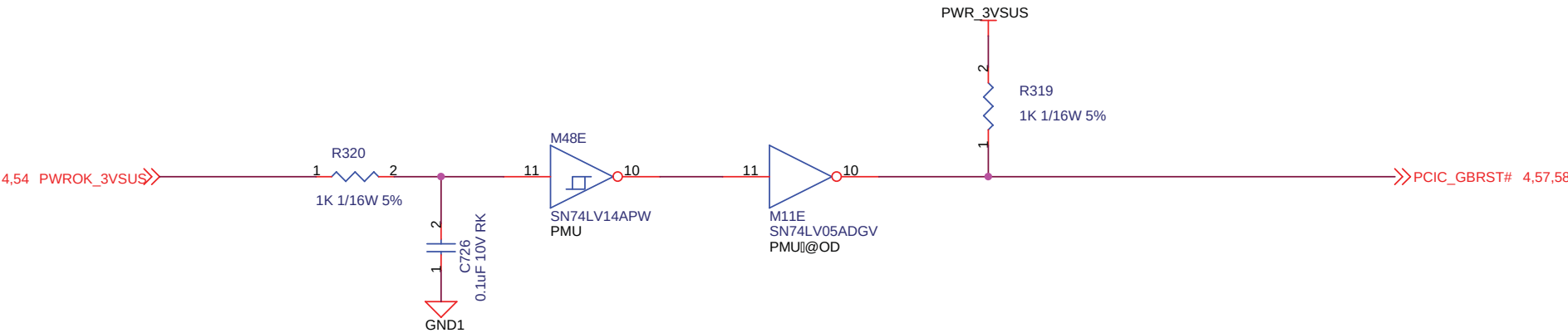
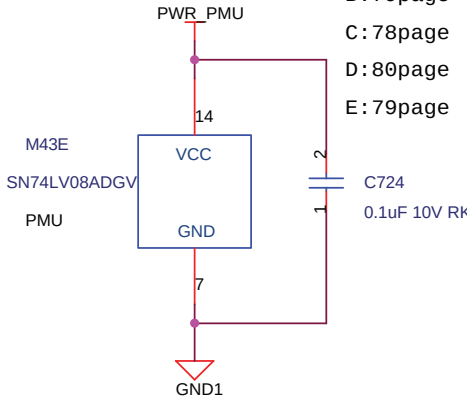
A: 80page
B: 80page
C: 80page
D: 80page
E: 80page
F: 80page
G: 79page

A: 80page
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E: 80page
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C: 80page
D: 79page
E: 71page
F: 79page
G: 79page



A: 79page
B: 79page
C: 78page
D: 80page
E: 79page



遅延ターゲット
BD5327G:
 $T_{plh}(s) = 0.69(TYP) \times 9(M\Omega) \times CT(F)$

RESET IC

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						TITLE		
						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD. 75 / 93



Falcon Power Supply

Caution

Features

- 1/ Voltage Regulator for AMD K8 Rev.F Processor
- 2/ ATI RS480M Chipset
- 3/ DDR2 Memory
- 4/ Internal VGA (PowerPlay is not supported)
- 5/ Normal Speed Charger
- 6/ 19V AC Adaptor
- 7/ A circuit reducing a rush current from AC adaptor
- 8/ Internal Battery with 4 or 3 Seirial cells and Digital Interface

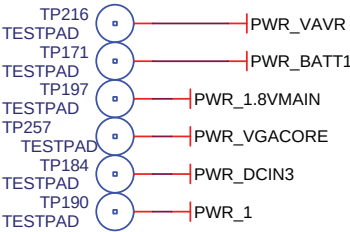
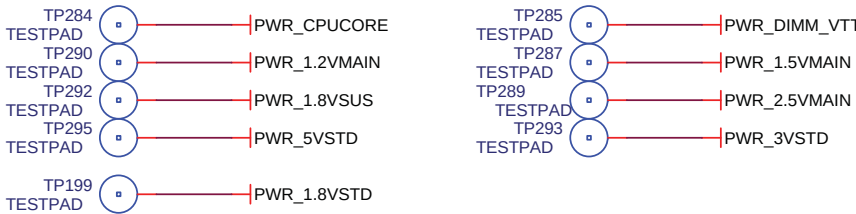
Voltage Regulator Spec.

DDC	CPUCore	TBD	35A	typ/peak
	1.2VMain	1.200V +/-5% (1.140V-1.260V)	6A	typ / 8Apeak
	1.8VSus	1.800V +/-5% (1.710V-1.890V)	6A	typ / 8Apeak
	3VStd	3.300V +/-5% (3.135V-3.465V)	6A	typ / 8Apeak
	5VStd	5.000V +/-4% (4.800V-5.200V)	6A	typ / 8Apeak
Charger	CV 3-serial 12.60V +/-1.2% (12.45V-12.75V)CC 1.33A			
	CV 4-serial 16.80V +/-1.2% (16.60V-17.00V)CC 1.33A			
LDO	DimmVtt	0.900V +/-100mV (0.800-1.000V)	+/-0.25A typ / +1Apeak	
	1.5VMain	1.500V +/-5% (1.425V-1.575V)	1A	
	1.8VStd	1.800V +/-5% (1.710V-1.890V)	0.3A	
	2.5VMain	2.500V +/-5% (2.375V-2.625V)	40mA	
	VAVR	3.300V +/-2% (3.234V-3.366V)	30mA	

Power Contents

Contents		Page#	Contents		Page#
DDC	TopPage	82	Node	DCIn,Battery	91
	Delivery	83		Switch1	92
	CPUCore	84		Switch2	93
	(reserved)	85	PMU	LUNA1 (PMU part)	94
	1.05V/1.8V	86		LUNA2 (KBC part)	95
LDO	3.3V/5V	87		Etc0 (Common)	96
	(reserved)	88		Etc1 (Battery1)	97
	Charger	89			
		90			

TestPad (for SFJ)

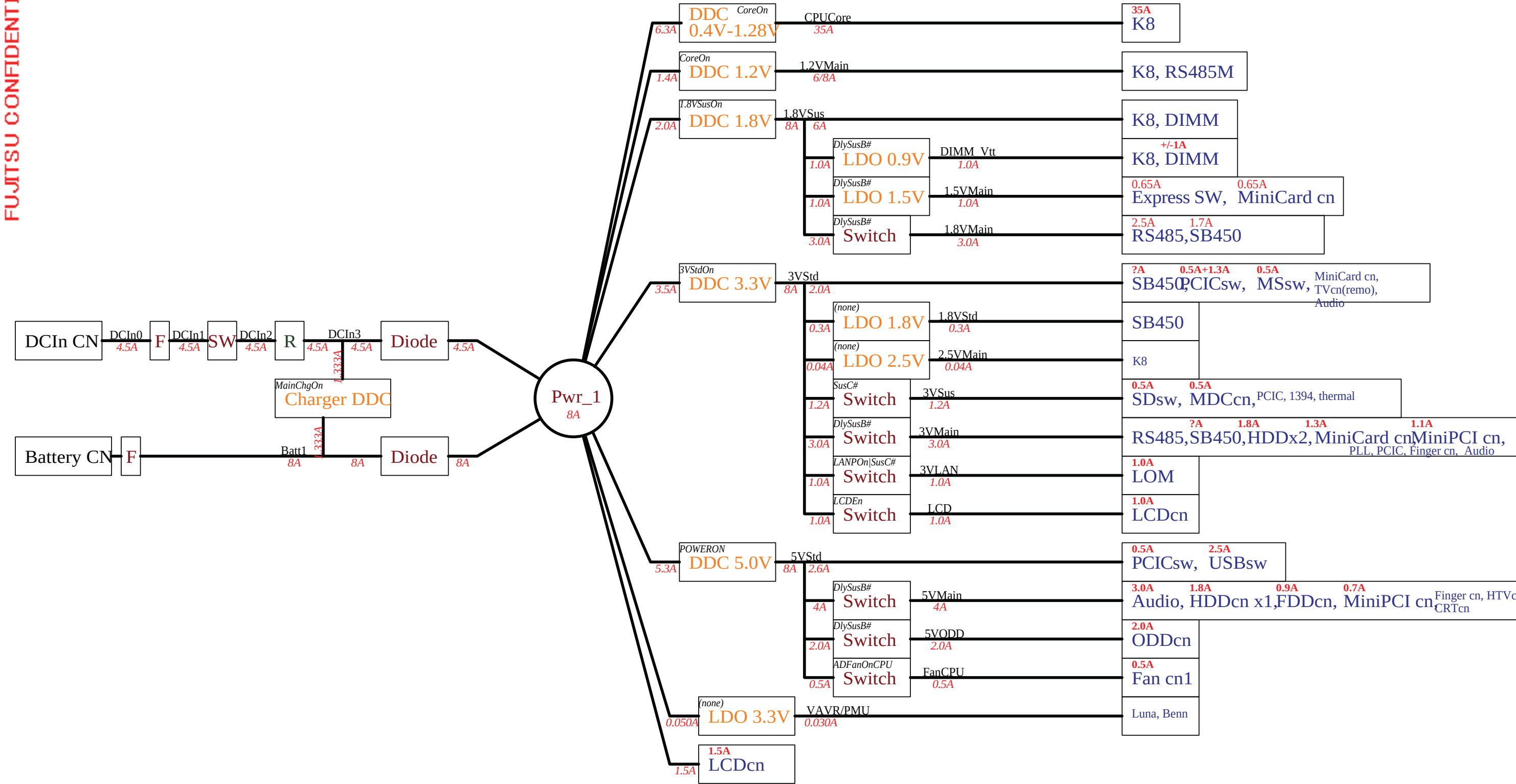


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Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	77 / 93

Dolphin

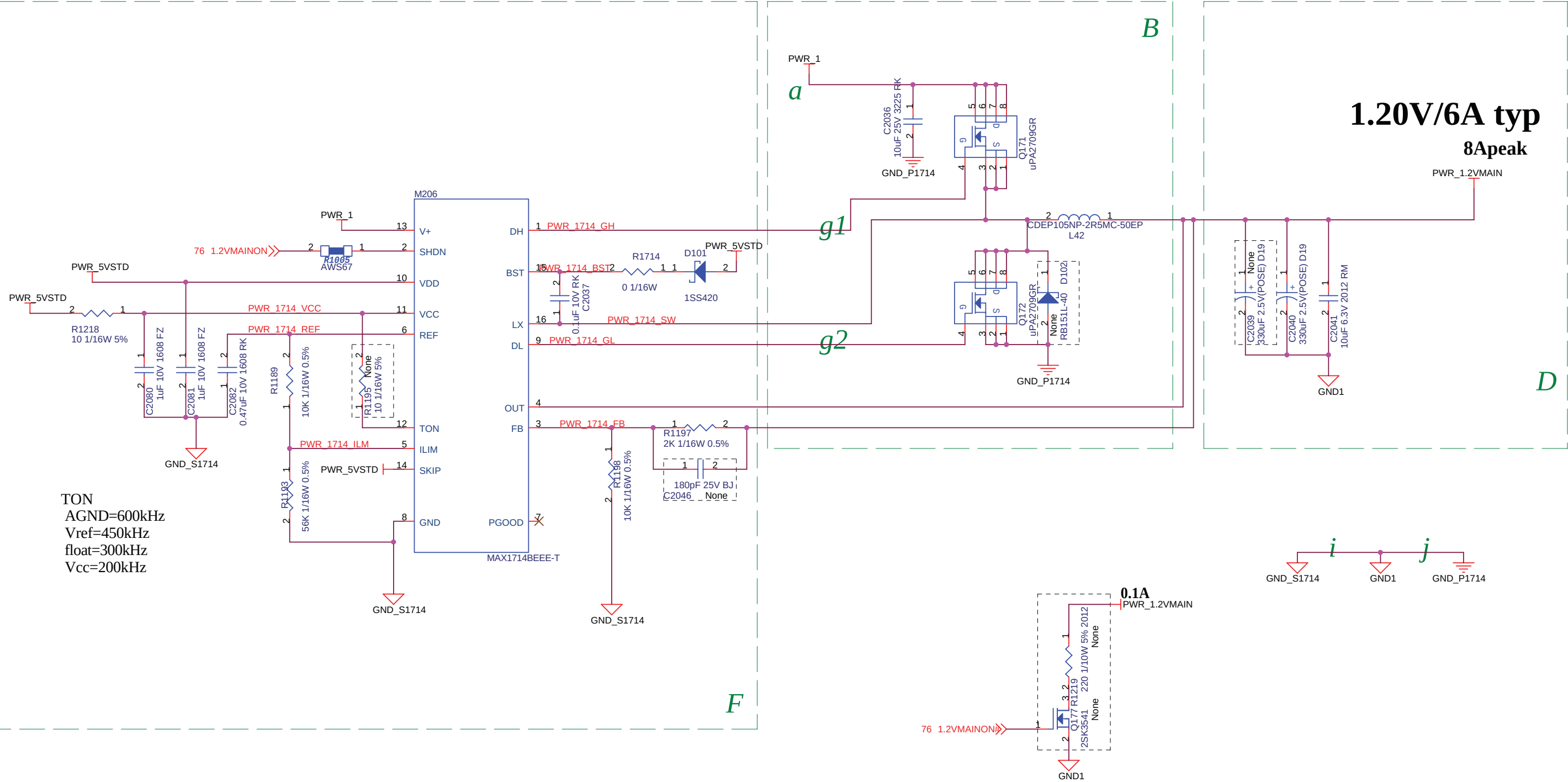
Power Delivery

FUJITSU CONFIDENTIAL



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Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	78 / 93

									TITLE	
									VB313AA	
									DRAW. No.	CAST
									C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	79 / 93		

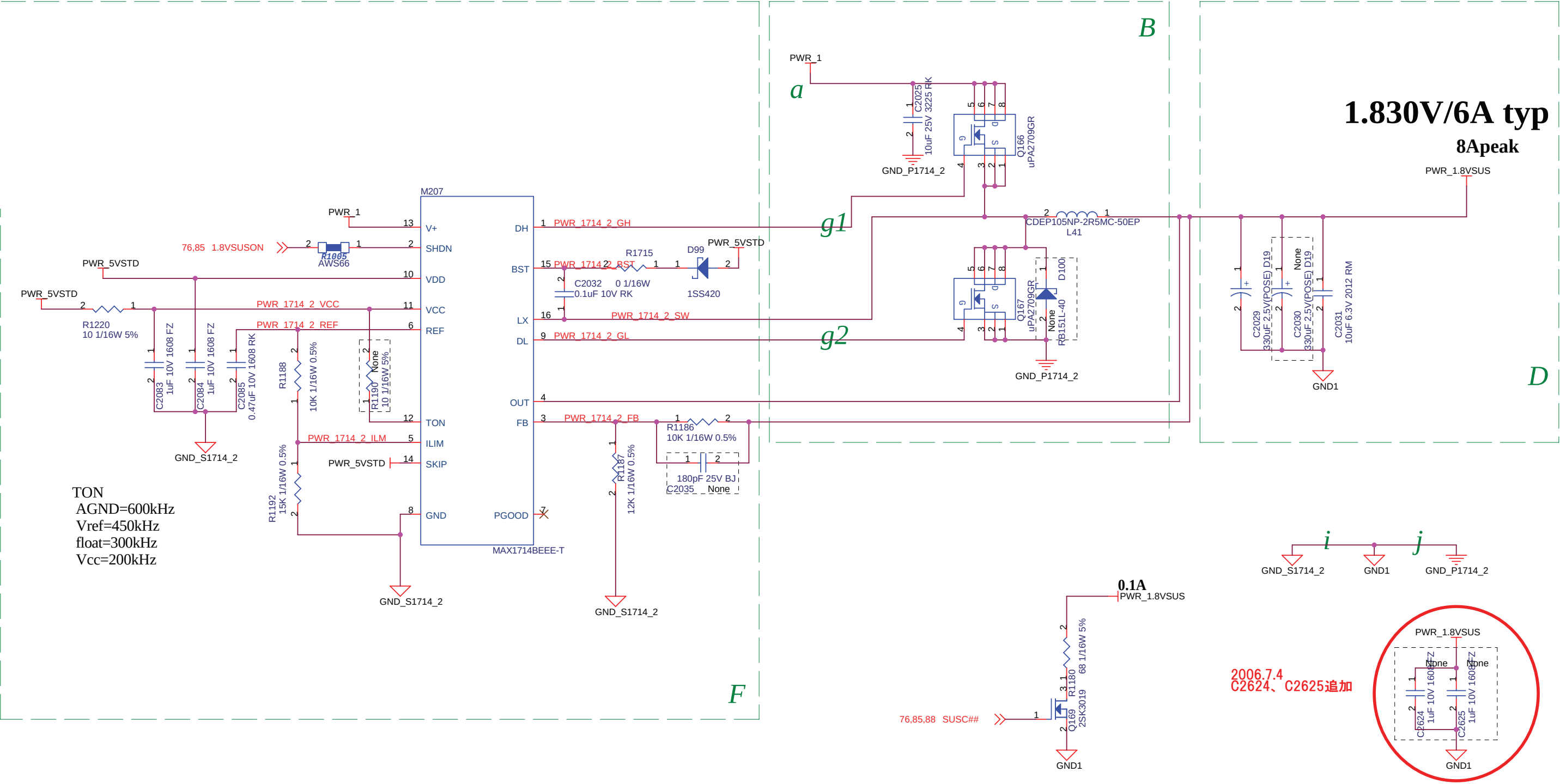


Power/ DDC/ 1.2VMAIN

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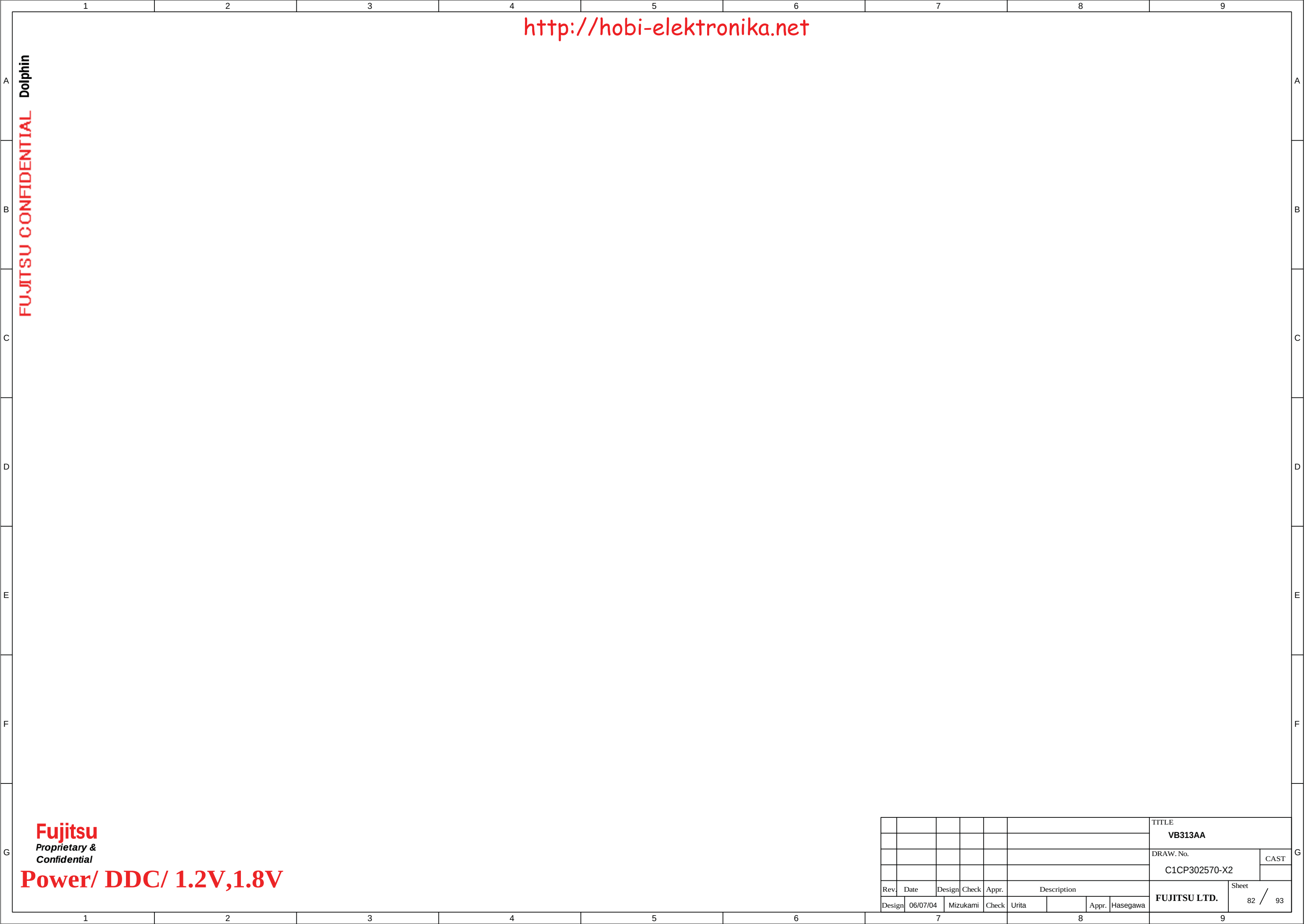
Power/ DDC/ VGA

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Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	80 / 93		



Power/ DDC/ 1.8VSus

									TITLE	
									VB313AA	
									DRAW. No.	CAST
									C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	81 / 93		



http://hobi-elektronika.net

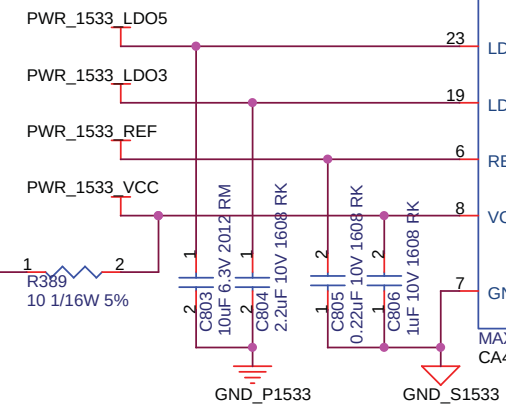
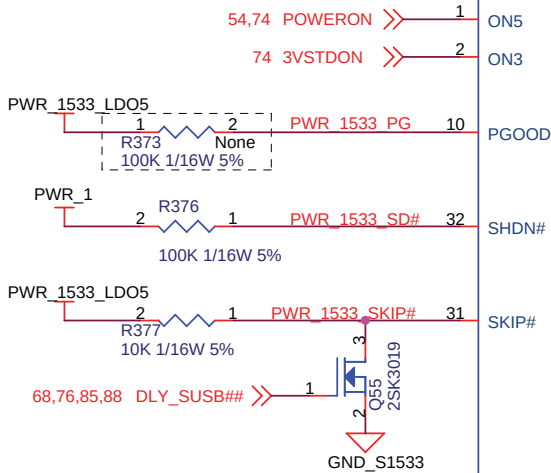
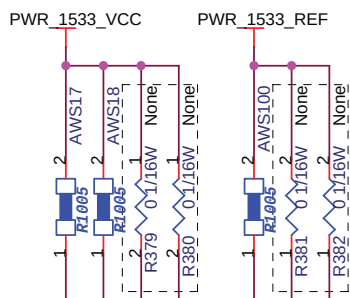
FUJITSU CONFIDENTIAL

Dolphin

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Proprietary & Confidential
Power/ DDC/ 1.2V,1.8V

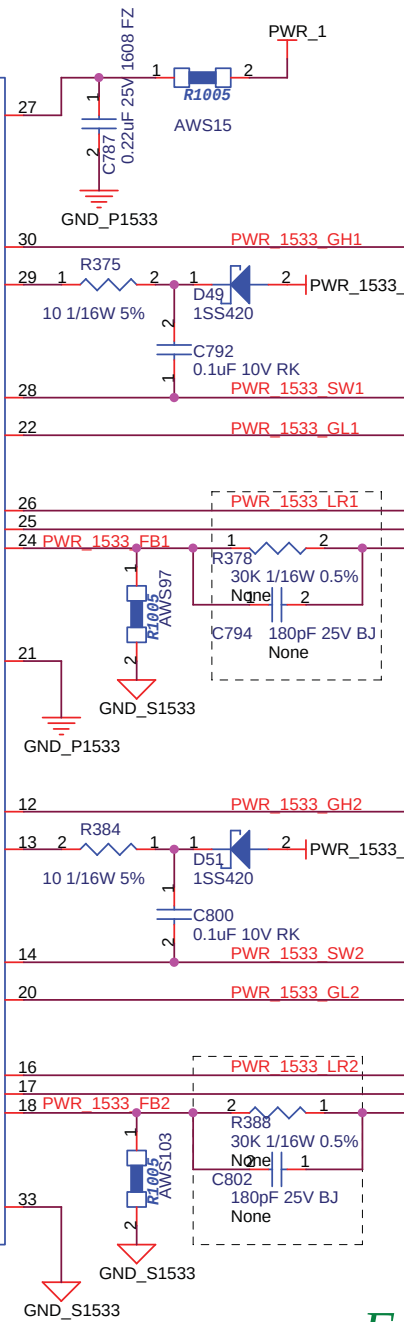
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						VB313AA			
						DRAW. No.			CAST
						C1CP302570-X2			
Rev.	Date	Design	Check	Appr.	Description		Fujitsu Ltd.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	82 / 93	

Frequency Select: FSEL(3pin)
VCC=500kHz
REF=300kHz
GND=200kHz
I Limit: ILIM(4,5pin)
VCC=75mV
or
V(ILIM)/10 V
(50mV-200mV)
Under/Over Voltage Protection:
OVP#(15pin)/UVP#(11pin)
H=disable
L=enable

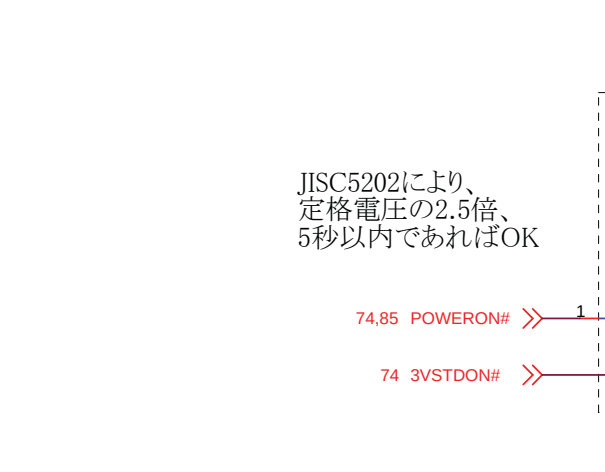
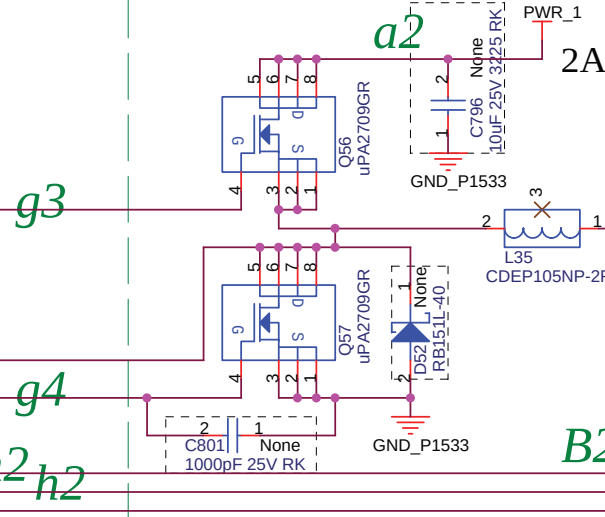
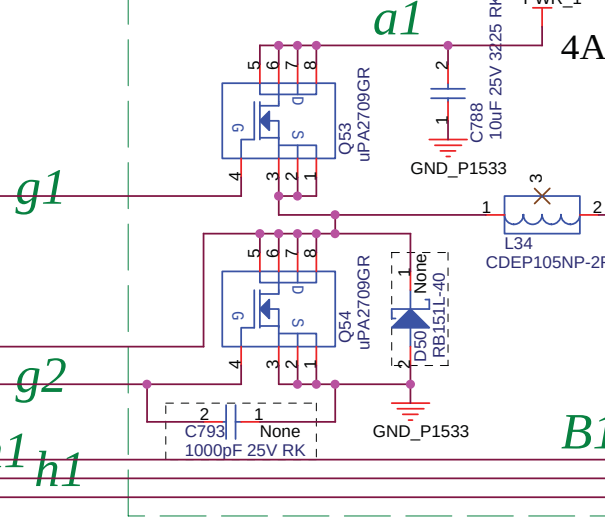
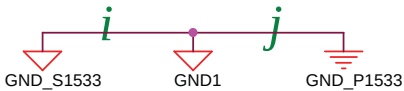


MAX1533

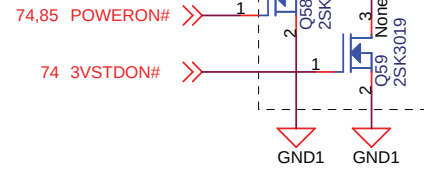
MAX1533A
CA46710-0076



F



JISC5202により、
定格電圧の2.5倍、
5秒以内であればOK

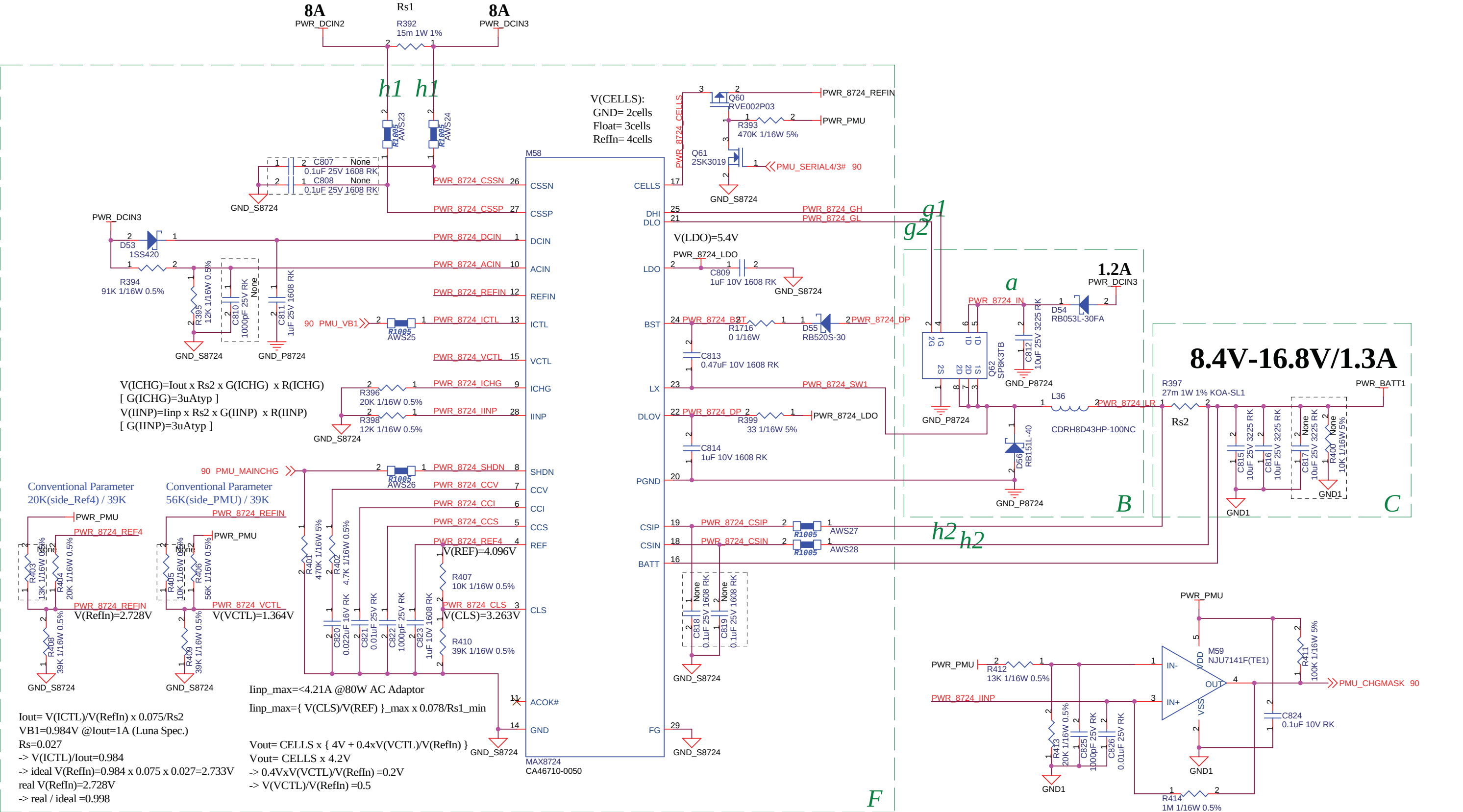


5.025V/6A typ
8Apeak

3.324V/6A typ
8Apeak

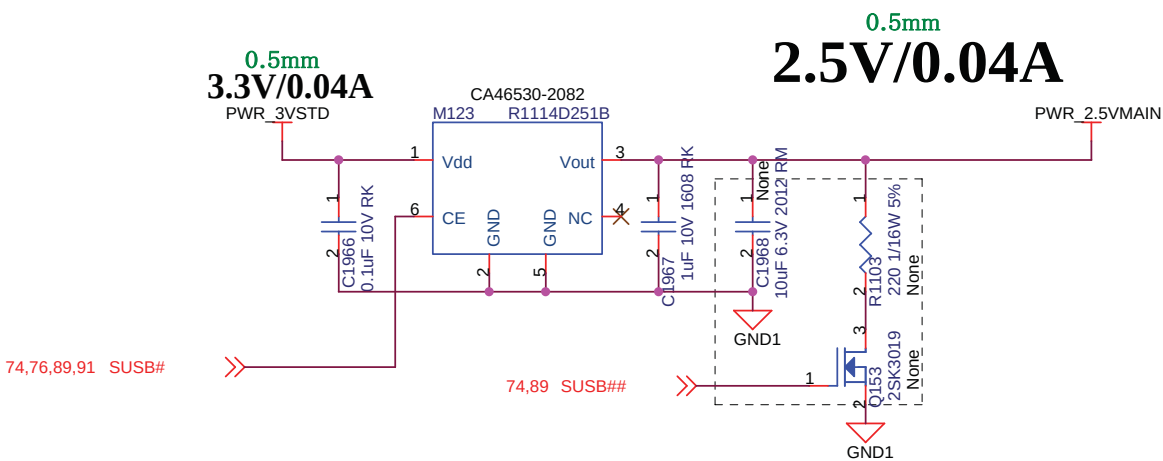
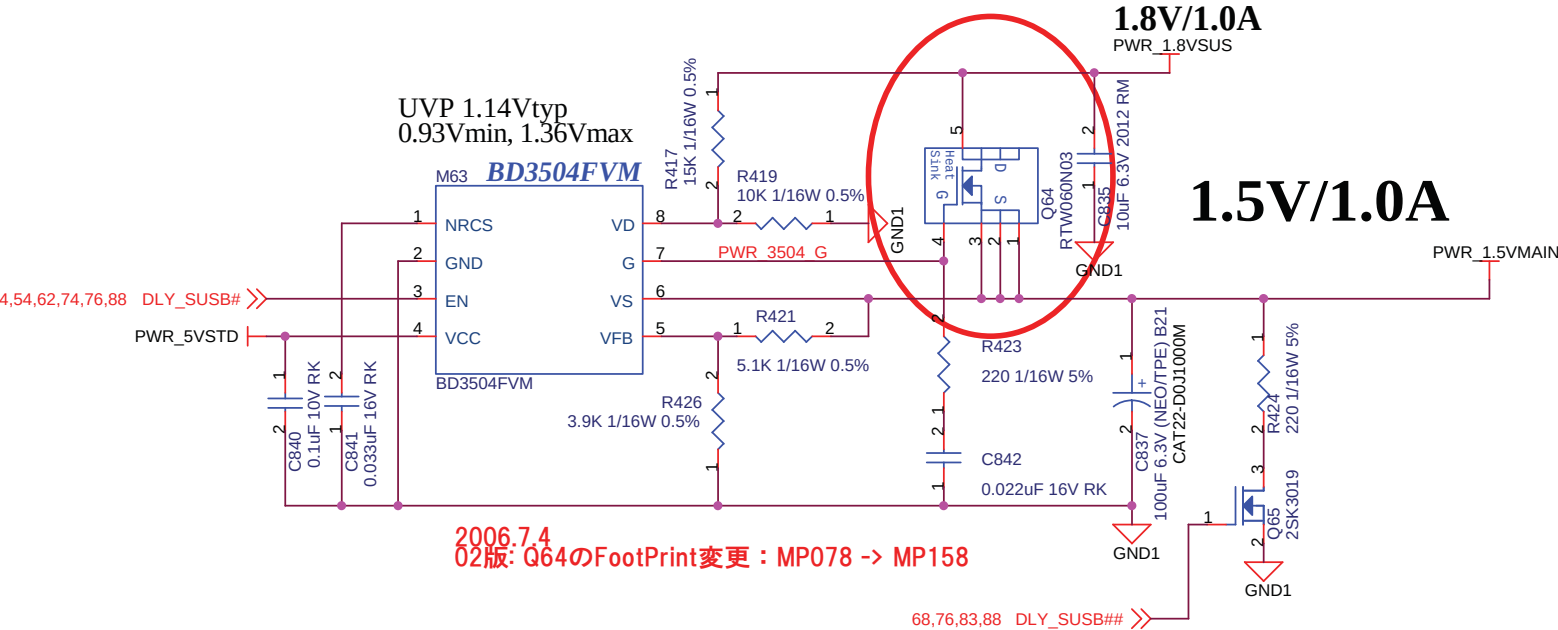
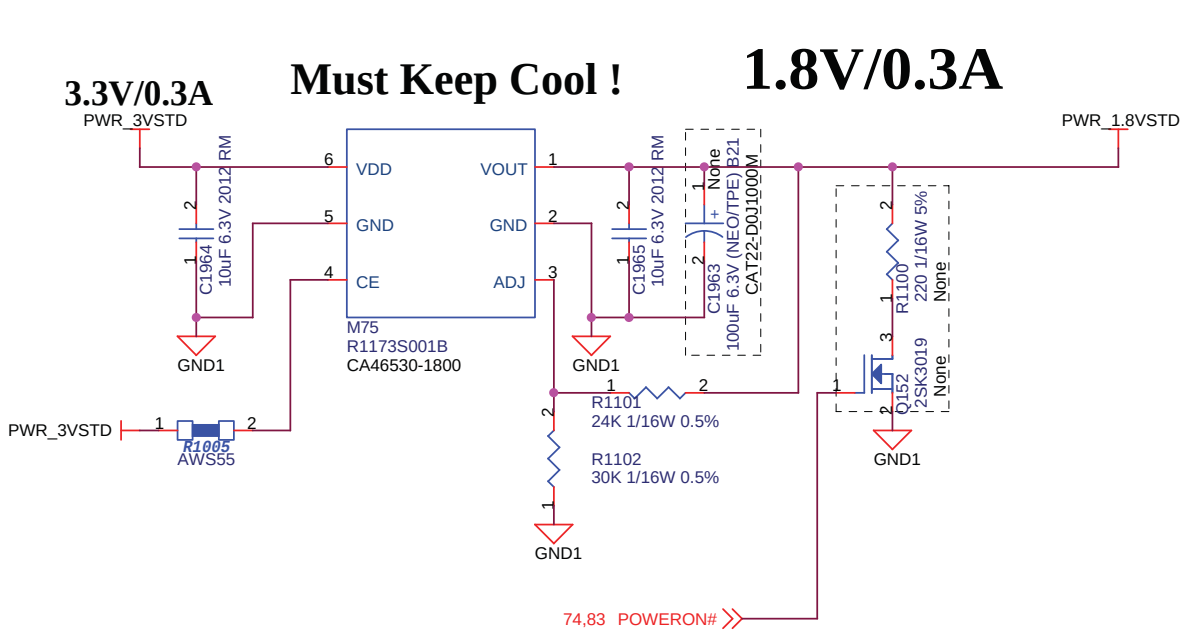
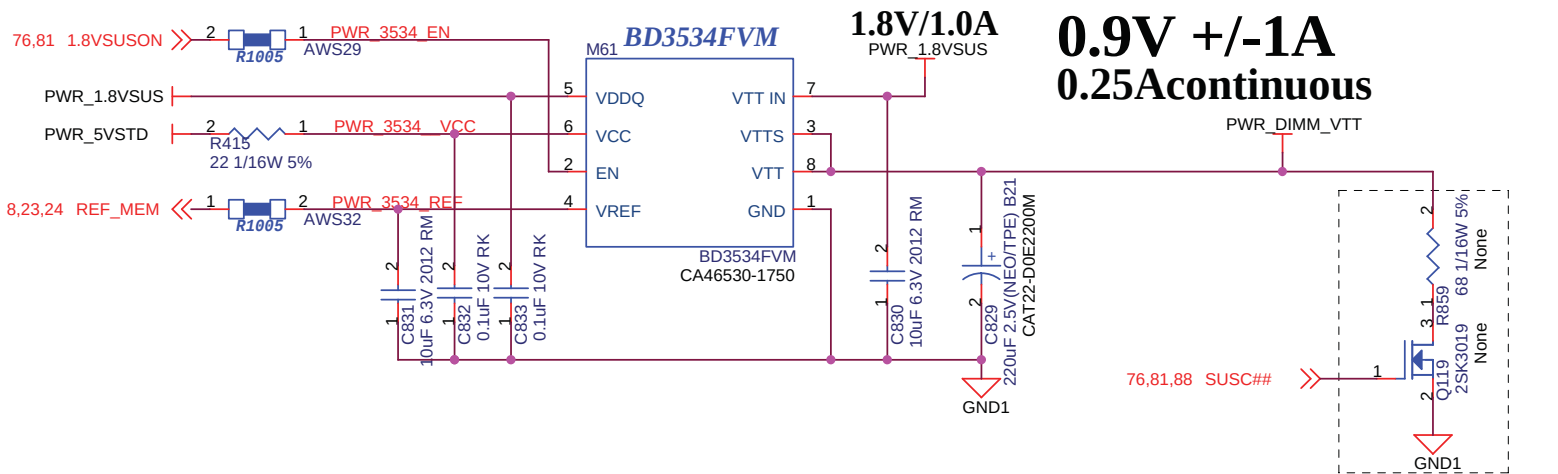
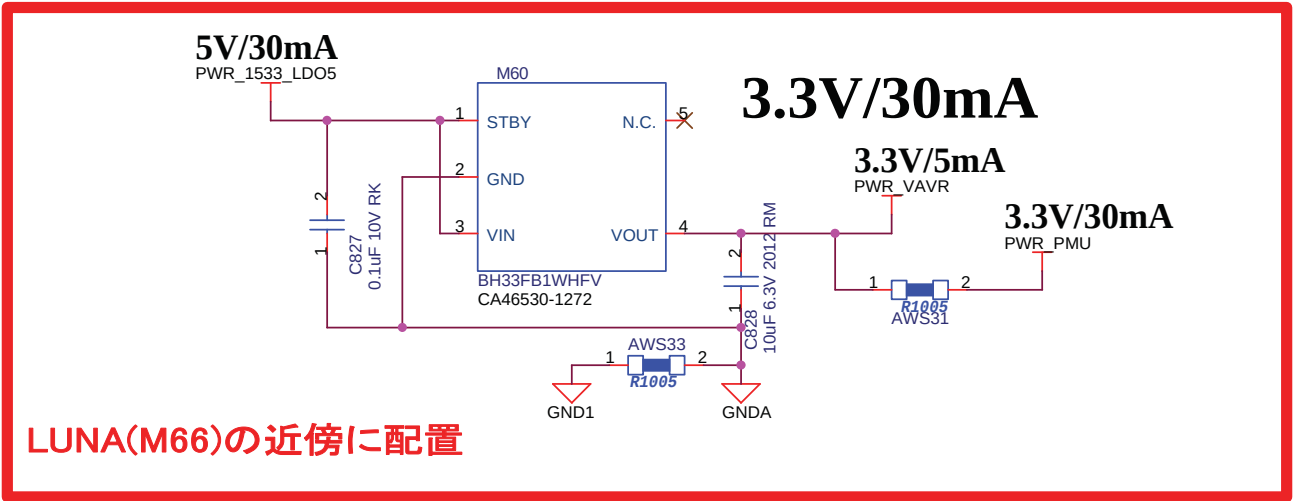
Fujitsu
Proprietary &
Confidential
Power/ DDC/ 3.3V,5V

								TITLE	
								VB313AA	
								DRAW.No.	CAST
								C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.	Sheet
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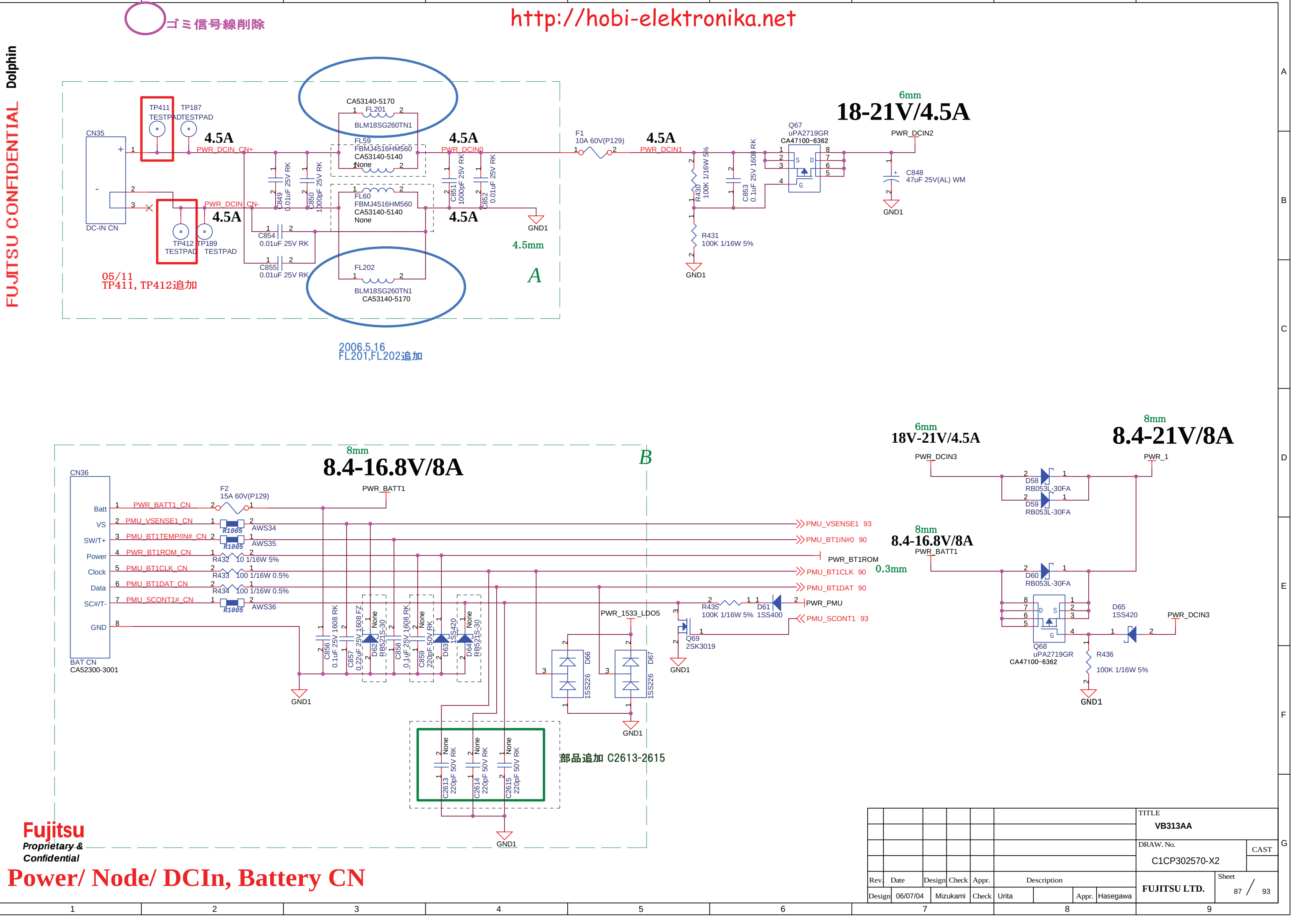
↑ 64Wアダプタ設定
2006. 05. 31
ACアダプタ80W化に伴う変更
R398: 12k -> 10K
R407: 12k -> 10K
R410: 20k -> 39K

					TITLE				
					VB313AA				
					DRAW. No.				CAST
					C1CP302570-X2				
Rev.	Date	Design	Check	Appr.	Description				
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD.	Sheet 84 / 93

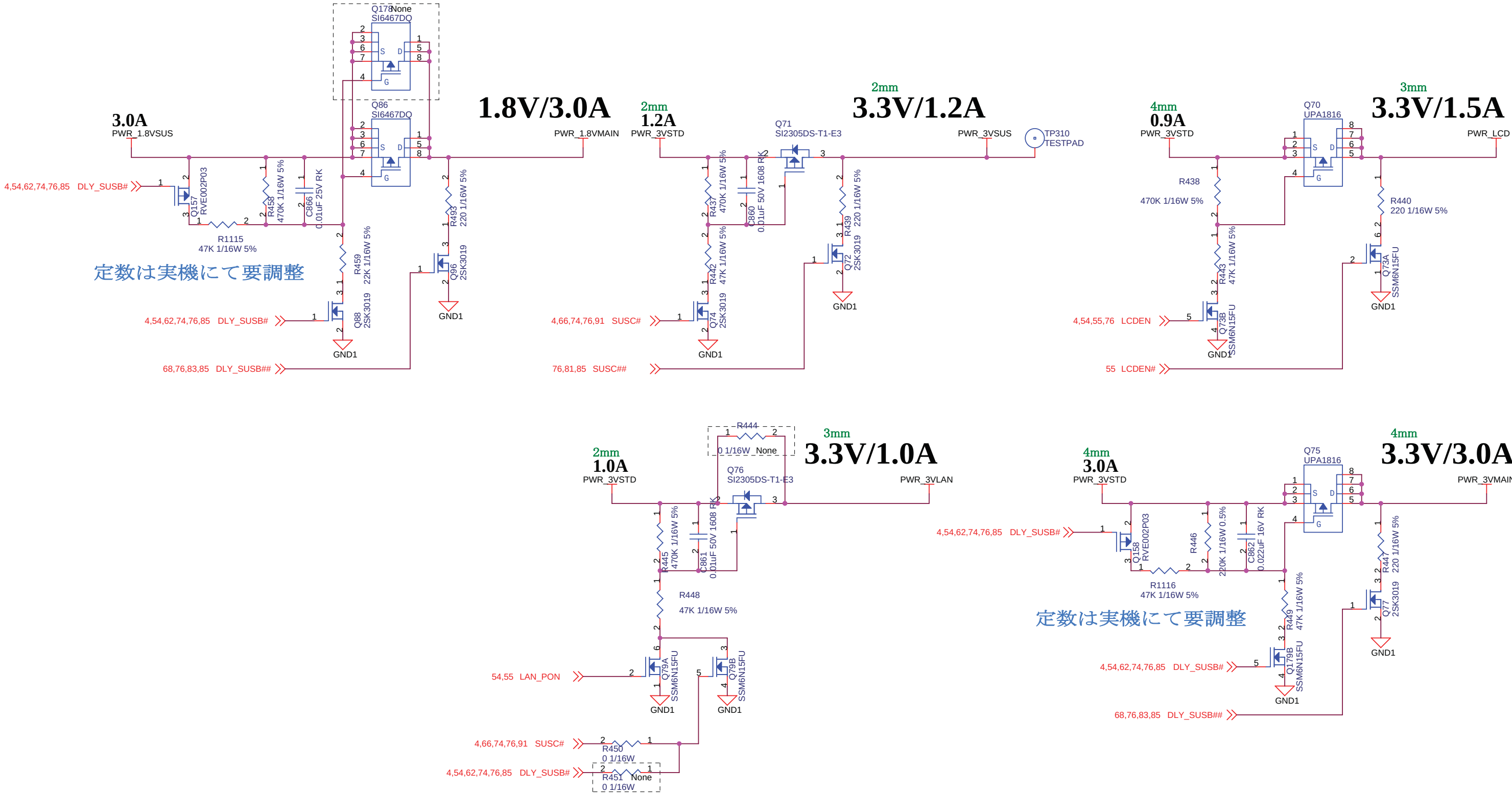


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Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr. Hasegawa	FUJITSU LTD.	
							85 / 93	

1		2		3		4		5		6		7		8		9	
http://hobi-elektronika.net																	



FUJITSU CONFIDENTIAL Dolphin

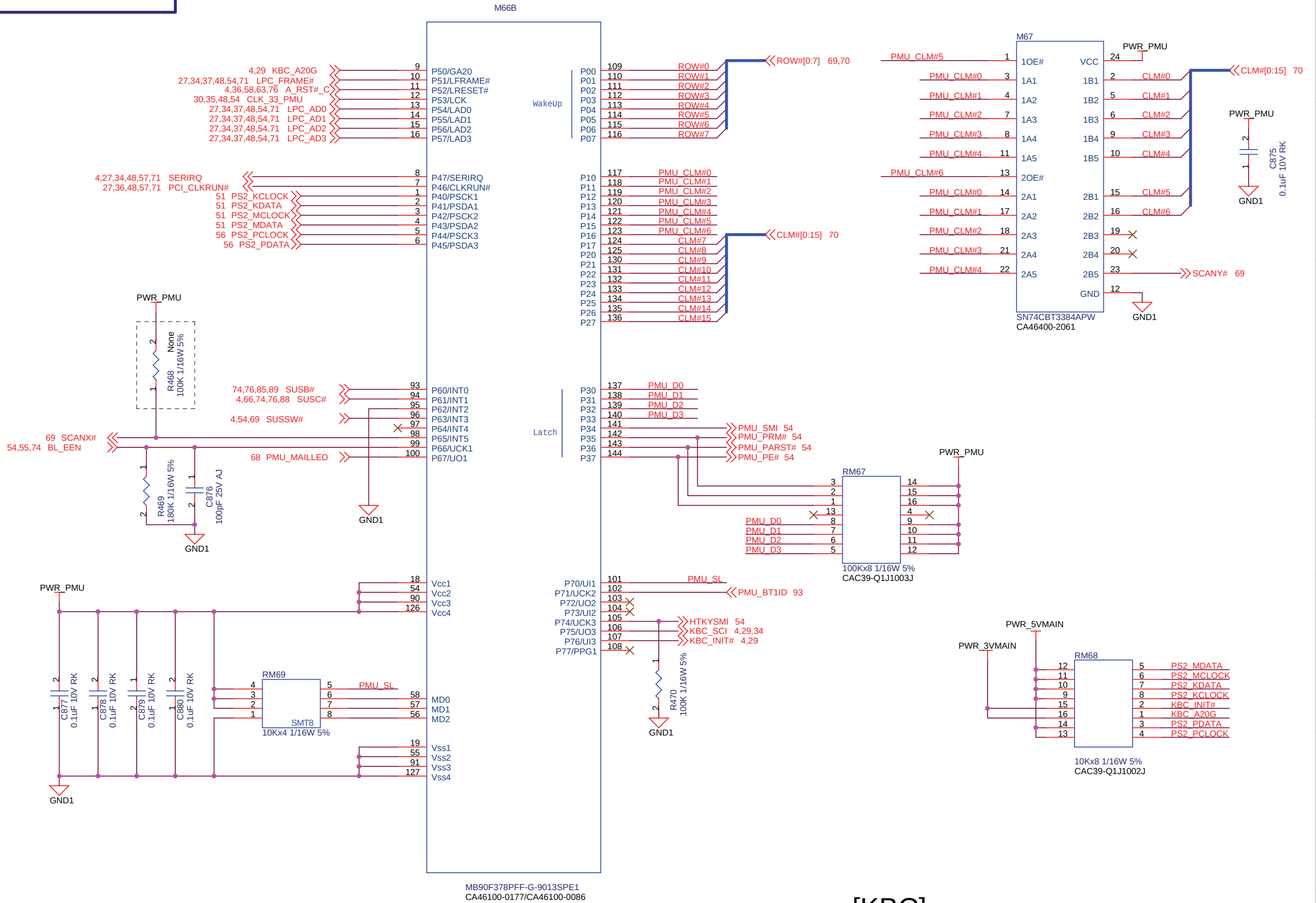


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Rev.	Date	Design	Check	Appr.	Description					Sheet	
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa	FUJITSU LTD.	88 / 93	



								TITLE		
								VB313AA		
								DRAW. No.	CAST	
								C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	90 / 93		

<http://hobi-elektronika.net>

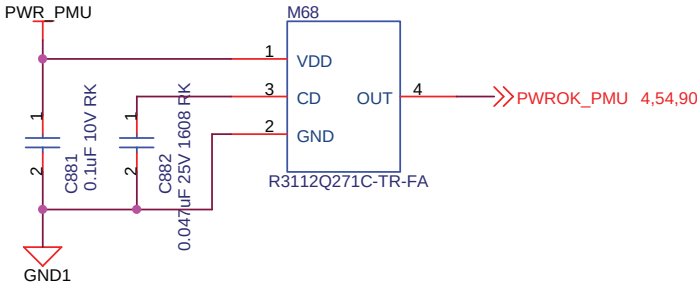
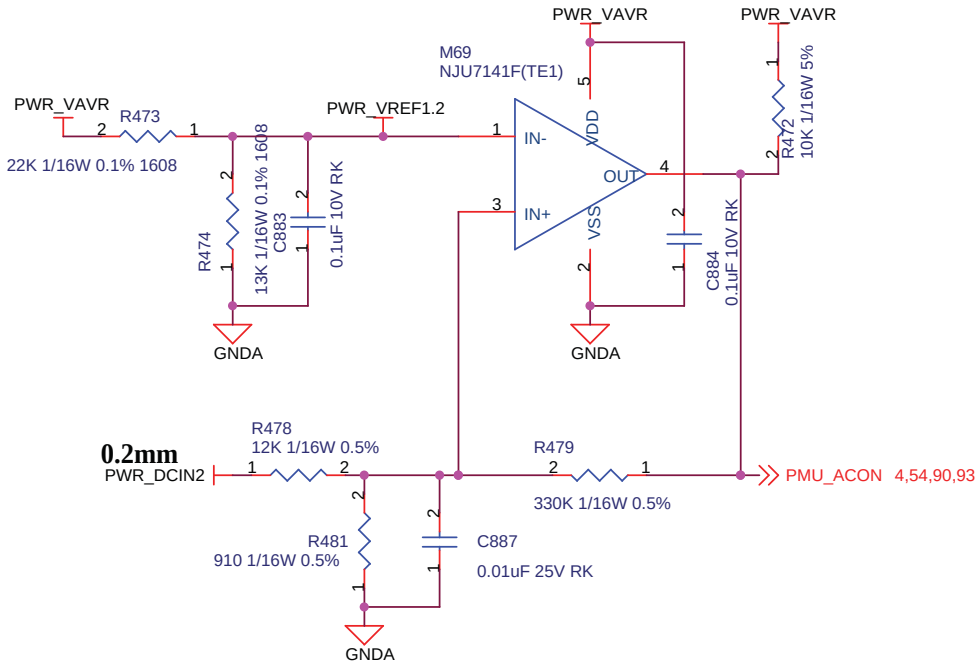


本ページの抵抗・コンデンサはM38867付近に配置すること。
 パスコンについてはM38867の電源ピンに対して均等になるように配置分散し、
 電源ピンまでのリード長を最大限短くなるようレイアウトすること。

[KBC]

									TITLE	
									VB313AA	
									DRAW. No.	
									CAST	
									C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description					
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa	FUJITSU LTD.	Sheet 91 / 93

FUJITSU CONFIDENTIAL Dolphin



Target 200ms
遅延ターゲット
R3112N271C-TR:
 $T_{plh}(s) = 0.69(TYP) \times 6.5(M\Omega) \times CT(F)$

A
LUNA近傍に配置

						TITLE	
						VB313AA	
						DRAW. No.	CAST
						C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description	Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa
FUJITSU LTD.						92 /	93

