

LA-2251

Compal confidential

Schematics Document

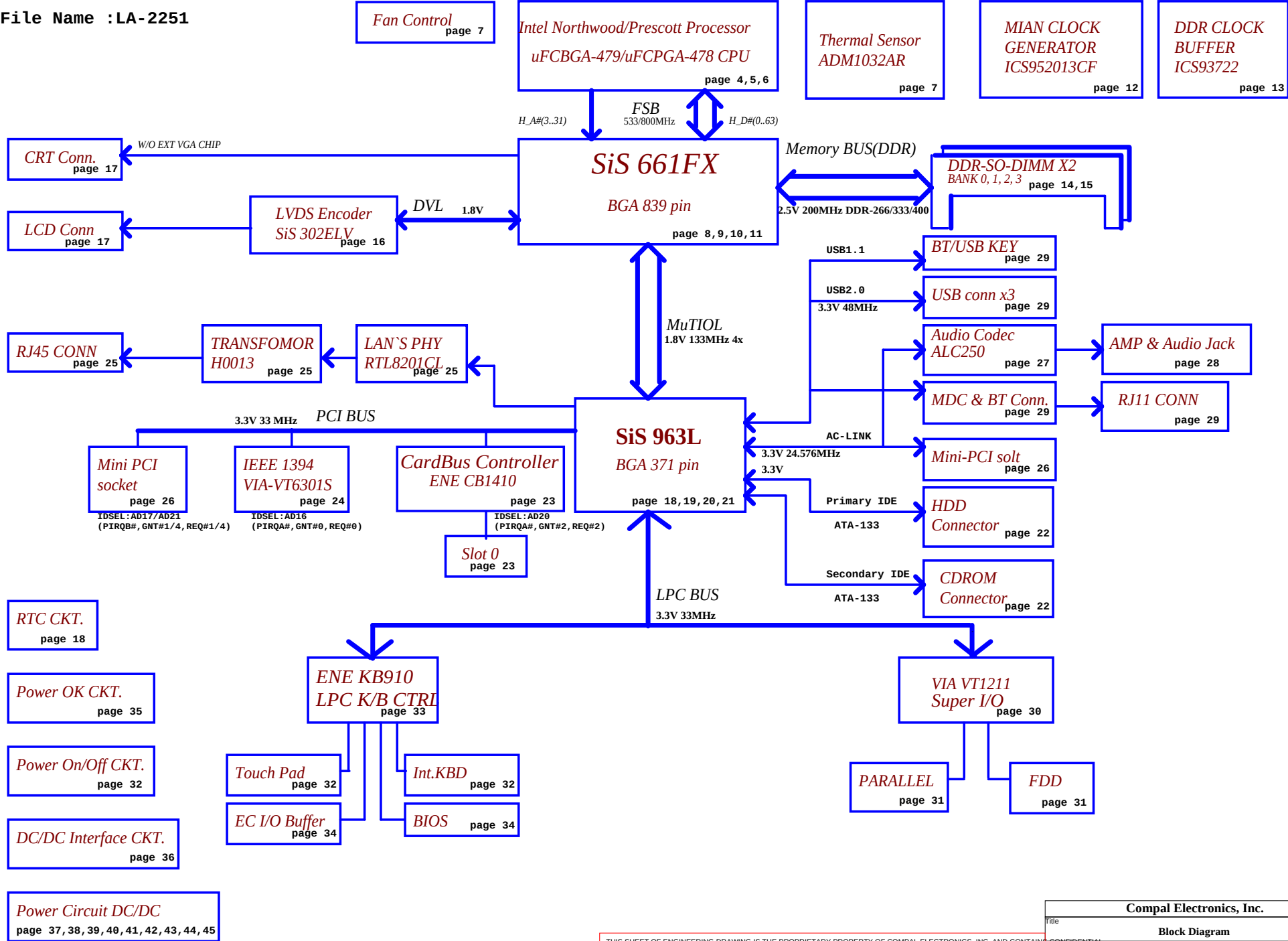
DT TRANSPORT or Prescott uFCPGA
with Sis661FX+Sis963L core logic

2004-05-17

REV:1.0

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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.2V	The voltage(1.2V) for Processor VID select	ON	OFF	OFF
+1.25VS	1.25V switched power rail for DDR Vtt	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON*	ON*
+1.8VS	1.8V switched power rail for SIS M661FX NB.	ON	OFF	OFF
+2.5V	2.5V system power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail for DDR Clock Buffer	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
NB Internal VGA	N/A	N/A	A
AGP BUS	AGP_DEVSEL	N/A	A
SOUTHBRIDGE	AD13 (INT.)	N/A	N/A
USB	AD14 (INT.)	N/A	E/F/H
AC97	AD13 (INT.)	N/A	C
ATA 100	AD13 (INT.)	N/A	A
ETHERNET	AD15 (INT.)	N/A	D
1394	AD16	0	A
LAN	AD19	3	D
CARD BUS	AD20	2	A
Wireless LAN(MINI PCI)	AD17/AD21	1/4	B

 Note: PLACE CLOSE TO M661FX,
USE 10/10 WIDTH/SPACE

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

FIR@ : means just build when FIR Module build in .

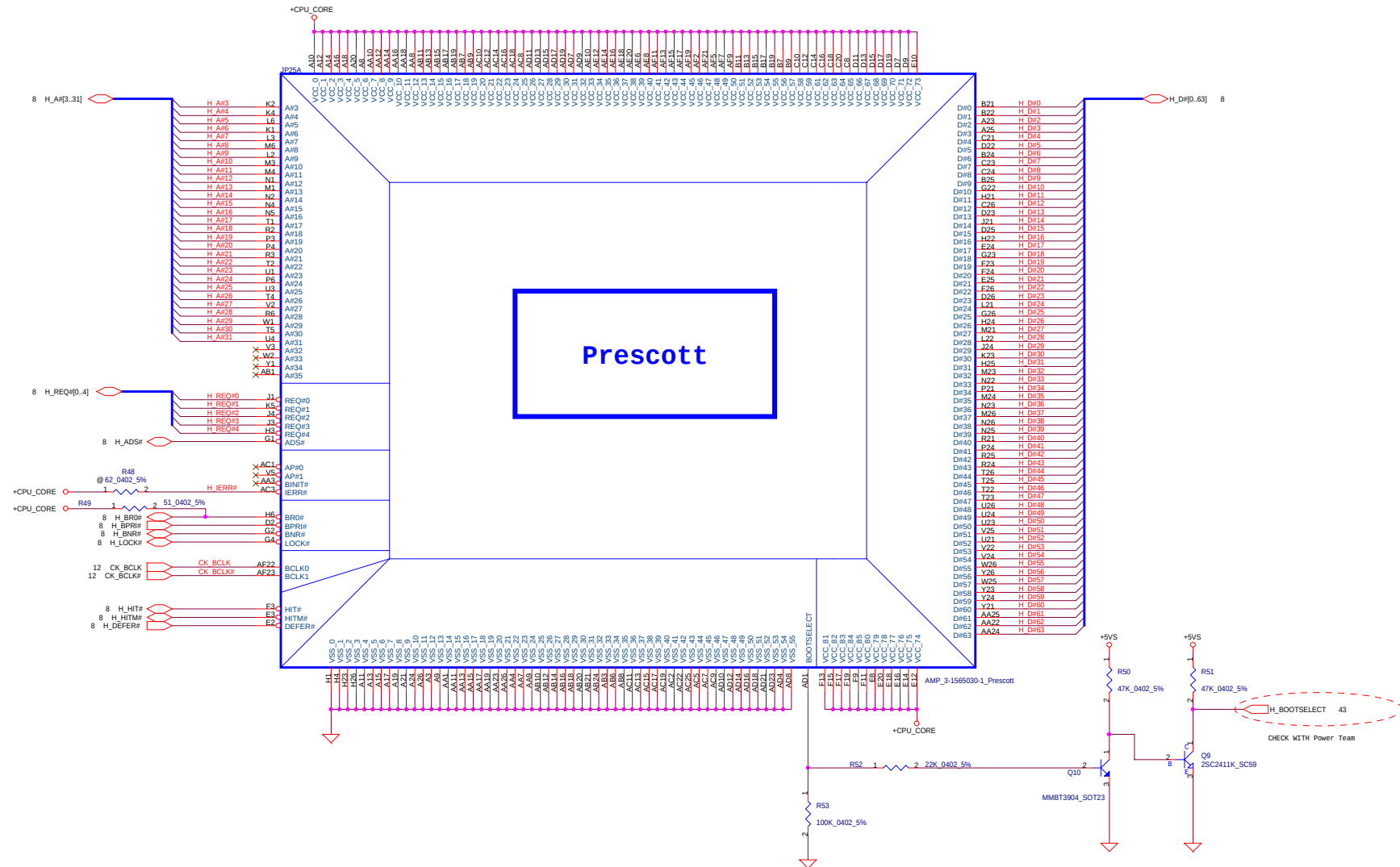
Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

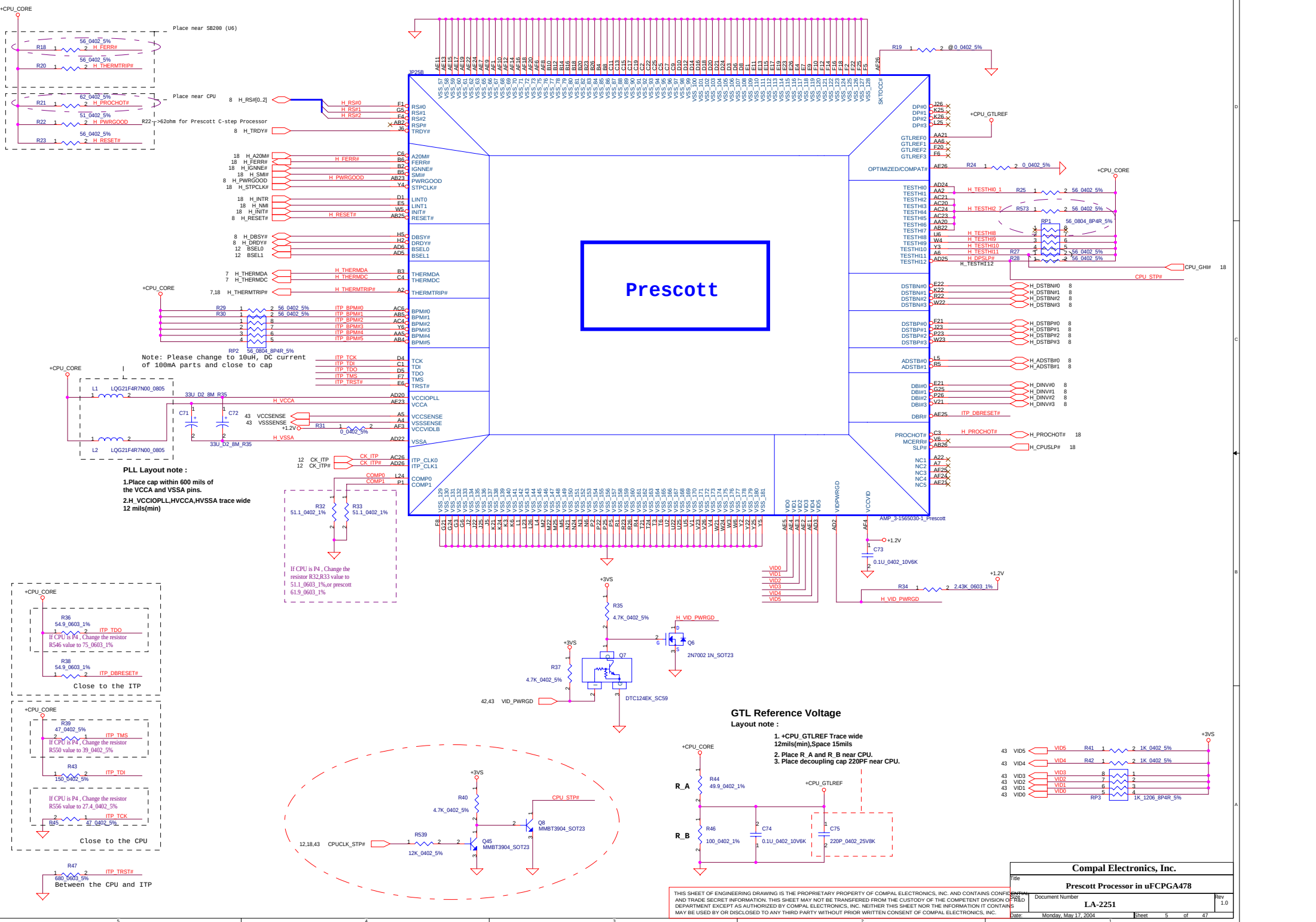
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

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Prescott

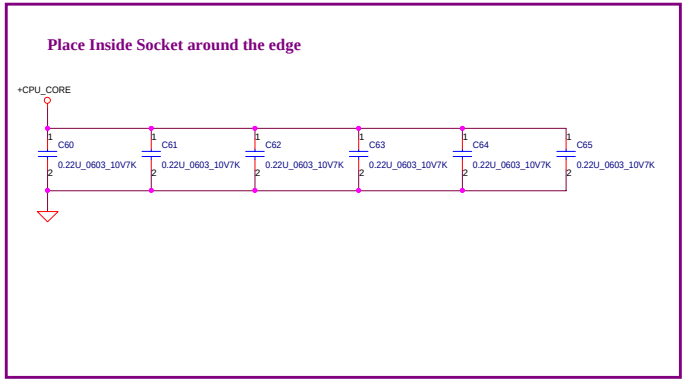
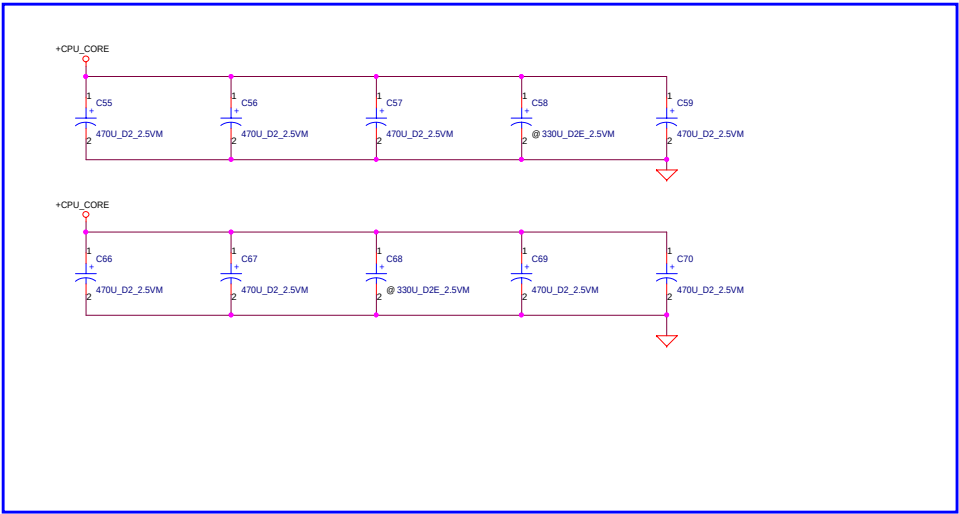
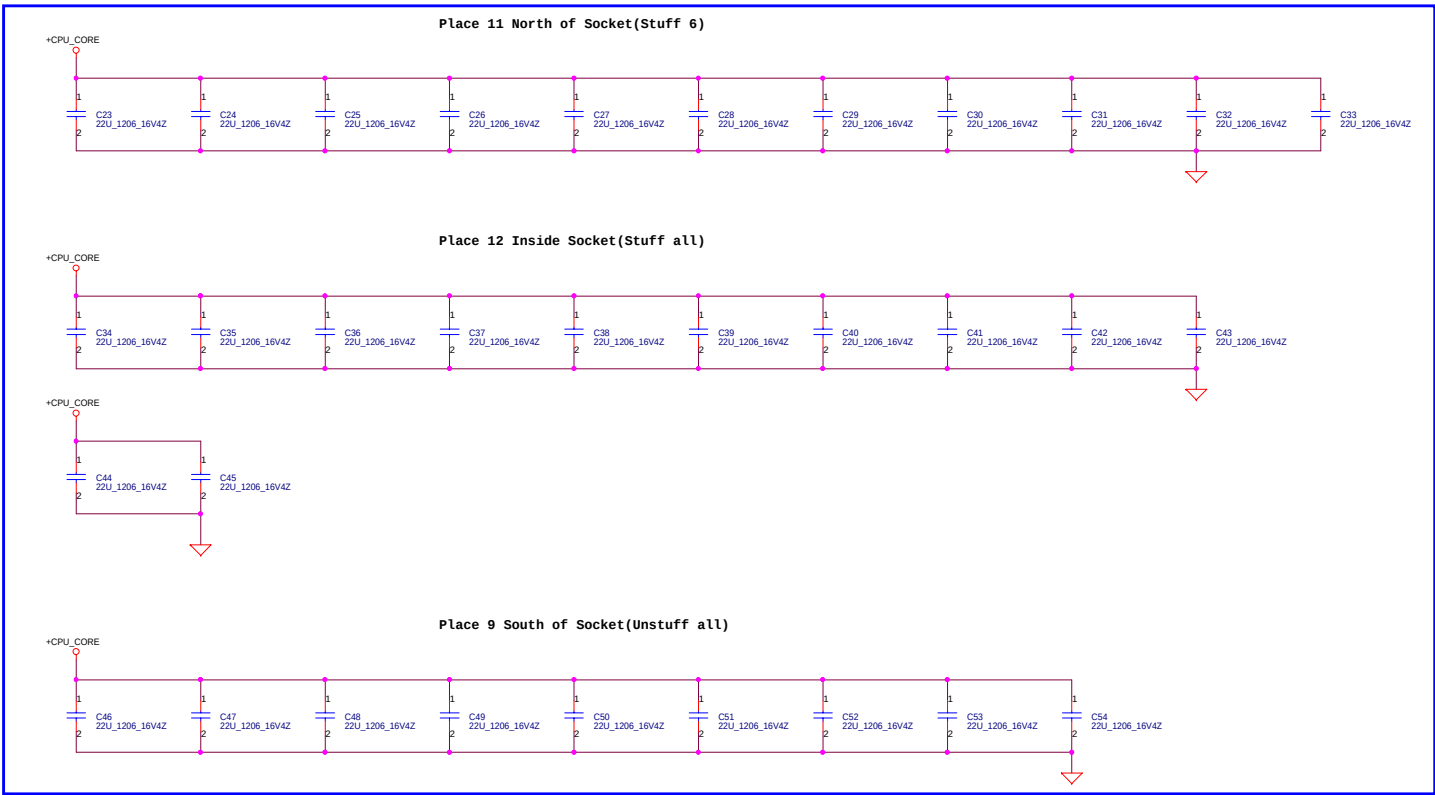
Note: Please change to 10uH, DC current of 100mA parts and close to cap

- PLL Layout note :
- 1.Place cap within 600 mils of the VCCA and VSSA pins.
 - 2.H_VCCIOPL,HVCCA,HVSSA trace wide 12mils(min)

GTL Reference Voltage Layout note :

- 1.+CPU_GTLREF Trace wide 12mils(min),Space 15mils
- 2. Place R_A and R_B near CPU.
- 3. Place decoupling cap 220PF near CPU.

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Prescott Processor in uPCPGA478			
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Thermal Sensor ADM1032AR

Thermal Sensor ADM1032AR

W=15mil

+3V(ALW)

R535
0.0402_5%

C10
0.1uF_0402_16V42

R9
@ 10K_0402_5%

C11
2200P_0402_25V7K

U1

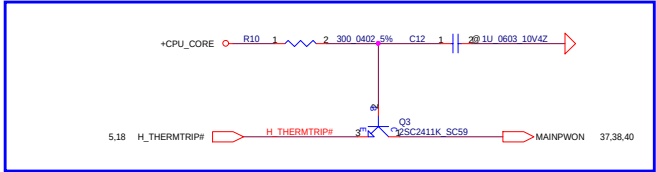
VDD
SCLK
D+
SDATA
ALERT#
THERM#
GND

H_THERMDA
H_THERMDC
EC_SMC_2
EC_SMD_2

ADM1032AR_SOP8

Address:1001_100X

Note: PLACE C10 CLOSE TO U1.1



FAN CONN. 2

Fan Control circuit

The schematic diagram illustrates a Fan Control circuit. Key components and connections include:

- Op-Amp (U2):** LM321MF, SOT23-5. Non-inverting input (pin 3) is connected to +12V/ALW via capacitor C13 (0.1uF, 0402_1B4V42). Inverting input (pin 2) is connected to +3V via resistor R12 (10K, 0402_5%) and capacitor C17 (0.001uF, 0402_50V7M). Output (pin 1) is connected to MOSFET Q4 base and capacitor C19 (0.001uF, 0402_50V7M).
- MOSFET (Q4):** SI3456DV-T1_TSP06. Source (pin 5) is grounded. Drain (pin 6) is connected to +5V via resistor R12 (10K, 0402_5%) and capacitor C21 (0.001uF, 0402_50V7M). Gate (pin 4) is connected to op-amp output.
- Resistors:** R16 (13K, 0603_1%), R17 (7.52K, 0603_1%), R18 (10K, 0402_5%), R19 (10K, 0402_5%).
- Capacitors:** C13 (0.1uF, 0402_1B4V42), C14 (10uF, 0805_10V42), C15 (0.001uF, 0402_50V7M), C16 (0.001uF, 0402_50V7M), C17 (0.001uF, 0402_50V7M), C18 (0.001uF, 0402_50V7M), C19 (0.001uF, 0402_50V7M), C20 (0.001uF, 0402_50V7M), C21 (0.001uF, 0402_50V7M).
- Other Components:** D3 (RB751U, SOD323), J1 (Molex 53358-0390), J2 (3P27).

[illegible]

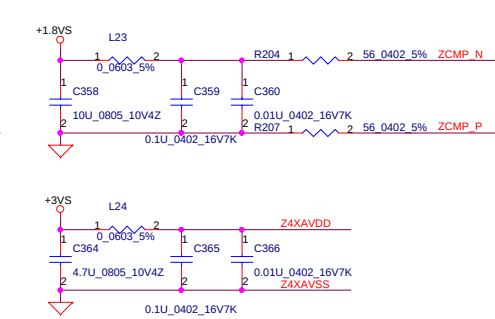
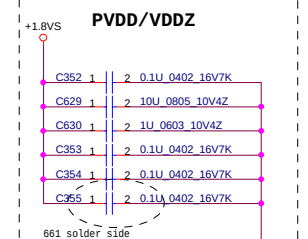
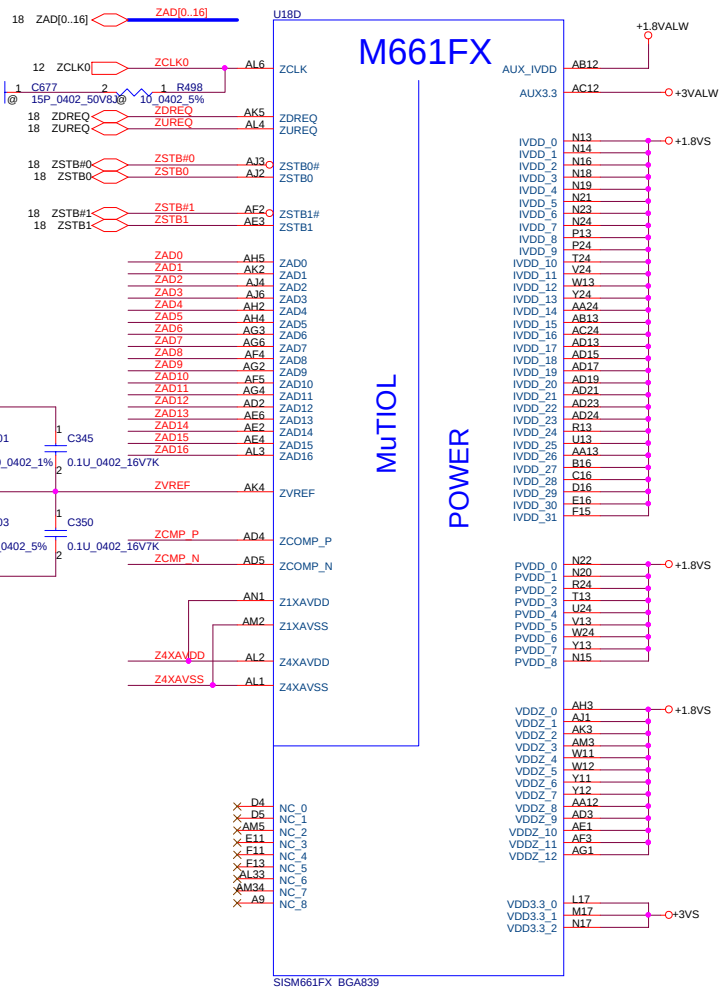


Figure 10 displays the pin connections for the AD9288, organized into two columns. Each pin connection is represented by a wavy line with a pin number and a signal name.

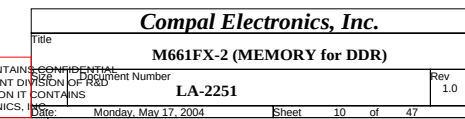
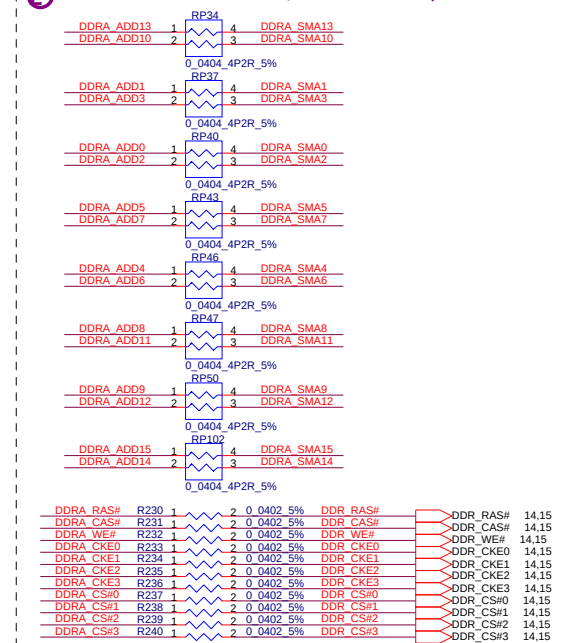
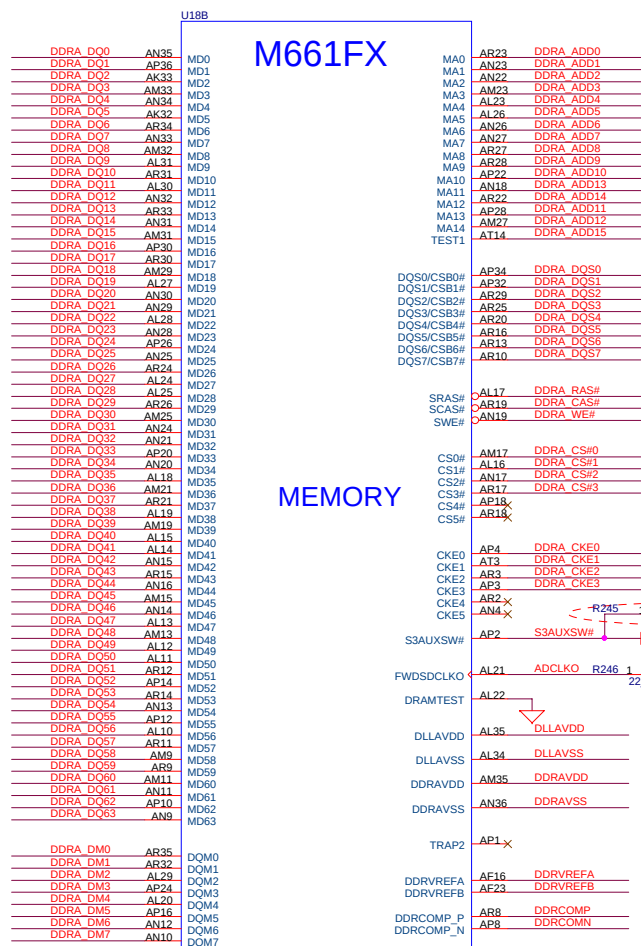
Left Column (Pins 1-26):

- DDRA_DQ03, DDRA_DQ04, DDRA_DQ05, DDRA_DQ06, DDRA_DQ07, DDRA_DQ08, DDRA_DQ09, DDRA_DQ10, DDRA_DQ11, DDRA_DQ12, DDRA_DQ13, DDRA_DQ14, DDRA_DQ15, DDRA_DQ16, DDRA_DQ17, DDRA_DQ18, DDRA_DQ19, DDRA_DQ20, DDRA_DQ21, DDRA_DQ22, DDRA_DQ23, DDRA_DQ24, DDRA_DQ25, DDRA_DQ26, DDRA_DM0, DDRA_DM1, DDRA_DM2, DDRA_DM3

Right Column (Pins 27-52):

- DDRA_DQ32, DDRA_DQ33, DDRA_DQ34, DDRA_DQ35, DDRA_DQ36, DDRA_DQ37, DDRA_DQ38, DDRA_DQ39, DDRA_DQ40, DDRA_DQ41, DDRA_DQ42, DDRA_DQ43, DDRA_DQ44, DDRA_DQ45, DDRA_DQ46, DDRA_DQ47, DDRA_DQ48, DDRA_DQ49, DDRA_DQ50, DDRA_DQ51, DDRA_DQ52, DDRA_DQ53, DDRA_DQ54, DDRA_DQ55, DDRA_DM4, DDRA_DM5, DDRA_DM6, DDRA_DM7

The diagrams show various signal types, including data signals (DDRA_DQ), address signals (DDRA_A), and data strobe signals (DDRA_DS). The connections are labeled with pin numbers and signal names, and the diagrams are organized into groups of four pins each, with a 4P2R_5% label indicating a 4-pin to 2-pin connection with 5% tolerance.

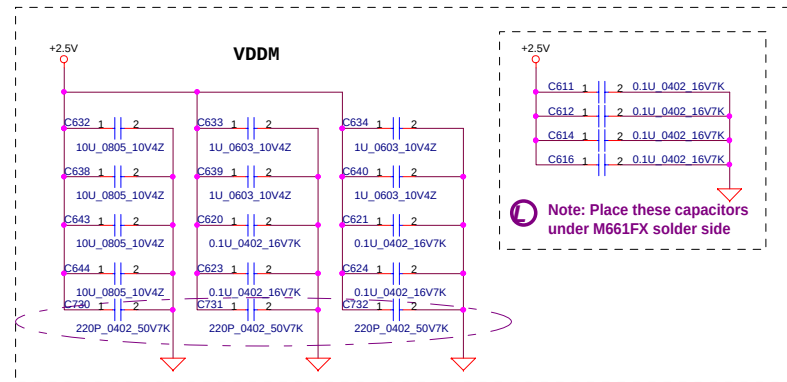
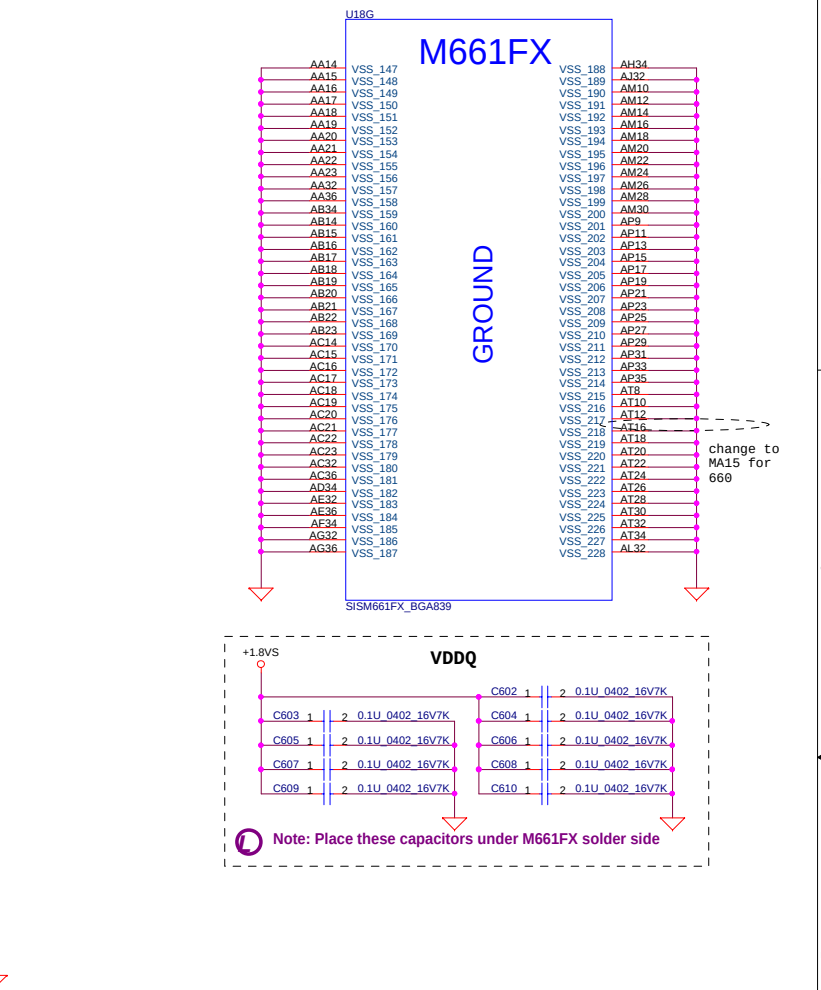


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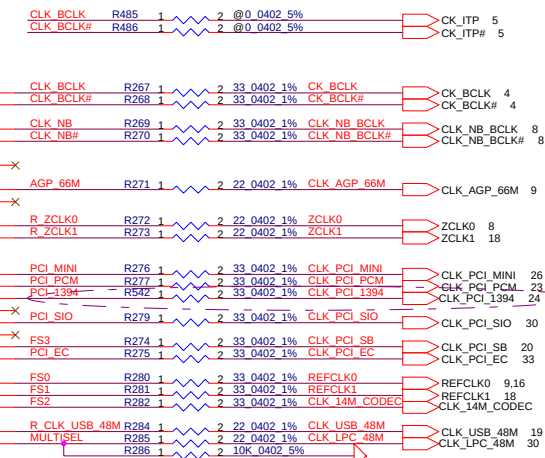
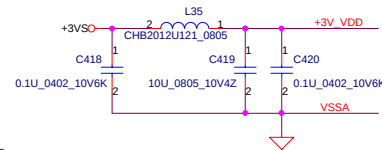
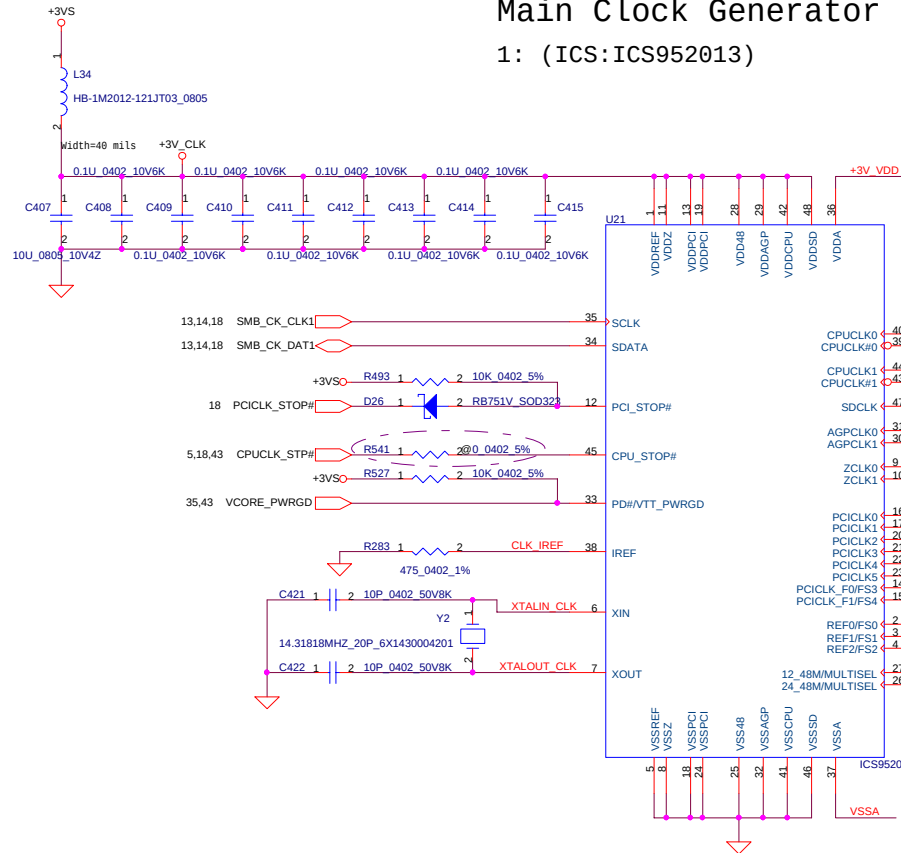
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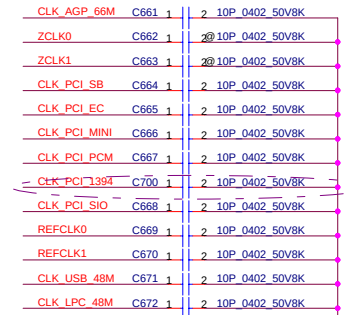
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Title			
M661FX-4 (Powers)			
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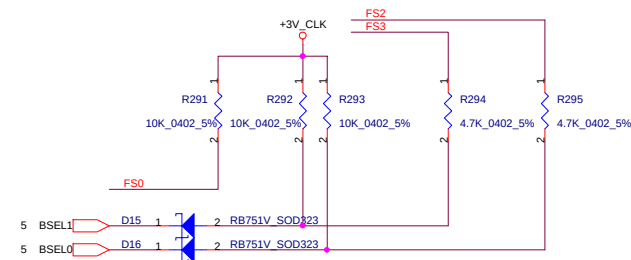
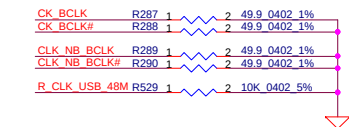
1: (ICS:ICS952013)



Place near to the Clock Outputs



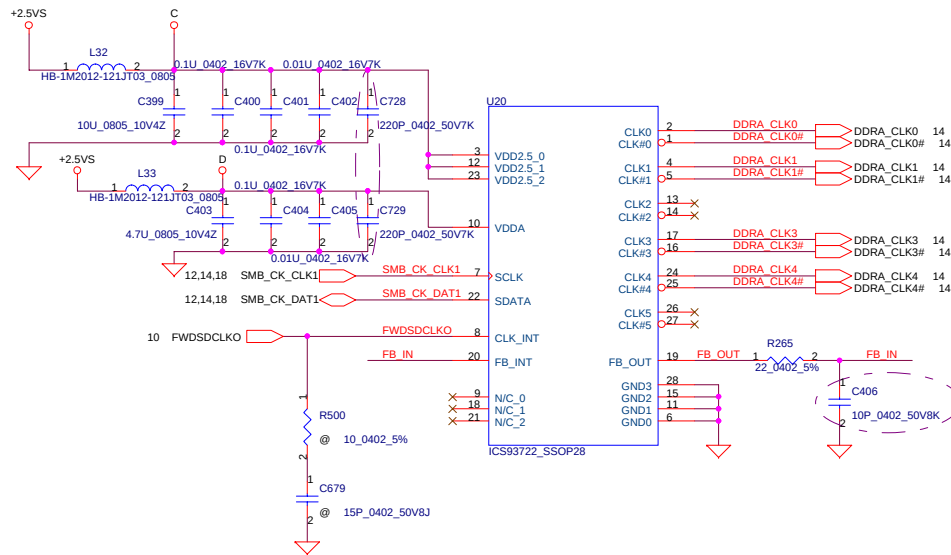
Place near to the Clock Outputs



FS3	FS2	CPU	ZCLK	AGP	PCI
0	0	100	133	66	33
0	1	133	133	66	33
1	0	200	133	66	33

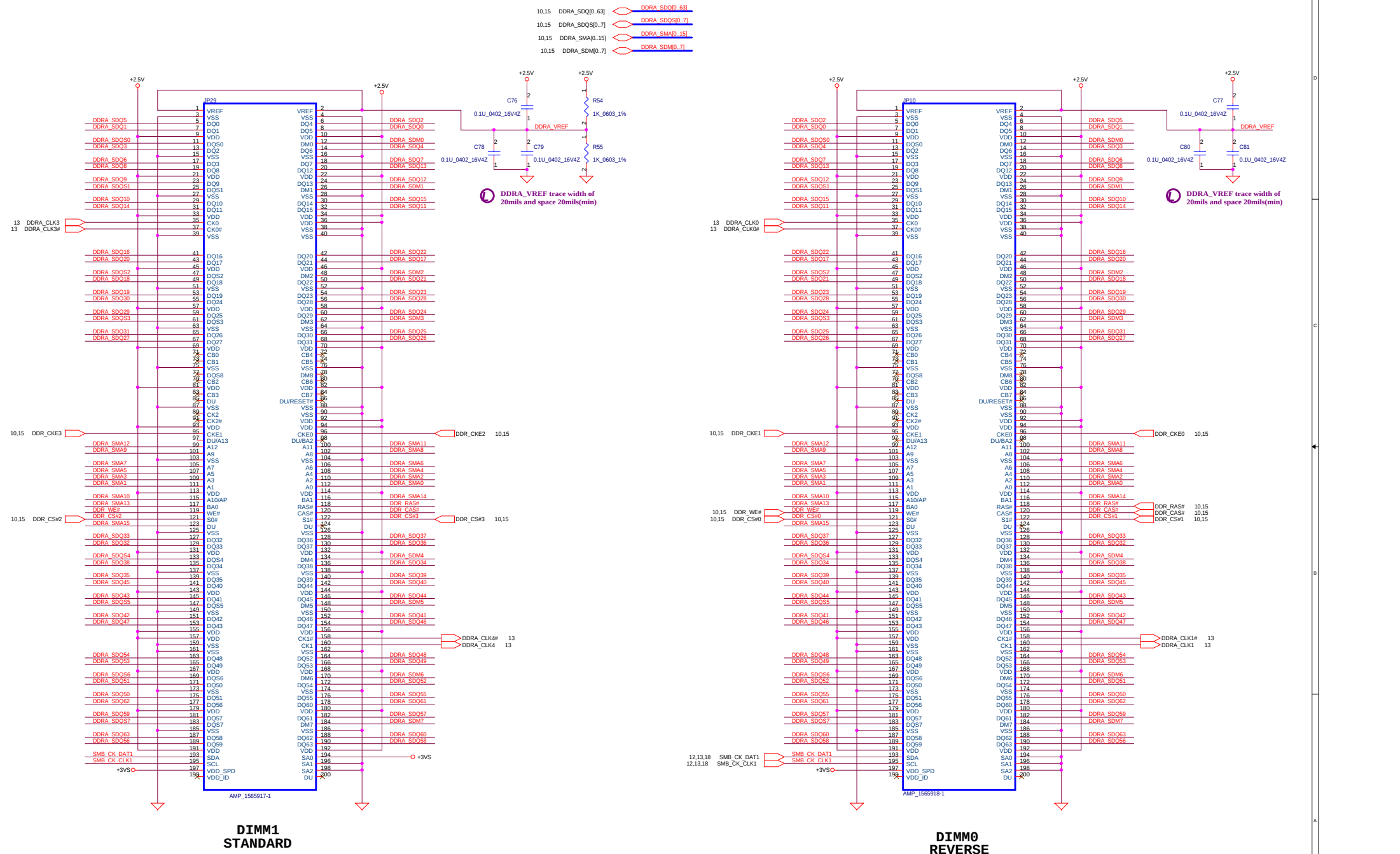
Clock Buffer (DDR)

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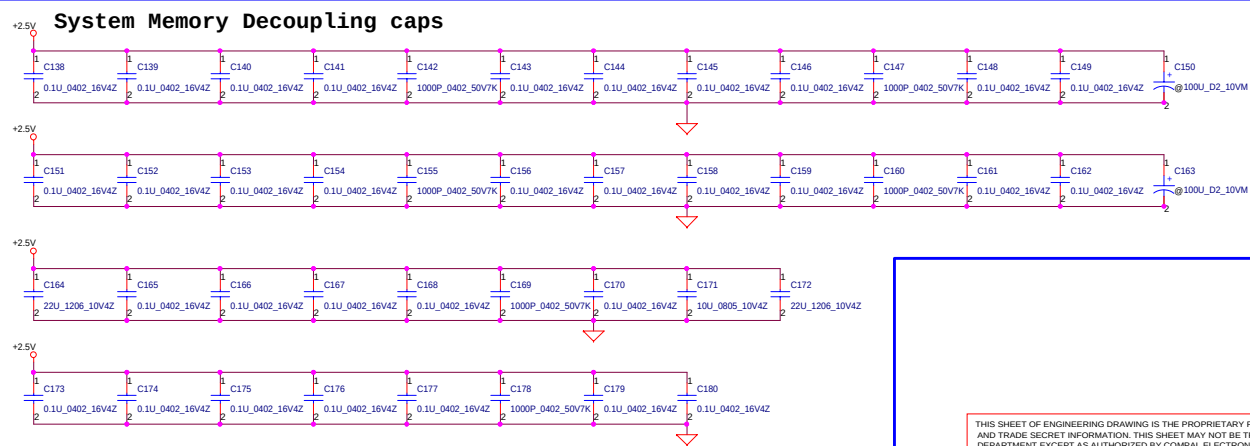
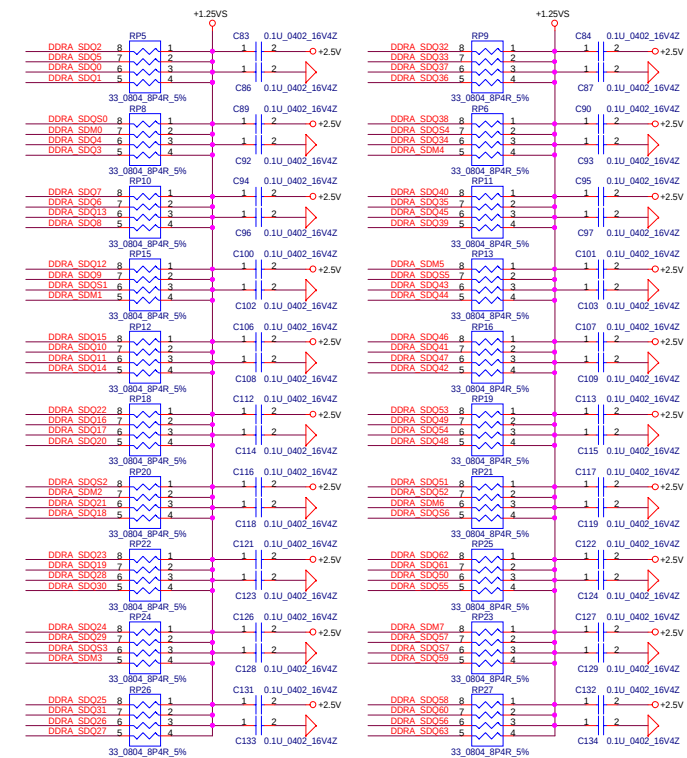


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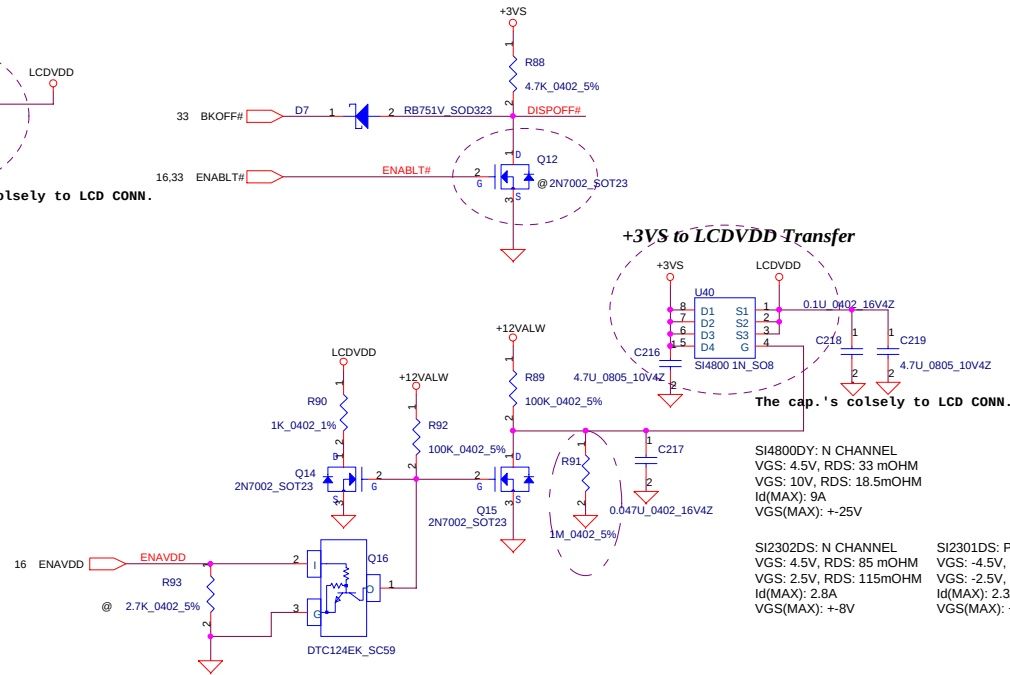
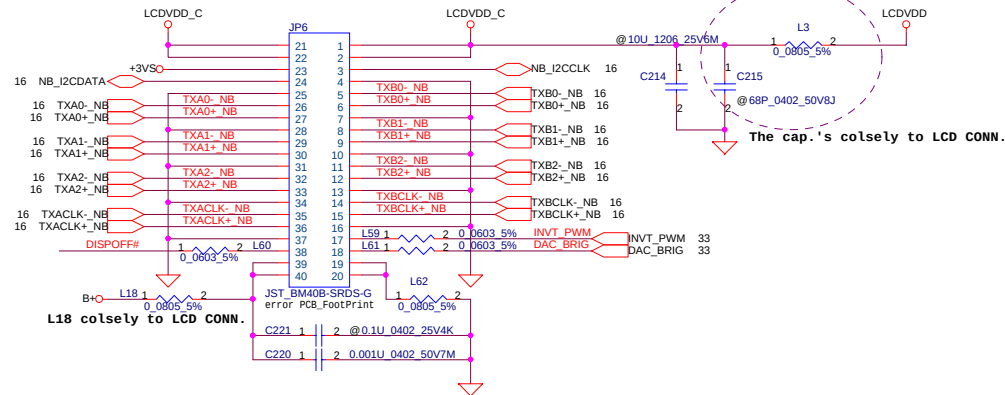
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DDR Clock Buffer			
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DDR Termination resistors & Decoupling caps

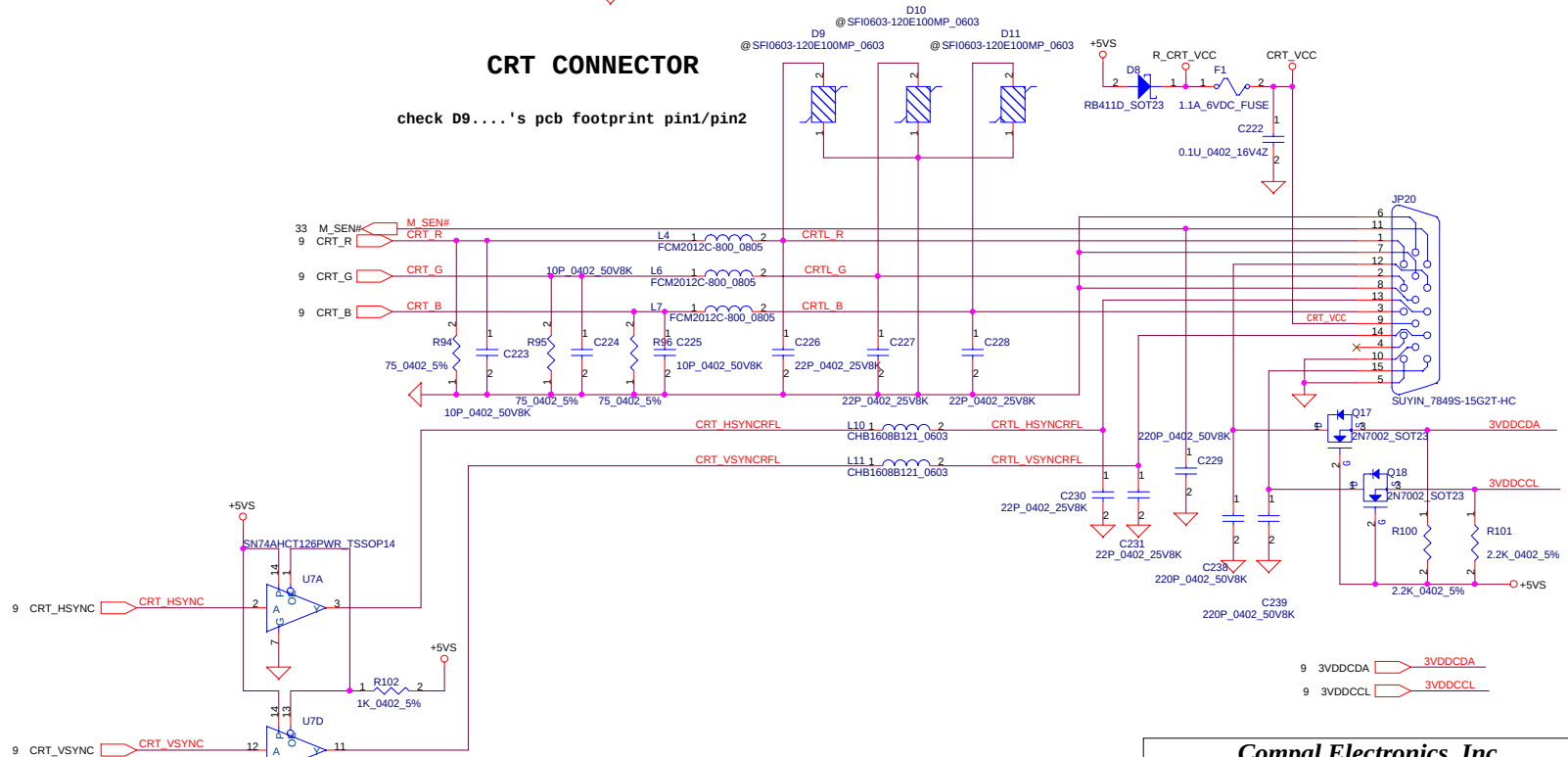


LCD CONN



CRT CONNECTOR

check D9....'s pcb footprint pin1/pin2



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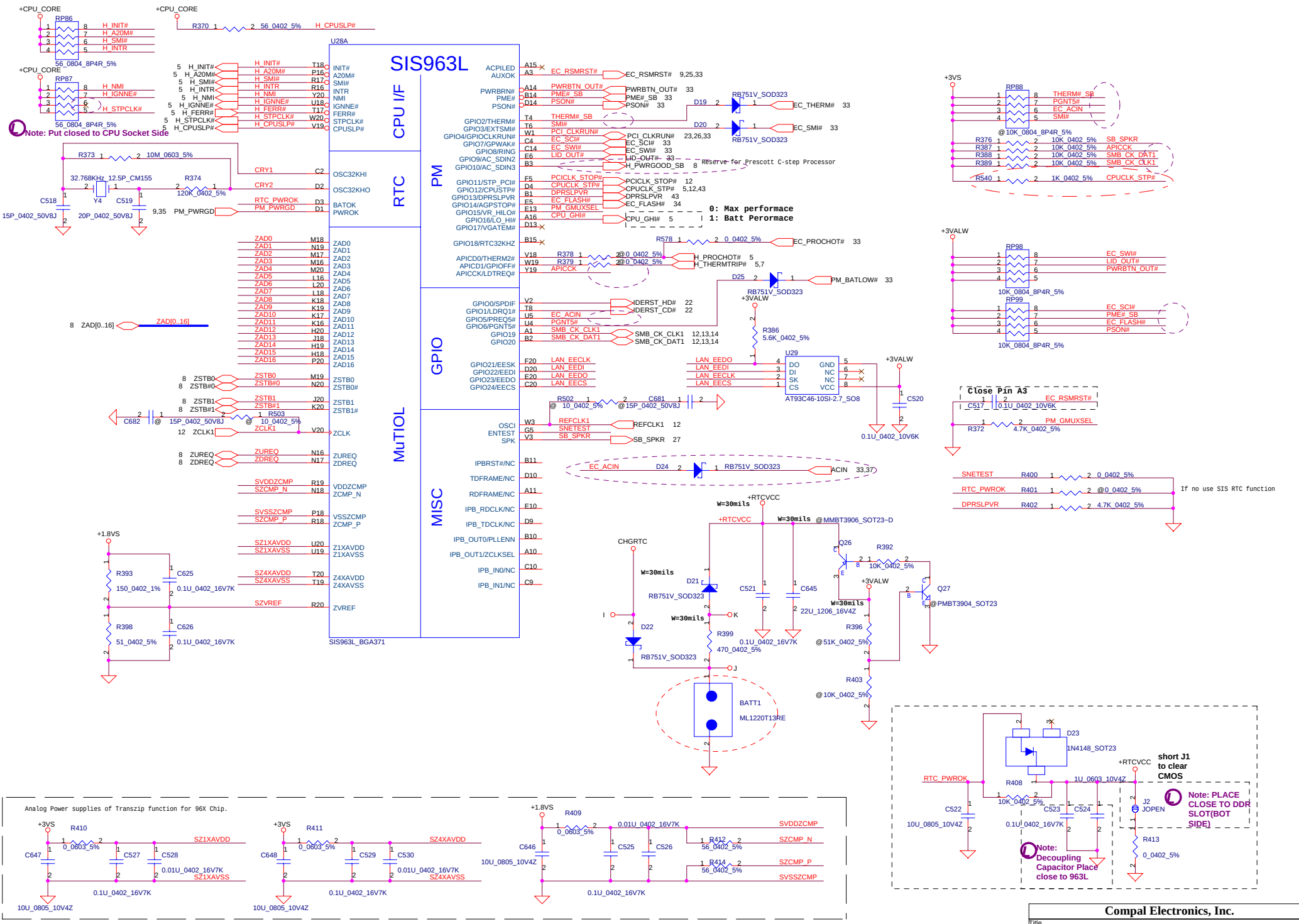
LCD/Inverter BD & CRT CONN.

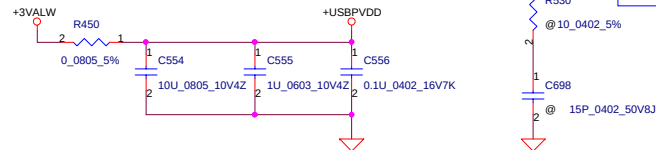
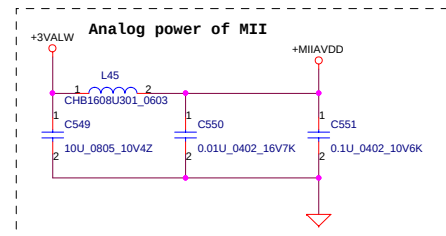
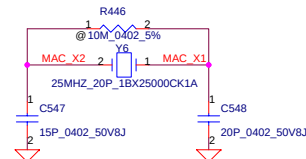
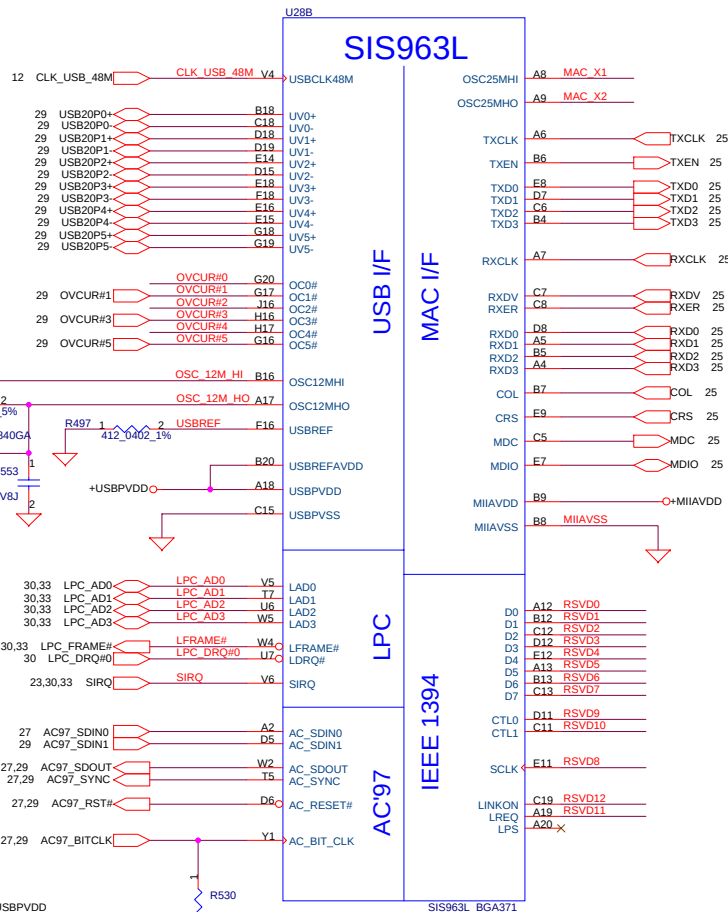
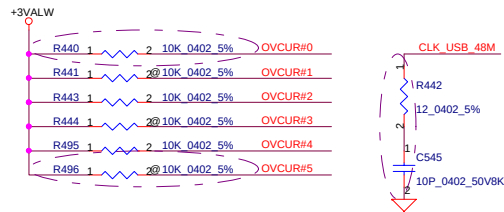
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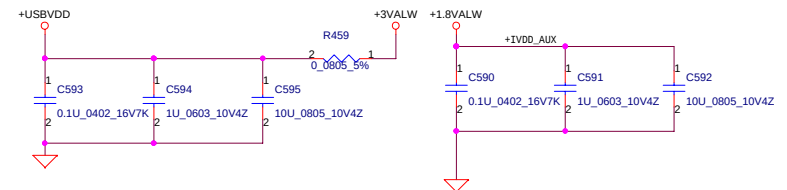
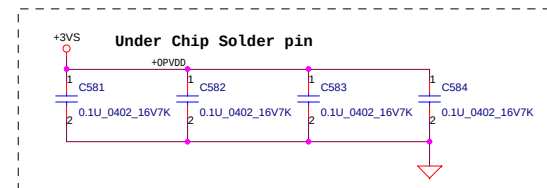
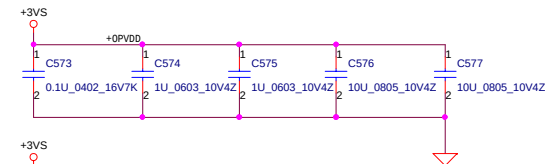
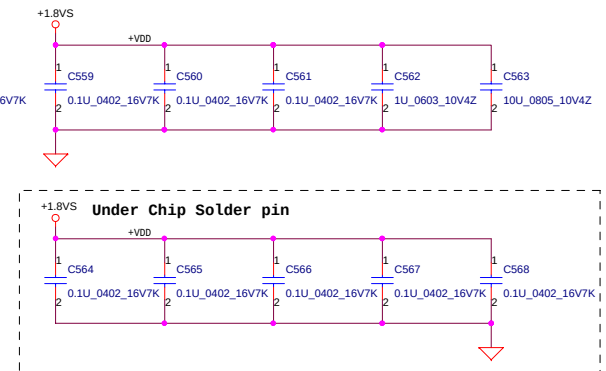
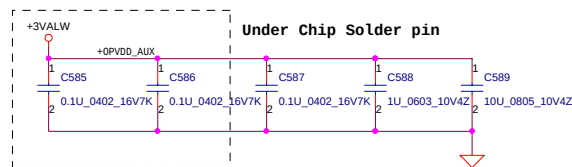
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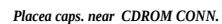
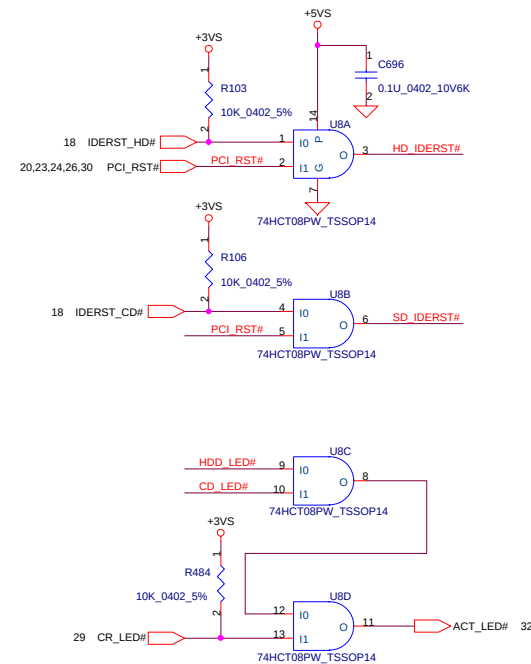




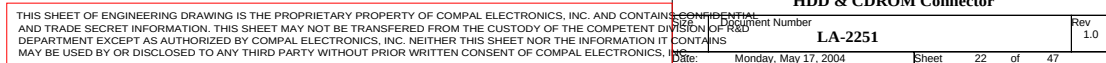
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Title	963L-2 (USB/LPC/AC97/1394/MAC)		
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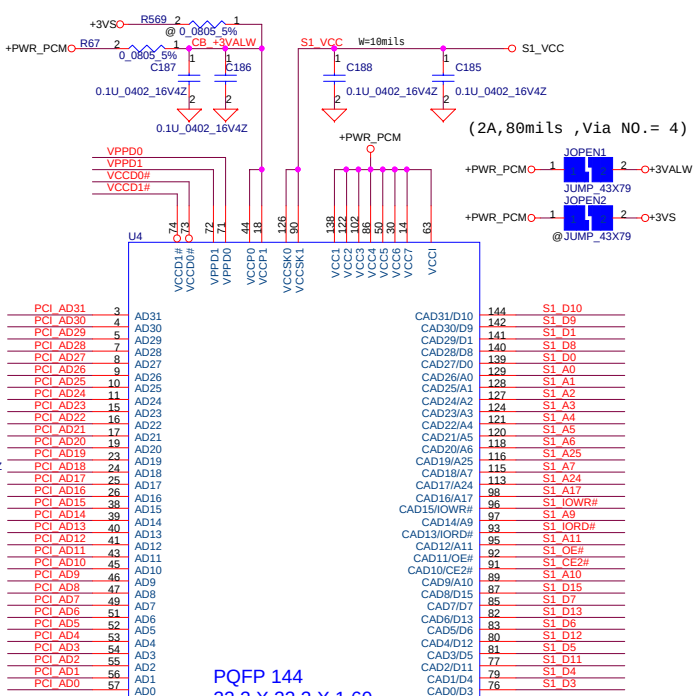
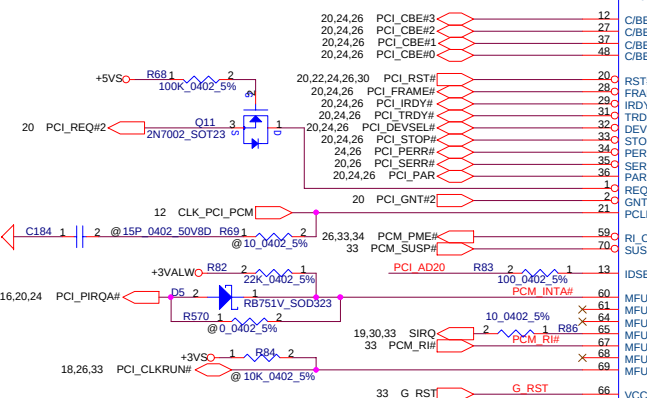
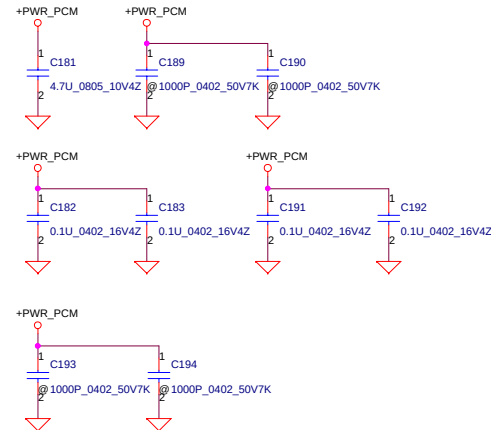




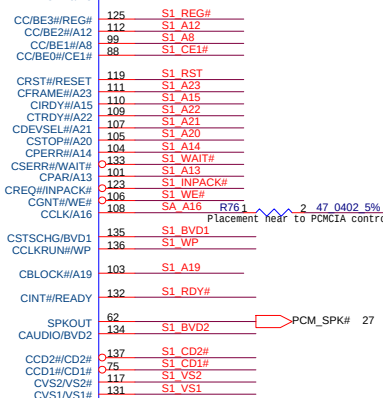
+5VS for CD trace to CONN W=100mils



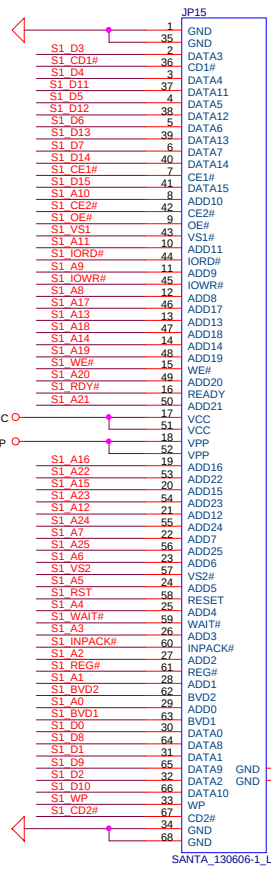
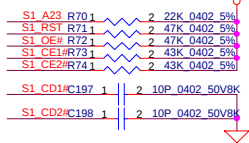
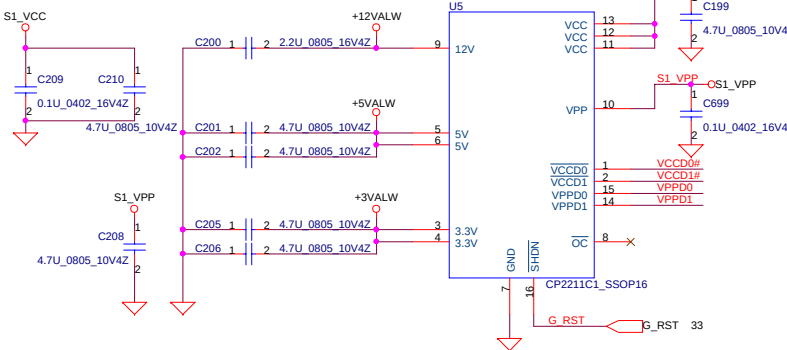
CARDBUS CB1410



PQFP 144
22.2 X 22.2 X 1.60



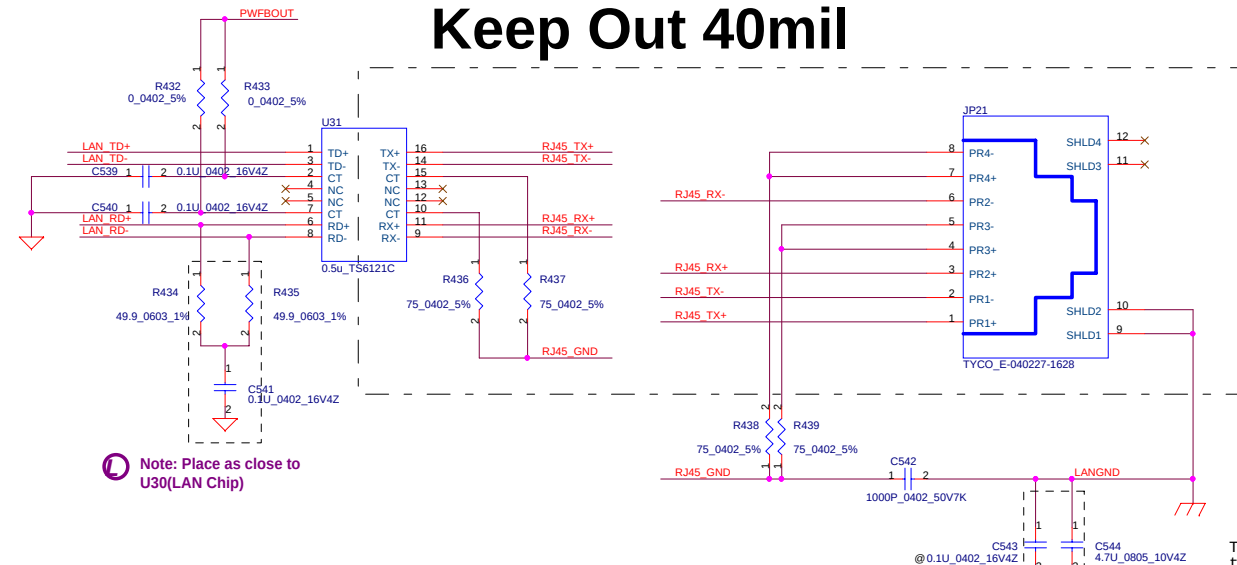
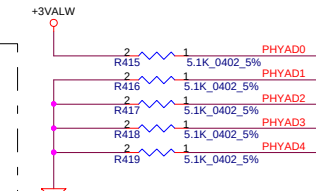
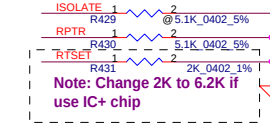
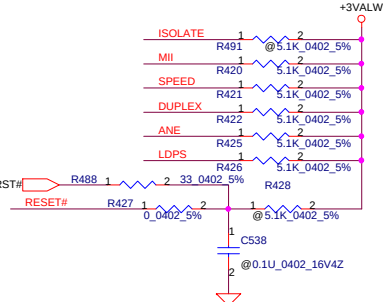
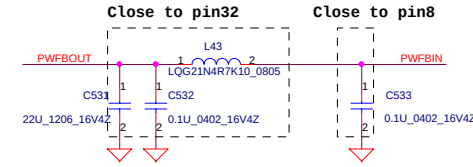
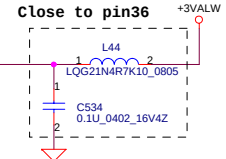
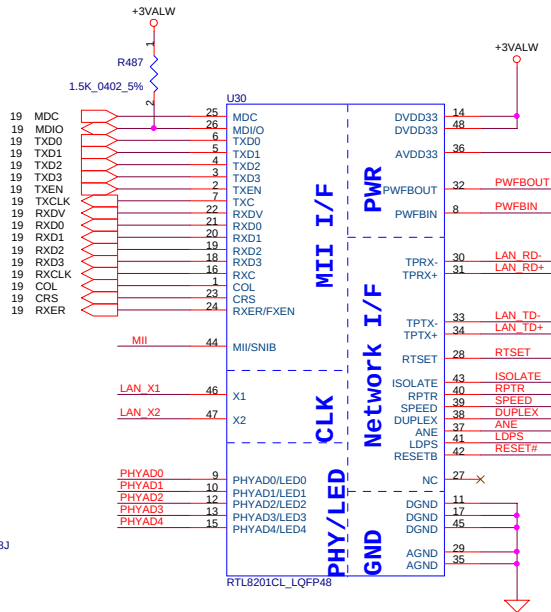
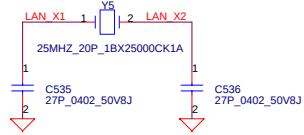
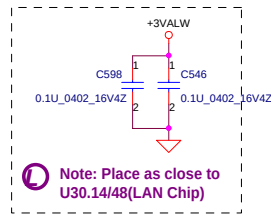
PCMCIA POWER CTRL.



CARDBUS SOCKET

Compal Electronics, Inc.			
Title			
CardBus Controller CB1410/CardBus Socket/Power Switch			
AIN: CONFIDENTIAL	Document Number	Rev 1.0	
IT DIVISION OF R&D	LA-2251		
IT CONTAINS			
CS, S, C			
Date: Monday, May 17, 2004	Sheet 23 of 47		

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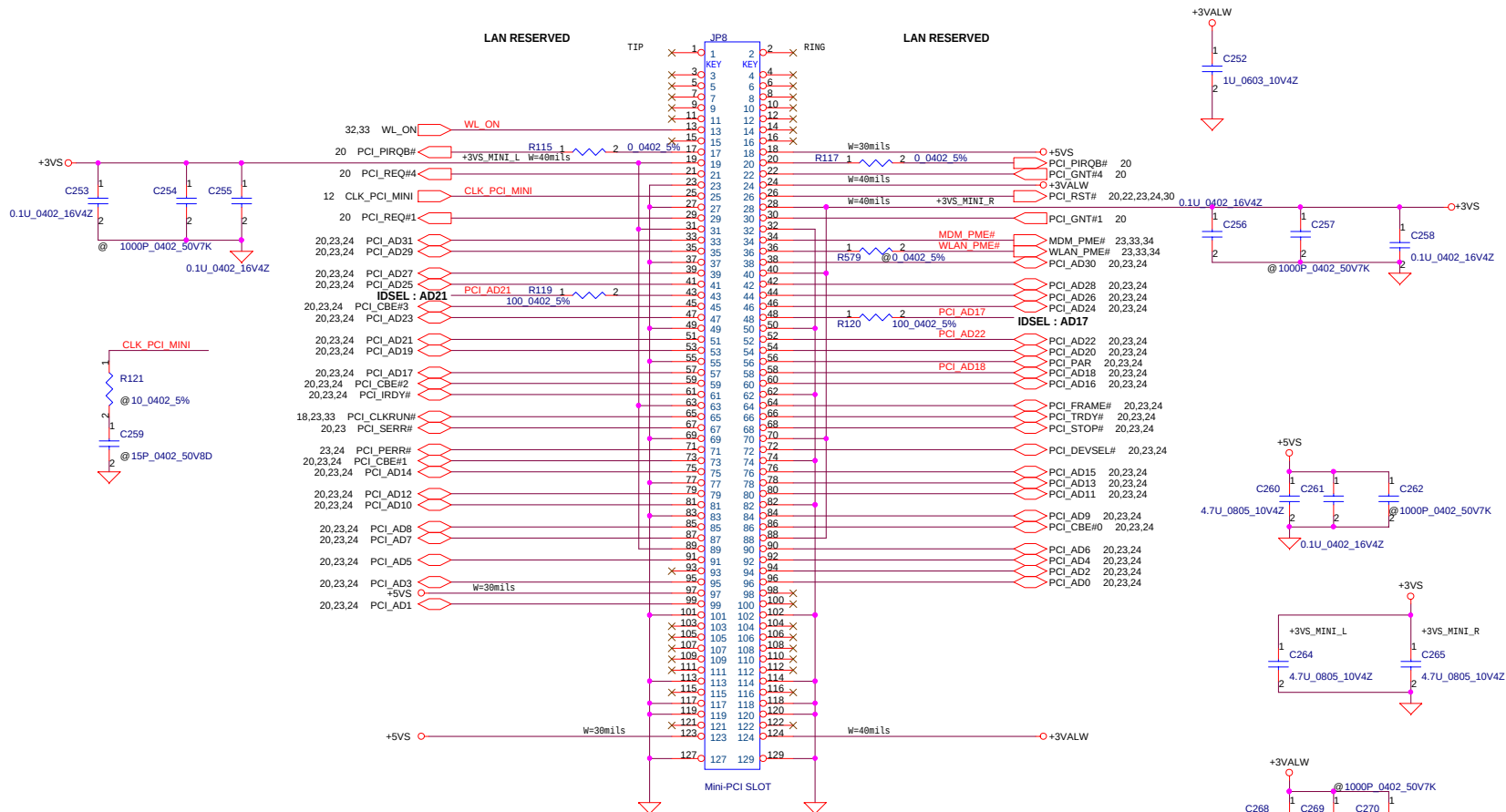
Keep Out 40mil

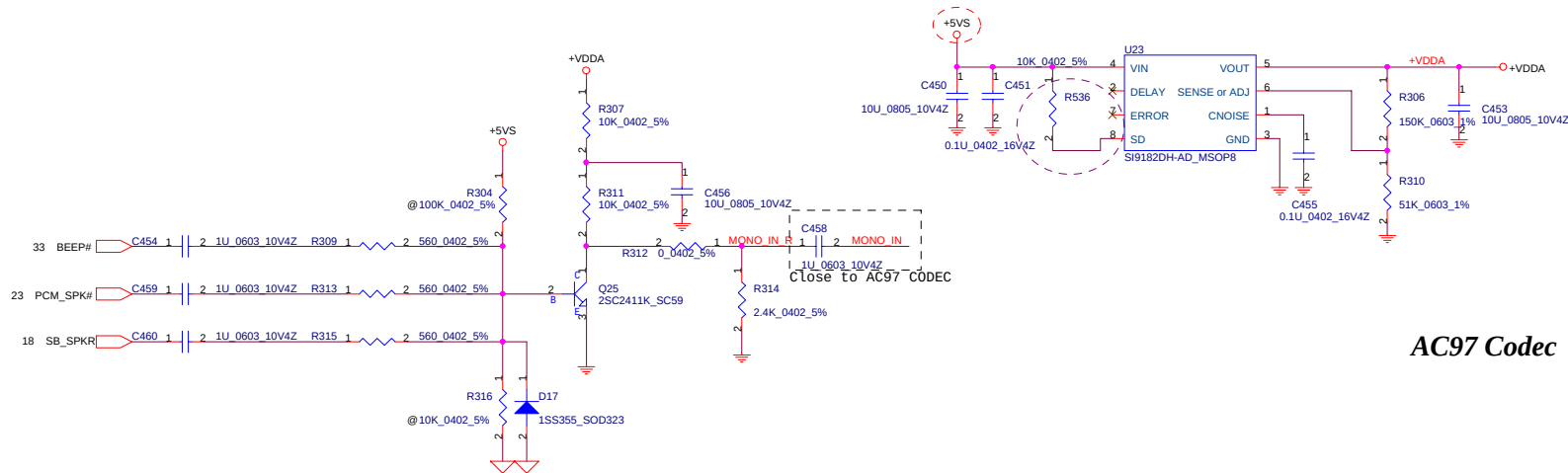
LAYOUT NOTICE: This area do not connect to power plan include Vcc and GND in any layer

Termination plane should be copled to chassis ground and also depends on safety concern

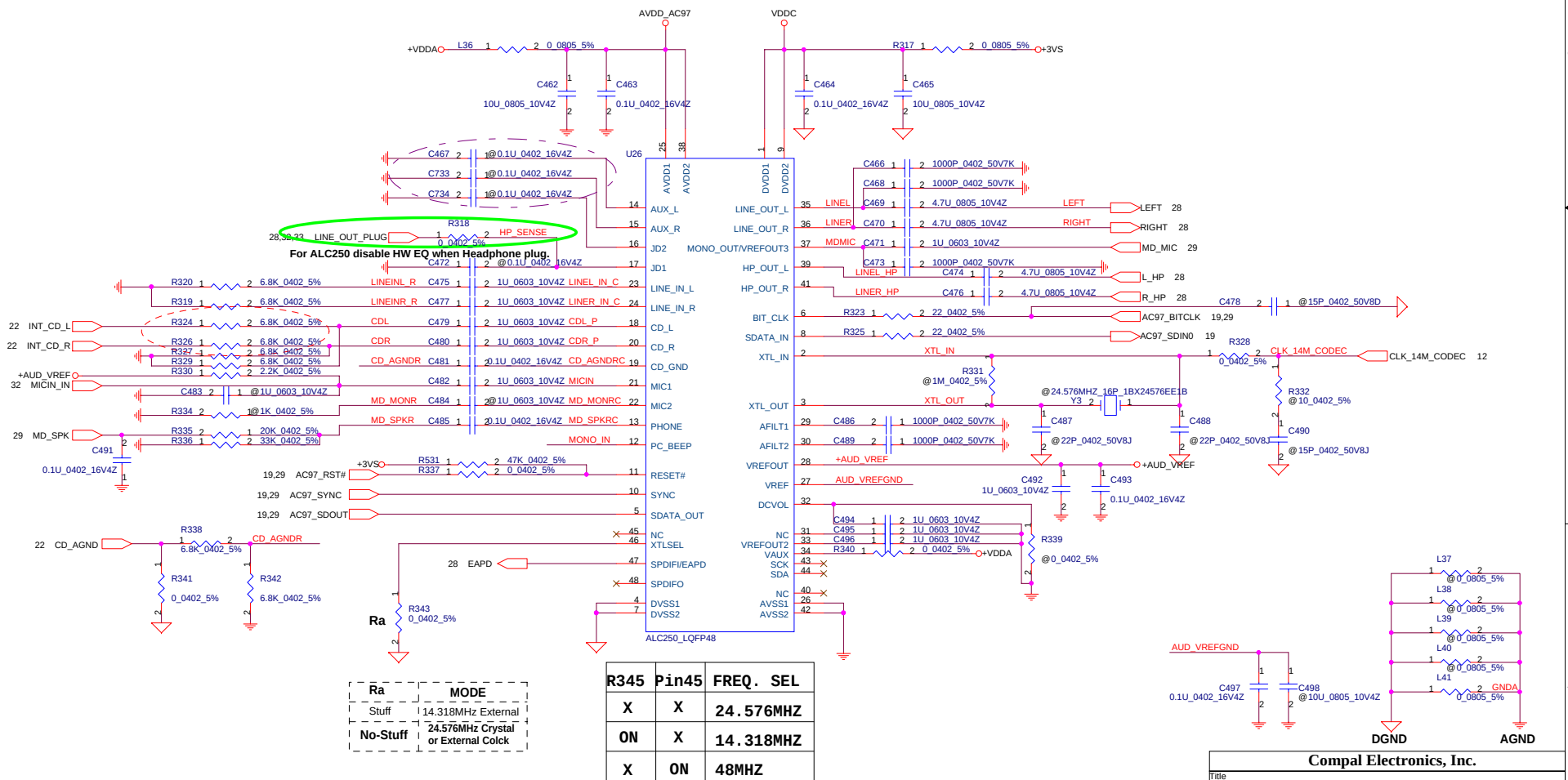
Compal Electronics, Inc.			
Title	LAN-PHY RTL8201CL		
Revision	1.0	Sheet	25 of 47
Date	Monday, May 17, 2004	Sheet	25 of 47

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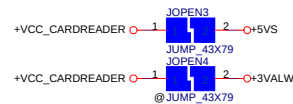




AC97 Codec

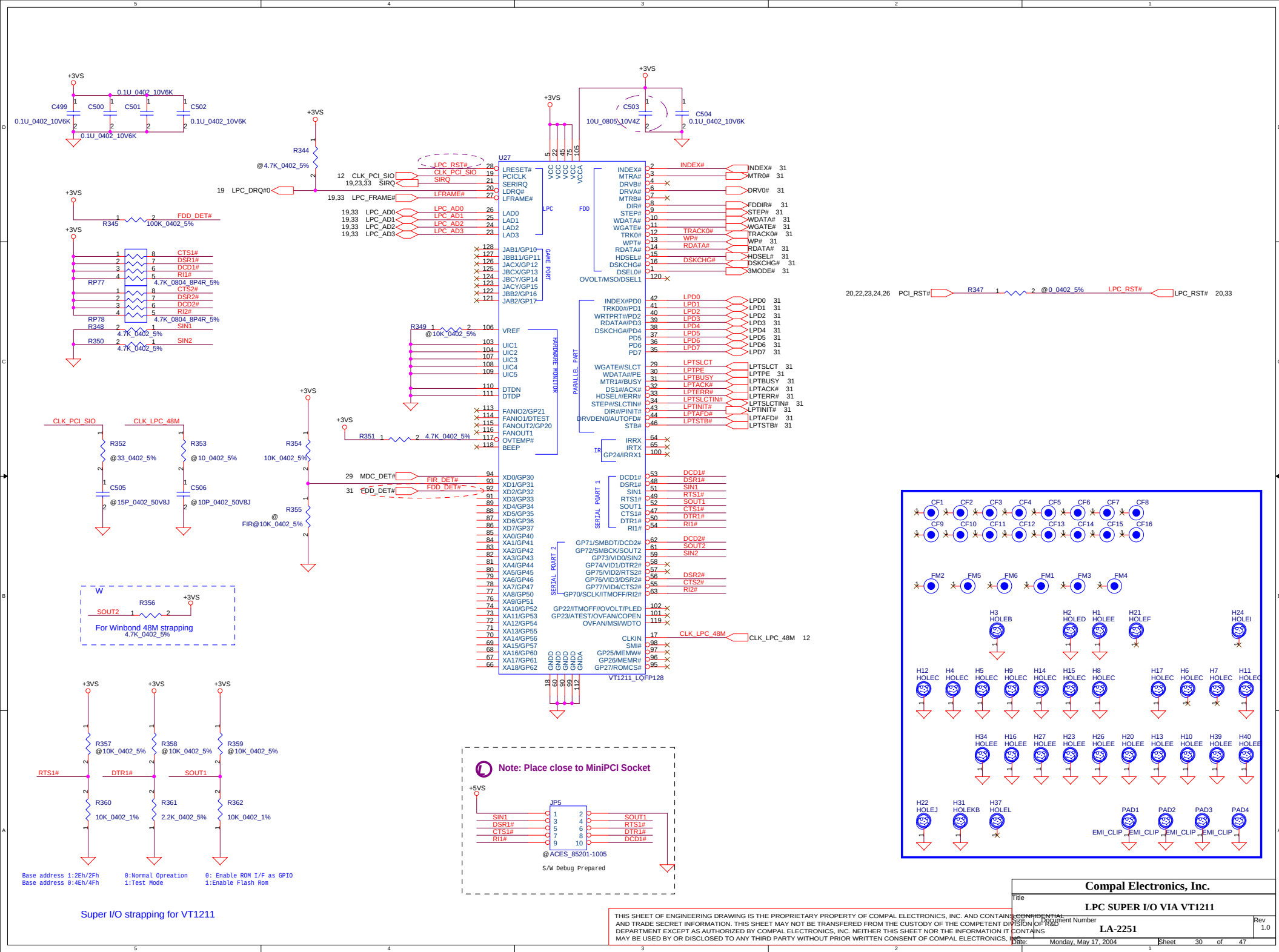


Pin 1 is NC for Pctel and connexant MDC modem
Pin 2 is NC for Pctel and connexant MDC modem



Compal Electronics, Inc.	
Title	MDC , Bluetooth & USB CONN.
AIN'S CONFIDENTIAL T DIVISION OF PRO IT CONTAINS S. INC.	Document Number LA-2251
Monday, May 17, 2004	Sheet 29 of 47
Rev 1.0	

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Parallel Port

The schematic diagram illustrates the electrical connections for a Parallel Port interface. Key components and connections include:

- Power Supply:** +5V PRN is connected to the circuit.
- Capacitors:** C507 (4.7uF 0805 10V42) and C508 (0.1uF 0402 10V6K) are used for decoupling.
- Diode:** D18 (1SS355 SOD323) is connected in series with the +5V PRN line.
- Resistors:** R363 (33 ohm 0402 5%), R364 (2.7K 0402 5%), R365 (33 ohm 0402 5%), RP79 (2.7K 1206 8P4R 5%), RP80 (2.7K 1206 8P4R 5%), RP81 (2.7K 1206 8P4R 5%), RP82 (2.7K 1206 8P4R 5%), RP85 (2.7K 1206 8P4R 5%), RP101 (68 ohm 0804 8P4R 5%), and RP101 (68 ohm 0804 8P4R 5%) are used for signal conditioning and termination.
- Connectors:** The circuit is connected to a parallel port connector (JP1) with pins 1 through 25. The connector is labeled SUIYN_7313S-25G2T-AA.
- Signal Lines:** The circuit includes signal lines for LPTSTB#, LPTAFD#, LPTERR#, LPTINIT#, LPTSLCTIN#, LPTACK#, LPTBUSY, LPTPE, LPTSLCT, and LPTD[0..7].

FDD CONN.

The diagram illustrates the FDD connection, starting with a +5V trace to the connector (CONN) with a width of 100mils. The trace is shown with several capacitors (C509, C510, C511, C512) and a 1000P_0402_50V7K capacitor. The signal lines are labeled with their respective functions and pin numbers. A note indicates: "Note: Place caps. near FDD CONN."

Signal Lines and Pin Numbers:

- INDEX# (26, 25, 24, 23, 22, 21)
- DRV0# (20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1)
- DSKCHG# (26, 25, 24, 23, 22, 21)
- MTR0# (20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1)
- FDDIR# (26, 25, 24, 23, 22, 21)
- 3MODE# (20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1)
- STEP# (26, 25, 24, 23, 22, 21)
- FDD_DET# (20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1)
- WDATA# (26, 25, 24, 23, 22, 21)
- WGATE# (20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1)
- TRACK0# (26, 25, 24, 23, 22, 21)
- WP# (20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1)
- RDATA# (26, 25, 24, 23, 22, 21)
- HDSEL# (20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1)

EMI Requirement

The EMI requirement section shows the connection of the FDD to the system. It includes the following components and connections:

- CP7: 220P_1206_8P4C_50V8K
- CP8: 220P_1206_8P4C_50V8K
- CP9: 220P_1206_8P4C_50V8K
- C516: 1K_1206_8P4R_5%
- RP84: 1K_1206_8P4R_5%
- RP83: 1K_1206_8P4R_5%
- RP100: 1K_1206_8P4R_5%

The connections are as follows:

- INDEX# (1) to CP7 (1)
- DRV0# (2) to CP7 (2)
- DSKCHG# (3) to CP7 (3)
- MTR0# (4) to CP7 (4)
- FDDIR# (1) to CP8 (1)
- 3MODE# (2) to CP8 (2)
- STEP# (3) to CP8 (3)
- WDATA# (4) to CP8 (4)
- WGATE# (1) to CP9 (1)
- TRACK0# (2) to CP9 (2)
- WP# (3) to CP9 (3)
- RDATA# (4) to CP9 (4)
- HDSEL# (1) to C516 (1)
- HDSEL# (2) to C516 (2)
- HDSEL# (3) to C516 (3)
- HDSEL# (4) to C516 (4)
- HDSEL# (5) to C516 (5)
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- HDSEL# (97) to C516 (97)
- HDSEL# (98) to C516 (98)
- HDSEL# (99) to C516 (99)
- HDSEL# (100) to C516 (100)

Diagram illustrating the CPU and memory components of the TMS320C49:

- CP7 (CPU)** is connected to **INDEX#** (1), **DRV0#** (2), **DSKCHG#** (3), and **MTR0#** (4).
- CP8 (220P_1206 8P4C_50V8K)** is connected to **FDDR#** (1), **3MODE#** (2), **STEP#** (3), and **WDATA#** (4).
- CP9 (220P_1206 8P4C_50V8K)** is connected to **WGATE#** (1), **TRACK0#** (2), **WP#** (3), and **RDATA#** (4).
- CS16 (220P_0402 50V9J)** is connected to **HDSEL#** (1).

[illegible]

L

[illegible]

Note: REQUEST CLOSEST JP9 ADD BY EMI REQUEST

Pin	Signal
C687 1	2 @100P_0402_50VB3 PMLD_Q#
C689 1	2 @100P_0402_50VB3 BATLED_Q#
C691 1	2 @100P_0402_50VB3 ACT_LED#
C692 1	2 @100P_0402_50VB3 BT_ON#
C693 1	2 @100P_0402_50VB3 LINE_OUT_PLUG
C695 1	2 @100P_0402_50VB3 MICIN_IN

11

1

1

The diagram illustrates the electrical connections for the JP9 connector. The pins are numbered 1 through 20. The signals and their connections are as follows:

- Pin 1:** R506, 2 0 0.402 5%
- Pin 2:** R507, 2 0 0.402 5%
- Pin 3:** TP DATA
- Pin 4:** TP CLK
- Pin 5:** +5VALW
- Pin 6:** R516, 1
- Pin 7:** R517, 2 0 0.402 5%
- Pin 8:** R518, 2 0 0.402 5%
- Pin 9:** R513, 1
- Pin 10:** R515, 2 0 0.402 5%
- Pin 11:** R519, 1
- Pin 12:** R520, 2 0 0.402 5%
- Pin 13:** R521, 2 0 0.402 5%
- Pin 14:** R522, 2 0 0.402 5%
- Pin 15:** R524, 2 0 0.402 5%
- Pin 16:** BT_ON#
- Pin 17:** PMLED_0#
- Pin 18:** BATLED_0#
- Pin 19:** ACT_LED#
- Pin 20:** LINE_OUT_PLUG
- Pin 21:** MICIN_IN
- Pin 22:** INTSPK_L+
- Pin 23:** INTSPK_L-
- Pin 24:** INTSPK_R+
- Pin 25:** INTSPK_R-

Note: NEED CLOSEST JP9 ADD BY EMI REQUEST

ACES_85201-2002

W/L_ON 26.33

C5

@220P_0.402_50VBK

LINE_OUT_PLUG 27.28.33

@33P_0.402_50VBK

INTSPK_L+ 28

INTSPK_L- 28

INTSPK_R+ 28

INTSPK_R- 28

C6

@33P_0.402_50VBK

C7

C8

C9

@33P_0.402_50VBK

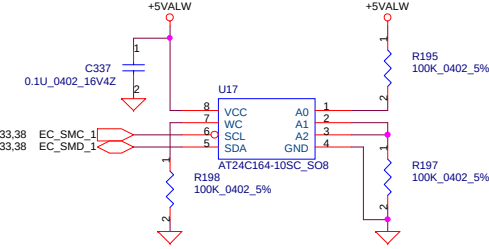
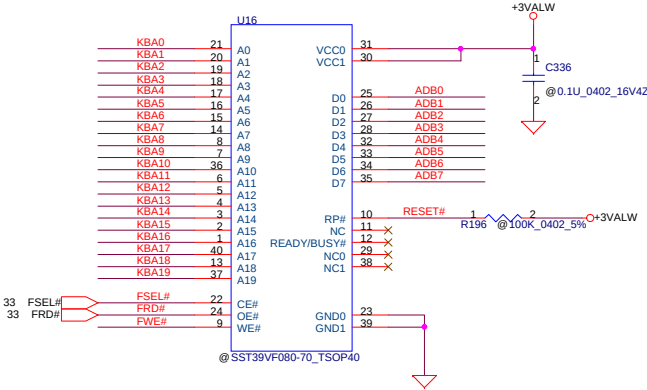
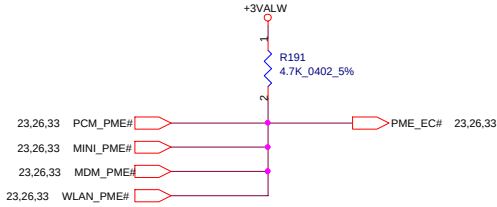
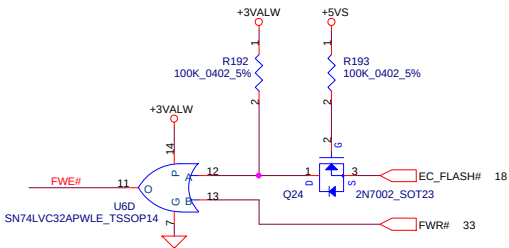
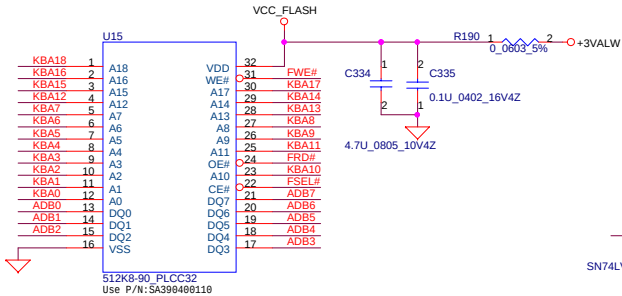
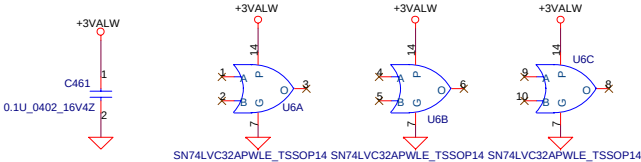
+5VS

C4

0.1U_0.402_16V4Z

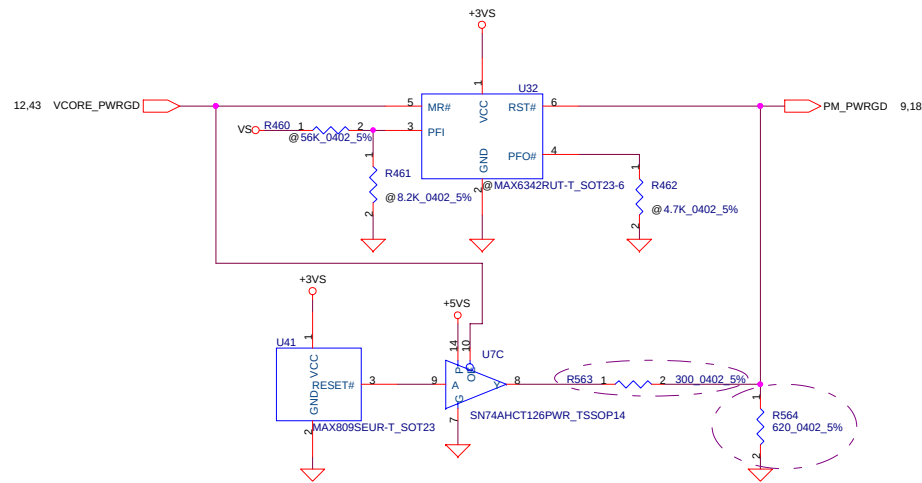
R52

002



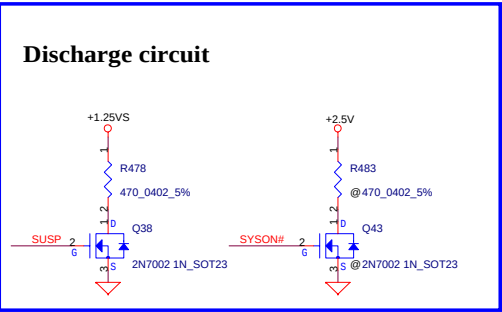
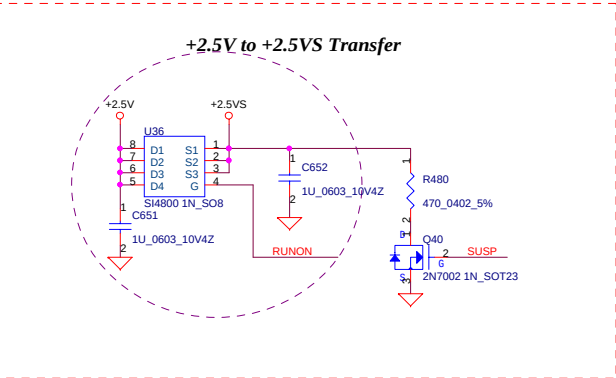
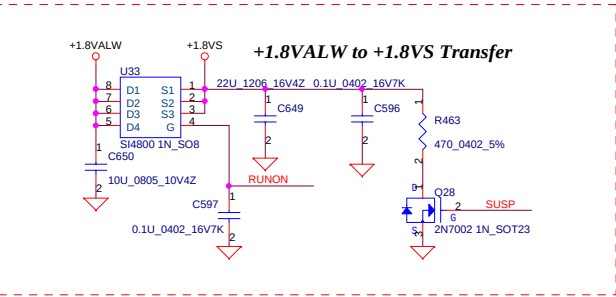
Compal Electronics, Inc.			
Title	BIOS & EC I/O Port		
Document Number	LA-2251		
Rev	1.0		
Date	Monday, May 17, 2004	Sheet	34 of 47

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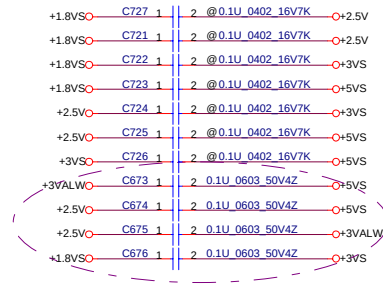
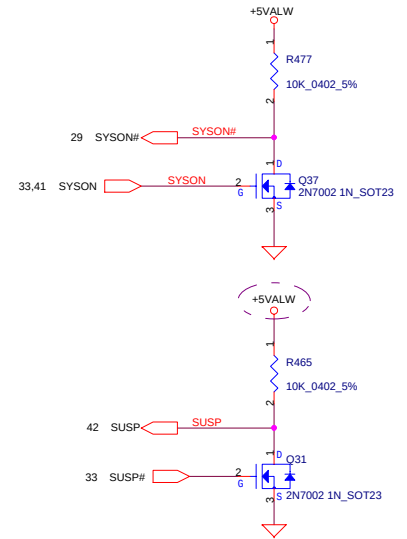
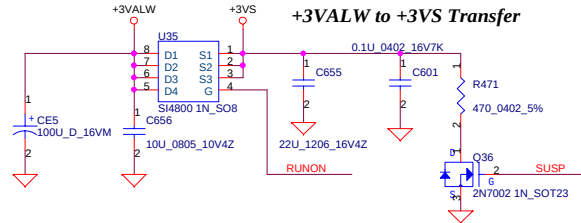
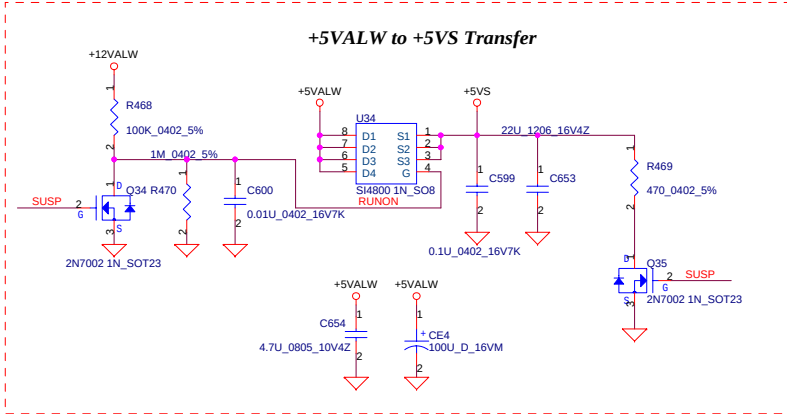


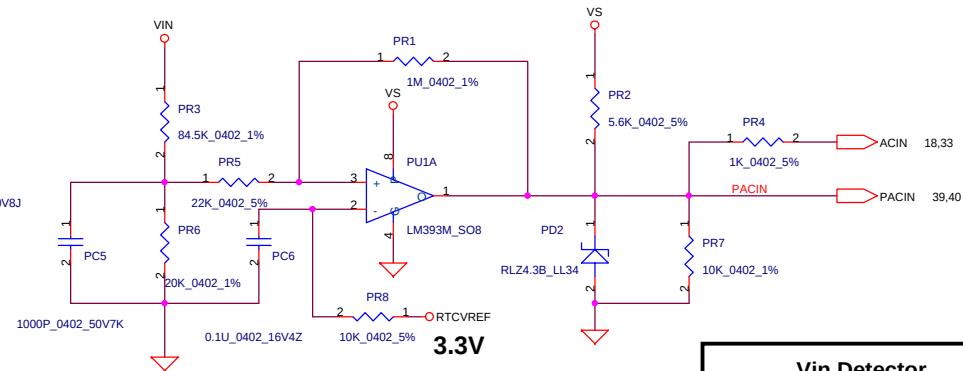
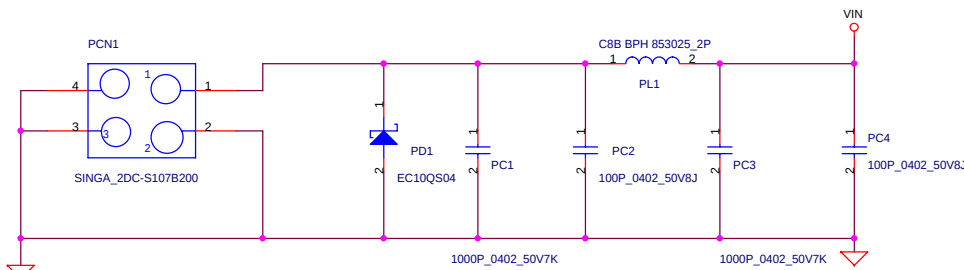
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Compal Electronics, Inc.			
Title			
RESET & PS2 Connector			
Revision			
1.0			
Date			
Monday, May 17, 2004			
Sheet			
35 of 47			

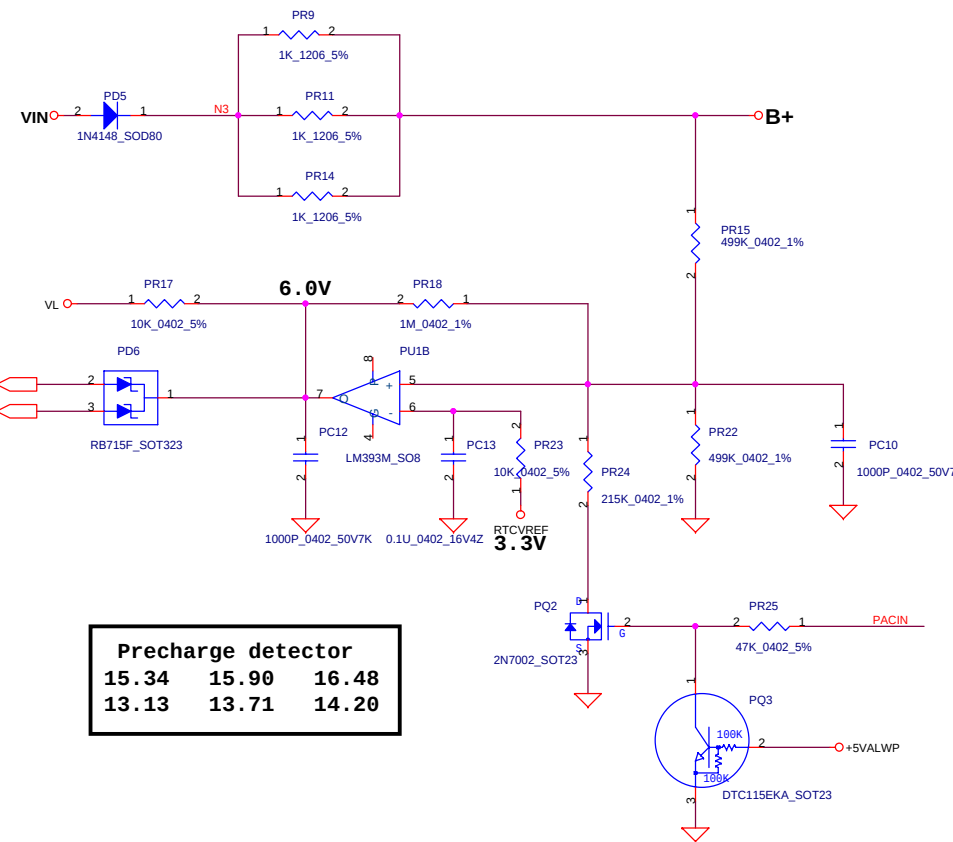
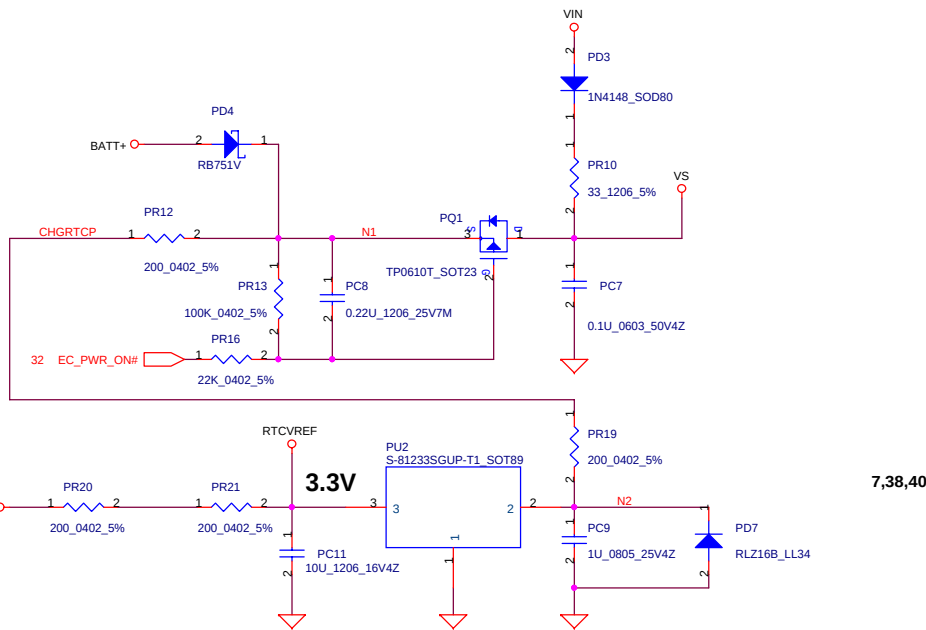


1.8VALW/+1.5VS Power direct provide

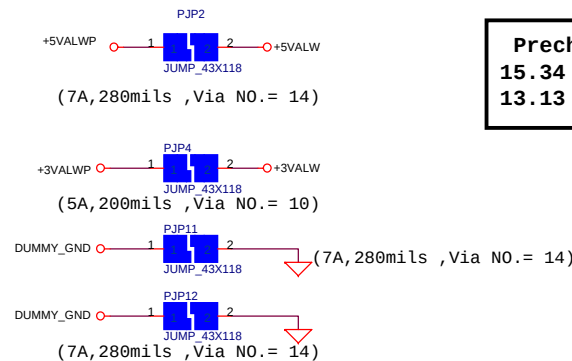
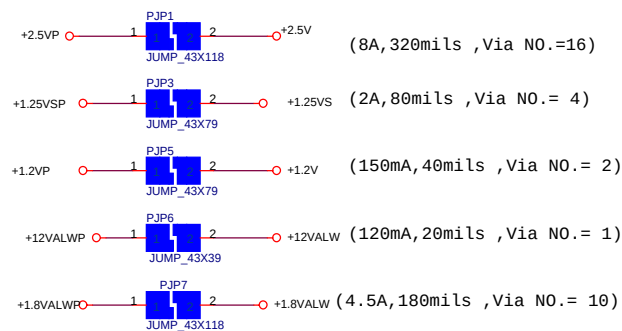




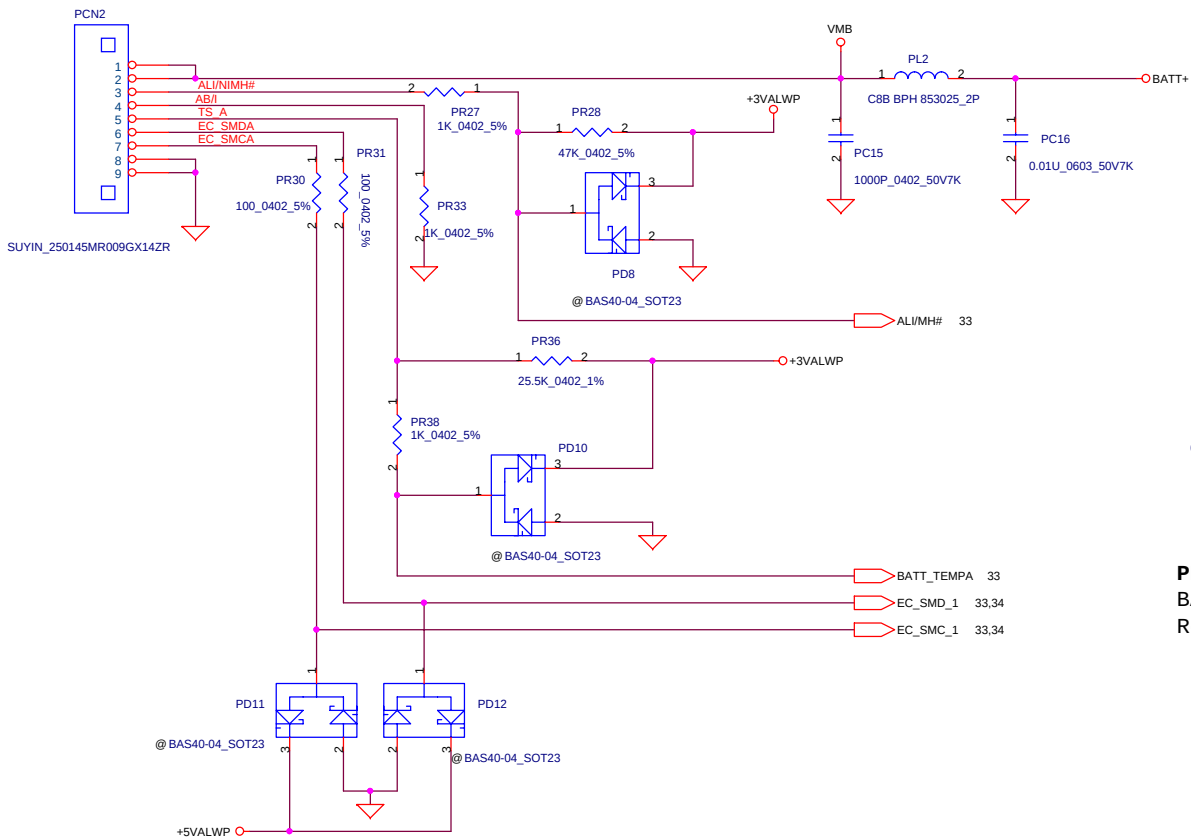
Vin Detector
High 17.58
Low 14.11



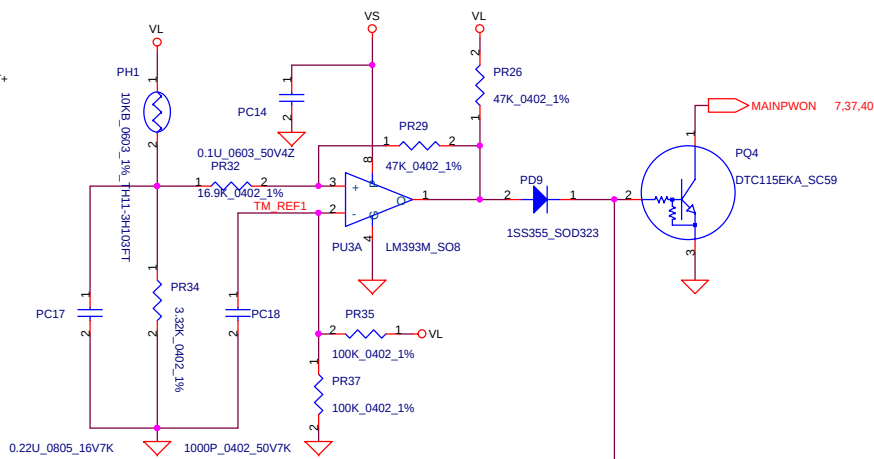
Precharge detector
15.34 15.90 16.48
13.13 13.71 14.20



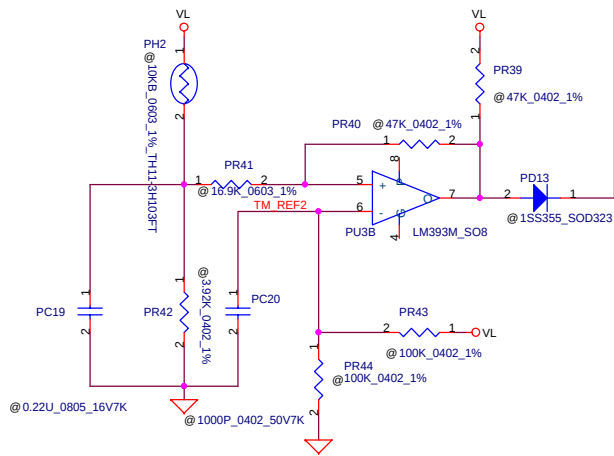
CHANGE CONNECTER



PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 78 degree C
Recovery at 45 degree C



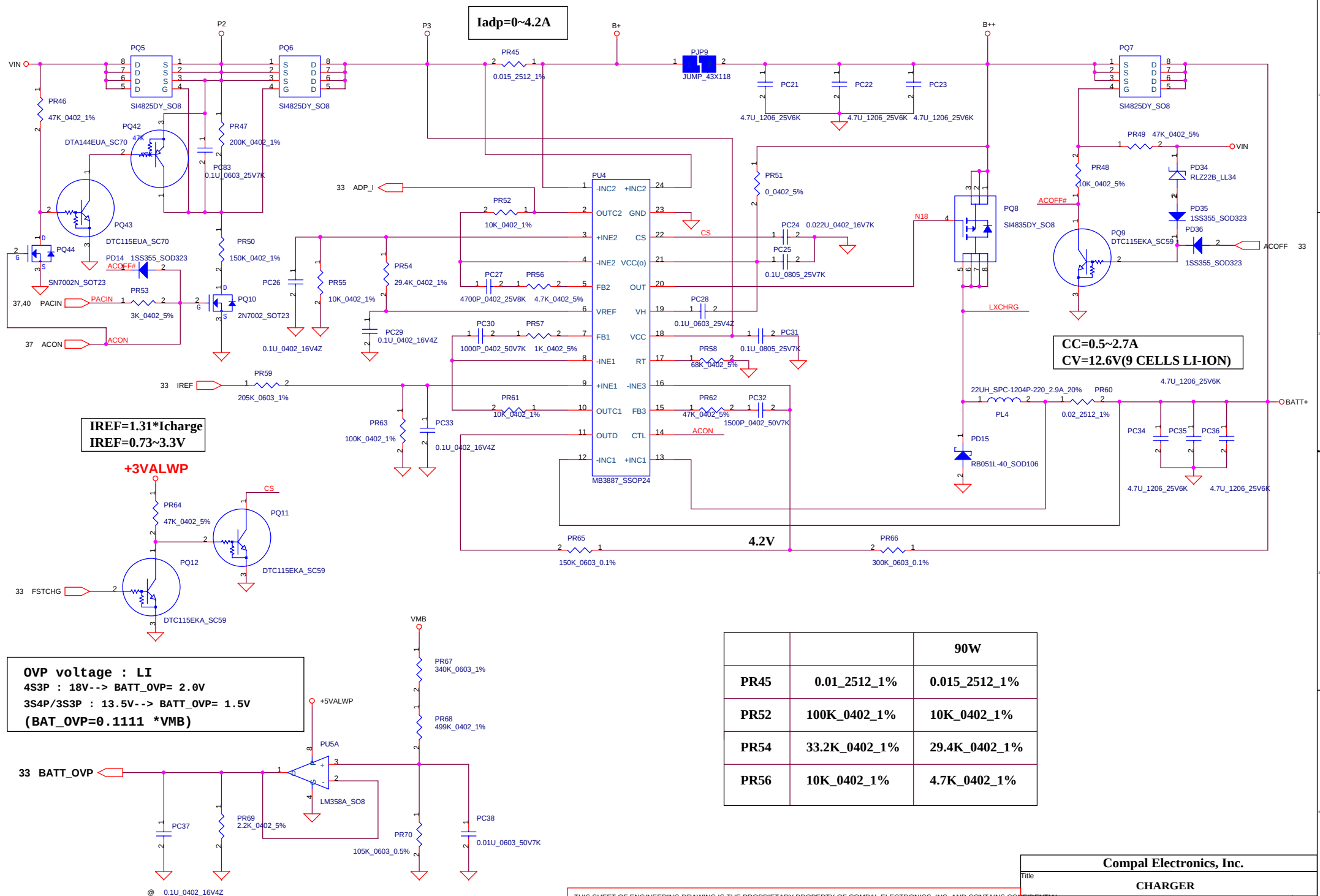
Compal Electronics, Inc.

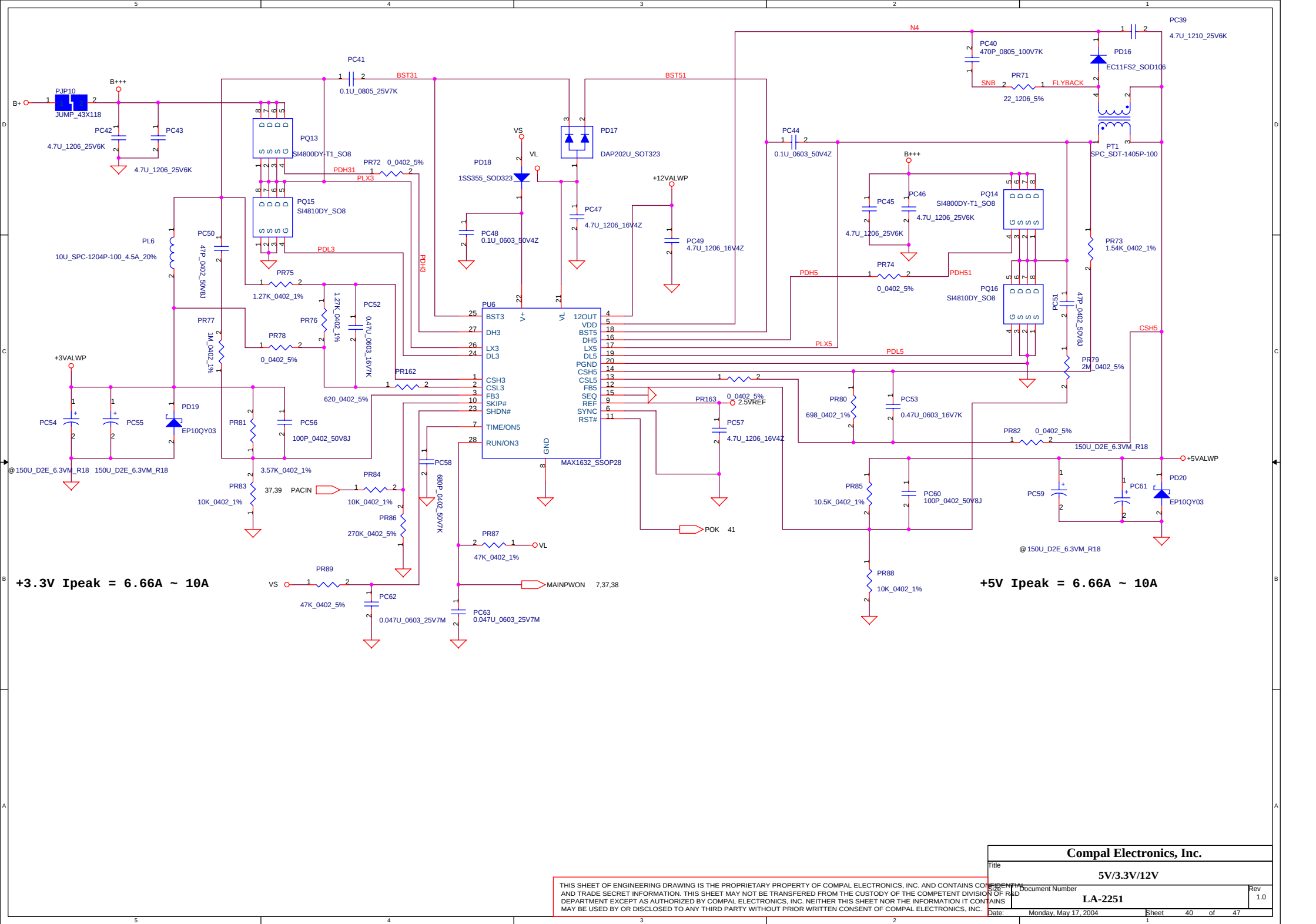
BATTERY CONN / OTP

LA-2251

Rev 1.0

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+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

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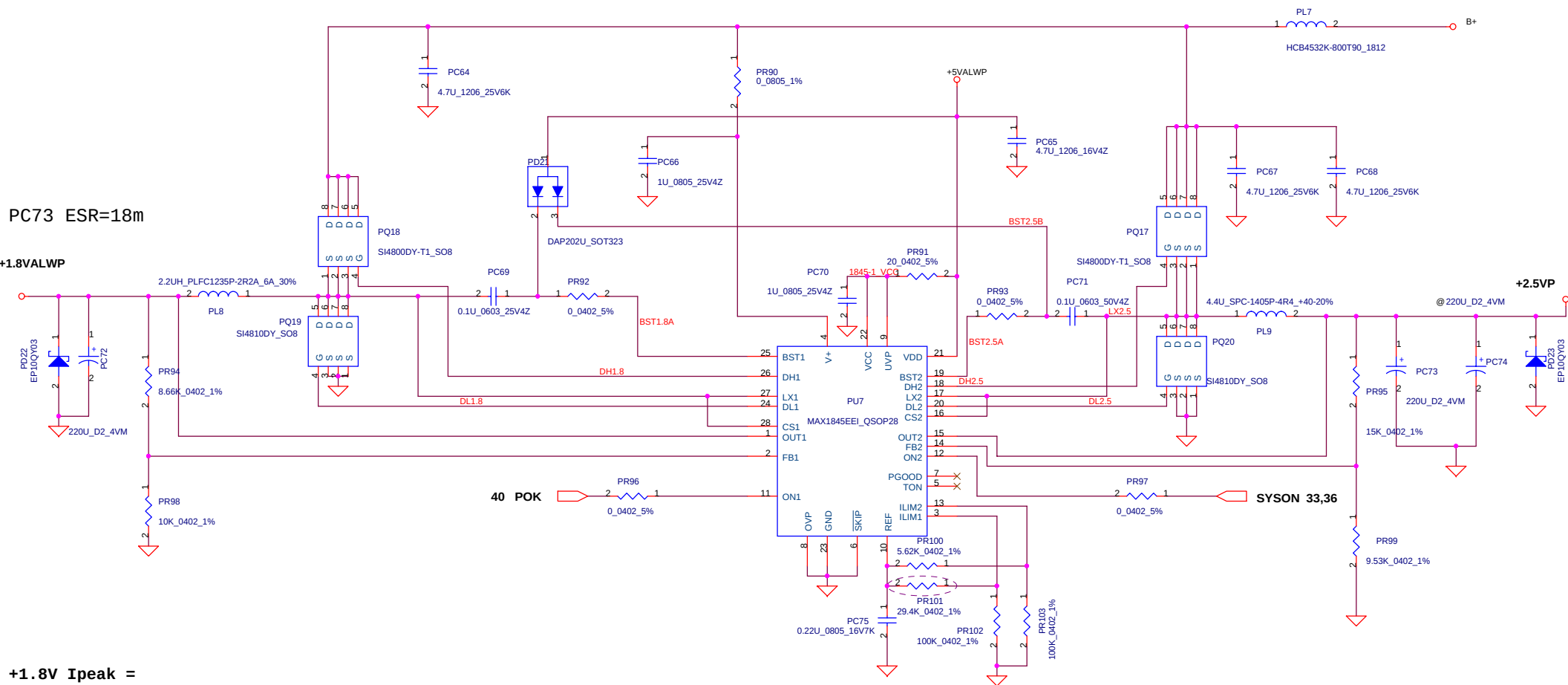
Title		Compal Electronics, Inc.	
Size		5V/3.3V/12V	
Document Number		L/A-2251	
Date		Monday, May 17, 2004	Sheet 40 of 47
Rev		1.0	

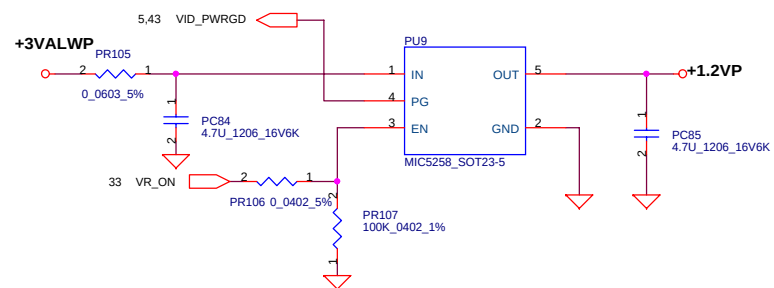
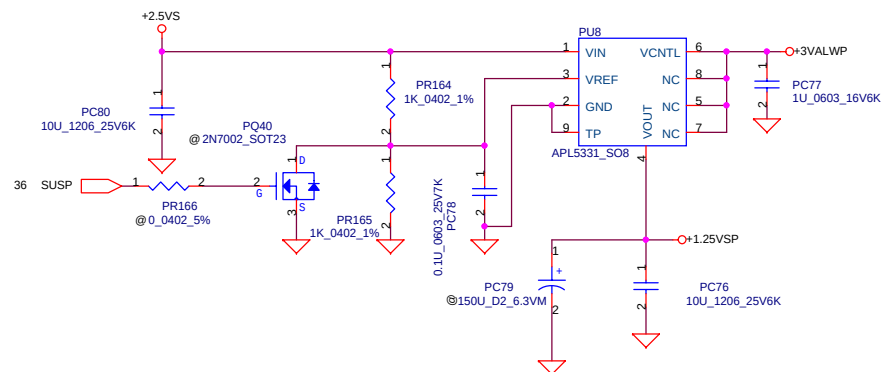
PC73 ESR=18m

+1.8VALWP

+1.8V Ipeak =

+2.5V Ipeak = 12.06A ~ 22.41A

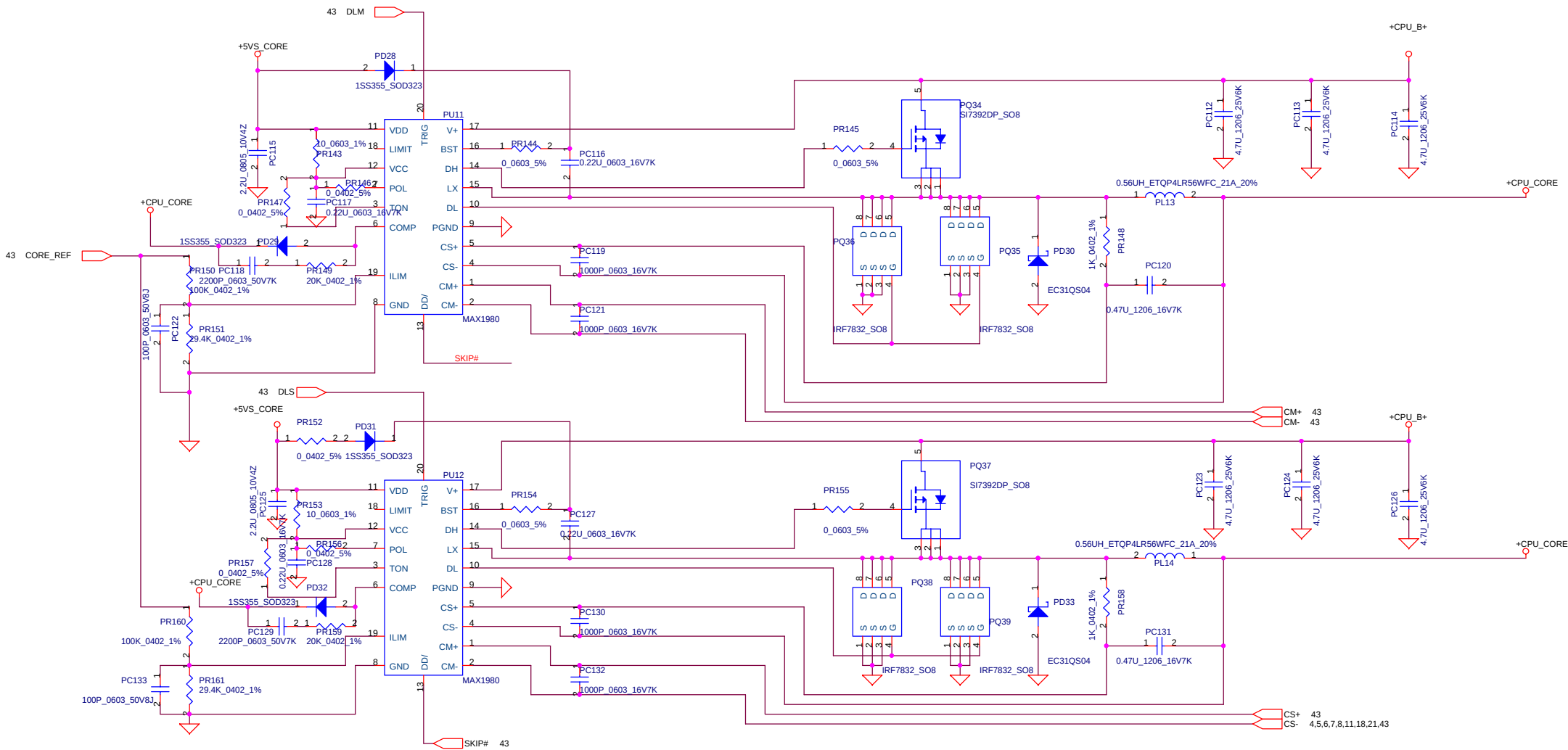




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Compal Electronics, Inc.			
Title		1.25V/1.2V	
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120W	POP	PD28, PC115, PR143, PR144, PC116PR146, PR147, PC117, PD29, PR149, PC118 PR150, PR151, PC122, PU11, PC119, PC121, PQ34, PQ36, PQ35, PD30, PL13, PR148, PC120
90W	UNPOP	PD28, PC115, PR143, PR144, PC116PR146, PR147, PC117, PD29, PR149, PC118 PR150, PR151, PC122, PU11, PC119, PC121, PQ34, PQ36, PQ35, PD30, PL13, PR148, PC120

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Compal Electronics, Inc.		
Title		
+CPU_CORE(2)		
Sheet	Document Number	Rev
44	LA-2251	1.0
Date:	Monday, May 17, 2004	Sheet 44 of 47

Version Change List (P. I. R. List) for Power Circuit

[illegible]

Compal Electronics, Inc.			
Title			
Changed-List History-1			
Size	Document Number		Rev
	LA-2251		1.0
Date:	Monday, May 17, 2004	Sheet	45 of 47

DFY30 from Pre-DB Step to DB-Step LA-2251 REV:0.0 -> 0.1 Modify <92.12.08.~93.02.05. >

1. Pull High 2.2Kohm_0402 from NB_I2CDATA/NB_I2CCLK to +3VS for panel I2C sense function . <Page 16> 92.12.25.

-Add R525,R526(2.2Kohm_0402) and related net . (Modify CKT,BOM&Layout)

2. Add Prescott C-step Processor reserve schematic . <Page 8,18> 92.12.30.

-Reserve R532(@470ohm_0402),R533(@1Kohm_0402),Q44(@2N7002),add R534(0ohm_0402) and related net . (Modify CKT,BOM&Layout)

3. Update ICS952013 CLK GEN. U21 CIS library . <Page 12> 92.12.31.

-Update U21(ICS952013) . (Modify CKT&Layout)

4. Remove ISOLATE function selection resistors for cost down . <Page 25> 92.12.31.

-Remove R49,R429(from 5.1K_0402_5% to @5.1K_0402_5%) . (Modify CKT&BOM)

5. Modify Prescott C-step Processor reserve schematic . <Page 18> 92.12.31.

-Modify net (H_PWRGOOD_SB and EC_ACIN) connection with U28 . (Modify CKT&Layout)

6. Add Pull High schematic for KBC ENE-KB910 . <Page 33> 92.12.31.

-Reserve R202(@10K_0402) for KBA1 . (Modify CKT&Layout)

-Add R194(10K_0402) for KBA4 . (Modify CKT,BOM&Layout)

7. Modify Material for CIS/BOM match . <Page 12> 92.12.31.

-Change C407.C419(from SE077106M00(1206) to SE053106Z00(0805)) . (Modify CKT&BOM)

8. Modify SB GPIO connection and PH/PL states . <Page 18> 93.01.02.

-Add R387,R388,R389(10Kohm_0402);Del R375(51Kohm_0402),R376,R382,R383(10Kohm_0402) . (Modify CKT,BOM&Layout)

9. Add RC temination for Thermal IC ADM1032 recommend . <Page 7> 93.01.05.

-Add R535(0ohm_0402) between +3VALW and U1.1 . (Modify CKT,BOM&Layout)

10. Change AAT14610's enable pin from SYSON to SYSON# . <Page 29> 93.01.05.

-Change U10.4 and U11.4's net from SYSON to SYSON# . (Modify CKT&Layout)

11. Change BIOS IC's P/N and wait CIS updated . <Page 34> 93.01.05.

-Change U15's P/N from SA390400100 to SA390400110 . (Modify CKT&BOM)

12. Remove Modem related EMI/Safety reserve material for cost down . <Page 29> 93.01.05.

-Remove VH1(@DSSA-P3100SB),C294,C295(@220P_1808_3KV8K) . (Modify CKT&BOM)

13. Change SI2306 to SI4800 for Cost Down . <Page 36> 93.01.07. **BOM Release**

-Del Q30(SI2306DS),Add U36(SI4800) and modify related net connection . (Modify CKT,BOM&Layout)

14. Change U25F to U24F for Cost Down . <Page 27> 93.01.07.

-Del U25 , Change U25F to U24F(74LVC14) and modify related net connection . (Modify CKT,BOM&Layout)

15. Correct LCDVDD/B+ EMI solution . <Page 17> 93.01.08. **Net-In 8nd**

-Change L3(from FBM-L11-*_0805 to 0ohm_0805),Add L18(FBM-L11-*_0805) between B+ and JP2.1,remove C215(@68P_0402),Remove Q12(@2N7002) . (Modify CKT,BOM&Layout)

16. Modify the CPU related schematic for Cost Down . <Page 5> 93.01.08.

-Del R26(56ohm_0402) and change the net(H_TESTHI2_7) to RP1.1 PH . (Modify CKT,BOM&Layout)

17. Correct the NET Name for EC define clear . <Page 10,12,18,33> 93.01.08.

-Change the NET from SLP_S3# to S3AUXSW# . (Modify CKT&Layout)

-Change the D26.1&U28.F5's NET from PCL_STOP# to PCICLK_STOP# . (Modify CKT&Layout)

-Change the NET from SLP_S5# to PSON# . (Modify CKT&Layout)

18. Change PCPIRQ connection . <Page 26> 93.01.08.

-Change R115.1 from PCI_PIRQC# to PCI_PIRQB,R117.2 from PCI_PIRQD# to PCI_PIRQB . (Modify CKT&Layout)

19. Modify AC97_Codec related schematic . <Page 27> 93.01.08.

-Add R537(0ohm_0402) between U24.12 and C454.1,add R536(10Kohm_0402) between U23.4 and U23.8 . (Modify CKT,BOM&Layout)

20. Short all Jopen Pad Named JSH? for GerberOut Prepared . <Page 8,9,18> 93.01.08.

-Short JSH1~9(JOPEN) . (Modify CKT&Layout)

21. Remove some parts abot EMI related for cost down . <Page 23,26,27,29,> 93.01.12.

-Remove R69,R121,R153(@10ohm_0402),C184,C259,C478(@15P_0402),C296(@22P_0402) . (Modify CKT&BOM)

22. Remove some parts abot EE related for cost down . <Page 29,> 93.01.12.

-Remove C299,C307,C311(@1000P_0402_50V) . (Modify CKT&BOM)

23. Remove some parts abot USB related for Function Trial . <Page 19> 93.01.12.

-Remove R440,R441,R444(@10K_0402) . (Modify CKT&BOM)

24. Modify Material P/N for BOM correction . <Page 8,9,10,18,19,21> 93.01.12.

-Modify C356,C357,C360,C361,C363,C366,C367,C370,C382,C385,C389,C391,C392,C394,C396,C397,C402,C405,C526,C528,C530,C550,C557,C600(from P/N:SE076103Z00 to SE076103K00) . (Modify CKT&BOM)

25. Modify Material P/N for Purchase Dept. Recommend . <Page 25> 93.01.12.

-Modify C542(from P/N:SE068102K00 to SE074102K00) . (Modify CKT&BOM)

26. Remove some material EMI related for Cost Down . <Page 7,17,23,26,27,32,> 93.01.13.

-Remove C15,C16(@0.001U_0402_50V),C189,C190,C193,C194,C254,C257,C262,C267,C270(@1000P_0402_50V),C2,C3(@22P_0402_25V),C4(@0.1U_0402_16V),C5(@220P_0402_50V),C6,C7,C8,C9(@33P_0402_50V),CP1~CP6(@100P_1206_8P4C_50V8) . (Modify CKT&BOM)

-Change L18(from KC FBM-L11-201209-221LMAT_0805 to 0ohm_0805),L36(from HB-1M2012-121JT03_0805 to 0ohm_0805) . (Modify CKT,BOM&Layout)

27. Modify Material P/N for BOM items simplify (Cost is the same) . <Page 25> 93.01.14.

-Modify C531(22U_1206_16V from P/N:SE021226Z10 to SE021226Z00) . (Modify CKT&BOM)

A-TEST SMT BUILT

DFY30 from DB-Step to Pre SI-Step LA-2251 REV:0.1 -> 0.2 Modify <93.02.06.~93.03.08. >

28. Modify "CPUCLK_STP#" related schematic for Risk fixed and Cost Down . <Page 5,12,18> 93.02.16.

-Add Q45(SB339040100) , R539(SD028120200) , R540(SD028100100) and R541(SD028000000);del D27(SC1B751V005) & R278(SD028100200) and modify the related schematic . (Modify CKT,BOM&Layout)

29. Modify "PWRBTN_OUT#" related schematic for Cost Down . <Page 18> 93.02.16.

-Modify "PWRBTN_OUT#" related schematic and del R381(SD028100200) . (Modify CKT,BOM&Layout)

30. Change "FANSPEED1" and "FANSPEED2" pull high power source from +5VS to +3VS for power saving . <Page 7> 93.02.16.

-Change R12.1 and R13.1's connection from +5VS to +3VS . (Modify CKT&Layout)

31. LCD Connector combined with Inverter Connector for cost down . <Page 17> 93.02.16.

-Modify the related schematic and del JP2 . (Modify CKT,BOM&Layout)

32. Remove TV-OUT function . <Page 17> 93.02.16.

-Modify the related schematic and del D12,D13,D14,L5,L8,L9,C232C233,C234,C235,C236,C237,R97,R98,R99,JP19 . (Modify CKT,BOM&Layout)

33. Modify PCMCIA spec from 2 slots to 1 slot . <Page 23> 93.02.16.

-Change U4 CB1420 to CB1410 and U5 CP2216 to CP2211 , del R85,D6,R75,C195,C196,R77~R81,C211,C212,C213,C204,C203,C207,R87 , add C699 . (Modify CKT,BOM&Layout)

34. Change SI2302 to SI4800 for Cost Down . <Page 17> 93.02.16.

-Change Q13(P/N: SB523020005) to U40(P/N: SB548000100) and modify the related schematic (Modify CKT,BOM&Layout)

35. Add IEEE1394 function and related schematic/material . <Page 24> 93.02.16.

-Add C701,C702,C703,C704,C705,C706,C707,C708,C709,C713,C710,C711,C712,C714,C715,C716,JP23,R543,R547,R544,R545,R546,R550,R551,R548,R549,R552,R553,R554,R555,U38,U39,X1 and modify the related schematic . (Modify CKT,BOM&Layout)

36. Change JP9 from P/N: SP010019210 to SP010009910 for cost down . <Page 32> 93.02.16.

-Change JP9 from P/N: SP010019210 to SP010009910 , del R508,R509,R510,R523,C684,C685,C686,C694 and modify the related schematic . (Modify CKT,BOM&Layout)

37. Modify BIOS pin definition and remove BIOS beffer IC for cost down plan . <Page 33,34> 93.02.16.

-Del U13,U14,RP33,C331,RP32,R186,R189,C333,C332,R188 and modify the related schematic . (Modify CKT,BOM&Layout)

38. LED function re-defined for cost down plan . <Page 32,33> 93.02.20.

-Del C688,C690,R512,R514, and modify the related schematic . (Modify CKT,BOM&Layout)

39. Issue BEEP# from EC pin directly for cost down plan . <Page 27> 93.02.22.

-Move U6,U24 location ; Del R305,R308,R303(@),R537,C457 and modify the related schematic . (Modify CKT,BOM&Layout)

40. Add EMI request schematic for Inverter related reserved . <Page 17> 93.02.22.

-Add L59,L60,L61,L62(close to JP6) and modify the related schematic . (Modify CKT,BOM&Layout)

41. Add pull down design for "SYSON","SUSP#","EC_RSMRST#" floating risk . <Page 33> 93.02.22.

-Add R556,R557,R558(close to U12) and modify the related schematic . (Modify CKT,BOM&Layout)

42. Modify the "PCI_RST#" related schematic for Cost Down verified and prepared . <Page 20> 93.02.23.

-Add R559,R560,C717,R561,R562,R565; (Remove U24,C380,C452(@)) and modify the related schematic . (Modify CKT,BOM&Layout)

43. Change Reset IC from MAX6342RUT to MAX809SEUR for Cost Down . <Page 35> 93.02.23.

-Add U41,R563,R564 ; (Remove U32,R460,R461,R462(@)) and modify the related schematic . (Modify CKT,BOM&Layout)

----PLEASE SEE NEXT PAGE

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H/W2 EE Dept. PIR SHEET(1)

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DFY30 from DB-Step to Pre SI-Step LA-2251 REV:0.1 -> 0.2 Modify <93.02.06.~93.03.09. >

44. Reserve EMI request design for LVDS clock related signal . <Page 9,16> 93.02.23.

-Add R566(@),C718(@),R567(@),R568(@),C719(@),C720(@),move R215 (close to U22) and modify the related schematic . (Modify CKT&Layout)

45. Create +PWR_PCM for U4(CB1410) core power +3VALW and +3VS power source option . <Page 23> 93.02.25.

-Modify the related schematic to change +3VALW to +PWR_PCM . (Modify CKT&Layout)

46. Reserve +3VS power source option for U4(CB1410) pin18&44 . <Page 23> 93.02.25.

-Add R569(@),R570(@)(close to U4) and modify the related schematic . (Modify CKT&Layout)

47. Reserve some CAPs for Power Plane through mode risk improved . <Page 36> 93.02.25.

-Add C721~C726(@) and modify the related schematic . (Modify CKT&Layout)

48. Cancel VGA_GND for EMI request . <Page 16,17> 93.03.02.

-Del L54,L55,L56,L57 and modify the related schematic . (Modify CKT,BOM&Layout)

49. Remove MiniPCI Modem function . <Page 26> 93.03.02.

-Del R123 , C266(@),C267(@),R122(@),C263(@) and modify the related schematic . (Modify CKT,BOM&Layout)

50. Remove MiniPCI Modem function . <Page 27> 93.03.03.

-Del R333, Remove R334,C484(Close to Pin22) and modify the related schematic . (Modify CKT,BOM&Layout)

51. Modify Pull High Resistor Value from 100K to 10K for standard design . <Page 12> 93.03.03.

-Modify R527 from 100Kohm to 10Kohm . (Modify CKT&BOM)

52. Remove some parts because remove ACER keyboard function . <Page 32> 93.03.03.

-Remove Q1,R4,R5,R6 . (Modify CKT&BOM)

53. Add the Pull High Resistor to enable the VGA tuned function for SIS request . <Page 09> 93.03.03.

-Add R210 (P/N: SD028470100/ S RES 1/16W 4.7K +-5% 0402) . (Modify CKT&BOM)

54. Modify the resistor's value to 1Mohm for SI4800 design . <Page 17> 93.03.03.

-Change R91(P/N: SD028150300 to SD028100400) . (Modify CKT&BOM)

55. Modify NB_RST# related and change LPC_RST# resistor value for signal quality improved . <Page 20> 93.03.09.

-Change R346(0ohm->10ohm) ; Add R571(10ohm) . (Modify CKT,BOM&Layout)

56. Change SIS302ELV pin60 level latch power source from +3VS to +1.8VS(same as SIS661FX U18.W3 power source) for SIS Design Change . <Page 16> 93.03.09.

-Change L47.1's power source from +3VS to +1.8VS . (Modify CKT&Layout)

57. Modify PCI_RST# related and change PCI_RST# resistor value for signal rising time risk fixed . <Page 20> 93.03.18.

-Change R562(1Kohm->300ohm);R565(2Kohm->620ohm);Remove C717(10PF_0402).(Modify CKT&BOM)

58. Modify PM_PWRGD related and change PM_PWRGD resistor value for signal rising time risk fixed . <Page 35> 93.03.18.

-Change R563(1Kohm->300ohm) ; R564(2Kohm->620ohm) . (Modify CKT&BOM)

59. Pull Down BT_WAKE_UP signal . <Page 33> 93.03.19.

~~-Add C330(100K_0603ohm;SD0131003T1) . (Modify CKT&BOM)~~

60. Change Material to meet Layout Size . <Page 30> 93.03.19.

-Change C503(10U_1206->10U_0805)(SE054106Z10->SE054106Z10) . (Modify CKT&BOM)

61. Disconnect CPUCLK_STP# to CLK_GEN . <Page 12> 93.03.19.

-Remove R541(@0ohm) . (Modify CKT&BOM)

62. Update PCMCIA SOCKET JP15 Library . <Page 23> 93.03.22.

-Update JP15 CIS library . (Modify CKT&Layout)

63. Correct H_FERR# have double Pull High problem . <Page 05> 93.04.05.

~~-Remove R18(56ohm) . (Modify CKT&BOM)~~

64. Modify JP26 pin4 connection for Pioneer ODD(DVD Dual DVR-K12TBC/DVR-K13TBC) used . <Page 22> 93.04.08.

-Reserve R572(@0ohm_0402) . (Modify CKT,BOM&Layout)

65. Add Decoupling Capacitor 220PF close to DDR Clock Buffer for EMI request . <Page 13> 93.04.10.

-Add C728,C729(220PF_0402) close to U20 . (Modify CKT,BOM&Layout)

66. Add Decoupling Capacitor 220PF close to NB M661FX VDDM for EMI request . <Page 11> 93.04.10.

-Add C730,C731,C732(220PF_0402) close to U18 . (Modify CKT,BOM&Layout)

67. Modify H_TESTHI2_7 Pull-High Resistor connection for Layout placement issue . <Page 05> 93.04.10.

-Add R573(56ohm_0402) close to JP25 . (Modify CKT,BOM&Layout)

68. Del H19 for PCB space free . <Page 30> 93.04.10.

-Del H19 . (Modify CKT&Layout)

69. Modify Audio Codec pins connection related to fix the noise issue . <Page 27> 93.04.12.

-Remove C467(@0.1UF_0402) . (Modify CKT&BOM)

-Reserve C733,C734(@0.1UF_0402) . (Modify CKT&Layout)

70. ~~Modify JP32 power source pins connection for new CardReader Board cost down and SB chip power issue fixed . <Page 29> 93.04.12.~~

~~-Change JP32.1&JP32.7 from +5VS to +3VALW ; JP32.2&JP32.8 from +5VS to +3VS . (Modify CKT&Layout)~~

71. Modify the USB ports definition and related connection for SB USB power source issue improved . <Page 19,29> 93.04.12.

-Change USB ports from P0 to P3 ; P3 to P5 ; P5 to P4 ; P4 to P0 . (Modify CKT&Layout)

-Remove OVCUR#5 R496(@10K_0402) , Add OVCUR#0 R440(10K_0402) . (Modify CKT&BOM)

72. Add BT_WAKE_UP Pull Down resistor . <Page 33>93.04.12.

-Add R574(100Kohm_0402) . (Modify CKT,BOM&Layout)

73. Add some material to BOM for EMI request . <Page 9,13,19>93.04.15.

-Add C406,C545(10PF_0402) . (Modify CKT&BOM)

-Add R566,R442(12ohm_0402) . (Modify CKT&BOM)

-Add C718(15PF_0402) . (Modify CKT&BOM)

74. Modify H_PROCHOT# connection and add EC_PROCHOT# pin for Throttling function control by EC . <Page 5,18,33>93.04.19.

-Add R21 (62ohm_0402)(Because SB Int. PH disconnection) . (Modify CKT&BOM)

-Remove R378(0_0402) ; Add R578(0_0402) to connect CPU and EC CTRL(U12.92) . (Modify CKT,BOM&Layout)

75. Correct H_FERR# have double Pull High problem . <Page 18> 93.04.19.

-Del RP87.6(H_FERR# connection) . (Modify CKT&Layout)

76. Modify IEEE1394 related schematic for the Vendor VIA recommend . <Page 24> 93.04.19.

-Add R576(0ohm_0805) . (Modify CKT,BOM&Layout)

-Add C735,C736,C737,C738(0.1UF_0402) . (Modify CKT,BOM&Layout)

-Remove R544(1Kohm_0402) . (Modify CKT&BOM)

-Connect R550.2,R551.2,R552.1&C712.1 . (Modify CKT&Layout)

77. Disconnect JP8.36(WLAN_PME#) for normal design . <Page 26> 93.04.19.

-Reserve R579(@0ohm_0402) . (Modify CKT&Layout)

78. Change VBCAD's Pull-High Power Source from +3VS to +1.8VS for the vendor SIS recommend . <Page 16> 93.04.19.

-Change R384.1's connection from +3VS to +1.8VS . (Modify CKT&Layout)

79. Modify JP32 power source pins connection for new CardReader Board cost down and SB chip power issue fixed option . <Page 29> 93.04.19.

-Change JP32.1/2/7/8 from +5VS only to+5VS(JOPEN3)/+3VALW(JOPEN4) option . (Modify CKT,BOM&Layout)

80. Disconnect MDC Connector JP14.29 for power consumption save . <Page 29> 93.04.19.

-Reserve R575(@0_0402) between JP14.29 and GND . (Modify CKT&Layout)

81. Modify LPC_RST# and NB_RST# related resistor value to fix signal quality issue . <Page 20> 93.03.18.

-Change R346(0ohm_0402->10ohm_0402) ; Add R571(10ohm_0402) . (Modify CKT,BOM&Layout)

DFY30 from PV-Step to Pre MV-Step LA-2251 REV:0.3 -> 1.0 Modify <93.04.19.~93.05.27. >

82. Modify Audio AMP LIN/RIN CAPs' value to improve audio noise issue . <Page 28> 93.04.29.

-Change C283,C284 from 0.47UF_0603 to 22PF_0603 . (Modify CKT&BOM)

83. Modify Audio AMP FADE# pin define to improve audio noise issue . <Page 28> 93.04.29.

-Change U9.16(FADE#)'s connection from AGND to +5VAMP by 10Kohm resistor(R580_0402) . (Modify CKT,BOM&Layout)

84. Change EC_SMD_2/EC_SMC_2's pull high power source from +3VALW to +5VALW because ENE_KB910 SMBUS1/2 use the same power level . <Page 33> 93.05.05.

-Change RP31.7/RP31.8 from +3VALW to +5VALW . (Modify CKT&Layout)

85. Modify SI102221K05 to SI102221K10 for material shortage issue . <Page 31> 93.05.13.

-Change CP7,CP8,CP9 from SI102221K05 to SI102221K10 . (Modify CKT&BOM)

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