

Desert Eagle
LA-3161P

Compal confidential

HEL80/HEL81 Schematics Document

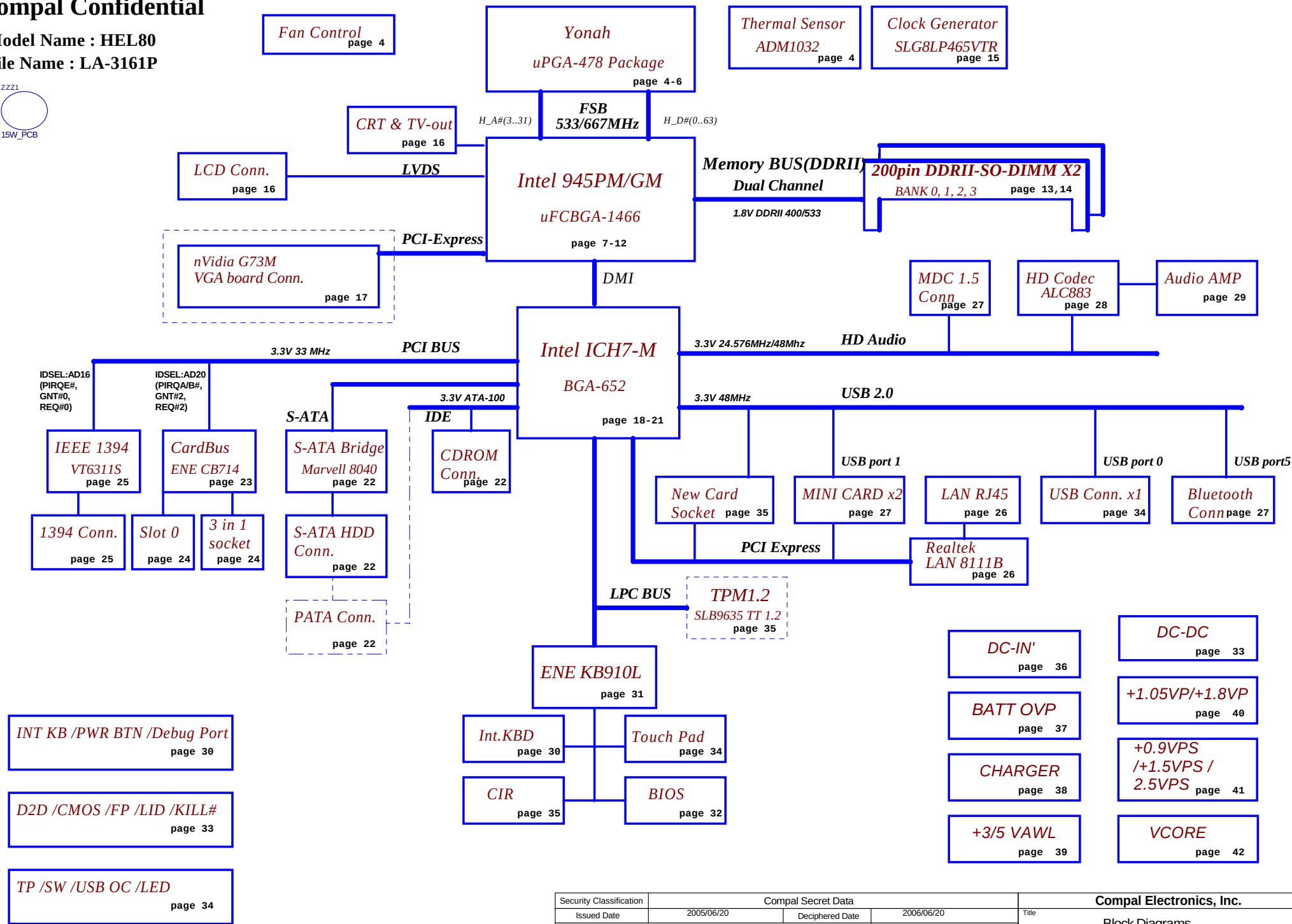
Mobile Yonah uFCPGA with Intel
Calistoga_GM/PM+ICH7-M

Thursday, February 23, 2006
REV: 0.3

Security Classification		Compal Secret Data		Title	
Issued Date		2005/10/06		Deciphered Date	
		2006/10/06		2006/10/06	
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HEL80 LA-3161P				0.3	
Sheet				1 of 43	

Compal Confidential

Model Name : HEL80
File Name : LA-3161P



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Size	Custom	Document Number	HEL80 LA-3161P	Rev	0.2
Date		Thursday, February 23, 2006		Sheet	2 of 43

Voltage Rails

power plane State	+B LD03 LD05	+5VALW +3VALW	+1.8V +5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.2VS +VGA_CORE +0.9VS +CPU_CORE +VCCP
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

0 MEANS ON
X MEANS OFF

S3 : STR
S4 : STD
S5 : SOFT OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/B
1394	AD16	0	PIRQE

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		

ICH7 SM Bus address

Device	Address
Clock Generator (SLG8LP465VTR)	1101 001Xb
DDRII DIMM0	1010 000Xb
DDRII DIMM1	1010 010Xb

SKU ID Table

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

SKU ID	HEL80/81 SKU
* 0	HEL80 SKU
1	HEL81 SKU
2	TEST MODE
3	
4	
5	
6	
7	

BOM Structure

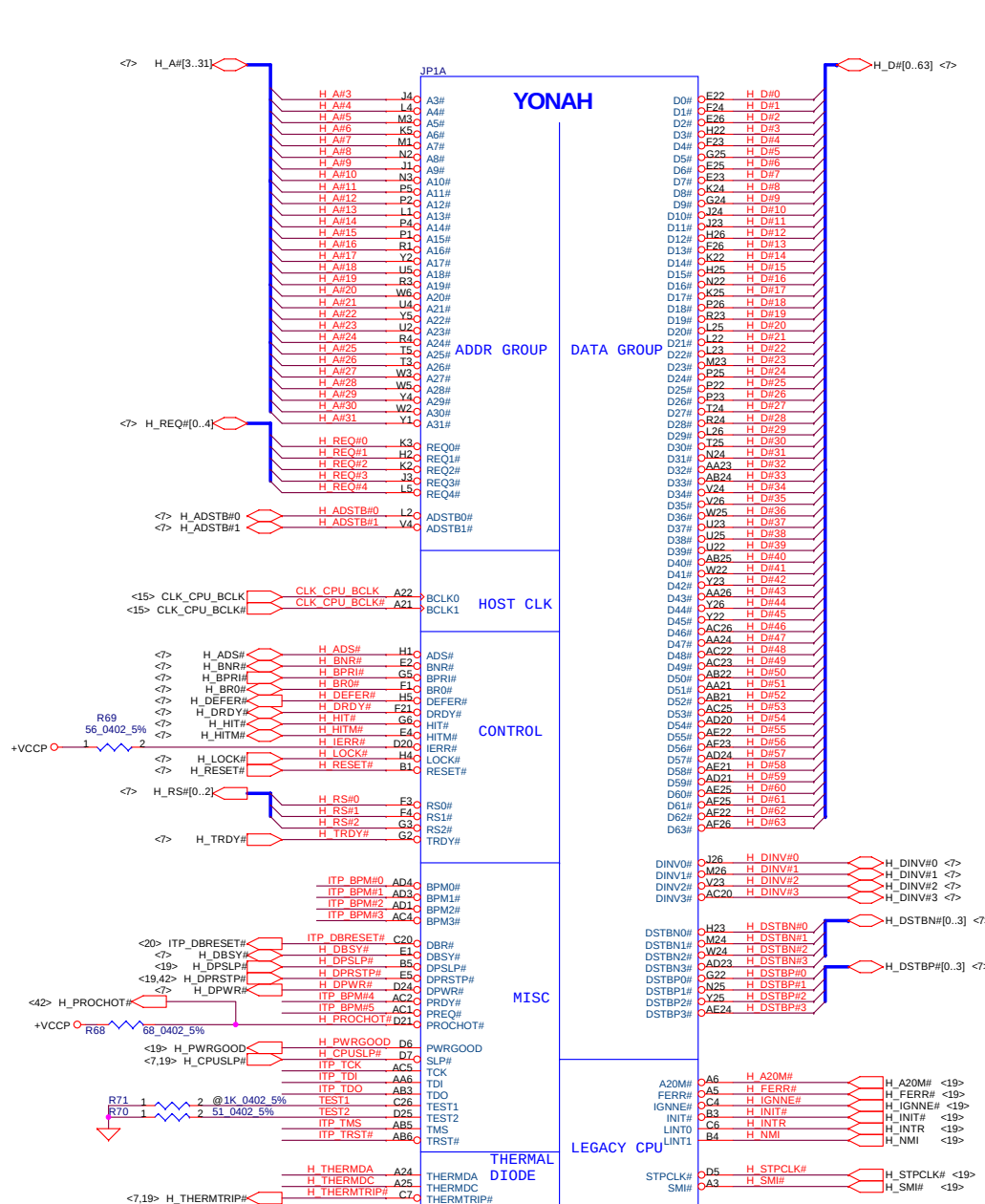
MARK	FUNCTION
@	NC FOR ALL
UMA@	Internal 945GM
VGA@	External G7xM
TPM@	TPM1.2
CIR@	CIR
1394@	1394
SATA@	SATA HDD
8040@	PATA HDD
IOMP@	IOMP
15W@	15W PANEL
APA@	HP out from AMP
HPA@	HP out from HP AMP
HP@	HP out from CODEC

USB PORT LIST

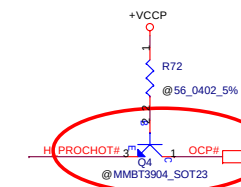
PORT	DEVICE
0	LEFT SIDE
1	BLUE TOOTH
2	RIGHT SIDE
3	CMOS
4	RIGHT SIDE
5	FINGER PRINTER
6	NEW CARD
7	TV

+3VALW	KB910L SB RTL8110SBL/CL	mA 160mA
+CPU_CORE	CPU	36A
+VCCP	CPU NB	2.5A 9.8A (14.7A)
+5VS	EXPRESS CARD HDD ODD MDC APA2066 TPA0211 AD1986 USB PORT * 6	1A 1.5A 1.8A 300mA 1A mA 70mA 3A
+3VS	NB EXPRESS CARD CLK_GEN LCDVCC VGA CARD (G7XM) SB R5C832 BIOS ROM KB910L CB1410	480mA 1A 200mA 1A 655mA 680mA mA 15mA 200mA mA
+2.5VS	VGA CARD (G7XM) NB	130mA (143mA)
+1.8V	DDR2_DIMM NB (667Mhz)	8A 3.1A
+1.8VS	GDDR2 VGA CARD (G7XM)	6A 4.06A
+0.9VREF	DDR2_DIMM	10mA
+0.9VS	GDDR2 DDR2_DIMM	1A 2A
+1.5V	SB	40mA
+1.5VS	NB SB MiniCard EXPRESS CARD VGA CARD (G7XM)	8.9A(13.8A) 3.8A 1A 0.65A 2A

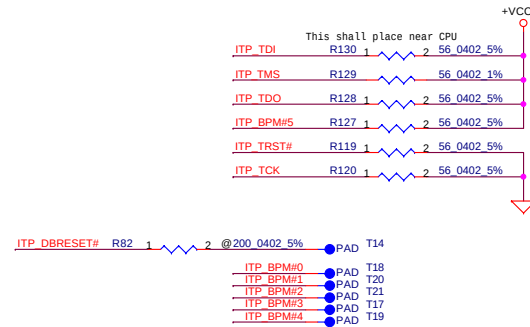
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				Size	Document Number	Rev
					HEL80 LA-3161P	0.2
				Date:	Thursday, February 23, 2006	Sheet 3 of 43



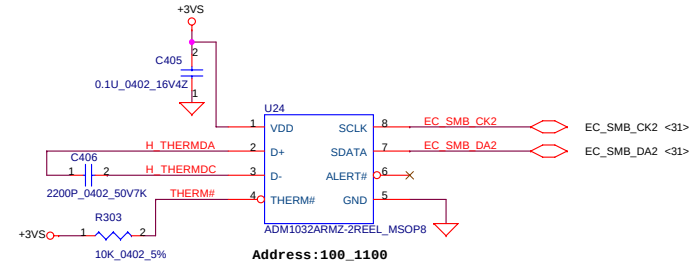
H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil



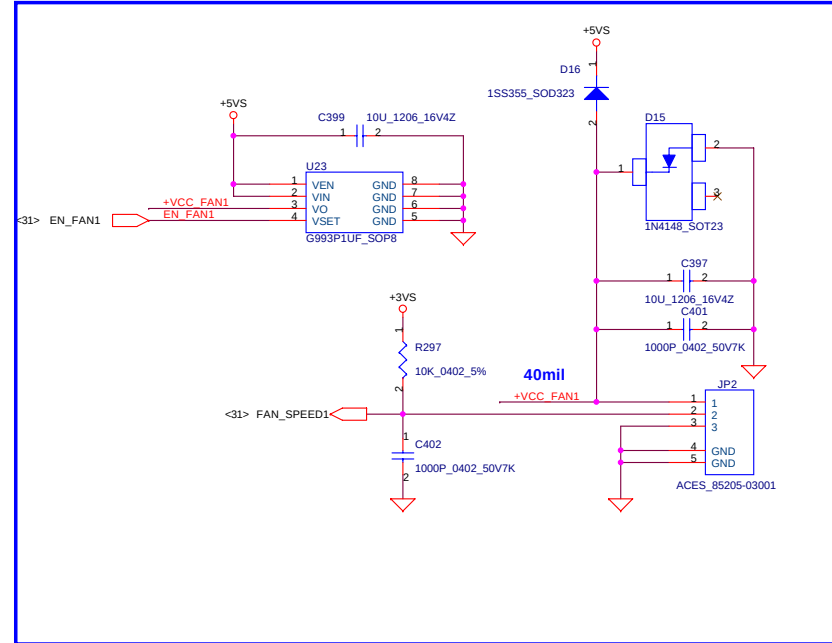
2005/11/07
Modified Q4 part number to SB039040000.



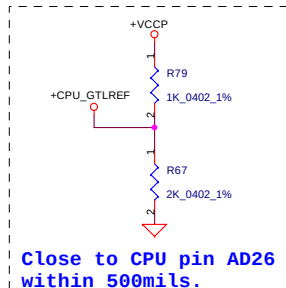
Thermal Sensor ADM1032AR



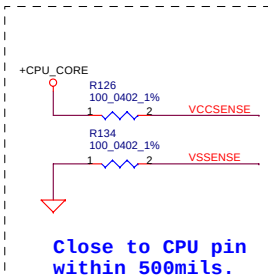
Note : ADM1032 has no S08 lead free ones.Only MS08



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				Date	Thursday, February 23, 2006
				Sheet	4 of 43

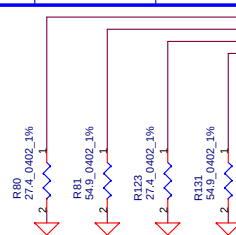


Trace / Width = 4 / 25 mils

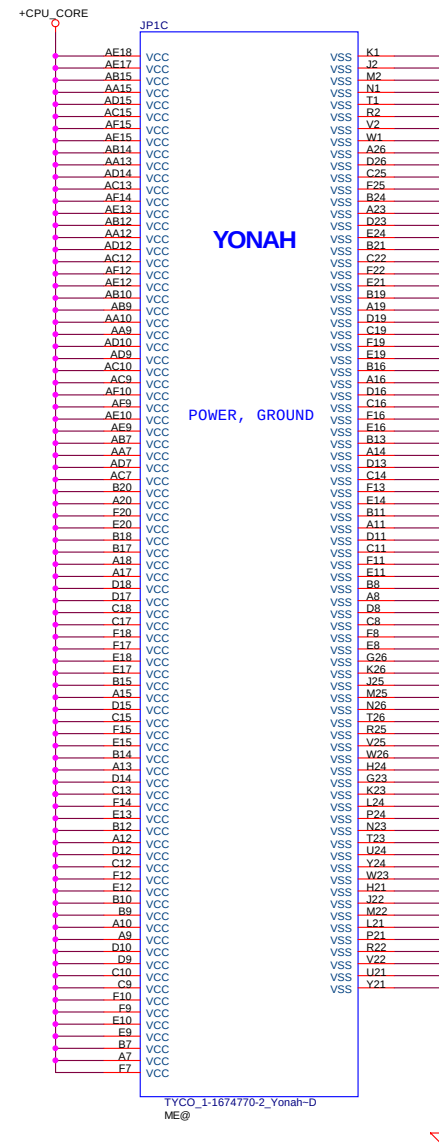
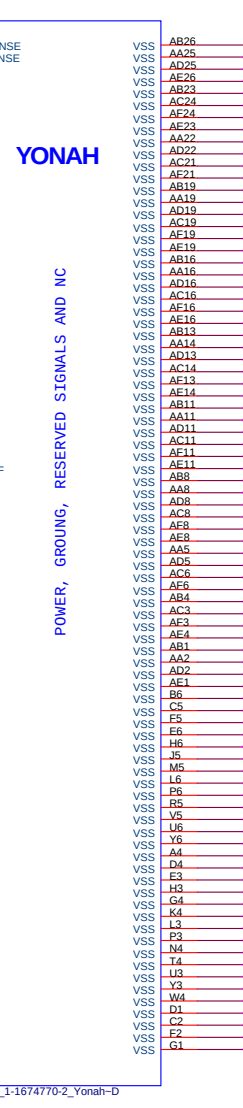
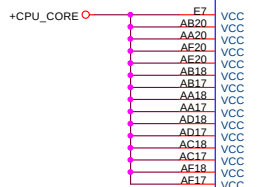
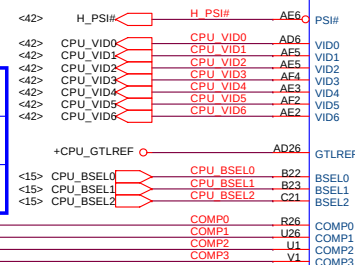
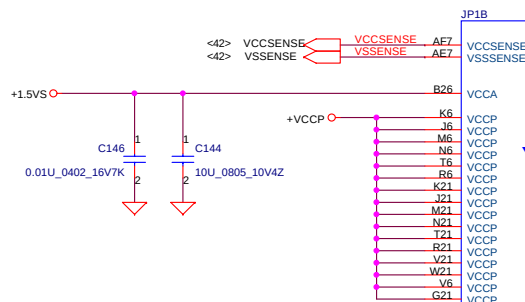


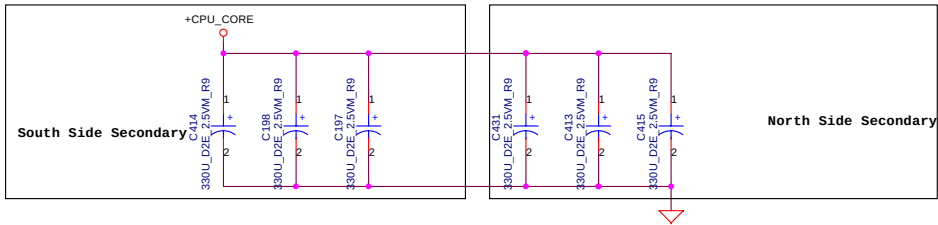
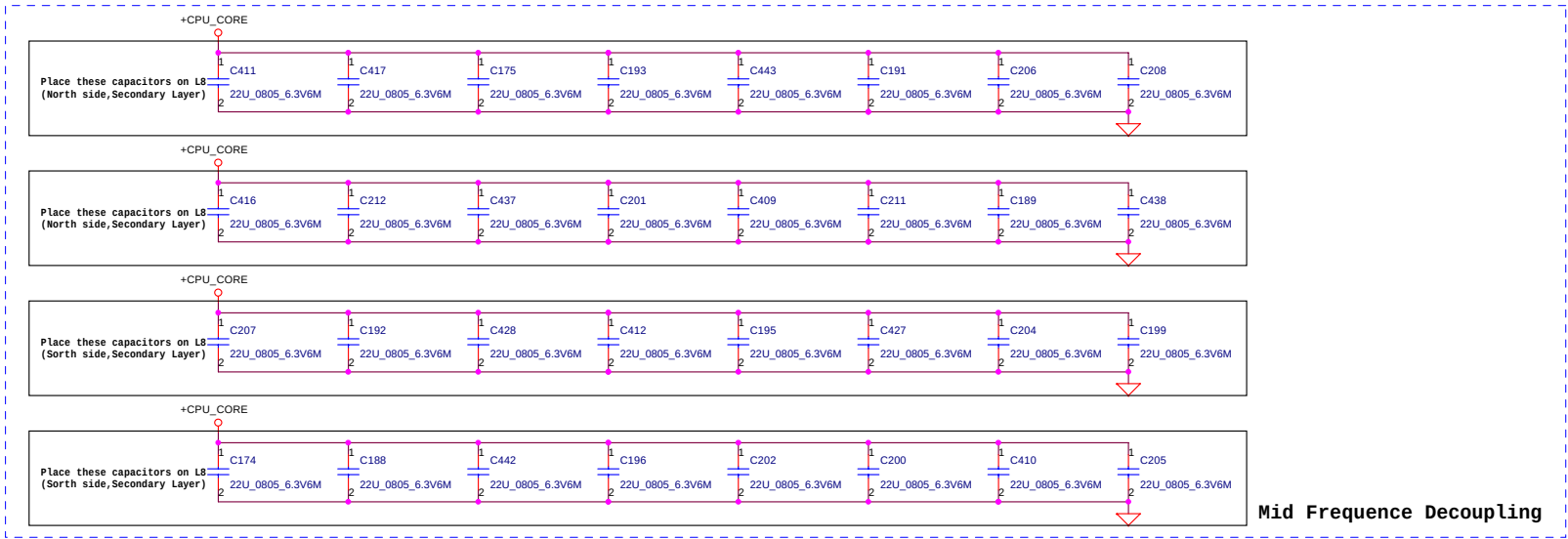
Trace / Width = 18 / 50 mils

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

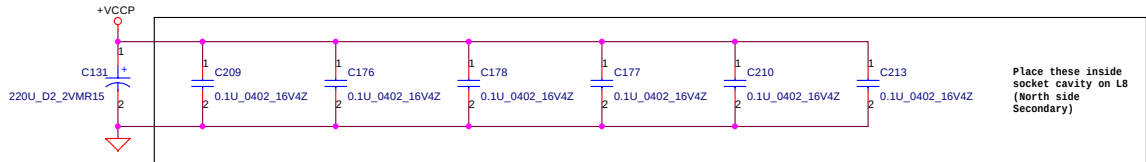


COMP 0/2 Trace / Width = 18 / 25 mils
COMP 1/3 Trace / Width = 5 / 25 mils

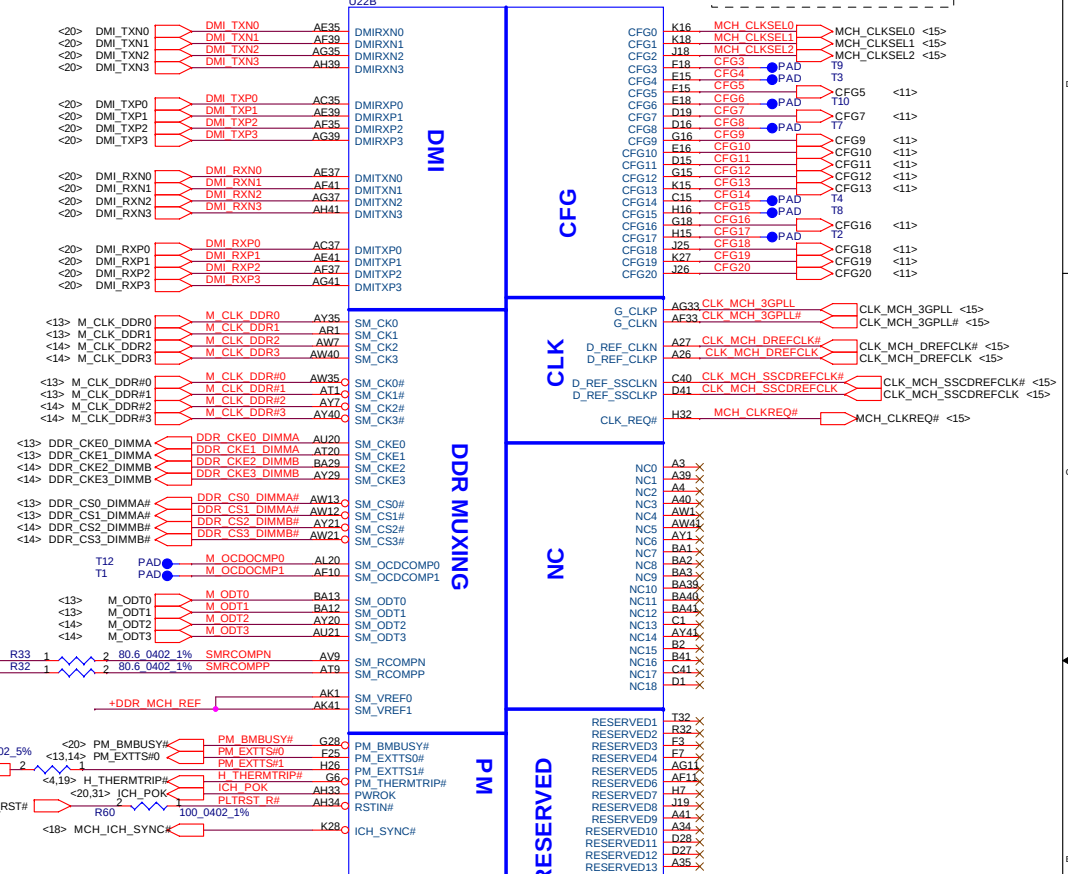
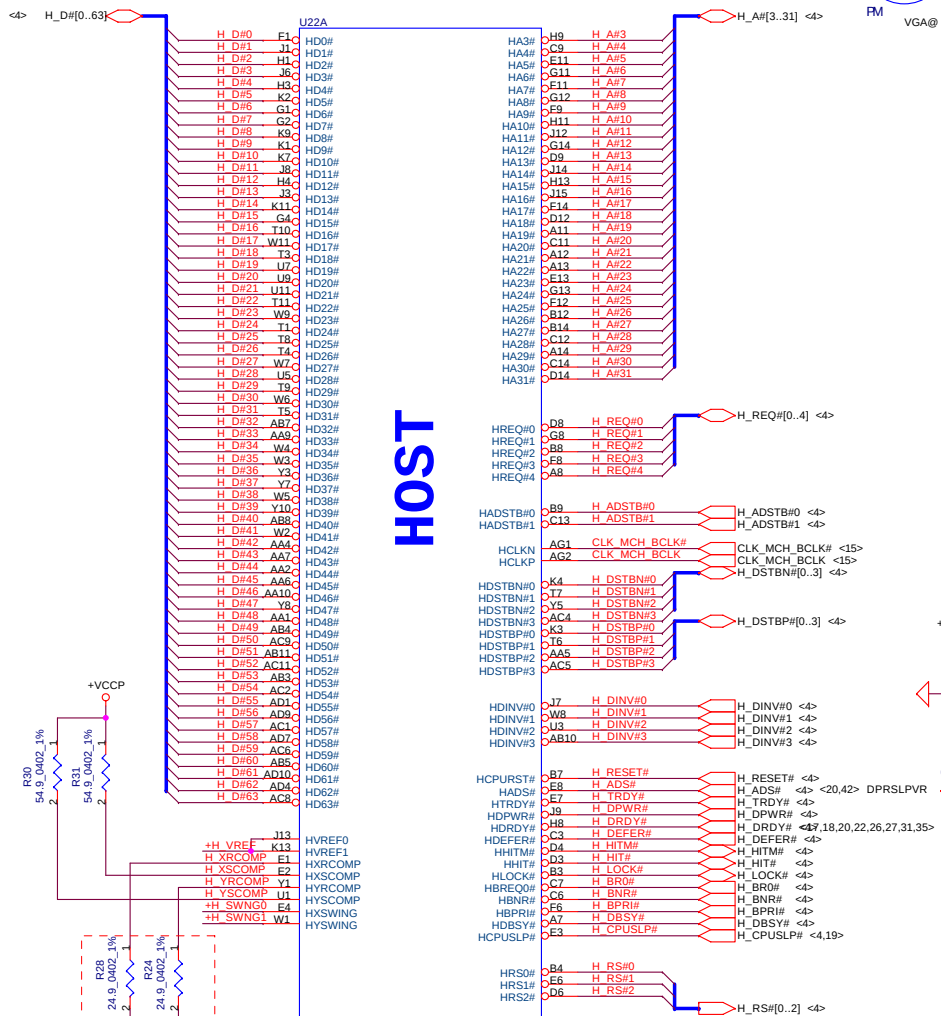




ESR <= 1.5m ohm
Capacitor > 1980uF



Note : 2005/12/26 modify pm
PM : SA00000KDC0
GM : SA0000059H0

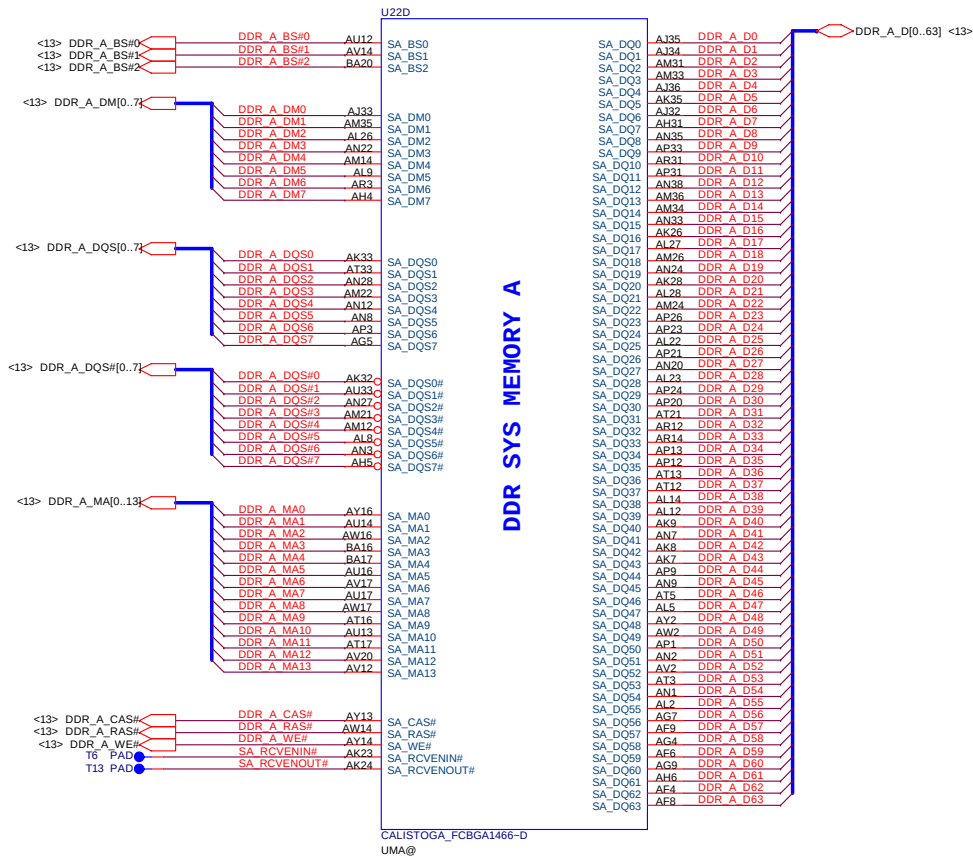


Description at page 11.

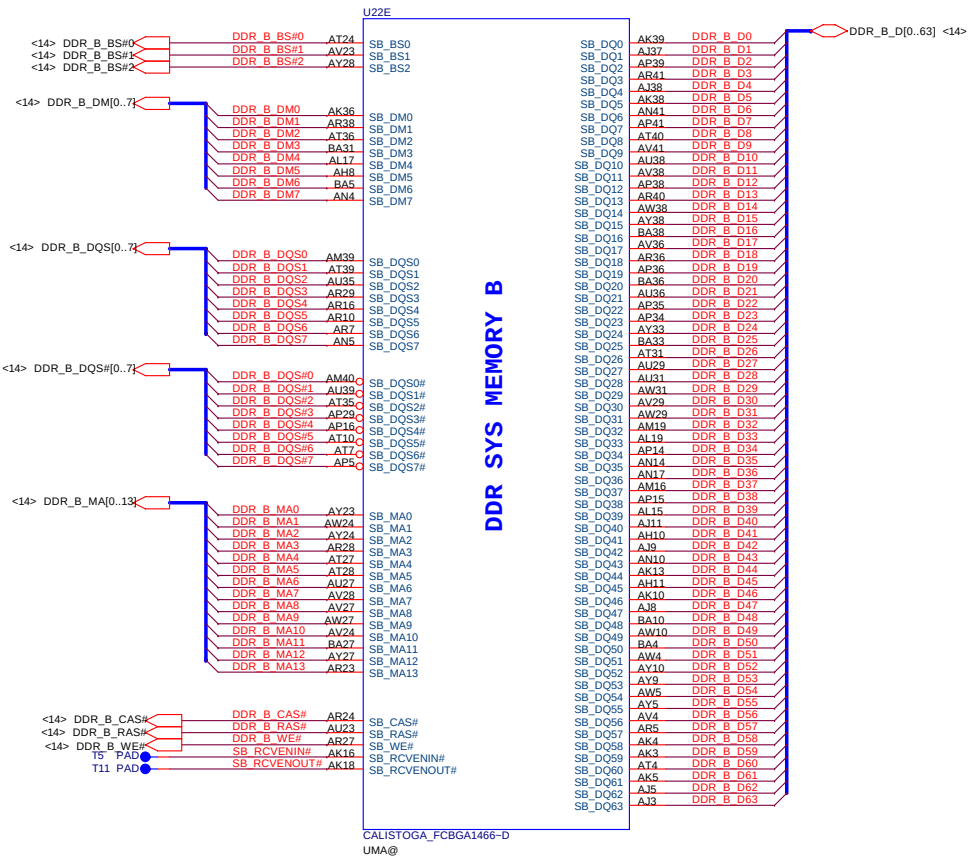
Layout Note:
H_XRCOMP / H_YRCOMP / +H_VREF / +H_SWNG0 /
+H_SWNG1 trace width and spacing is 10/20.

Layout Note:
+DDR_MCH_REF
trace width and
spacing is 20/20.

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	Custom	HEL80/81 LA-3161P	0.2																				
Date	Thursday, February 23, 2006	Sheet	7 of 43																				

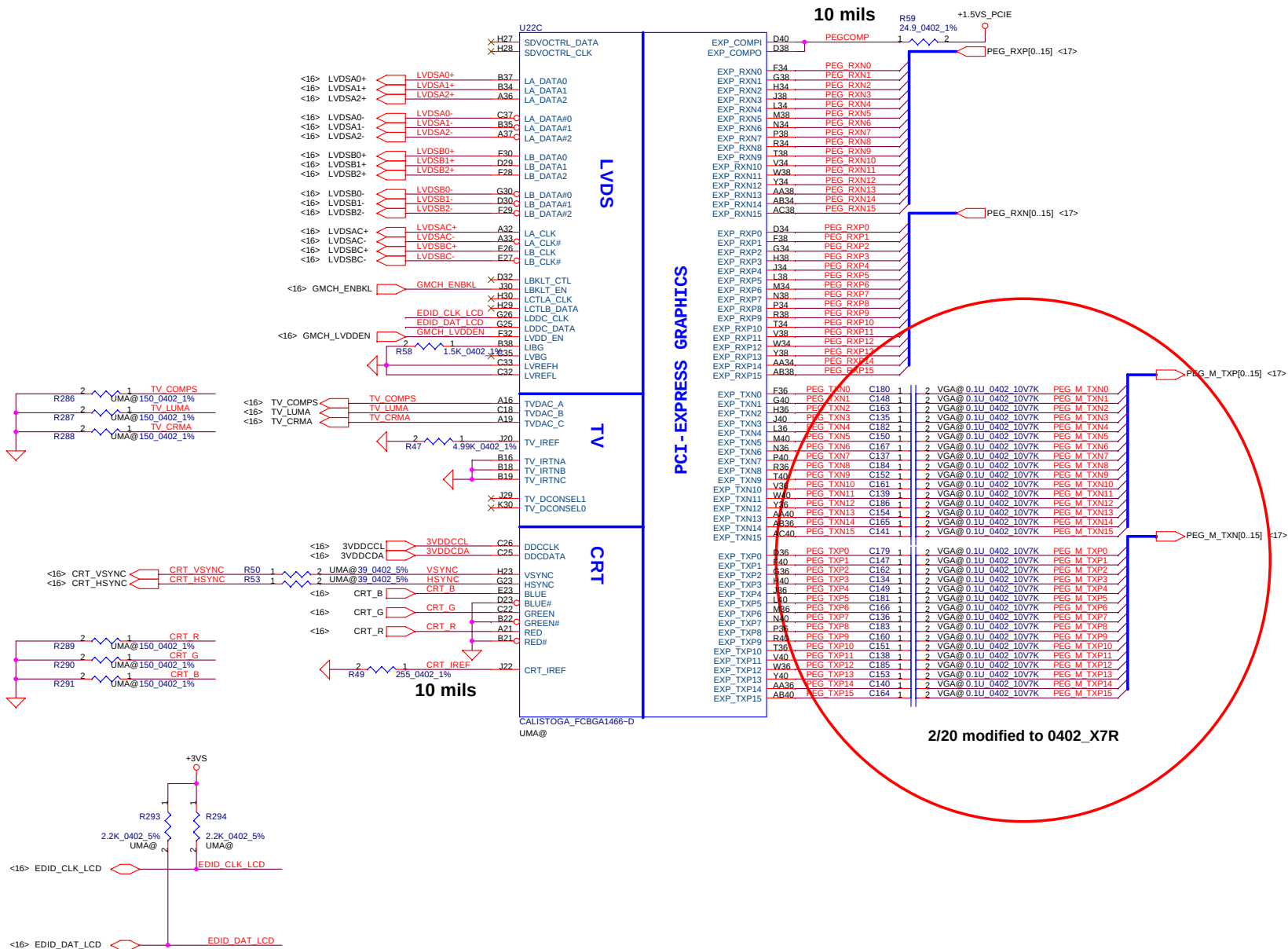


CALISTOGA_FCBGA1466-D
 UMA@

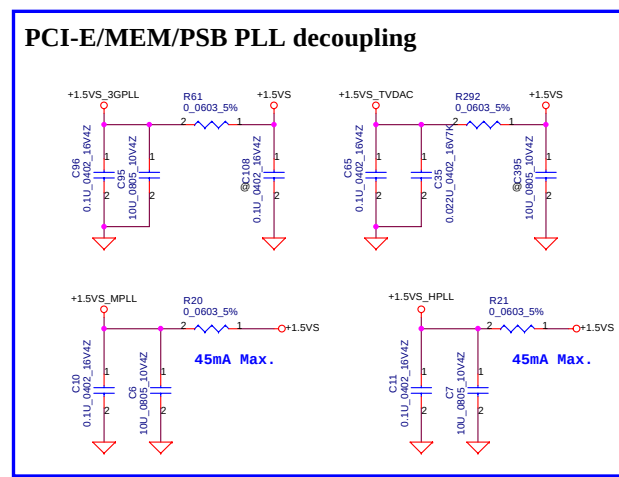
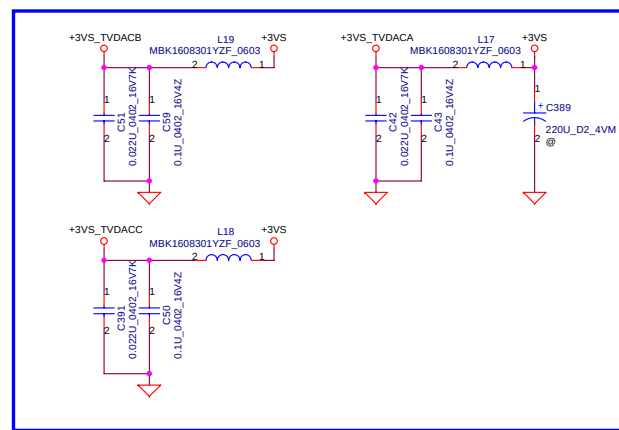
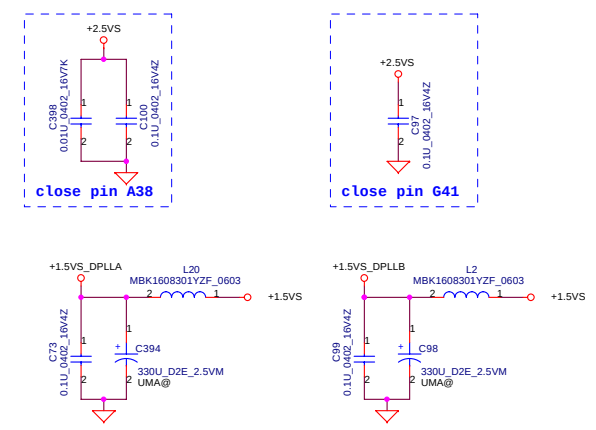
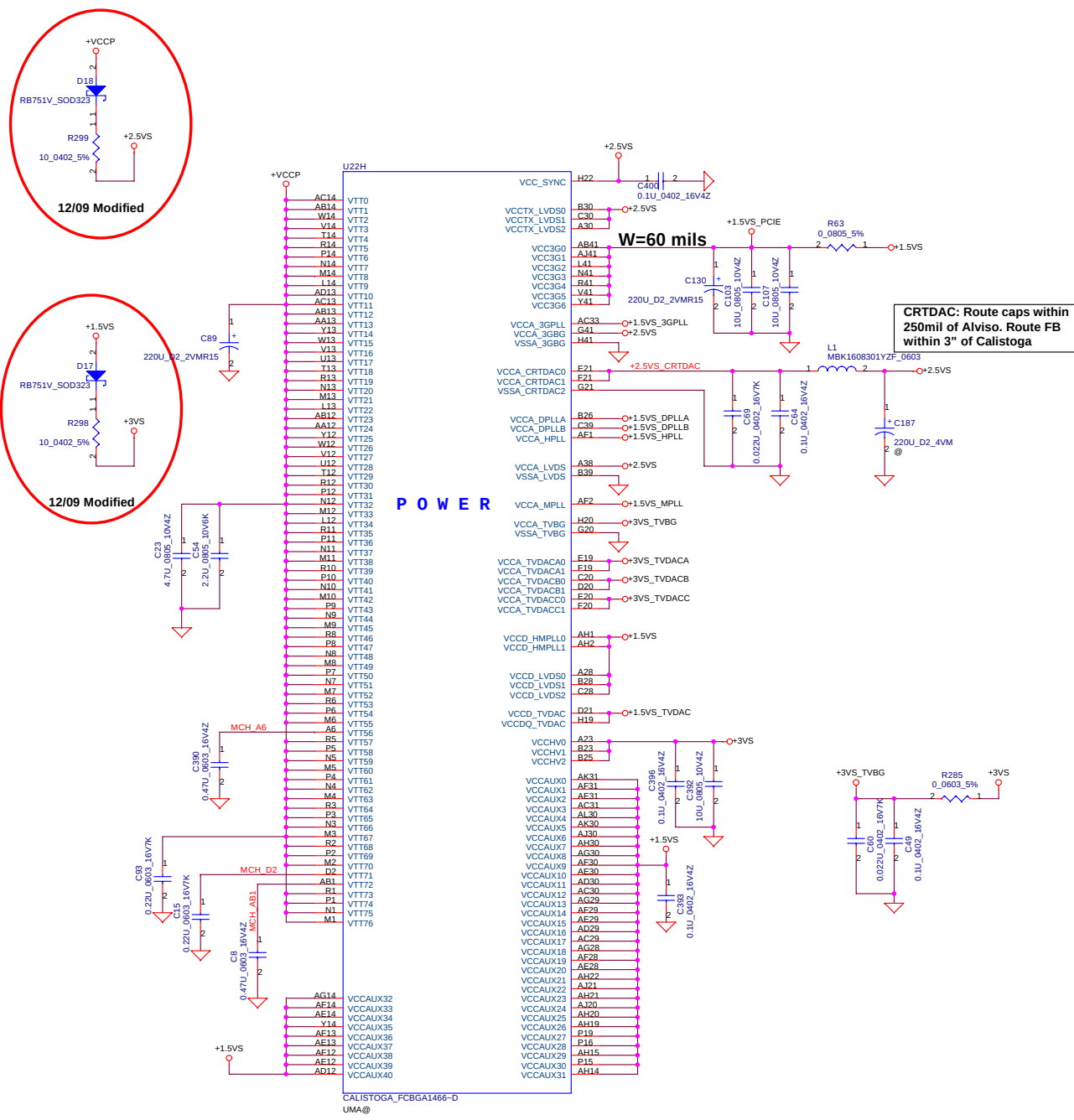


CALISTOGA_FCBGA1466-D
 UMA@

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Custom	HEL80/81 LA-3161P	0.2		Thursday, February 23, 2006	
Sheet		8		of 43	

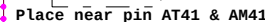


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				Custom	HEL80/81 LA-3161P	0.2
				Date:	Thursday, February 23, 2006	Sheet 9 of 43



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				Customer	HEL80/81 LA-3161P
				Date	Thursday, February 23, 2006
				Sheet	10 of 43
				Rev	0.2

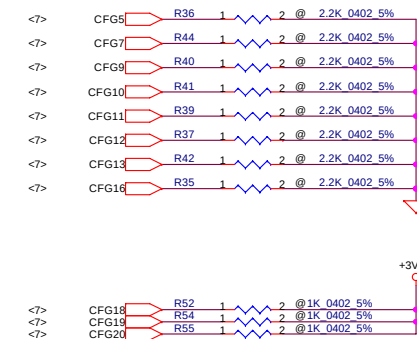
CFG[3:17] have internal pull up
CFG[19:18] have internal pull down



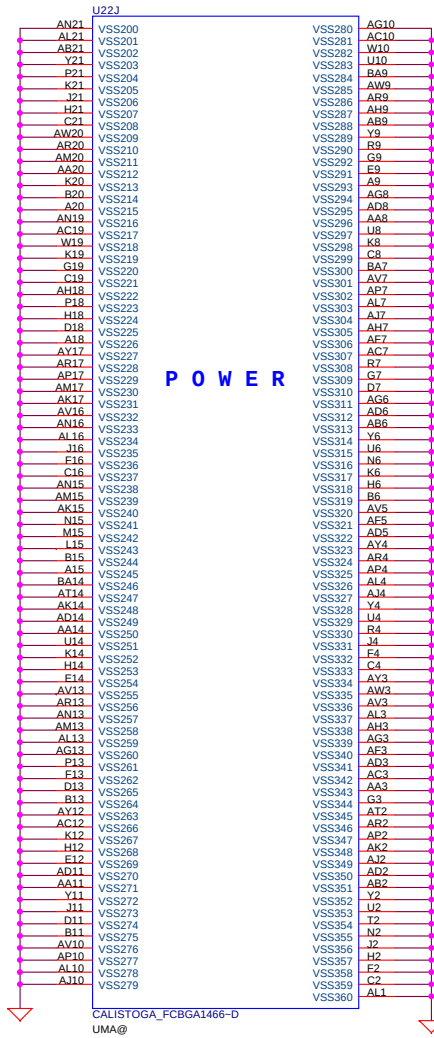
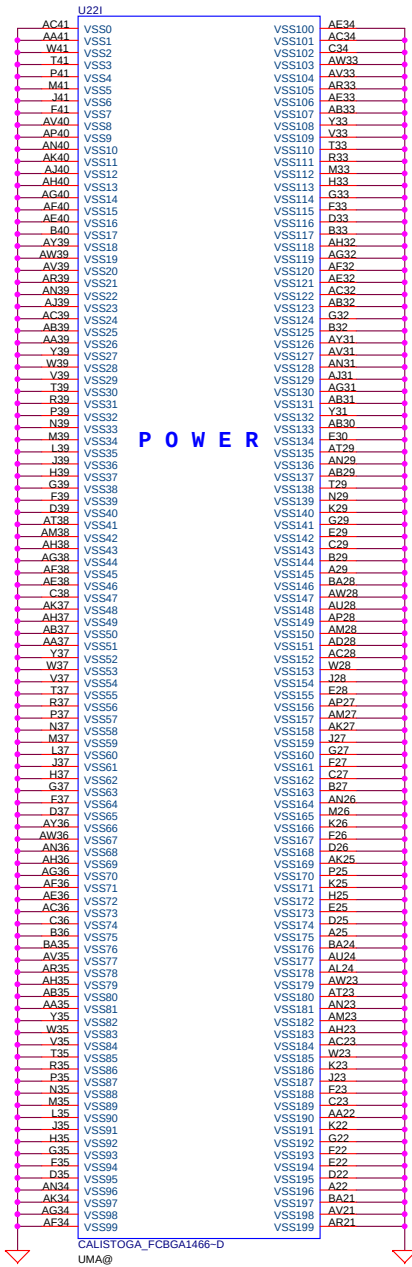
Place near pin BA23

Place near pin BA15

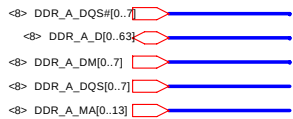
CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default) *
CFG66	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All 2 Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V *(Default) 01 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



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				Custor	HEL801/LA-3161P	0
				Date:	Thursday, February 23, 2006	Sheet 11 of 43

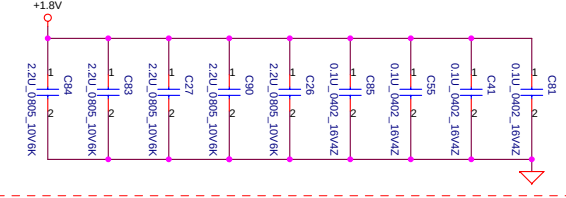


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				Date	Thursday, February 23, 2006
				Sheet	12 of 43
				Rev	0.2

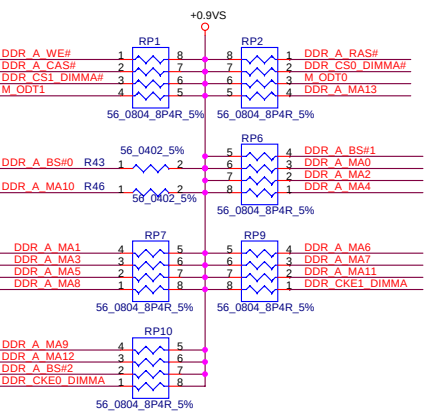
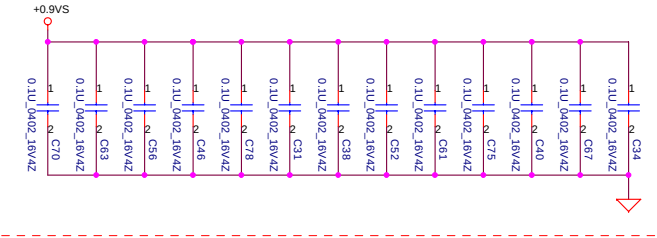


Layout Note:
Place near JP41

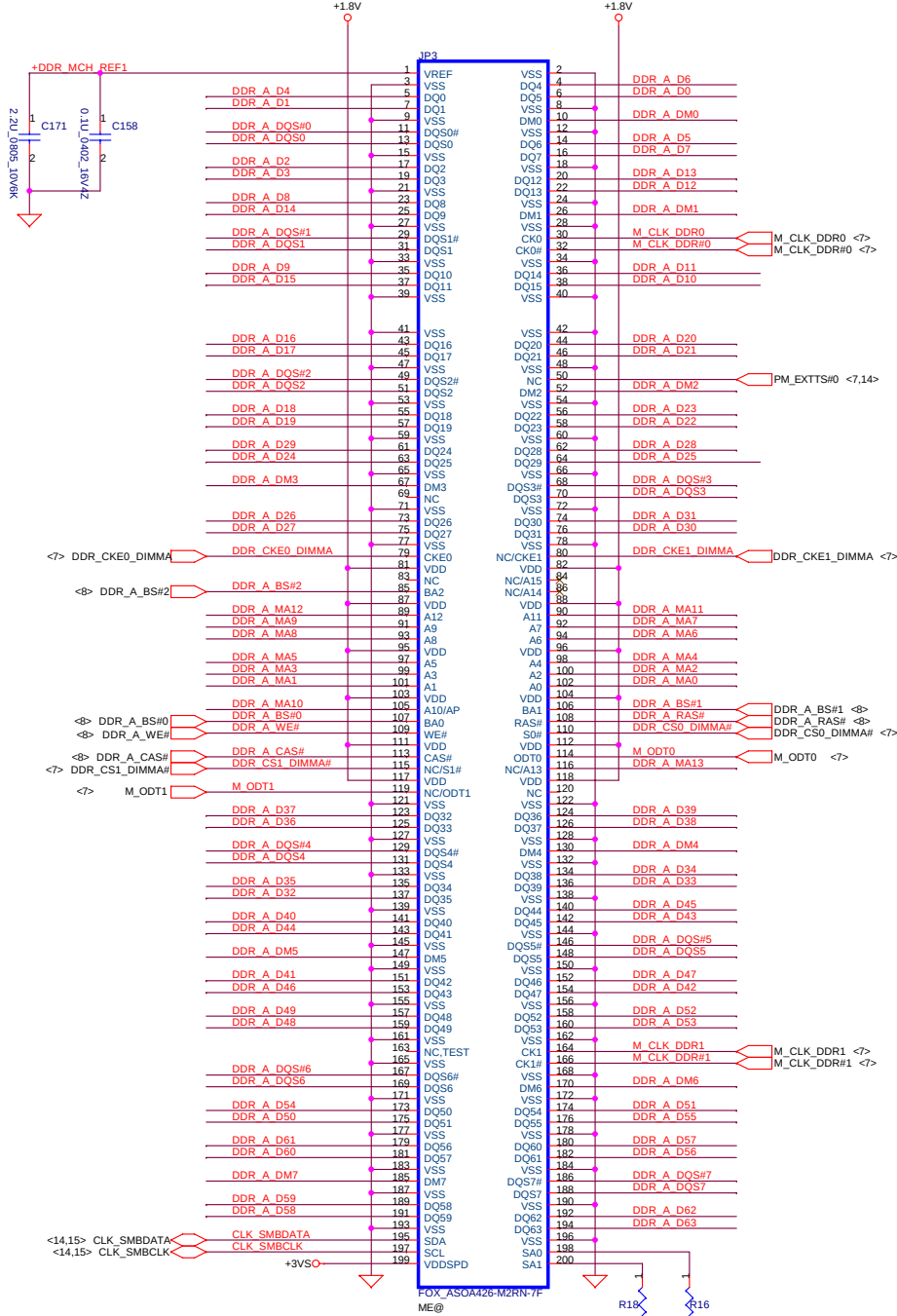
Layout Note:
+DDR_MCH_REF
trace width and
spacing is 20/20.



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS



Layout Note:
Place these resistor
closely JP41,all
trace length Max=1.5"

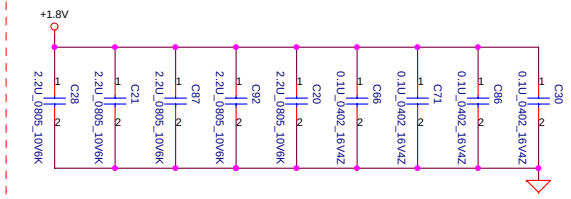
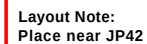


11/9 Modify pn to SP070006V00

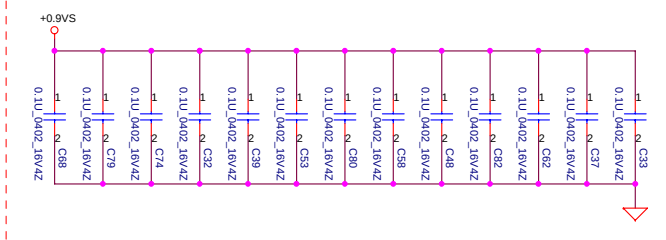
SO-DIMM A

Top side

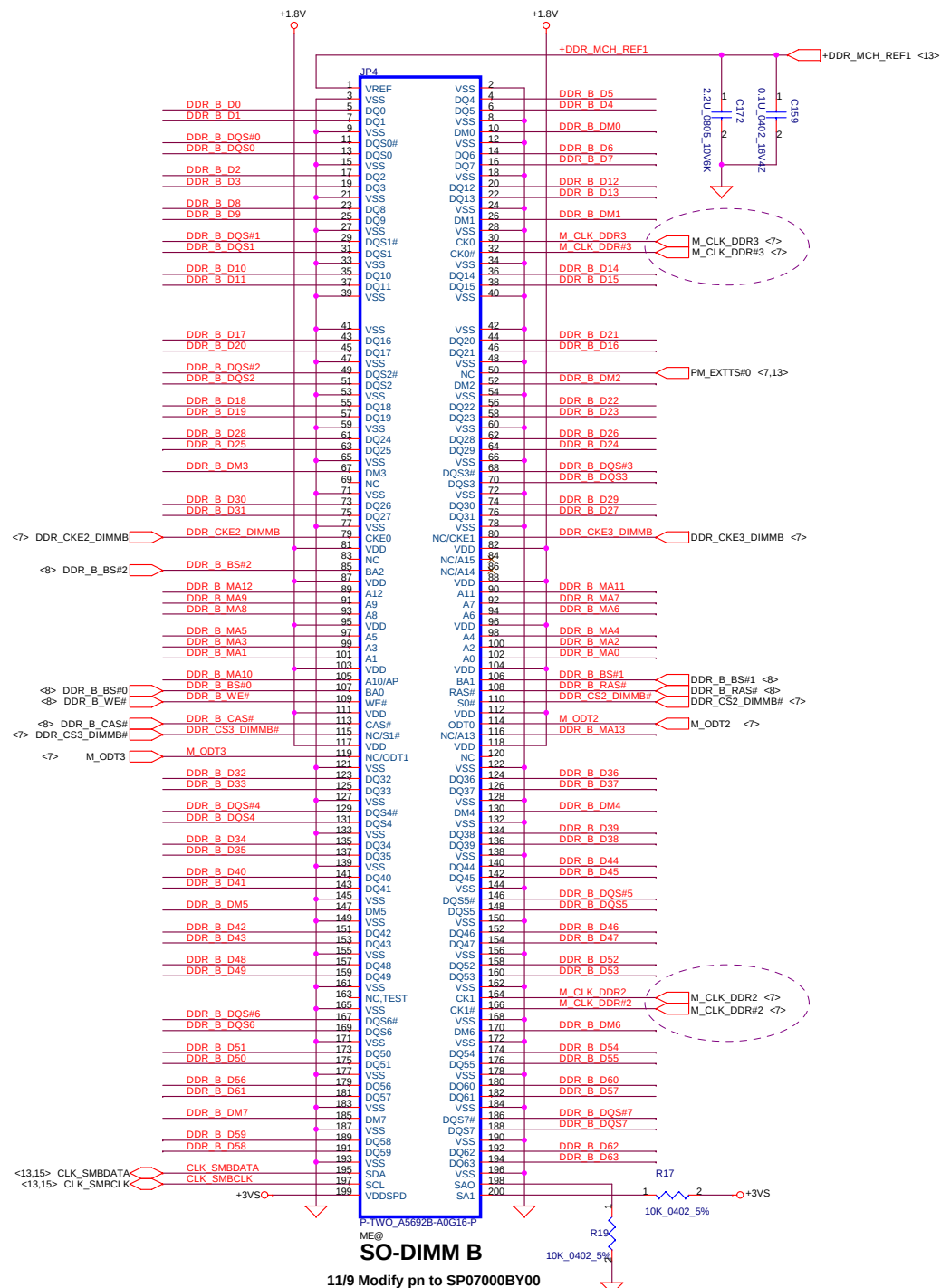
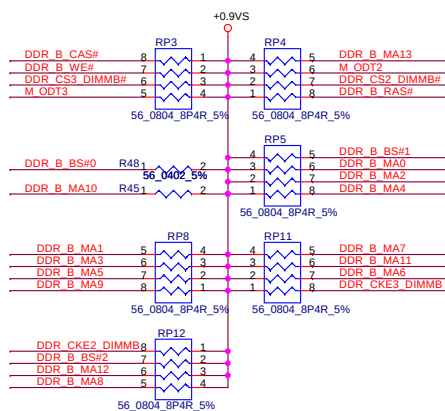
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2005/10/06				2006/10/06				Compal Electronics, Inc.			
								DDRII-SODIMM SLOT1			
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				Custom				HEL80 LA-3161P			
				Date				Thursday, February 23, 2006			
								Sheet 13 of 43			



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

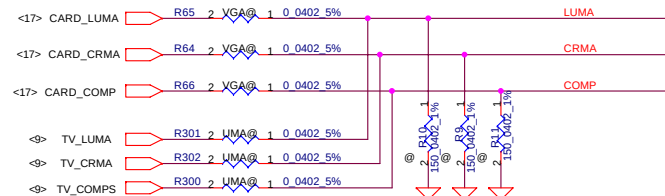


Layout Note:
Place these resistor
closely JP42,all
trace length Max=1.5"



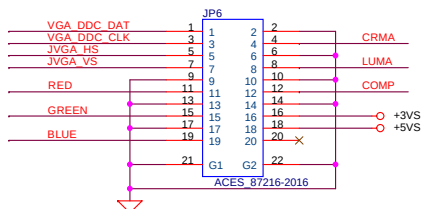
11/9 Modify pn to SP07000BY00

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					HEL80 LA-3161P	0.2
Date:	Thursday, February 23, 2006	Sheet	14	of	43	

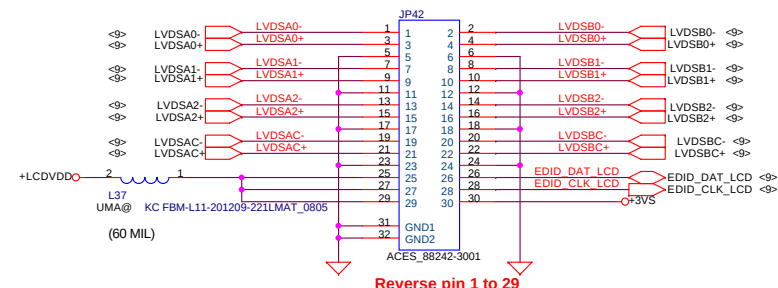
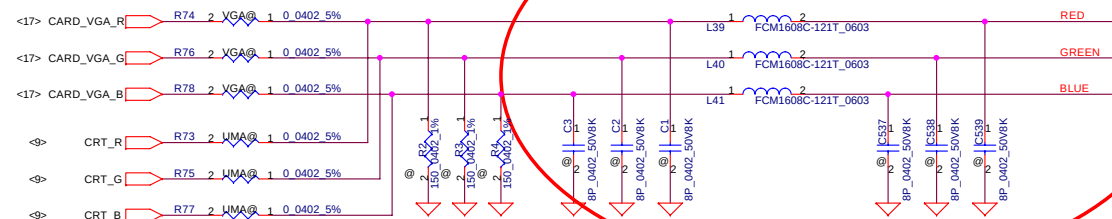
TV-OUT Conn.

Pop when with internal graphics

VGA I/O PORT Conn.

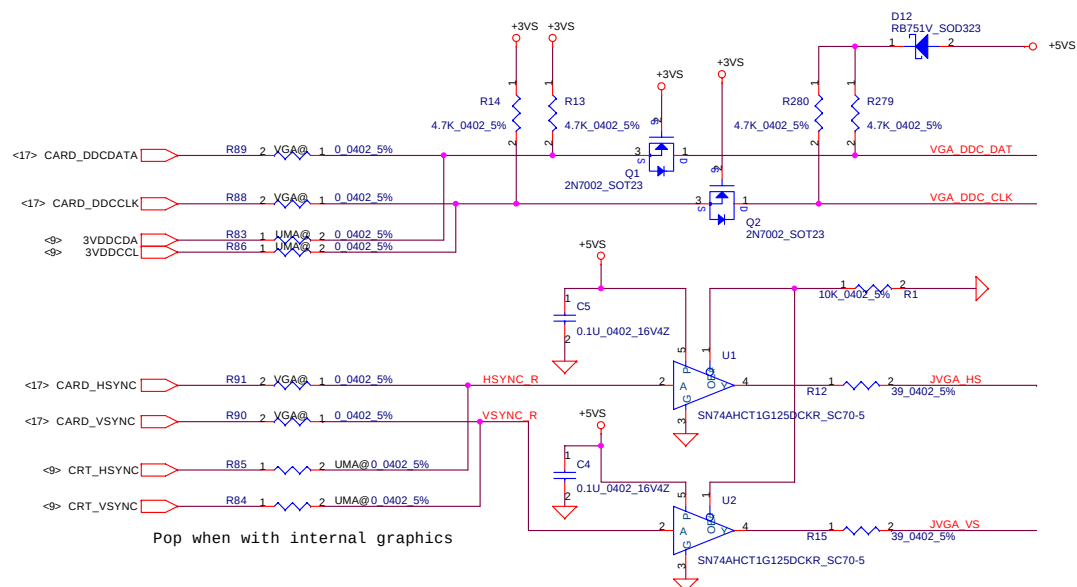
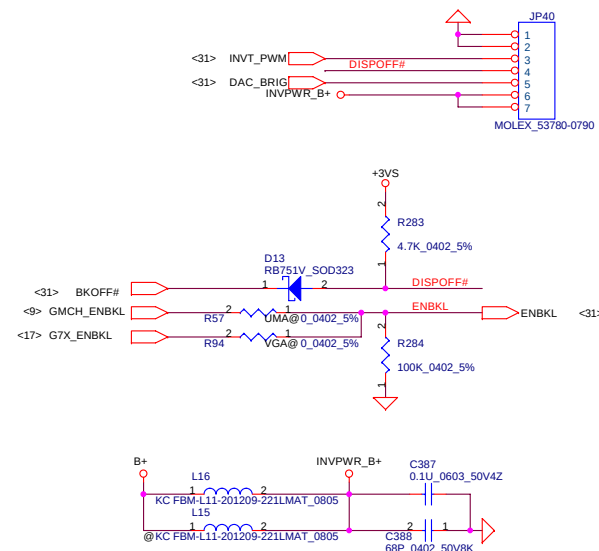


UMA LCD / PANEL Conn.

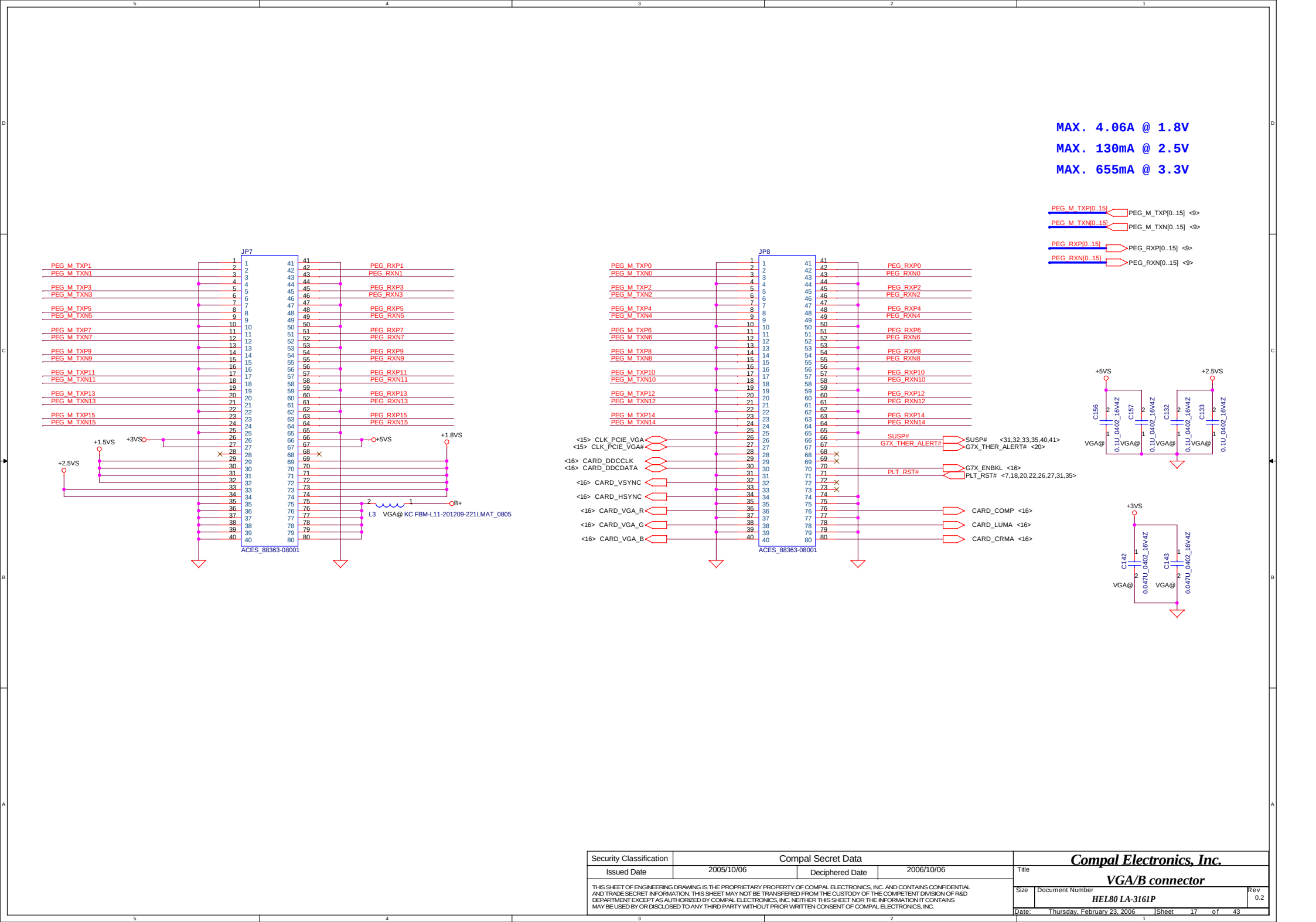
**CRT Conn.**

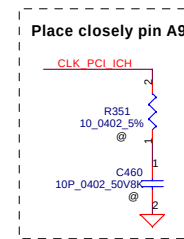
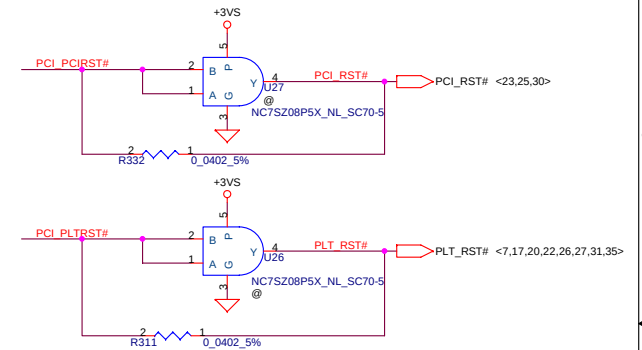
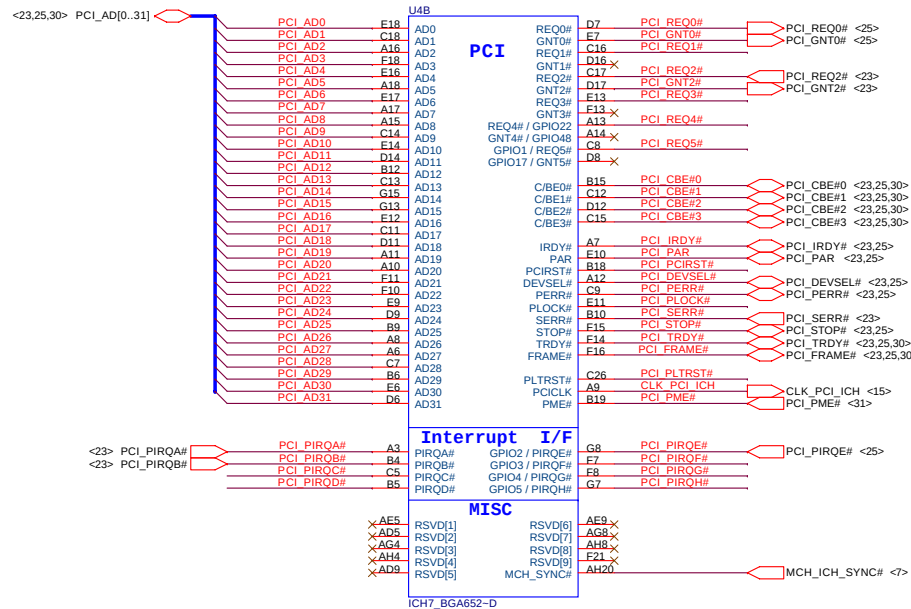
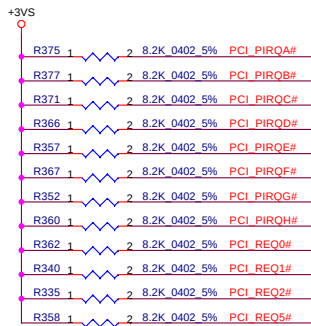
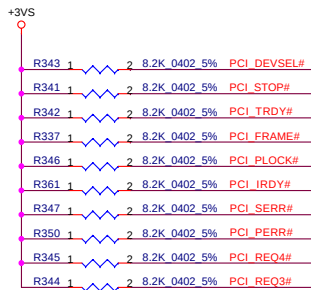
Pop when with internal graphics

2/09 Add for Compliance Engineering request

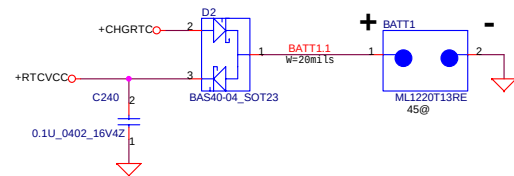
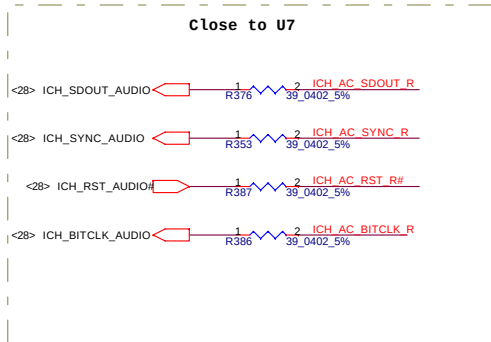
**INVERTER Conn.**

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				Custom	HEL80 LA-3161P	0.
				Date:	Thursday, February 23, 2006	Sheet 16 of 43

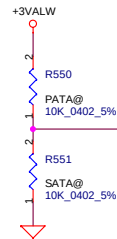
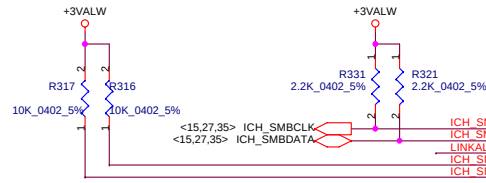
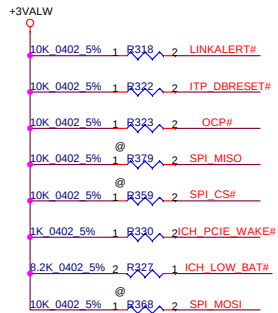
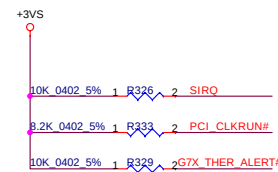




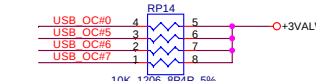
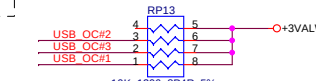
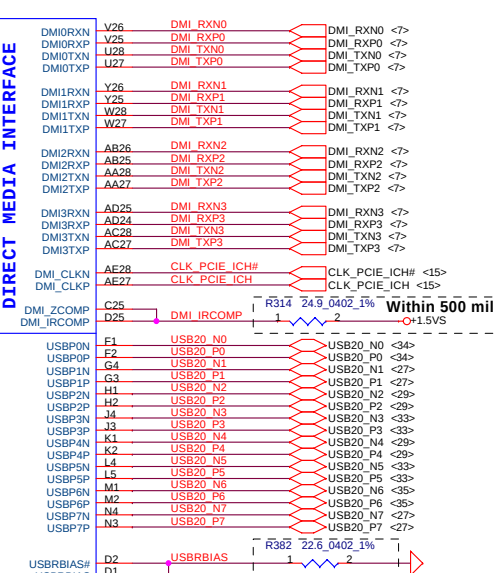
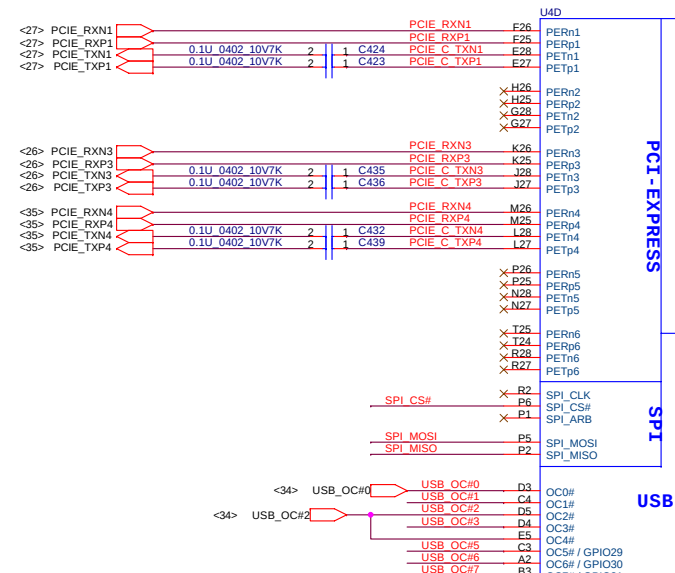
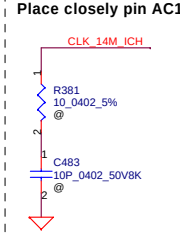
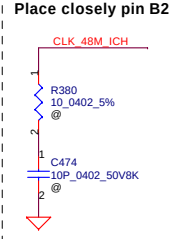
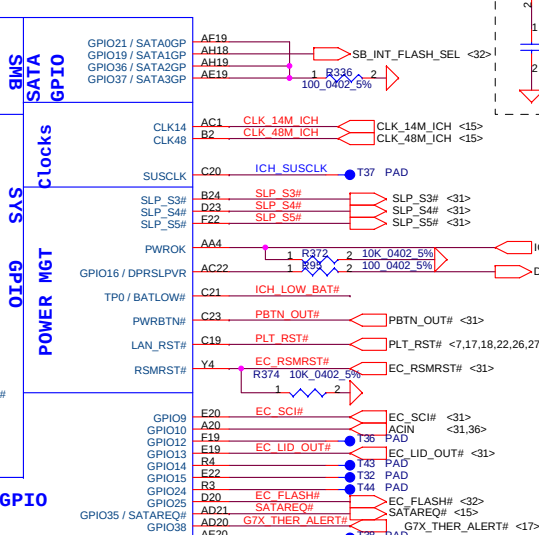
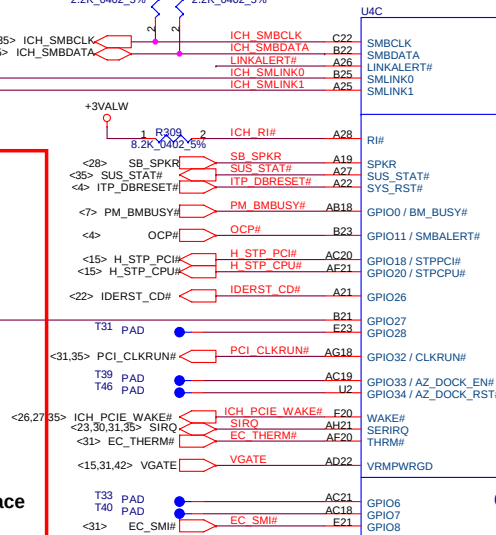
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Date: Thursday, February 23, 2006				Sheet 18	of 43



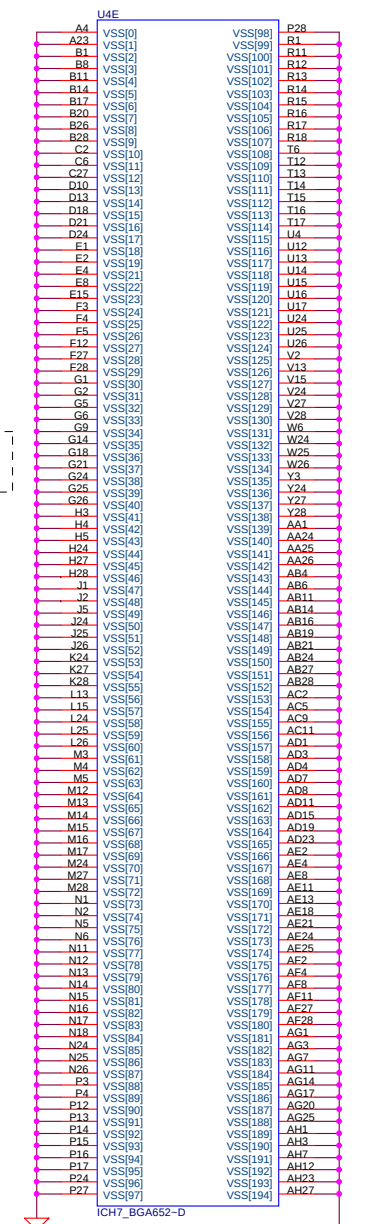
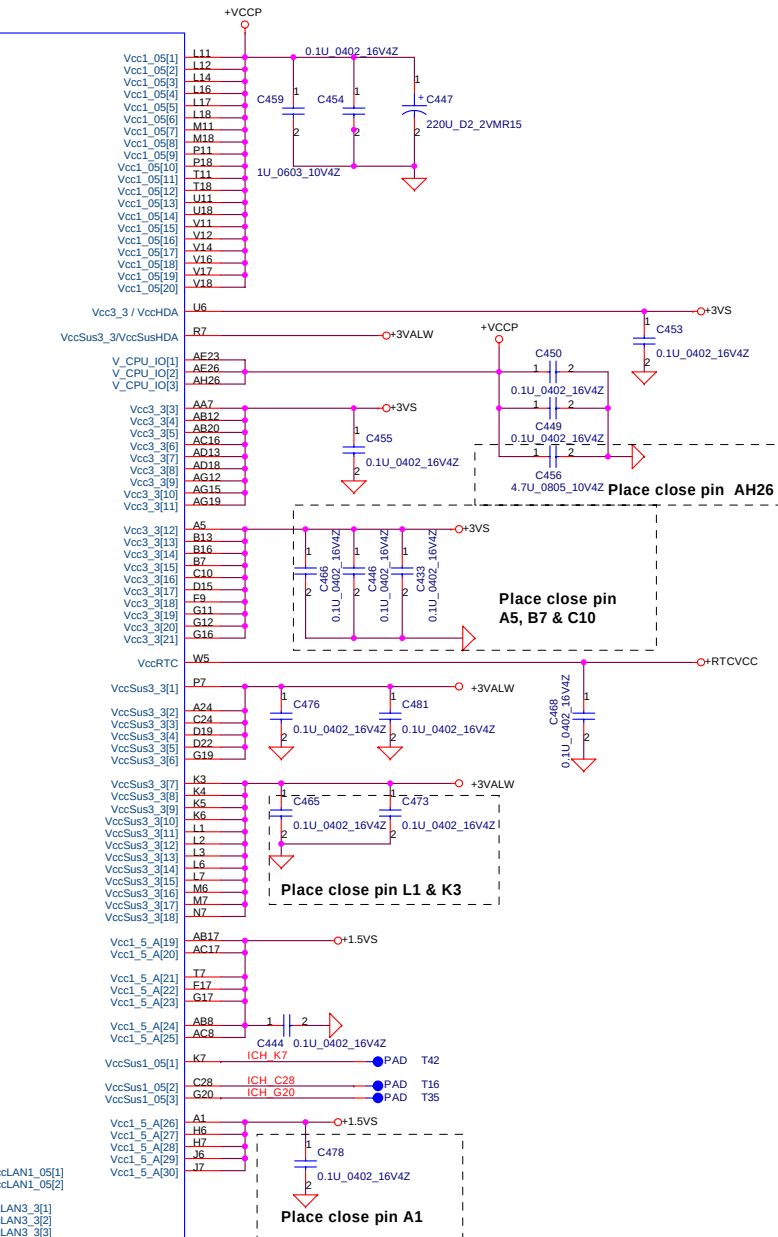
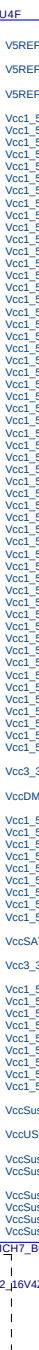
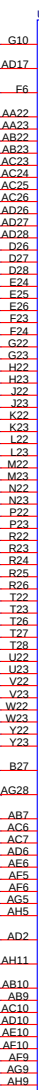
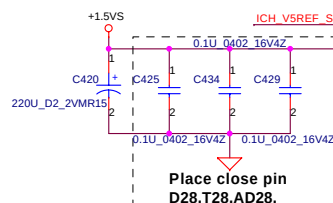
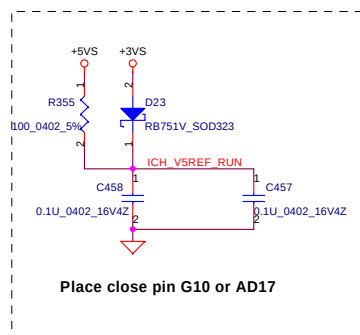
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				Custom	HEL80 LA-3161P	0.2
				Date:	Thursday, February 23, 2006	Sheet 19 of 43



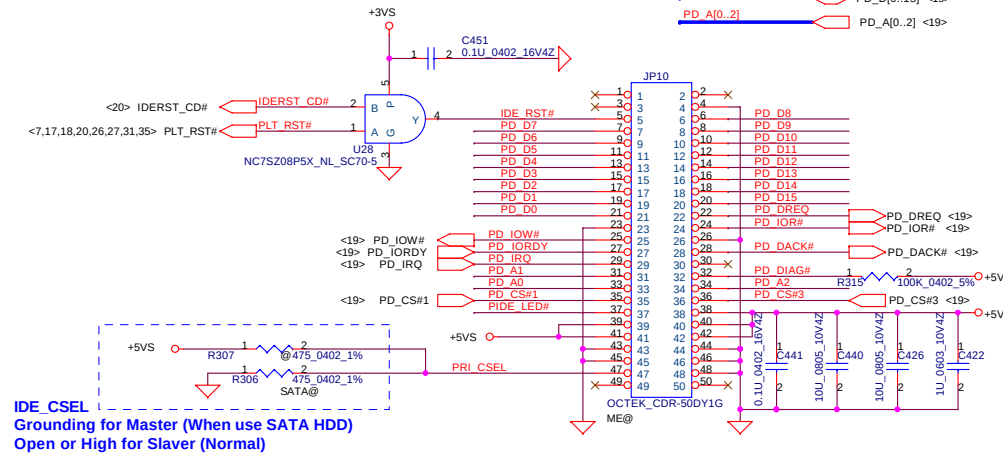
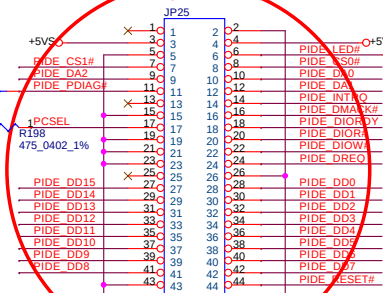
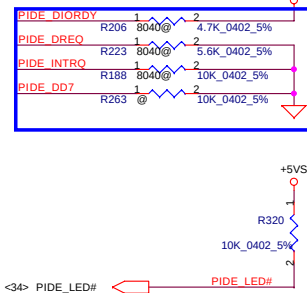
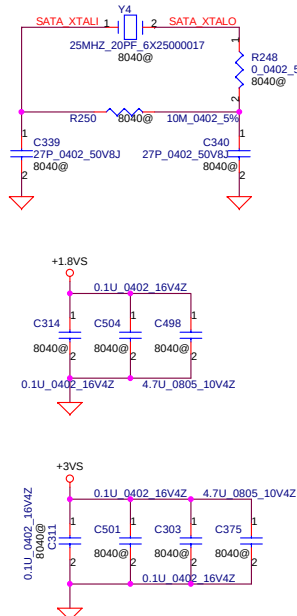
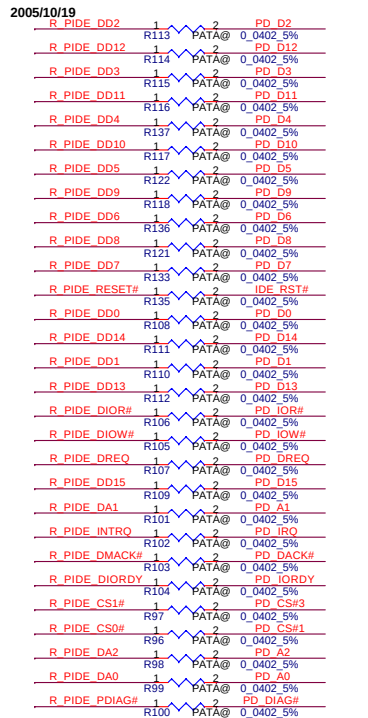
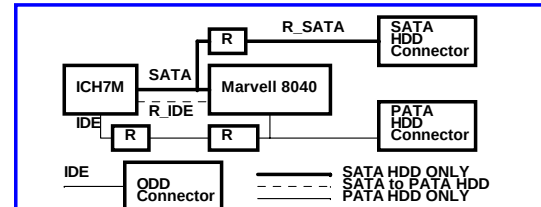
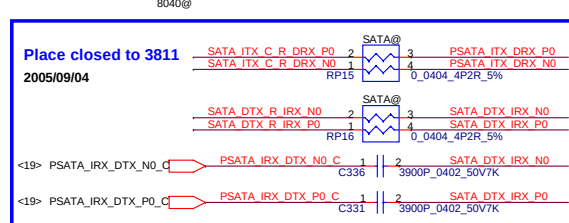
2/13 Add feature:
Pull high for pure IDE interface
Pull low for SATA interface



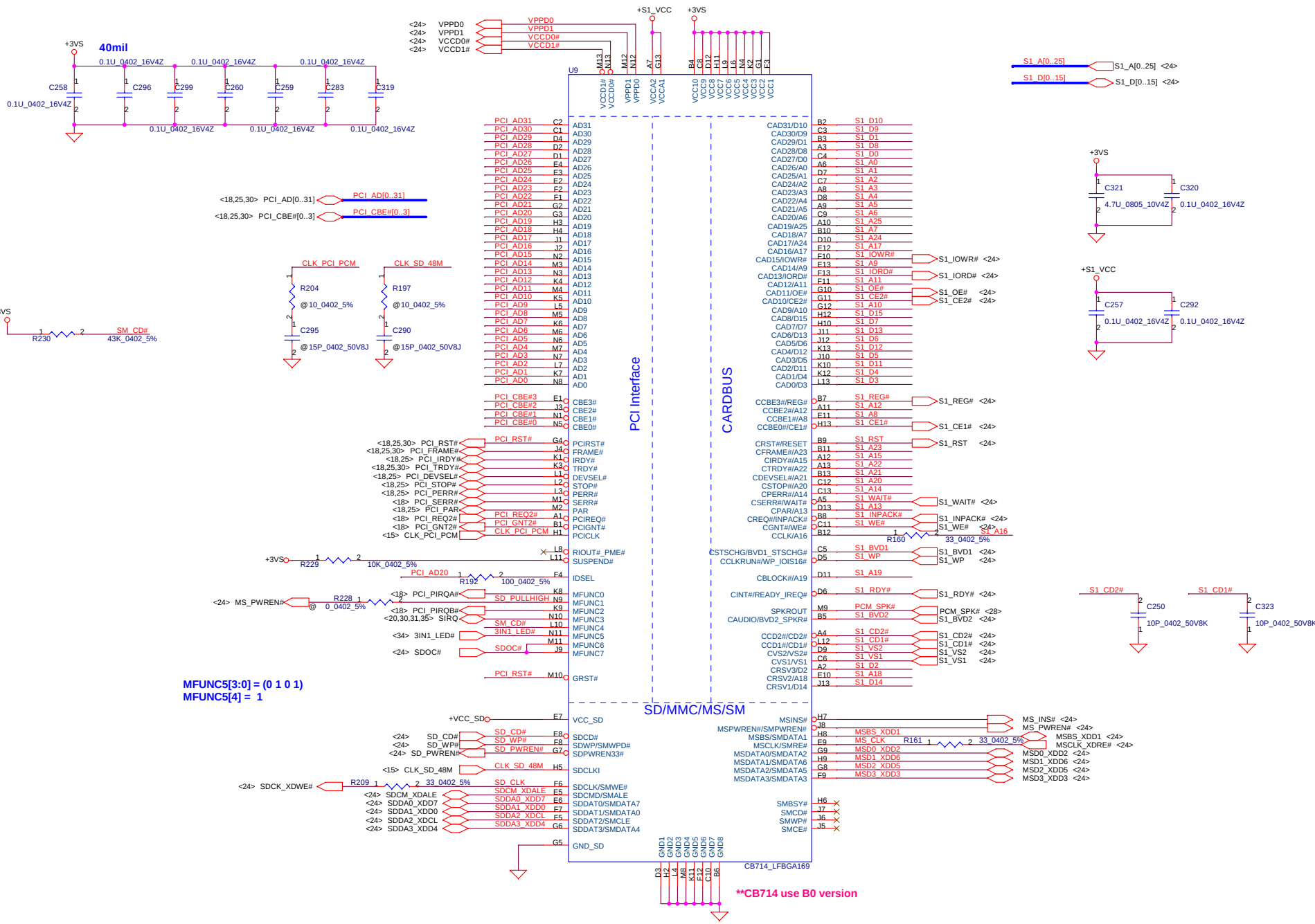
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Date	Thursday, February 23, 2006	Sheet	20	of	43



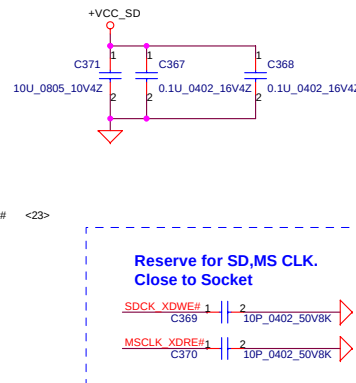
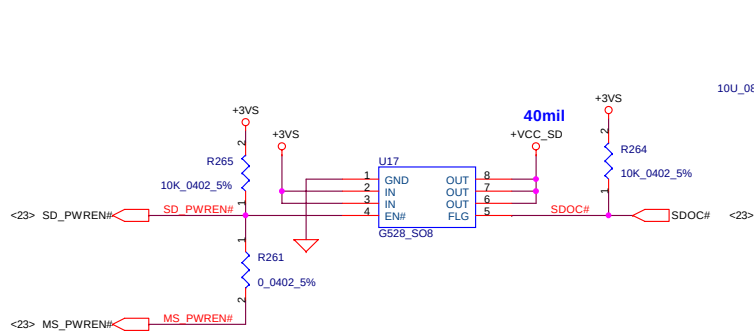
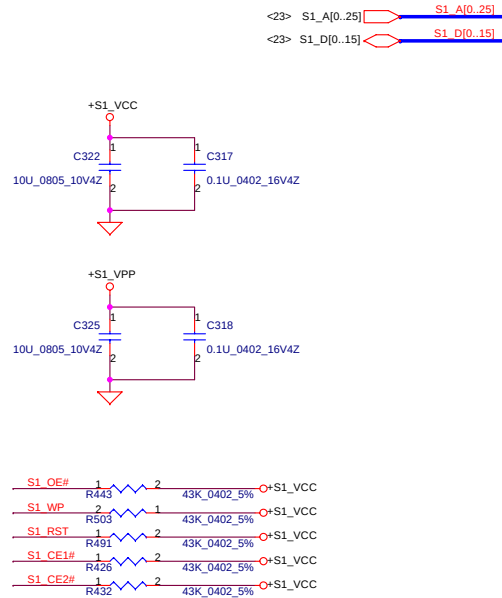
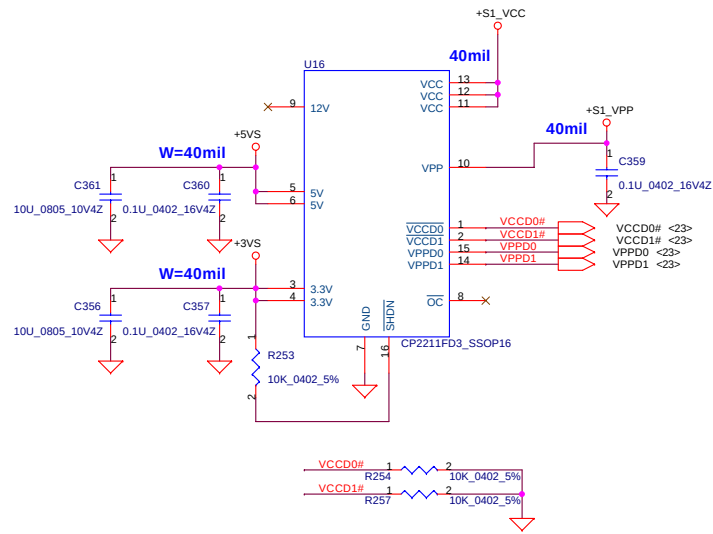
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Issued Date	2005/10/06	Deciphered Date	2006/10/06			
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				Custor	HEL80 LA-3161P	0.2
				Date:	Thursday, February 23, 2006	Sheet 21 of 43



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						Size	Document Number			Rev	0.
						Custom	HEL80- LA-3161P				
						Date:	Thursday, February 23, 2006		Sheet	22	of 43



PCMCIA Power Control

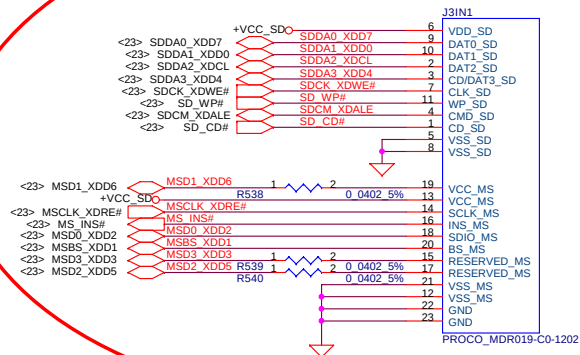
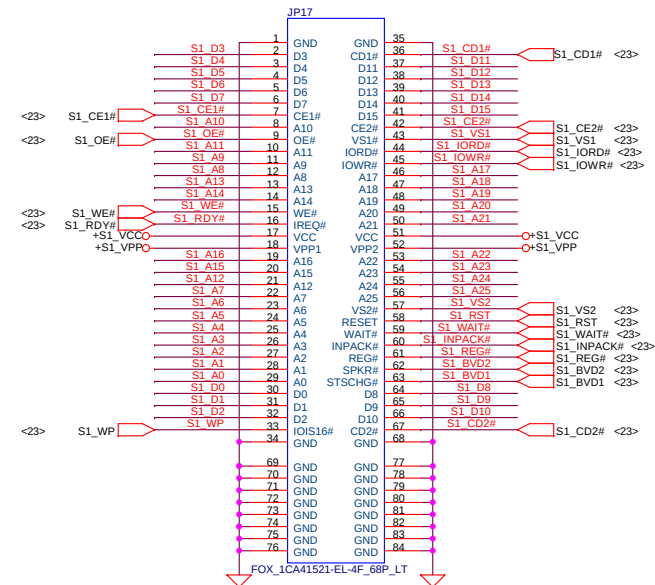


PCMCIA Socket

Note : 11/10 modify library to meet spec

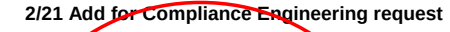
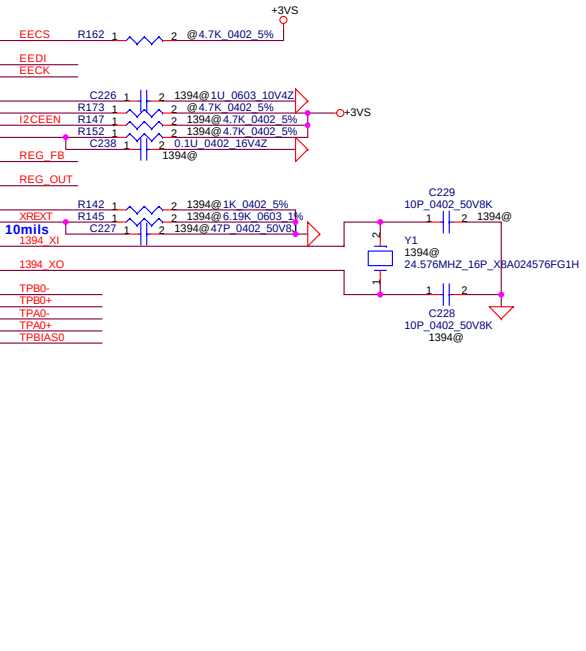
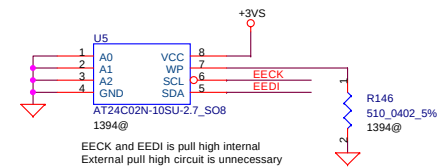
pn: SP01000IC00

02/17 modify footprint to FOX_1CA41521-EL-4F_68P_LT



12/20 modified

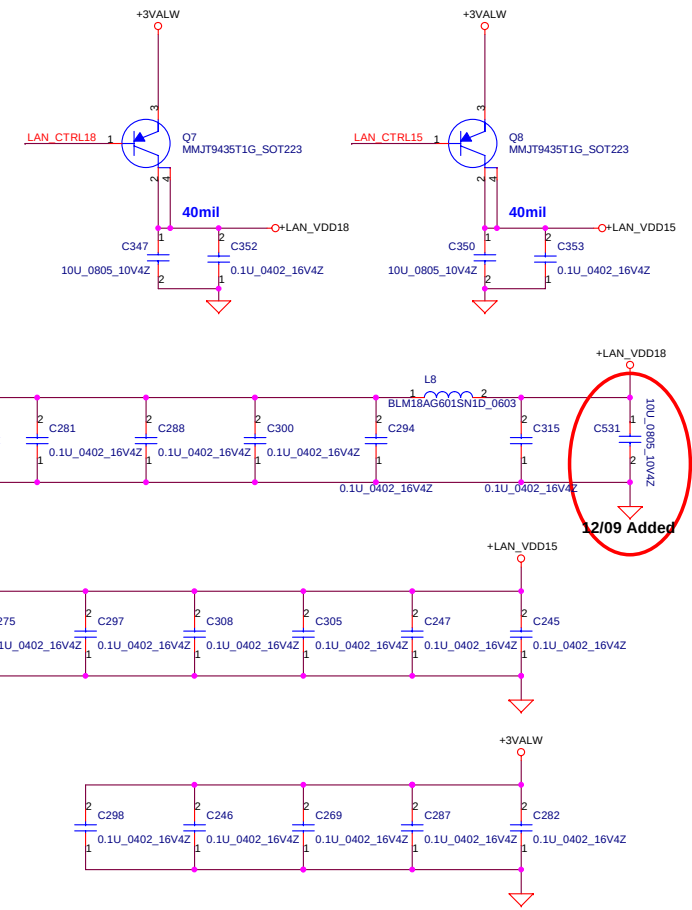
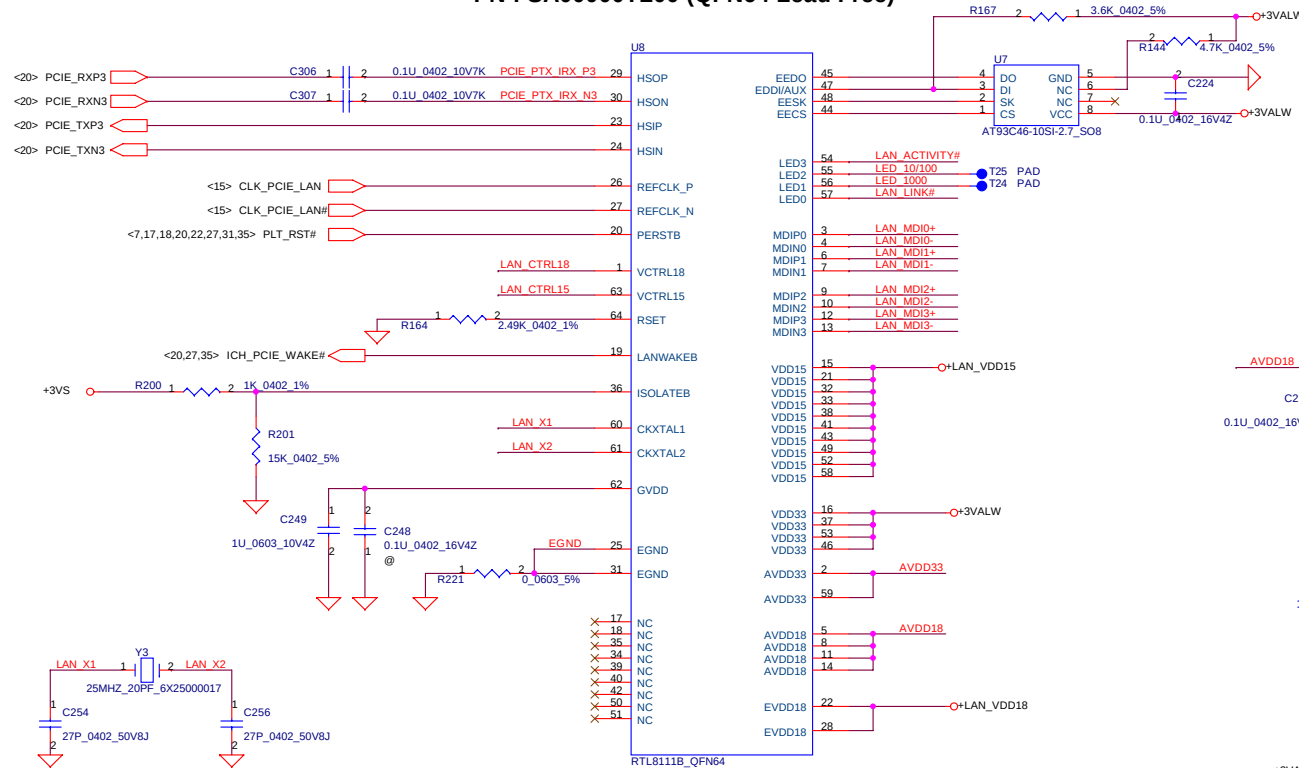
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Issued Date	2005/06/20	Deciphered Date	2006/06/20	PCMCIA Socket	
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				Date	Thursday, February 23, 2006
				Sheet	24 of 43
				Rev	0.2



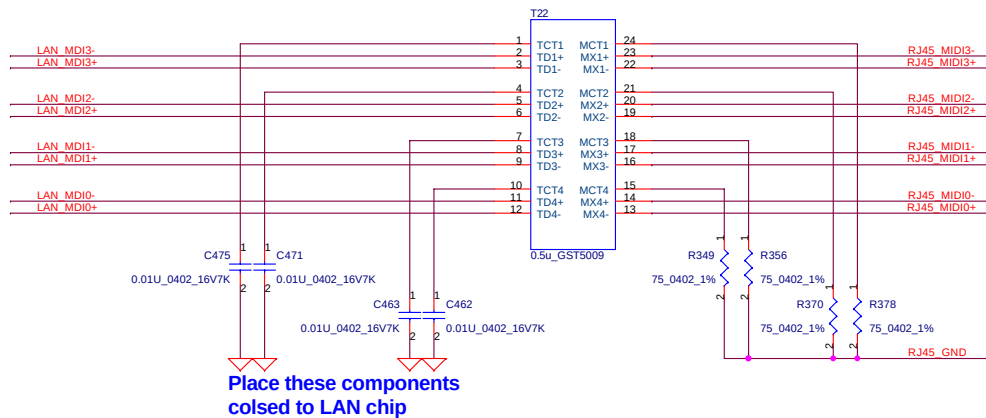
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				Custom	HEL80 LA-3161P	0.2	
				Date:	Thursday, February 23, 2006	25	
3		2		1	Sheet	of 43	

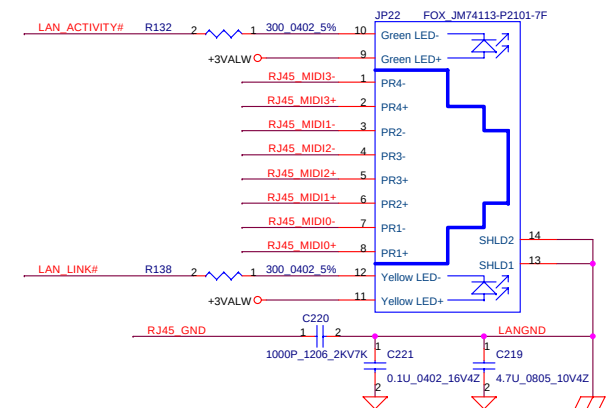
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GbE Transformer: GST5009 (SP050005610) MY



LAN Conn.

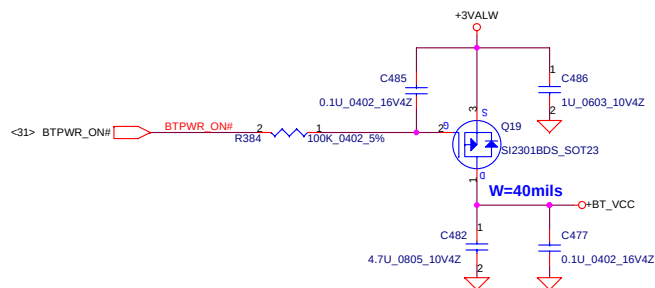
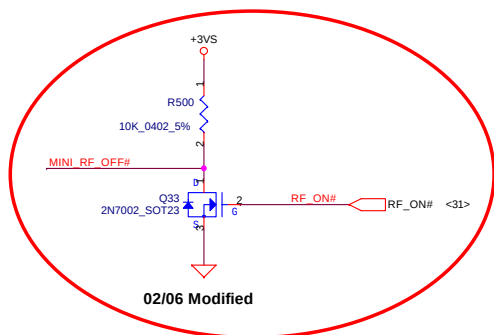
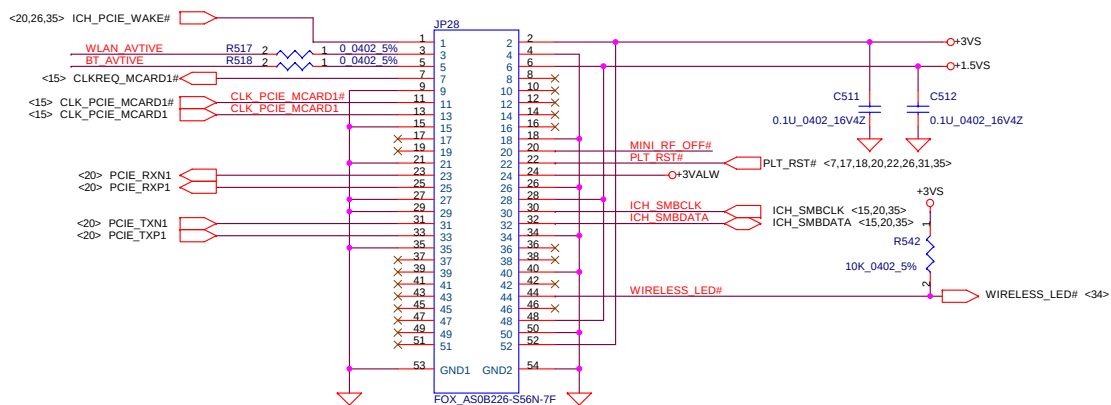


Compal Electronics, Inc.

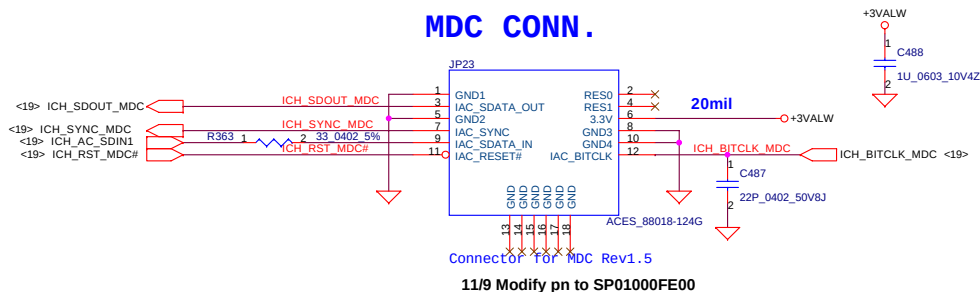
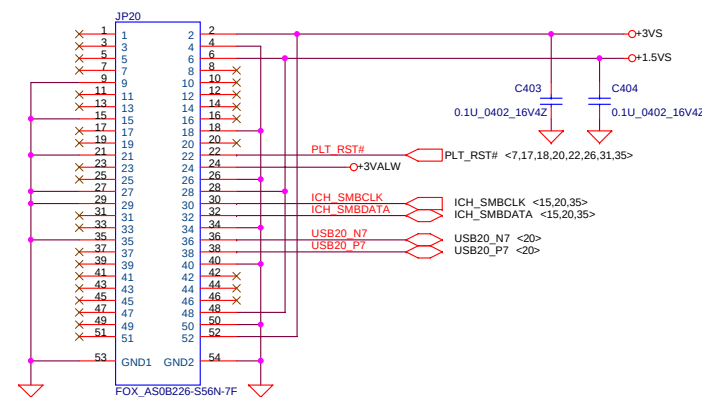
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	Size	Document Number		Rev
		HEL80 LA-3161P		0.2
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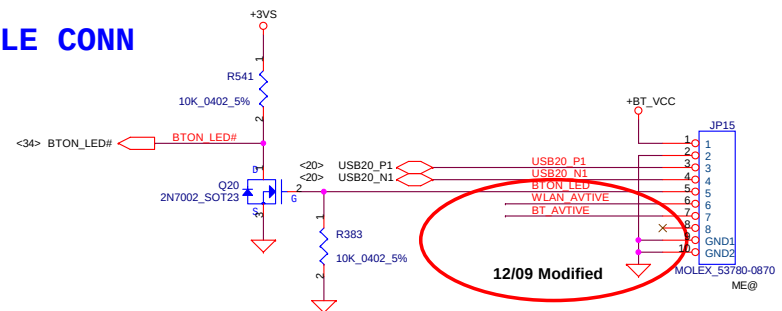
Mini-Express Card(Slot 1-WLAN)



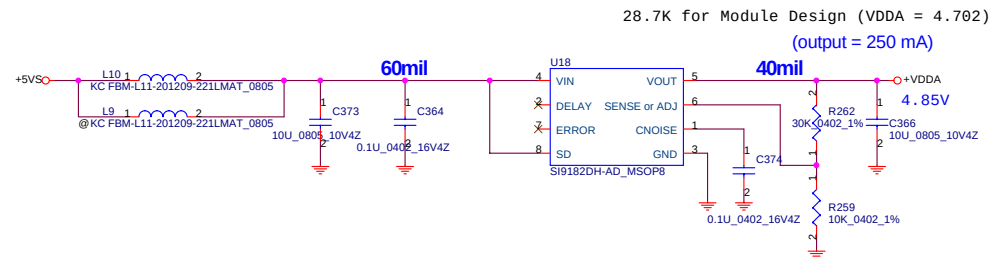
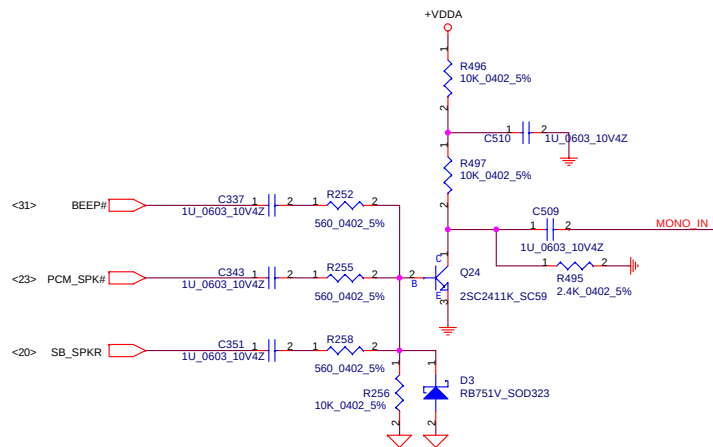
Mini-Express Card(Slot 2-TV)



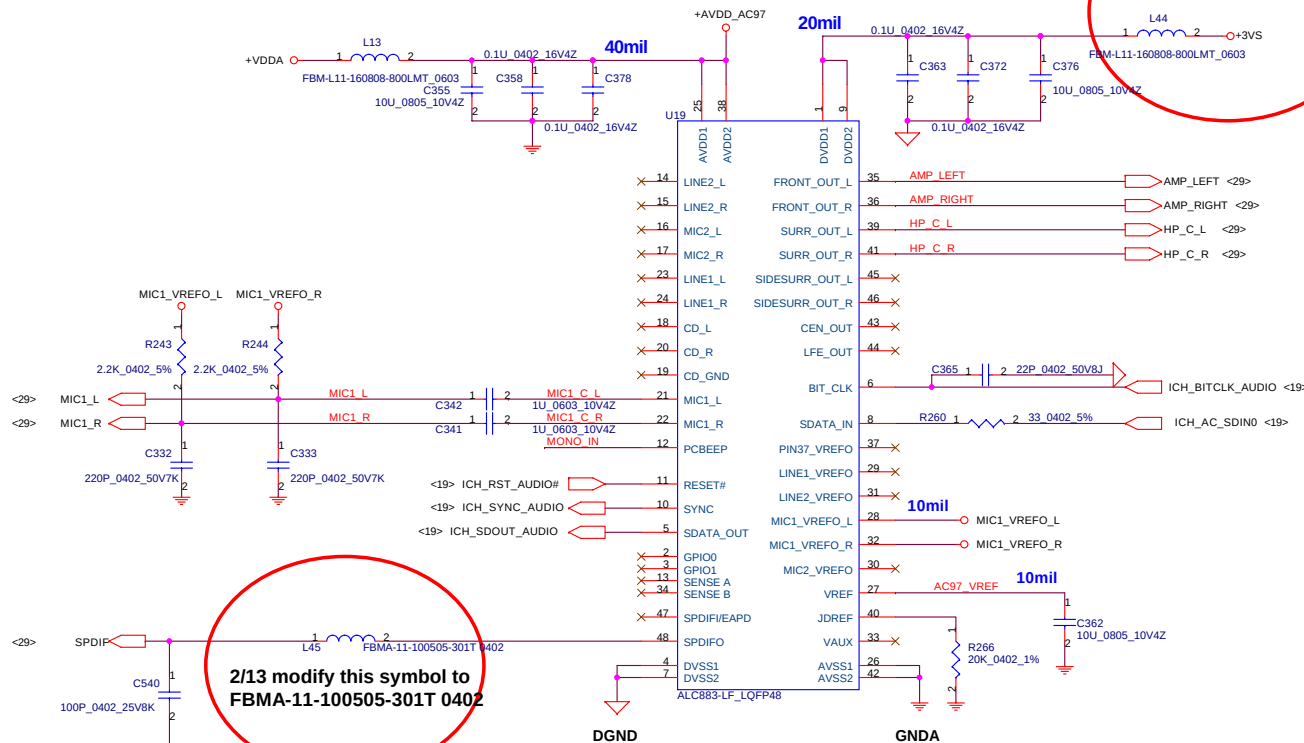
BT MODULE CONN



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Issued Date		2005/10/06	Deciphered Date	2006/10/06	Title	Mini Card / MDC CONN		
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					Custom	HEL80/81 LA-3161P	0.2	
					Date:	Thursday, February 23, 2006	Sheet	27 of 43



HD Audio Codec

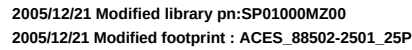


Security Classification		Compal Secret Data		Title	
Issued Date	2005/10/06	Deciphered Date	2006/10/06	HD CODEC ALC883	
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				Custom	HEL80 LA-3161P
				Date	Thursday, February 23, 2006
				Sheet	28 of 43

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Issued Date	2005/10/06	Deciphered Date	2006/10/06	Title	
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				Custom	HEL80 LA-3161P Rev 0.2
				Date:	Thursday, February 23, 2006
				Sheet	29 of 43

KSI[0..7] KSI[0..7] <31>

KSO[0..15] KSO[0..15] <31>



TOP Side

3V3VW

R267 100K_0402_5%

J2 @ JOPEN

J5 @ JOPEN

Bottom Side

<34> ON/OFFBTN#

ON/OFFBTN#

D6 DAN202U_SC70

ON/OFF#

51ON#

ON/OFF# <31>

51ON# <34,36>

<31> EC_ON

EC_ON

R268 10K_0402_5%

Q11 2N7002_SOT23

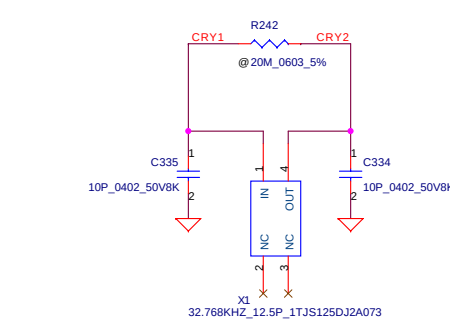
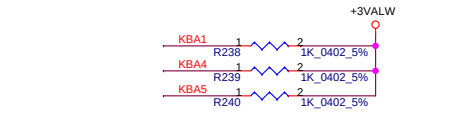
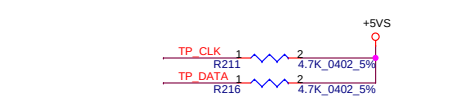
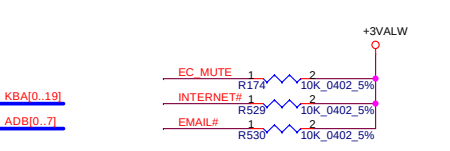
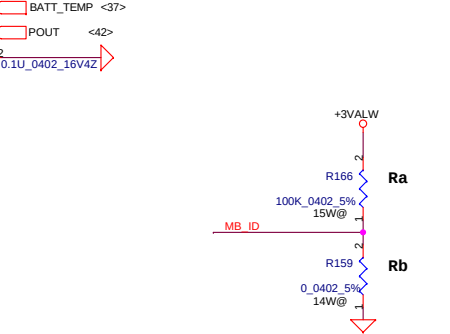
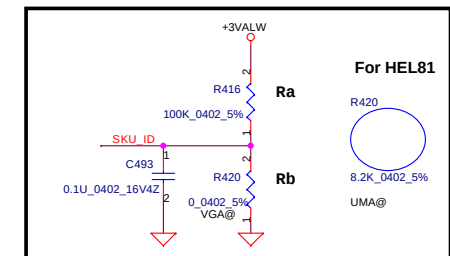
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Issued Date	2005/10/06	Deciphered Date	2006/10/06	Title	
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				Document Number	0.2
				CUSTO HEL80 LA-3161P	
Date: Thursday, February 23, 2006		Sheet 30 of 43			

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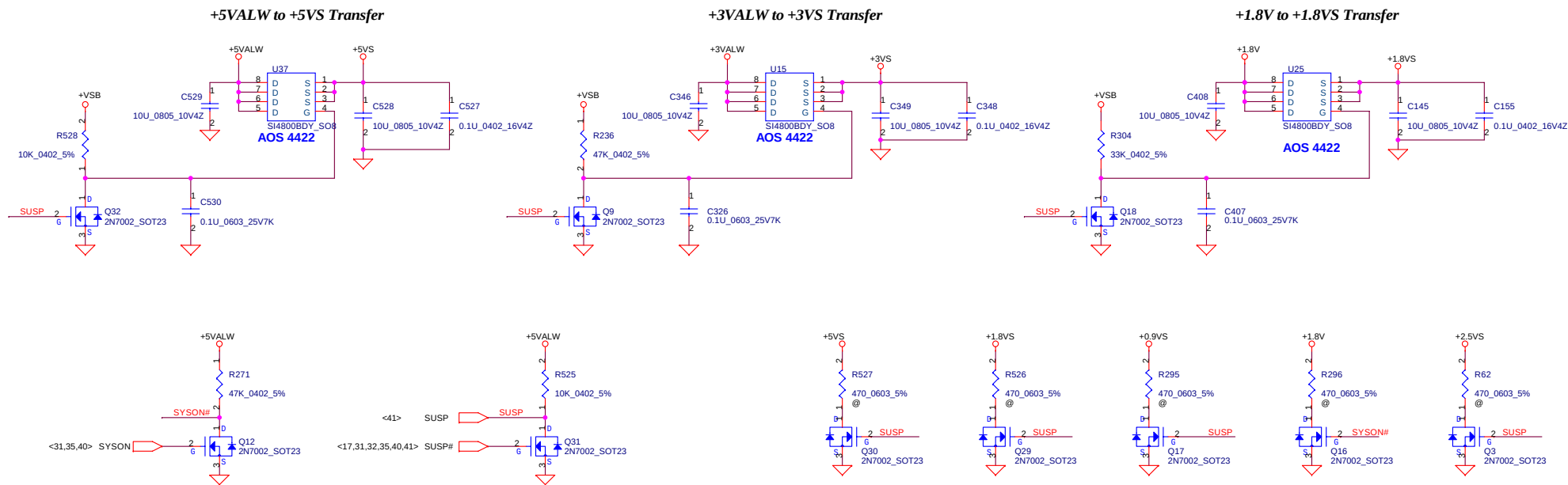
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30	INTERNET#	User-2
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2/20 New added

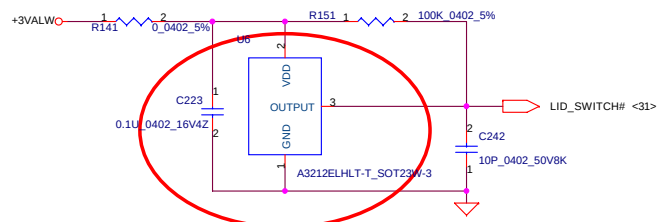
Security Classification	Compal Secret Data
Issued Date	2005/10/06
Deciphered Date	2006/10/06
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Compal Electronics, Inc.	
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Size	Document Number
Custom	HEL80 LA-3161P
Date	Thursday, February 23, 2006
Sheet	31 of 43

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Issued Date	2005/10/06	Deciphered Date	2006/10/06			
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				BIOS & EC I/O Port		
				Size	Document Number	Rev
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				Date:	Thursday, February 23, 2006	ISheet 32 of 43

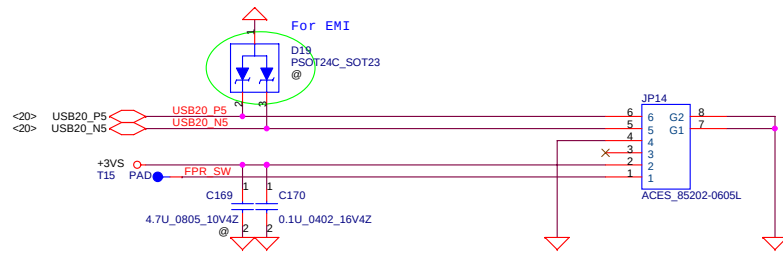


LID Switch



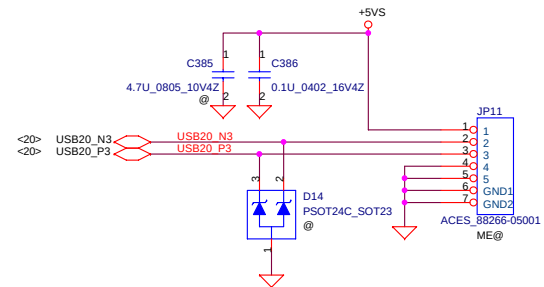
12/9 Change to SA032120010

Finger Print board + MP3 Module CONN.

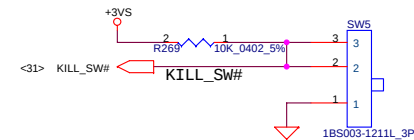


ACES

CMOS Camera Conn

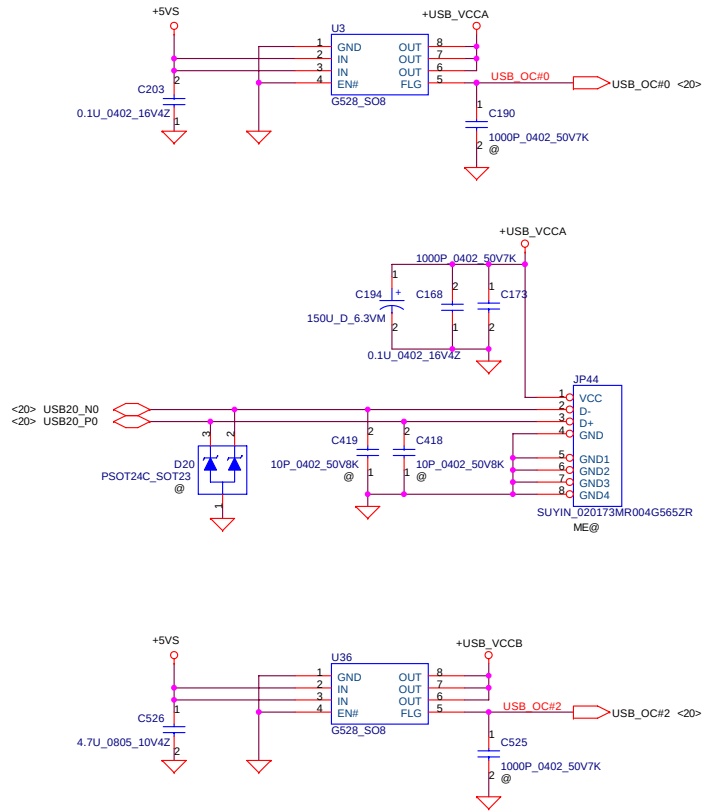


Kill Switch

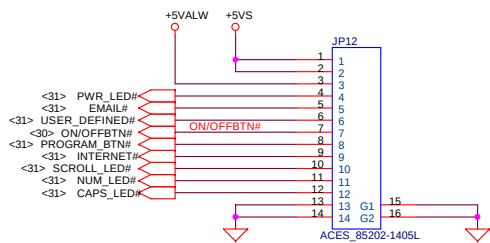


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Issued Date	2005/10/06	Deciphered Date	2006/10/06	Title	DC/DC Circuit
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				Custom	HEL80 LA-3161P
				Date:	Thursday, February 23, 2006
				Sheet	33 of 43
				Rev	0.2

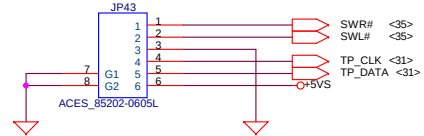
USB Port



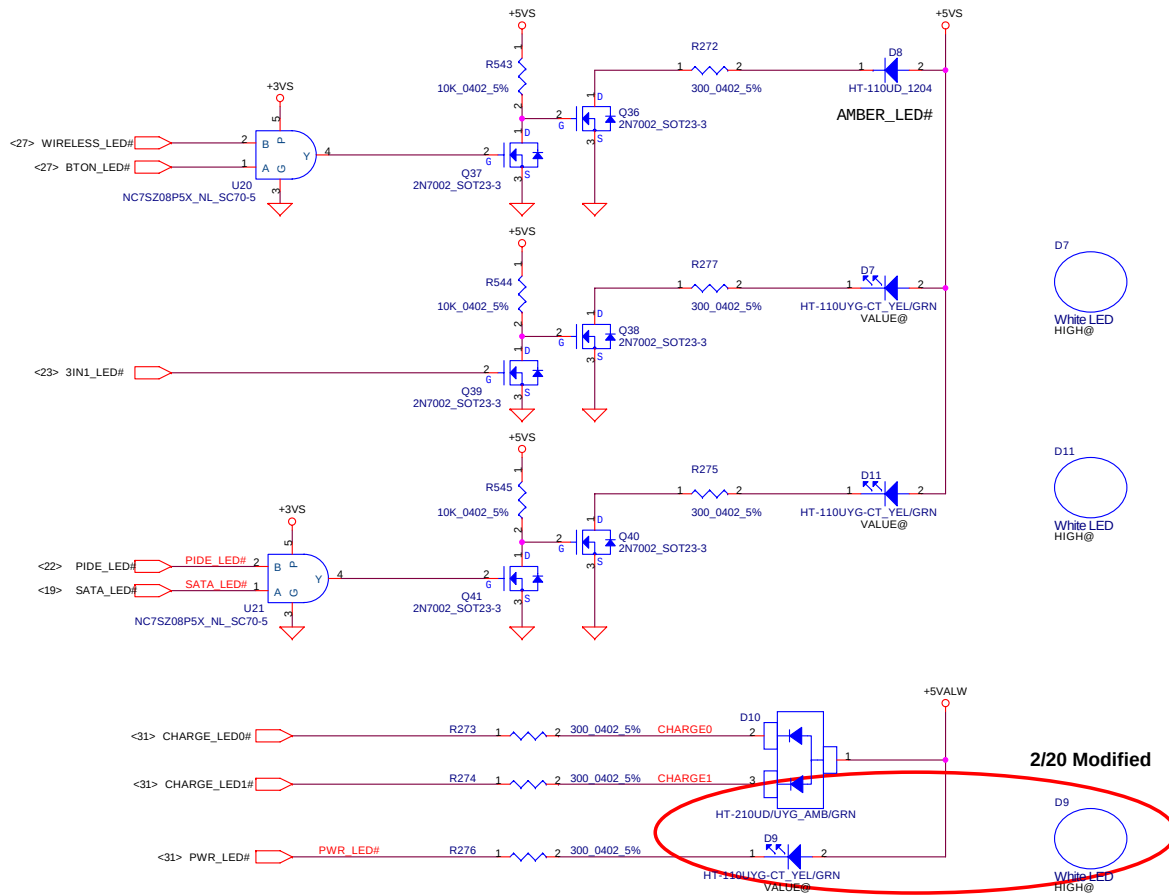
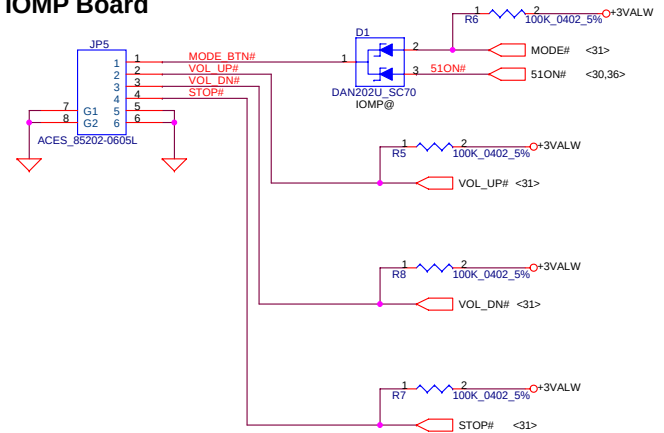
Switch Board CONN.



T/P Board

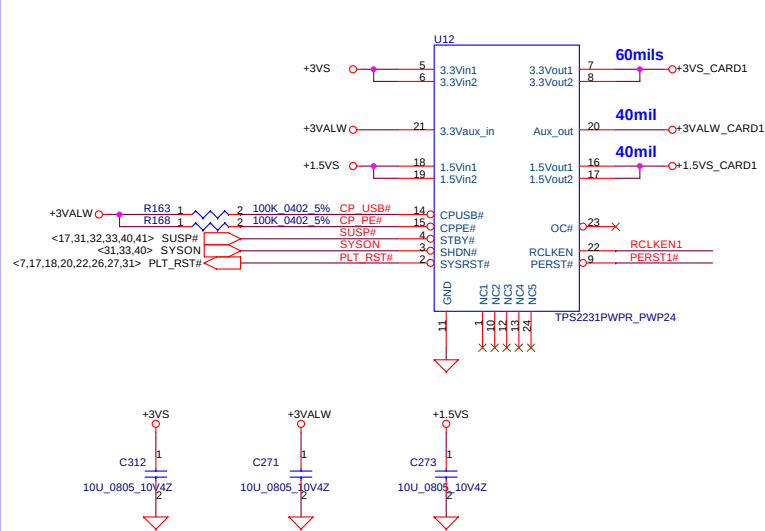


IOMP Board

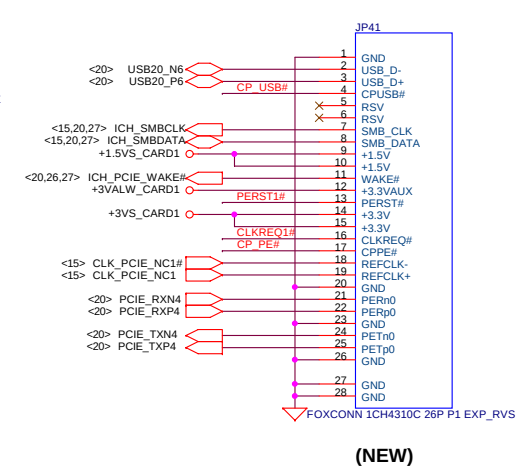


Security Classification	Compal Secret Data			Compal Electronics, Inc.			
Issued Date	2005/10/06	Deciphered Date	2006/10/06	Title	INDICATE LED		
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				Custom	HEL80 LA-3161P	0.2	
				Date:	Thursday, February 23, 2006	Sheet	34 of 43

New Card Power Switch

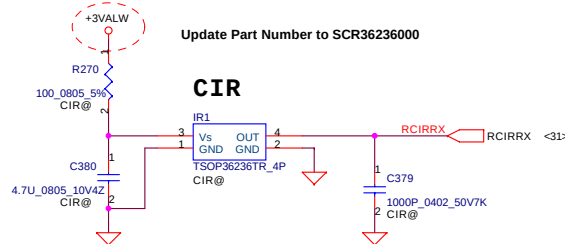


New Card Socket (Left)

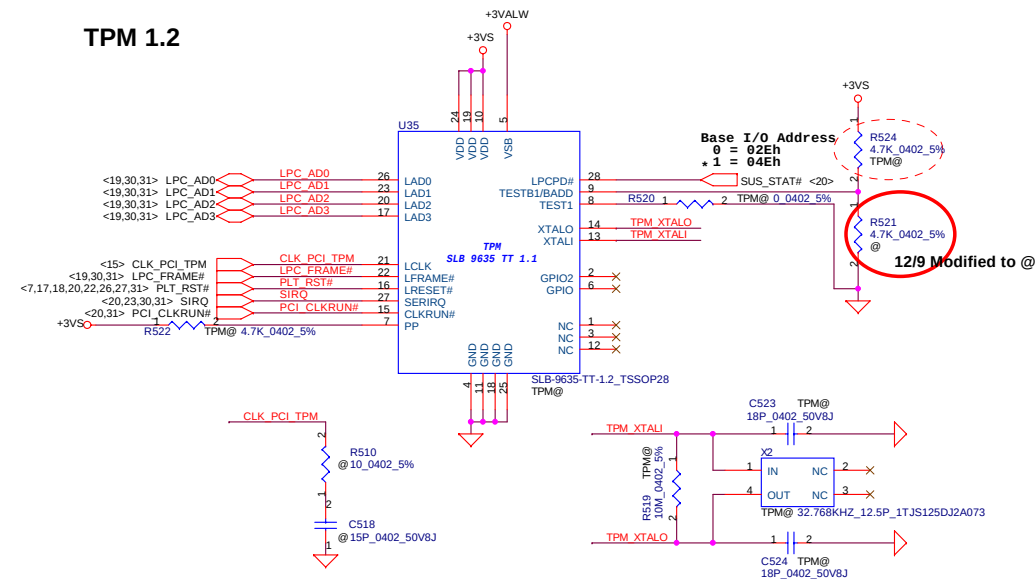


(NEW)
2005/11/4 Modified library pn:SP02000JC00
2005/12/9 Modified footprint to FOX_ICX43201_26P_LB

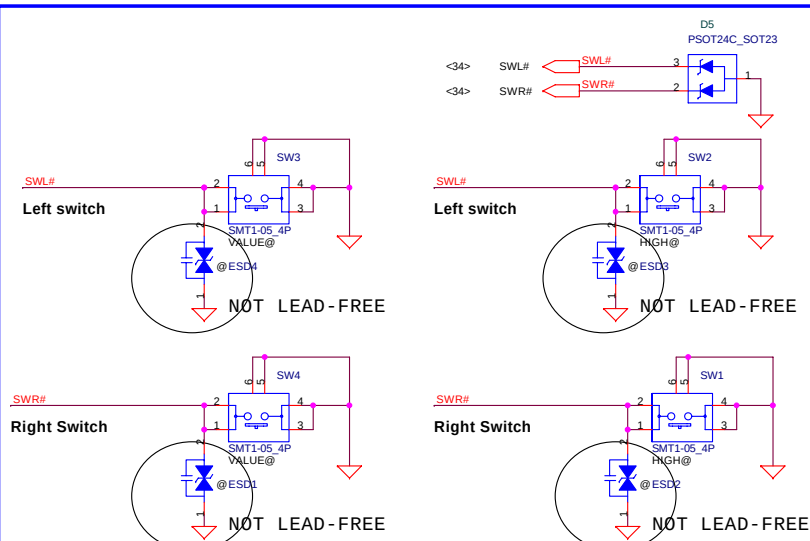
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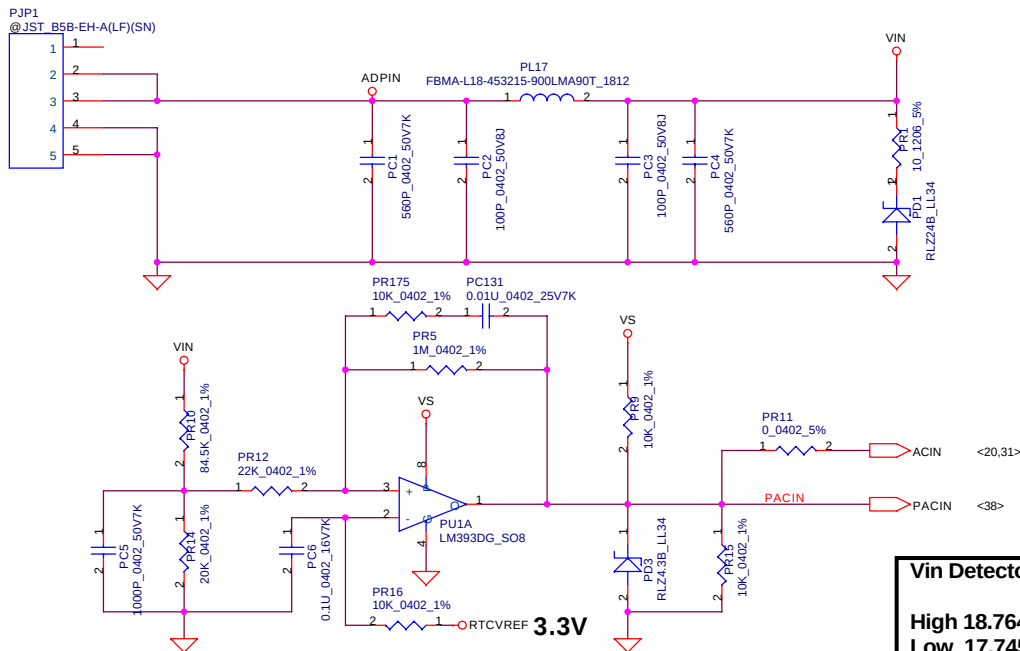
TPM 1.2



Note : TPM IC Lead free status is MN



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/10/06	Deciphered Date	2006/10/06	Title	New card
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				Customer	HEL80 LA-3161P
				Date	Thursday, February 23, 2006
				Sheet	35 of 43
				Rev	0.2

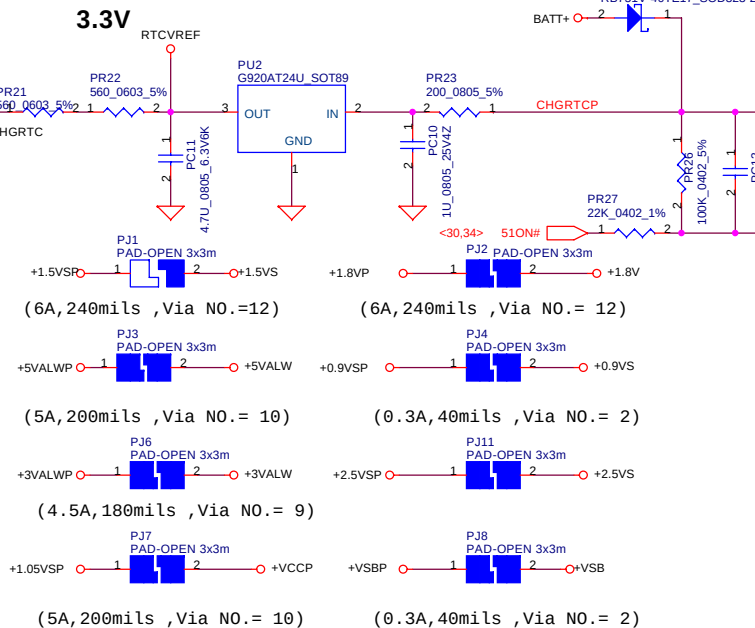
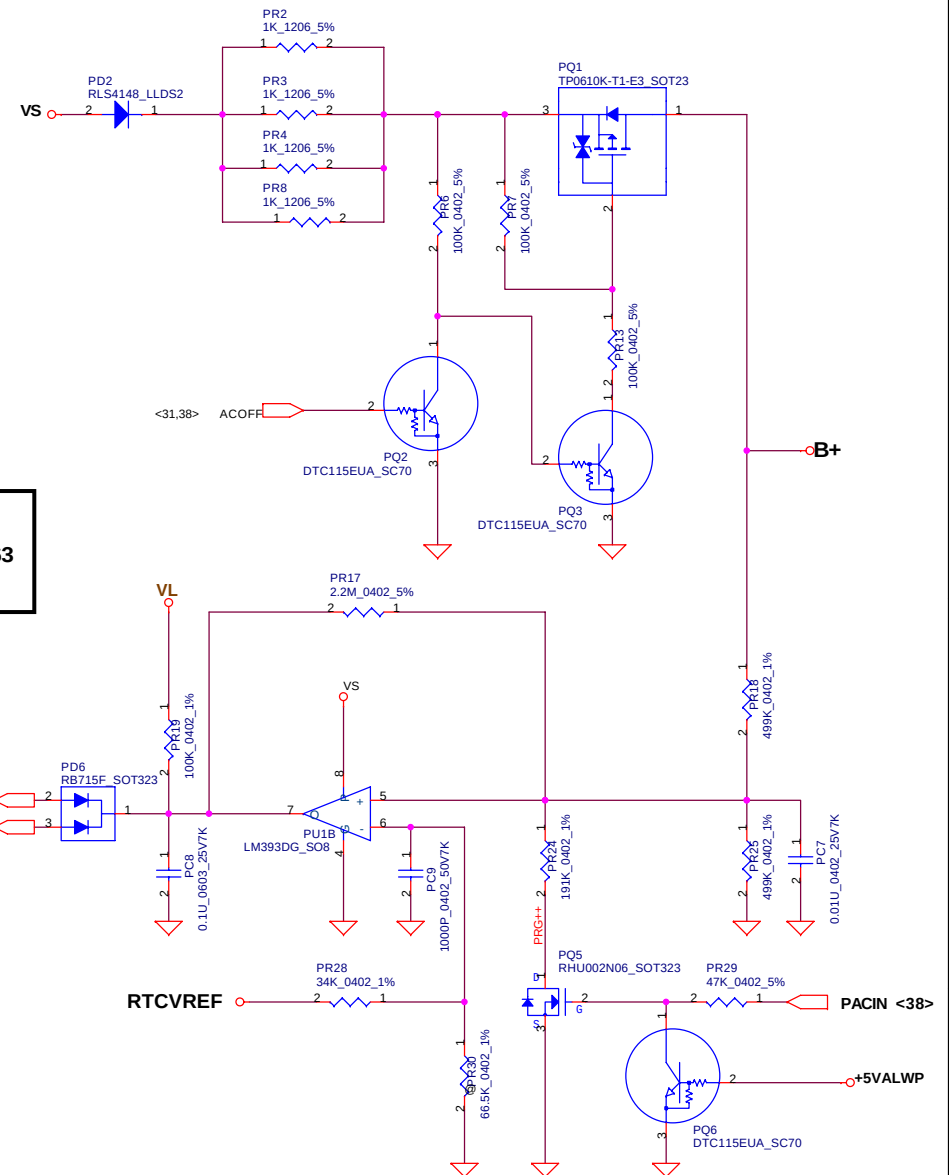


ACIN

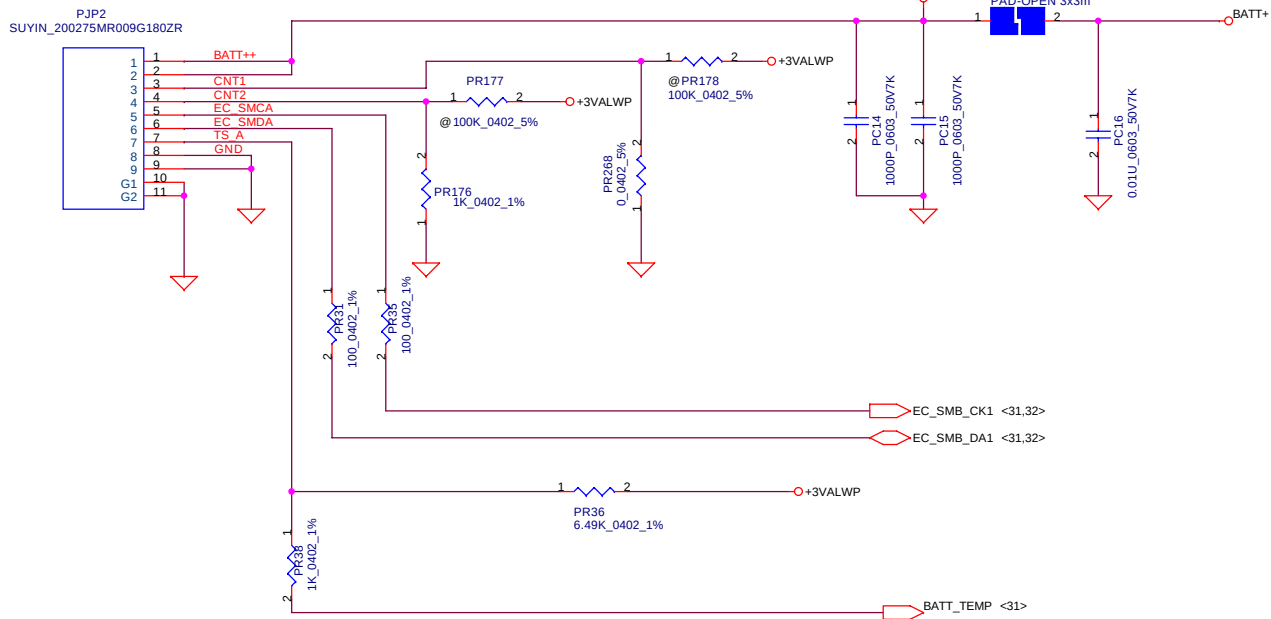
Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

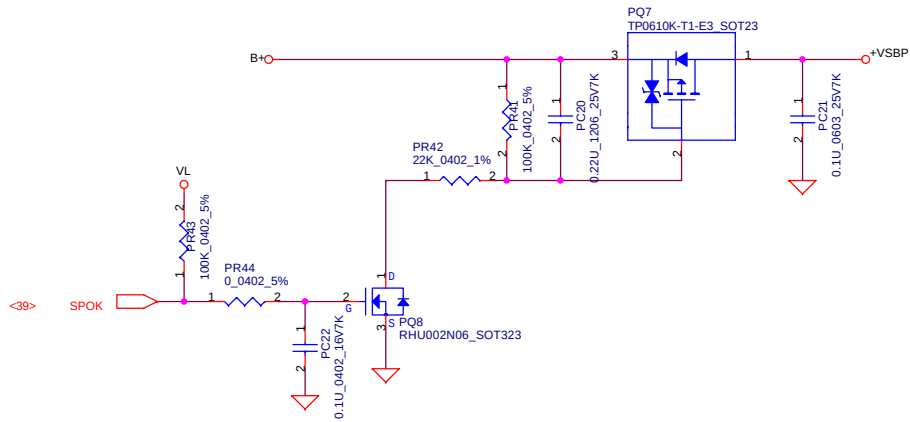
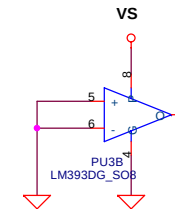
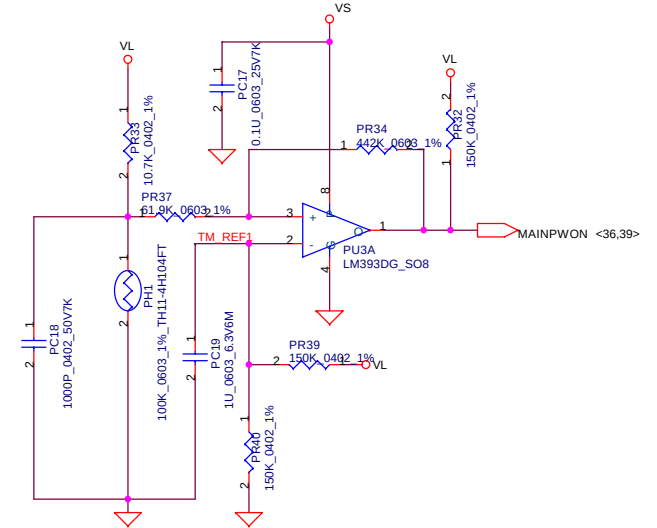
Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



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								0.2			
Date:				Thursday, February 23, 2006				Sheet			
								36 of 43			



PH1 under CPU bottom side :
CPU thermal protection at 85 degree C
Recovery at 70 degree C

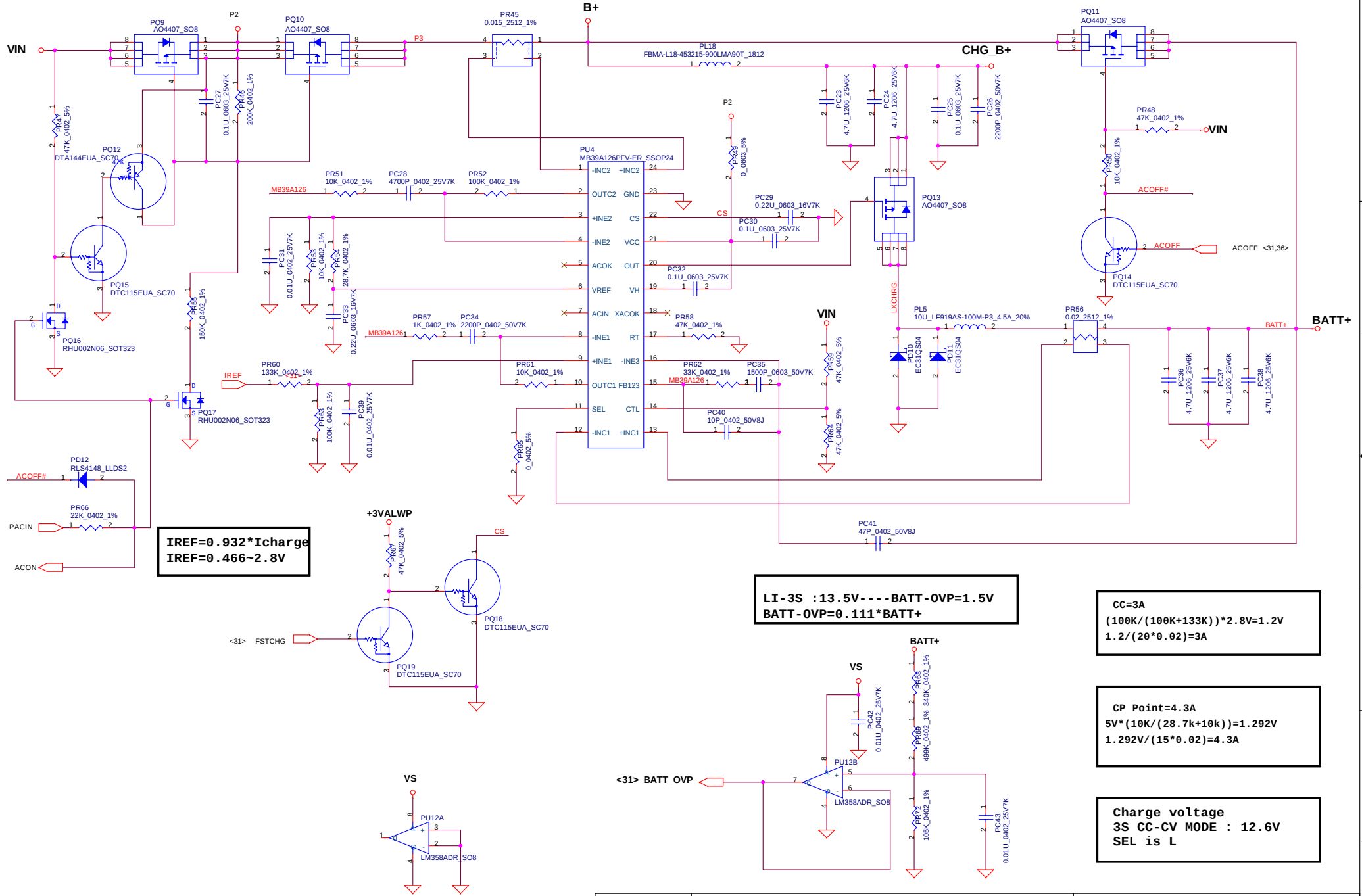


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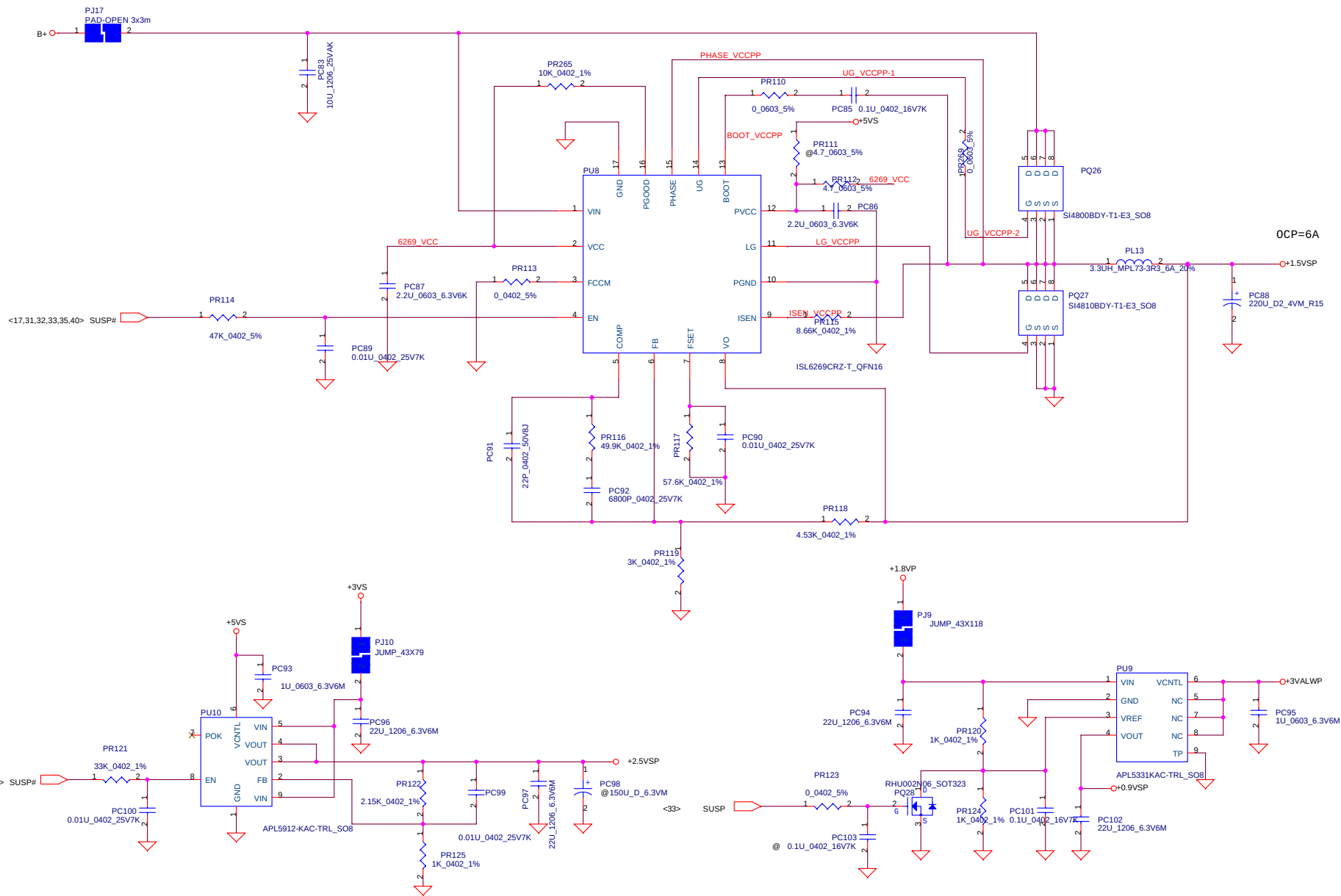
75W PR45=0.02_2512_1% PR54=23.7K_0402_1% Iadp=0~3.71A
90W PR45=0.15_2512_1% PR54=28.7K_0402_1% Iadp=0~4.3A

Fosc=14100/Rt=14100/47=300KHz

Charger

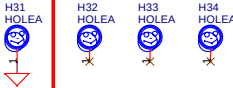
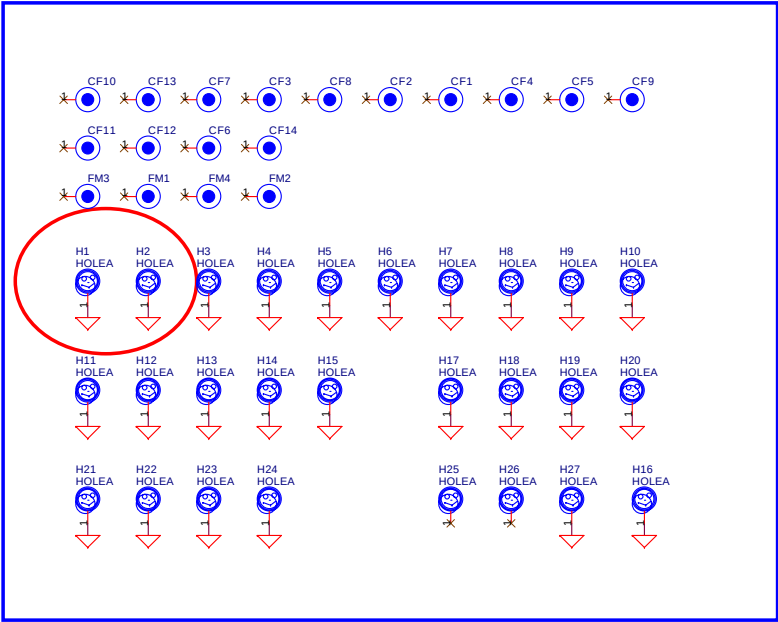


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				Date	Thursday, February 23, 2006	Sheet 38 of 43



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		Size		Document Number				Rev	
		Custom						0.1	
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2/13 Modified



2/13 New added

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				Size Custom	Rev 0.1
				Date: Thursday, February 23, 2006	Sheet 43 of 43