

Compal Confidential

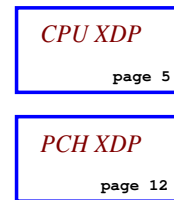
QAL30 Project

LA-8061P REV 0.4 Schematic

Intel Ivy Bridge/Panther Point

2012-01-13 Rev. 0.4

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Issued Date	2011/05/23	Deciphered Date	2012/12/31	Title	Cover Sheet
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Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.168V	0.250 V	0.362 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	QAL30
1	
2	
3	
4	
5	
6	
7	

SMBUS Control Table

	SOURCE	MINI1	BATT 0001 011x b	SODIMM 1001 000x b	SODIMM 1001 010x b	PCH		
EC_SMB_CK1 EC_SMB_DA1	KB930 KB9012	X	V	X	X	X		
EC_SMB_CK2 EC_SMB_DA2	KB930 KB9012	X	X	X	X	V		
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	V	V			
PCH_SML1CLK PCH_SML1DATA	PCH	X	X	X	X			

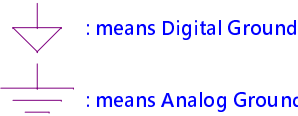
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	TPM
PCI3	None
PCI4	None

PCH	USB PORT#	DESTINATION
	0	USB2/3 (Left Hand disc front)
	1	USB2/3 (Left Hand disc back)
	2	None
	3	None
	4	USB2 (Right Hand side front)
	5	None
	6	None
	7	None
	8	None
	9	USB2 (Left Hand side back)
	10	CAMERA
	11	Card Reader
	12	None
	13	BT Comb

OPTIMUS: XDP@/D@

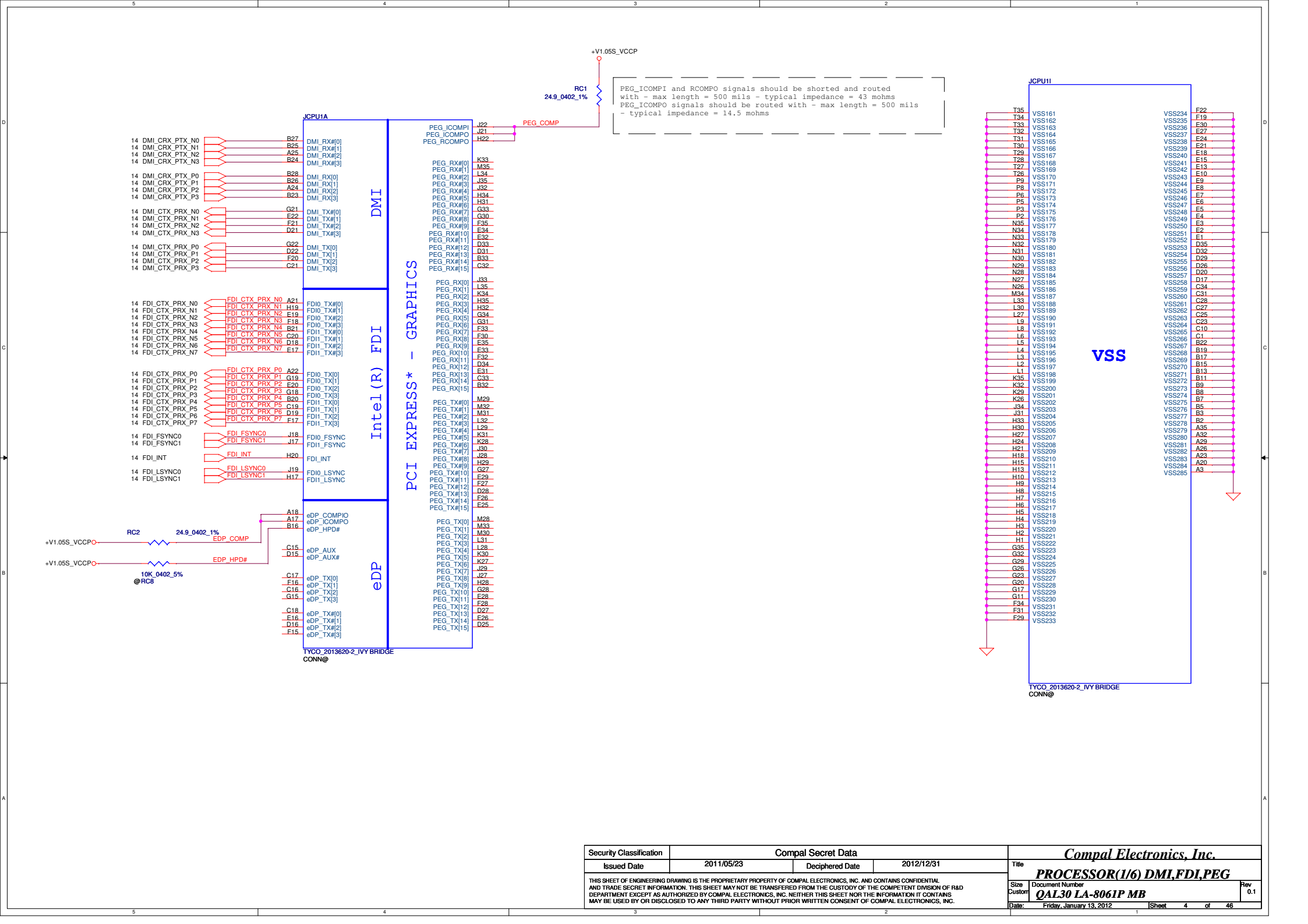
CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_A	VGA		
	CLKOUT_PEG_B	None		

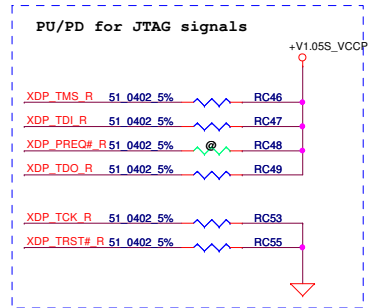
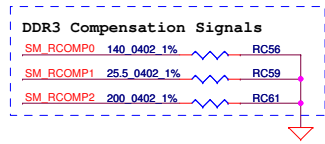
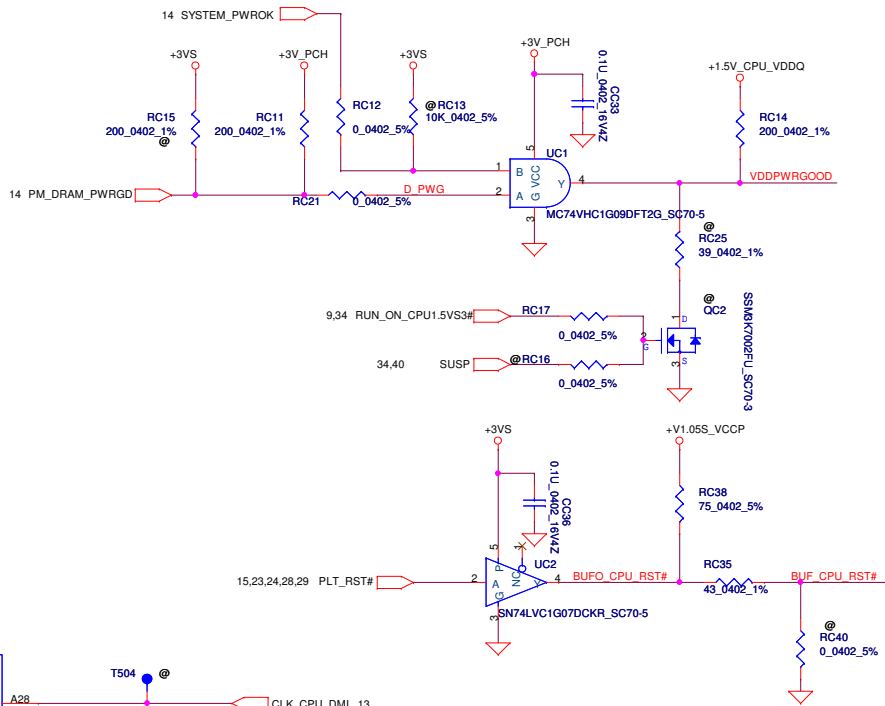
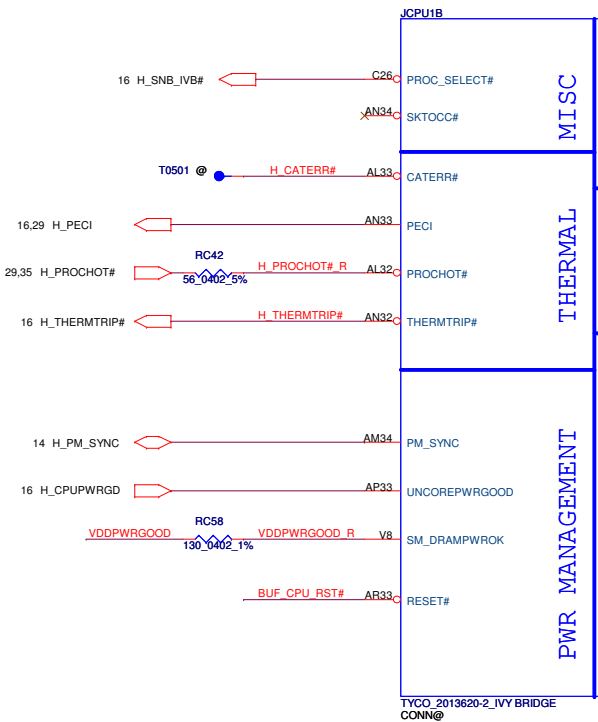
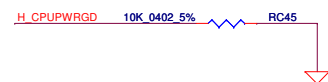
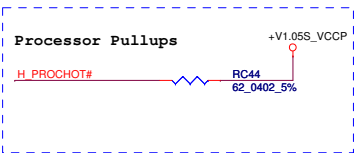
Symbol Note :

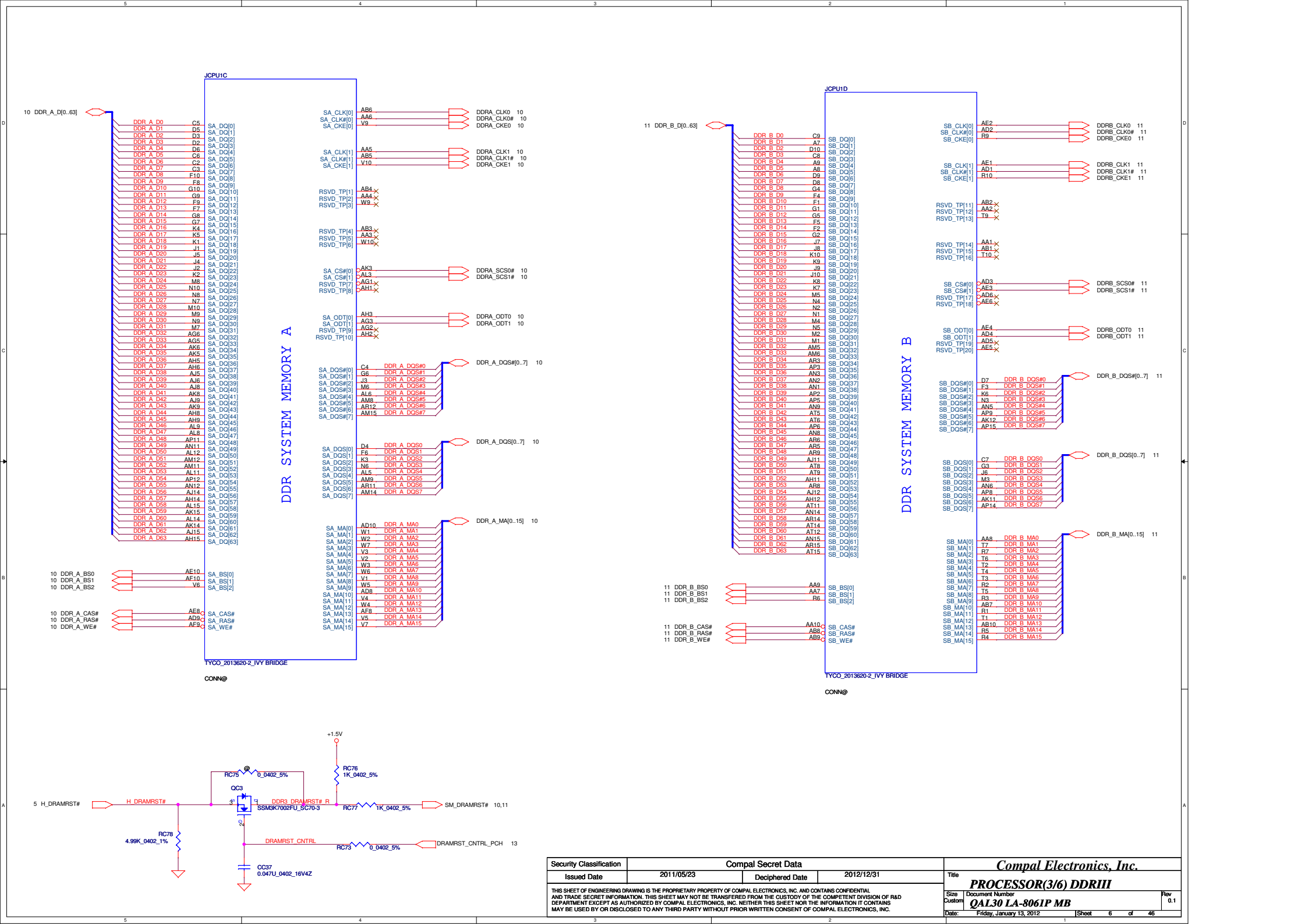


SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

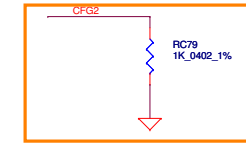
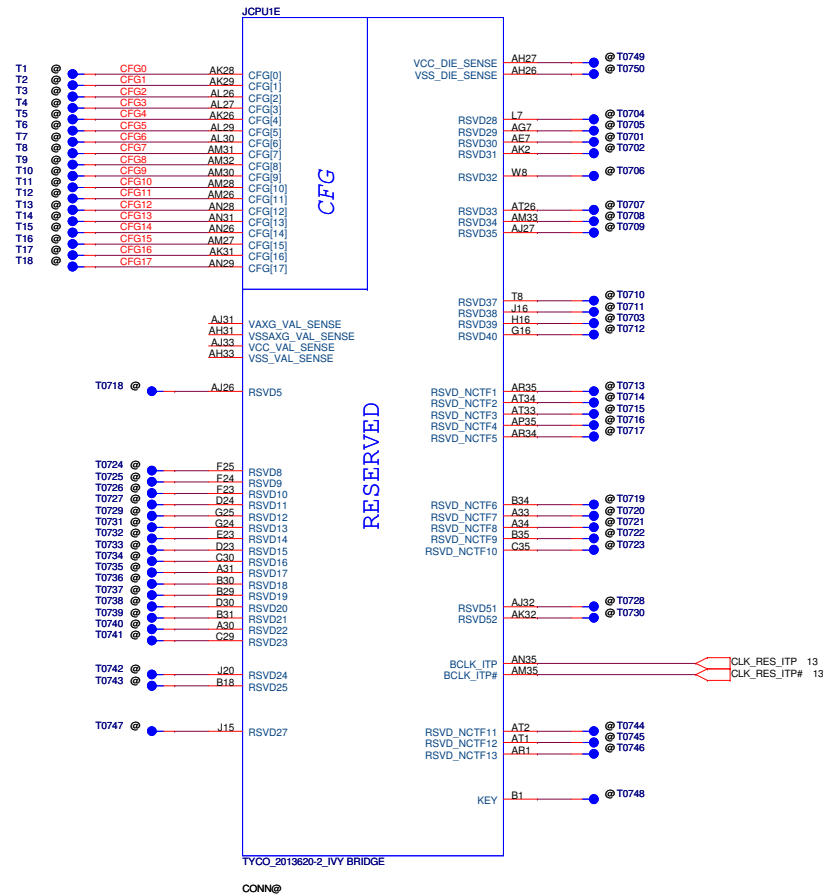
PCI EXPRESS	DESTINATION
Lane 1	LAN
Lane 2	WLAN
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None



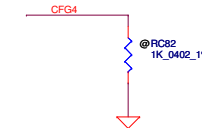




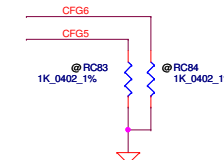
CFG Straps for Processor



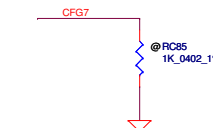
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



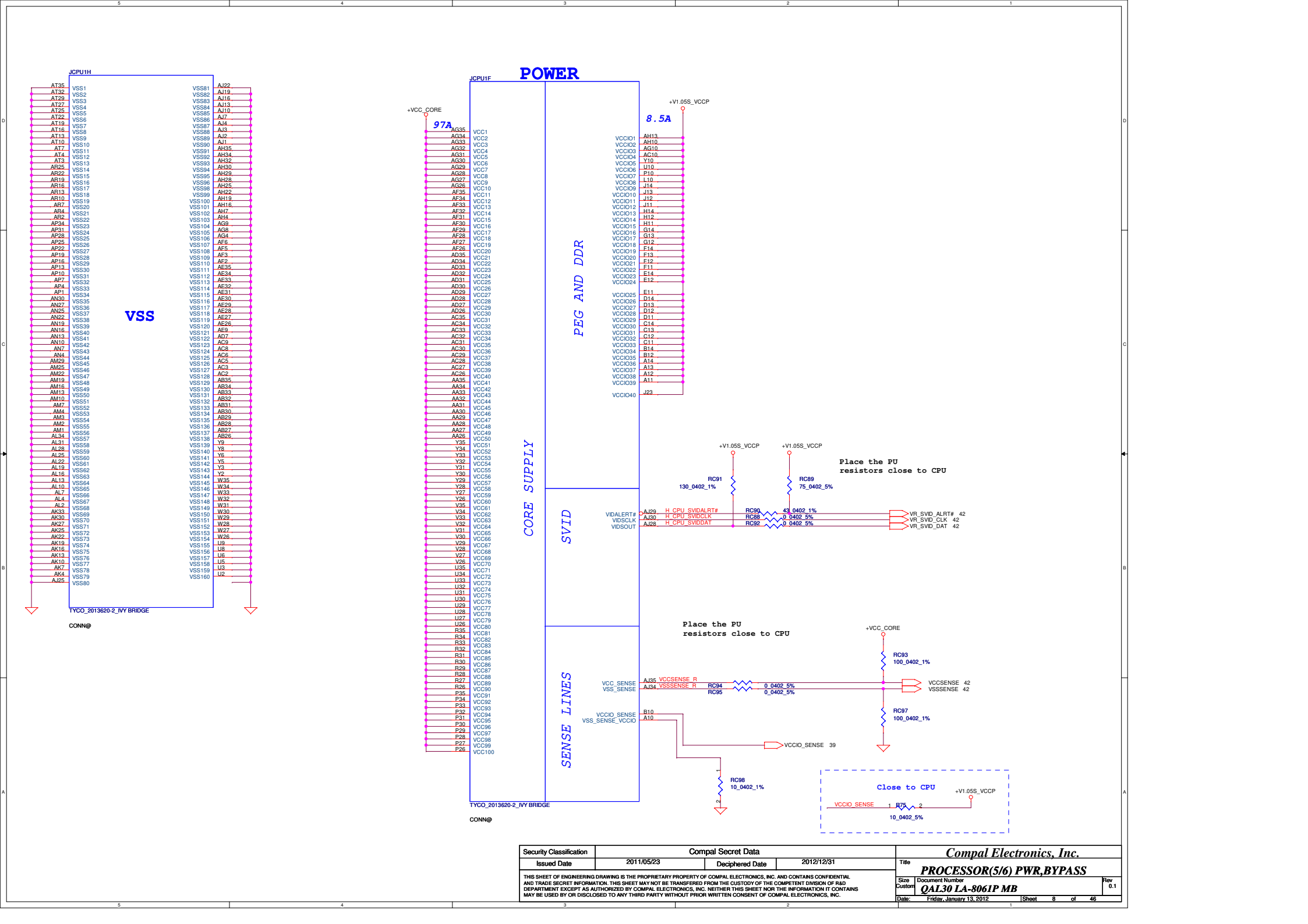
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

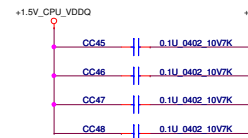


PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



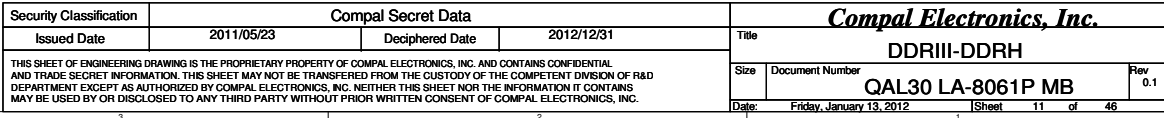
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following RESETB de assertion 0: PEG Wait for BIOS for training

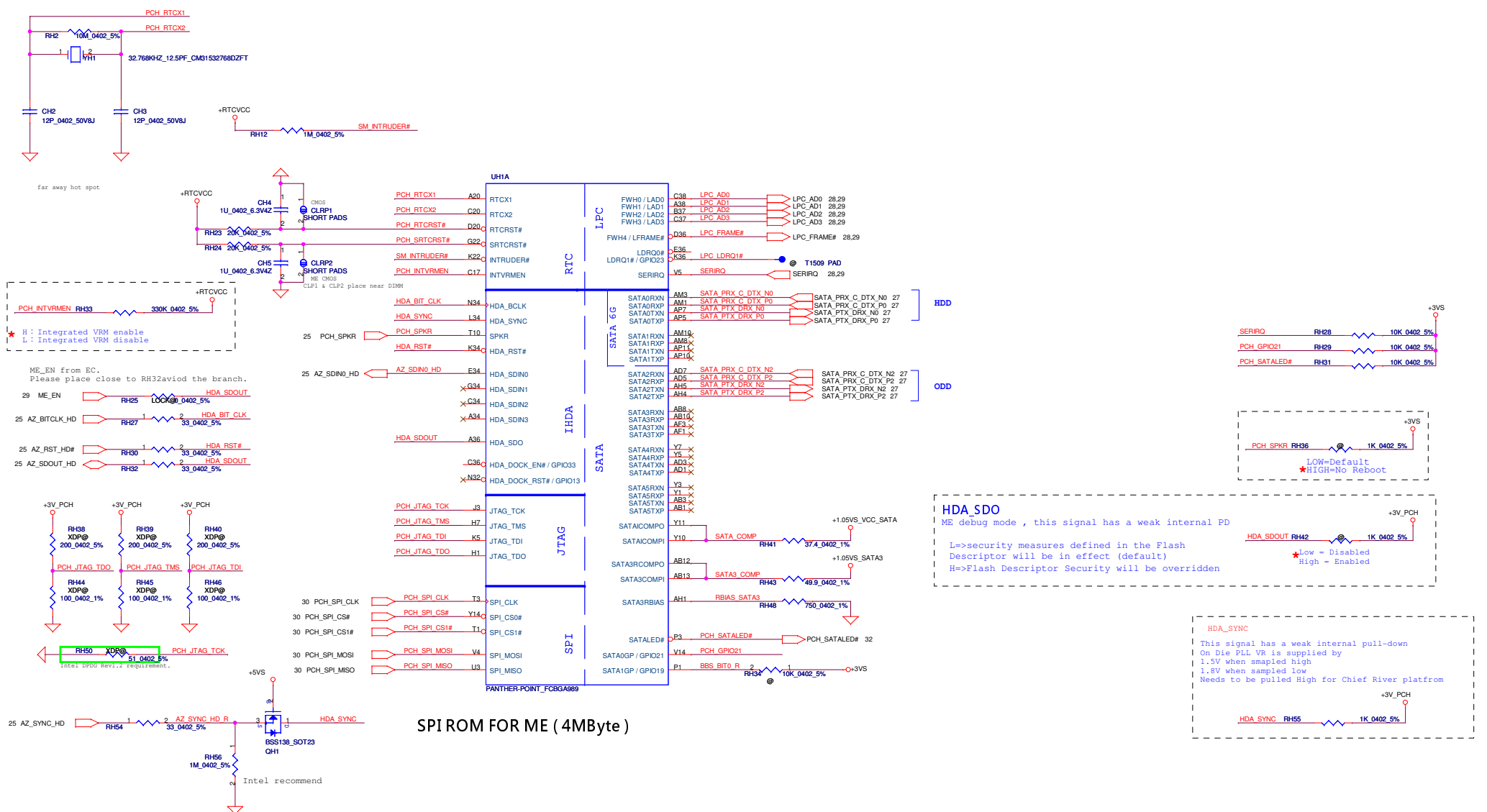


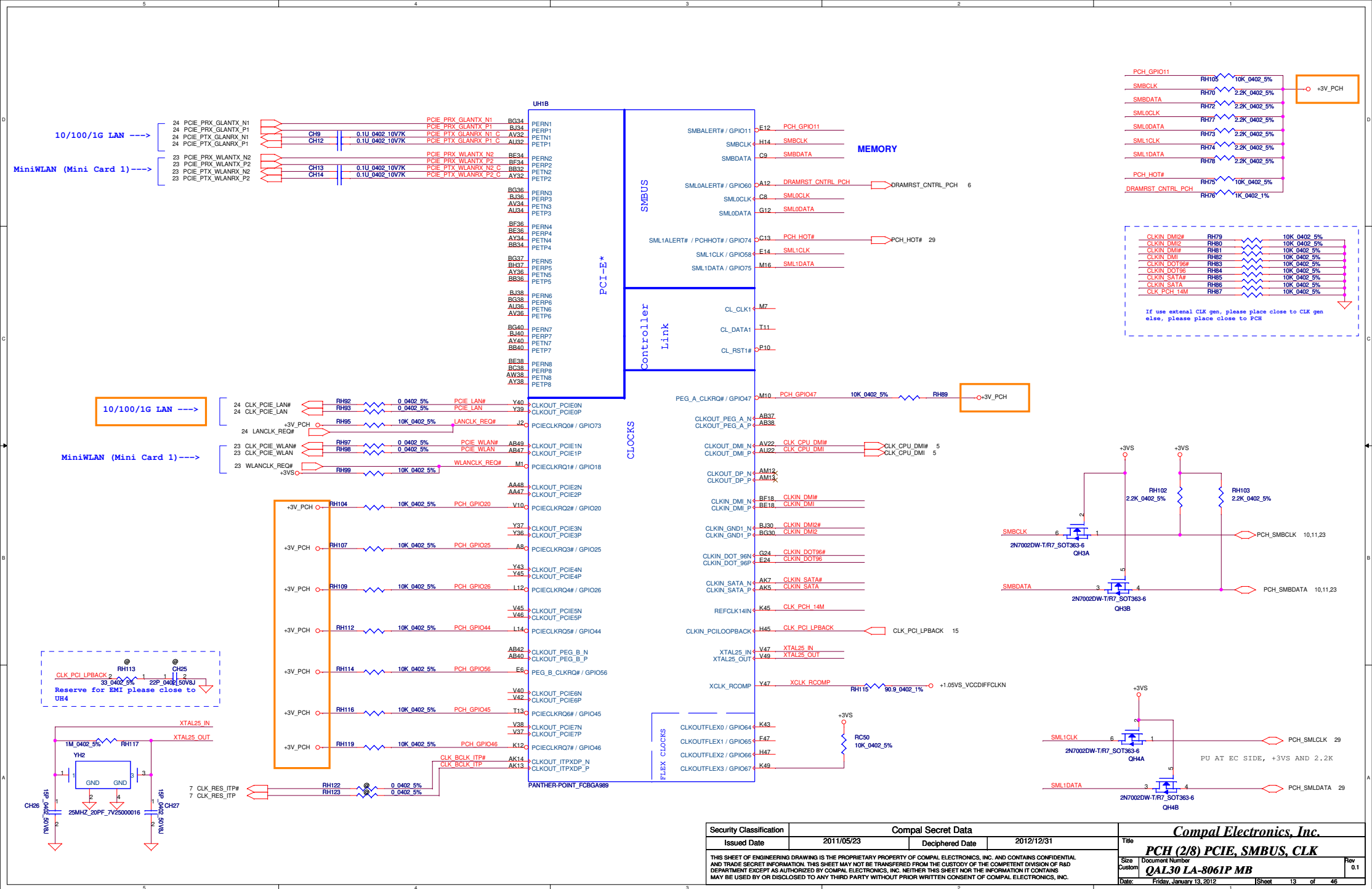


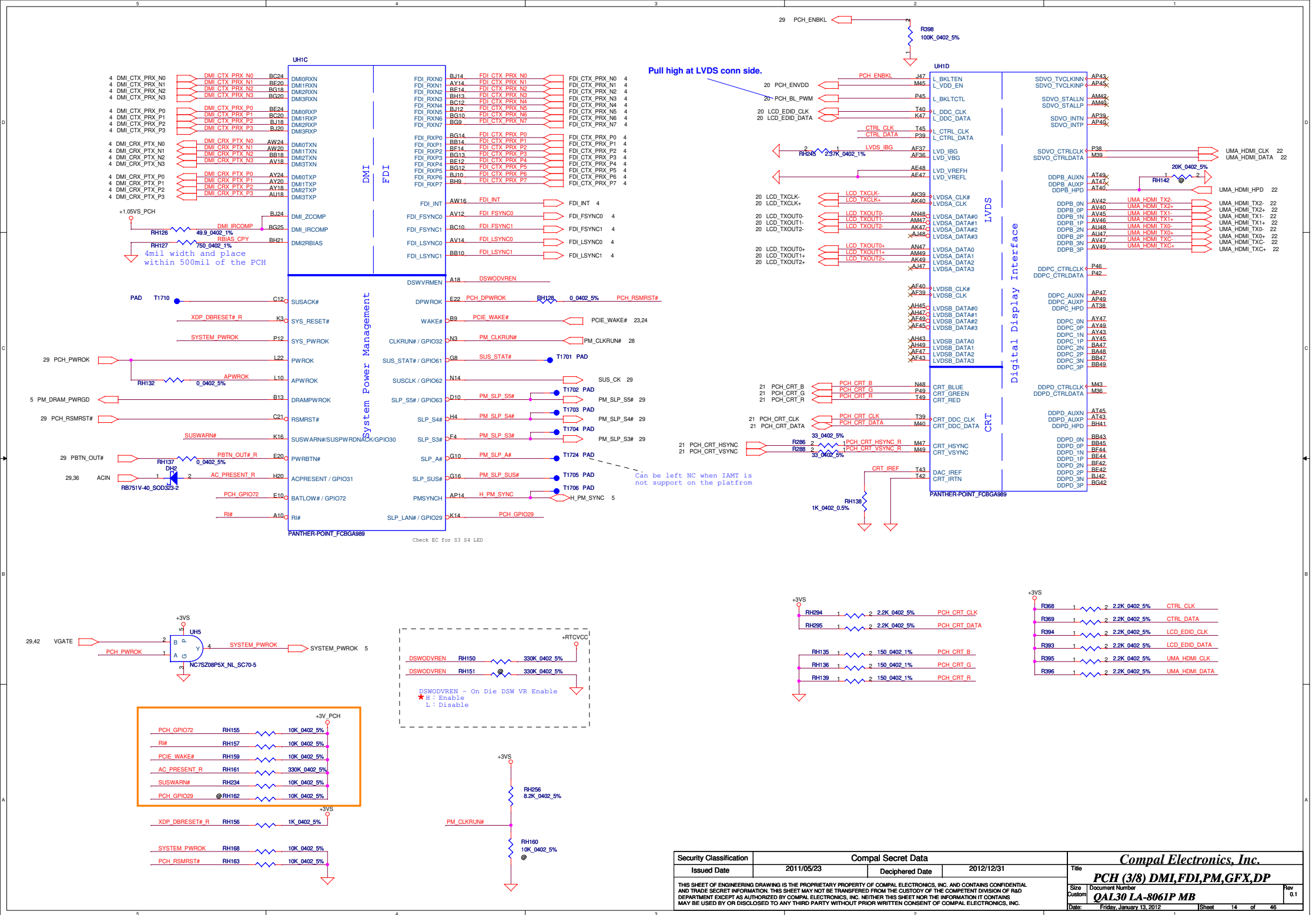
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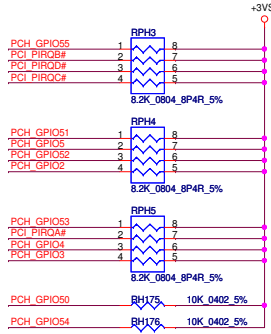
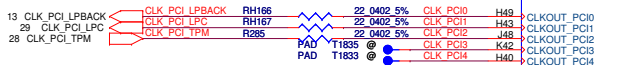
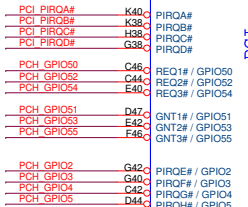
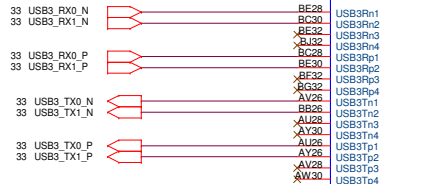






USB3.0 Port0
Port 0 : Left USB3.0

USB3.0 Port1
Port 1 : Left USB3.0 with e-SATA

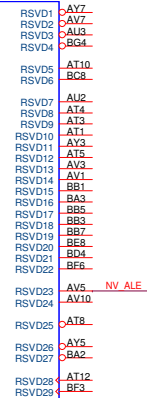


RSVD

PCI

USB

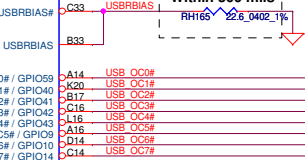
PANTHER-POINT_FCBGA989



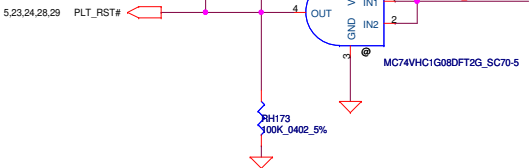
Reserved for USB3.0



Port 9 : RHS SB USB2.0
Port 10 : Int. Carema
Port 11 : Card Reader
Port 13 : BT

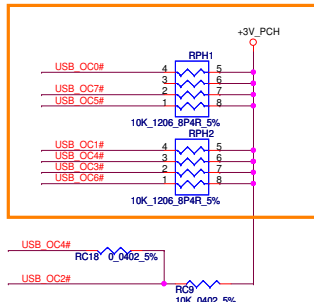
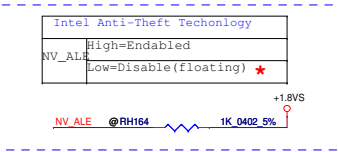


PLT_RST#

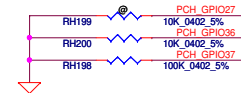
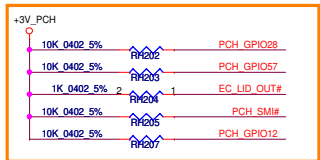
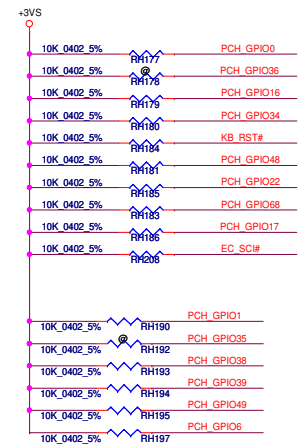


GPIO19 => BBS_BIT0
GPIO51 => BBS_BIT1

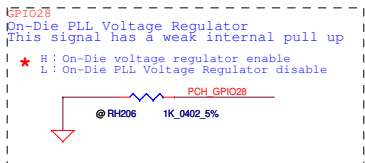
Boot BIOS Strap		
BBS_BIT0	BBS_BIT1	Boot BIOS Location
0	0	LPC
0	1	Reserved(NAND)
1	0	Reserved
1	1	SPI ★



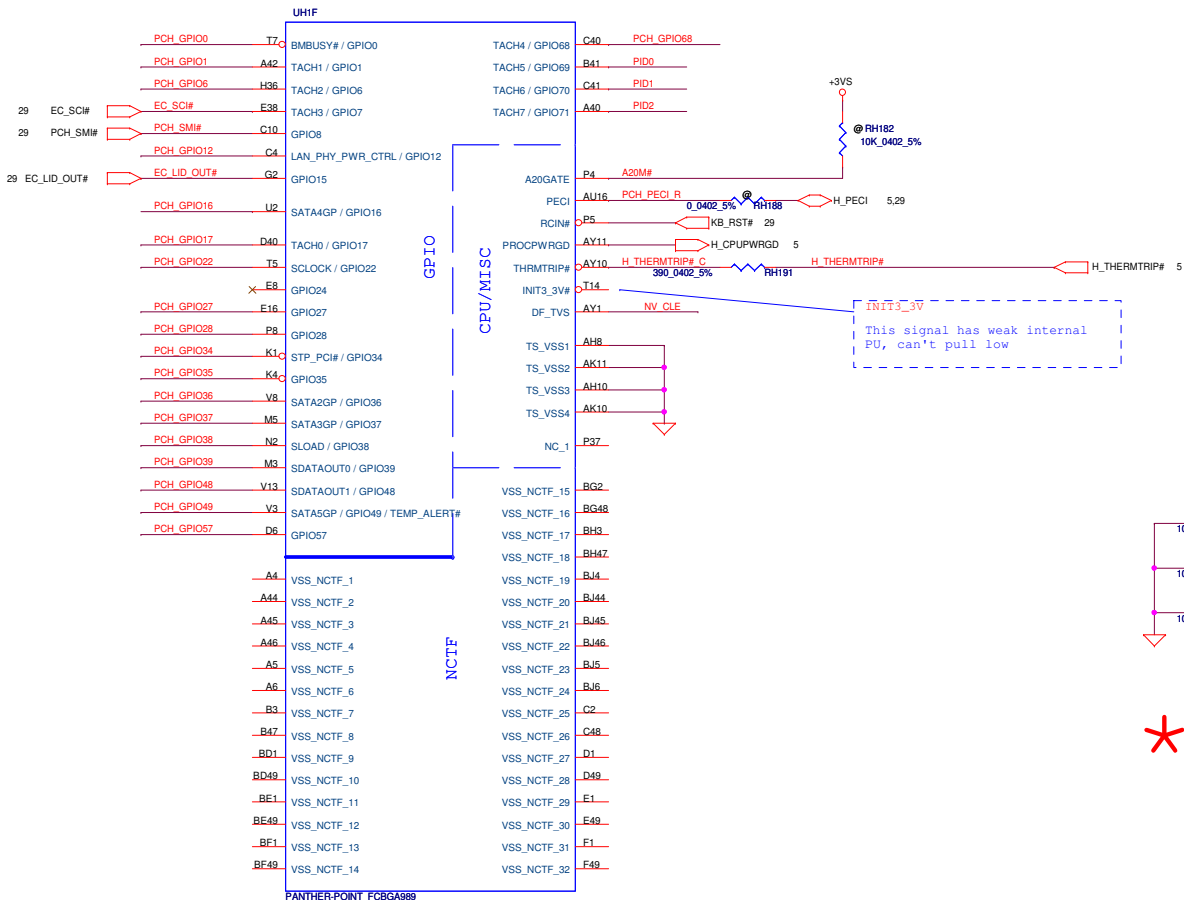
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GPIO36/37
When Unused as GPIO or SATA*GP -
Use 8.2K-10K pull-down to ground.

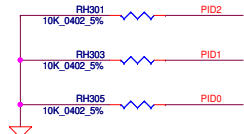
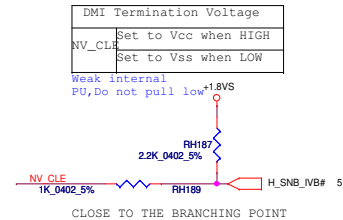


On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable



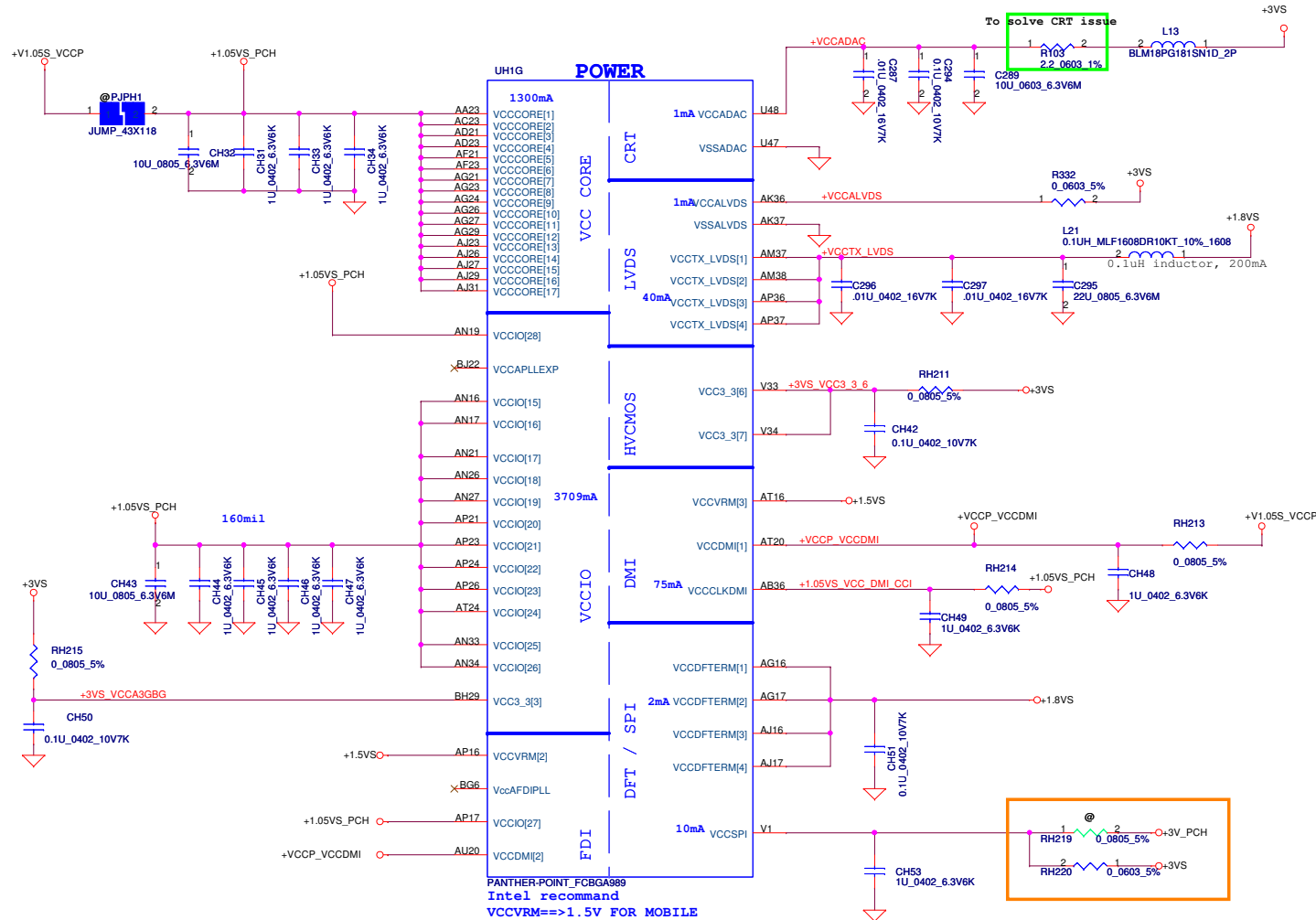
PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16

Please refer to Huron River Debug Board DG 1.2

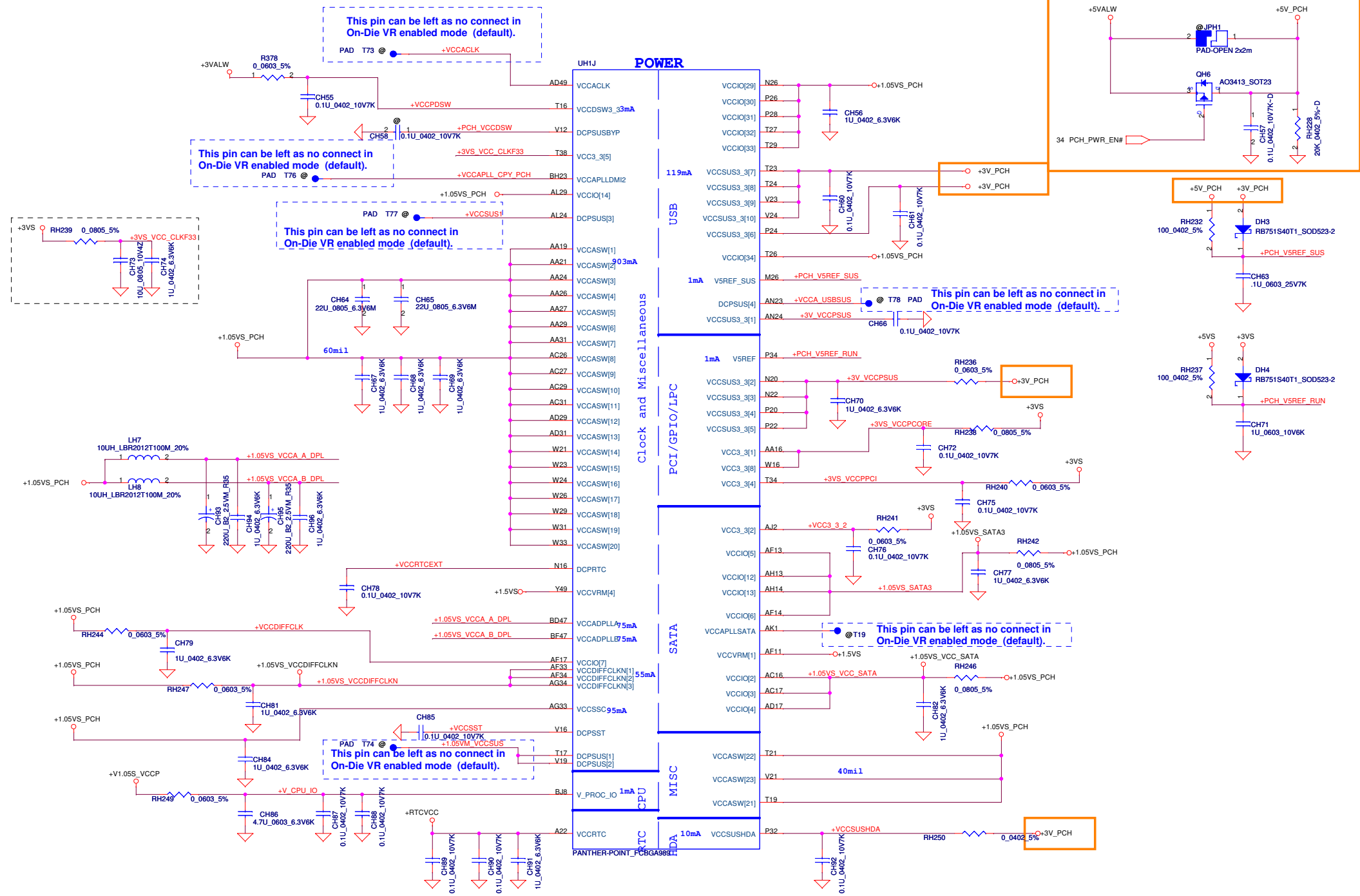


PID :	210	
QAL30	000	(UMA)
QAL31	001	(DIS)
QAL50	010	(UMA)
QAL51	011	(DIS)
KSPD		
Q0000	1XX	

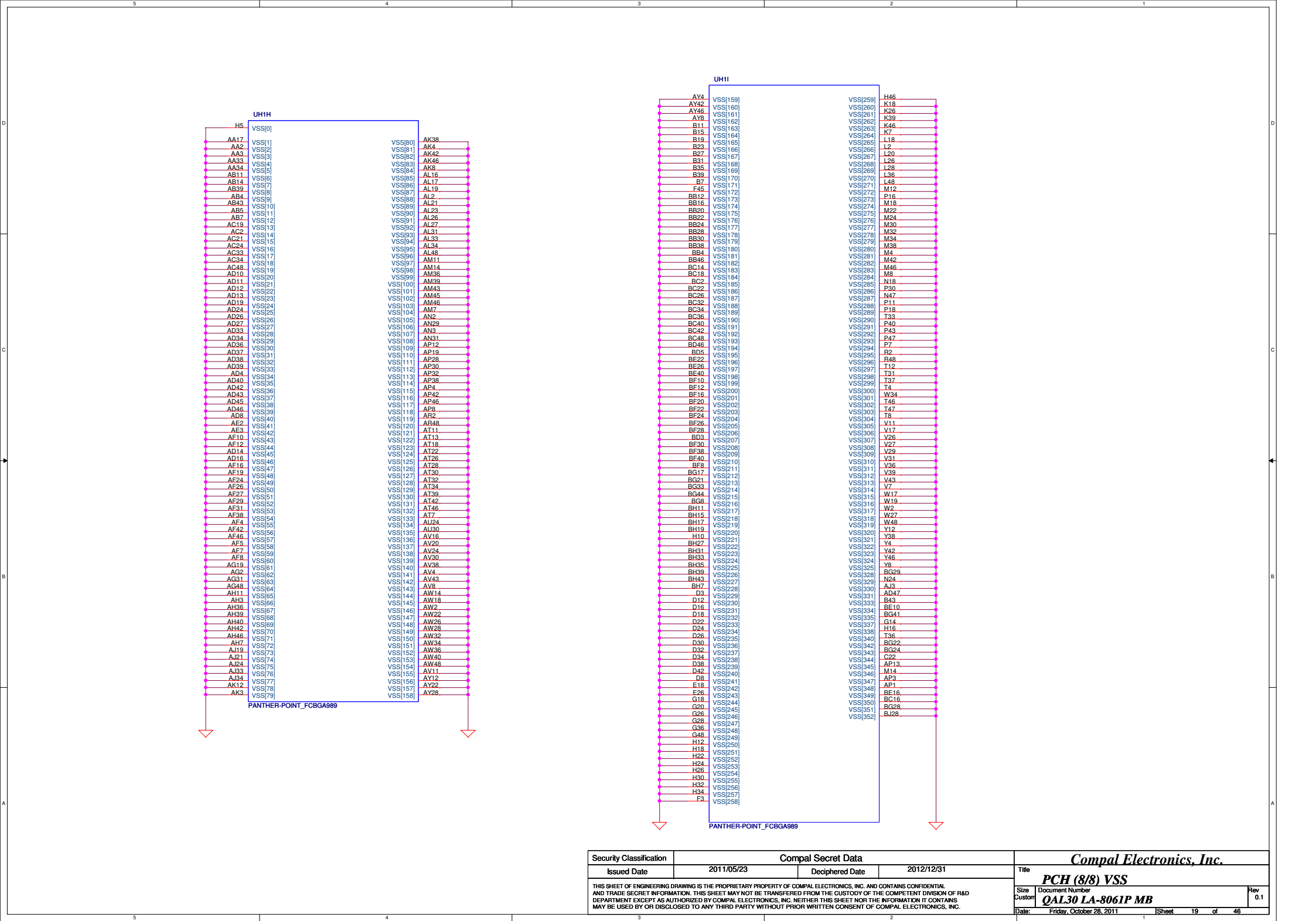
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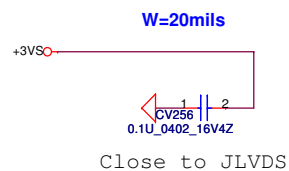
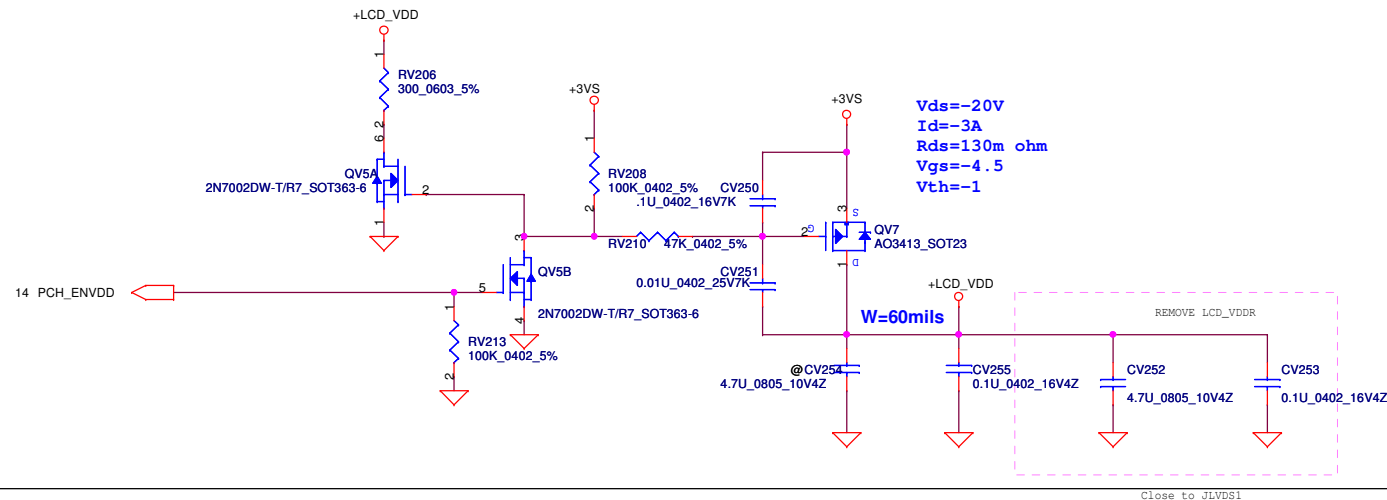
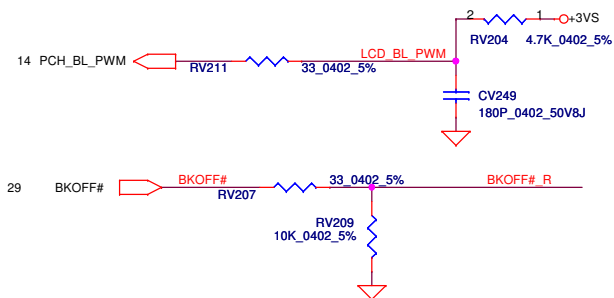


PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04



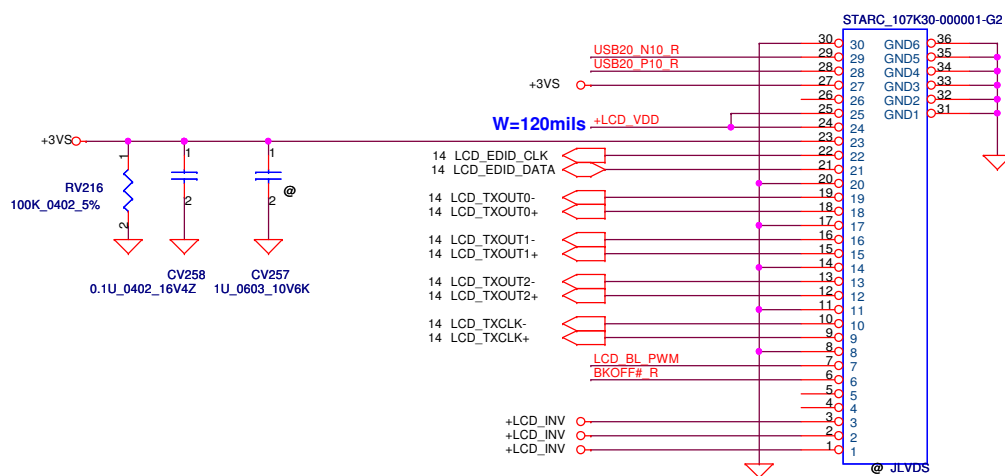
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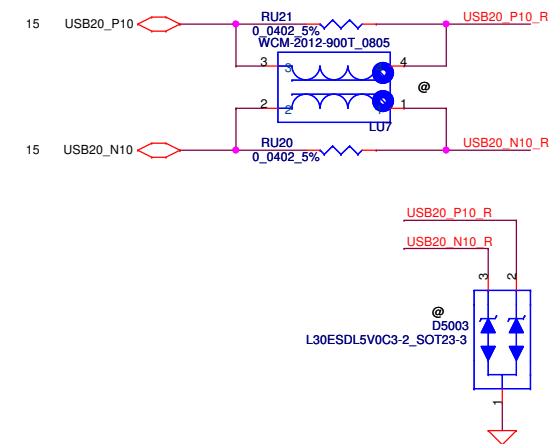
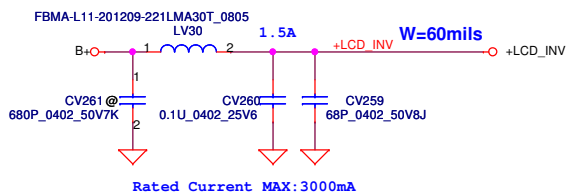


Change to 30 pin.

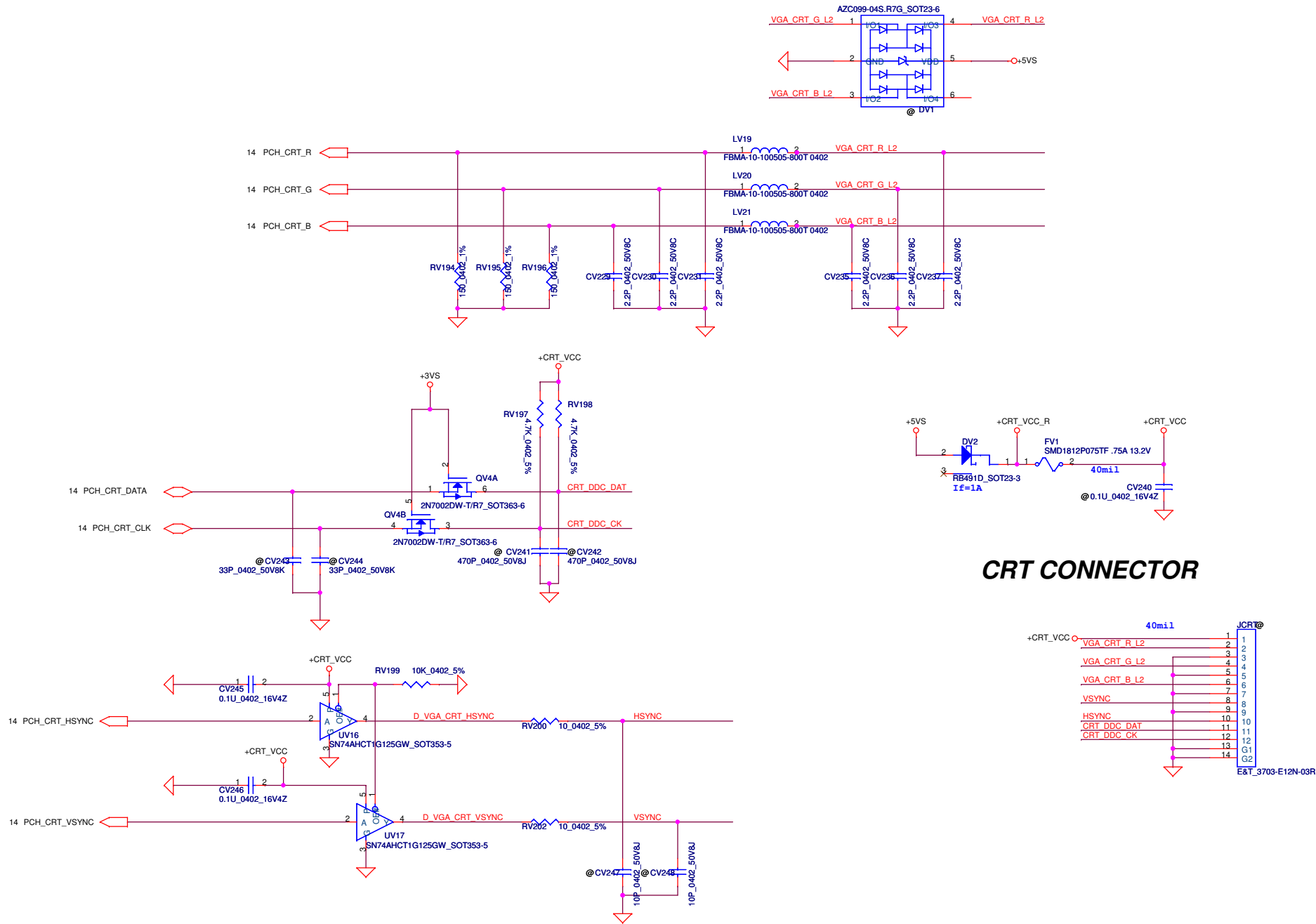
Single Channel LVDS



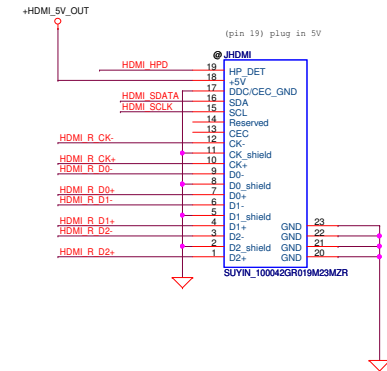
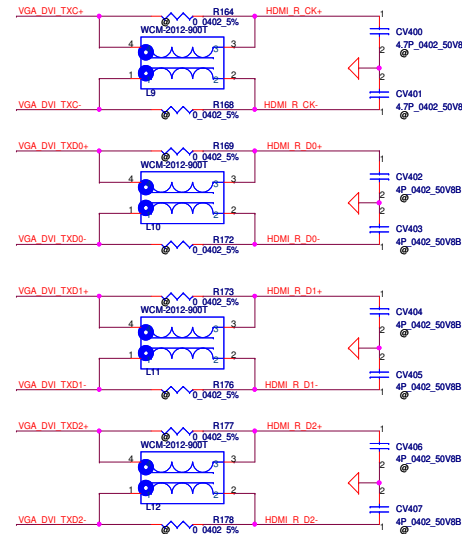
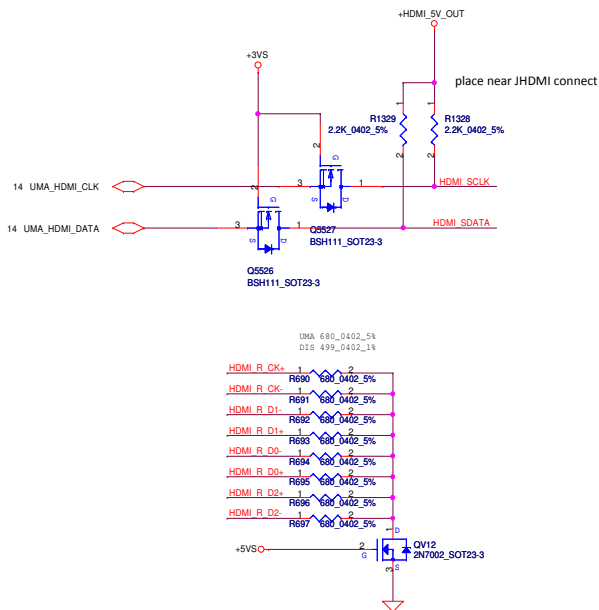
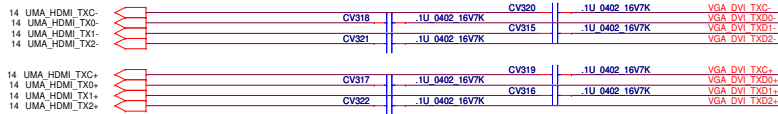
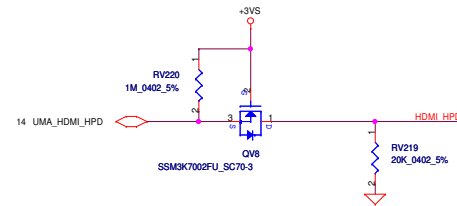
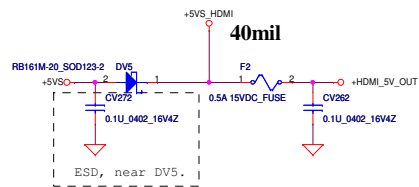
LCD/PANEL BD. Conn.



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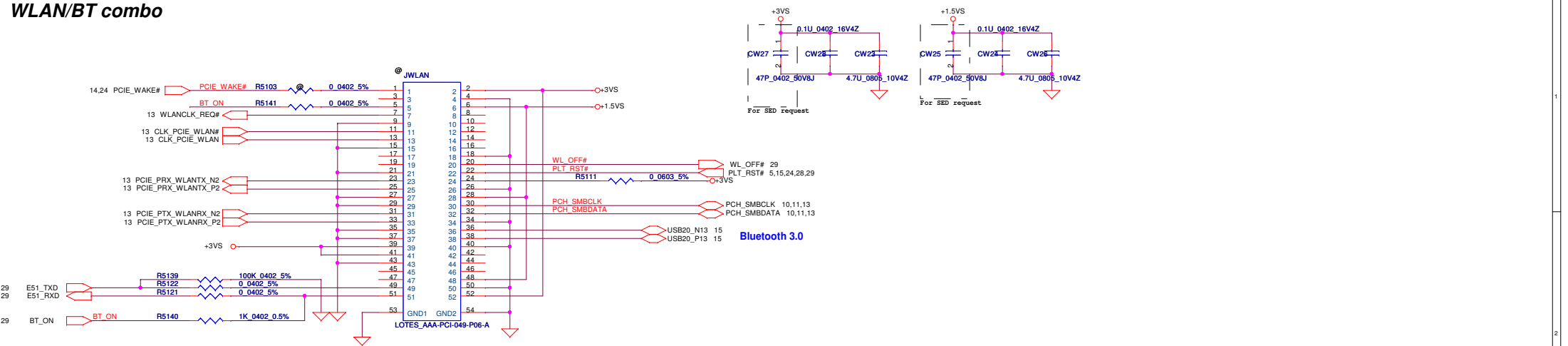


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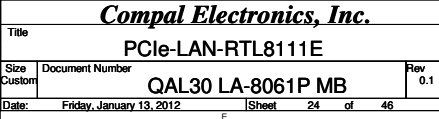


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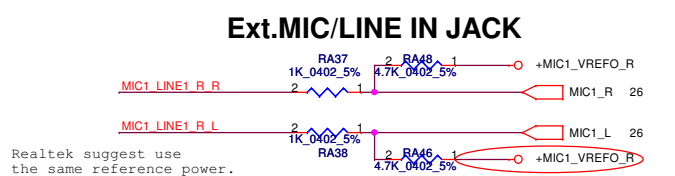
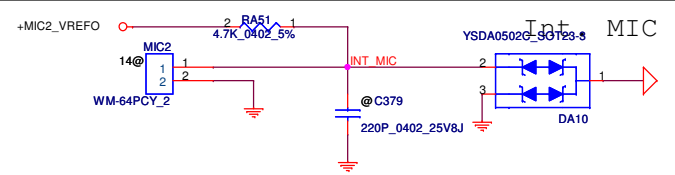
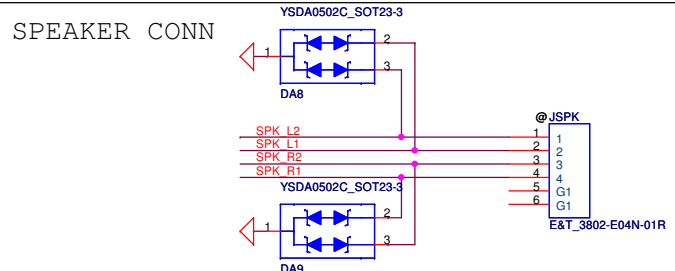
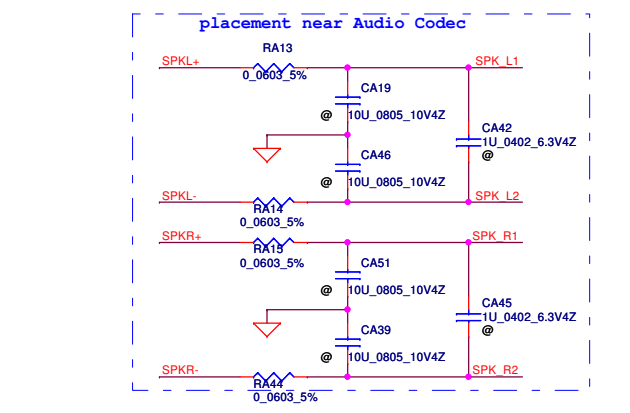
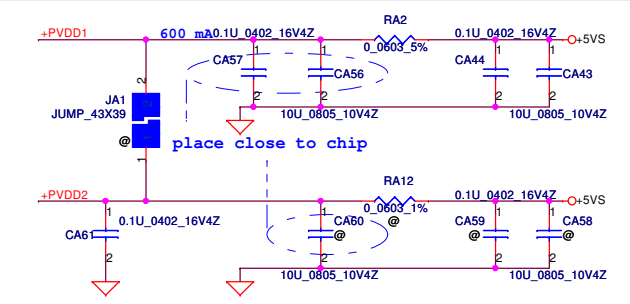
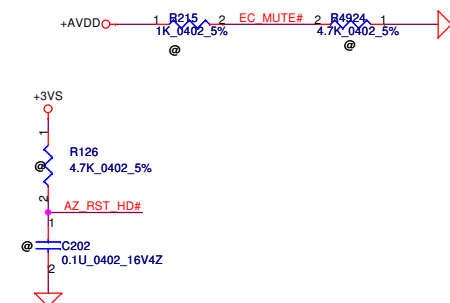
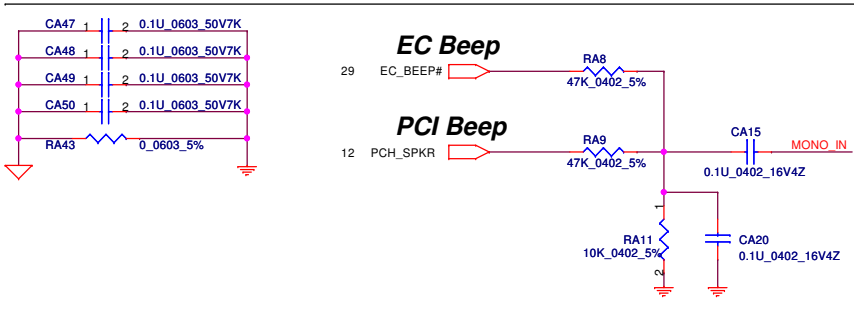
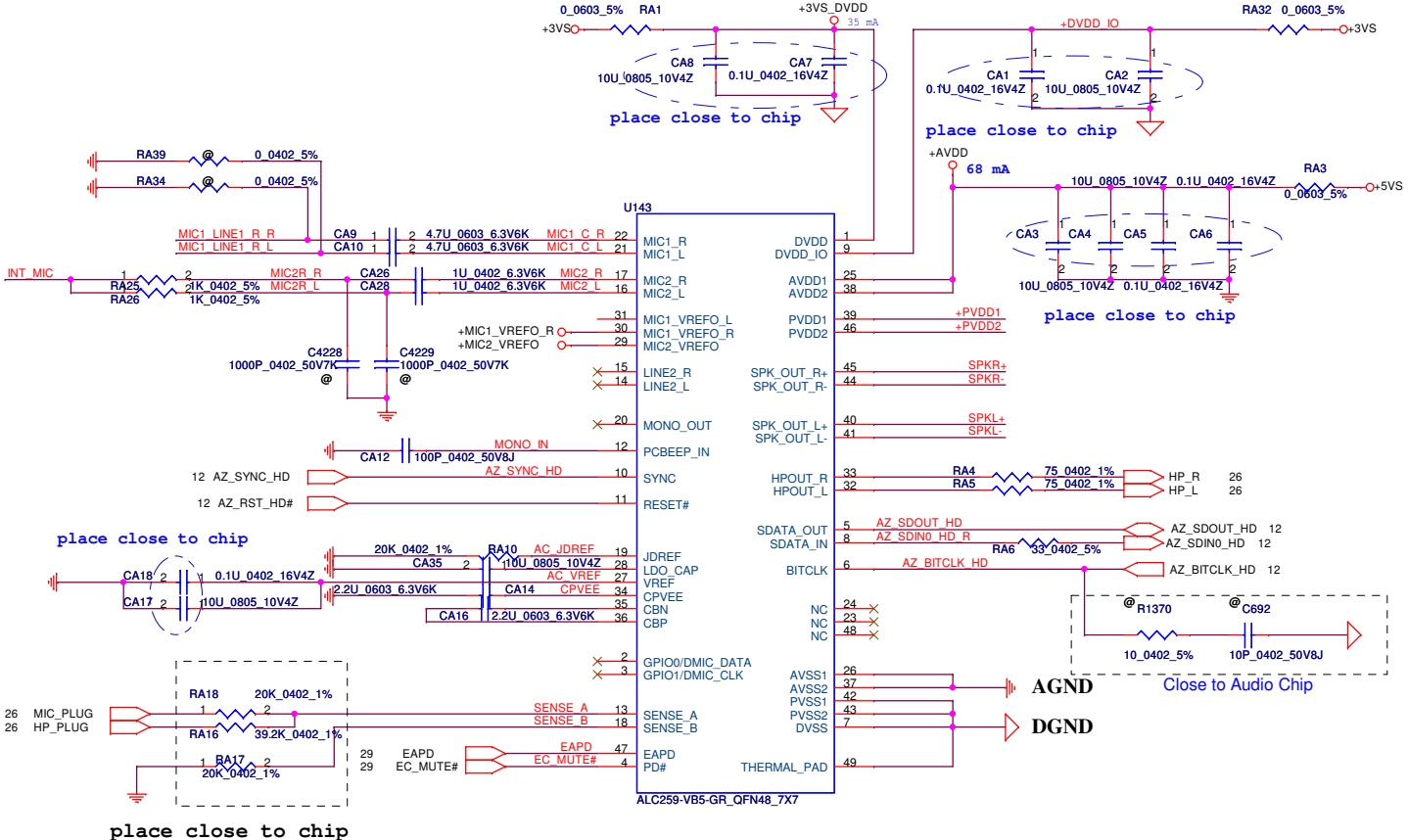
WLAN/BT combo



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								Size	Document Number	Rev
								Custom	QAL30 LA-8061P MB	0.1
								Date:	Friday, January 13, 2012	Sheet



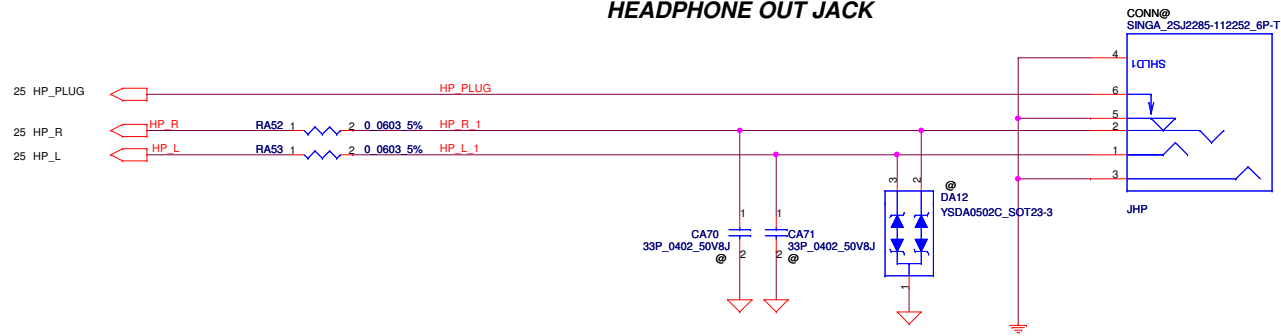
+3VALW TO +3V_LAN



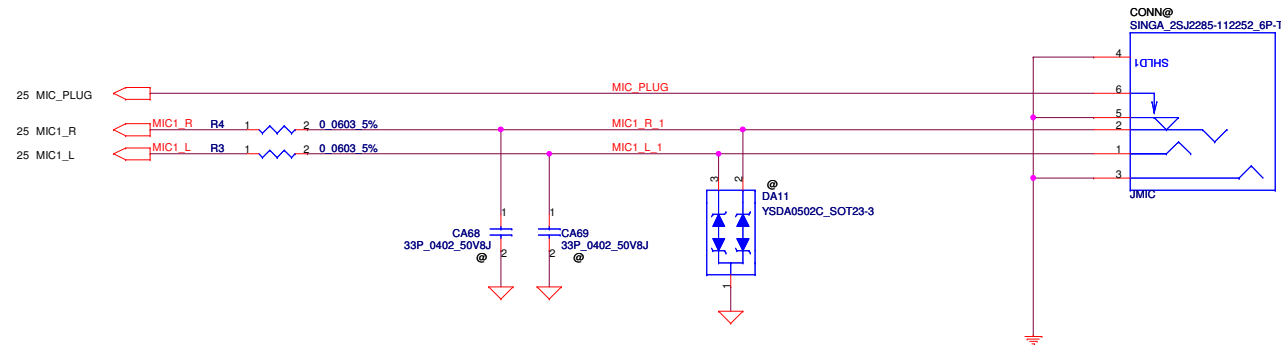
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
SENSE B	20K	PORT-F (PIN 16, 17)	Int. MIC

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				Date: Friday, January 13, 2012	
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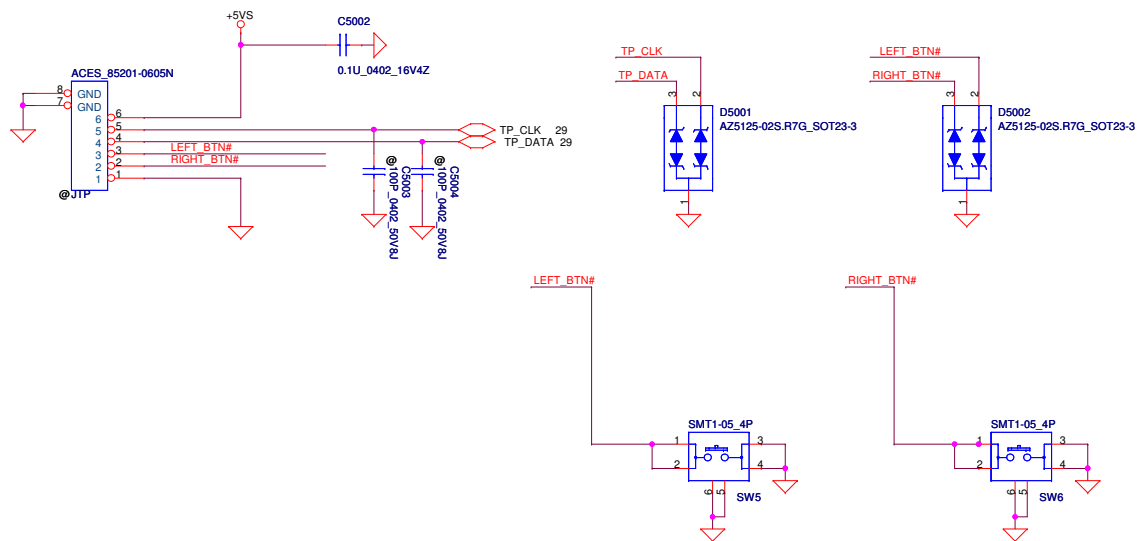
HEADPHONE OUT JACK



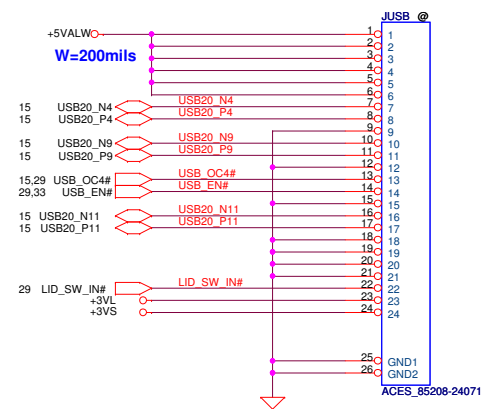
MICROPHONE IN JACK



Touch/B Connector

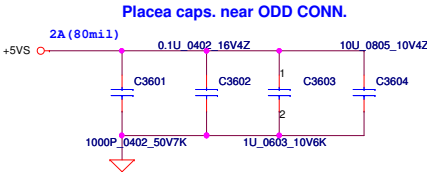
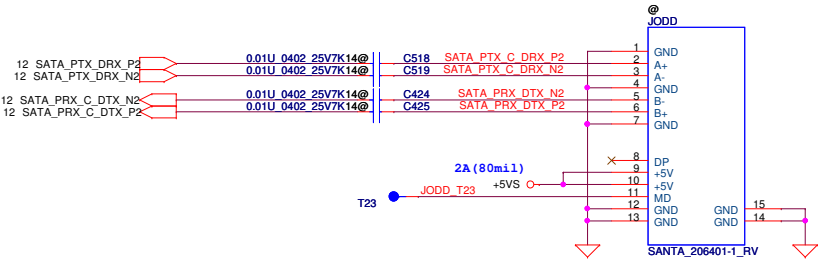


USB + LID SB

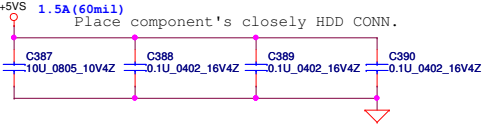
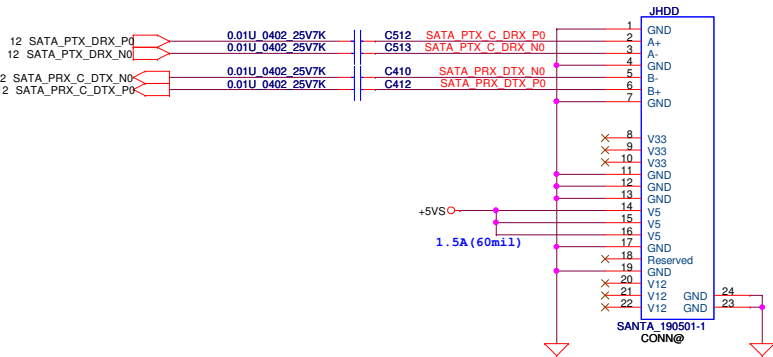


Title			
AUDIO CONN/TP/FUNB			
Size	Document Number	QAL30 LA-8061P MB	
		Rev 0.1	
Date:	Friday, January 13, 2012	Sheet	26 of 46

SATA ODD Conn.

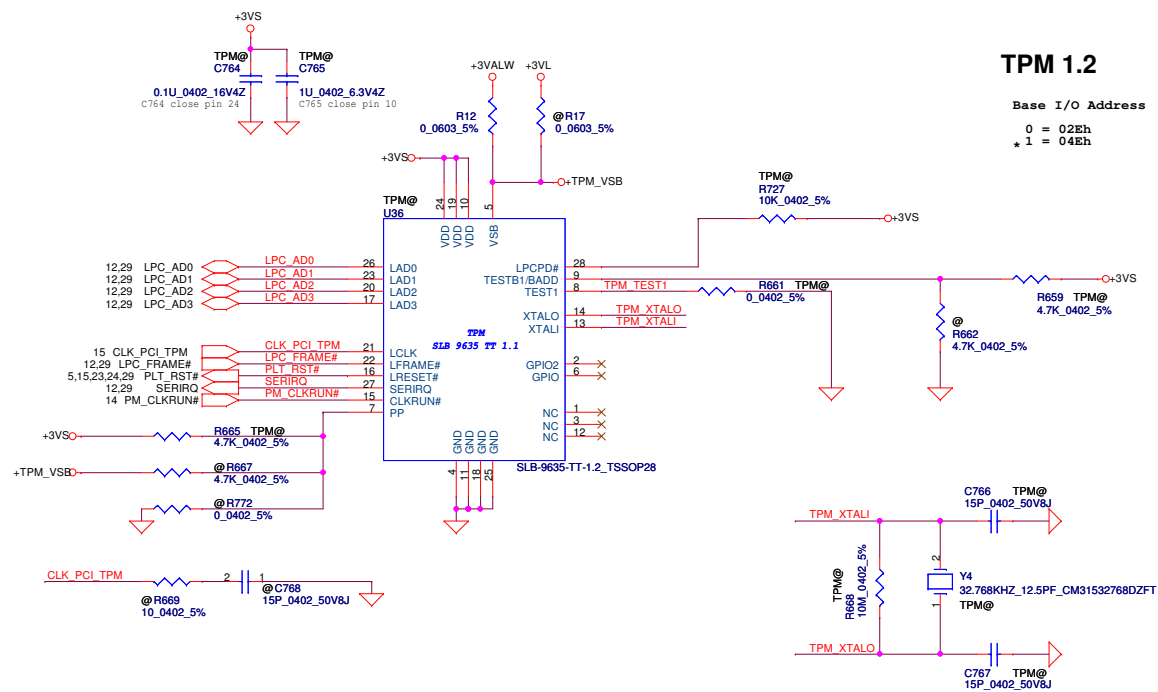


SATA HDD Conn.



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				SATA HDD / ODD			
				Size		Document Number	Rev
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				Date: Friday, January 13, 2012			Sheet 27 of 46

SPI ROM For Basic ME ROM size
(w/o Braidwood & system BIOS):
4MByte

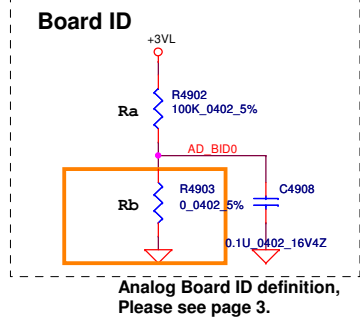


TPM 1.2

Base I/O Address

0 = 02Eh
* 1 = 04Eh

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BIOS Bus switch

R401

0.0402_5%

NOW8@

R402

0.0402_5%

NOW8@

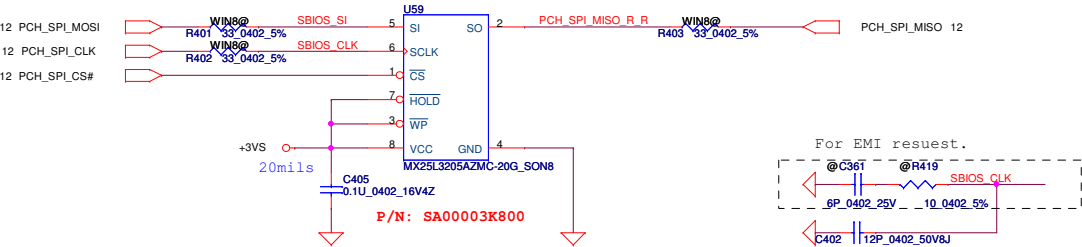
R403

0.0402_5%

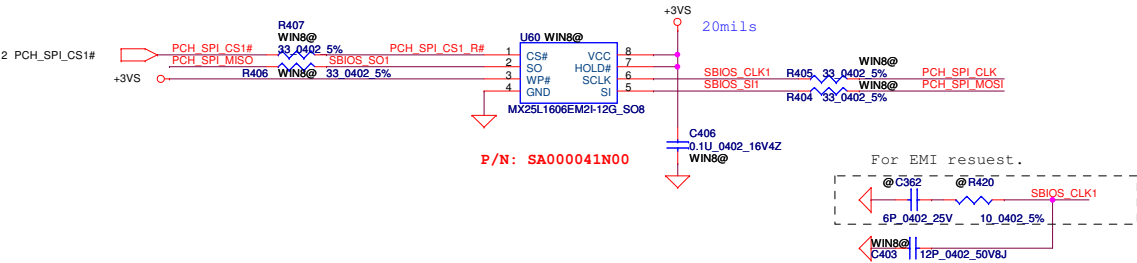
NOW8@

When use single ROM, use 0 ohm.

BIOS SPI Flash (4MByte*1)



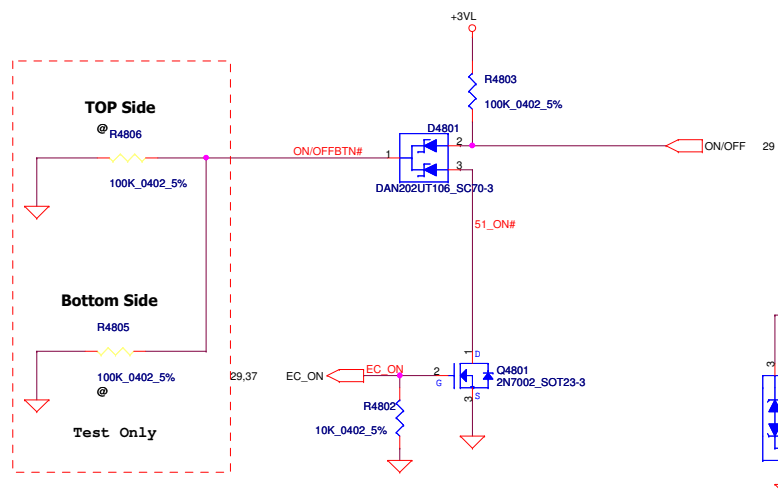
BIOS SPI Flash (2MByte*1) For Win8



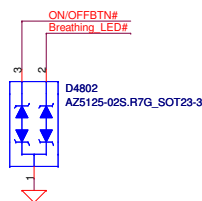
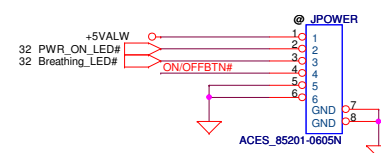
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Issued Date	2011/05/23	Deciphered Date	2012/12/31	SBIOS & EC ROM	
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Power Button

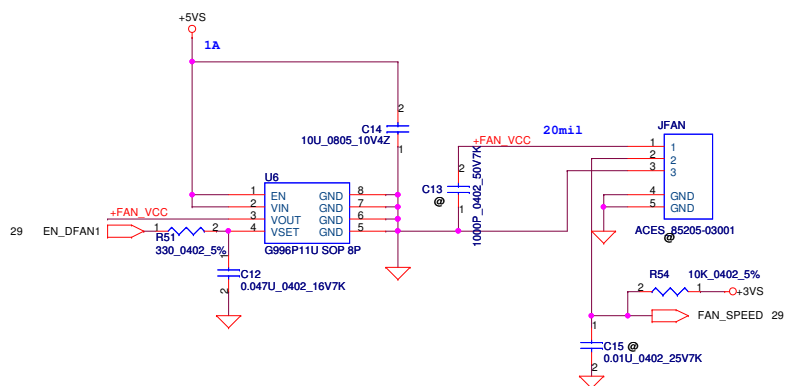
ON/OFF switch



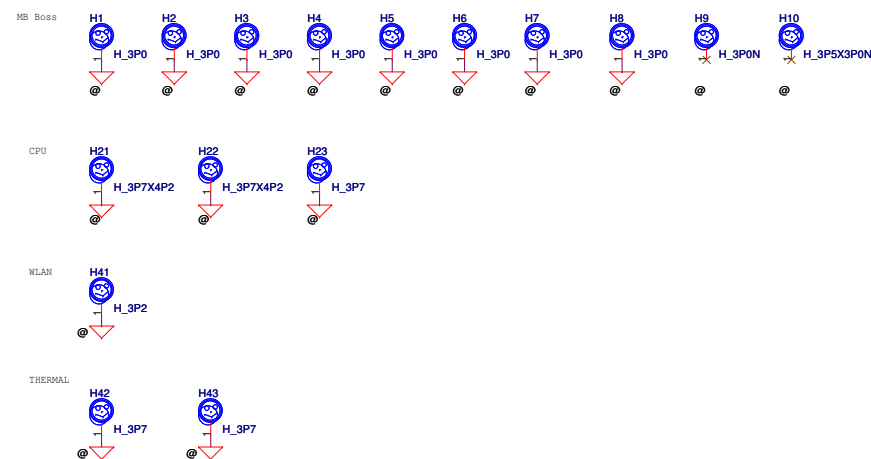
To POWER/B



Fan Control Circuit



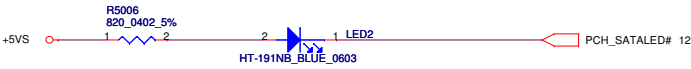
Screw Hole



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LED

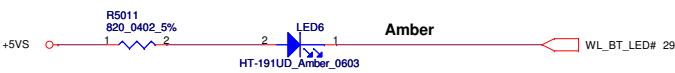
SATA



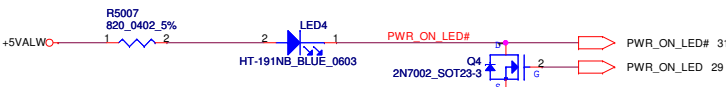
Battery



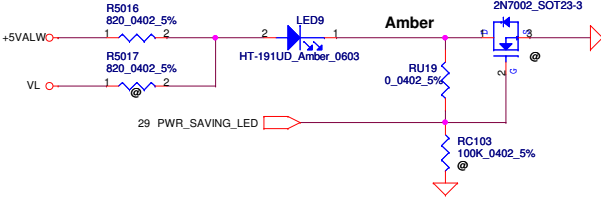
Wireless



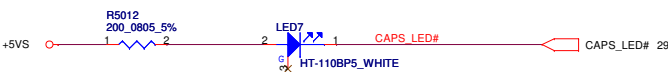
Power



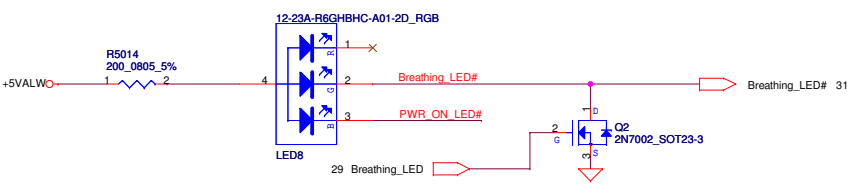
Power Saving



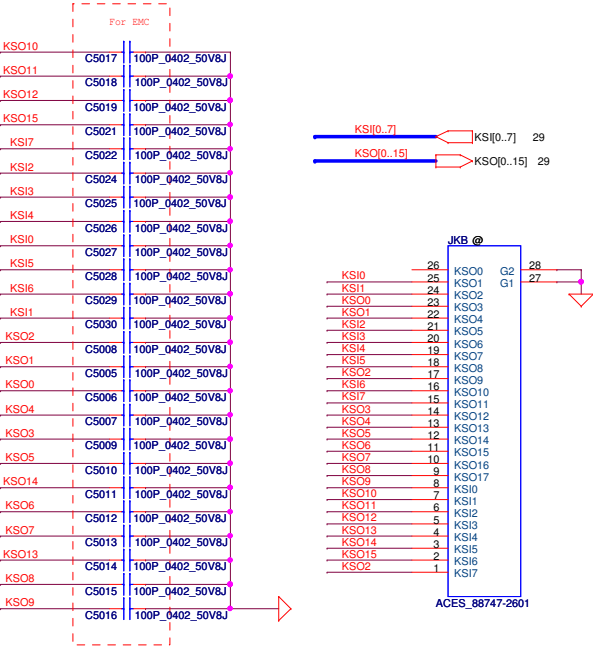
CAP Lock



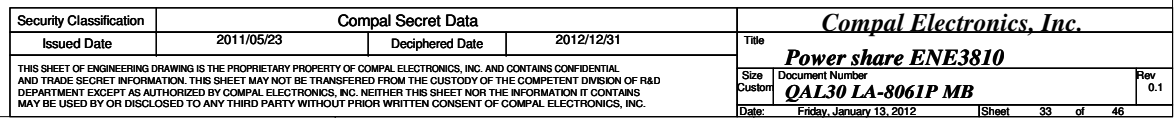
Breathing



INT_KBD Conn.



USB3.0 Port0
Port 0 : Left USB3.0



The schematic diagram illustrates the power supply circuitry for the TMS320C6701 evaluation module. It features two main input rails: +5VALW and +5VS. The +5VALW rail is connected to a network of capacitors (C5501, C5502) and a resistor (R5502), which then feeds into the gate of MOSFET Q5501 (AO478L 1N S08). The +5VS rail is similarly decoupled by capacitors C5503 and C5504 before connecting to the drain of Q5501. A second MOSFET, Q5502 (2N7002_SOT23-3), is configured as a source follower, driven by the +5VBIO rail through resistor R5502. Its source is connected to ground via capacitor C5505 and resistor RS522 (0_0402_5%). The output of Q5502 provides the +5VSD signal, which is further decoupled by capacitor C5506 and resistor RS501 (470_0603_5%) before reaching the +5VSD pin of the IC.

+3VALW to +3V_PCH

3V_PCH

JP5502

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The four circuit diagrams illustrate different MOSFET driver topologies:

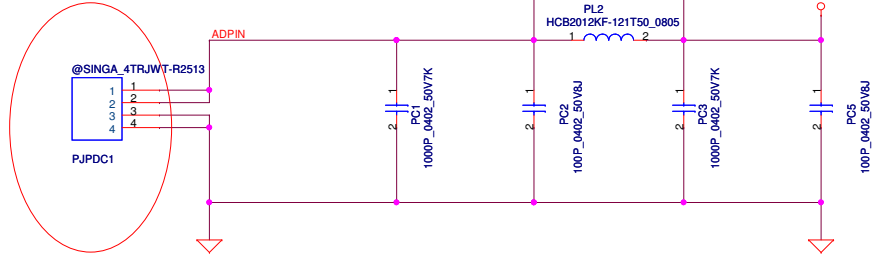
- Common Source:** The MOSFET (Q5514) has its source connected to ground. The gate is driven by a voltage divider (R5518) connected to +1.5V. The drain is connected to the load (SYSONB).
- Common Drain:** The MOSFET (Q5515) has its source connected to ground. The gate is driven by a voltage divider (R5508) connected to +1.5VS. The drain is connected to the load (SUSP).
- Common Gate:** The MOSFET (Q5518) has its source connected to ground. The gate is connected to a fixed bias voltage (+V1_05S_VCCP). The drain is driven by a voltage divider (R5509) connected to +V1_05S_VCCP.
- Common Drain with Source Resistor:** The MOSFET (Q5519) has its source connected to ground through a resistor (R5511). The gate is driven by a voltage divider connected to +3VS. The drain is connected to the load (SUSP).

The left diagram shows the sensor connected to a 1.8V supply through a 22k resistor (R5525). The sensor's VDD pin is connected to the 1.8V supply, and its GND pin is connected to ground. The sensor's SDA pin is connected to the 5.9 RUN_ON_CPU1.5V33R signal line, and its SCL pin is connected to the SUSP signal line.

The right diagram shows the sensor connected to a 0.75V supply through a 22k resistor (R5520). The sensor's VDD pin is connected to the 0.75V supply, and its GND pin is connected to ground. The sensor's SDA pin is connected to the 5.9 RUN_ON_CPU1.5V33R signal line, and its SCL pin is connected to the SUSP signal line.

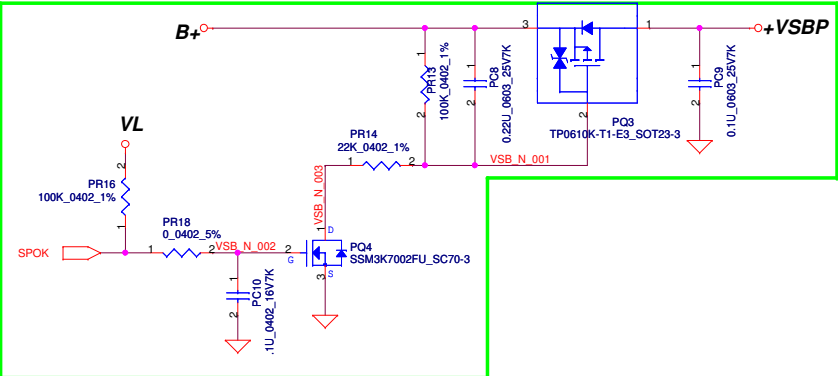
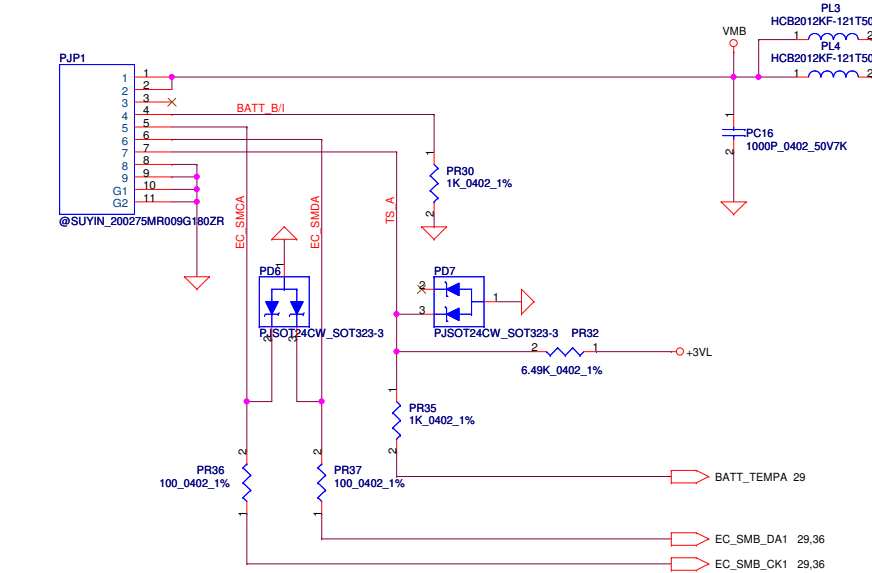
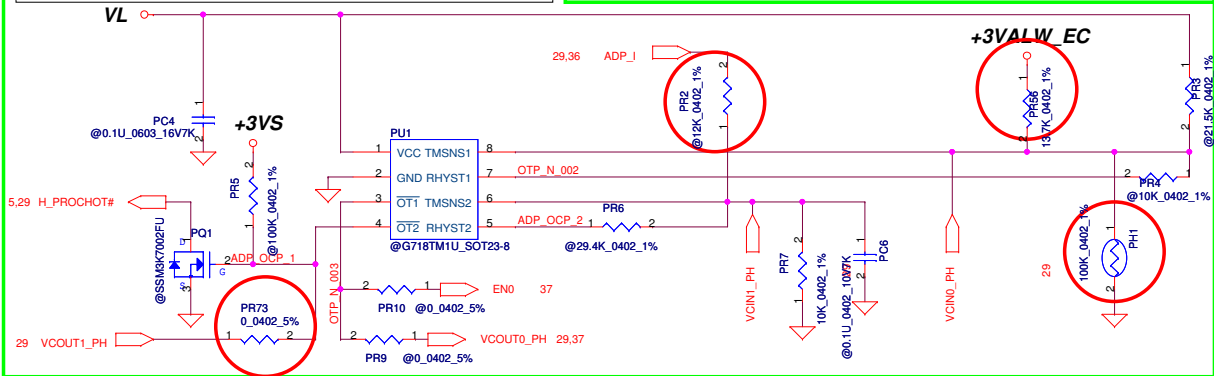
Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i> DC/DC Interface		
Issued Date	2011/05/23	Deciphered Date	2012/12/31	Title		
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DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME

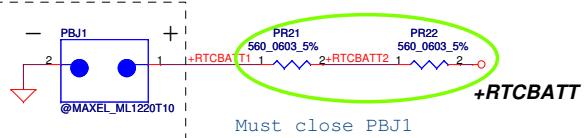


PH1 under CPU bottom side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU1 circuit, but keep PR56
PH1, PR2, PQ1, PR7,PQ15,PR73,PR56

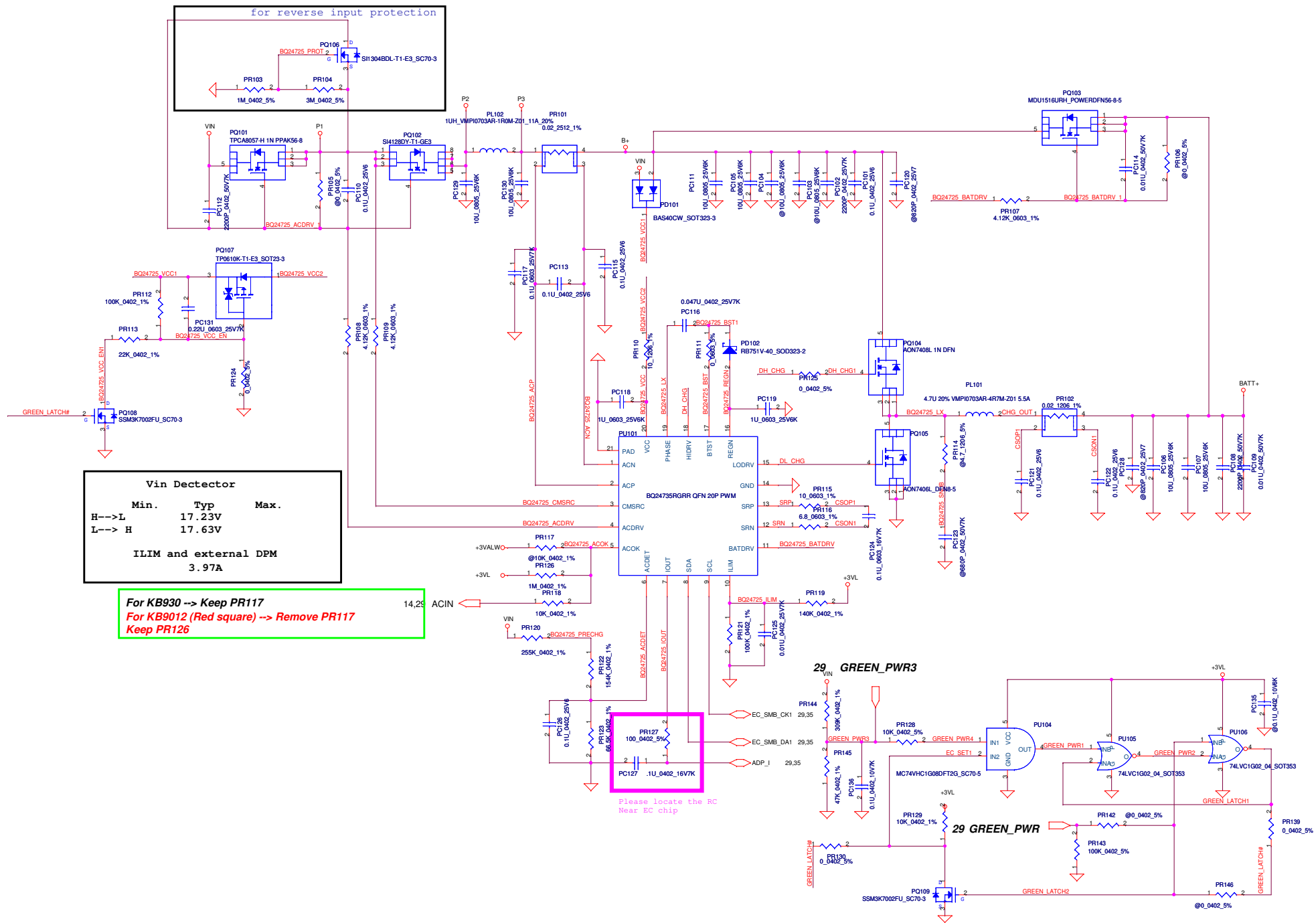


RTC Battery

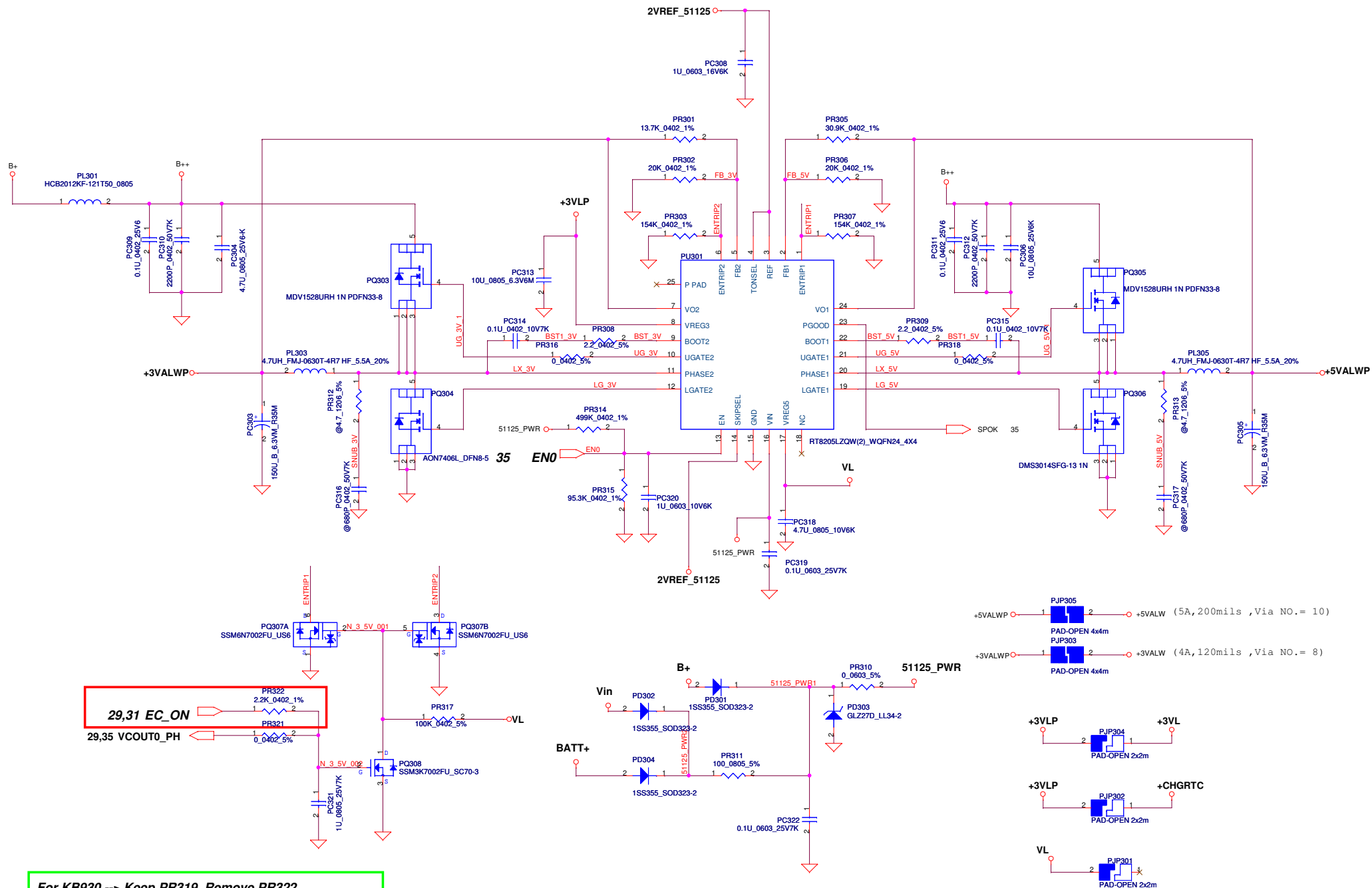


SP093MX0000
Change RTC For Cost Down

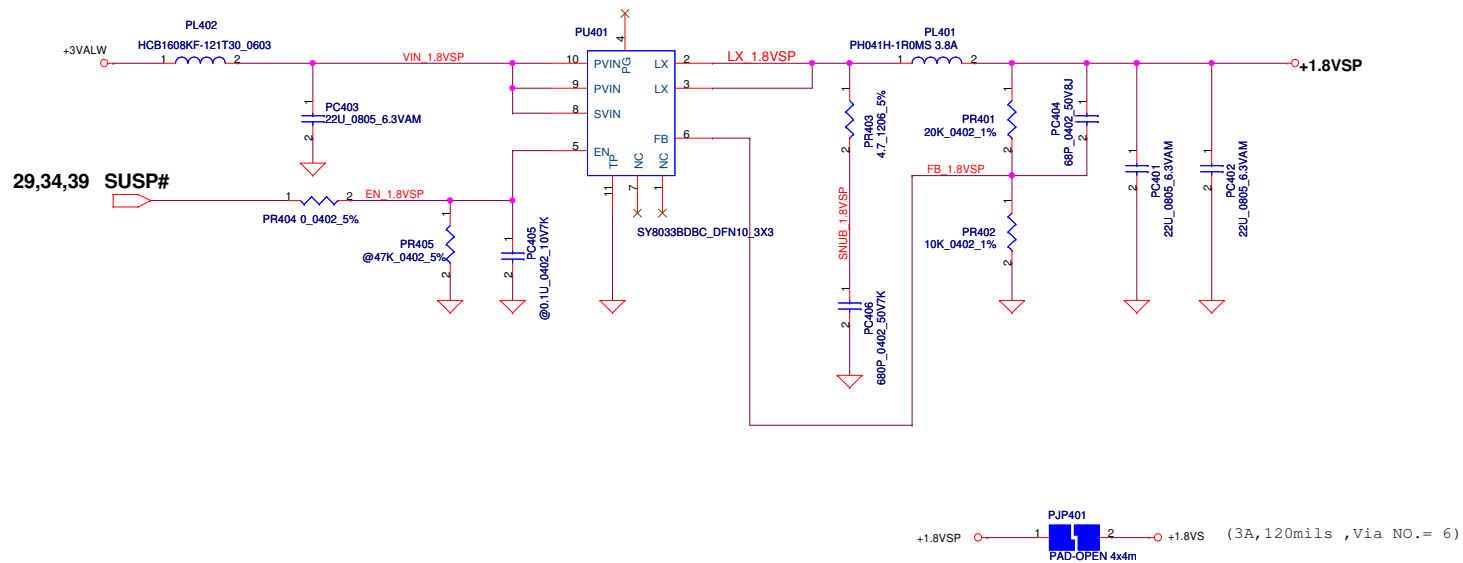
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Issued Date		2011/05/23		PWR-DCIN / BATT CONN / OTP	
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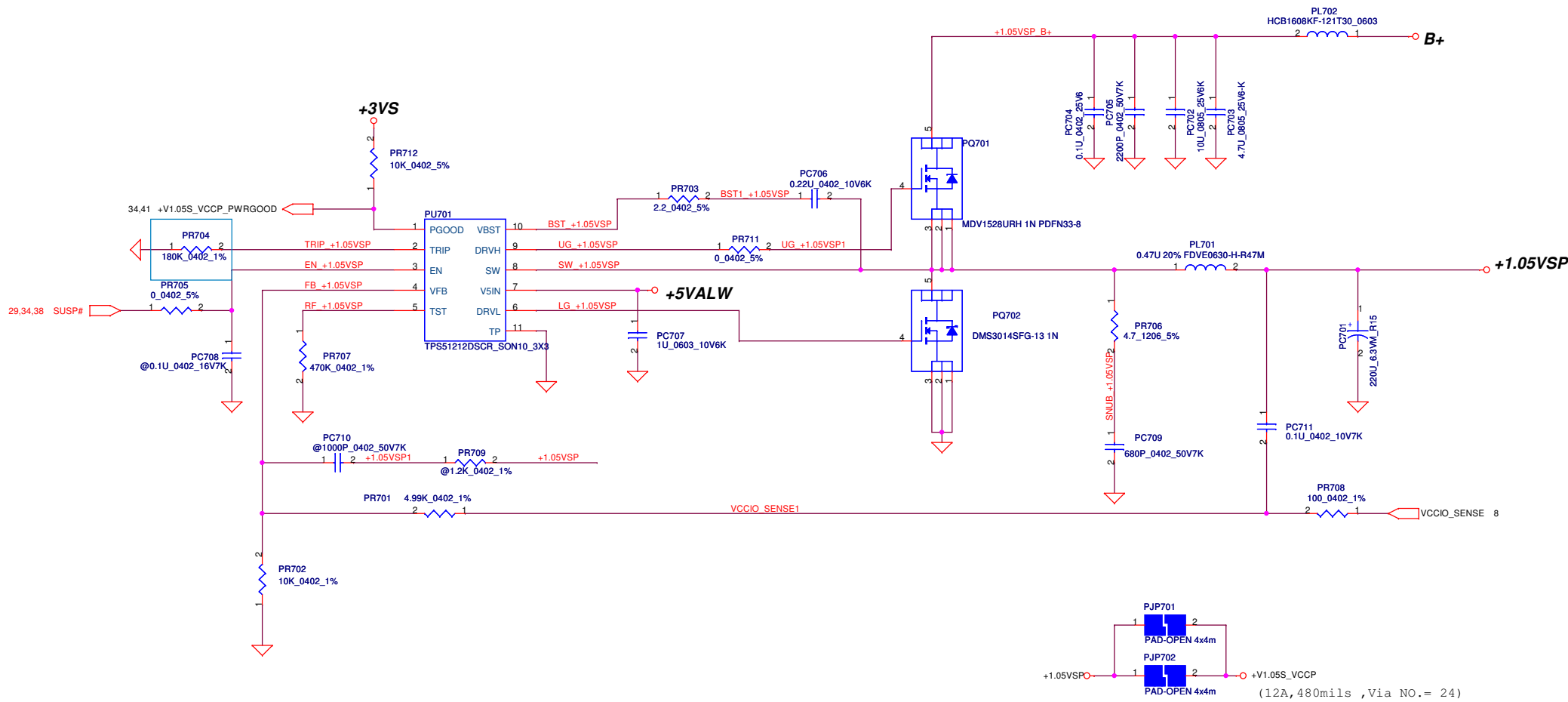
Security Classification		Compal Secret Data		Title	
Issued Date	2011/05/23	Deciphered Date	2012/12/31	PWR-CHARGER	
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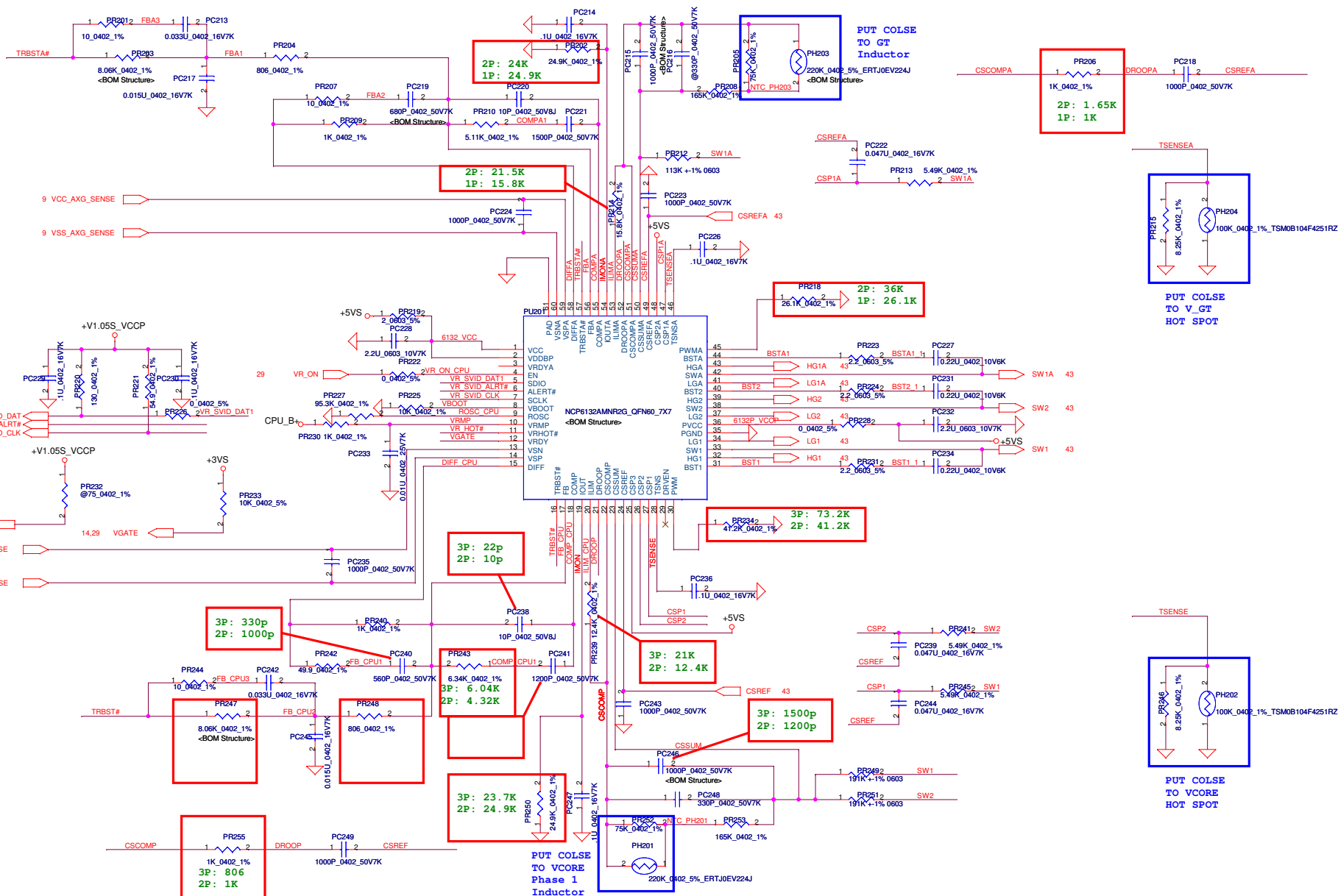
Security Classification		Compal Secret Data		Title	
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				Rev	0.1



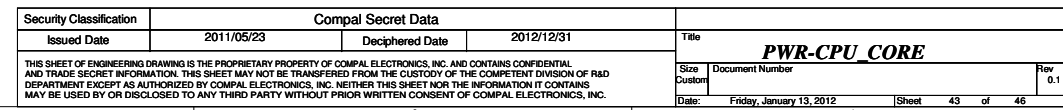
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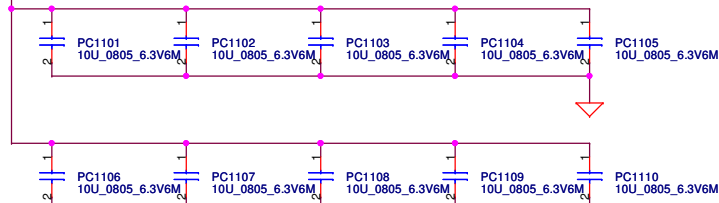
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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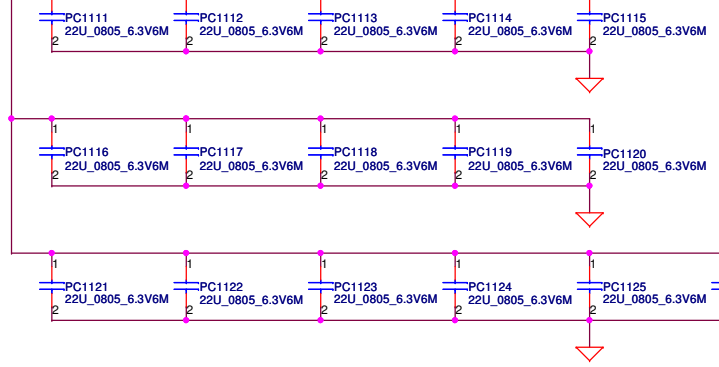
Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i> PWR-CPU CORE		
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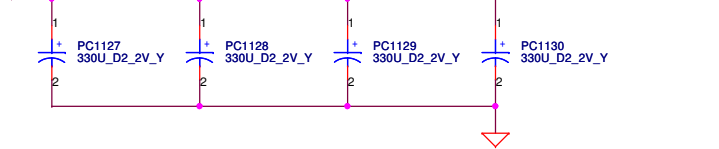
+VCC_CORE



+VCC_CORE



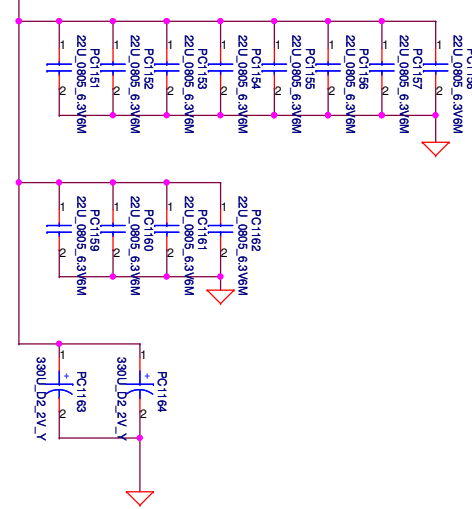
+VCC_CORE



+VCC_CORE

+GFX_CORE

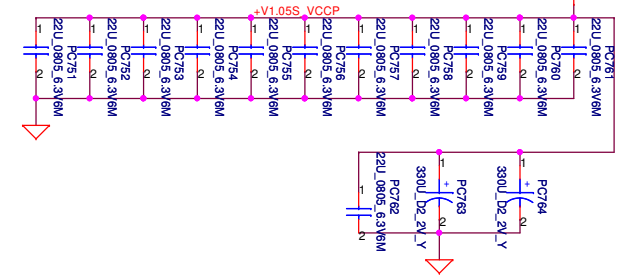
+GFX_CORE



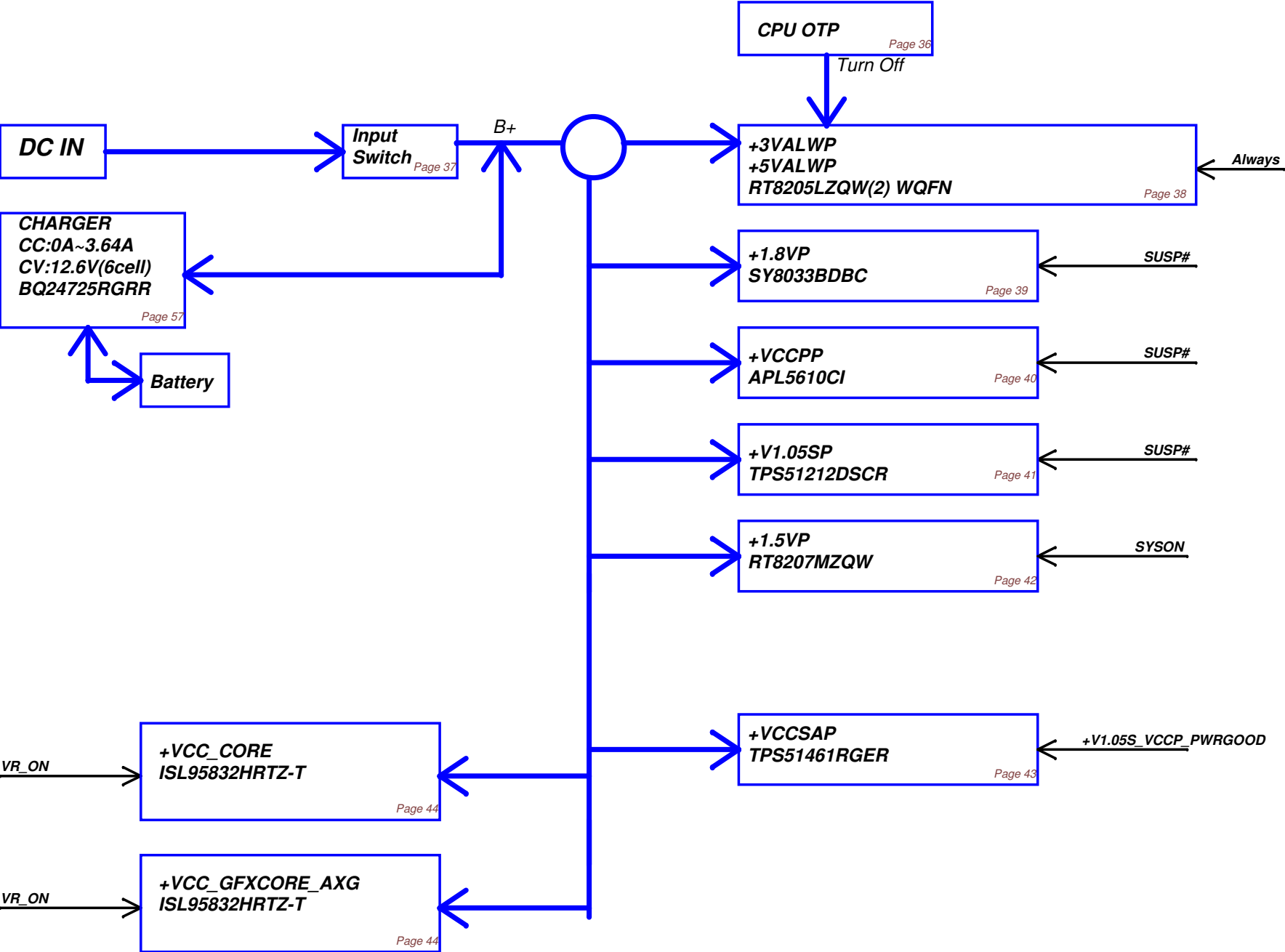
Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+V1.05S_VCCP



Power block



Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1					PR504 change from 15K to 15.4K		
2					charger IC change form bq24725A to bq24735		
3					PQ104,PQ303,PQ305,PQ701 charge form SIS412DN to MDW1528URH		
4					PQ306 charge from AON7702L to FDMC7692S		