

Compal Confidential

Schematics Document

AMD Turion/Sempron + Nvidia MCP67-MV

2007-01-12

Rev: 0.1

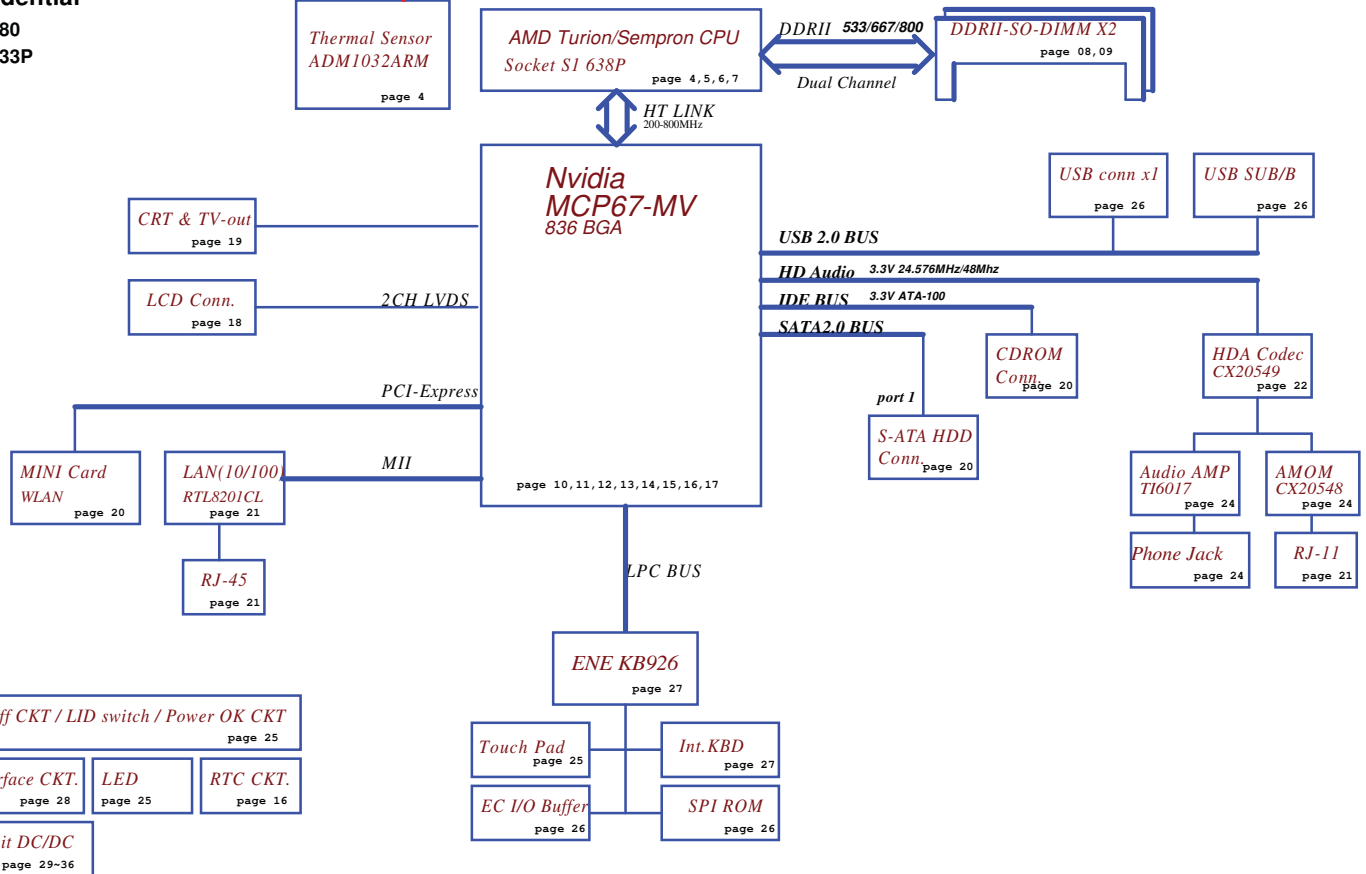


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Compal confidential

Project Code: IBL80

File Name : LA-3733P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.2VALW	1.2V always on power rail	ON	ON	ON*
+1.2VS	1.2V switched power rail	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra/Rc/Rd	100K +/- 5%				
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	
0	0	0 V	0 V	0 V	
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

External PCI Devices

Device	IDSEL#	REQ#GNT#	Interrupts
--------	--------	----------	------------

BTO Option Table

BTO Item	BOM Structure
DIP CAP & RTC	45@

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b

EC SM Bus2 address

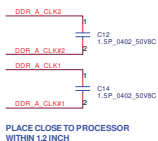
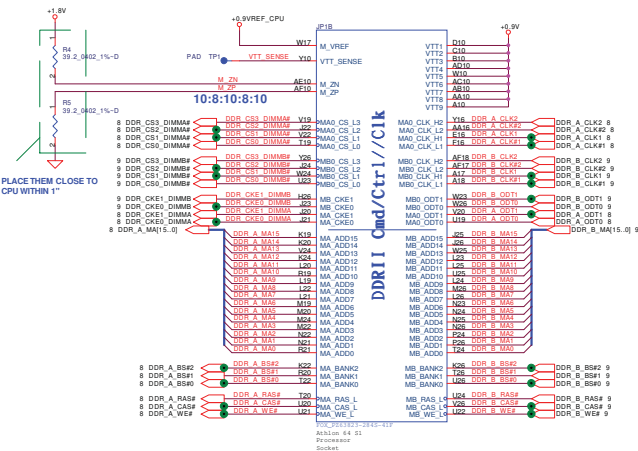
MCP67 SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 001Xb
MINI CARD	

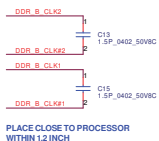
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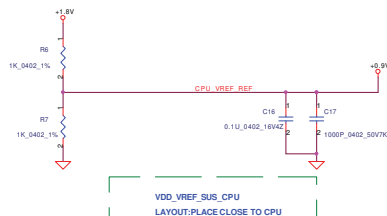
VDD VTT SUS CPU IS CONNECTED TO THE VDD VTT SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO REGULATOR AND TO THE GROUND PLANE.



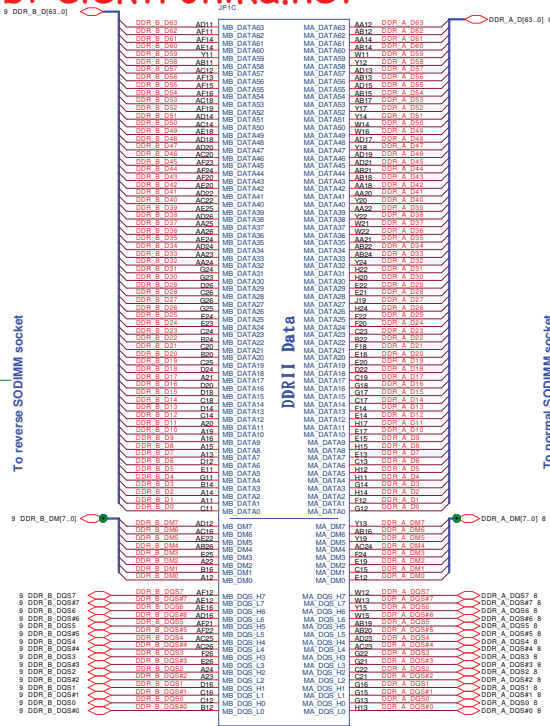
PLACE CLOSE TO PROCESSOR
WITHIN 1.2 INCH



PLACE CLOSE TO PROCESSOR
WITHIN 1.2 INCH

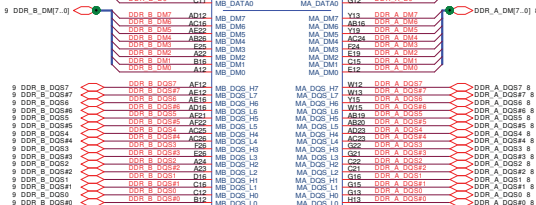


VDD_VREF_SUS_CPU
LAYOUT: PLACE CLOSE TO CPU



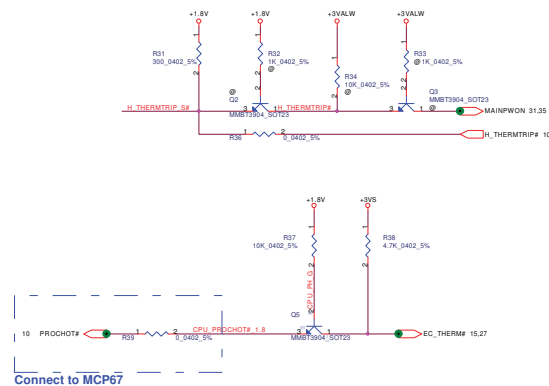
To reverse SODIMM socket

To normal SODIMM socket

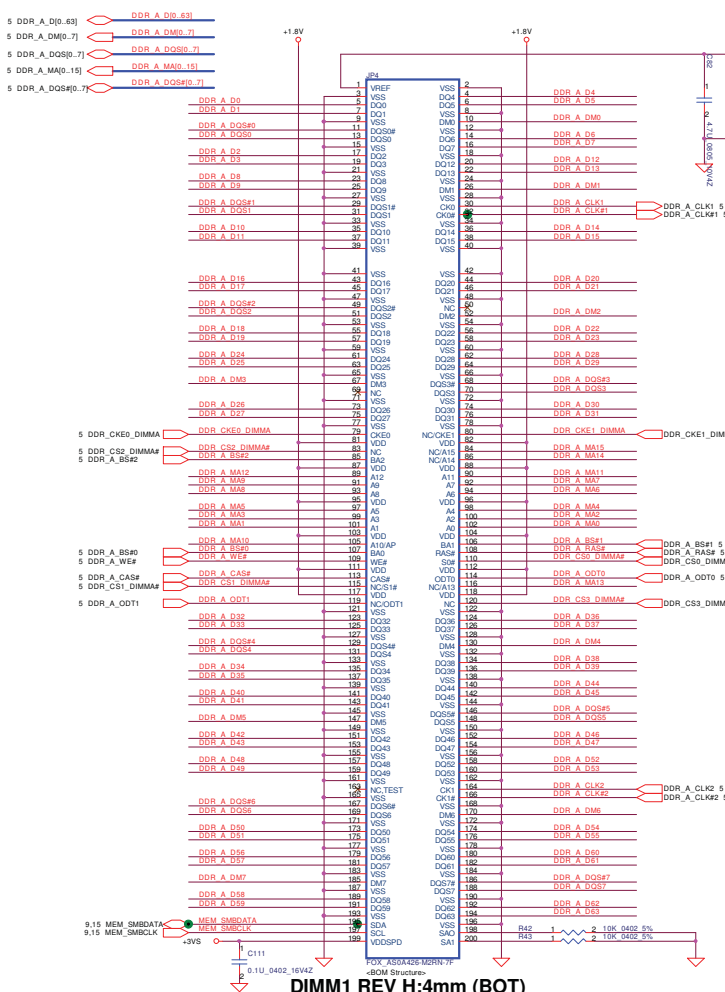


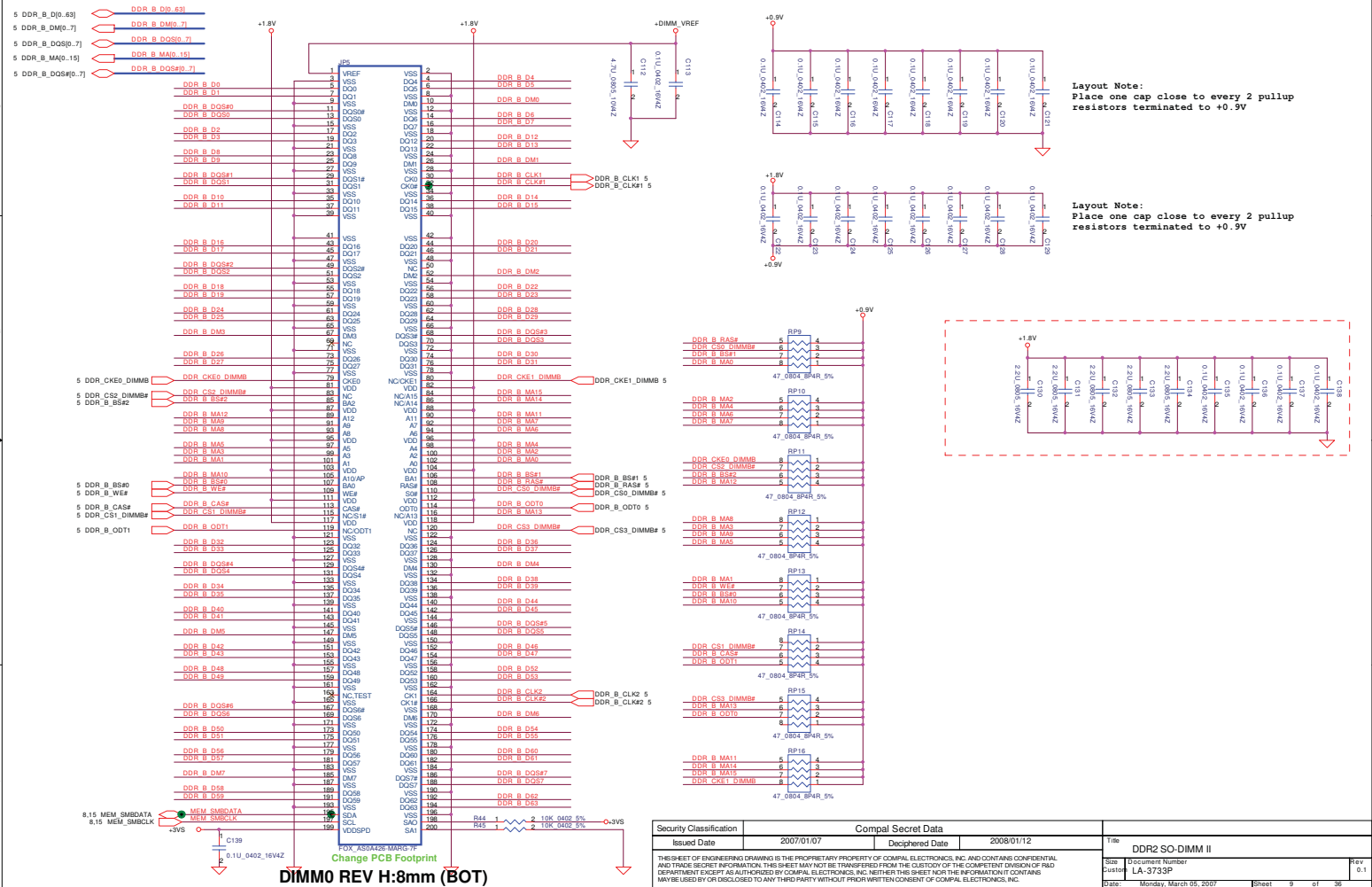
Athlon 64 S1
Processor Socket

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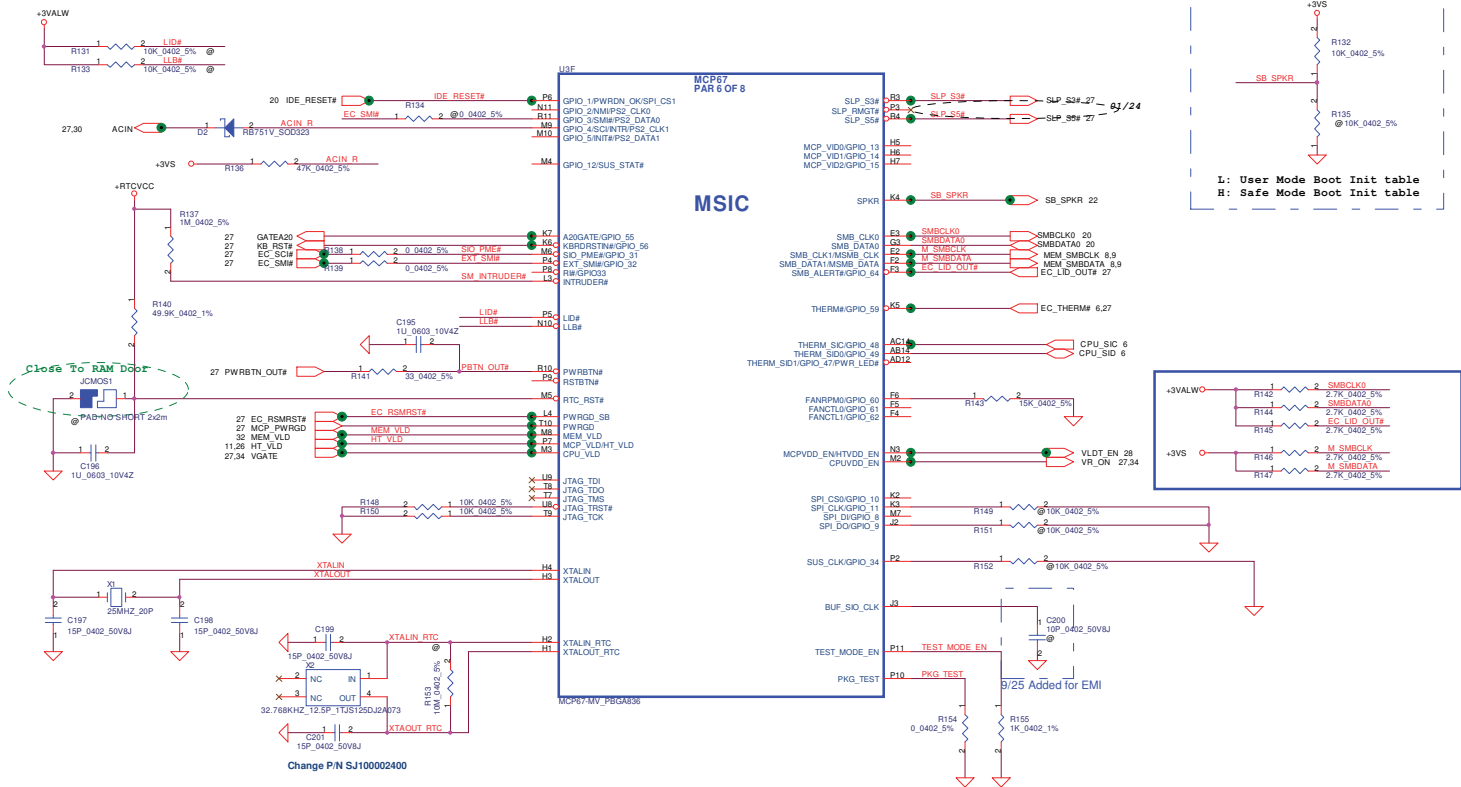


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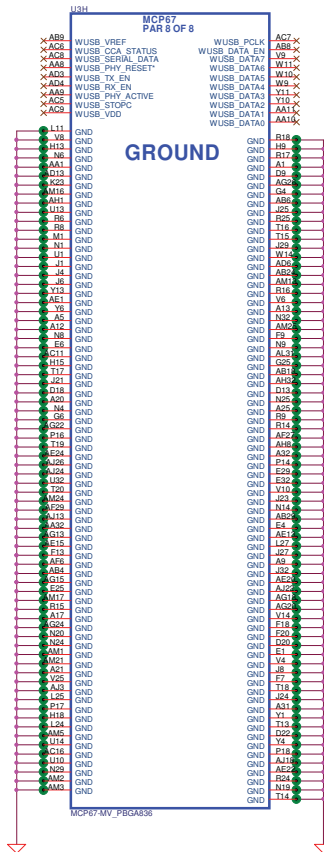






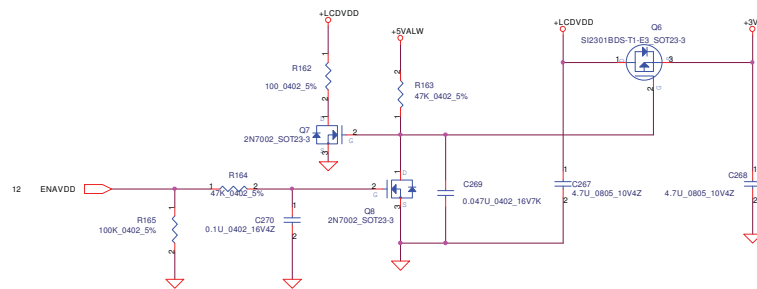
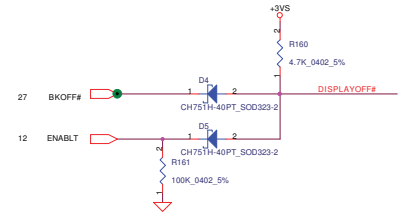
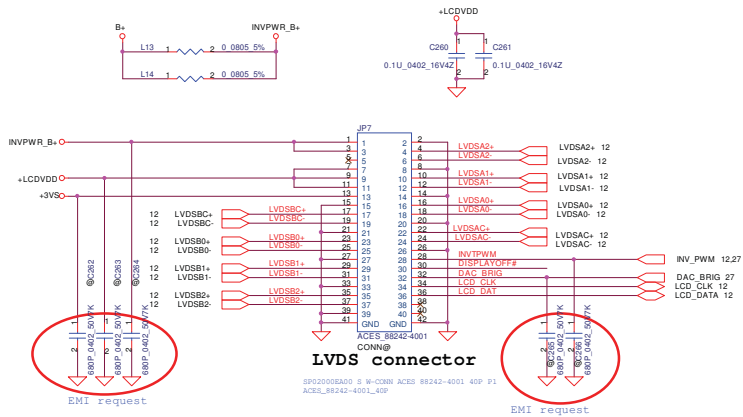
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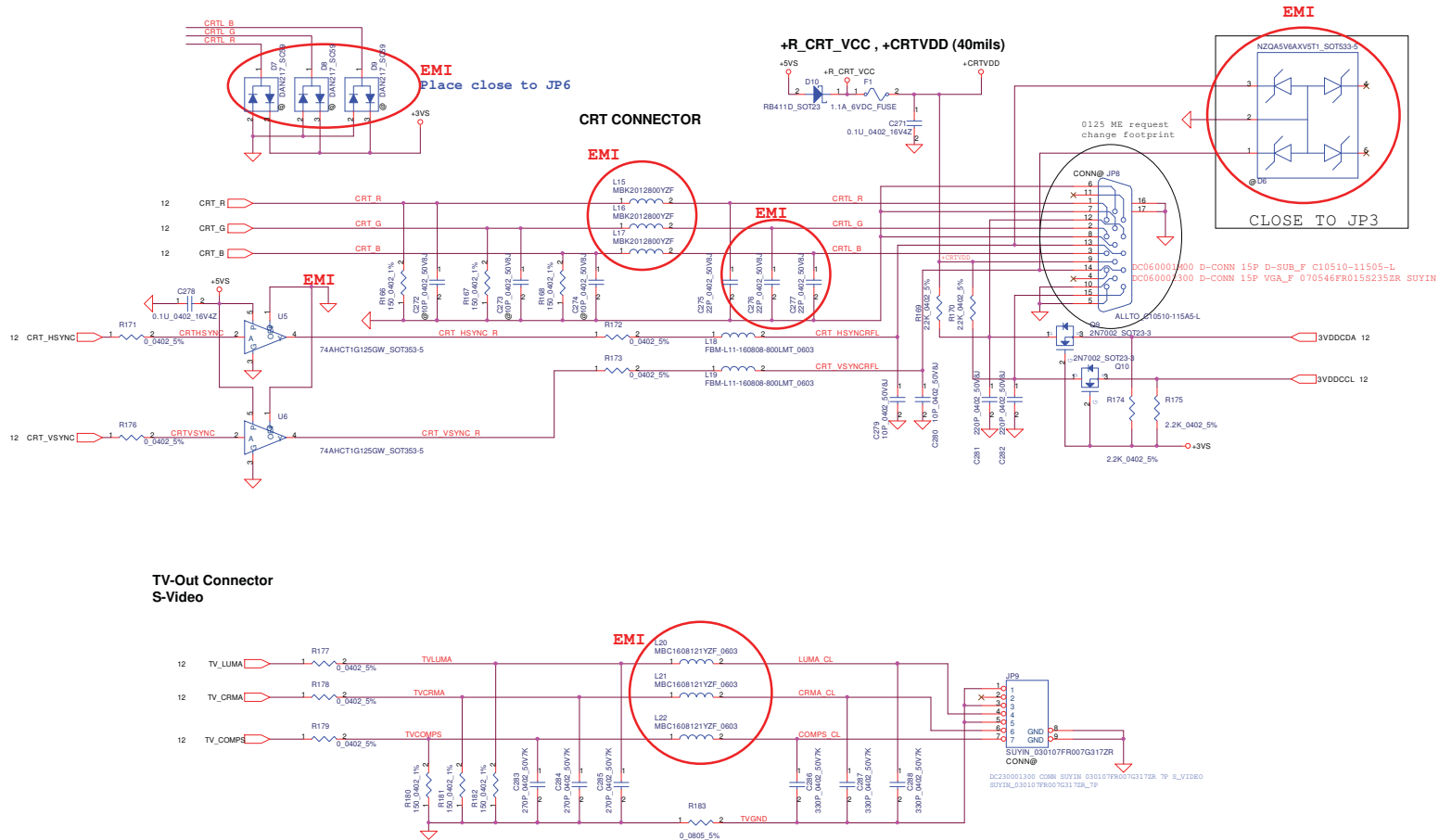


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LVDS CONN

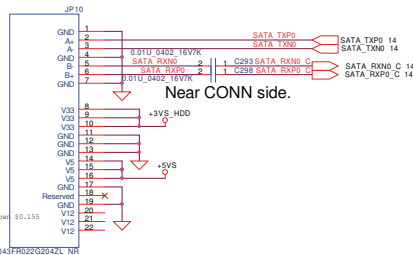
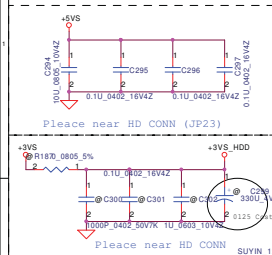


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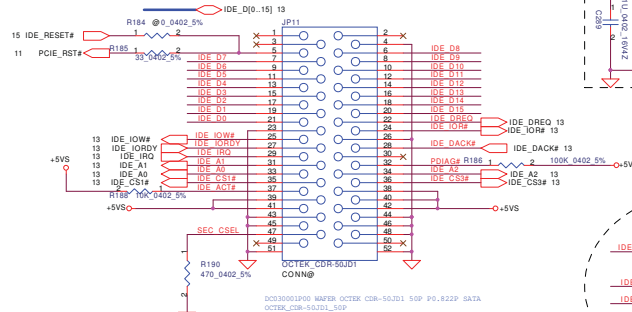


HDD Connector

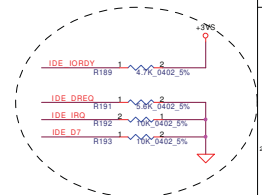
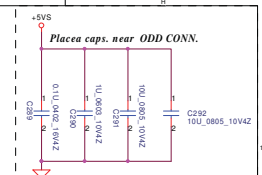
CD-ROM Connector



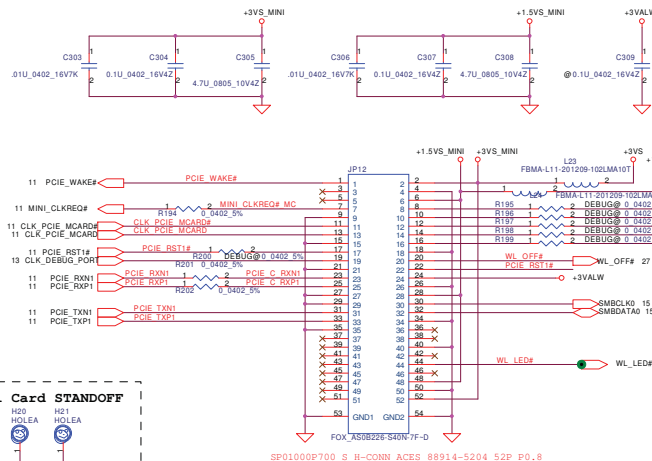
DC310003P00 ROSSING SUYIN 127043FR022G2045L 22P SATA
SUYIN_127043FR022G2045L_22P_NH



DC330003P00 WAFER OCTER CDR-50J01 50P P0.822P SATA
OCTER_CDR-50J01_50P

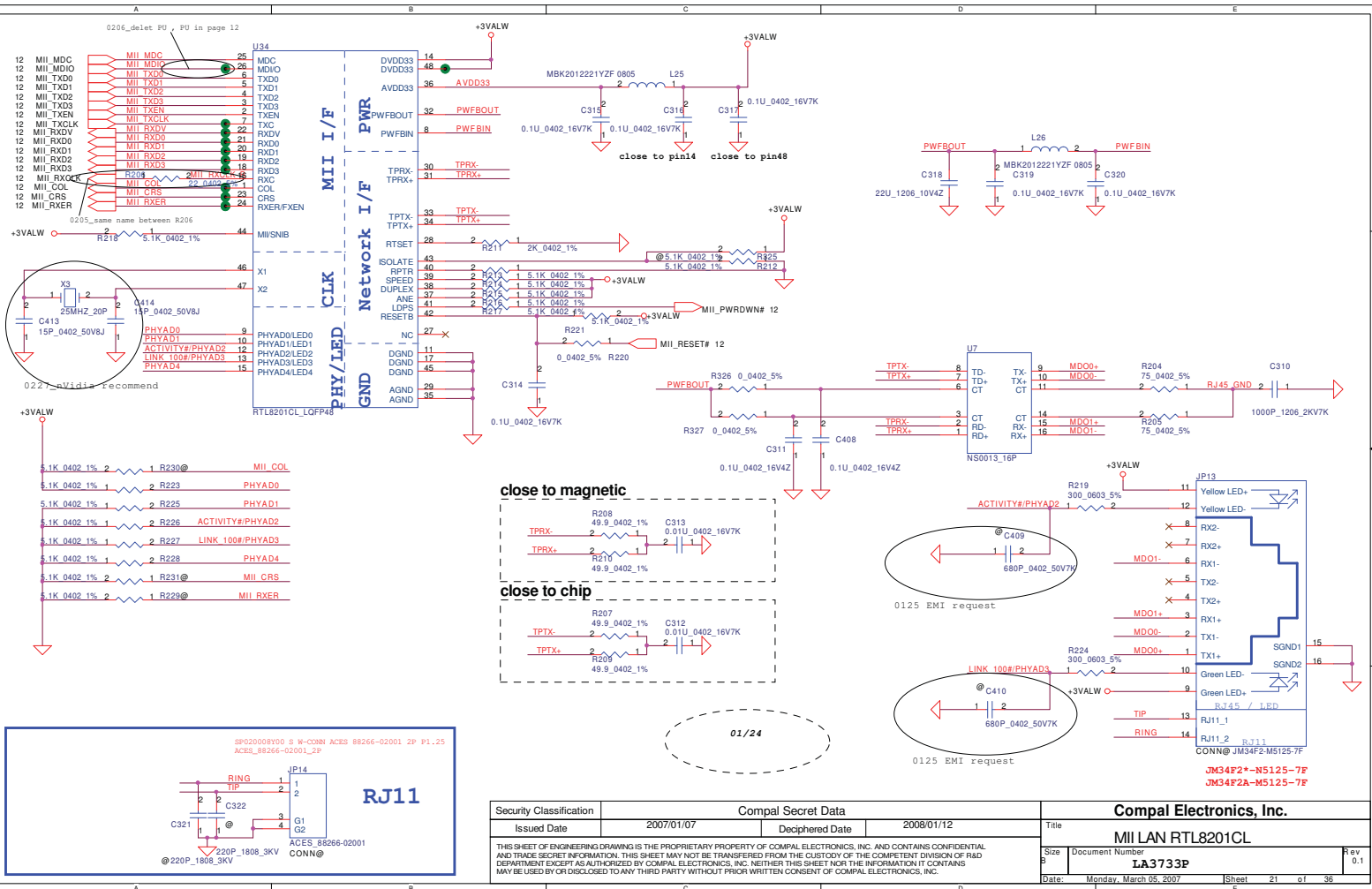


Mini-Express Card---WLAN



SP010007P00 S H-CONN ACES 88914-5204 52P P0.8

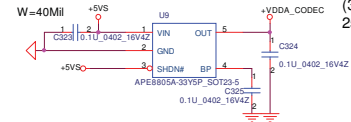
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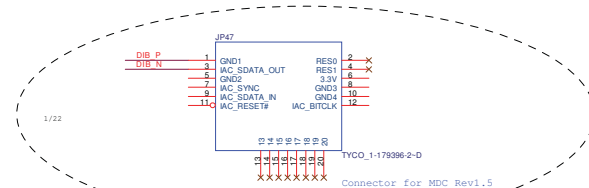
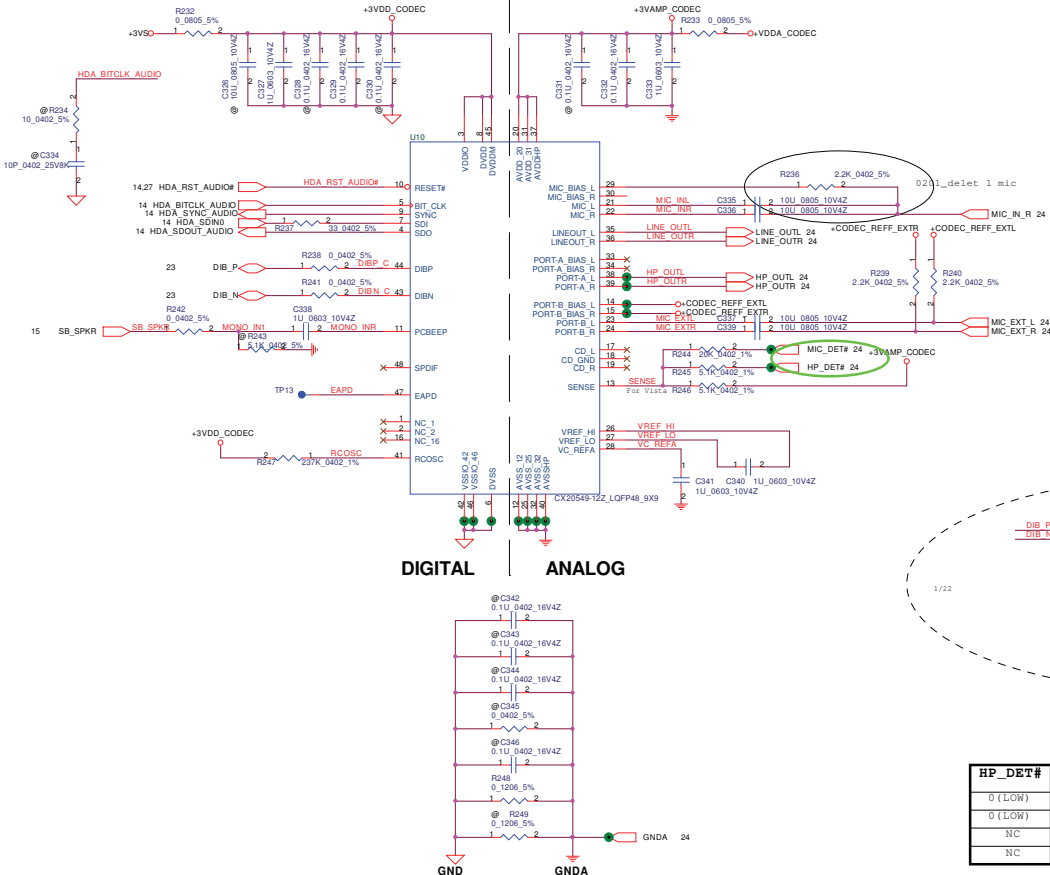
CODEC POWER

(3.33V)
250mA

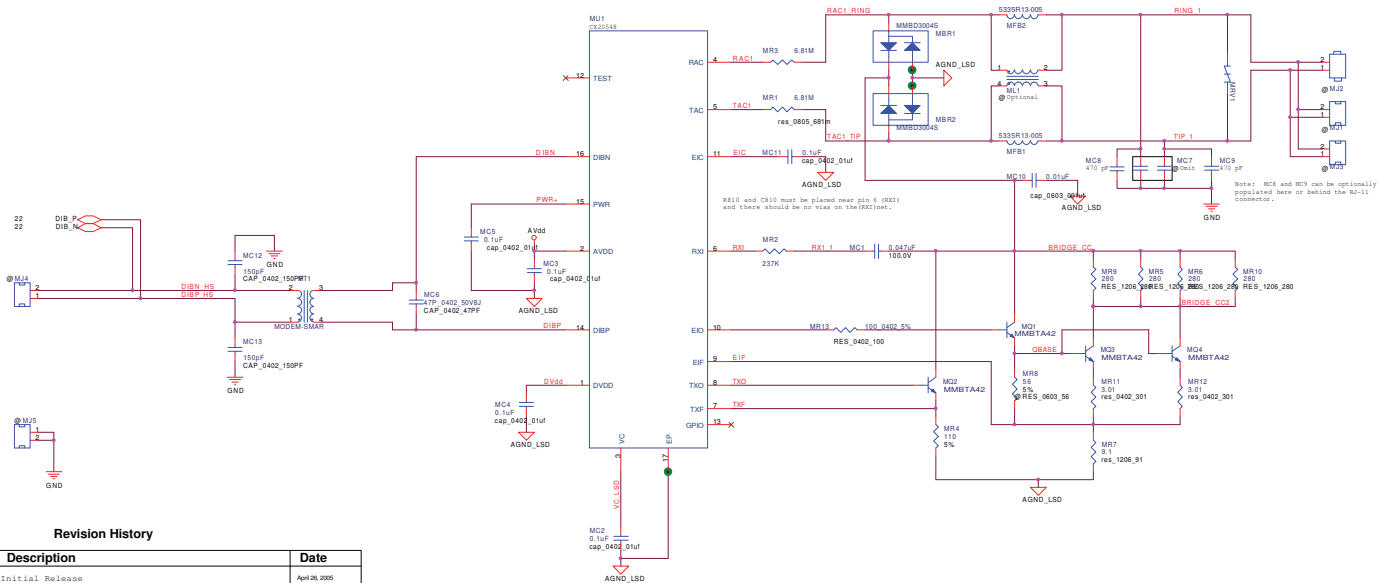


In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

For Layout:
Place decoupling caps near the power pins of SmartAMC device.



HP_DET#	MIC_DET	LINEOUT	PORT-A <Earphone OUT>	MIC	EQ
0 (LOW)	0 (LOW)	OFF	ON	ON	Disable
0 (LOW)	NC	OFF	ON	OFF	Disable
NC	0 (LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable



Revision History

REV	Description	Date
0	Initial Release	April 26, 2005
1	No changes to schematic. PCB updated to -003. Updated footprints and corrected via spacing errors.	August 18, 2005
2	Changed MC8 and MC9 pads. No schematic changes. PCB updated to -005.	November 3, 2005
3	Added MR11 and MR12. PCB updated to -007.	November 16, 2005
4	Added MR13. PCB updated to -009.	January 3, 2006
4.01	AVL update only.	April 20, 2006

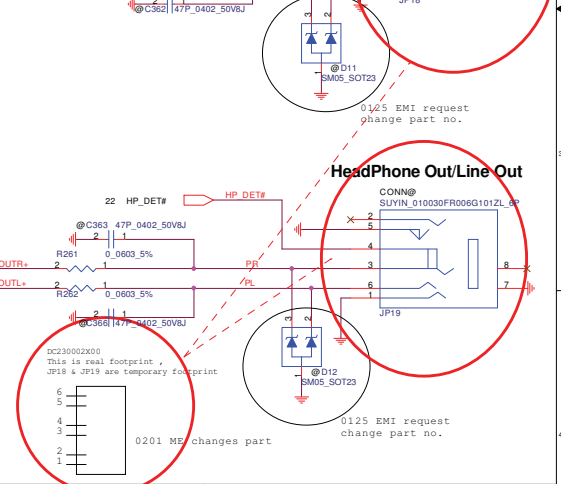
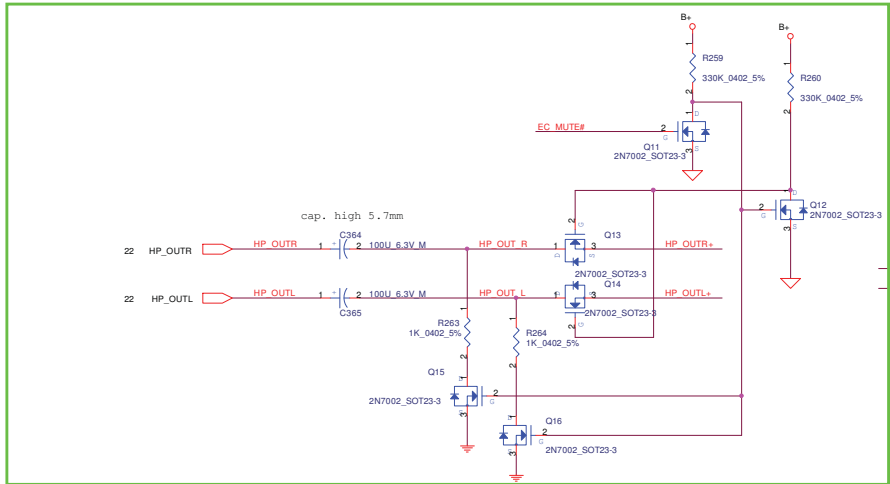
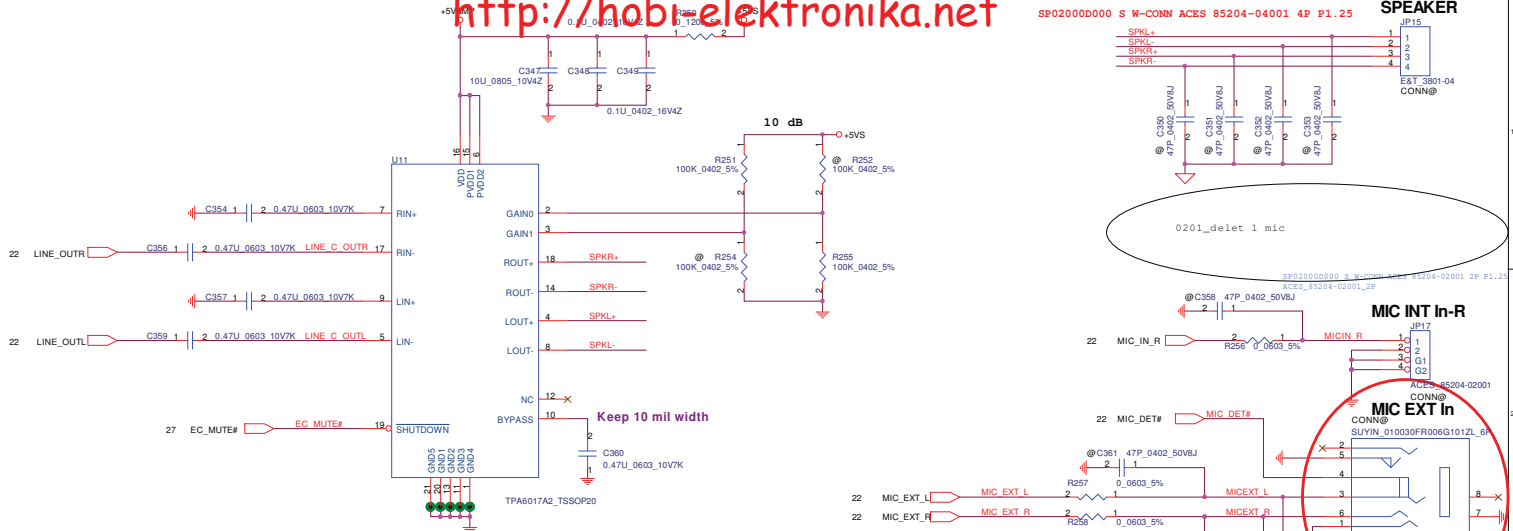
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AMOM-CX20548

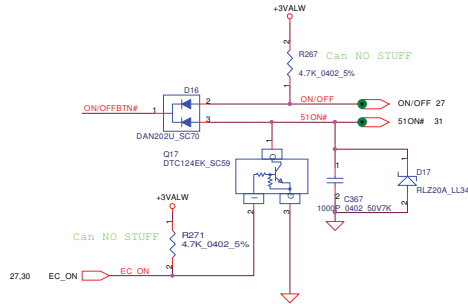
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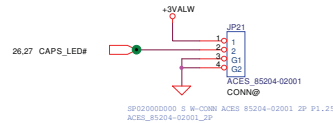


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Power ON/OFF



M/B to SB (Caps Lock LED)

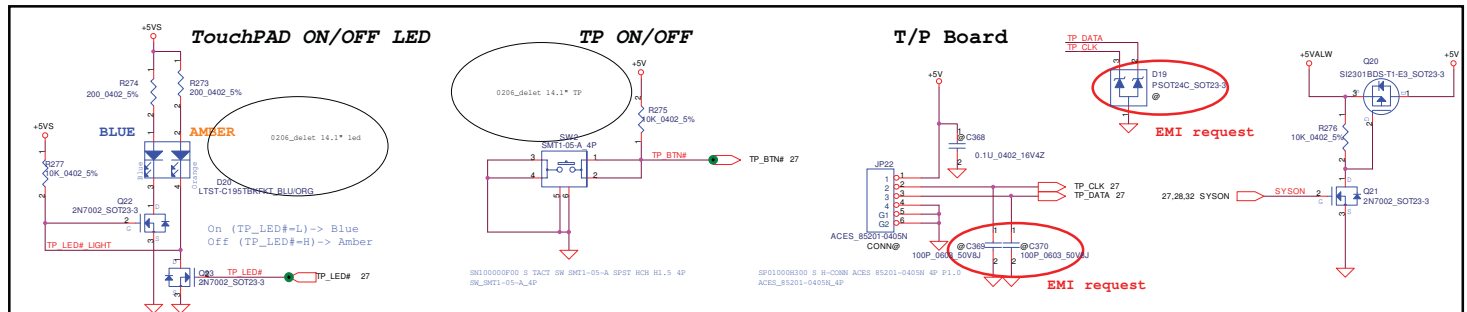


D21, D25, D23 Footprint can not match part number.

TouchPAD ON/OFF LED

TP ON/OFF

T/P Board



POWER LED (Left 1)

BLUE



Battery Charge LED (Left 2)

BLUE

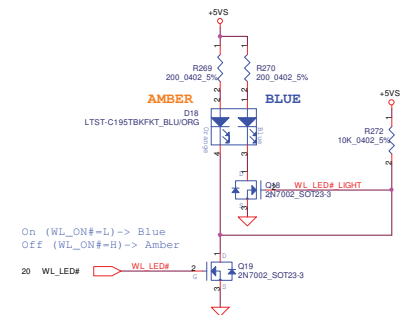


HDD LED (Left 3)

BLUE



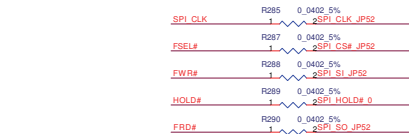
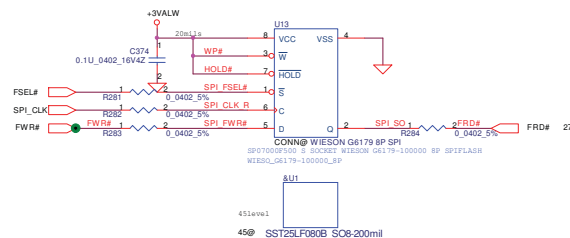
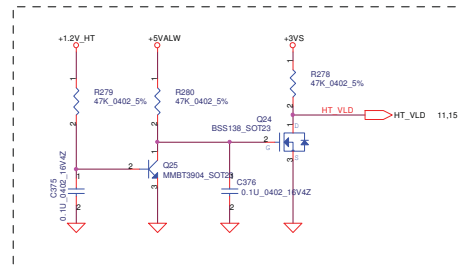
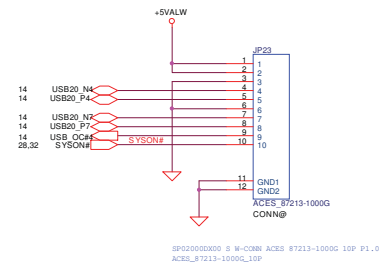
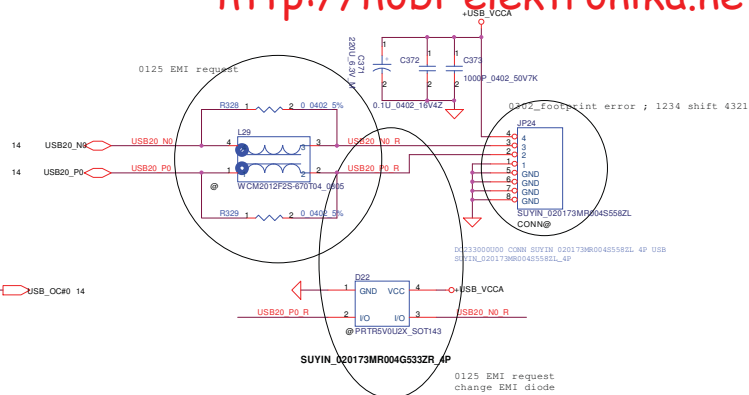
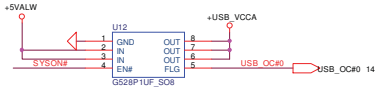
Wireless ON/OFF LED (Left 4)



On (WL_ON#-L)-> Blue
Off (WL_ON#-H)-> Amber

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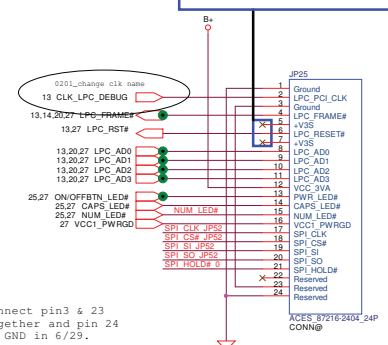
USB Port



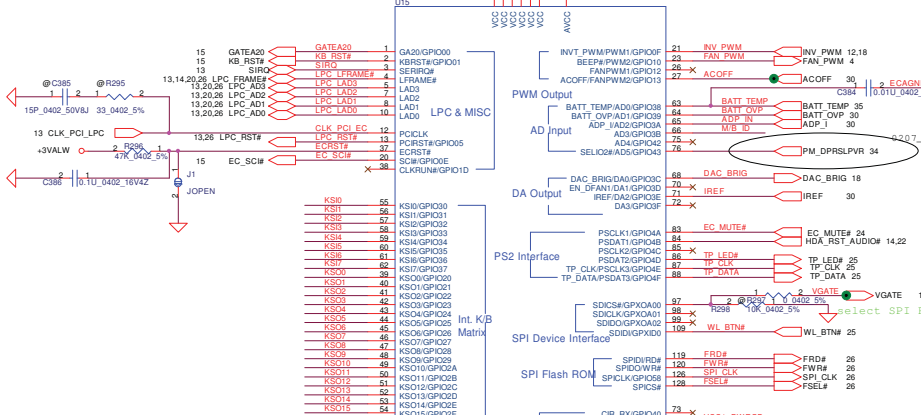
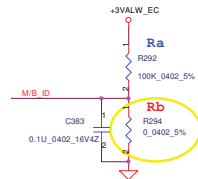
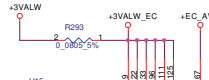
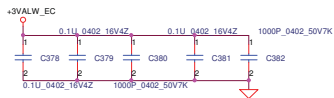
SPI ROM

LPC Debug Port

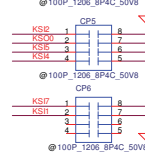
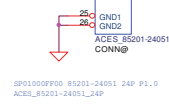
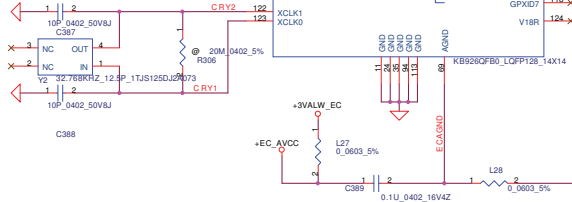
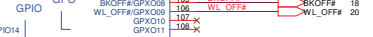
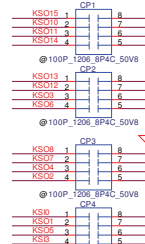
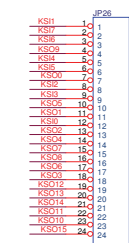
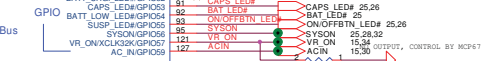
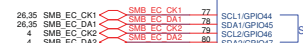
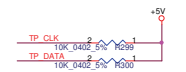
Change from +3VL to +3VS. 6/9
Removed +3VS. 6/13



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VCC		3.3V+/-5%			
Ra		100K+/-5%			
Board ID	Rb	V _{AD,REG} min	V _{AD,REG} typ	V _{AD,REG} max	
0	0	OV	OV	OV	0V
2	8.2K+/-5%	0.216V	0.250V	0.289V	
2	18K+/-5%	0.436V	0.503V	0.538V	
3	33K+/-5%	0.712V	0.819V	0.875V	
4	56K+/-5%	1.036V	1.185V	1.264V	
5	100K+/-5%	1.453V	1.650V	1.759V	
6	200K+/-5%	1.935V	2.200V	2.341V	
7	NC	2.500V	3.300V	3.300V	

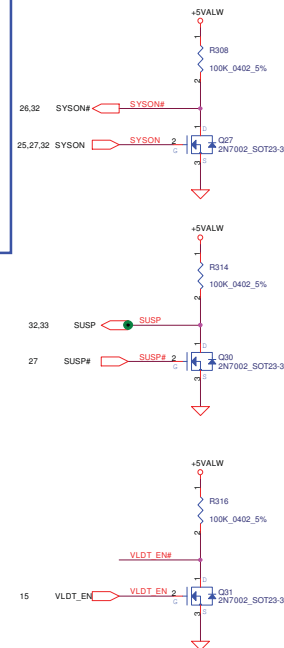
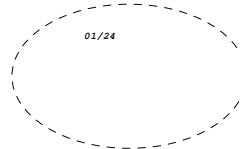
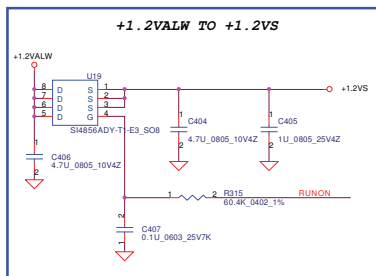
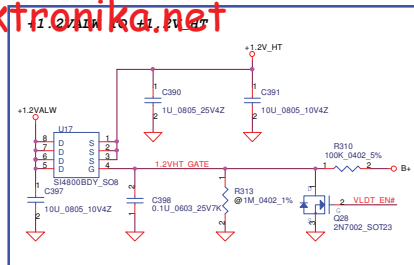


EC DEBUG port

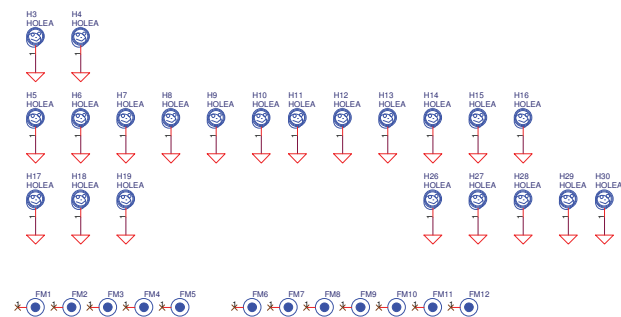


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0201_delet debug port_function same to JP25
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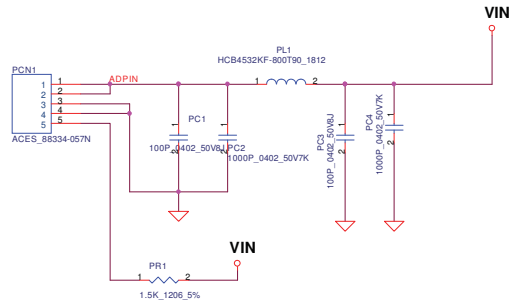
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Issued Date	2007/01/07	Deciphered Date	2008/01/12	
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		Monday, March 05, 2007		0.1
		Sheet	27	of 36



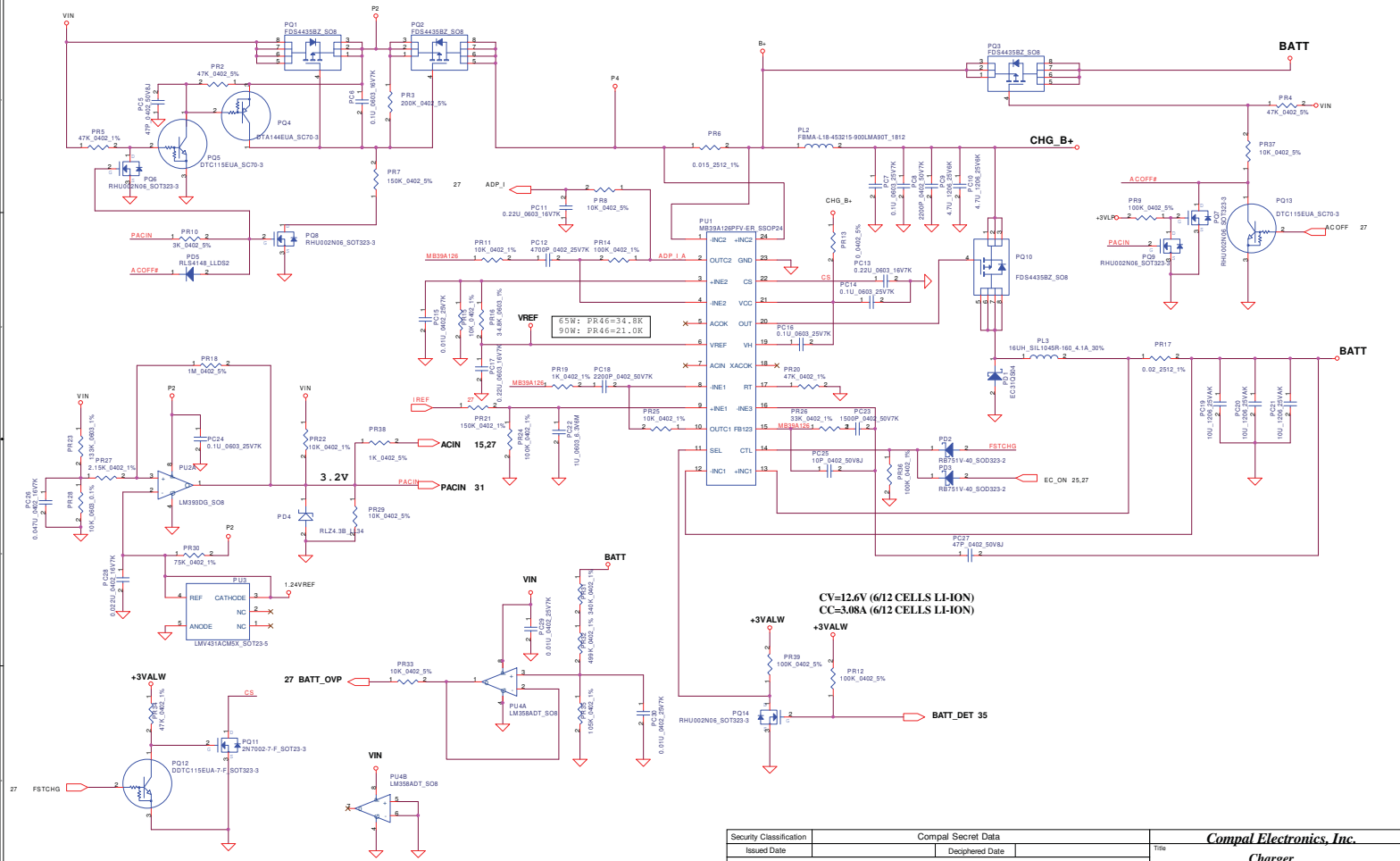
The schematic diagram illustrates a 10-bit DAC ladder network. It consists of a series of resistors (R318 to R324) and switches (Q34 to Q40) connected to a 5VGS supply and ground. The resistors are labeled with values 470, 0402, 5%. The output is taken from the node between Q39 and Q40. The diagram shows the internal structure of the DAC, including the resistors and the switches controlled by the DAC control signals.



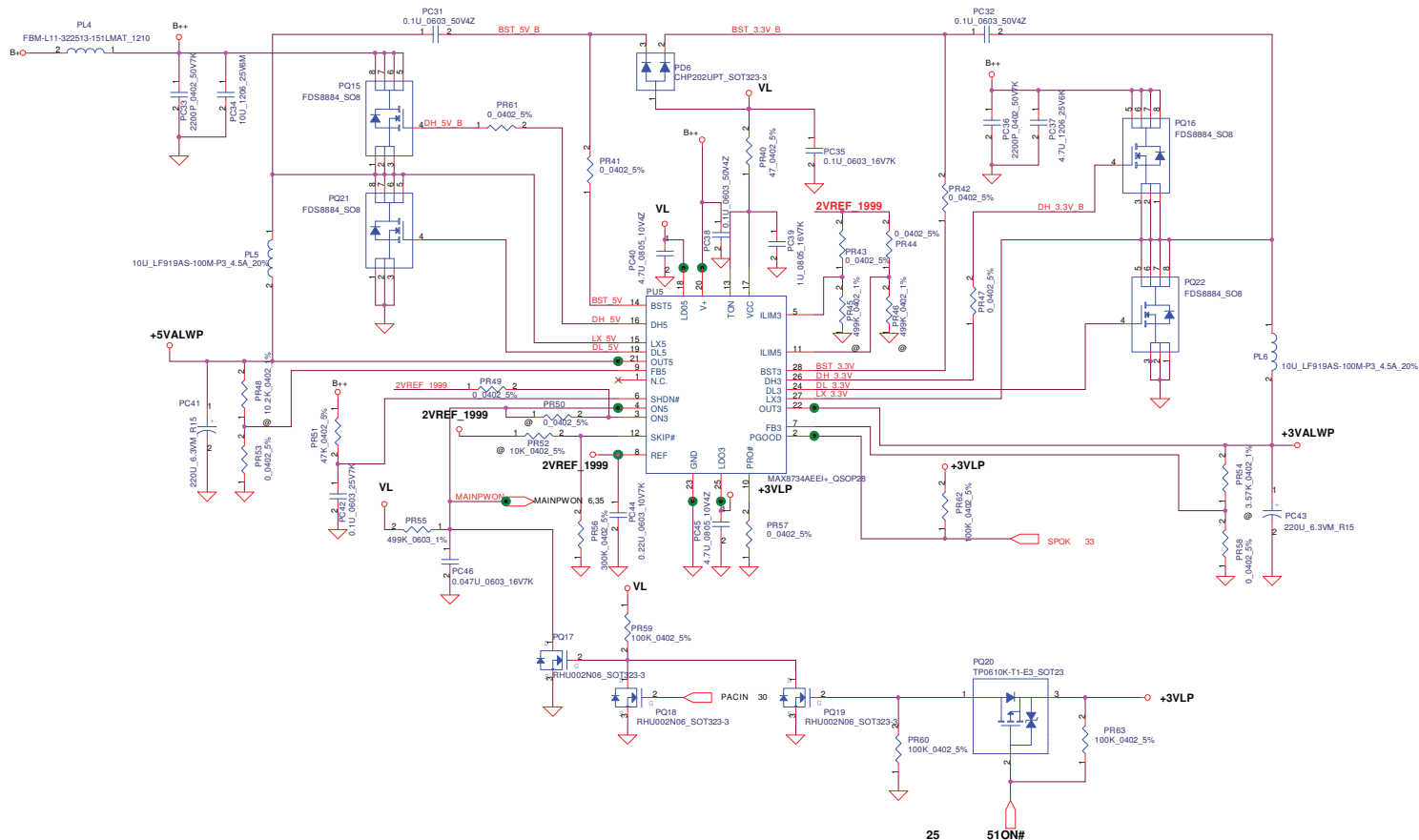
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			DC CONN Rev



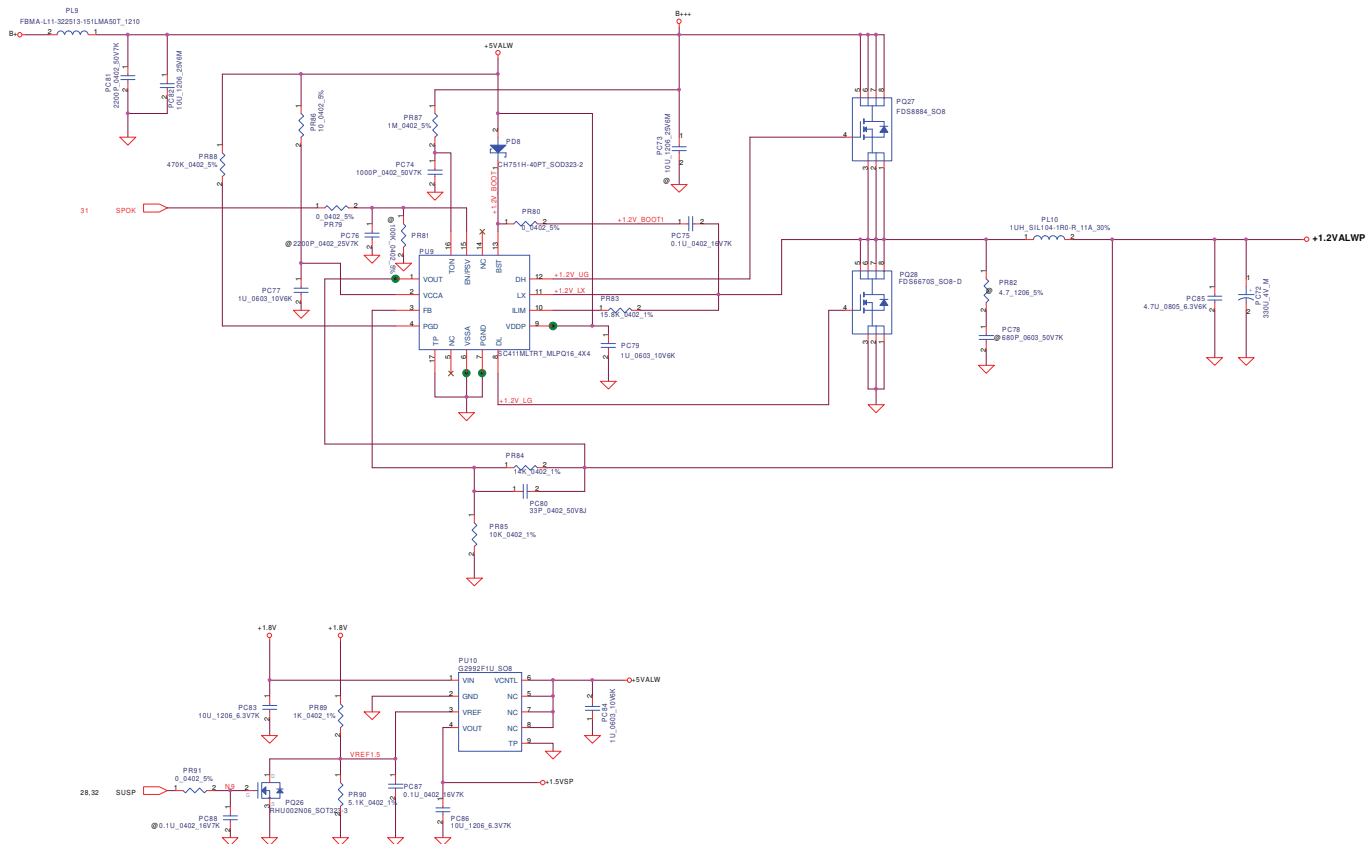
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Issue	2-1500				
Issue	Mod557, May20 05, 2007	Issue	30	31	31



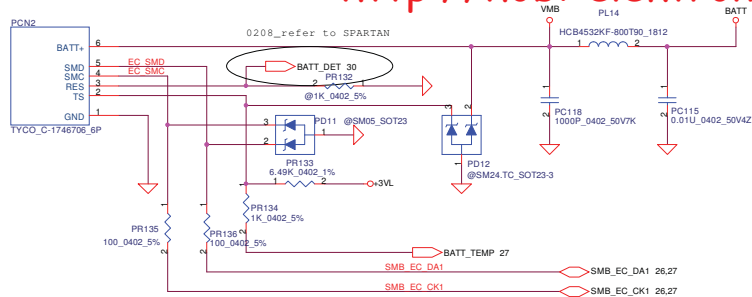
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510N#

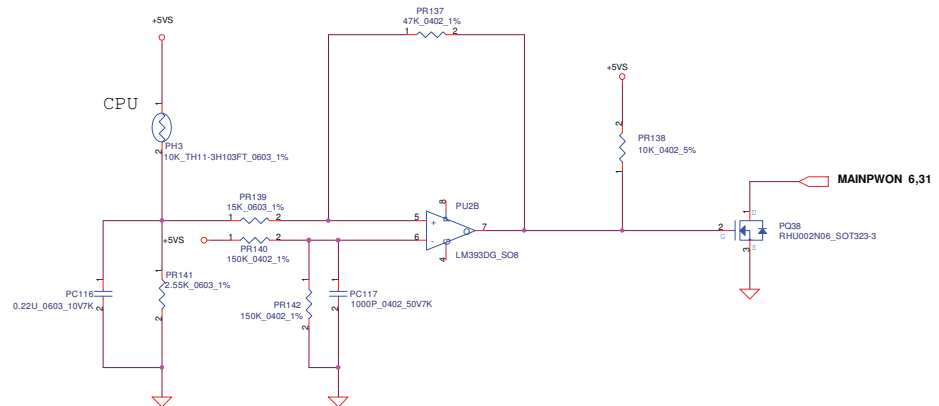
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PH1 under CPU botten side :
CPU thermal protection at 90 $\pm$ 3 degree C
Recovery at 47 $\pm$ 3 degree C



Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
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13					
14					

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Power On Sequence (AC IN mode)

