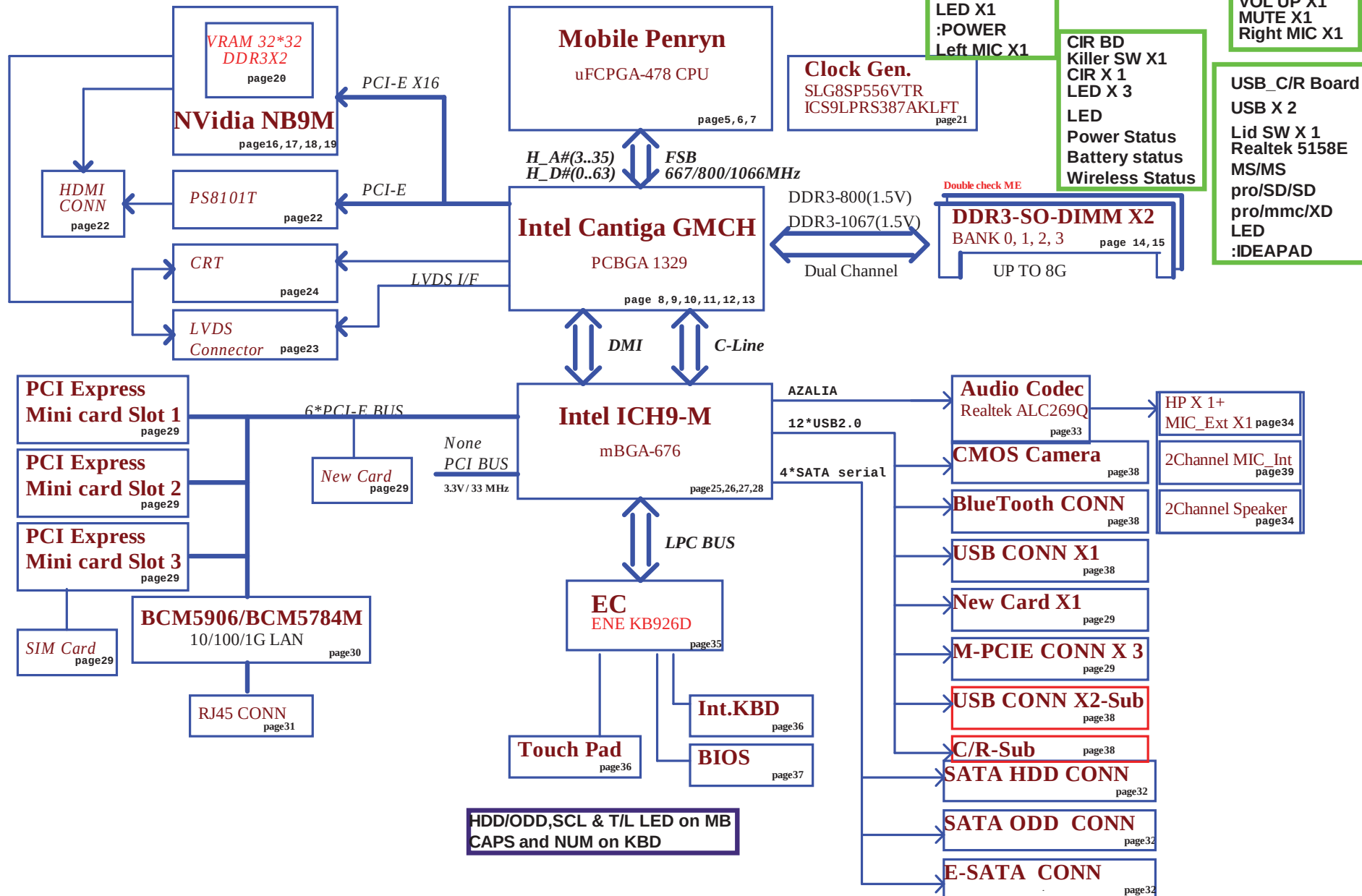


KIWB3/B4

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM/PM+ICH9-M core logic
REV:0.1

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		Size	Document Number	Rev	
		B	KIWB3/B4_LA4551P	0.1	
		Date: Friday, June 27, 2008		Sheet	1 of 49
				E	



DDR3 Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.5V +1.8V +0.75V	+5VS +3VS +1.5VS +1.1VS +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

PM@ , GM@ , N9@ , N10@

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	V	X	X	X	X	X	V	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMI_CLK_NB HDMI_DAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	VGA	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	VGA	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT	VGA	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	VGA	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPT_S0_SB SPT_CLK_SB FWR#SPT_SI_SB	ICH9	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPT_S0 SPT_CLK FWR#SPT_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

VGA and DDR2 Voltage Rails (NB9M-GS)

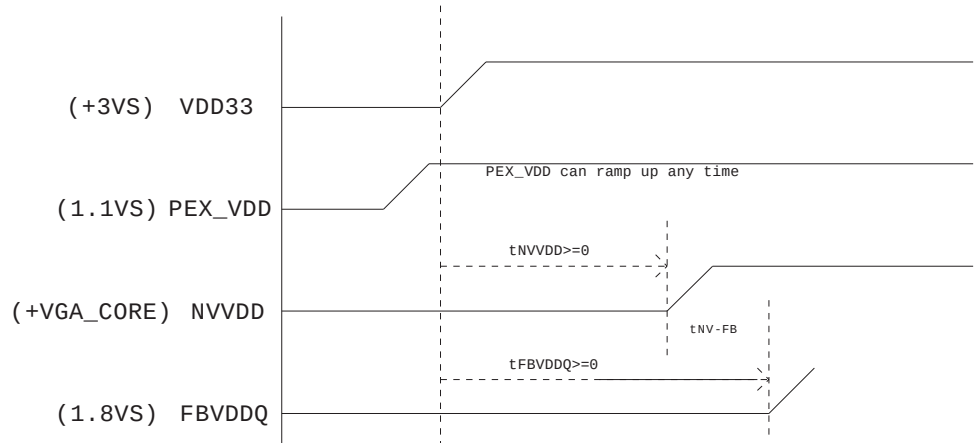
power plane			+1.8V	+3VS +VGA_CORE +1.1VS
State				
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

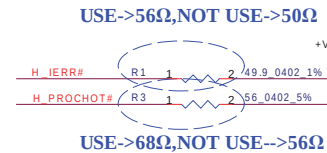
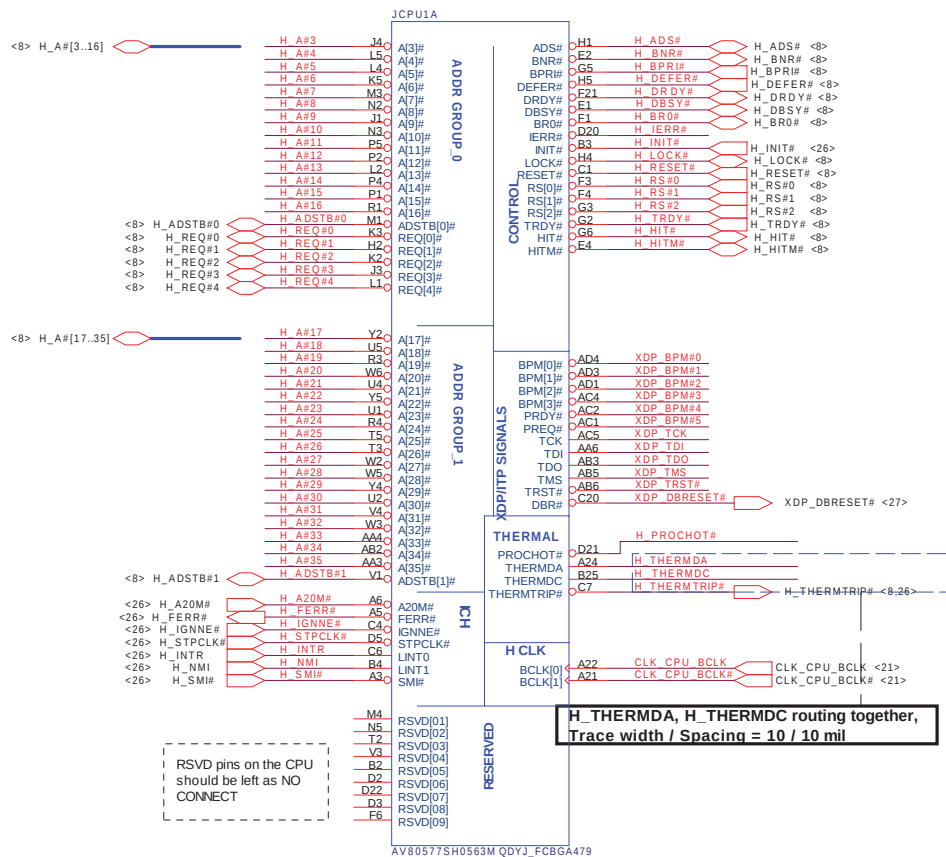
EDP at Tj = 97C*

Power Supply Rail		NB9M-GS		NB9M-GE	
	(V)	GDDR3	DDR2	GDDR3	DDR2
NVVD	Variable	11.22A	10.87A	9.2A	8.88A
FB_DLLAVDD	1.1	25mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	385mA			
IFPD_IOVDD	1.1	385mA			
IFPE_IOVDD	1.1	385mA			
IFPF_IOVDD	1.1	385mA			
PEX_IOVDD/Q	1.1	1550mA			
PEX_PLLVDD	1.1	165mA			
PLLVD	1.1	55mA			
SP_PLLVDD	1.1	25mA			
VID_PLLVDD	1.1	50mA			
TOTAL	1.1	3.425A			
FBVDD/Q	1.8	2.24A	1.65A	2.17A	1.63A
IFPA_IOVDD	1.8	50mA			
IFPB_IOVDD	1.8	50mA			
IFPAB_PLLVDD	1.8	100mA			
IFPCD_PLLVDD	1.8	160mA			
IFPEF_PLLVDD	1.8	160mA			
TOTAL	1.8	2.76A	2.17A	2.69A	2.15A
DACA_VDD	3.3	110mA			
DACB_VDD	3.3	125mA			
DACC_VDD	3.3	110mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	80mA			
TOTAL	3.3	0.445A			

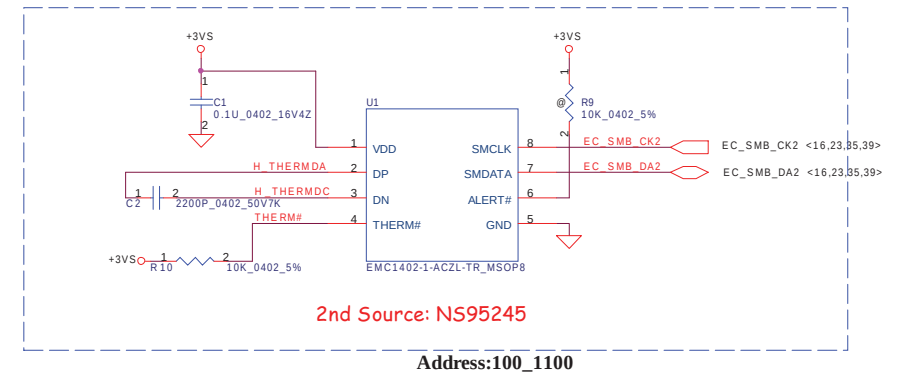
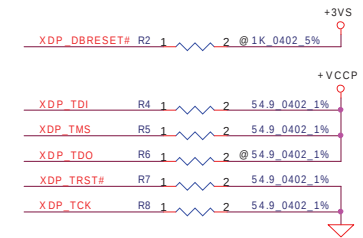
POWER SQUENCE

The ramp time for any rail must be more than 40us

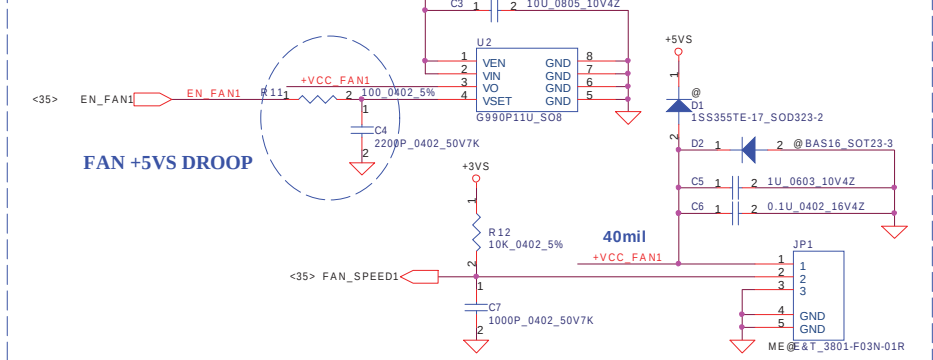


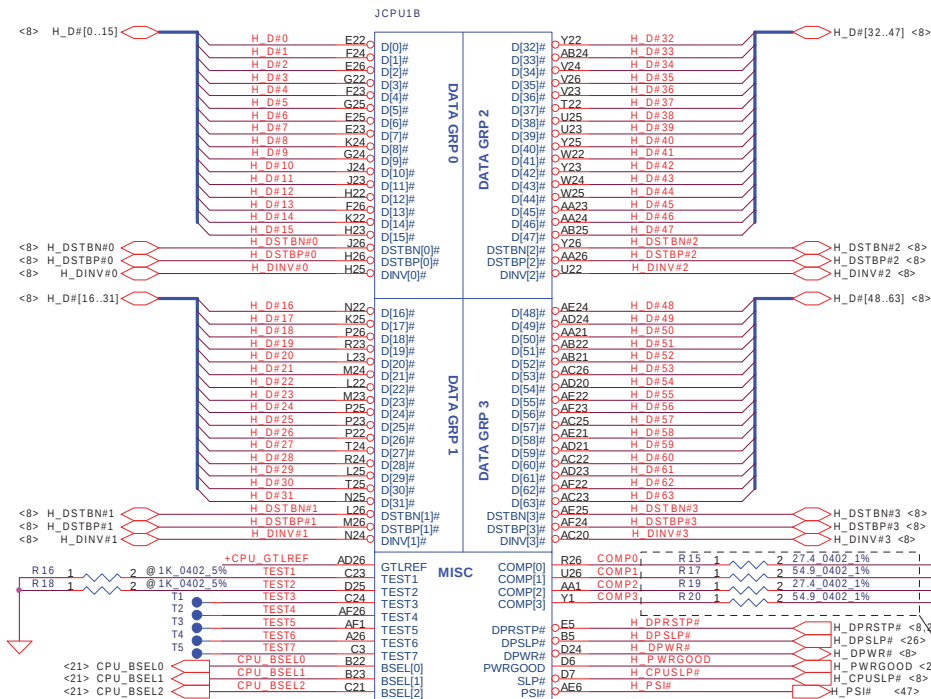


XDP Reserve



FAN1 Comm





Trace Close CPU < 0.5'

Width=4 mil,
Spacing: 15mil
(550hm)

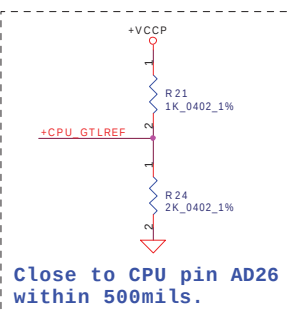
TRACE CLOSELY CPU < 0.5'

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 5mils and Space 25mils (550hm)

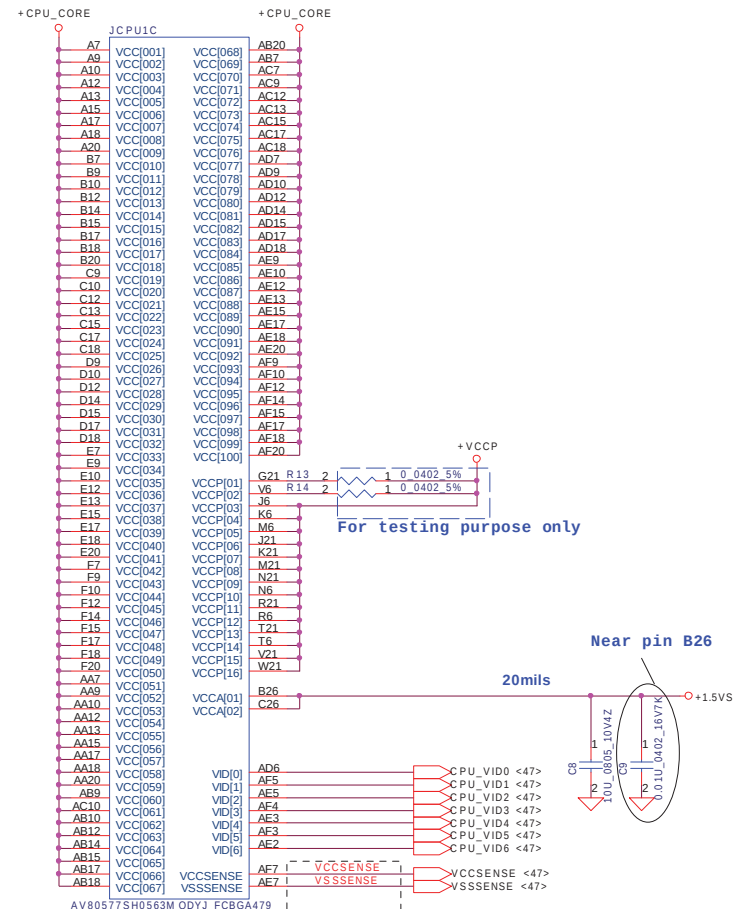
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TP's

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

Layout note: Z0=55 ohm
0.5" max for GTLREF.



Close to CPU pin AD26
within 500mils.



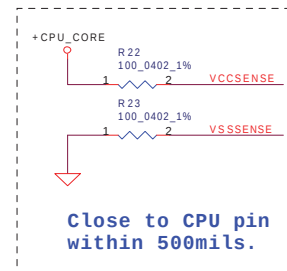
For testing purpose only

Near pin B26

20mils

Length match within 25 mils.
The trace width/space/other is
18/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at
27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.



Close to CPU pin
within 500mils.

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				Size B	Document Number			Rev
				KIWB3/B4_LA4551P			0.1	
				Date:	Friday, June 27, 2008		Sheet	6





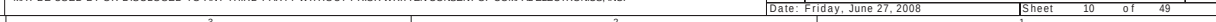
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				Document Number	
				KTWB3/B4_LA4551P Date: Friday, June 27, 2008	Sheet 8 of 49

1. Data Bus;
2. Data Strobe Differential Pairs;
3. Data Mask Bits;
4. Address Group;
5. Bank Select Group;
6. Command Group;
7. CLK Group;
- *. Reset Group;



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				Document Number KIWB3/B4_LA4551P	
Date:		Friday, June 27, 2008		Sheet 9	of 49

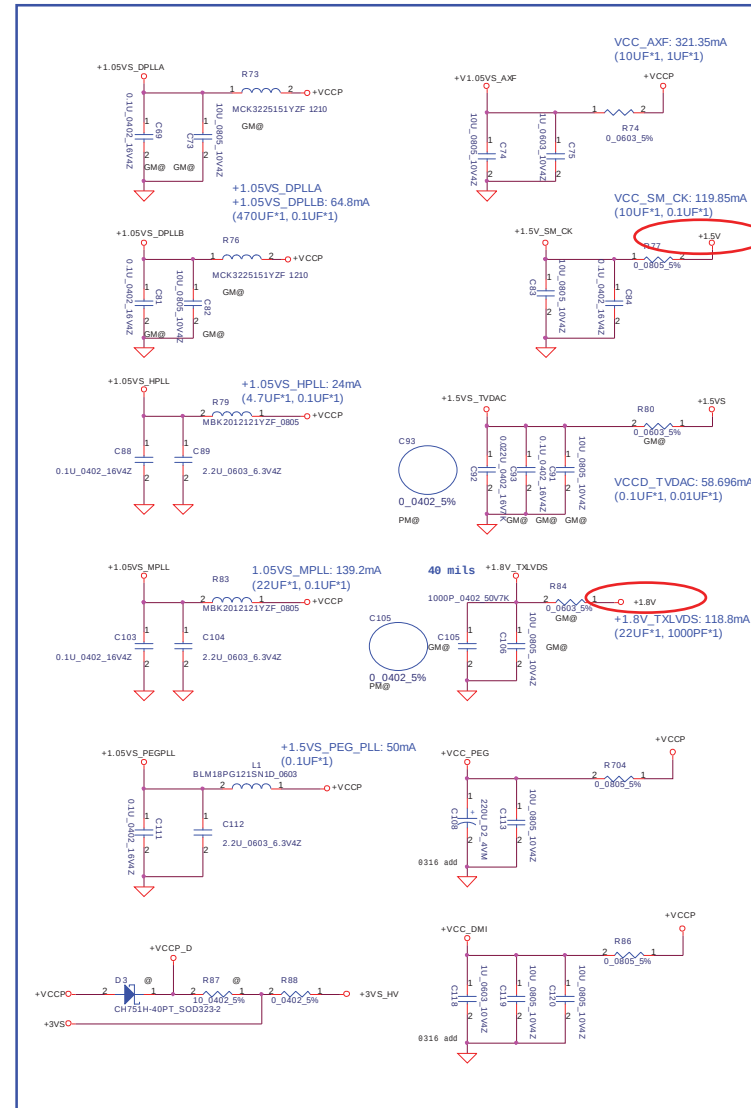
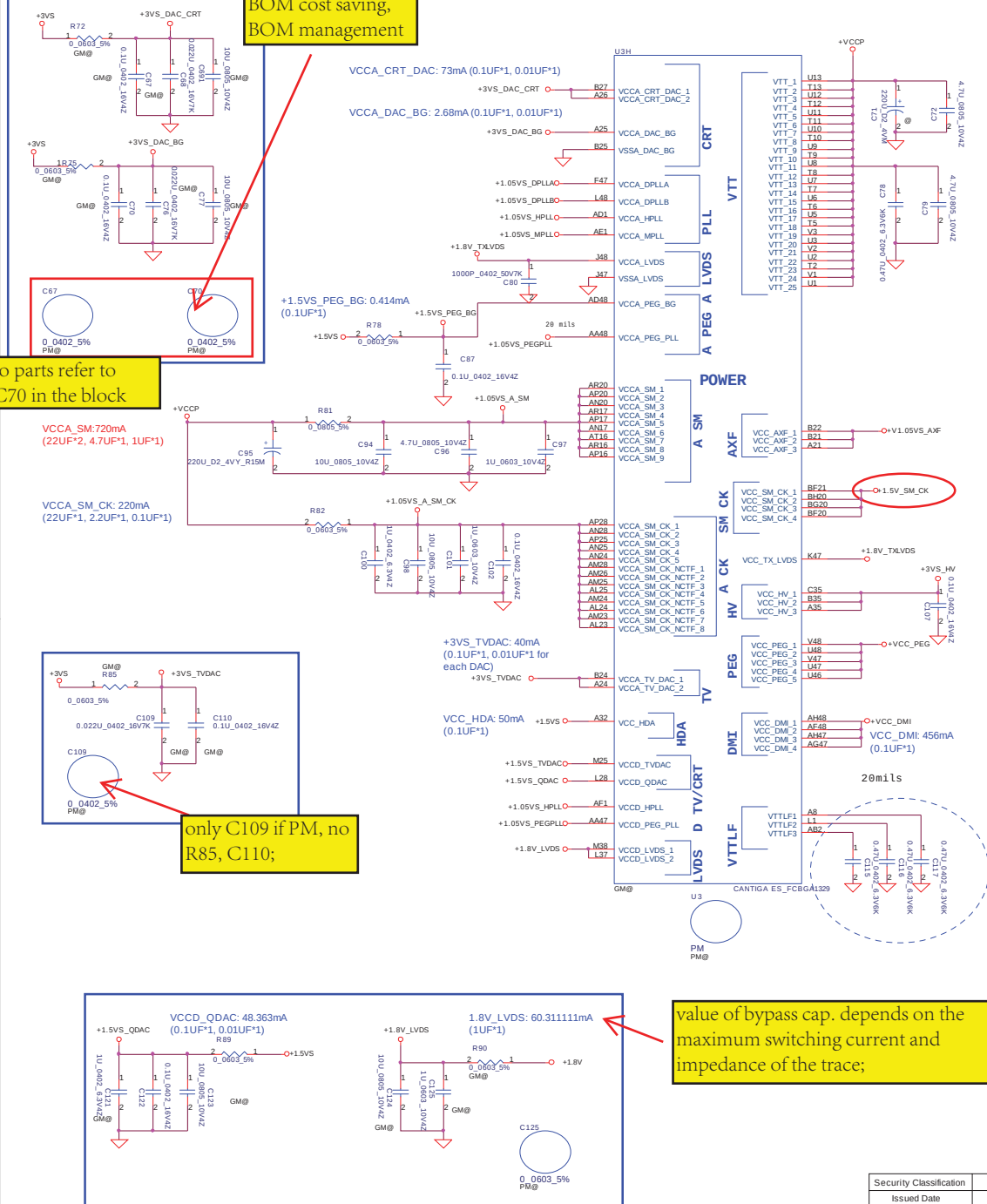


BOM cost saving,
BOM management

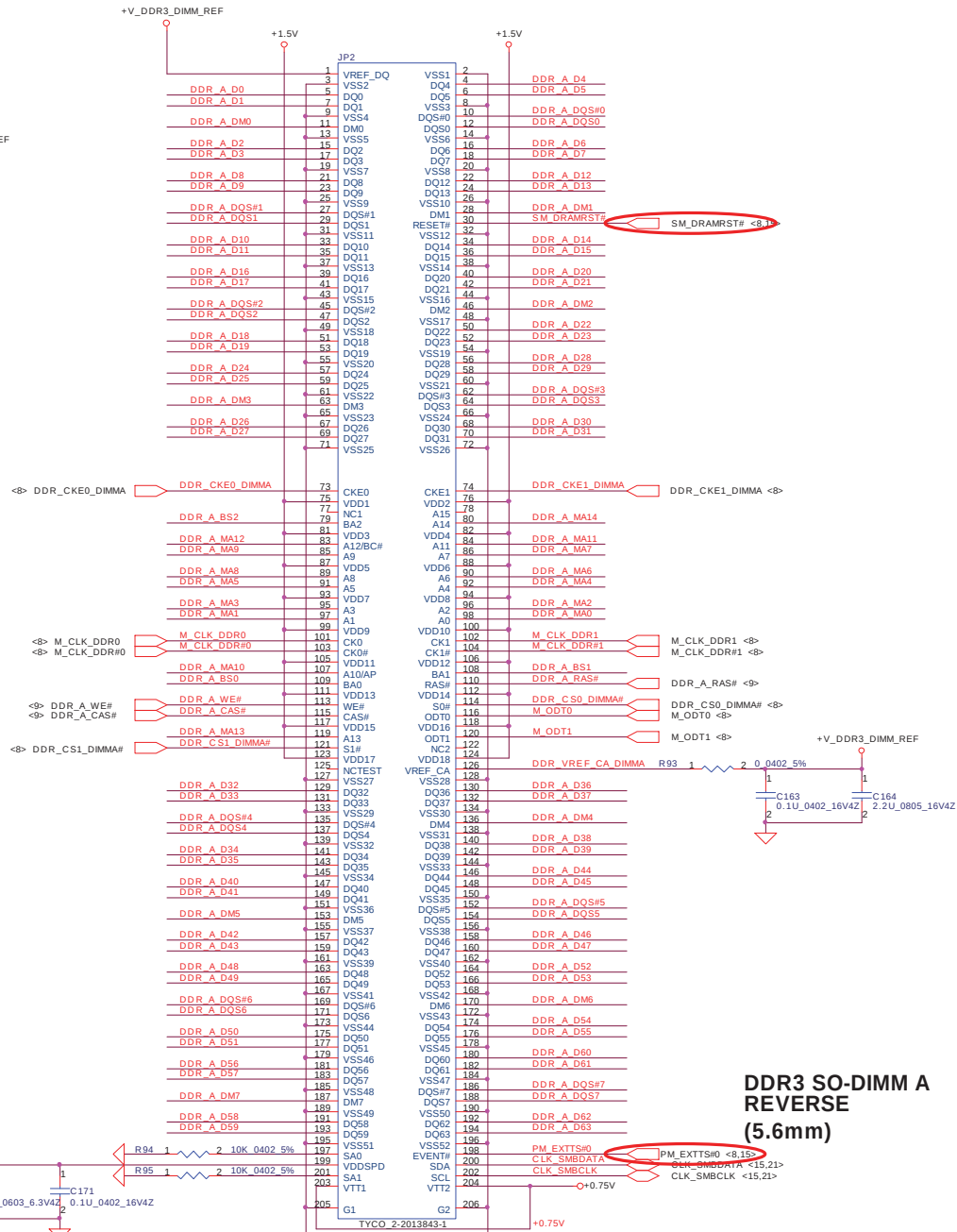
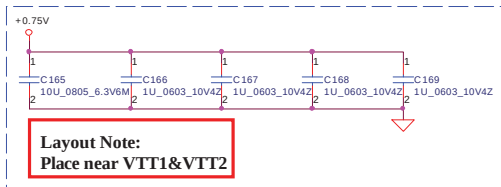
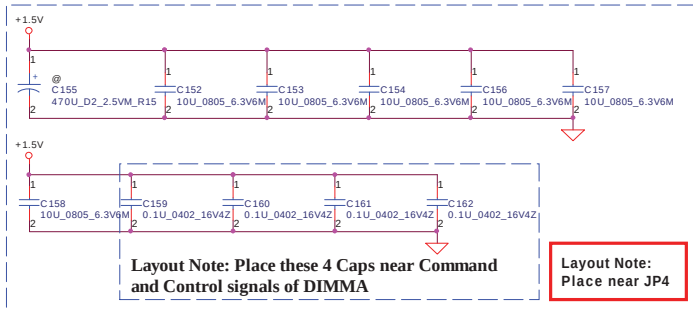
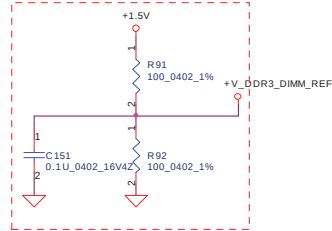
the two parts refer to
C67, C70 in the block

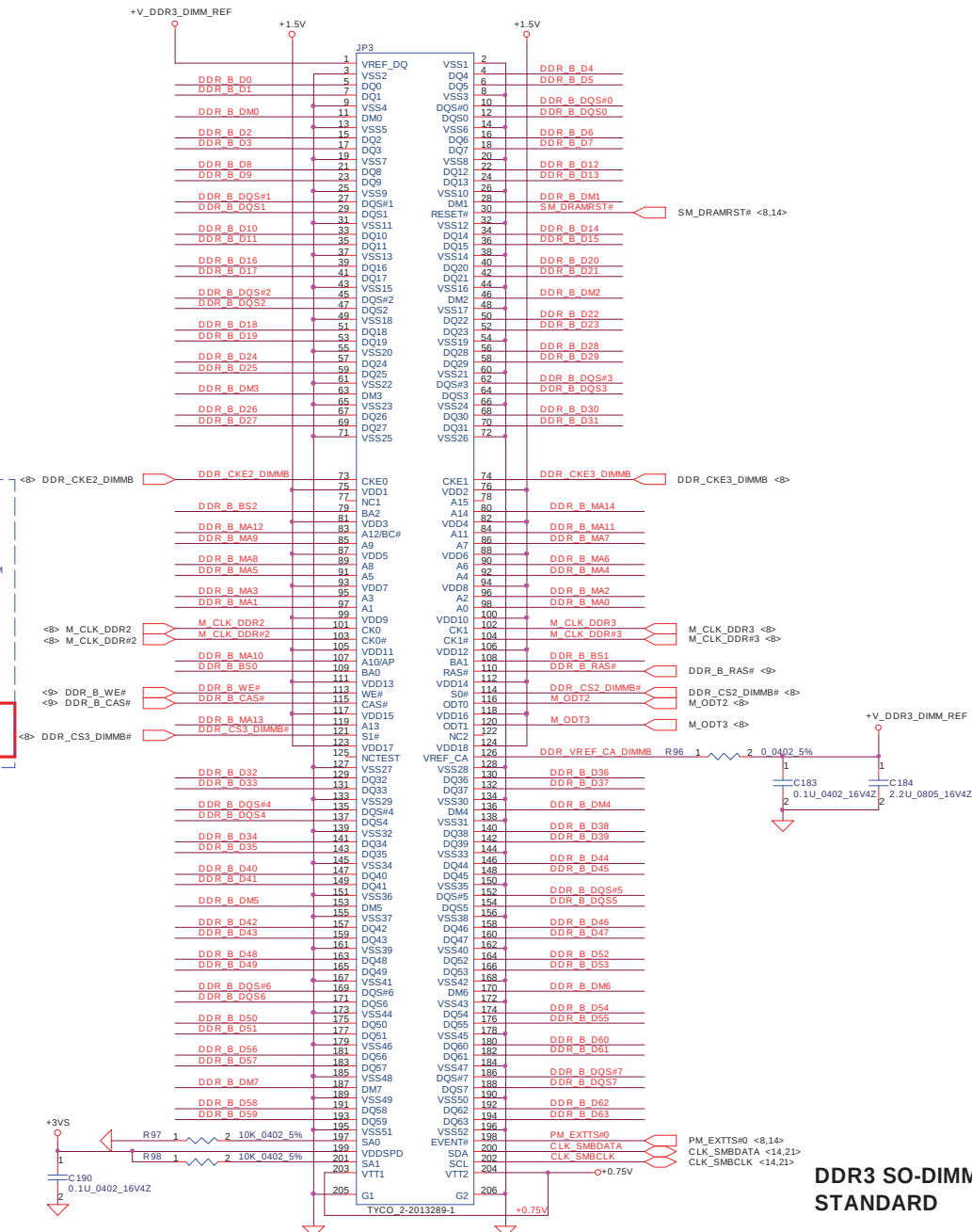
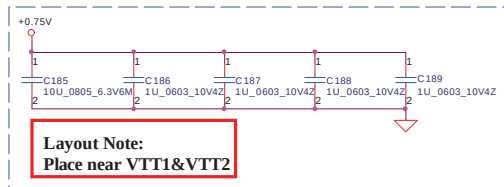
only C109 if PM, no
R85, C110;

value of bypass cap. depends on the
maximum switching current and
impedance of the trace;



<9> DDR_A_DQS#[0..7]
 <9> DDR_A_D[0..63]
 <9> DDR_A_DM[0..7]
 <9> DDR_A_DQS[0..7]
 <9> DDR_A_MA[0..14]
 <9> DDR_A_BS[0..2]





DDR3 SO-DIMM B STANDARD

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					KIWB3/B4_LA4551P	0
				Date:	Friday, June 27, 2008	Sheet 15 of 49

<10> PCIE_MTX_C_GRX_N0_15] PCIE_MTX_C_GRX_N0_15]

<10> PCIE_MTX_C_GRX_P0_15] PCIE_MTX_C_GRX_P0_15]

<10> PCIE_GTX_C_MRX_N0_15] PCIE_GTX_C_MRX_N0_15]

<10> PCIE_GTX_C_MRX_P0_15] PCIE_GTX_C_MRX_P0_15]

PCIE_MTX_C_GRX_P0 AE12

PCIE_MTX_C_GRX_N0 AE12

PCIE_MTX_C_GRX_P1 AG12

PCIE_MTX_C_GRX_N1 AG13

PCIE_MTX_C_GRX_P2 AE13

PCIE_MTX_C_GRX_N2 AE13

PCIE_MTX_C_GRX_P3 AE15

PCIE_MTX_C_GRX_N3 AF15

PCIE_MTX_C_GRX_P4 AG15

PCIE_MTX_C_GRX_N4 AG16

PCIE_MTX_C_GRX_P5 AE16

PCIE_MTX_C_GRX_N5 AF16

PCIE_MTX_C_GRX_P6 AE18

PCIE_MTX_C_GRX_N6 AF18

PCIE_MTX_C_GRX_P7 AG18

PCIE_MTX_C_GRX_N7 AG19

PCIE_MTX_C_GRX_P8 AE19

PCIE_MTX_C_GRX_N8 AE19

PCIE_MTX_C_GRX_P9 AE21

PCIE_MTX_C_GRX_N9 AE21

PCIE_MTX_C_GRX_P10 AG21

PCIE_MTX_C_GRX_N10 AG22

PCIE_MTX_C_GRX_P11 AE22

PCIE_MTX_C_GRX_N11 AE22

PCIE_MTX_C_GRX_P12 AE24

PCIE_MTX_C_GRX_N12 AE24

PCIE_MTX_C_GRX_P13 AG24

PCIE_MTX_C_GRX_N13 AF25

PCIE_MTX_C_GRX_P14 AG25

PCIE_MTX_C_GRX_N14 AG26

PCIE_MTX_C_GRX_P15 AE27

PCIE_MTX_C_GRX_N15 AE27

PCIE_GTX_C_MRX_P0 C193 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_N0 C194 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_P1 C195 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_N1 C196 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_P2 C197 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_N2 C198 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_P3 C199 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_N3 C200 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_P4 C201 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_N4 C202 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_P5 C203 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_N5 C204 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_P6 C205 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_N6 C206 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_P7 C207 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_N7 C208 PM@ 1 2 0.1U 0402_16V7K

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PCIE_GTX_C_MRX_N8 C210 PM@ 1 2 0.1U 0402_16V7K

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PCIE_GTX_C_MRX_N9 C212 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_P10 C213 PM@ 1 2 0.1U 0402_16V7K

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PCIE_GTX_C_MRX_P11 C215 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_N11 C216 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_P12 C217 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_N12 C218 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_P13 C219 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_N13 C220 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_P14 C221 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_N14 C222 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_P15 C223 PM@ 1 2 0.1U 0402_16V7K

PCIE_GTX_C_MRX_N15 C224 PM@ 1 2 0.1U 0402_16V7K

<21> CLK_PCIE_VGA CLK_PCIE_VGA

<21> CLK_PCIE_VGA# CLK_PCIE_VGA#

R118 2.0K_0402_5% PM@

R119 2.4K_0402_1% PM@

PLT_RST#

R122 10K_0402_5% PM@

OSC_SPREAD OSC_OUT

R125 10K_0402_5% PM@

R126 10K_0402_5% PM@

If External Spread Spectrum not stuff then stuff resistor

C229 20P_0402_50V8 PM@

27MHz_16PF_X7502700BG1H-U PM@

C230 20P_0402_50V8 PM@

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Part 1 of 5

GPIO

DACA

DACB

DACC

I2C

TEST

CLK

HDA

GPIO0 N1 X

GPIO1 G1 X

GPIO2 M2 X

GPIO3 P3 X

GPIO4 K3 X

GPIO5 K2 X

GPIO6 K3 X

GPIO7 C2 X

GPIO8 M1 X

GPIO9 D2 X

GPIO10 D1 X

GPIO11 J1 X

GPIO12 J1 X

GPIO13 K1 X

GPIO14 F3 X

GPIO15 F3 X

GPIO16 G2 X

GPIO17 F1 X

GPIO18 F2 X

GPIO19 F2 X

DACA_HS_VSYNC DACA_HS_VSYNC

DACA_VSYNC DACA_VSYNC

DACA_RED DACA_RED

DACA_BLUE DACA_BLUE

DACA_GREEN DACA_GREEN

DACA_VREF DACA_VREF

DACA_RST DACA_RST

DACB_CS_VSYNC DACB_CS_VSYNC

DACB_RED DACB_RED

DACB_BLUE DACB_BLUE

DACB_GREEN DACB_GREEN

DACC_VREF DACC_VREF

DACC_RST DACC_RST

DACC_HS_VSYNC DACC_HS_VSYNC

DACC_VSYNC DACC_VSYNC

DACC_RED DACC_RED

DACC_BLUE DACC_BLUE

DACC_GREEN DACC_GREEN

DACC_VREF DACC_VREF

DACC_RST DACC_RST

I2CA_SCL I2CA_SCL

I2CA_SDA I2CA_SDA

I2CB_SCL I2CB_SCL

I2CB_SDA I2CB_SDA

I2CC_SCL I2CC_SCL

I2CC_SDA I2CC_SDA

I2CD_SCL I2CD_SCL

I2CD_SDA I2CD_SDA

I2CE_SCL I2CE_SCL

I2CE_SDA I2CE_SDA

I2CH_SCL I2CH_SCL

I2CH_SDA I2CH_SDA

I2CS_SCL I2CS_SCL

I2CS_SDA I2CS_SDA

JTAG_TCK JTAG_TCK

JTAG_TDI JTAG_TDI

JTAG_TDO JTAG_TDO

JTAG_TMS JTAG_TMS

JTAG_TRST_N JTAG_TRST_N

TESTMODE TESTMODE

SPDIF_IN SPDIF_IN

VDD_SENSE VDD_SENSE

HDA_RST_N HDA_RST_N

HDA_SDI HDA_SDI

HDA_SDO HDA_SDO

HDA_SYNC HDA_SYNC

HDA_BCLK HDA_BCLK

GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.9V	10,12
1	1	1.17V	0
0	1	1.09V	8

VGA_CRT_R R99 1 PM@ 2 150 0402_1%

VGA_CRT_G R100 1 PM@ 2 150 0402_1%

VGA_CRT_B R101 1 PM@ 2 150 0402_1%

GPU_VID1 GPU_VID1 <46>

GPU_VID0 GPU_VID0 <46>

VGA_GPIO11 R887 10K_0402_5% N10@

VGA_GPIO14 R888 10K_0402_5% N10@

VGA_HS_VSYNC R102 2.2K_0402_5% PM@

VGA_VSYNC R103 2.2K_0402_5% PM@

VGA_CRT_R R104 10K_0402_5% PM@

VGA_CRT_B R105 2.2K_0402_5% PM@

VGA_CRT_G R106 10K_0402_5% PM@

VGA_CRT_B R107 100K_0402_1% PM@

VGA_HS_VSYNC R110 2.2K_0402_5% PM@

VGA_VSYNC R111 2.2K_0402_5% PM@

VGA_HS_VSYNC R112 2.2K_0402_5% PM@

VGA_VSYNC R113 2.2K_0402_5% PM@

VGA_HS_VSYNC R114 2.2K_0402_5% PM@

VGA_VSYNC R115 2.2K_0402_5% PM@

VGA_HS_VSYNC R116 2.2K_0402_5% PM@

VGA_VSYNC R117 2.2K_0402_5% PM@

VGA_HS_VSYNC R118 2.2K_0402_5% PM@

VGA_VSYNC R119 2.2K_0402_5% PM@

VGA_HS_VSYNC R120 2.2K_0402_5% PM@

VGA_VSYNC R121 2.2K_0402_5% PM@

VGA_HS_VSYNC R122 2.2K_0402_5% PM@

VGA_VSYNC R123 2.2K_0402_5% PM@

VGA_HS_VSYNC R124 2.2K_0402_5% PM@

VGA_VSYNC R125 2.2K_0402_5% PM@

VGA_HS_VSYNC R126 2.2K_0402_5% PM@

VGA_VSYNC R127 2.2K_0402_5% PM@

VGA_HS_VSYNC R128 2.2K_0402_5% PM@

VGA_VSYNC R129 2.2K_0402_5% PM@

VGA_HS_VSYNC R130 2.2K_0402_5% PM@

VGA_VSYNC R131 2.2K_0402_5% PM@

VGA_HS_VSYNC R132 2.2K_0402_5% PM@

VGA_VSYNC R133 2.2K_0402_5% PM@

VGA_HS_VSYNC R134 2.2K_0402_5% PM@

VGA_VSYNC R135 2.2K_0402_5% PM@

VGA_HS_VSYNC R136 2.2K_0402_5% PM@

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VGA_VSYNC R139 2.2K_0402_5% PM@

VGA_HS_VSYNC R140 2.2K_0402_5% PM@

VGA_VSYNC R141 2.2K_0402_5% PM@

For N10M

For N10M

For N10M

For N10M

For N10M

For N10M

For N10M

For N10M

For N10M

For N10M

For N10M

For N10M

For N10M

For N10M

For N10M

For N10M

For N10M

For N10M

For N10M

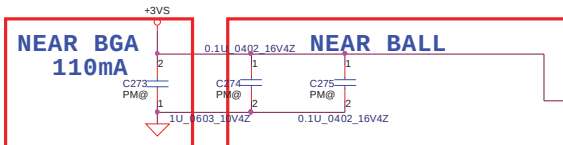
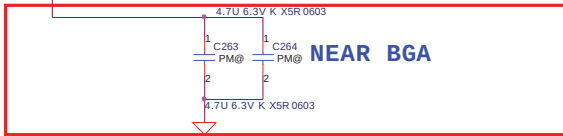
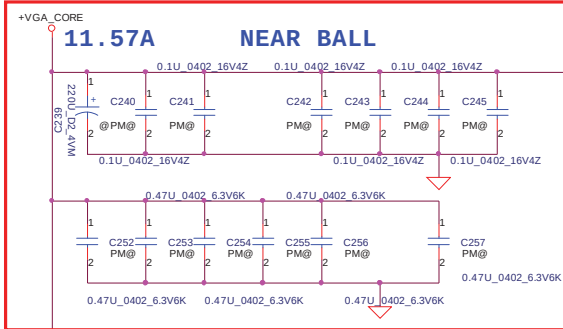
For N10M

For N10M

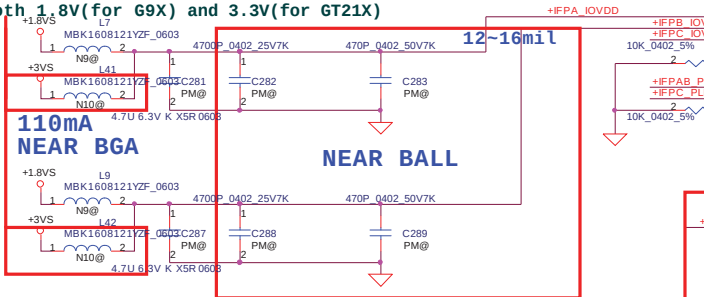
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Issued Date	2007/10/15	Deciphered Date	2008/10/15
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Size	Document Number	Rev	
B	KIWB3/B4_LA-4551P	0.1	
Date	Friday, June 27, 2008	Sheet	16 of 48



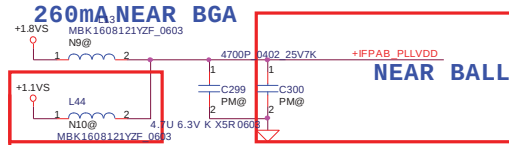
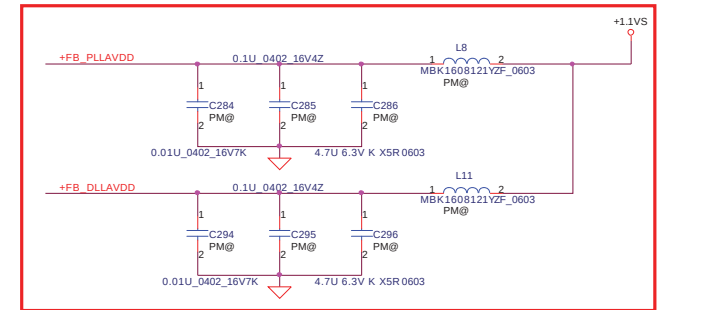
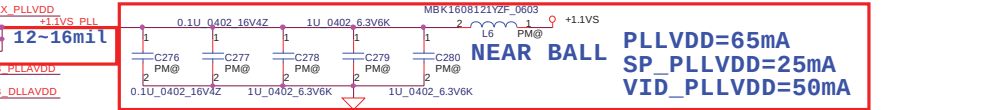
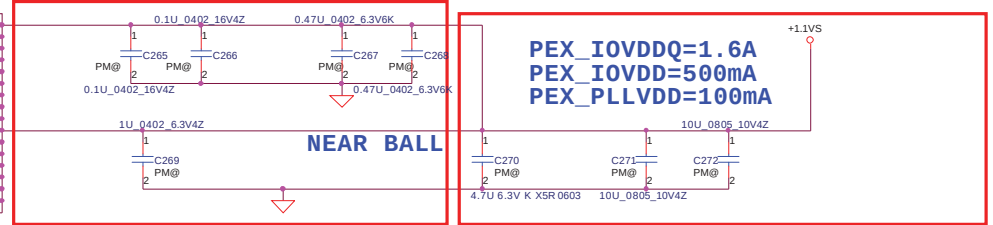
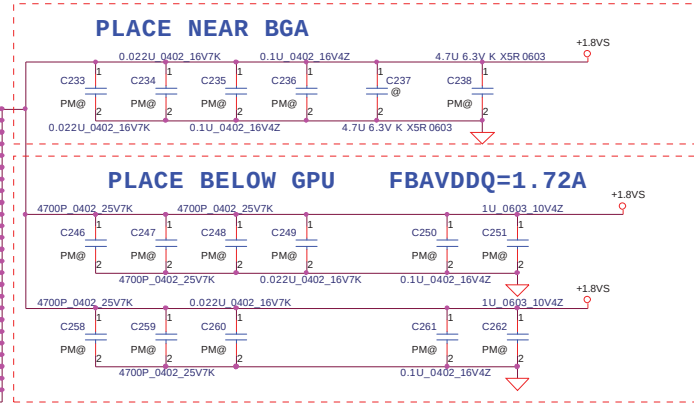
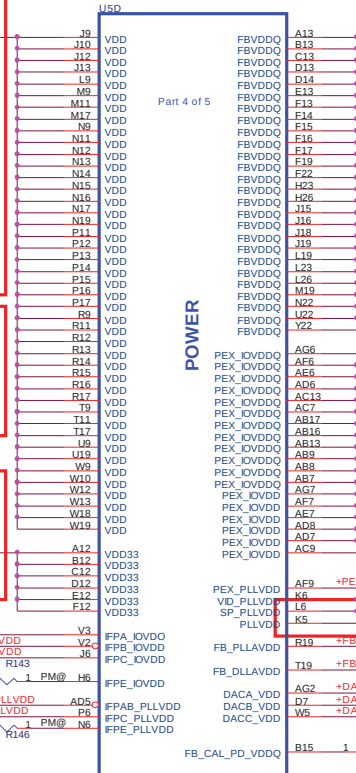
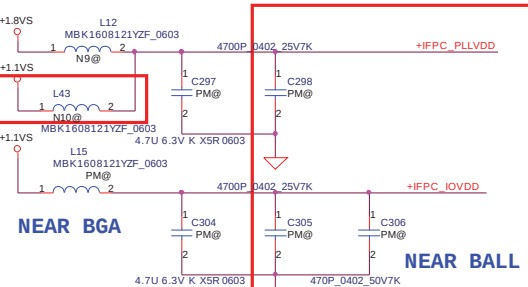
FOR N10M , 1.1VS will changed to 1.05VS



IFPA/B_IOVDD: please add option to support both 1.8V(for G9X) and 3.3V(for GT21X)

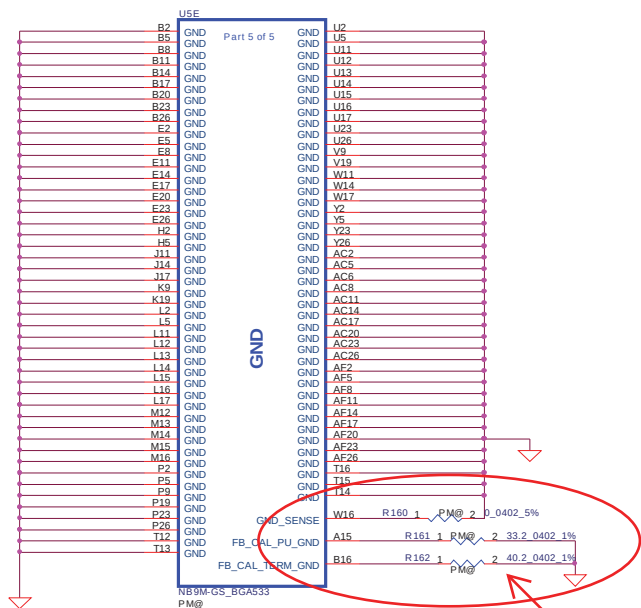


IFPC_PLLVDD: please add option to support both 1.8V (for G9X) and 1.05V(for GT21X)



IFPAB_PLLVDD: please add option to support both 1.8V(for G9X) and 1.05V(for GT21X)

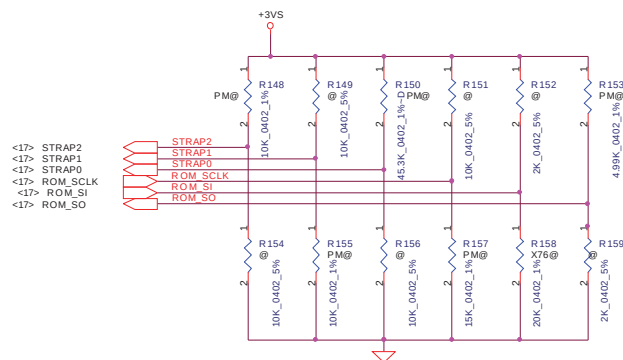
Security Classification	Compal Secret Data			Compal Electronics, Inc. NB9M-GS Power		
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title		
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				Cuspm	KIWB3/B4_LA-4551P	0.1
				Date:	Friday, June 27, 2008	Sheet 18 of 49



Memory/PKG	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR2	30.1ohm	30.1ohm	NC
GDDR3	33.2ohm	44.2ohm	40.2ohm

To update for NV PUN-03304-001_V06 (2008/4/01)

A total of 8 signals are required for GB1 strapping this includes
 2 reference signals
 6 physical strapping pins
 4 logical strapping bits
 A total of 24 logical strapping bits are available



GB1 Family GPU Strap Options

GPU	FB Memory (GDDR3)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
NB9M-GS (0x06E9)	Samsung	16Mx32	PU 5K PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
		32Mx32	PU 5K PD 15K	PD 45K	PU 10K	PD 10K	PU 45K
	Hynix	16Mx32	PU 5K PD 15K	PD 15K	PU 10K	PD 10K	PU 45K
		32Mx32	PU 5K PD 15K	PD 35K	PU 10K	PD 10K	PU 45K
	Qimonda	16Mx32	PU 5K PD 15K	PD 10K	PU 10K	PD 10K	PU 45K
		32Mx32	PU 5K PD 15K	PD 30K	PU 10K	PD 10K	PU 45K

P/N:SA00002D700 (8101T)
P/N:SA00001U920 (CH7318C)

U11
OE# 25
SCL_SINK 28
SDA_SINK 29
HPD_SINK 30
DDC_EN 32
CFG0 34
CFG1 35

<10> TMDS_B_CLK 48 IN_D4+
<10> TMDS_B_CLK# 47 IN_D4-
<10> TMDS_B_DATA0 45 IN_D3+
<10> TMDS_B_DATA0# 44 IN_D3-
<10> TMDS_B_DATA1 42 IN_D2+
<10> TMDS_B_DATA1# 41 IN_D2-
<10> TMDS_B_DATA2 39 IN_D1+
<10> TMDS_B_DATA2# 38 IN_D1-

TMDS pull down (500ohm) resistors G9x only

HDMI_CLK+ CONN 1 2 PM@ 499_0402_1%
HDMI_CLK- CONN 2 1 PM@ 499_0402_1%
HDMI_TX0+ CONN 3 2 PM@ 499_0402_1%
HDMI_TX0- CONN 4 1 PM@ 499_0402_1%
HDMI_TX1+ CONN 5 2 PM@ 499_0402_1%
HDMI_TX1- CONN 6 1 PM@ 499_0402_1%
HDMI_TX2+ CONN 7 2 PM@ 499_0402_1%
HDMI_TX2- CONN 8 1 PM@ 499_0402_1%

NEAR CONNECTOR

HDMI_CLK- 1 L18 2 HDMI_CLK- CONN
HDMI_CLK+ 4 L18 3 HDMI_CLK+ CONN
WCM-2012-900T_4P
HDMI_TX0- 1 L19 2 HDMI_TX0- CONN
HDMI_TX0+ 4 L19 3 HDMI_TX0+ CONN
WCM-2012-900T_4P
HDMI_TX1- 1 L21 2 HDMI_TX1- CONN
HDMI_TX1+ 4 L21 3 HDMI_TX1+ CONN
WCM-2012-900T_4P
HDMI_TX2- 1 L22 2 HDMI_TX2- CONN
HDMI_TX2+ 4 L22 3 HDMI_TX2+ CONN
WCM-2012-900T_4P

R246 1 2 @ 0 0402 5% HDMI_CLK+ CONN
R247 1 2 @ 0 0402 5% HDMI_CLK- CONN
R248 1 2 @ 0 0402 5% HDMI_TX0+ CONN
R249 1 2 @ 0 0402 5% HDMI_TX0- CONN
R250 1 2 @ 0 0402 5% HDMI_TX1+ CONN
R251 1 2 @ 0 0402 5% HDMI_TX1- CONN
R252 1 2 @ 0 0402 5% HDMI_TX2+ CONN
R253 1 2 @ 0 0402 5% HDMI_TX2- CONN

9/14 Modify for
UMA used

9/14 Reserve for VGA
used;check pin name

<16> HDMI_DETECT_VGA HDMI_DETECT_VGA

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Issued Date	2008/03/25	Deciphered Date	2008/04/

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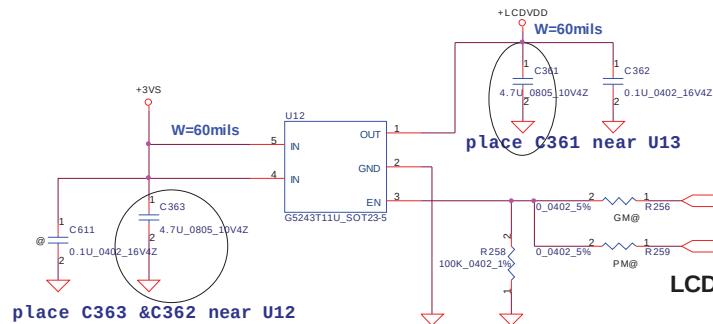
Compal Electronics, Ltd.

Level Shifter_PS8101T

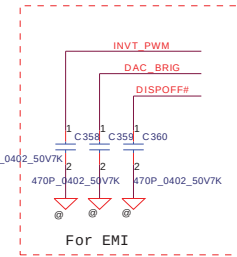
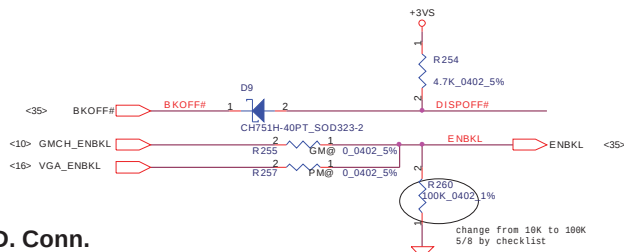
Size	Document Number	Rev
Cust	KIWB3/B4_LA4551P	0.1
Date	Friday, June 27, 2008	Sheet 22 of 49

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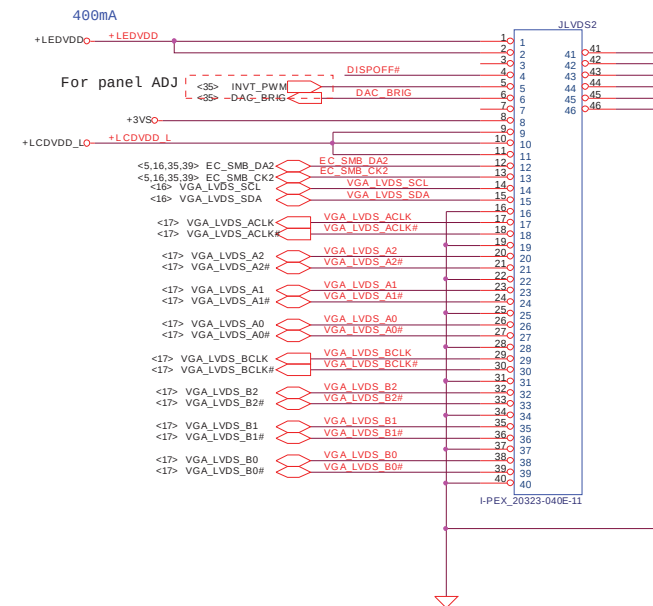
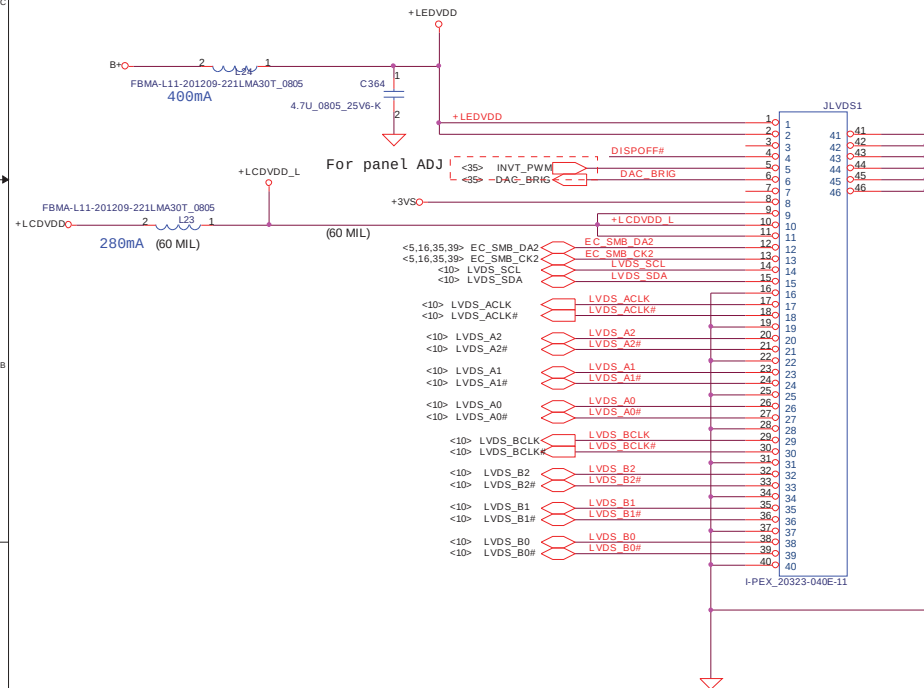
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.

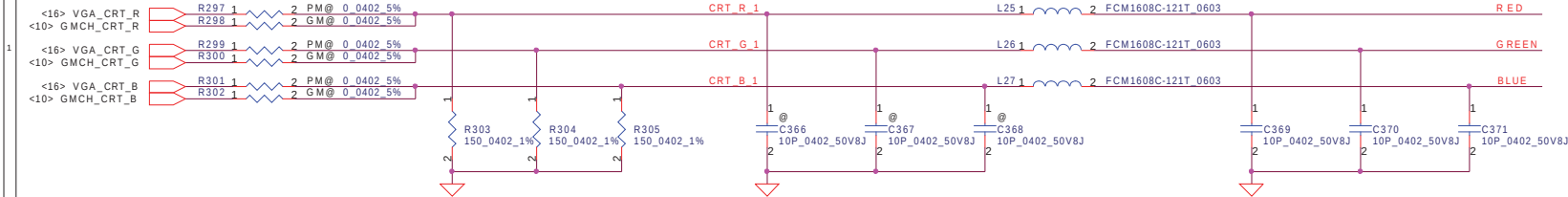


LCD/PANEL BD. Conn.

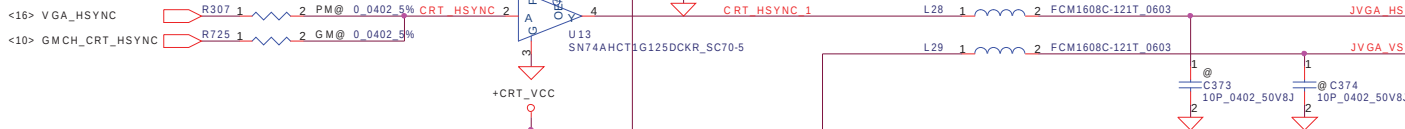


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Compal Electronics, Inc.				2008/10/15
LVDS & DVI Connector				2008/10/15
Size	Document Number	JITRI_LA-4141P		Rev 0.1
Date	Friday, June 27, 2008	Sheet	23	of 49

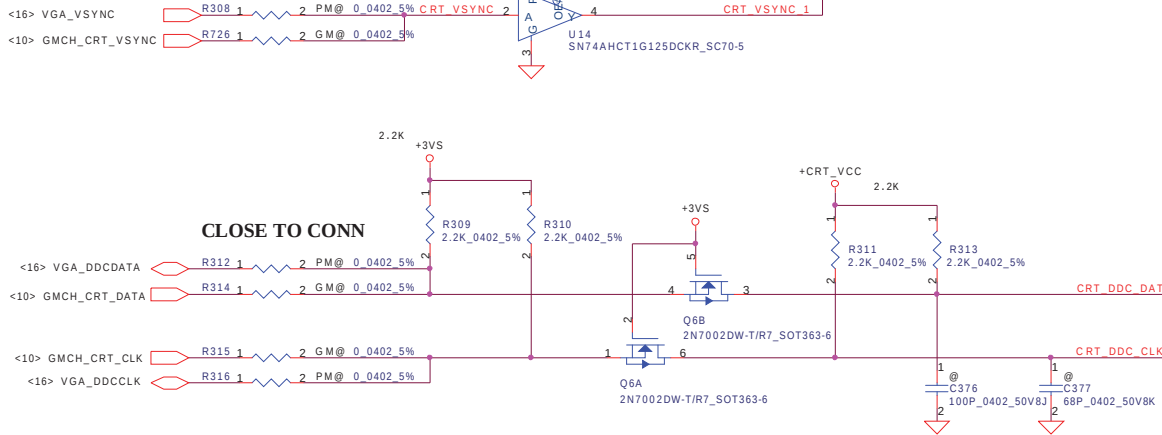
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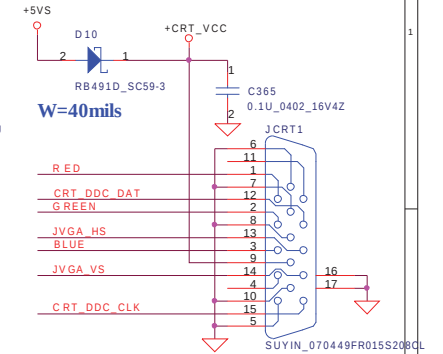
CLOSE TO CONN



CLOSE TO CONN

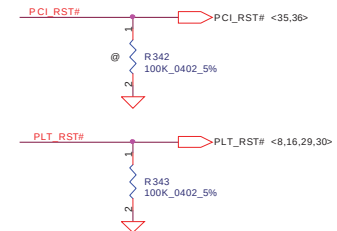
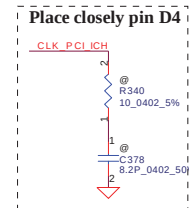
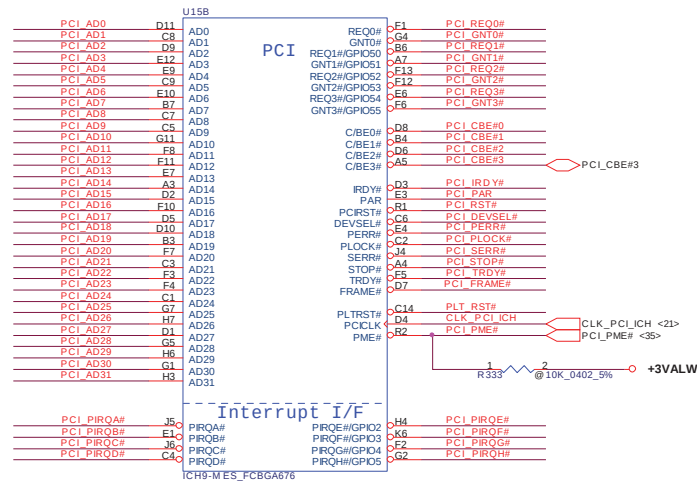
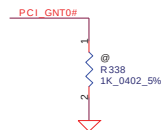
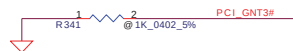
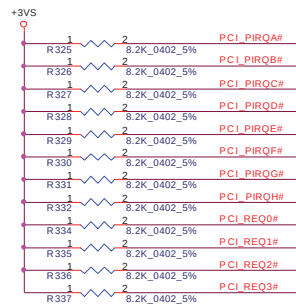
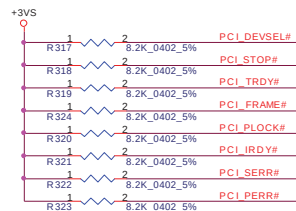


CRT Connector



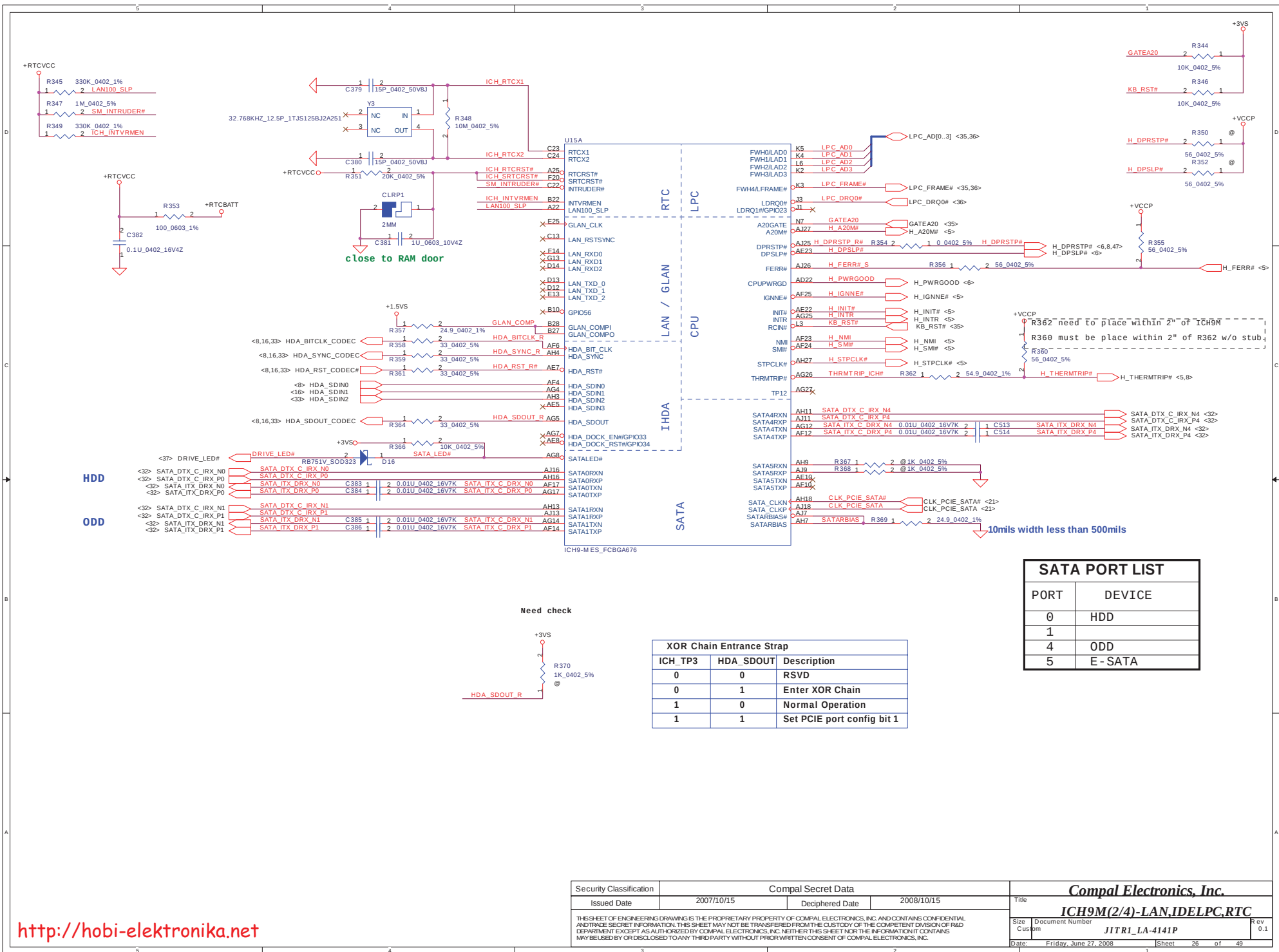
PIN ASSIGMENT

D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4



A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

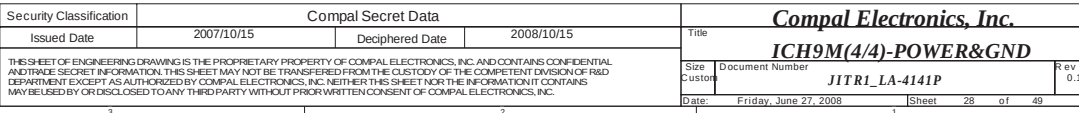
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

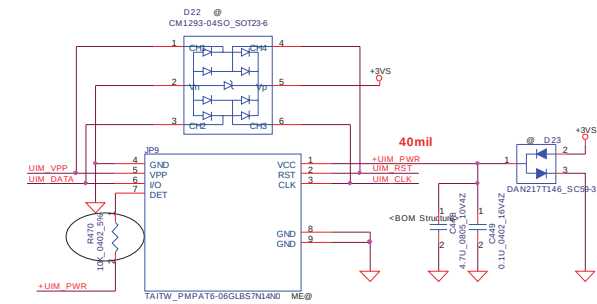
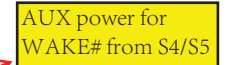


SATA PORT LIST	
PORT	DEVICE
0	HDD
1	
4	ODD
5	E-SATA

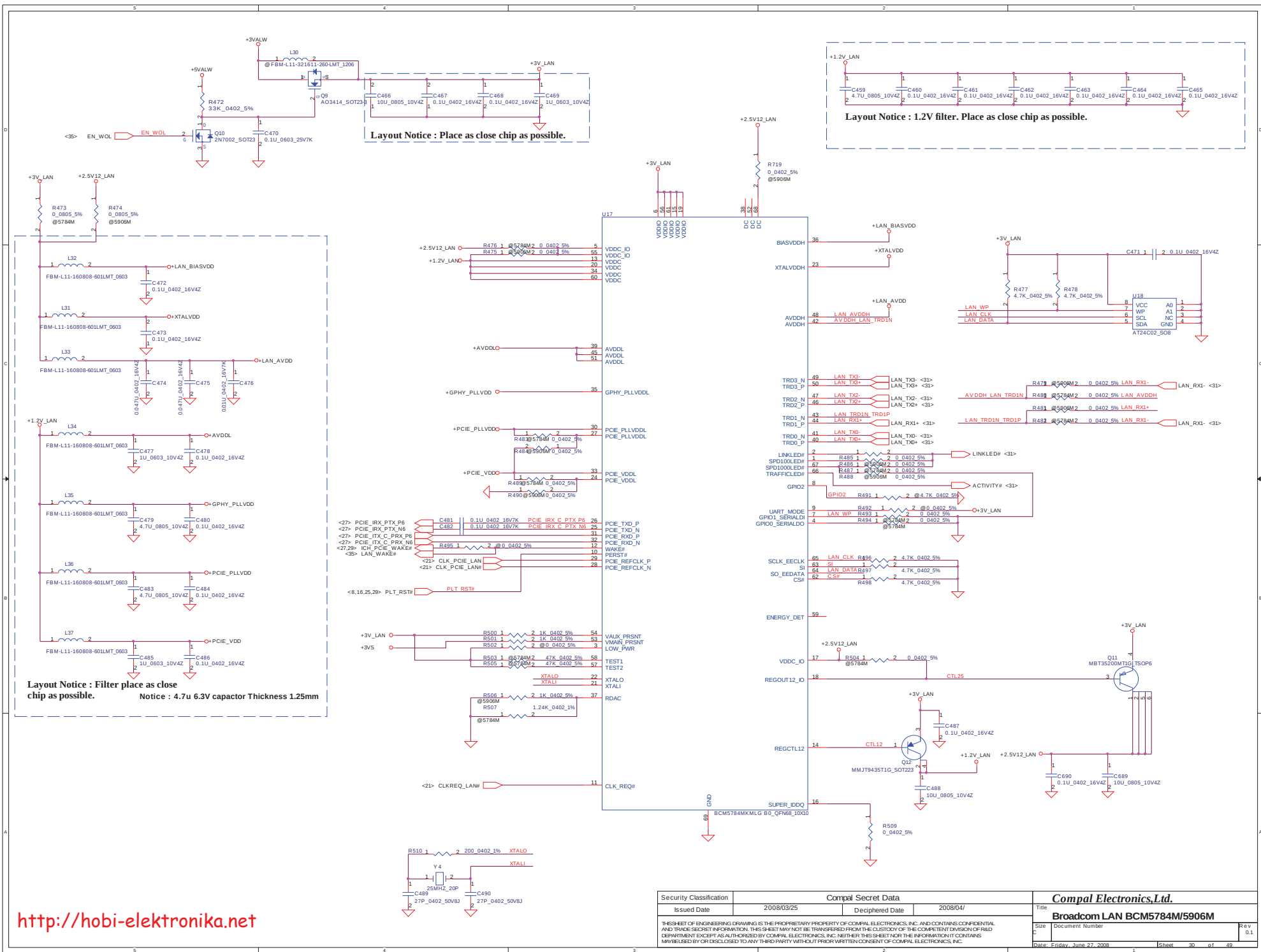
XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

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				Rev	
				0.1	
Date				Friday, June 27, 2008	
Sheet				26 of 49	

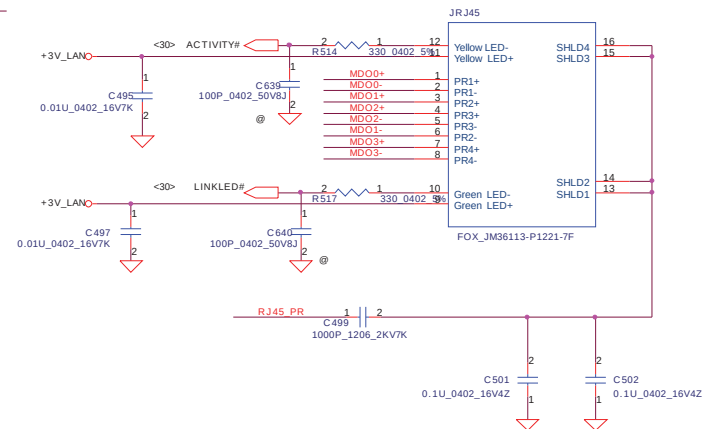


Mini-Express Card(Slot 1-TV TUNNER) 4.0mm high

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				Date:	Friday, June 27, 2008	Sheet 29 of 49

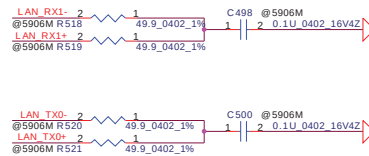


RJ45 CONN

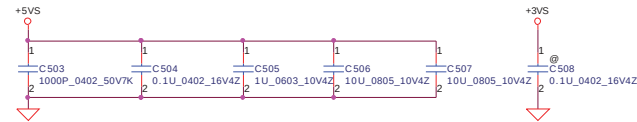


Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF

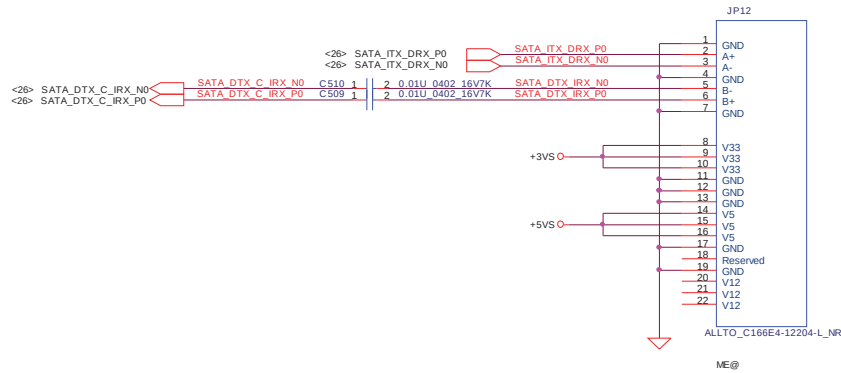
near LAN controller



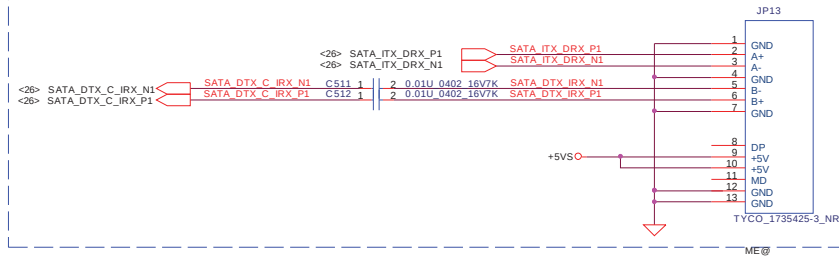
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title		
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				Size	Document Number	Rev
				Custom	JITR1_LA-4141P	0.1
				Date	Friday, June 27, 2008	Sheet 31 of 49



SATA HDD Conn.

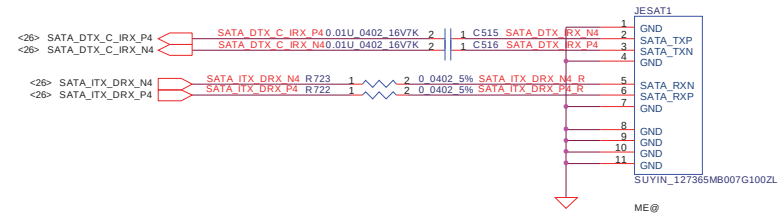


SATA ODD Conn.

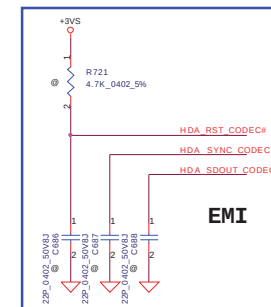
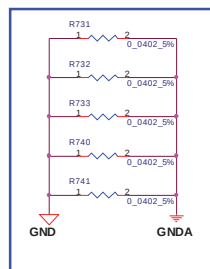
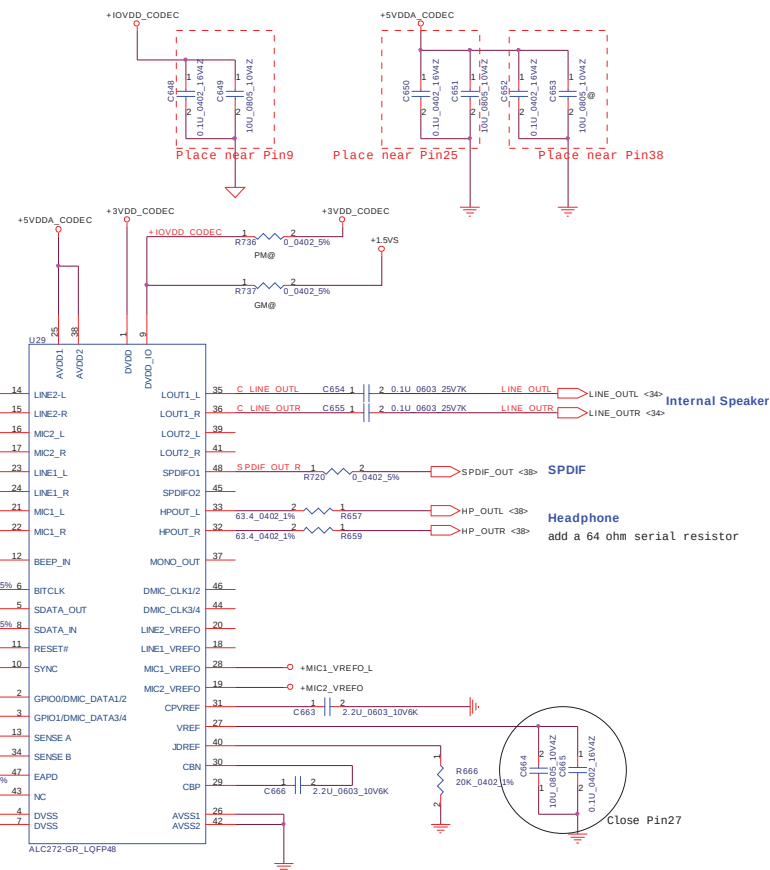
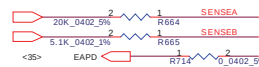
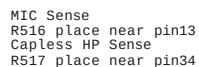
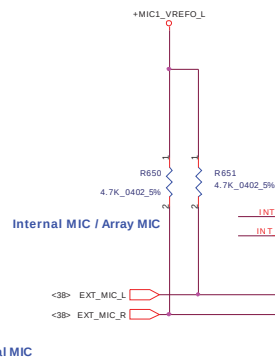
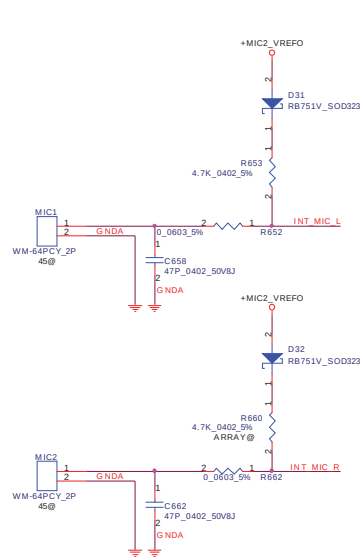


E-SATA Conn.

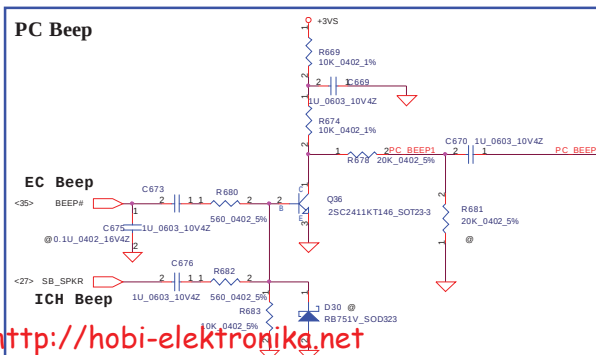
place R722&R723&C515&C516
near JESAT1



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				Document Number
				JITR1_LA-4141P
				Rev 0.1
				Date: Friday, June 27, 2008
				Sheet 32 of 49

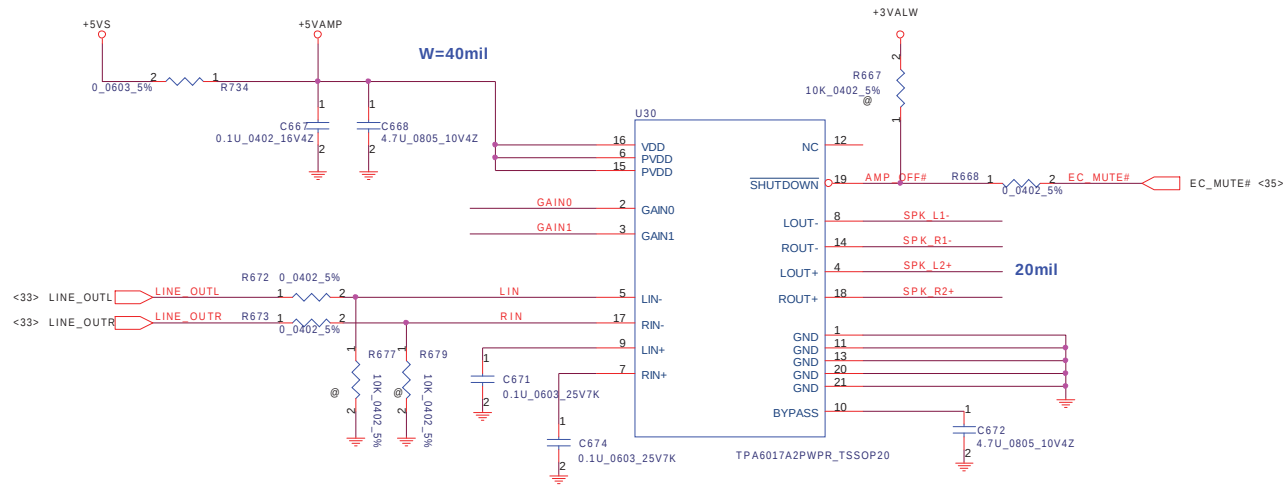


Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	Line in
MIC1(Pin21/22)	External	Mic in
MONO-OUT(Pin37)	Internal	Internal Subwoofer
MIC2(Pin16/17)	Internal	Internal Mic

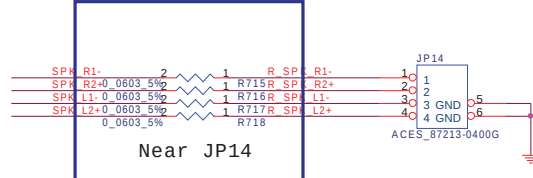
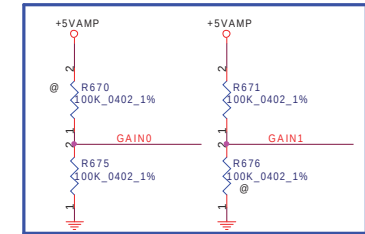


Security Classification	Compel Secret Data		Title	
Issued Date	2008/03/25	Deciphered Date	2008/04/	Compal Electronics, Ltd. HD Audio Codec ALC272 Document Form No. KIWB3/B4_L4_4551P
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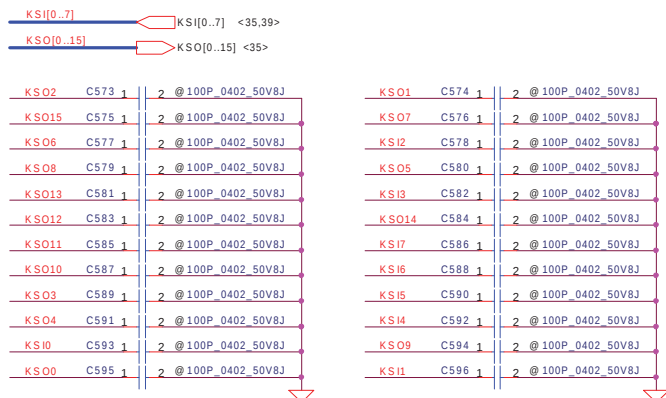
Speaker Connector



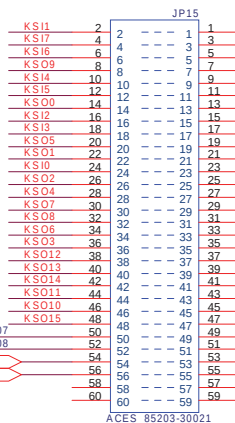
GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



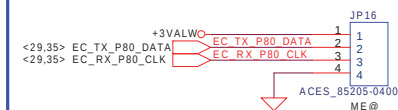
INT_KBD Conn.



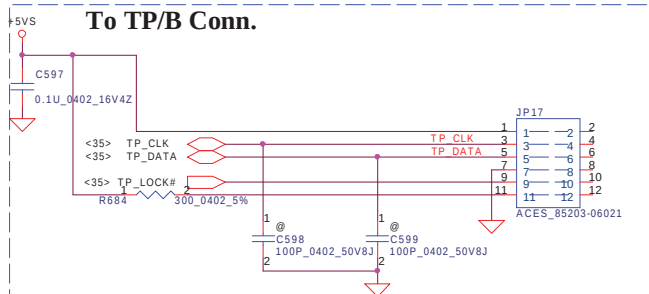
Source:SP01000IE00
2nd source:SP01000IF00
30 pin



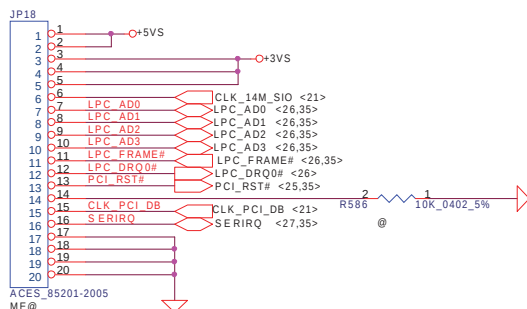
EC DEBUG PORT



To TP/B Conn.

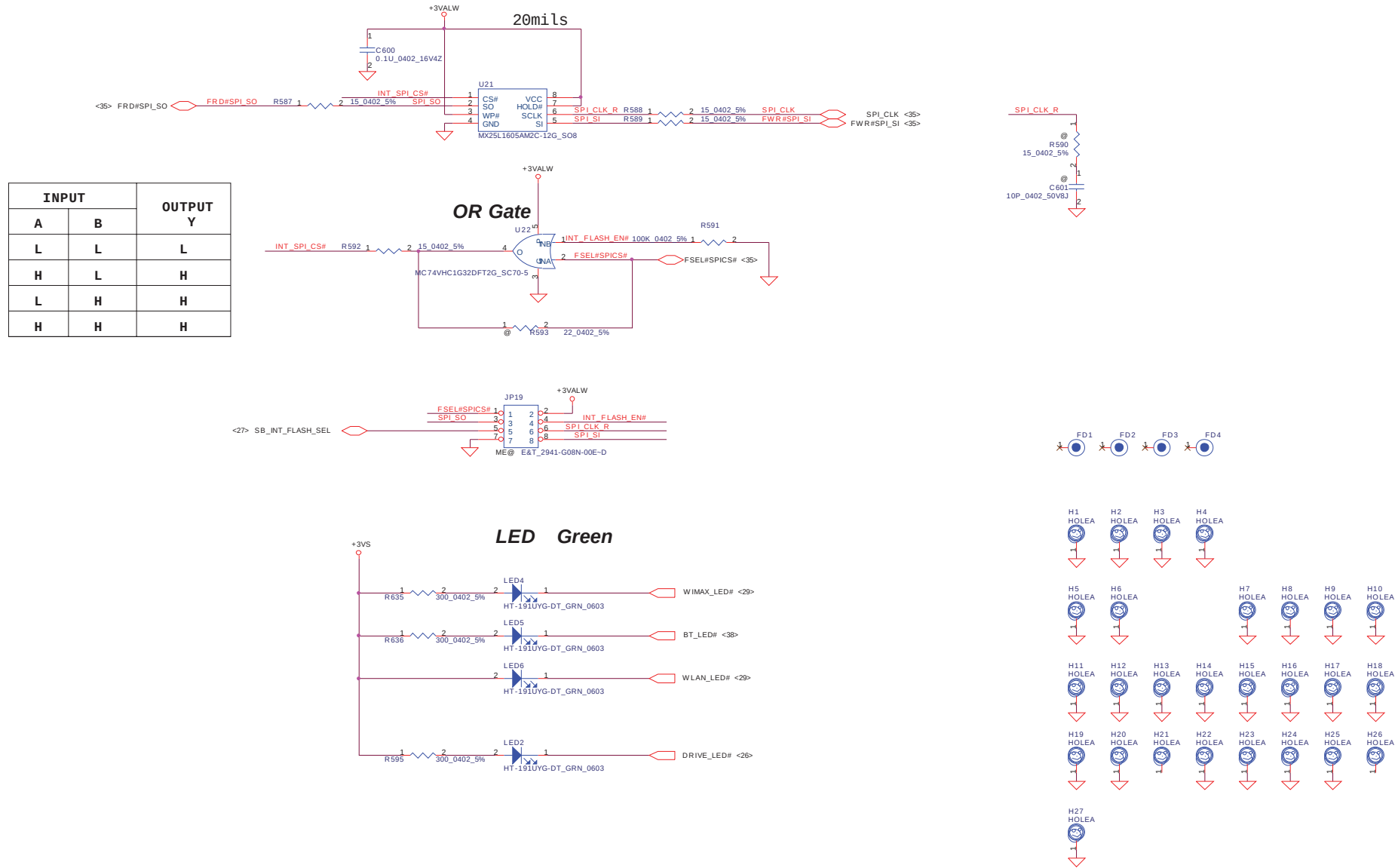


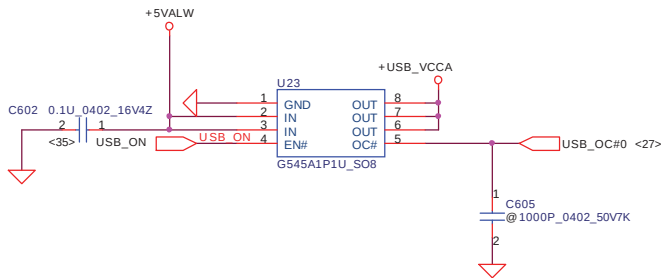
FOR LPC SIO DEBUG PORT



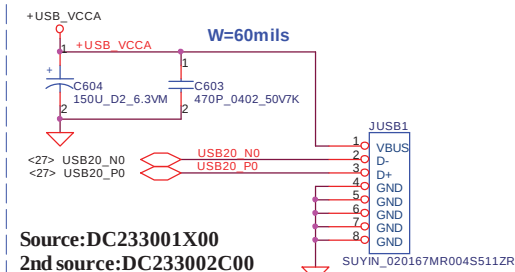
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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Size	Document Number	JITR1_LA-4141P		Rev	
Date:	Friday, June 27, 2008	Sheet	36	of	49

FOR EC 16M SPI ROM



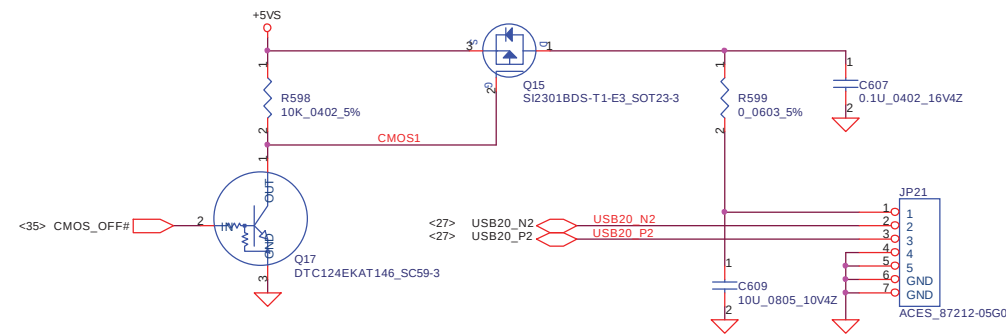


LIFT USB CONN. 1

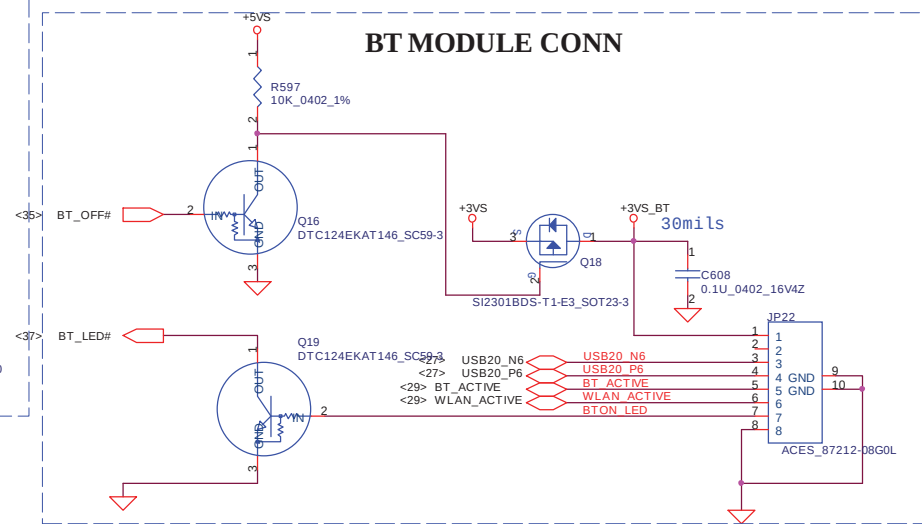


Source:DC233001X00
2nd source:DC233002C00

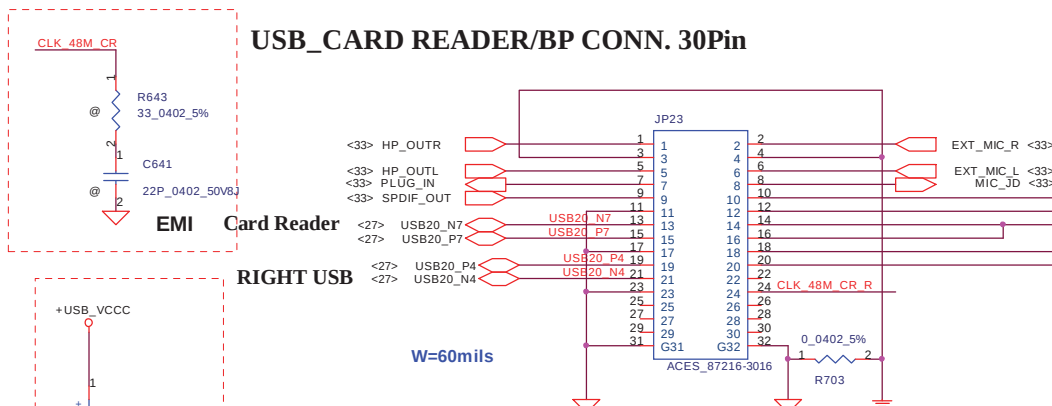
CMOS Camera Conn



BT MODULE CONN



USB_CARD READER/BP CONN. 30Pin



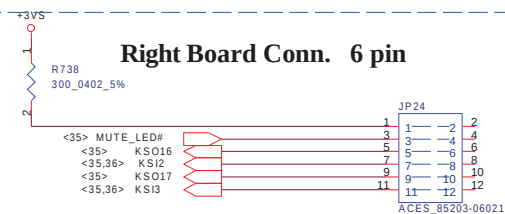
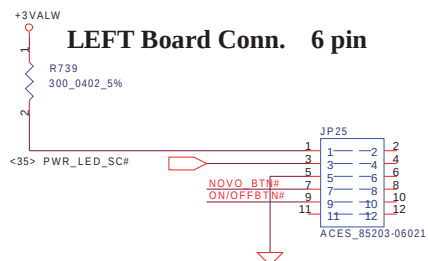
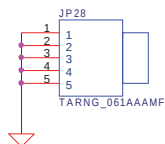
EMI Card Reader

RIGHT USB

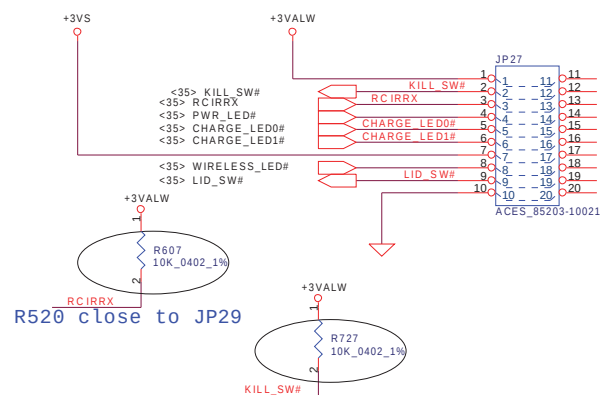
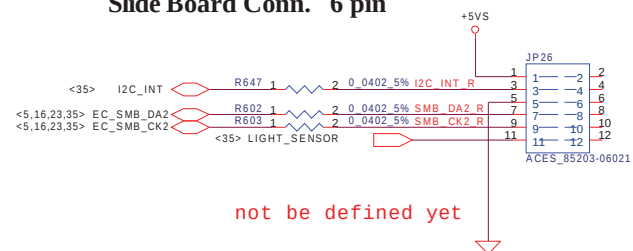
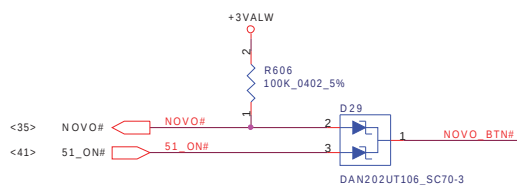
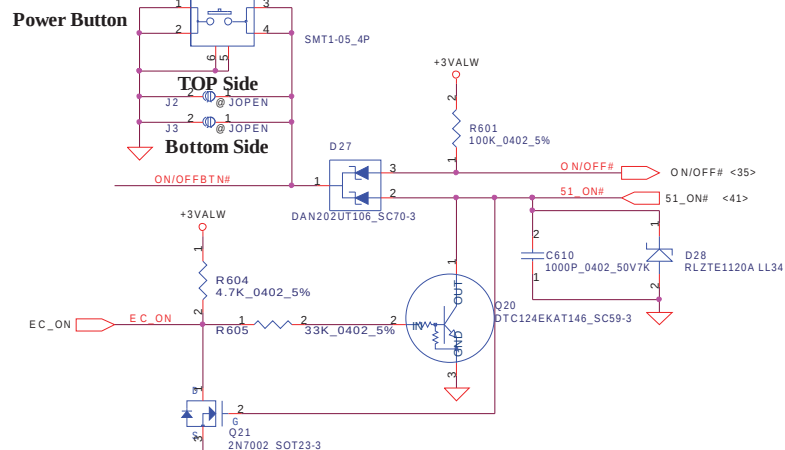
W=60mils

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Custom		KIWB3/B4 LA4551P		0.1	
Date:		Friday, June 27, 2008		Sheet 38 of 49	

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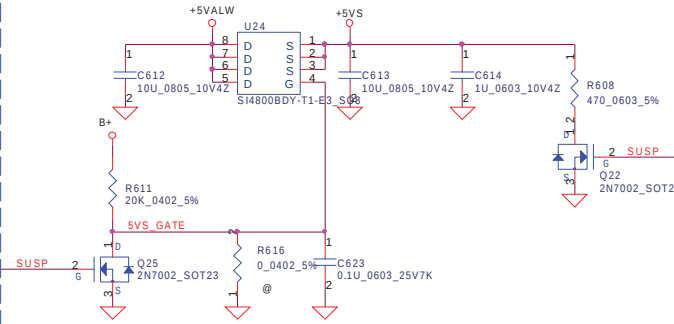


BTN FUNCTION	KEY MATRIX	
	IN	OUT
UP	KS016	KSI2
DOWN	KS017	KSI2
MUTE	KS017	KSI3

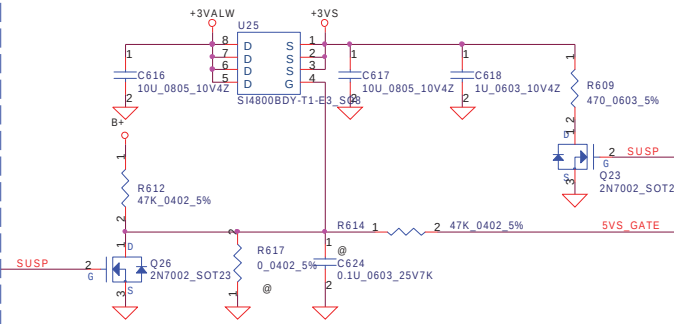


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				Date	Friday, June 22, 2008
				Sheet	30 of 48

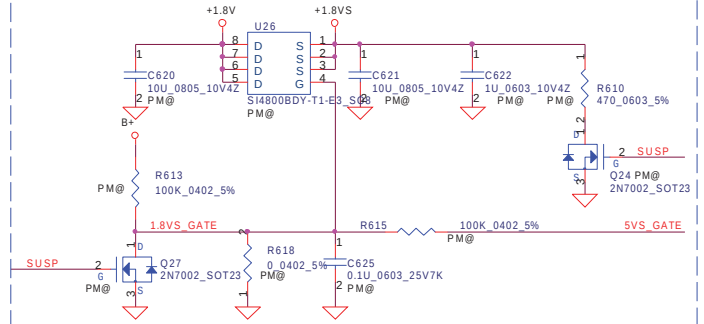
+5VALW TO +5VS



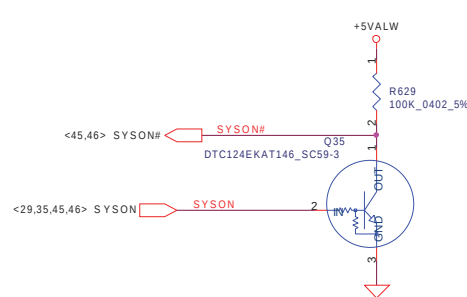
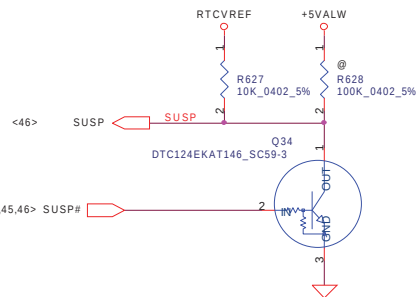
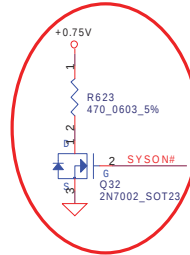
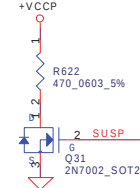
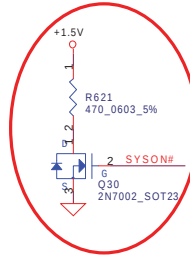
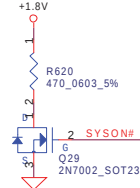
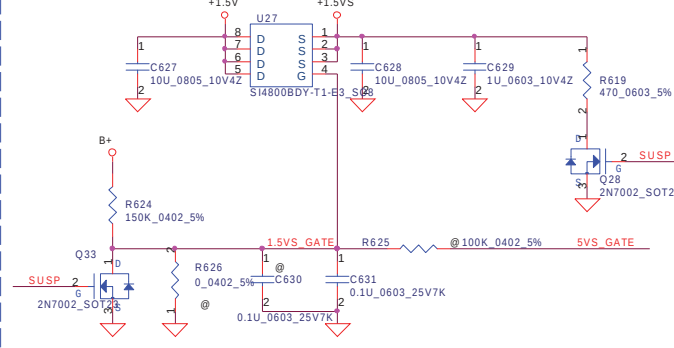
+3VALW TO +3VS



+1.8V to +1.8VS

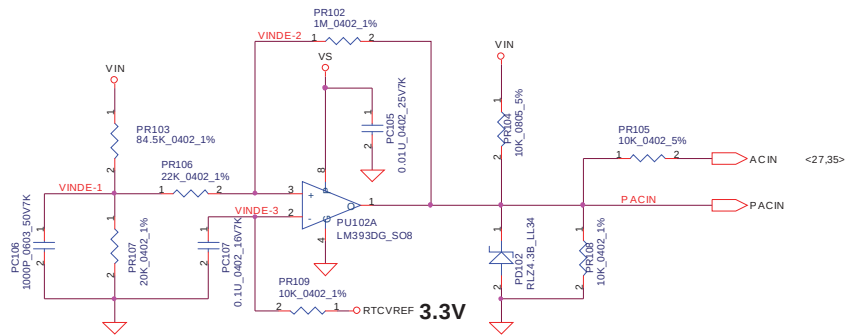
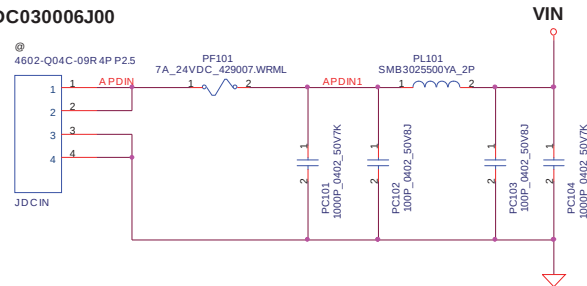


+1.5V to +1.5VS



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				Custom	KIWB3/B4_LA4551P
				Date	Friday, June 27, 2008
				Sheet	40 of 49
				Rev	0.1

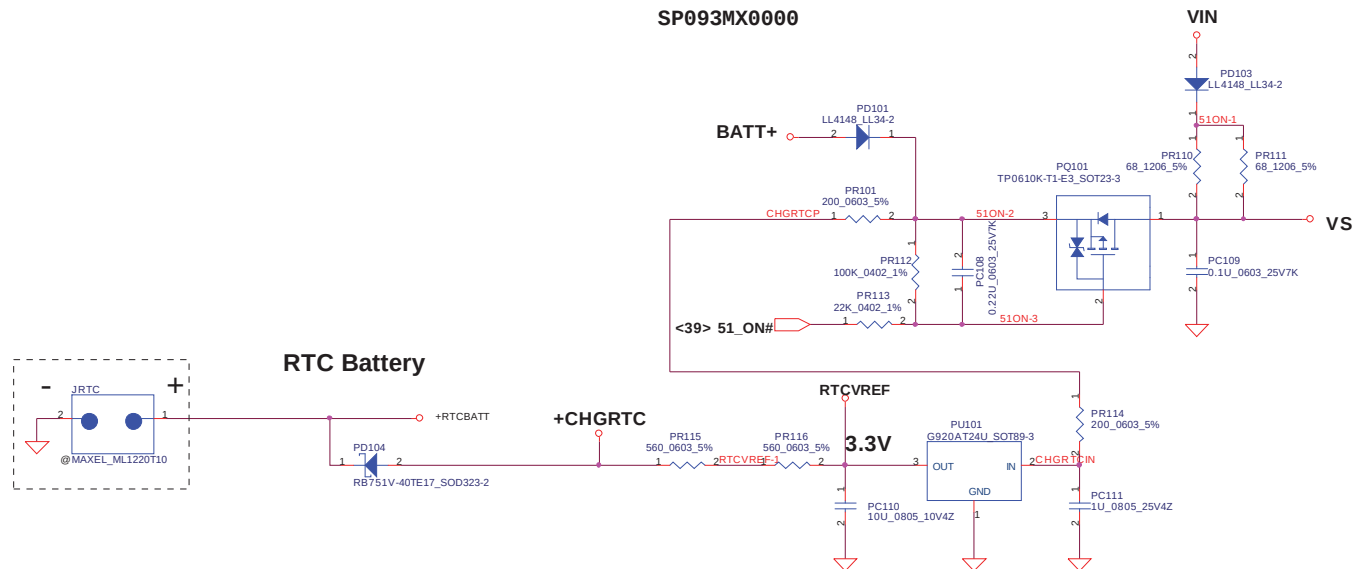
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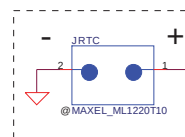
Vin Detector

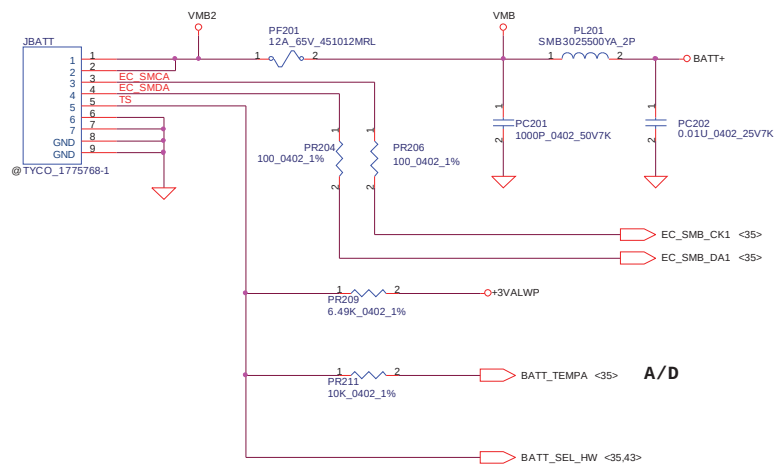
High 18.384 17.901 17.430
Low 17.728 17.257 16.976

SP093MX0000

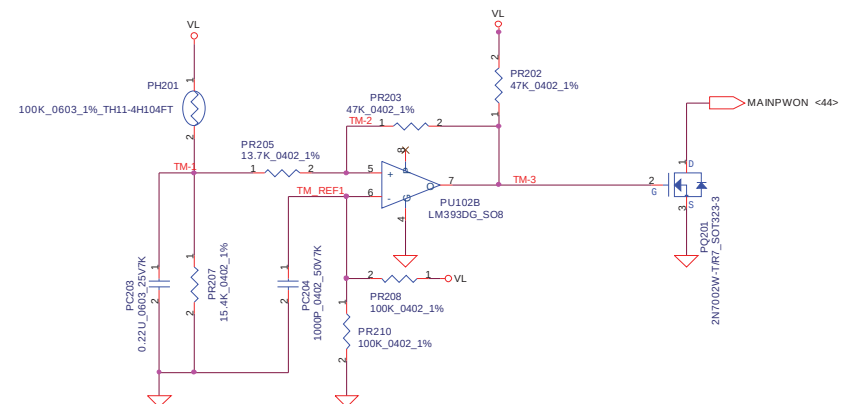


RTC Battery

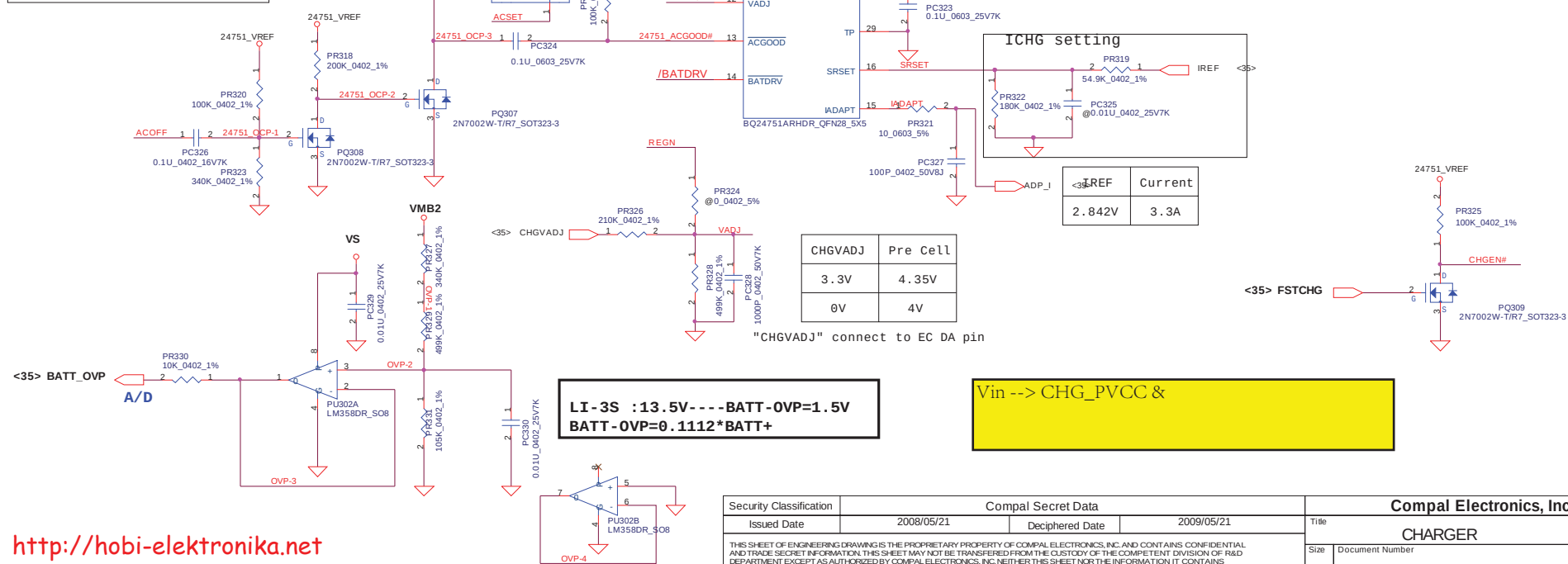
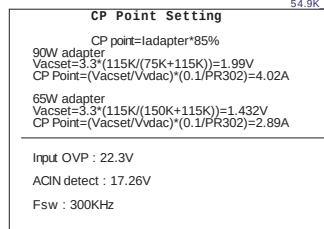




PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



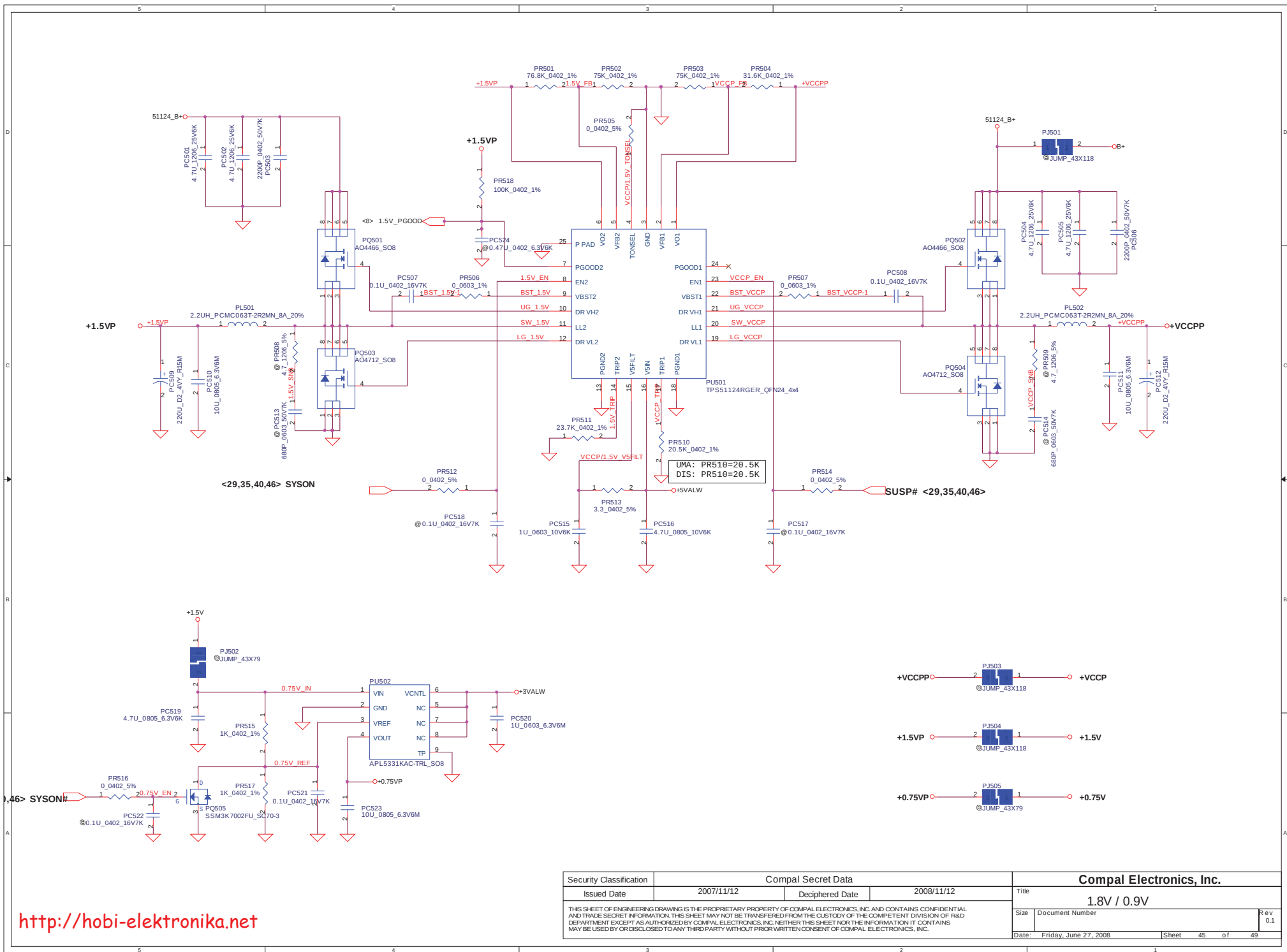
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2. BATT_OVP
 BATT_CELL
 CHG_VOLT
 CHG_CURT
 BATT_LEARN
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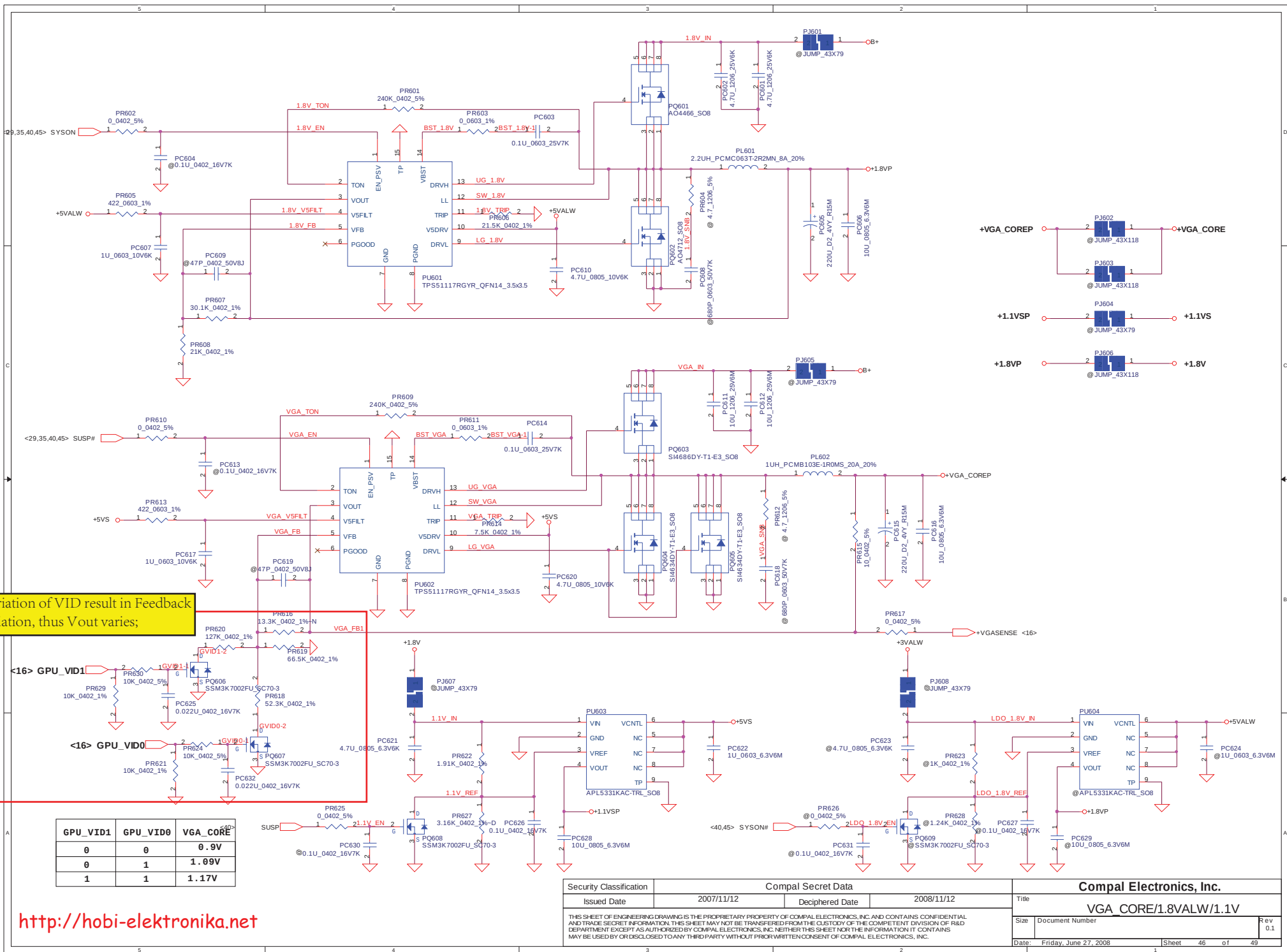


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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            |                          |                       |                |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            | Date:                    | Fridav, June 27, 2008 | Sheet 43 of 49 |









## Version change list (P.I.R. List)

Page 1 of 2  
for PWR

| Item | Fixed Issue | Reason for change | Rev. | PG#                  | Modify List                                                                                                                                                                                                                                                                                                                                                                            | Date | Phase |
|------|-------------|-------------------|------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|
| 1    |             | Schematic modify  | 0.1  | 41<br>43<br>46<br>47 | Add PR334, PR861, PR862, PR863, PR864<br>Canel PH802<br>Change PR841, PR846 to 0ohm<br>Change PC831 to 10U<br>Change PR840, PR850 to 194K<br>Change PR801, PR848 to 15.4K<br>Change PR842, PR851 to 28.7K<br>Change PC106 to 1000P<br>Change PC829, PC835 to 0.022U<br>Change PR622 to 1.91K<br>Change PR627 to 3.16K<br>Change PR628 to 1.24K<br>PU401 main source change to TPS51427 |      | EVT   |
| 2    |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 3    |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 4    |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 5    |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 6    |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 7    |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 8    |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 9    |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 10   |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 11   |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 12   |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 13   |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 14   |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 15   |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 16   |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 17   |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 18   |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 19   |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 20   |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |
| 21   |             |                   |      |                      |                                                                                                                                                                                                                                                                                                                                                                                        |      |       |

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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            |                          |                       |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Date                     | Friday, June 27, 2008 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Sheet                    | 48 of 49              |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Rev                      | 0.1                   |

| 5           | 4    | 3    | 2                 | 1       |
|-------------|------|------|-------------------|---------|
| NO          | DATE | PAGE | MODIFICATION LIST | PURPOSE |
| <div></div> |      |      |                   |         |

D

C

B

A

|       |  |  |                                 |  |  |
|-------|--|--|---------------------------------|--|--|
| Title |  |  | <b>Compal Electronics, Inc.</b> |  |  |
| Size  |  |  | Document Number                 |  |  |
| B     |  |  | KIWB3/B4_LA4551P                |  |  |
| Date: |  |  | Friday, June 27, 2008           |  |  |
| Sheet |  |  | 49 of 49                        |  |  |
| 1     |  |  |                                 |  |  |