

Compal confidential

Schematics Document

Mobile P4 uFCBGA/uFCPGA with INTEL
MONTARA-GML/ICH4-M core logic

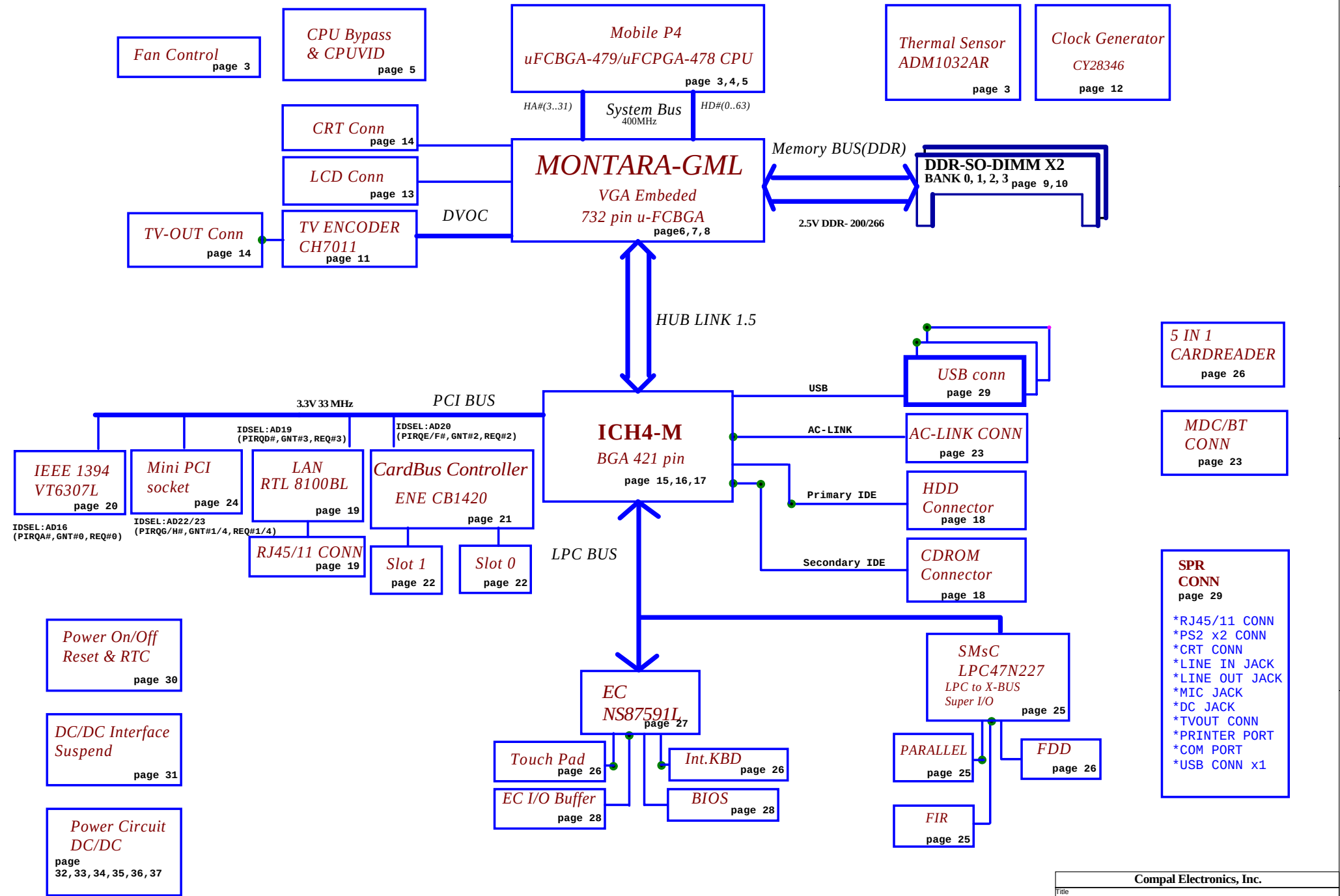
2002-02-10

REV:1.0

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SCHEMATIC M/B LA-1571		
Size	Document Number	Rev
	401238	3B
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File Name : LA-1571

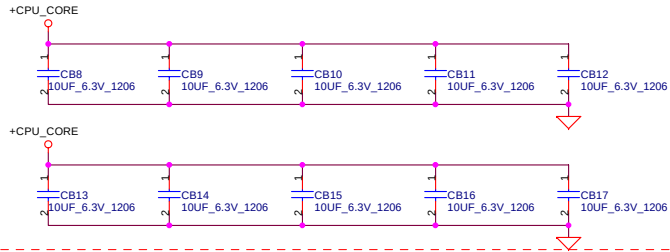


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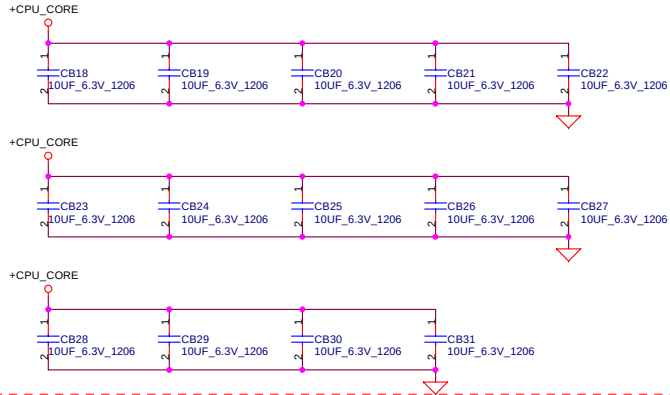
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	401238	1.0	
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Layout note :
Place close to CPU. Use 2~3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

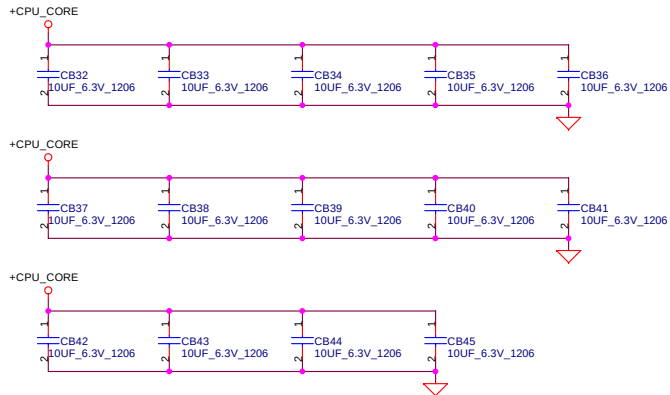
Please place these cap in the socket cavity area



Please place these cap on the socket north side

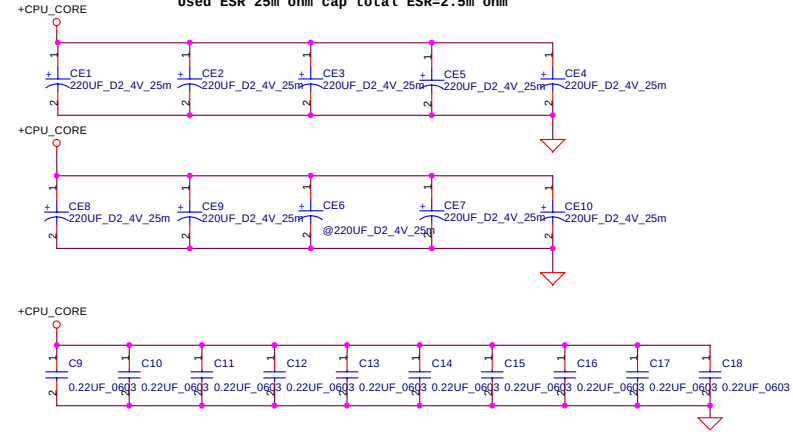


Please place these cap on the socket south side



Layout note :
Place close to CPU power and
ground pin as possible
(<1inch)

Used ESR 25m ohm cap total ESR=2.5m ohm



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DDR SMA0 AC18C
DDR SMA1 AD14C
DDR SMA2 AD13C
DDR SMA3 AD17C
DDR SMA4 AD11C
DDR SMA5 AC13C
DDR SMA6 AD8C
DDR SMA7 AD7C
DDR SMA8 AC6C
DDR SMA9 AC5C
DDR SMA10 AC19C
DDR SMA11 AD5C
DDR SMA12 AB8C

DDR SDO59 AG2
DDR SDO51 AH5
DDR SDO52 AH8
DDR SDO53 AC9
DDR SDO54 AH17
DDR SDO55 AE21
DDR SDO56 AH24
DDR SDO57 AH27
AD15

DDR SWE# AD25C
DDR SRAS# AC21C
DDR SCAS# AC24C

9 DDR_CLK0 AB2
9 DDR_CLK0# AC28C
9 DDR_CLK1 AB25C
9 DDR_CLK1# AC3C
9 DDR_CLK3 AC2
9 DDR_CLK3# AD2C
9 DDR_CLK4 AB23C
9 DDR_CLK4# AB24C
9 DDR_CLK4# AA3
9 DDR_CLK4# AB4C

9.10 DDR_CKE0 AC7
9.10 DDR_CKE1 AB1
9.10 DDR_CKE2 AC9
9.10 DDR_CKE3 AC10
9.10 DDR_CKE4 AD23C
9.10 DDR_CKE5 AC28C
9.10 DDR_CKE6 AC22C
9.10 DDR_CKE7 AC25C
9.10 DDR_CKE8 AC25C

DDR SBO0 AD22
DDR SBO1 AD20

DDR SDO0 AE8
DDR SDO1 AE9
DDR SDO2 AE12
DDR SDO3 AH12
DDR SDO4 AD19
DDR SDO5 AD21
DDR SDO6 AD24
DDR SDO7 AH28
AH15

DDR SMA B1 AD16
DDR SMA B2 AC12
DDR SMA B4 AF11
DDR SMA B5 AD10

AC15C RCVENOUT#
AC16C RCVENIN#
MRCOMP AB1
MVSWINGL AJ22
MVSWINGH AJ19C

Montara-GM(L)

MEMORY

SDQ0
SDQ1
SDQ2
SDQ3
SDQ4
SDQ5
SDQ6
SDQ7
SDQ8
SDQ9
SDQ10
SDQ11
SDQ12
SDQ13
SDQ14
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SDQ66
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AG14
AE14
AE17
AG16
AH14
AE15
AE16
AE17

SMVREF0

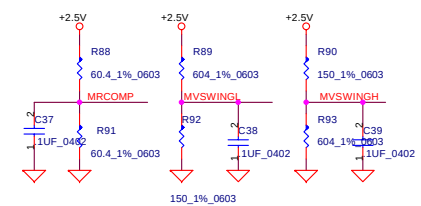
A324

C36

1UF_0402

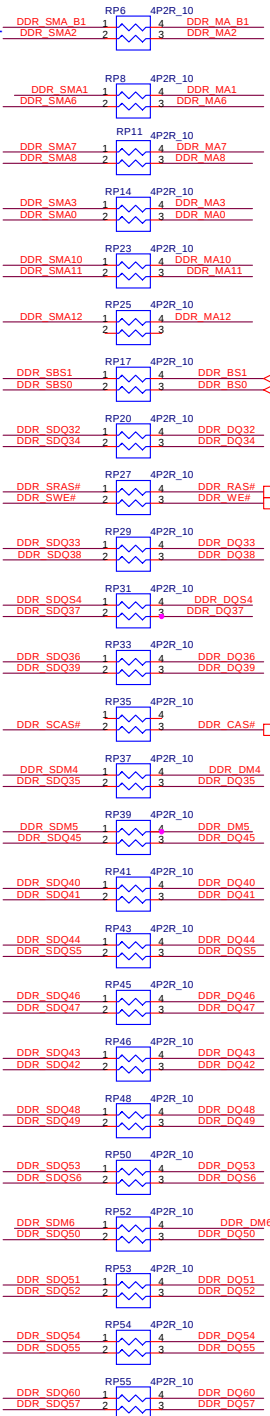
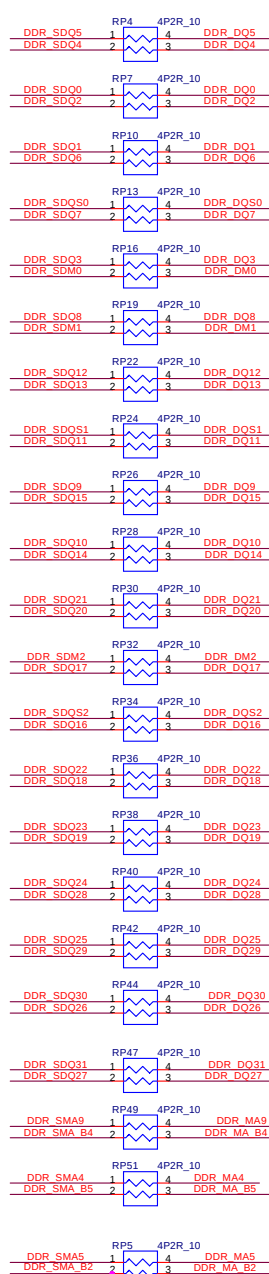
SDREF

DDR REF & SWING VOLTAGE



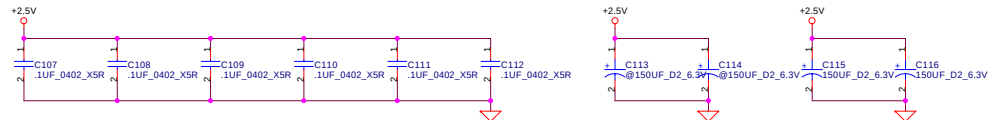
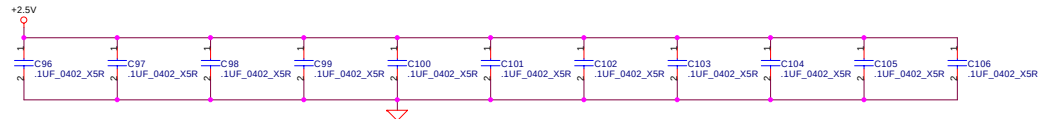
Layout note

Place these resistor
closely DIMM0,
all trace length
Max=0.75"

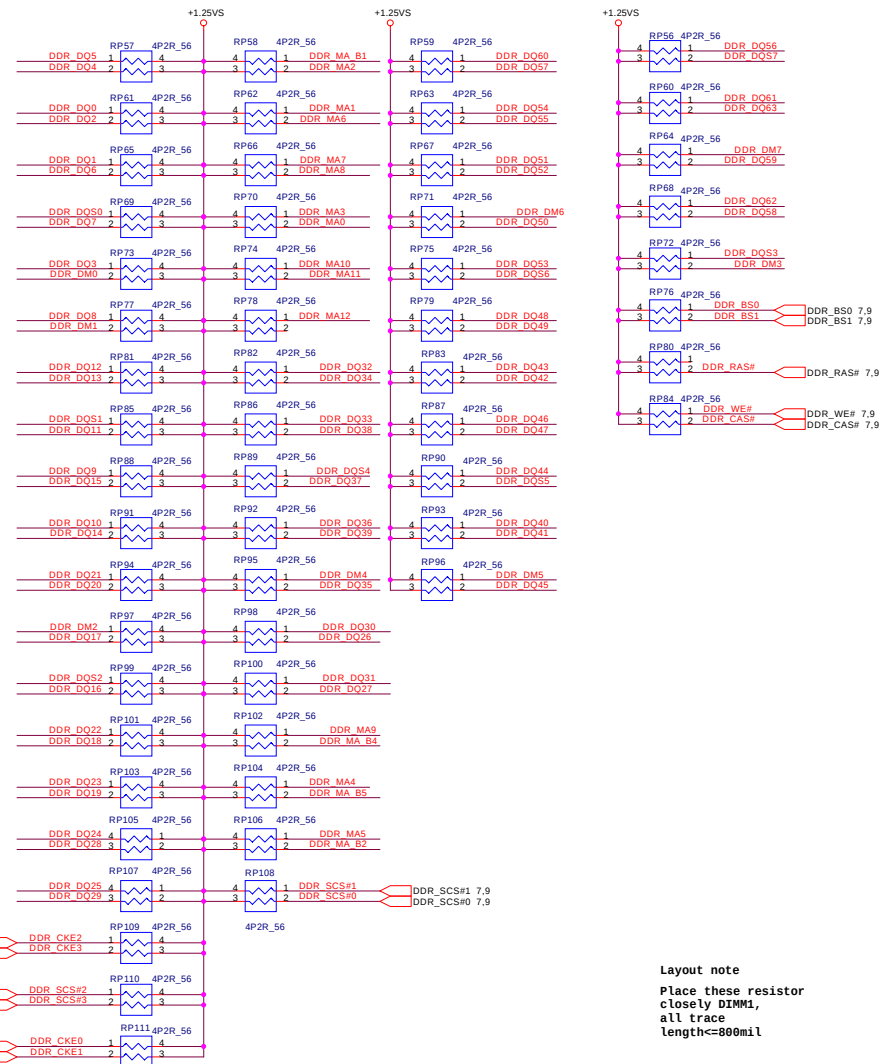
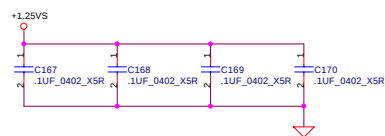
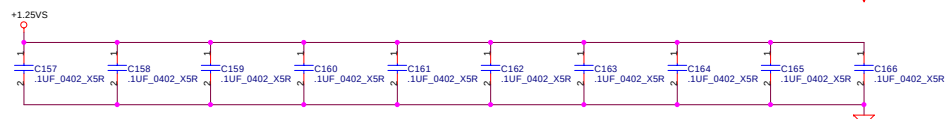
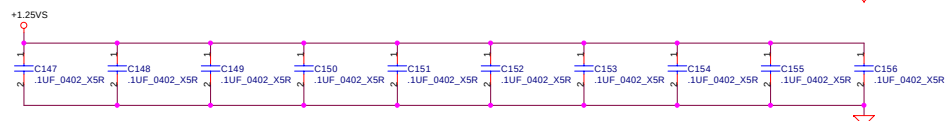
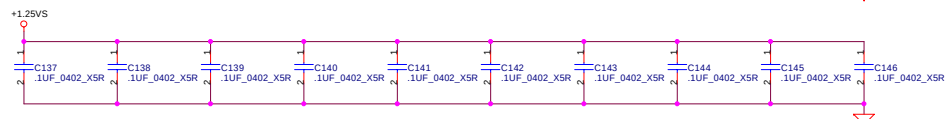
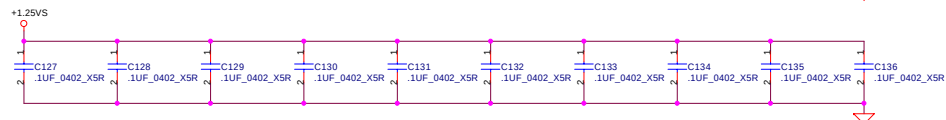
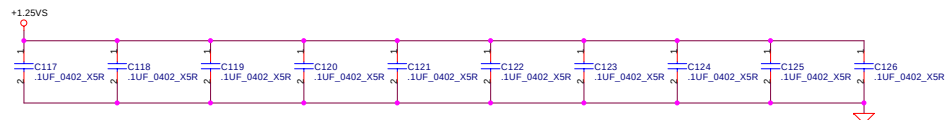


DDR_DM[0..7] 9.10
DDR_DQ[0..63] 9.10
DDR_DQS[0..8] 9.10
DDR_MA[0..12] 9.10
DDR_MA_B1[1..2] 9.10
DDR_MA_B4[4..5] 9.10

Layout note:
Distribute as close as possible
to DDR-SODIMM.

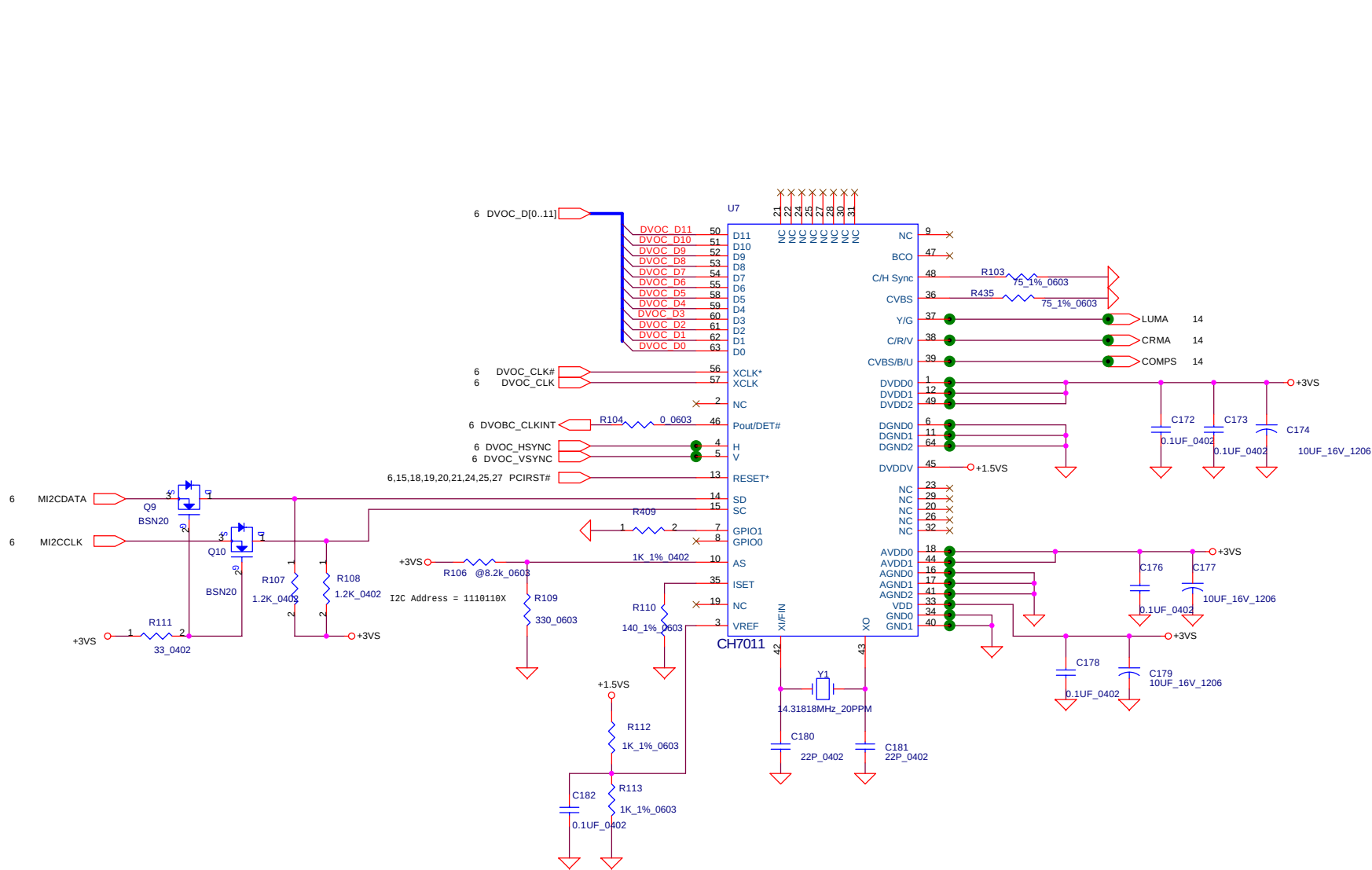


Layout note:
Place one cap close to every 2 pull up resistors termination to
+1.25V



Layout note
Place these resistor
closely DIMM1,
all trace
length<=800mil

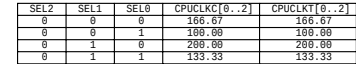
DDR_DM[0..8] DDR_DM[0..8] 7.9
DDR_DQ[0..63] DDR_DQ[0..63] 7.9
DDR_DQS[0..8] DDR_DQS[0..8] 7.9
DDR_MA[0..12] DDR_MA[0..12] 7.9
DDR_MA_B[1..2] DDR_MA_B[1..2] 7.9
DDR_MA_B[4..5] DDR_MA_B[4..5] 7.9



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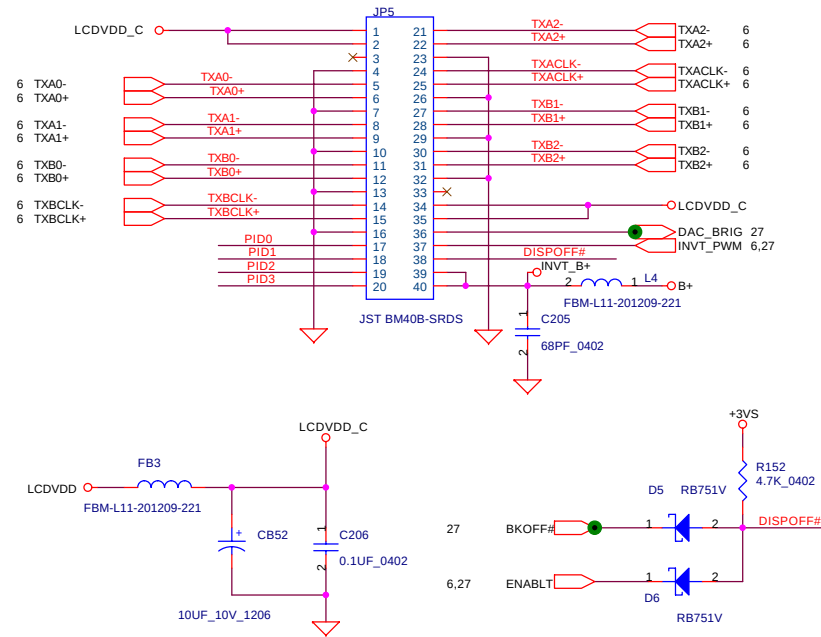
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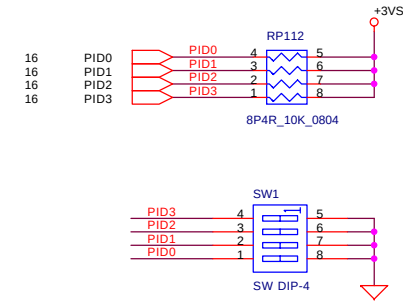
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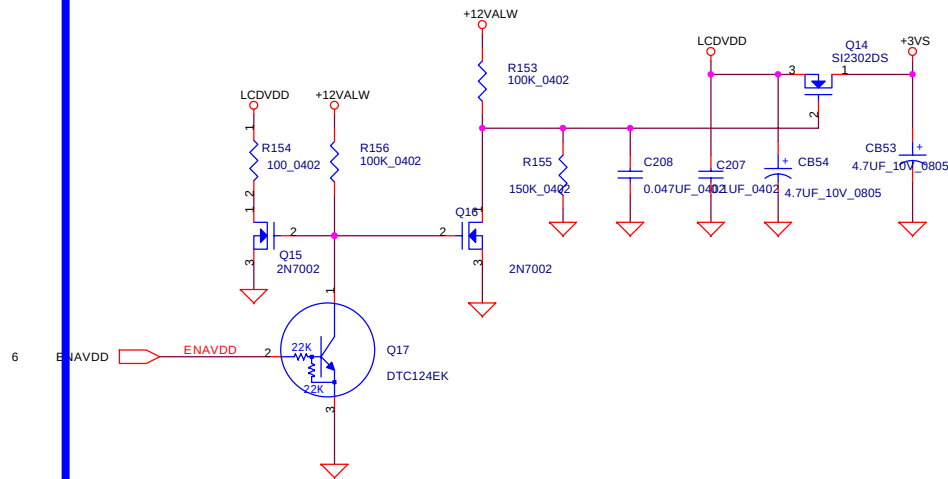
LCD CONN



PANEL ID switch



LCD POWER CIRCUIT



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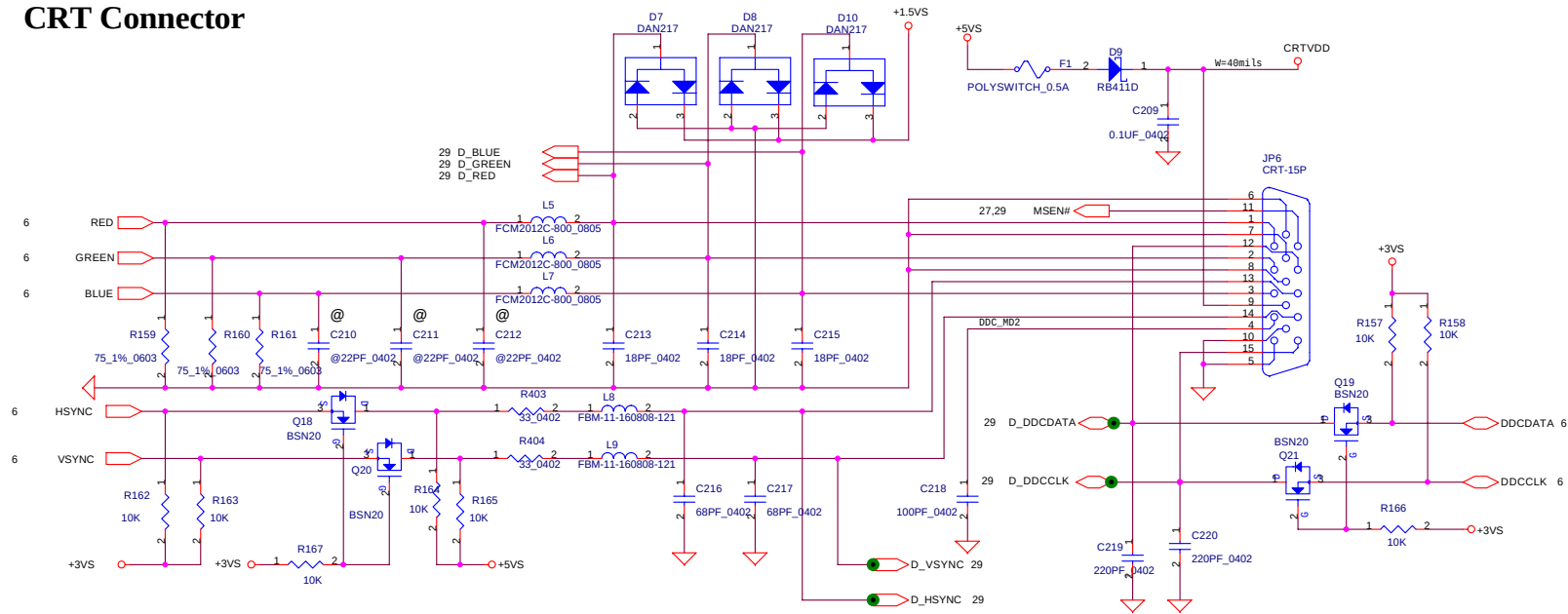
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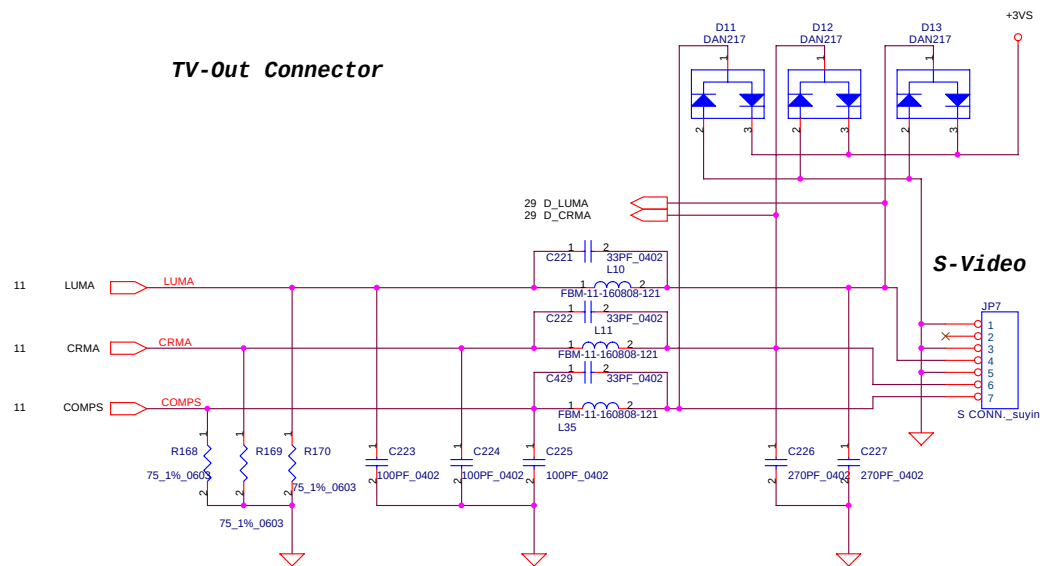
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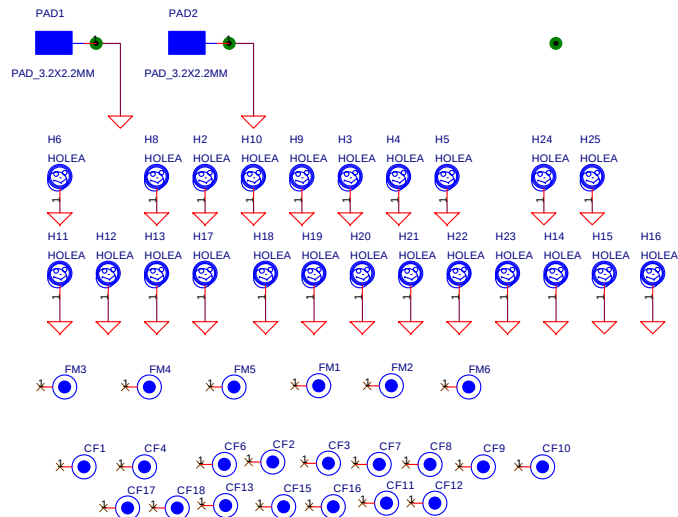
CRT Connector



TV-Out Connector



S-Video



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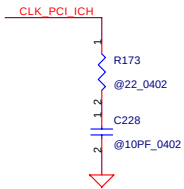
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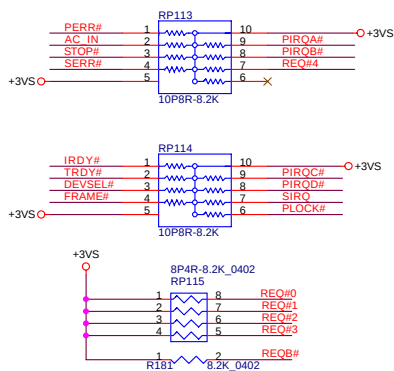
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PCI Pullups



19,20,21,24 AD[0..31] AD[0..31]

19,20,21,24 CBE#0 C/BE#0 B1C REQ#0 B1C REQ#0 B1C
19,20,21,24 CBE#1 C/BE#1 K4C REQ#1 A2C REQ#1 A2C
19,20,21,24 CBE#2 C/BE#2 M4C REQ#2 B3C REQ#2 B3C
19,20,21,24 CBE#3 C/BE#3 N4C REQ#3 C7C REQ#3 C7C
20 REQ#0 REQ#0 B1C REQ#0 B1C REQ#0 B1C
24 REQ#1 REQ#1 A2C REQ#1 A2C REQ#1 A2C
21 REQ#2 REQ#2 B3C REQ#2 B3C REQ#2 B3C
19 REQ#3 REQ#3 C7C REQ#3 C7C REQ#3 C7C
24 REQ#4 REQ#4 B6C REQ#4 B6C REQ#4 B6C
20 GNT#0 GNT#0 C1C GNT#0 C1C GNT#0 C1C
24 GNT#1 GNT#1 E6C GNT#1 E6C GNT#1 E6C
21 GNT#2 GNT#2 A7C GNT#2 A7C GNT#2 A7C
19 GNT#3 GNT#3 D6C GNT#3 D6C GNT#3 D6C
24 GNT#4 GNT#4 D6C GNT#4 D6C GNT#4 D6C
12 CLK_PCI_ICH CLK_PCI_ICH P5C PCICLK
19,20,21,24 FRAME# FRAME# F1C FRAME# F1C FRAME# F1C
19,20,21,24 DEVSEL# DEVSEL# M3C DEVSEL# M3C DEVSEL# M3C
19,20,21,24 IRDY# IRDY# G1C IRDY# G1C IRDY# G1C
19,20,21,24 PAR PAR L4C PAR L4C PAR L4C
19,20,21,24 PERR# PERR# M2C LOCK# M2C LOCK# M2C
19,21,24 SERR# SERR# K5C PCIRST# K5C PCIRST# K5C
19,20,21,24 STOP# STOP# F3C STOP# F3C STOP# F3C
19,20,21,24 TRDY# TRDY# F2C TRDY# F2C TRDY# F2C
27,32,35 ACIN ACIN B5C REQ#4/GPIO REQ#4/GPIO REQ#4/GPIO
18 PDD_RST# PDD_RST# A6C REQ#5/GPIO REQ#5/GPIO REQ#5/GPIO
18 SDD_RST# SDD_RST# E8C GNT#4/GPIO16 GNT#4/GPIO16 GNT#4/GPIO16
18 GNT#5/GPIO17 GNT#5/GPIO17 GNT#5/GPIO17

ICH4-M

SM I/F

CPU I/F

HUB I/F

Interrupt I/F

EEPROM I/F

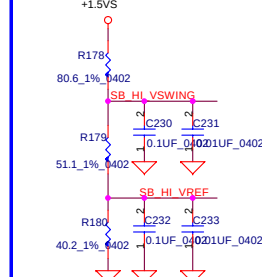
LAN I/F

ICH4-M

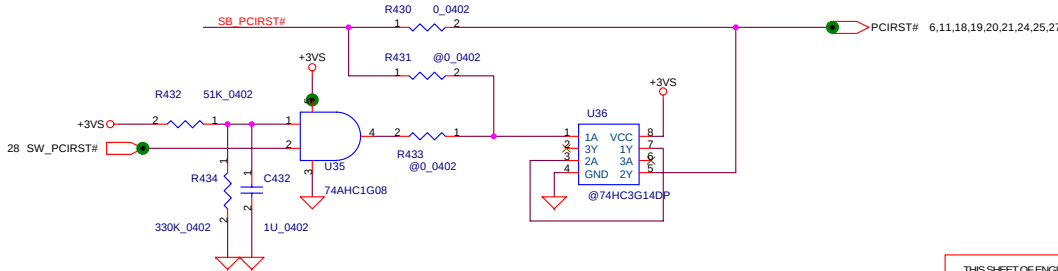
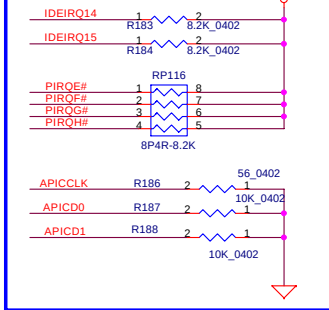
SM BUS



HL REF & SWING VOLTAGE

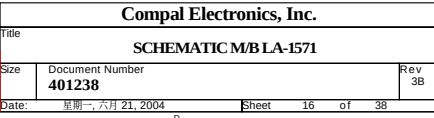


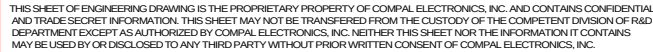
INT I/F



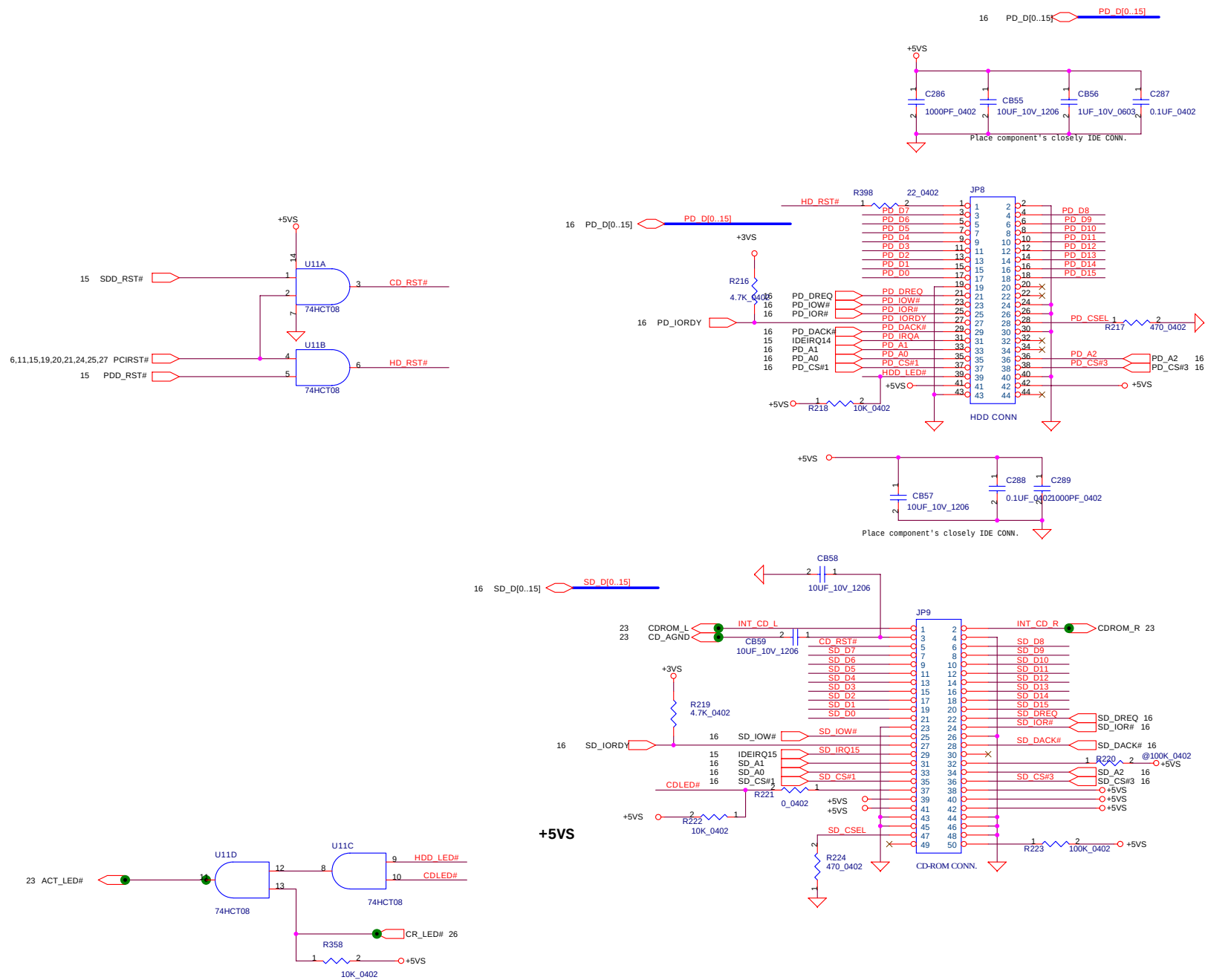
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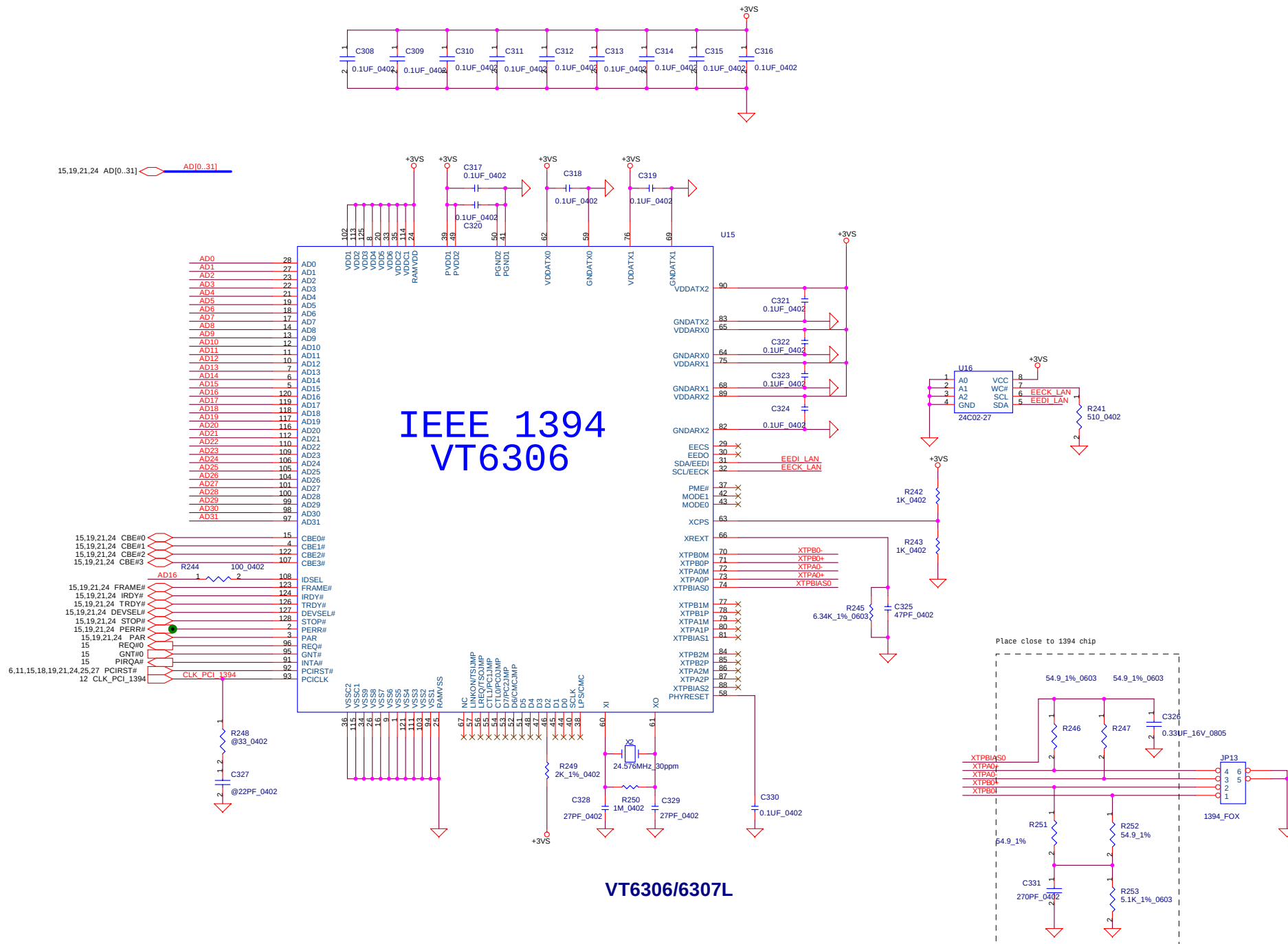


HDD/CD-ROM Module



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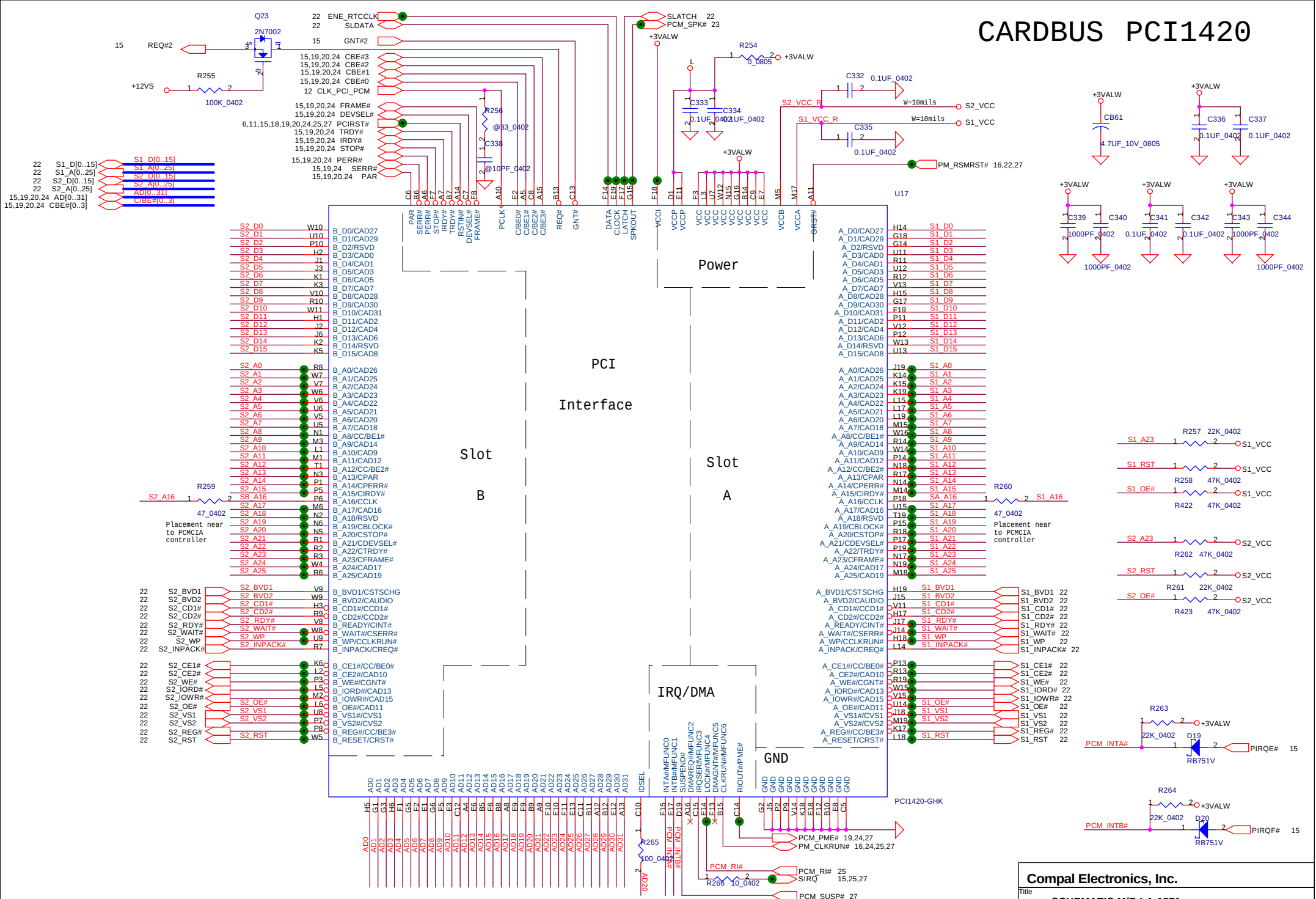
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CARDBUS PCI1420



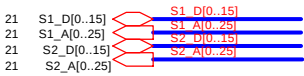
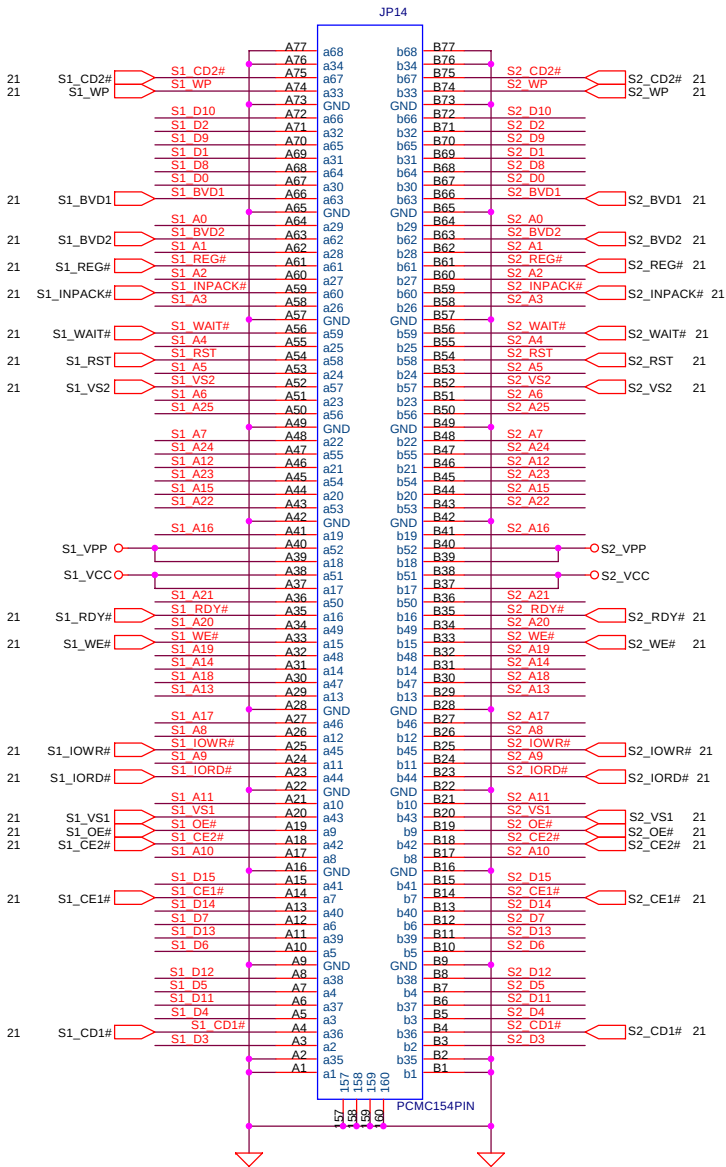
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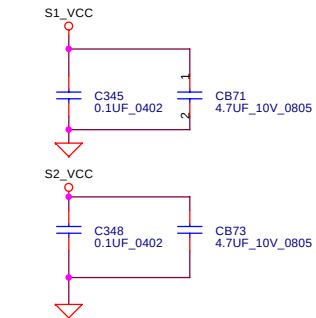
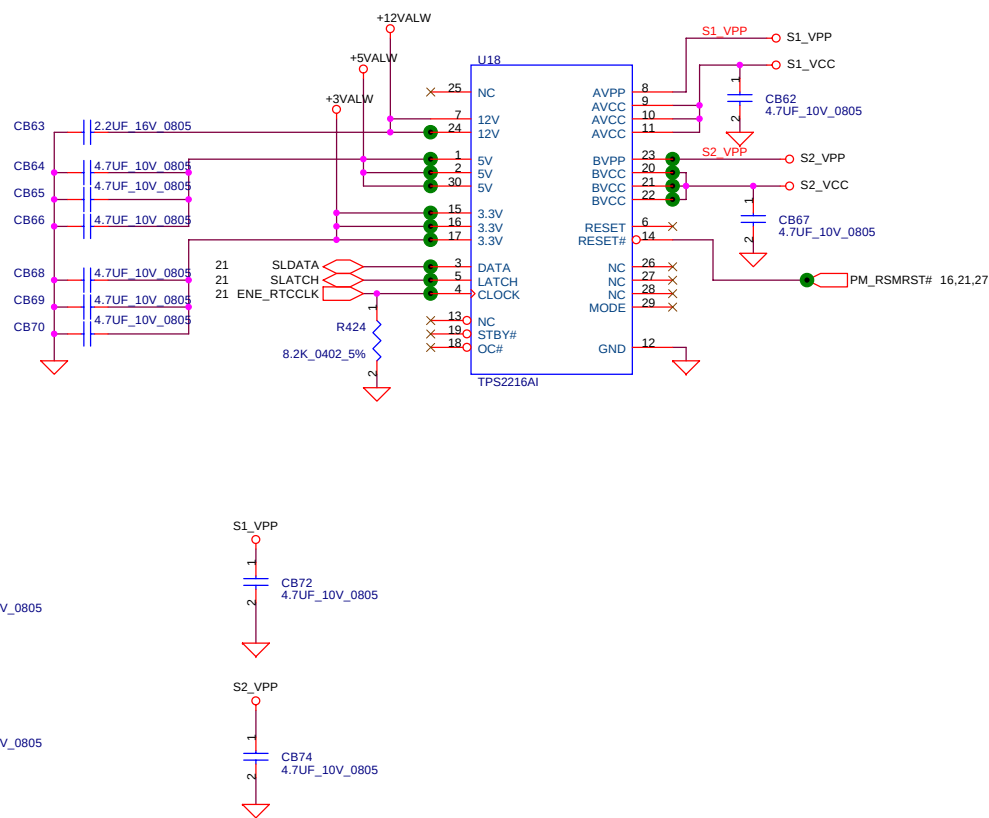
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CARDBUS SOCKET



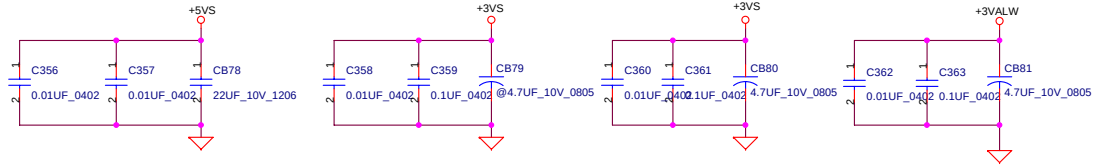
PCMCIA POWER CTRL.



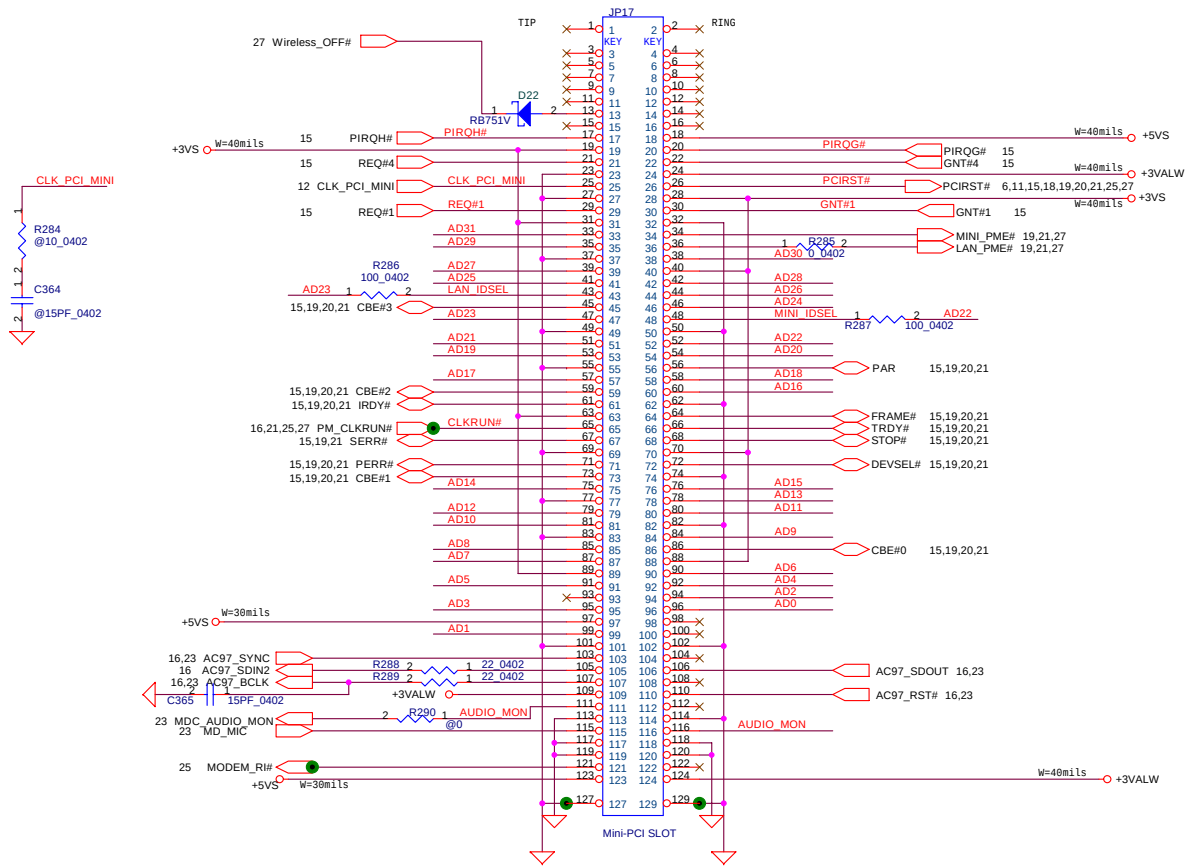


Place close to JP29

Mini-PCI Slot



AD[0..31] AD[0..31] 15,19,20,21

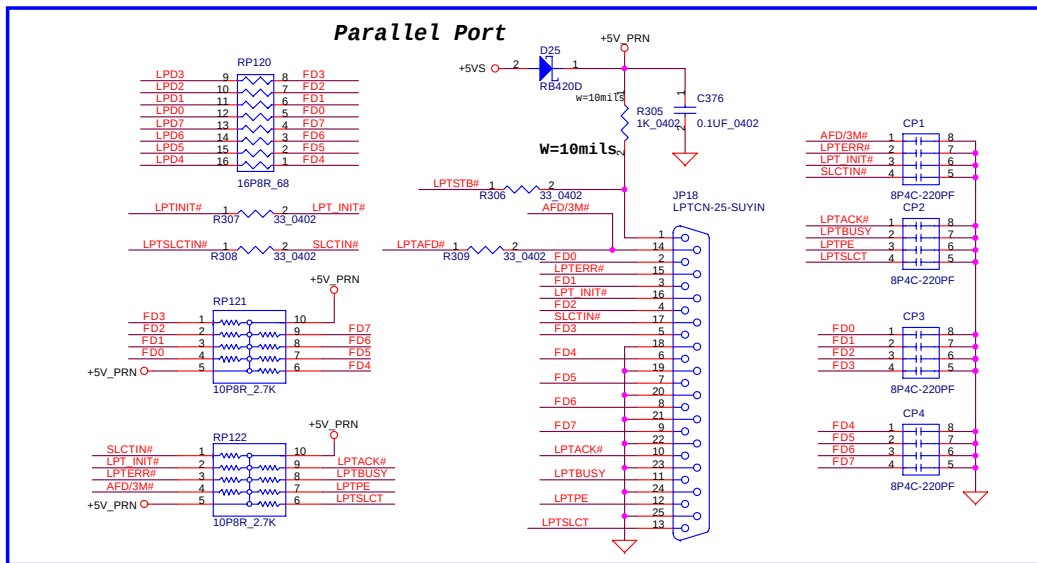
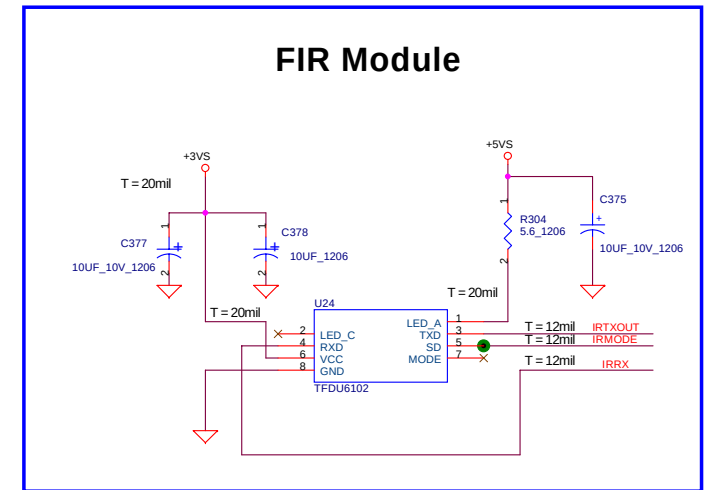
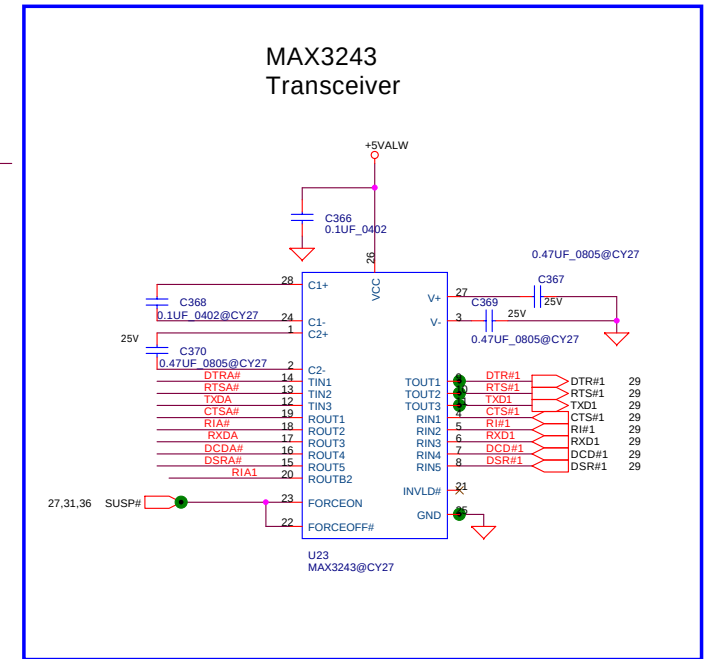
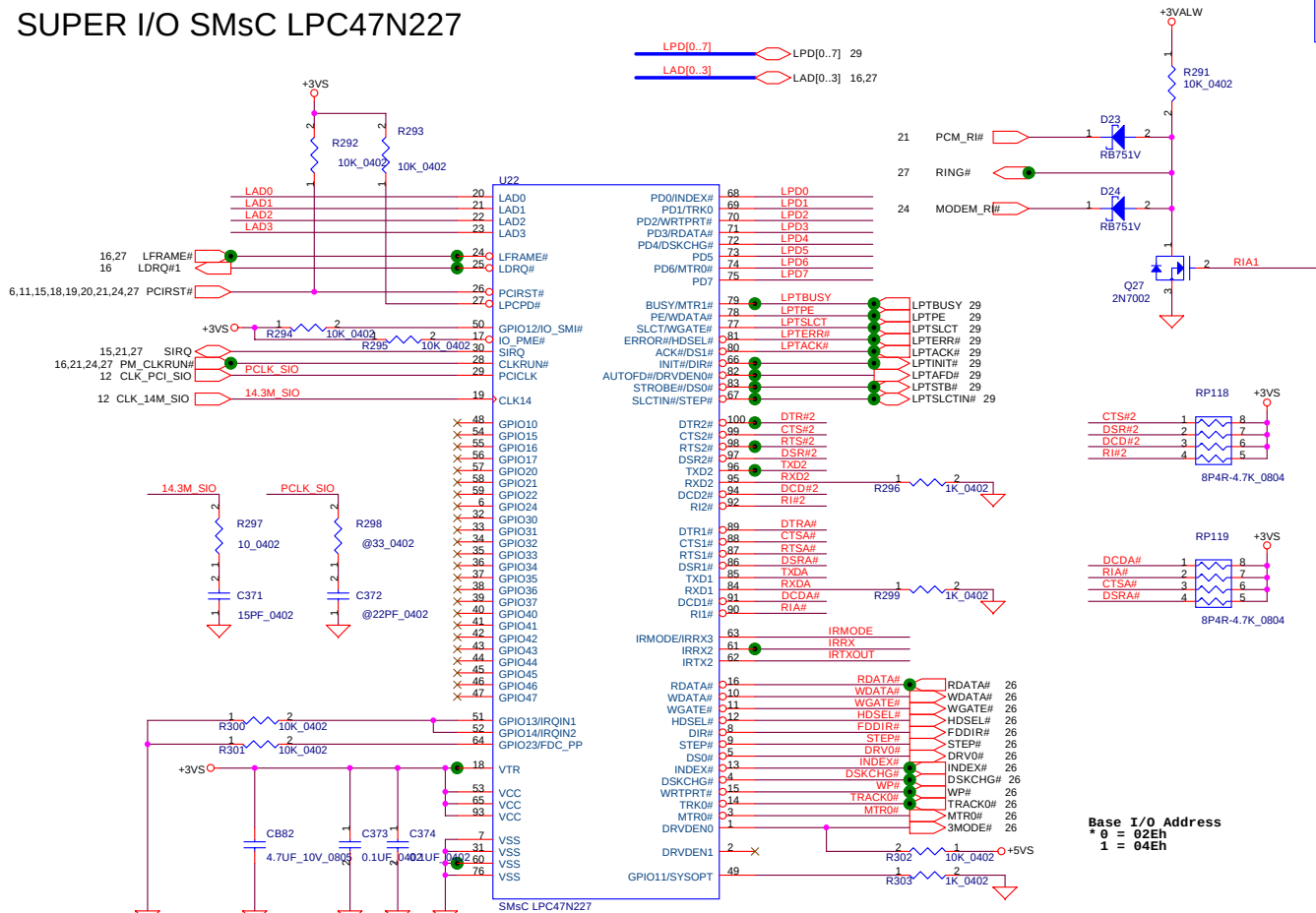


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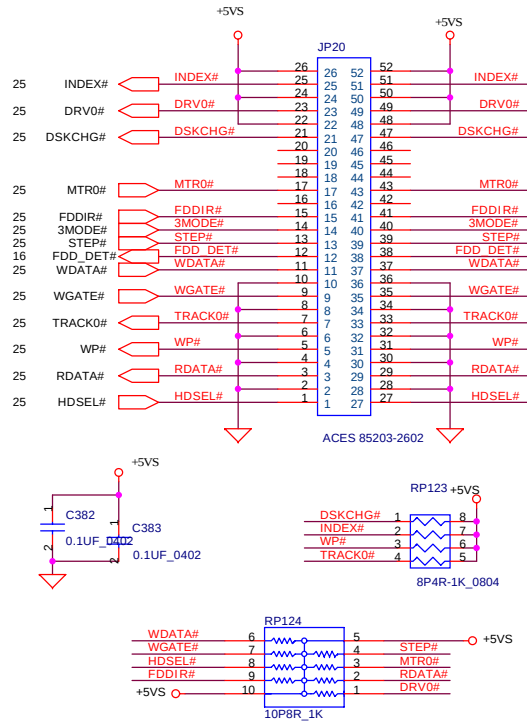
SUPER I/O SMsC LPC47N227

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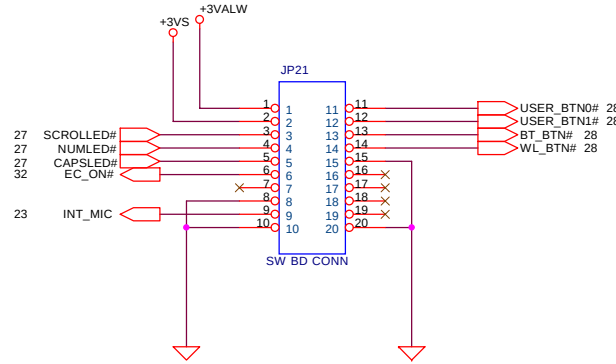


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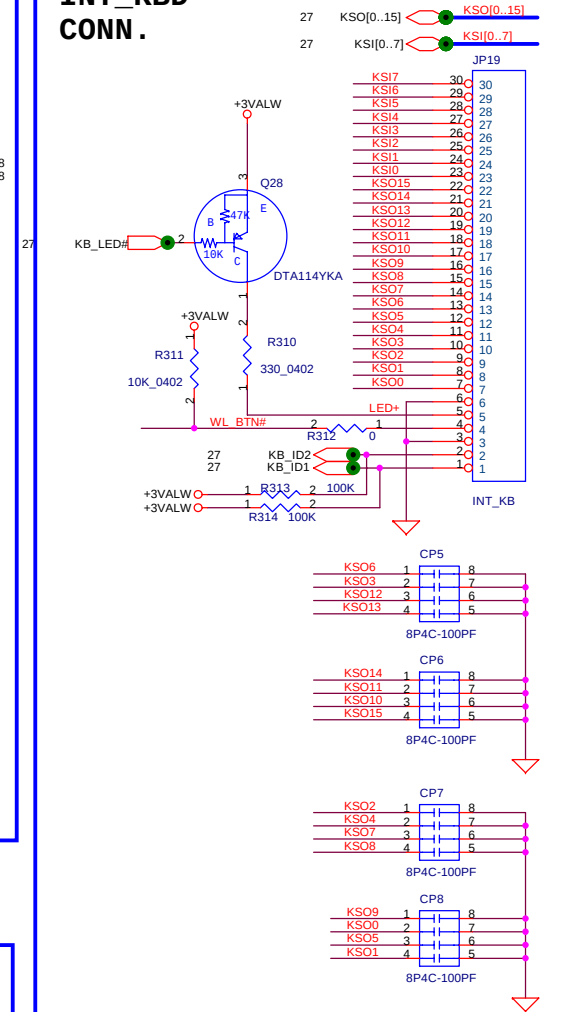
FDD CONN.



SWITCH BOARD CONN.

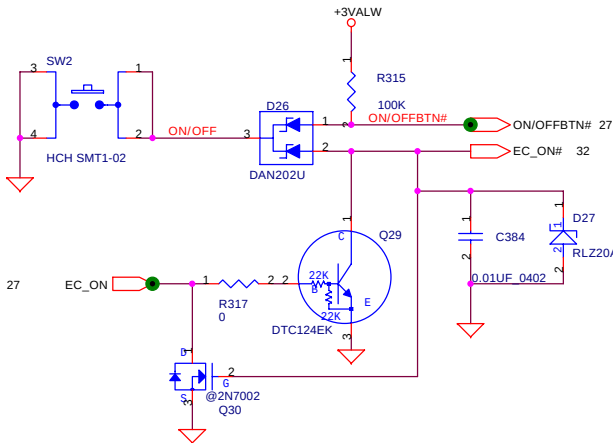


INT_KBD CONN.

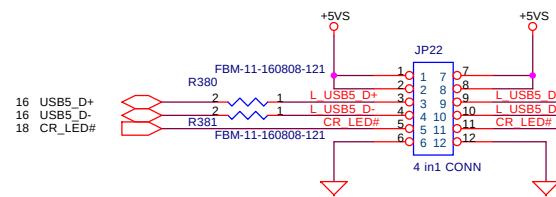


NEED CLOSEST JP18 ADD BY EMI REQUEST

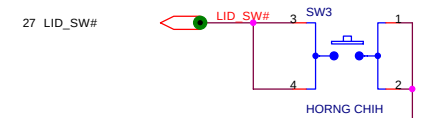
ON/OFF BUTTON



5 IN 1 CONN



LID SW

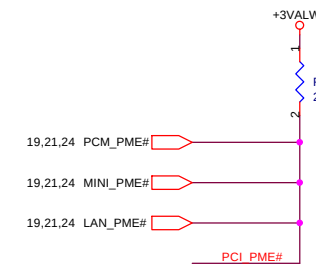


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```
SHBM=1: Enable shared memory with host BIOS
TRIS=1: While in IRE and OBD, float all the
        signals for clip-on ISE use
```

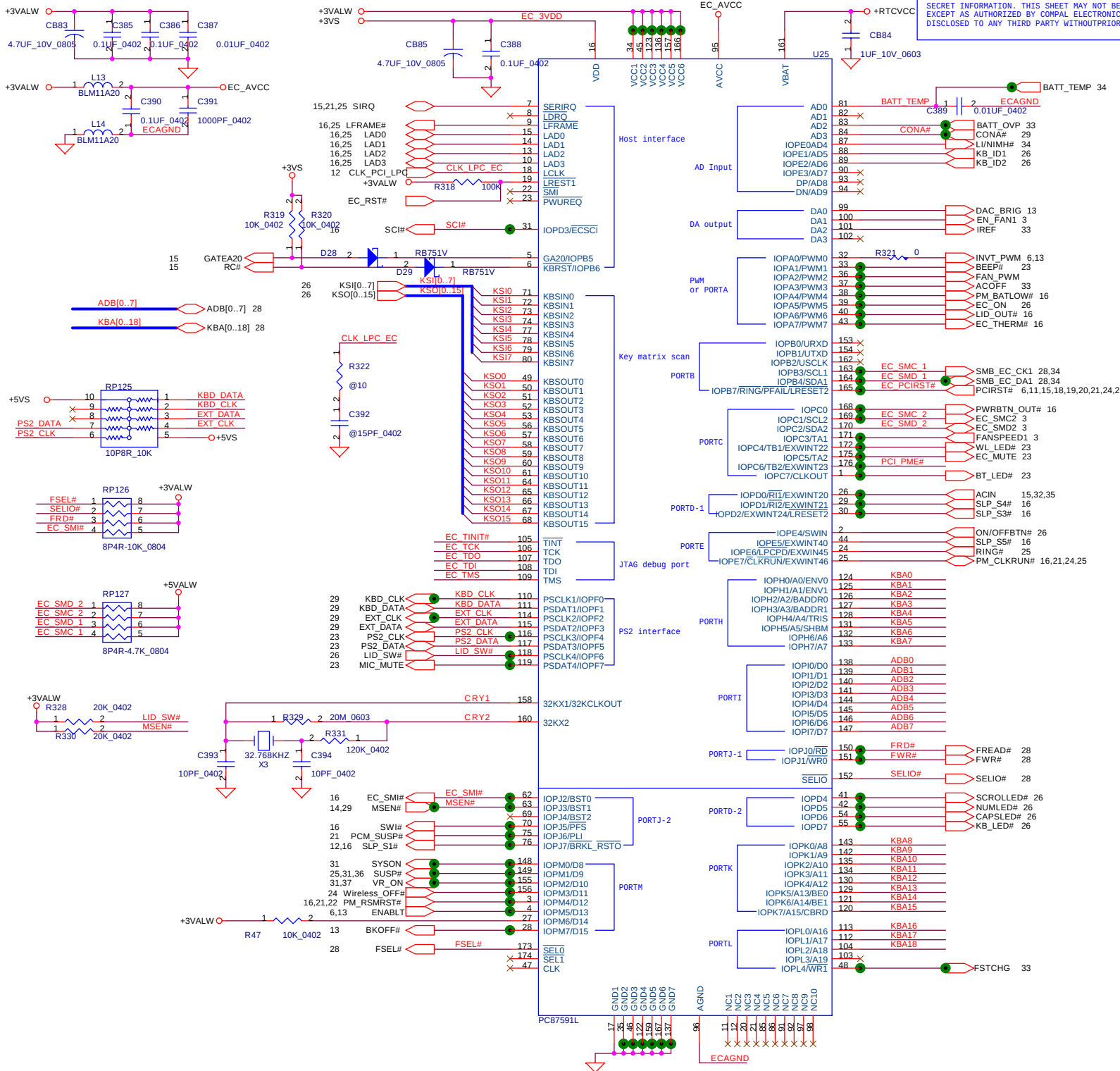


JP23

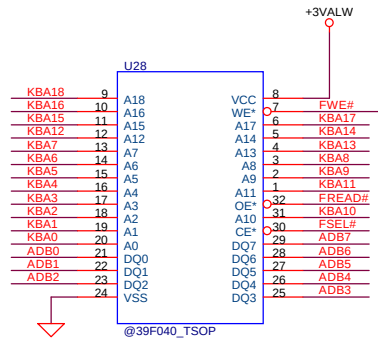
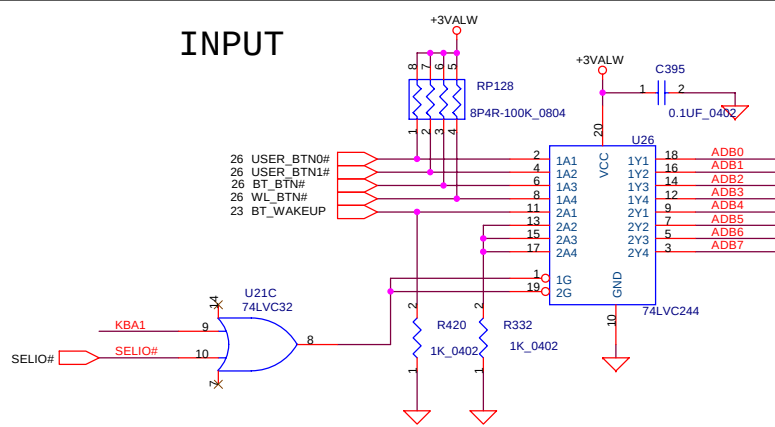
Pin	Signal
1	EC TINIT#
2	EC TCK
3	EC TDO
4	EC TDI
5	EC TMS
6	
7	
8	
9	
10	

+5VALW

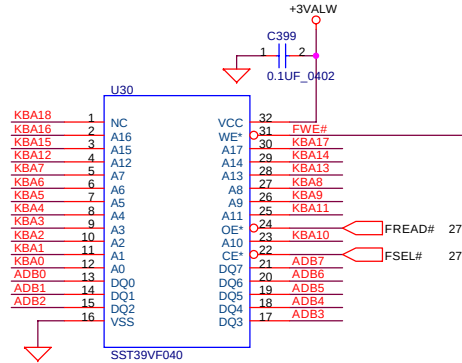
@96212-1011S



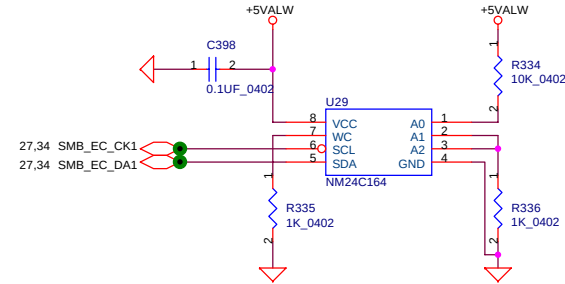
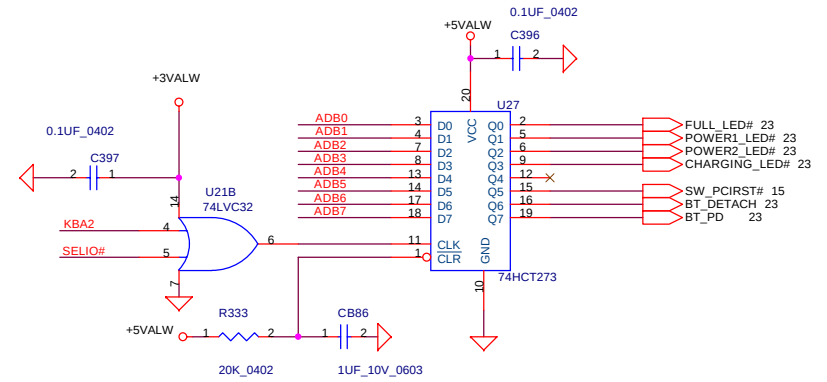
INPUT



27 KBA[0..18] KBA[0..18]
27 ADB[0..7] ADB[0..7]



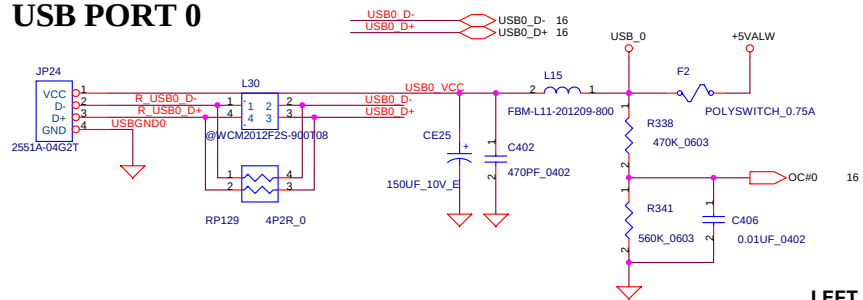
OUTPUT



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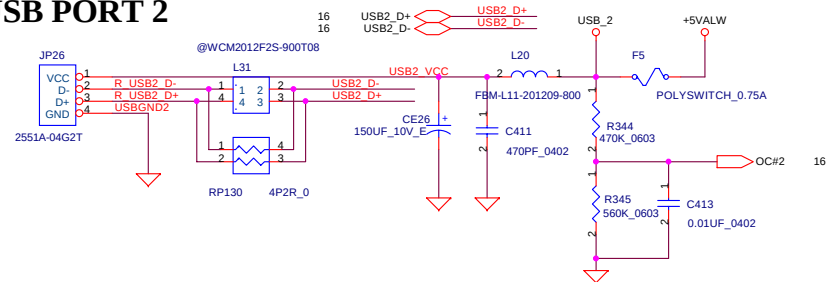
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USB PORT 0



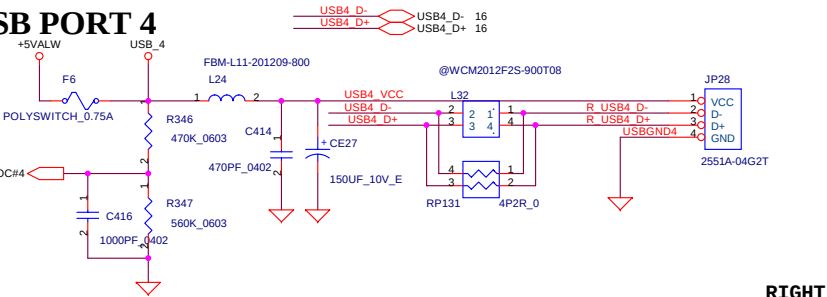
LEFT

USB PORT 2

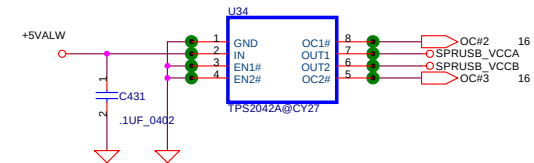
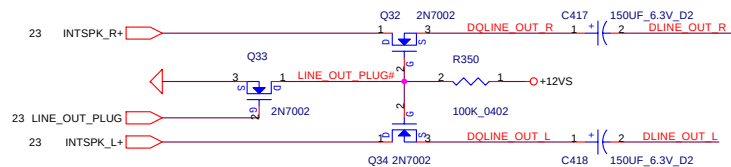


MIDDLE

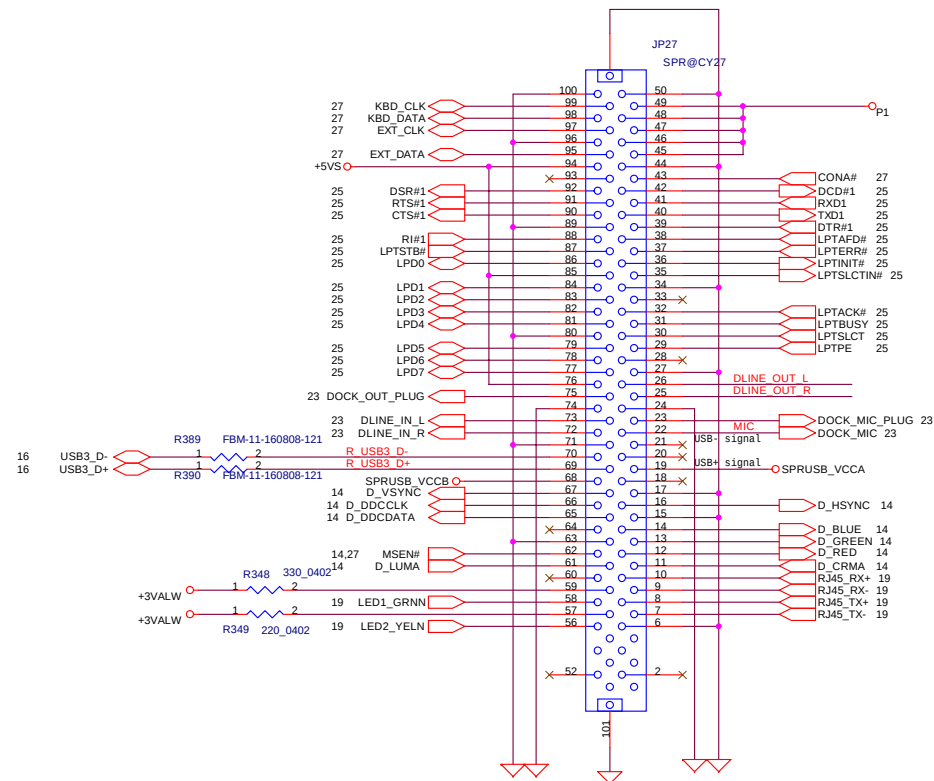
USB PORT 4



RIGHT



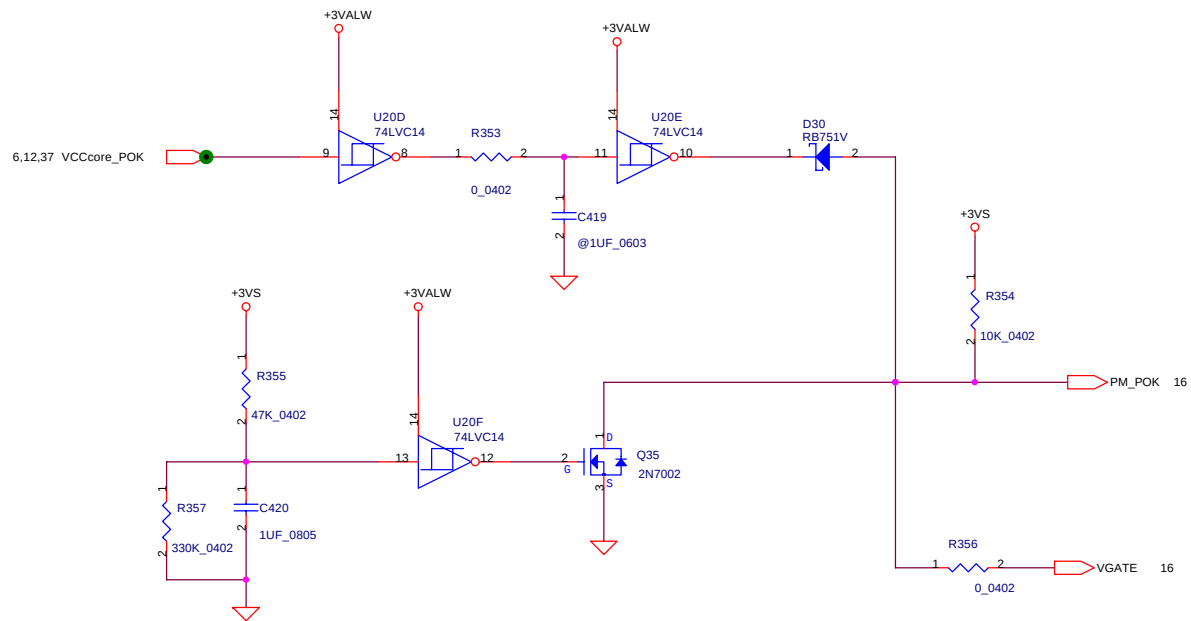
SPR CONN 204PIN



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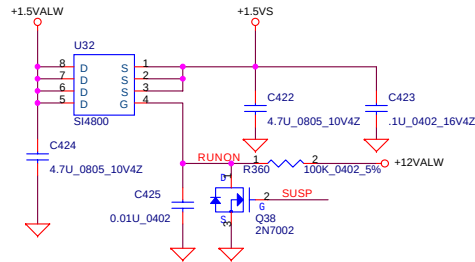
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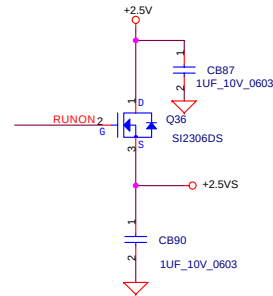
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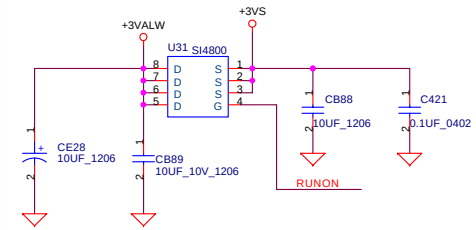
+1.5VALW To +1.5VS Transfer



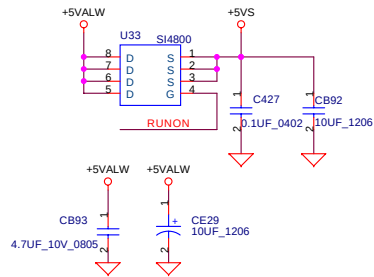
+2.5V to +2.5VS Transfer



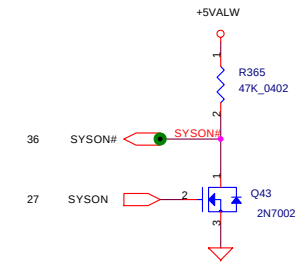
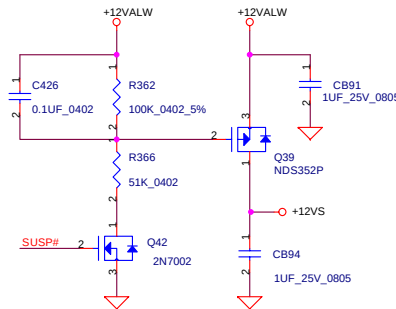
+3VALW to +3VS Transfer



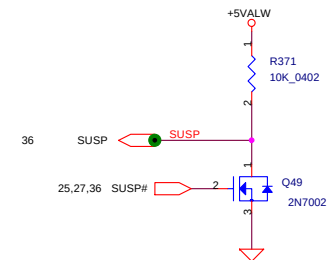
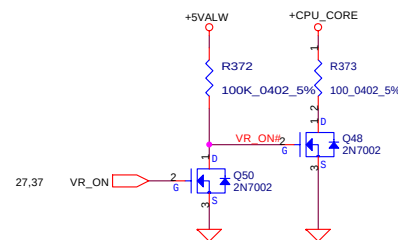
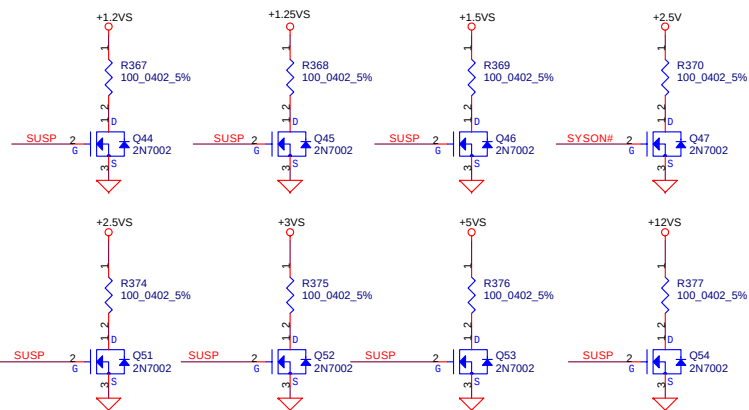
+5VALW to +5VS Transfer



+12VALW TO +12VS Transfer

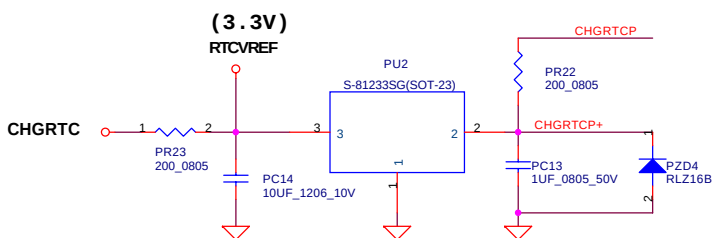
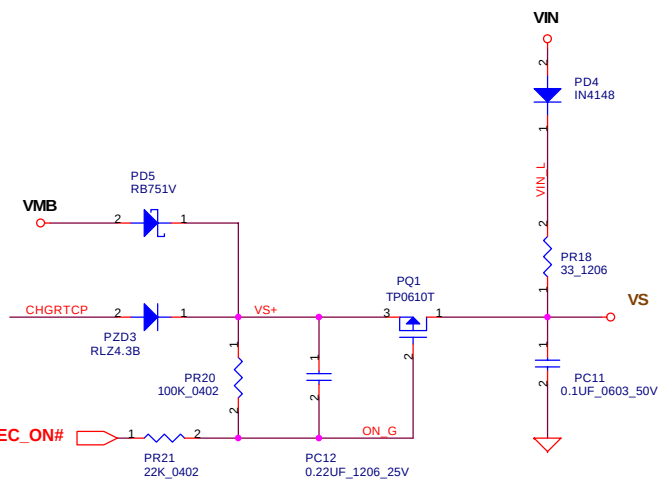
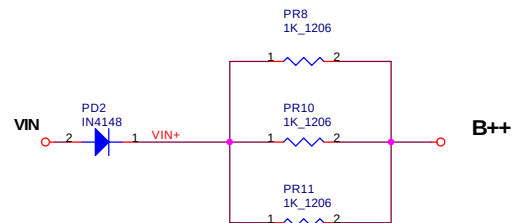
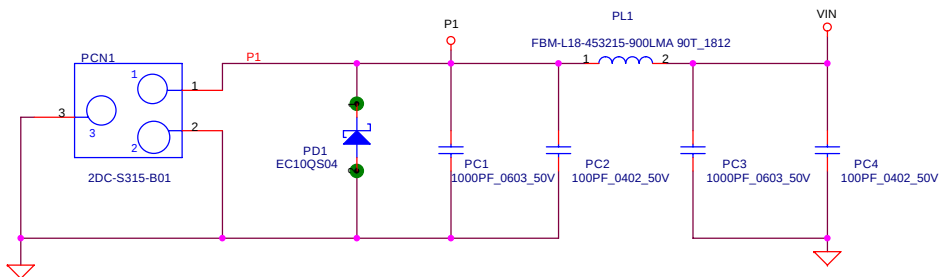


Discharge circuit



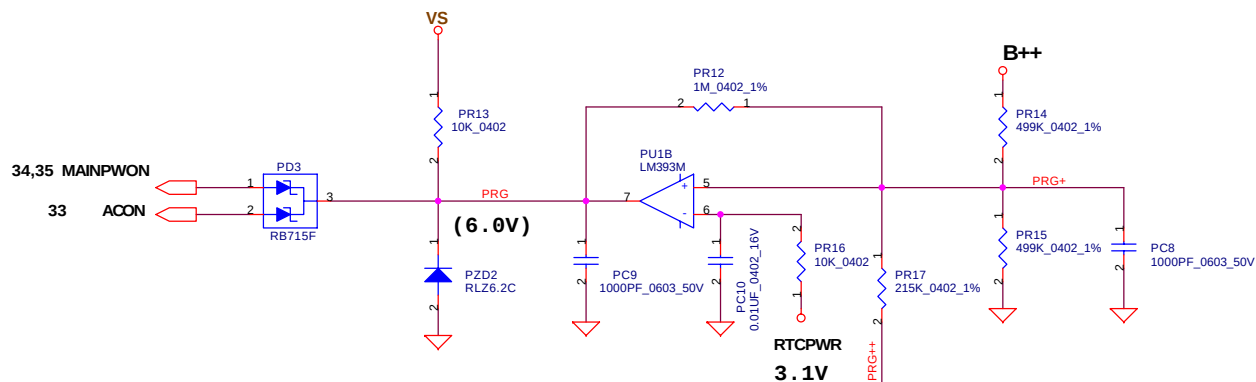
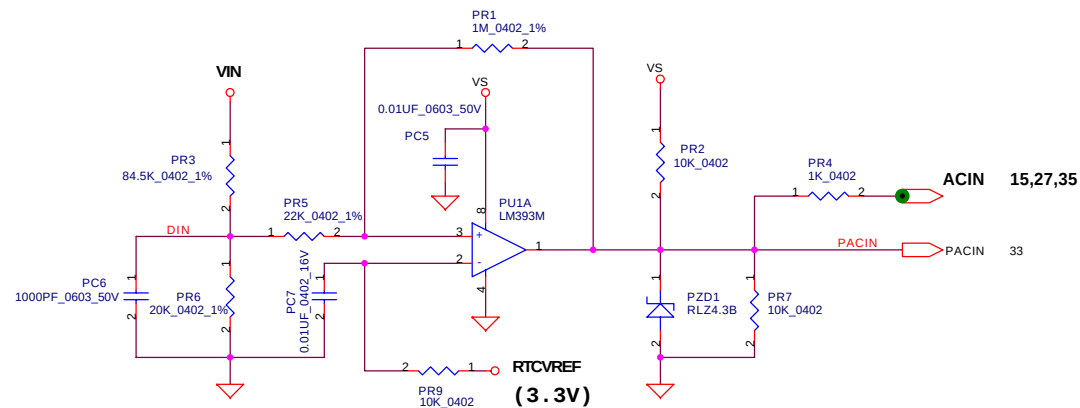
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Vin Detector

High 18.784 17.901 17.077 V
Low 17.877 17.043 16.195 V



ACIN

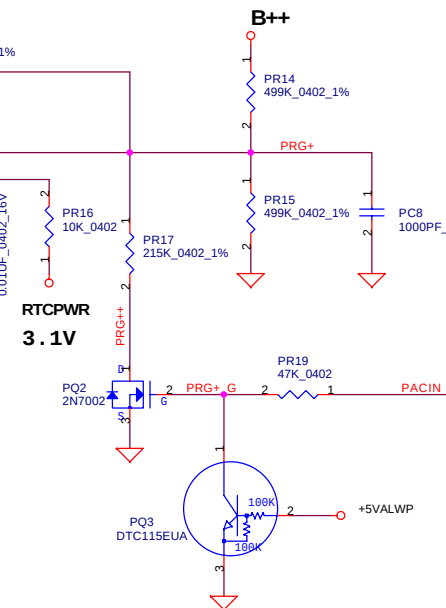
Precharge detector

16.6 15.9 15.2
13.48 12.93 12.09

BAT ONLY

Precharge detector

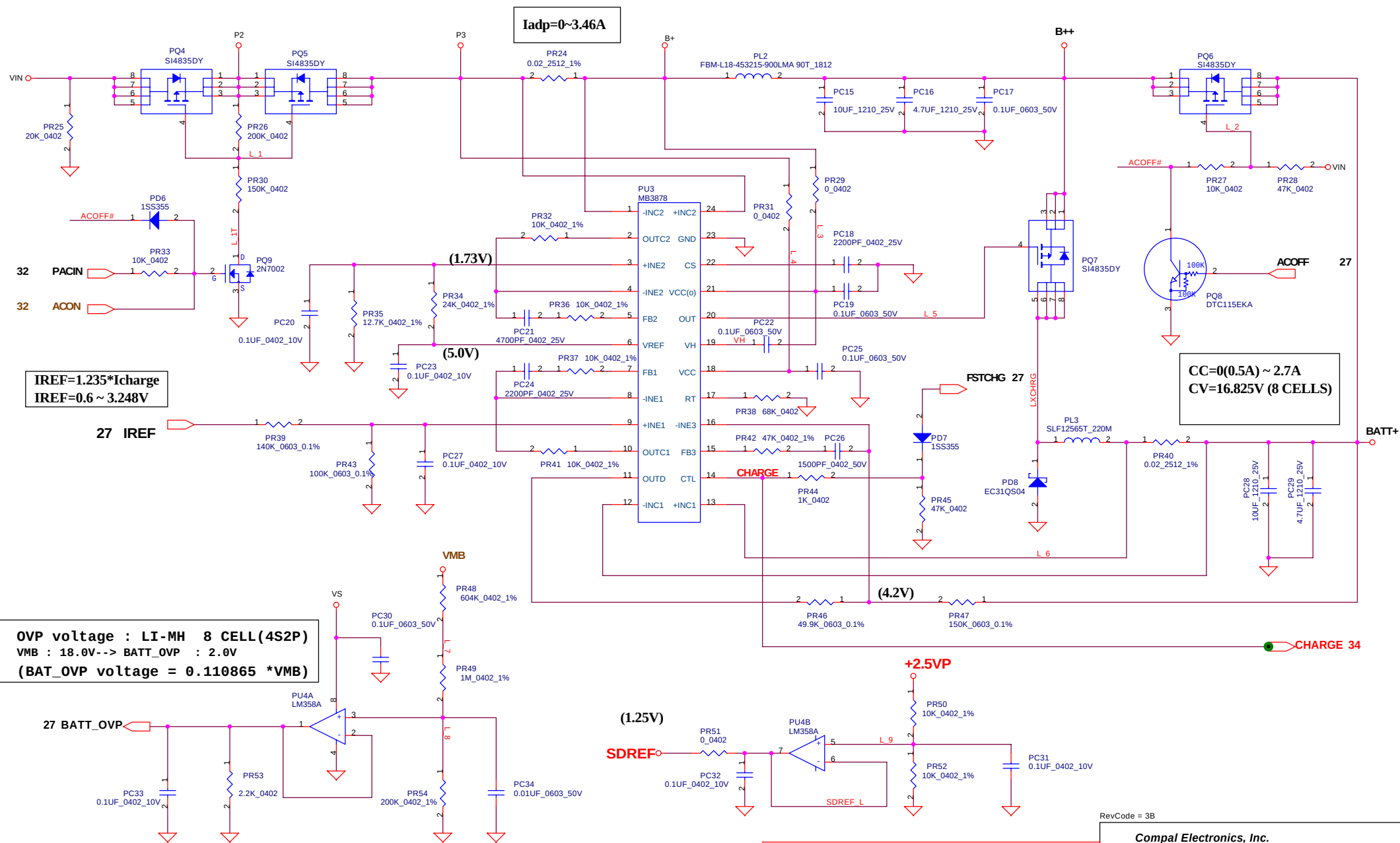
8.597 8.247 7.904
6.310 6.101 5.683

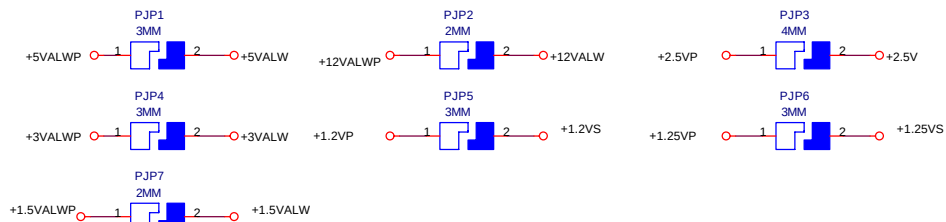


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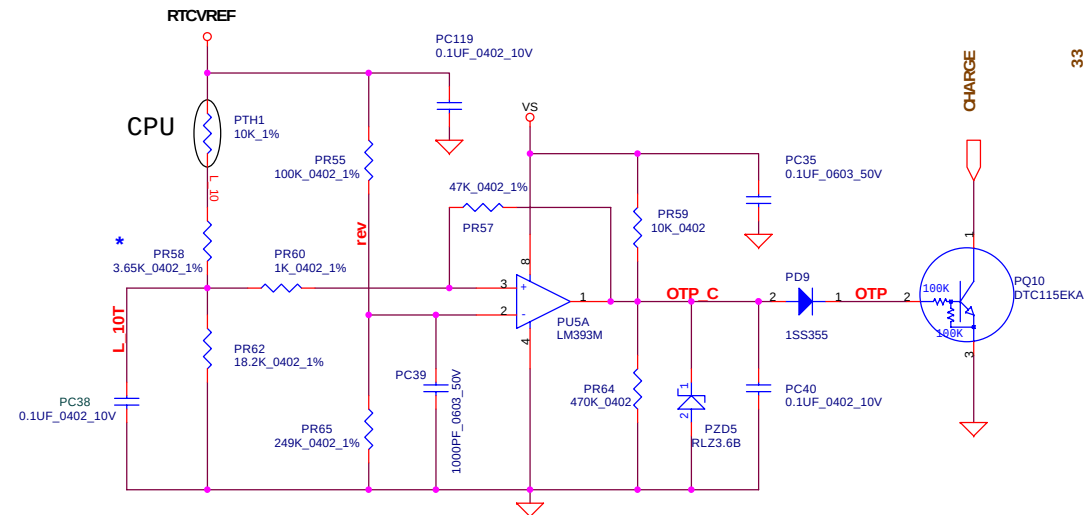
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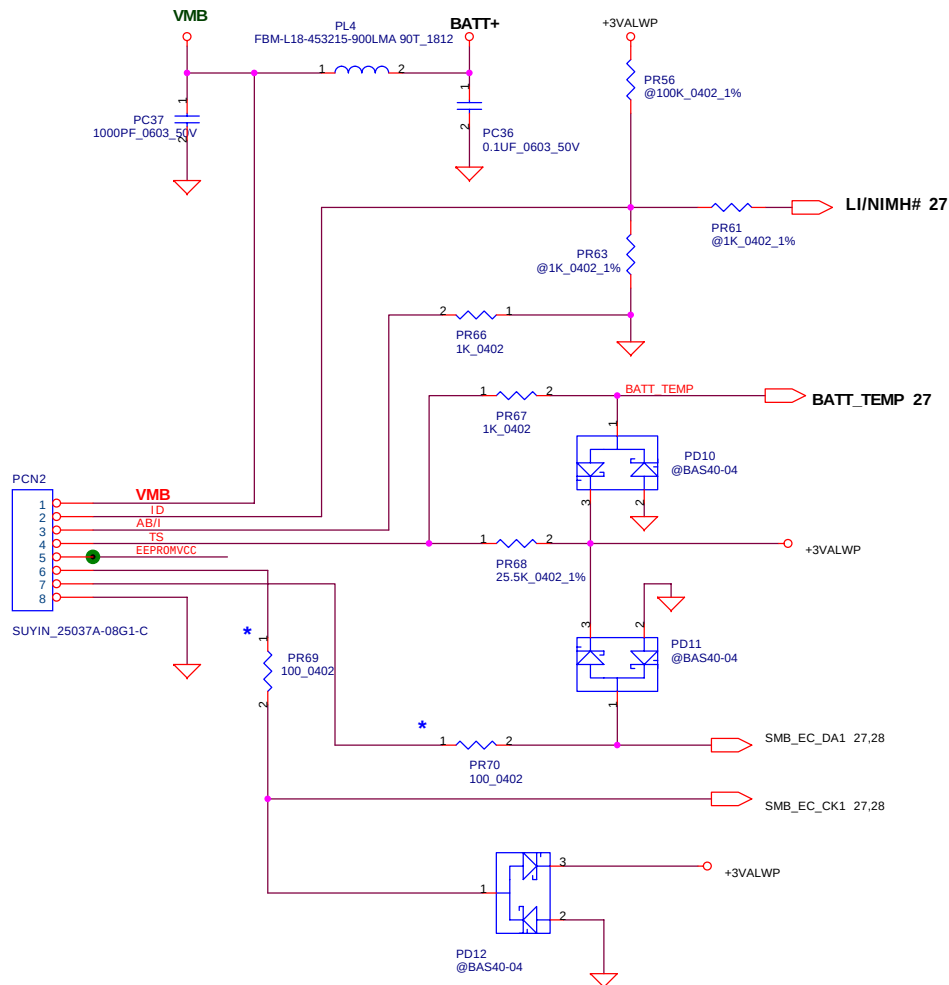
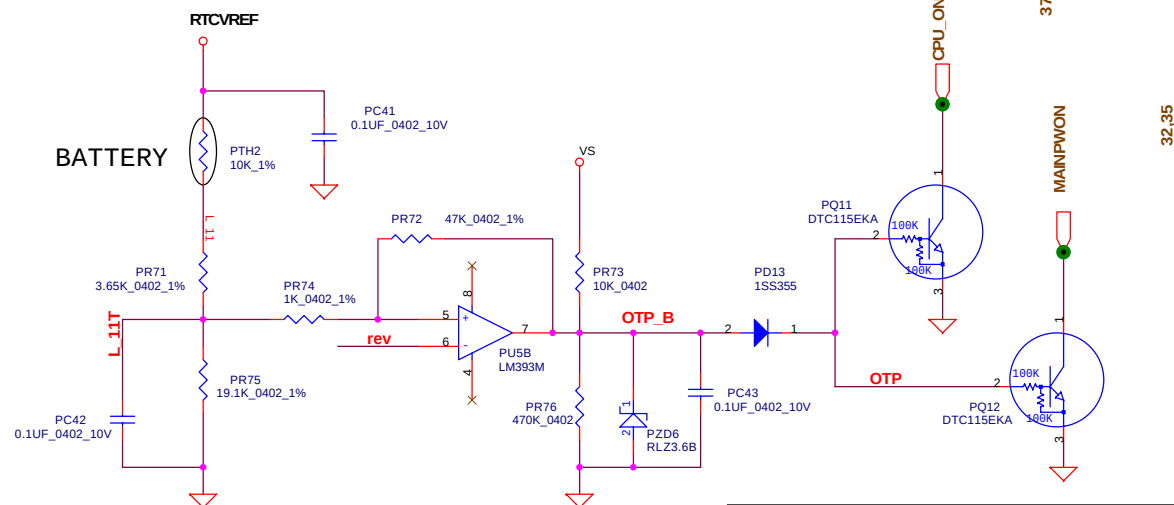




PH1 under CPU botten side :
 CPU thermal protection at 90(91)+-3 degree C
 Recovery at 50(51)+-3 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 85(86)+-3 degree C
 Recovery at 50(51) degree C

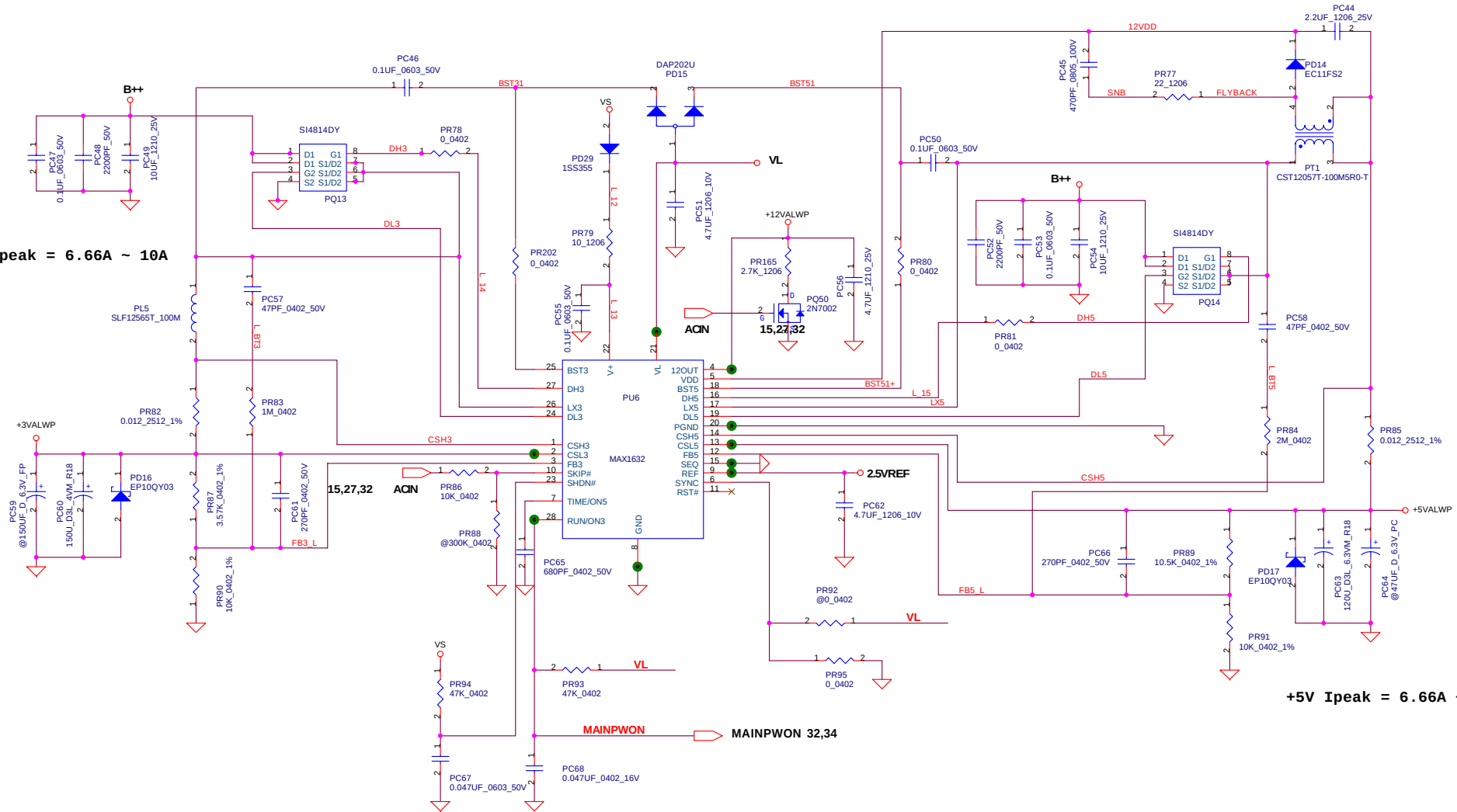


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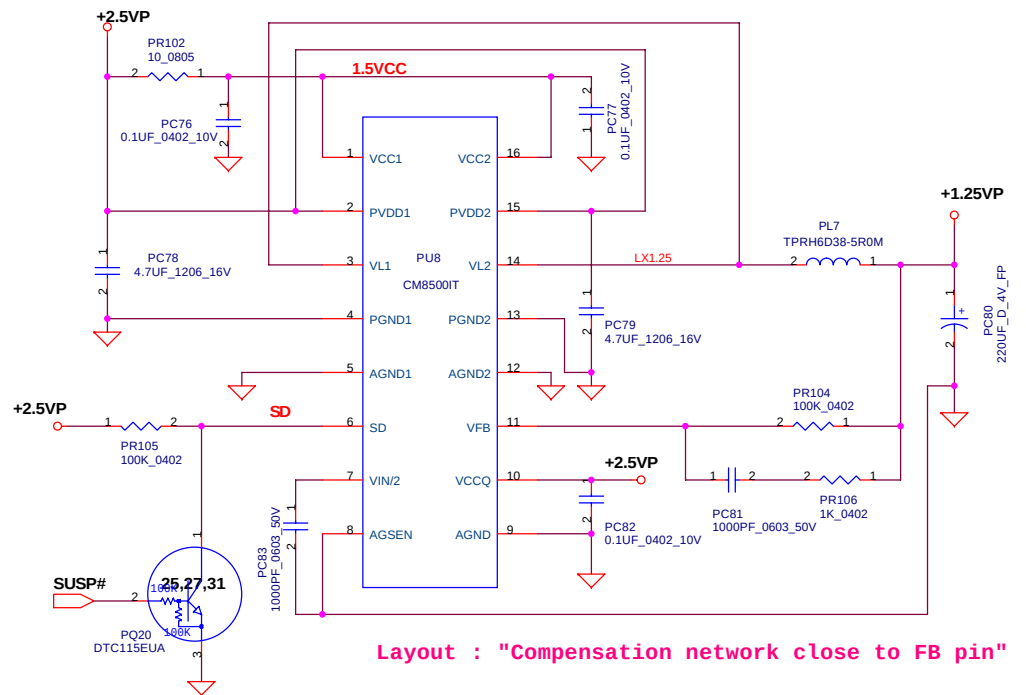
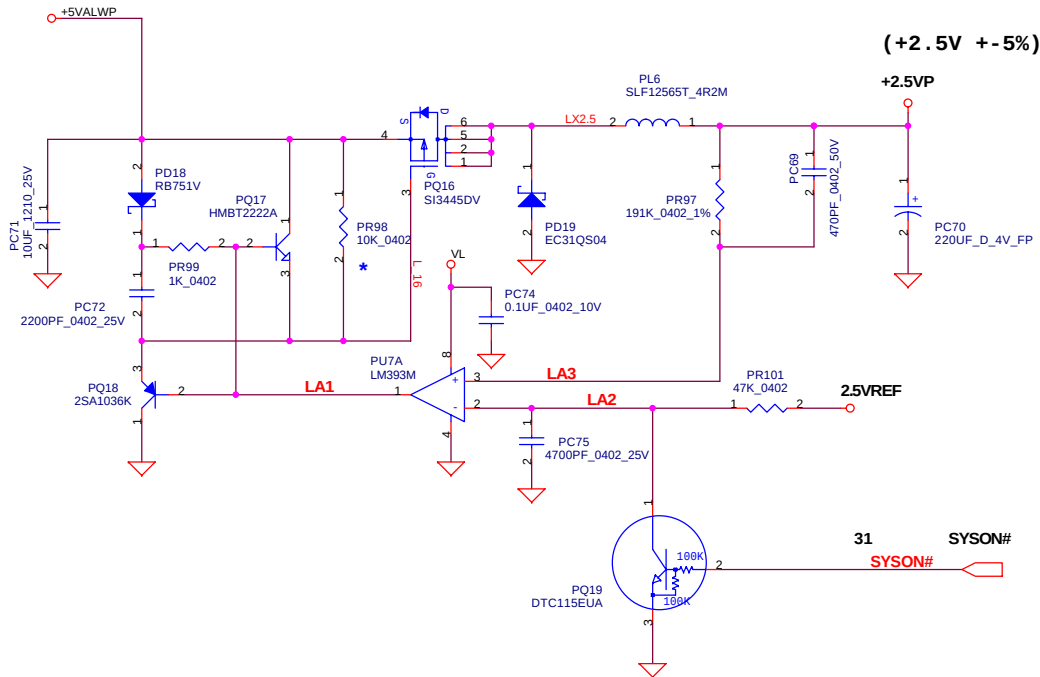
+3.3V Ipeak = 6.66A ~ 10A



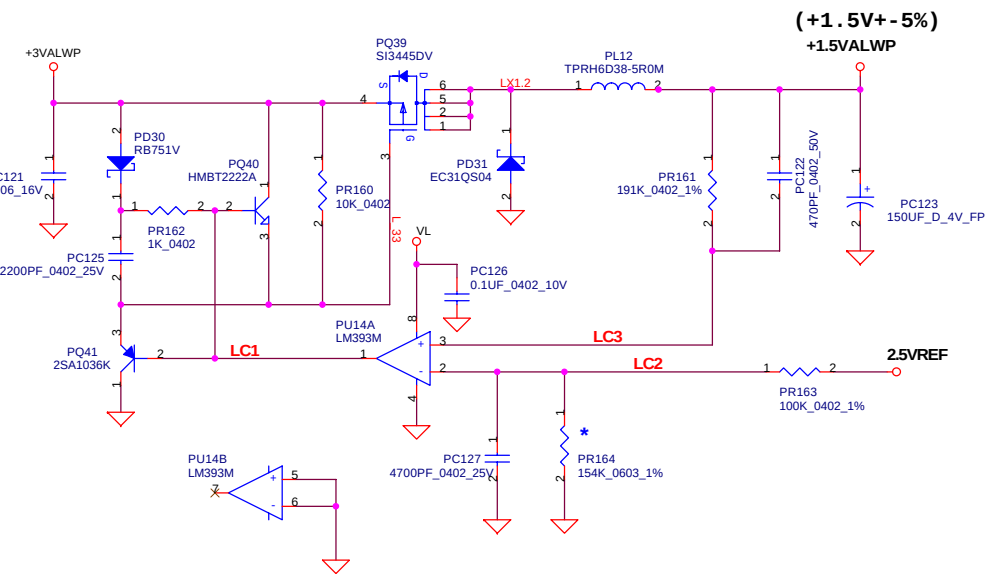
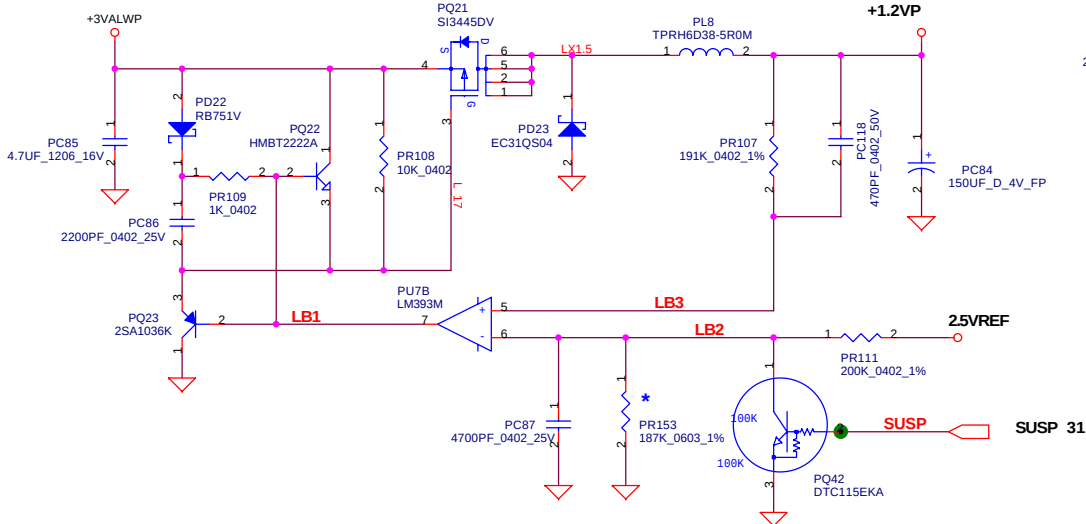
+5V Ipeak = 6.66A ~ 10A

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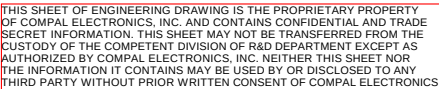
Layout : "Compensation network close to FB pin"



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+3VALW/+5VALW/
+12VALW/+1.5VALW

PM_RSMRST#

>10 ms

ON/OFF

PWRBTN_OUT#

>1ms

110ms

SYSON / SUSP#

10ms

+1.25VS/+1.5VS/+2.5V/
+3VS/+5VS/+12VS

10ms

CLOCK

7.5ms

VR_ON

1.6ms

+1.2VPP

1ms

+CPU_CORE

3ms

VCCcore_POK

1.3ms

PM_POK/CPUPWRGD

12ms

PCIRST#

1ms

CPURST#

1ms

A-TEST (2002-09-09)

Fine tune power on sequence

- 1.C425 change to 0.01U
- 2.Delete R364
- 3.R396 change to 4.7K_0402
- 4.Delete R194
- 5.Delete R351
- 6.Delete R87
- 7.Delete R359 , Q37 , R361 , Q40 , R364 , C428 , R363 , Q41
- 8.Delete U10
- 9.Add D31

Page04 =To solve 4 sec shutdown restart issue : Delete Q3

Page03 = JP1 change to 3 pin connector(No PWM)

Page11 : EMI solution

- 1.Add U35 , L36 , C432 , R414 , R415 , R416

Page12 : TV-OUT issue

1. R107 , R108 changeto 4.7K

Page06 = Base on Intel spec : Delete Q6 , Q7 , R59 , R61 , C21, R87

Page20 = Delete R248 , C327

Page21 = R258 , R261 change to 47K_0402
Add R422 , R423 47K_0402
Delete R256 , C338

Page22 : Add R424 8.2K_0402

Page25 : Delete R298 , C372

Page28 : Add R420 pull low

Page29 : Add R421 , Q58

Page15 : Add R425 PULL UP

Page16 : Add R426 pull up , R427 pull down

B-TEST (2002-10-10)

Page08 : FB1,2,4,5 change to 0_0805

Page11 : R111 change to 1K_0402

Page12 : Del L36,C432,R414,R415,R416,U35,R148

Page16 : Add R428,R429 for FDD_DET#

Page23 : Add R195,C235
Del R273,R275
Add R281,C353

Page29 : Del R382,3,4,5,6,7. L30,31,32
Add RP129,130,131

Page30 : C420 change to 1UF_0805

B2-TEST (2002-12-26)

Page27 : Change RP125 to 10K

Page29 : Delete Q57, Q58 , R421 , R388 , R391

MP (2003-07-28)

Page11 : Change R107,R108 from 1K_0402 to 1.2K_0402

MP (2004-06-15)

Page11 : Change R111 from 1K_0402 to 33_0402

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