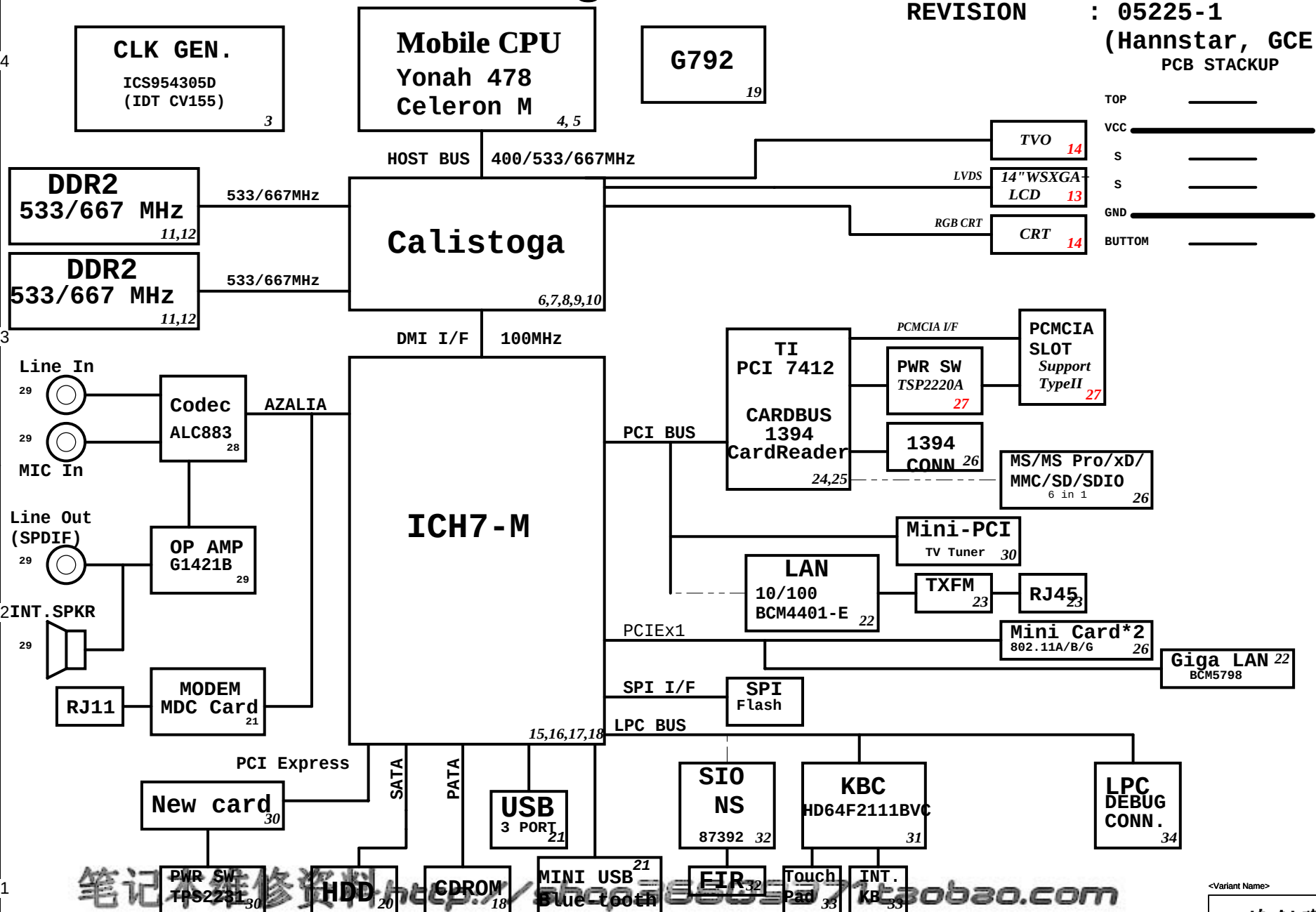


AG1 Block Diagram

Project code: 91.4A901.001
PCB P/N : 55.4A903.XXX
REVISION : 05225-1
(Hannstar, GCE)
PCB STACKUP



SYSTEM DC/DC TPS51120 41	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5
SYSTEM DC/DC MAX8743EE 42	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
TPS51100 44	
1D8V_S3	DDR_VREF
APL5332KAC 44	
3D3V_S5	2D5V_S0
APL5912-U 44	
3D3V_S5	1D5V_S0

MAXIM CHARGER MAX8725+Max1773 43	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6262 <i>39,40</i>	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 48A

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN,EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FWH[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT,ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS,SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPI025	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#/ XOR Chain Selection. Rising Edge of PWROK	Reserved	IBP, Chapter 2
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO_REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

954305D 27Mhz/LCDCLK Spread and Frequency Selection Table

page 3

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+ -0.25 Center
1	0	0	1	+ -0.5 Center
1	0	1	0	+ -0.75 Center
1	0	1	1	+ -1.0 Center
1	1	0	0	+ -0.25 Center
1	1	0	1	+ -0.5 Center
1	1	1	0	+ -0.75 Center
1	1	1	1	+ -1.0 Center

PCI Routing

page 16

	IDSEL	INT -> PIRQ	REQ/GNT
7412	22	A->F, B->B'	0
MiniPCI	21	A/B -> E	1
LAN	23	A -> H	2
1410	25	A->G, B->B,	0

History

6/6 drawing SA
7/11 Rename for placement

Calistoga Strapping Signals and Configuration

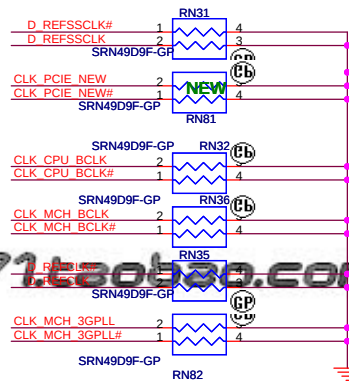
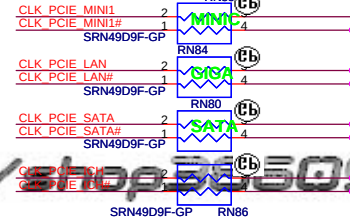
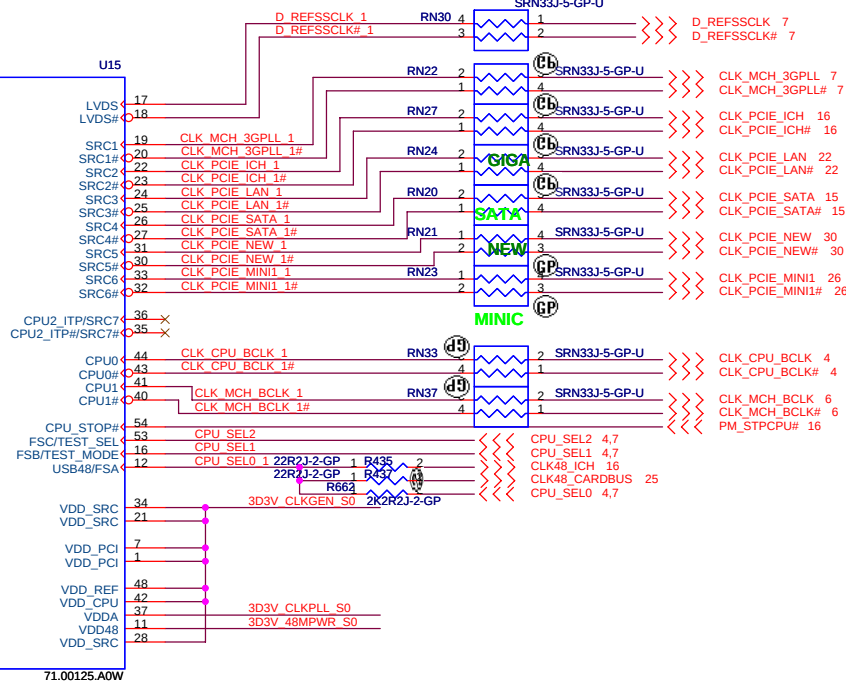
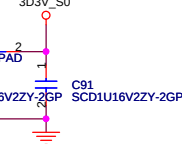
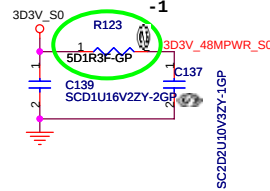
EDS 17050 0.71 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCTRL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

<Variant Name>

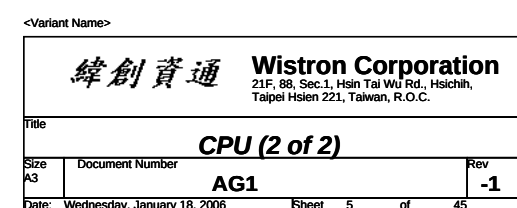
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reference			
Size A3	Document Number AG1		Rev -1
Date:	Monday, January 09, 2006	Sheet 2 of	45

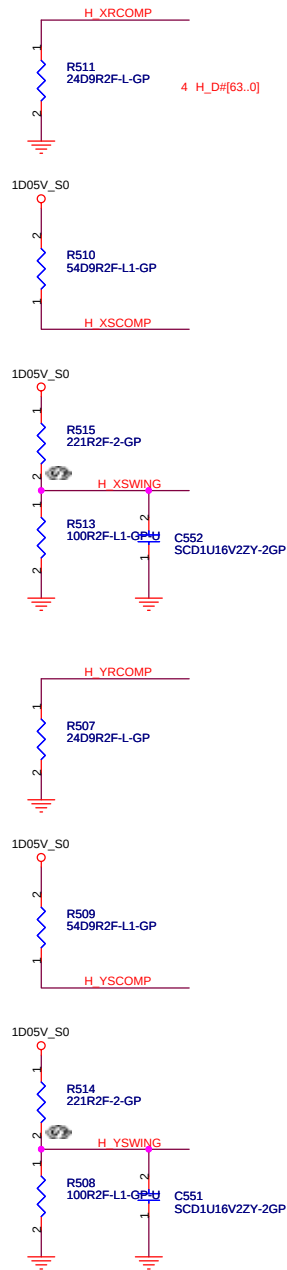


Signal	Pin	Function	Notes
PCLK_SIO	1	EC29	dy
CLK_ICH14	1	EC26	dy
PCLK_MINI	1	EC28	dy
PCLK_KBC	1	EC27	dy
CLK_ICHPCI	1	EC32	dy
CLK48_ICH	1	EC15	dy

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<i>Clock Generator ICS954305D</i>			
Size A3	Document Number AG1		Rev -1
Date:	Wednesday, January 18, 2006	Sheet 3 of	45





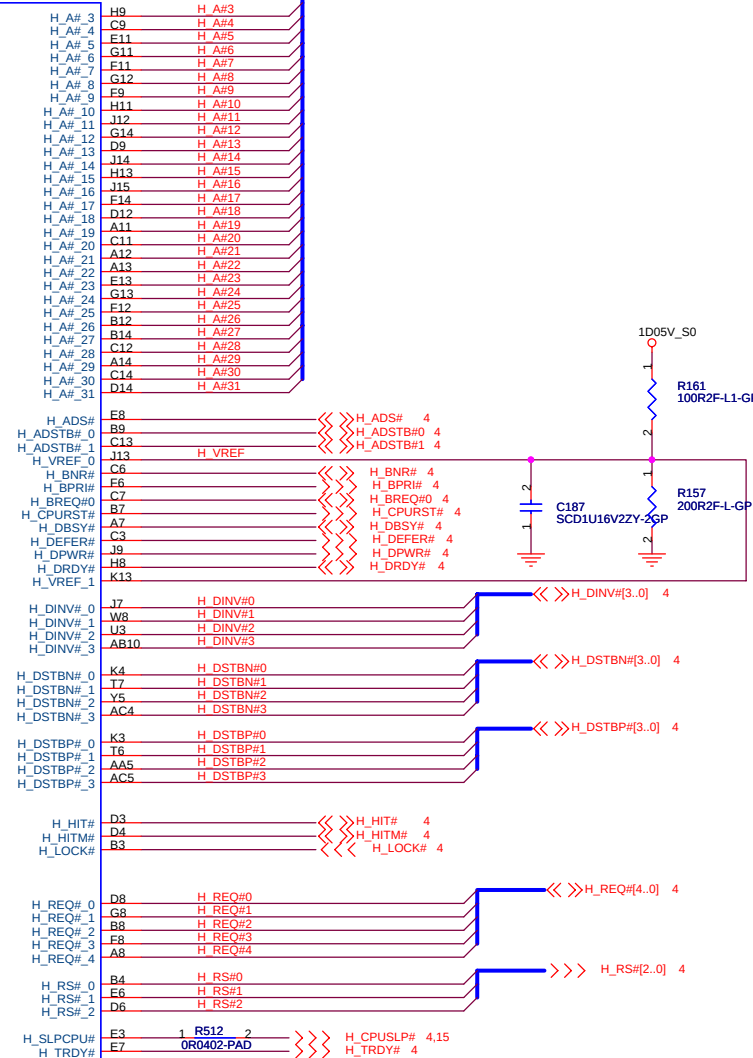
<<>>

3 CLK_MCH_BCLK
3 CLK_MCH_BCLK#

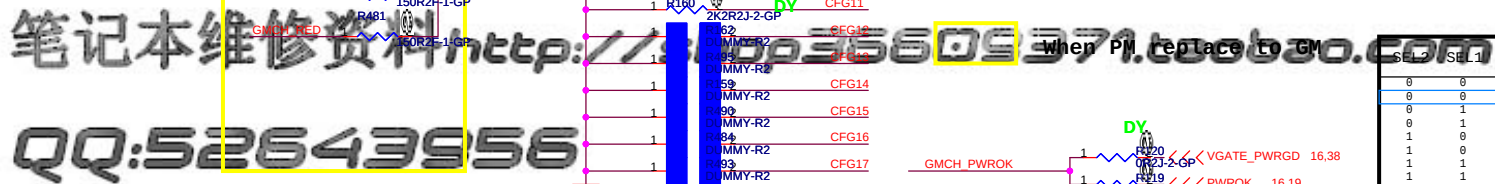
H_D#0	F1	H_D#_0
H_D#1	J1	H_D#_1
H_D#2	H1	H_D#_2
H_D#3	J6	H_D#_3
H_D#4	H3	H_D#_4
H_D#5	K2	H_D#_5
H_D#6	G1	H_D#_6
H_D#7	G2	H_D#_7
H_D#8	K9	H_D#_8
H_D#9	K1	H_D#_9
H_D#10	K7	H_D#_10
H_D#11	J8	H_D#_11
H_D#12	H4	H_D#_12
H_D#13	J3	H_D#_13
H_D#14	K11	H_D#_14
H_D#15	G4	H_D#_15
H_D#16	T10	H_D#_16
H_D#17	W11	H_D#_17
H_D#18	T3	H_D#_18
H_D#19	U7	H_D#_19
H_D#20	U9	H_D#_20
H_D#21	U11	H_D#_21
H_D#22	T11	H_D#_22
H_D#23	W5	H_D#_23
H_D#24	T1	H_D#_24
H_D#25	T8	H_D#_25
H_D#26	T4	H_D#_26
H_D#27	W7	H_D#_27
H_D#28	U5	H_D#_28
H_D#29	T9	H_D#_29
H_D#30	W6	H_D#_30
H_D#31	T5	H_D#_31
H_D#32	AB7	H_D#_32
H_D#33	AA9	H_D#_33
H_D#34	W4	H_D#_34
H_D#35	W3	H_D#_35
H_D#36	Y3	H_D#_36
H_D#37	Y7	H_D#_37
H_D#38	W5	H_D#_38
H_D#39	Y10	H_D#_39
H_D#40	AB8	H_D#_40
H_D#41	W2	H_D#_41
H_D#42	AA4	H_D#_42
H_D#43	AA7	H_D#_43
H_D#44	AA2	H_D#_44
H_D#45	AA6	H_D#_45
H_D#46	AA10	H_D#_46
H_D#47	Y8	H_D#_47
H_D#48	AA1	H_D#_48
H_D#49	AB4	H_D#_49
H_D#50	AC9	H_D#_50
H_D#51	AB11	H_D#_51
H_D#52	AC11	H_D#_52
H_D#53	AB3	H_D#_53
H_D#54	AC2	H_D#_54
H_D#55	AD1	H_D#_55
H_D#56	AD9	H_D#_56
H_D#57	AC1	H_D#_57
H_D#58	AD7	H_D#_58
H_D#59	AC6	H_D#_59
H_D#60	AB5	H_D#_60
H_D#61	AD10	H_D#_61
H_D#62	AD4	H_D#_62
H_D#63	AC8	H_D#_63

CALISTOGA

HOST



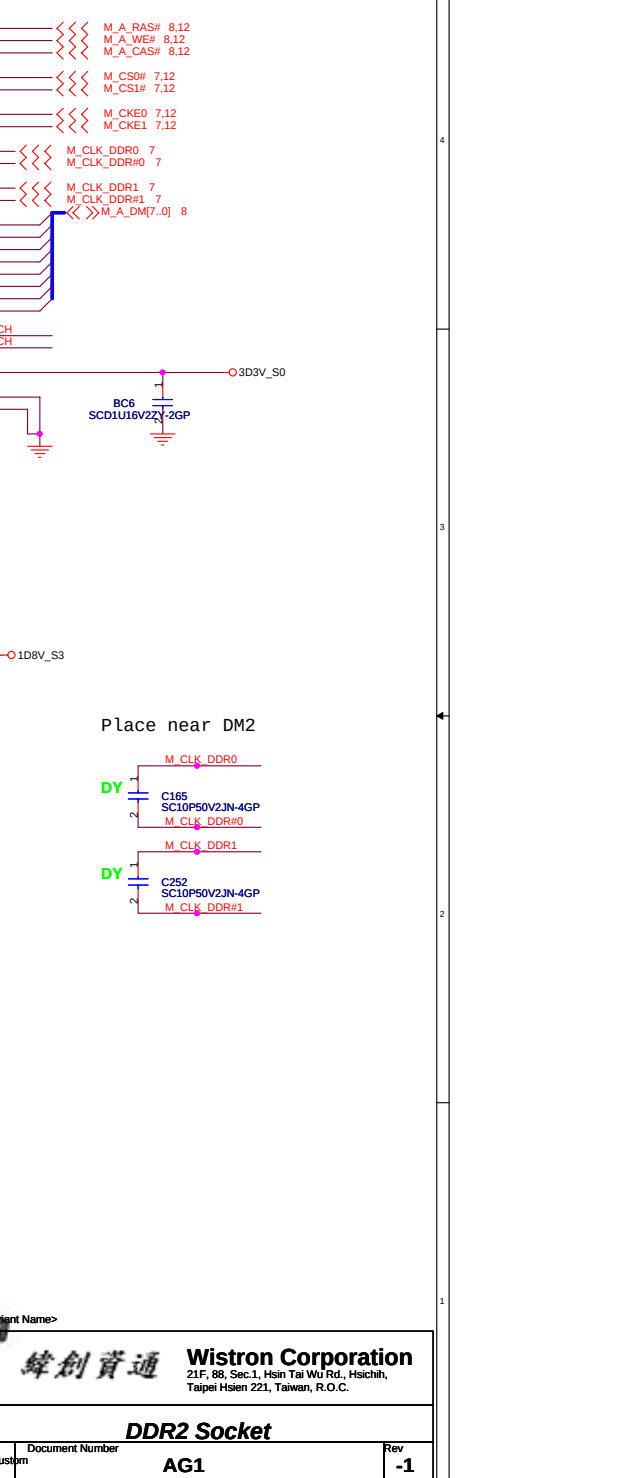
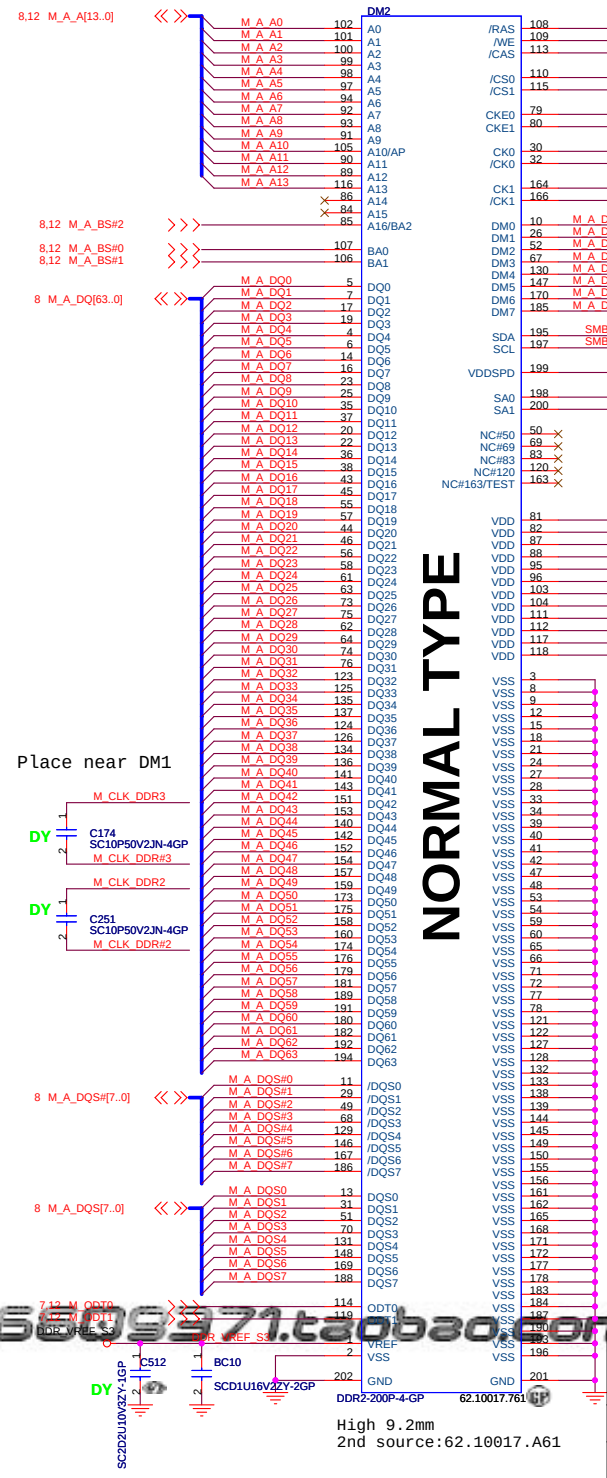
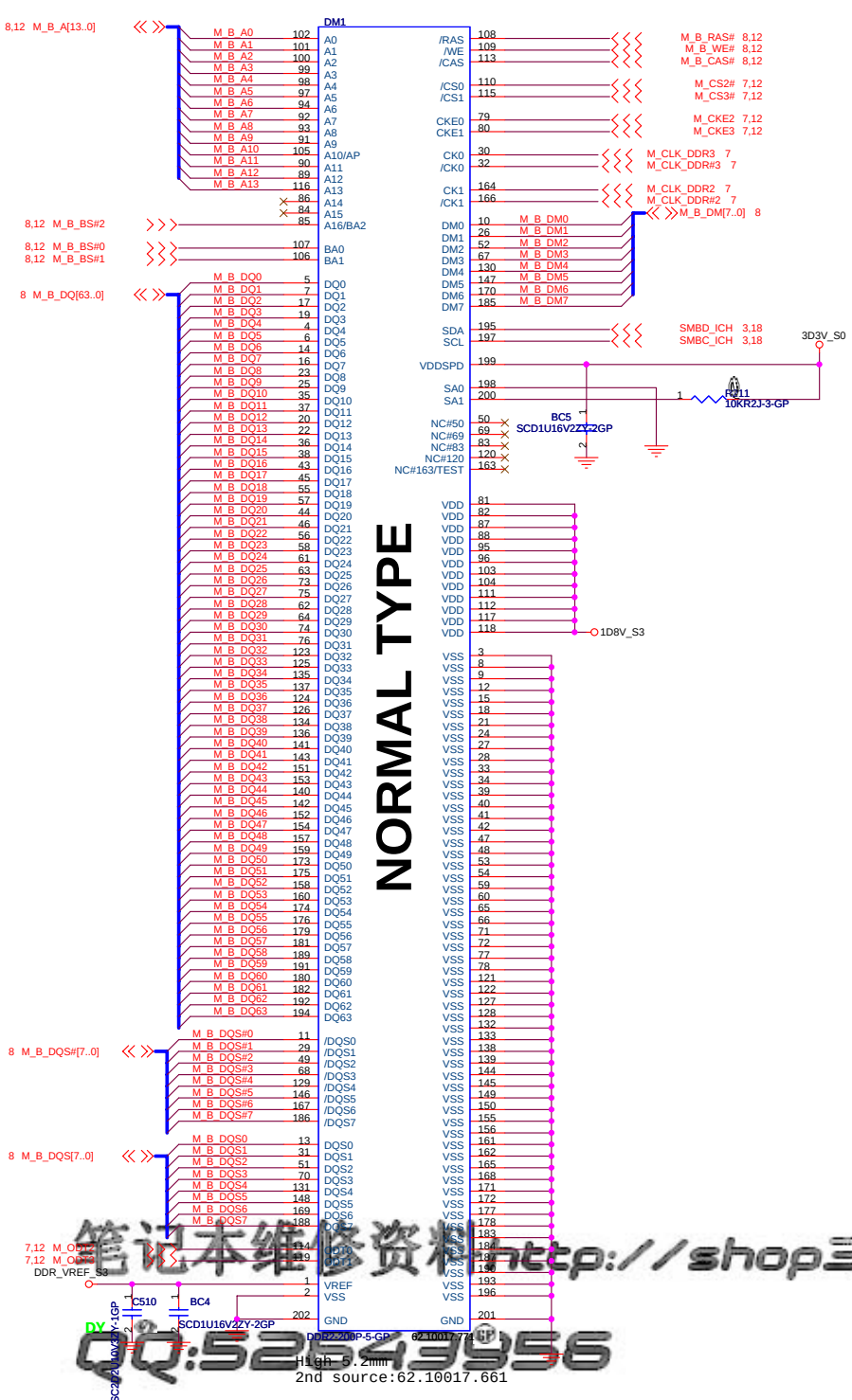
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NORMAL TYPE

NORMAL TYPE



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR2 Socket**

Size: Custom Document Number: **AG1** Rev: **-1**

Date: Wednesday, January 18, 2006 Sheet: 11 of 45

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

RN44

1 M B A12

2 M B A9

SRN56J3-2-GP

M_CKE2 7,11

M_B_BS#2 8,11

M_A_A[13..0] 8,11

M_B_A[13..0] 8,11

R196 2 56R2J-4-GP

R187 2 56R2J-4-GP

R182 2 56R2J-4-GP

R184 56R2J-4-GP

M_ODT1 7,11

M_ODT3 7,11

M_A A9

M B A8

RN47

1 M B A5

2 M B A3

3 M B A1

4 M B A10

SRN56J3-2-GP

RN53

1 M B A13

M_ODT2 7,11

M_CS# 7,11

M_B_RAS# 8,11

RN49

1 M B A0

2 M B A2

3 M B A4

SRN56J3-2-GP

M_B_BS#1 8,11

RN45

1 M B A6

2 M B A7

3 M B A11

SRN56J3-2-GP

M_CKE3 7,11

RN52

1 M B BS#0 8,11

2 M B WE# 8,11

3 M_CS# 7,11

4 M_B_CAS# 8,11

SRN56J3-2-GP

RN54

1 M A A13

M_ODT0 7,11

M_CS# 7,11

M_A_RAS# 8,11

RN50

1 M_A BS#1 8,11

2 M_A A0

3 M_A A2

4 M_A A4

SRN56J3-2-GP

RN51

1 M_A BS#0 8,11

2 M_A WE# 8,11

3 M_A_CAS# 8,11

4 M_CS# 7,11

SRN56J3-2-GP

RN43

1 M_CKE0 7,11

2 M_A_BS#2 8,11

3 M_A A12

4 M_A A8

SRN56J3-2-GP

RN46

1 M_A A6

2 M_A A7

3 M_A A11

SRN56J3-2-GP

M_CKE1 7,11

RN48

1 M_A A5

2 M_A A3

3 M_A A1

4 M_A A10

SRN56J3-2-GP

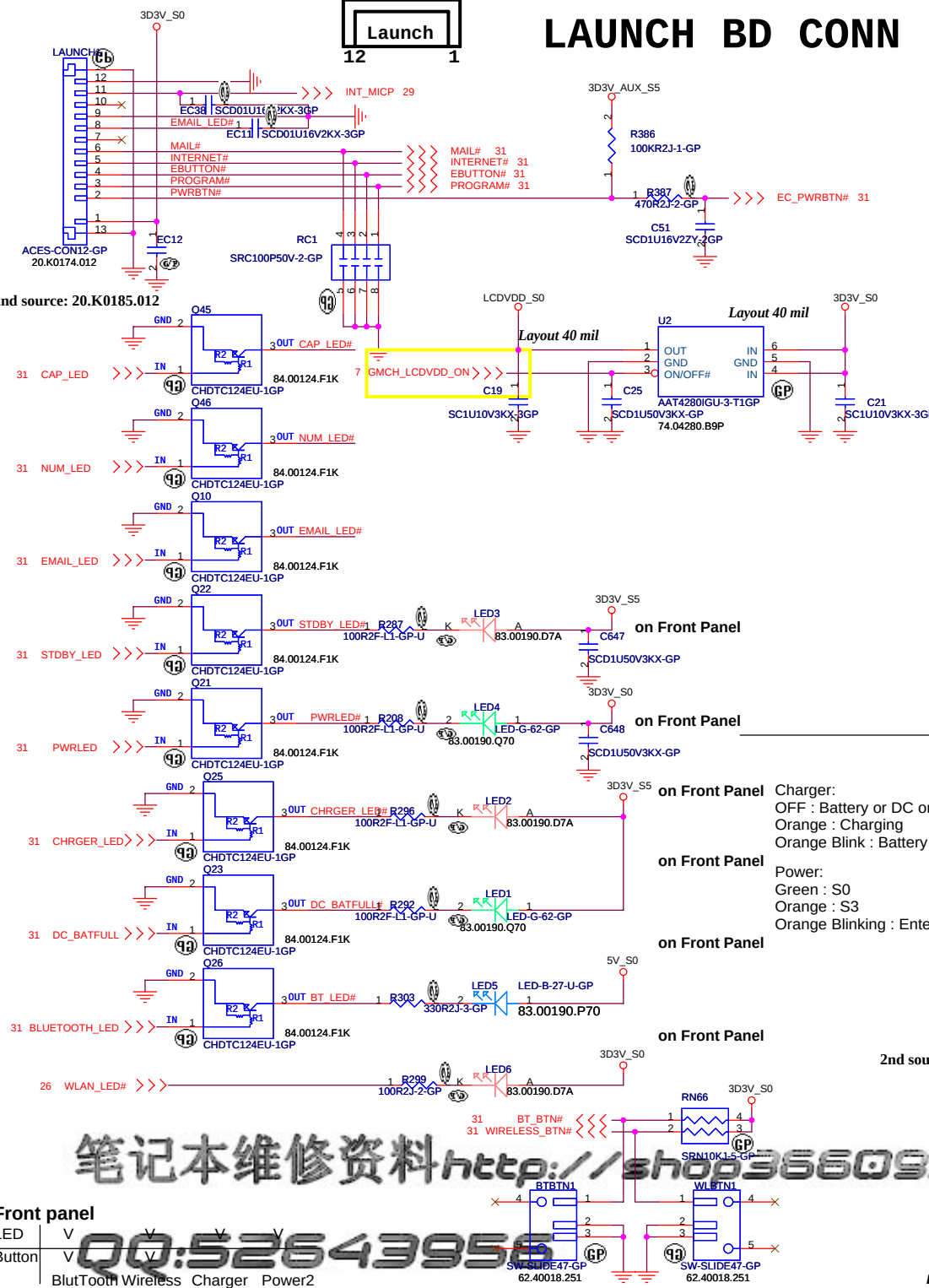
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Title	
DDR2 Termination Resistor	
Size A3	Document Number AG1
Date: Wednesday, January 18, 2006	Sheet 12 of 45 -1

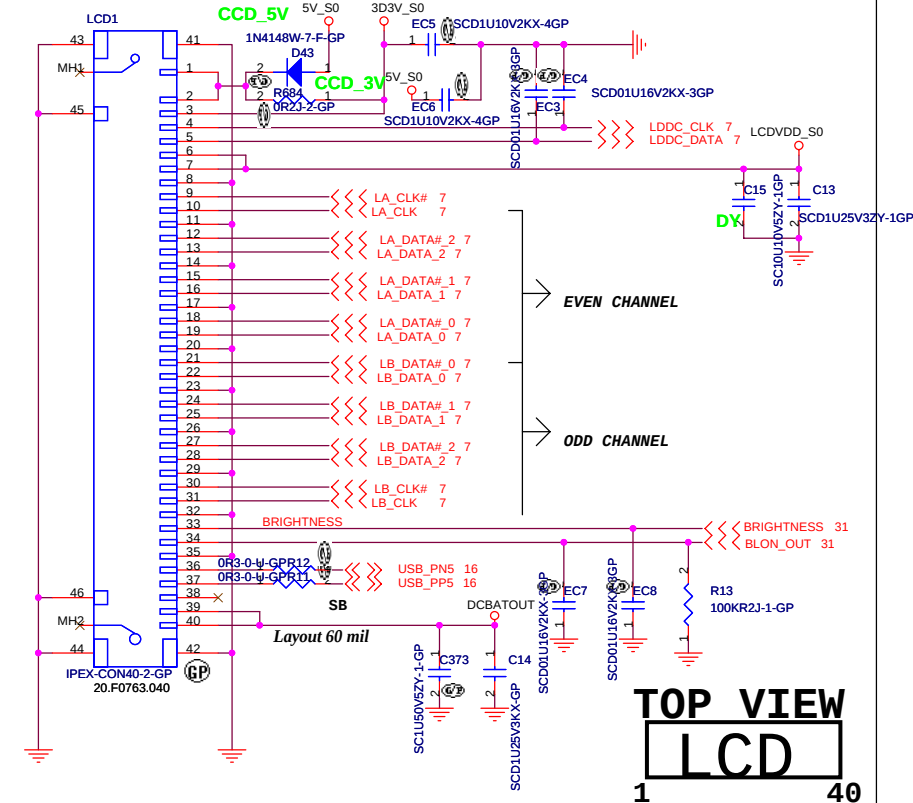
A diagram showing a horizontal timeline with a thick black line. A rectangular box labeled "Launch" is positioned above the timeline. Below the timeline, the number "12" is on the left and "1" is on the right, indicating the start and end of the event.



CCD Pin	
Pin	Symbol
1	5V
2	USB-
3	USB+
4	GND
5	GND

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

Launch BD	
Pin	Symbol
1	3V_S0
2	PWRBTN#
3	PROGRAM#
4	EBUTTON#
5	INTERNET#
6	MAIL#
7	NC
8	MAIL_LED#
9	PWR_B_LED
10	NC
11	INT_MICP
12	INT_MICN



3D3V_S0

LED B1

MLX-CON8-7-GP-U
CONNECTOR
20.K0185.008

228.008

8

1.t30830.com

3

ger

3D3V_S0

EC34 10V2X4GP

CAP_LED#

NUM_LED#

MEDIA_LED#

D39

BAW56PT-U
83.00056.E11

5V_S0

R465
4K7R2J-2-GP

3D3V_S0

R473
10K7J-3-GP

R472
10K7J-3-GP

HDD_LED#

SATA_LED#

15

AG1

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih Taipei Hsien 221, Taiwan, R.O.C.

LCD / LAUNCH / LEDS

AG1

<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

LCD / LAUNCH / LEDs

Size

Document Number

AG1

Rev

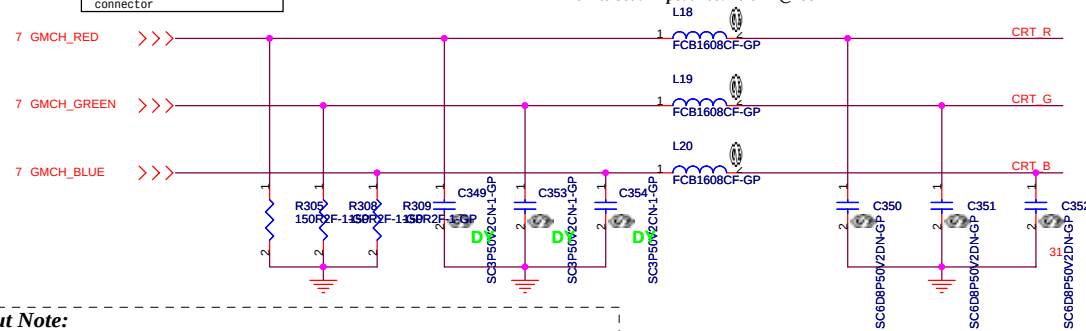
Date: Wednesday, January 18, 2006

Sheet 13 of 45

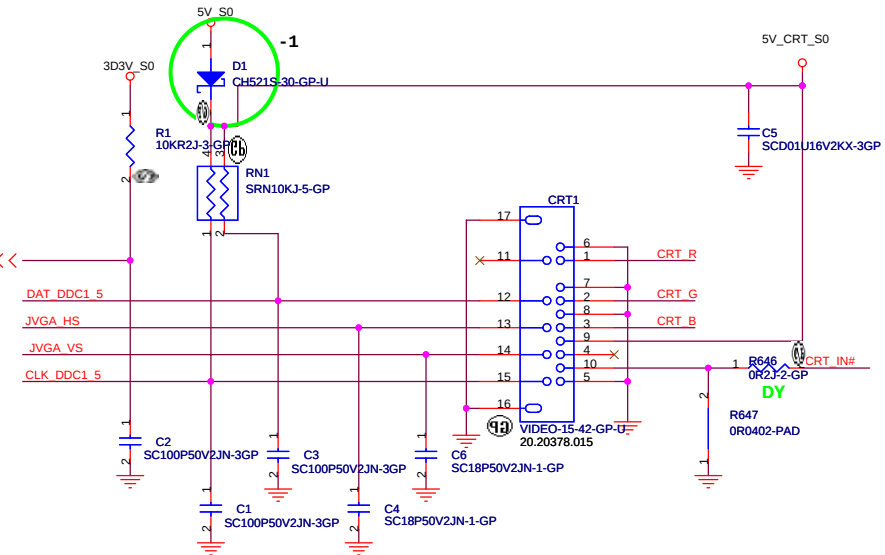
CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector

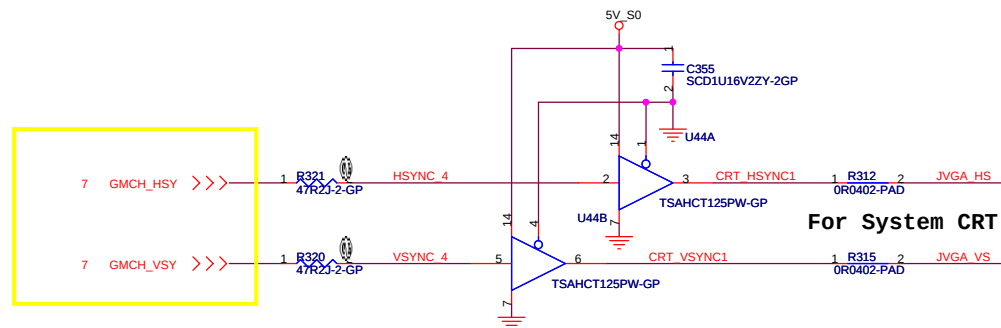
Ferrite bead impedance: 10 ohm@100MHz



Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

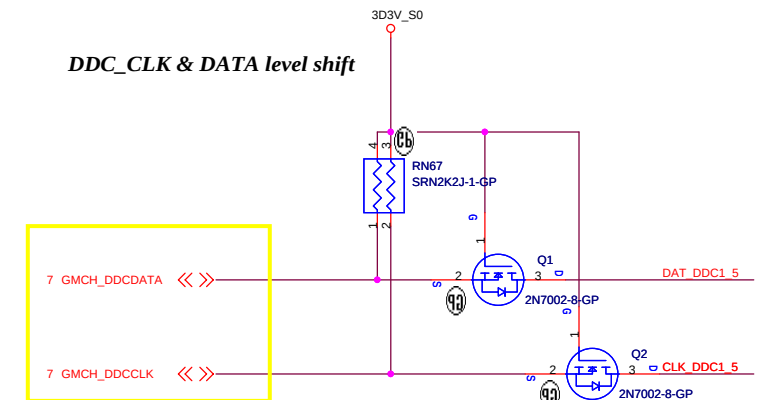


Hsync & Vsync level shift

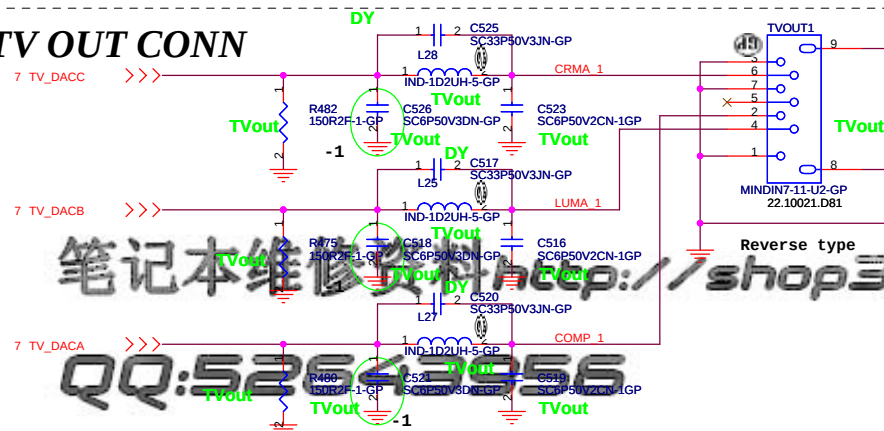


For System CRT

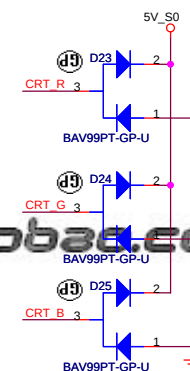
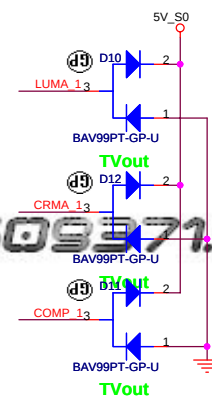
DDC_CLK & DATA level shift



TV OUT CONN



Reverse type



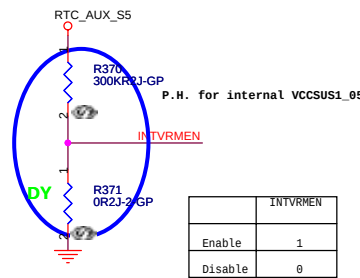
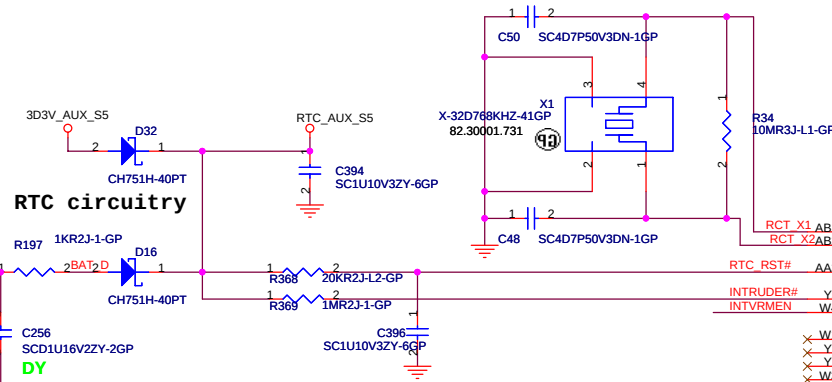
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

CRT/TV Connector		
Size A3	Document Number	Rev
	AG1	-1
Date: Friday, February 24, 2006	Sheet 14	of 45

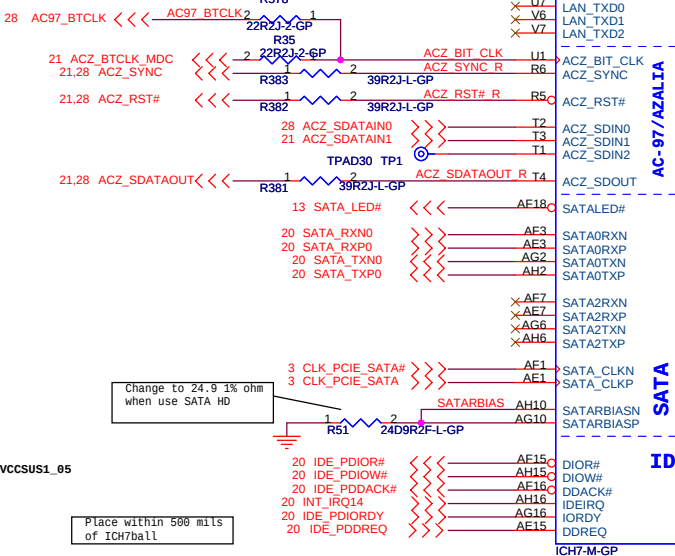
2nd source: 20.D0198.103

RTC circuitry



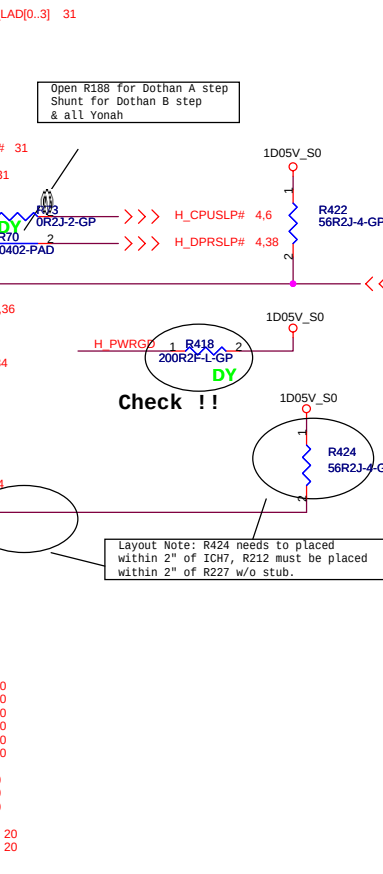
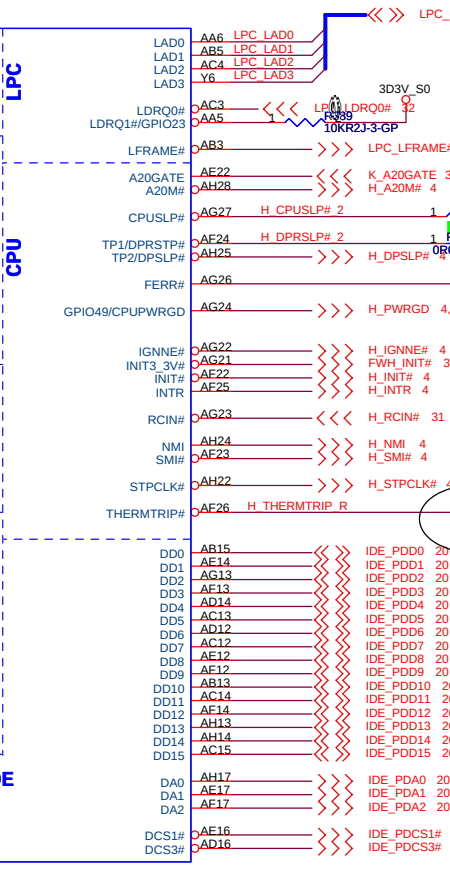
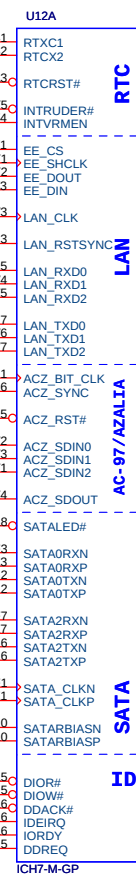
Placement Note:
Distance between the ICH-7 M and cap on the "P" signal
should be identical distance between the ICH-7 M and cap
on the "N" signal for same pair.

	INTVRMEN
Enable	1
Disable	0



Change to 24.9 1% ohm
when use SATA HD

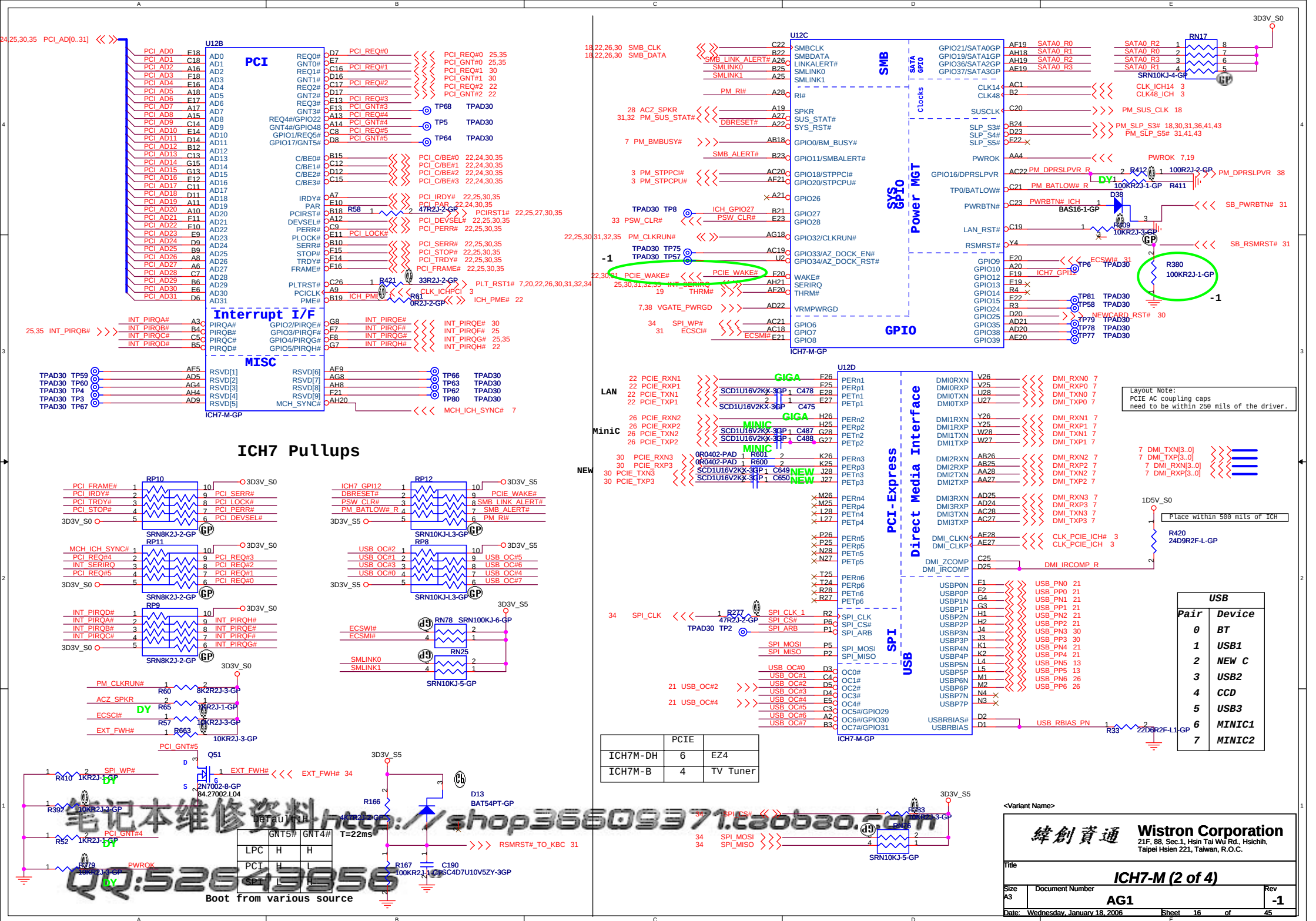
Place within 500 mils
of ICH7ball



Check !!

Layout Note: R424 needs to be placed
within 2" of ICH7, R212 must be placed
within 2" of R227 w/o stub.

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QQ:52643956

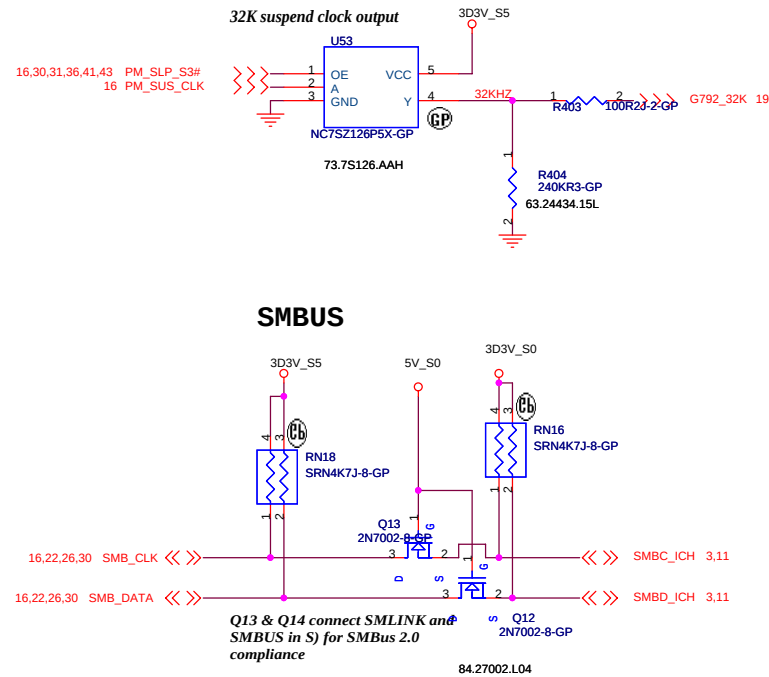




U12E		
A4	VSS[1]	VSS[98]
A23	VSS[2]	VSS[99]
B1	VSS[3]	VSS[100]
B8	VSS[4]	VSS[101]
B11	VSS[5]	VSS[102]
B14	VSS[6]	VSS[103]
B17	VSS[7]	VSS[104]
B20	VSS[8]	VSS[105]
B26	VSS[9]	VSS[106]
B28	VSS[10]	VSS[107]
C2	VSS[11]	VSS[108]
C6	VSS[12]	VSS[109]
C27	VSS[13]	VSS[110]
D10	VSS[14]	VSS[111]
D13	VSS[15]	VSS[112]
D18	VSS[16]	VSS[113]
D21	VSS[17]	VSS[114]
D24	VSS[18]	VSS[115]
E1	VSS[19]	VSS[116]
E2	VSS[20]	VSS[117]
E4	VSS[21]	VSS[118]
E8	VSS[22]	VSS[119]
E15	VSS[23]	VSS[120]
F3	VSS[24]	VSS[121]
F4	VSS[25]	VSS[122]
F5	VSS[26]	VSS[123]
F12	VSS[27]	VSS[124]
F27	VSS[28]	VSS[125]
F28	VSS[29]	VSS[126]
G1	VSS[30]	VSS[127]
G2	VSS[31]	VSS[128]
G5	VSS[32]	VSS[129]
G6	VSS[33]	VSS[130]
G9	VSS[34]	VSS[131]
G14	VSS[35]	VSS[132]
G18	VSS[36]	VSS[133]
G21	VSS[37]	VSS[134]
G24	VSS[38]	VSS[135]
G25	VSS[39]	VSS[136]
G26	VSS[40]	VSS[137]
H3	VSS[41]	VSS[138]
H4	VSS[42]	VSS[139]
H5	VSS[43]	VSS[140]
H24	VSS[44]	VSS[141]
H27	VSS[45]	VSS[142]
H28	VSS[46]	VSS[143]
J1	VSS[47]	VSS[144]
J2	VSS[48]	VSS[145]
J5	VSS[49]	VSS[146]
J24	VSS[50]	VSS[147]
J25	VSS[51]	VSS[148]
J26	VSS[52]	VSS[149]
K24	VSS[53]	VSS[150]
K27	VSS[54]	VSS[151]
K28	VSS[55]	VSS[152]
L13	VSS[56]	VSS[153]
L15	VSS[57]	VSS[154]
L24	VSS[58]	VSS[155]
L25	VSS[59]	VSS[156]
L26	VSS[60]	VSS[157]
M3	VSS[61]	VSS[158]
M4	VSS[62]	VSS[159]
M5	VSS[63]	VSS[160]
M12	VSS[64]	VSS[161]
M13	VSS[65]	VSS[162]
M14	VSS[66]	VSS[163]
M15	VSS[67]	VSS[164]
M16	VSS[68]	VSS[165]
M17	VSS[69]	VSS[166]
M24	VSS[70]	VSS[167]
M27	VSS[71]	VSS[168]
M28	VSS[72]	VSS[169]
N1	VSS[73]	VSS[170]
N2	VSS[74]	VSS[171]
N5	VSS[75]	VSS[172]
N6	VSS[76]	VSS[173]
N11	VSS[77]	VSS[174]
N12	VSS[78]	VSS[175]
N13	VSS[79]	VSS[176]
N14	VSS[80]	VSS[177]
N15	VSS[81]	VSS[178]
N16	VSS[82]	VSS[179]
N17	VSS[83]	VSS[180]
N18	VSS[84]	VSS[181]
N24	VSS[85]	VSS[182]
N25	VSS[86]	VSS[183]
N26	VSS[87]	VSS[184]
P3	VSS[88]	VSS[185]
P4	VSS[89]	VSS[186]
P12	VSS[90]	VSS[187]
P13	VSS[91]	VSS[188]
P14	VSS[92]	VSS[189]
P15	VSS[93]	VSS[190]
P16	VSS[94]	VSS[191]
P17	VSS[95]	VSS[192]
P24	VSS[96]	VSS[193]
P27	VSS[97]	VSS[194]

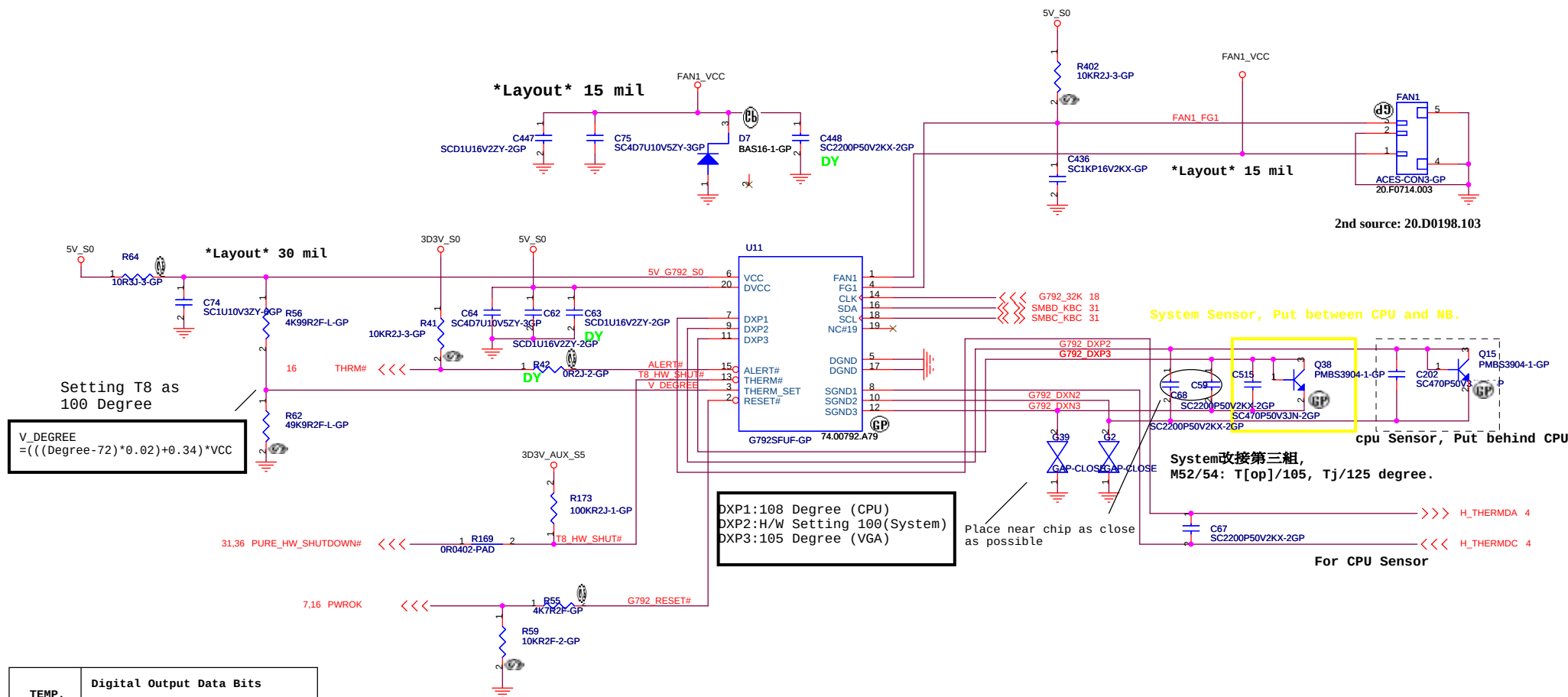
ICH7-MGP

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QQ:52643956



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
ICH7-M (4 of 4)/ODD		
Size	Document Number	Rev
A3	AG1	-1
Date: Wednesday, January 18, 2006 Sheet 18 of 45		



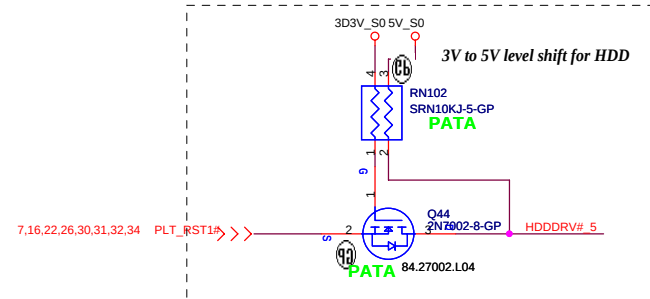
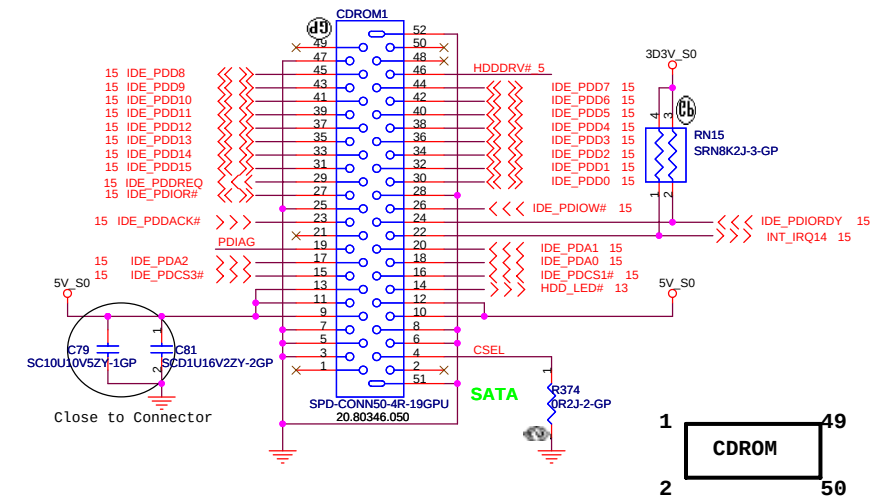
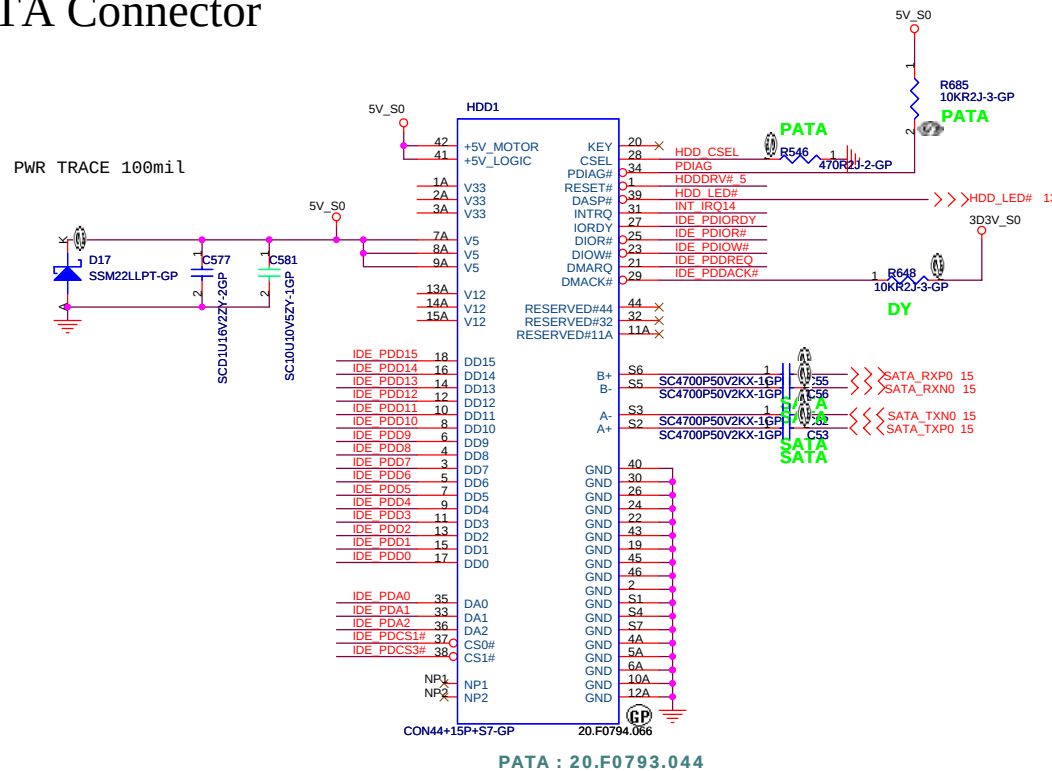
TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0111	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

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CDROM Connector

PWR TRACE 100mil



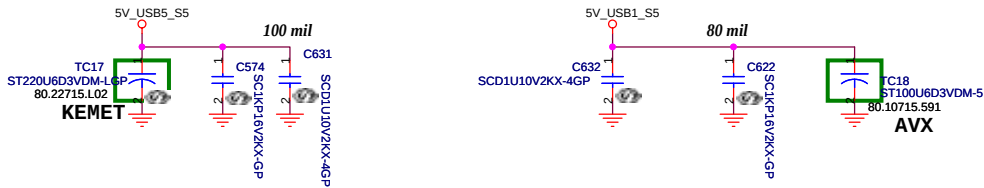
笔记本维修资料<http://shop36609371.taobao.com>

QQ:52643956

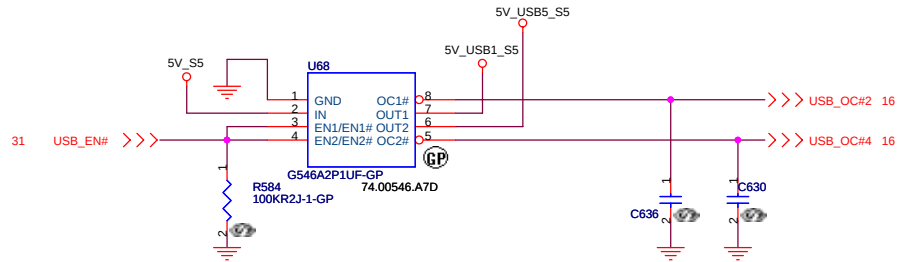
<Variant Name>

緯創資通

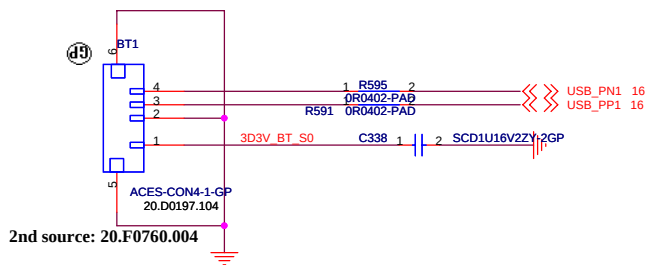
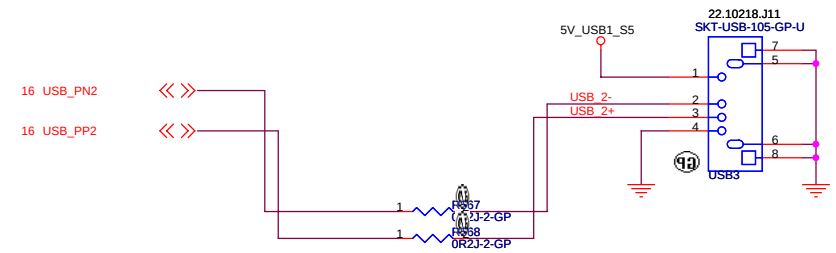
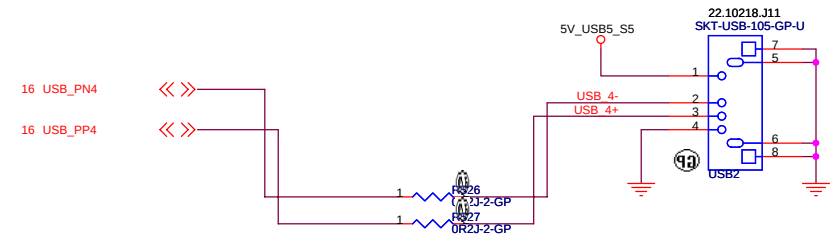
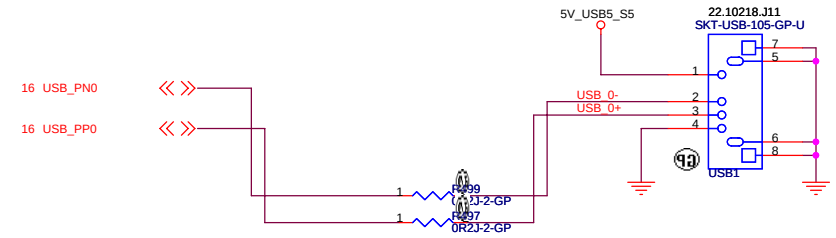
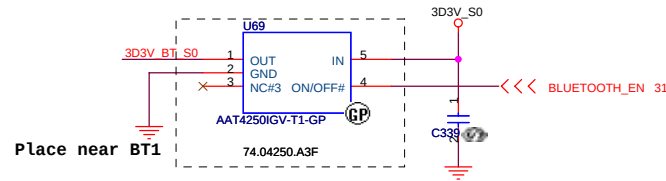
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.



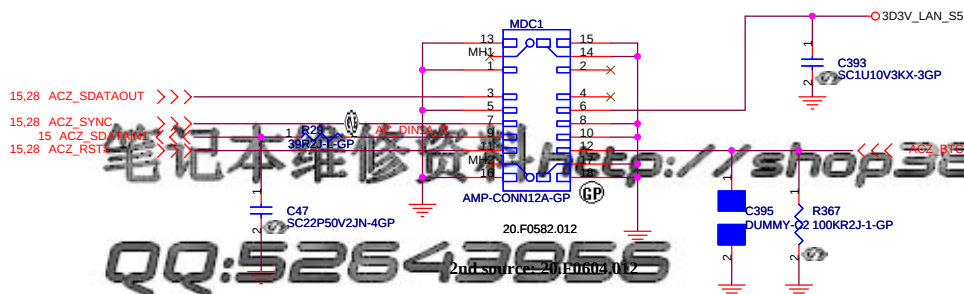
USB PORT



BLUETOOTH MODULE CONNECTOR



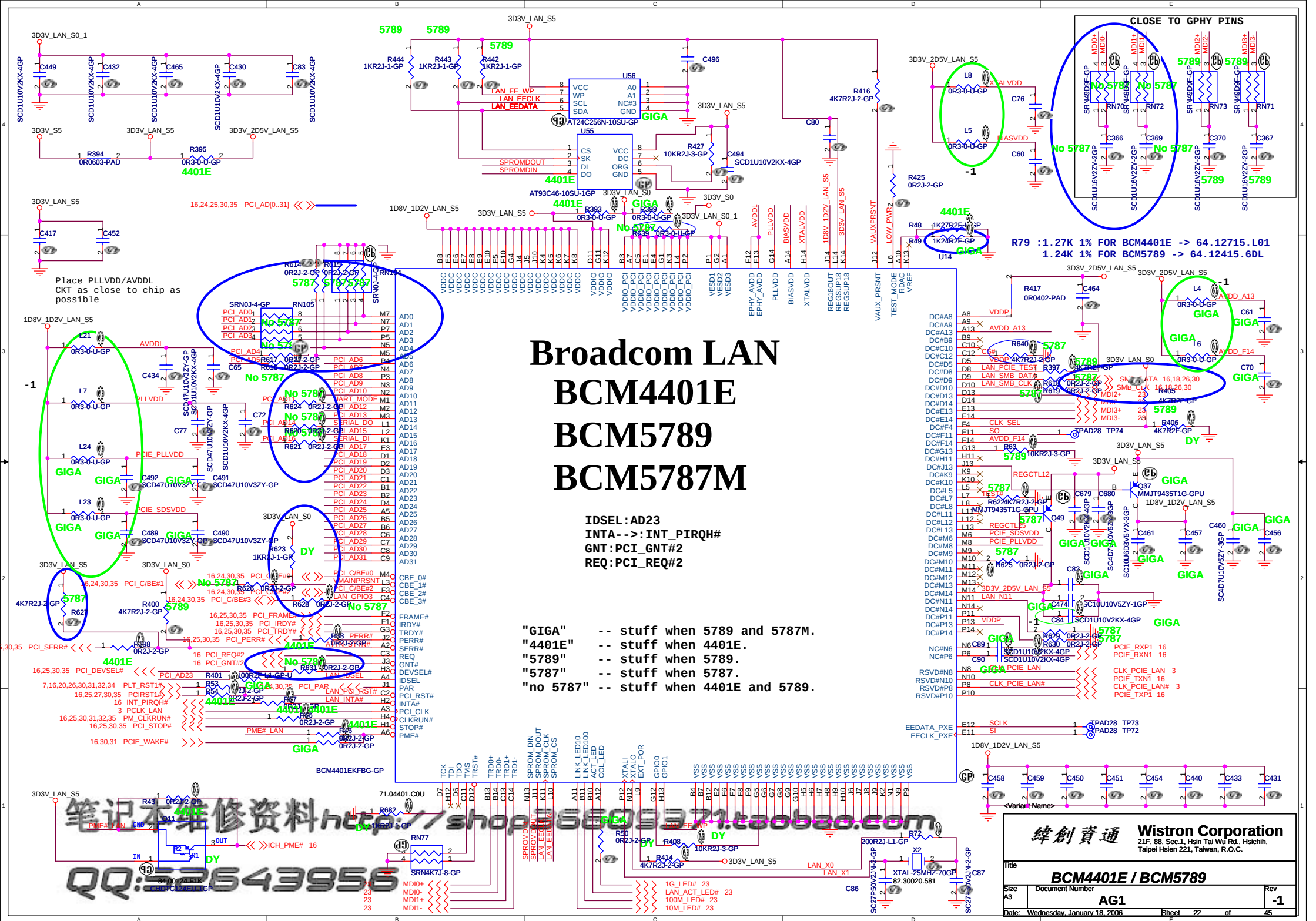
MDC 1.5 CONN



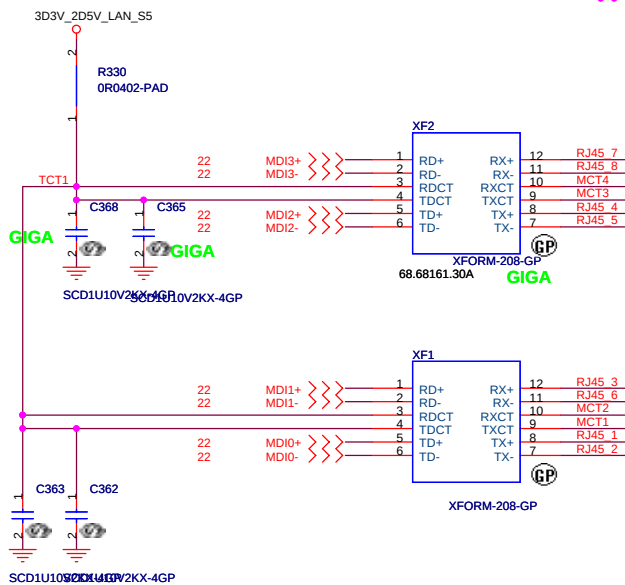
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
USB and MDC I/F		
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Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	



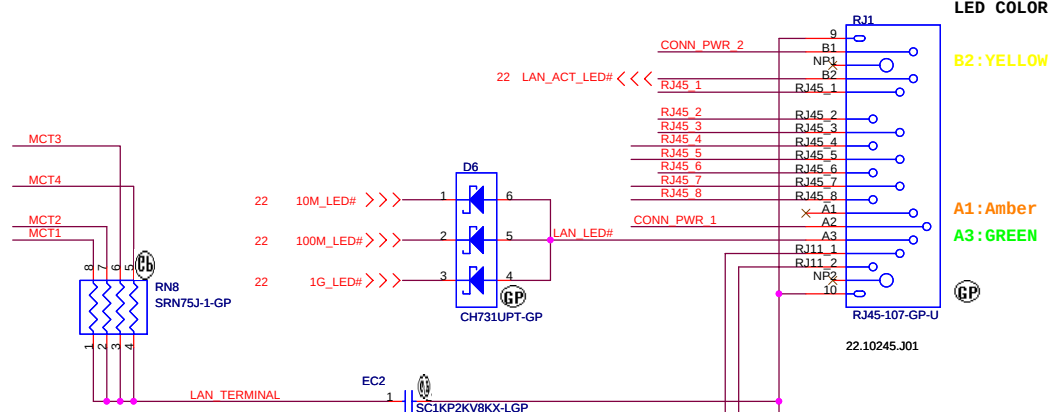
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

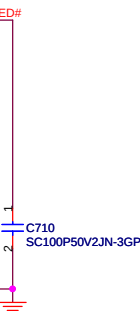
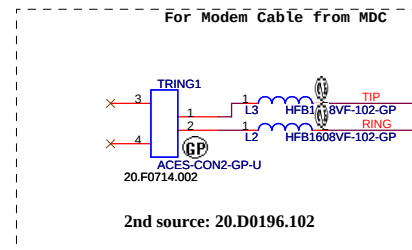
10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

LAN Connector



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transferring data.



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QQ:52643956

<Variant Name>

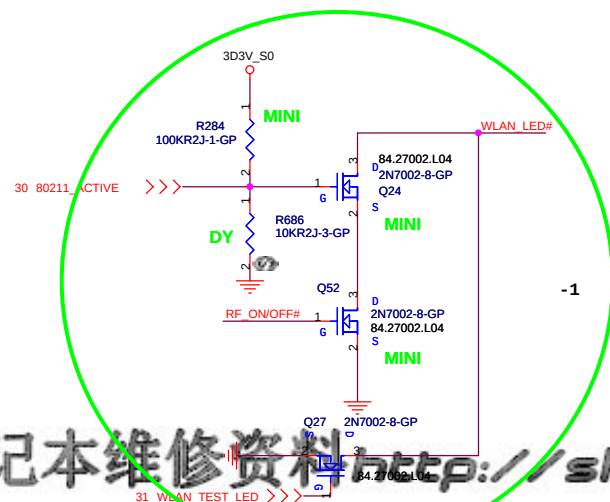
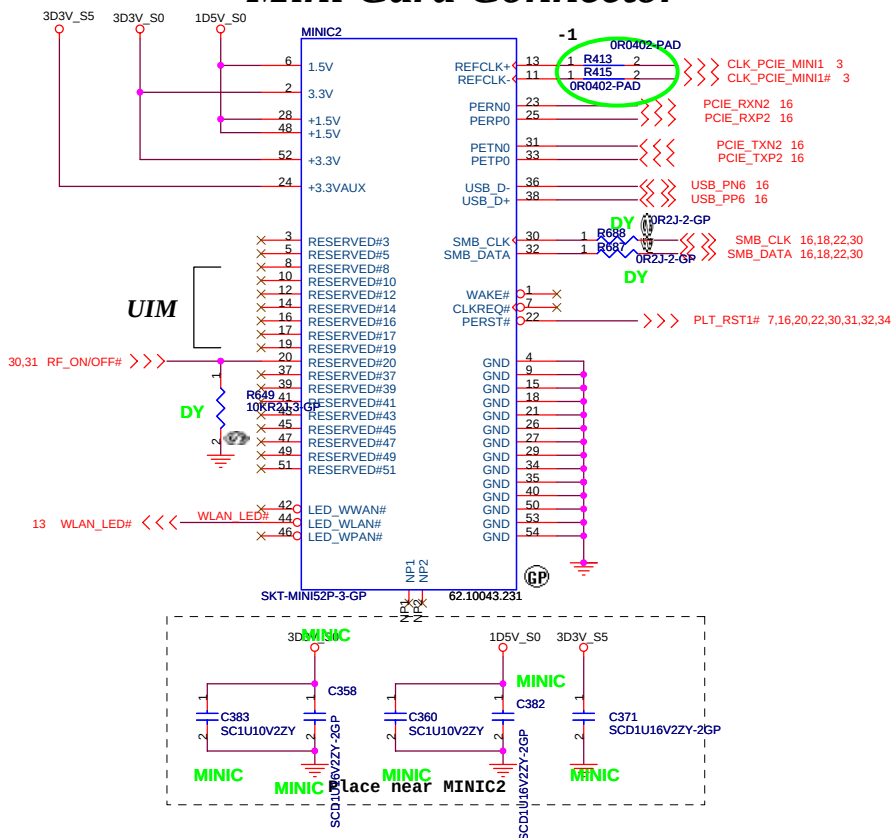
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size A3 Document Number **AG1** Rev **-1**

Date: Wednesday, January 18, 2006 Sheet 23 of 45

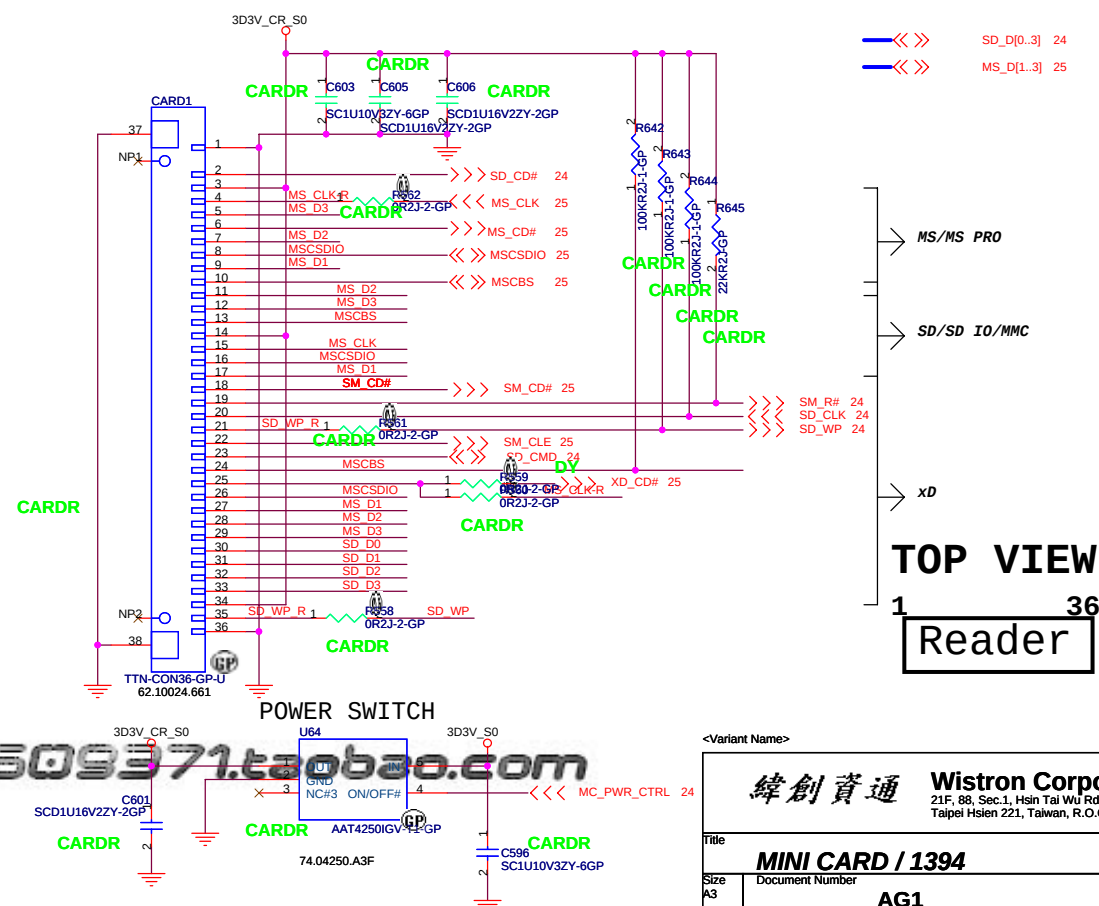
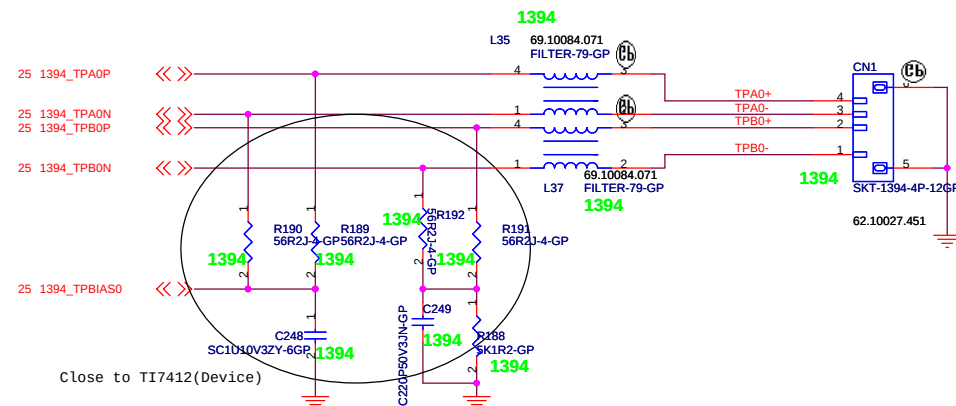
Mini Card Connector



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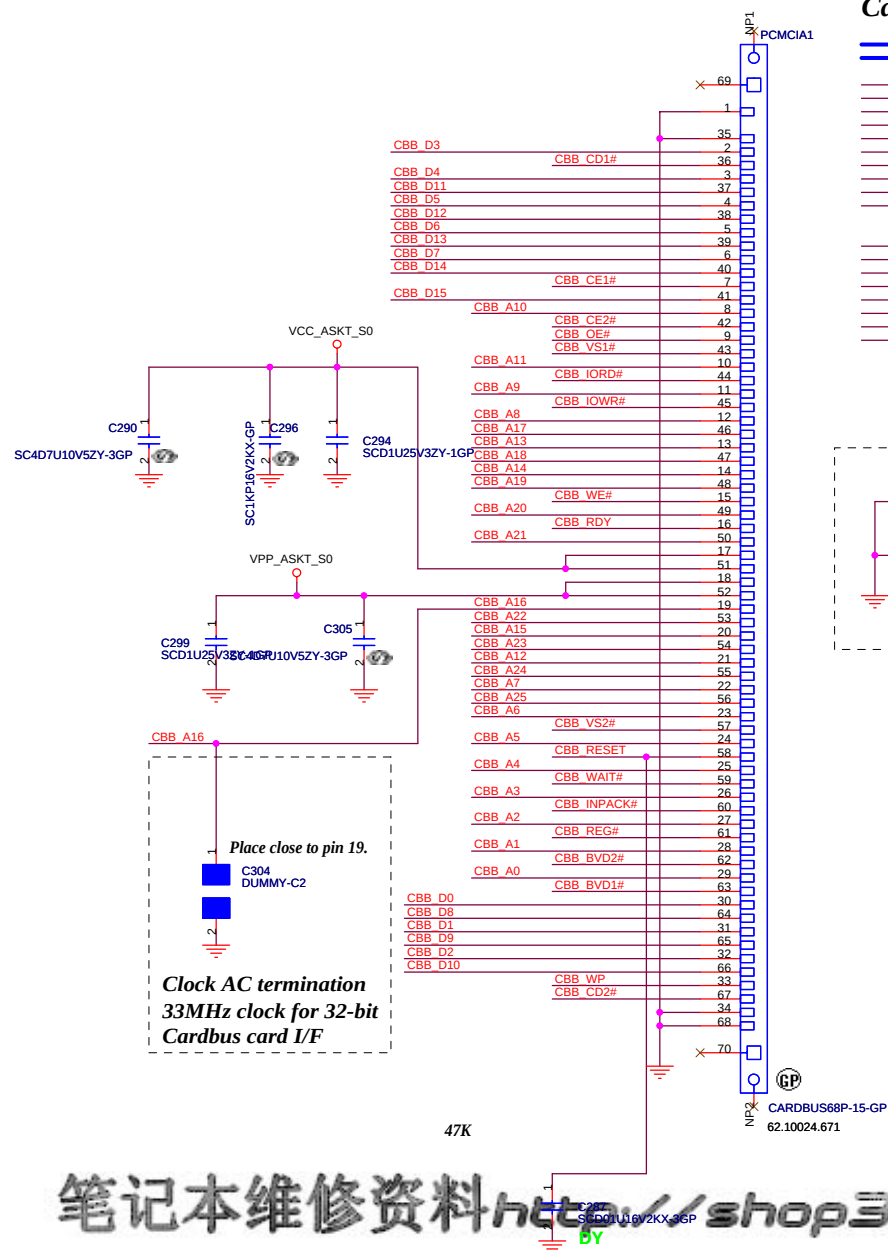
QQ:52643956

1394 Connector

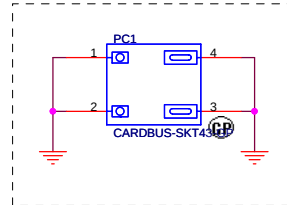
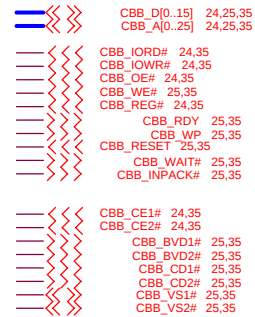


<Variant Name>			
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MINI CARD / 1394			
Size A3	Document Number		Rev -1
AG1			
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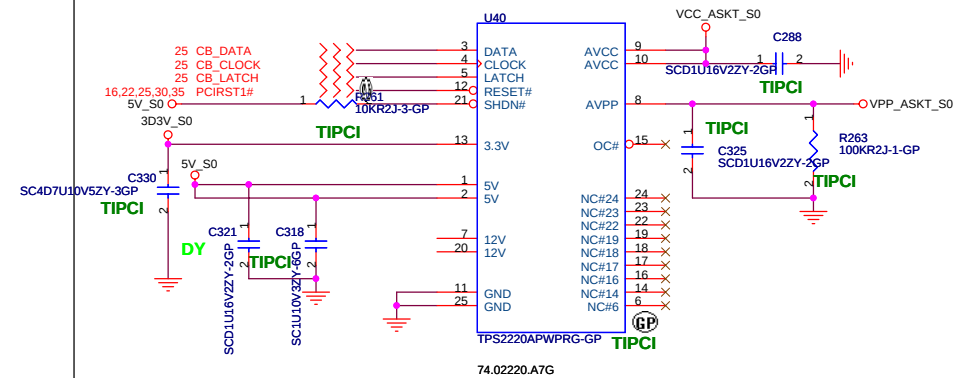
PCMCIA Socket



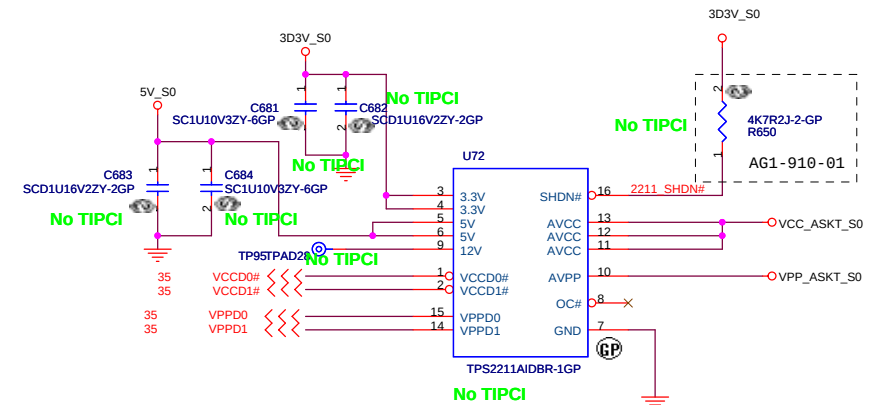
Cardbus I/F



TI Power switch



ENE Power switch



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QQ:52643956

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCMCIA
-------	---------------

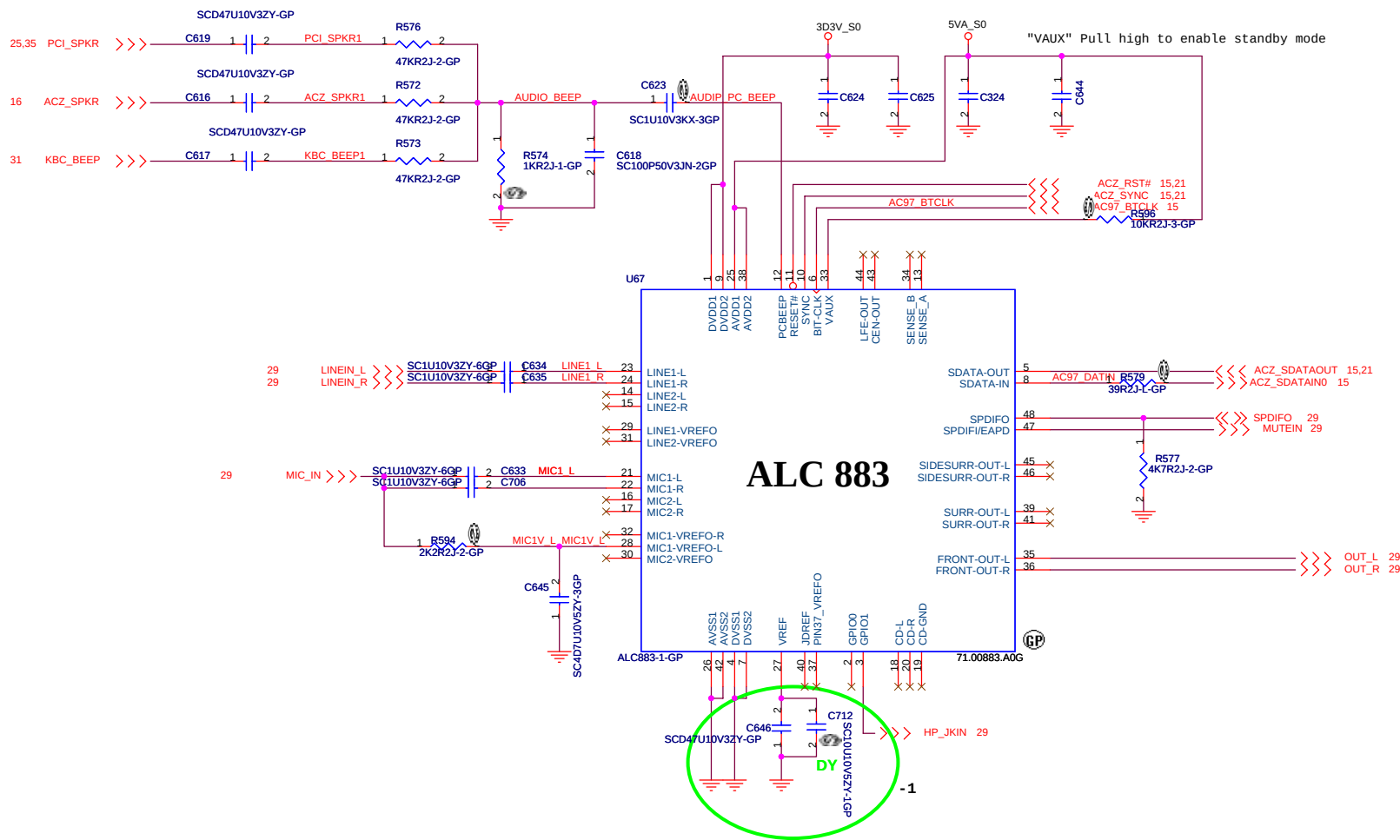
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AG1

Rev 1

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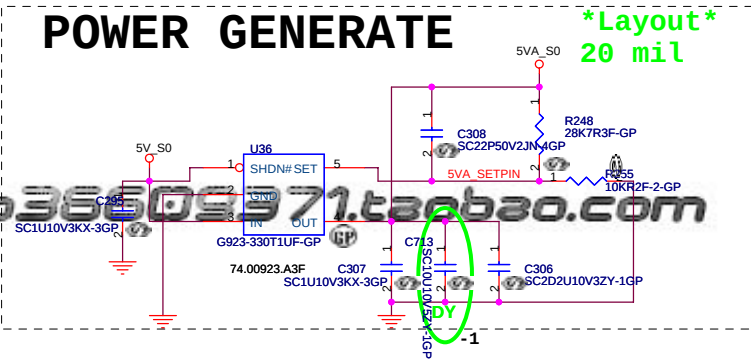
- 1) When GPIO0 is asserted, AMP should be muted.
- 2) SPDIFO should be turned off when not used.

Configuration:
(3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.

Pin	Symbol	Location	Re-tasking
35/36	FRONT	AMP, Jack1	AMP output, line input
39/41	SURR	X	X
43/44	GEN/LEFT	X	SURR_VREF0-L/R
45/46	SIDESURR	X	SIDESURR-L is MIC2-VREF0-R, SIDESURR-R is LINE2-VREF0-R
23/24	LINE1	Jack 2	Line input, line output
21/22	MIC1	Jack 3	Mic input, line output
14/15	LINE2	X	X
16/17	MIC2	Int. Mic	Mic input

POWER GENERATE

Layout
20 mil



<Variant Name>

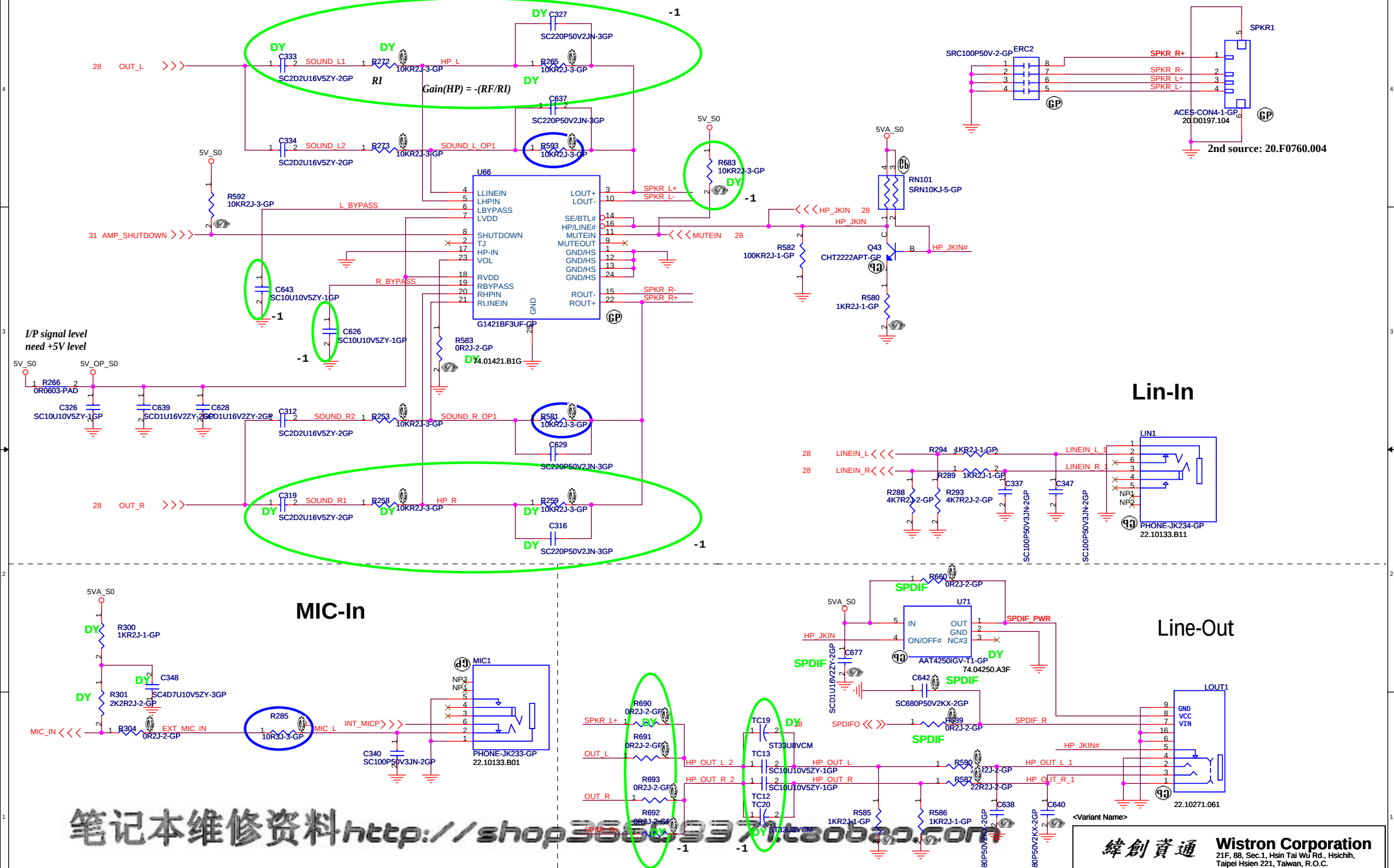
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title Azalia codec ALC883

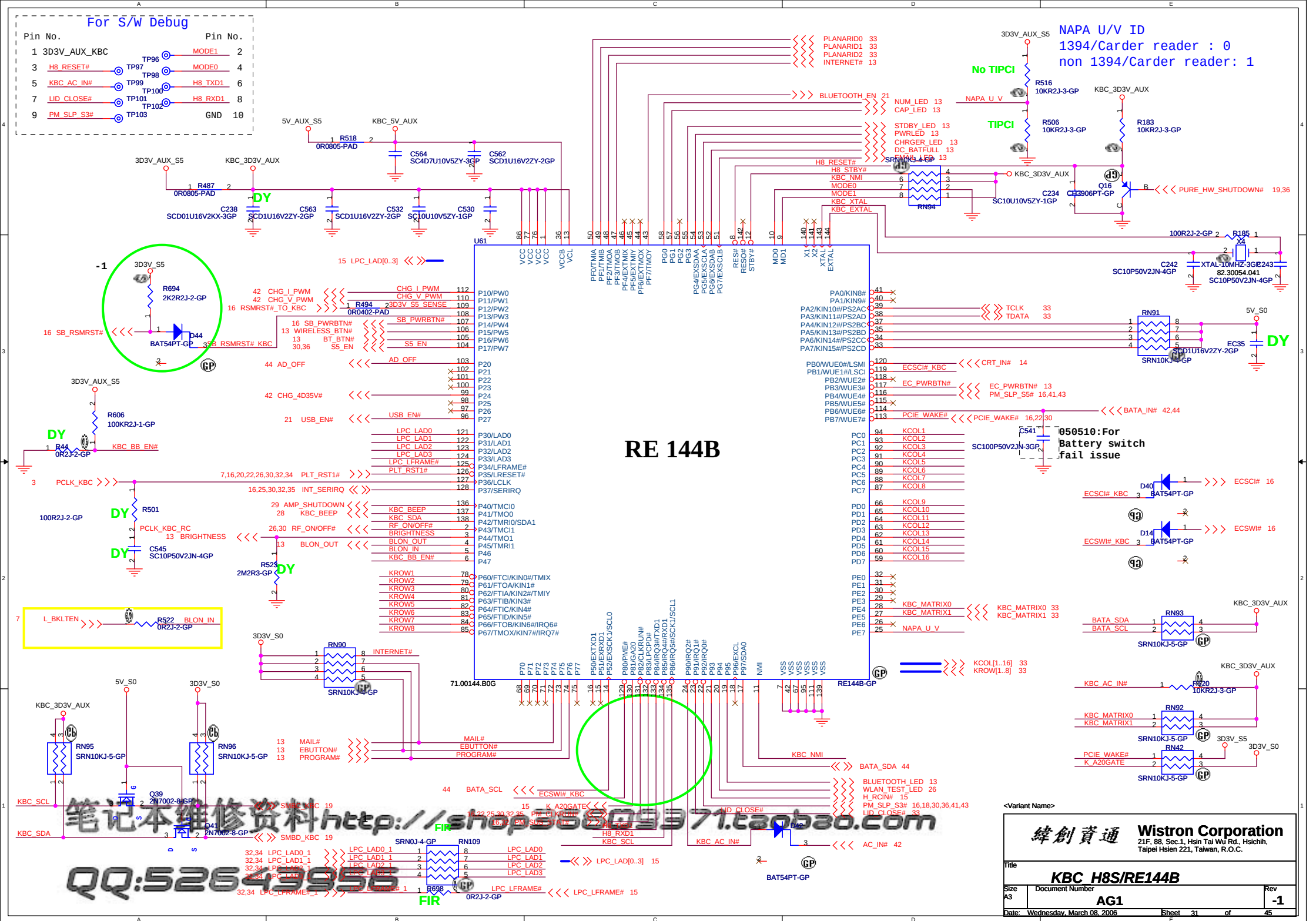
Size A3 Document Number AG1 Rev -1

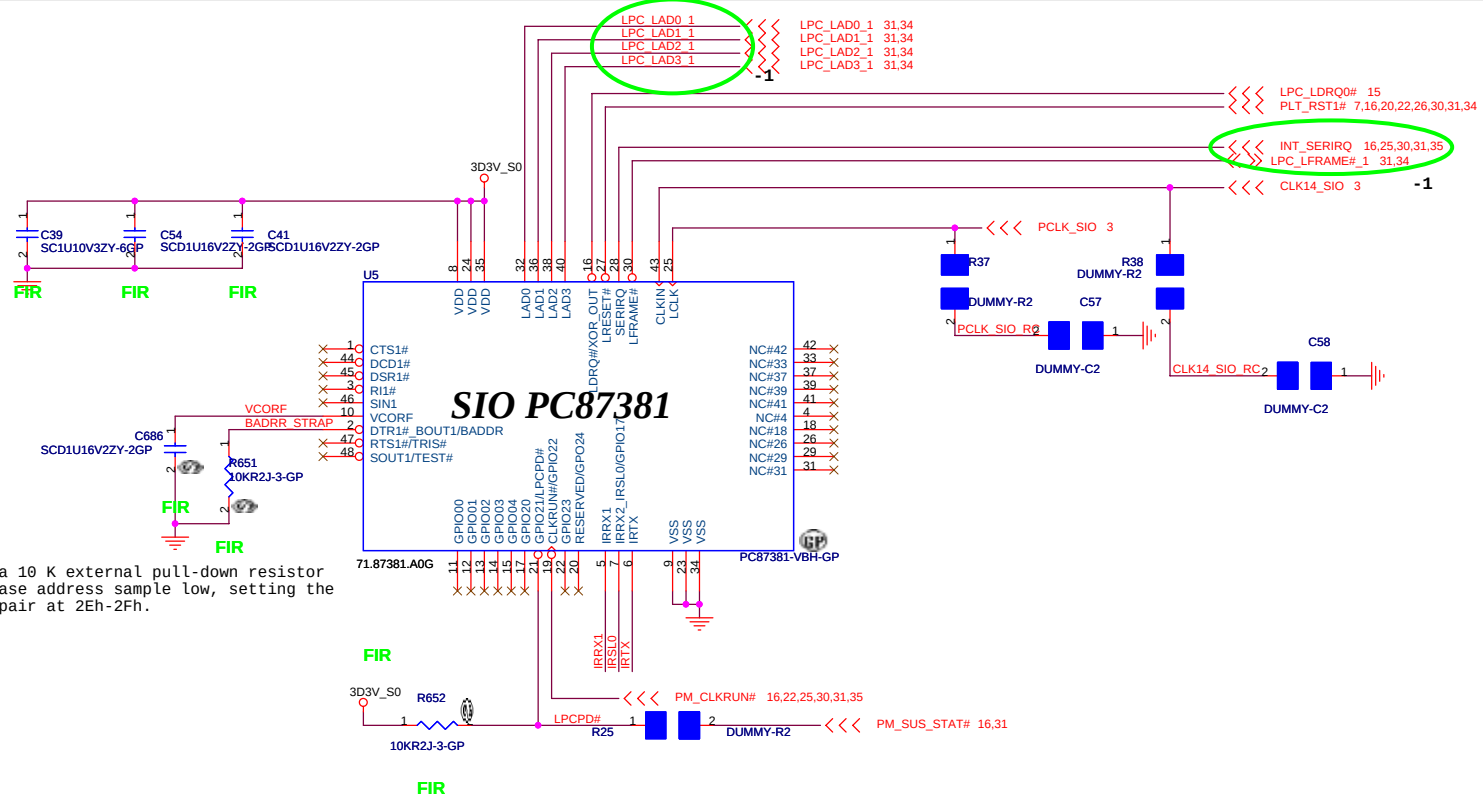
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AUDIO OP AMPLIFIER



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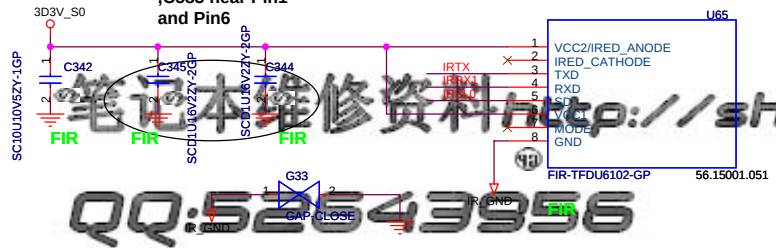


Connecting a 10 K external pull-down resistor makes the base address sample low, setting the Index-Data pair at 2Eh-2Fh.

VISHAY FIR/CIR Module

Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close
to U32

Place C581
,C583 near Pin1
and Pin6



<Variant Name>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

SIO 87392 / FIR

Size
A3

Document Number

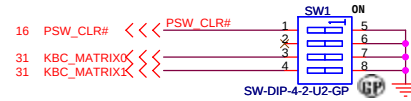
AG1

Rev
-1

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Internal KeyBoard Connector



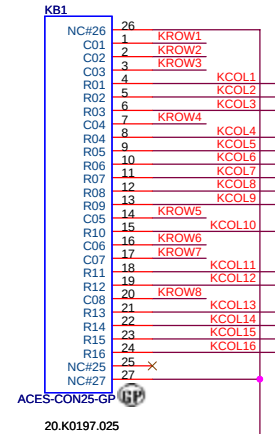
Keyboard matrix (from vendor)

	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0

PSW_CLR#	Low Active
1 - 5 ON	
KBC_BB_EN#	2 - 6 ON
KBC_MATRIX1	3 - 7 ON
KBC_MATRIX2	4 - 8 ON

31 KROW[1..8] <<<

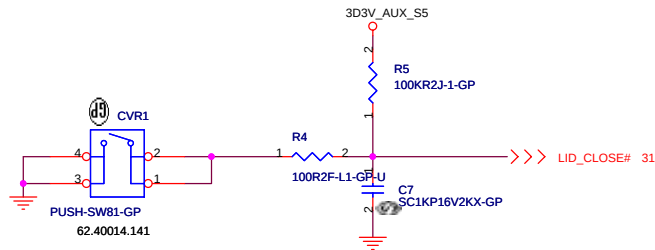
31 KCOL[1..16] <<<



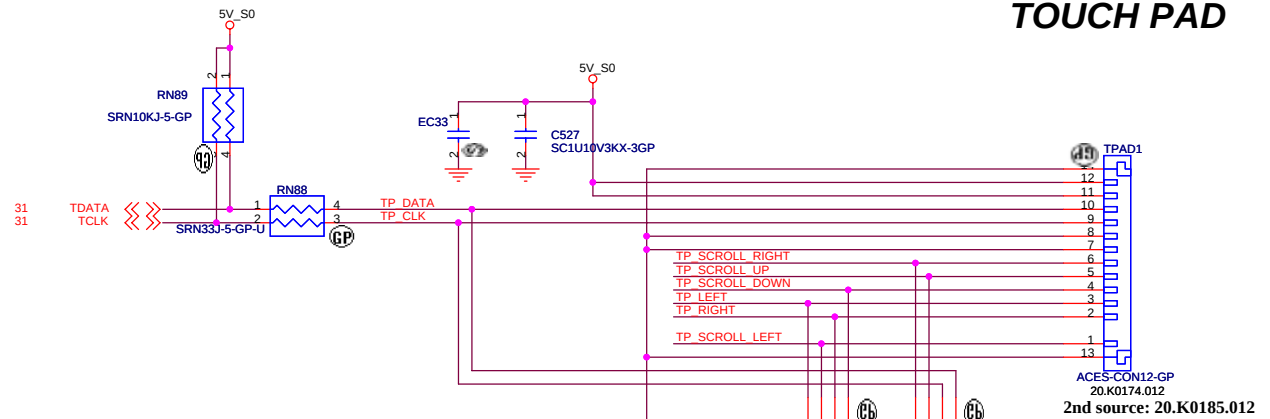
2nd source: 20.K0198.025



COVER SWITCH

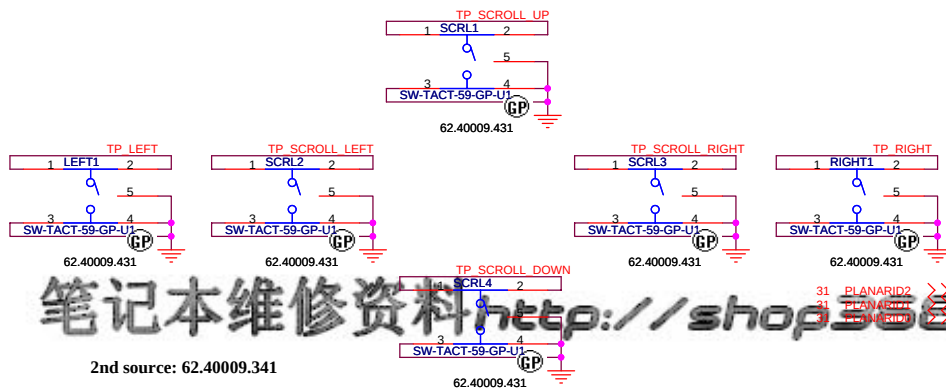


TOUCH PAD



2nd source: 20.K0185.012

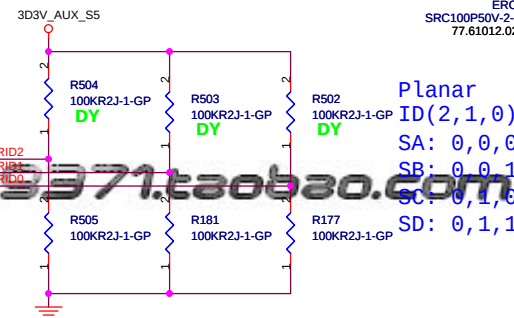
SCROLL KEY



2nd source: 62.40009.431

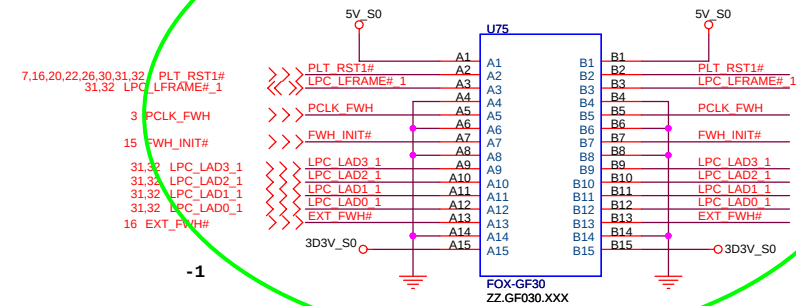
笔记本维修资料 <http://shop3509371.taobao.com>

QQ:52643956



Planar
ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1

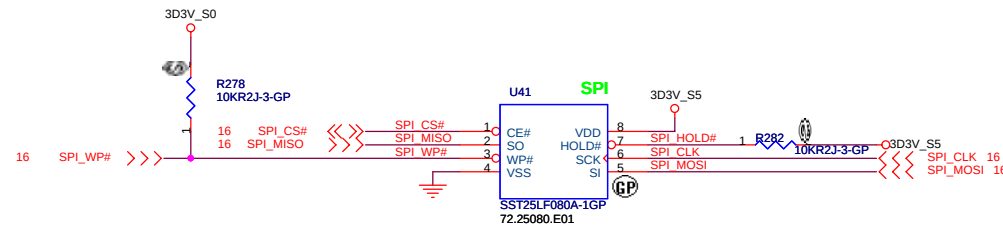
GOLDEN FINGER FOR DEBUG BOARD



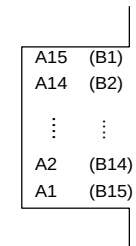
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

SPI FLASH ROM

8M Bits



TOP VIEW



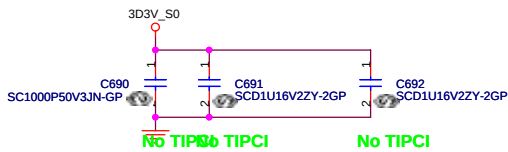
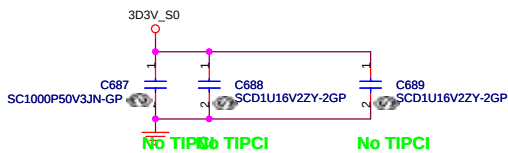
(BOTTOM VIEW)

SOIC 200 Socket P/N:
Wieson: 62.10076.001
SPI ROM:
SST25LF080A: 72.25080.E01
SST25VF080B : 72.25080.G01
ST M25P80: 72.25P80.001

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QQ:52643956

<Variant Name>

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Title	
BIOS : SPI	
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16,22,24,25,30 PCI_AD[0..31]

PCI_AD31 3
PCI_AD30 4
PCI_AD29 5
PCI_AD28 7
PCI_AD27 8
PCI_AD26 9
PCI_AD25 11
PCI_AD24 10
PCI_AD23 15
PCI_AD22 16
PCI_AD21 17
PCI_AD20 19
PCI_AD19 23
PCI_AD18 24
PCI_AD17 25
PCI_AD16 26
PCI_AD15 38
PCI_AD14 39
PCI_AD13 40
PCI_AD12 41
PCI_AD11 43
PCI_AD10 45
PCI_AD9 46
PCI_AD8 47
PCI_AD7 49
PCI_AD6 51
PCI_AD5 52
PCI_AD4 53
PCI_AD3 54
PCI_AD2 55
PCI_AD1 56
PCI_AD0 57

16,22,24,30 PCI_C/BE#3
16,22,24,30 PCI_C/BE#2
16,22,24,30 PCI_C/BE#1
16,22,24,30 PCI_C/BE#0

16,22,25,30 PCI_FRAME#
16,22,25,30 PCI_IRDY#
16,22,25,30 PCI_TRDY#
16,22,25,30 PCI_STOP#

16,22,25,30 PCI_DEVSEL#
16,22,25,30 PCI_PERR#
16,22,25,30 PCI_SERR#
16,22,24,30 PCI_PAR

16,22,25,27,30 PCIRST1#

16,25 PCI_GNT#0
16,25 PCI_REQ#0

16,25 PCI_GNT#1
16,25 PCI_REQ#1

16,25 PCI_GNT#2
16,25 PCI_REQ#2

16,25 PCI_GNT#3
16,25 PCI_REQ#3

16,25 PCI_GNT#4
16,25 PCI_REQ#4

16,25 PCI_GNT#5
16,25 PCI_REQ#5

16,25 PCI_GNT#6
16,25 PCI_REQ#6

16,25 PCI_GNT#7
16,25 PCI_REQ#7

16,25 PCI_GNT#8
16,25 PCI_REQ#8

16,25 PCI_GNT#9
16,25 PCI_REQ#9

16,25 PCI_GNT#10
16,25 PCI_REQ#10

16,25 PCI_GNT#11
16,25 PCI_REQ#11

16,25 PCI_GNT#12
16,25 PCI_REQ#12

16,25 PCI_GNT#13
16,25 PCI_REQ#13

3D3V_S0

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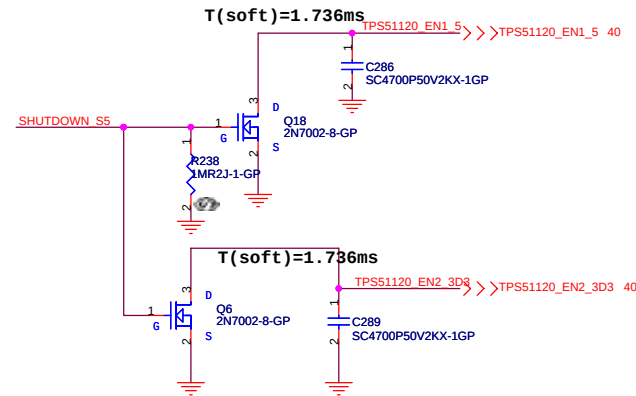
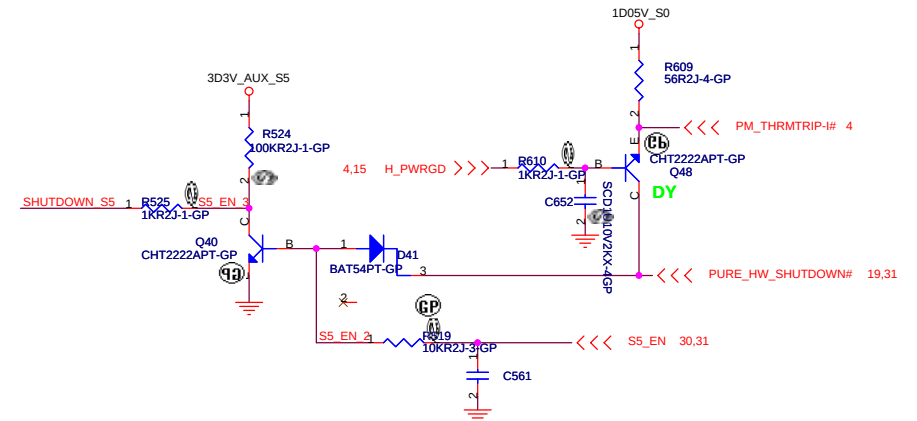
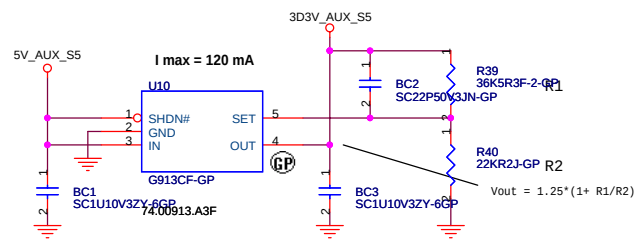
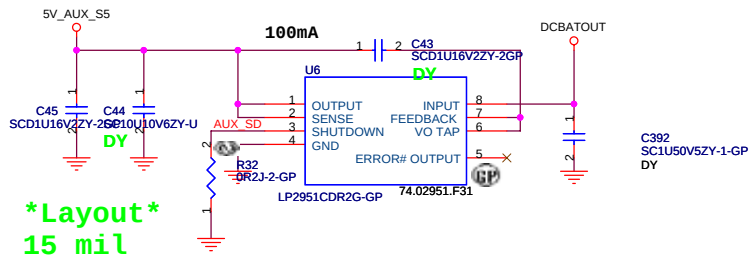
3D3V_S0

3D3V_S0

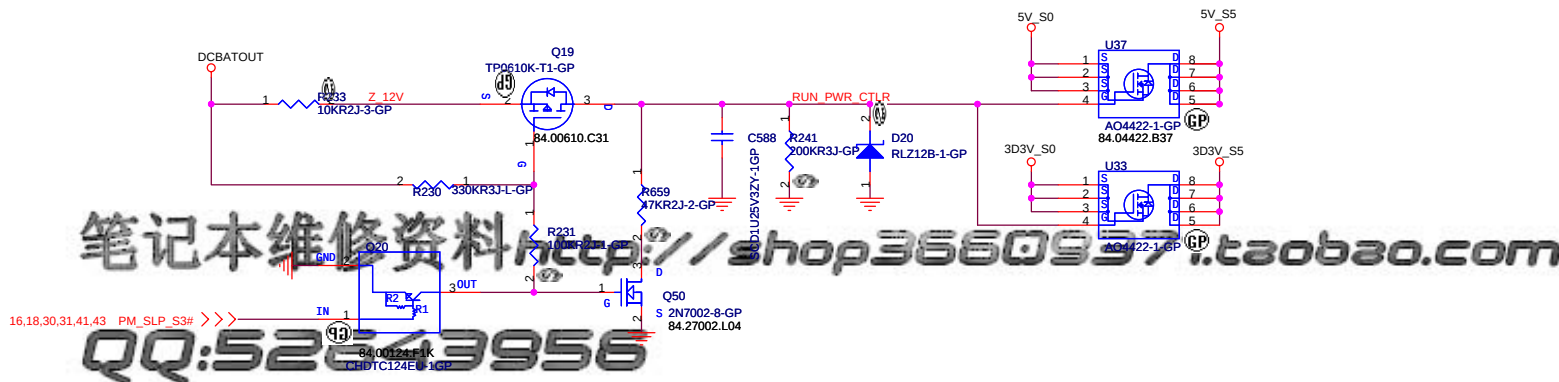
3D3V_S0

3D3V_S0

Aux Power



Run Power

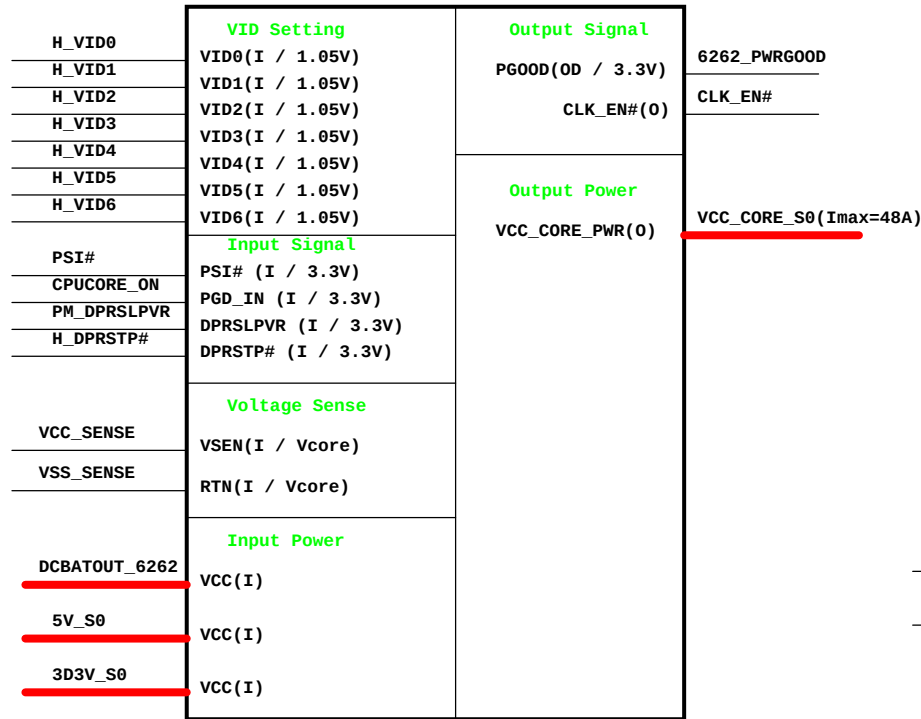


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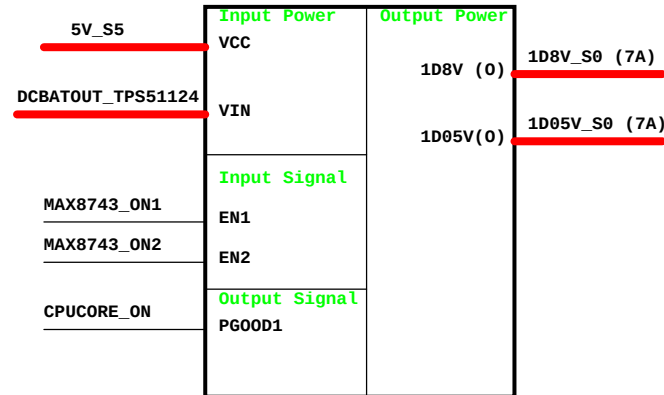
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
RUN and AUX POWER		
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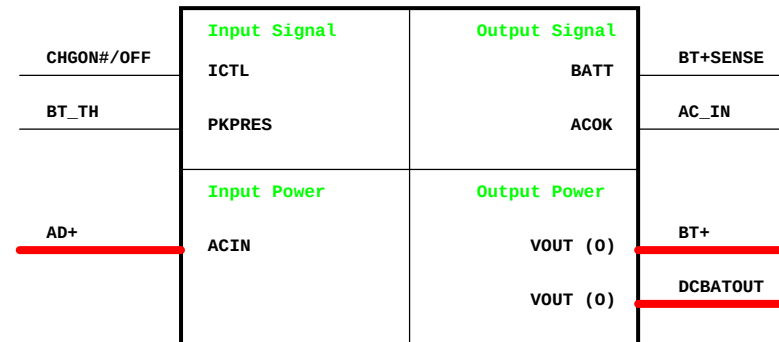
CPU_CORE
Intersil ISL6262



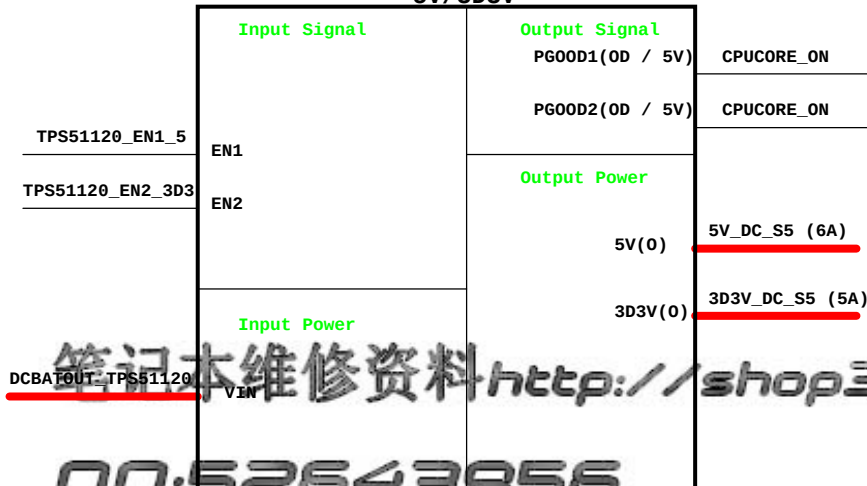
MAX8743
1D8V/1D05V



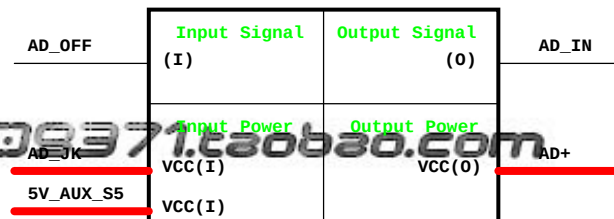
Charger Max8725

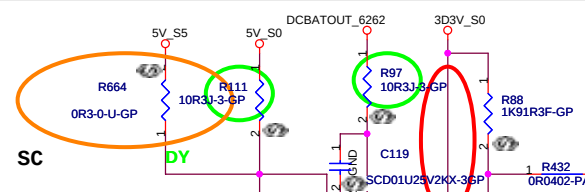


TPS51120
5V/3D3V



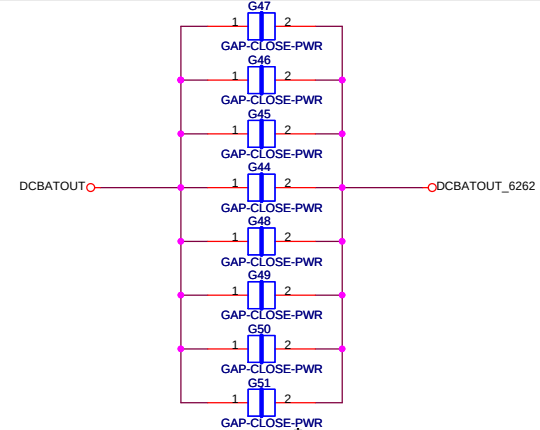
Adapter



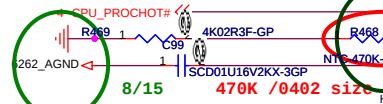


PGOOD
Power good open-drain output.
Will be pulled up externally by
a 680. resistor to VCCP or 1.9k. to 3.3V.

PWRGD for NB and SB

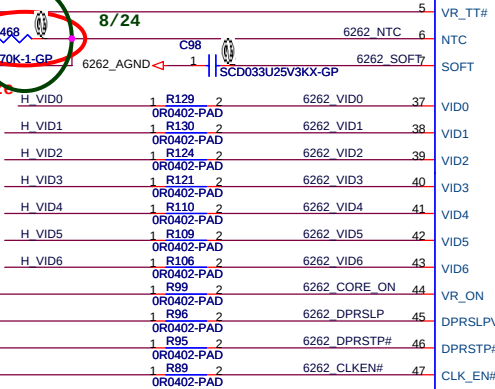


Place close to phase 1 choke

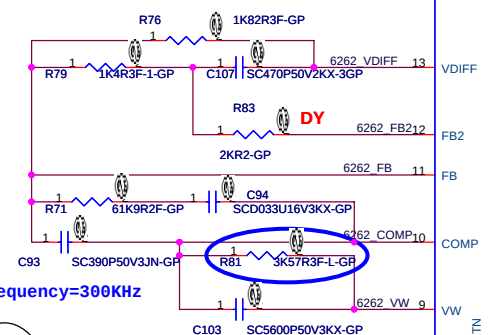


If NTC=330Kohm, R10=8.66K

- 40,41,43 CPUCORE_ON >>>
- 16 PM DPRSLPVR >>>
- 4,15 H DPRSLP# >>>
- 3 CLK_EN# <<<



Switching Frequency=300KHz

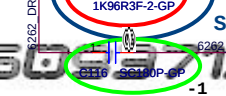


PL

PH

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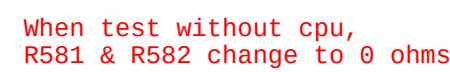


SB Not lead free

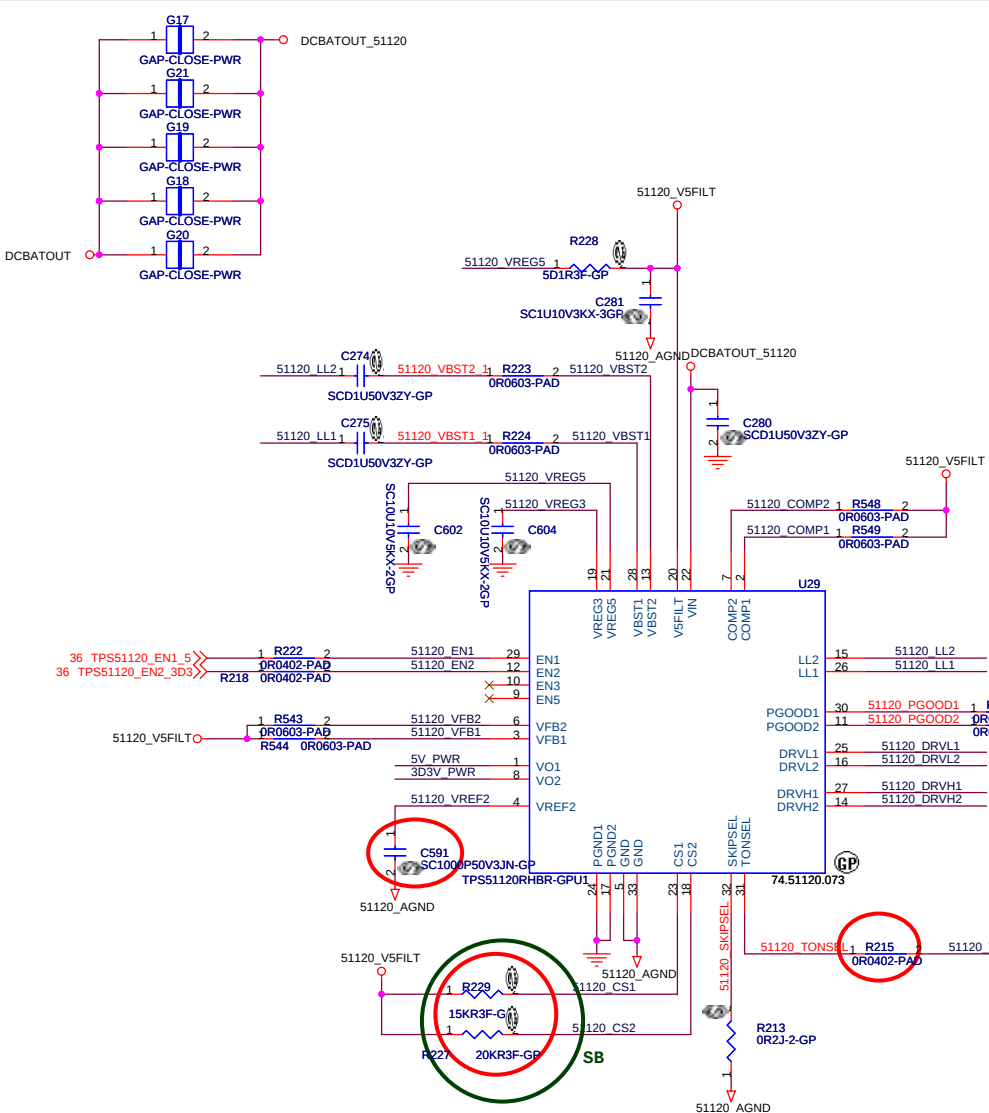
Place close to phase 1 choke

OCP>=88A

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Title CPU Vcore Power_1		
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	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 290k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 250k/CH2
VFB1	N/A	not use	ADJ.	Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	not use	not use	SWITCH ON	SWITCH ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on

Iomax=11A
Qg=9.8nC,
Rdson=20~25mohm

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

Iomax=11A
Qg=9.8nC,
Rdson=20~25mohm

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

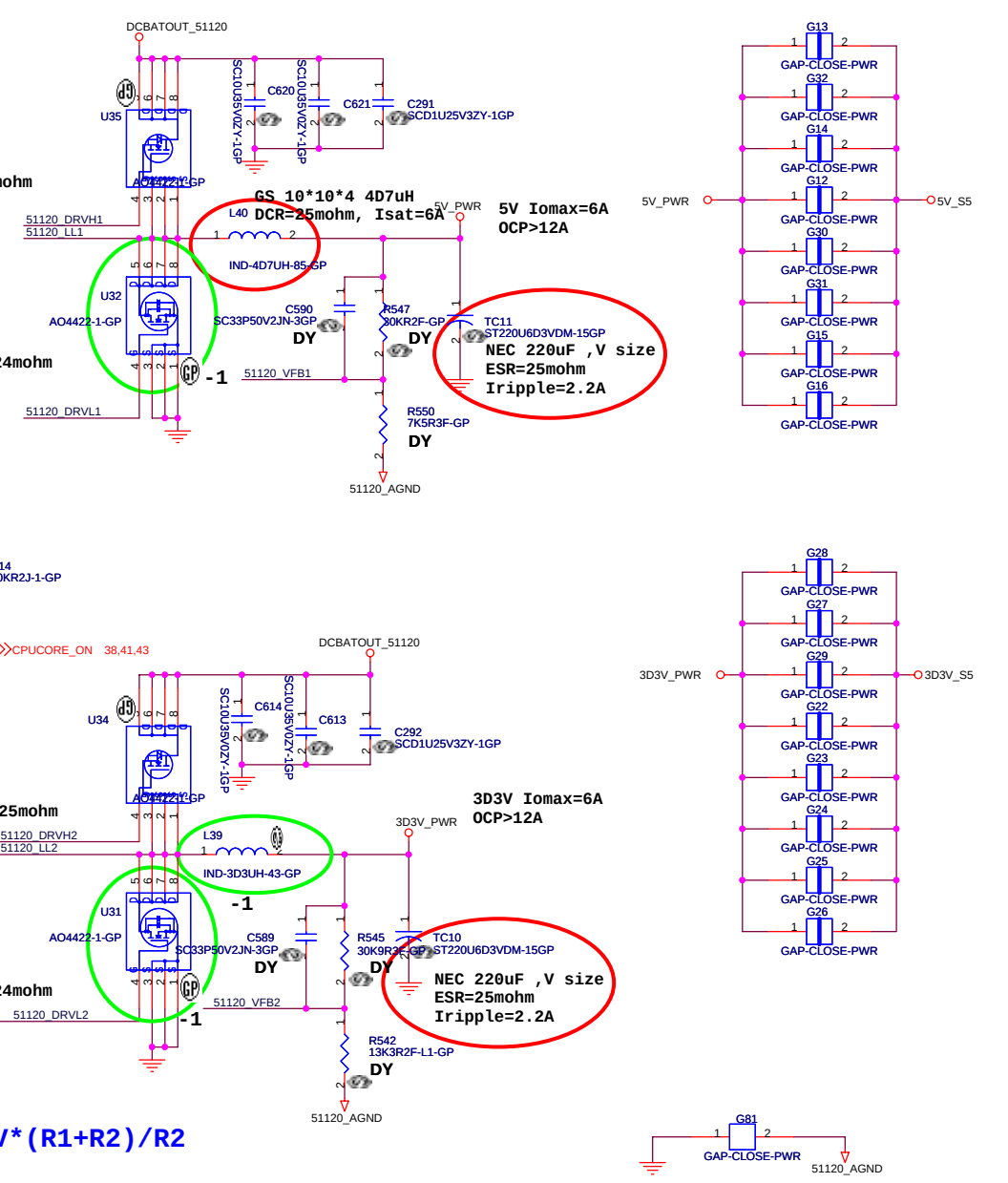
$$V_{out} = 1V * (R1 + R2) / R2$$

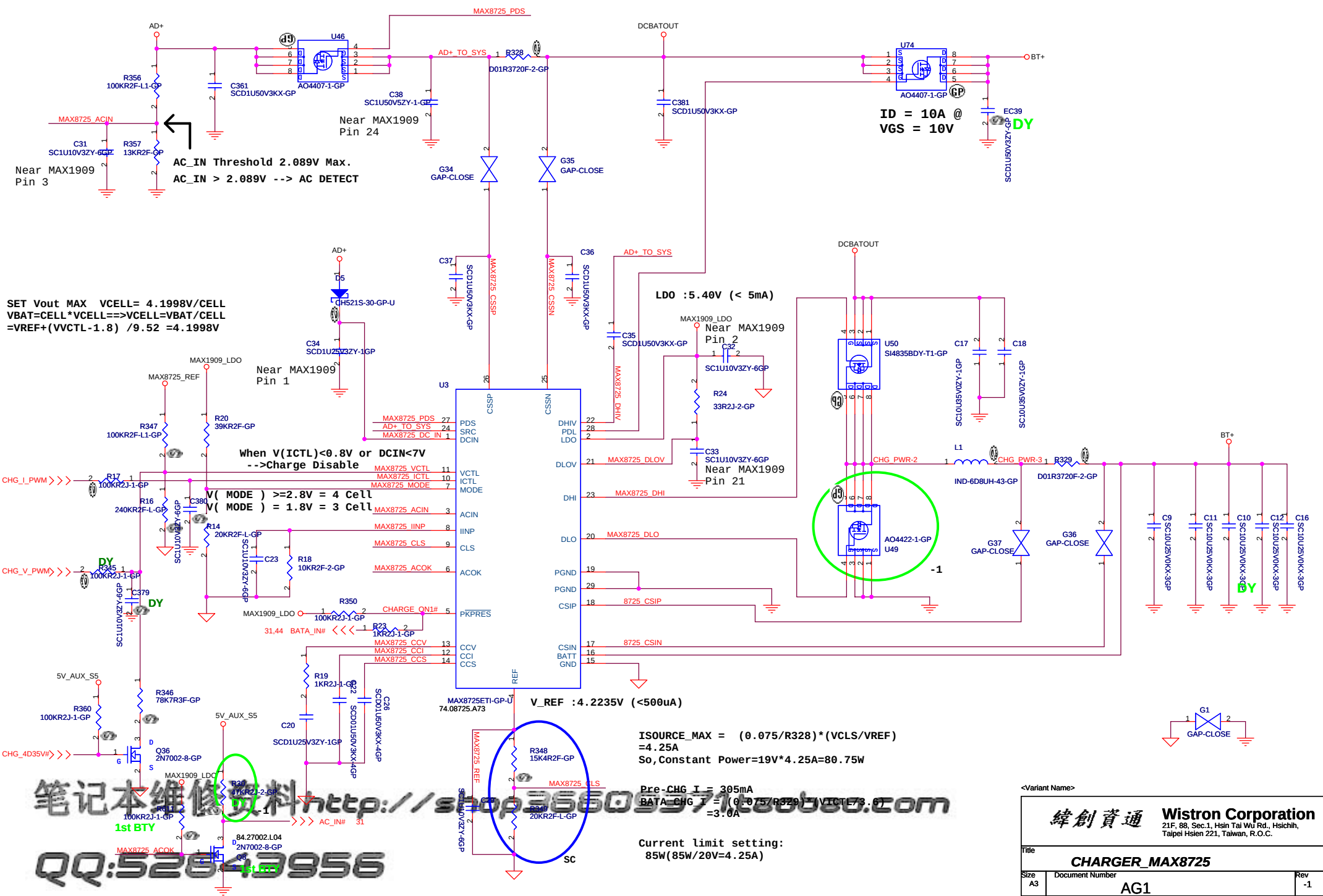
For TPS51120,
Vout=5V

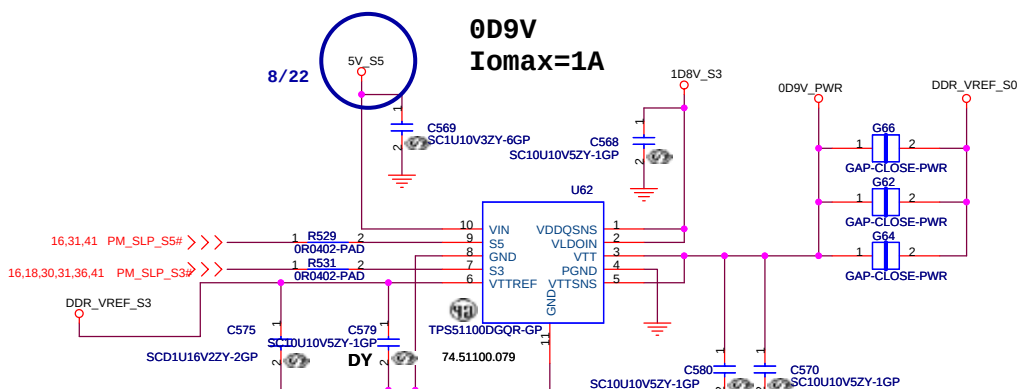
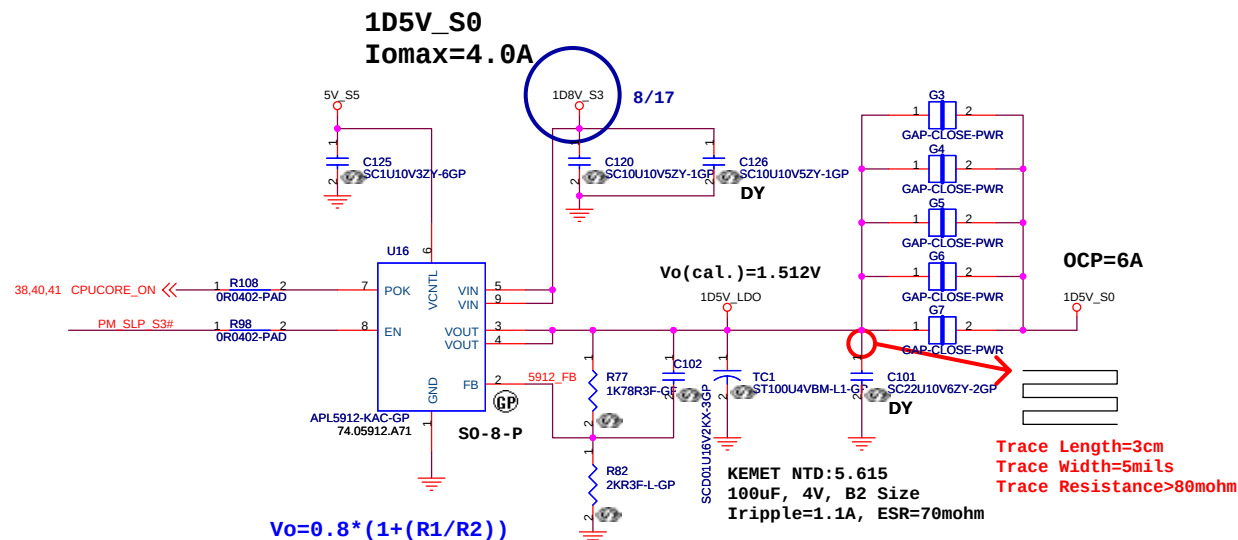
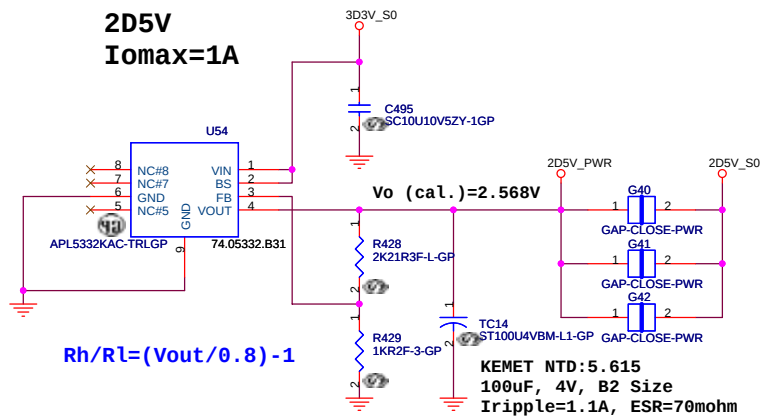
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 49m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V

1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.







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2nd source: 74.02997.079
G2997F6U

QQ:52643956

<Variant Name>

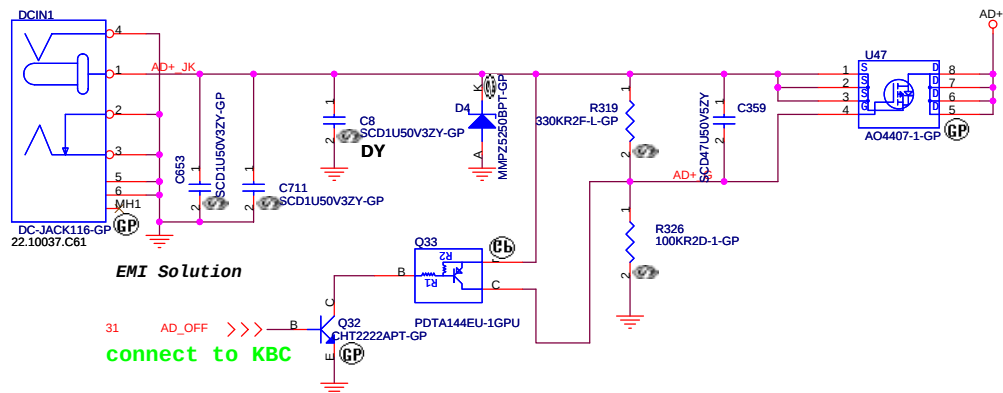
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Taipei Hsien 221, Taiwan, R.O.C.

Title
0D9V/1D5V/2D5V

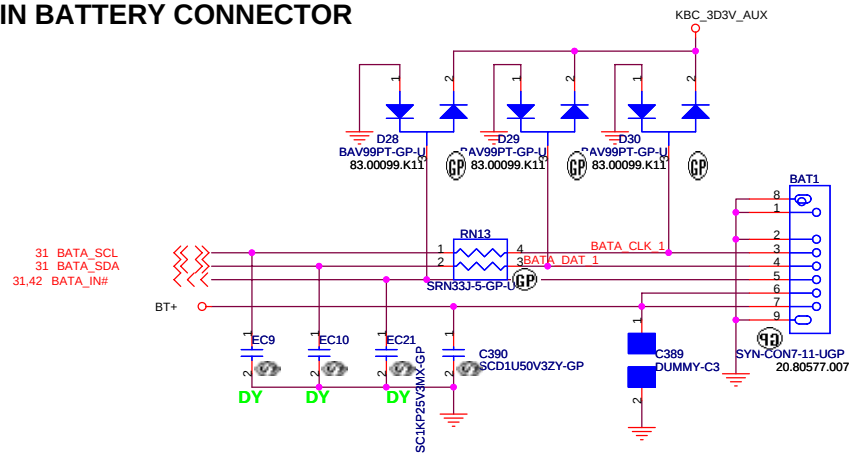
Size A3 Document Number
AG1

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ADAPTER IN CIRCUIT



MAIN BATTERY CONNECTOR



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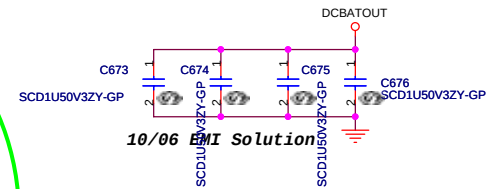
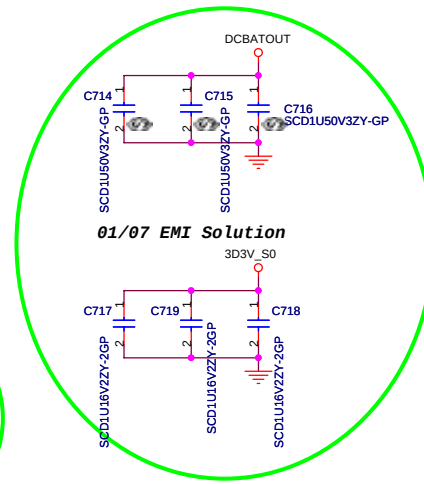
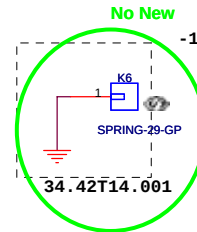
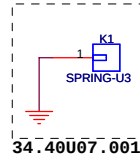
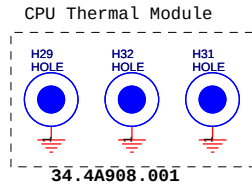
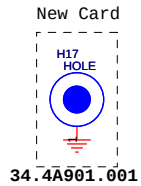
QQ:52643956

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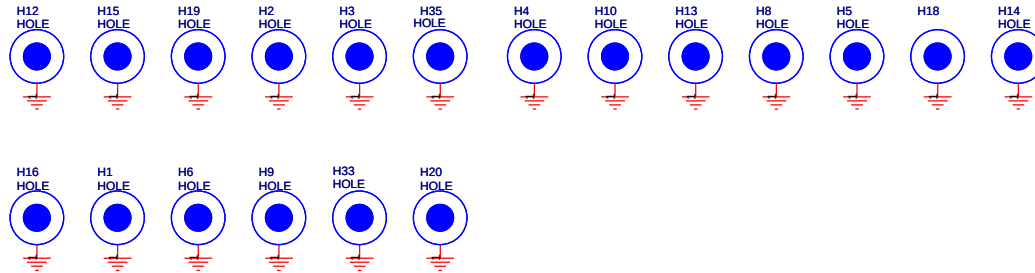
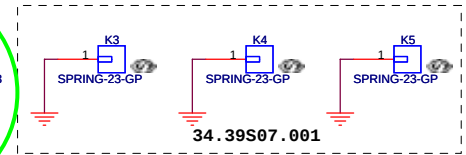
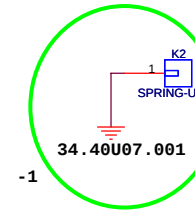
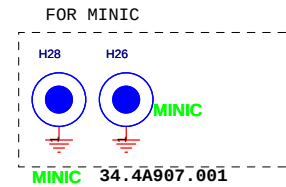
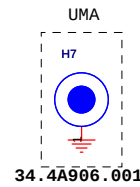
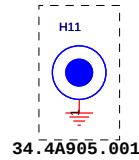
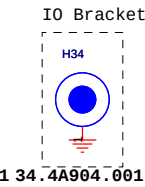
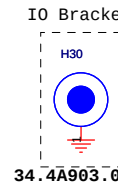
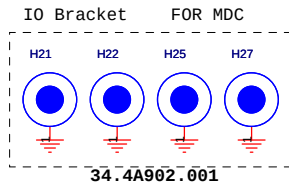
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Taipei Hsien 221, Taiwan, R.O.C.

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TOP SIDE:



BOTTOM SIDE:



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QQ:52643956

<Variant Name>			
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Title SPRING & BOSS			
Size A3	Document Number AG1		Rev -1
Date: Tuesday, January 24, 2006		Sheet 45 of 45	