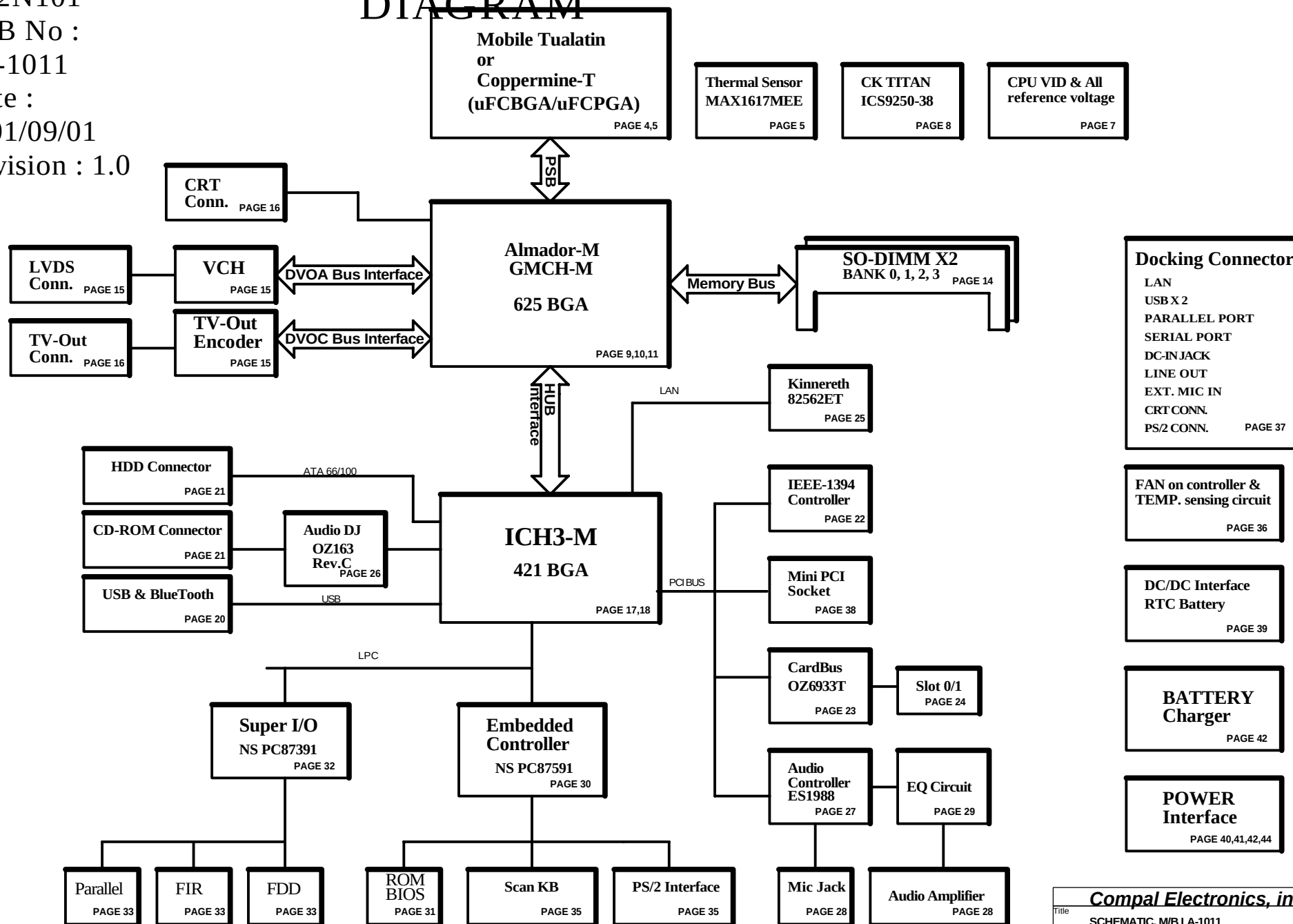


Model Name :
N32N101
PCB No :
LA-1011
Date :
2001/09/01
Revision : 1.0

BLOCK DIAGRAM

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_H_CORE	Core voltage for CPU	ON	OFF	OFF
+VTT	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.5V_ALW	1.5V always on power rail	ON	ON	ON*
+1.5V_SW	AGP 4X	ON	OFF	OFF
+1.8V_ALW	1.8V always on power rail	ON	ON	ON*
+1.8V_SW	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5V_MRIMM	2.5V switched power rail	ON	OFF	OFF
+3V_ALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3V_SW	3.3V switched power rail	ON	OFF	OFF
+5V_ALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5V_SW	5V switched power rail	ON	OFF	OFF
+12V_ALW	12V always on power rail	ON	ON	ON*
+12V_SW	12V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
LAN	(AD24 internal)		
CardBus	AD20	2	PIRQA/PIRQB
Audio Controller	AD19	3	PIRQD
Mini-PCI	AD18	1	PIRQC
Mini-PCI(LAN)	AD22	4	PIRQD
IEEE-1394 Controller	AD16	0	PIRQA

EC SM Bus1 address

Device		Device	
Smart Battery	0001 011X b	MAX1617MEE	1001 110X b
EEPROM	1010 000X b	OZ163	0011 0100 b
		Docking	0011 011X b
		DOT Board	XXXX XXXXb

EC SM Bus2 address

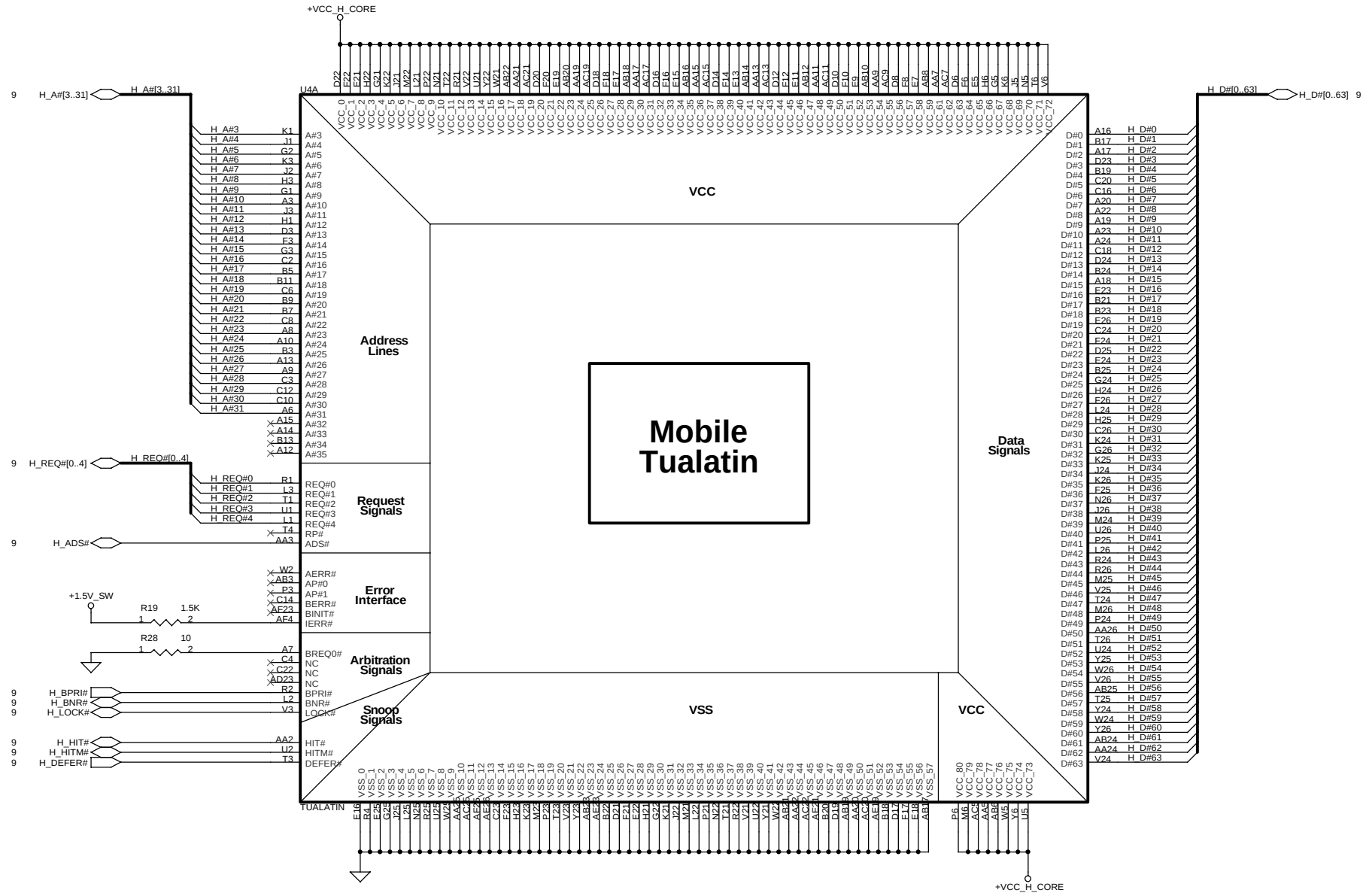
ICH3 SM Bus address

Device	
SODIMM	1010 000X b
Clock Gen.	1101 001X b

*P.S:Default Resistor & Capacitor's package are 0402.
Default 8P4R package is 0402.*

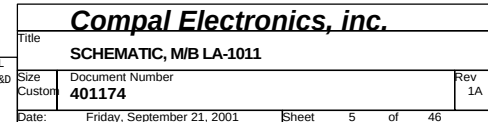
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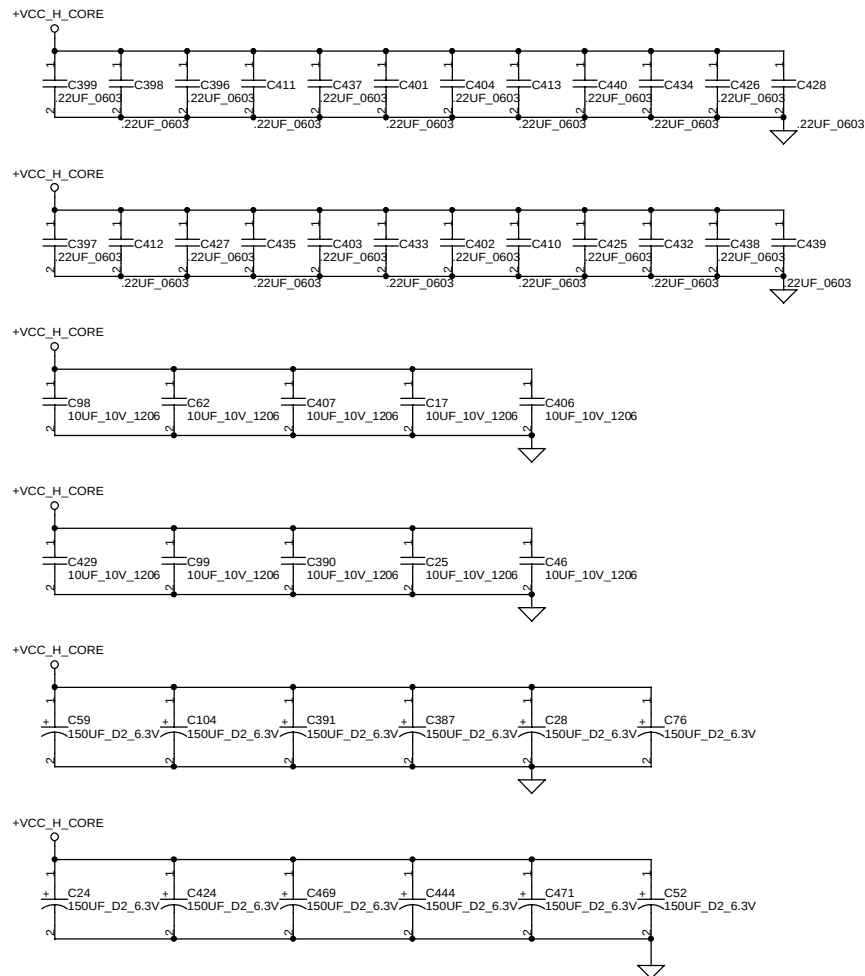


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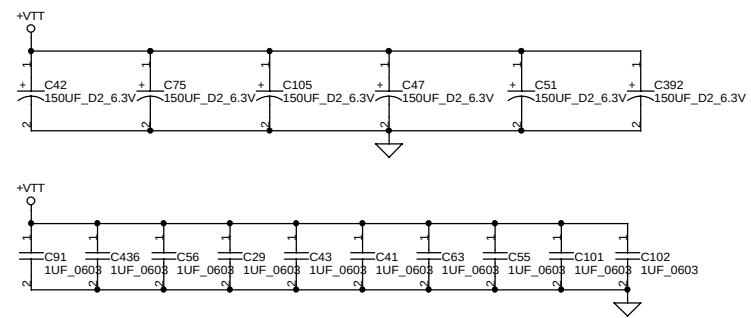
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Layout note :
Place close to CPU, Use 2-3 vias per PAD.
Place .47uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2-3 vias per PAD.



Layout note :
Place close to CPU,
Use 2 vias per PAD.



Tualatin

D4	D3	D2	D1	D0	CPU_Core(V)	QS(MP)
0	1	0	0	1	1.40V	
0	1	1	0	0	1.15V	

Coppermine-T

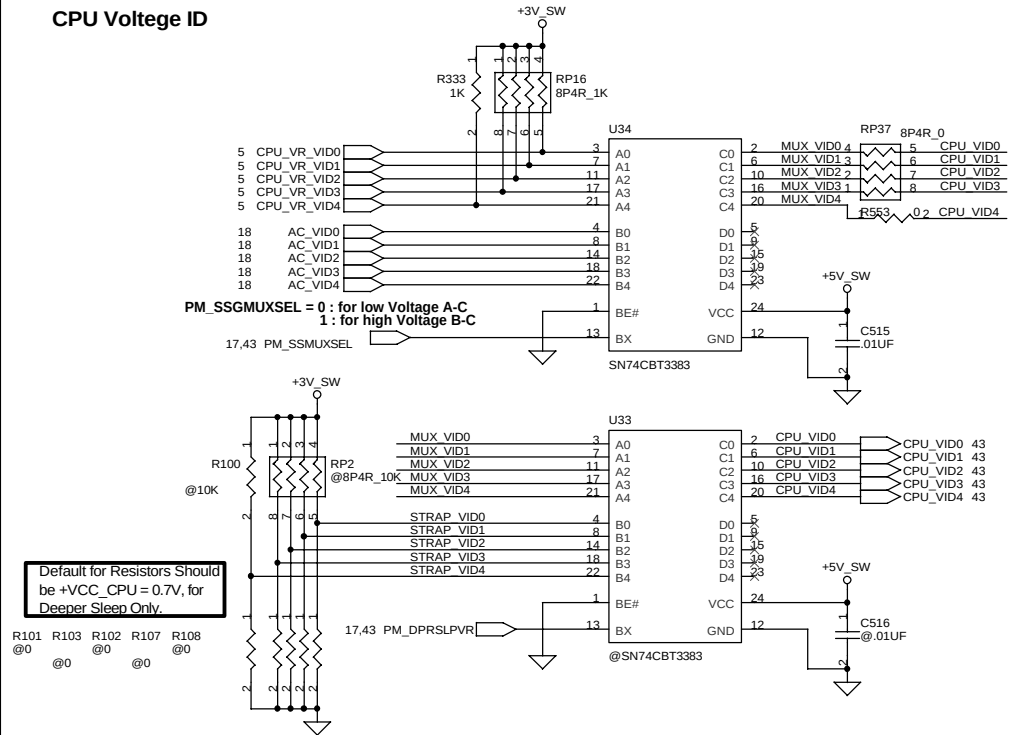
D4	D3	D2	D1	D0	CPU_Core(V)	ES(before MP)
0	0	0	0	1	1.70V	
0	1	0	0	0	1.35V	

D4	D3	D2	D1	D0	CPU_Core(V)	QS(MP)
0	0	0	0	1	1.70V	
0	1	0	0	0	1.35V	

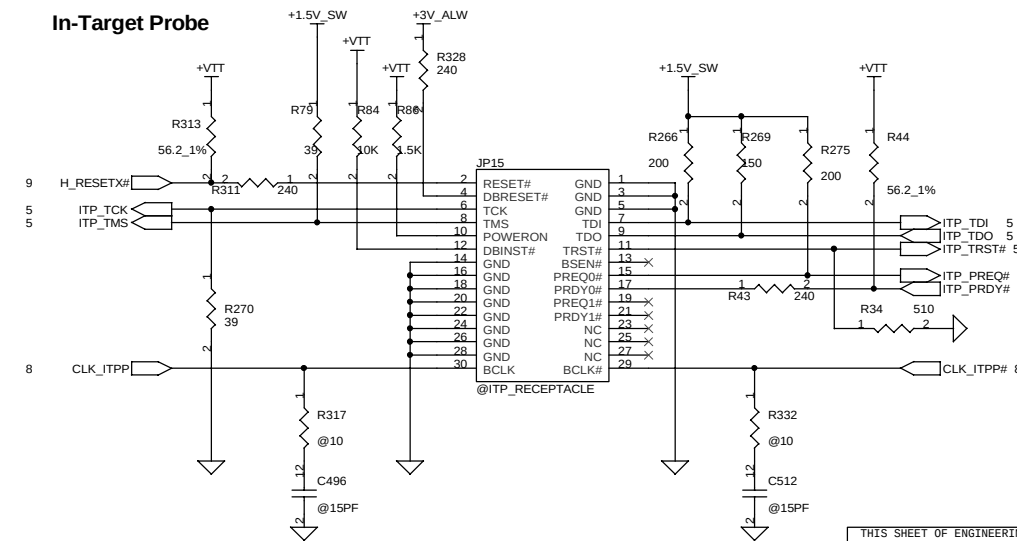
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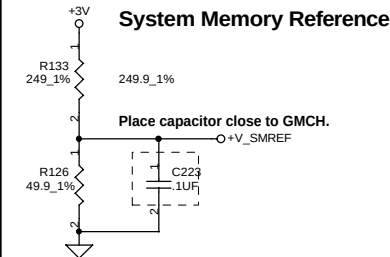
CPU Voltage ID



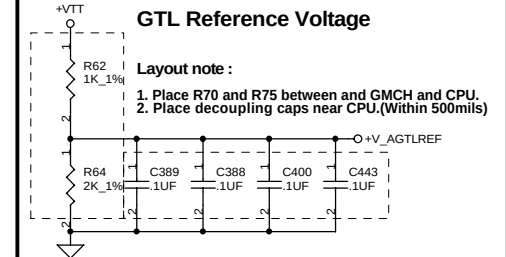
In-Target Probe



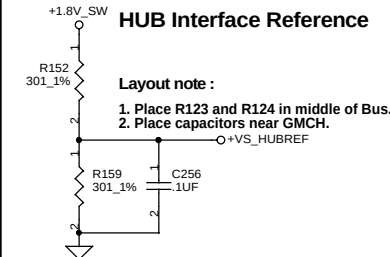
System Memory Reference



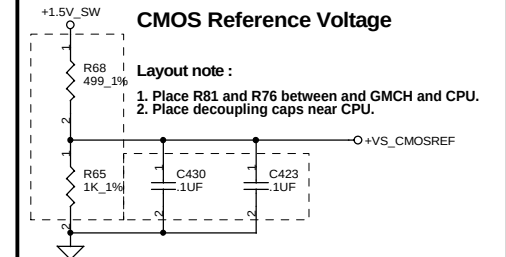
GTL Reference Voltage



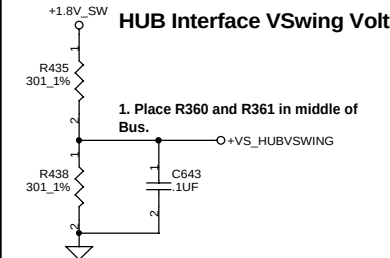
HUB Interface Reference



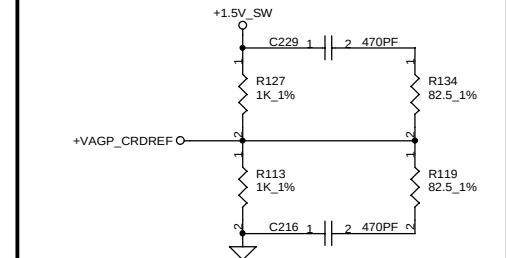
CMOS Reference Voltage



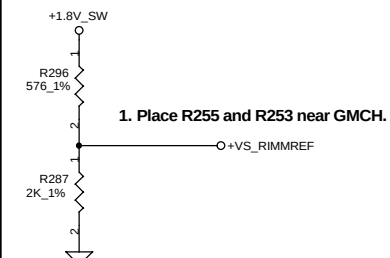
HUB Interface VSwing Voltage



Place Reference Circuit near GMCH



1. Place R255 and R253 near GMCH.

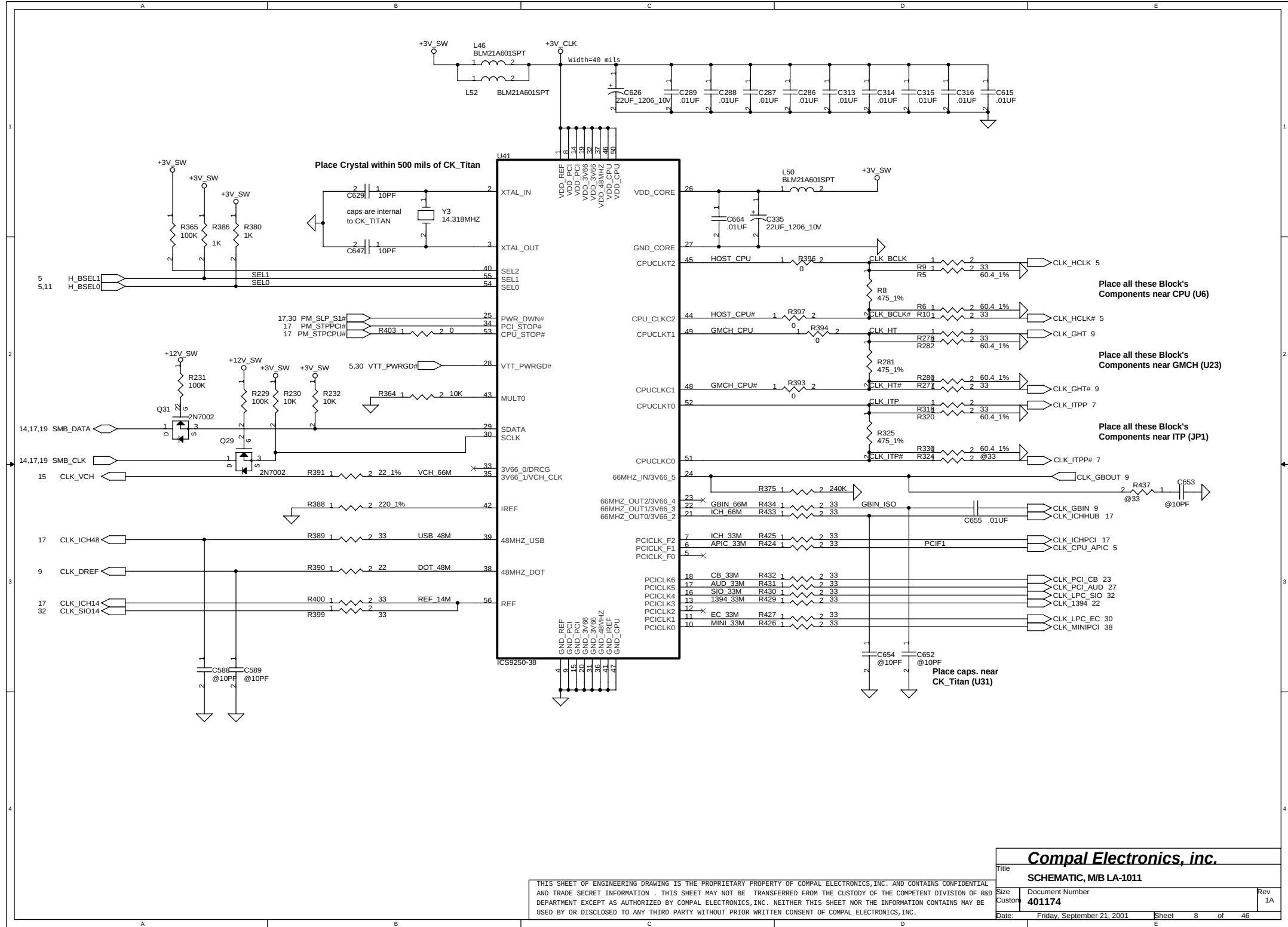


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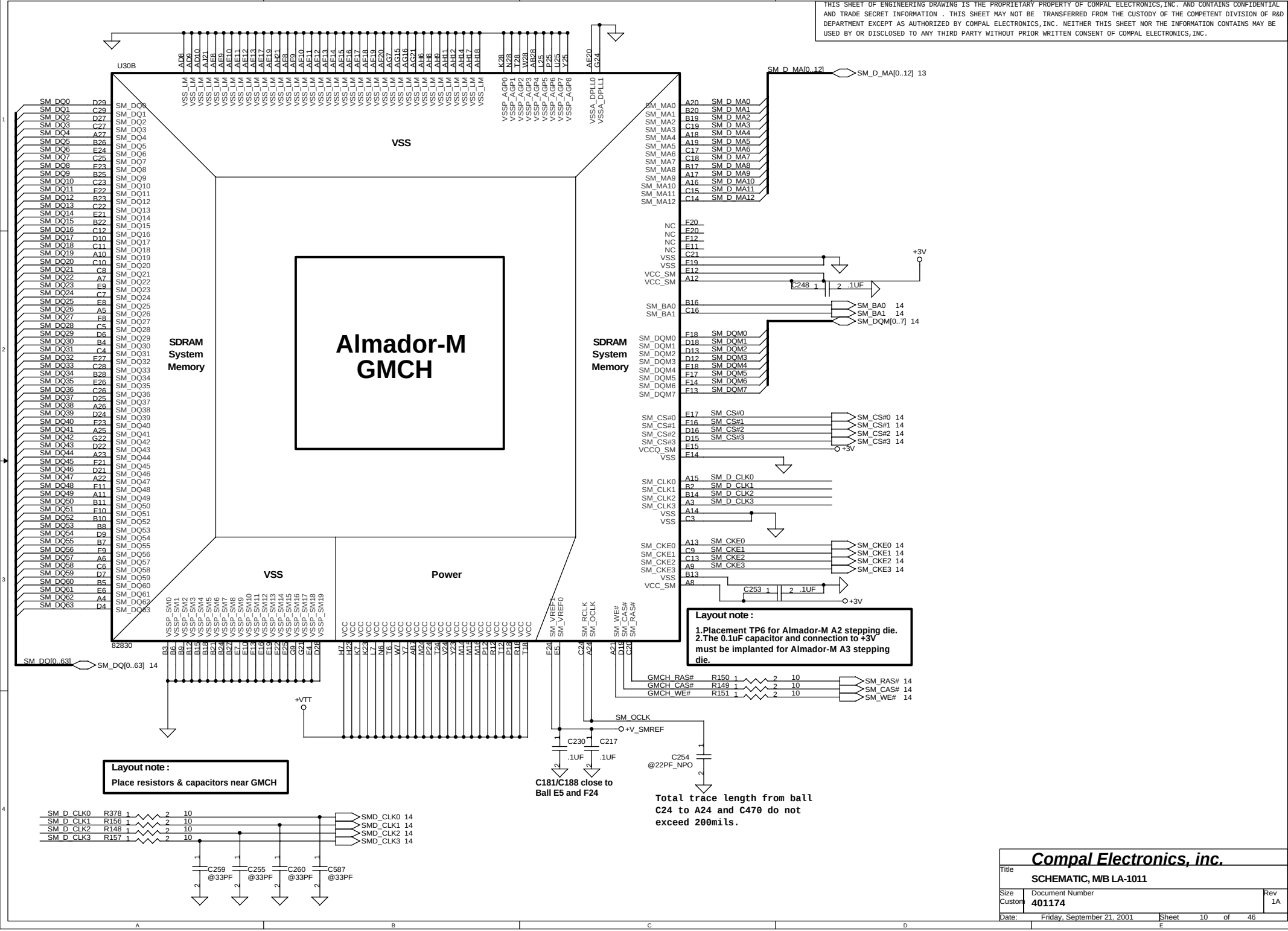
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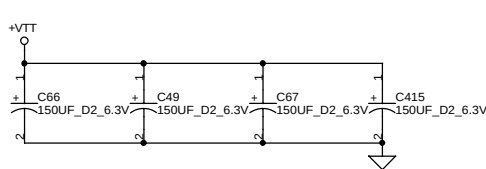
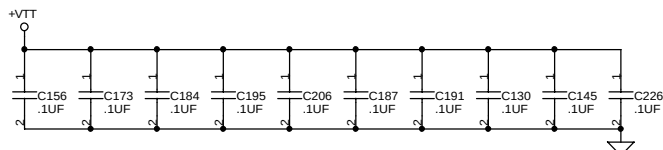
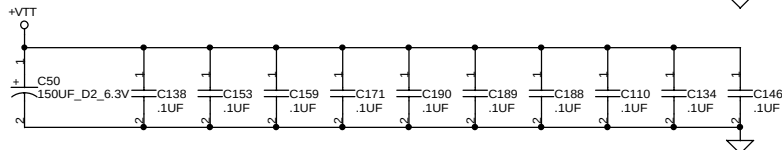
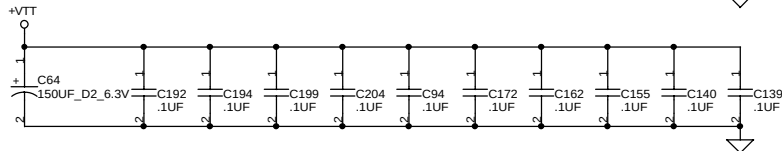
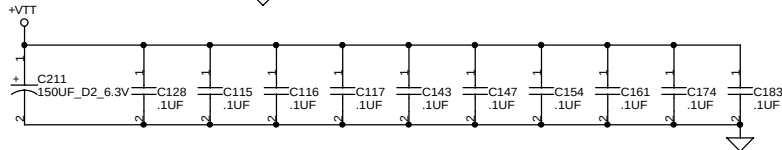
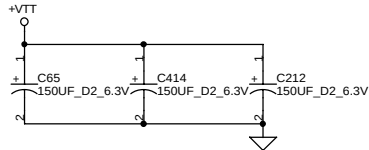
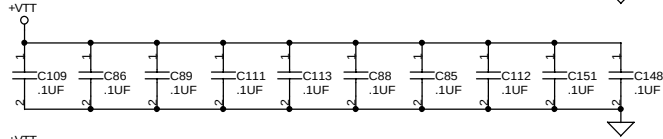
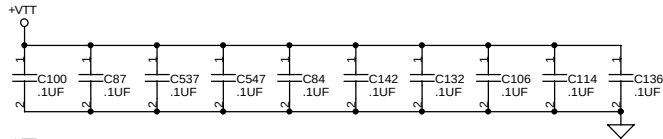


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Title			
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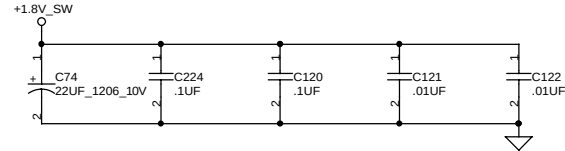
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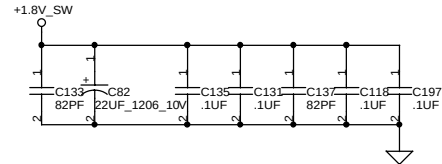
Layout note :
Distribute as close as possible
to GMCH Processor Quadrant .



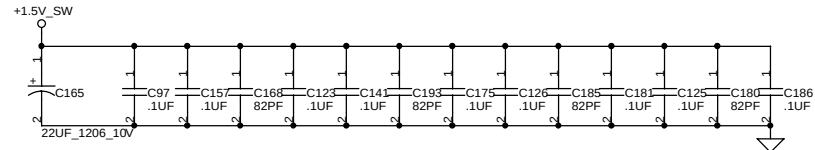
Layout note :
Distribute as close as possible
to VCCPCMOS_LM .



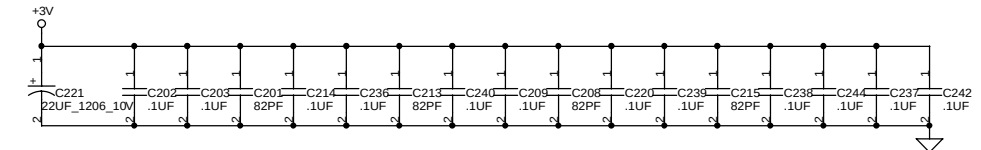
Layout note :
Distribute as close as possible
to GMCH Local Memory Quadrant .



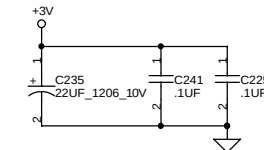
Layout note :
Distribute as close as possible
to GMCH AGP/DVO Quadrant .



Layout note :
Distribute as close as possible
to GMCH System Memory Quadrant .



Layout note :
Distribute as close as possible
to IO Quadrant .



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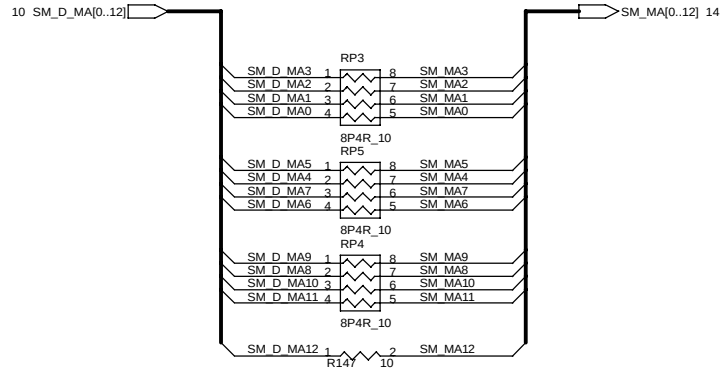
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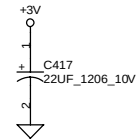
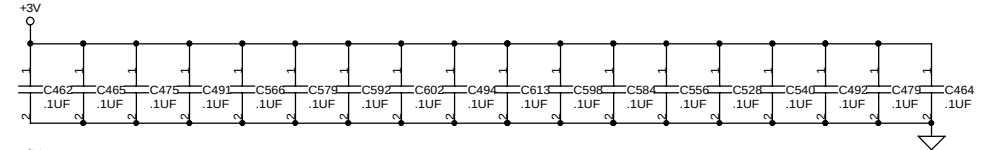
Size
Custom
Document Number
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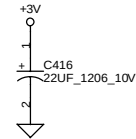
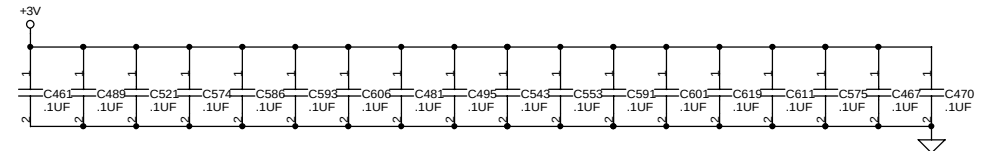
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Layout note :
One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 0) pin .



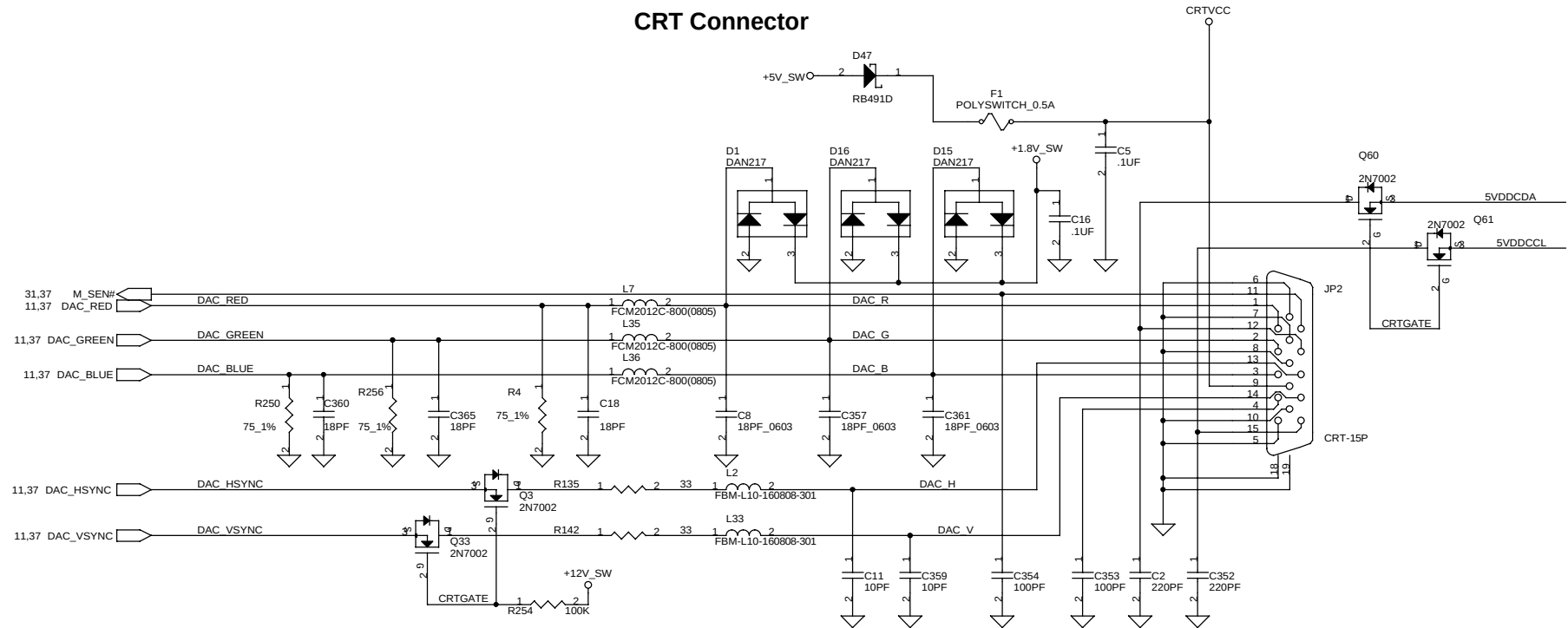
Layout note :
One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 1) pin .



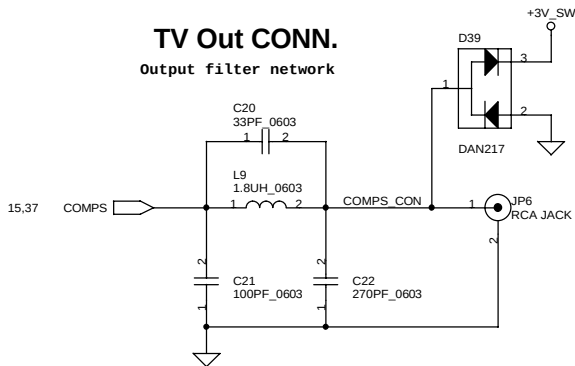
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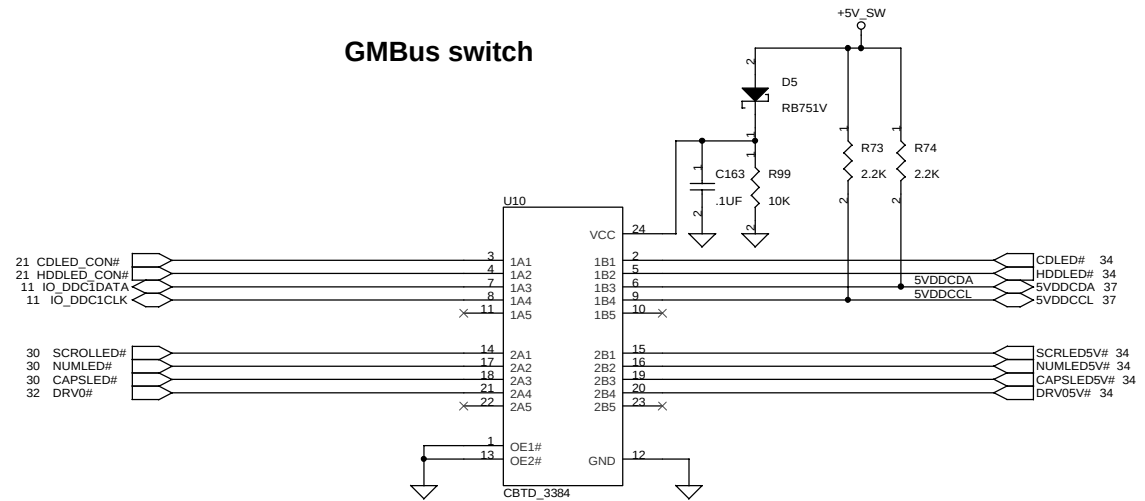
CRT Connector



TV Out CONN. Output filter network



GMBus switch

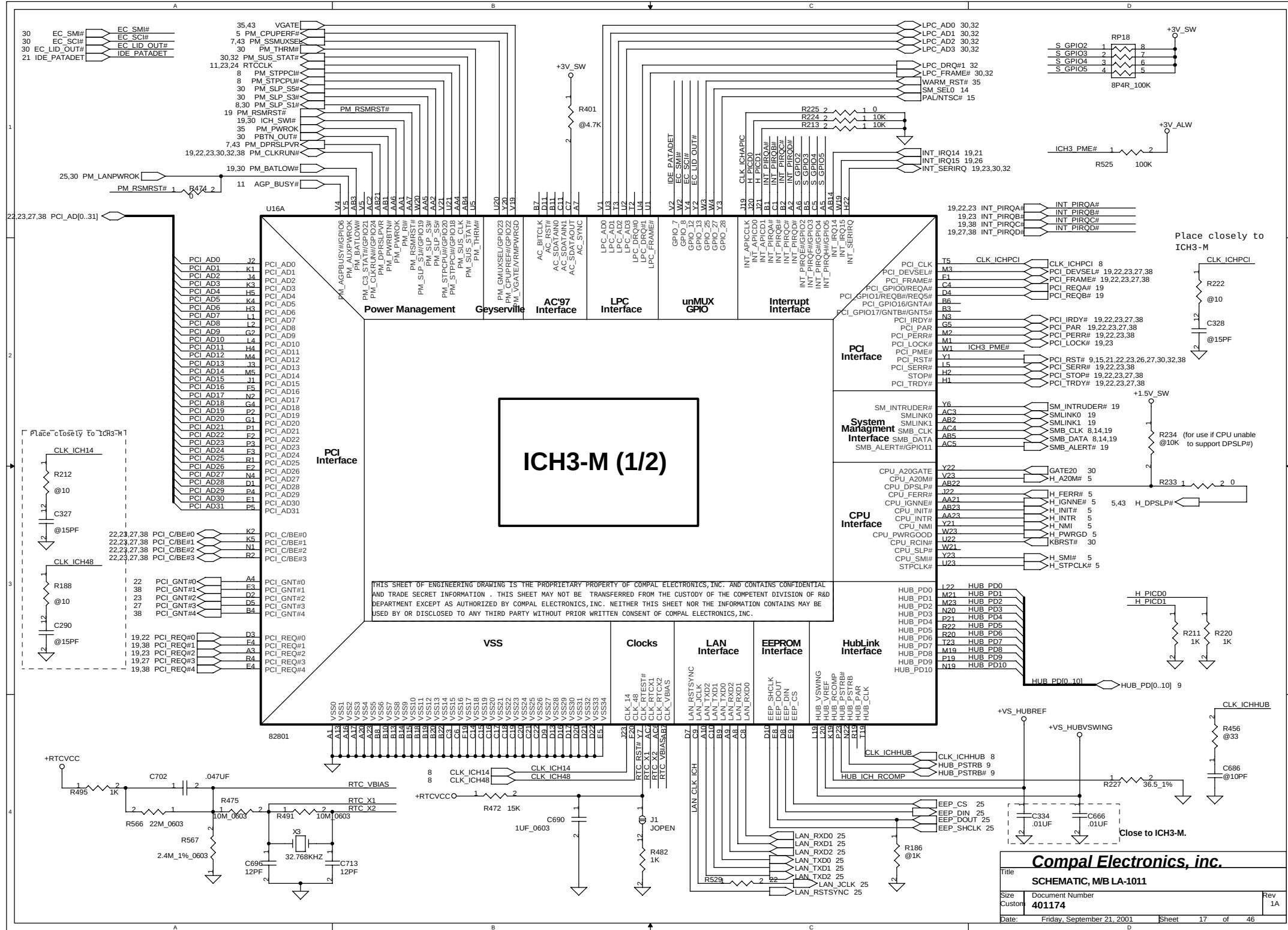


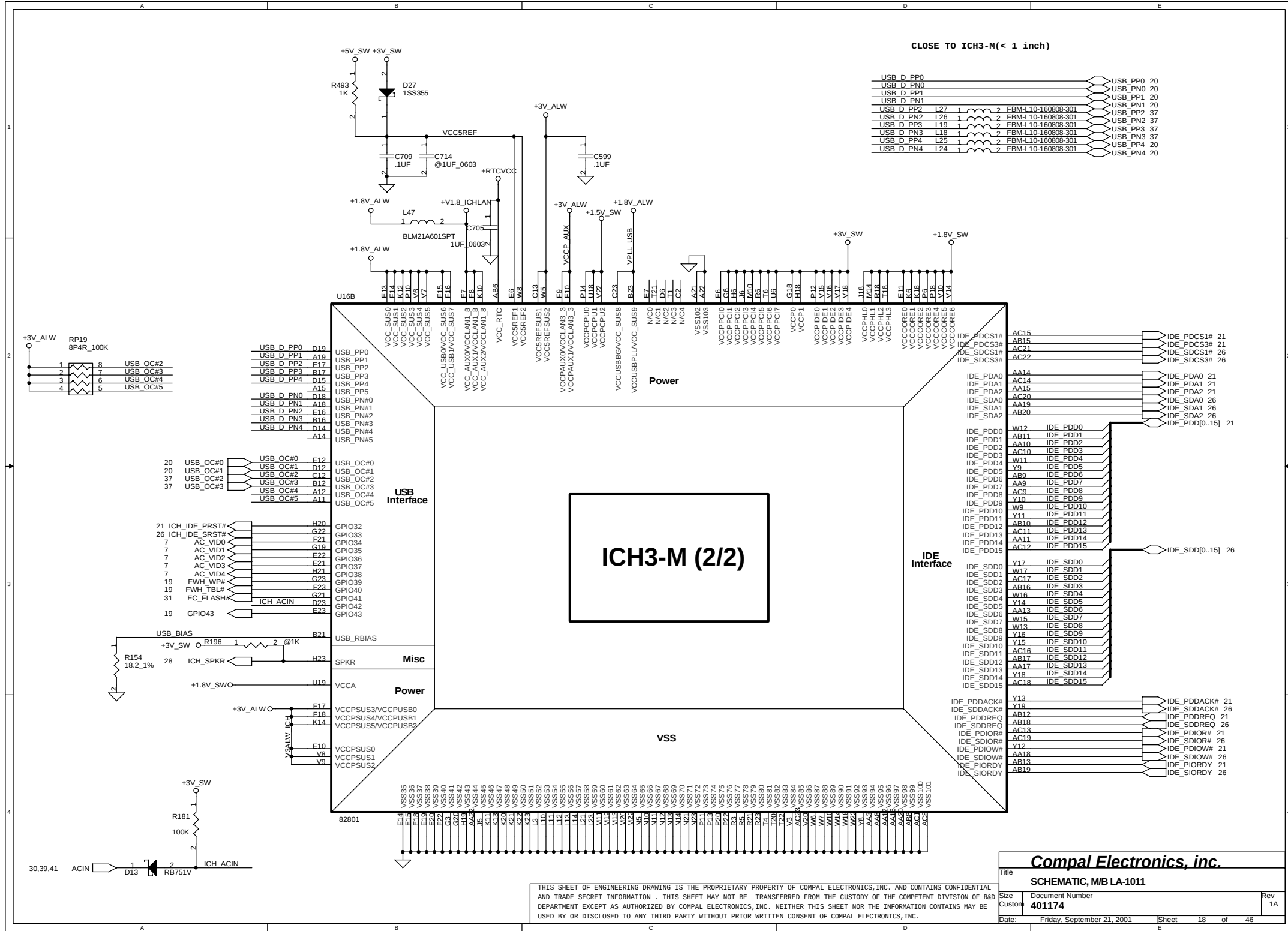
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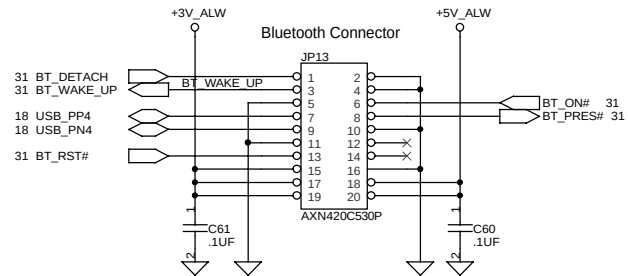
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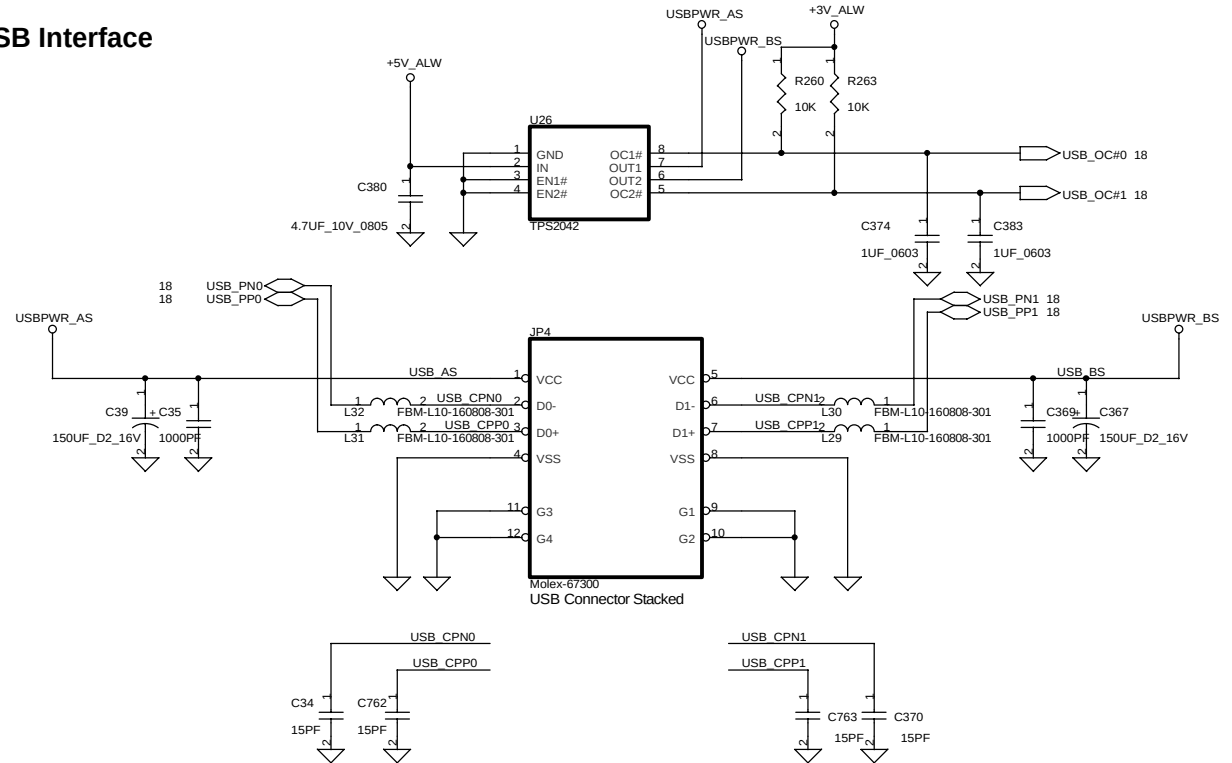




BlueTooth Interface



USB Interface

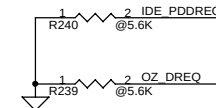
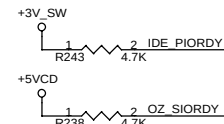
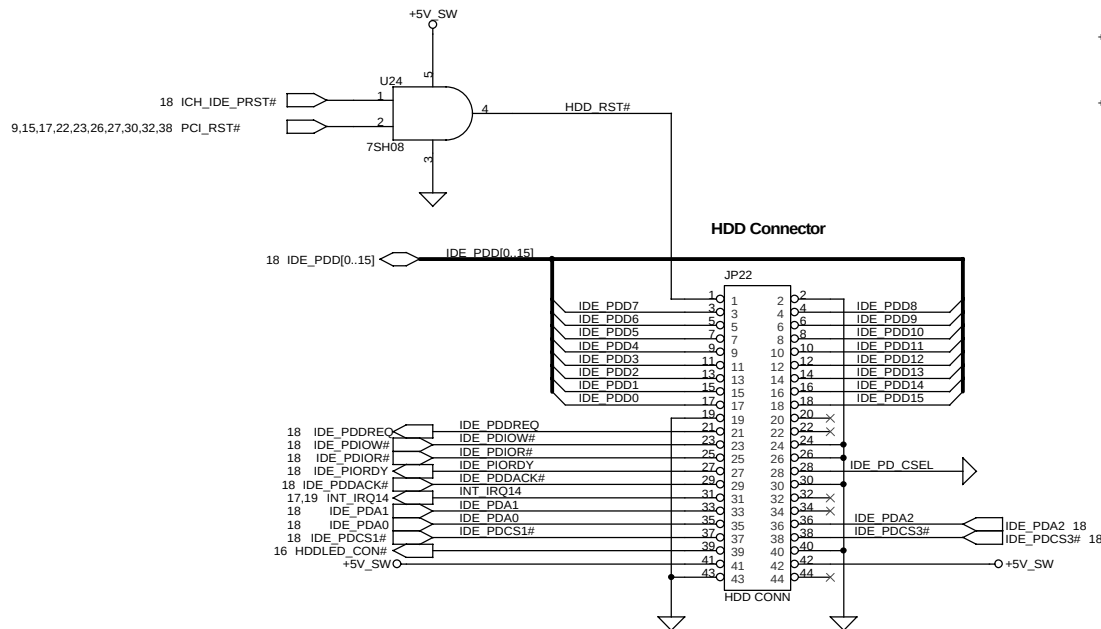


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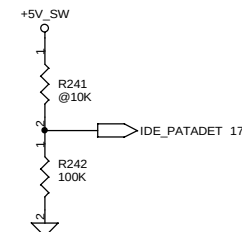
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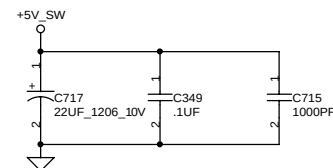
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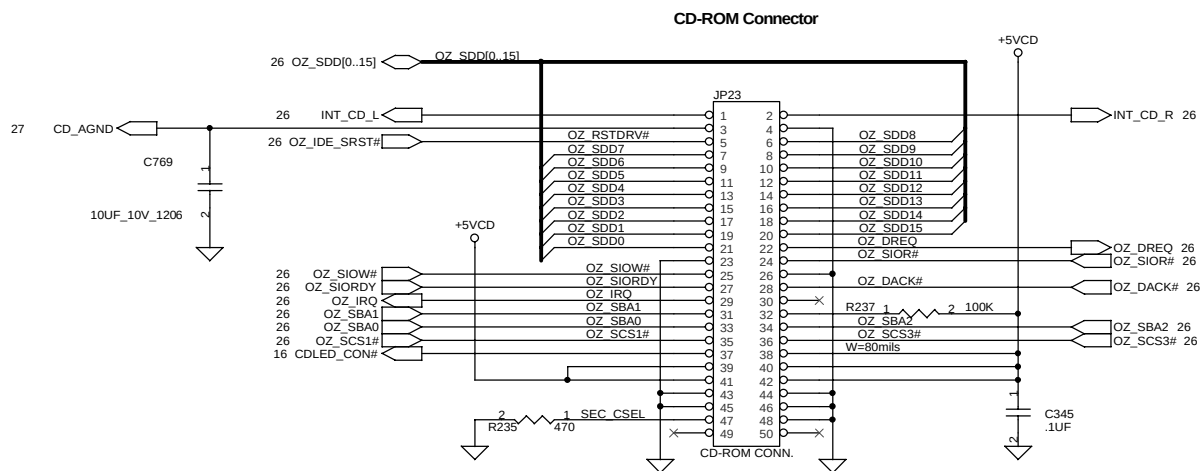
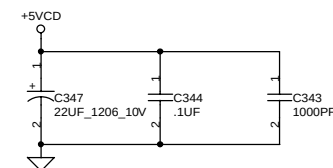
HDD Manual ATA Type Selection:
ATA33 : populate R224, de-populate R225.
ATA66/100 : populate R225, de-populate R224.



Layout note :
Place capacitors near HDD connector .

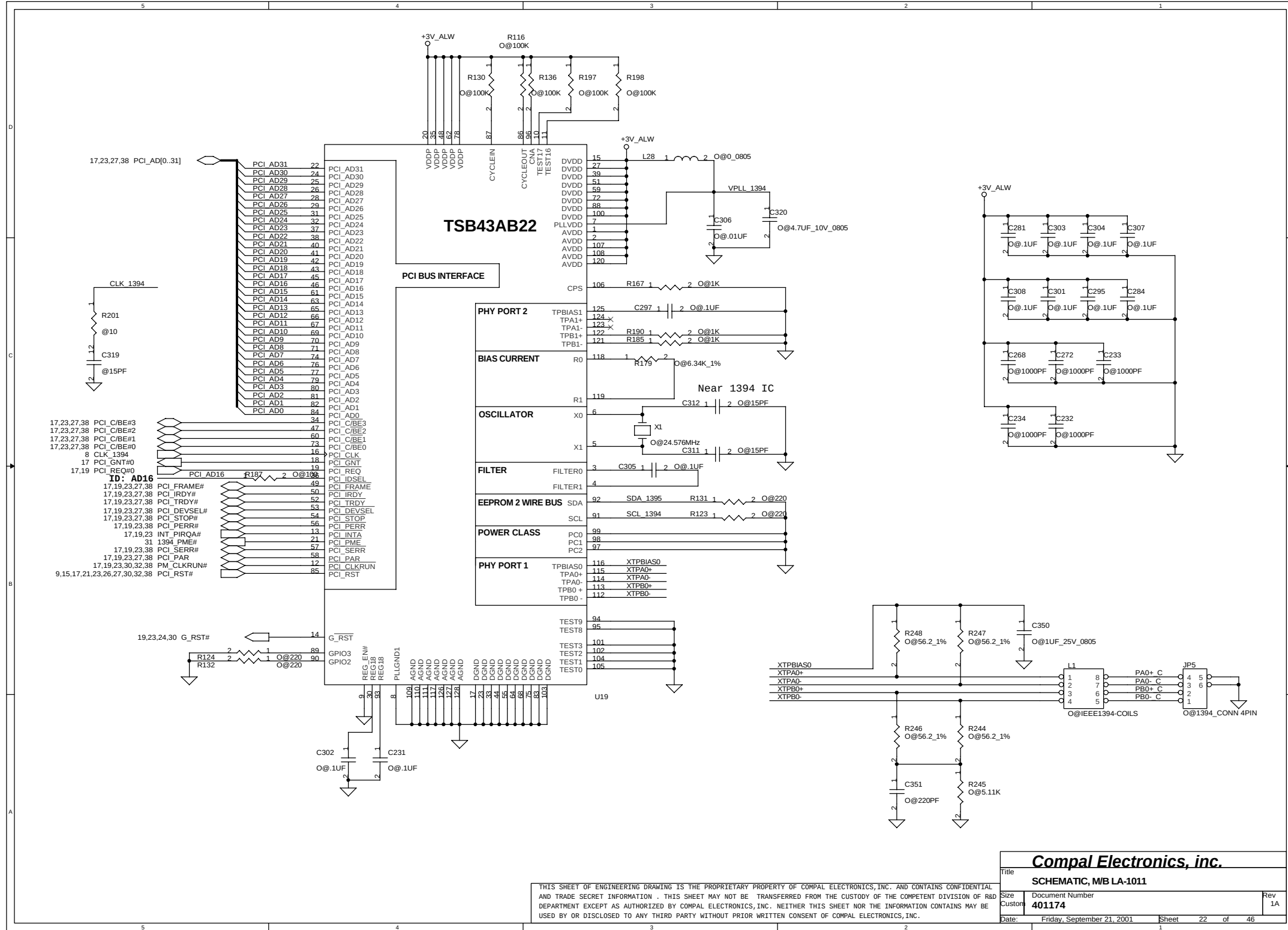


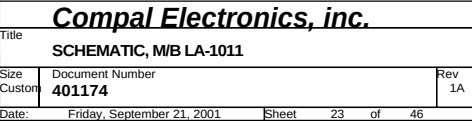
Layout note :
Place capacitors near CD-ROM connector .



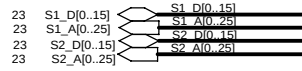
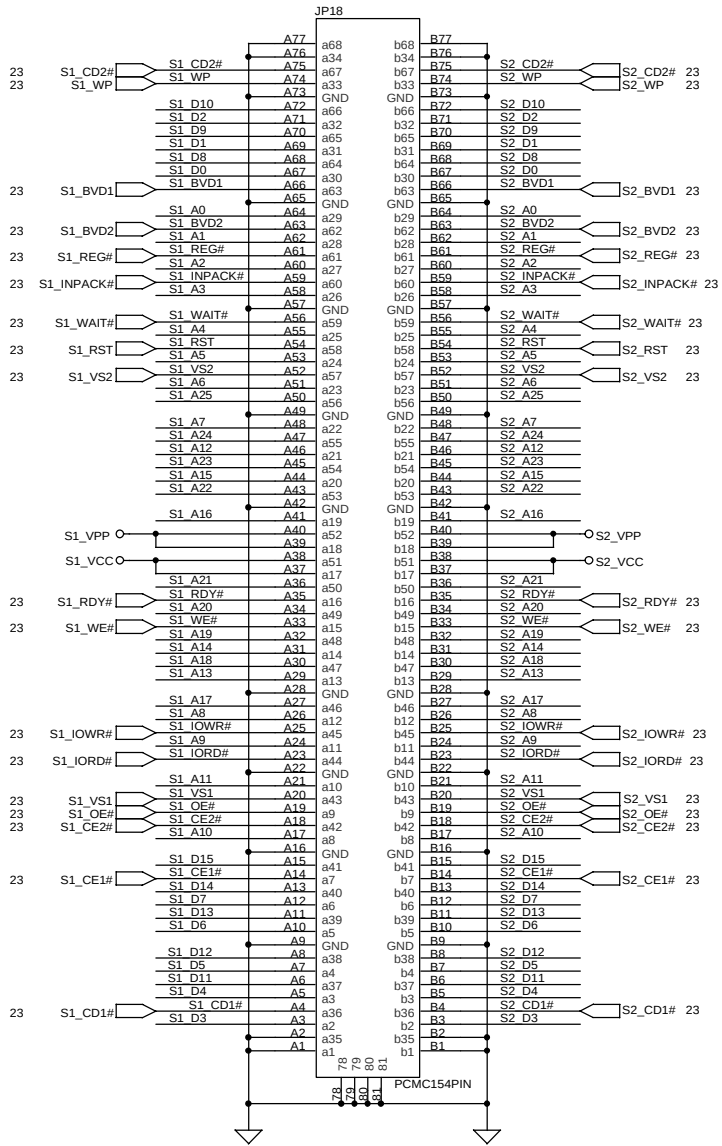
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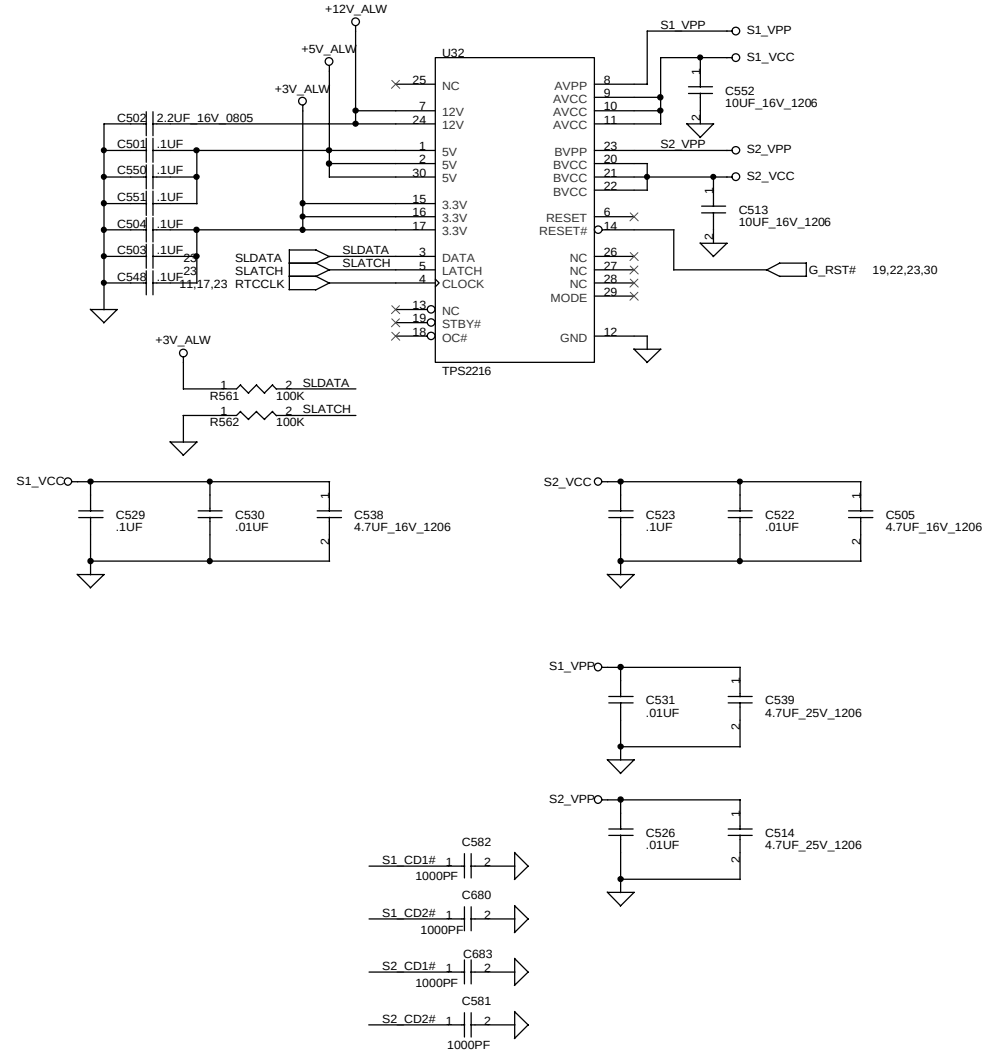




CARDBUS SOCKET



PCMCIA POWER CTRL.



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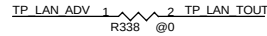
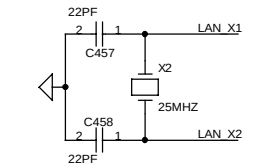
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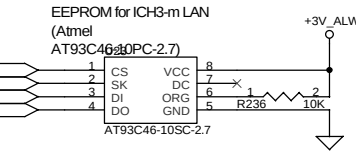
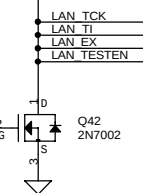
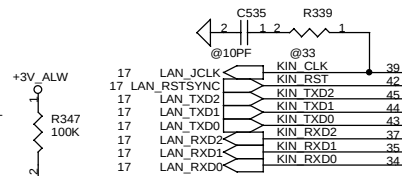
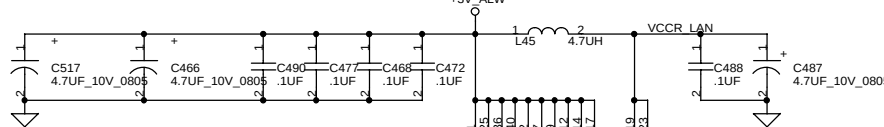
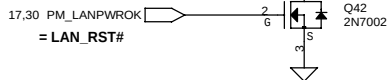
Size	Document Number
Custom	401174

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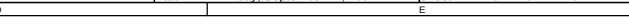
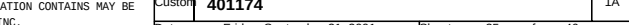
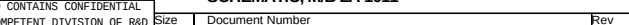
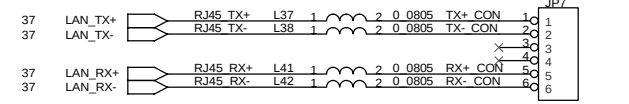
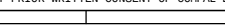
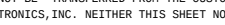
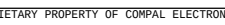
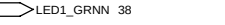
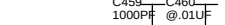
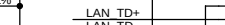
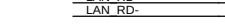
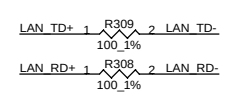
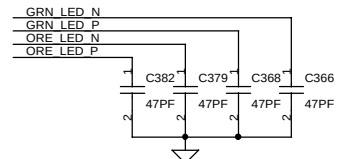
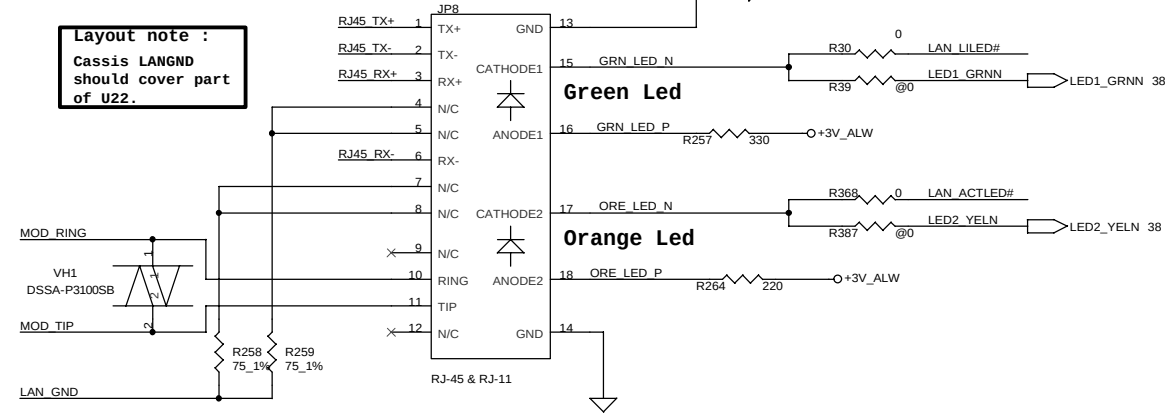
ev	
1A	

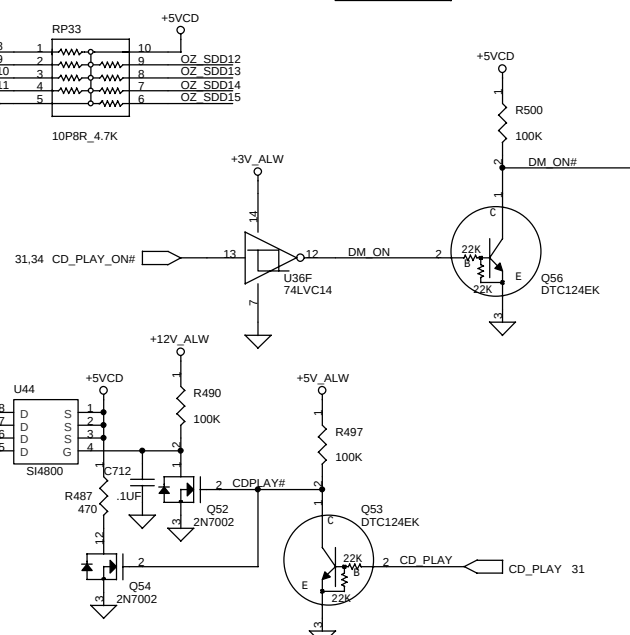
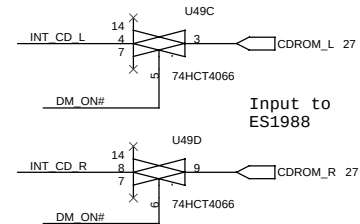
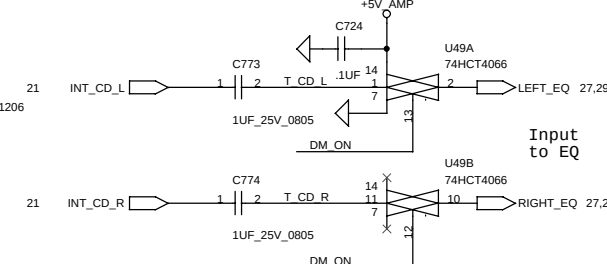
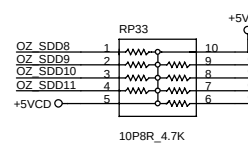
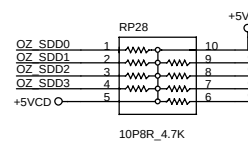
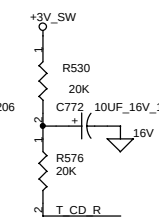
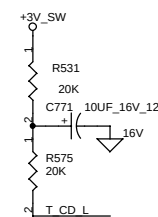
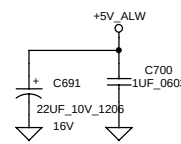
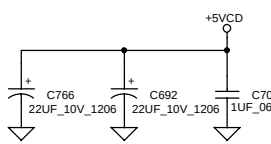
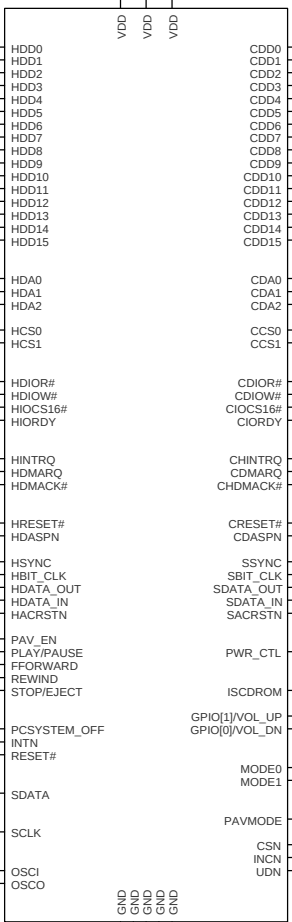
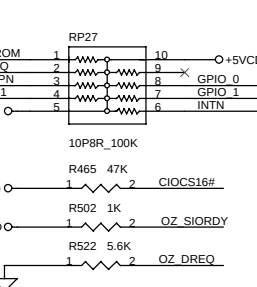
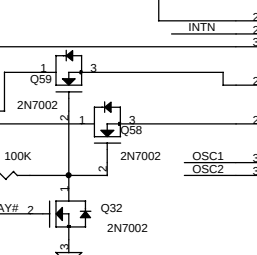
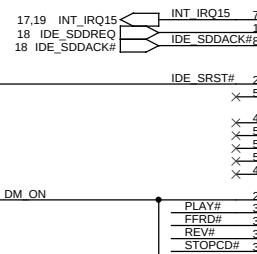
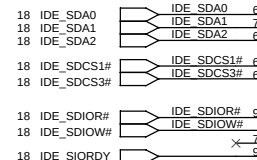
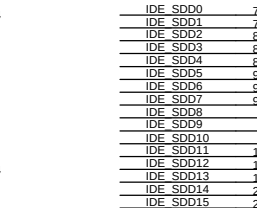
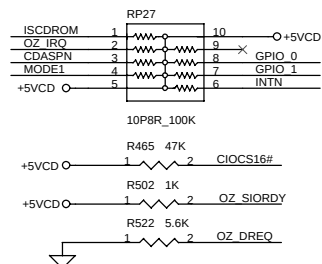
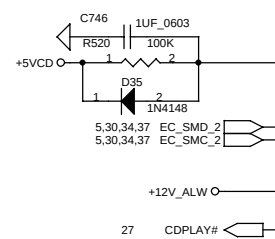
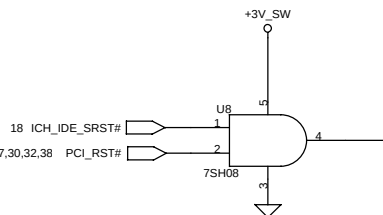
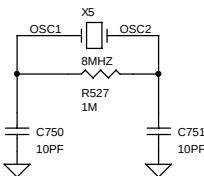
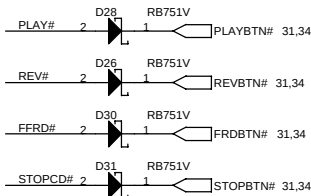
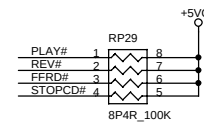


If LAN is enable,
PM_LANPWROK
waits for PM_PWROK
to go high and stays high in S3



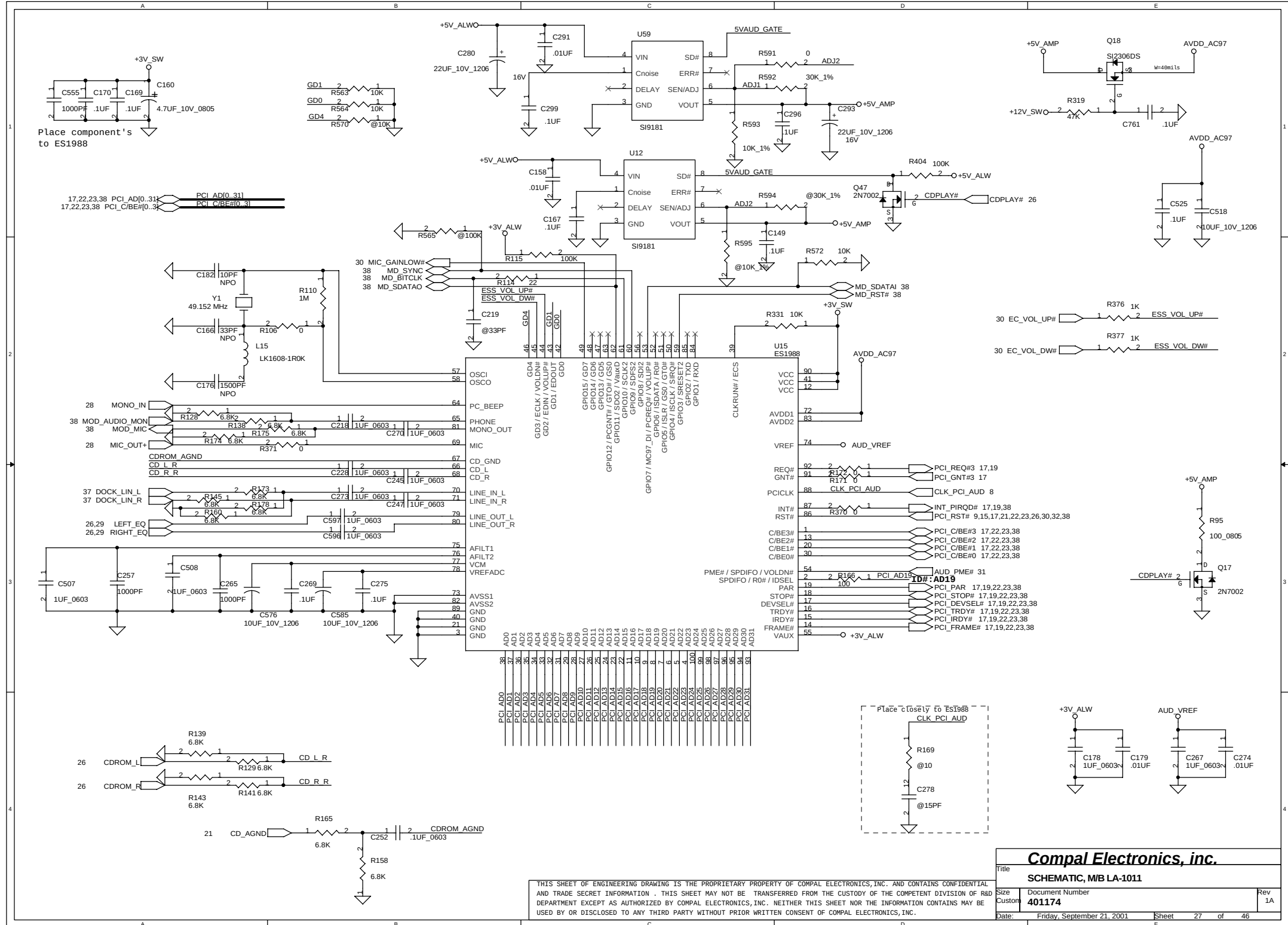
Layout note :
Cassia LANGND
should cover part
of U22.



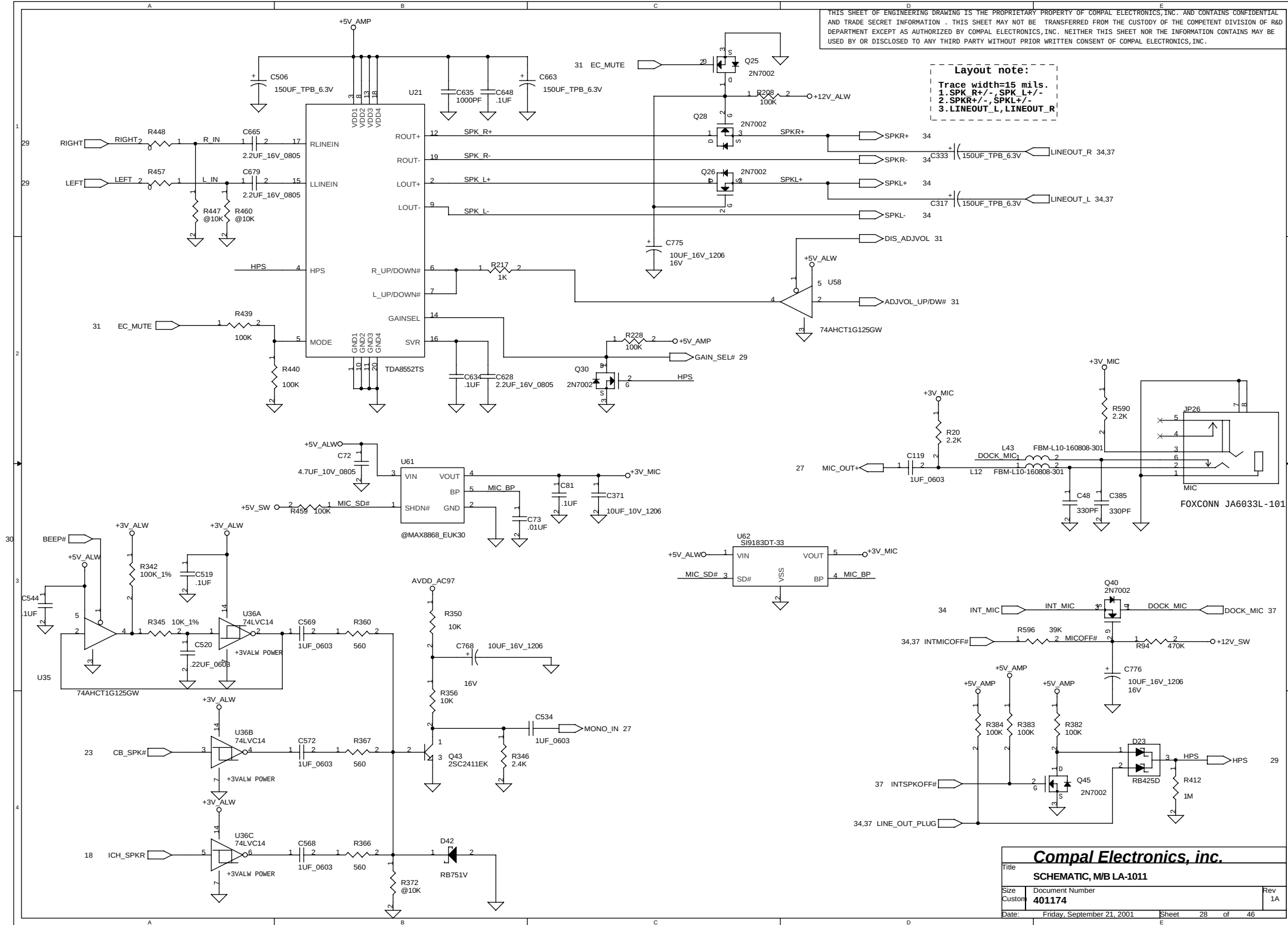


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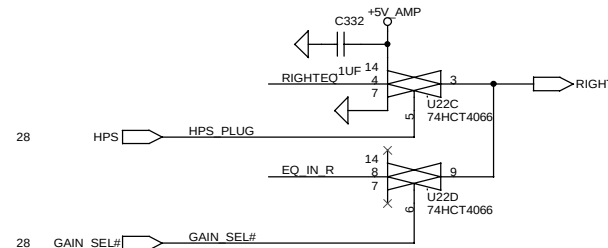
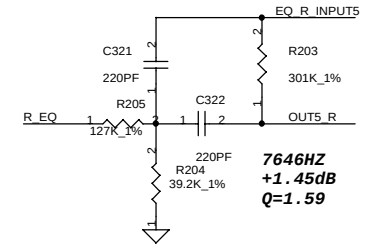
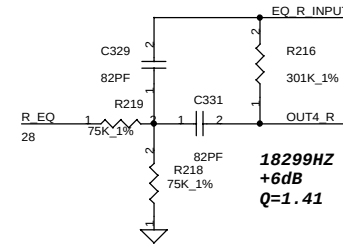
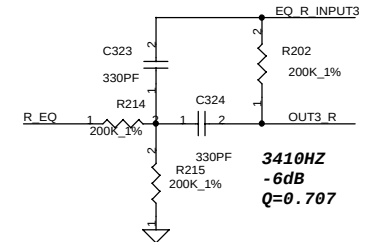
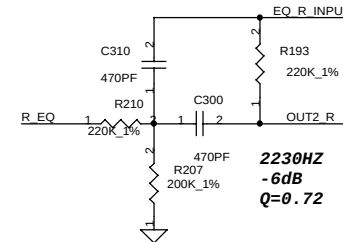
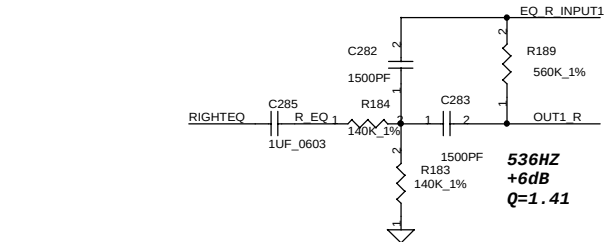
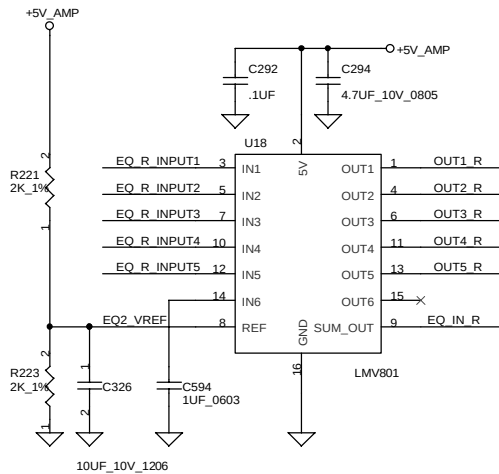
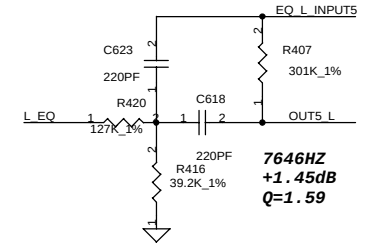
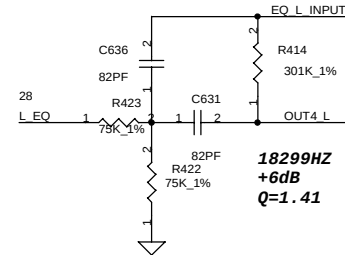
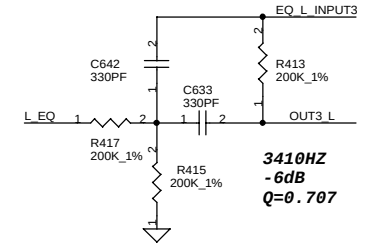
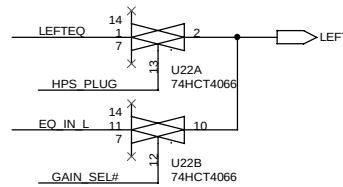
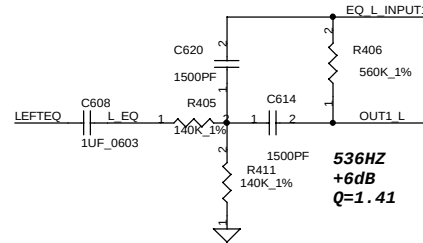
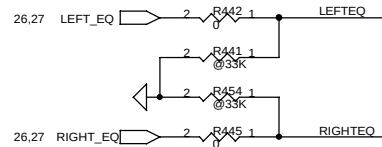
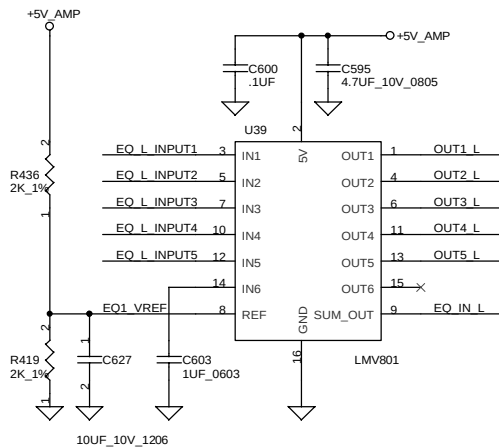


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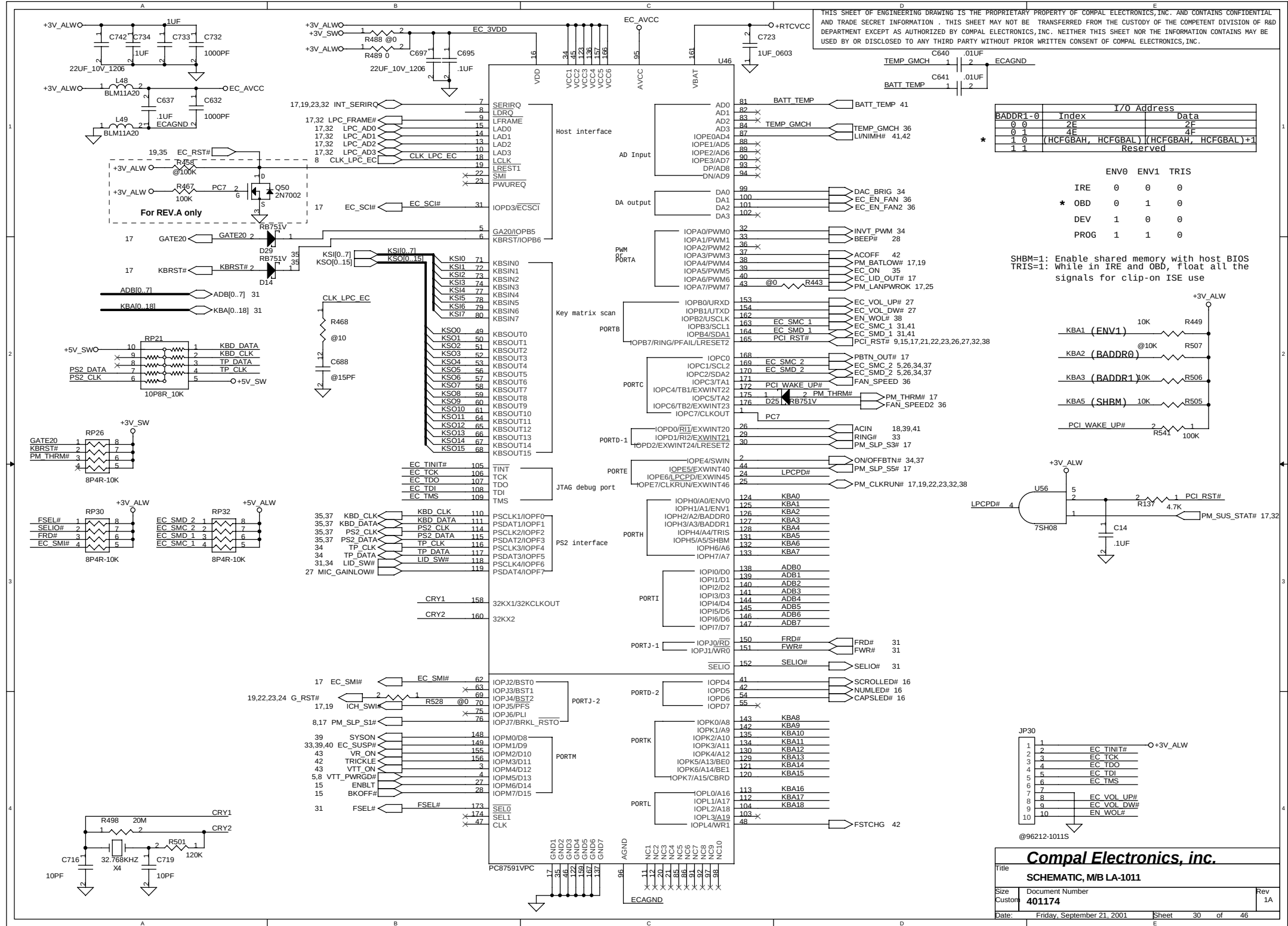
Size	Document Number
Custom	401174

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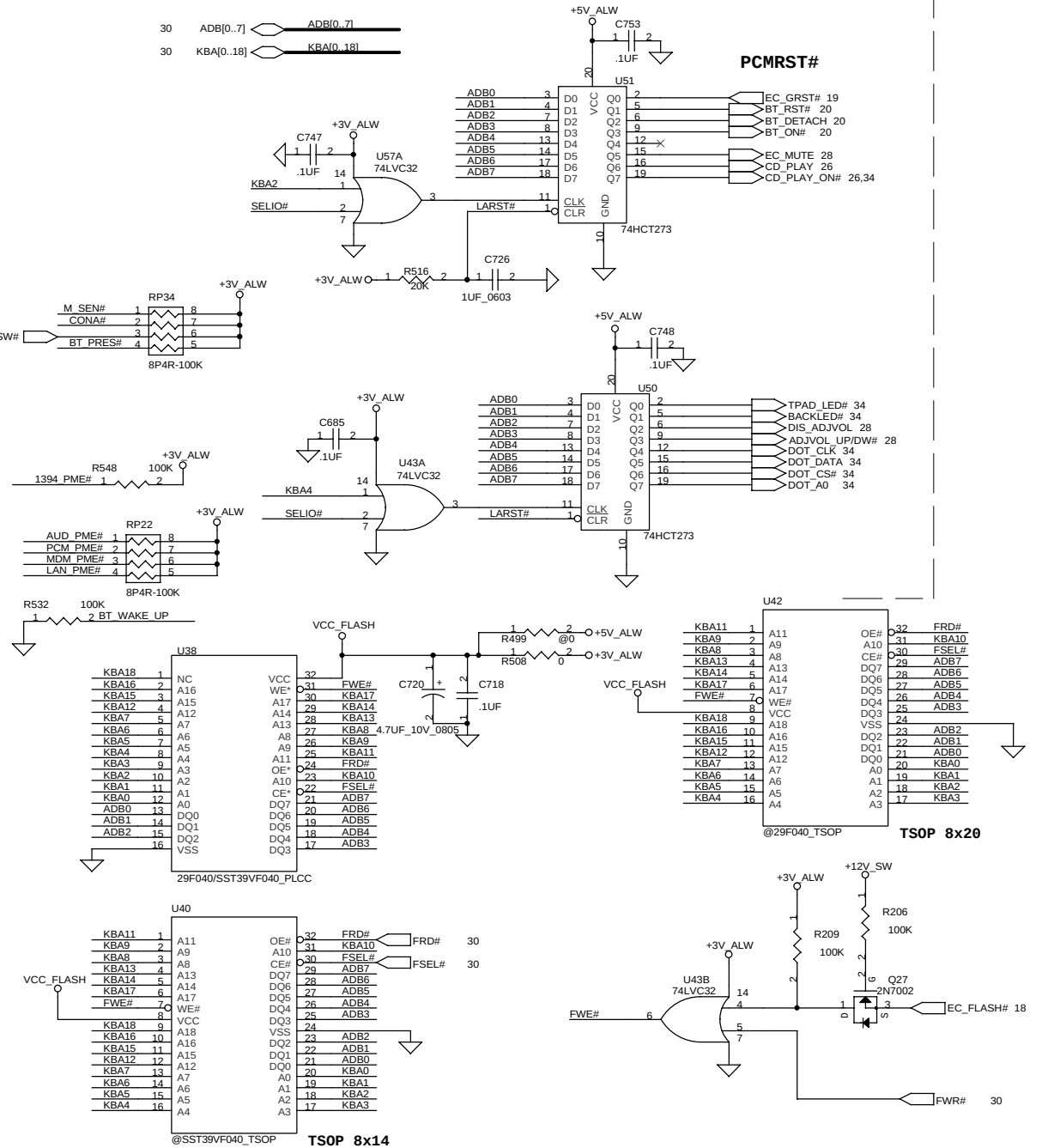


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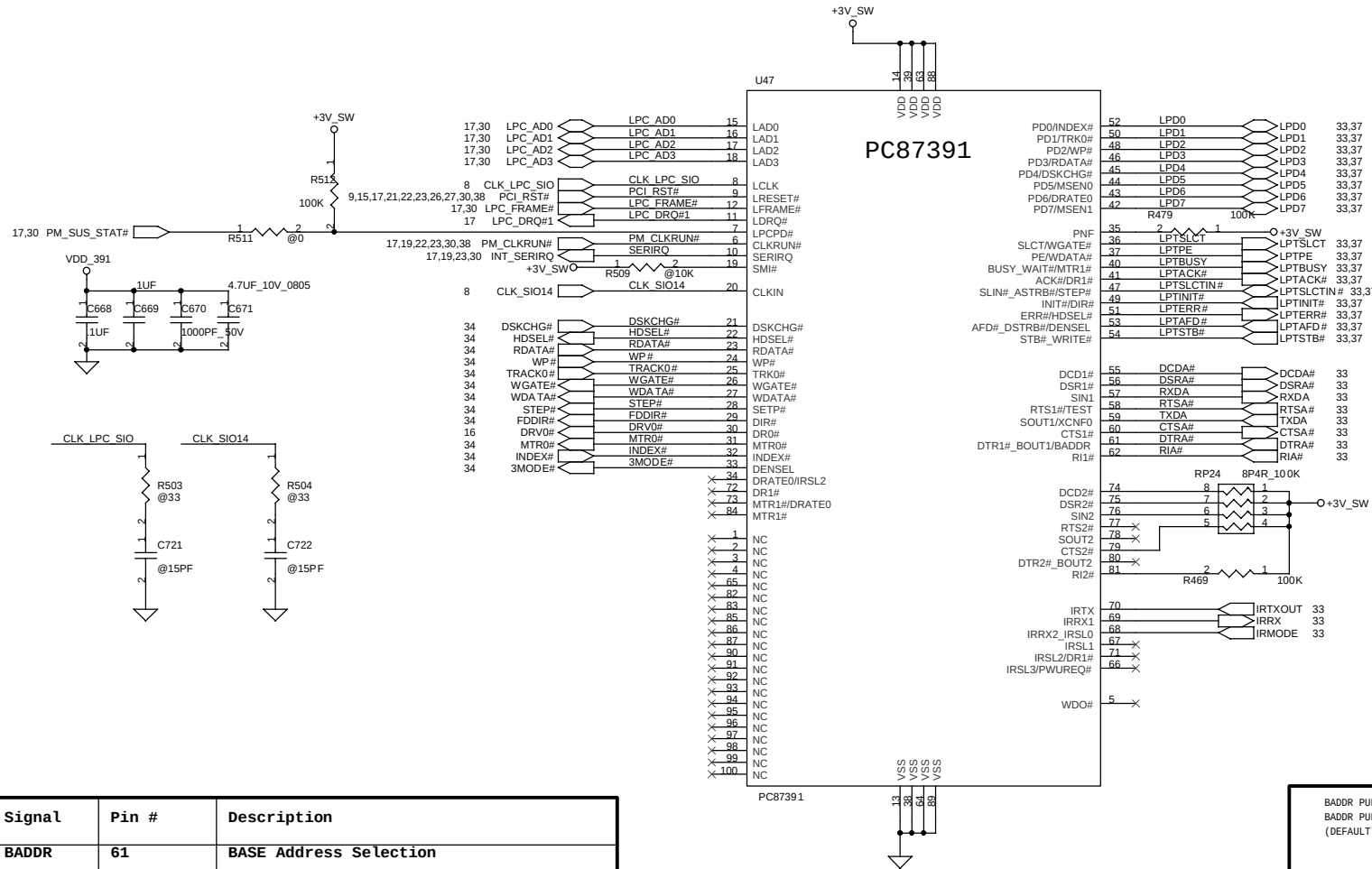
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Title	SCHEMATIC, M/B LA-1011		
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Date:	Friday, September 21, 2001	Sheet	29 of 46



OUTPUT



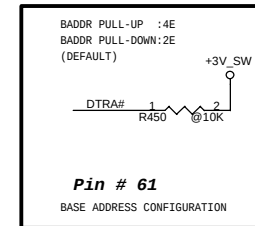
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Signal	Pin #	Description
BADDR	61	BASE Address Selection "0": 2E~2F (Default) "1": 4E~4F
TEST	58	"0": Normal (Default) "1": Test Mode
XCNF[2:0]	90, 4, 59	2 1 0 Function
		x 0 0 No BIOS
		x 0 1 Normal Mode. XRDY disabled
		0 1 0 Latch Mode. XA12~19, XRDY enabled
		1 1 0 Latch Mode. GPIO10~17,XRDY enabled
		0 1 1 Latch Mode. XA12~19, XRDY disabled
		1 1 1 Latch Mode. GPIO10~17,XRDY disabled

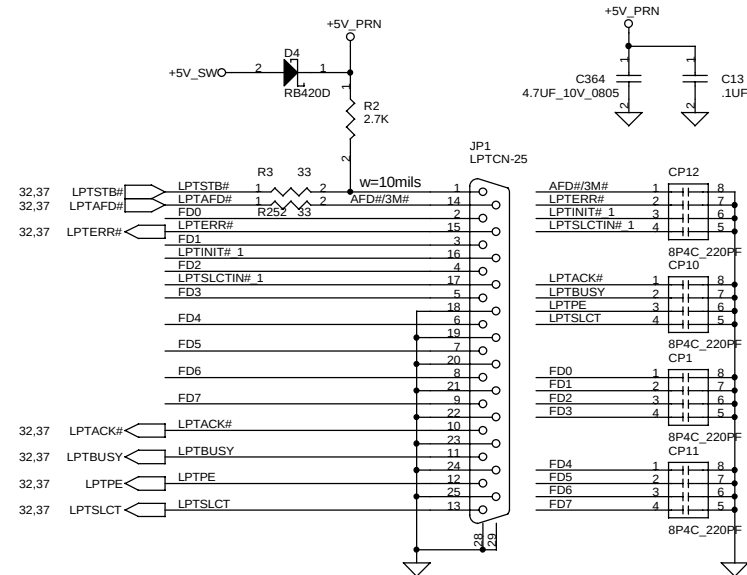
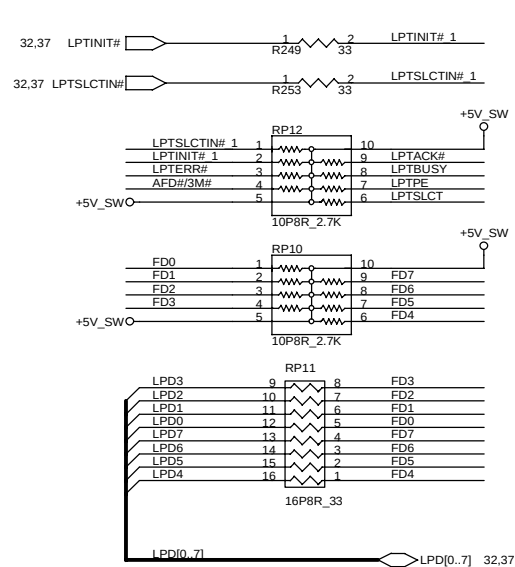
*1.ROM SOLUTION for PC87391

*2.ROM SOLUTION for PC87393

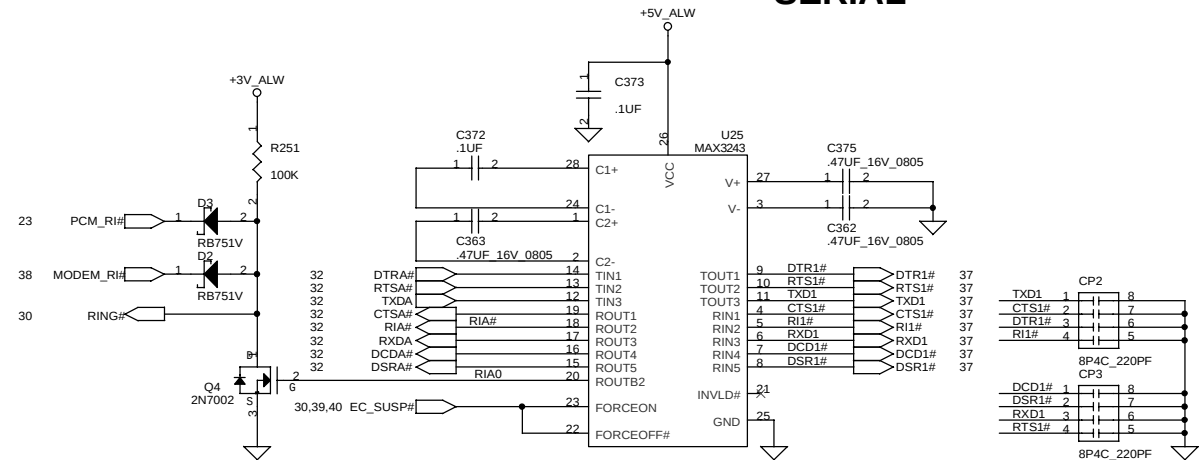
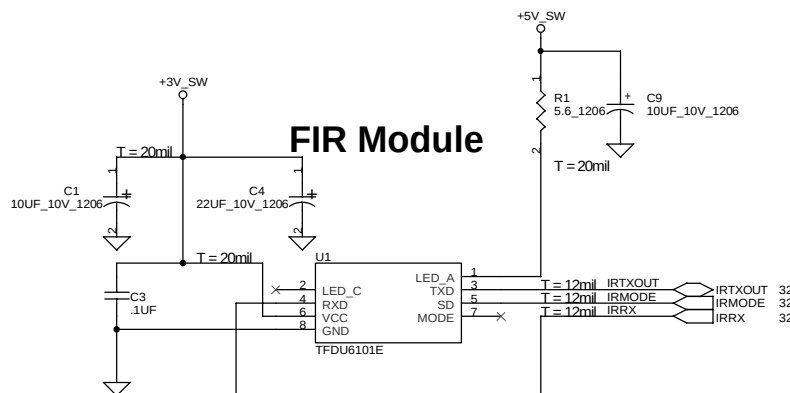


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PARALLEL



SERIAL



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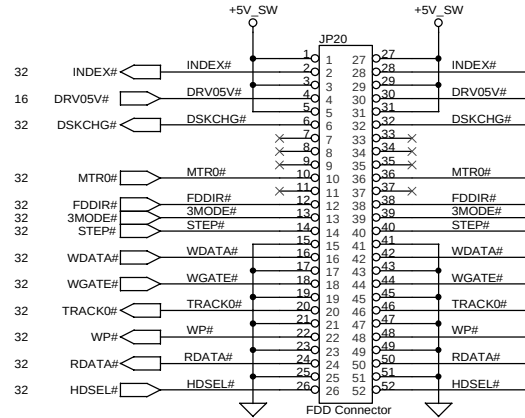
SCHEMATIC, M/B LA-1011

Size	Document Number
Custom	401174

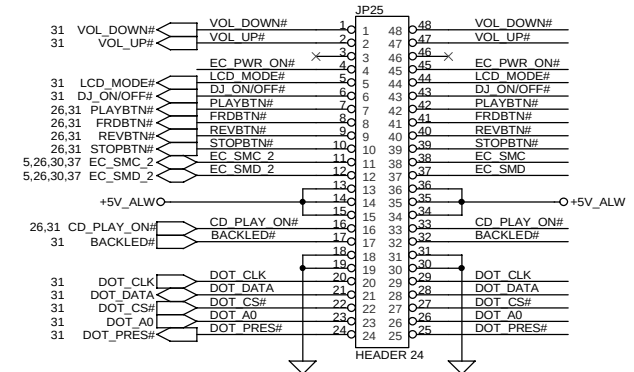
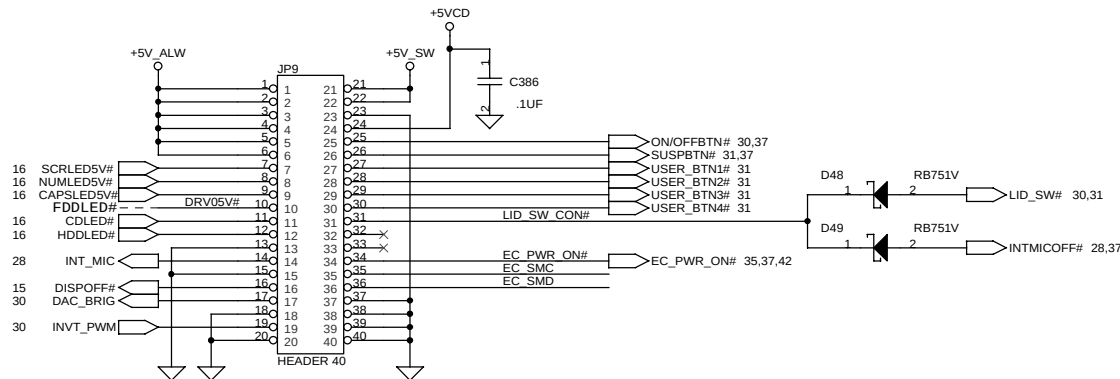
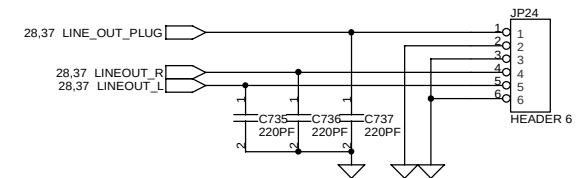
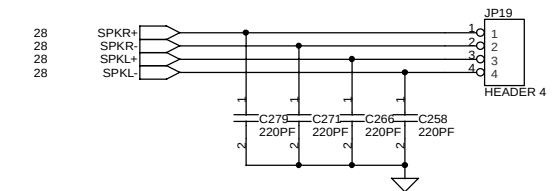
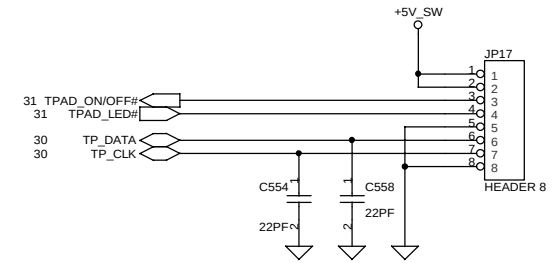
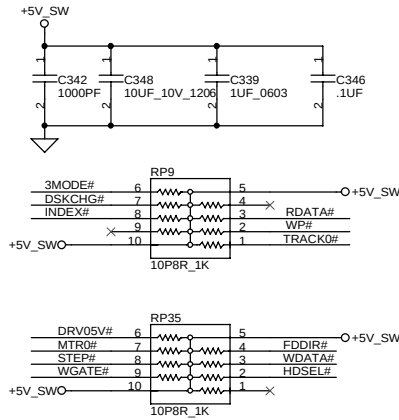
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FDD Connector



Layout note :
Place capacitors near Floppy connector .

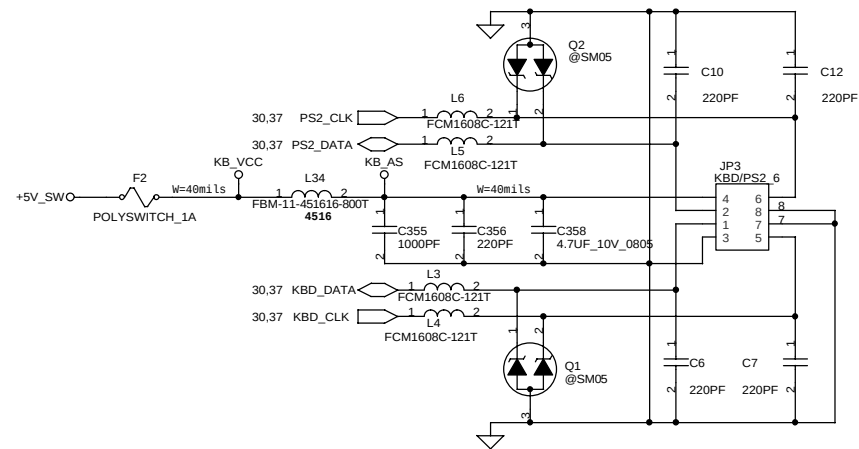
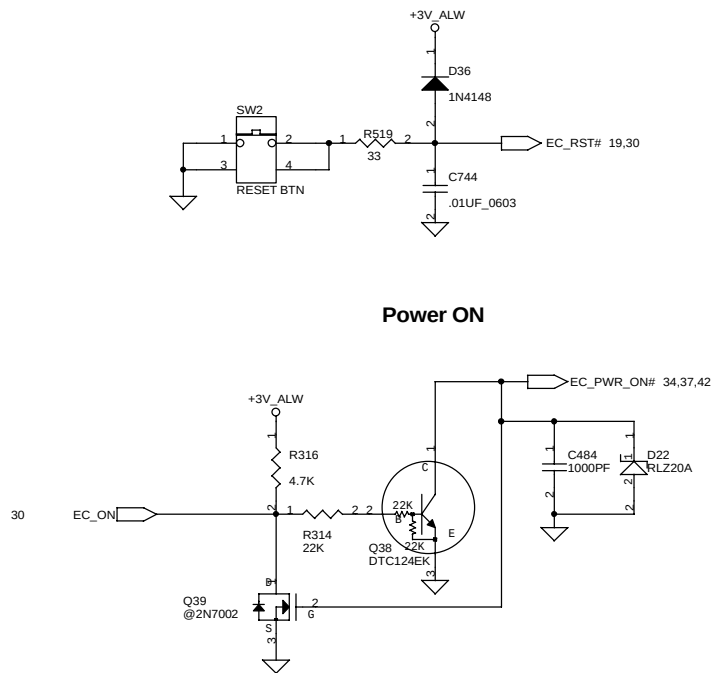
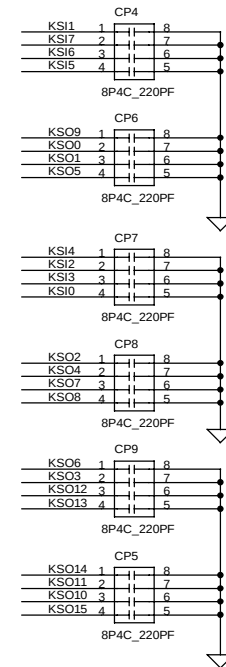
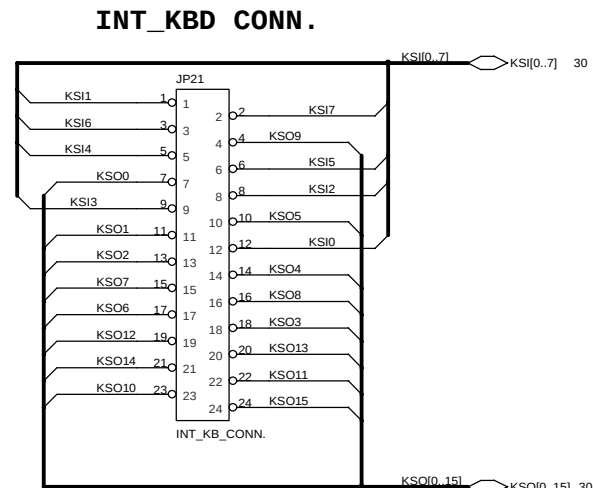
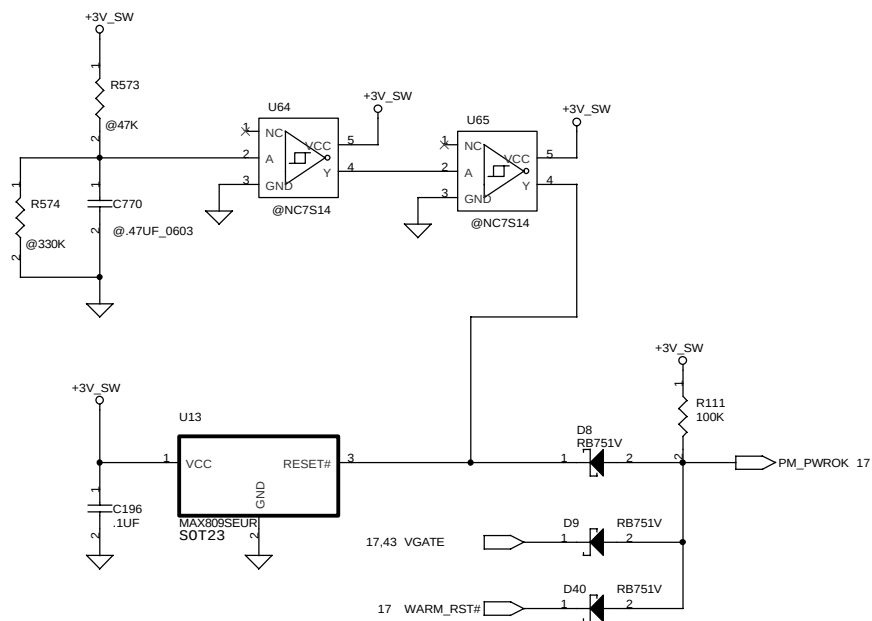


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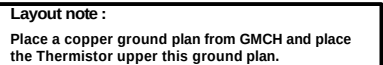
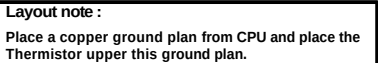
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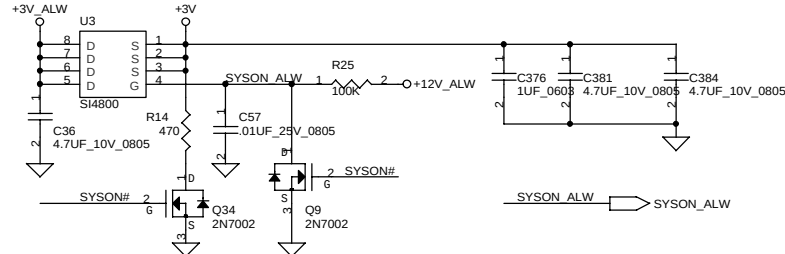


The circuit diagram shows the input stage of a 4-bit parallel adder. It consists of three inverters (U11B, U43C, U43D) and two 741VC32 inverters. The inputs are VL, +12V_ALW, +3V_ALW, and +3V_ALW. The outputs are 7, 8, 11, and 12.

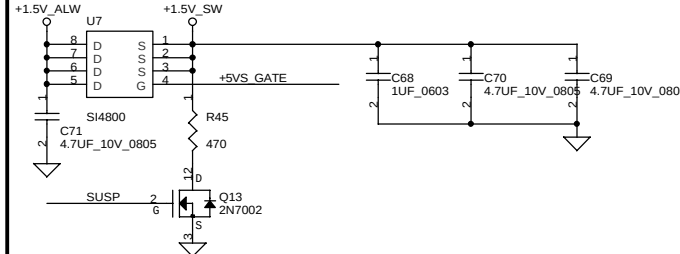
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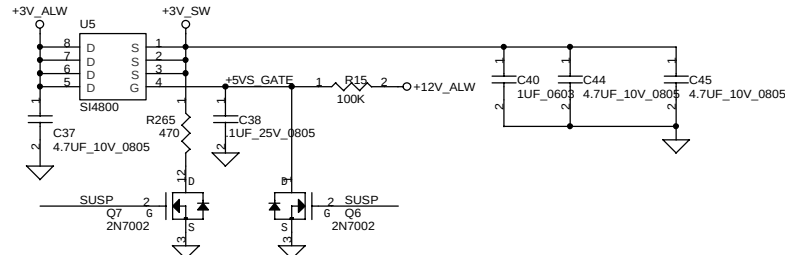
+3V_ALW TO +3V Transfer



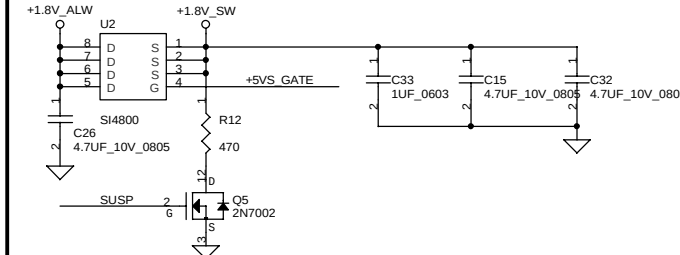
+1.5V TO +1.5V_SW Transfer



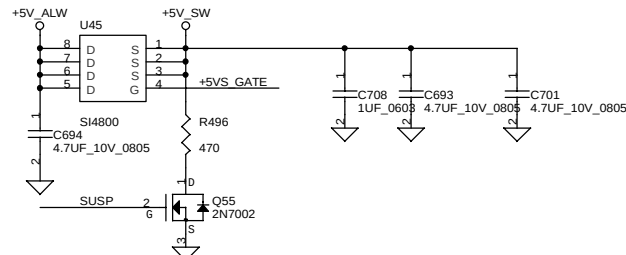
+3V_ALW TO +3V_SW Transfer



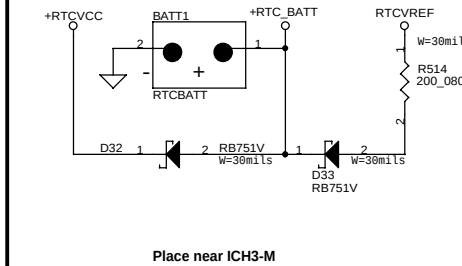
+1.8V_ALW TO +1.8V_SW Transfer



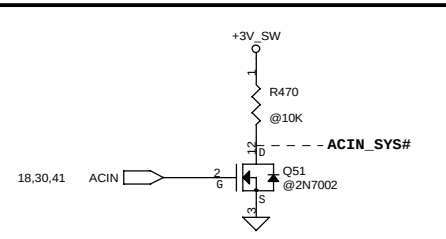
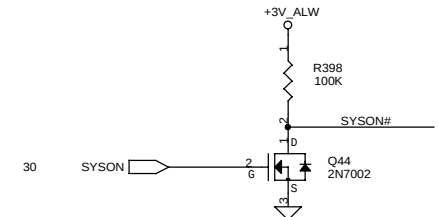
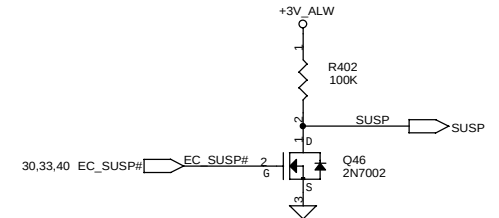
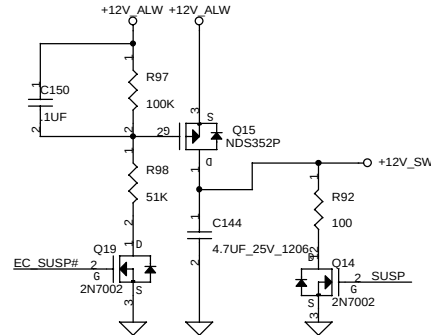
+5V_ALW TO +5V_SW Transfer



RTC Batt. Connector



+12V_ALW TO +12V_SW Transfer

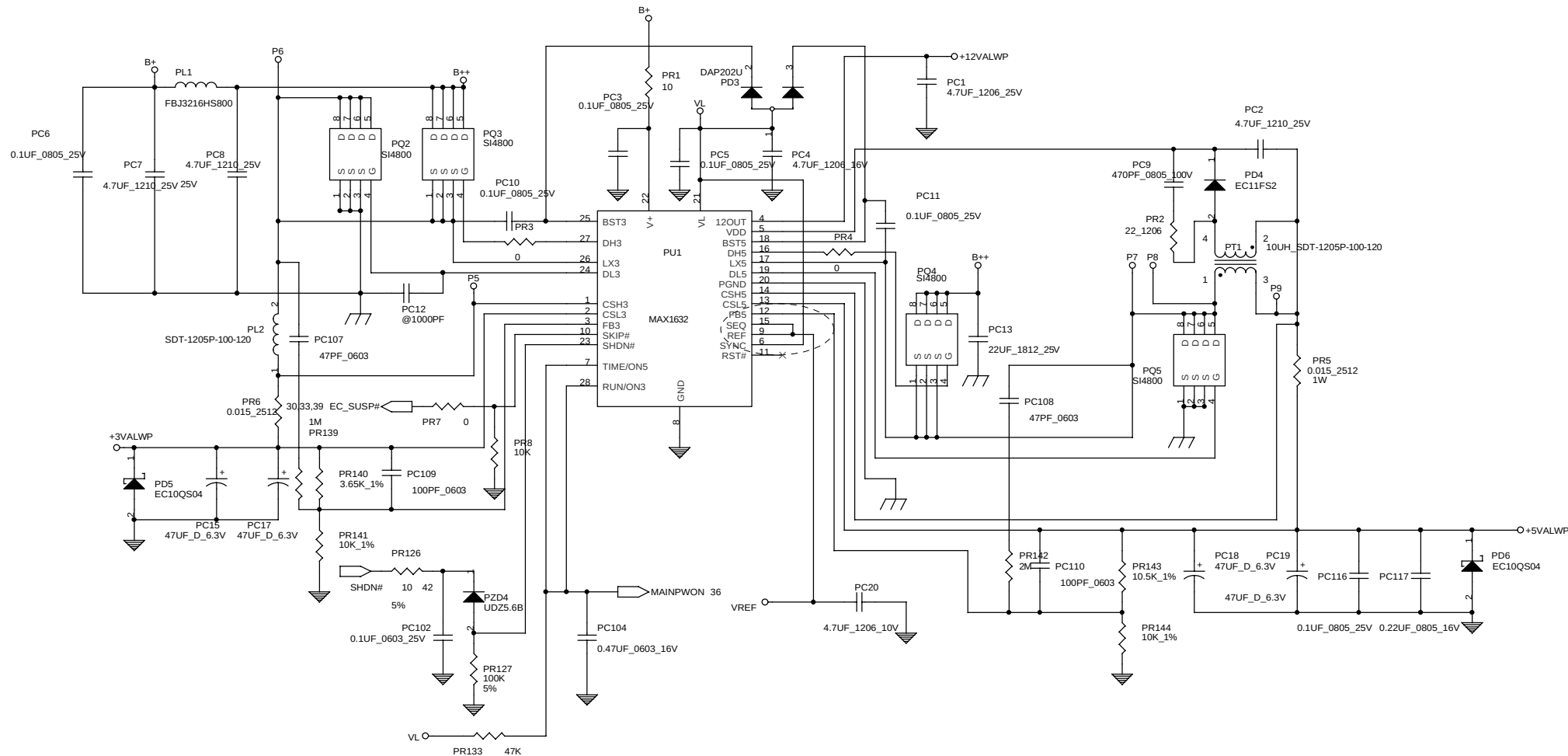


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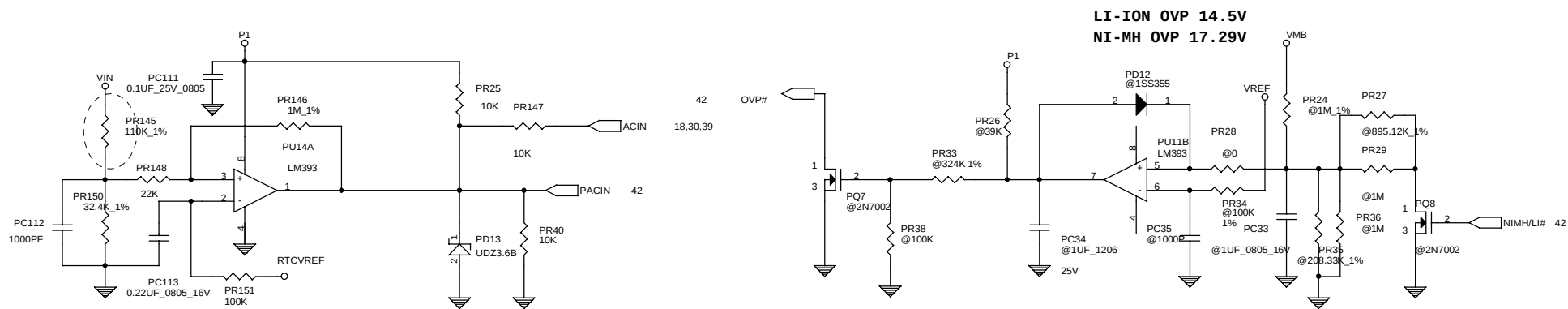
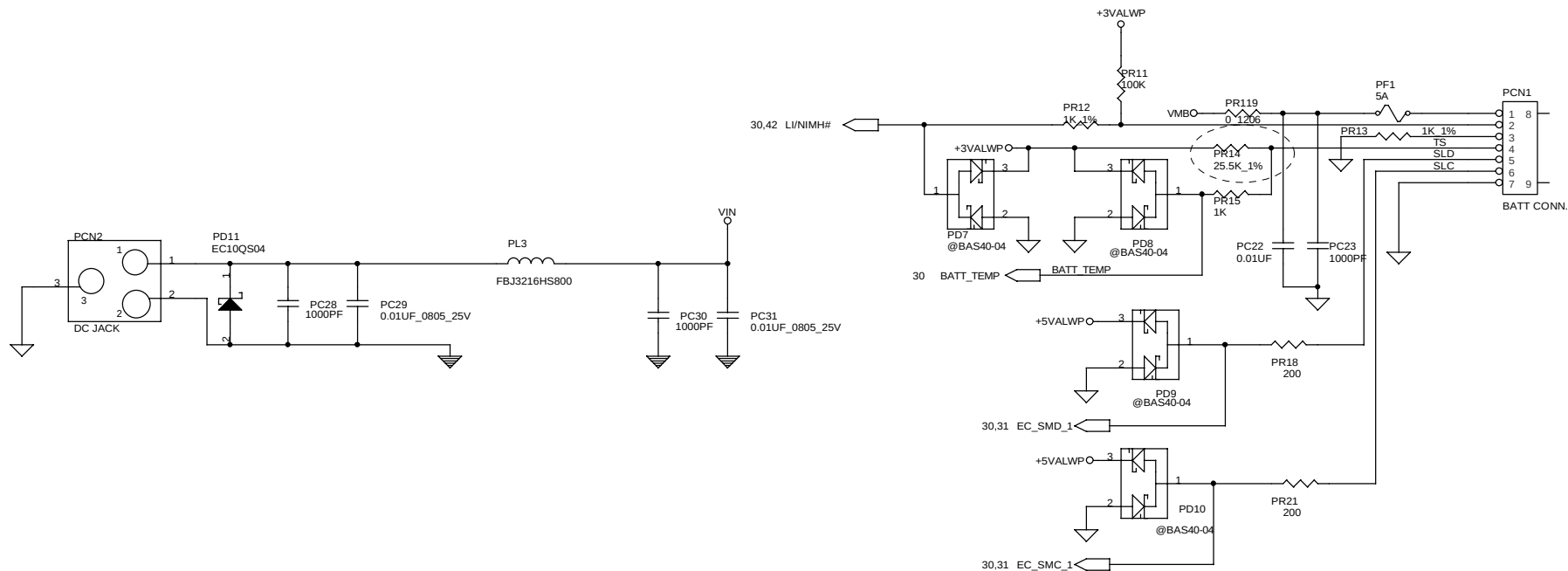
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ADAPTER CURRENT 2.9A

VINO

PR45 10K

PQ9 SI4835

PR42 @0

PQ11 SI4435

PR43 0.02_2512

PR47 150K

PC118 @1000PF

PQ10 SI4435

PC41 4.7UF_1210_25V

PC42 4.7UF_1210_25V

PQ43 0.1UF_0805_25V

PQ12 SI4435

PL5 22UH_SPC-1207P-220

PR46 0.02_2512

PR40 1W

PC40 4.7UF_1210_25V

PC106 22UF_1812_25V

PQ13 2N7002

PR152 47K

PD27 1SS355

PQ14 DTC115EK

ACO

PR53 10K

PR54 27K_1%

PR55 10K

PC46 4700PF_0603_50V

PC48 2200PF_0603_50V

PR57 10K

PR58 24.9K_1%

PC47 0.1UF

PR61 1.2K_0.5%

PR60 16.9K_1%

PC51 0.1UF_0805_25V

PR64 10K_1%

PR62 10K

PR63 324K_1%

PC50 1500PF

PR65 47K

PR66 69.8K_0.5%

PR67 150K_0.5%

PR68 215K_0.5%

PR69 100K

PQ17 2N7002

PC52 0.1UF

PQ19 DTC115EK

LI/NIMH# 30,41

CHGRTCP

PR70 200_0805

PC54 1UF_0805_25V

PZD2 RLZ16B

PC55 10UF_1206_10V

PU6 S-81235SG

CHGRTCP

PR71 100K

PZD1 RLZ6.2C

PC53 0.22UF_1206_25V

PR72 22K

EC_PWR_ON#

SHDN#

PD18 RB751V

PD19 RLS4148

PQ18 TP0610T

TRICKLE

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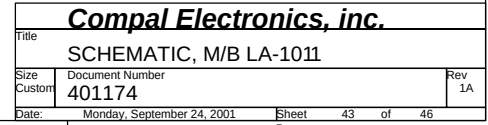
339

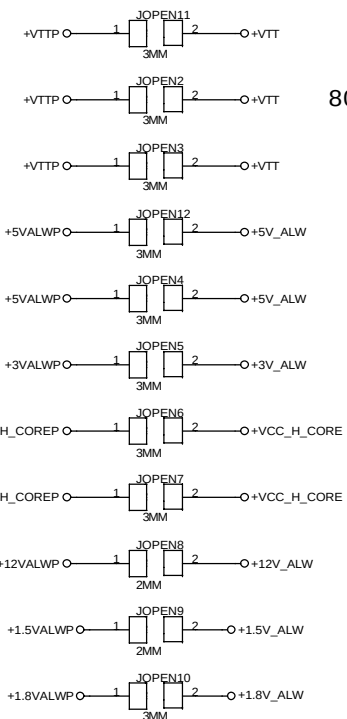
CC: 2.87A LI-ION FAST
CC: 2A NI-MH FAST
.273A LI-ION TRICKLE
.265A NI-MH TRICKLE

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Power PIR

Item	Fixed Issue	Reason for change	Page	Modify item	MB_Ver.	Phase
1		System shutdown	41	Add PR126,PC102,PZD4,PR127	0.2	EVT
2		Modify OTP function	41	Add PR132,PR133,PC104	0.2	EVT
3		Improve cpucore thermal and efficiency	43	Add PR128,PR129,PR130,PR131,PC103,PU13	0.2	EVT
4		Change VTTP OCP protect point	43	1.Change PR107 from 15K to 10K 2.Change PR108 from 10K to 15K	0.2	EVT
5		Eliminate +2.5VP	44	Delete PQ33,PQ34,PR122,PR121,PR123,PR124 PC99,PC98,PC100,PC101,PQ32	0.2	EVT
6		Change VTTP output voltage from 1.2V to 1.35V	43	Change PR106 from 2K to 3.57K	0.2	EVT
7		Change cpucore offset voltage	43	1.Change PR100 from 402K to 604K 2.Change PR101 from 64.5K to 61.9K 3.Change PR103 from 16.9K to 16.2K	0.2	EVT
8		Change cpucore deepper sleep mode output voltage	43	1.Connect S0 to REF 2.Connect S1 to REF	0.2	EVT
9		Avoid Vgate going low when cpu make speedstep transition	43	Add PR134,135,136 &PD26	0.2	EVT
10		EC can't detect the BATT. by PC87591	41	Change TS pin pull high voltage from +5VALWP to +3VALWP	0.3	DVT
11		Improved cpucore efficiency	43	1.Eliminate PR120 2.Change PR85 from 4m to 2m 3.connect Ton pin to VCC	0.3	DVT
12		Change VTTP OCP protection point	43	1.Change PR108 from 15K to 30K	0.3	DVT
13		To avoid mechanical interferenc	42	Add PC106		
14		Change geyserville function from MAX1718 to external	43	1.Delete PR73~76,PC56~60 2.Delete PR80,82,83,84.86 3.Connect PU8.19PIN to GND	0.3	DVT
15		To improve EMI issue	43	1.Add PR87 to PU8.28 PIN in series 2.Add PR138 to PU10.1 PIN in series	0.3	DVT
16		Delete redundant parts.	42 & 43	1. Delete PC39 on page 42. 2. Delete PD21 on page 43.	0.5	DVT

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N32N101 Rev0.4 HISTORY LIST (PIR)

For C-Test 09/03/2001 Rev:1.0

Date	Page	Description
07/09	P11	SWAP DVOA_I2CCLK & DVOA_I2CDATA R105 REPLACEMENT DVOC_FLD CHANGE TO U30.M25
	P15	BOM ADD C560 22PF,C578 12PF BOM DEL R534 75_1%
	P16	R4,R256,R250 150_1% --> 75_1% ADD R135,R142 33
	P21	R243 PULL HIGH TO +3V_SW
	P35	BOM DEL Q39 2N7002
	P27	BOM DEL R570 10K
07/16	P30	Remove CDLED#,HDDLED#
	P37	Add D12 DAN202U
	P26	Add R530,R531 10K
	P31	ADD RP22 8P4R_10K R548 10K
	P16/21	HDDLED# LEVEL SHIFT
07/19	P38	BOM del R478, add R477 0 CONNECT JP31 Pin111 TO Pin116
	P27	C507,C508 1UF_0603
	P28	BOM DEL U61,ADD U62 SI9183DT-33
	P30	BOM DEL R458 10K
	P19	ADD R549 0,U63 7SH08
	P31	U51.2 EC_GRST#
07/23	P16	ADD D47 RB491 ADD Q61,Q61 2N7002
	P31	ADD R532 10K
07/25	P5	R37,R273 10K -> 100K
	P8	R365,R231,R229 10K -> 100K
	P11	R363,R369 4.7K -> 100K RP36 8P4R_4.7K -> 8P4R_100K
	P14	R194 10K -> 100K
	P15	RP15 8P4R_4.7K -> 8P4R_100K R337 10K -> 100K
	P17	RP18 8P4R_10K -> 8P4R_100K
	P18	RP19 8P4R_10K -> 8P4R_100K
	P19	R461,R466,R550 10K -> 100K R558,R559 4.7K -> 100K
	P21	R242 10K -> 100K
	P22	R130,R116,R136,R197,R198 4.7K -> 100K
	P24	R561,R562 10K -> 100K
	P25	R347 10K -> 100K
	P26	R462,R463,R480,R530,R531 10K -> 100K
		RP29 8P4R_10K -> 8P4R_100K RP27 10P8R_10K -> 10P8R_100K
	P27	R115 10K -> 100K
	P28	U35 74LVC125 -> 74AHCTG125GW R439 4.7K -> 100K
		R440 20K -> 100K Add U66 NC7ST32
	P30	R467,R541 10K -> 100K R449,R506,R505 1K -> 10K
	P31	RP22,RP34 8P4R_10K -> 8P4R_100K R548,R532 10K -> 100K
	P32	RP24 8P4R_10K -> 8P4R_100K R469,R479 10K -> 100K
	P35	R111 10K -> 100K
	P36	R276,R510 10K -> 100K
	P37	Add PAD4,5,6,7
	P39	R402,R398 10K -> 100K
07/27	P27/30	Add MIC_GAINLOW# IN U15.49 & U46.119
07/31	P27	R139,R143 33K->6.8K R129,R141 20K->6.8K
	P26	ADD R575,R576 10K C771,C772 10UF
08/01	P26	ADD C773, C774 1uF/25V

Date	Page	Description
08/03	P28	Remove U66, connect "EC_MUTE" to R439.1
	P37	Add D48, connect D48.3 to JP9.31, D48.1 to "LID_SW#", D48.2 to "INTMICOFF#"
08/16	P28	Add C775 parallel with pin R208.1 and GND, add a 2.2K ohm bias resistor R590 by +3V_MIC on pin JP26.3 and change R217 value from 2.2K ohm to 1K ohm.
09/03	P27	Change SI9181(U12 & U59) from fixed to adjustable version. Add 30Kohm resistor R592(R594) and 10Kohm resistor R593(R595) to make output voltage at 4.8V.
	P28	Add a 39Kohm serial resistor R596 and change R94 value from 100Kohm to 470Kohm to solve pop sound when Int-MIC mute.
	P34	Change D48 from one DAN202U to two RB751Vs.
	P7	Change R68 from 1Kohm_1% to 499ohm_1% and R65 from 2Kohm_1% to 1Kohm_1% by Intel recommended.
09/05	P27	Change C167, C299 value from .01uF to .1uF.

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