

U1 - KAL00

Compal Confidential
Schematics Document

AMD S1g2/ ATI RS780M / SB700

Wednesday, January 16, 2008

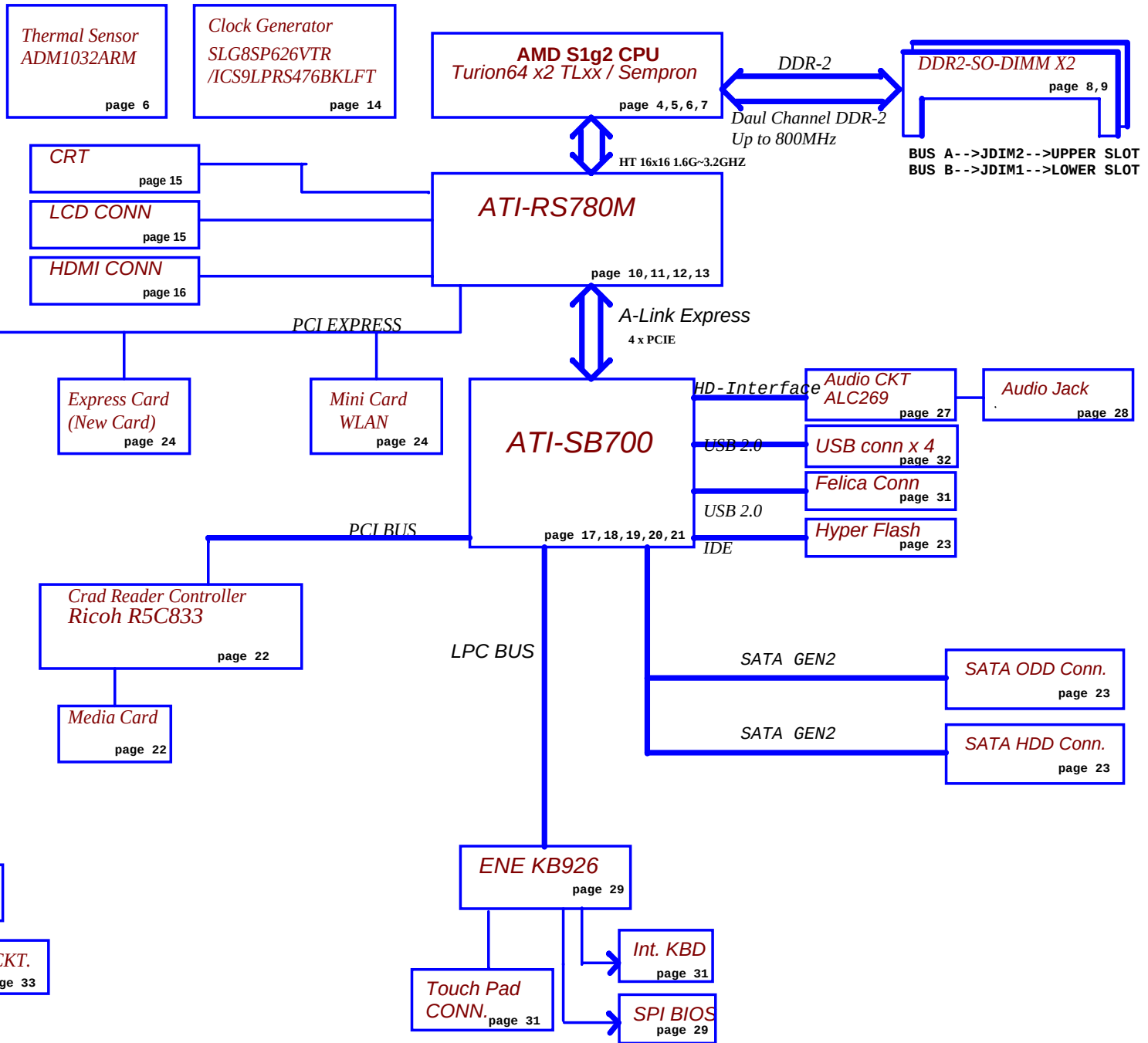
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Issued Date	2007/12/12	Deciphered Date	2008/12/12	Cover Sheet	
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Project Code: ANRKAL0000(KAL00)

File Name : LA-4381P

PCB P/N:



Security Classification	Compal Secret Data			Title	
Issued Date	2007/12/12	Deciphered Date	2008/12/12	Block Diagrams	
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Power Plane	Description	S1	S3	S4/ S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE0,1	Core voltage for CPU	ON	OFF	OFF
+VDDNB	+0.8V~1.1V CPU NBVDD	ON	ON	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.2VALW	1.2V always on power rail	ON	ON	ON
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD21	0	PIRQE/PIRQF/PIRQG

Device	Address	Device	Address
Smart Battery	0001 011X b?	ADM1032	1001 110X b?
EEPROM(24C16/02)	1010 000X b?		
(24C04)	1011 000Xb?		

Device	Address
Clock Generator (ICS9LPRS476BKLFT)	1101 001Xb?
DDRII DIMM0	1001 000Xb?
DDRII DIMM1	1001 010Xb?

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

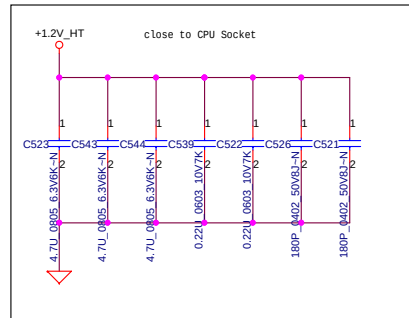
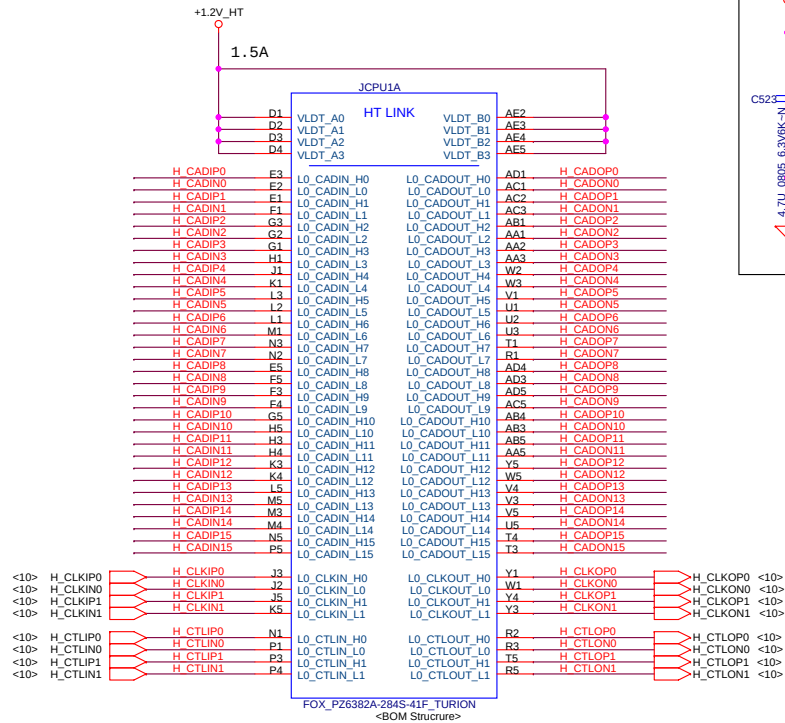
Board ID	PCB Revision
0	0.1 (U1 ES1)
1	0.2 (U1 ES2)
2	0.3 (U1 PP)
3	0.4 (U1 PPR)
4	1.0 (U1 IRT)
5	
6	
7	

[illegible]

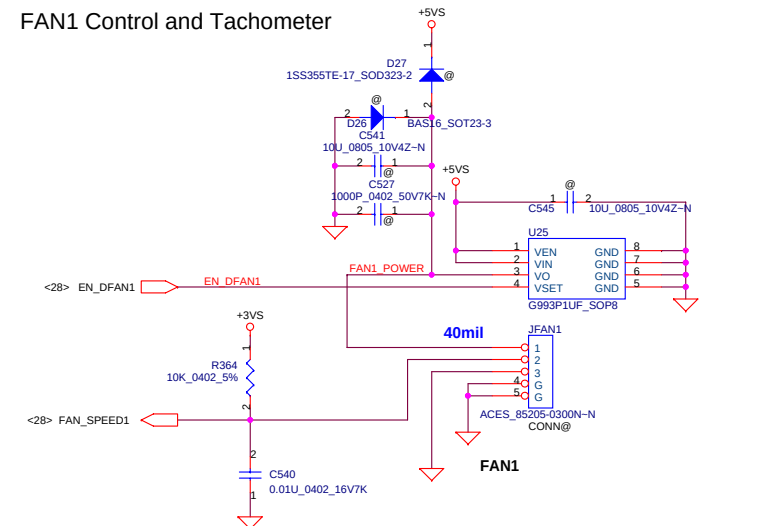
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<10> H_CADIP[0..15] H_CADIP[0..15]
<10> H_CADIN[0..15] H_CADIN[0..15]

H_CADOP[0..15] H_CADOP[0..15] <10>
H_CADON[0..15] H_CADON[0..15] <10>

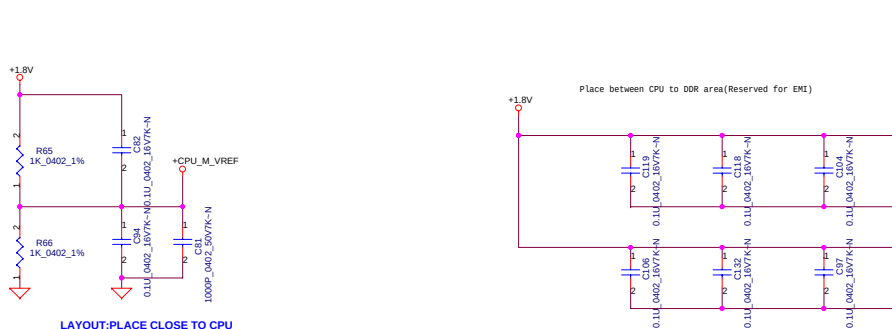
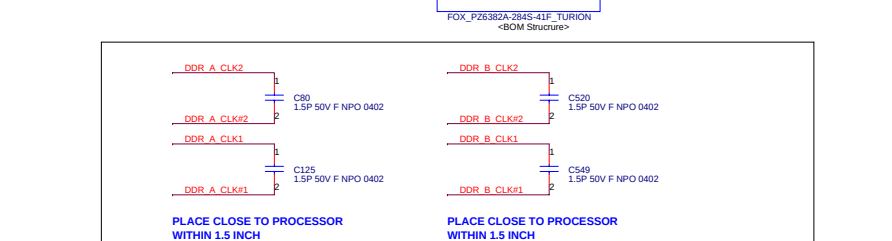
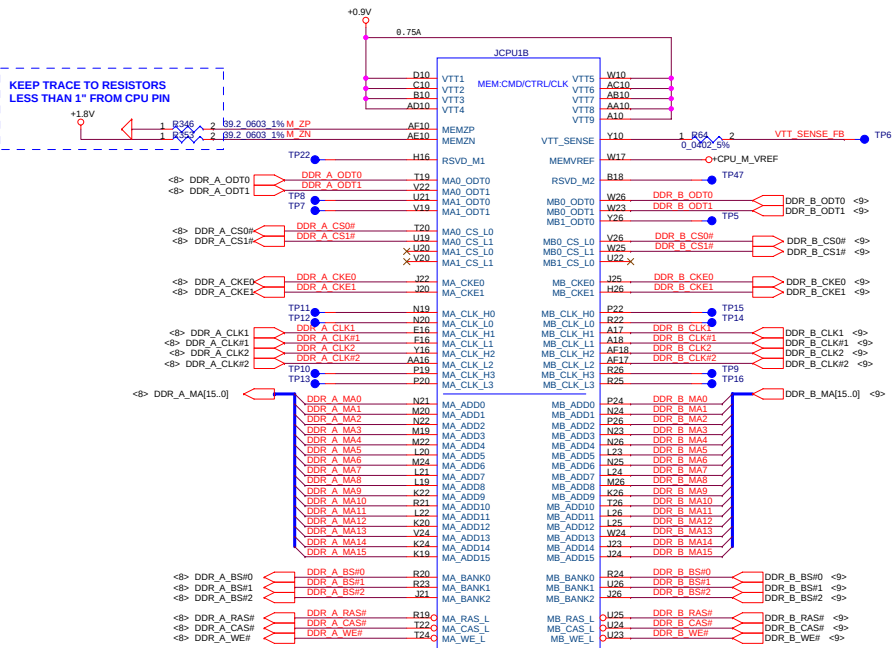


FAN1 Control and Tachometer

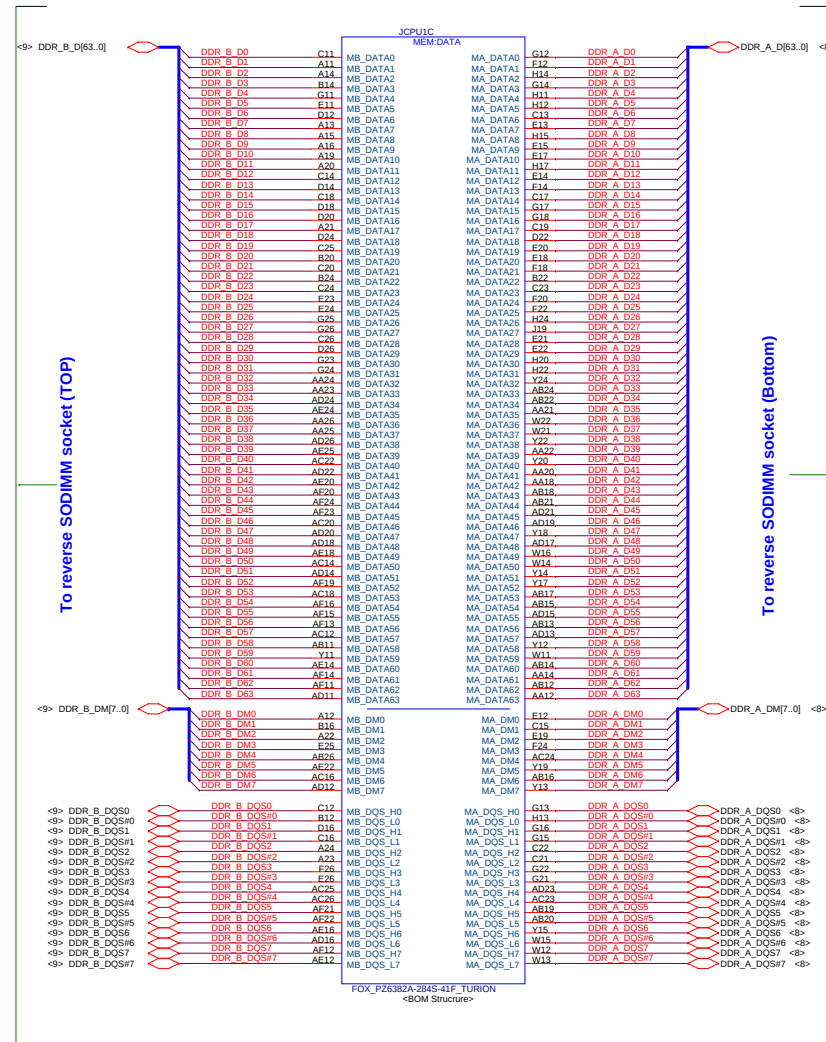


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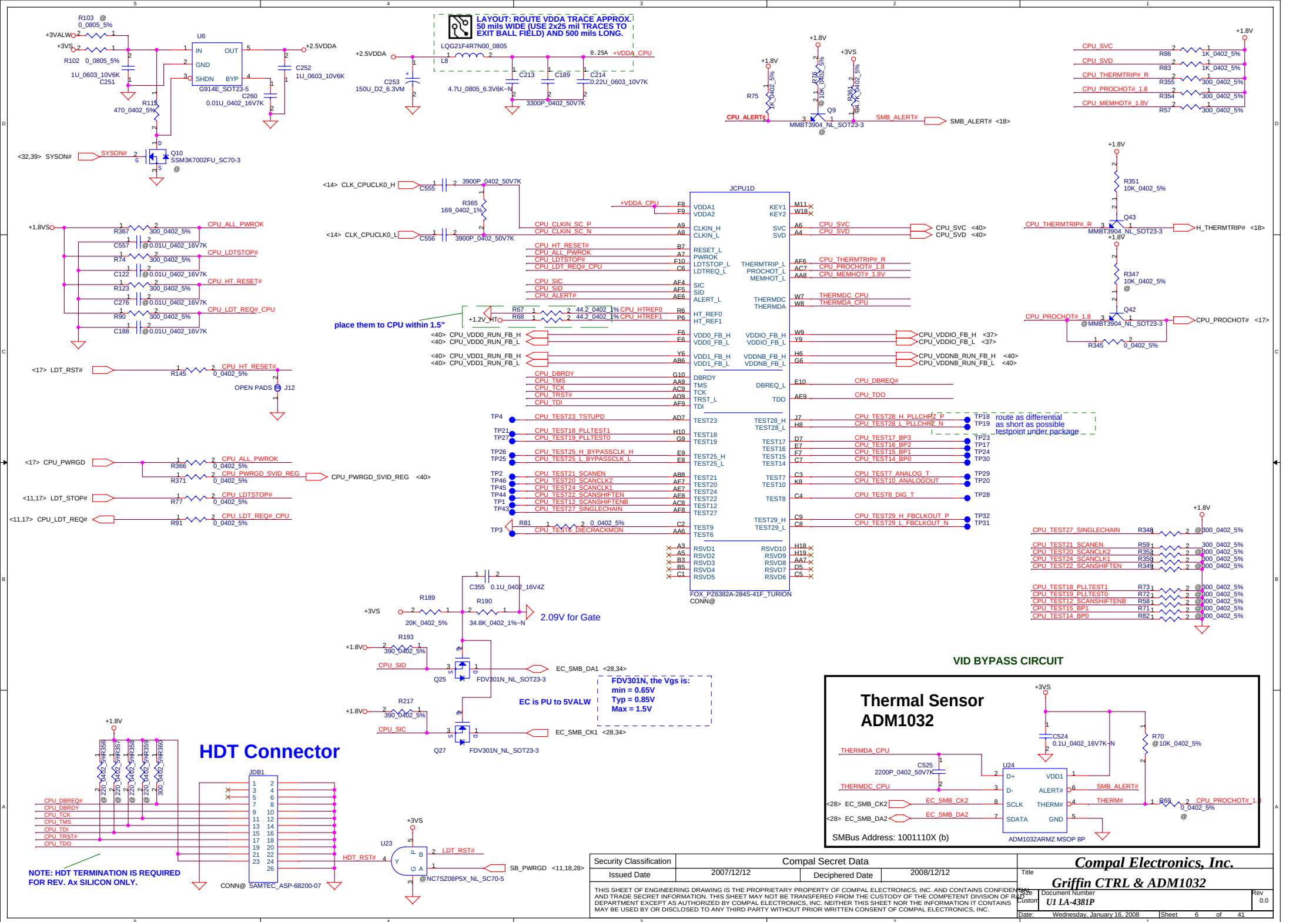
VDD VTT SUS CPU IS CONNECTED TO THE VDD VTT SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Processor DDR2 Memory Interface



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VDD(+CPU_CORE) decoupling.

Near CPU Socket

Under CPU Socket

Under CPU Socket

Between CPU Socket and DIMM

180PF Qt'y follow the distance between CPU socket and DIMM0. <2.5inch>

A: Add C165 and C176 to follow AMD Layout review recommend for EMI

C: Change to NBO CAP

+CPU_CORE_NB decoupling.

The diagram illustrates the decoupling circuit for the CPU core. It consists of three capacitors, C113, C114, and C102, all specified as 22U_0805_6.3V6M. These capacitors are connected in parallel between the +VDDNB supply line and a common ground. The ground connection is indicated by a red triangle pointing downwards.

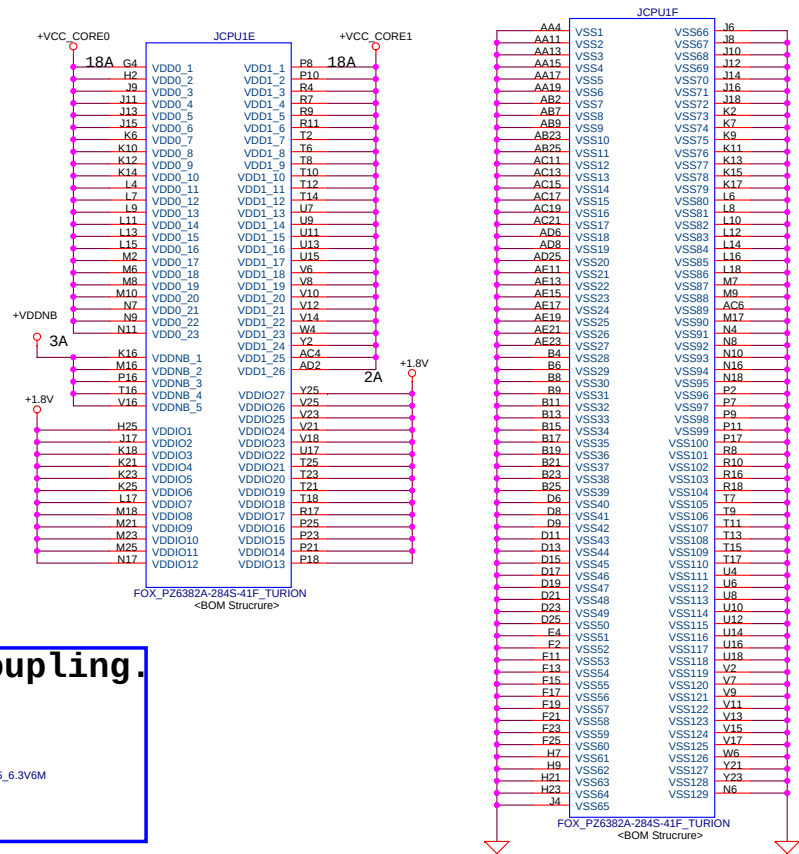
VTT decoupling.

Near Power Supply
C: Change to NBO CAP
C50
220U_Y_4VM

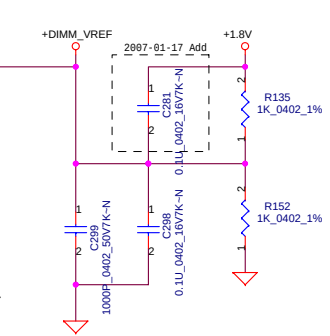
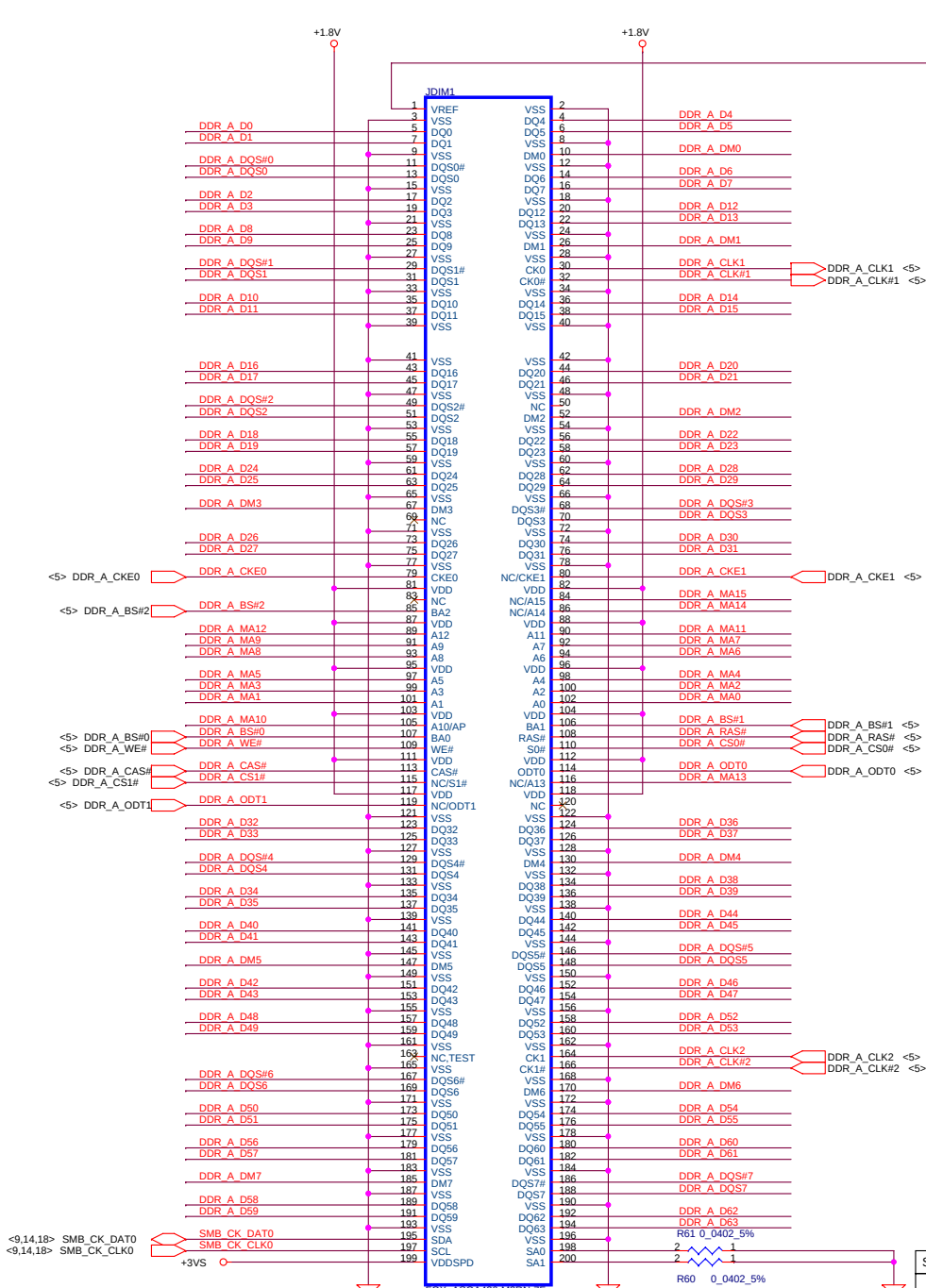
Near CPU Socket Right side.

Near CPU Socket Left side.

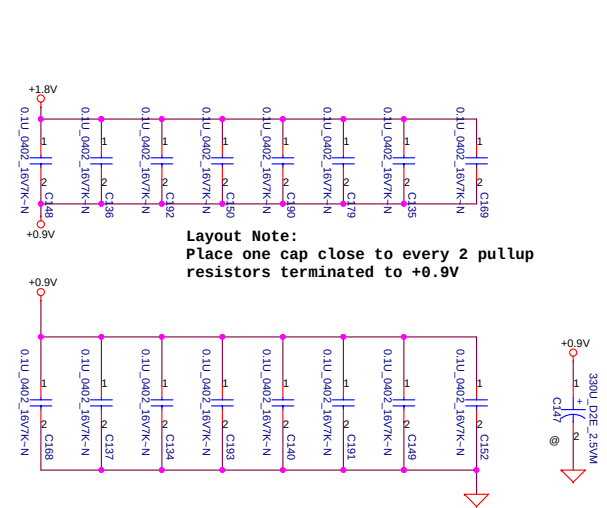
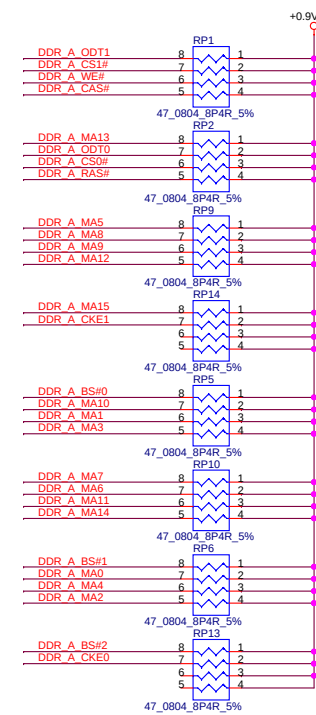
The diagram illustrates the VTT decoupling layout. It shows a top layer (blue) and a bottom layer (green) connected by vias (yellow). The layout includes a power supply section at the top with a +0.9V source and a decoupling capacitor C50 (220U_Y_4VM). Below this, there are two rows of decoupling capacitors (C215, C216, C551, C550, C553, C554, C552, C559) connected to the +0.9V supply. The bottom row of capacitors (C49, C47, C48, C46, C77, C45, C79, C78) is connected to the bottom layer. The layout is labeled 'Near CPU Socket Right side.' and 'Near CPU Socket Left side.'.



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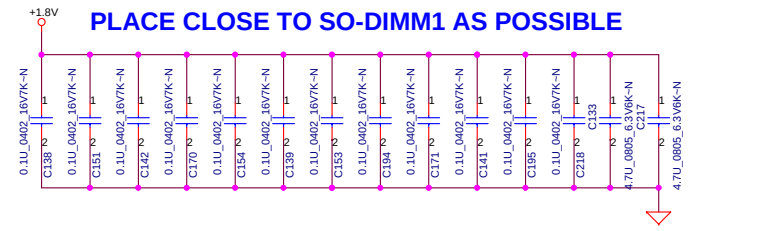
- <5> DDR_A_D[0..63] → DDR A D[0..63]
- <5> DDR_A_DM[0..7] → DDR A DM[0..7]
- <5> DDR_A_DQS[0..7] → DDR A DQS[0..7]
- <5> DDR_A_MA[0..15] → DDR A MA[0..15]
- <5> DDR_A_DQS[0..7] → DDR A DQS[0..7]



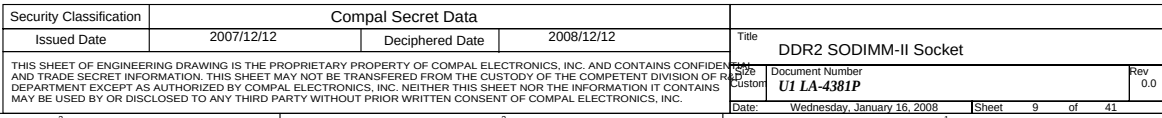
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

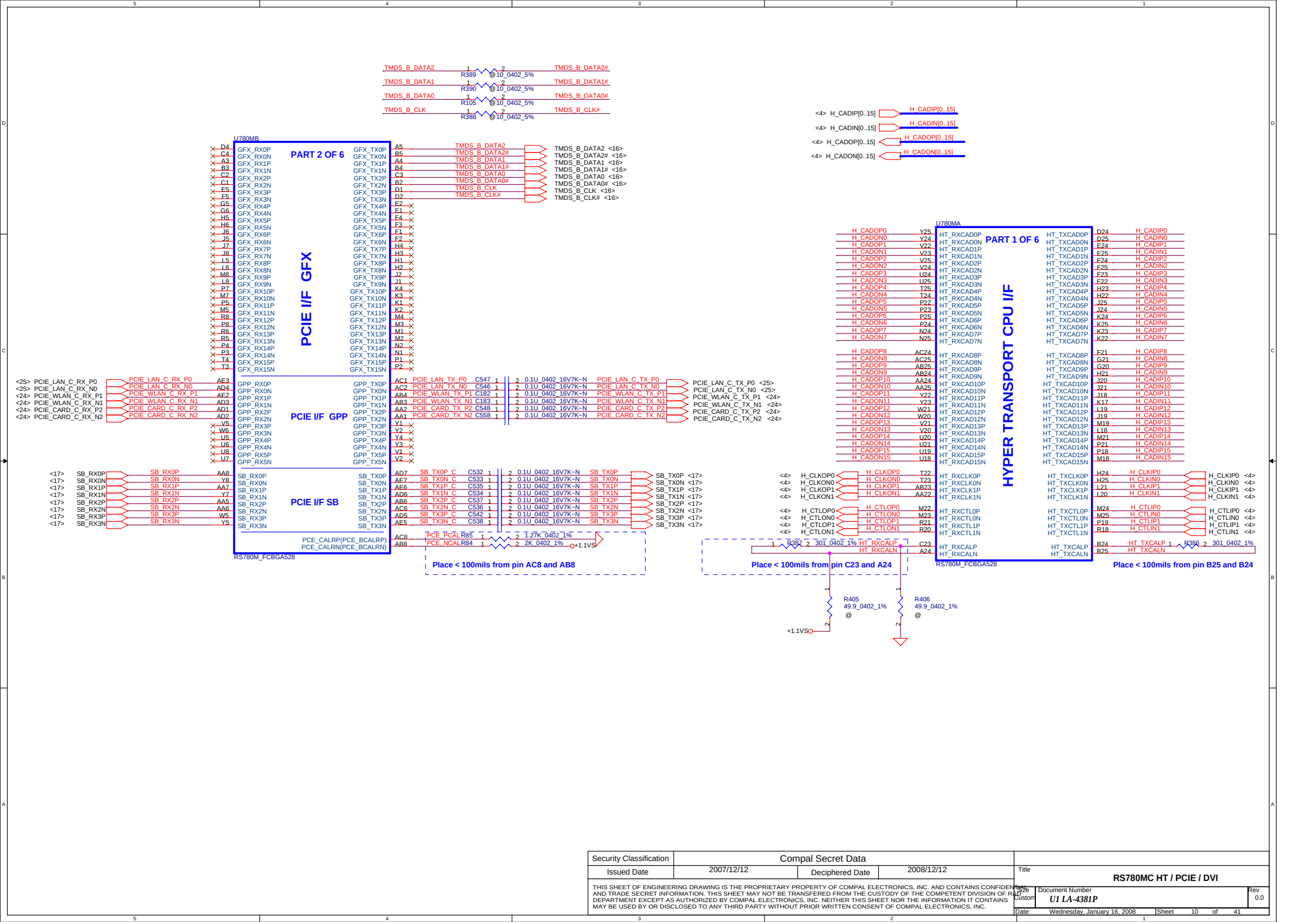
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

PLACE CLOSE TO SO-DIMM1 AS POSSIBLE

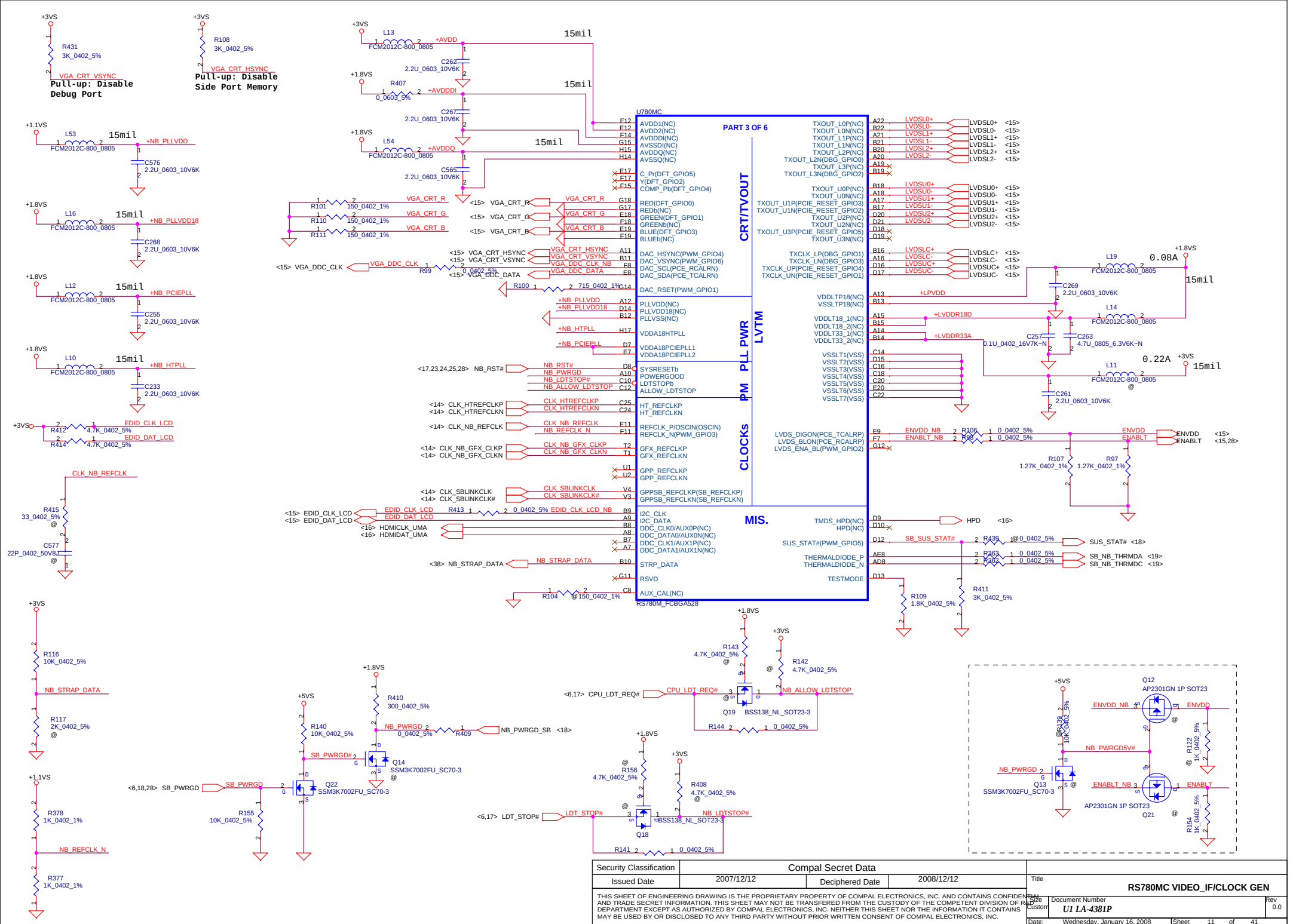


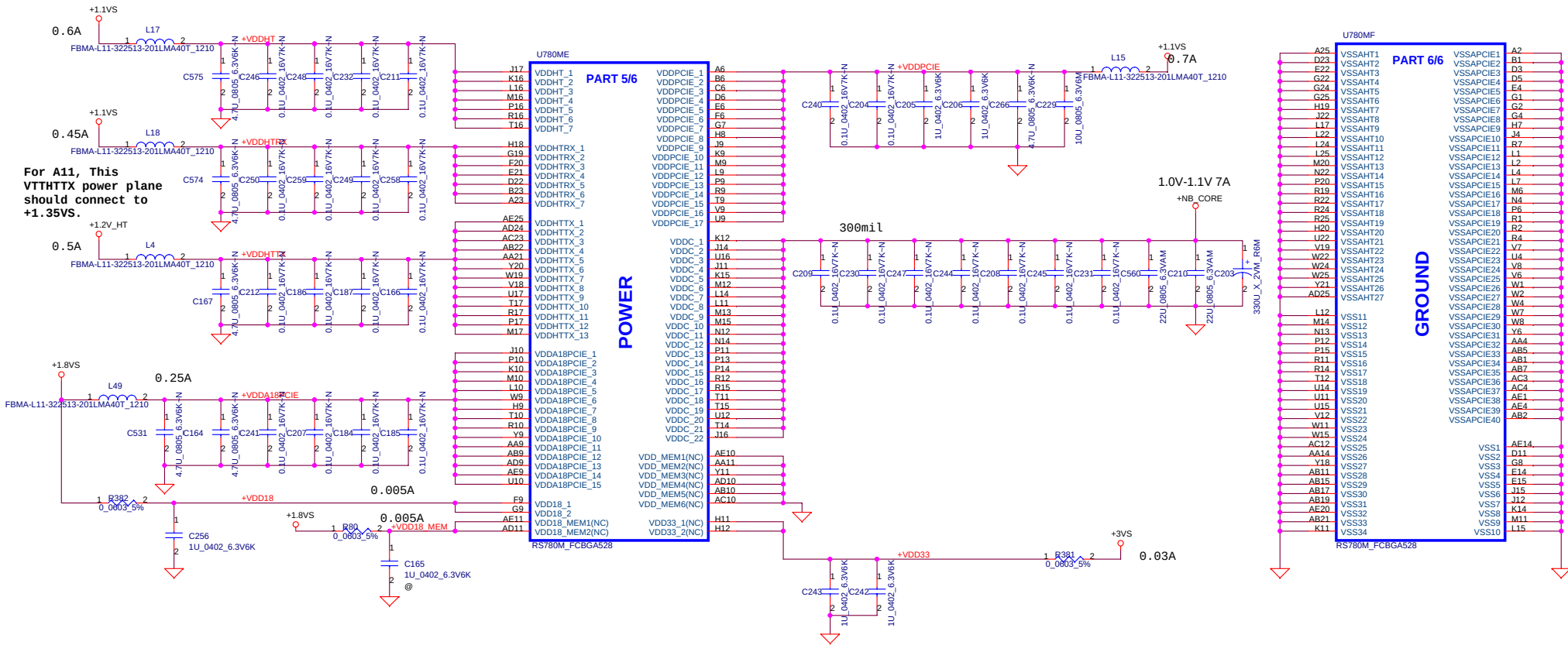
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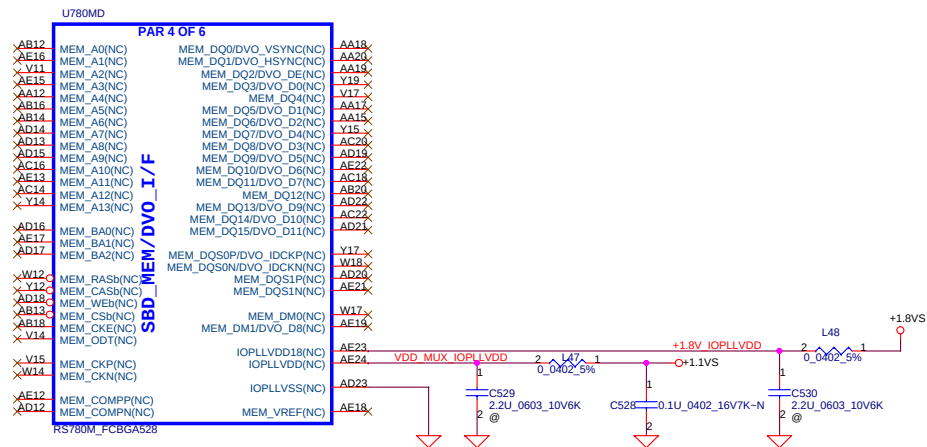
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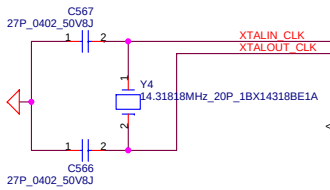
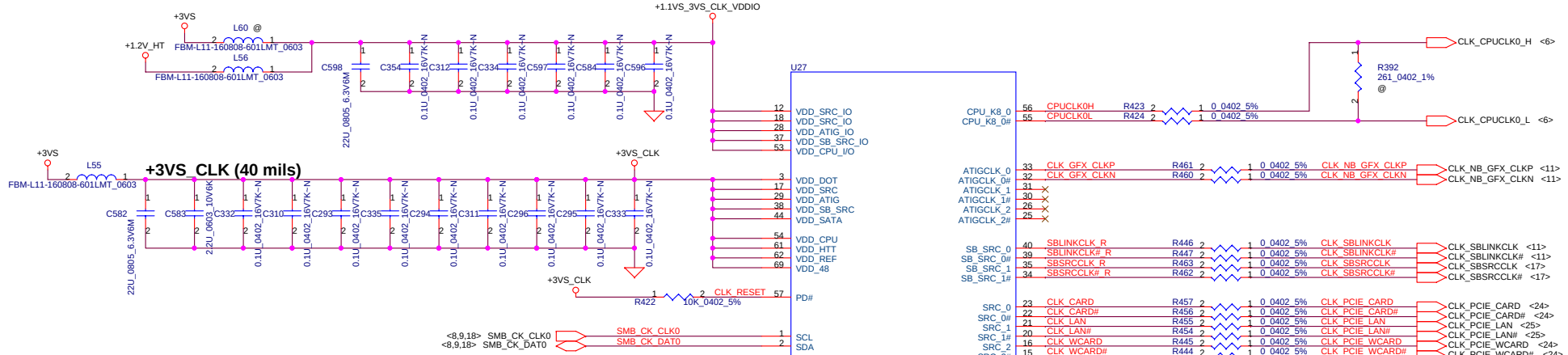
RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDDG18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDLT18	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLT18	+1.8V	NC	+1.8V
VDDG33	+3.3V	NC	+3.3V	VDDLT33	+3.3V	NC	NC
IOPLLVD18	+1.8V	NC	+1.8V				



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VDDIO voltage range is 1.05V-3.3V



NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

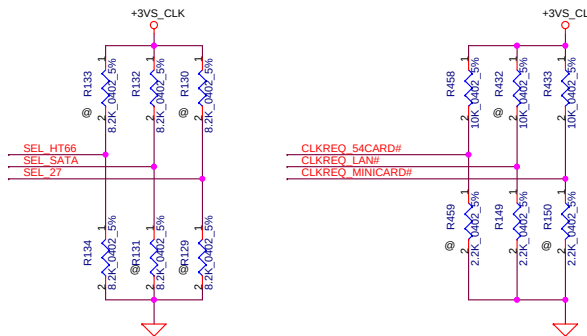
* RS780 can be used as clock buffer to output two PCIe reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.

R40/R41 (value may change)

OSC 14M_NB	
RS740	3.3V 33R serial
RX780	1.8V 33R/43R
RS780	1.1V 200R/100R

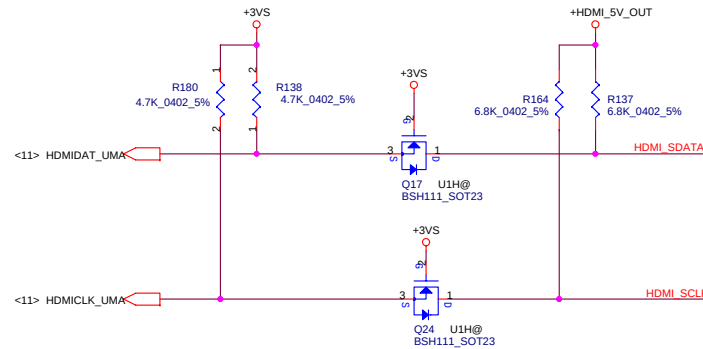
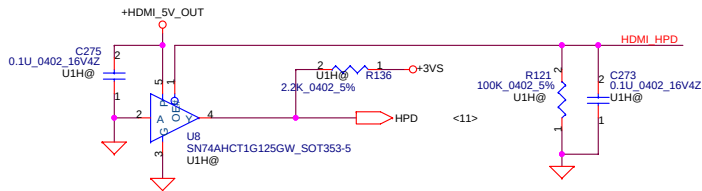
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	Pin 4 / 5 configure as 27M and 27M_SS outputs
	0*	Pin 4 / 5 configure as SRC_7 output

* default

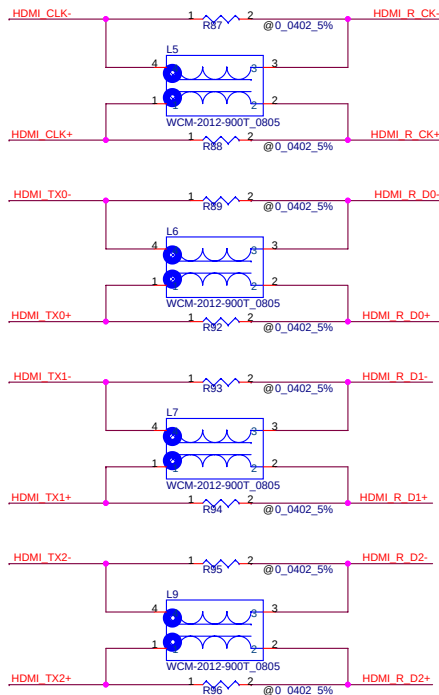


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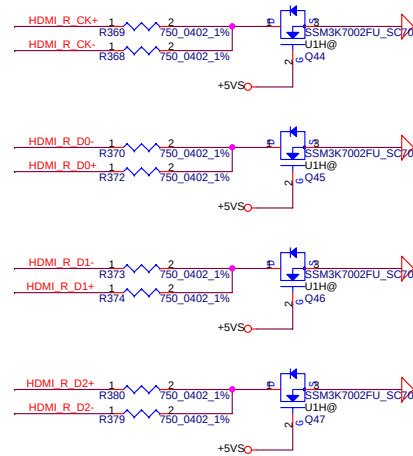
FOR U1H



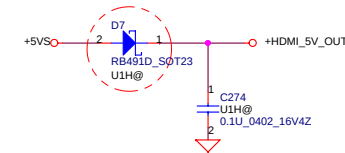
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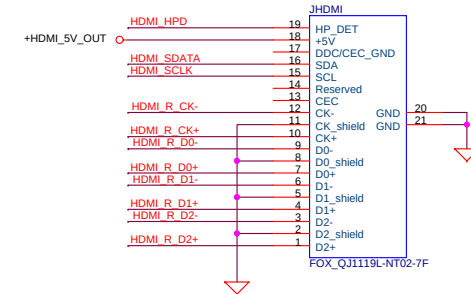
SI:Add Q136 & Q137 for AMD request



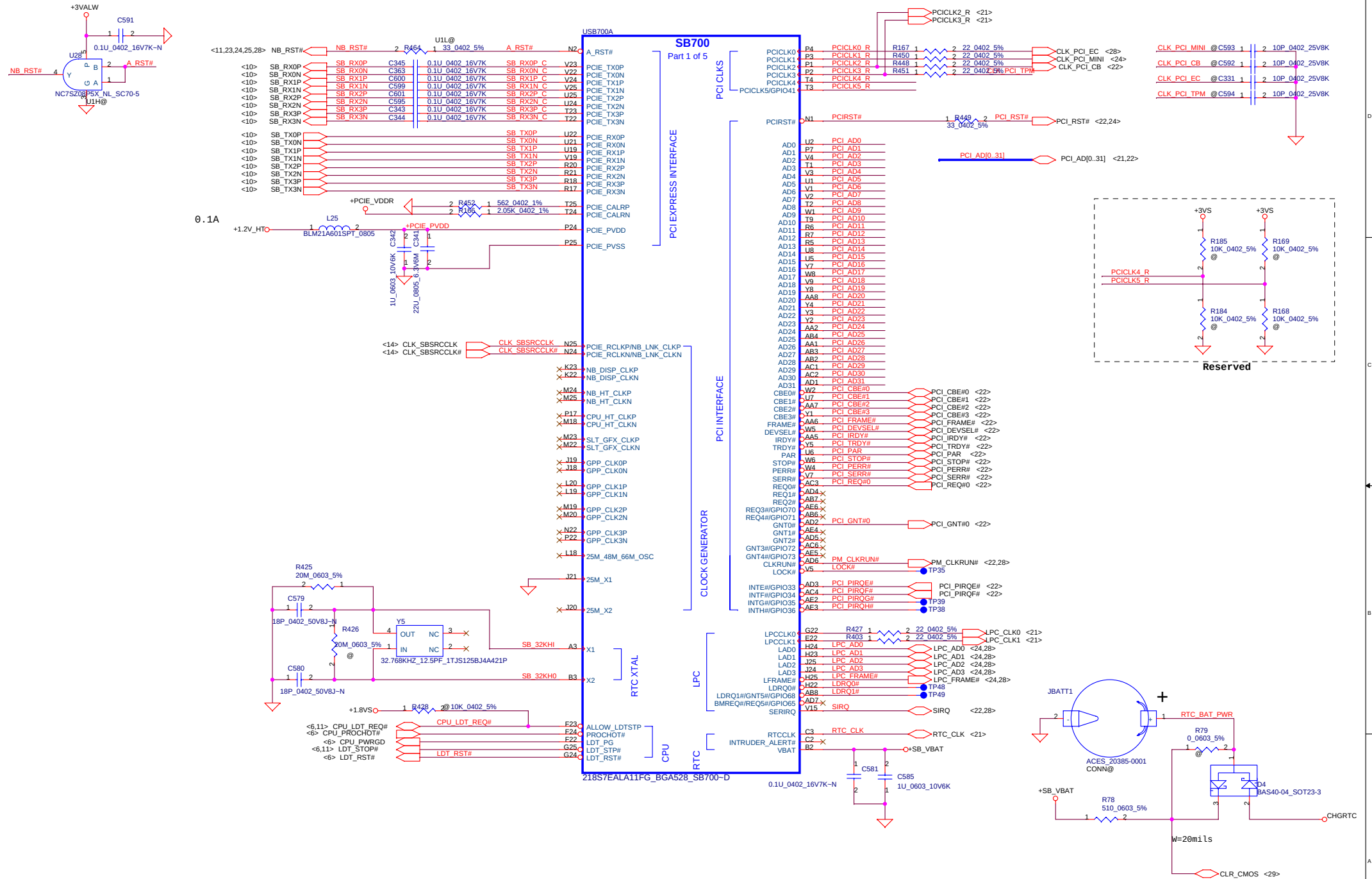
MP:Update D10 to meet HDMI.



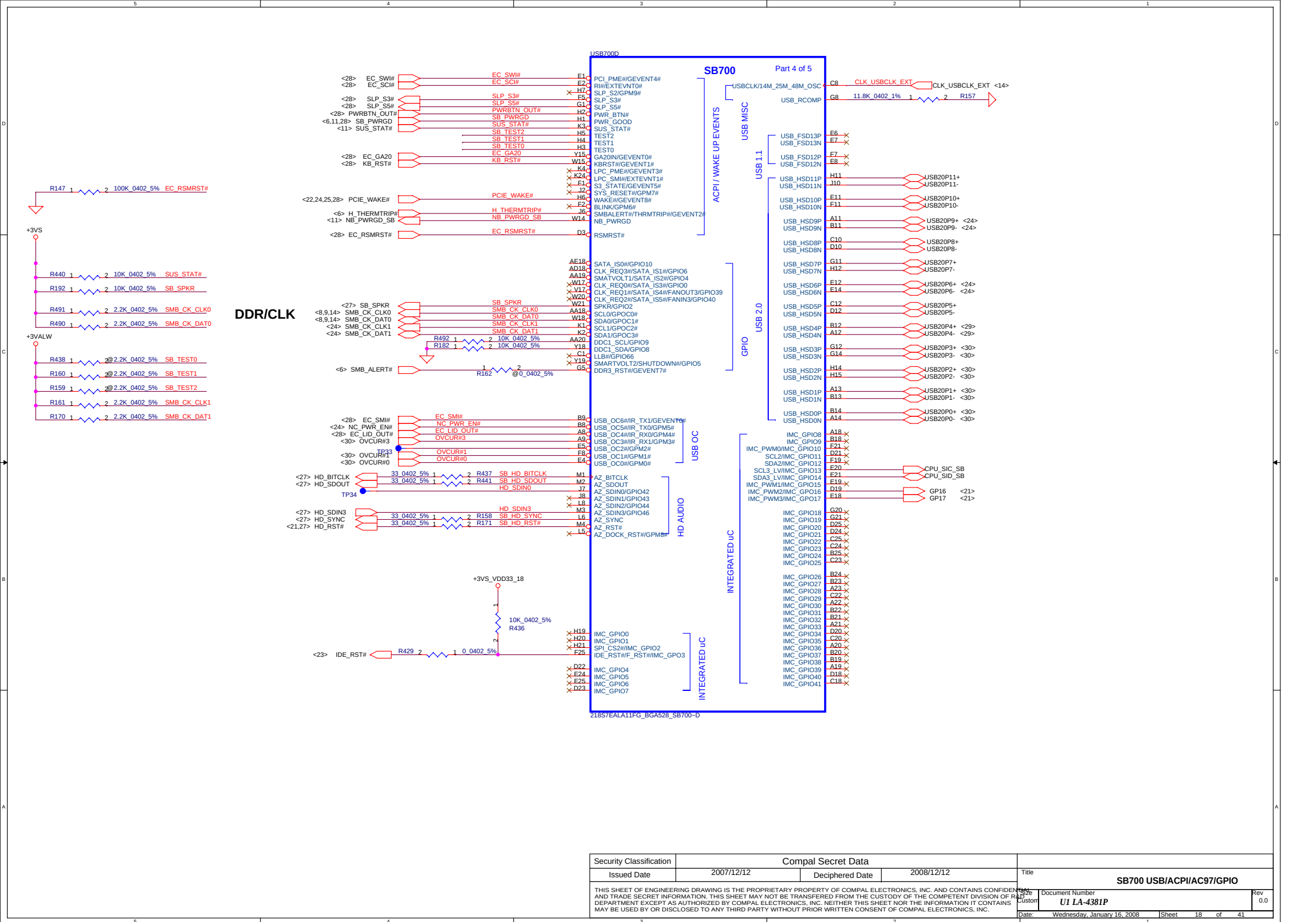
HDMI Connector

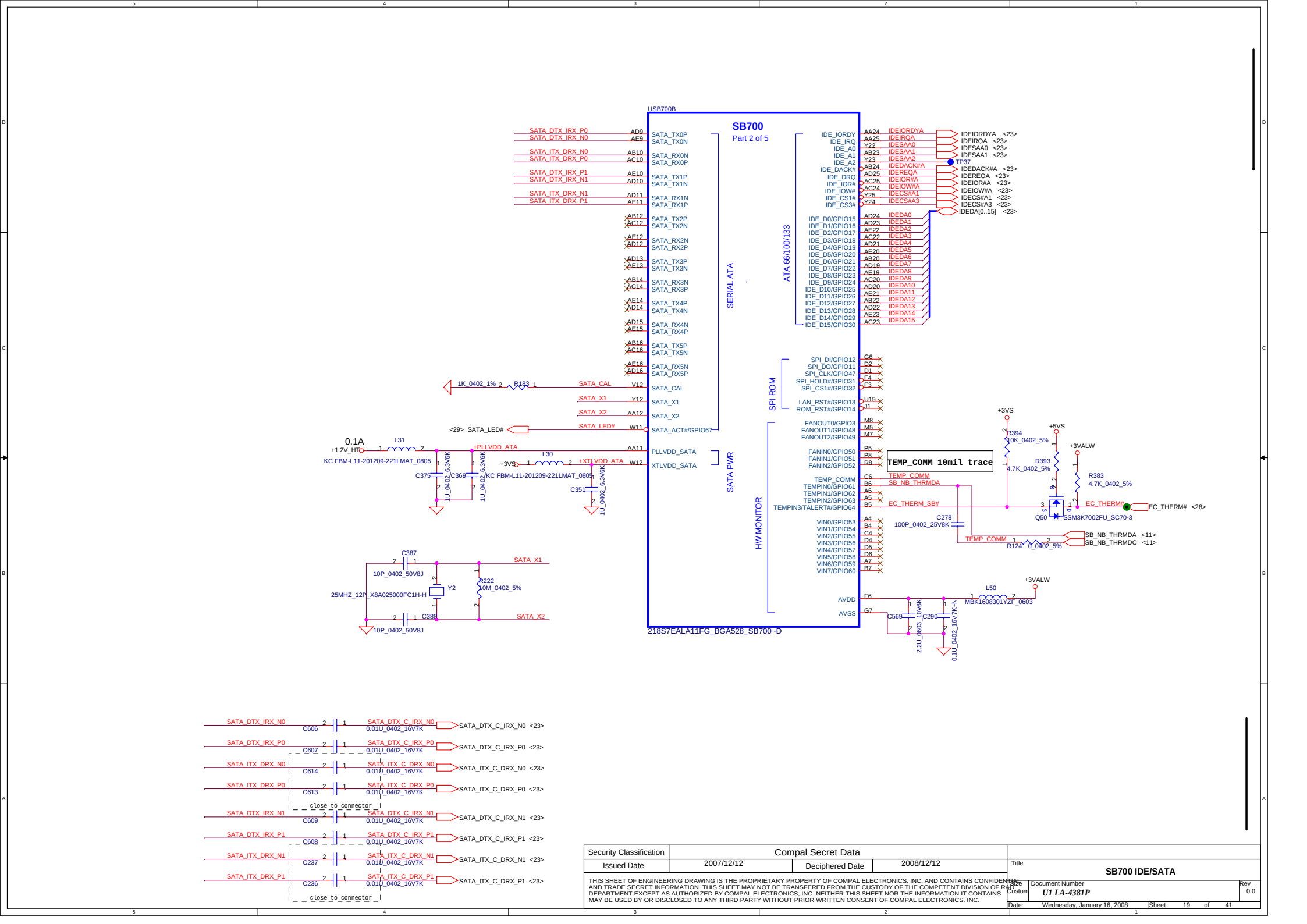


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2007/12/12				2008/12/12				HDMI			
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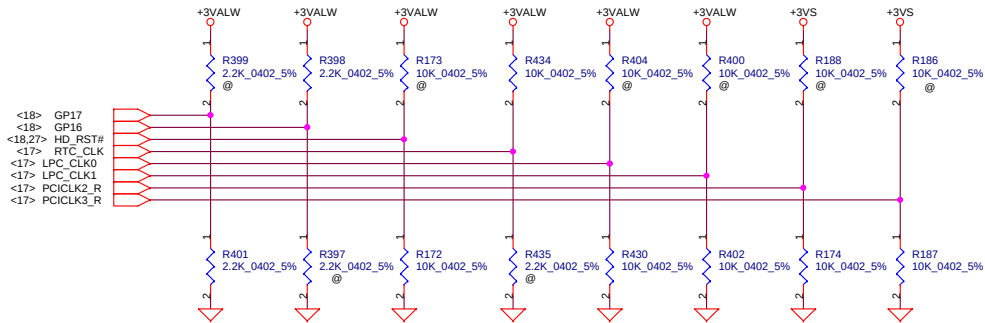


	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	

WITH A12 SB700, STRAP PIN FOR MEM BOOT AND EC ENABLE SWAPED.
I.E. LPC_CLK0 FOR EC ENABLE, AZ_RST# FOR MEM BOOT ENABLE.



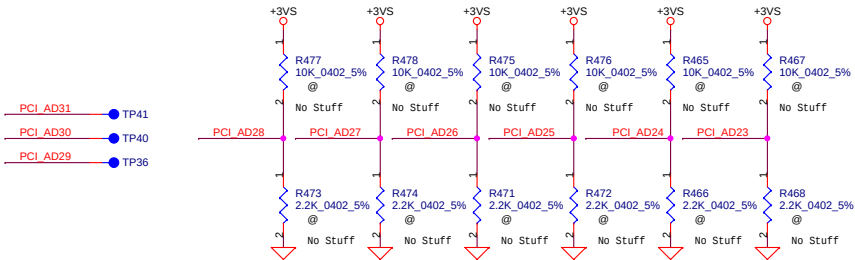
REQUIRED STRAPS



DEBUG STRAPS

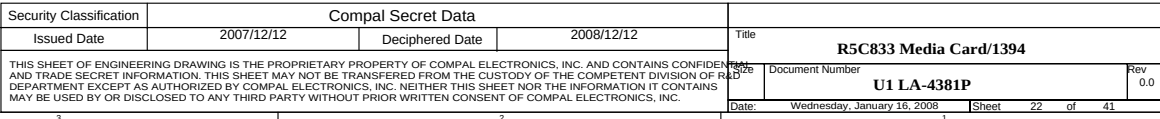
PCI_AD[0..31] PCI_AD[0..31] <17,22>

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



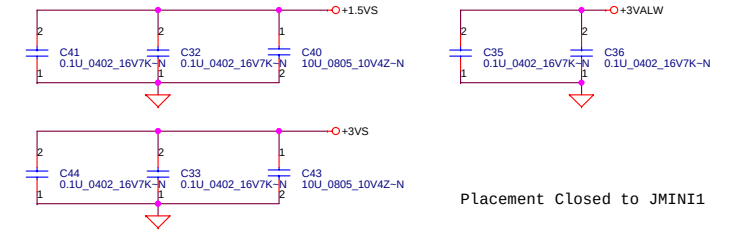
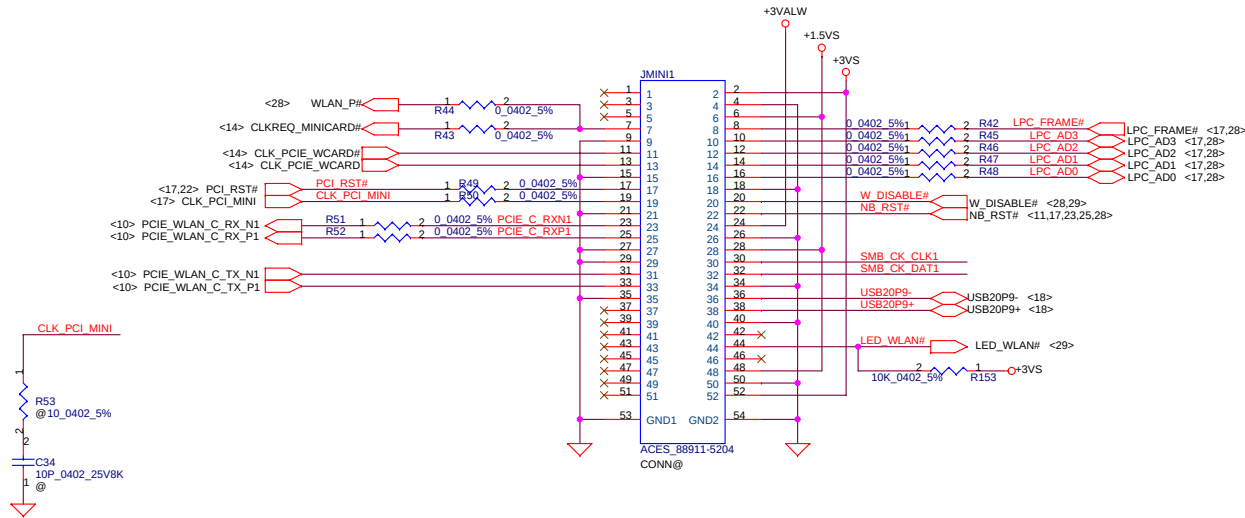
	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	RESERVED	RESERVED	RESERVED	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	RESERVED
PULL LOW				USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

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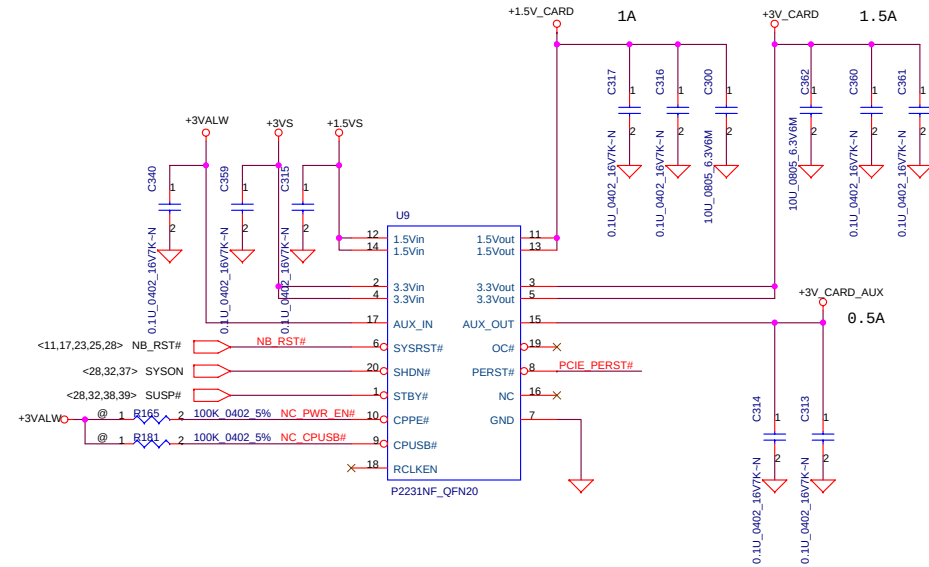
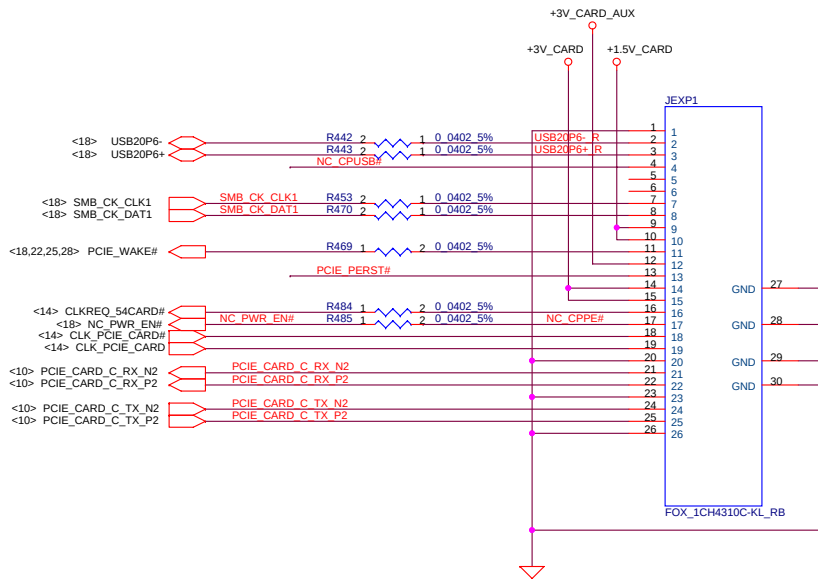


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				Part Number	Document Number	Rev	
				CustID	U1 LA-4381P	0.0	
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Mini-Express Card



New Card

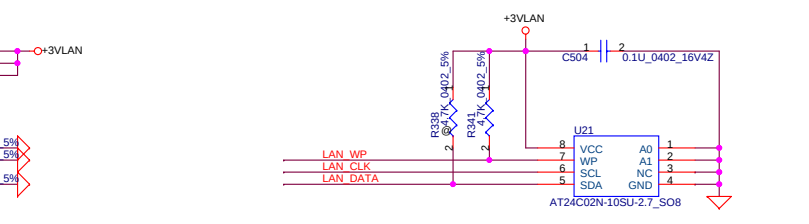
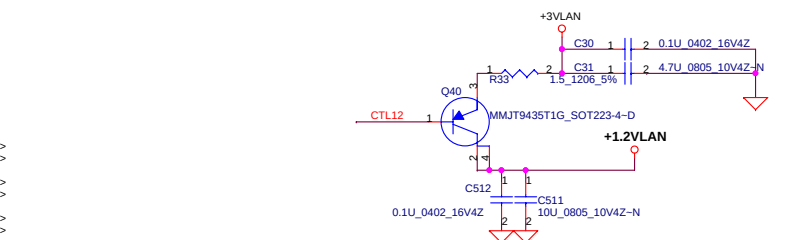
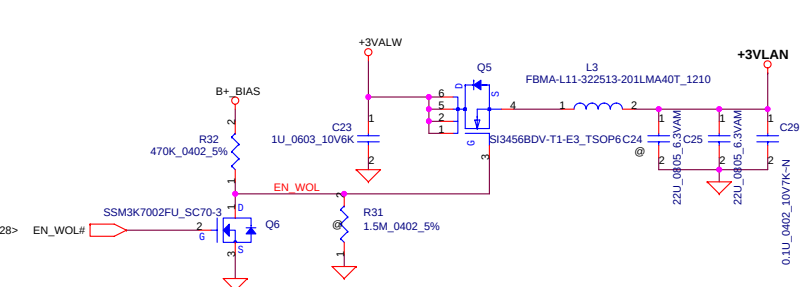
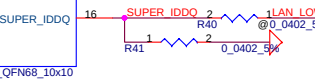
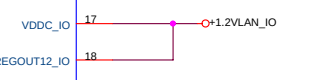
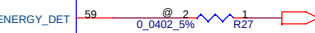
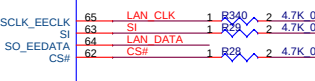
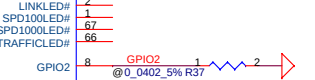
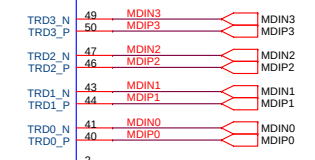
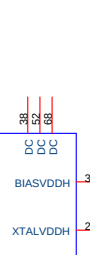
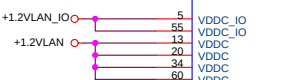
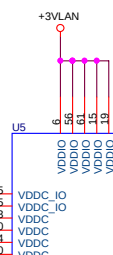
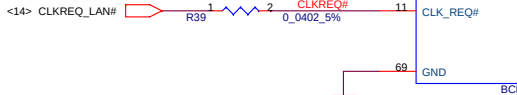
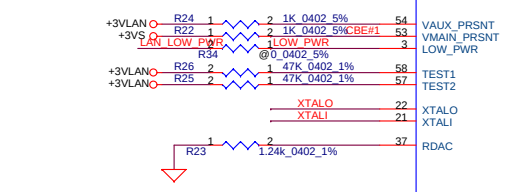
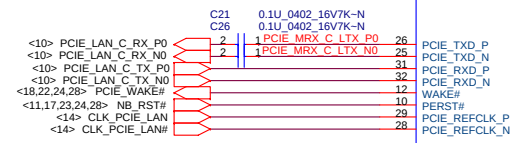
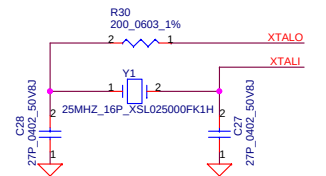
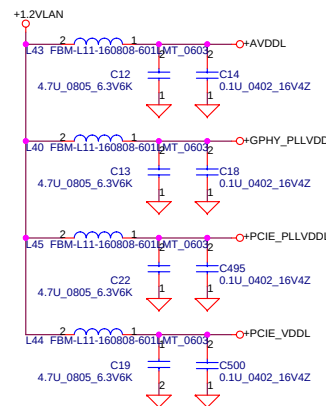
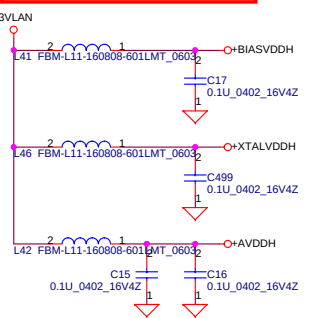
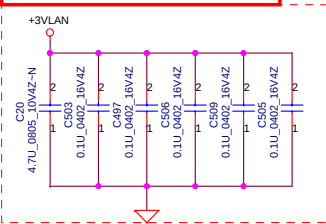
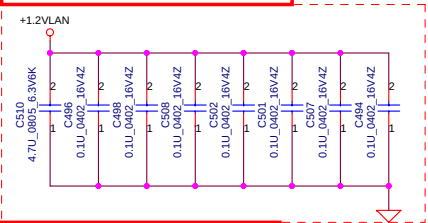


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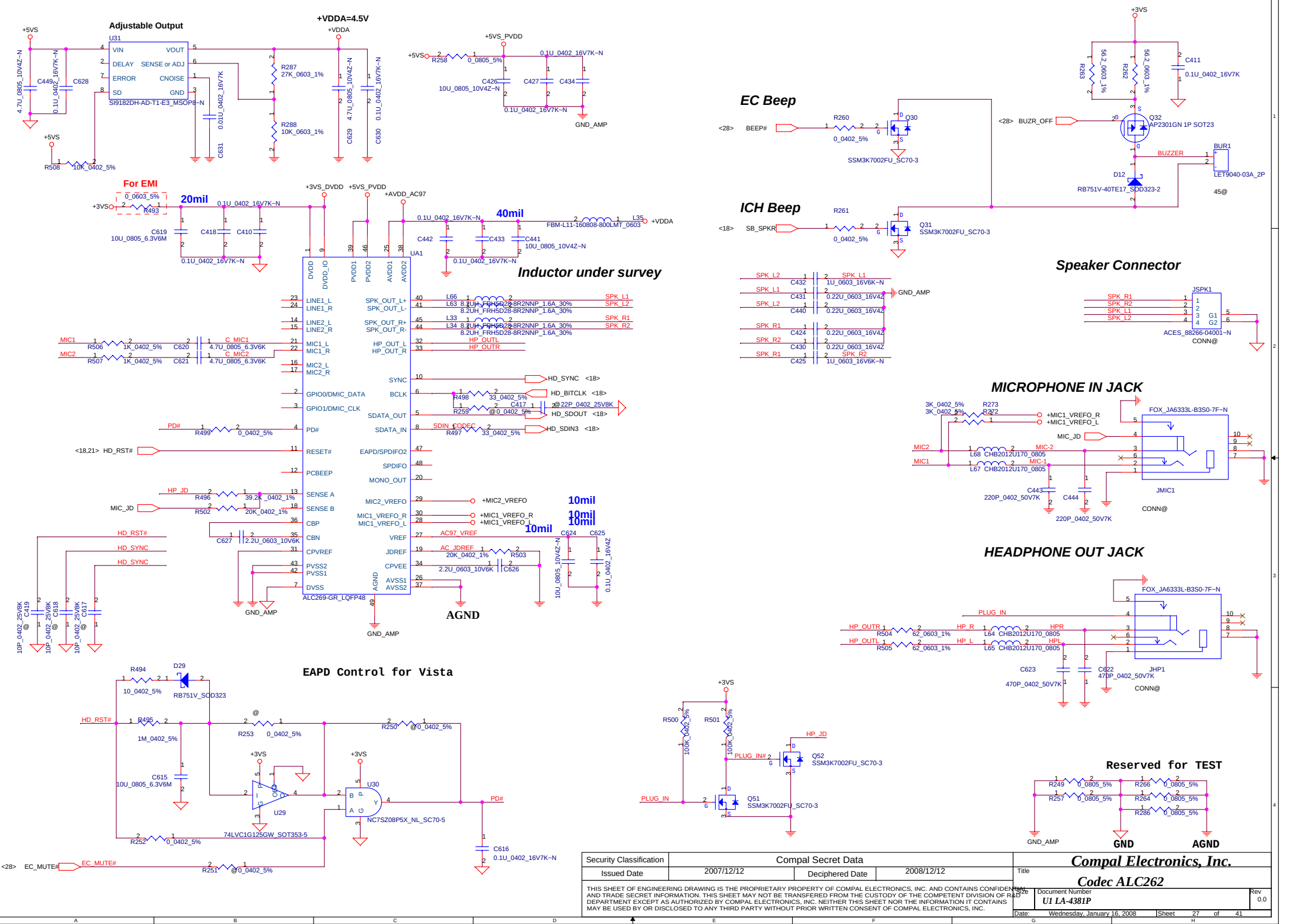
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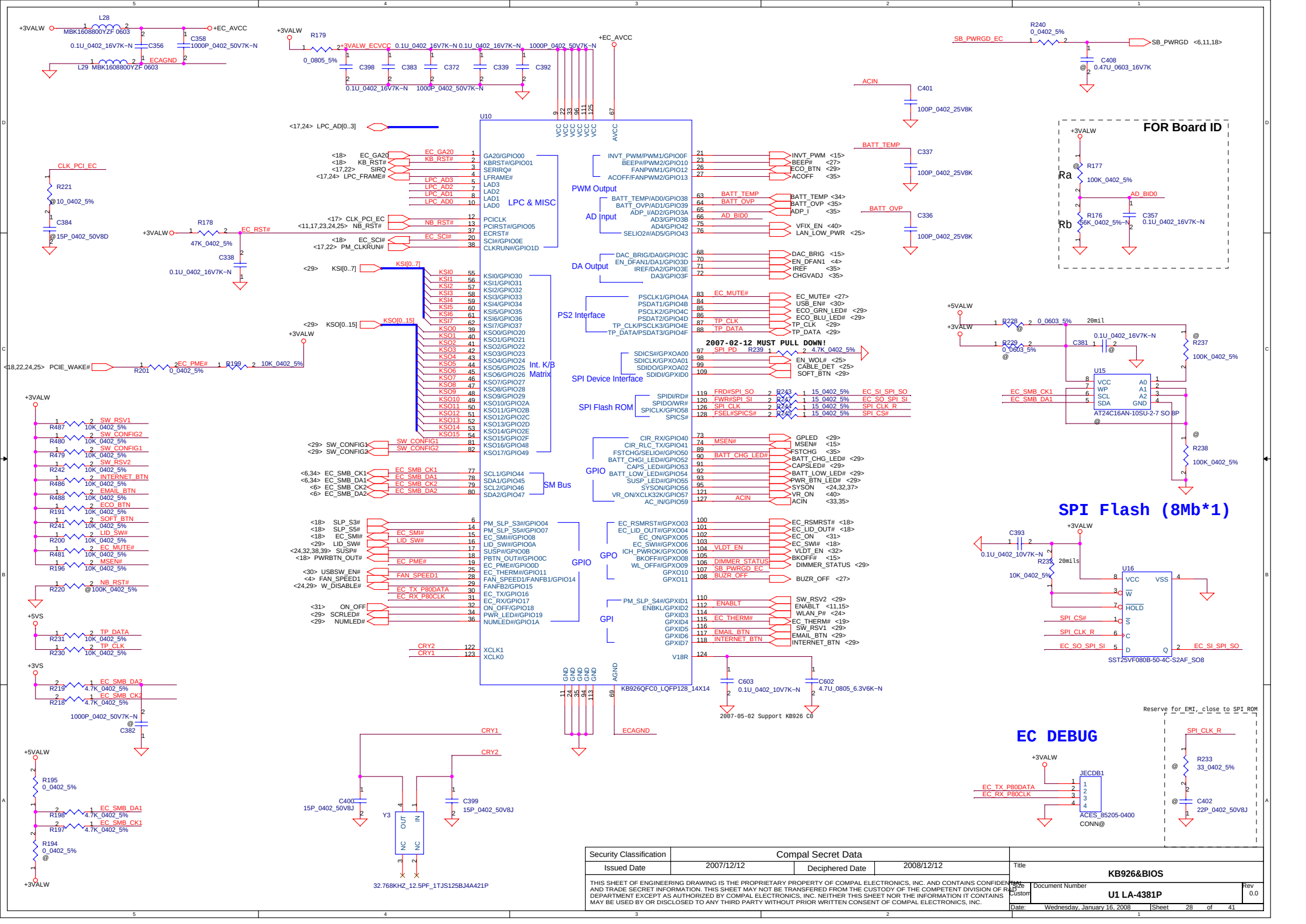
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Layout Notice : Filter place as close chip as possible.

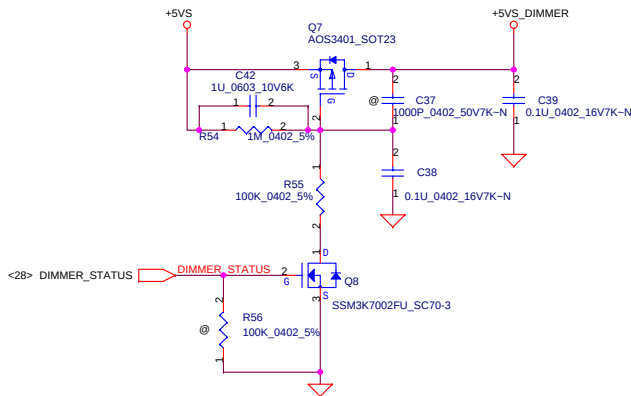
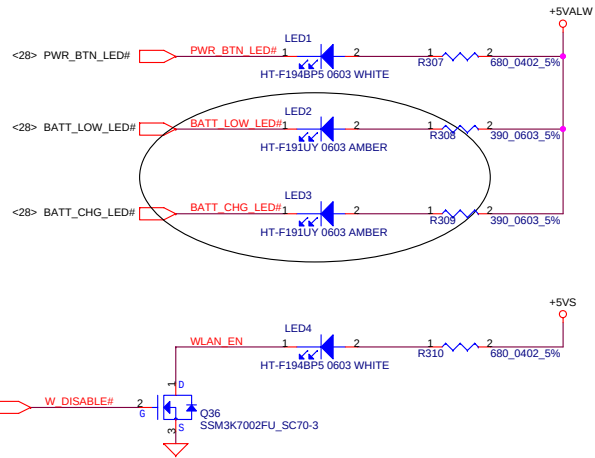
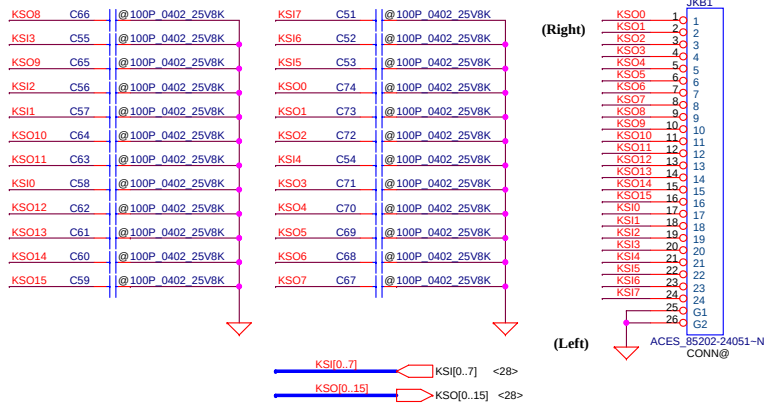


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				Document Number			Rev
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Date:		Wednesday, January 16, 2008		Sheet		25 of 41	

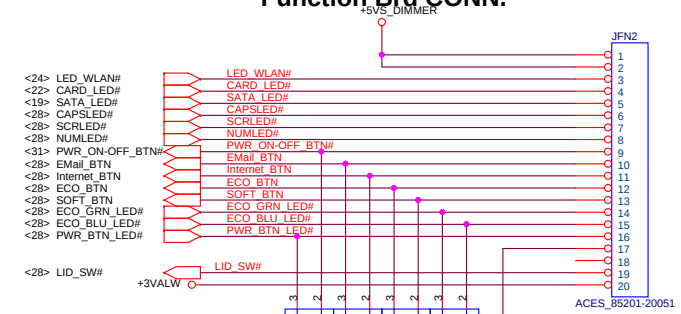




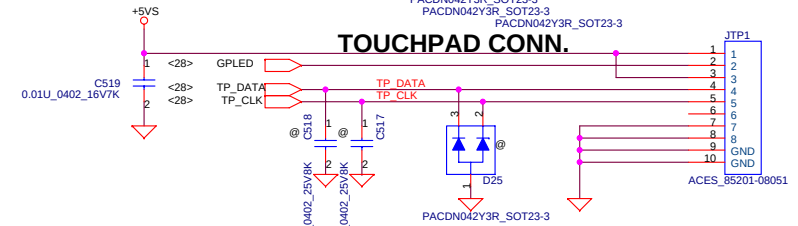
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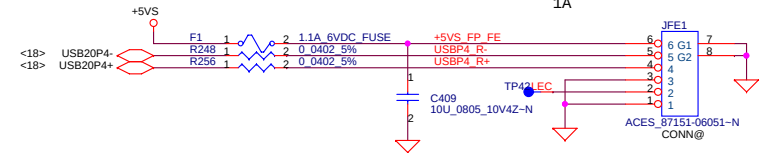
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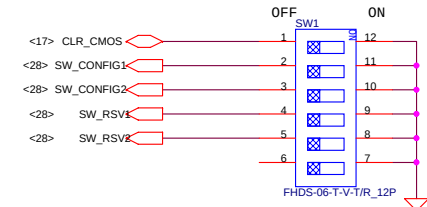
TOUCHPAD CONN.



Felica CONN.

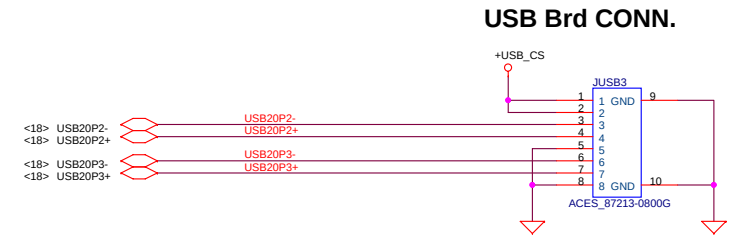
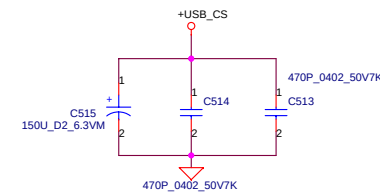
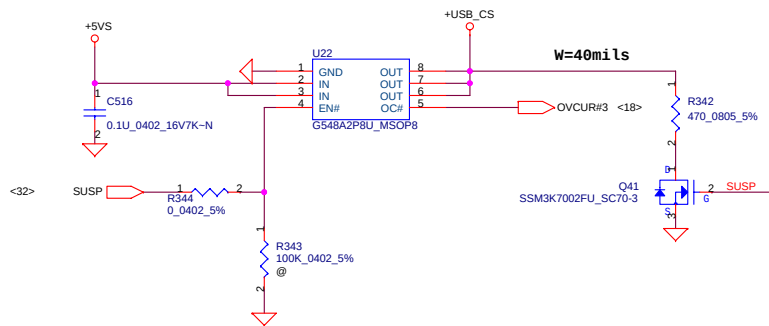
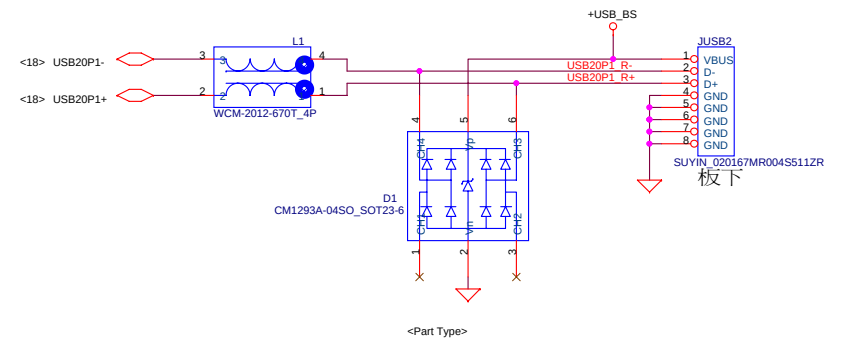
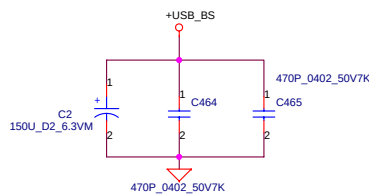
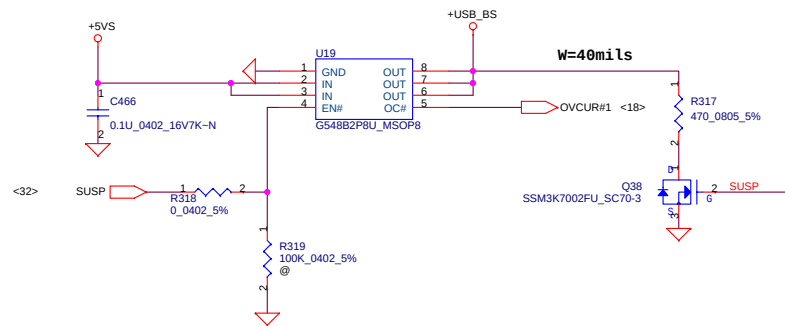
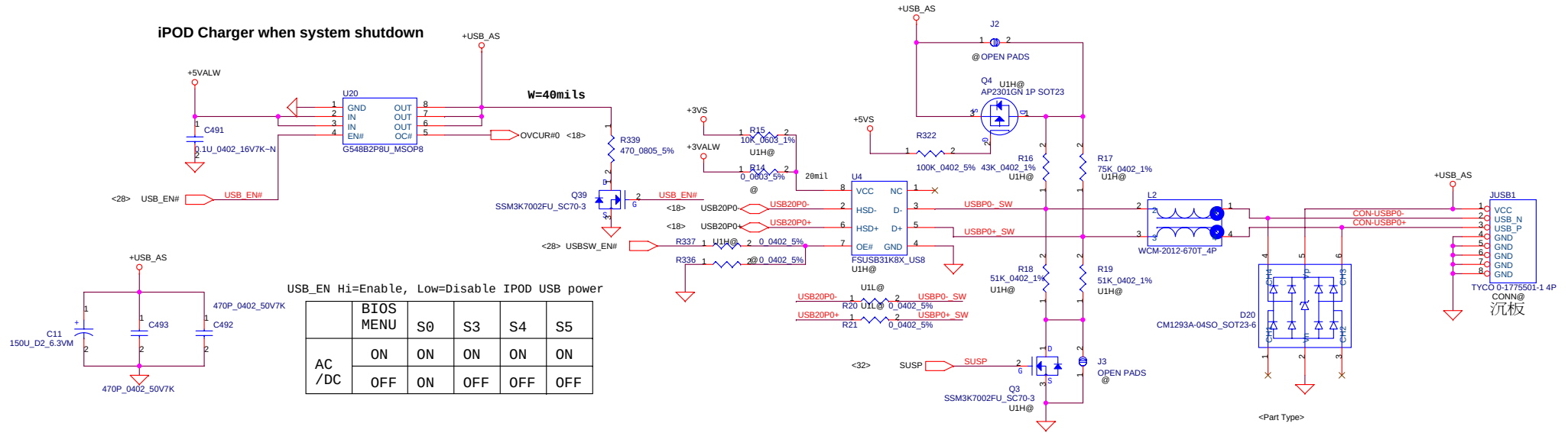


Dip Switch CONN.

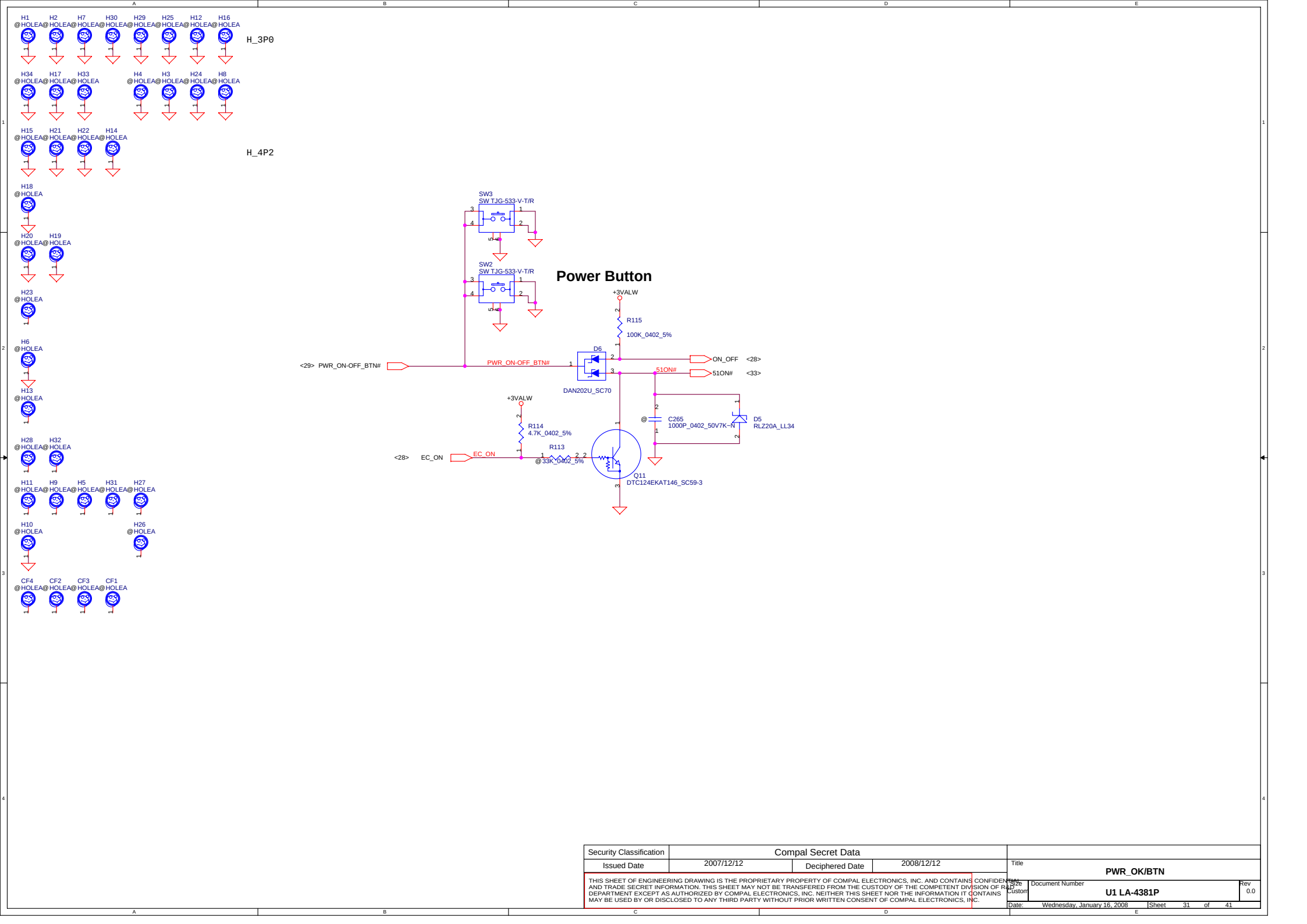


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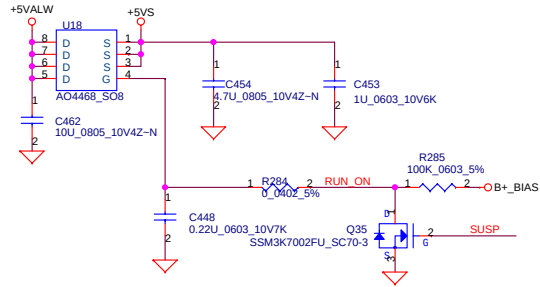
iPOD Charger when system shutdown

**USB Brd CONN.**

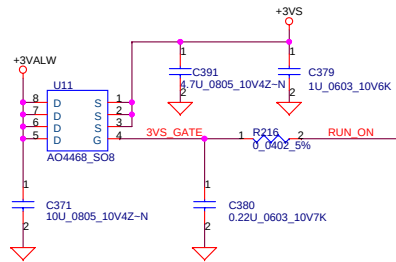
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AC /DC	ON	ON	ON	ON	ON
	OFF	ON	OFF	OFF	OFF



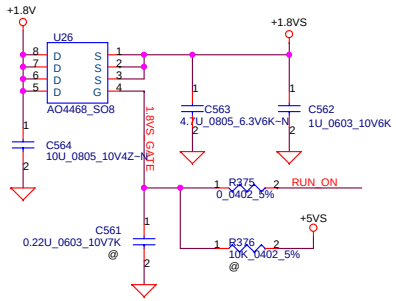
+5VALW TO +5VS



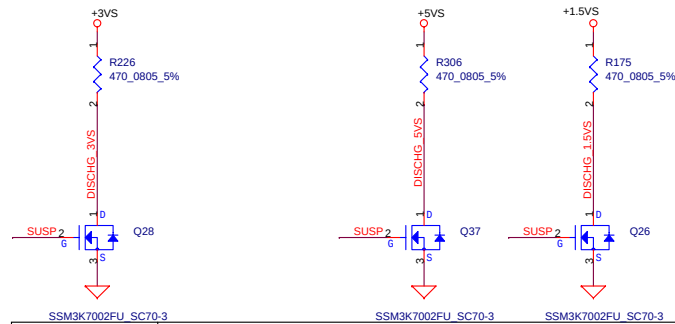
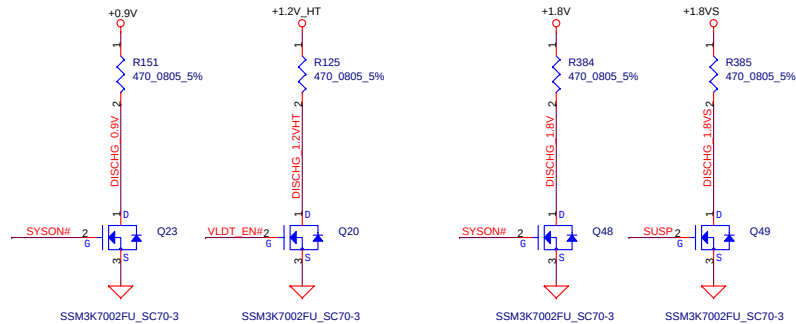
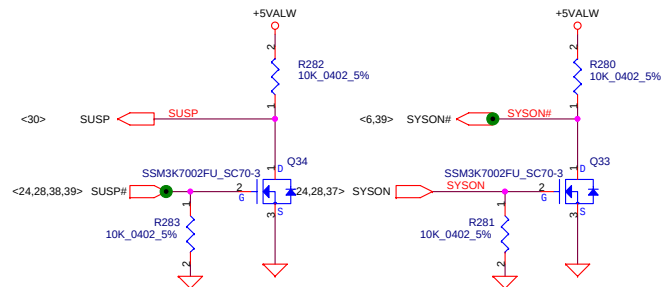
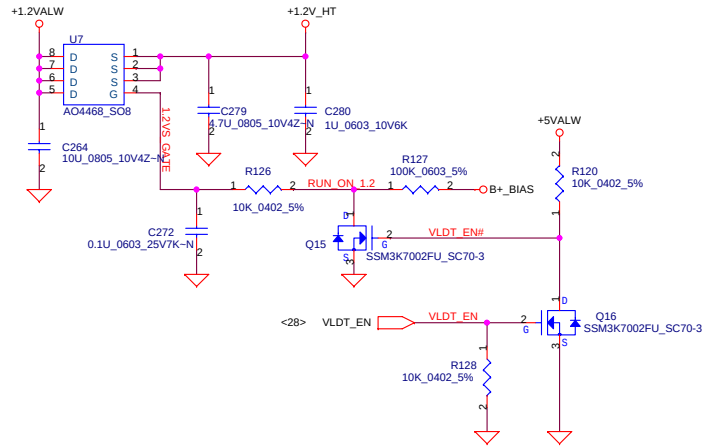
+3VALW TO +3VS



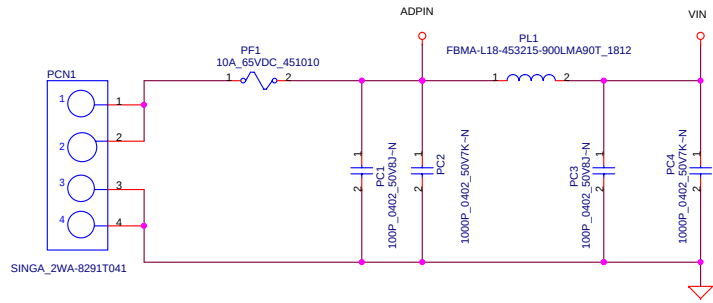
+1.8V TO +1.8VS



+1.2VALW TO +1.2V_HT

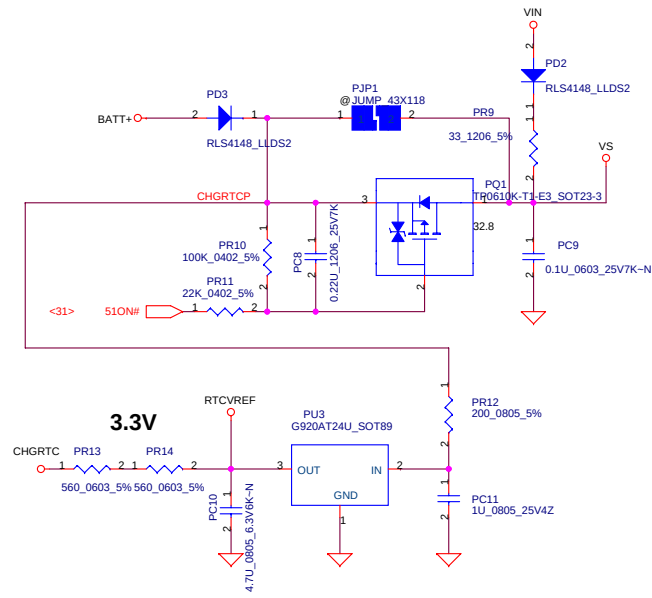
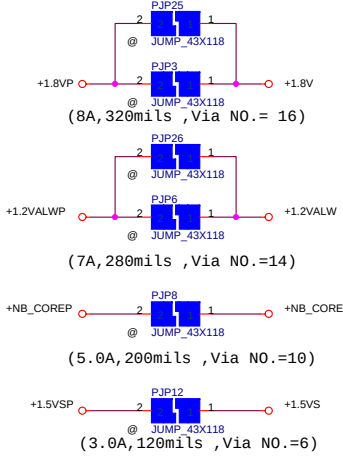
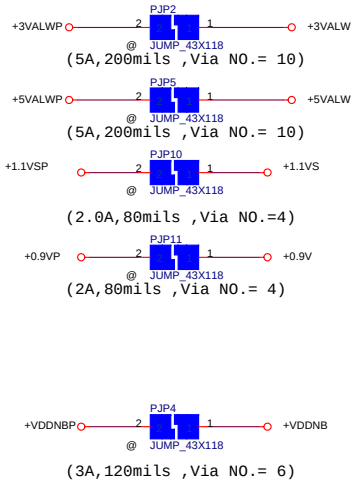
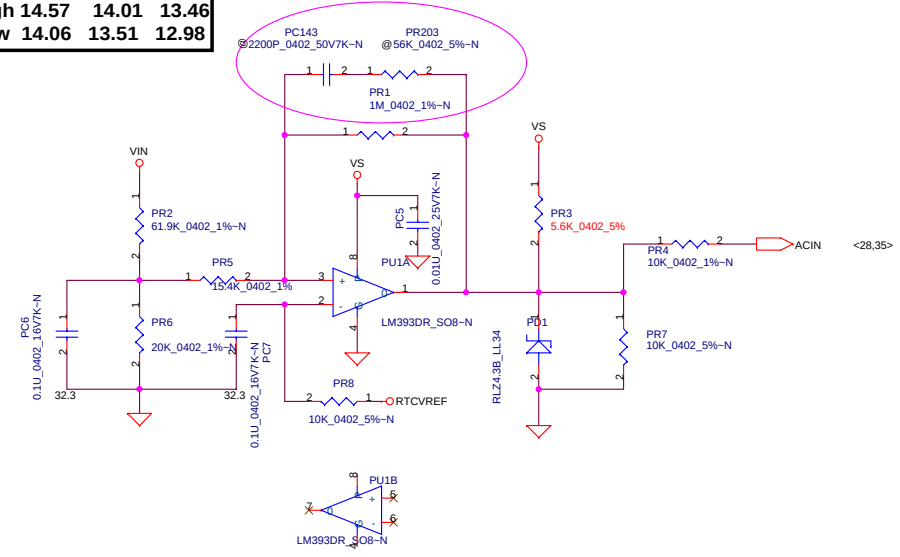


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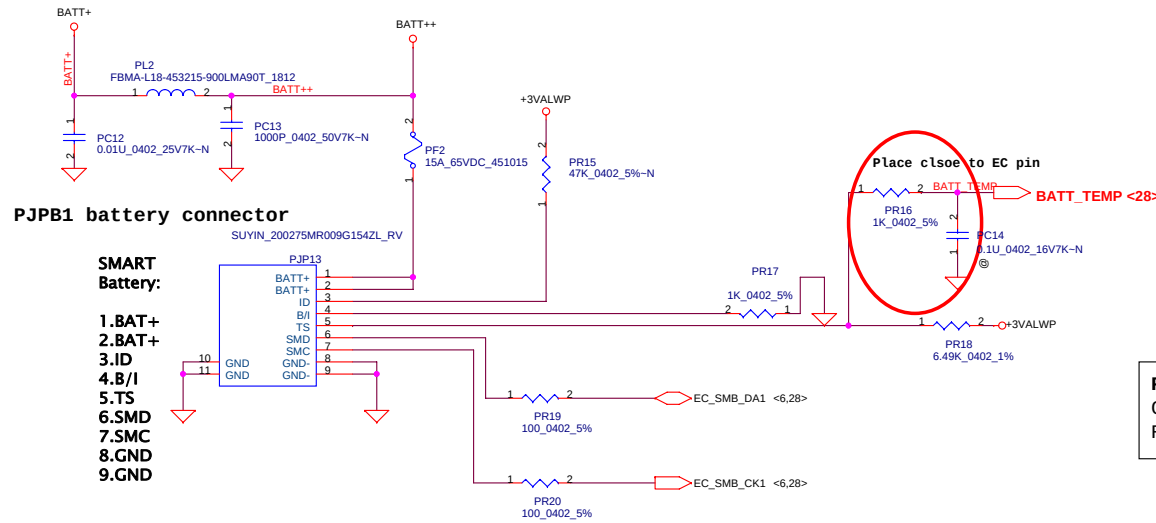


Vin Detector

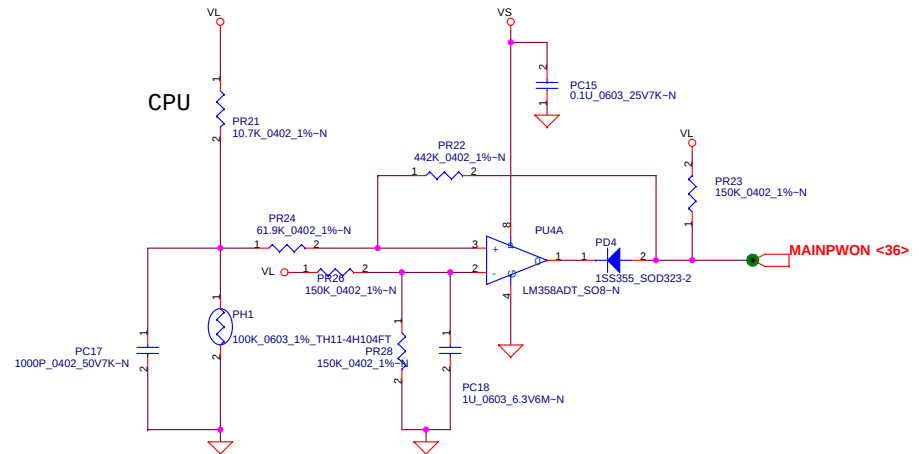
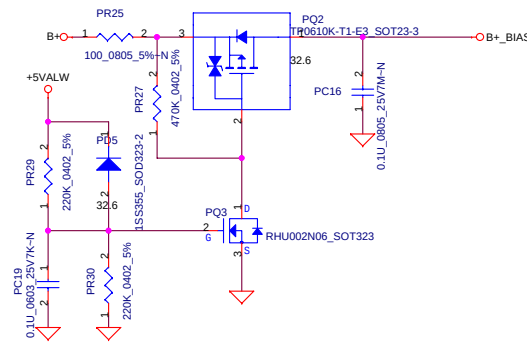
High 14.57 14.01 13.46
Low 14.06 13.51 12.98



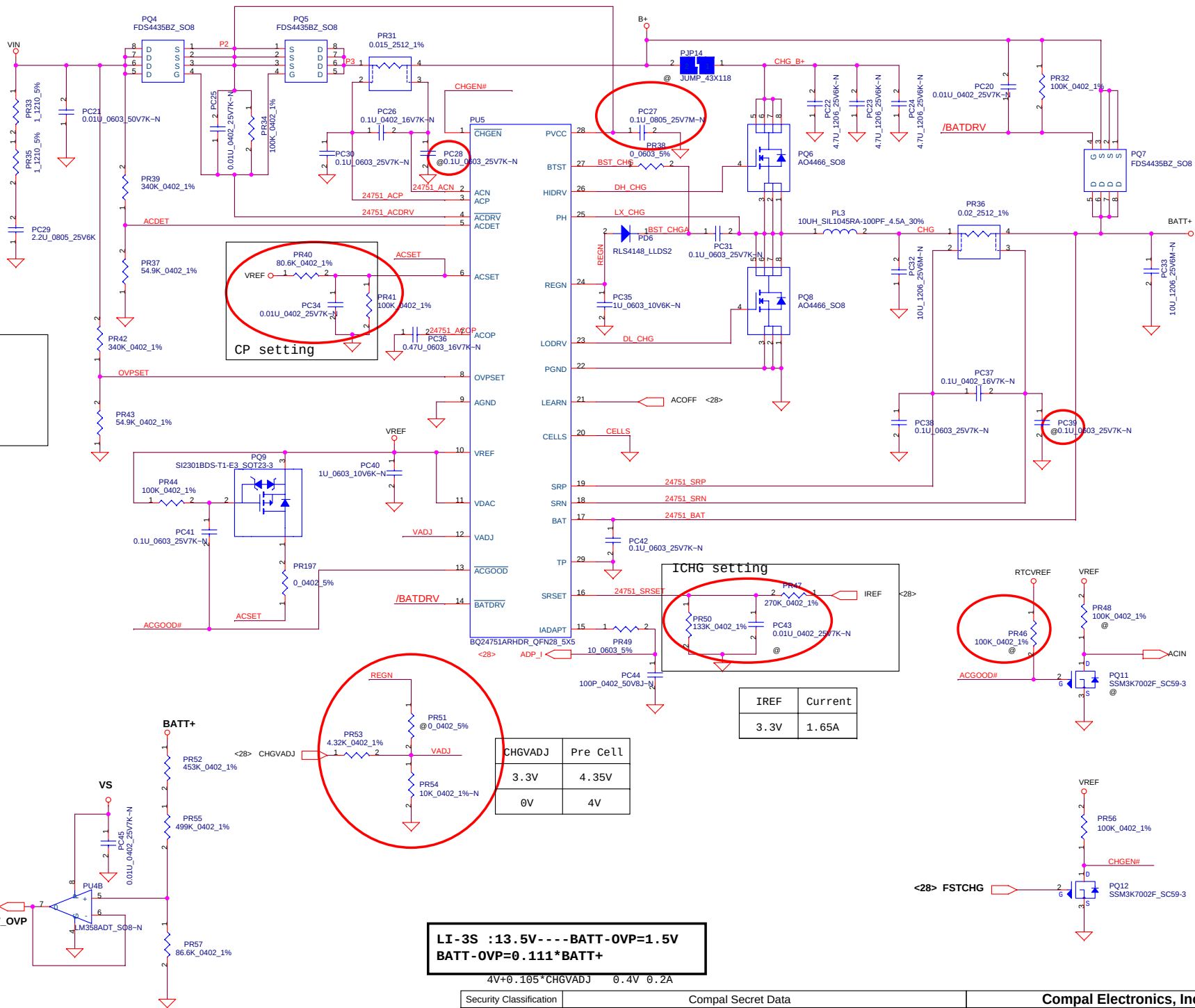
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PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C

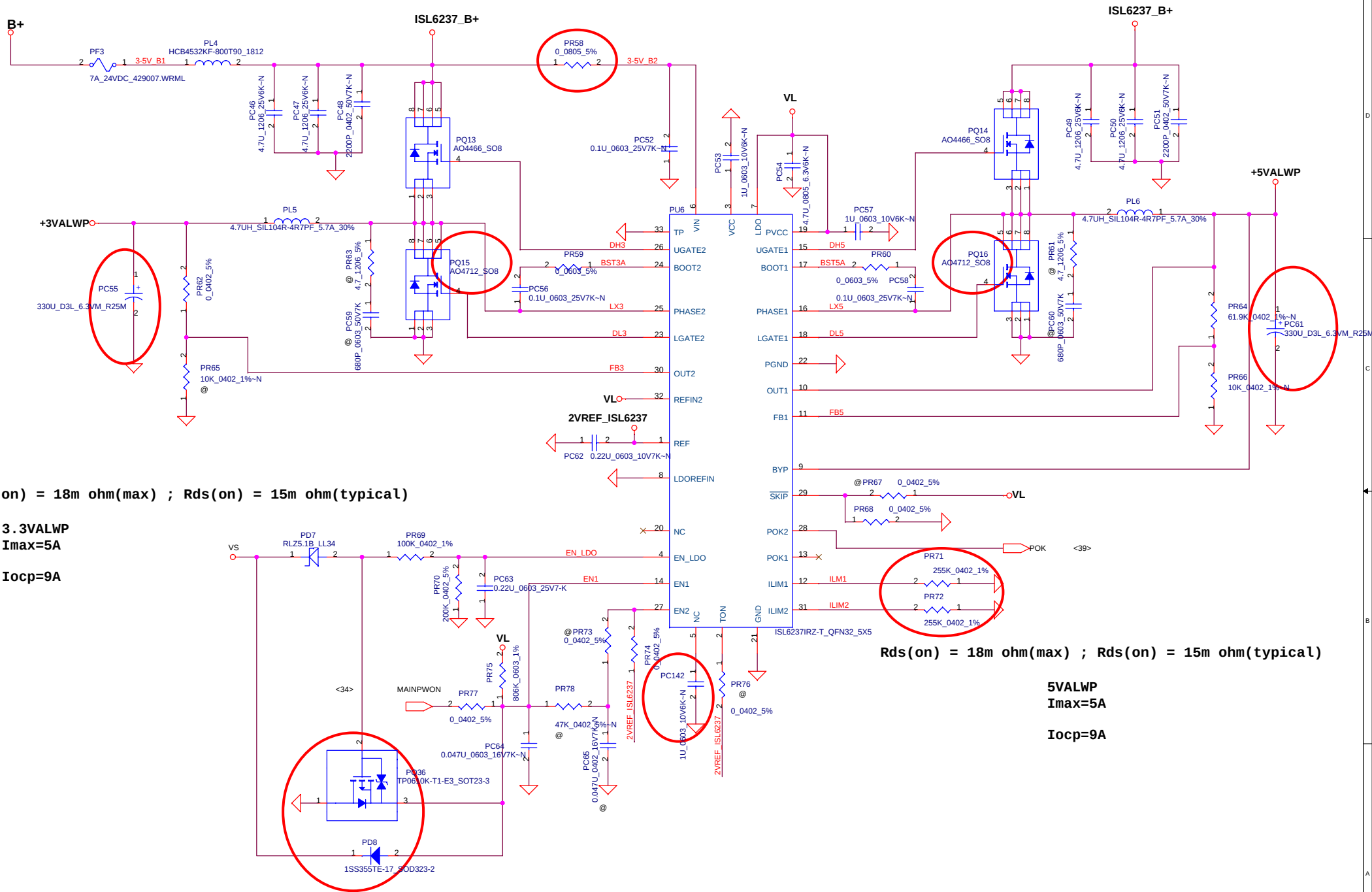


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				Date	Wednesday, January 16, 2008	Sheet	34 of 41

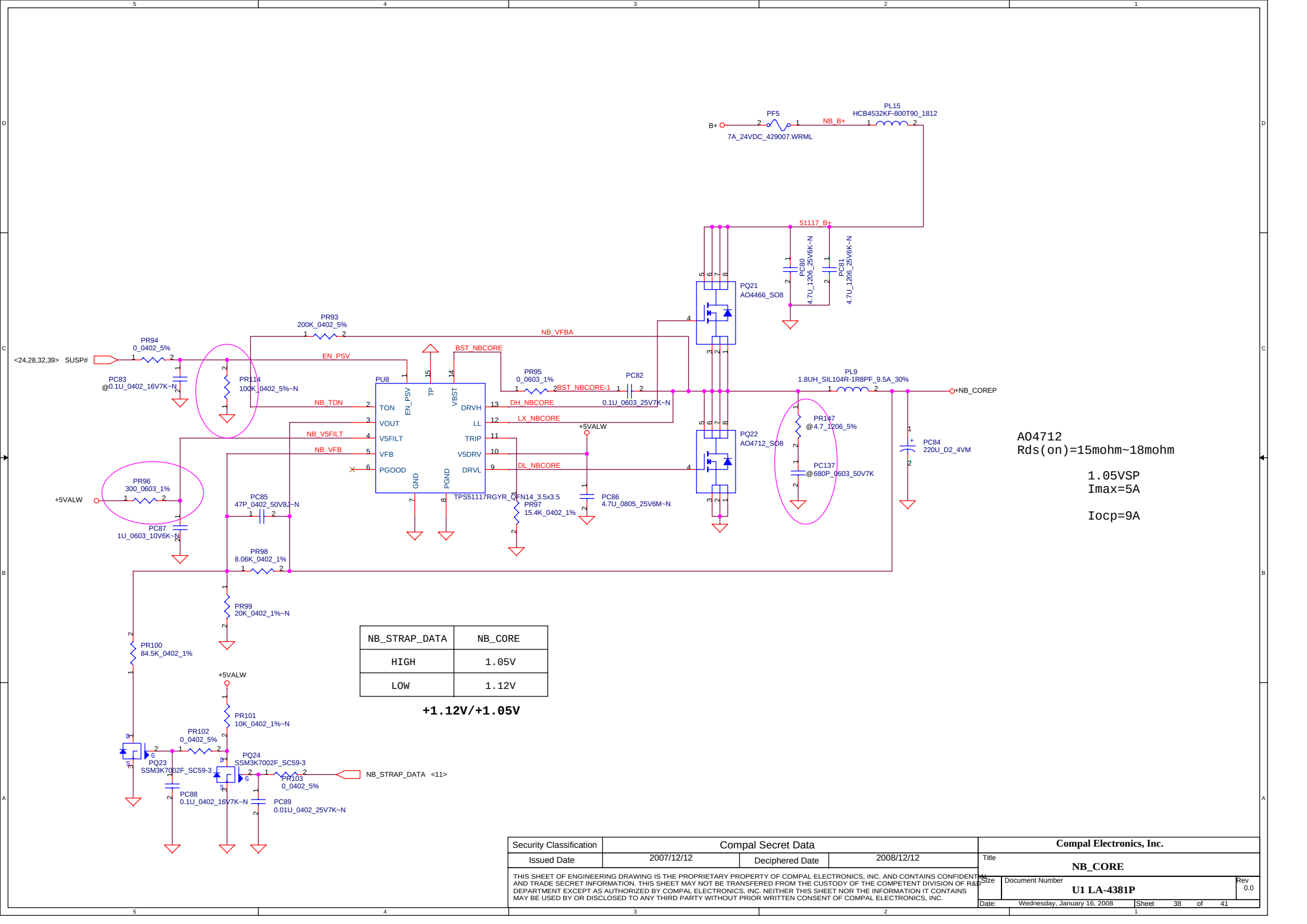


LI-3S :13.5V---BATT-OVP=1.5V
BATT-OVP=0.111*BATT+
4V+0.105*CHGVADJ 0.4V 0.2A

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				Document Number	LA-4381P
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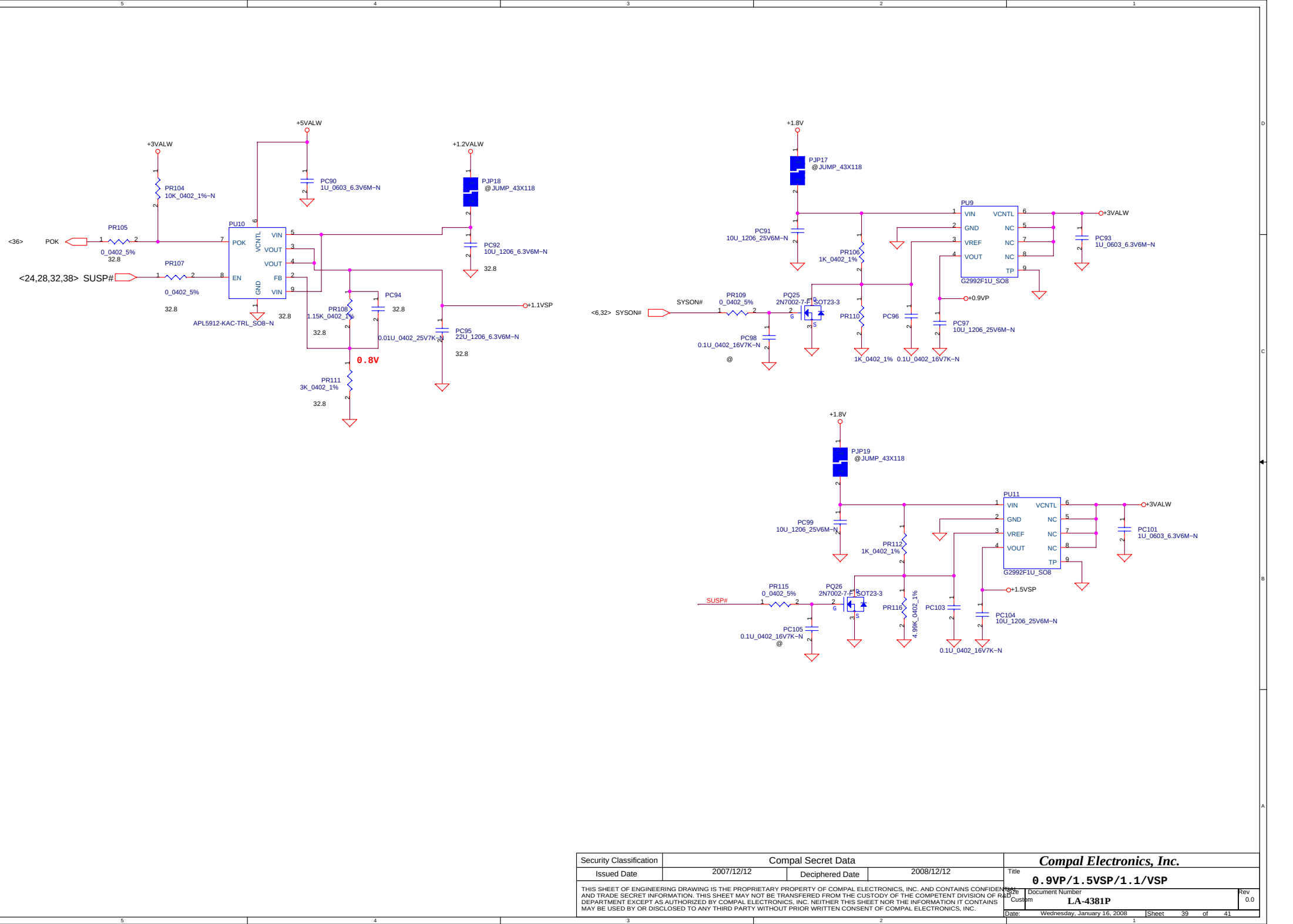
A04712
Rds(on)=15mohm~18mohm

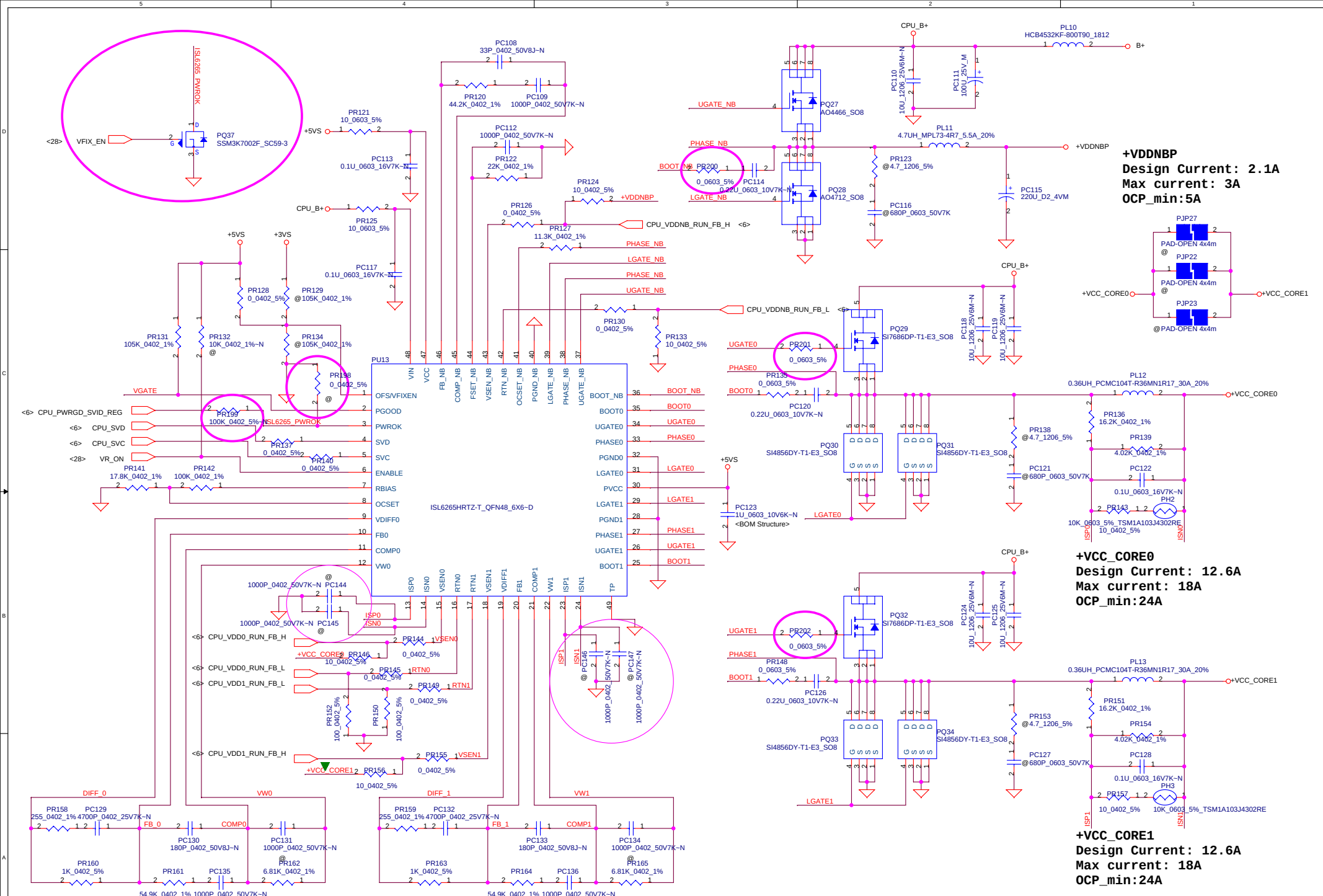
1.05VSP
Imax=5A

Iocp=9A

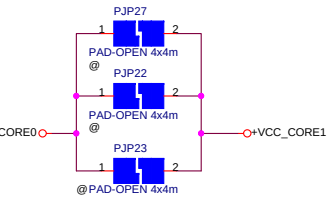
NB_STRAP_DATA	NB_CORE
HIGH	1.05V
LOW	1.12V

+1.12V/+1.05V





+VDDNB
Design Current: 2.1A
Max current: 3A
OCP_min:5A



+VCC_CORE0
Design Current: 12.6A
Max current: 18A
OCP_min:24A

+VCC_CORE1
Design Current: 12.6A
Max current: 18A
OCP_min:24A

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date		2007/12/12	Deciphered Date	2008/12/12		Title
						+CPU_CORE
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P41	+CPU_CORE	08'01/02	Compal	Intersil FAE request.	Add PR200 for B00T_NB.	0.1
2	P37	1.8VP/1.2VALWP	08'01/08	Compal	modify current limit	Change PQ17 PQ18 from A04466 to FDS8884 Change PQ19 PQ20 from A04712 to FDS6690AS	0.1
3	P37	1.8VP/1.2VALWP	08'01/08	Compal	adjust 1.8VP/1.2VALWP OCP set	Change PR88 from 16.5K to 14K Change PR89 from 20.5K to 14K	0.1
4	P38	NB_CORE	08'01/08	Compal	Modify NB_CORE turn off avoised cause force PWM mode	Change PR114 from @0 to 100K	0.1
5	P41	+CPU_CORE	08'01/08	Compal	Modify while S3 mode avoised cause voltage drop	Change PR199 from 0ohm to 100K ADD PQ37	0.1
6	P41	+CPU_CORE	08'01/08	Compal	Modify improve EMI	ADD PR201 PR202	0.1
7	P36	+3VALWP,+5VALWP	08'01/08	Compal	adjust +3VALWP,+5VALWP ocp set	Change PR71 from 330K to 255K Change PR72 from 330K to 255K	0.1
8	P35	Charger	08'01/08	Compal	adjust Charger pre cell set	Change PR53 from 15K to 4.32K	0.1
9	P38	NB_CORE	08'01/08	Compal	TI FAE request.	Change PR96 from 0ohm to 300ohm	0.1

Next: PR238, PC202, PQ56, PD42, PJP21

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Compal Electronics, Inc.	
Title EE-PIR	
Drawing Number U1 LA-4381P	
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