

Compal Confidential

QIWG7 DIS M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

nVIDIA N13P-GL

2011-12-28

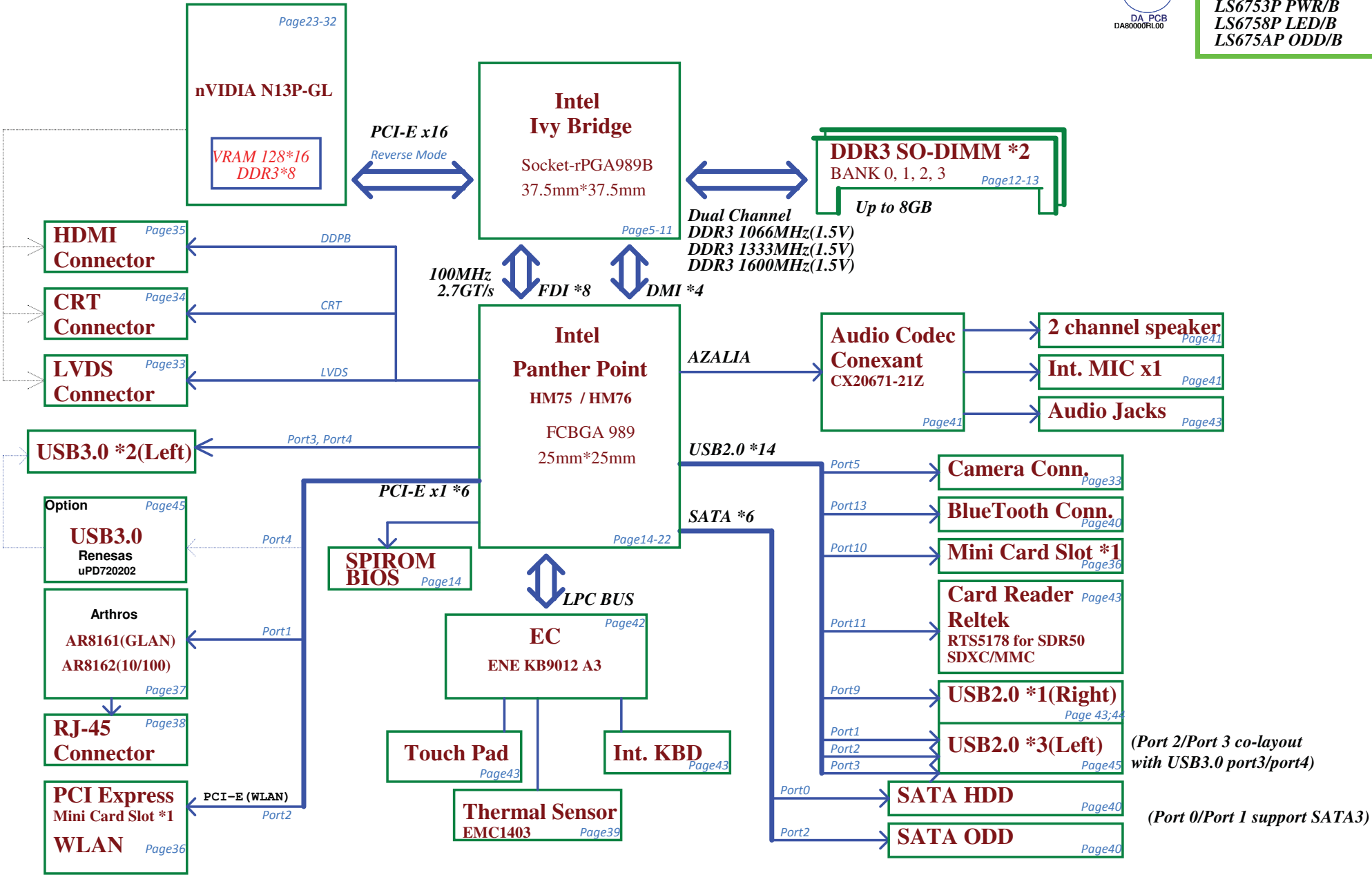
LA-7983P

REV: 0.3

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	Cover Page
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-7983P	0.3
				Date: Thursday, January 05, 2012	Sheet 1 of 60



LS7988P CR_AUDIO/B
LS7987P USB/B
LS6753P PWR/B
LS6758P LED/B
LS675AP ODD/B



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY CUSTOMER DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-7983P	0.3
				Date: Thursday, January 05, 2012	Sheet 2 of 60

power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

EC SM Bus2 address

Device	Device	Address
Smart Battery	0001 011X b	Thermal Sensor F75303M
		1001 101xb

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Vcc	3.3V +/- 5%					
Ra/Rc/Re	100K +/- 5%					
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	Porject	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Y-series	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Y-series	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Y-series	PVT
7	NC	2.500 V	3.300 V	3.300 V	Y-series	MP

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	
		1	USB Port (Left Side) USB2.0
	UHCI1	2	USB Port (Left Side) USB3.0
		3	USB Port (Left Side) USB3.0
	UHCI2	4	
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	USB/B (Right Side USB-BD)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	Blue Tooth

BTO Item	BOM Structure
GPU:N13P-GL	N13P@
UMA only	UMA@
HDMI	HDMI@
Internal-Intel-USB3.0	IU3@
External-NEC-USB3.0	EU3@
Blue Tooth	BT@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8162@
GIGA LAN	GIGA@
Camera	CMOS@
Green Clock	GCLK@
	GCLK244@
Unpop	@

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Notes List		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FRODO DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number LA-7983P	Rev 0.3	
Date	Thursday, January 05, 2012		Sheet	3 of 60		

Hot plug detect for IFP link C

VGA and GDDR3 Voltage Rails (N13P GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	Thermal Alert
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull low)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	N/A	
GPIO15	IN		Hot plug detect for IFP link C
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN		Hot Plug Detect for IFPE
GPIO19	IN	N/A	

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

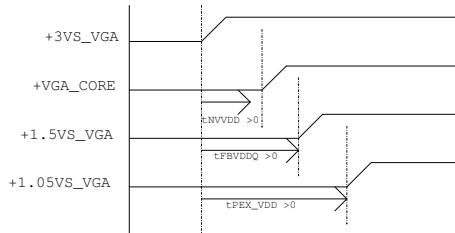
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13P-GL 64bit 1GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

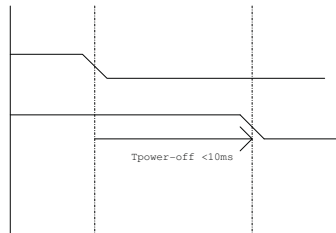
	Device ID
N13P-GL (28nm)	???

GPU	FB Memory (DDR3)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N13P-GL	Samsung 900MHz							
		64Mx16	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 900MHz							
		64Mx16	PD 10K	PD 15K	PD 15K	PU 20K	PD 35K	PU 45K
	Samsung 900MHz							
		128Mx16	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 900MHz							
		128Mx16	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K

X76

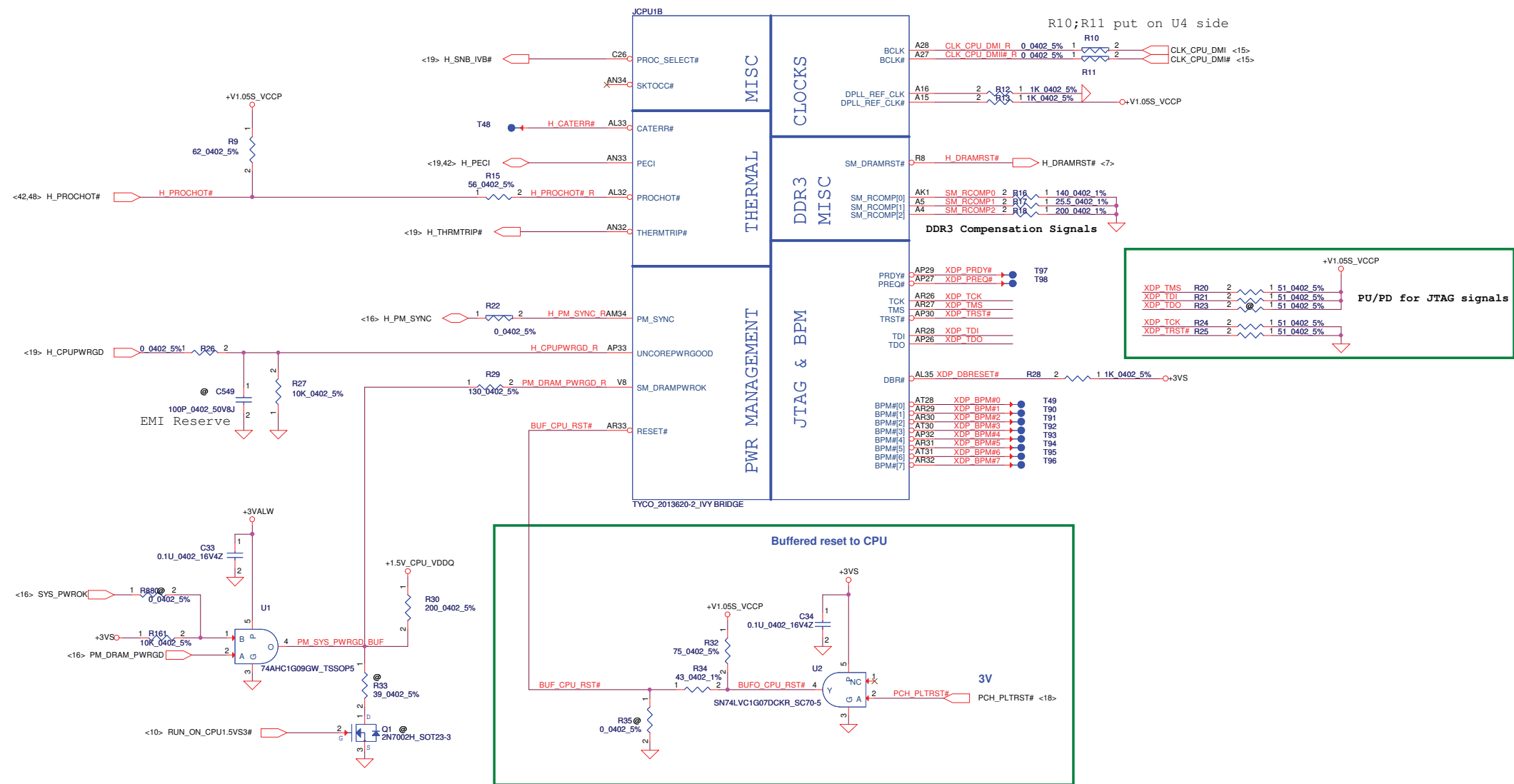


1. all power rail ramp up time should be larger than 40us
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

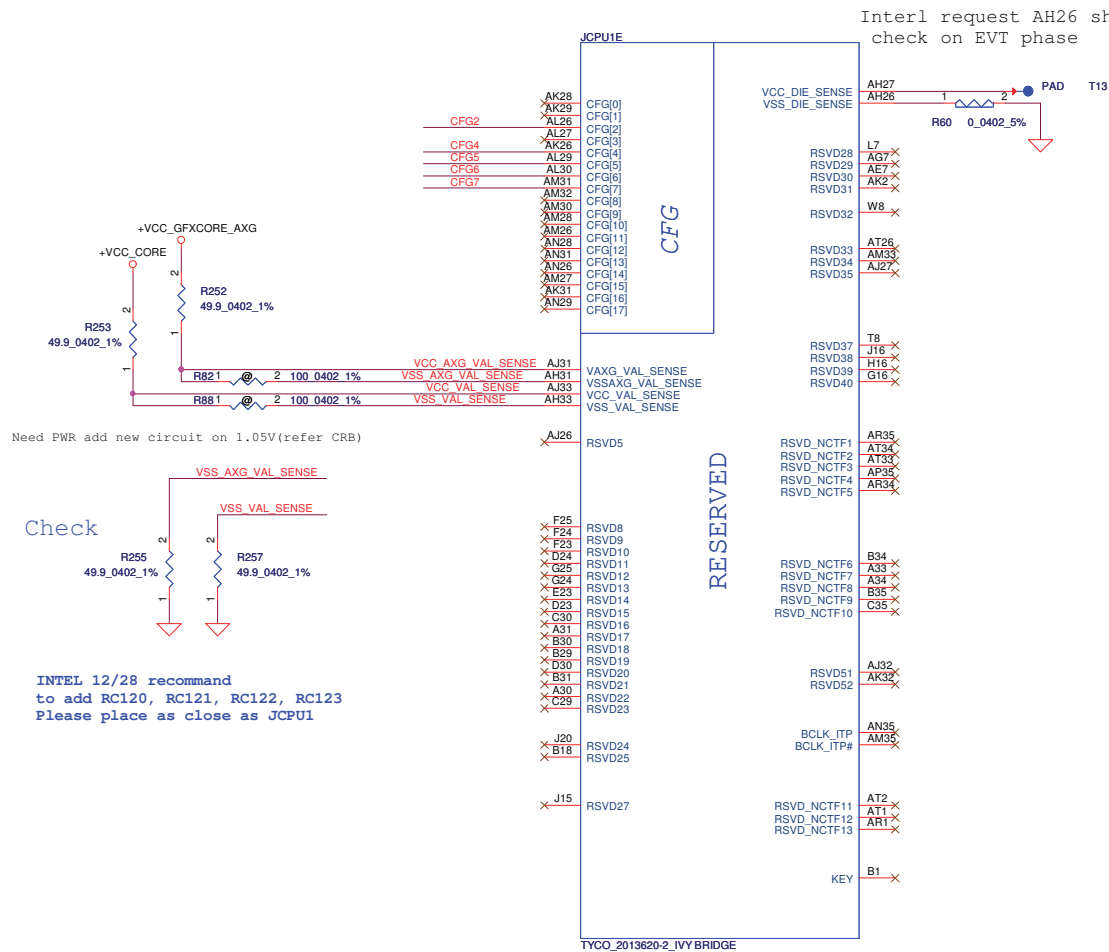


- 1.all GPU power rails should be turned off within 10ms

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIRST DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-7983P	0.3
				Date	Thursday, January 05, 2012
				Sheet	4 of 60



CFG Straps for Processor



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

POWER

EDS v1.5 QC=94A
DC=53A

JCPU1F

+V1.05S_VCCP

8.5A

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

VIDALERT#
VIDCLK
VIDSOUT

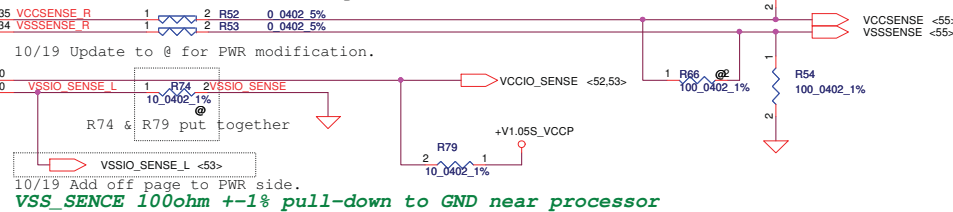
VCC_SENSE
VSS_SENSE
VCCIO_SENSE
VSS_SENSE_VCCIO

VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
VCC7
VCC8
VCC9
VCC10
VCC11
VCC12
VCC13
VCC14
VCC15
VCC16
VCC17
VCC18
VCC19
VCC20
VCC21
VCC22
VCC23
VCC24
VCC25
VCC26
VCC27
VCC28
VCC29
VCC30
VCC31
VCC32
VCC33
VCC34
VCC35
VCC36
VCC37
VCC38
VCC39
VCC40
VCC41
VCC42
VCC43
VCC44
VCC45
VCC46
VCC47
VCC48
VCC49
VCC50
VCC51
VCC52
VCC53
VCC54
VCC55
VCC56
VCC57
VCC58
VCC59
VCC60
VCC61
VCC62
VCC63
VCC64
VCC65
VCC66
VCC67
VCC68
VCC69
VCC70
VCC71
VCC72
VCC73
VCC74
VCC75
VCC76
VCC77
VCC78
VCC79
VCC80
VCC81
VCC82
VCC83
VCC84
VCC85
VCC86
VCC87
VCC88
VCC89
VCC90
VCC91
VCC92
VCC93
VCC94
VCC95
VCC96
VCC97
VCC98
VCC99
VCC100

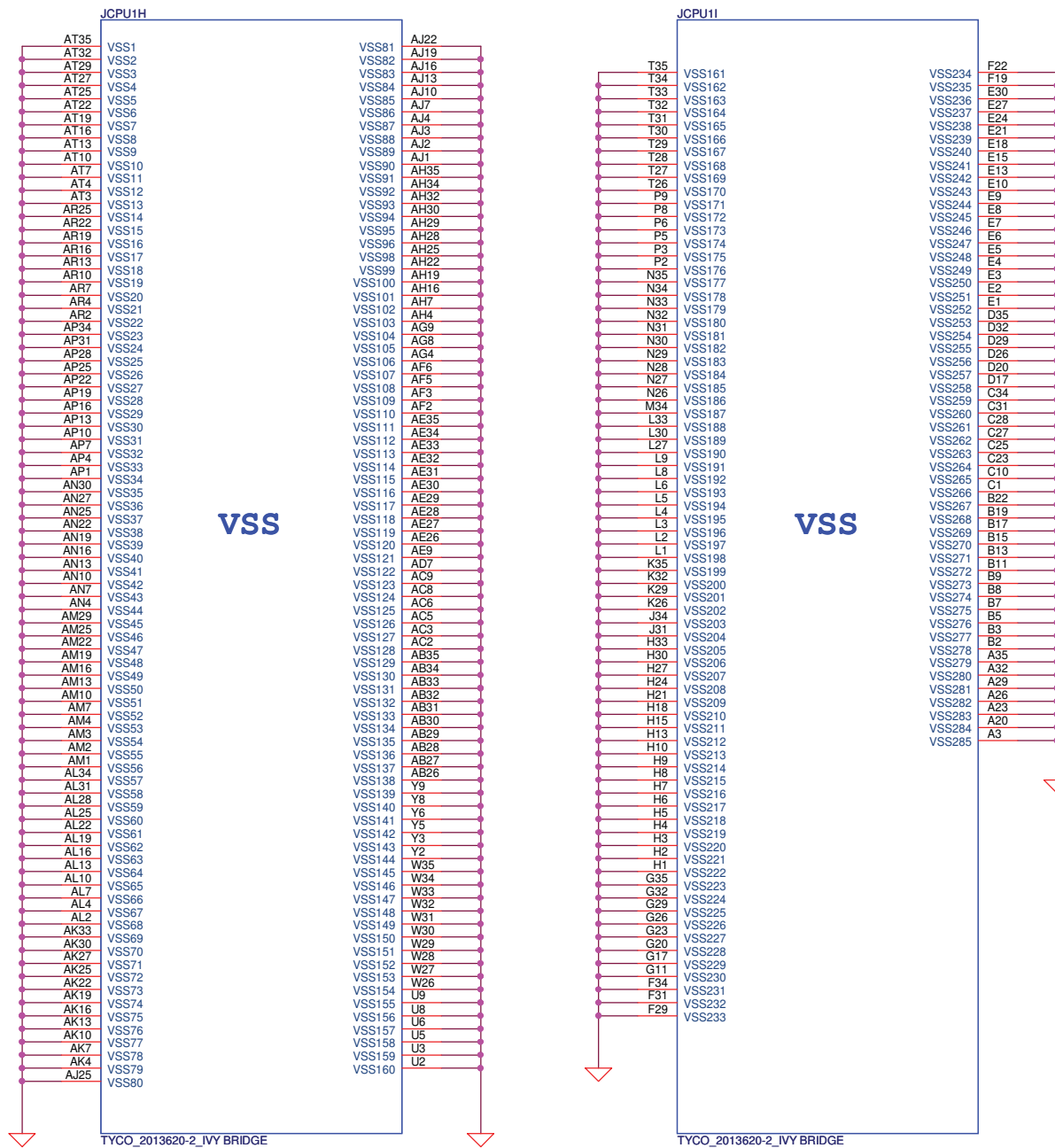
AH13
AH10
AG10
AC10
Y10
U10
P10
L10
J14
J13
J12
VCCIO10
VCCIO11
VCCIO12
VCCIO13
VCCIO14
VCCIO15
VCCIO16
VCCIO17
VCCIO18
VCCIO19
VCCIO20
VCCIO21
VCCIO22
VCCIO23
VCCIO24
E11
D14
D13
D12
D11
G14
C13
C12
C11
B14
B12
A14
A13
A12
A11
J23

VCC_SENSE 100ohm +-1% pull-up to VCC near processor

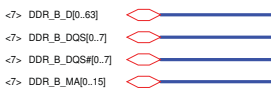
Trace Impedance =27-33 ohm
Trace Length Matc < 25 mils



Security Classification		Compal Secret Data				
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	PROCESSOR(5/7) PWR,BYPASS	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Doc No		
				Doc Custom	Document Number LA-7983P	Rev 0.3
				Date	Thursday, January 05, 2012	Sheet 9 of 60



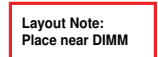
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	PROCESSOR(7/7) VSS
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number LA-7983P
				Date:	Thursday, January 05, 2012
				Sheet	11 of 60
				Rev	0.3



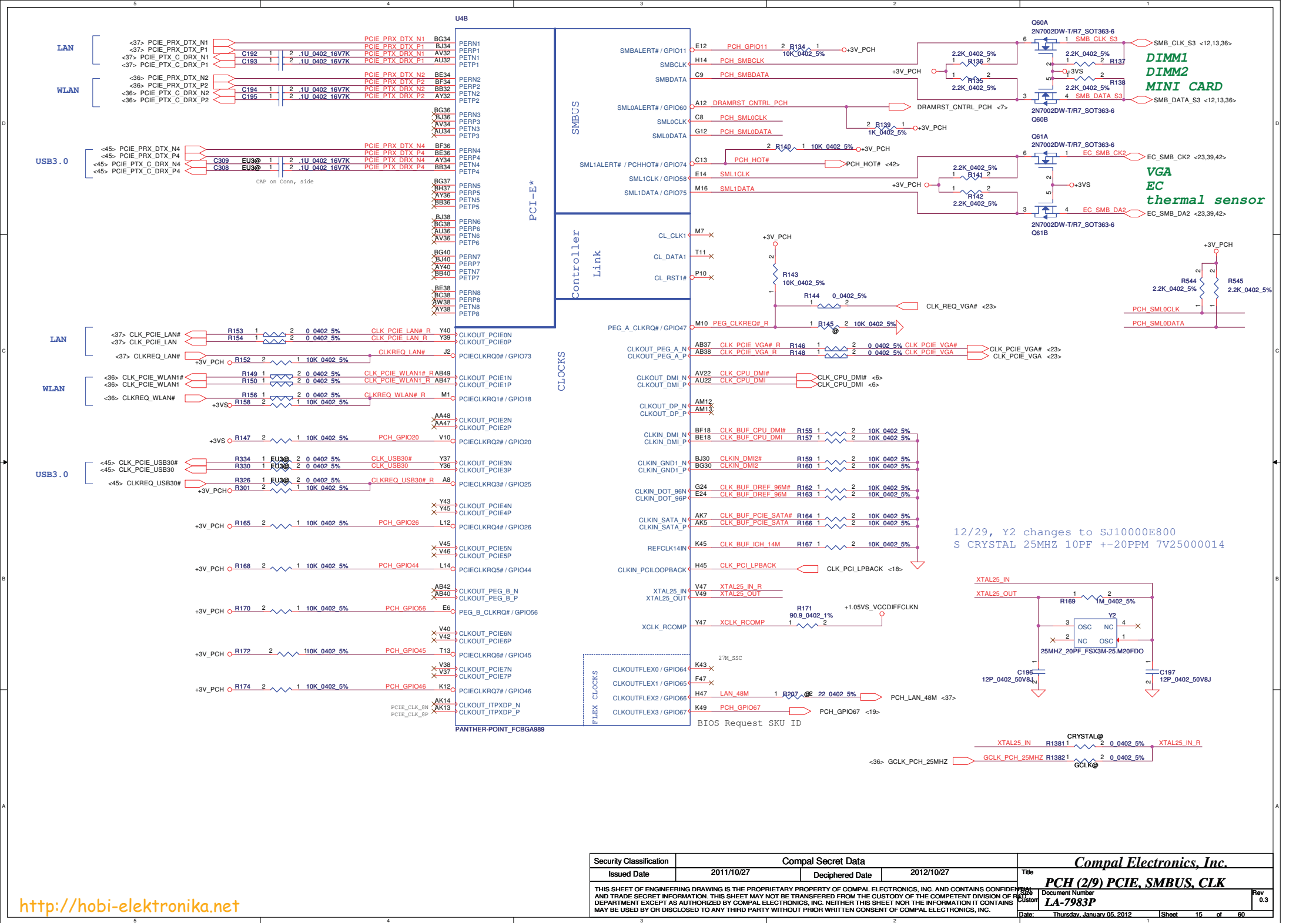
Layout Note:
Place near DIMM

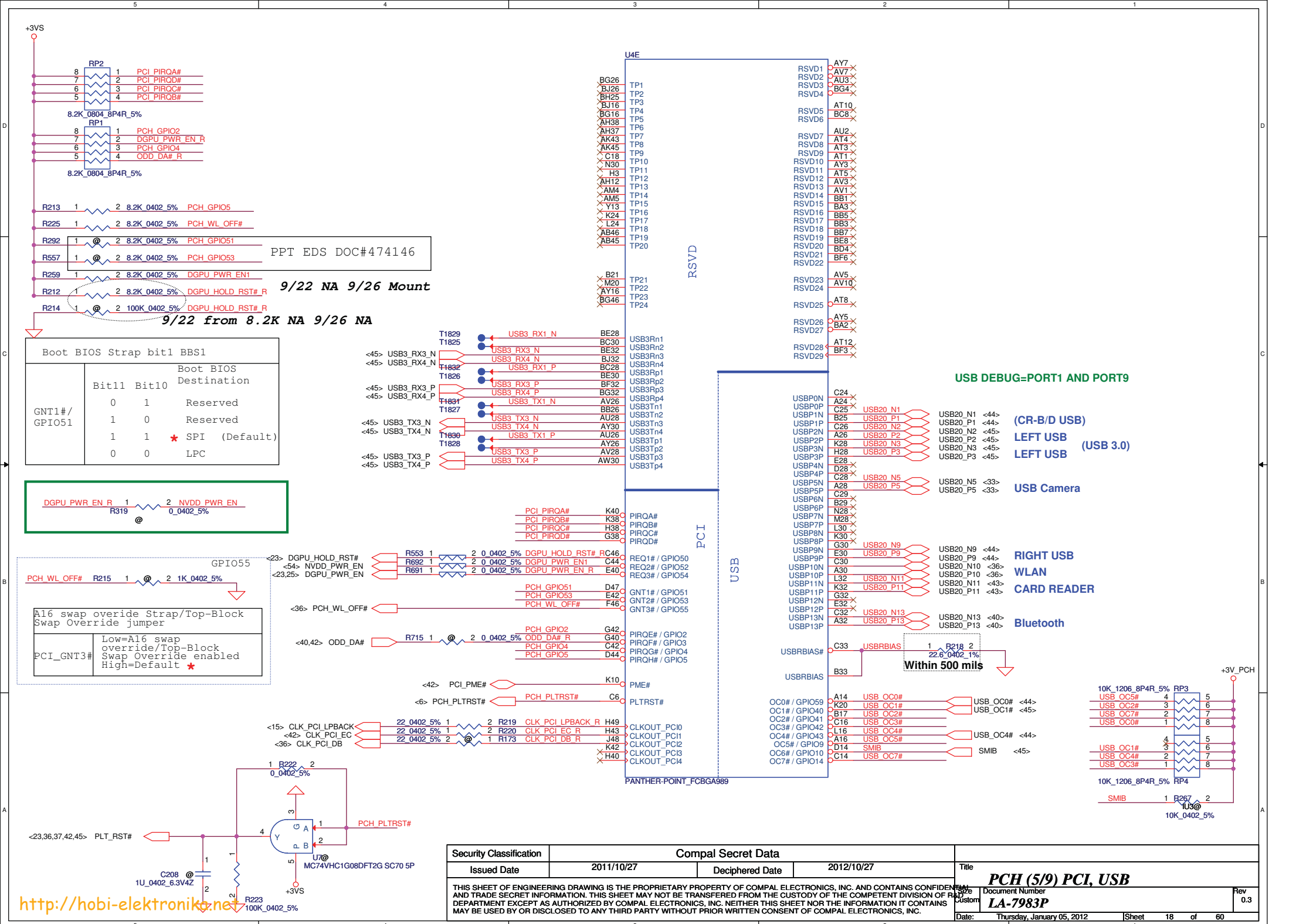
Layout Note:
Place near DIMM

Layout Note:
Place near DIMM



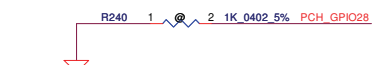
<http://hobi-elektronika.net>



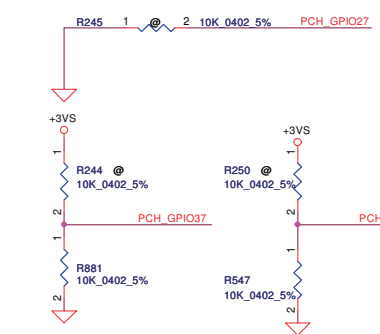




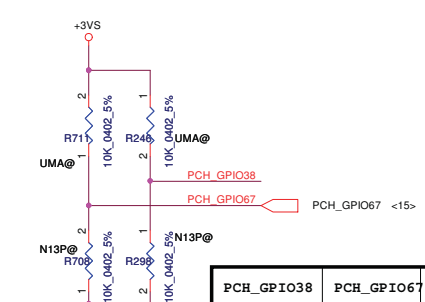
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable



★ PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

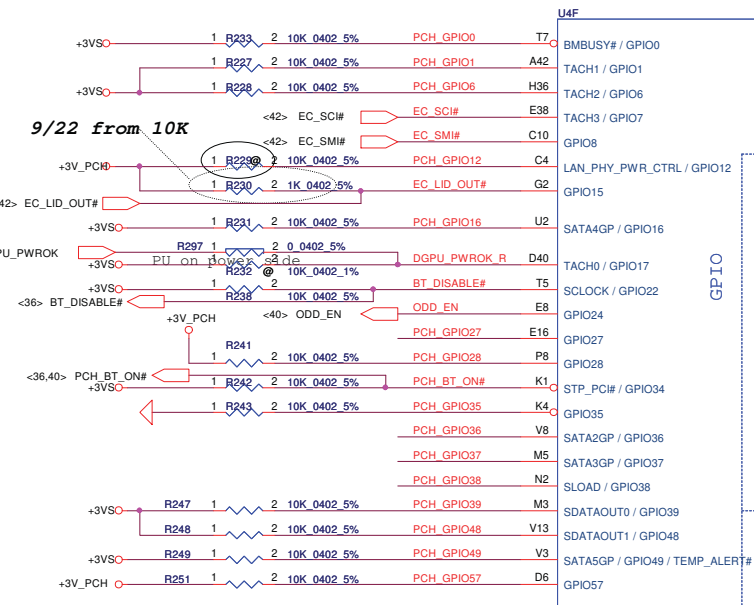


BIOS Request SKU ID



PCH_GPIO38	PCH_GPIO67	Function
0	0	Optimus
0	1	Reserved
1	0	DIS
1	1	UMA

9/22 from 10K



GPIO

NCIF

Security Classification		Compal Secret Data		Title	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Size	Custom
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-7983P	0.3
				Date: Thursday, January 05, 2012	Sheet 19 of 60

PCH_GPIO70	Function
0	14/15"
1	17"
PCH_GPIO71	
0	USB3.0 by PCH
1	USB3.0 by NEC

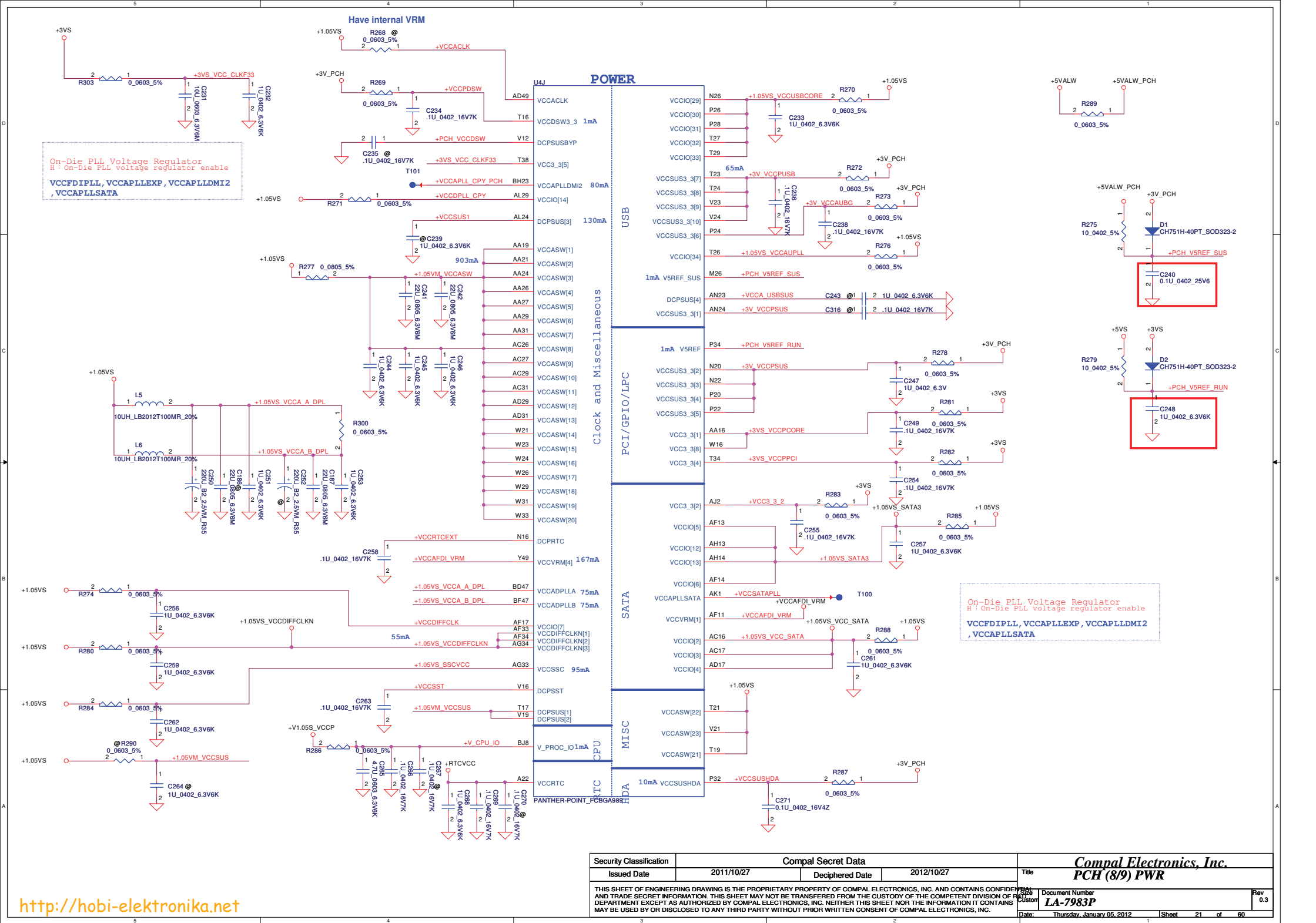
9/22 from 10K

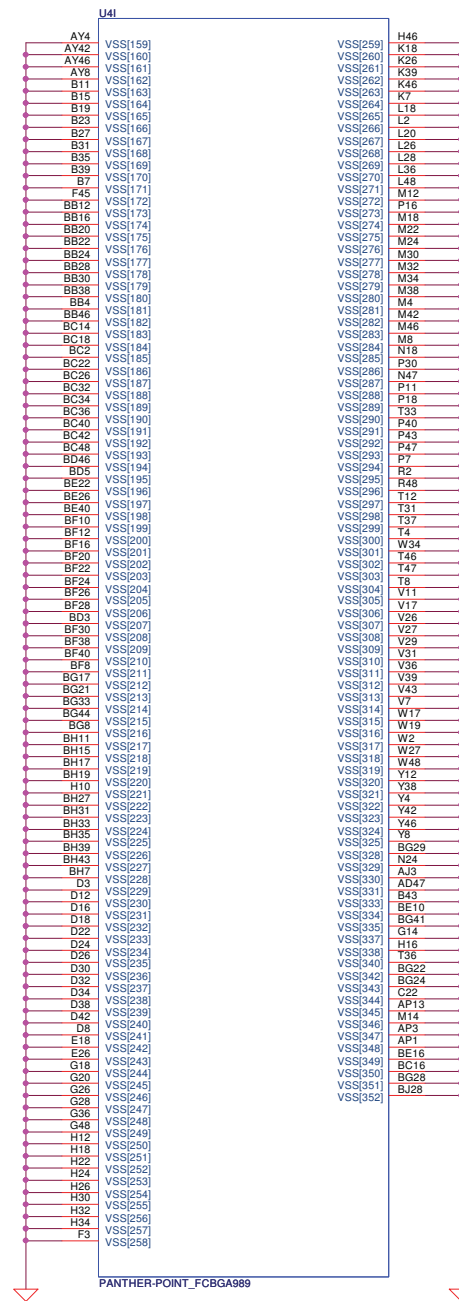
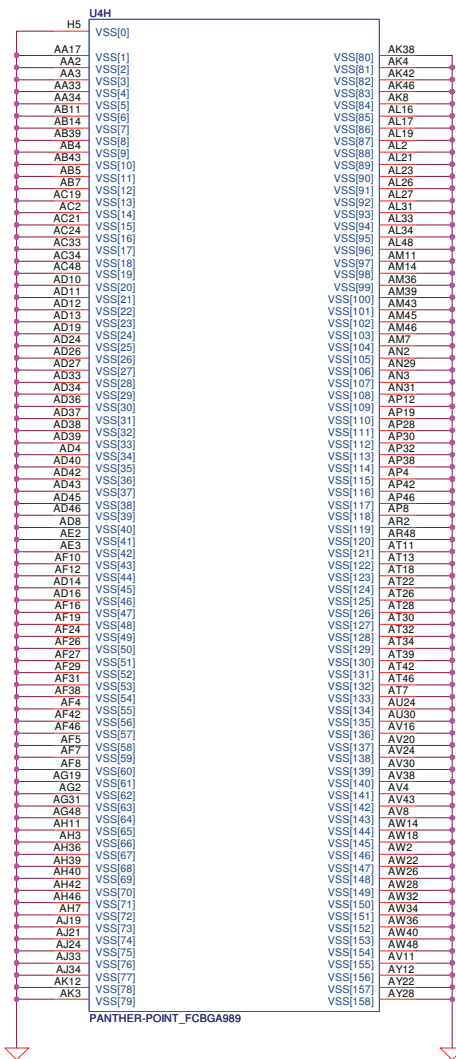
9/22 from 10K

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

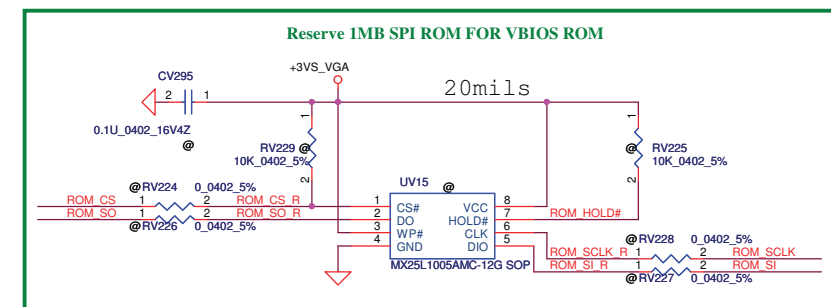
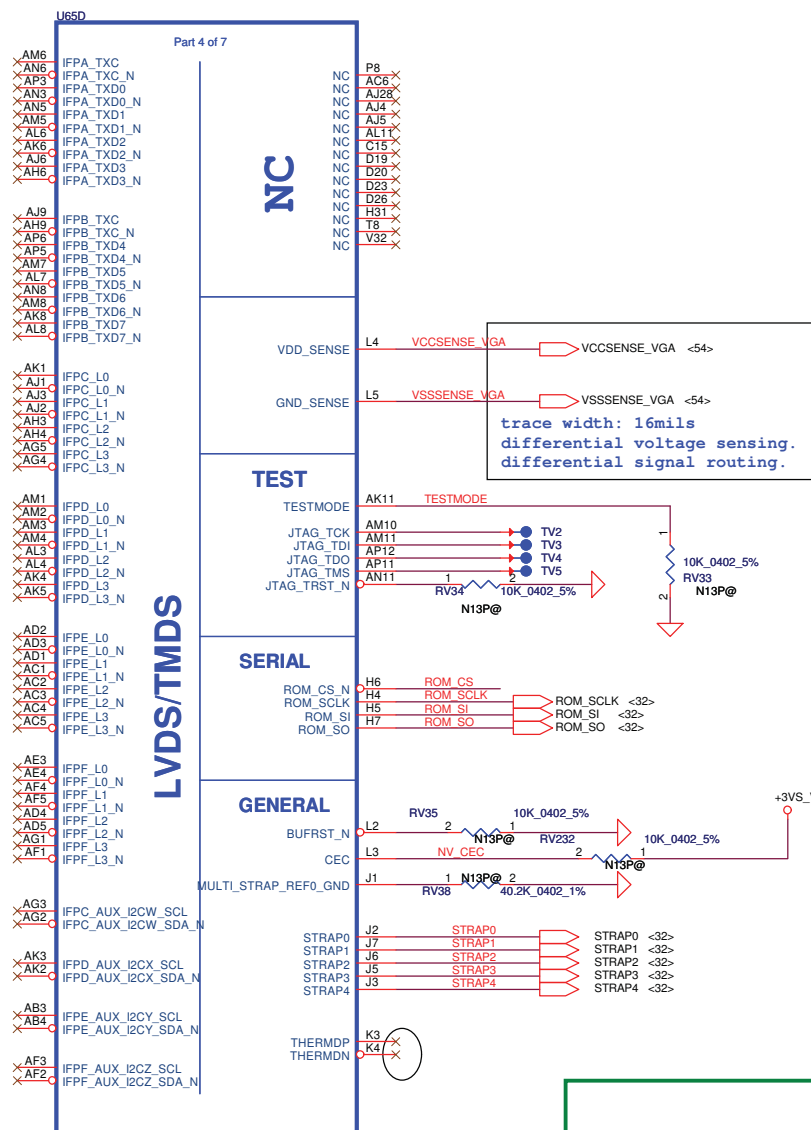
Weak internal PU, Do not pull low
CLOSE TO THE BRANCHING POINT

Compal Electronics, Inc.

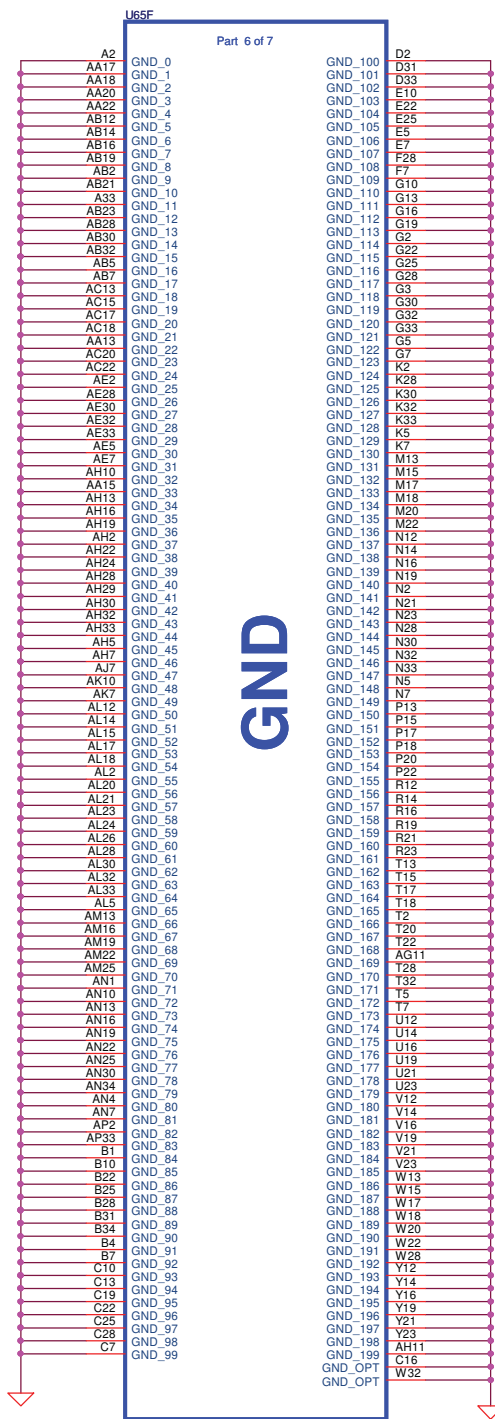




Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date		2011/10/27		Deciphered Date		2012/10/27	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF PANTHER-POINT WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title			
				PCH (9/9) VSS			
				Document Number			
				LA-7983P			
				Rev 0.3			
Date				Thursday, January 05, 2012		Sheet 22 of 60	

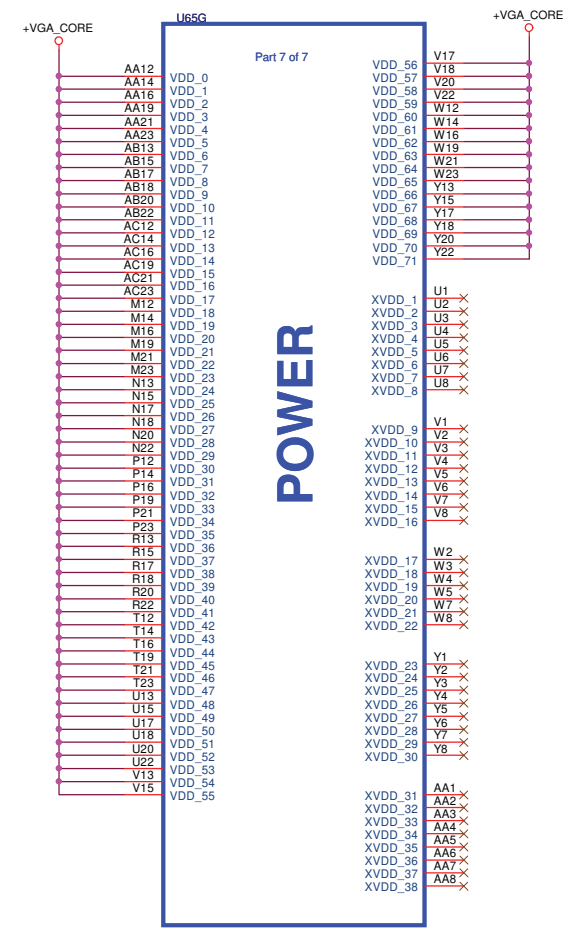


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	N13X-LVDS/HDMI/DP/THM	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
					LA-7983P	0.3
				Date	Thursday, January 05, 2012	Sheet 24 of 60



N13P-PES-A1_FCBGA908

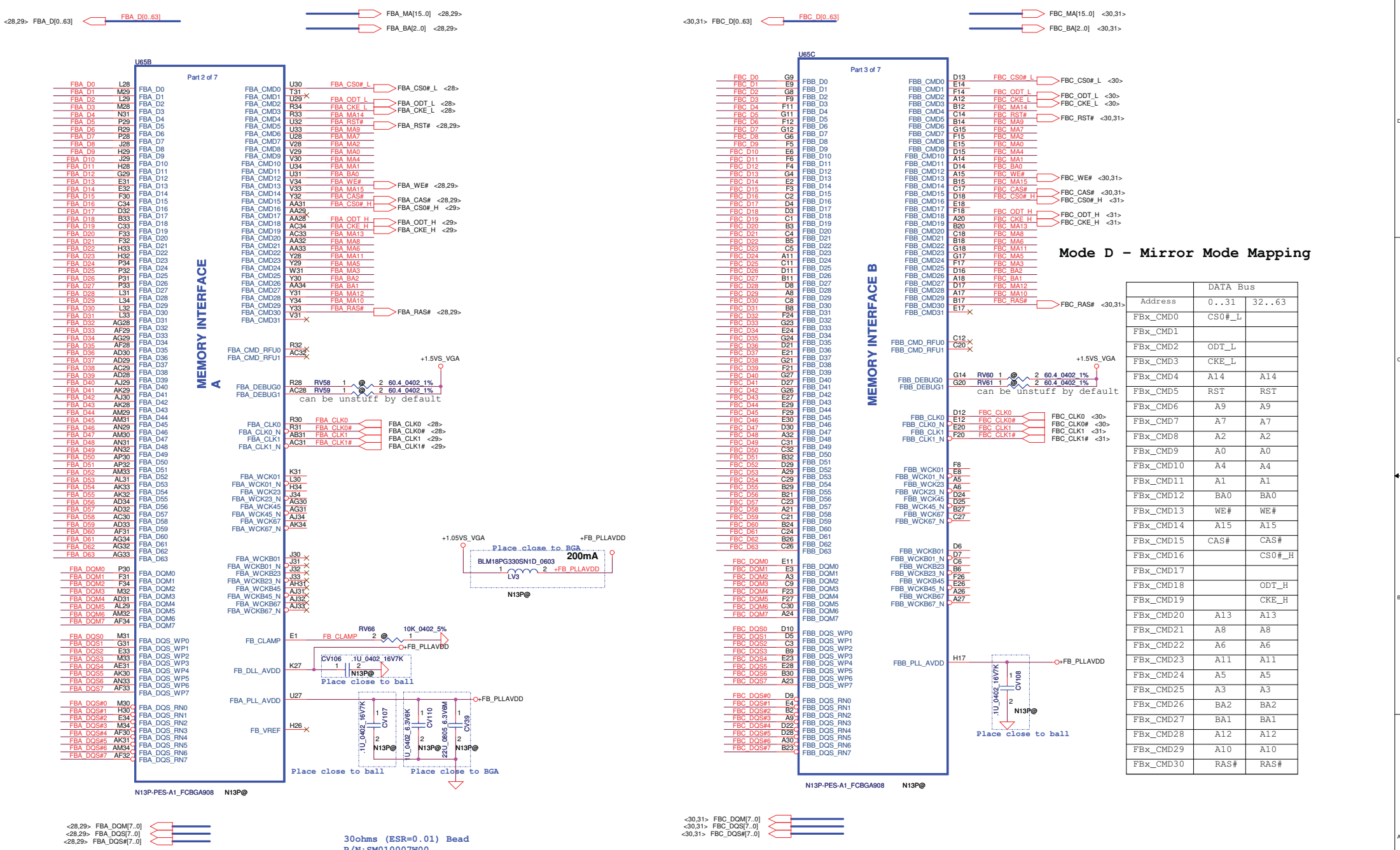
N13P@



N13P-PES-A1_FCBGA908

N13P@

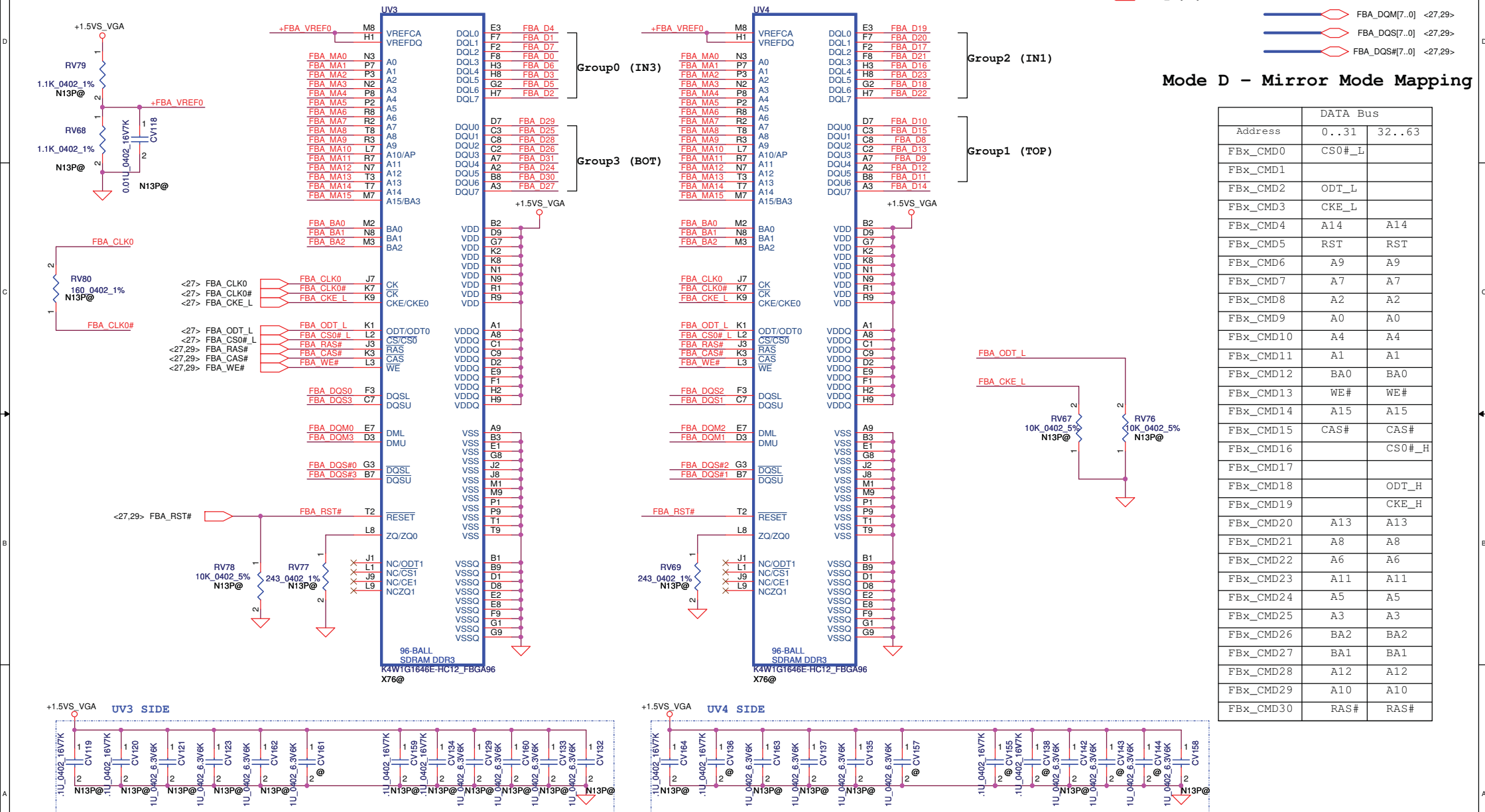
Security Classification		Compal Secret Data				Compal Electronics, Inc.				
Issued Date		2011/10/27		Deciphered Date		2012/10/27		Title		
								N13-VGA CORE, GND		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						Size	Document Number		Rev	
							LA-7983P		0.3	
		3		2		Date: Thursday, January 05, 2012		Sheet 26 of 60		



Mode D - Mirror Mode Mapping

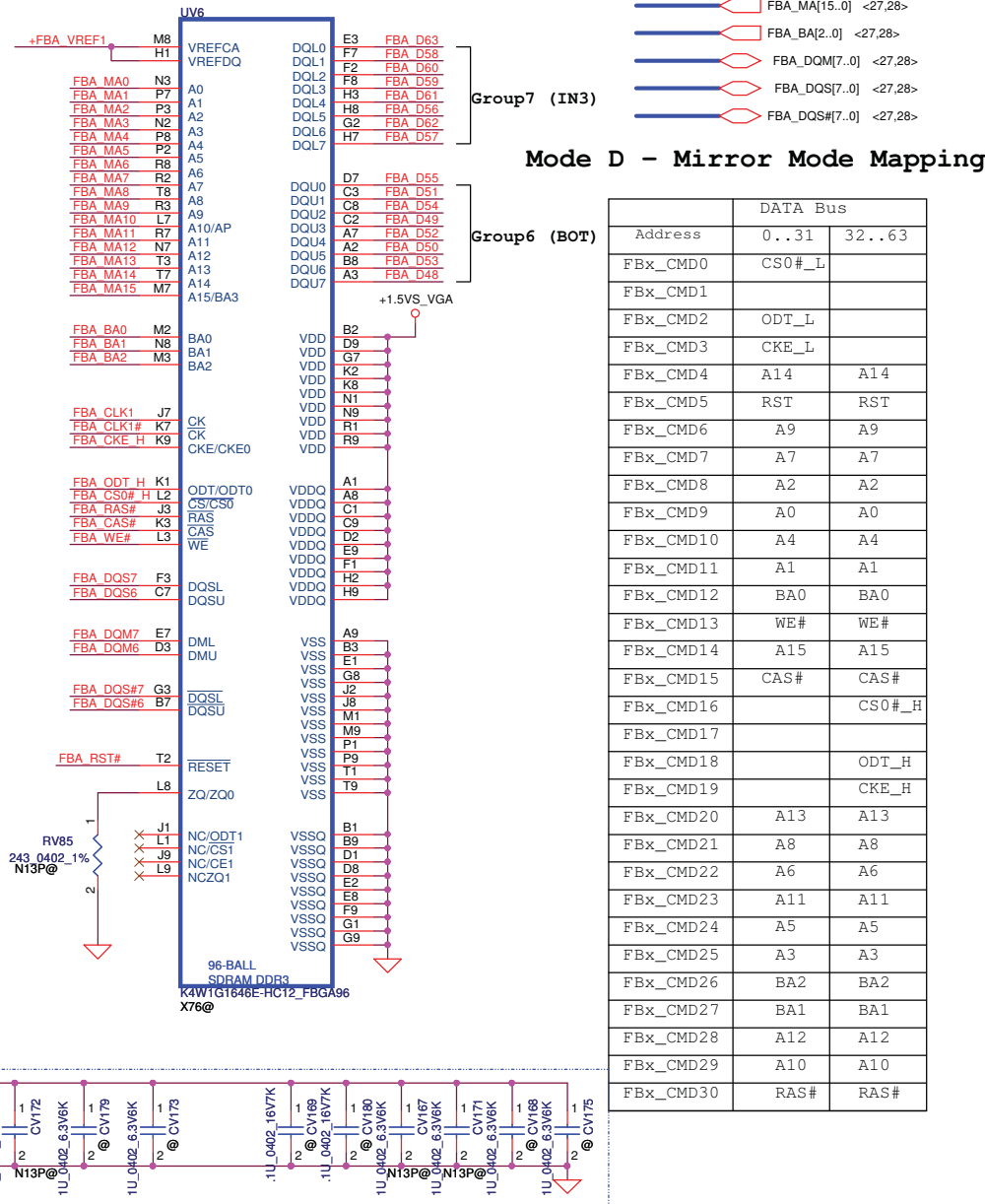
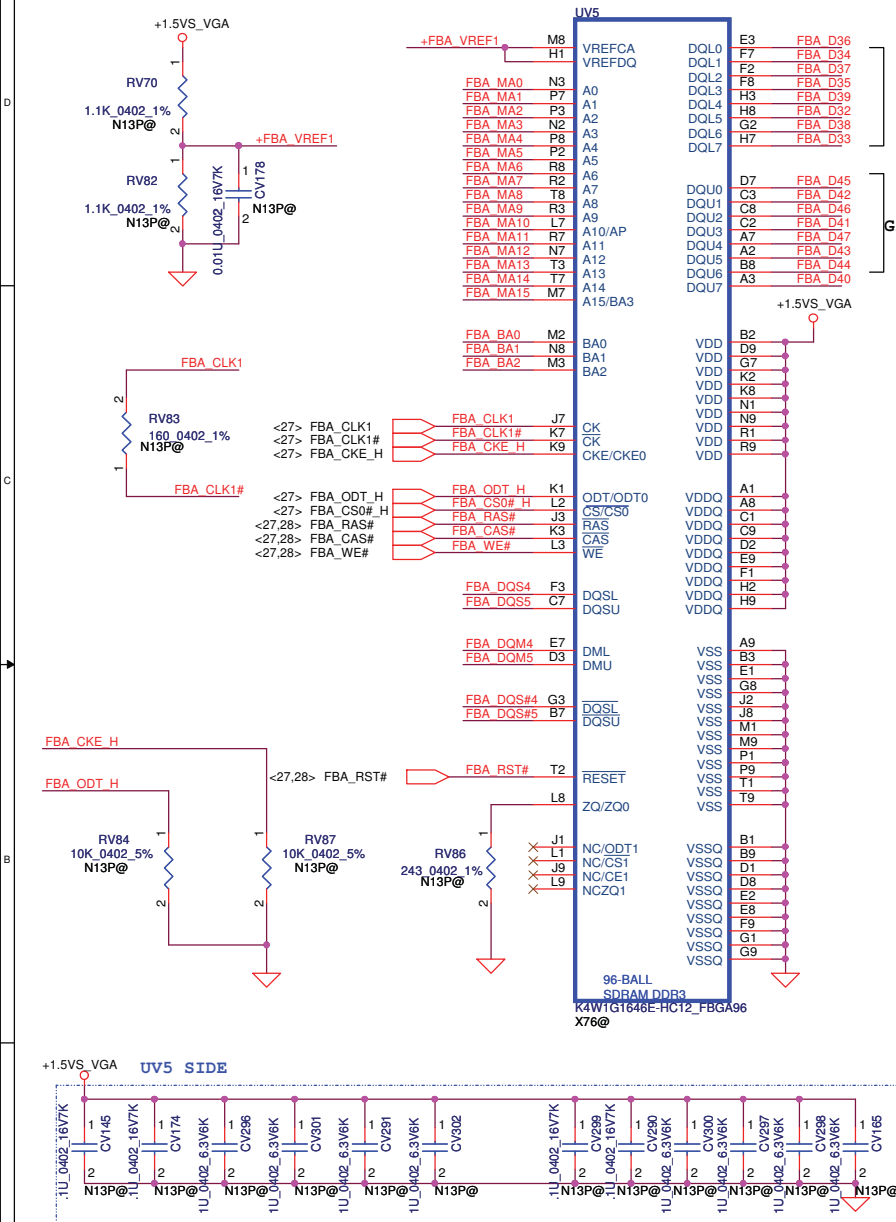
Address	DATA Bus
FbX_CMD0	CS0#_L
FbX_CMD1	ODT_L
FbX_CMD2	CKE_L
FbX_CMD4	A14
FbX_CMD5	RST
FbX_CMD6	A9
FbX_CMD7	A7
FbX_CMD8	A2
FbX_CMD9	A0
FbX_CMD10	A4
FbX_CMD11	A1
FbX_CMD12	BA0
FbX_CMD13	WE#
FbX_CMD14	A15
FbX_CMD15	CAS#
FbX_CMD16	CS0#_H
FbX_CMD17	
FbX_CMD18	ODT_H
FbX_CMD19	CKE_H
FbX_CMD20	A13
FbX_CMD21	A8
FbX_CMD22	A6
FbX_CMD23	A11
FbX_CMD24	A5
FbX_CMD25	A3
FbX_CMD26	BA2
FbX_CMD27	BA1
FbX_CMD28	A12
FbX_CMD29	A10
FbX_CMD30	RAS#

Memory Partition A - Lower 32 bits



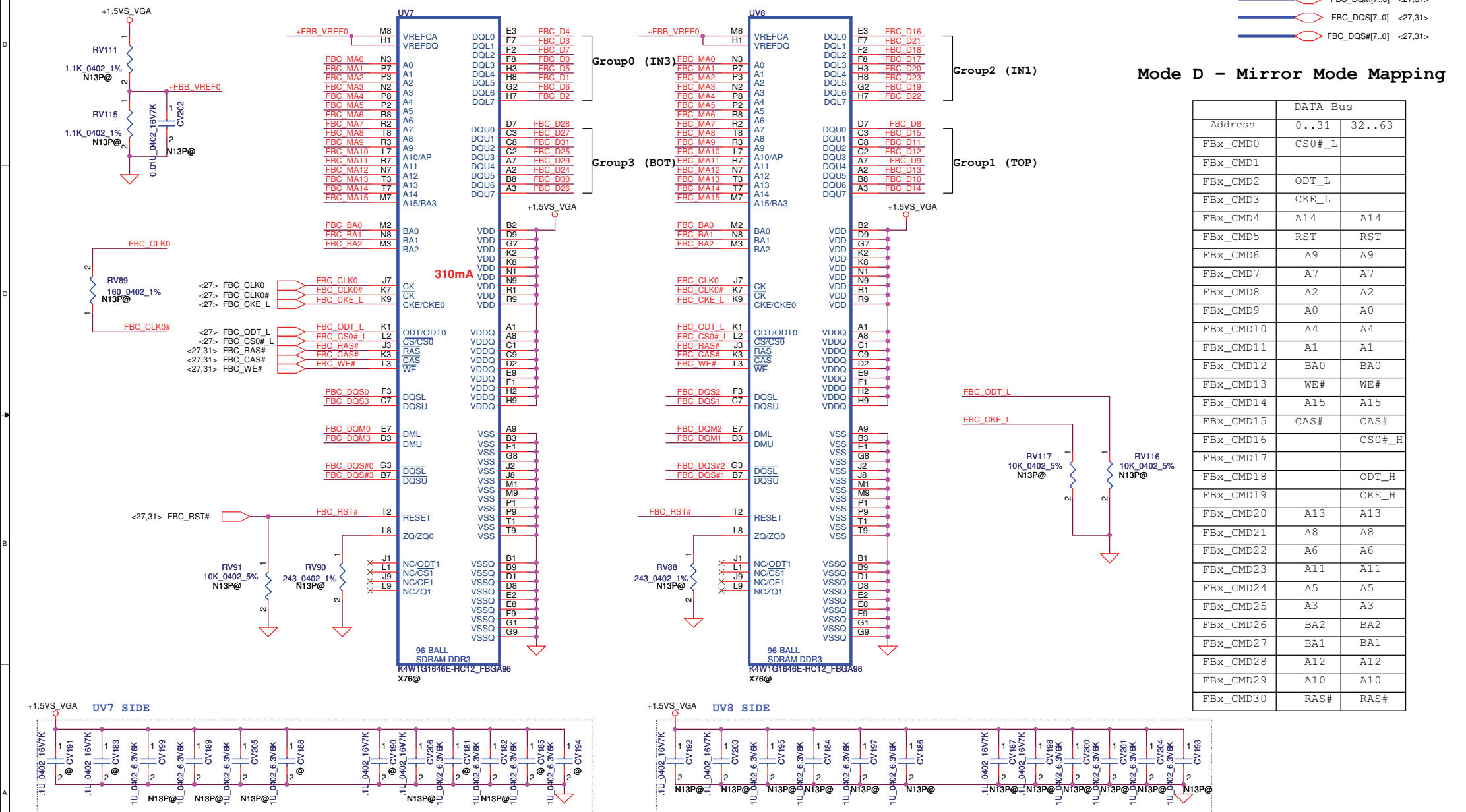
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	N13X-VRAM A Lower
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				LA-7983P	
				Date	Thursday, January 05, 2012
				Sheet	28 of 60

Memory Partition A - Upper 32 bits



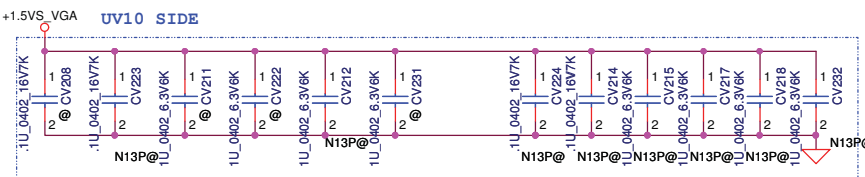
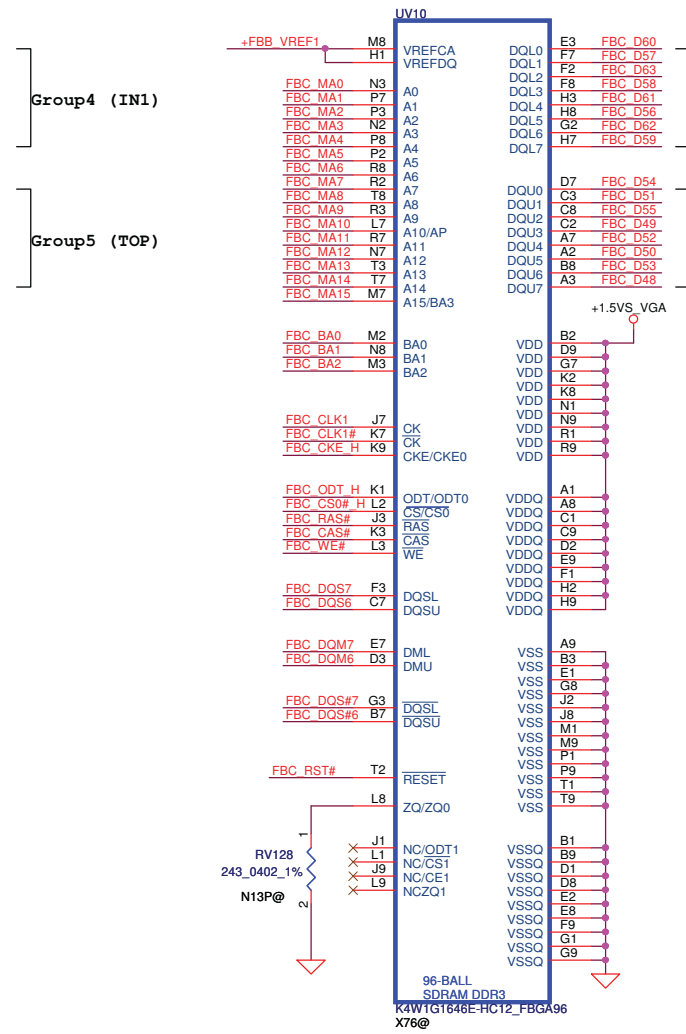
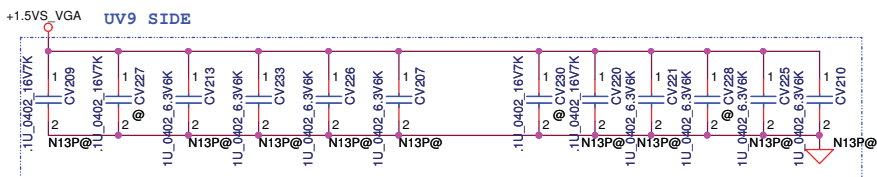
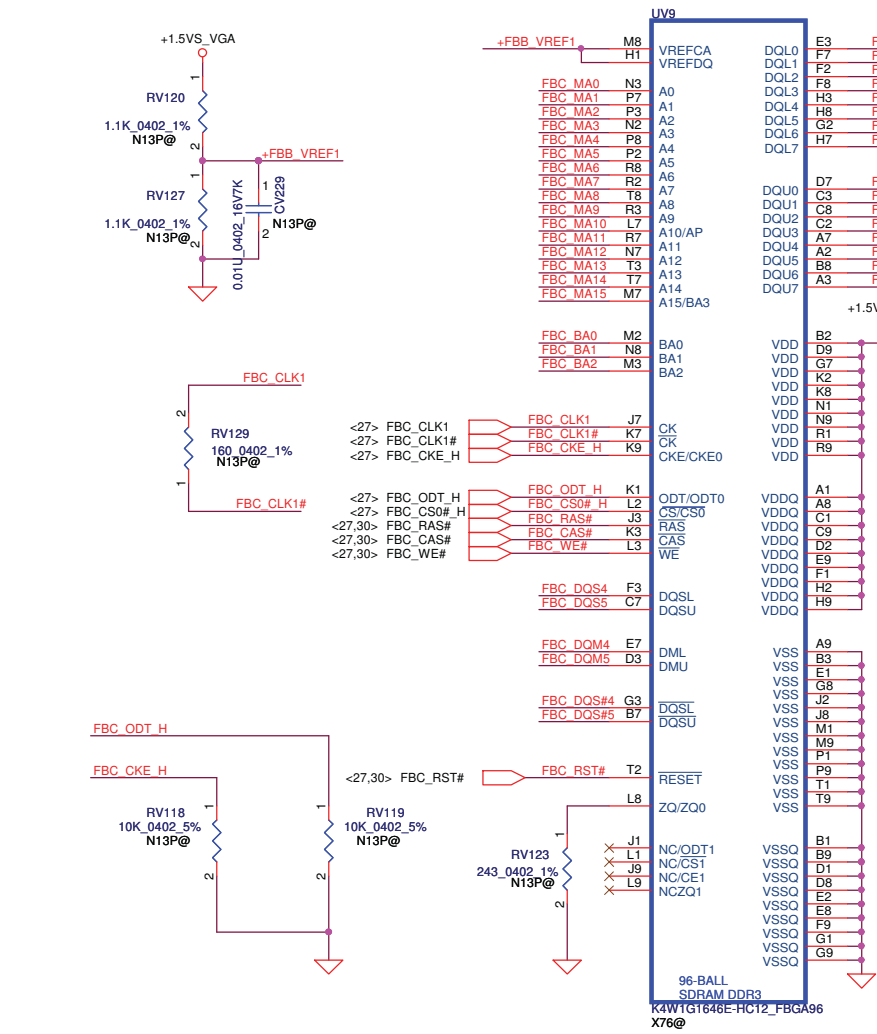
	DATA Bus	
Address	0..31	32..63
FbX_CMD0	CS0#_L	
FbX_CMD1		
FbX_CMD2	ODT_L	
FbX_CMD3	CKE_L	
FbX_CMD4	A14	A14
FbX_CMD5	RST	RST
FbX_CMD6	A9	A9
FbX_CMD7	A7	A7
FbX_CMD8	A2	A2
FbX_CMD9	A0	A0
FbX_CMD10	A4	A4
FbX_CMD11	A1	A1
FbX_CMD12	BA0	BA0
FbX_CMD13	WE#	WE#
FbX_CMD14	A15	A15
FbX_CMD15	CAS#	CAS#
FbX_CMD16		CS0#_I
FbX_CMD17		
FbX_CMD18		ODT_H
FbX_CMD19		CKE_H
FbX_CMD20	A13	A13
FbX_CMD21	A8	A8
FbX_CMD22	A6	A6
FbX_CMD23	A11	A11
FbX_CMD24	A5	A5
FbX_CMD25	A3	A3
FbX_CMD26	BA2	BA2
FbX_CMD27	BA1	BA1
FbX_CMD28	A12	A12
FbX_CMD29	A10	A10
FbX_CMD30	RAS#	RAS#

Memory Partition C - Lower 32 bits



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	N13X-VRAM C Lower
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev 0.3
				Document Number	LA-7983P
				Date	Thursday, January 05, 2012
				Sheet	30 of 60

Memory Partition C - Upper 32 bits



- FBC_D[0..63] <27,30>
- FBC_MA[15..0] <27,30>
- FBC_BA[2..0] <27,30>
- FBC_DQM[7..0] <27,30>
- FBC_DQS[7..0] <27,30>
- FBC_DQS# [7..0] <27,30>

Mode D - Mirror Mode Mapping

DATA Bus	
Address	0..31 32..63
FBx_CMD0	CS0#_L
FBx_CMD1	
FBx_CMD2	ODT_L
FBx_CMD3	CKE_L
FBx_CMD4	A14 A14
FBx_CMD5	RST RST
FBx_CMD6	A9 A9
FBx_CMD7	A7 A7
FBx_CMD8	A2 A2
FBx_CMD9	A0 A0
FBx_CMD10	A4 A4
FBx_CMD11	A1 A1
FBx_CMD12	BA0 BA0
FBx_CMD13	WE# WE#
FBx_CMD14	A15 A15
FBx_CMD15	CAS# CAS#
FBx_CMD16	
FBx_CMD17	CS0#_H
FBx_CMD18	ODT_H
FBx_CMD19	CKE_H
FBx_CMD20	A13 A13
FBx_CMD21	A8 A8
FBx_CMD22	A6 A6
FBx_CMD23	A11 A11
FBx_CMD24	A5 A5
FBx_CMD25	A3 A3
FBx_CMD26	BA2 BA2
FBx_CMD27	BA1 BA1
FBx_CMD28	A12 A12
FBx_CMD29	A10 A10
FBx_CMD30	RAS# RAS#

Security Classification

Compal Secret Data

Issued Date

2011/10/27

Deciphered Date

2012/10/27

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Title

Compal Electronics, Inc.

Size

Custom

Document Number

LA-7983P

Rev

0.3

Date

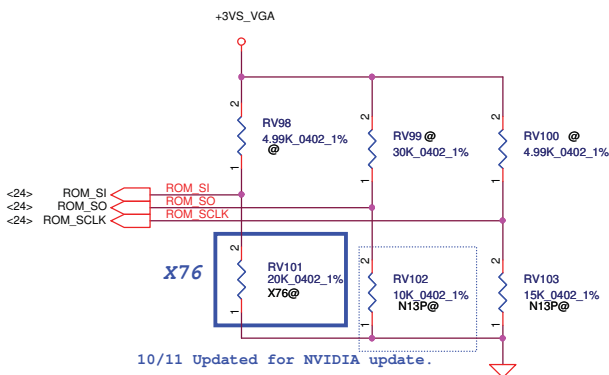
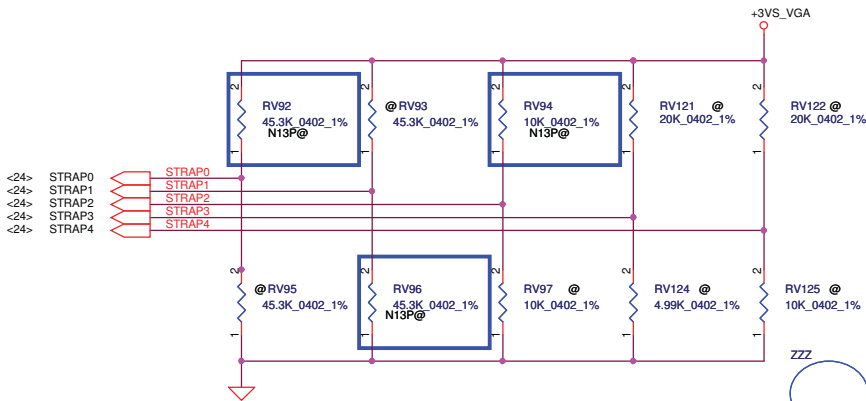
Thursday, January 05, 2012

Sheet

31

of

60



For N13P-GL strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GL	900 MHz	128M* 16" 8	Samsung (2Gb)	R	R	R	n/a	n/a	R	R	R
N13P-GL	900 MHz	128M* 16" 8	K4W2G1646C-HC11	PU 45K	PD 45K	PU 45K	n/a	n/a	PD 45K	PD 10K	PD 15K
N13P-GL	900 MHz	128M* 16" 8	Hynix (2Gb)	R	R	R	n/a	n/a	R	R	R
N13P-GL	900 MHz	128M* 16" 8	H5TQ1G63DFR-11C	PU 45K	PD 45K	PU 45K	n/a	n/a	PD 35K	PD 10K	PD 15K
N13P-GL	900 MHz	64M* 16" 8	Samsung (1Gb)	R	R	R	n/a	n/a	R	R	R
N13P-GL	900 MHz	64M* 16" 8	K4W1G1646G-BC11	PU 45K	PD 45K	PU 45K	n/a	n/a	PD 20K	PD 10K	PD 15K
N13P-GL	900 MHz	64M* 16" 8	Hynix (1Gb)	R	R	R	n/a	n/a	R	R	R
N13P-GL	900 MHz	64M* 16" 8	H5TQ1G63DFR-11C	PU 45K	PD 45K	PU 45K	n/a	n/a	PD 15K	PD 10K	PD 15K

10/11 Updated for NVIDIA update.

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

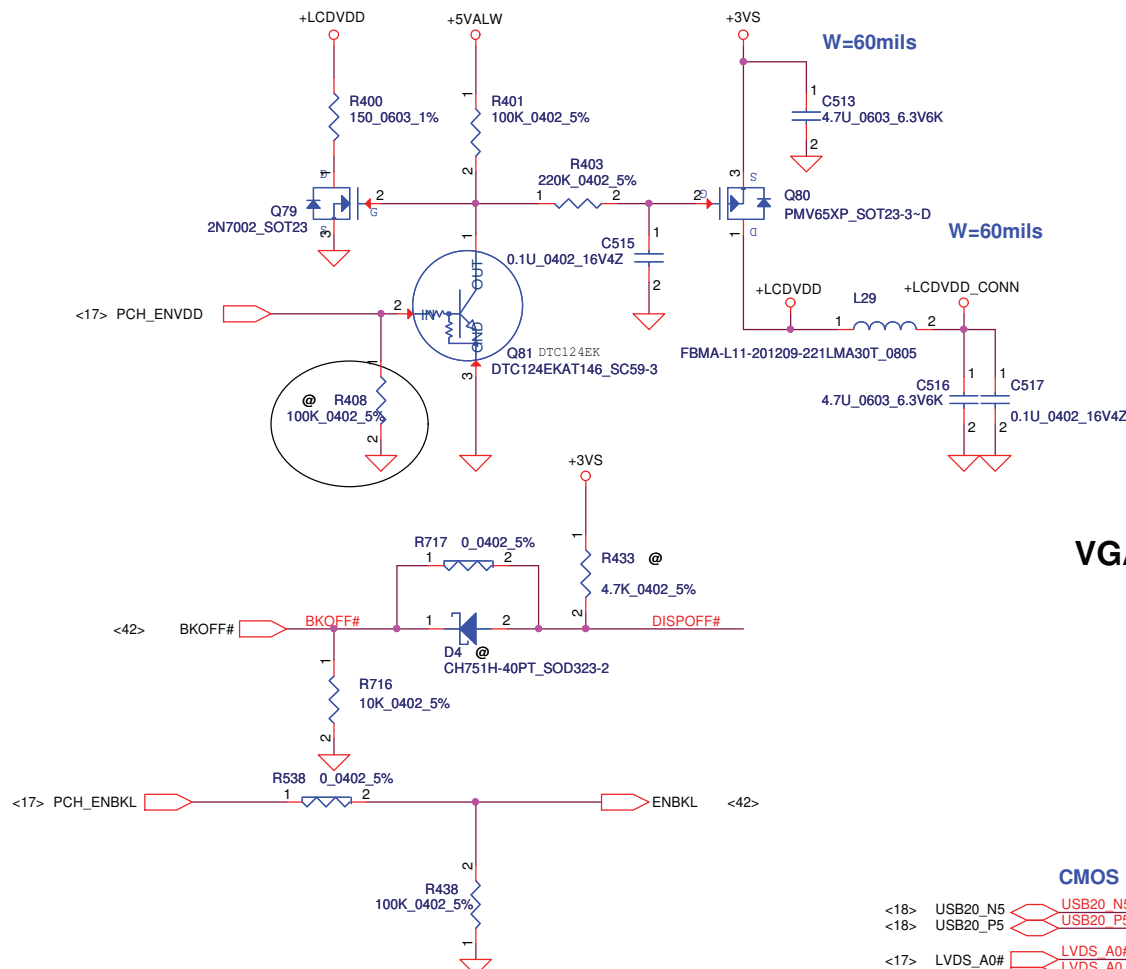
USER Straps	
User[3:0]	
1000-1100	Customer defined

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

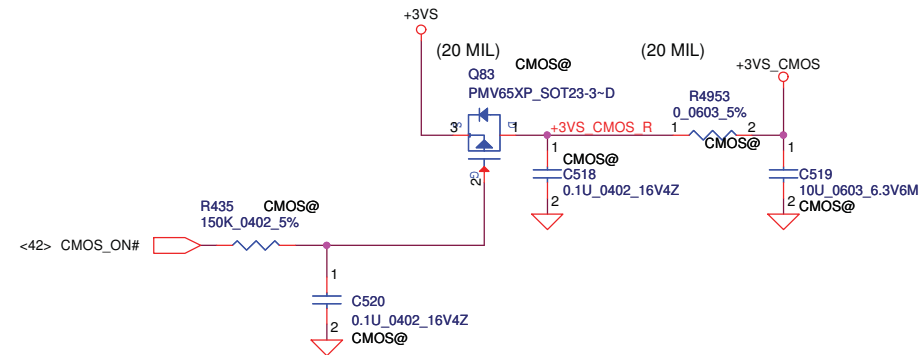
PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/10/27		Deciphered Date		2012/10/27		Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size		Document Number		Rev		Date	
				Custom		LA-7983P		0.3		Thursday, January 05, 2012	
										Sheet 32 of 60	

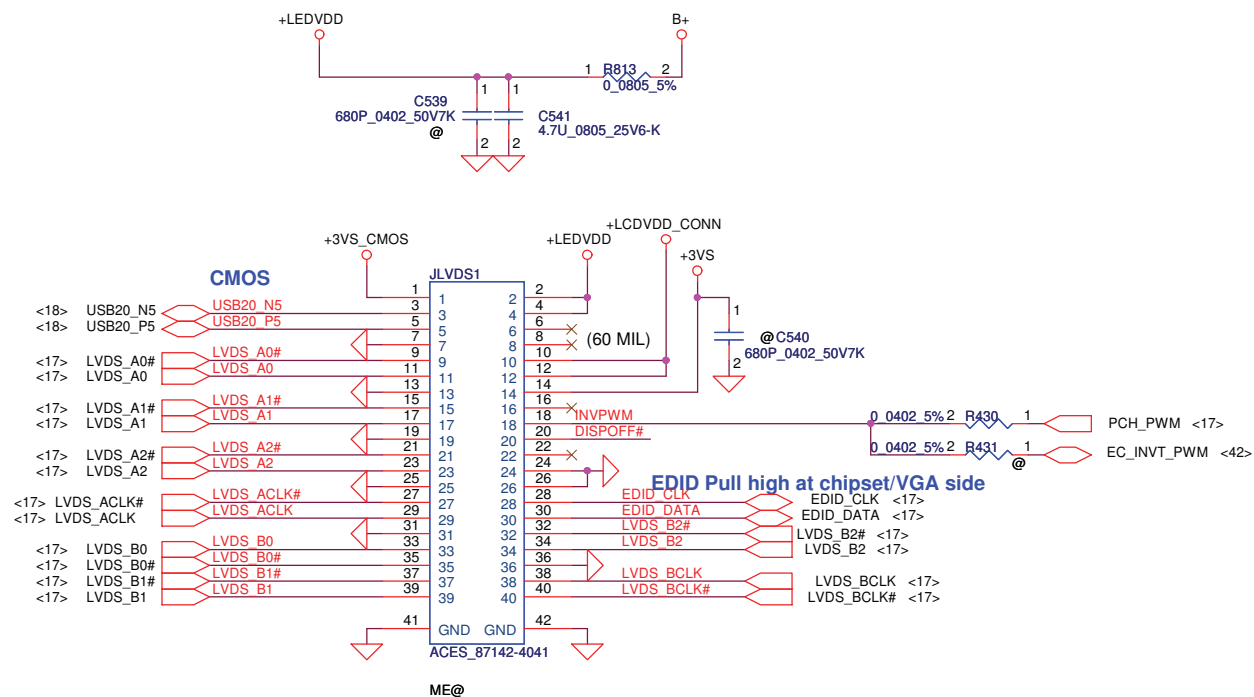
LCD POWER CIRCUIT



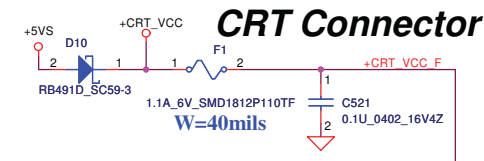
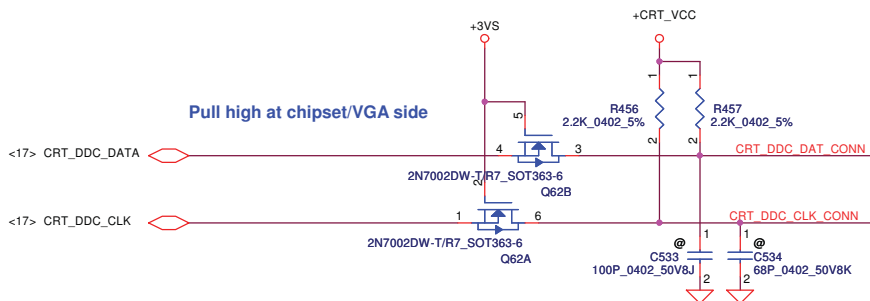
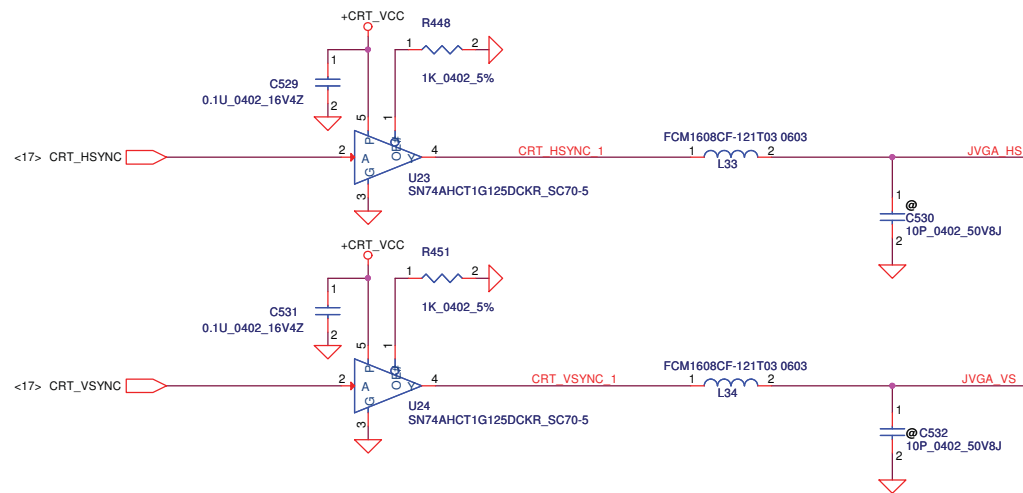
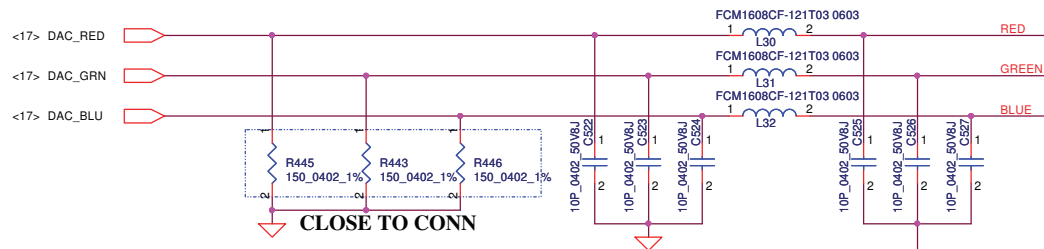
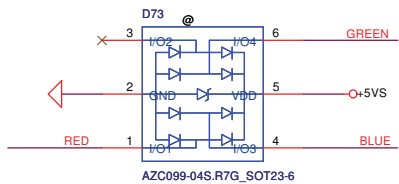
CMOS Camera



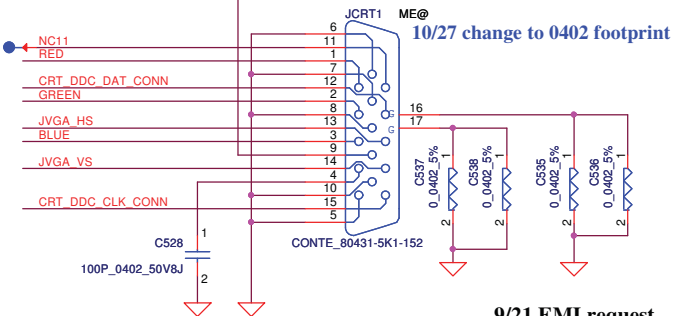
VGA LCD/PANEL BD. Conn.



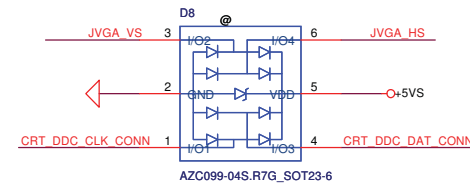
Security Classification	Compal Secret Data			Title	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	LA-7983P
				Rev	0.3
				Date:	Thursday, January 05, 2012
				Sheet	33 of 60



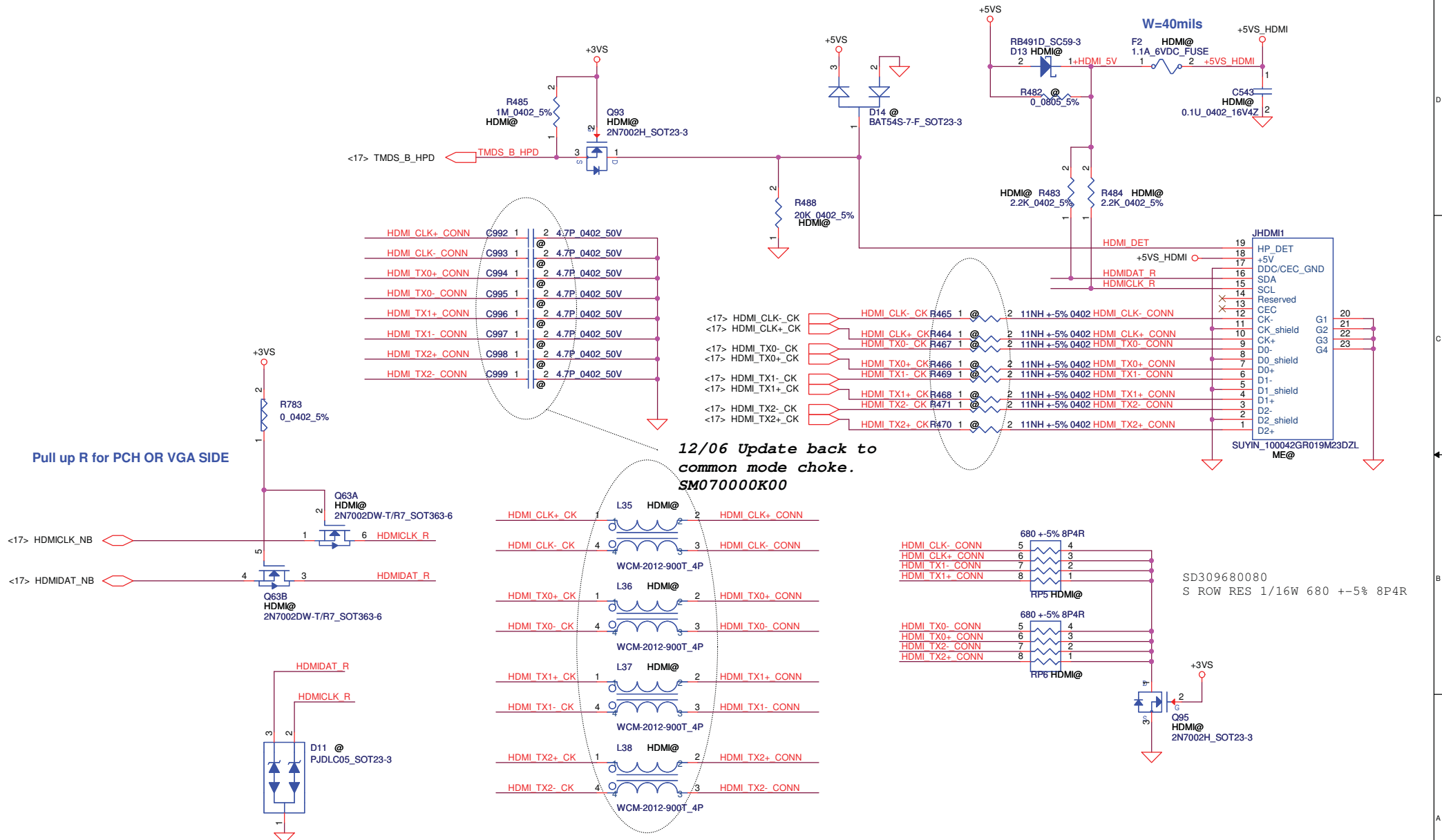
PAD T66



9/21 EMI request
0ohm and mount

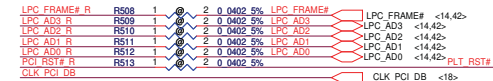


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				CRT Connector	
Size	Custom	Document Number	LA-7983P	Rev	0.3
Date:	Thursday, January 05, 2012	Sheet	34	of	60



Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	HDMI CONN
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Rev	0.3
				Date	Thursday, January 05, 2012
				Sheet	35 of 60

Mini-Express Card(WLAN/WiMAX)

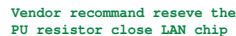


GCLK 27MHZ RG5 1 2 0 0 0402 5%

GCLK LAN 25MHZ RG6 1 2 0 0 0402 5%

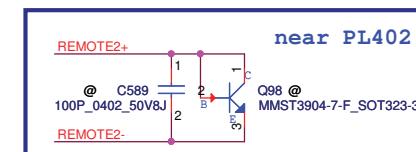
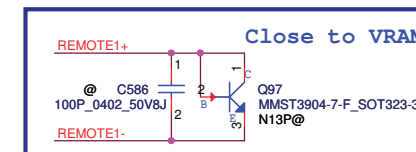
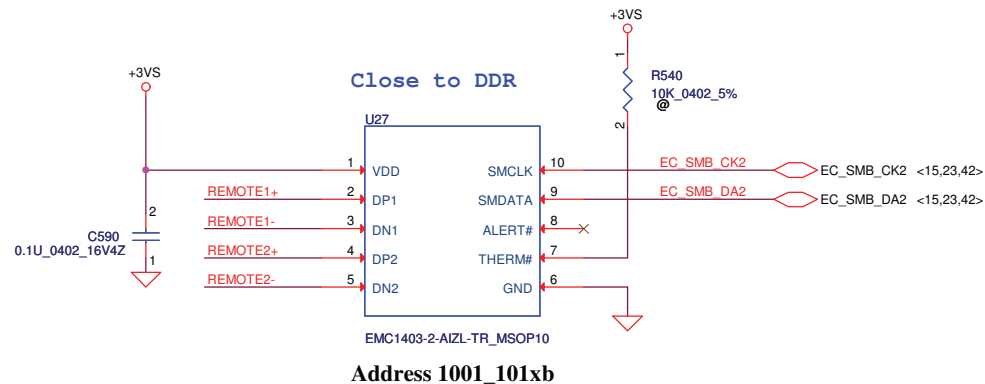
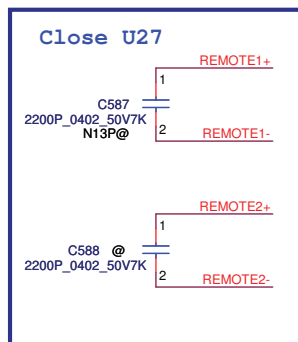
GCLK PCH 25MHZ RG7 1 2 0 0 0402 5%

+3VALW +3V_LAN

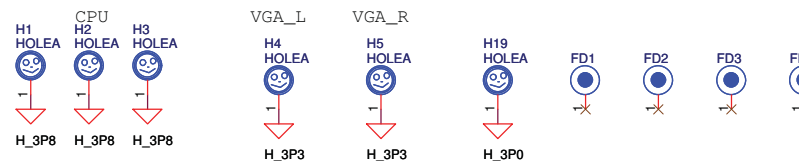


12/29, Y6 changes to SJ10000E800
S CRYSTAL 25MHZ 10PF +-20PPM 7V25000014

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



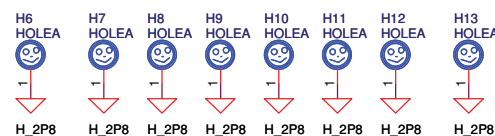
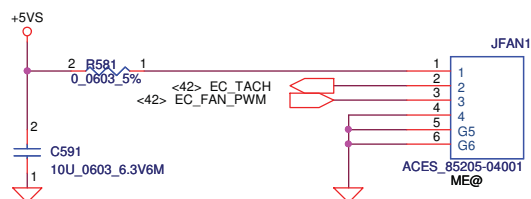
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



A

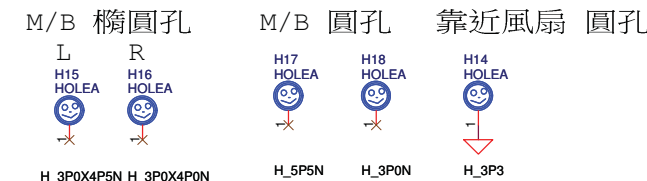
C

FAN1 Conn



B

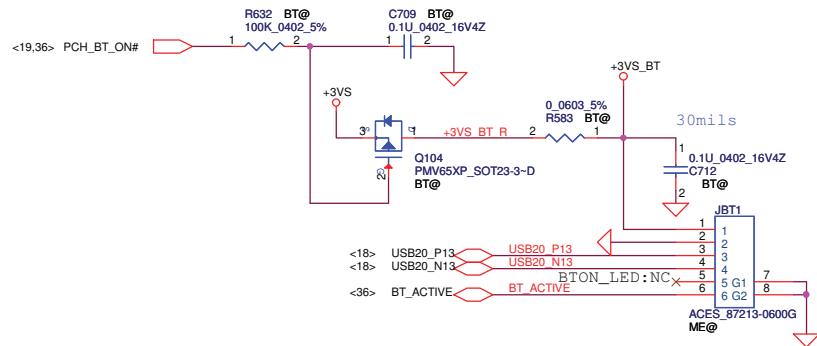
2P8 * 8pcs



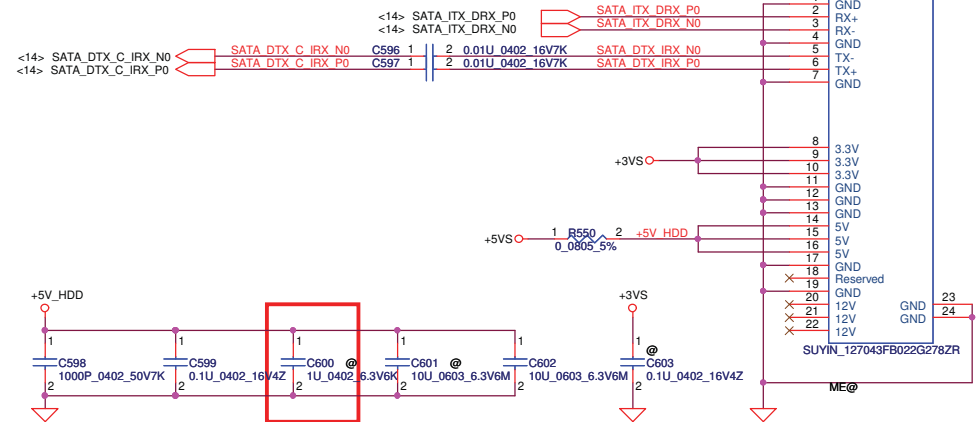
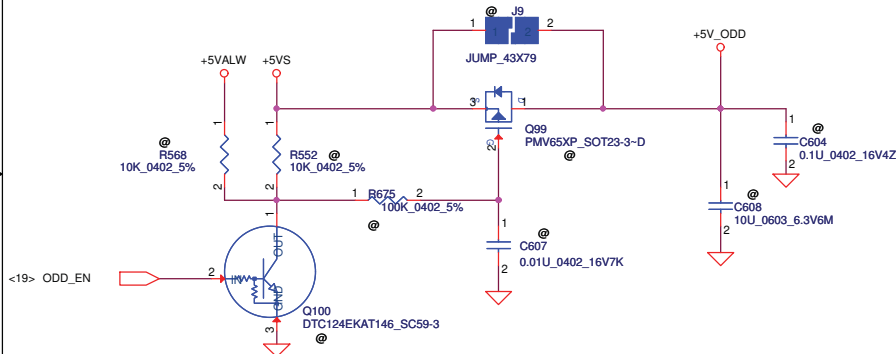
E

Security Classification	Compal Secret Data			Compal Electronics, Ltd.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	Fintek-Thermal IC/FAN/screw
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-7983P
				Date: Thursday, January 05, 2012	Sheet 39 of 60

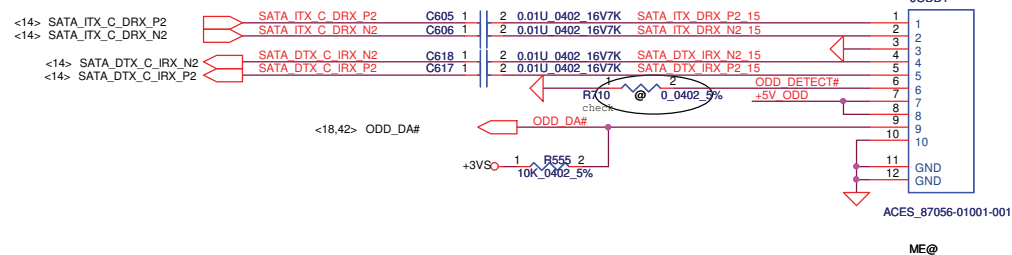
BT MODULE CONN



ODD Power Control

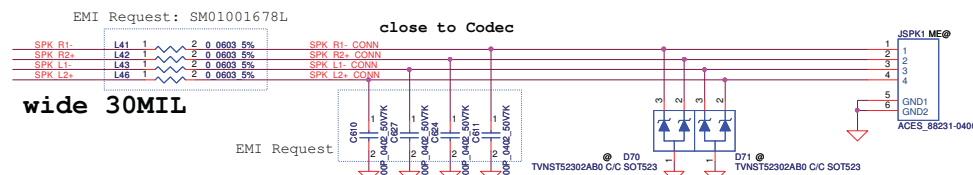
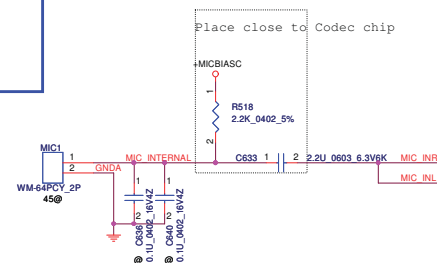
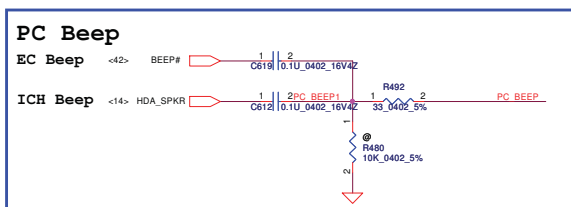
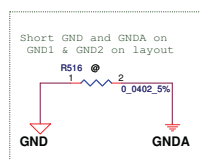
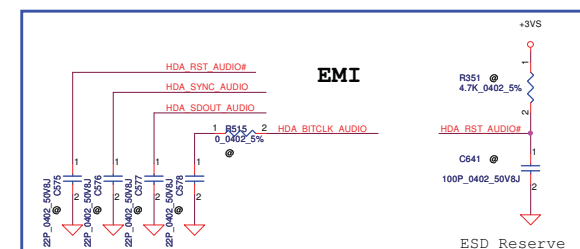
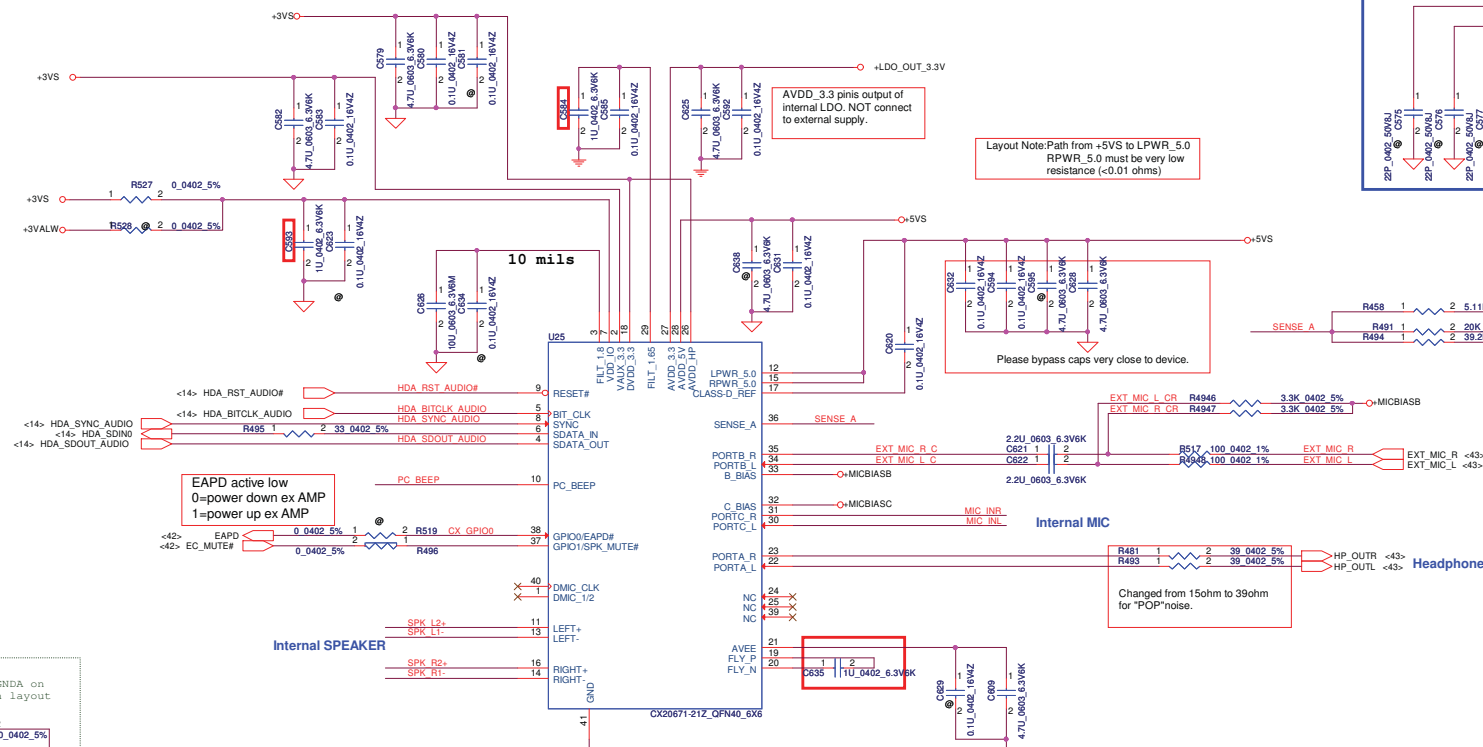


SATA ODD FFC Conn.



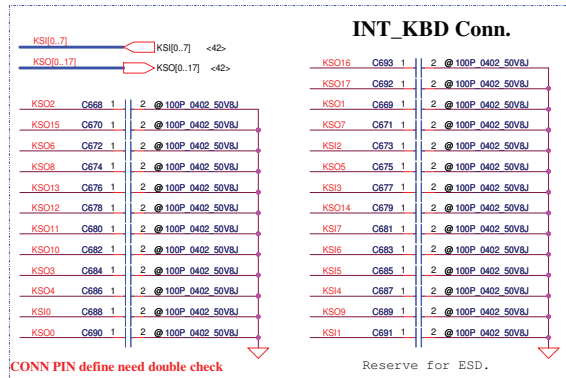
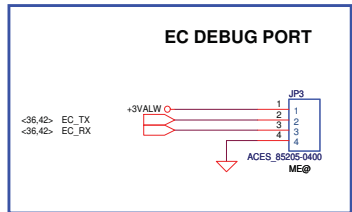
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title HDD/ODD/BT Connector		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	LA-7983P	0.3
Date:				Thursday, January 05, 2012	Sheet	40 of 60

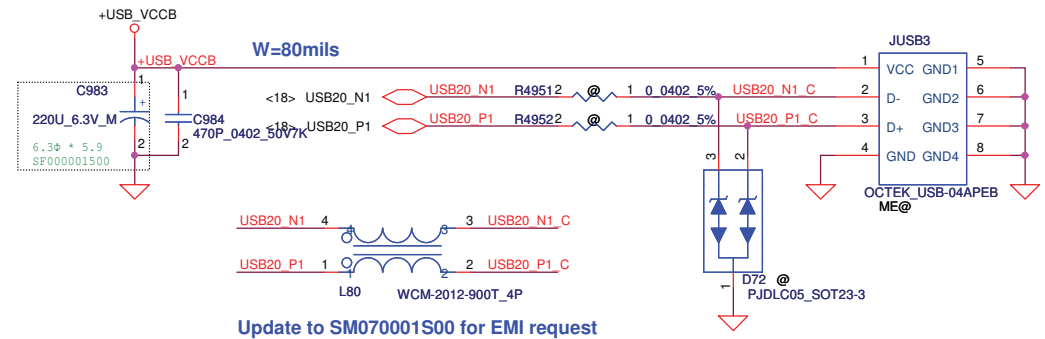
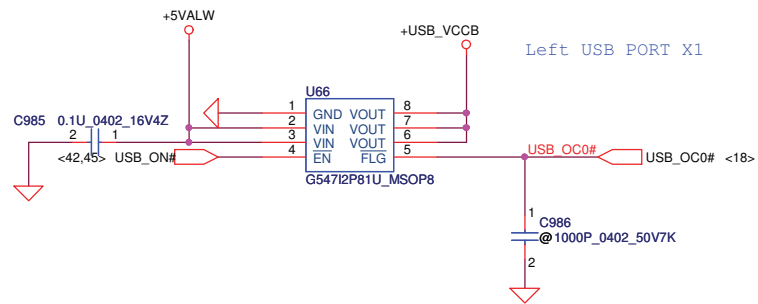
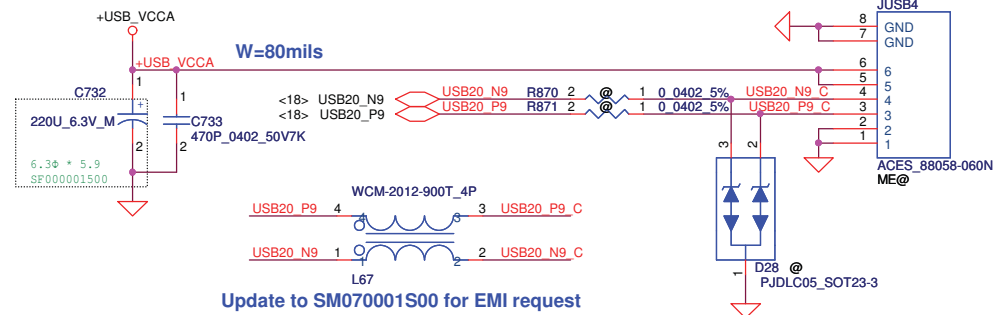
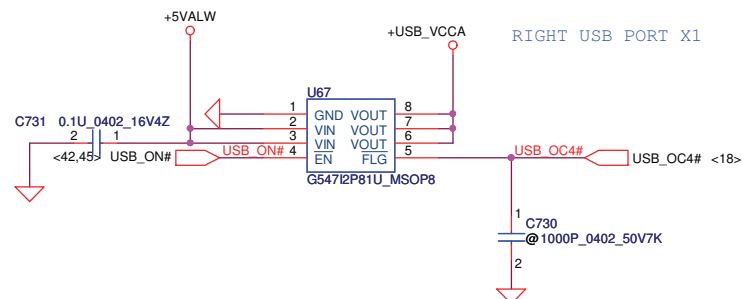
CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



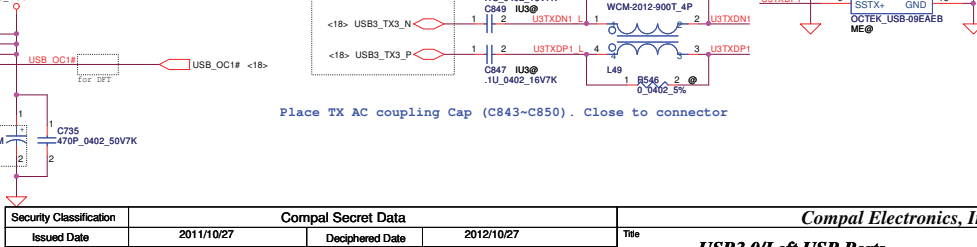
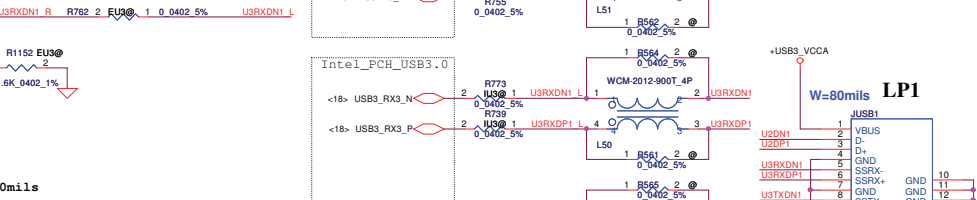
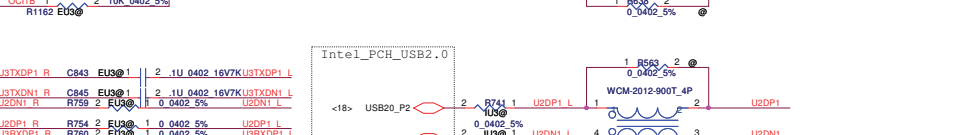
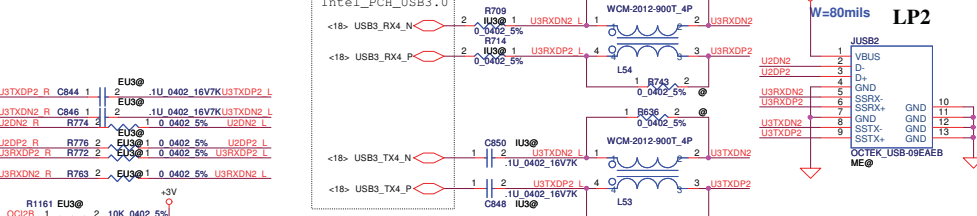
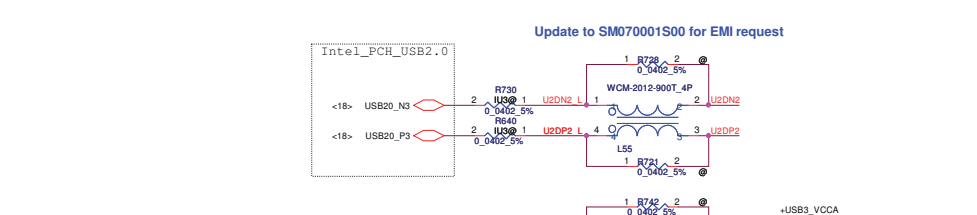
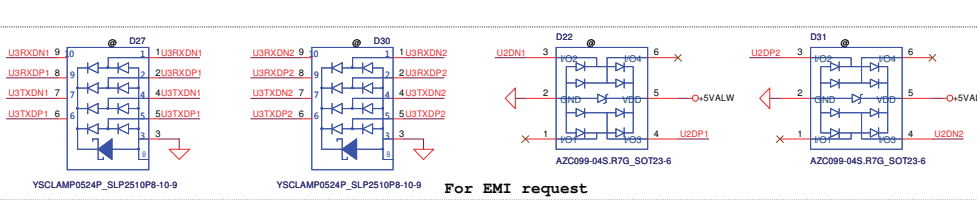
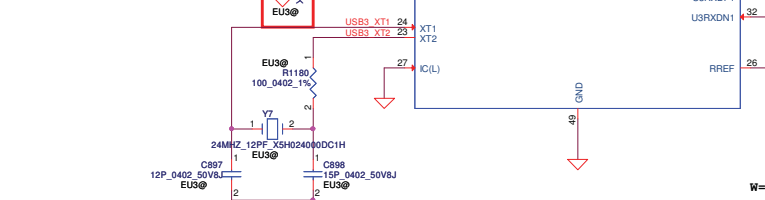
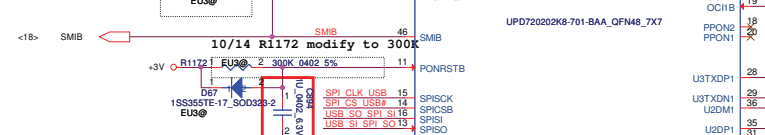
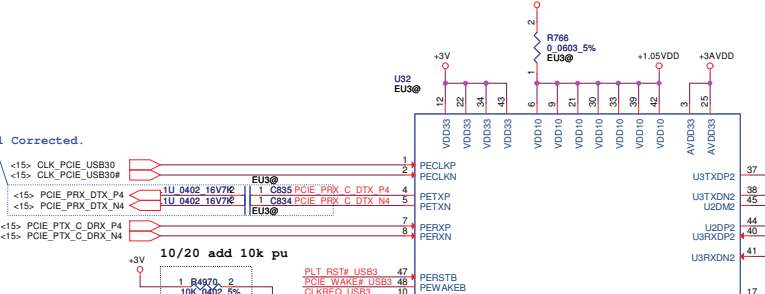
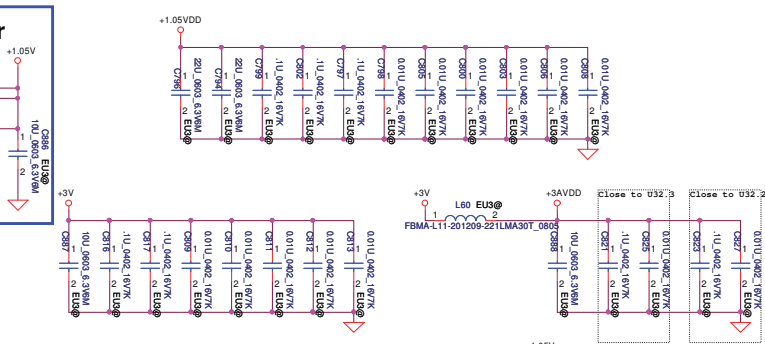
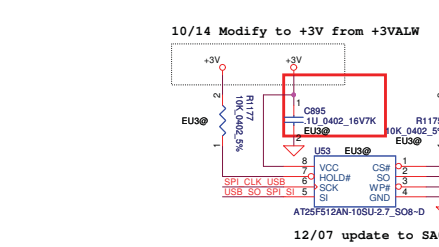
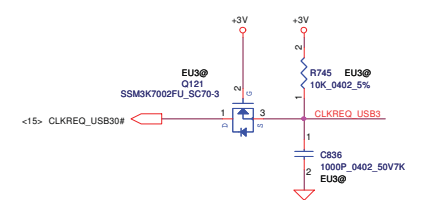
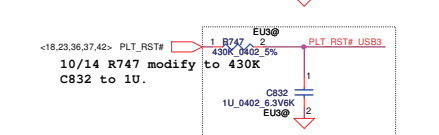
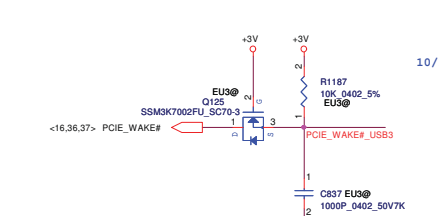
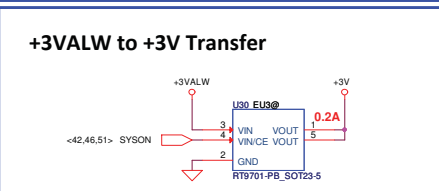
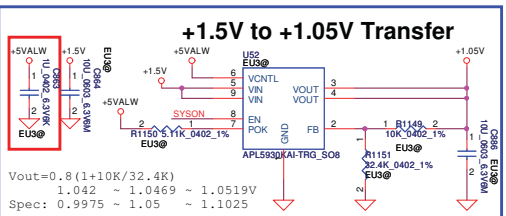
Security Classification		Compal Secret Data		Compal Electronics, Inc. Title CX20671 Codec Size C Custom Document Number LA-7983P Date: Thursday, January 05, 2012			Rev 0.5
Issued Date	2011/10/27	Deciphered Date	2012/10/27				
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.							
				Sheet 41 of 60			





Left Ext.USB Conn.**Right Ext.USB Cable Conn.**

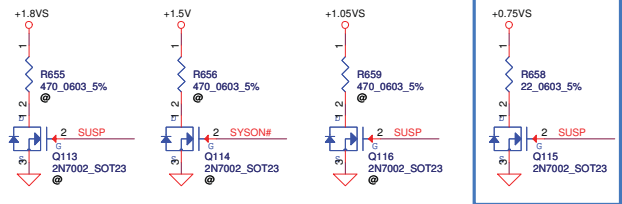
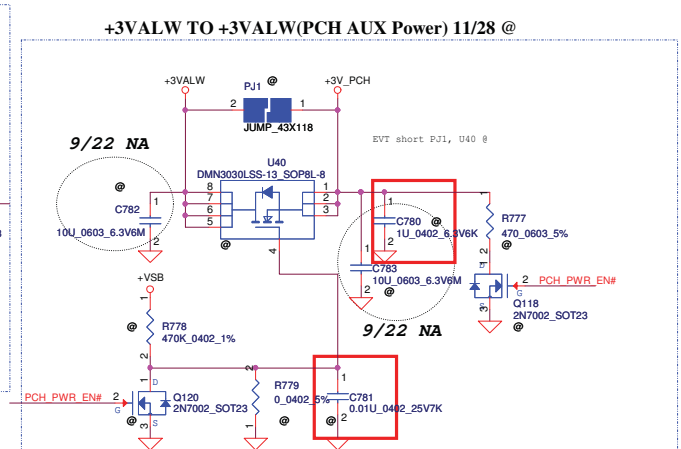
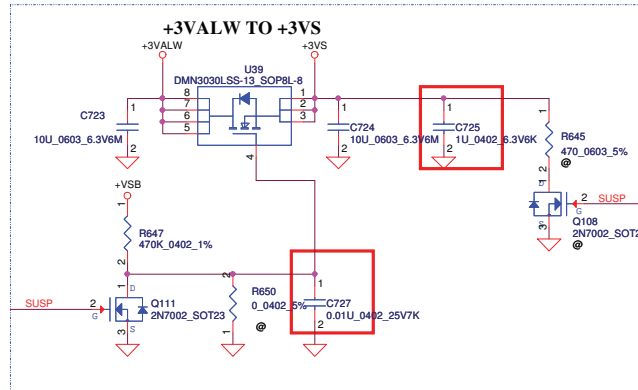
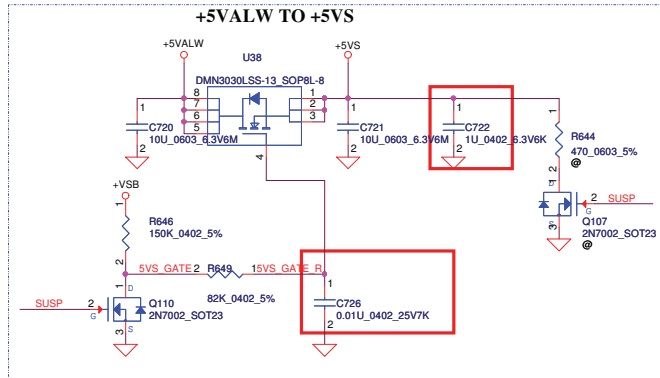
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	USB ext. ports	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size B	Document Number	Rev 0.3
				LA-7983P		
Date: Thursday, January 05, 2012				Sheet	44	of 60



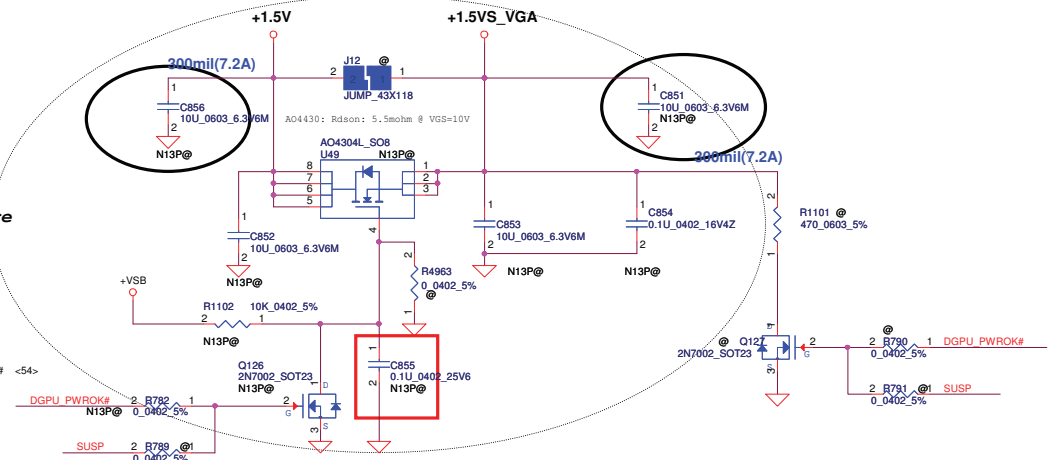
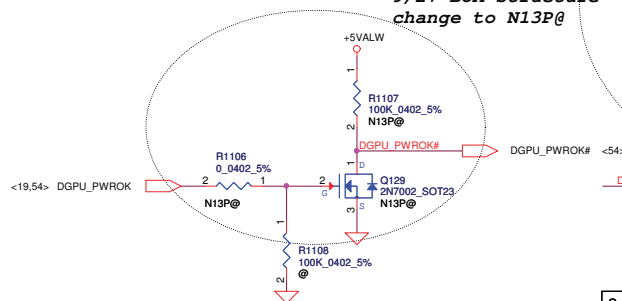
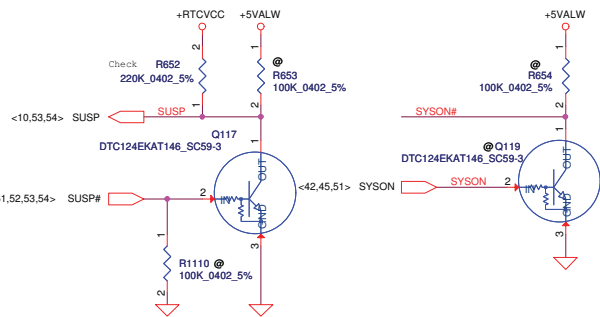
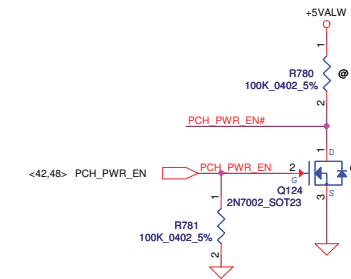
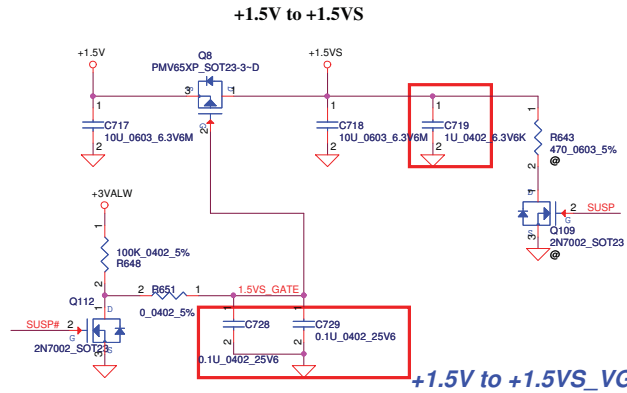
Security Classification	Compal Secret Data	Deciphered Date	2012/10/27
Issued Date	2011/10/27	Deciphered Date	2012/10/27

Size	Document Number	Rev
Custom	USB3.0/Left USB Ports	0.3

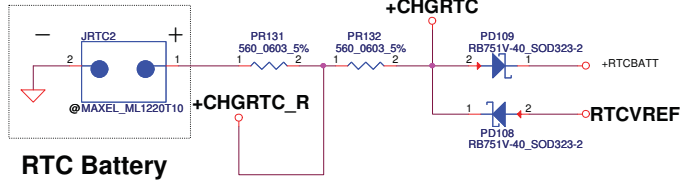
Date	Thursday, January 05, 2012	Sheet	45	of	60
------	----------------------------	-------	----	----	----

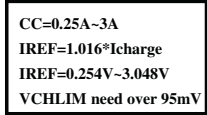


For Intel S3 Power Reduction.



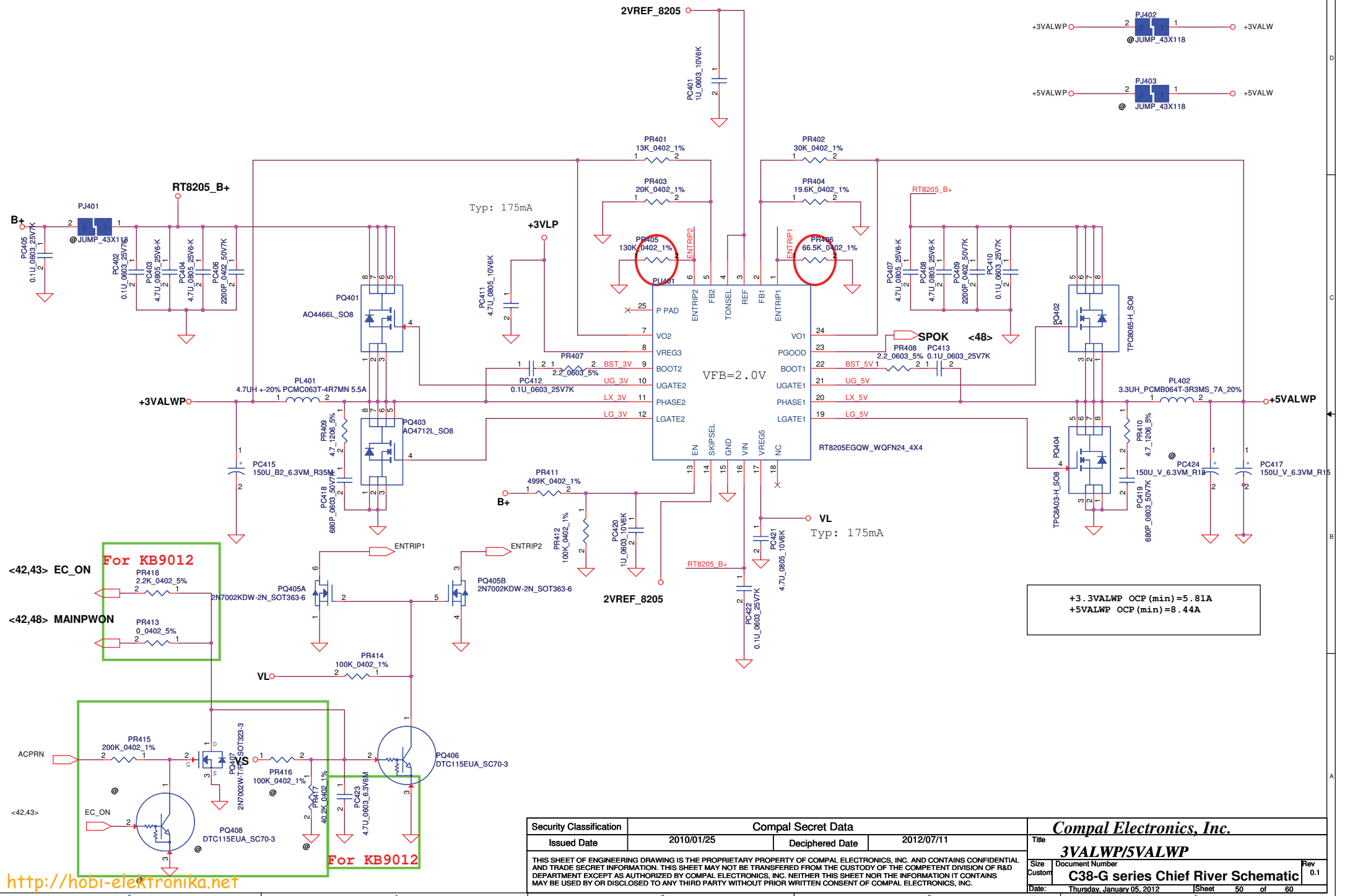
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	DC Interface	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	LA-7983P
				Date	Thursday, January 05, 2012
				Sheet	46 of 60
				Rev	0.3



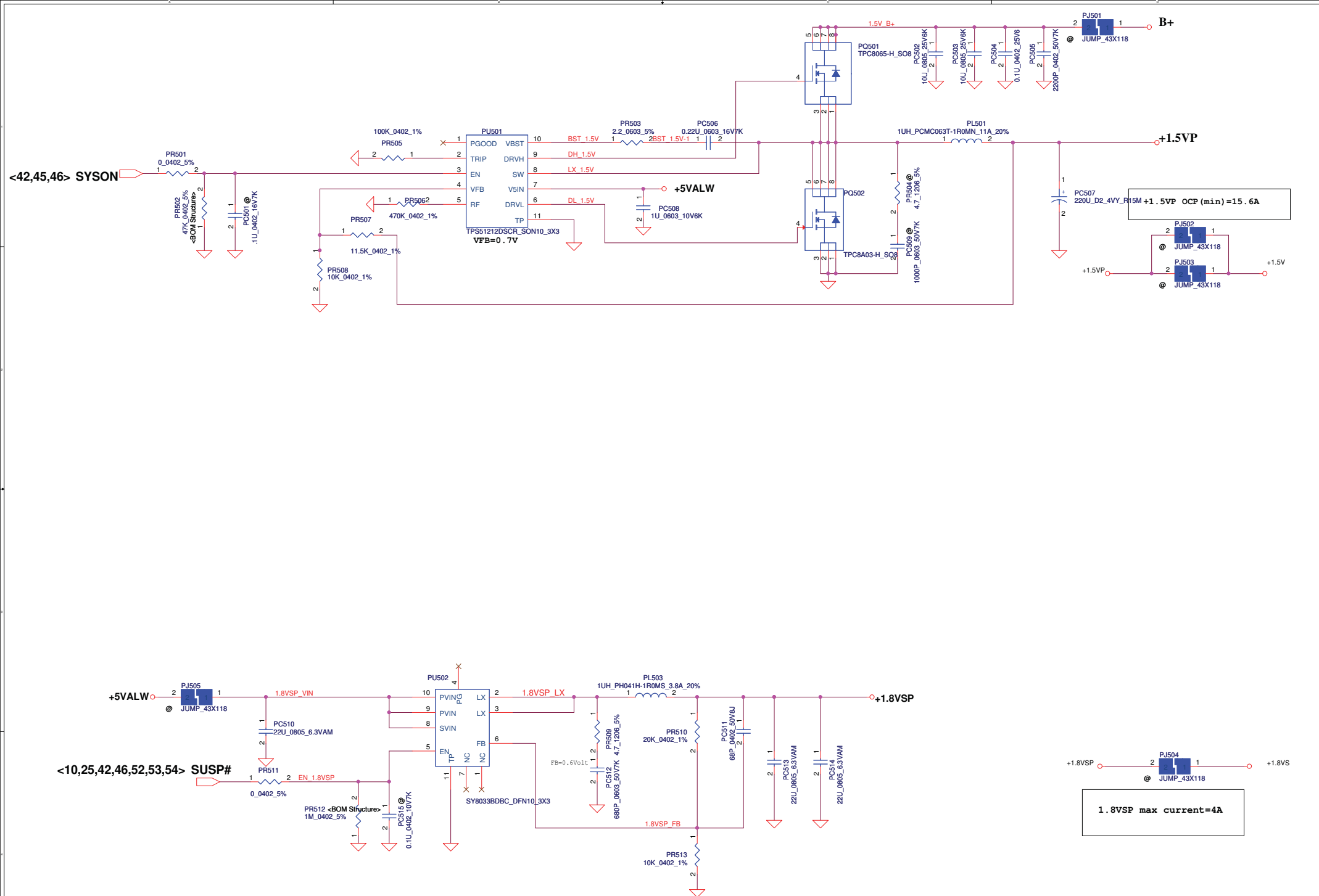


<http://hobi-elektronika.net>

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



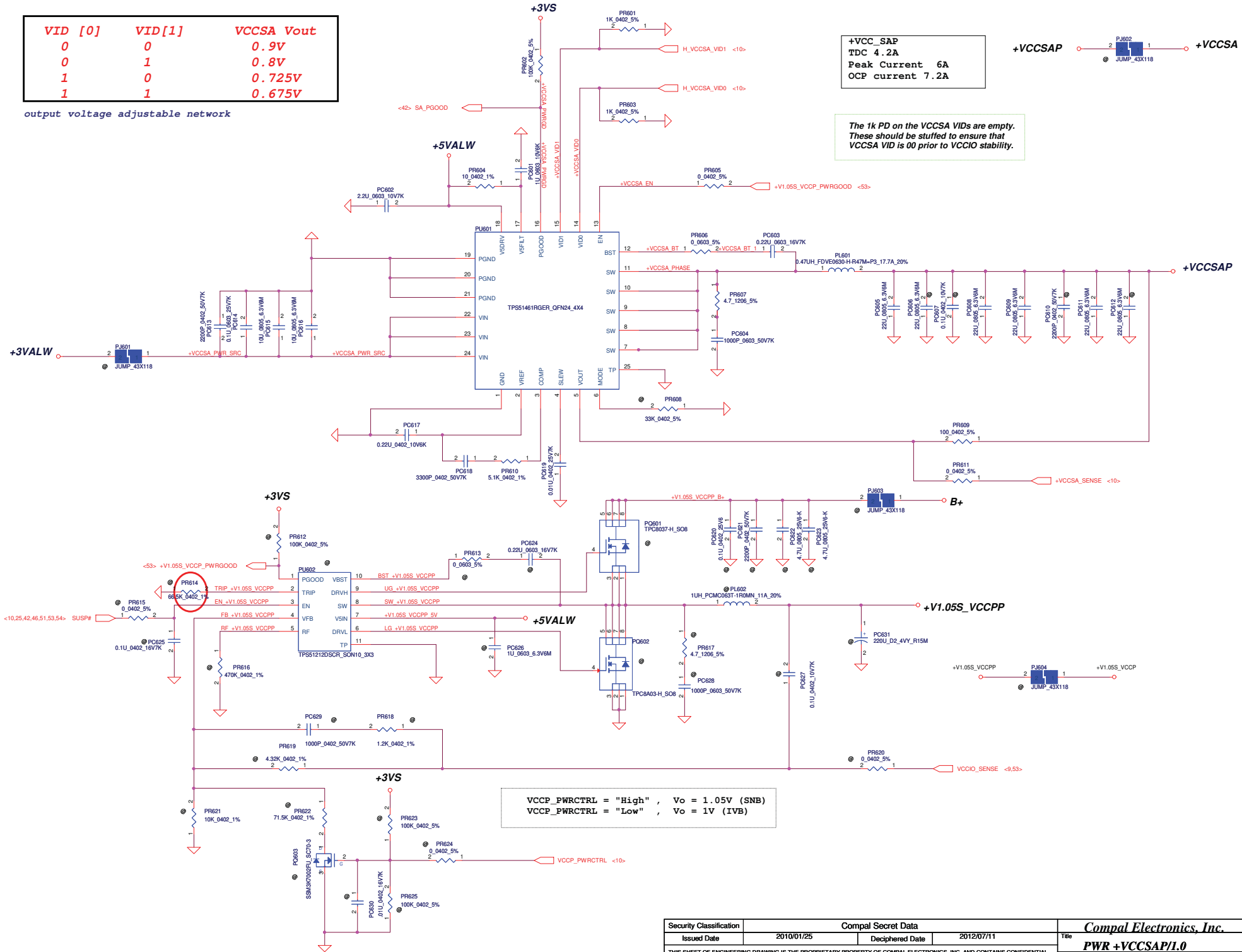
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2012/07/11	Title	3VALWP/5VALWP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number C38-G series Chief River Schematic
				Date	Thursday, January 05, 2012
				Sheet	50 of 60

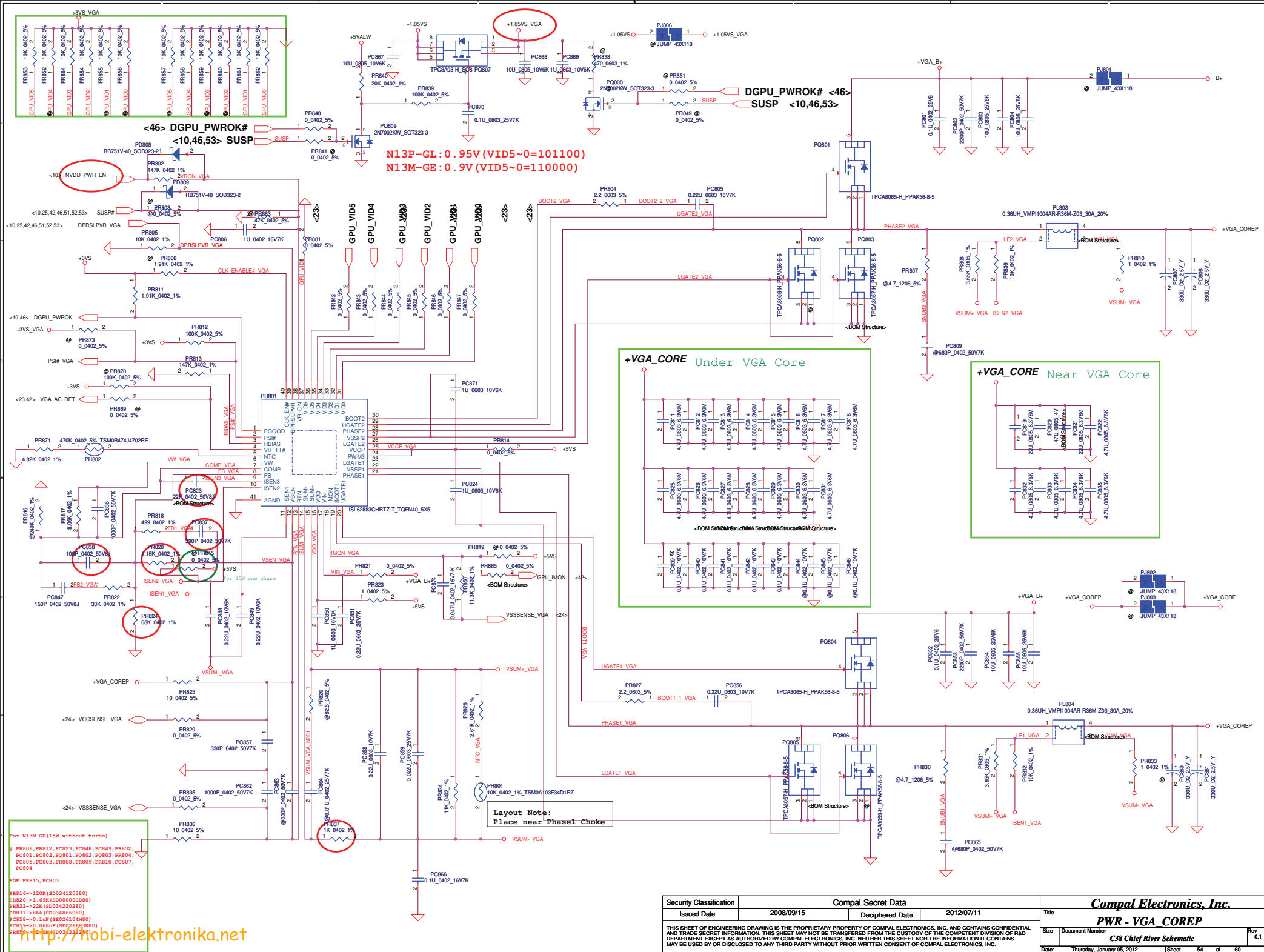


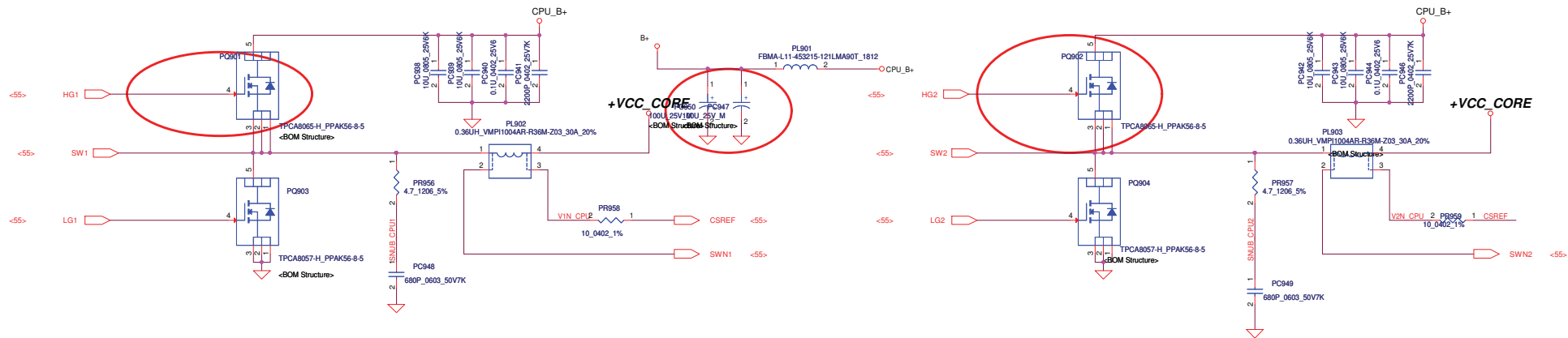
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2012/07/11	Title	PWR-+1.5VP/+1.8VSP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	C38-G series Chief River Schematic
				Date	Thursday, January 05, 2012
				Sheet	51 of 60
				Rev	0.1

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

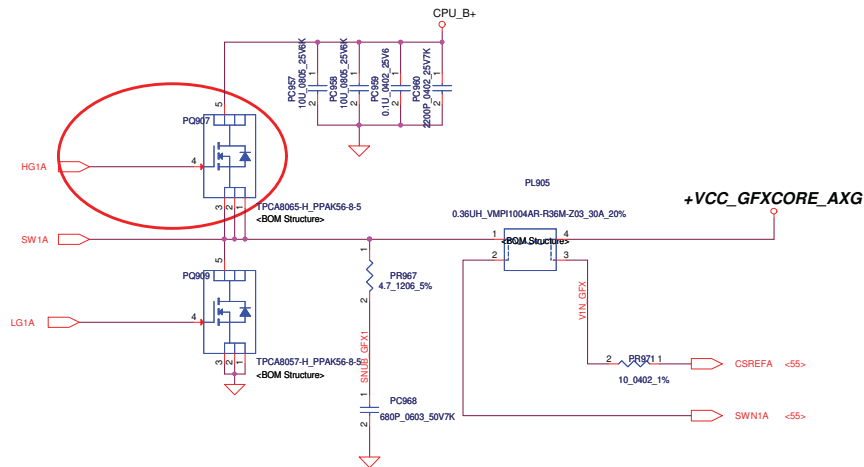






QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP-110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP-65A

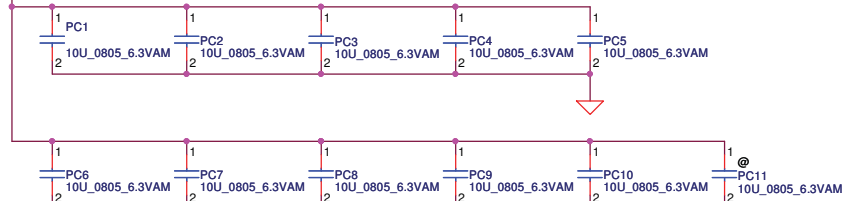


QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP-55A

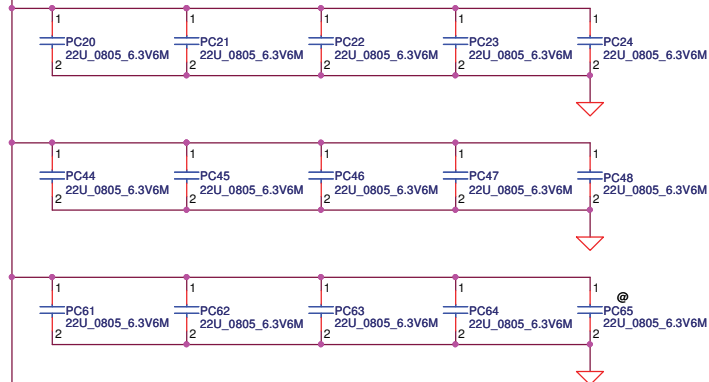
DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP-40A

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/12/01	Deciphered Date	2012/07/11	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PWR-CPU CORE	
Size	Document Number	C38-G series Chief River Schematic		Rev	0.1
Date	Thursday, January 05, 2012	Sheet	56	of	60

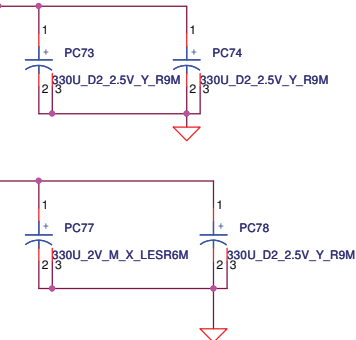
+VCC_CORE



+VCC_CORE



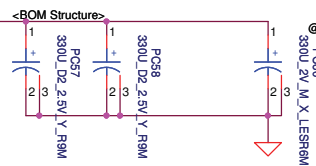
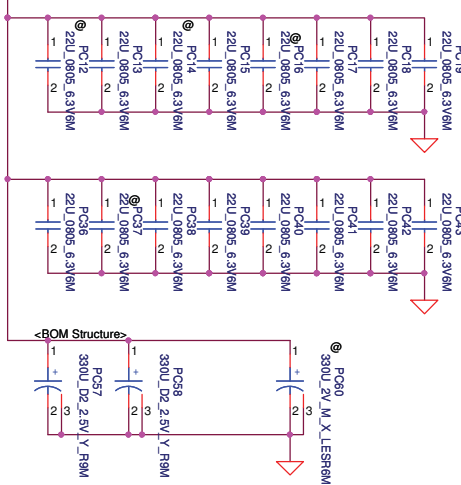
+VCC_CORE



+VCC_CORE

+VCC_GFXCORE_AXG

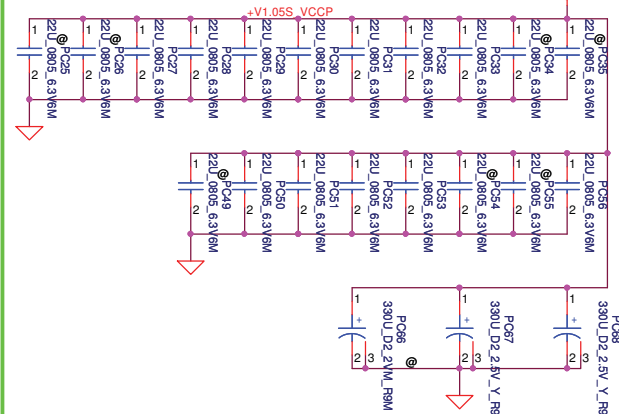
+VCC_GFXCORE_AXG



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+V1.05S_VCCP



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2012/07/11	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PWR - PROCESSOR DECOUPLING
C38-G series Chief River Schematic				Rev 0.1
Date: Thursday, January 05, 2012				Sheet 57 of 60

Version change list (P.I.R. List)

Page 1 of 1
for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	To facilitate EA test	P54	Change net name of pin 1 of PR825 from +VGA_CORE to +VGA_COREP	2011/10/19	DVT
2	Sense VSSIO_SENSE_L net close to IC	P53	Add PR718	2011/10/19	DVT
3	CPU controller compensation RC tuning	P55	Change PC904, PC907, PC908, PC909, PC926, PC928, PR929, PC936 and PR943	2011/10/19	DVT
4	EMI request	P51	Change PR503	2011/10/19	DVT
5	Back to Back MOS change	P49	Change PQ302	2011/12/06	PVT
6	Sense VSSIO_SENSE_L change according to FAE	P53	Add PR719 and PC721. Change PR718 and PR714	2011/12/06	PVT
7	Add IC G718	P48	Change PR205 to 4.42k (90W) and PR210 to 27.4k (90W)	2011/12/06	PVT
8	EC_ON RC change	P50	Change PR418 from 10k to 2.2k	2011/12/06	PVT
9	Unpop PR224 and add PR231 by HW request	P48	Unpop PR224 and add PR231	2011/12/21	PVT
10	Change CPU&GFX compensation RC by FAE recommendation	P55	PR902, PR903, PR947, PR948, PC901, PC905, PC929, PC930 and PC933	2011/12/21	PVT
11	Change charger's choke from 4.7u to 10u	P49	PL302	2011/12/21	PVT
12					
13					
14					
15					
16					
17					

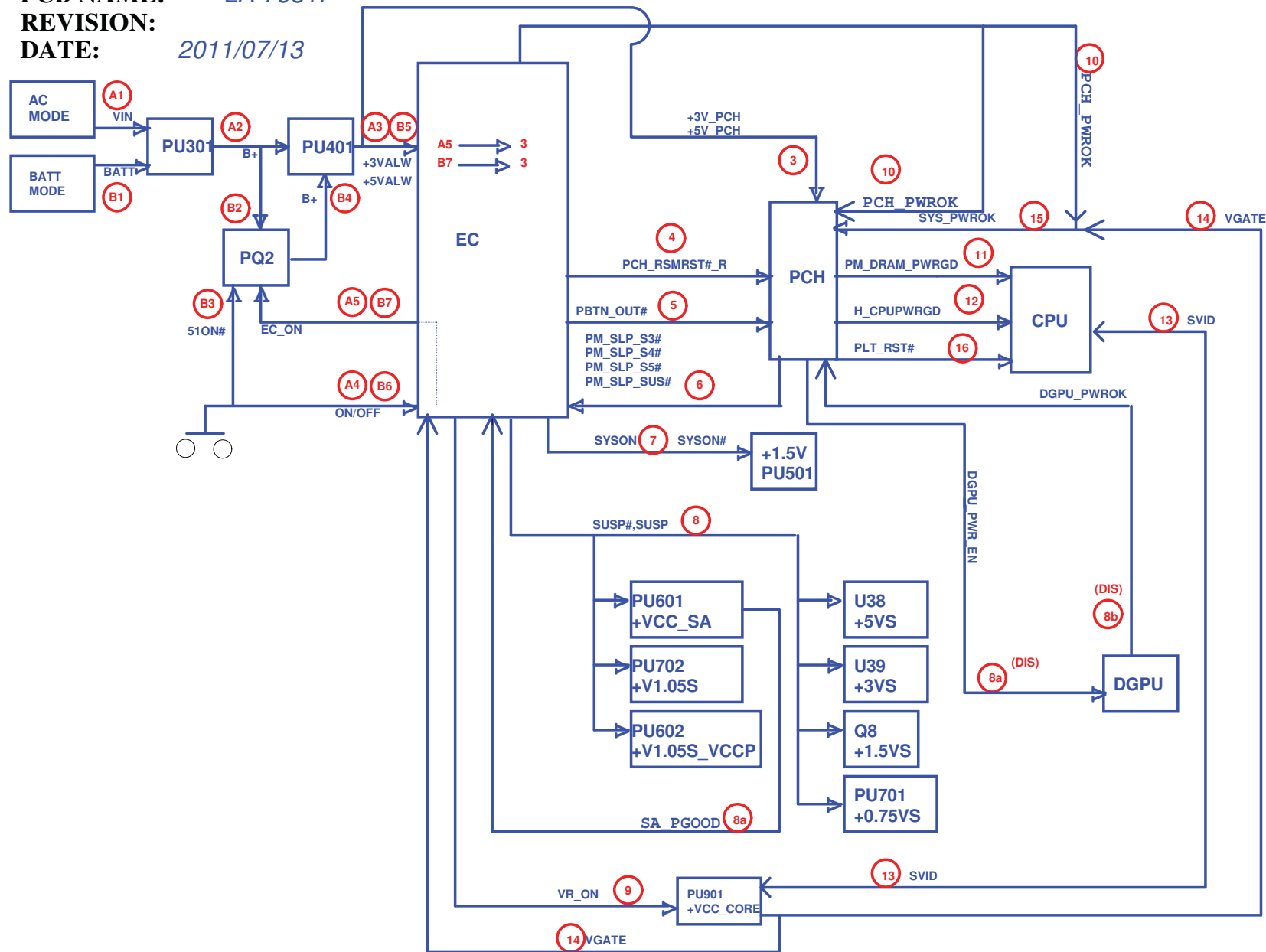
COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*

PCB NAME: *LA-7981P*

REVISION:

DATE: *2011/07/13*



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Title	Power sequence
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIELD DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-7983P
				Date	Thursday, January 05, 2012
				Sheet	59 of 60
				Rev	0.3

Version change list (P.I.R. List)

Page 1 of 1
for HW

Item	Reason for change	PG#	Modify List	Date	Phase
1	For NVIDIA update Strapping setting.	32	RV102 change to 10K ohm	10/11	B
2	PCIE BUS corrected for external USBcontroller	45	PCIE_PRX_DTX_P4/N4 Swapped	10/11	B
3	Modify USB3.0 Controller circuit	45	R1172 to 300k, R747 to 430k, C832 to 1U	10/14	B
4	Modify USB3.0 Controller circuit	45	U53.8 to +3V, R1177.2 to +3V . Add R4970	10/14	B
5	Modify LAN function design for surge.	38	Add R4966, R4967, R4968, R4969, for 10/100 SKU	10/18	B
6		38	Modify R1443 near to LAN chip side. Delete R1448 0 ohm.	10/18	B
7		38	Modify R1443 near to LAN chip side.	10/18	B
8		38	Add CHASSIS_GND, C989, C990, C991	10/18	B
9		38	Delete R1374, R1375, R1377, DL2~DL4.	10/25	B
10	Reserve HDMI EMI solution	35	Add C992~C999	10/25	B
11	Reserve LAN ESD solution	38	Add D74, link both MCTO_1 and chassis to ground.	10/27	B
12	Change component type.	43	C987 change to 0402 type	10/27	B
13		34	C538 change to 0402 type	10/27	B
14	Reserve LAN EMI solution	38	Add R4971~R4974	10/27	B
15	Reserve MAINPWON 0ohm.	38	Add R4978	12/21	C
16	LAN Power Switch	37	Add Q130, R4977, C1001	12/21	C
17					

Security Classification		Compal Secret Data		Title	
Issued Date	2011/10/27	Deciphered Date	2012/10/27	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIELD CUSTOMER DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	
				LA-7983P	
				Rev 0.3	
				Date: Thursday, January 05, 2012	
				Sheet 60 of 60	