

LONGBEACH 10/20

LA-2371 REV

1.0 Schematic

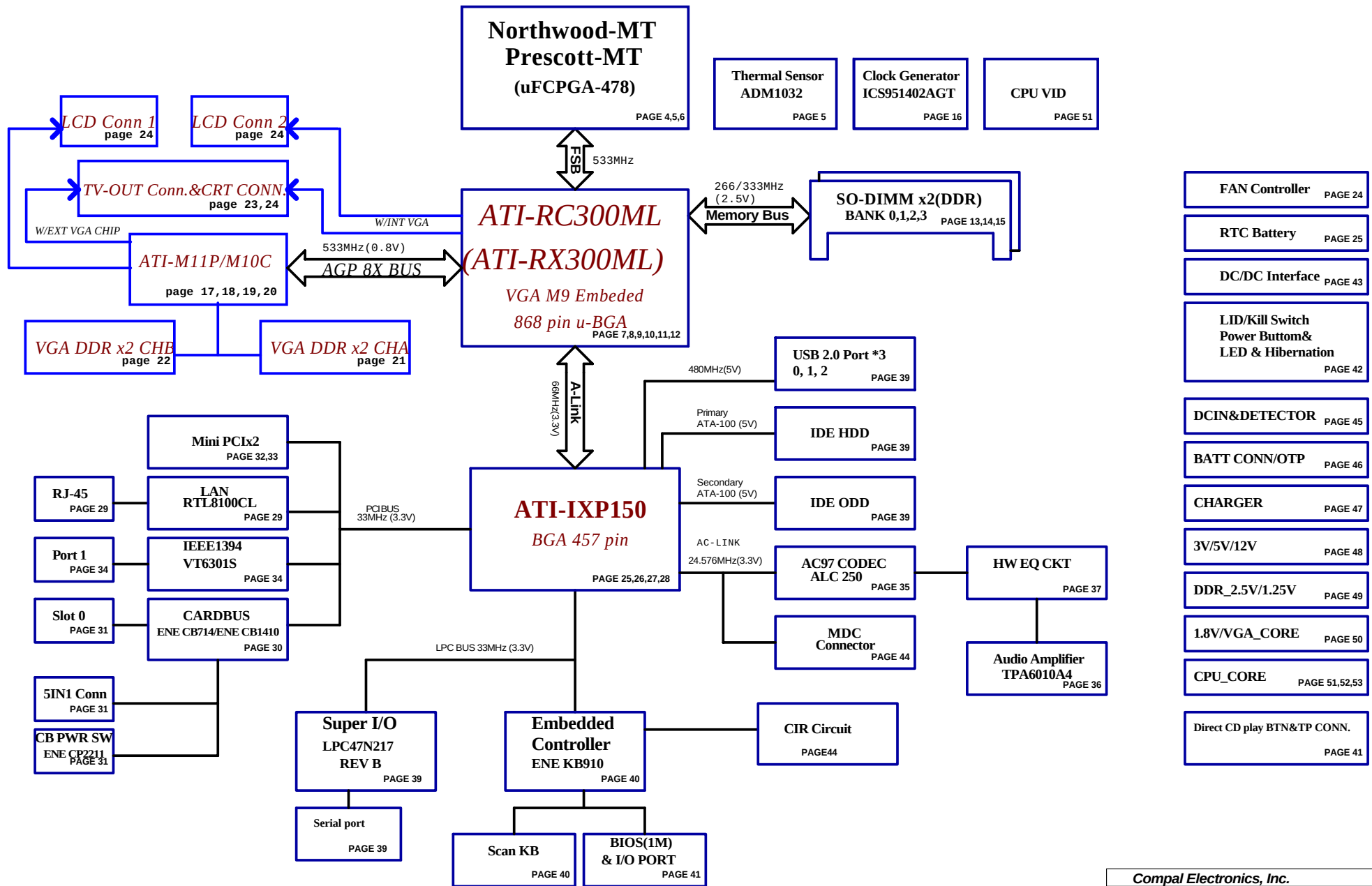
Portability Prescott/Northwood
RC300ML(RX300ML)+IXP150+ATI M11P(128MB VRAM)
2004-07-23

Compal confidential

Model Name : EFQ00 & EEQ00

File Name : LA-2371 Rev: 1.0

BLOCK DIAGRAM



Compal Electronics, Inc.

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VGA_CORE	1.0V/1.2V switched power rail for VGA chip	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 4X/8X	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+2.5VALW	2.5V always on power rail	ON	ON	ON*
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#GNT#	Interrupts
VGA	AD16		PIRQA
CardBus	AD20	2	PIRQA
LAN	AD19	3	PIRQD
Mini-PCI1	AD18	1(for Wireless Lan)	PIRQC/PIRQD
1394	AD16	0	PIRQA
5IN1	AD20	2	PIRQB
Mini-PCI2	AD22	4(for TV tuner)	PIRQC/PIRQD

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b		
(24C84)	1011 000Xb		

EC SM Bus2 address

IXP150 SM Bus address

Device	Address
Clock Generator (1CS951482A6T)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 001Xb

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

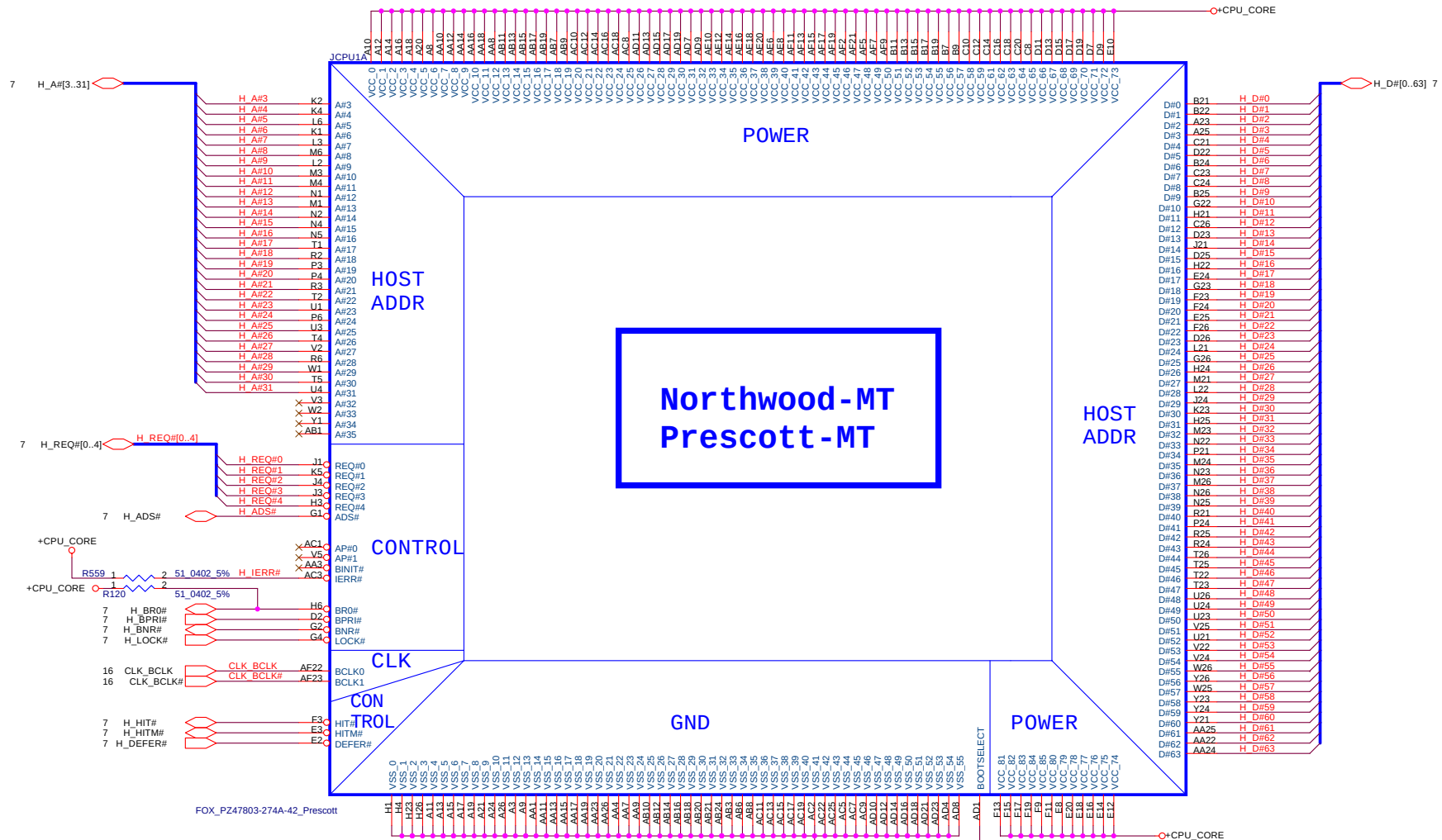
Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

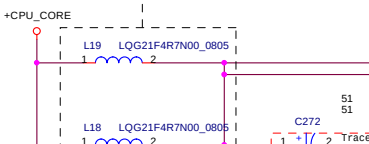
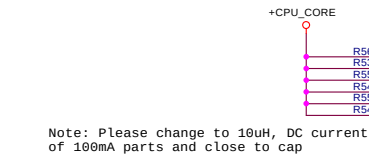
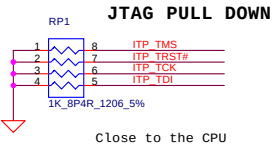
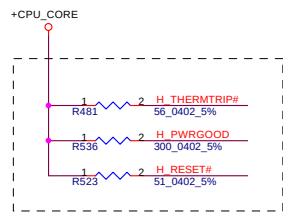
SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BIOS_ID: H EFW00
L EEW00



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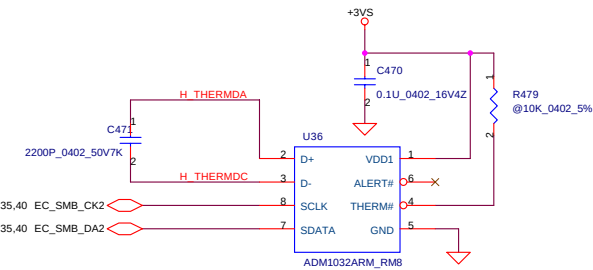


PLL Layout note :

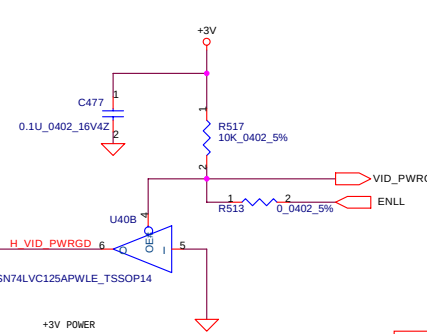
- Place cap within 600 mils of the VCCA and VSSA pins.
- H_VCCIOPLL, HVCCA, HVSSA trace wide 12 mils(min)



Thermal Sensor

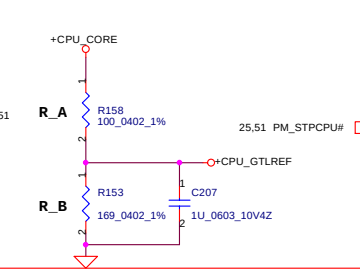


VID PWRGD Circuit

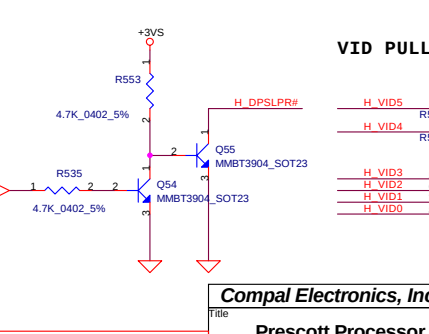


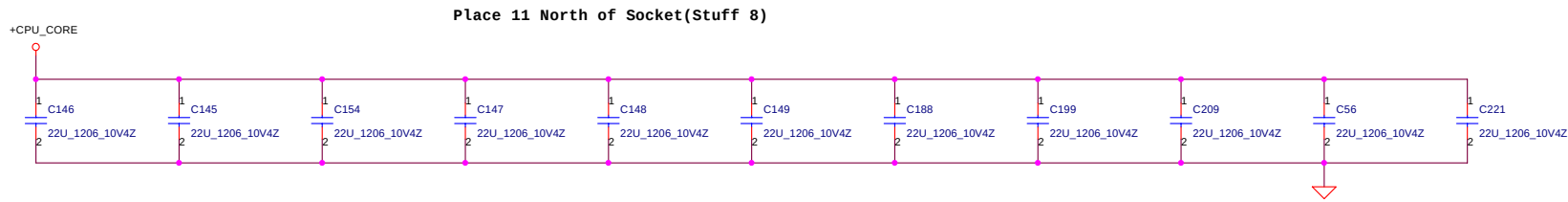
GTL Reference Voltage

- Layout note :
- Place R_A and R_B near CPU (Within 1.5").
 - +CPU_GTLREF Trace wide 12mils(min), Space 15mils

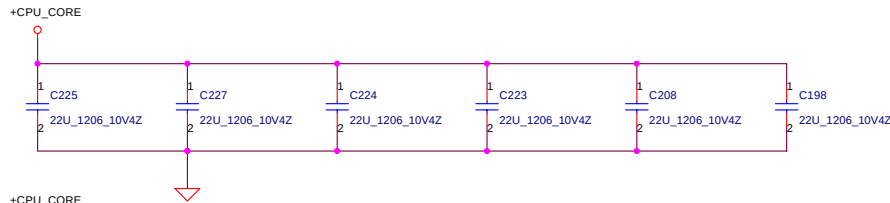
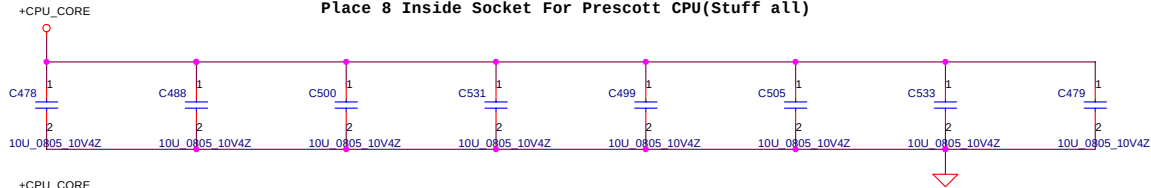


VID PULL HIGH



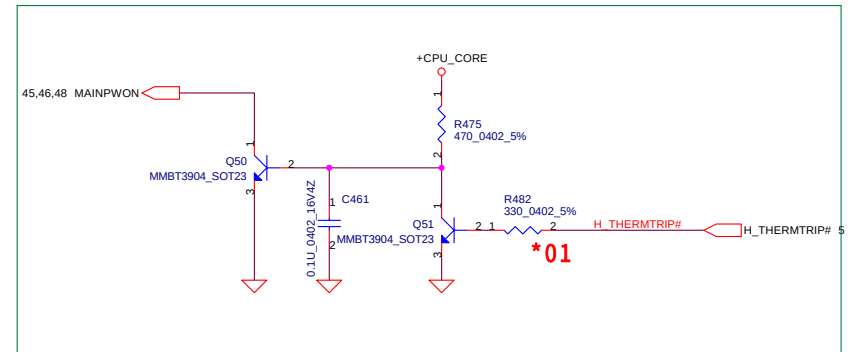
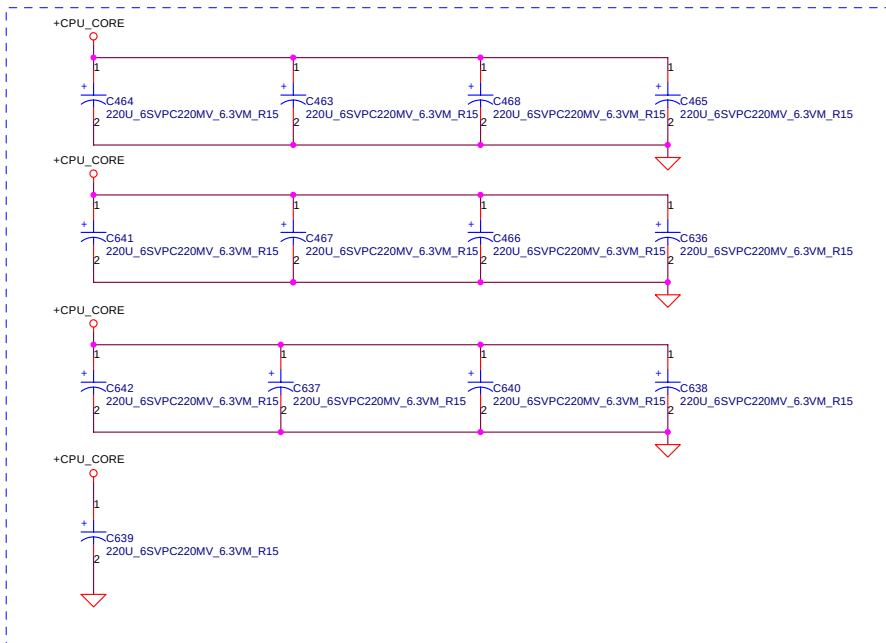


22uF depop reference
Springdale Customer Schematic R1.2 page82



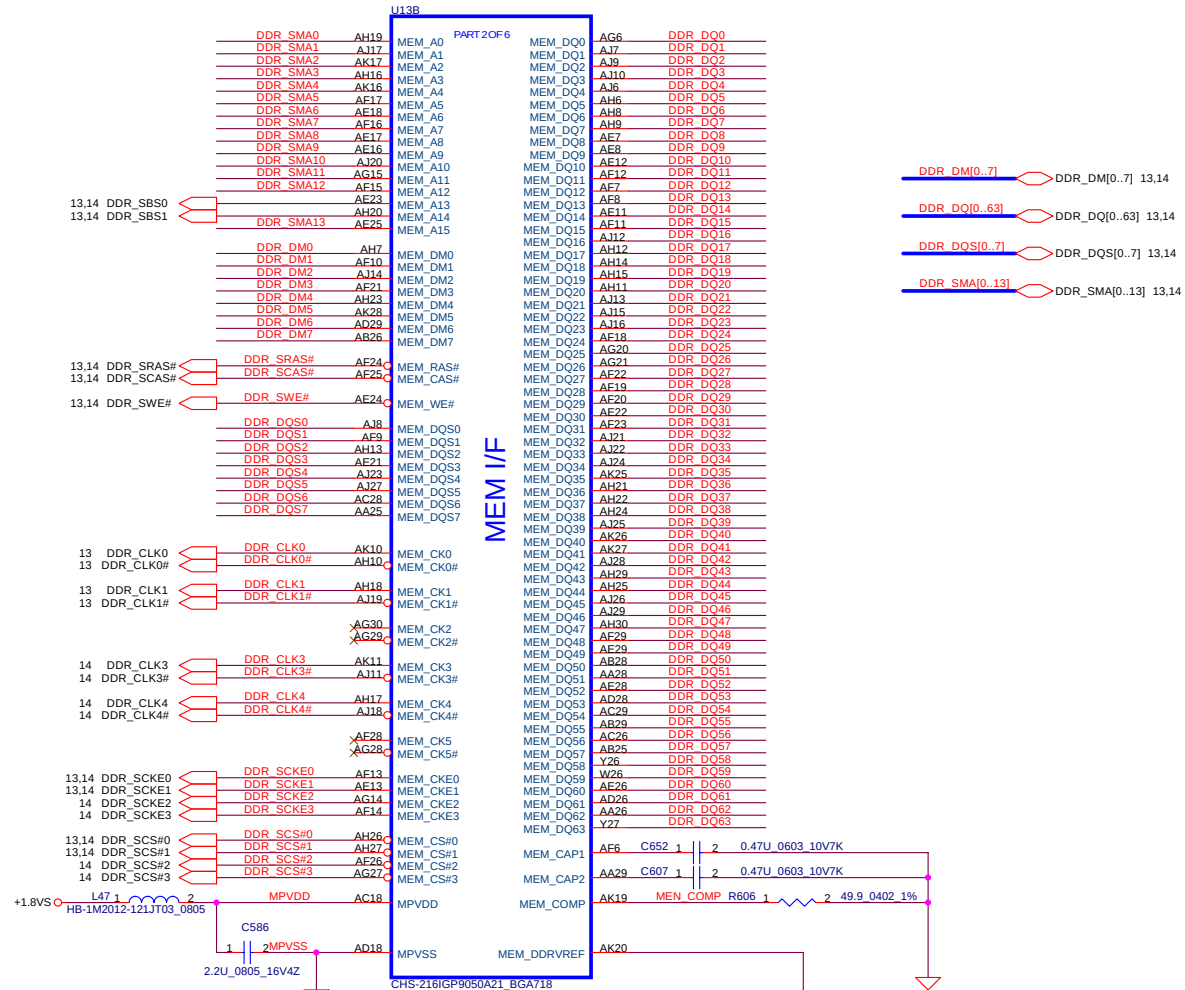
Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11
(12474)page239

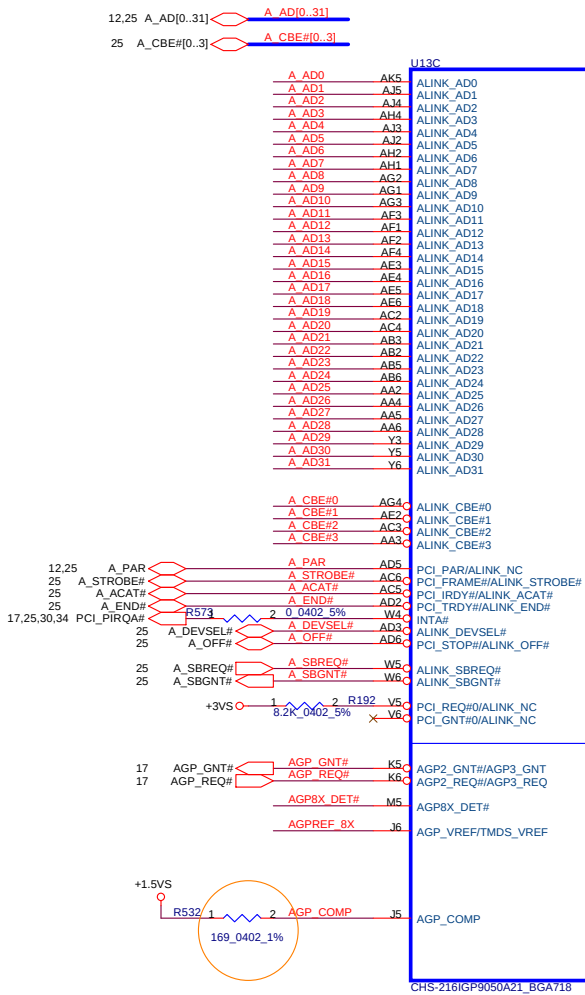
Decoupling Reference Requirement:
560uF Polymer, ESR:5m ohm(each) * 10
22uF X5R * 32



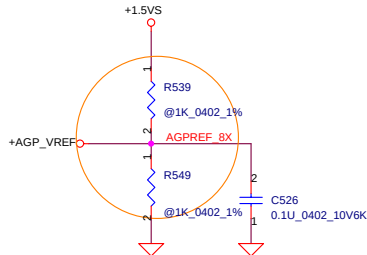
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Title		CPU Decoupling	
Size	Document Number	Rev 1.0	
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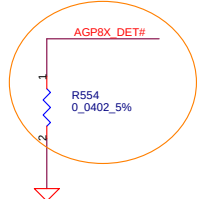




POP For EFQ00
DEPOP For EEQ00

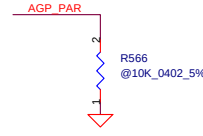
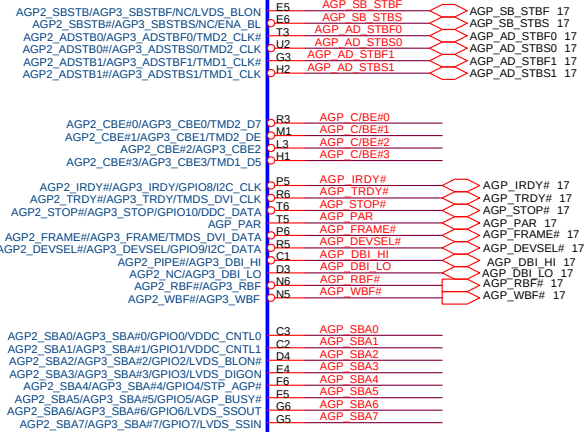


POP For EFQ00
DEPOP For EEQ00

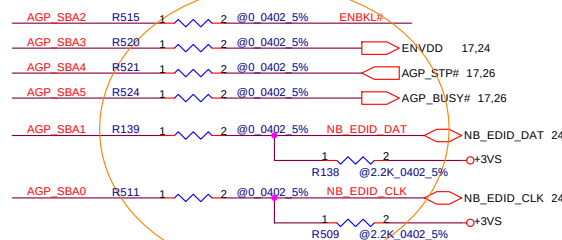


PCI Bus 0 / A-Link I/F

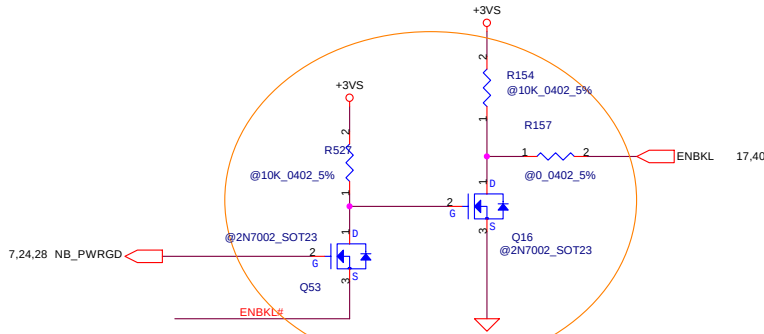
PCI BUS 1 / AGP Bus (GPIO , TMD5 , ZVPort)



POP For EFQ00
DEPOP For EFQ00

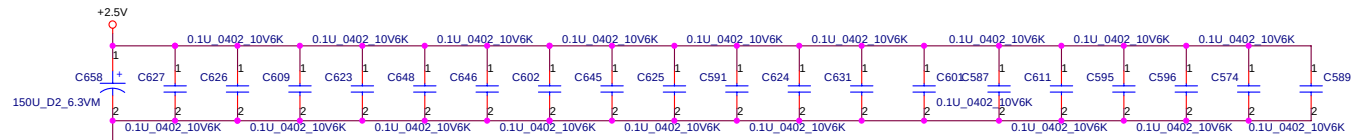
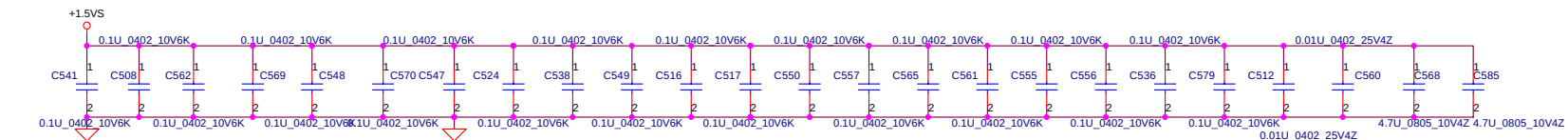
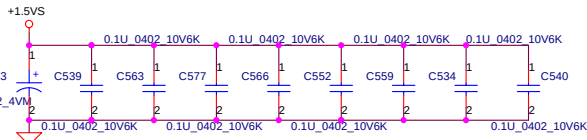
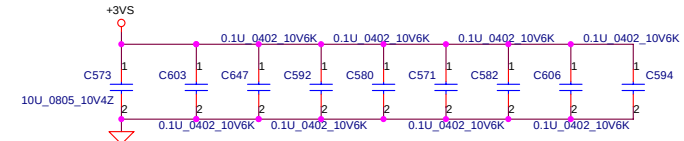
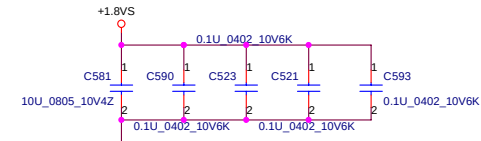
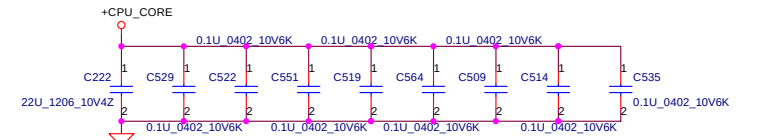
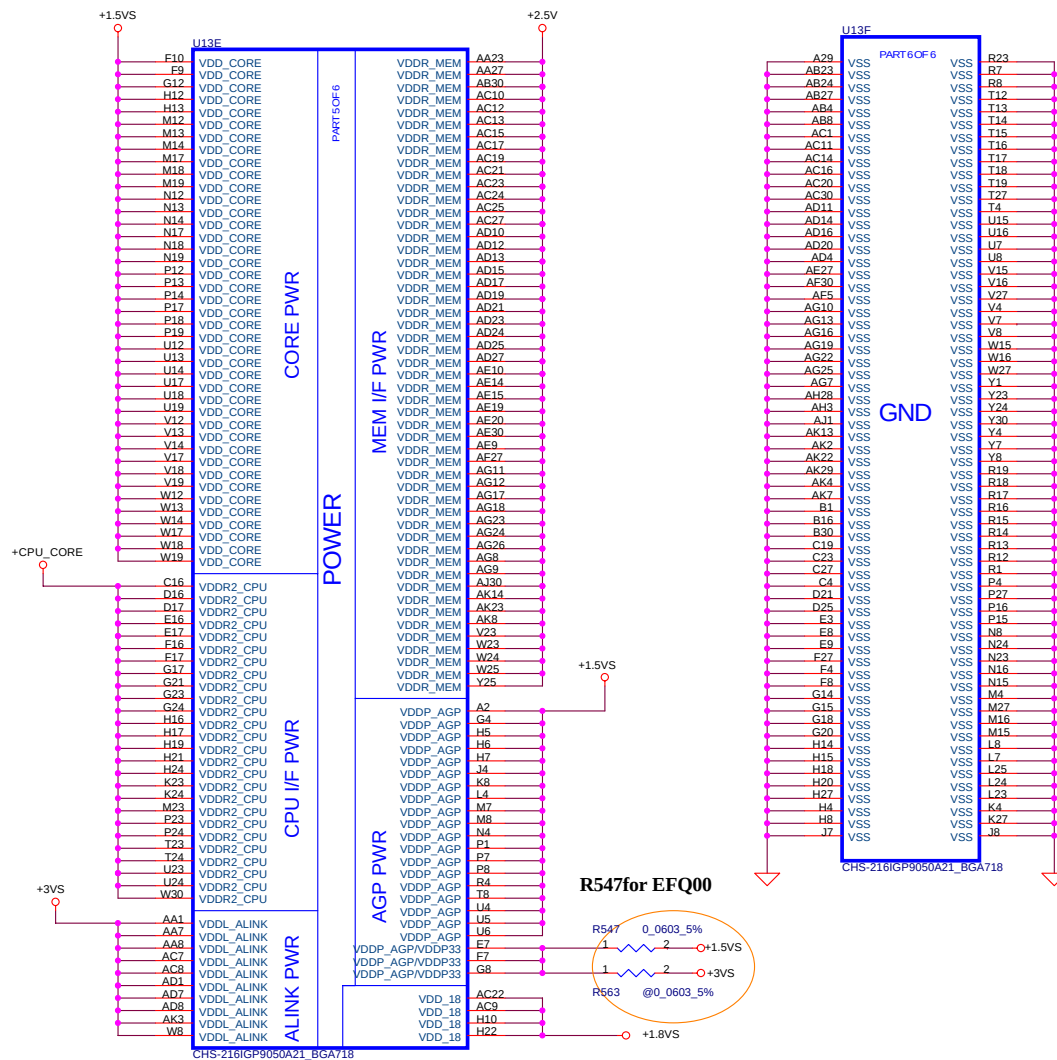


POP For EFQ00
DEPOP For EFQ00



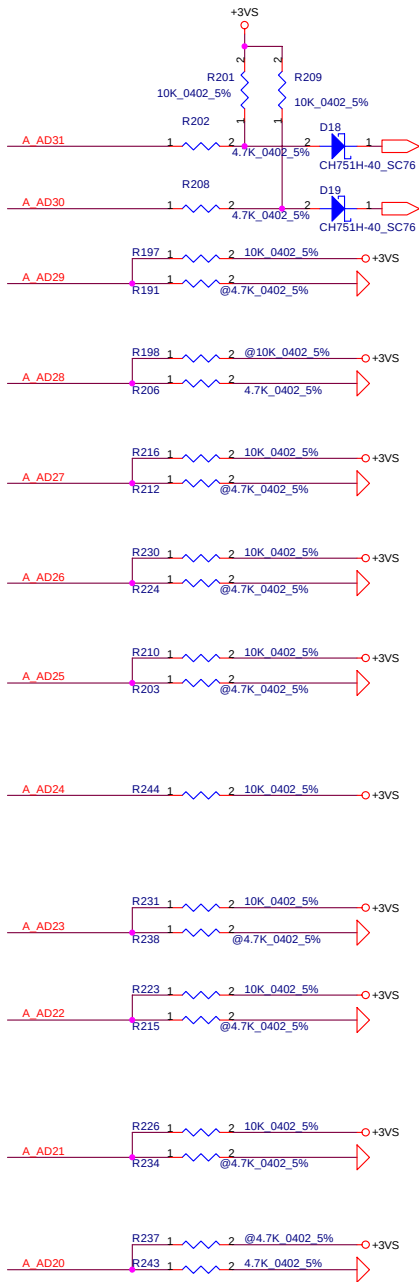
Title			
ATI RC300M-AGP, ALINK BUS			
Size	Document Number	Rev	
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Title			
AT1RC300M-POWER			
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A_AD[31..30] : FSB CLK SPEED
DEFAULT: 01
00: 100 MHZ
01: 133 MHZ
10: 200MHZ
11:166 MHZ

A_AD29: STRAP CONFIGURATION
DEFAULT:1
0:REDUCEDE SET
1: FULL SET

A_AD28: SPREAD SPECTRUM ENABLE
DEFAULT:0
0: DISABLE
1: ENABLE

A_AD27: FrcShortReset#
DEFAULT: 1
0: TEST MODE
1: NORMAL MODE

A_AD26 : ENABLE IOQ
DEFAULT: 1
0: IOQ=1
1: IOQ=12

A_AD25/A_AD17 : CPU VOLTAGE[1..0]
DEFAULT: 10
AD25=1 DESTOP CPU
AD25=0 MOBILE CPU
AD17-- DON'T CARE

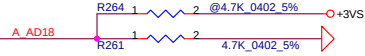
A_AD24 : MOBILE CPU SELECT
DEFAULT: 1
0: BANIAS CPU
1: OTHER CPU

A_AD23 : CLOCK BYPASS DISABLE
DEFAULT: 1
0: TEST MODE
1: NORMAL

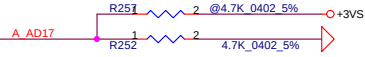
A_AD22 : OSC PAD OUTPUT PCICLK
DEFAULT : 1
0: PCICLK OUT
1: OSC CLK OUT

A_AD21 : AUTO_CAL ENABLE
DEFAULT : 1
0: DISABLE
1: ENABLE

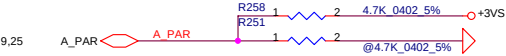
A_AD20 : INTERNAL CLK GEN ENABLE
DEFAULT : 0
0: DISABLE
1: ENABLE



A_AD18 : ENABLE PHASE CALIBRATION
DEFAULT: 0
0: DISABLE
1: ENABLE

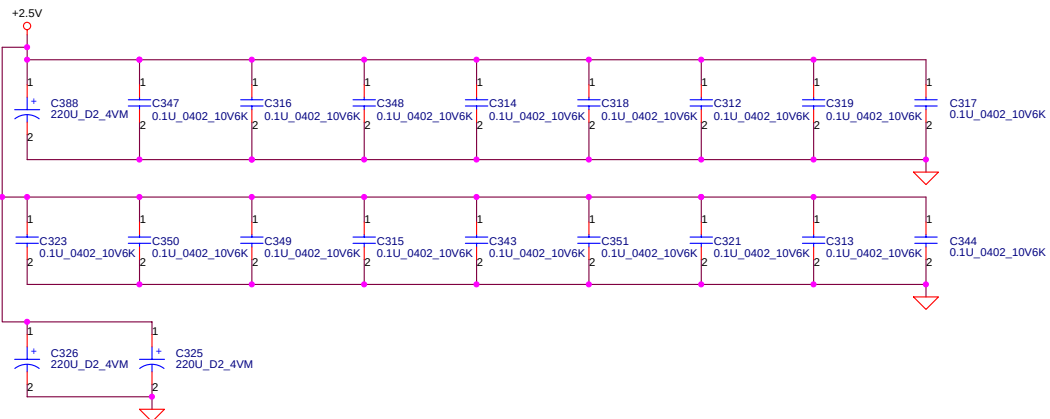


A_AD25/A_AD17 : CPU VOLTAGE[1..0]
DEFAULT: 0
00: 1.05V
01: 1.35V
11: 1.75V
10: 1.45V



PAR: EXTENDED DEBUG MODE
DEFAULT : 1
0: DEBUG MODE
1: NORMAL

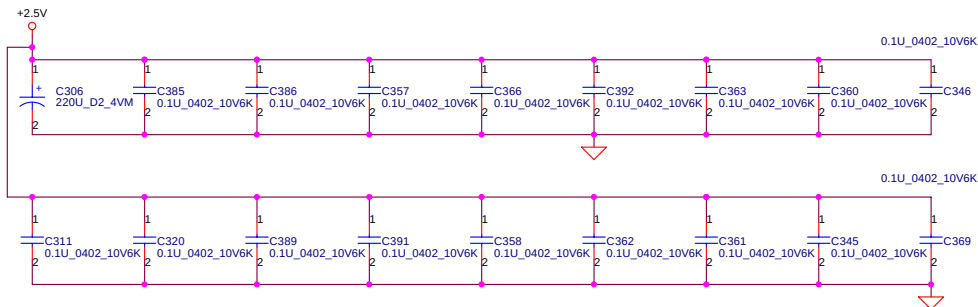
Layout note :
Distribute as close as possible
to DDR-SODIMM0.



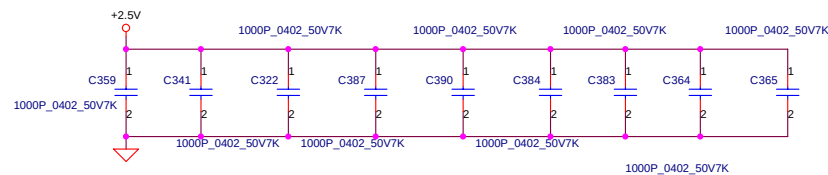
Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25VS



Layout note :
Distribute as close as possible
to DDR-SODIMM1.

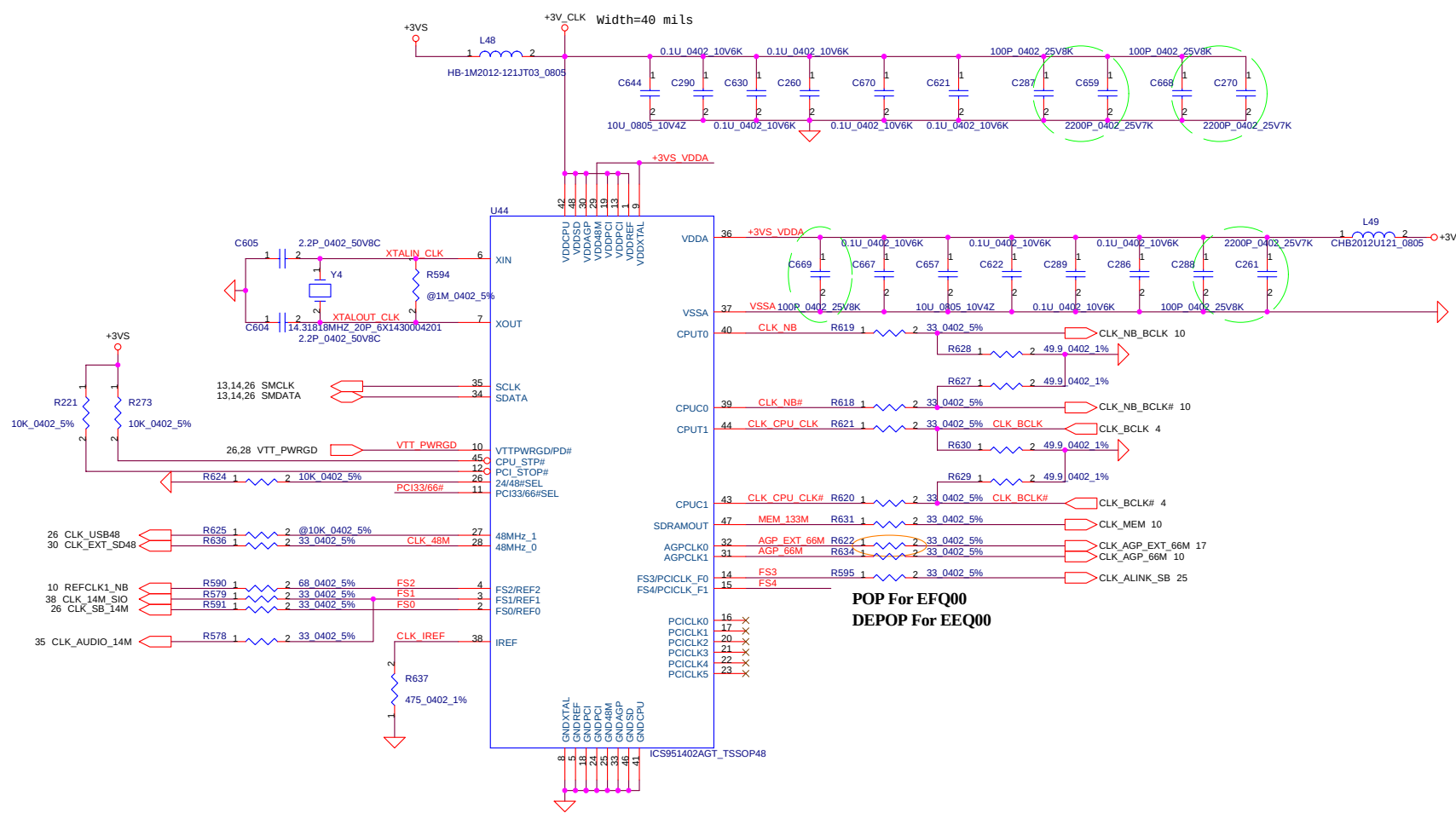


Layout note :
for EMI solution



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Title			
DDR SODIMM Decoupling			
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POP For EFQ00
DEPOP For EEQ00

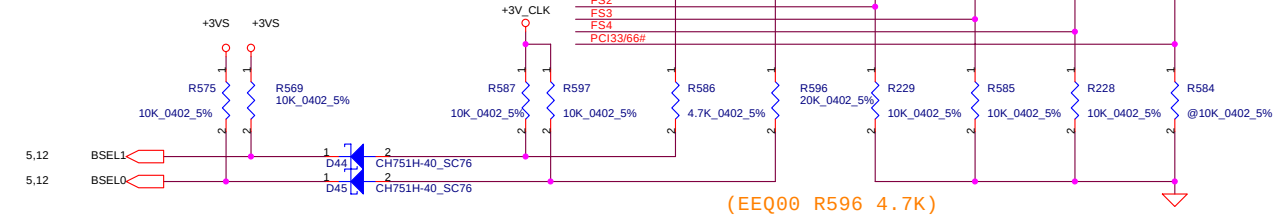
CLOCK FREQUENCY SELECT TABLE

FS4	FS3	FS2	FS1	FS0	CPU	MEM	With Spread Enabled...
0	0	0	1	0	200	200	Spread OFF OR Center spread +/-0.3%
0	0	0	0	1	133	133	
0	0	0	0	0	100	100	

A-LINK FREQ

PCI33/66# = HIGH	66MHZ
PCI33/66# = LOW	33MHZ

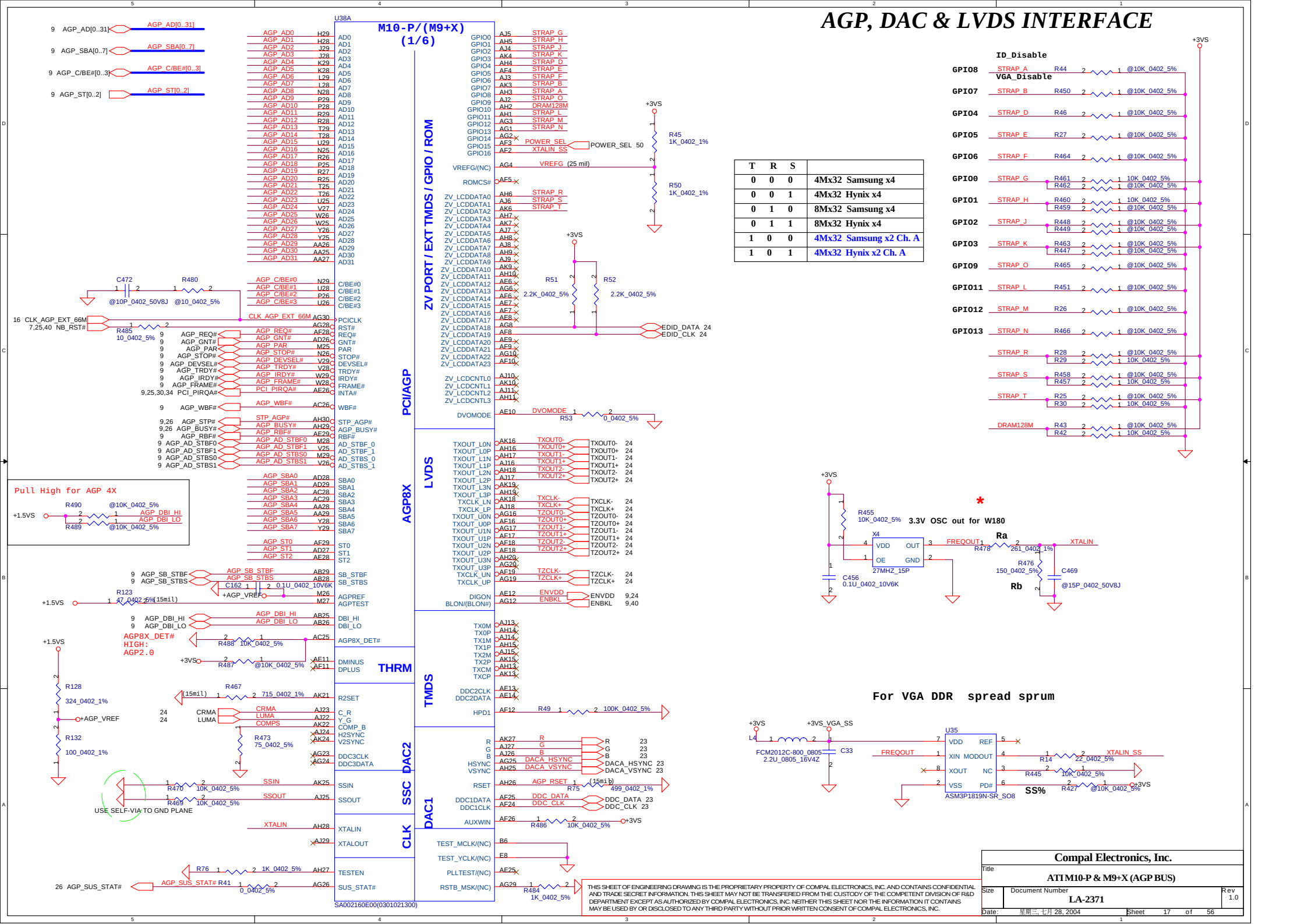
Note: 0 = PULL LOW
1 = PULL HIGH



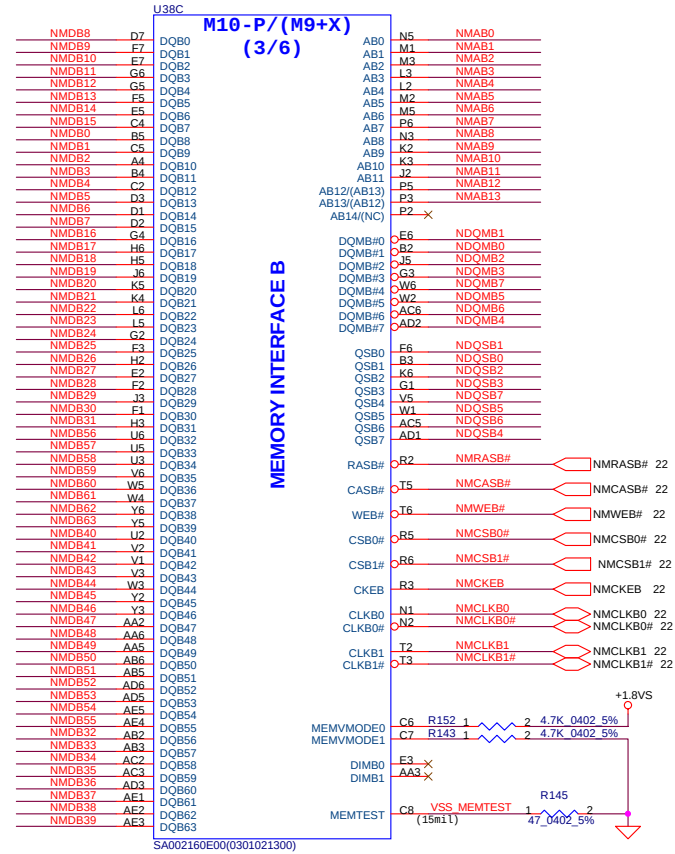
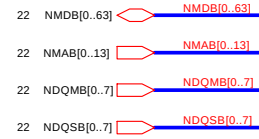
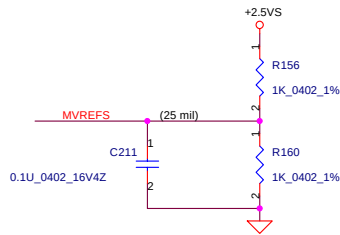
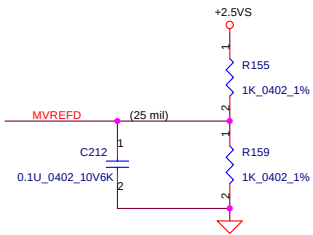
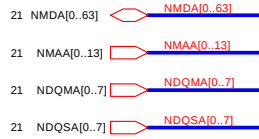
(EEQ00 R596 4.7K)

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AGP, DAC & LVDS INTERFACE



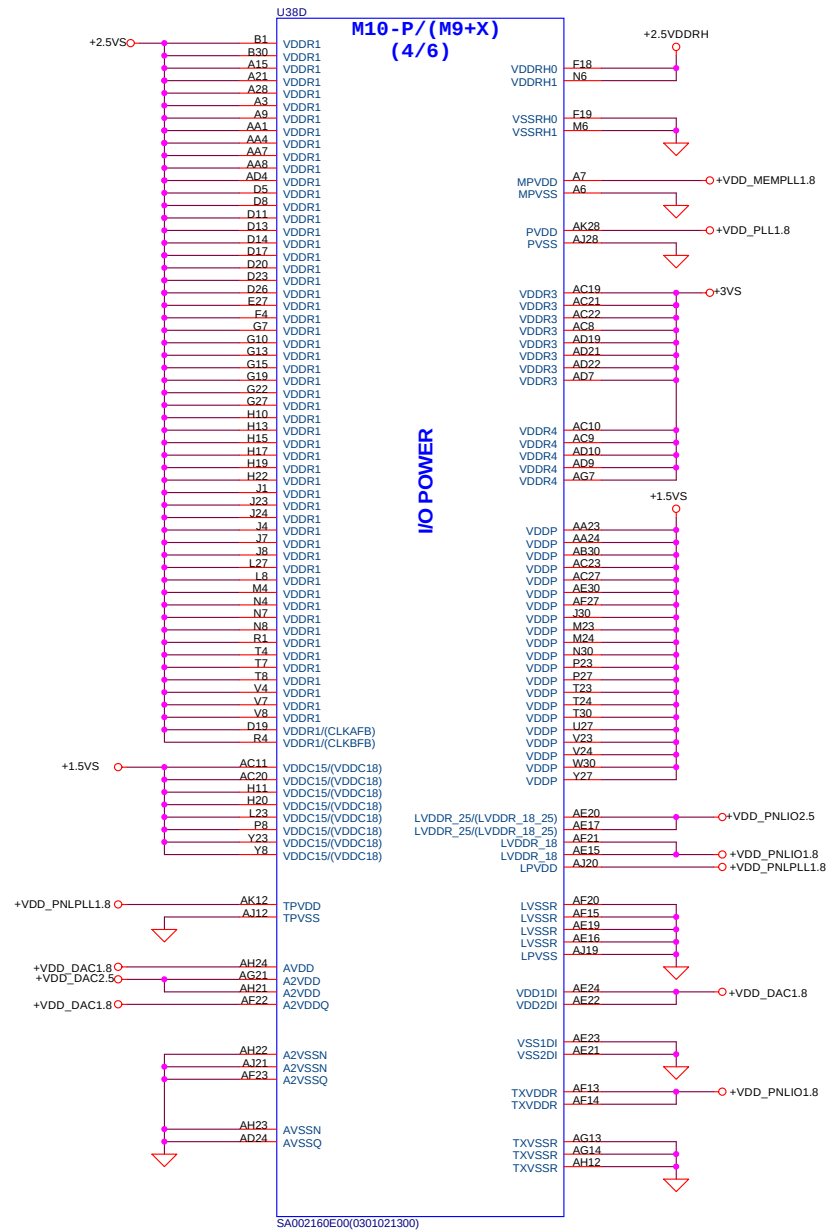
MEMORY INTERFACE A



Compal Electronics, Inc.		
Title		
ATI M10-P/M9+X DDR-A		
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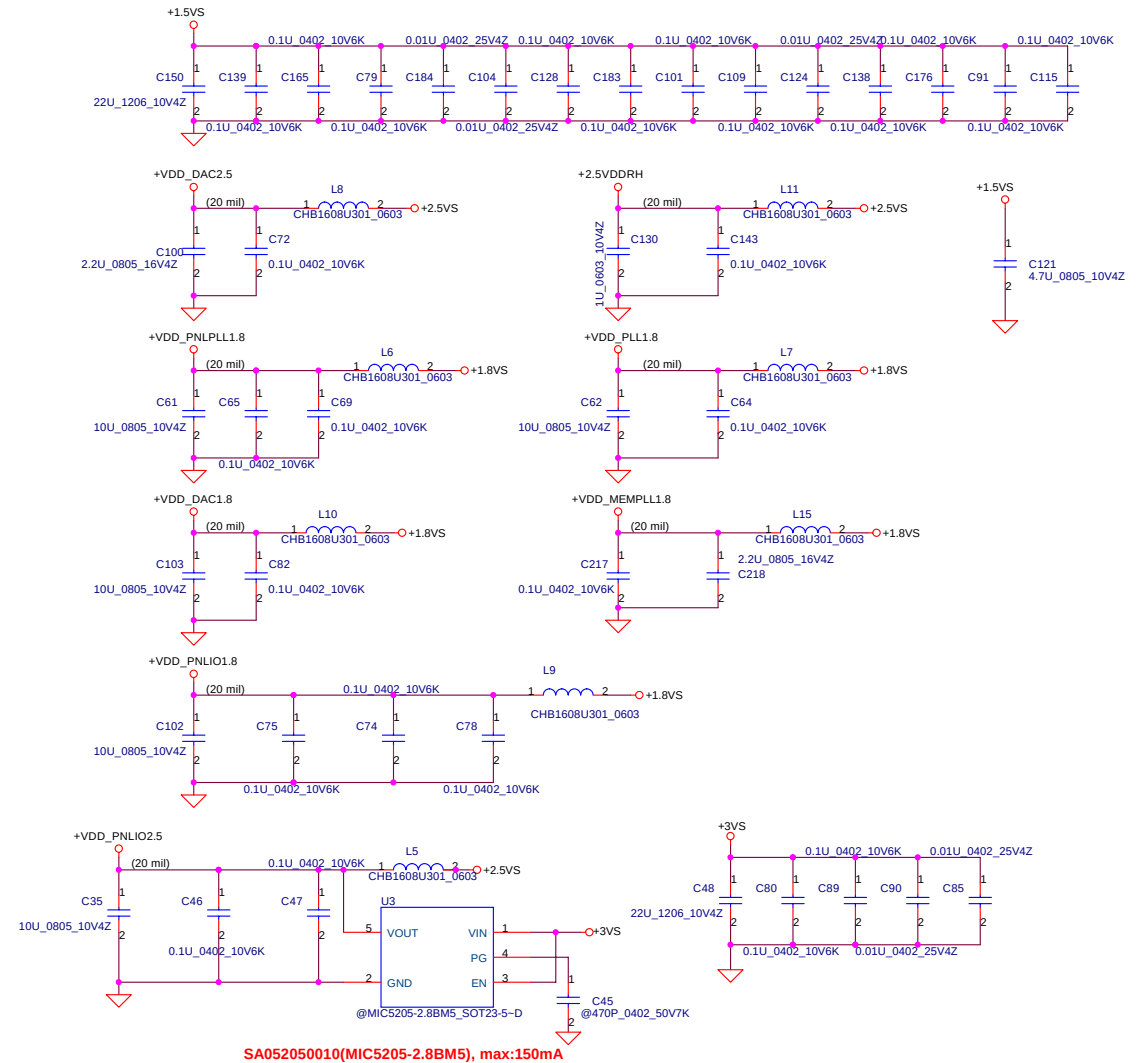
POWER INTERFACE



POWER Sequence

3.3VS --> 2.5VS --> 1.8VS --> +VGA_Core --> +1.5VS

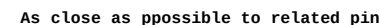
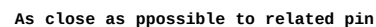
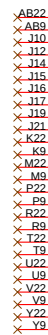
The differ between +2.5VS and +1.8VS should not be greater than 1.2V



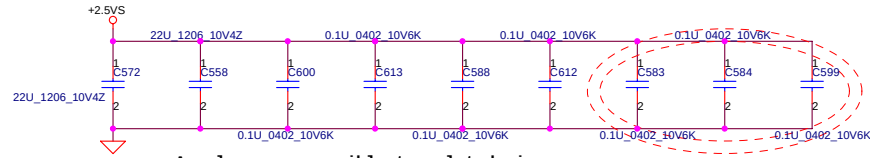
SA052050010(MIC5205-2.8BM5), max:150mA



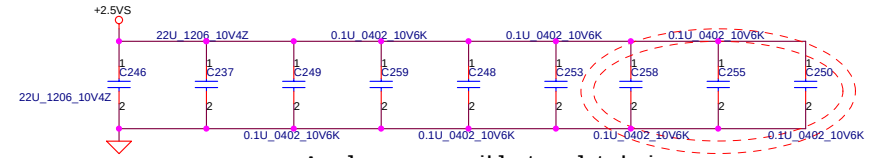
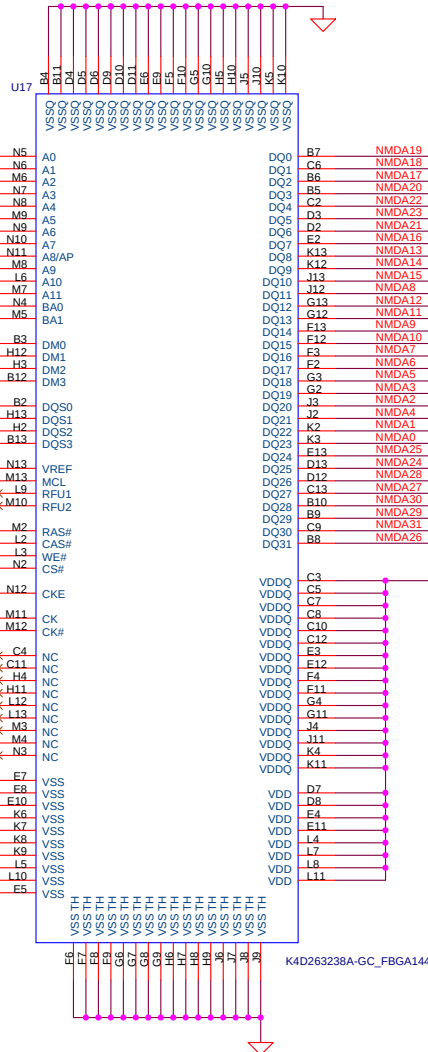
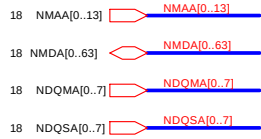
CORE POWER



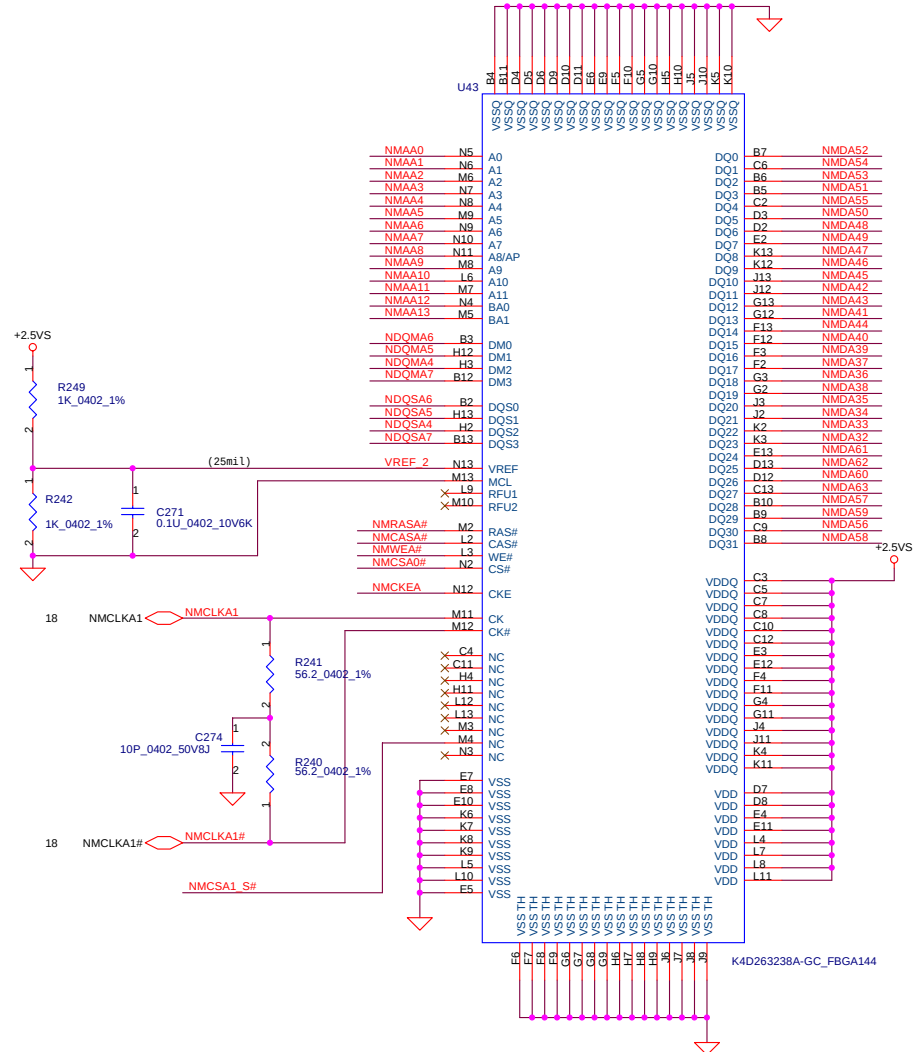
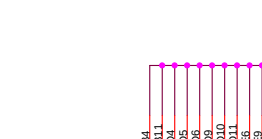
VGA DDR FOR CHANNEL A



As close as possible to related pin



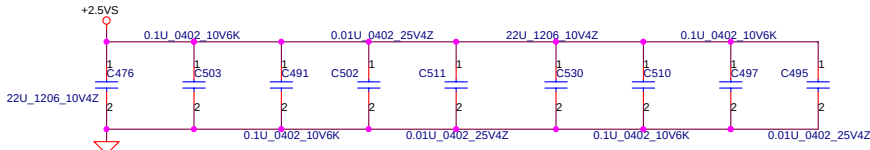
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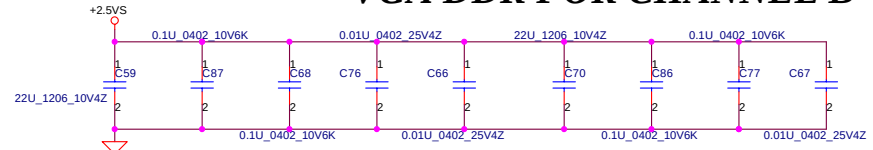
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VGA DDR FOR CHANNEL A			
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VGA DDR FOR CHANNEL B

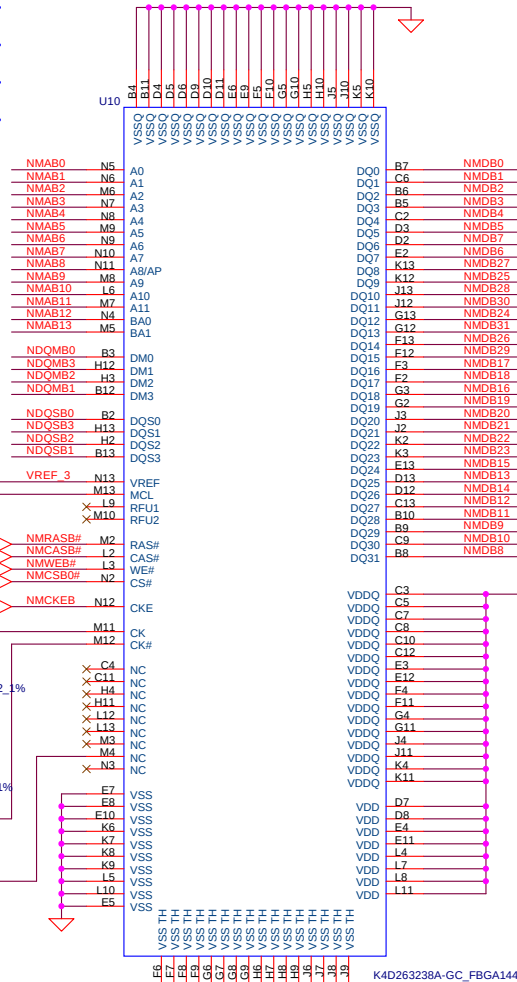


As close as possible to related pin

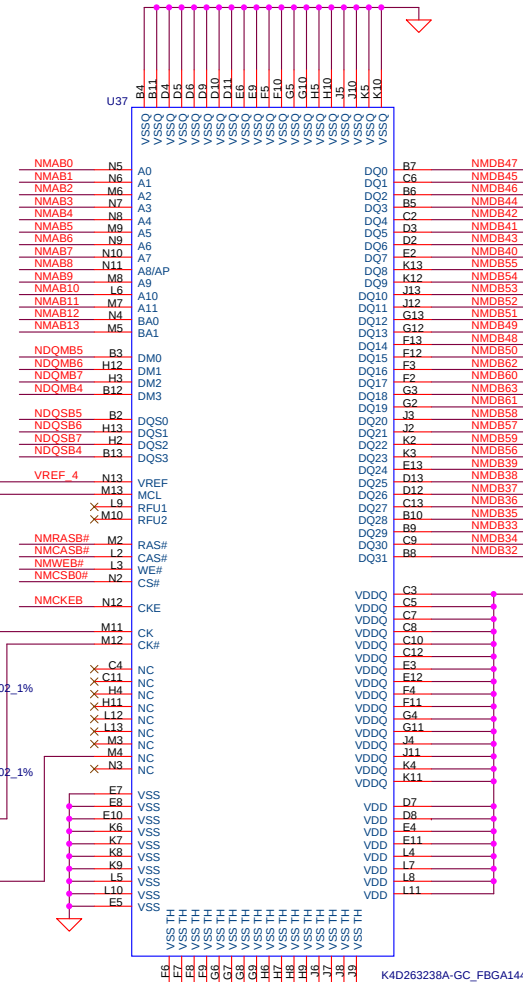


As close as possible to related pin

- 18 NMAB[0..13] NMAB[0..13]
- 18 NMDB[0..63] NMDB[0..63]
- 18 NDQMB[0..7] NDQMB[0..7]
- 18 NDQSB[0..7] NDQSB[0..7]



K4D263238A-GC_FBGA144



K4D263238A-GC_FBGA144

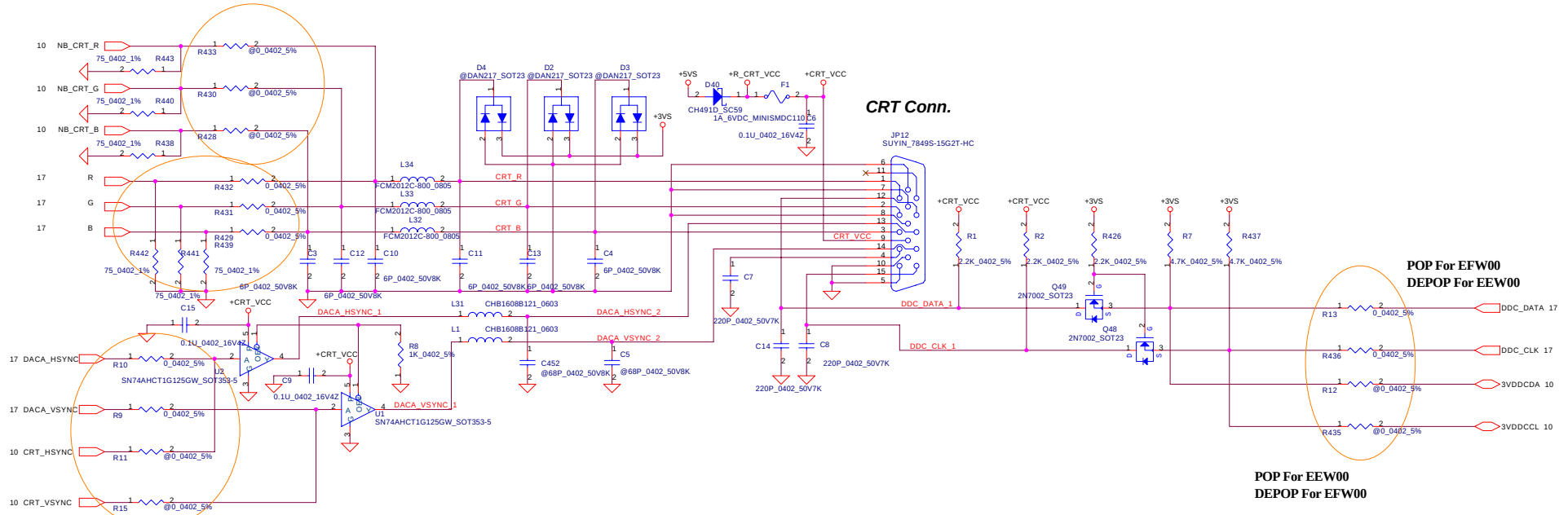
Compal Electronics, Inc.

VGA DDR FOR CHANNEL B

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POP For EFW00
DEPOP For EEW00



CRT Conn.

POP For EFW00
DEPOP For EEW00

POP For EEW00
DEPOP For EFW00

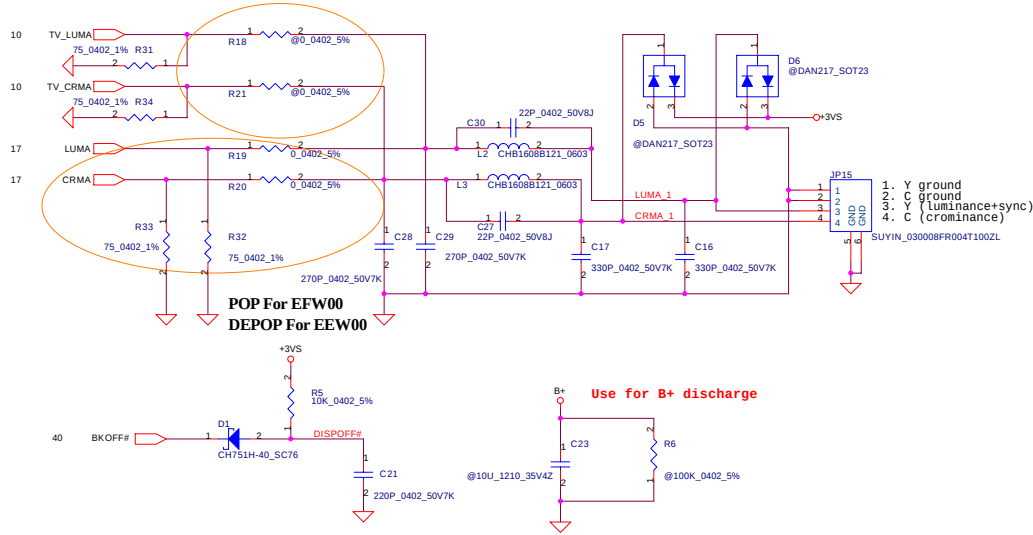
POP For EFW00
DEPOP For EEW00

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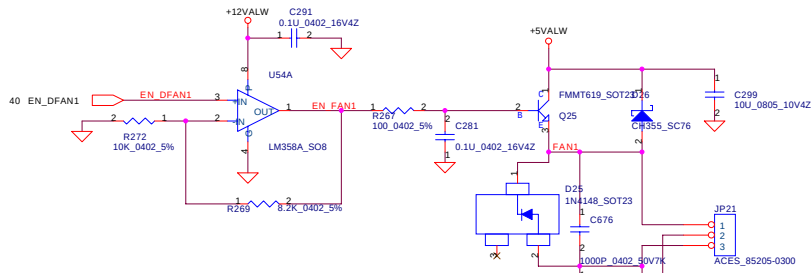
Compal Electronics, Inc.			
Title			
CRT Connector			
Size	Document Number		Rev
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POP For EEQ00
DEPOP For EFQ00

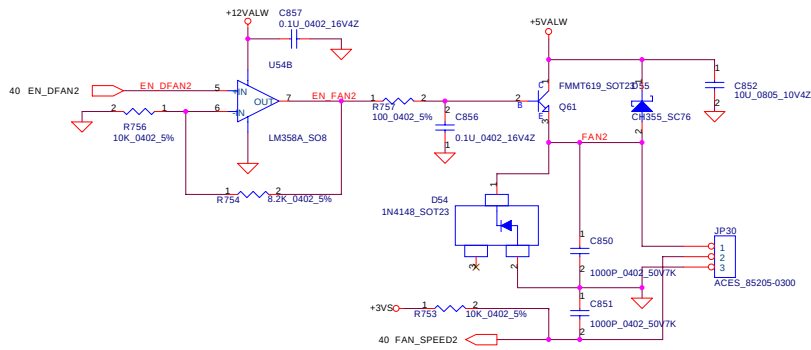
TV-OUT Conn.



FAN CONN. 1

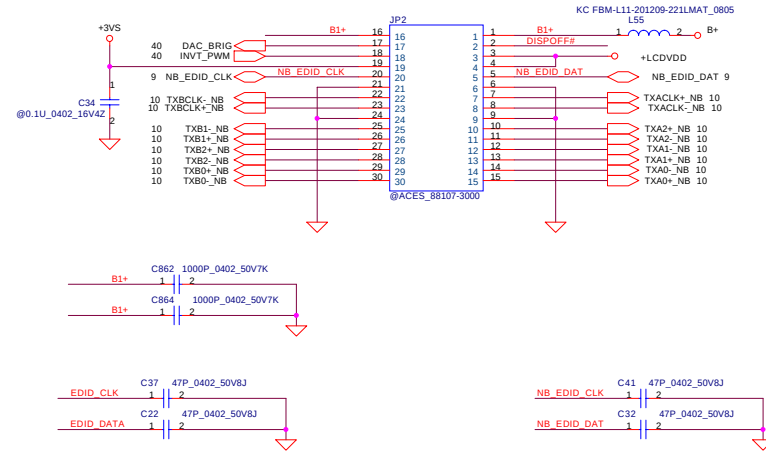


FAN CONN. 2



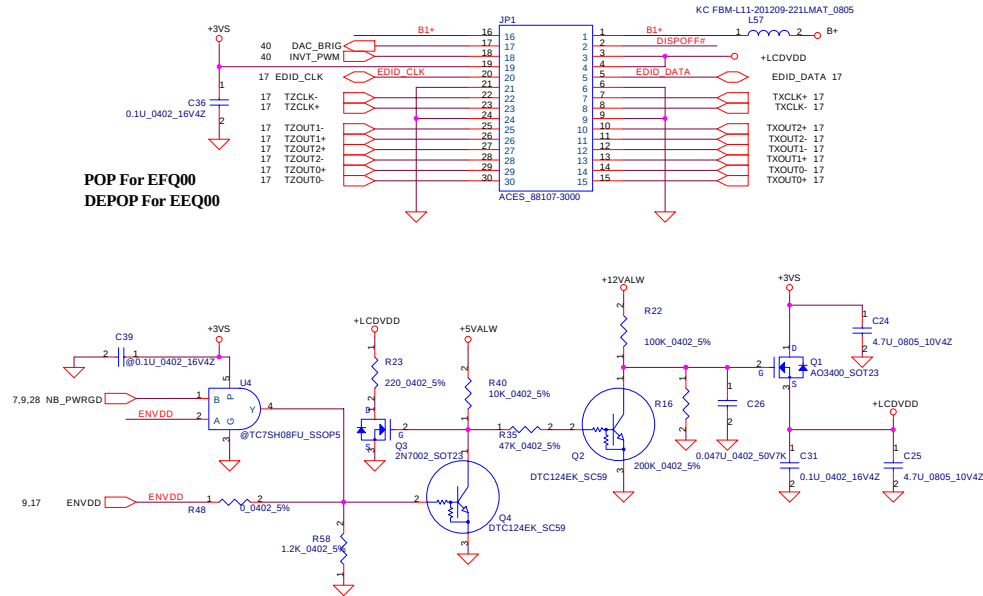
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POP For EEQ00
DEPOP For EFQ00



Width: 40mils

POP For EFQ00
DEPOP For EEQ00



Compal Electronics, Inc.

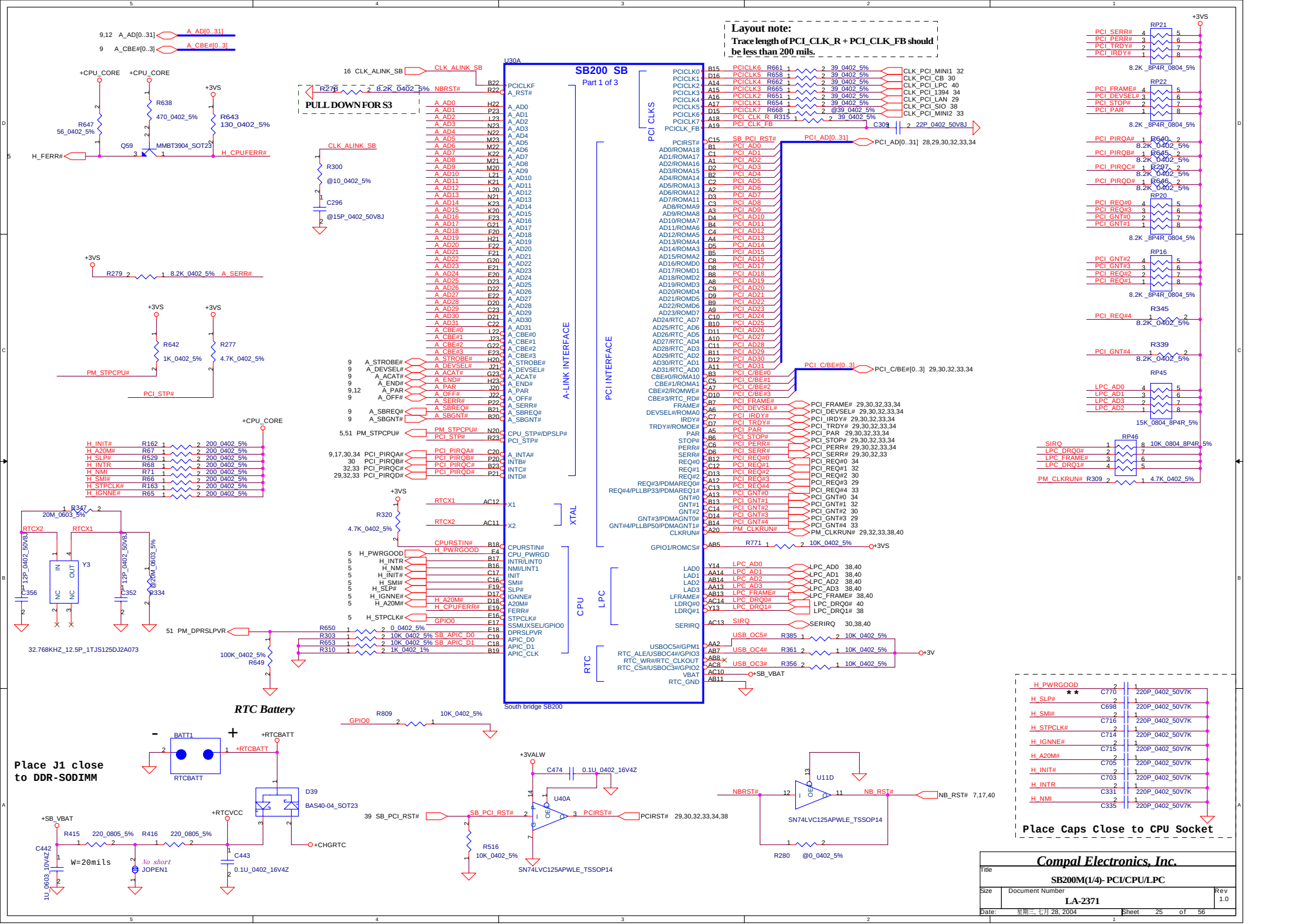
CRT,TV-OUT & LVDS Connector

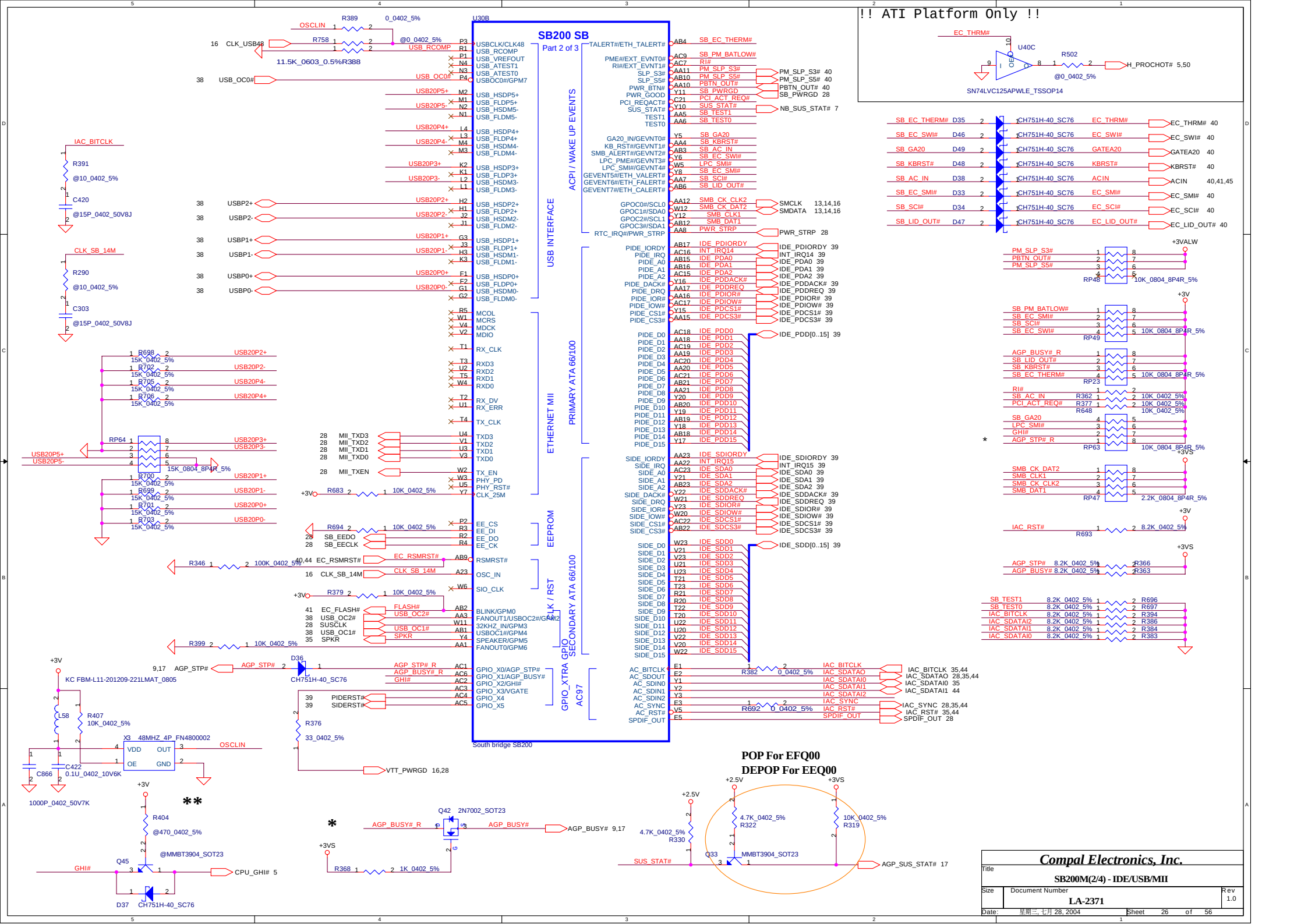
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LA-2371

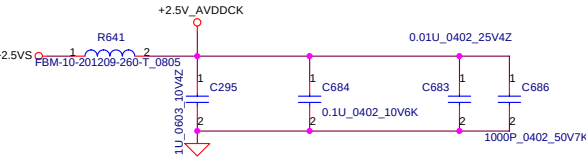
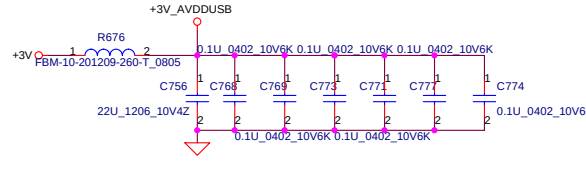
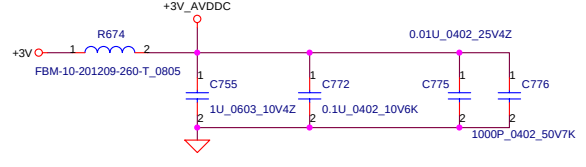
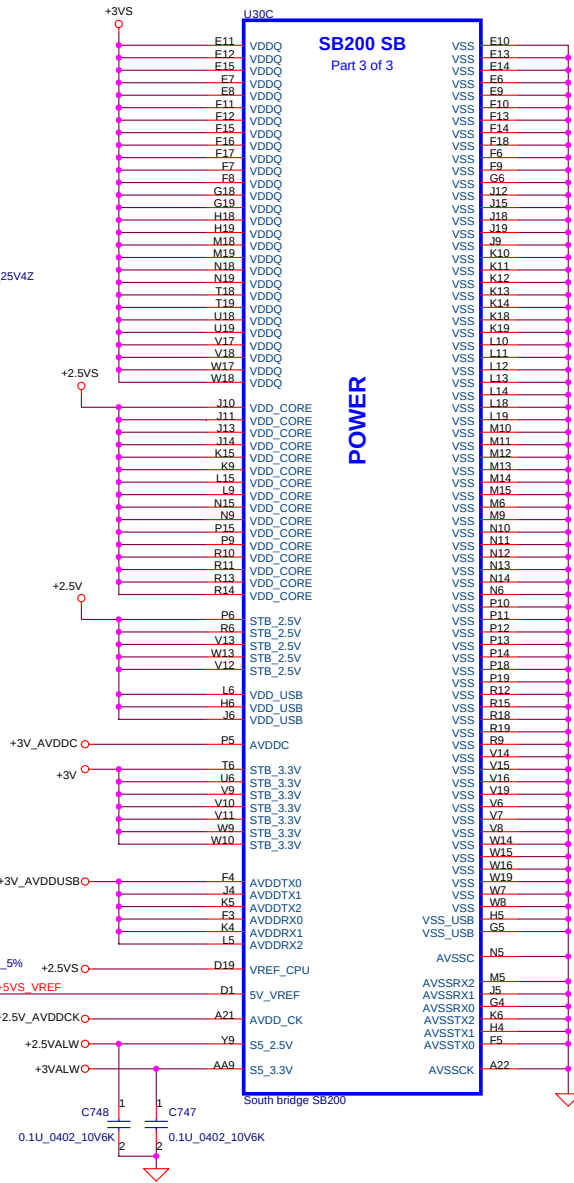
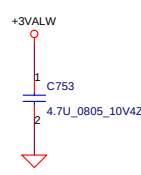
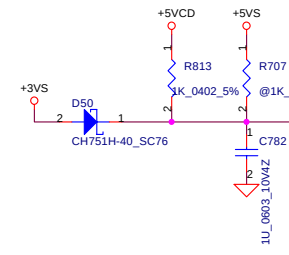
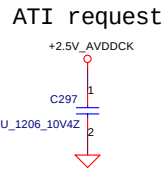
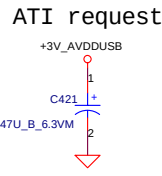
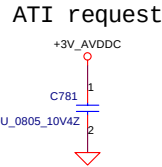
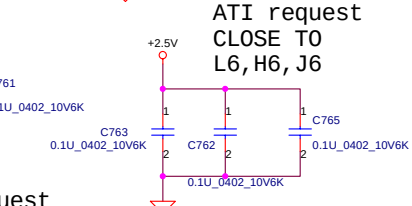
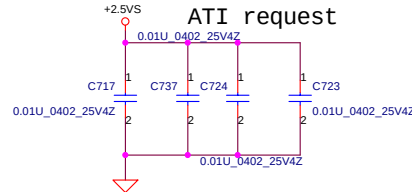
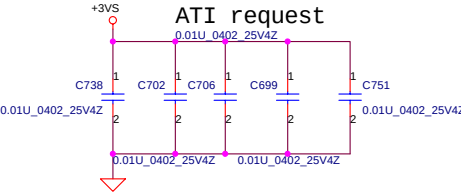
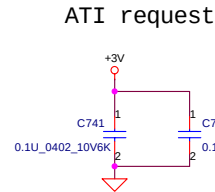
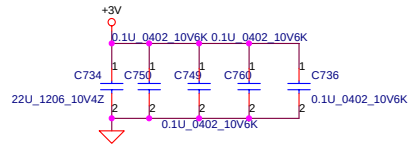
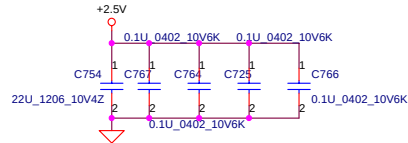
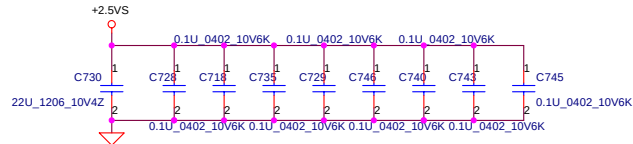
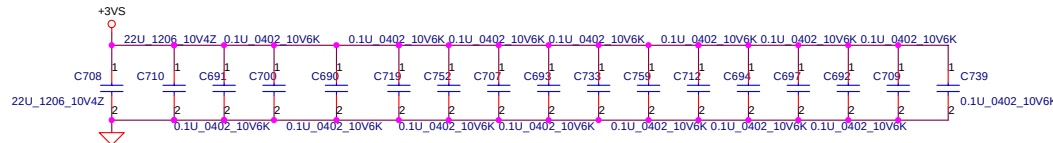
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1.0

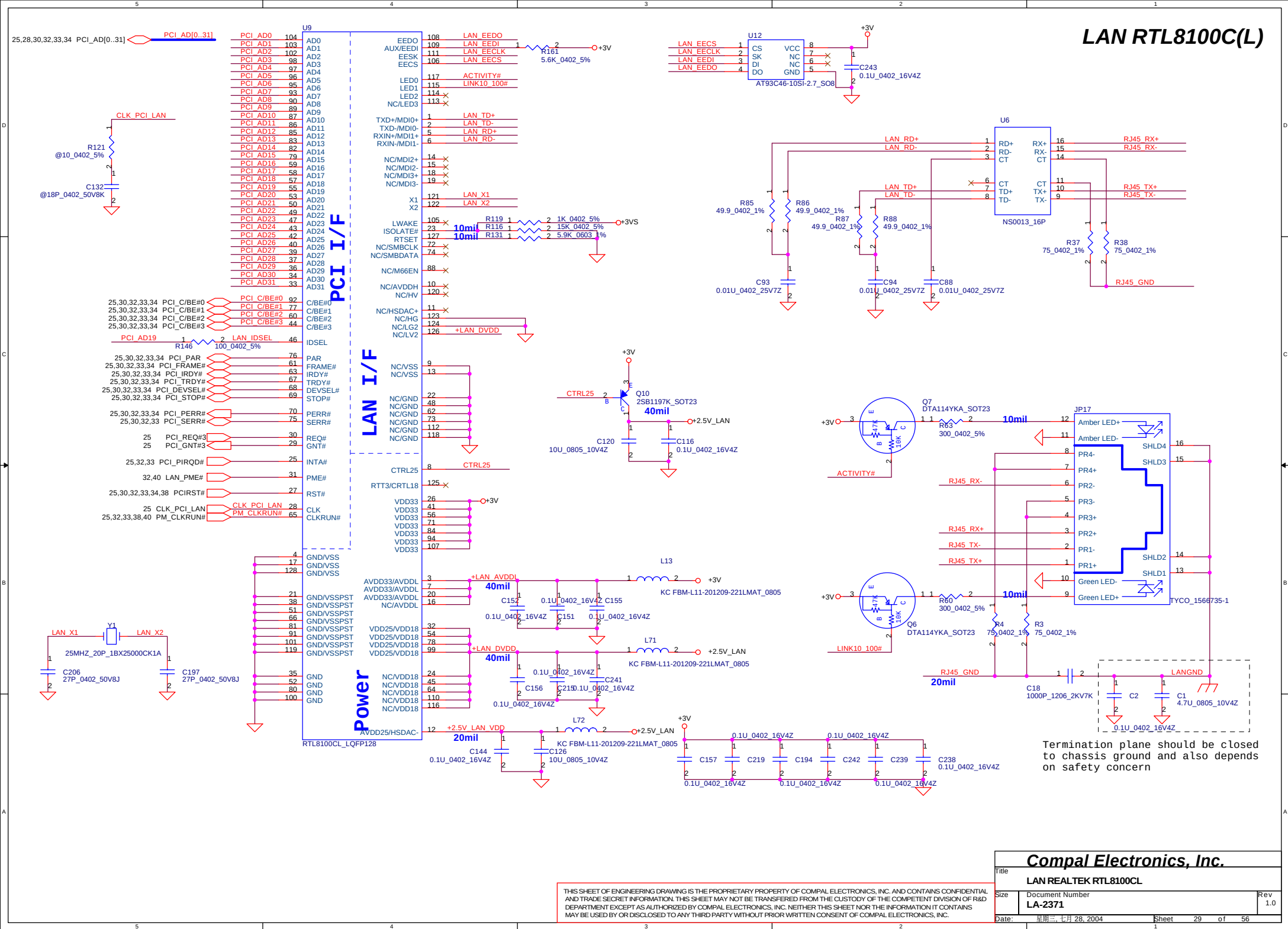
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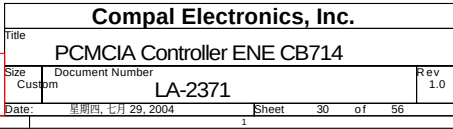
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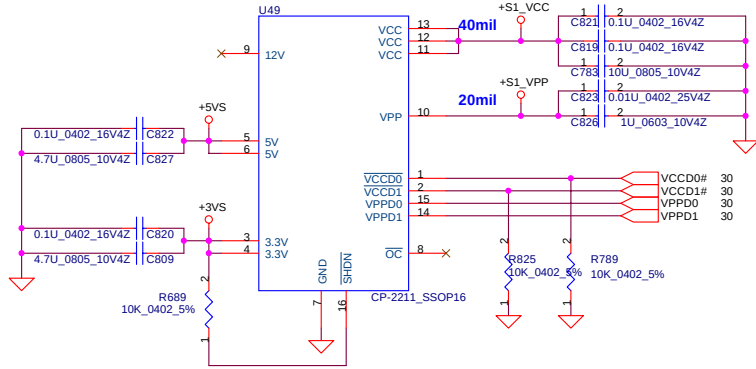
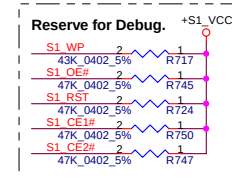
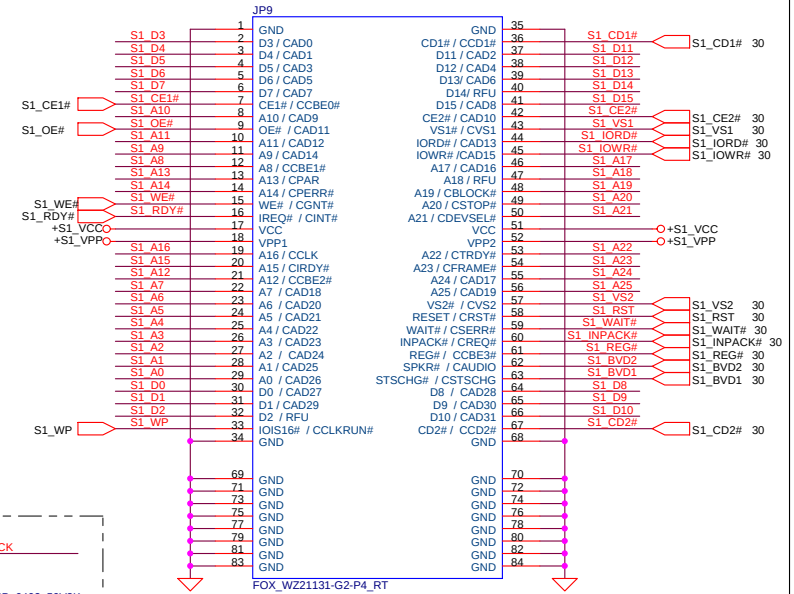
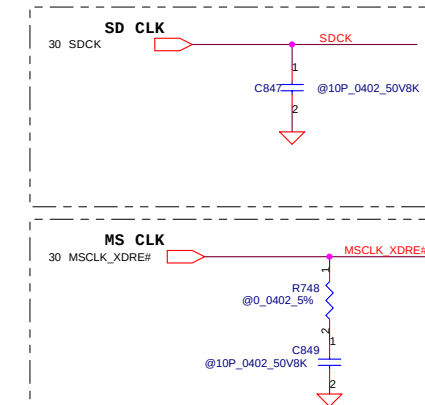
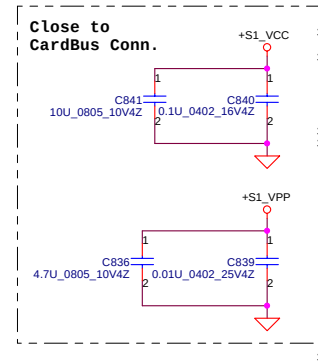
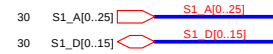




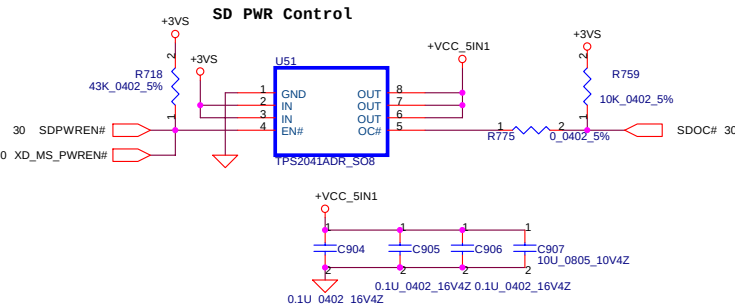
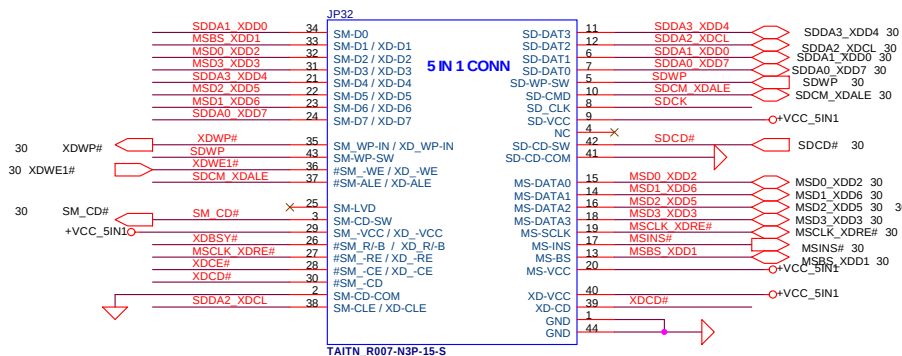




PCMCIA Power Controller

**CardBus Socket**

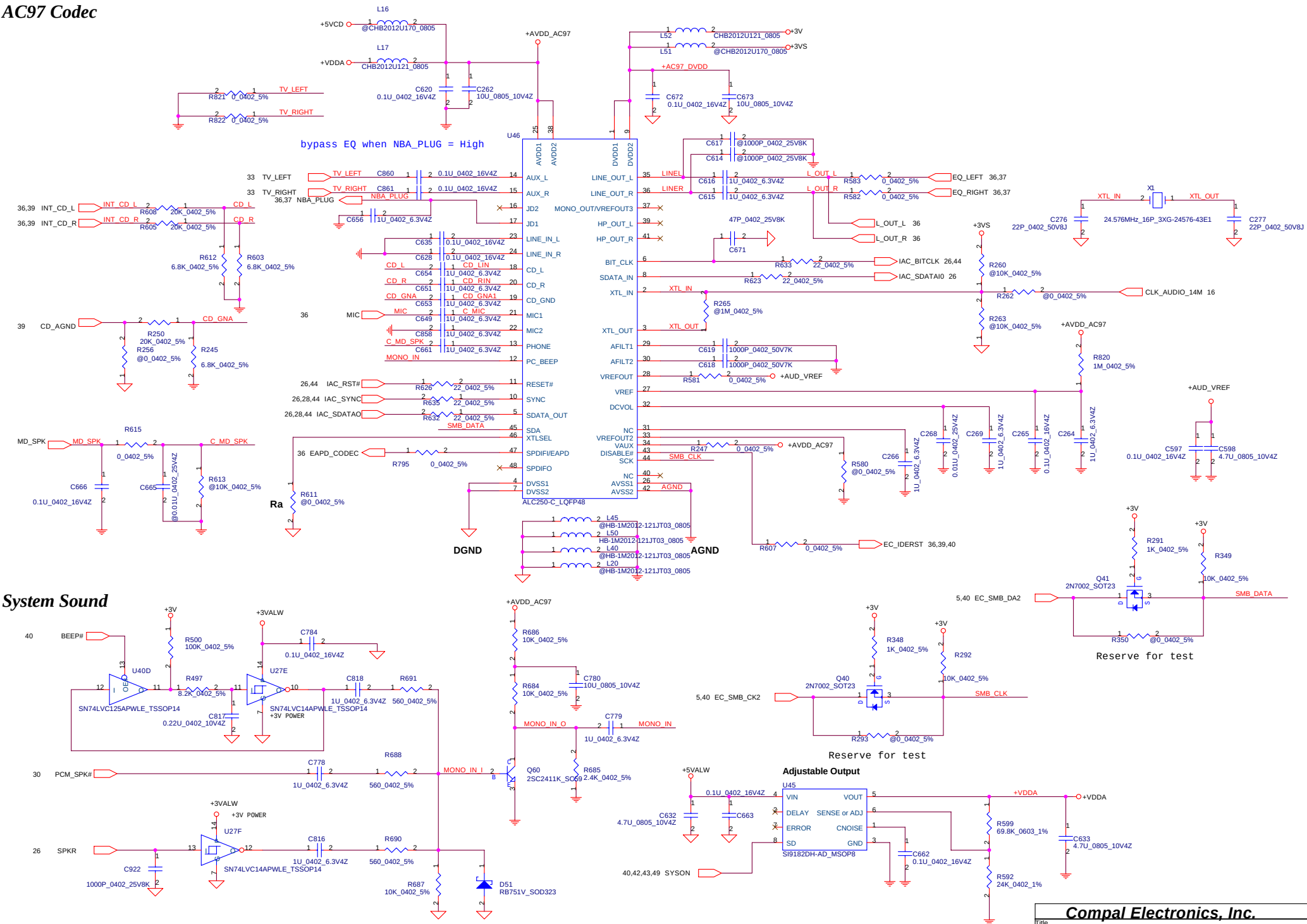
xD PU and PD. Close to Socket



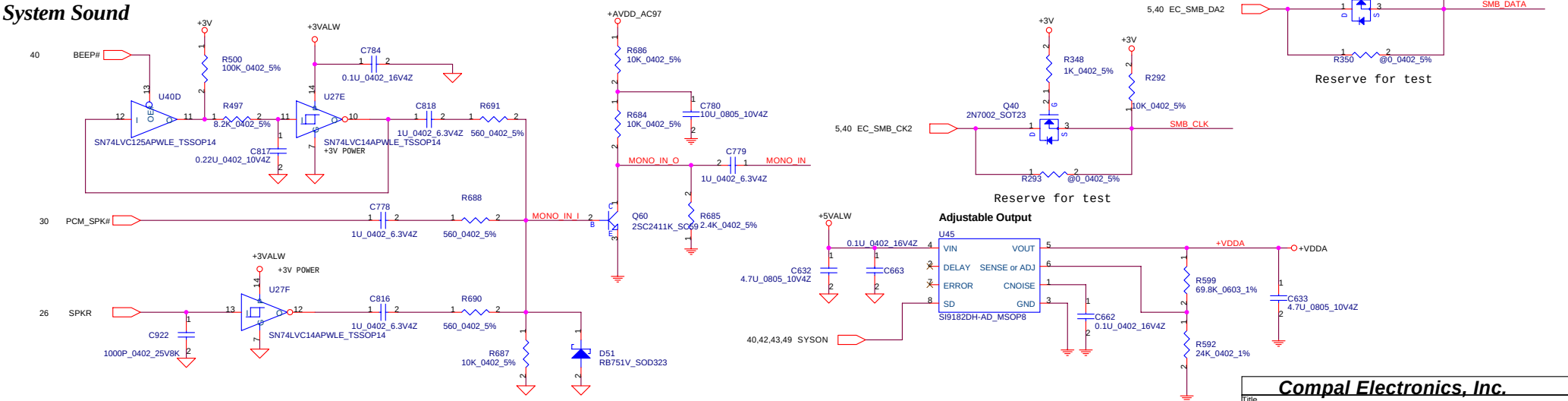
Compal Electronics, Inc.			
Title			
PCMCIA Socket			
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AC97 Codec



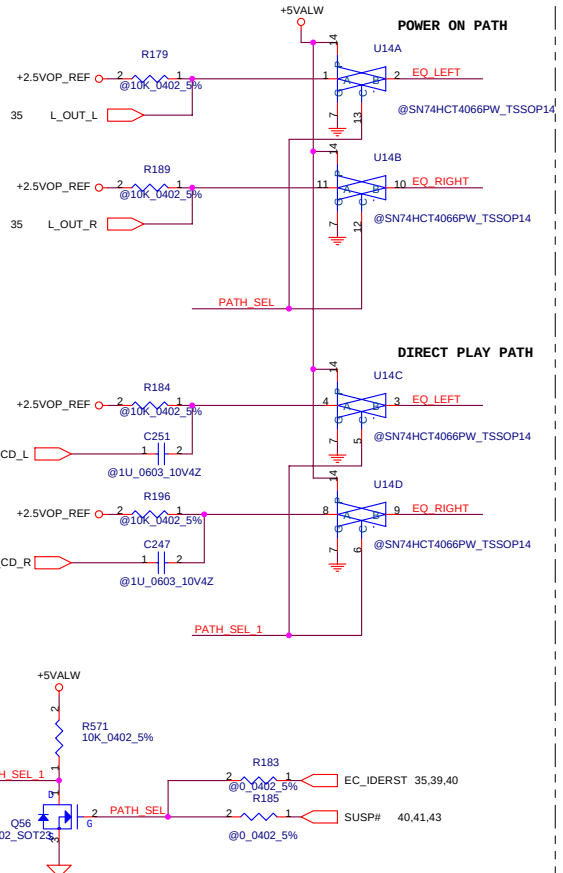
System Sound



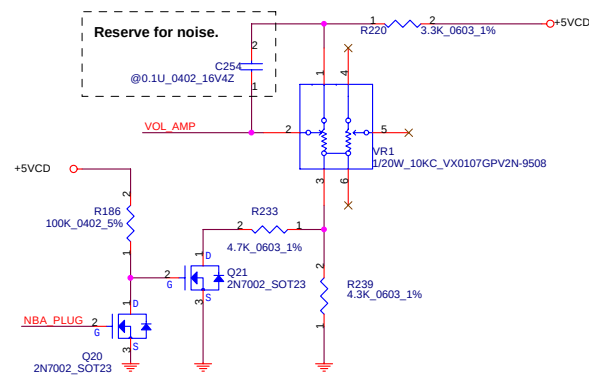
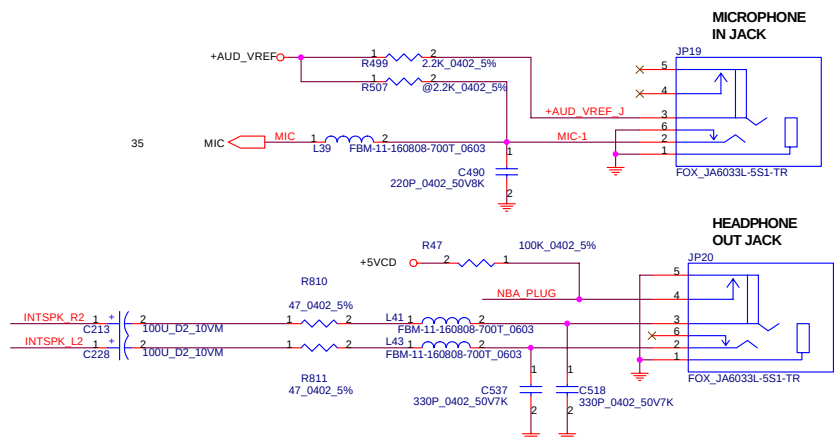
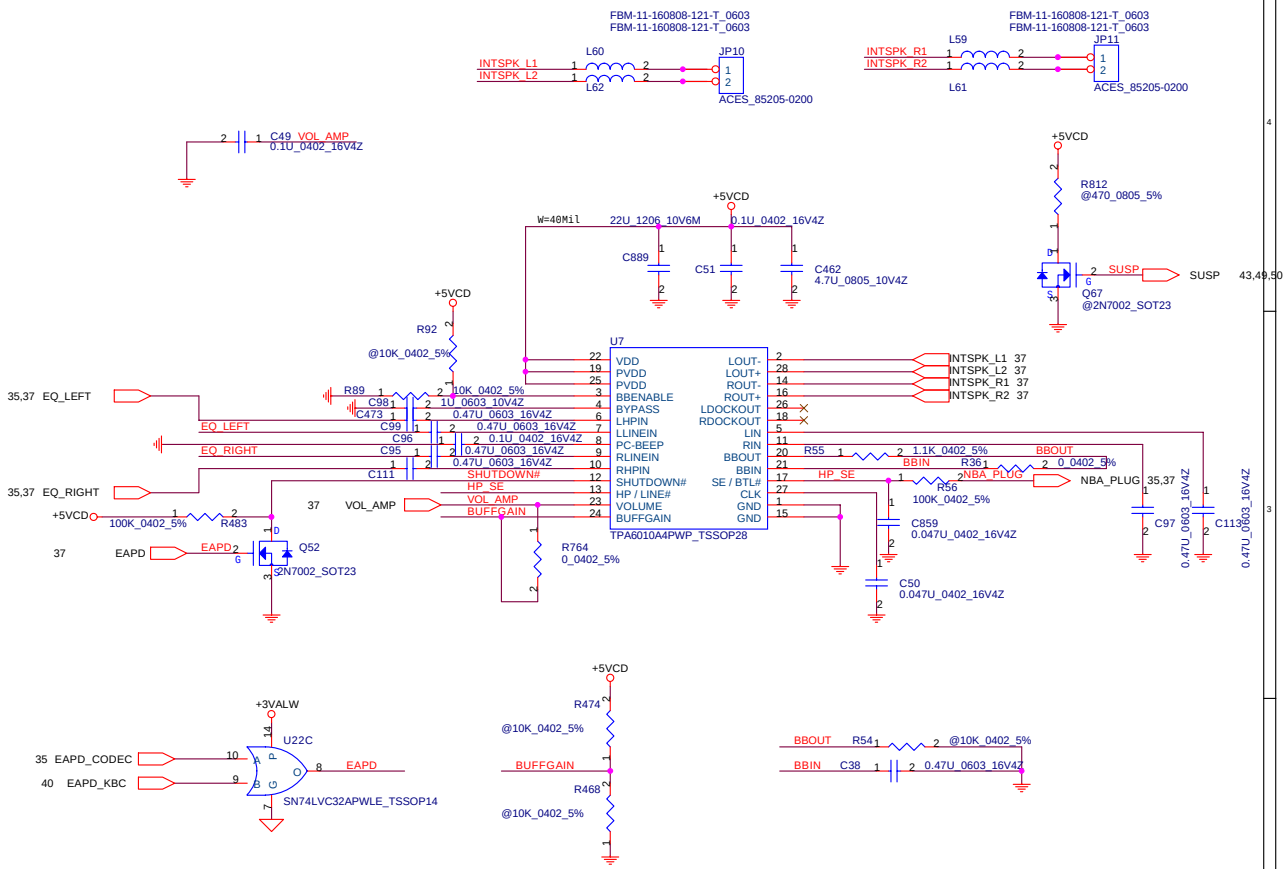
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AC97 Codec ALC250			
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**Direct CD
CTL**



Audio AMP



VR - C-Type

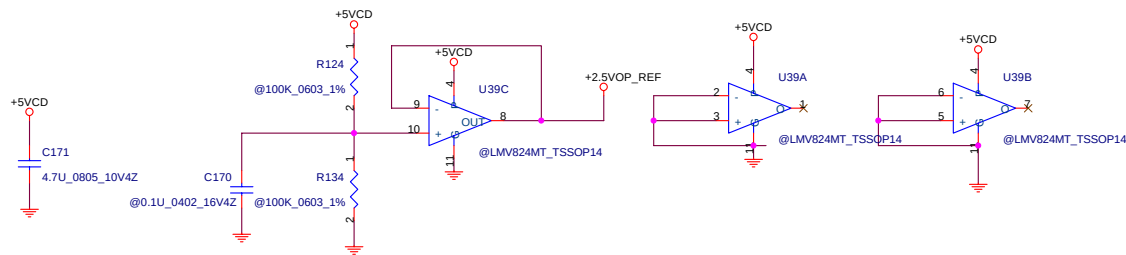
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R233	4.7K		
R239	4.3K		HP -4dB

Compal Electronics, Inc.

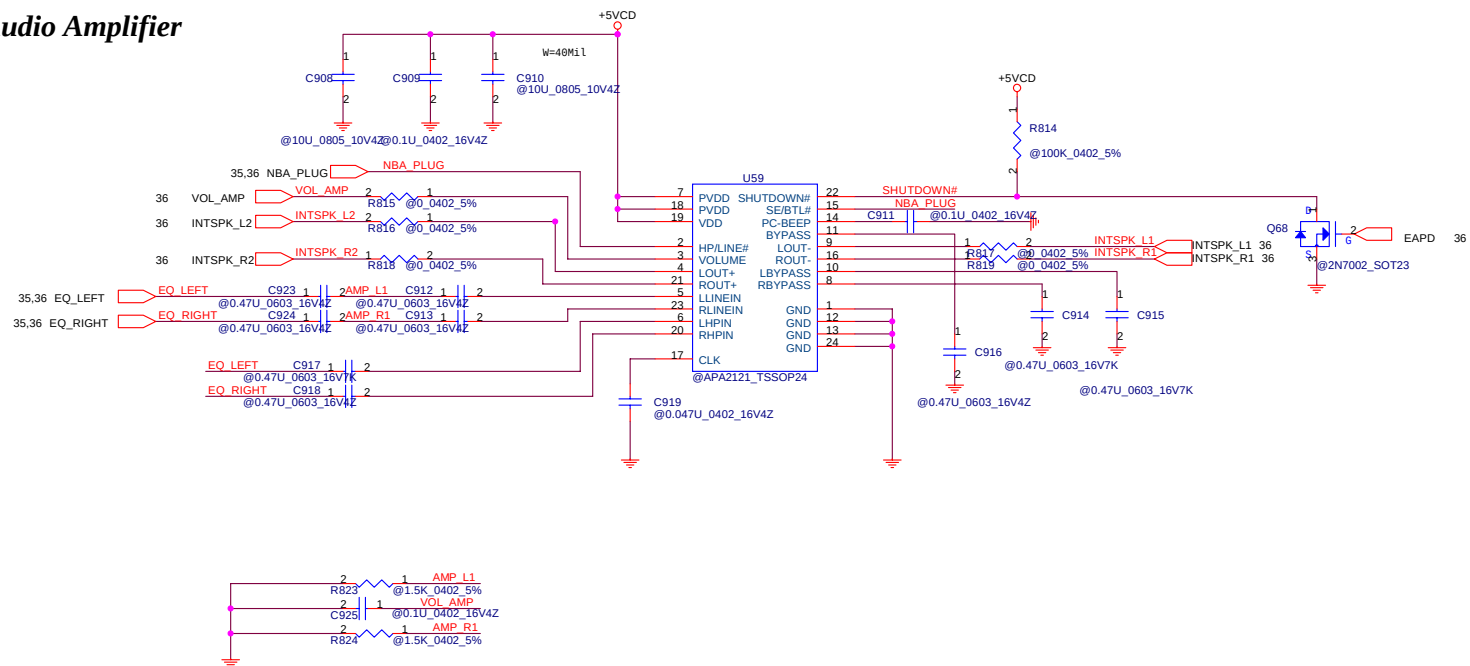
Audio AMP & JACK

Size	Document Number	Rev
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Audio Amplifier



Compal Electronics, Inc.

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APA2121 Audio Amplifier

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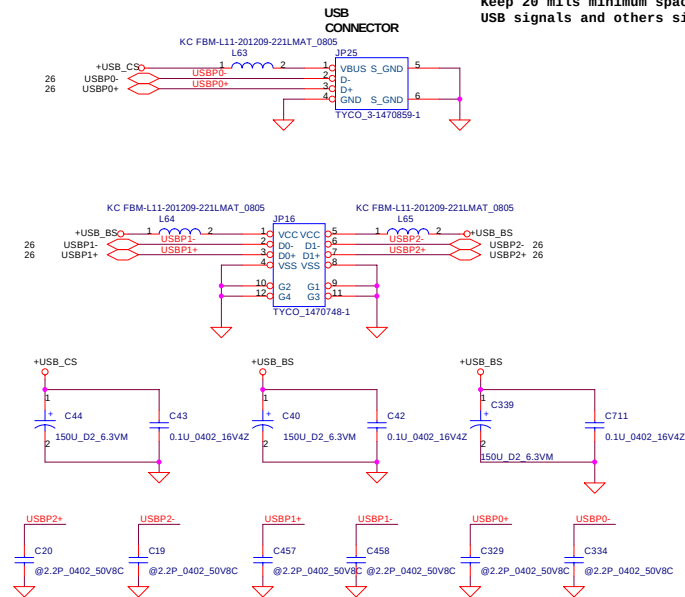
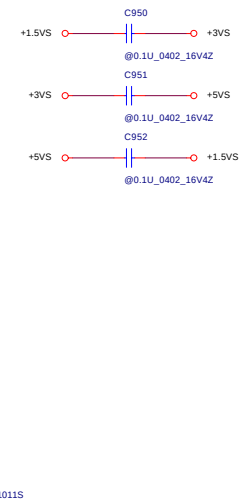
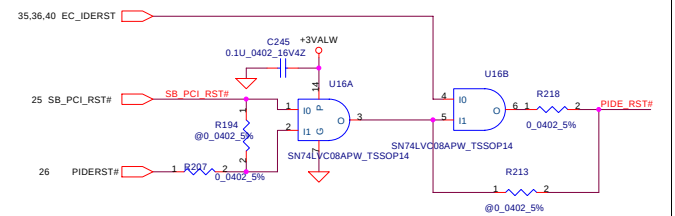
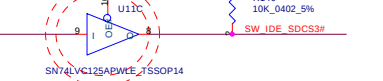
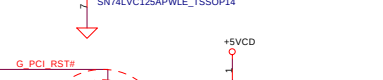
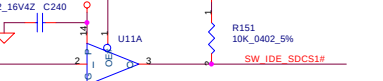
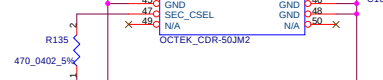
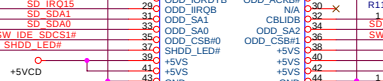
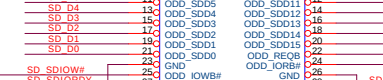
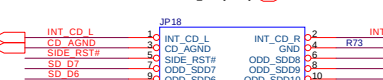
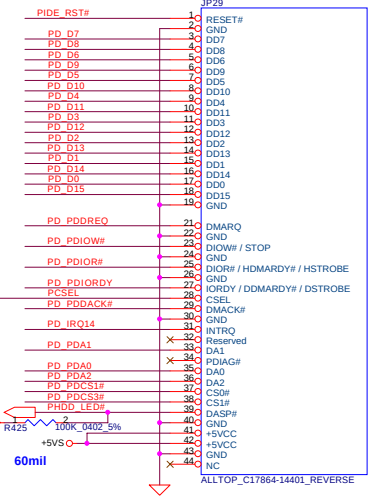
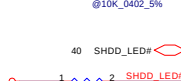
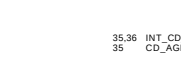
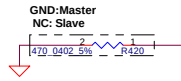
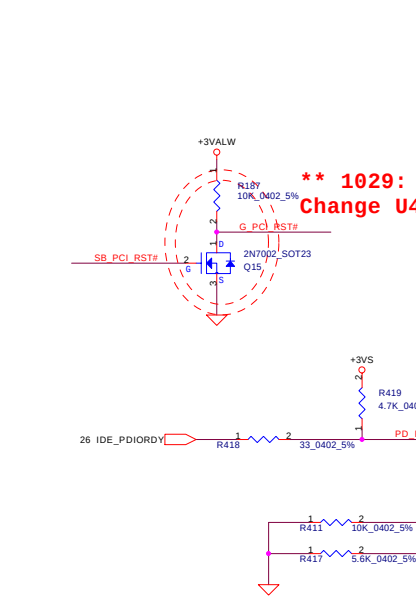
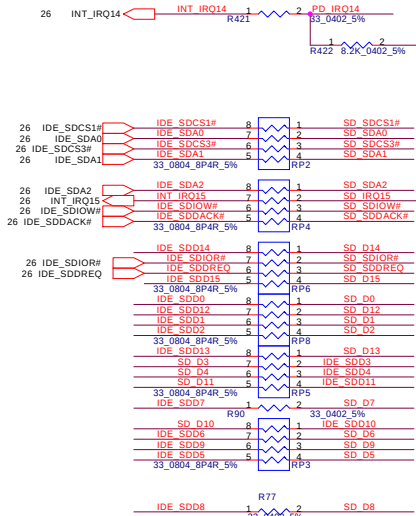
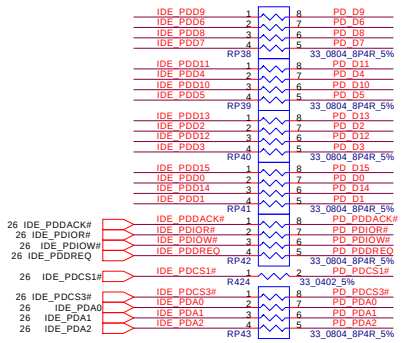


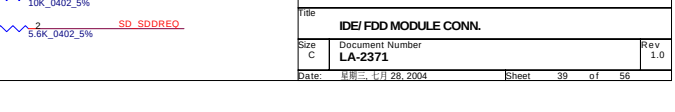
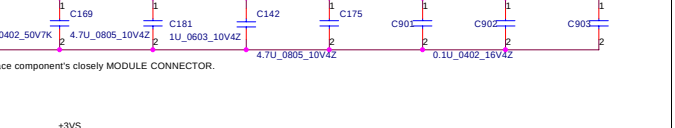
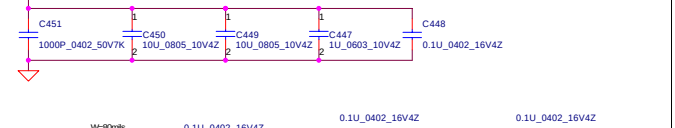
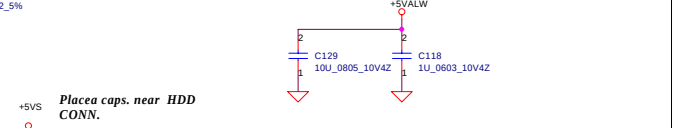
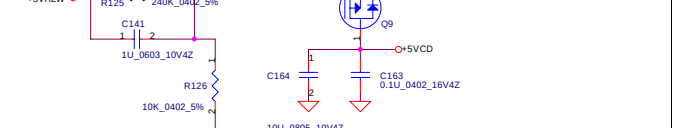
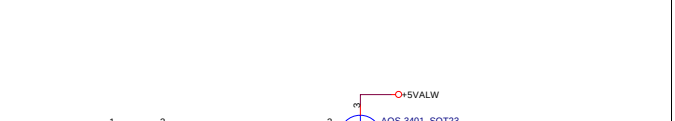
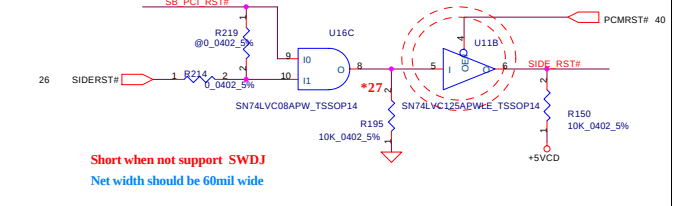
Diagram illustrating the power supply section for the ACES_8201-2005. The circuit includes two voltage regulators, R792 (5V) and R793 (3V), connected to a JP33 header. The 5V regulator is connected to the 5V pin of the JP33 header, and the 3V regulator is connected to the 3V pin. The regulators are connected to a common ground. The output of the 5V regulator is connected to the 5V pin of the JP33 header. The output of the 3V regulator is connected to the 3V pin of the JP33 header. The regulators are labeled R792 and R793. The JP33 header is labeled JP33. The ground connection is labeled @ACES_8201-2005.

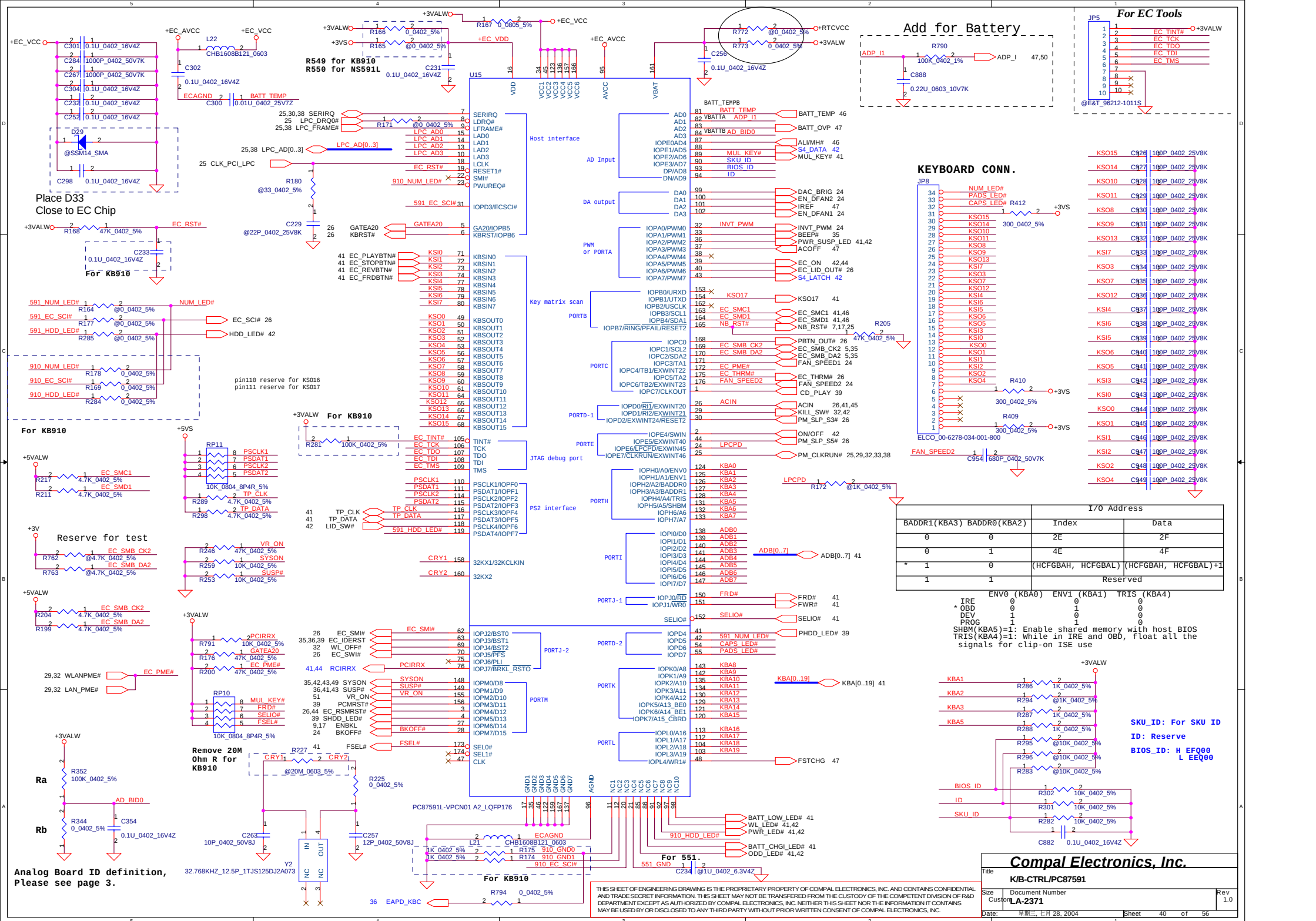


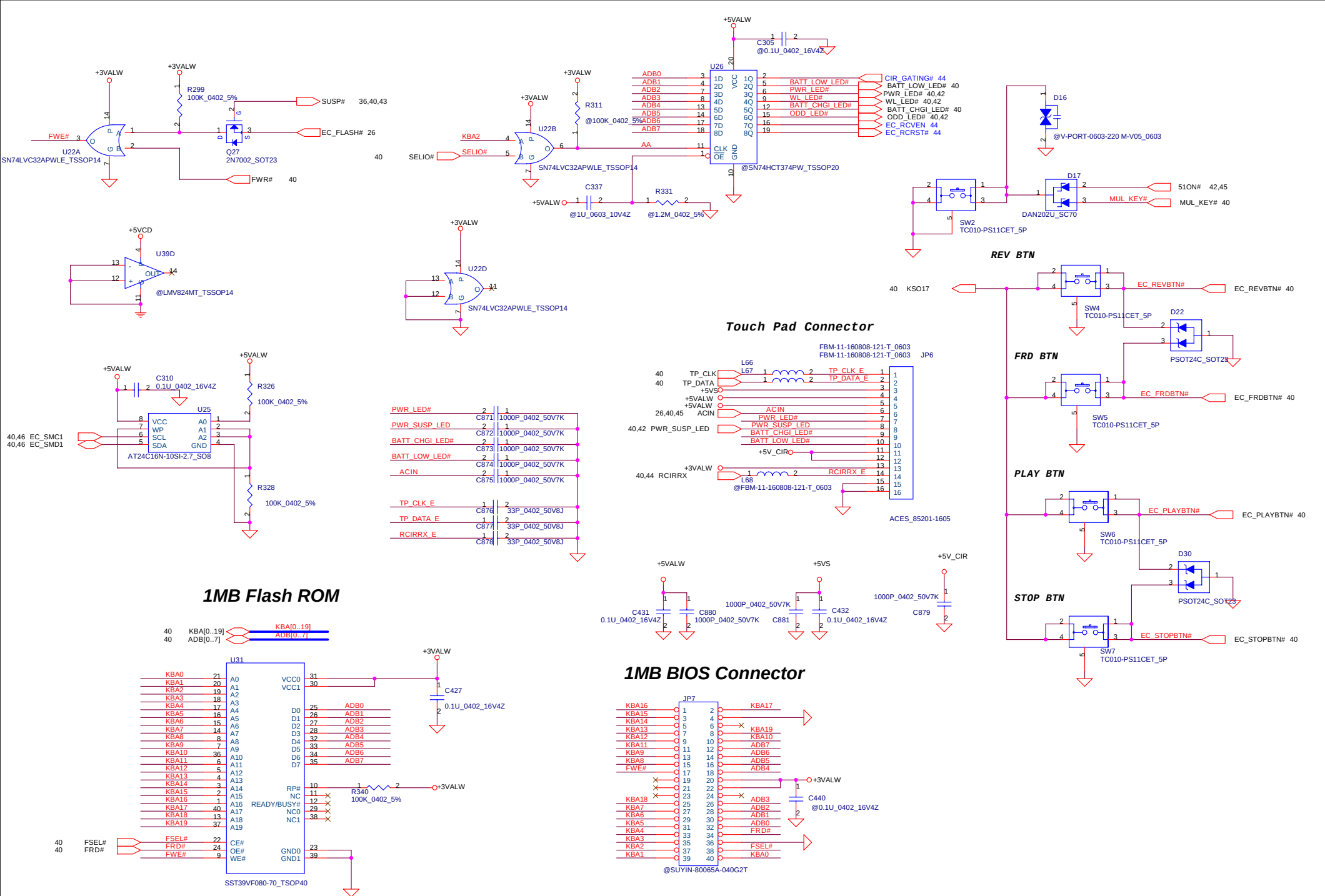
HDD CONNECTOR



**** 1029: Change U4D to U76D**







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Compal Electronics, Inc.			
Title			
BIOS & EXT. I/O PORT			
Size	Document Number	Rev	
Custom	LA-2371	1.0	
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[illegible][illegible]

Diagram showing six SMD40M80 components labeled CF1 through CF6, each with a red arrow pointing to a common ground symbol.

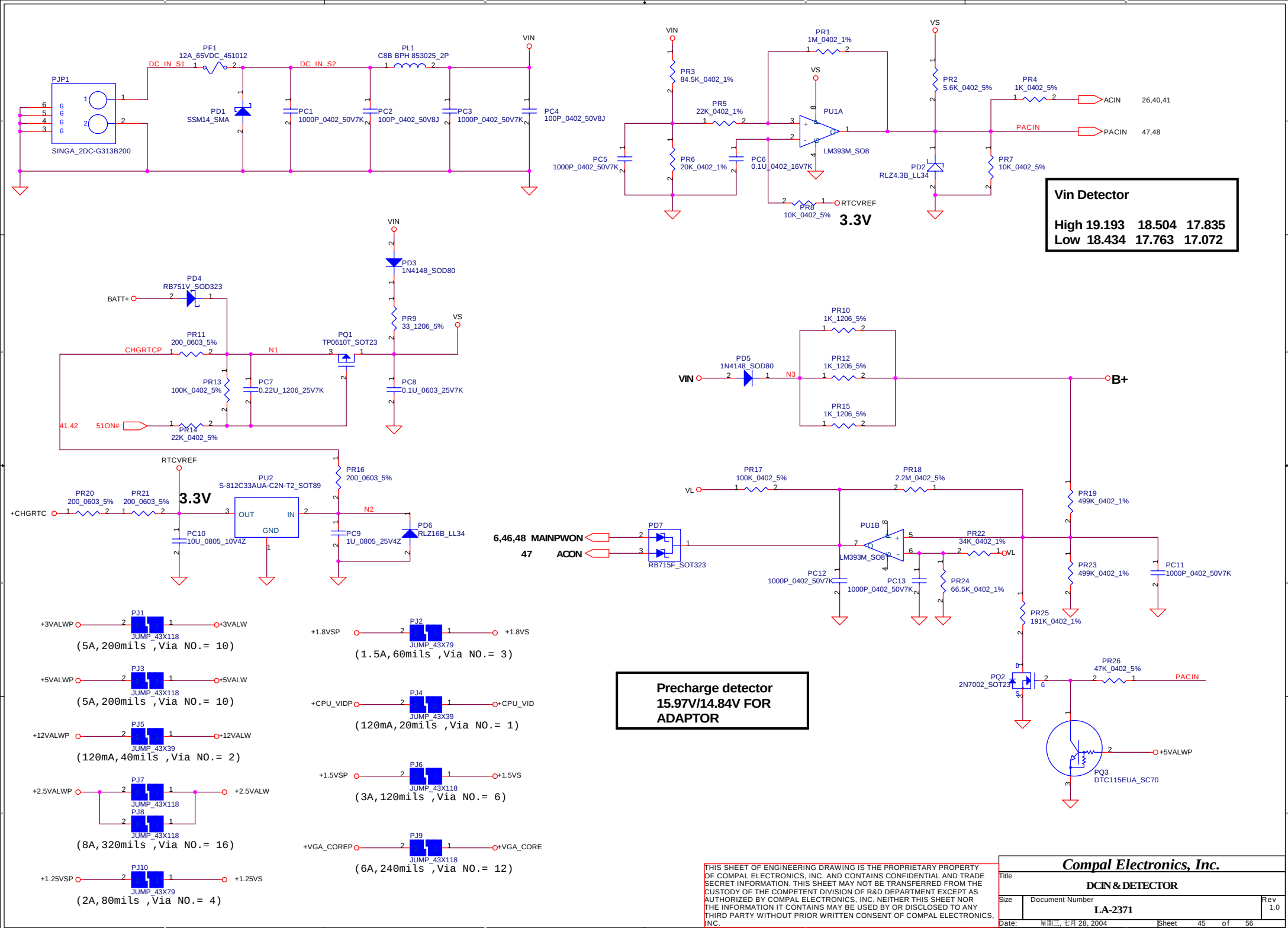
CF7 SMD40M80 CF8 SMD40M80 CF9 SMD40M80 CF10 SMD40M80 CF11 SMD40M80 CF12 SMD40M80

CF13 SMD40M80 CF14 SMD40M80 CF15 SMD40M80 CF16 SMD40M80 CF17 SMD40M80 CF18 SMD40M80

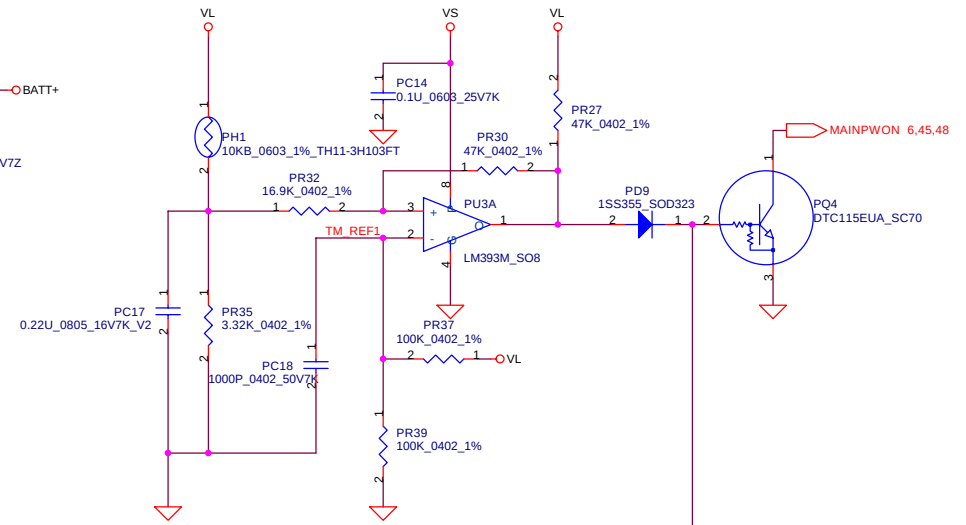
CF19 SMD40M80 CF20 SMD40M80 CF21 SMD40M80 CF22 SMD40M80

Title		POWER CONTROL CKT	
Size	Document Number	Rev	
Custom	LA-2371	1.	
Date	星期三, 七月 28, 2004	Sheet	43 of 56

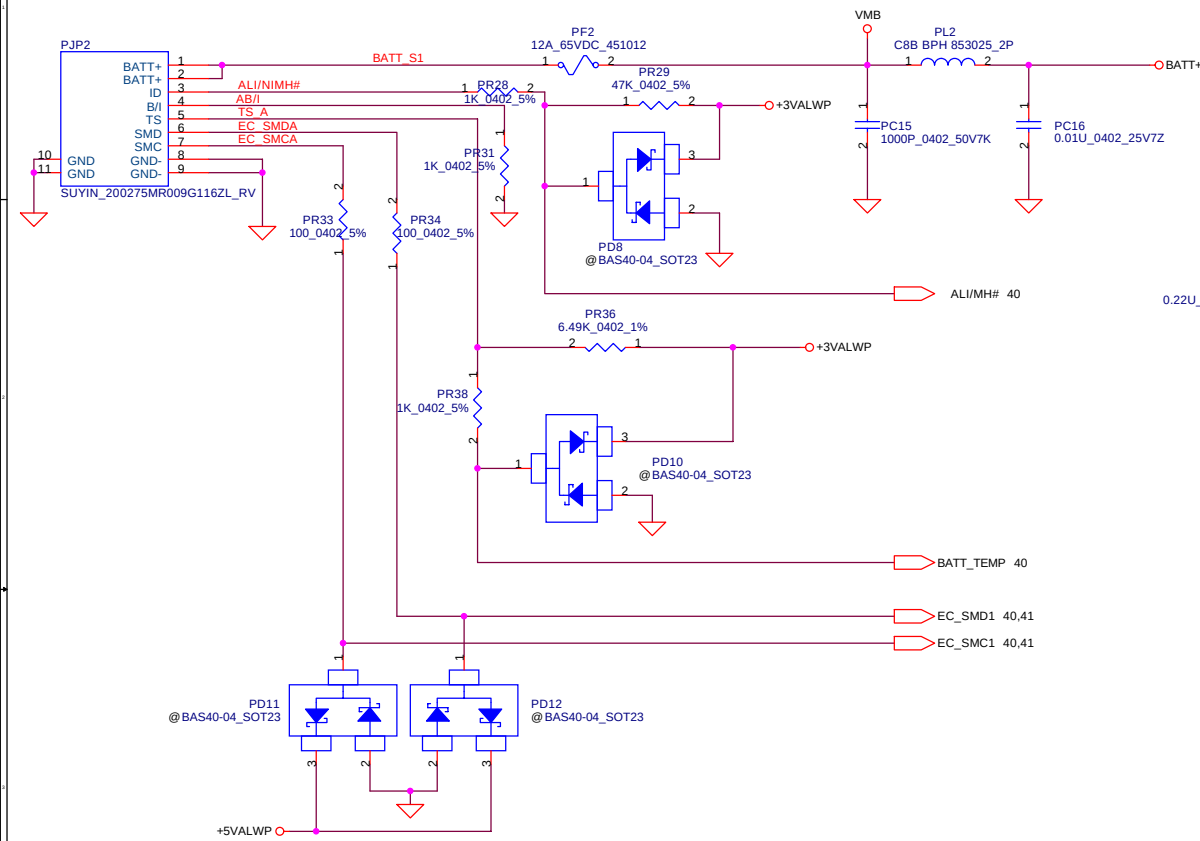
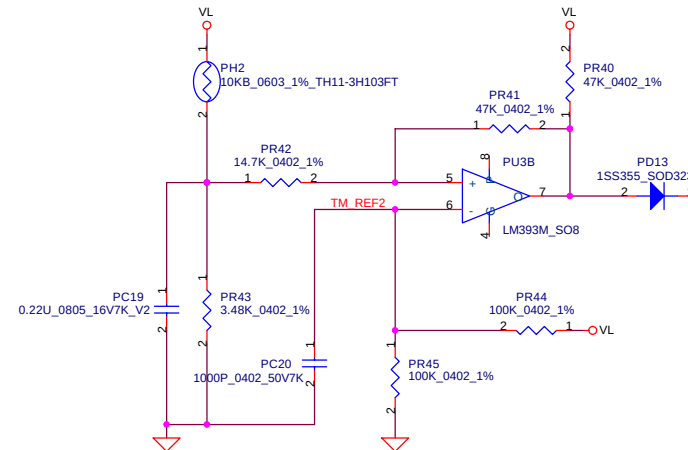
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PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C

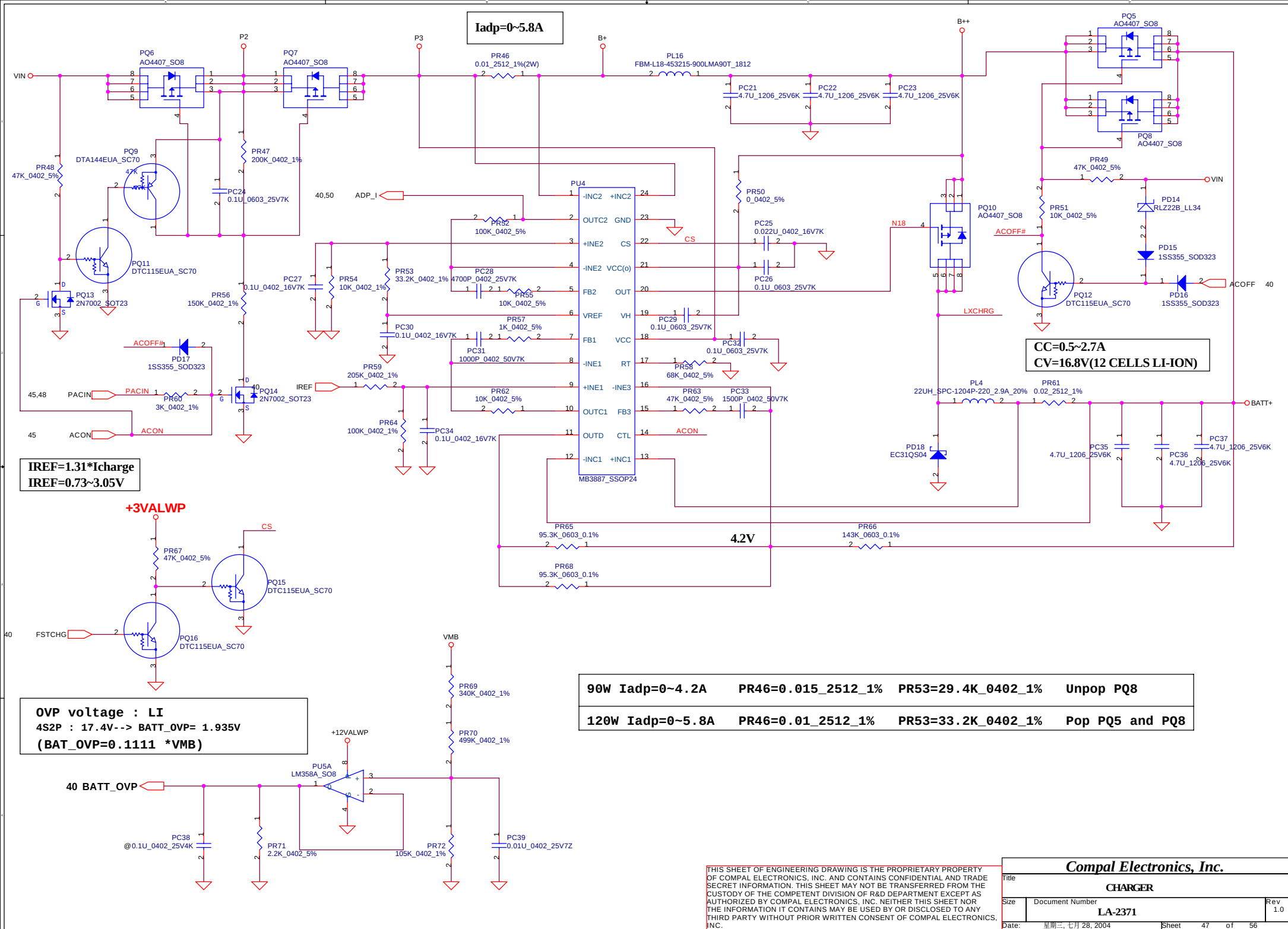


PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C



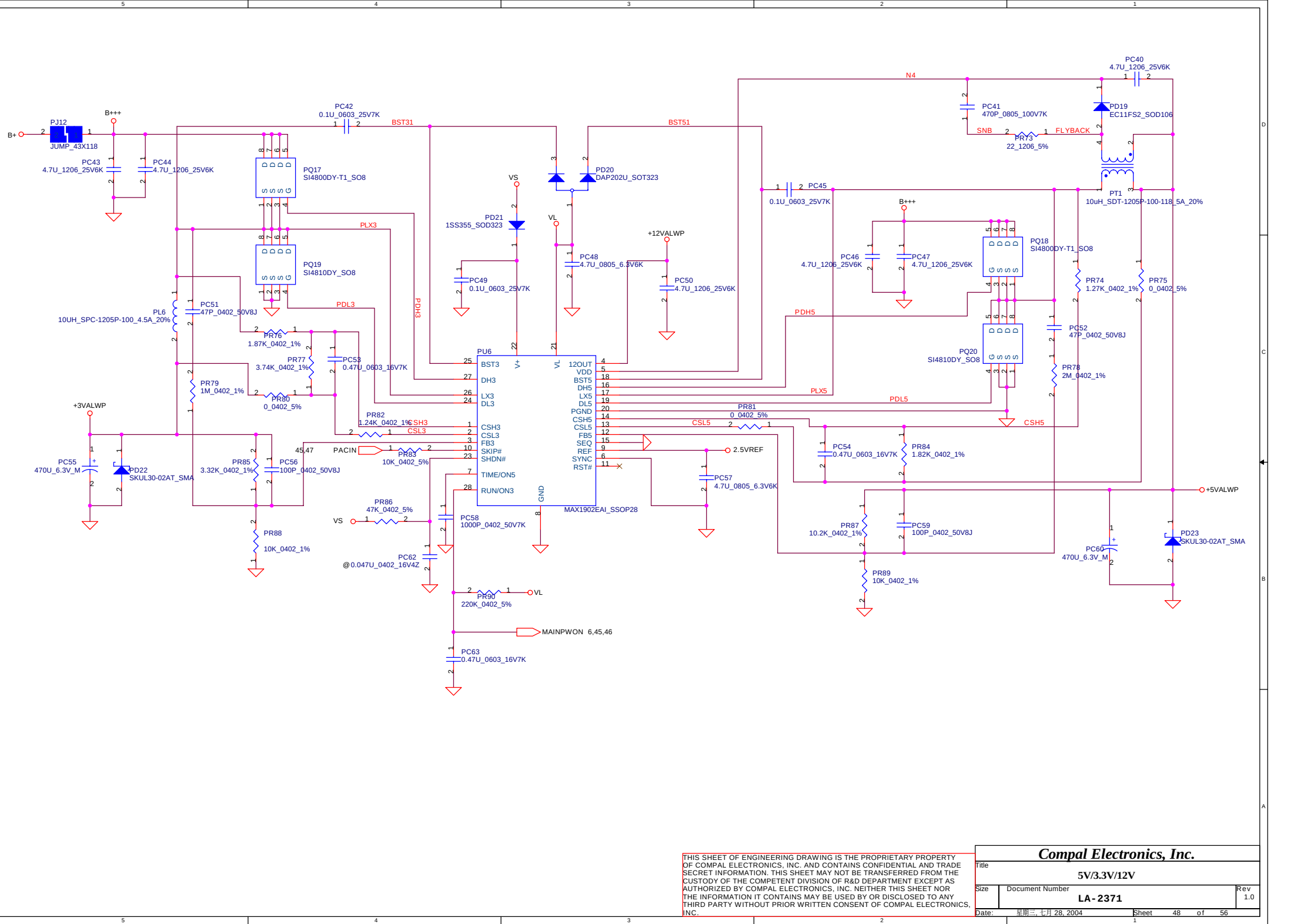
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Title			
BATTERY CONN/OTP			
Size	Document Number	Rev	
	LA-2371	1.0	
Date:	星期二, 七月 28, 2004	Sheet	46 of 56



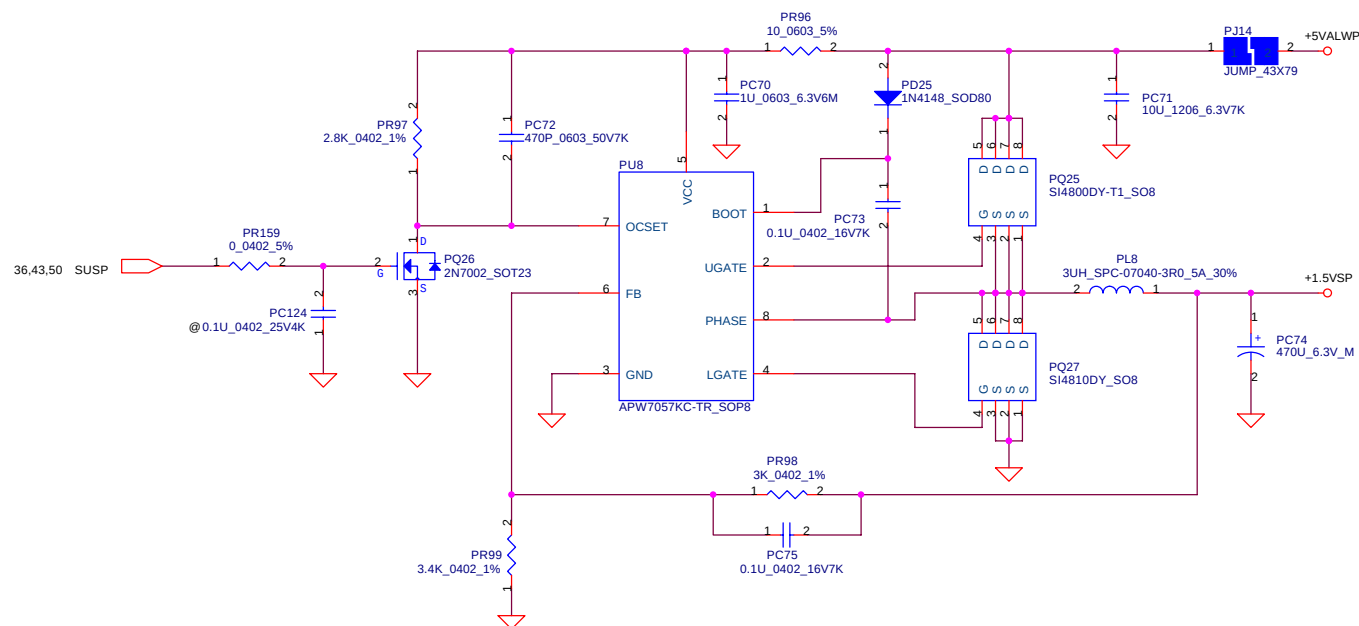
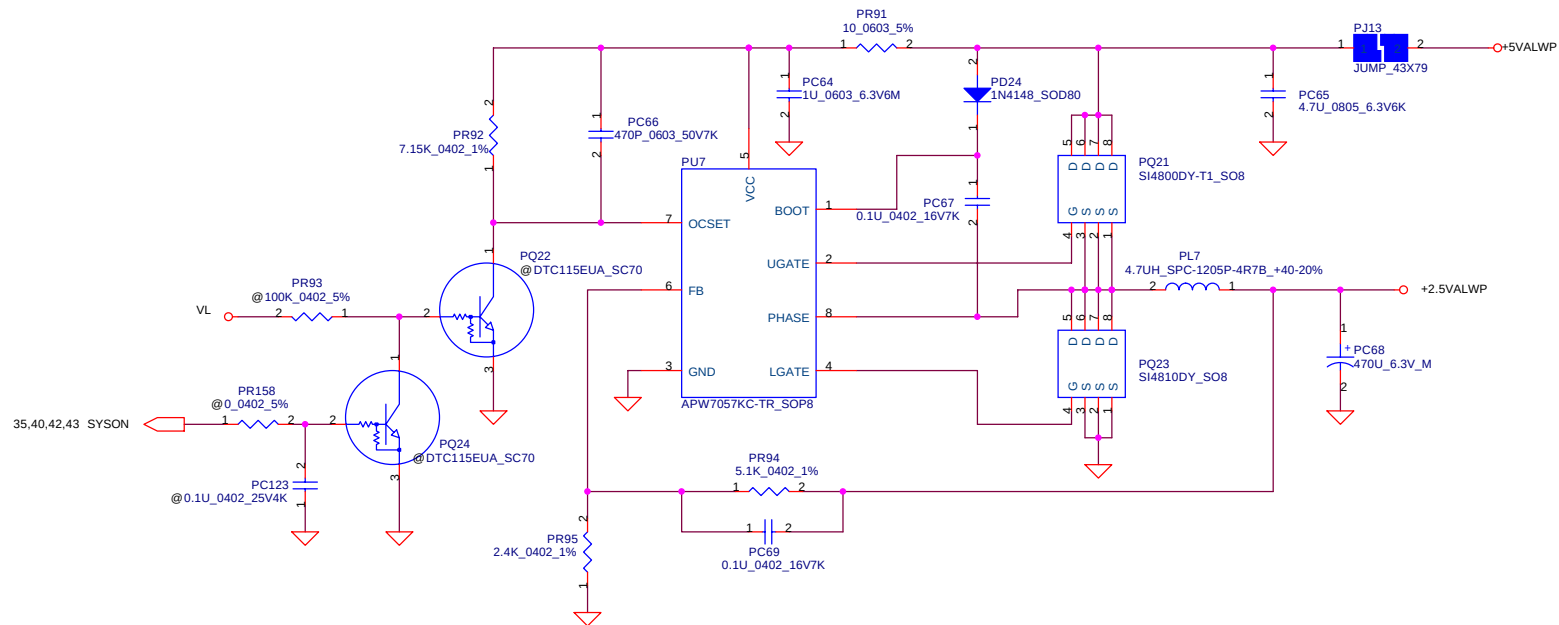
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Compal Electronics, Inc.			
CHARGER			
Size	Document Number	Rev	
	LA-2371	1.0	
Date:	星期三, 七月 28, 2004	Sheet	47 of 56



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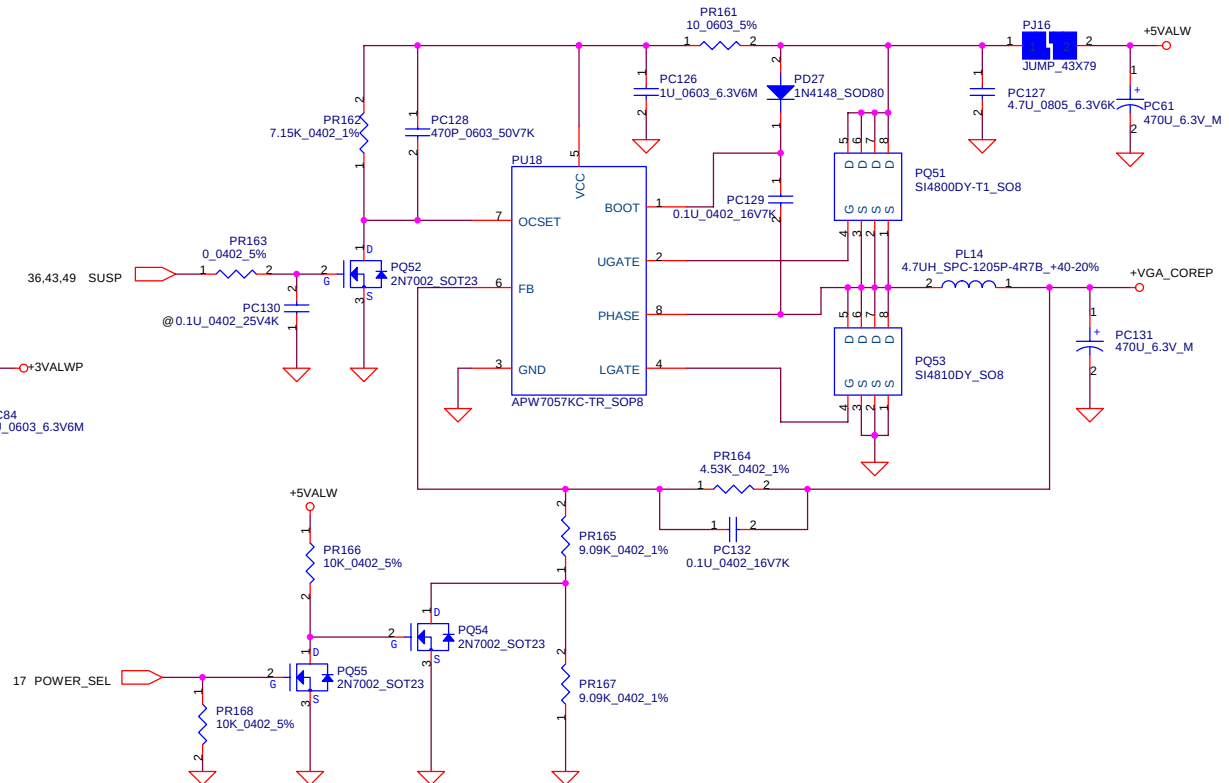
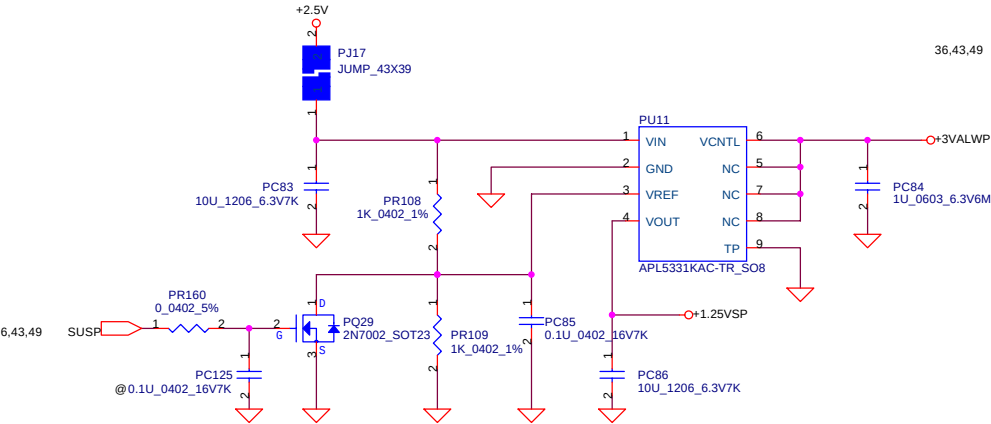
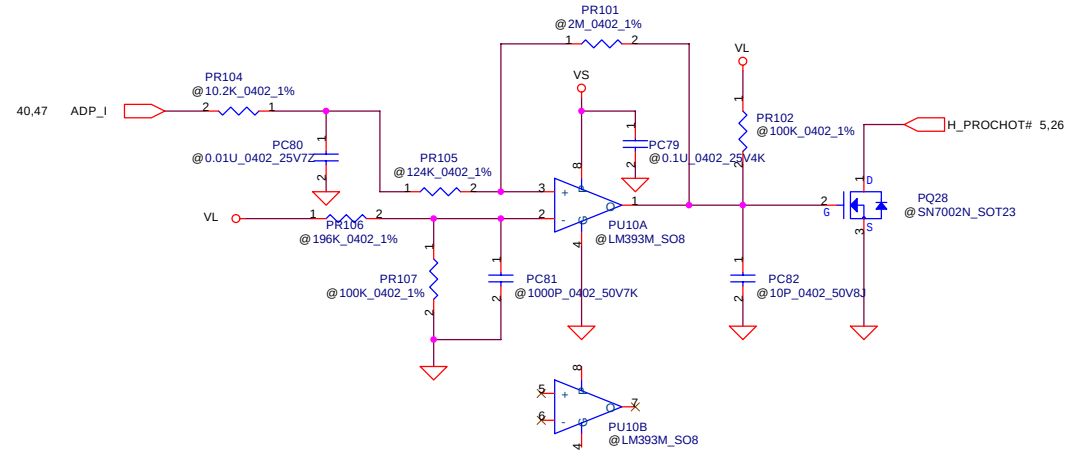
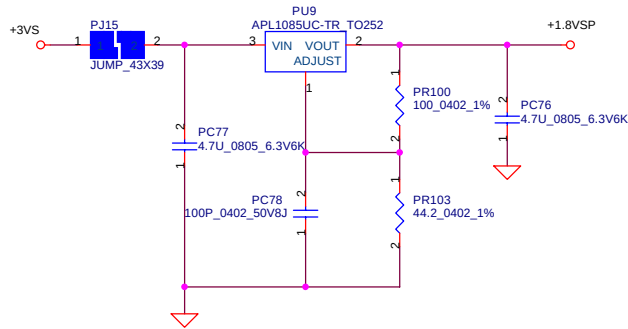
Title			5V/3.3V/12V		
Size			Document Number		
Date			Rev		
星期三, 七月 28, 2004			1.0		
Sheet			48 of 56		



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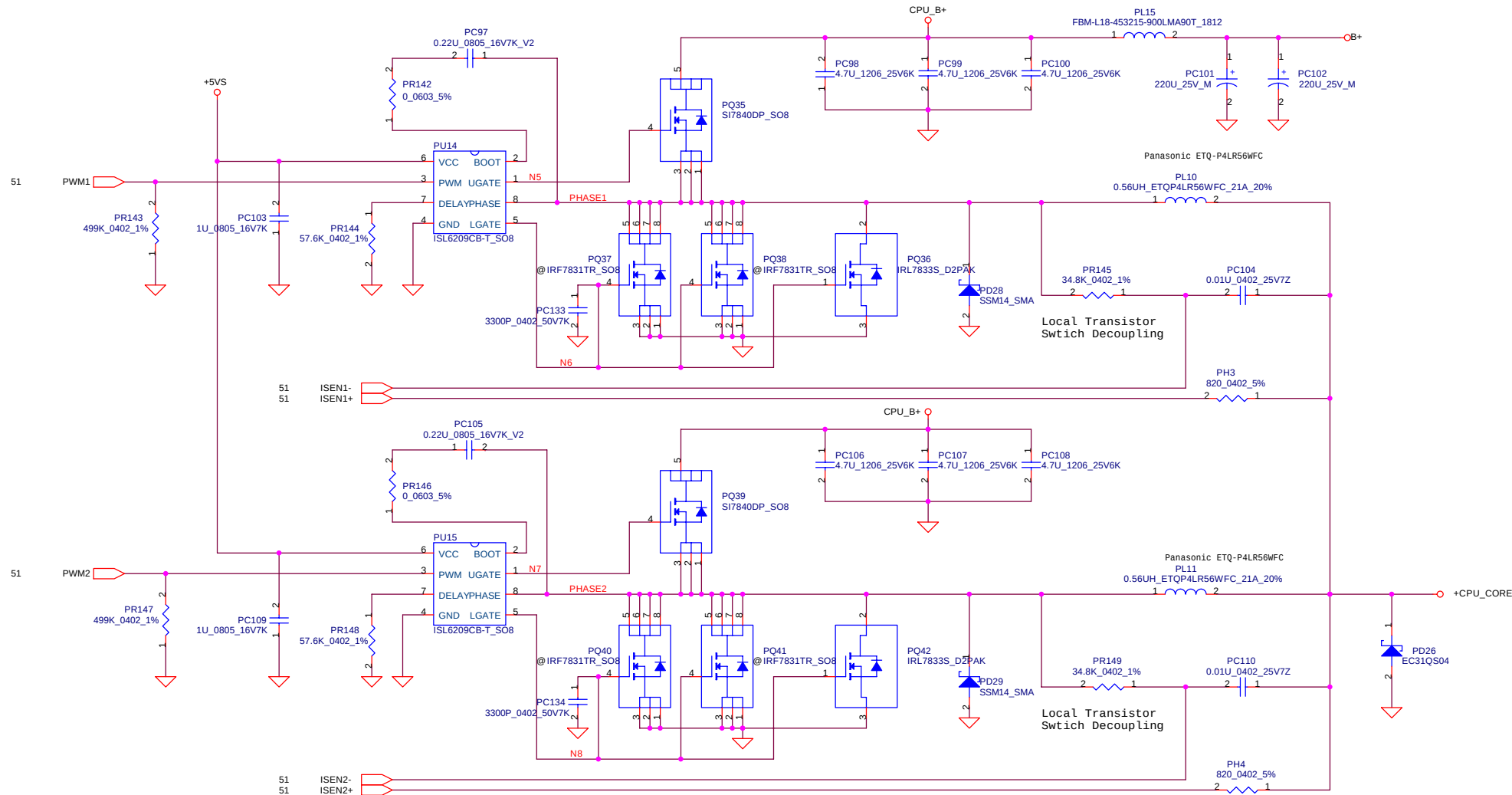
Compal Electronics, Inc.			
Title		2.5V/1.5V	
Size	Document Number		Rev
	LA - 2371		1.0
Date:	星期二, 七月 28, 2004	Sheet	49 of 56

85W THROTTLING 70W REVOVERY



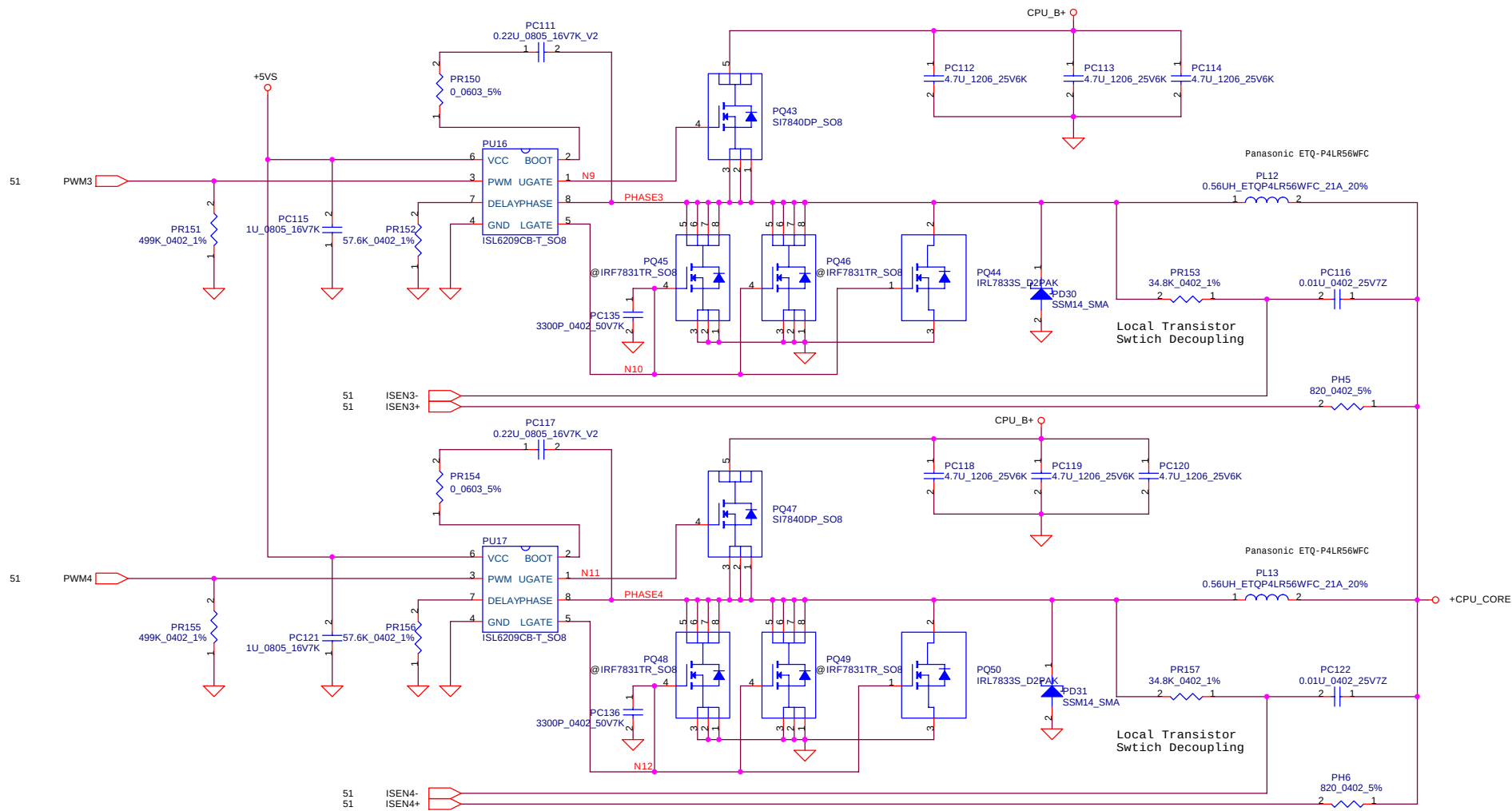
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Compal Electronics, Inc.			
Title			
1.8V/PROCHOT/1.25V/VGA			
Size	Document Number		Rev
	LA-2371		1.0
Date:	星期三, 七月 28, 2004		Sheet 50 of 56



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Compal Electronics, Inc.			
Title			
CPU_CORE (1)			
Size	Document Number	Rev	
	LA - 2371	1.0	
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Compal Electronics, Inc.			
Title			
CPU_CORE (2)			
Size	Document Number		Rev
	LA-2371		1.0
Date:	星期三, 七月 28, 2004		Sheet 53 of 56

POWER PIR LIST

page	Reason for change	Modify list
DVT	45,46,49,51	Update BOM
		Change PC7 form 0.022u to 0.22u(SE041224K03), PR36 from 25.5K to 6.49K(SD034649100)
		Change PC17,PC19 form 0.022u to 0.22u(SE030224KT1), PC71 from 4.7u to 10u(SE114106K00)
		Change PR130 from 340K to 681K(SD034681300)
	52	For EMI team request
	52	Solve noise issue
PVT		Add 2nd source
		Change PQ13,PQ14,PQ2,PQ26,PQ29,PQ30,PQ32,PQ33,PQ52,PQ54,PQ55 from SB570020500 to SB7700200T5
	45,47	For common part
		Change PD1 from EC10QS04(SC10QS041T4) to SSM14(SCSSSM14000)
		Change PD18 from RB051L(SC1B051L000) to EC31QS04(SC11QS04000)
	48	To decrease 3V/5V negative voltage
		Change PD22,PD23 from SSM14(SCSSSM14000) to SKUL30-02AT(SCSKUL30000)

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Compal Electronics, Inc.		
Title		
EFW00 PIR LIST		
Size	Document Number	Rev
B	LA-2371	1.0
Date: 星期二, 七月 27, 2004		
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
4/21	P.42	Move R57 to D8.2	Avoid leakage current	
	P.36	change footprint of U7	for SMT process	
	P.29	change footprint of U9	for SMT process	
	P.24	swap JP2 channel A and channel B pin	for LVDS Conn.issue	
4/22	P.36	Swap C38 & R54 location	For audio speak DC 2.5V level	
	P.36	Pop R55& R36 Depop R54	For Audio noise	
	P.36	mirror VR1	For Audio Volume smoothly	
	P.35	Del R611	For Audio clock 14.318MHz	
4/26	P.25	Add R771 pull high to +3VS	Modify IXP 150 GPIO pin	
	P.40	Add R772 & R773	To avoid RTCVCC loss in EC	
	P.40	Modify U15.90,U15.93,U15.94	To adjust SKU ID & BIOS ID	
4/27	P.31	Swap Jp31.19 and Jp31.25	For XD card issue	
	P.31	Change R746,R744,R751 power plane to +VCC_5IN1		
	P.31	Add R775 for Reserve		
	P.30	Add R774 for Reserve		
	P.30	Change R769 power plane to +VCC_5IN1		
	P.31	Add JP32 for Reserve		
	P.36	To change R220=3.3k,R233=4.7k,R239=4.3k	For Speak and HP Gain	
	P.36	Add R764,Del R468	For audio Gain adjust	
	P.36	To modfiy U7 CIS LIB	For Speaker can not mute when plug in HP	
4/30	P.24	Add L55,L57,C862,C864	for EMI issue	
	P.38	Add L63-L65	for EMI issue	
	P.26	Add L58,C866	for EMI issue	
	P.36	Add L59-L62	for EMI issue	
	P.29	Add L71,L72 / Del R97,R106 / Change L13	for EMI issue	
	P.25	Change R661,R658,R662,R665,R651,R654,R668,R315	for EMI issue	
	P.40	Pop CP1-CP6	for EMI issue	
	P.41	Add C871-C881,L66-L68	for EMI issue	
	P.43	Add L69,L70	for EMI issue	
	P.35	Change U46 CIS to ALC250 ver. C	for direct CD play issue	
5/3	P.40	Re-define EC_URXD/EC_UTXD/KS017 pin assignment	for CIR function	
	P.40	Add C882	for SKU ID	
5/4	P.24	Depop R58,R48/Pop U4,C39	for S3 panel garbage	
	P.38	Add U55	for G528 reserve	
	P.38	JP16 modify Layout LIB	for reverse type	
	P.38	Change Power from +USB_AS to USB_BS	for reverse type	
	P.24	Move R58 to Q4.2	for reserve	
	P.30	Add R776	for SM_CD# pull high	
	P.31	Define 5IN1 CONN. SM_CD# signal	for SM card protect	
5/5	P.17	Modify VRAM strap pin, Add R30	for 32MB/64MB/128MB	
5/6	P.26	Change R388 to 12K	for USB eyediagram	
	P.31	Depop R749/ Change R746,R744,R742 to 10K,Change R751 to 2.2K	for ENE suggestion	
	P.30	Depop R749,R735,R732,R727,R731,R738,R768,R741,R719/Pop R770/Change R768 to 2.2K	for ENE suggestion	
	P.42	Add Hibernation circuit	for S4 function	
	P.24	Change D25,D54 symbol	for 1N4148 Cache LIB	
	P.40	Re-define S4_DATA,S4_LATCH	for Hibernation function	
5/7	P.33	Change +5VS_miniPCI to +5VS	for Lifeview SPEC.	
	P.7	Add R785-R788,D59,D60	For ATI suggestion	
	P.35	Add C860,C861	For Analog TV sound	
	P.31	Add R789	For 5in1 issue	
5/8	P.40	Add R790,C888	for Battery.	
	P.23	Add L73-L75	For EMI issue	
	P.31	Change R718 to 43K	For 5IN1 function	
5/10	P.40	Change RCIRRXX to 76 pin	For CIS function	
	P.40	Add R791	For RCIRRXX pull high +3valw	
5/11	P.38	Reserve JP33,R792,R793	for debug	
	P.36	Add C889	For Audio noise	
	P.26	Del Q32,R317,R312,R318	For ATI suggestion	
5/12	P.28	Change R323,R332 to 300K/pop R736 10K	for power on sequence	
	P.23	Add Jump from RF GND to Digital GND	for EMI&ESD	
5/13	P.40	Reserve R794	for avoid "Po" noise when power on/off	
	P.30	Add R795	for "Po" noise test	
	P.34	Change IEEE 1394 to VT6301S	for cost down	

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
5/17	P.24	Add C862,C864	for EMI issue	
	P.43	Add H54	for ME	
	P.44	Change R406 to 22ohm	for modem function	
	P.23	Change R7,R437 to 4.7kohm	for CRT function	
5/18	P.39	Reserve L77 from CD_AGND to Digital GND	for Audio noise test	
	P.23	Add R809	for GPIO pin	
5/20	P.31	Add Q67,R810,R811,R812	for Audio noise test	
5/20	P.31	Add U22C OR gate	for Audio P0 sound	
=====Rev0.3=====				
6/17	write by Timo Teng			
P.27	Add R813	For S/W DJ Function		
P.31	Add C904, C905, C906 C907	For 5 in 1 card transfor noise		
P.35	Add R820	For BITCLK smooth		
	Add R822, R823, @ in L40			
	del @ in L50	For Audio noise		
P.36	Add @10k in R179, R189, R184 and R196	For SWDJ		
	Del R95, R98, C112, C110	For Cost down		
P.37	Del Hardware EQ circuits			
	Add APA2121 Audio Amplifier circuits	For Cost down		
P.40	Add GPIO at pin98, 97,92,85,86 of KB910	For cost down		
	Del @ inR773 and Add @ in R772	For RTC power saving		
P.41	Add @ in U26, C305, R311, C337 and R331	For cost down		
P.42	R235 pull up voltage from +5VS to +SVALW	For SWDJ LED		
P.43	H37 connects to GND			
P.43	Add @ in all CIR circuits.	For Del CIR function.		
6/21	write by Timo Teng			
P.20	Add C920			
	Change C230 value from 150uF to 220uF	For VGA_CORE stable.		
P.42	Change value of R235, R142 and R452 from 300 to 180 ohms	For cost down		
6/22	write by Timo Teng			
P.23	Del JP13, JP3, JP14, J1, L73, L74, L75	For take out TV turner		
P.31	Add @ into R743 and C847	For some SD Card can't be detected		
P.35	Add C922	For decrease Bo sound in Dos Mode		
P.36	Add R98, R95, C112, C110	For SWDJ if the SMBUS can't be programed		
P.37	Add R823, R824, C923, C924, C925	For SWDJ if the SMBUS can't be programed		
P.41	Add @ in L68	For take out CIR function.		
	Del C336, U33	For Del 512KB flash ROM		
6/23	write by Timo Teng			
P.40	Del CP1-CP6			
	Add C926-C949	For EMI Cost down		
6/27	write by Timo Teng			
P.24	Change Value of C26 from 1000P to 0.047U	For SWDJ backlight getting off		

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
7/1	P.30	Connect U52.M11 to U52.J9	for follow Fortworth definition	
	P.43	Del H52,H53	for layout modify	
	P.43	Reserve C950,C951,C952	for EMI test	
7/12	P.11	Del C567,C545 and Add C953	for Cost down	
=====Rev1.0=====				
7/23	write by Timo Teng			
P.23	Change R443,R440,R438,R442,R441,R439 from 75_0402.5% to 75_0402_1%			
P.25	Change R643 from 330 to 130 ohm	For TPDL issue		
	Add @ in R668	For EMI request		
P.26	Change R388 from 12K to 11.5K ohm	For USB2.0 quality		
P.34	Add @ in R802	For VIA recomanation		
P.36	Del R98, R95,C112, C110	For Harman request		
P.37	Add @ in APA2121 circuits			
P.38	Add @ in U5 and Super I/O circuits.			
	Del @ in U55			

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File

PIR LIST-2

Doc#

Document Number

LA-2371

Rev

1.0

P.40 Change R175 and R176 from 0 to 1K ohm
Add @ in R172

P.42 Modify S4 resume circuit

7/27 Write by Timo Teng

P.24 R31,R34,R32,R33 from 75_0402_5% to 1%

P.31 Add R825
Change 789 from 43K to 10K

P.36 Change JP10 and JP11 from ACES 85204-0200 to ACES 85205-0200

P.40 Add C954 at pin176 of U15

7/28 Write by Timo Teng

P.30 Add R826
Change R721 from 33 to 22 ohm

P.30 Del R743

For solve KB910 into test mode
For LPDPC doesn't be used
For solve KB910 into test mode

For solve power switch ripple
For ME request
For FAN2 test Fail

For SD Card Function