

COMPAL CONFIDENTIAL

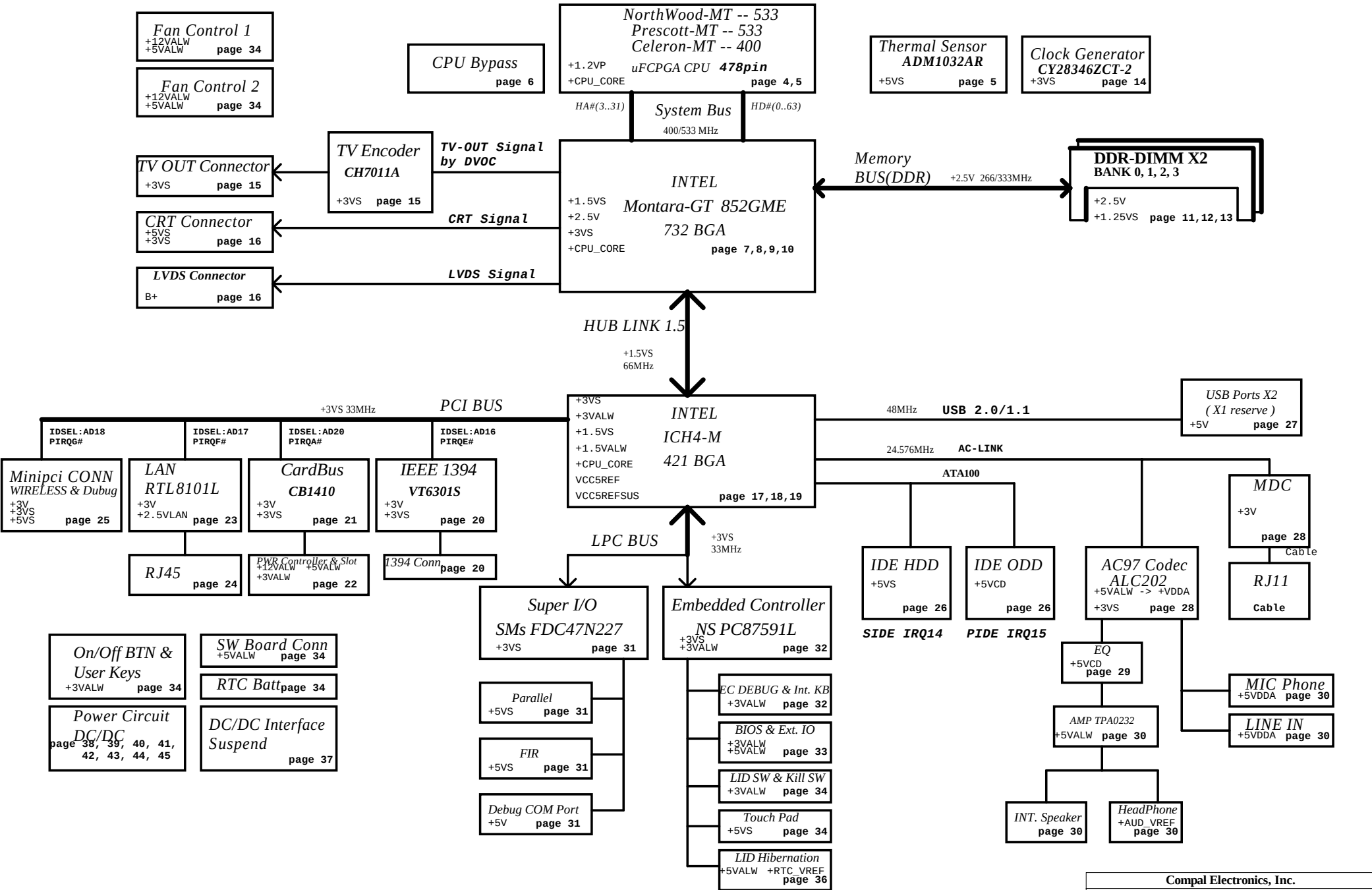
MODEL NAME : *DBL10 -- Sapporo X*
COMPAL P/N : *DA8BL10L010*
PCB NO : *LA-1931*
Revision : *1.0*

DBL10 -- Sapporo X Schematics Document
uFCBGA/uFCPGA NorthWood MT
2003-09-19 v1.0

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Model : DBL10 -- Sapporo X



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.2V	1.2V switched power rail for CPU AGTL Bus	ON	ON	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON
+RTCBATT	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices (follow PCI IRQ routing plannig ver0.2.04)

Device	IDSEL#	REQ#/GNT#	Interrupts - (ICH4-M)
CardBus (ENE-CB1410)	AD20	2	PIRQA#
IEEE 1394 (VIA-VT6301S)	AD16	0	PIRQE#
LAN (Realtek-RTL8101L)	AD17	3	PIRQF#
Mini-PCI	AD18	1 INTA#/INTB#	PIRQG# / PIRQH#

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16)	1010 000X b		

EC SM Bus2 address

ICH4 SM Bus address

Device	Address
CLK GEN (ICS-950810)	1101 001X

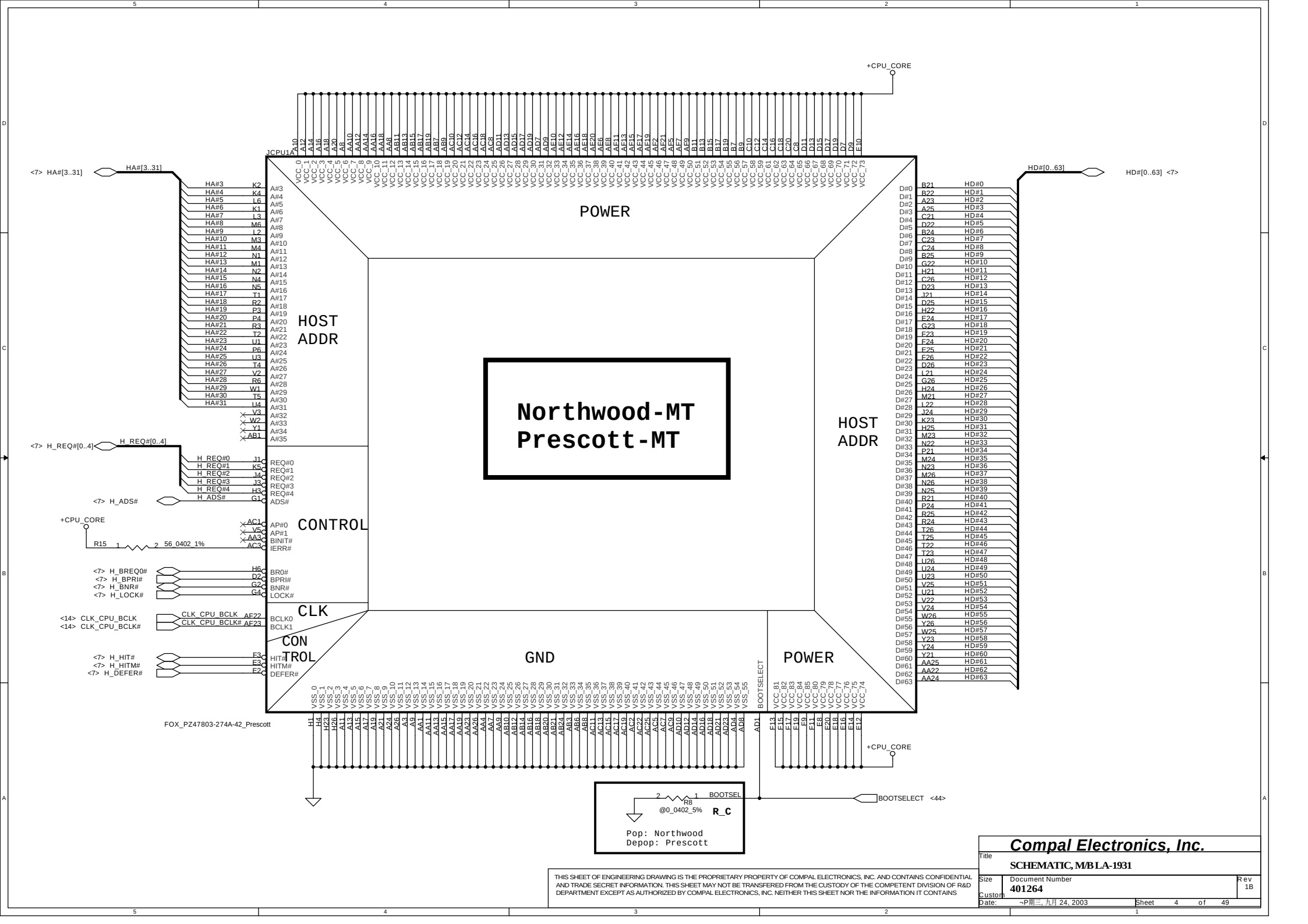
Power Managment table

Signal State	+1.5VALW +3VALW +5VALW +12VALW	+5V +3V +2.5V +1.2V	+5VS +3VS +1.5VS +CPU_CORE +1.25VS
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

Board ID Table for AD channel

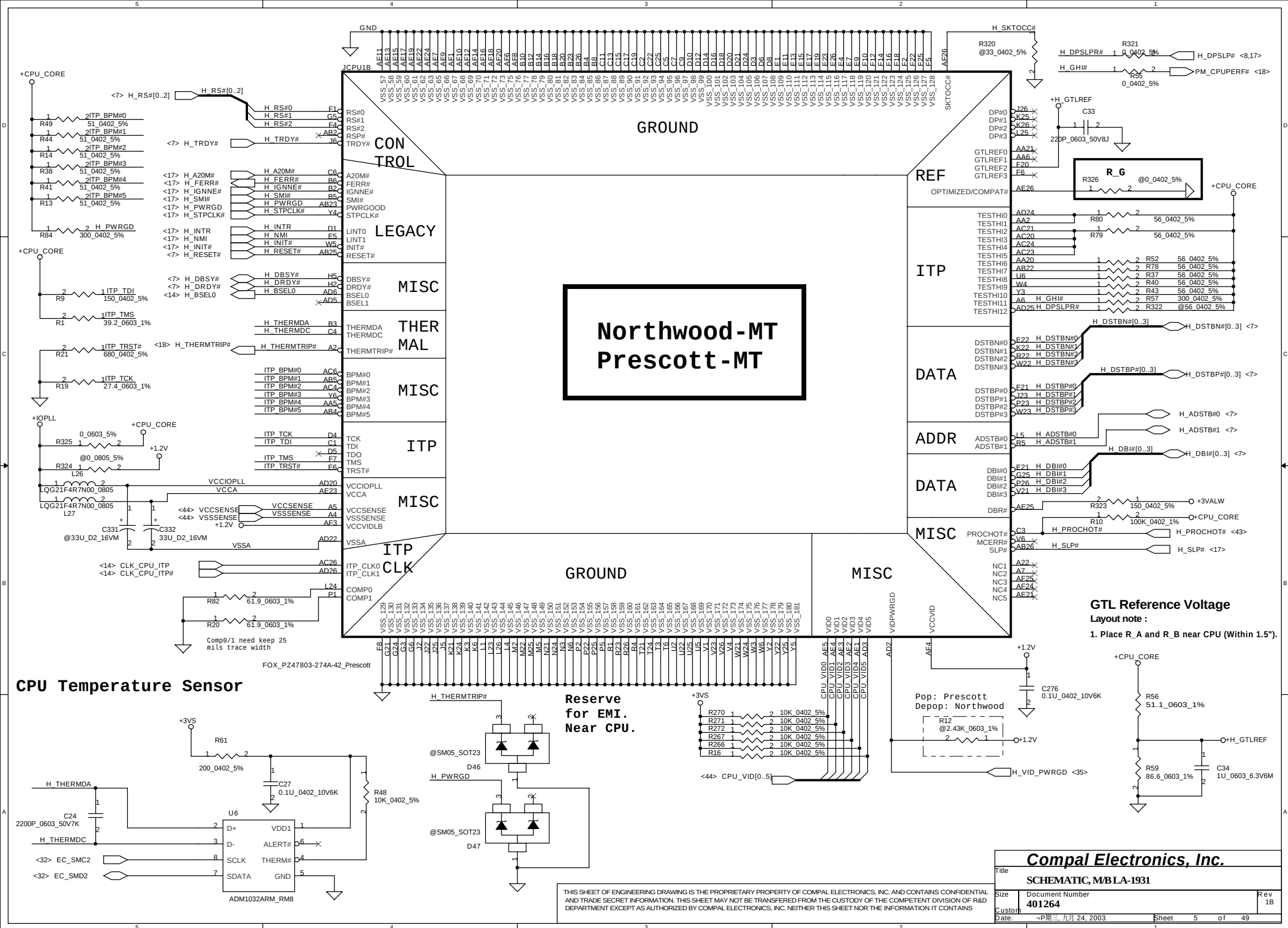
Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 1%	0.216 V	0.250 V	0.289 V
2	18K +/- 1%	0.436 V	0.503 V	0.538 V
3	33K +/- 1%	0.712 V	0.819 V	0.875 V
4	56K +/- 1%	1.036 V	1.185 V	1.264 V
5	100K +/- 1%	1.453 V	1.650 V	1.759 V
6	200K +/- 1%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	



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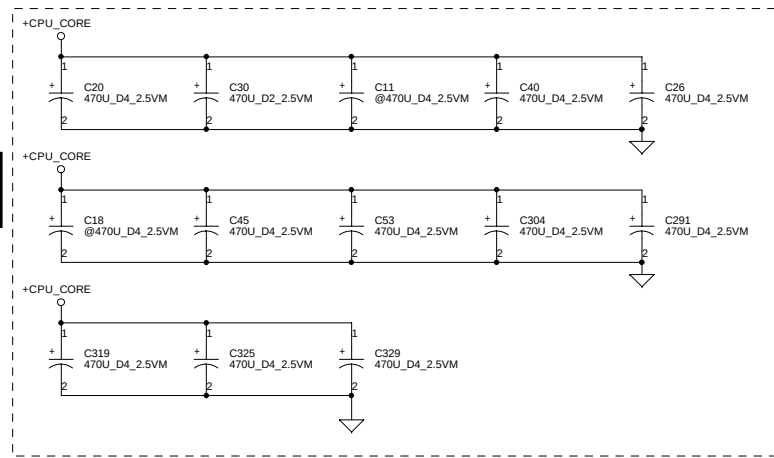
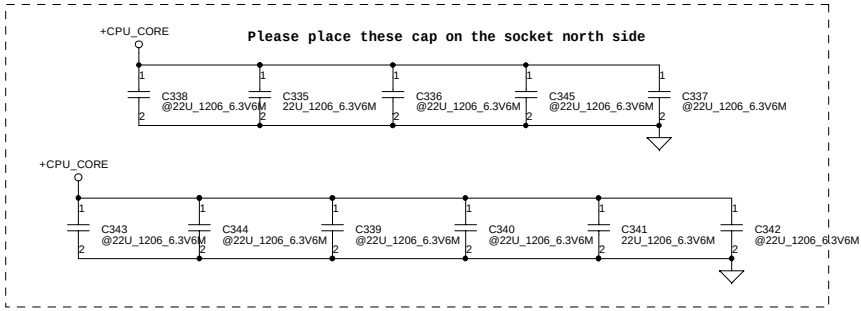
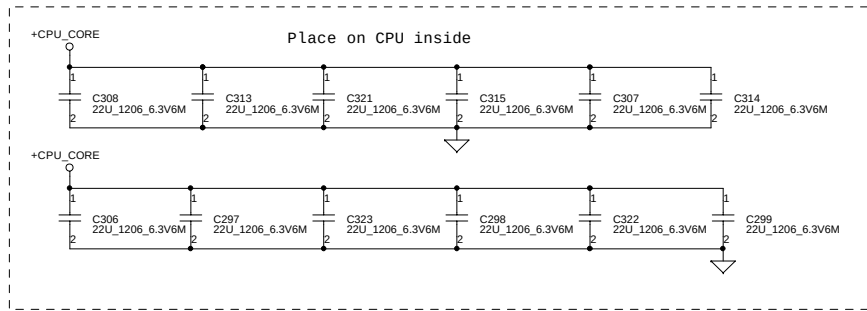
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Layout note :
Place close to CPU. Use 2-3 vias per PAD.
Place 22uF caps x31 pcs, populated 14pcs.

Layout note :
Place close to CPU power and ground pin as possible (<1inch)

For Desktop's CPU:
470uFx15/12mOhm H=1.8 each
Total 0.923m ohm





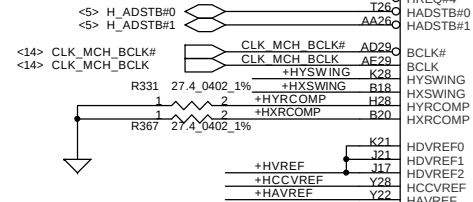
U26A

Montara-GT

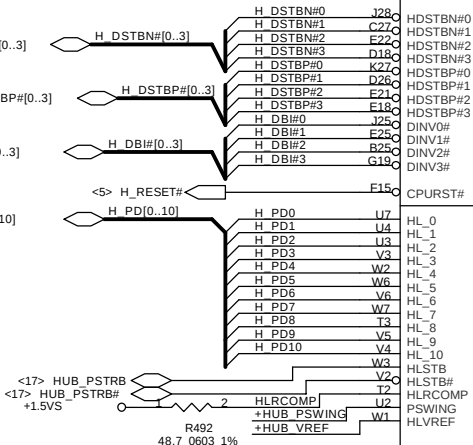
HA#3	P23C	HA#3
HA#4	T25C	HA#4
HA#5	T28C	HA#5
HA#6	R27C	HA#6
HA#7	U23C	HA#7
HA#8	U24C	HA#8
HA#9	U24C	HA#9
HA#10	U28C	HA#10
HA#11	V28C	HA#11
HA#12	U27C	HA#12
HA#13	T27C	HA#13
HA#14	V27C	HA#14
HA#15	V25C	HA#15
HA#16	V26C	HA#16
HA#17	Y24C	HA#17
HA#18	V25C	HA#18
HA#19	V23C	HA#19
HA#20	W25C	HA#20
HA#21	Y25C	HA#21
HA#22	AA27C	HA#22
HA#23	W24C	HA#23
HA#24	W23C	HA#24
HA#25	W27C	HA#25
HA#26	Y27C	HA#26
HA#27	AA28C	HA#27
HA#28	W28C	HA#28
HA#29	AB27C	HA#29
HA#30	Y26C	HA#30
HA#31	AB28C	HA#31

HD#0	HD#0
H27	HD#1
K25	HD#2
HD#2	HD#3
L24	HD#4
J27	HD#5
G28	HD#6
L27	HD#7
L23	HD#8
L25	HD#9
J24	HD#10
HD#9	HD#11
H25	HD#12
K27	HD#13
G27	HD#14
K28	HD#15
J23	HD#16
HD#13	HD#17
H26	HD#18
E25	HD#19
E26	HD#20
B27	HD#21
H23	HD#22
E27	HD#23
G25	HD#24
HD#21	HD#25
E28	HD#26
D27	HD#27
G24	HD#28
C28	HD#29
G22	HD#30
C26	HD#31
HD#28	HD#32
E26	HD#33
G23	HD#34
B28	HD#35
C21	HD#36
G21	HD#37
D22	HD#38
C25	HD#39
E24	HD#40
G20	HD#41
B22	HD#42
B23	HD#43
E23	HD#44
C21	HD#45
G17	HD#46
G18	HD#47
E19	HD#48
E20	HD#49
D20	HD#50
F19	HD#51
C19	HD#52
C17	HD#53
F17	HD#54
B19	HD#55
G16	HD#56
E18	HD#57
C16	HD#58
E17	HD#59
D16	HD#60
C18	HD#61
HD#63	HD#62

HOST

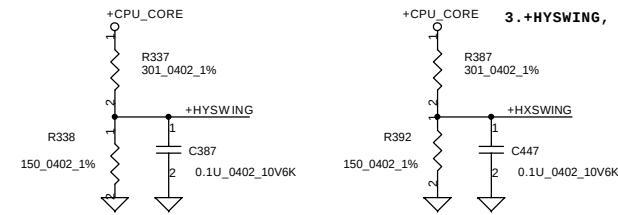


HUB I/F



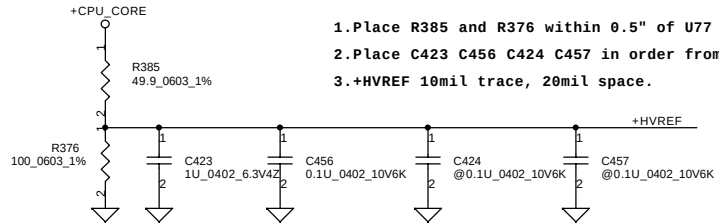
RG82G4350MA1_UFCBGA732_MONTARA-GT

HXSWING and HYSWING Ref. Voltage



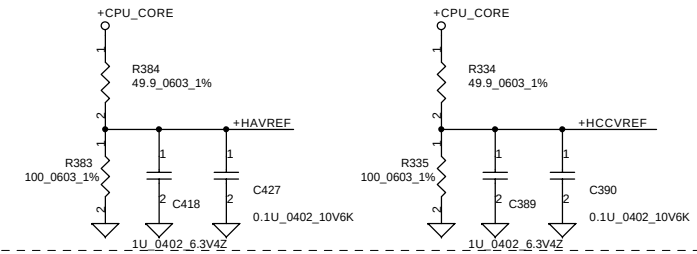
- 1.Place R337 and R338 within 0.5" of U77 pin K28
- 2.Place R387 and R392 within 0.5" of U77 pin B18
- 3.+HYSWING, +HXSWING 10mil trace, 20mil space.

Host data Ref. Voltage

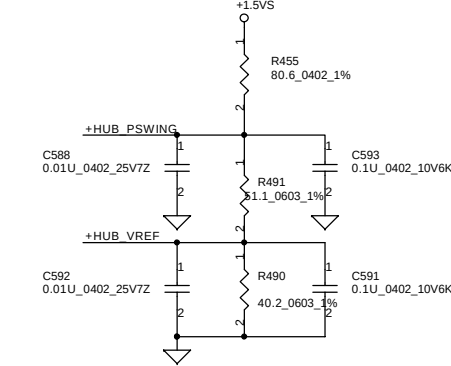


- 1.Place R385 and R376 within 0.5" of U77 pin K21 J21 J17
- 2.Place C423 C456 C424 C457 in order from U77 to divider
- 3.+HVREF 10mil trace, 20mil space.

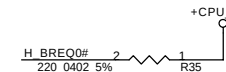
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HUBLink reference Voltage



Placed by GMCH

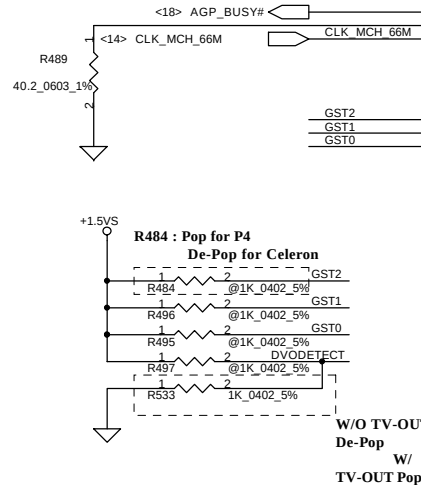
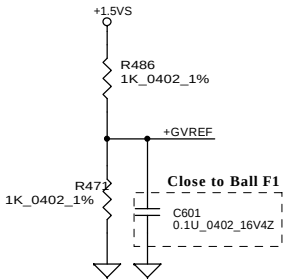
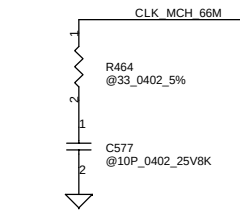
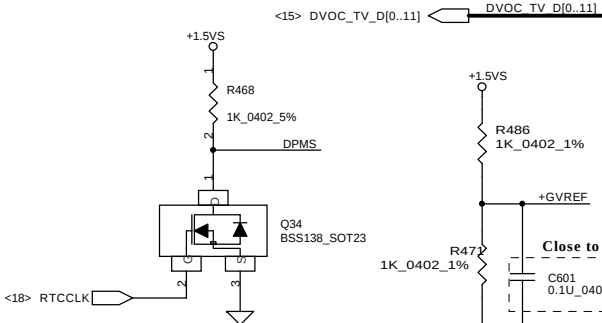
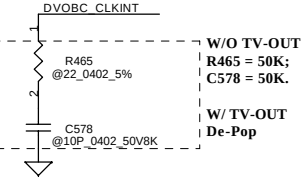
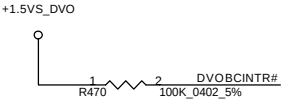
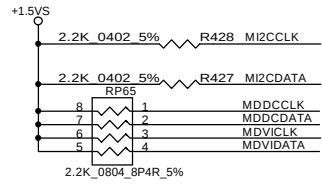


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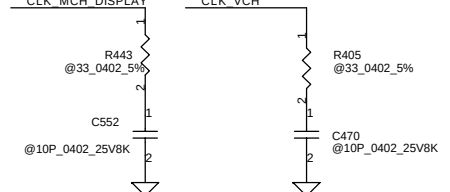
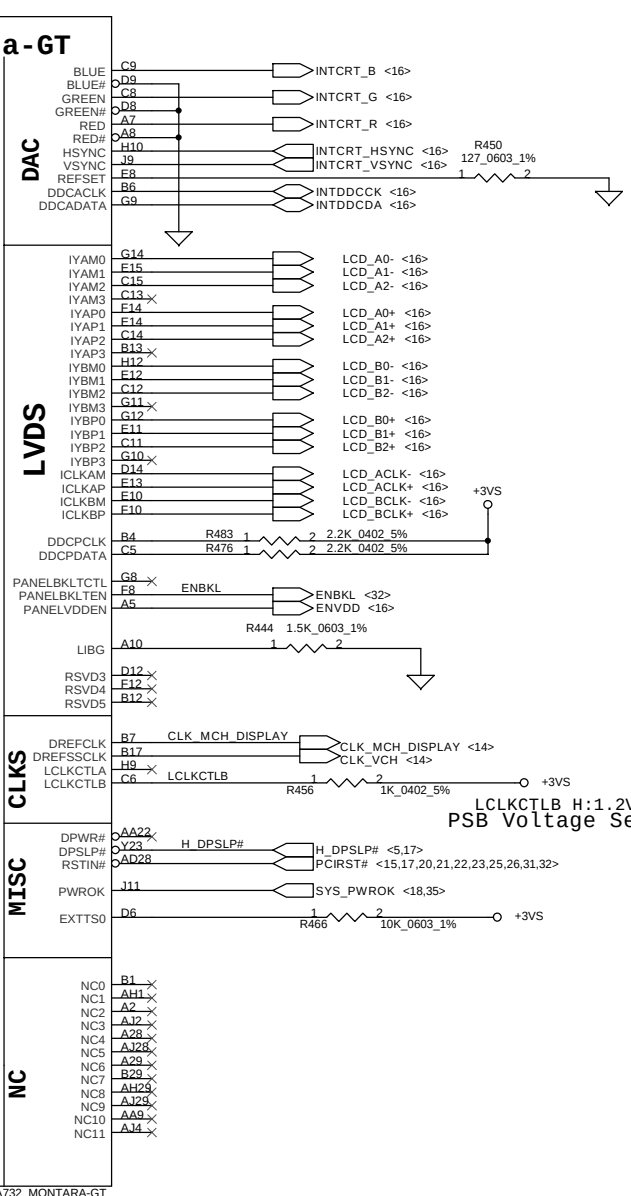
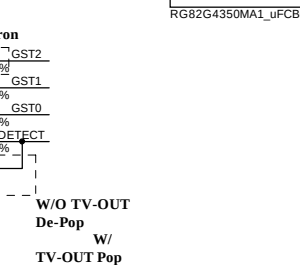
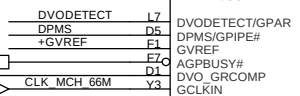
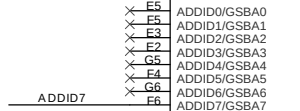
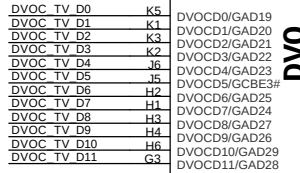
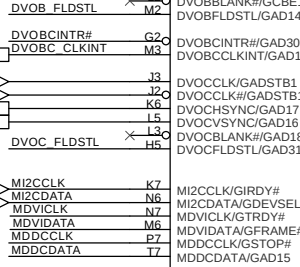
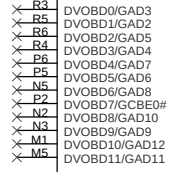
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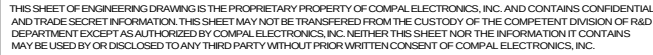
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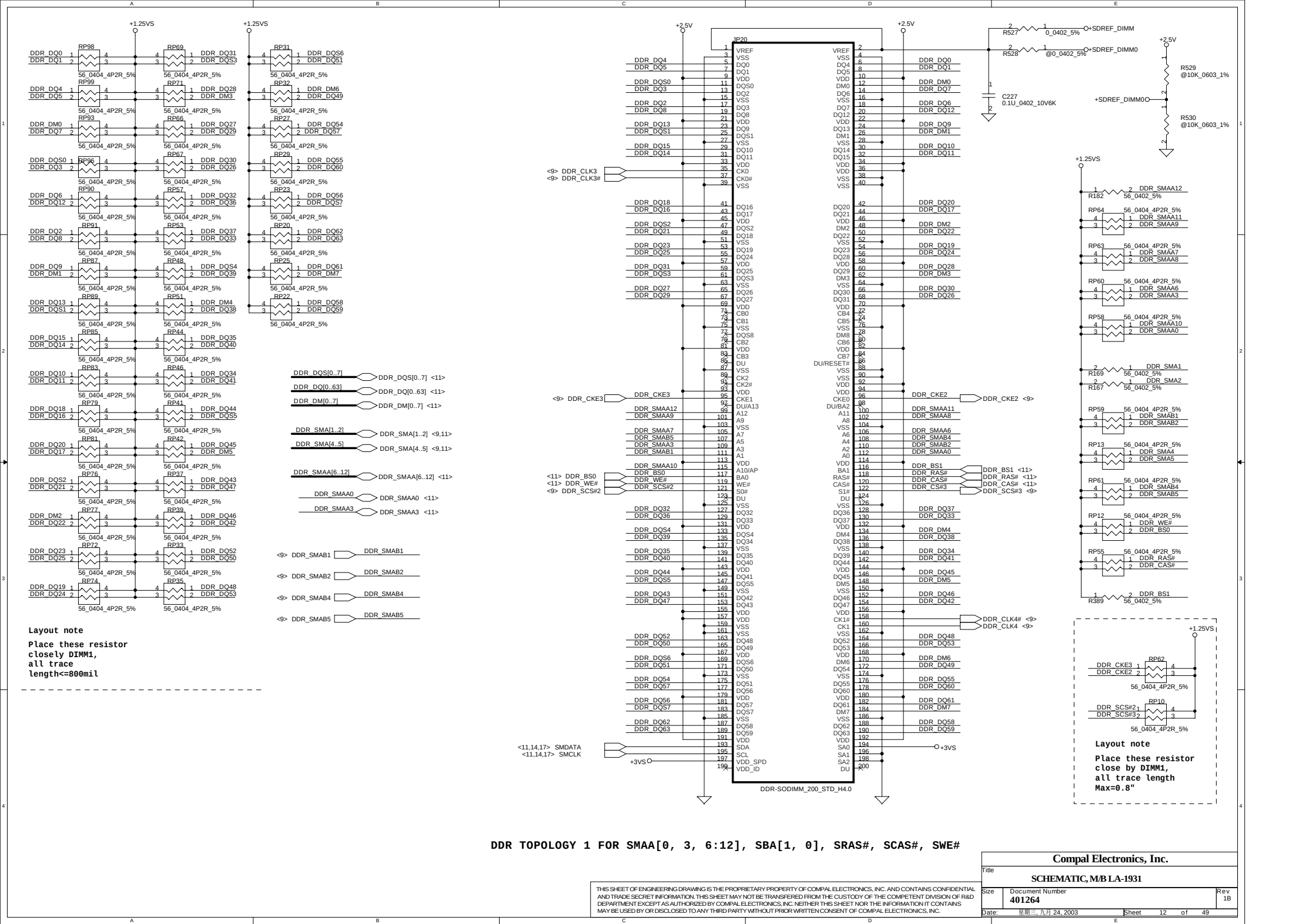
I2C BUS PULL UP



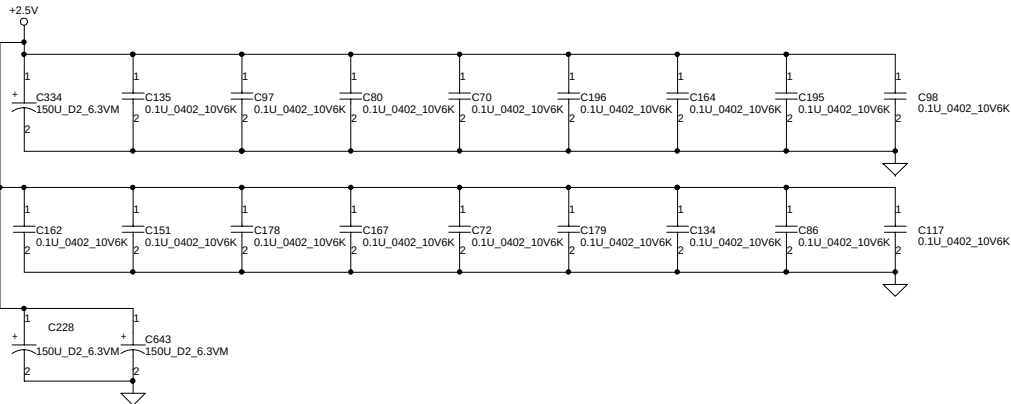
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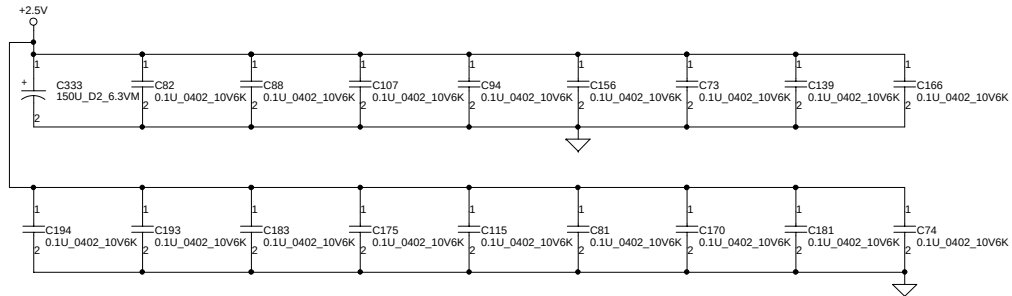




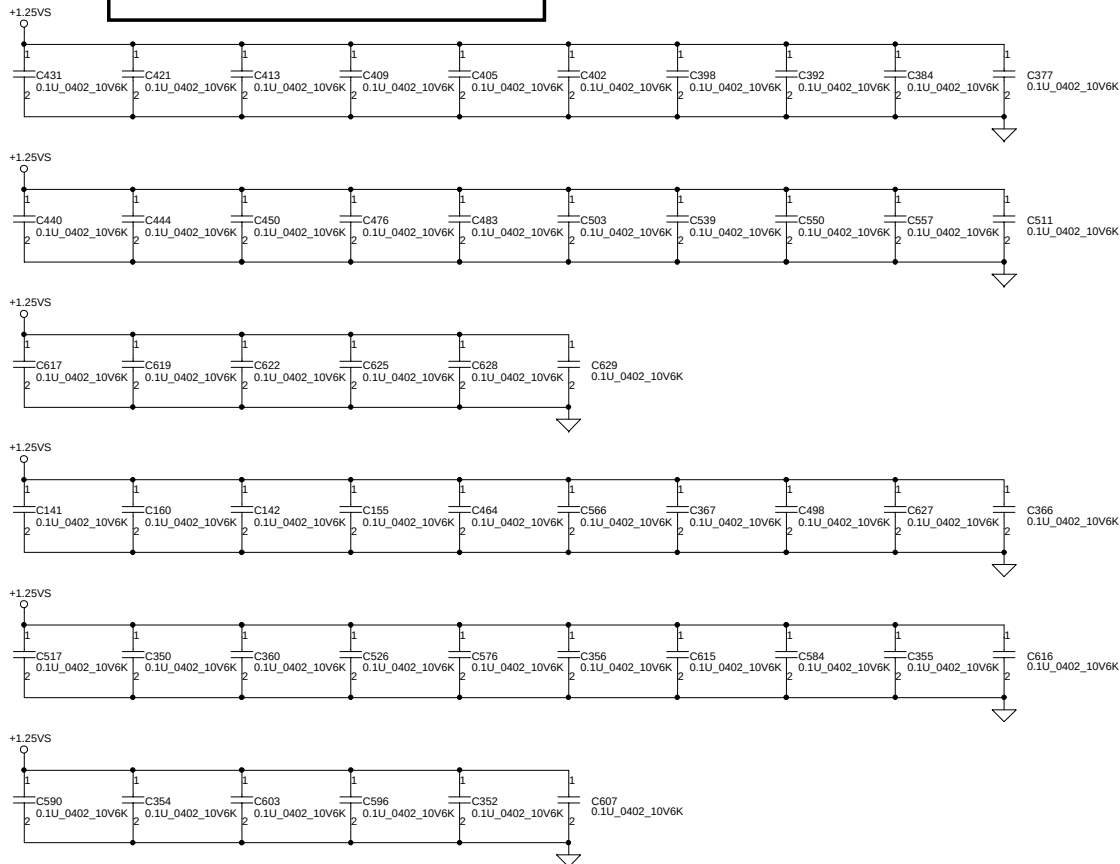
Layout note :
Distribute as close as possible
to DDR-SODIMM0.



Layout note :
Distribute as close as possible
to DDR-SODIMM1.



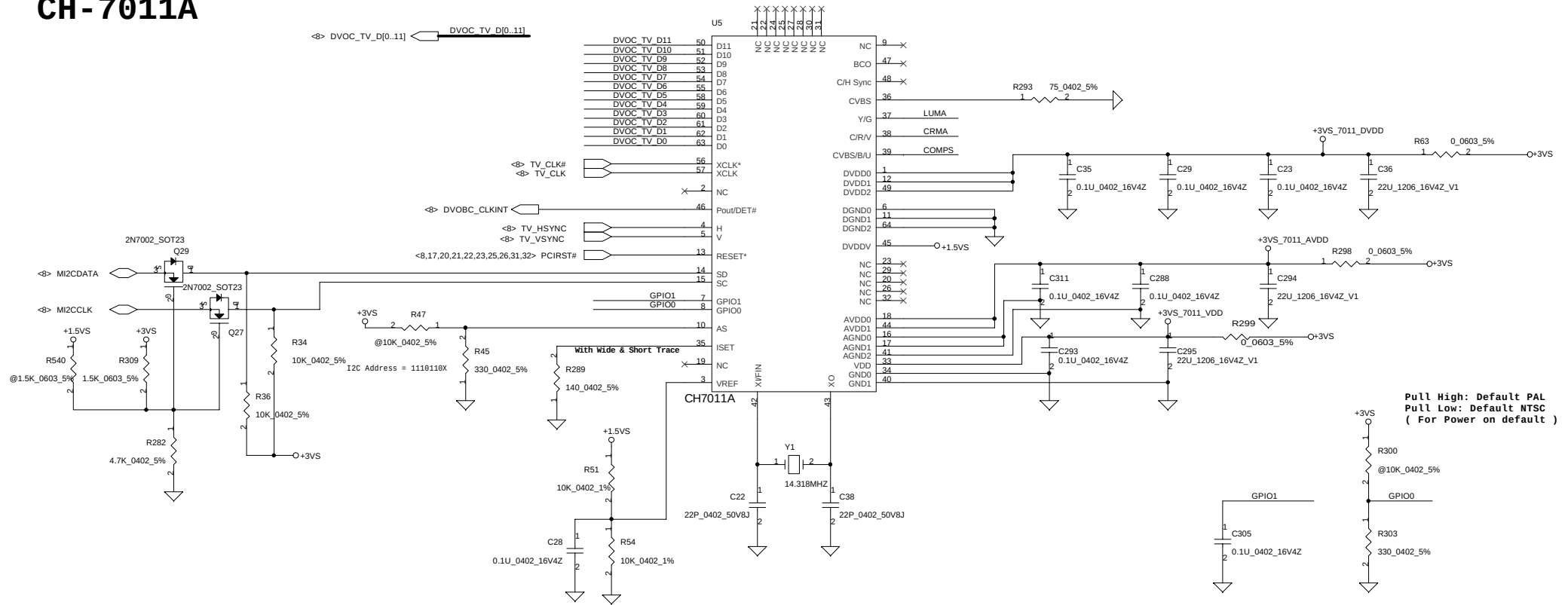
Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25VS



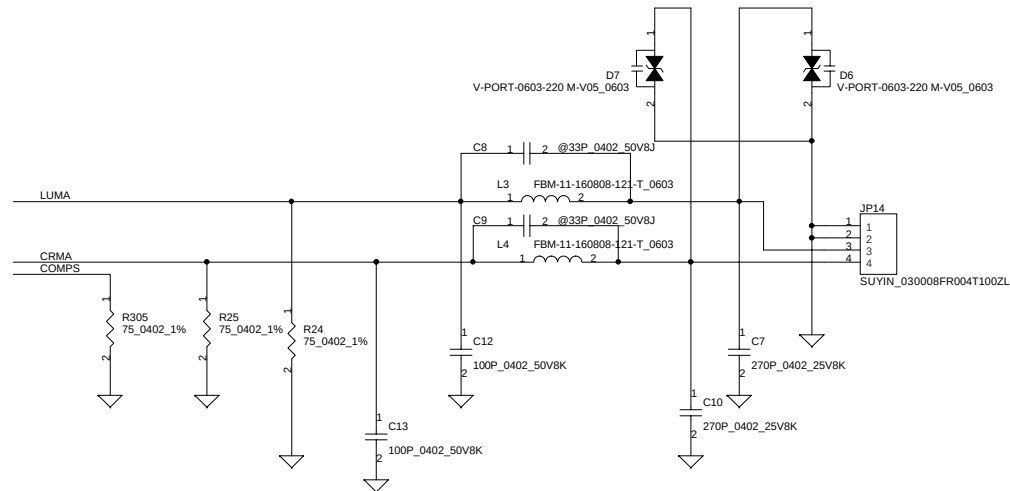
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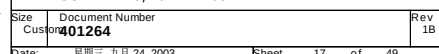


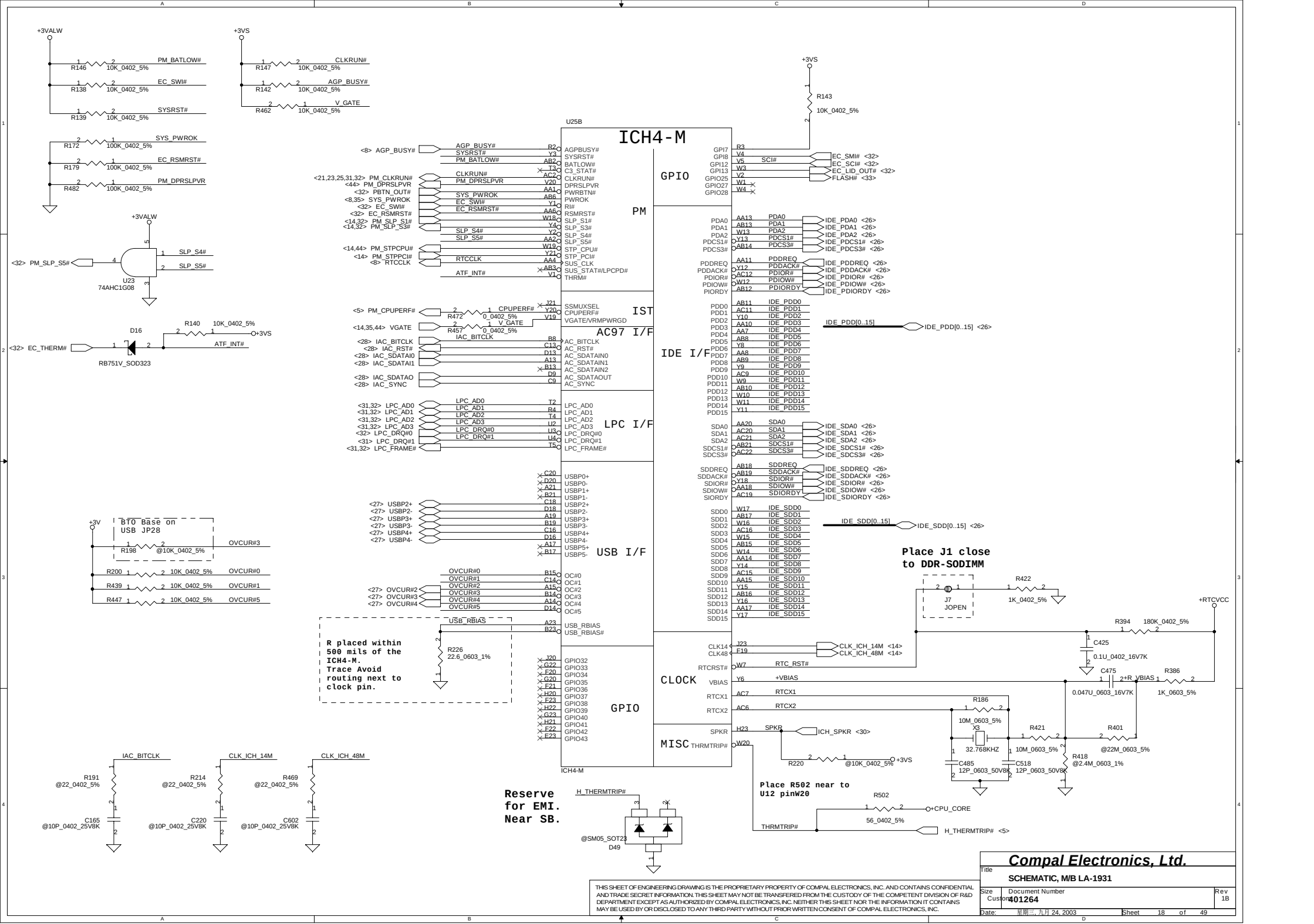
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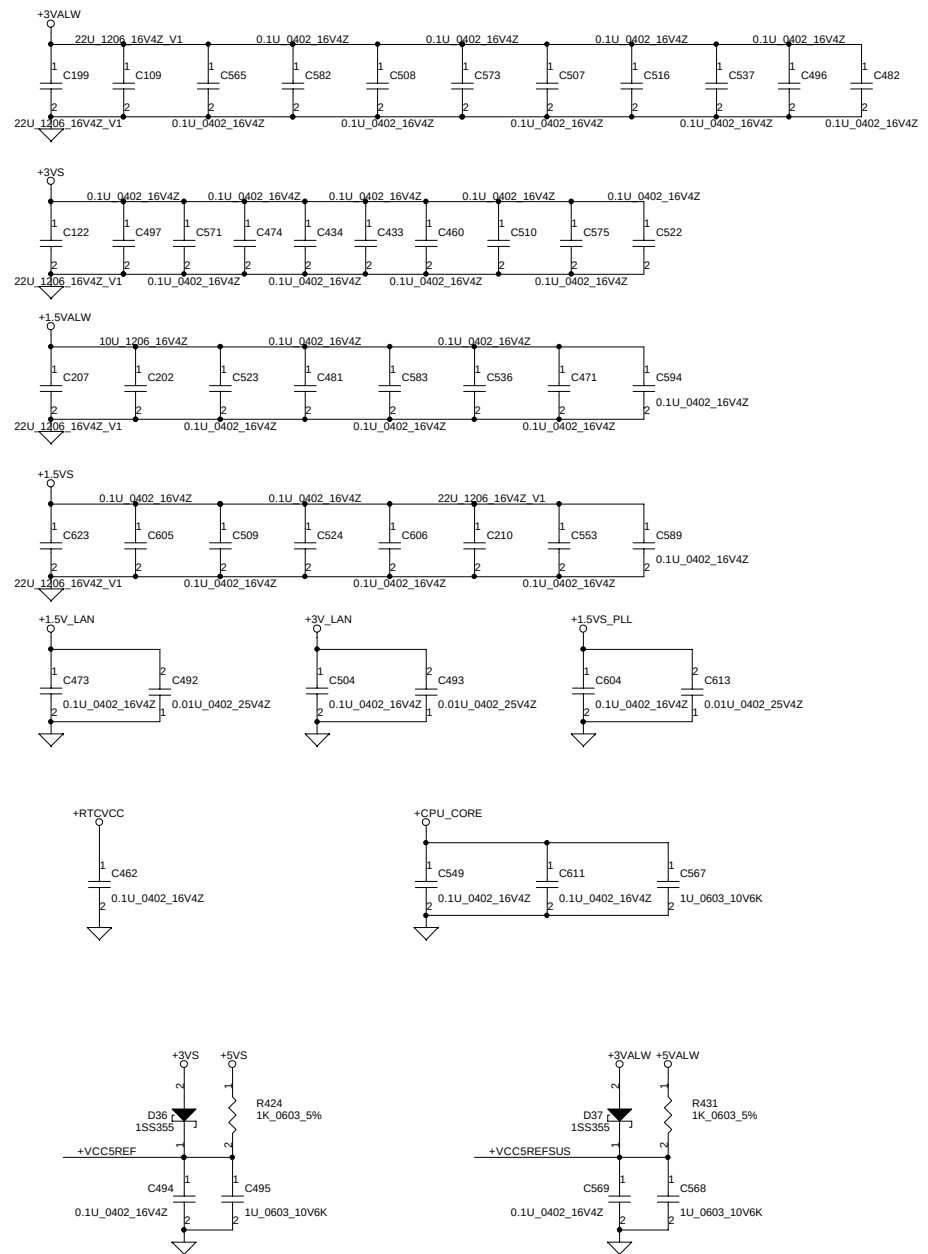
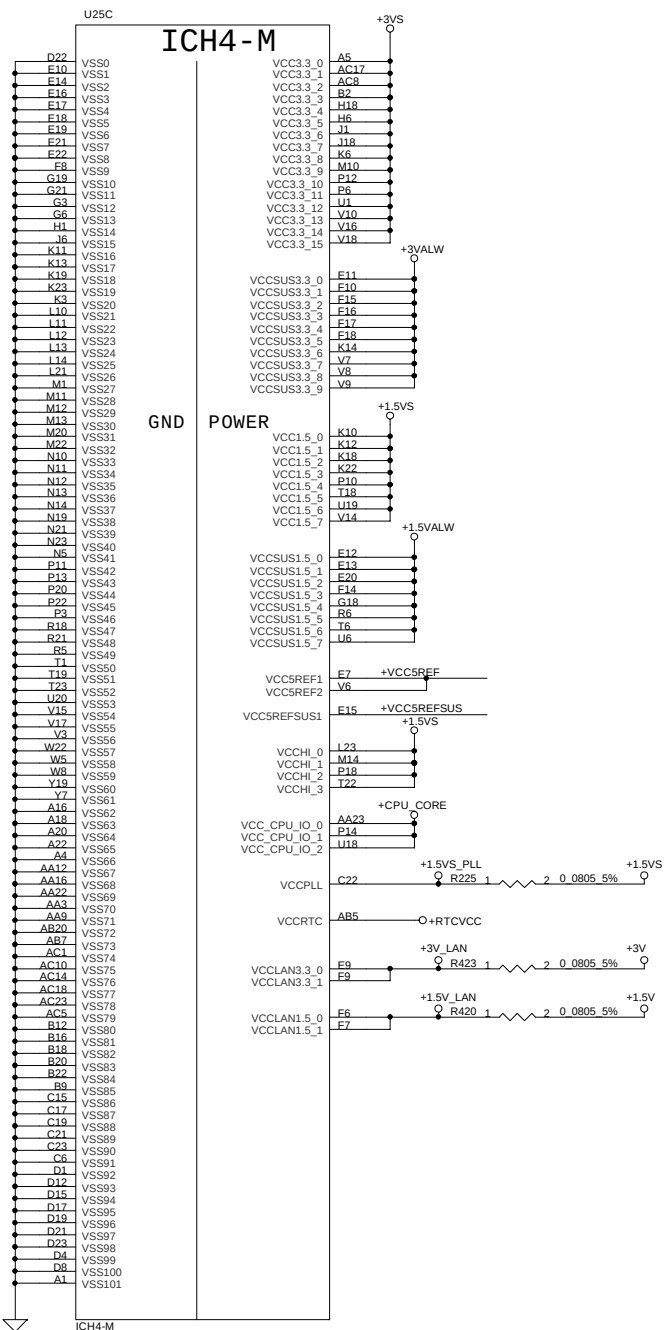


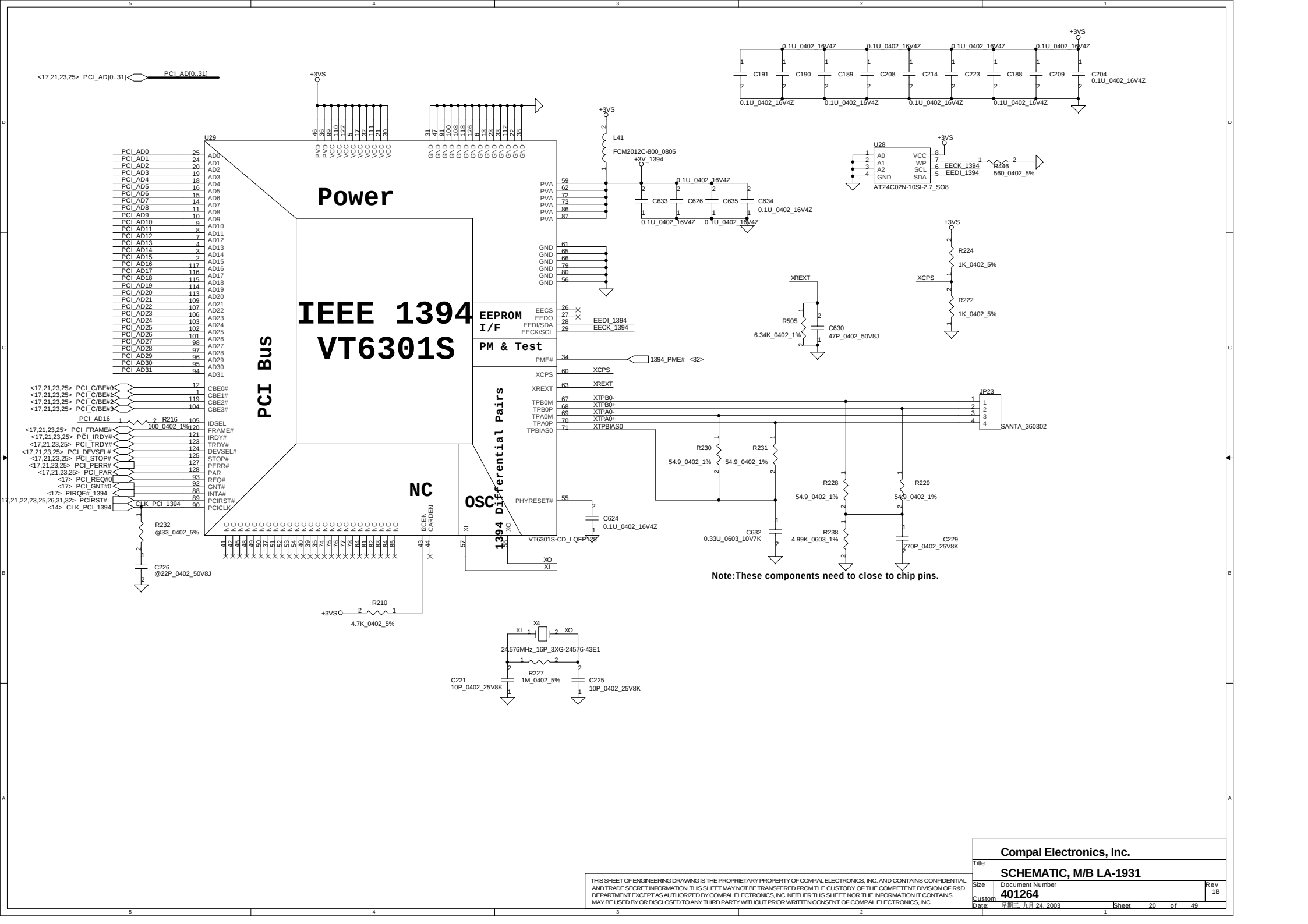
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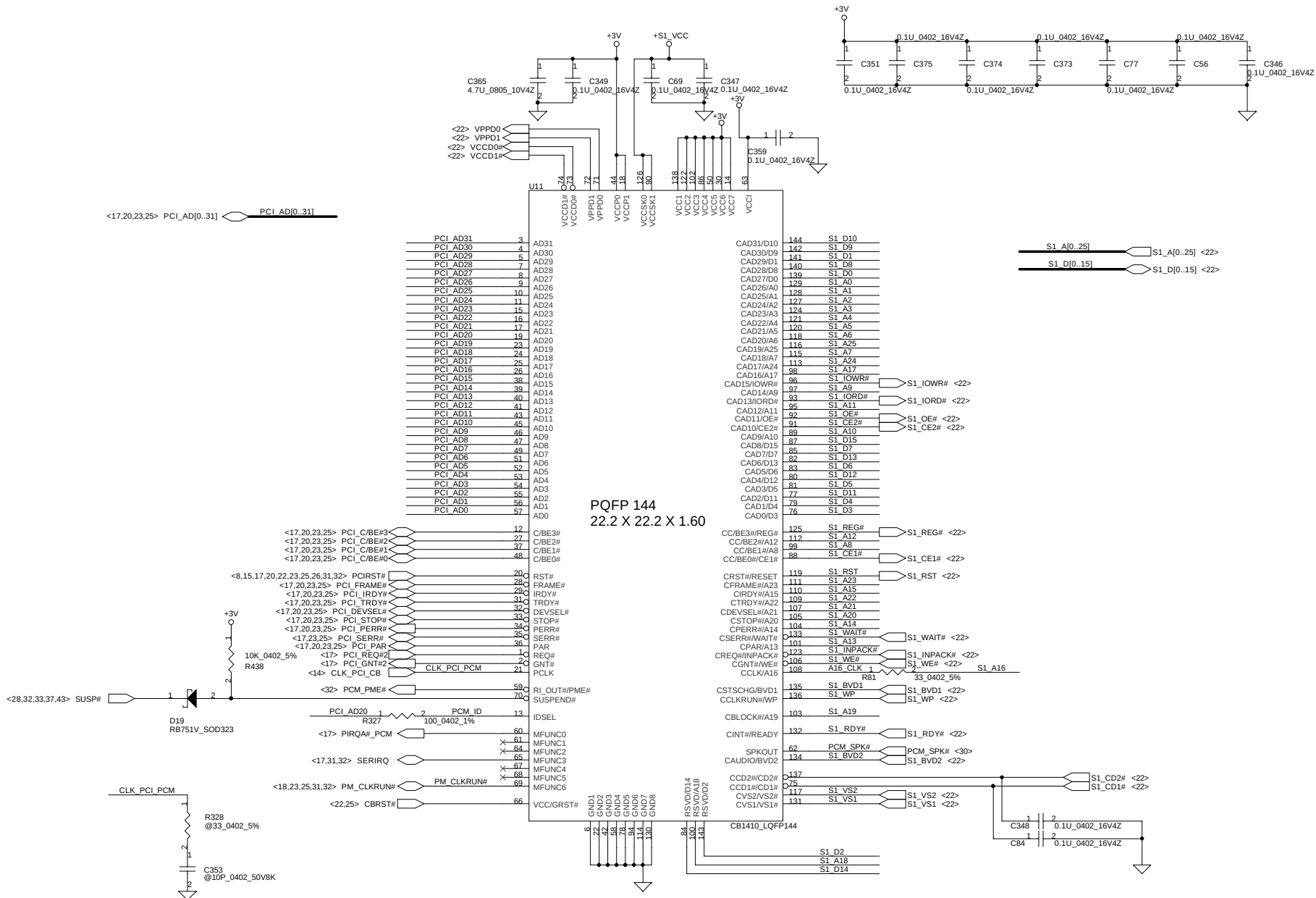






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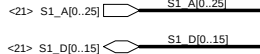
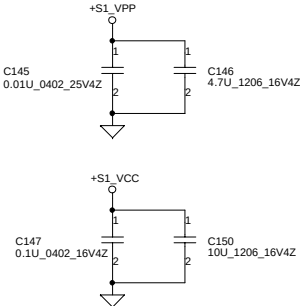
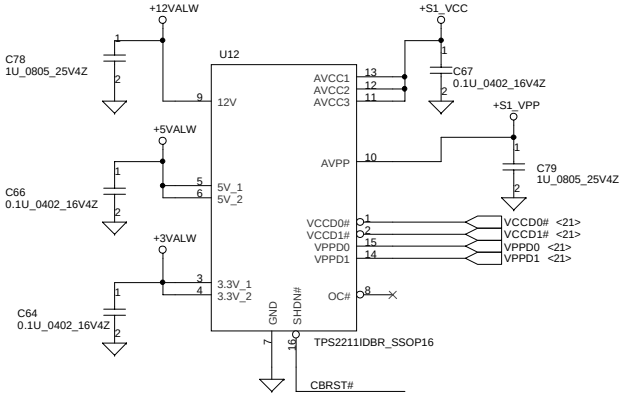
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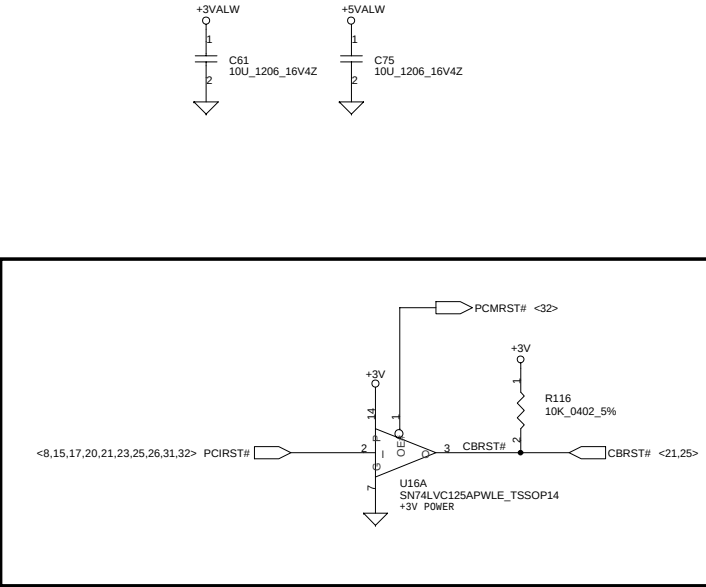
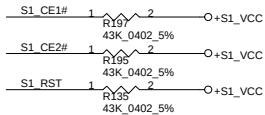
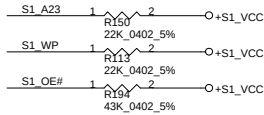
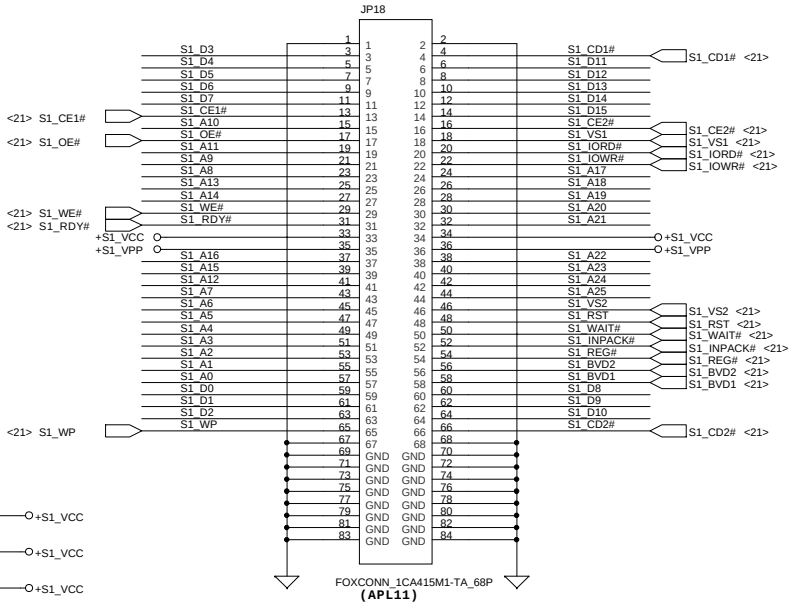
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PCMCIA Power Controller

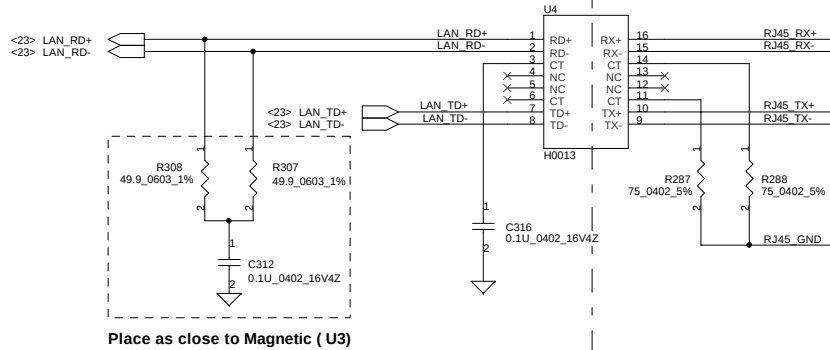


CardBus Socket

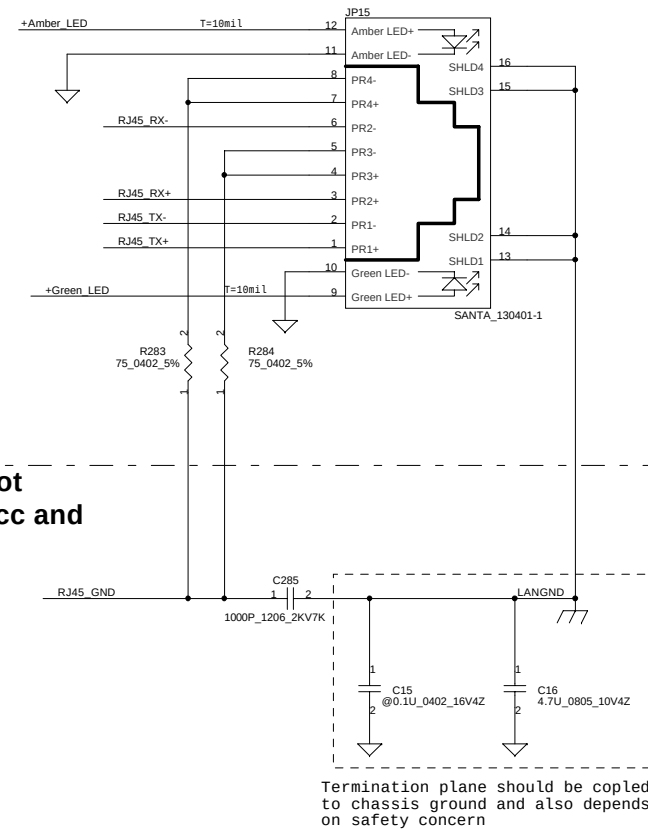
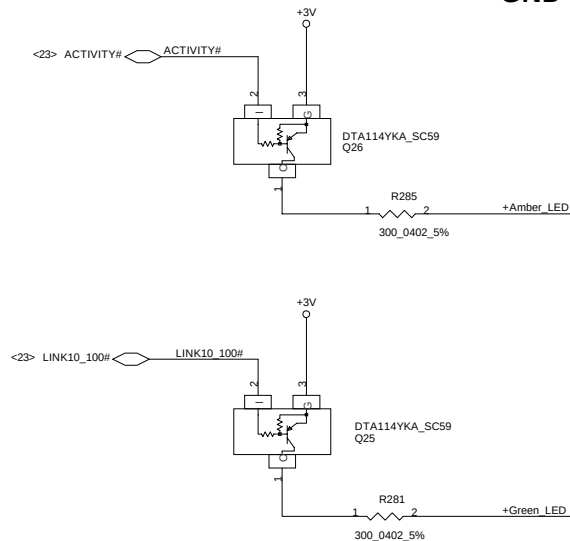


Keep Out 40mil

Layout Note
H0013 pls close to
conn.



LAYOUT NOTICE: This area do not
connect to power plan include Vcc and
GND in any layer



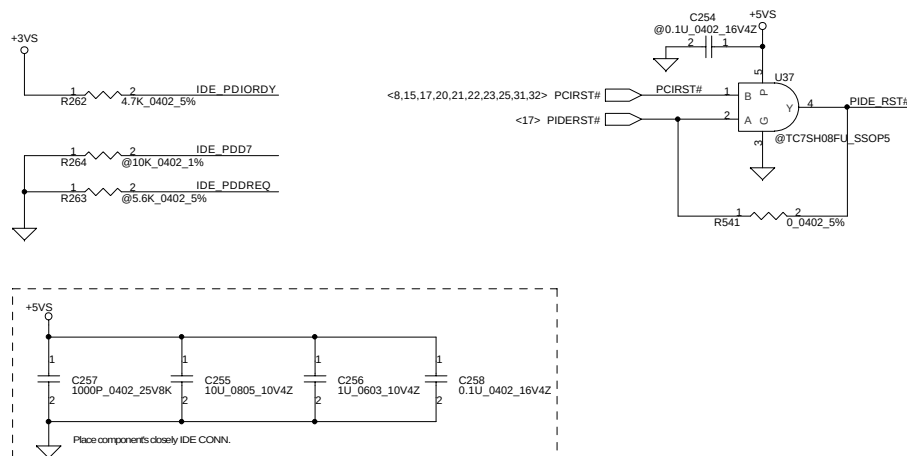
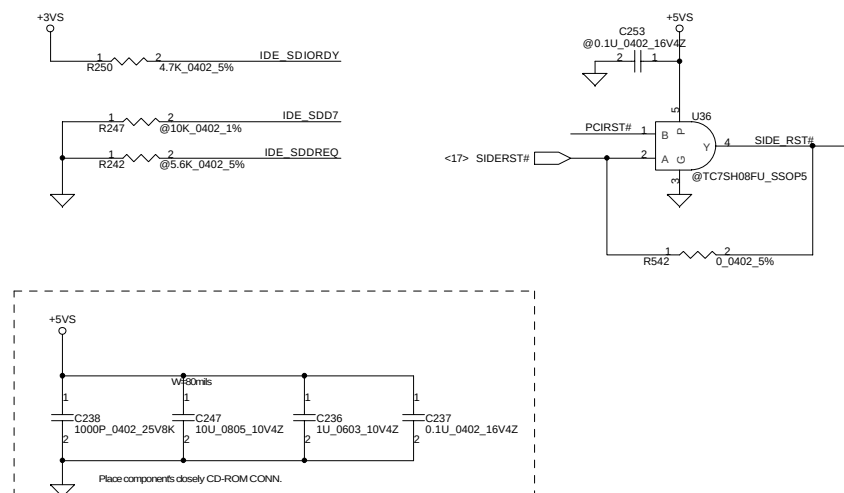
Compal Electronics, Ltd.

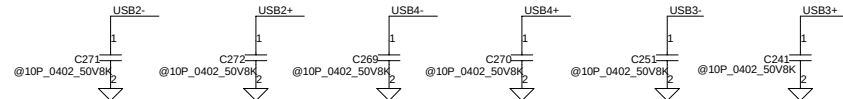
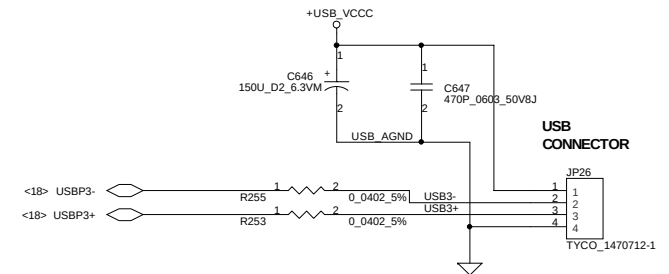
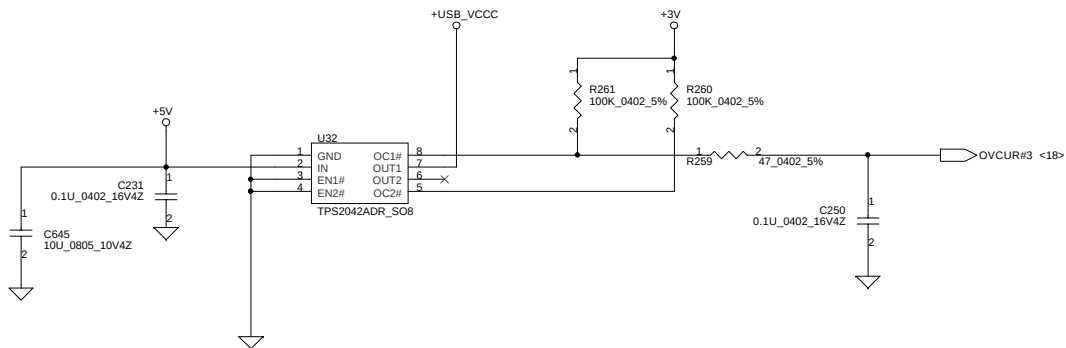
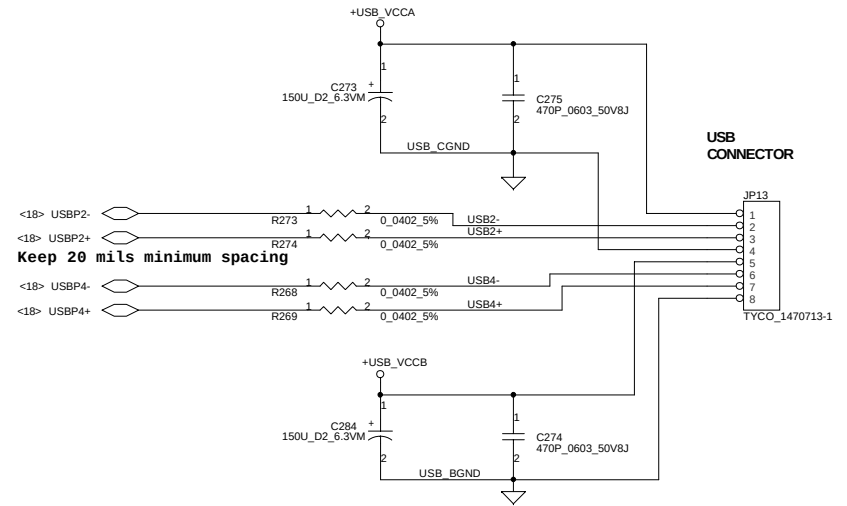
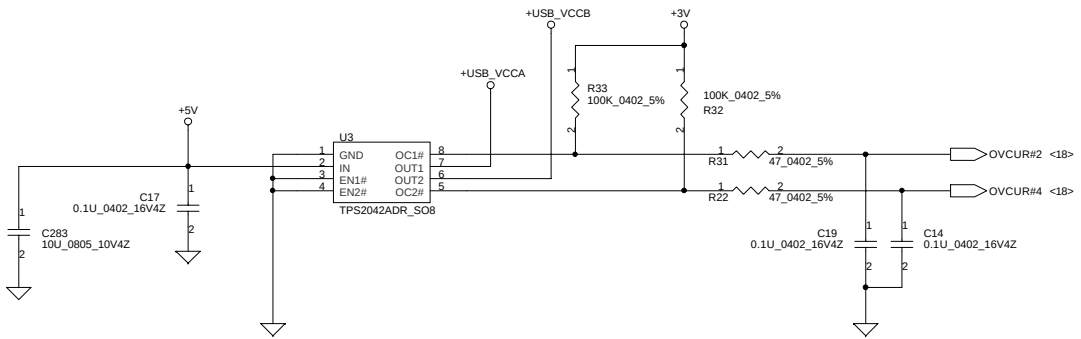
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IDE Module CONN.

**CD-ROM Module CONN.**



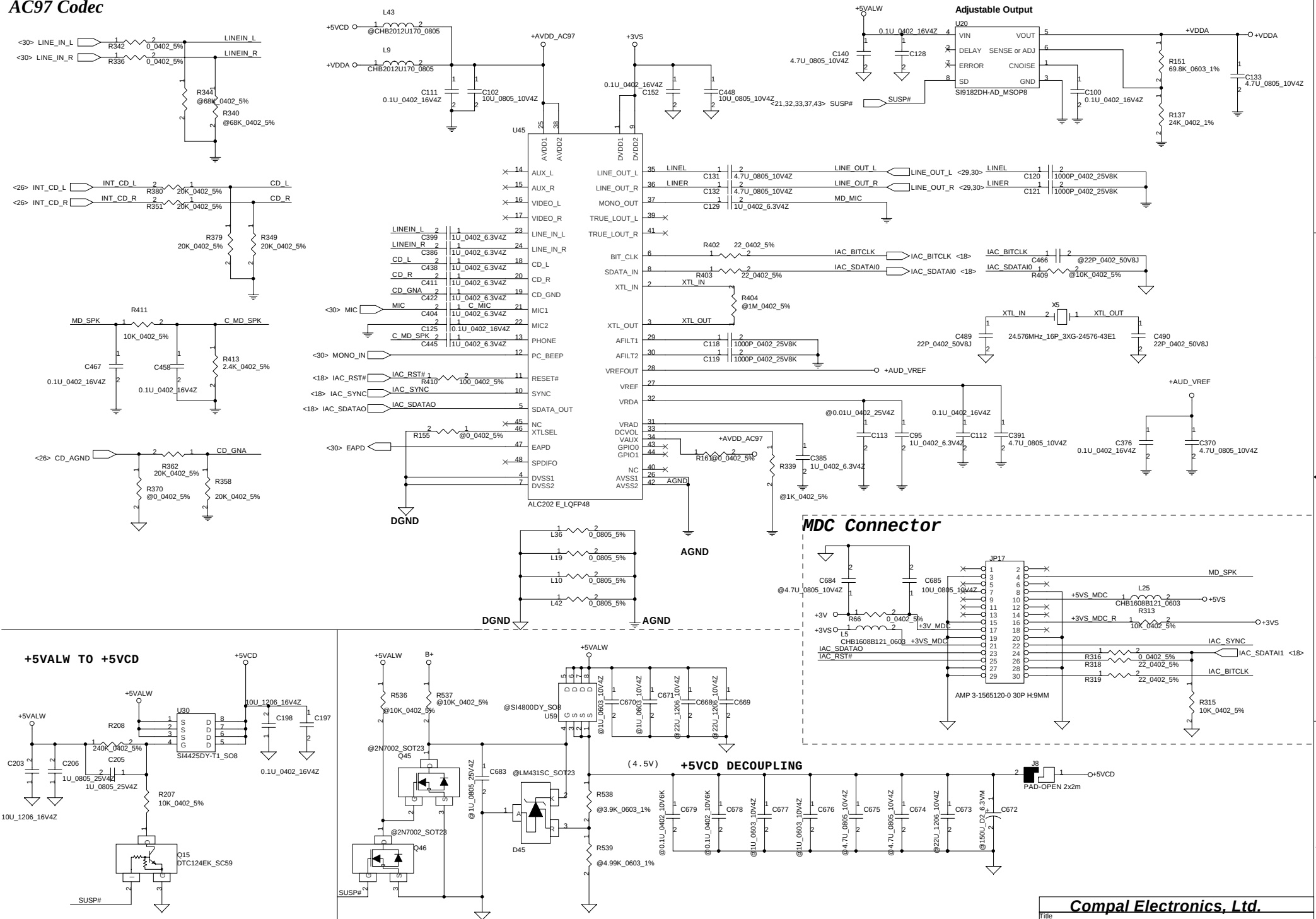
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AC97 Codec

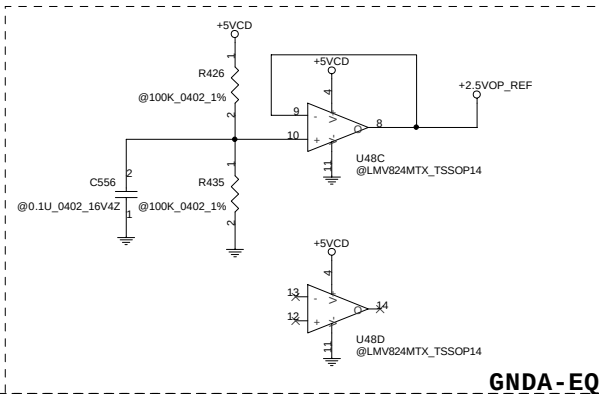


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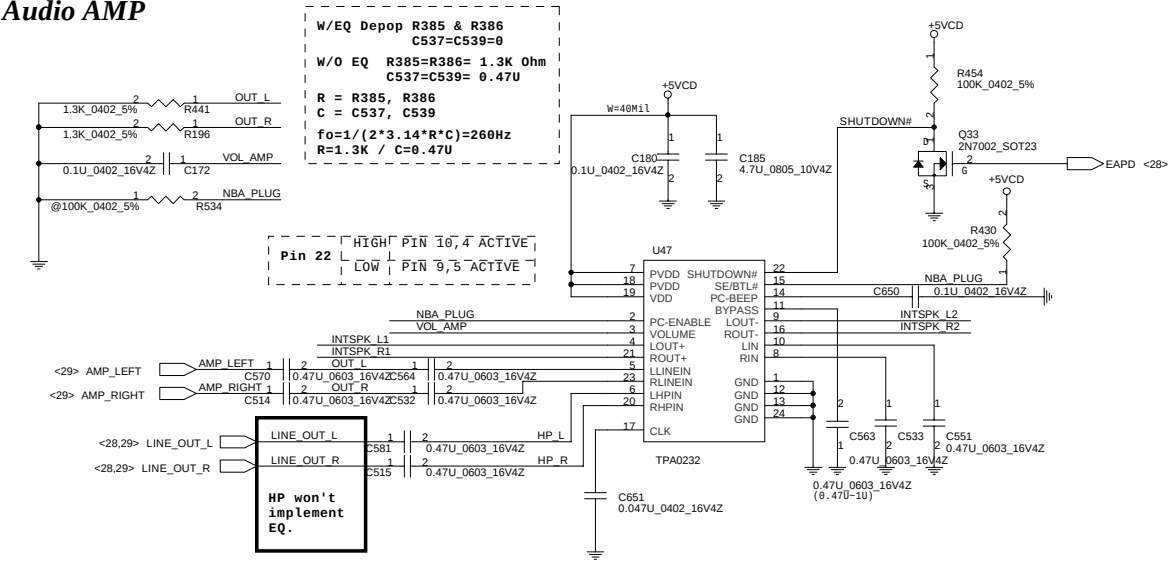
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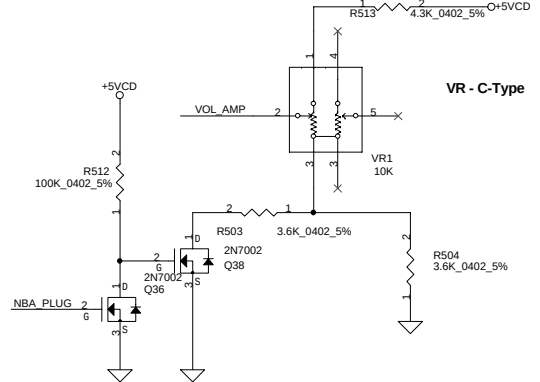
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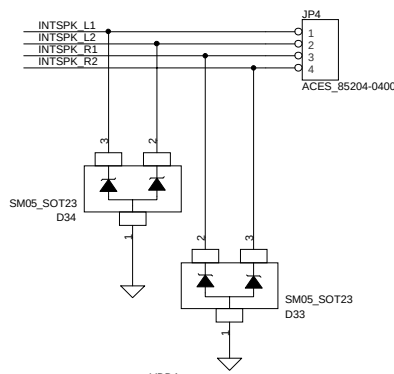
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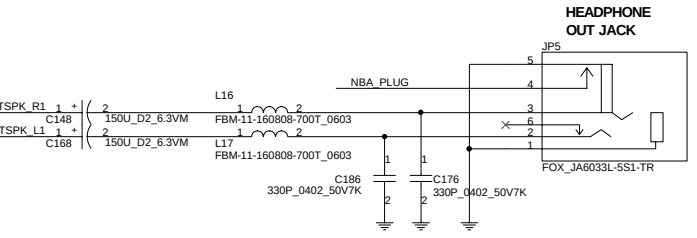
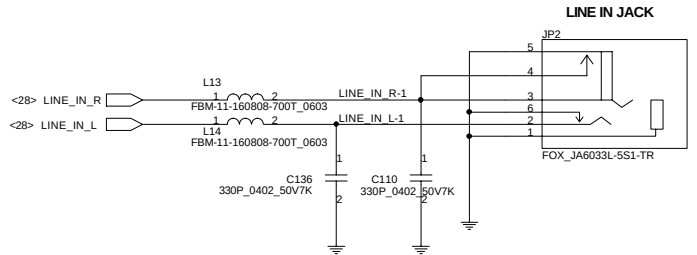
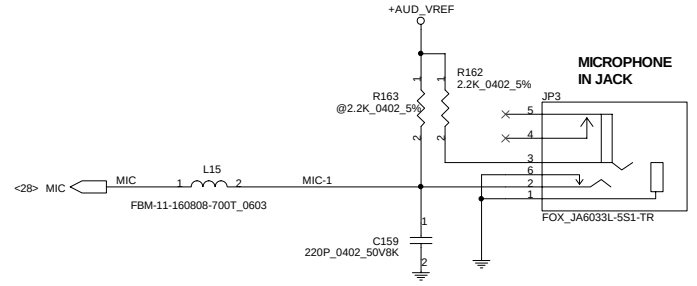
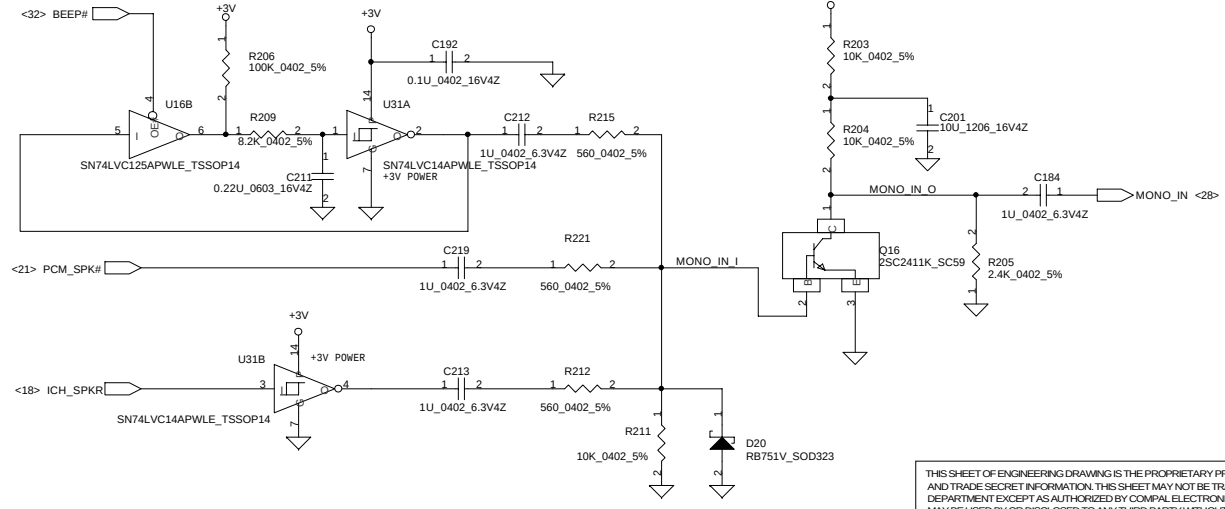
	W/ EQ	W/O EQ
R513	4.3K	4.3K
R504	3.6K	3.6K
R503	6.2K	3.6K
Bias (Gain)	SPK 0.687 V 10 dB HP 1.006 V -2 dB	SPK 0.560 V 12 dB HP 1.006 V -2 dB



Speaker Connector



System Sound



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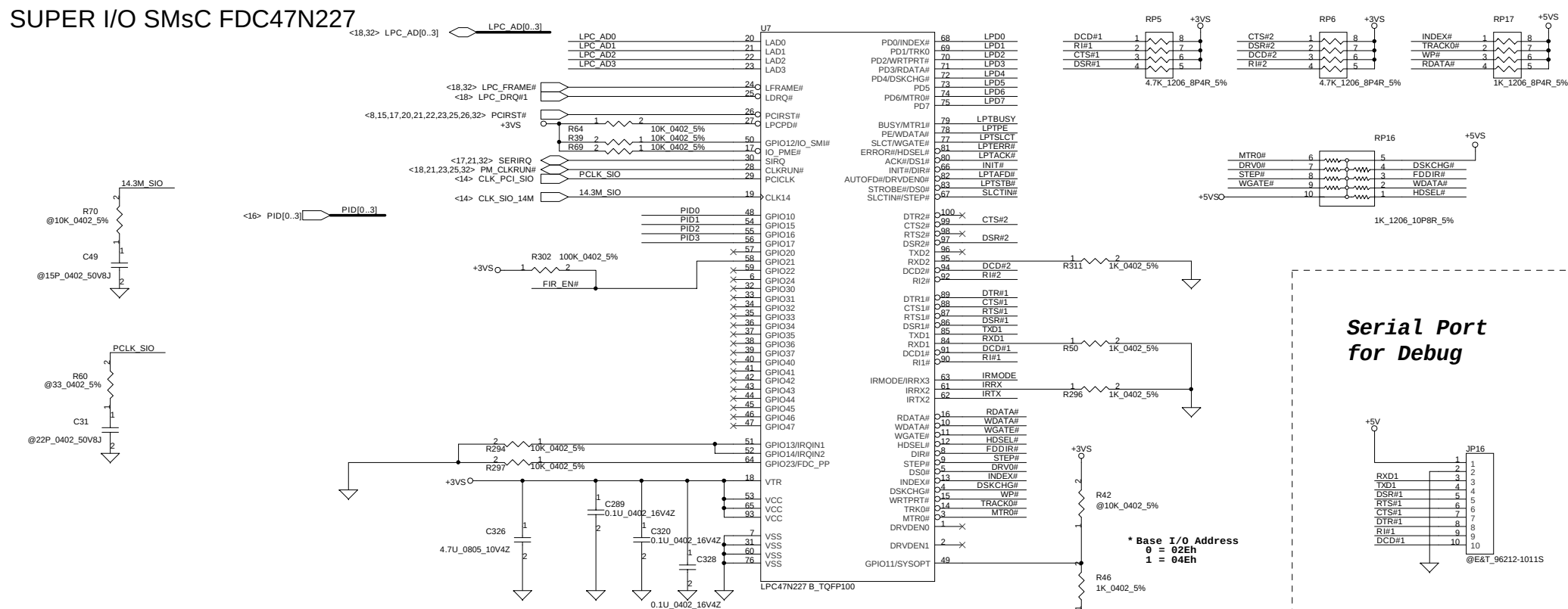
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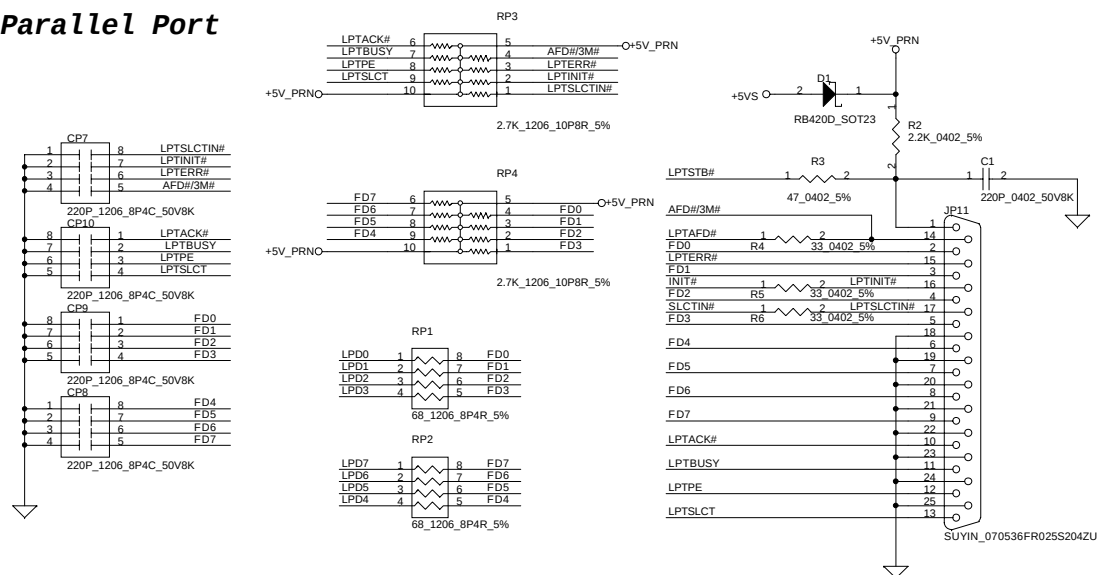
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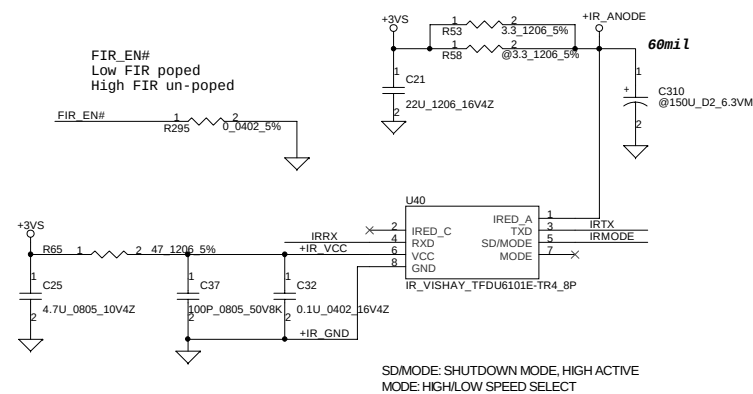
SUPER I/O SMsC FDC47N227



Parallel Port



FIR Module



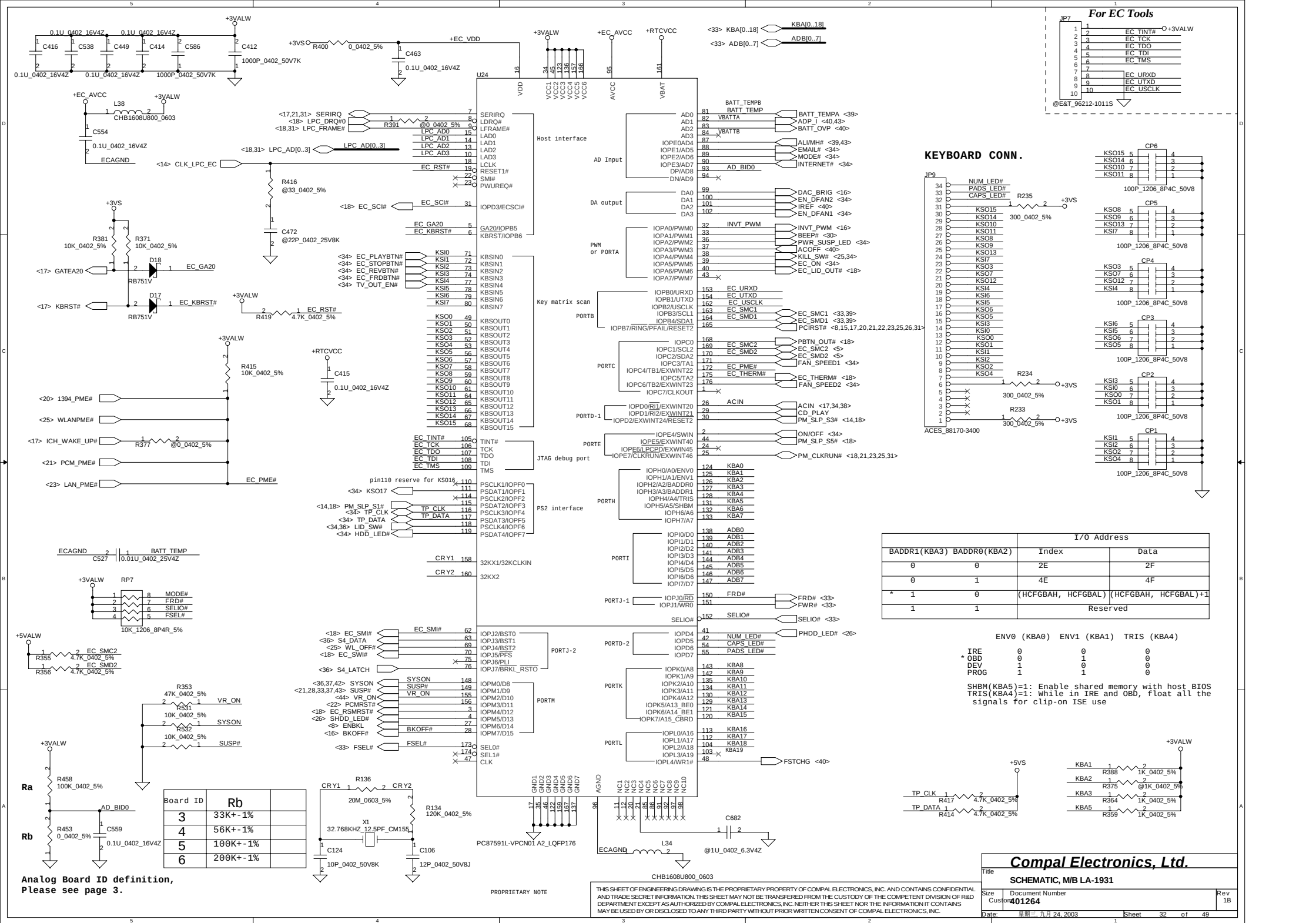
SD/MODE: SHUTDOWN MODE, HIGH ACTIVE
MODE: HIGH/LOW SPEED SELECT

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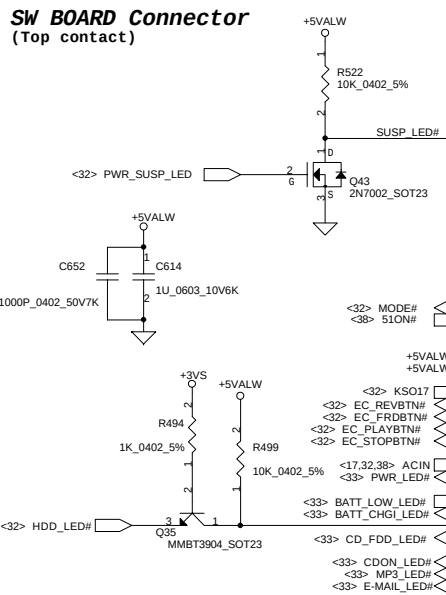
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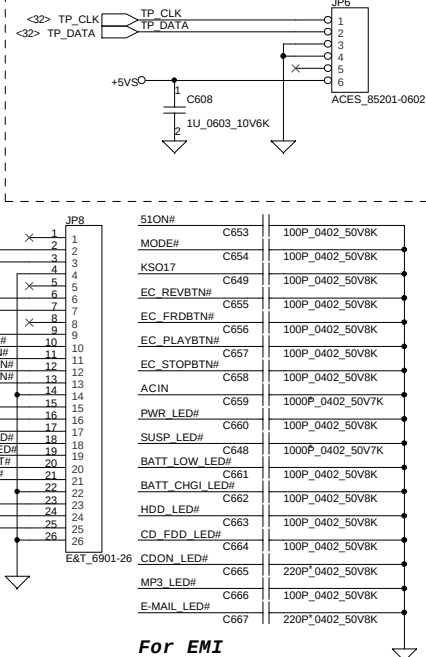
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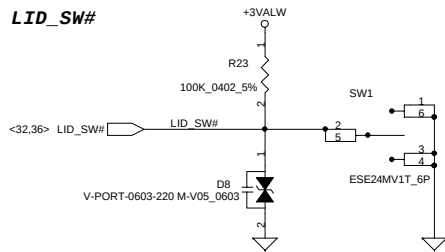
SW BOARD Connector (Top contact)



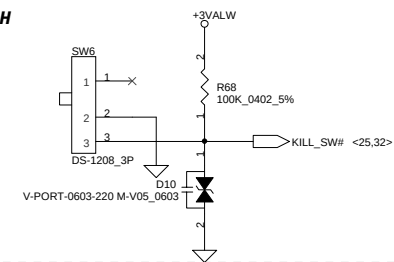
Touch Pad Connector



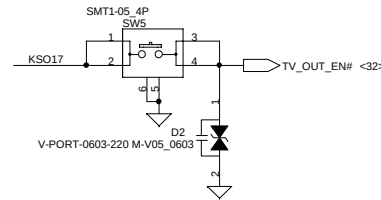
LID_SW#



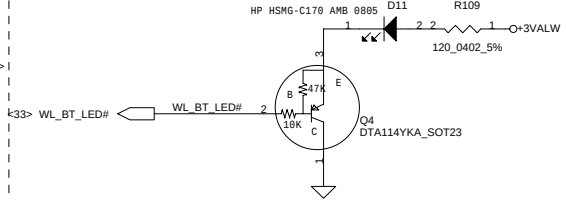
Kill SWITCH



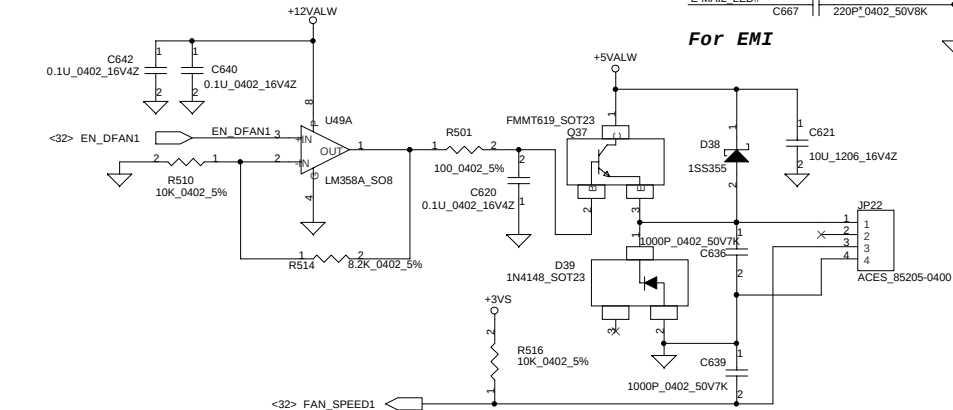
TV-OUT BUTTON



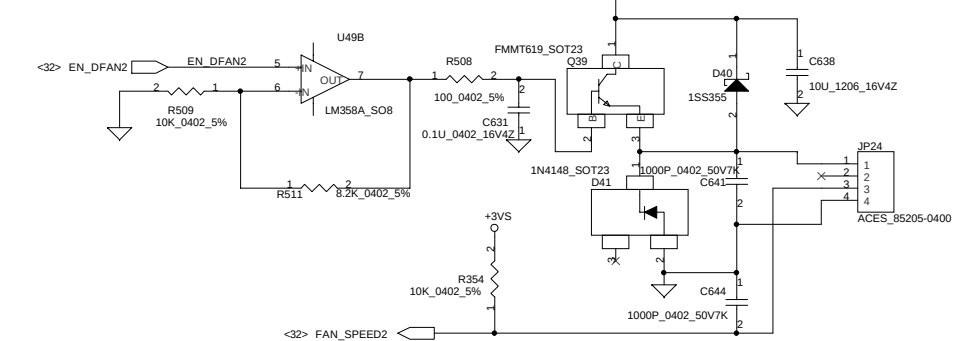
WIRELESS ACTIVE AMB LED



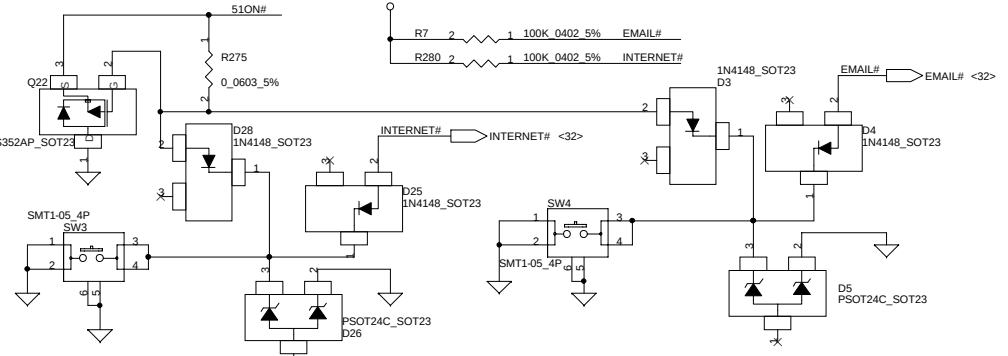
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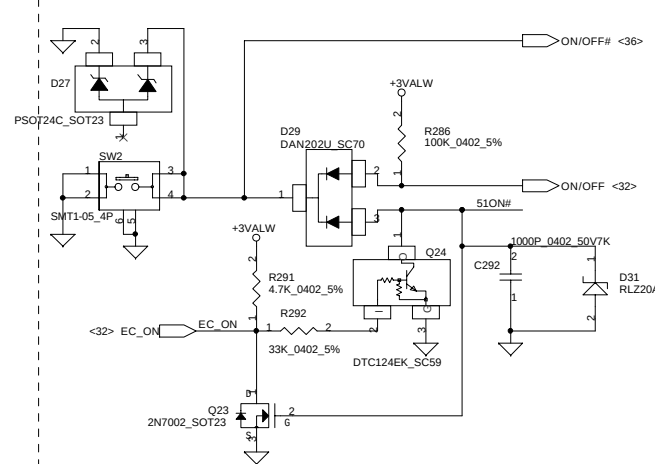
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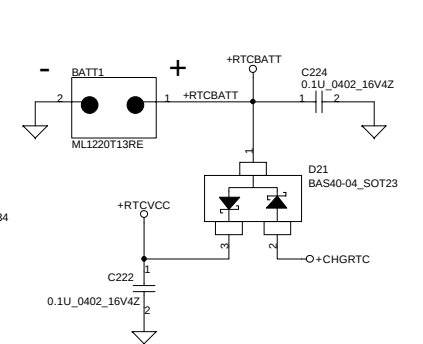
Internet Button



Power Button



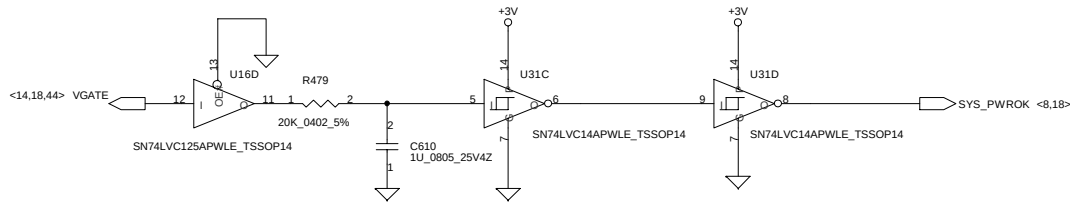
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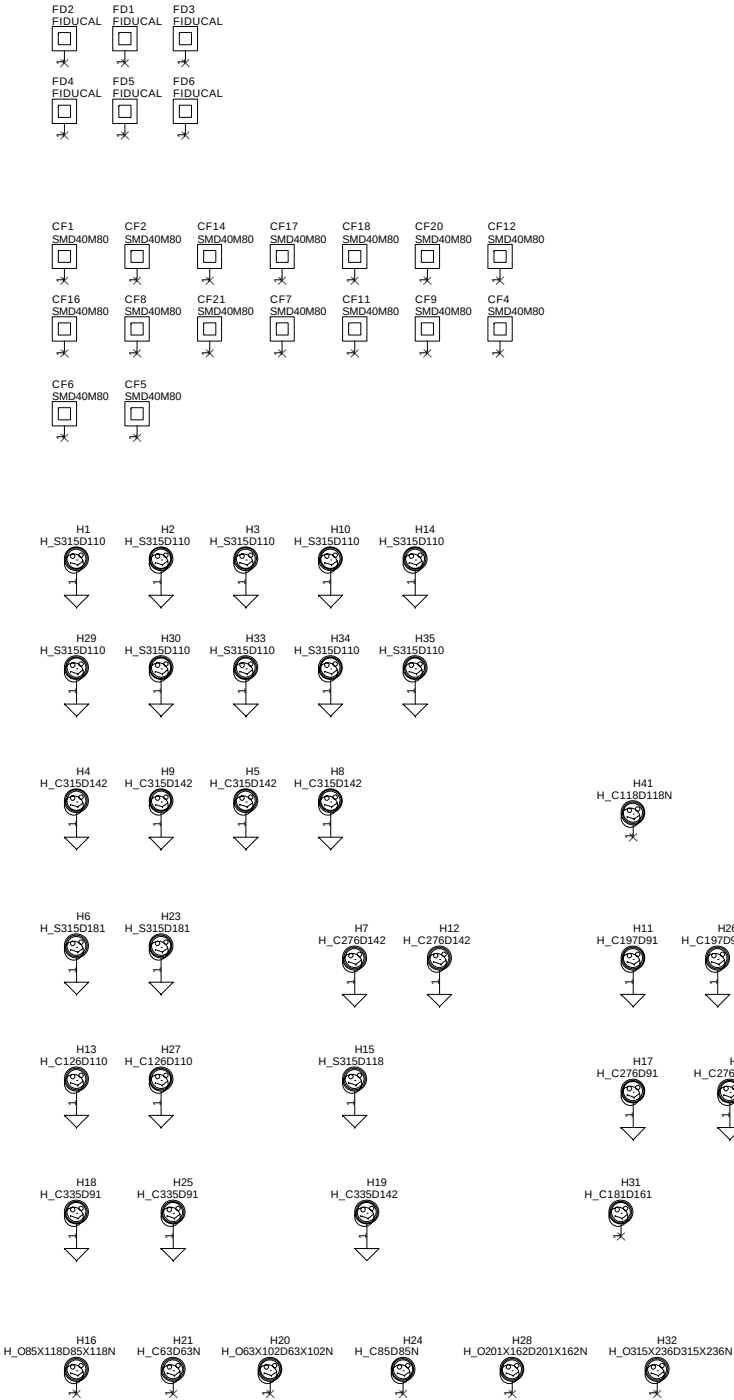
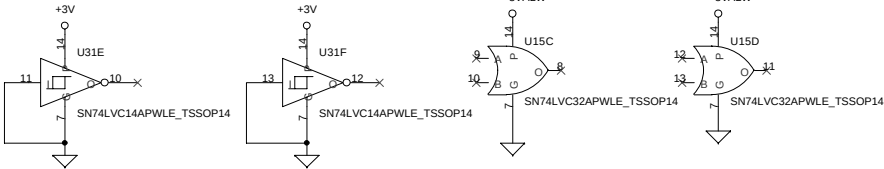
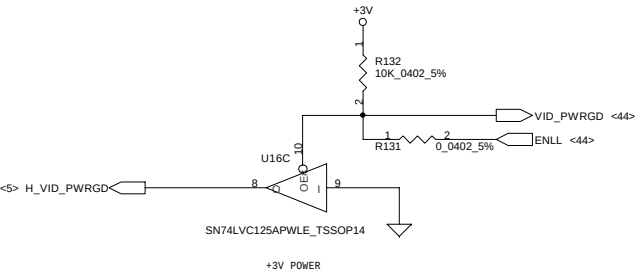
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Power Good Circuit

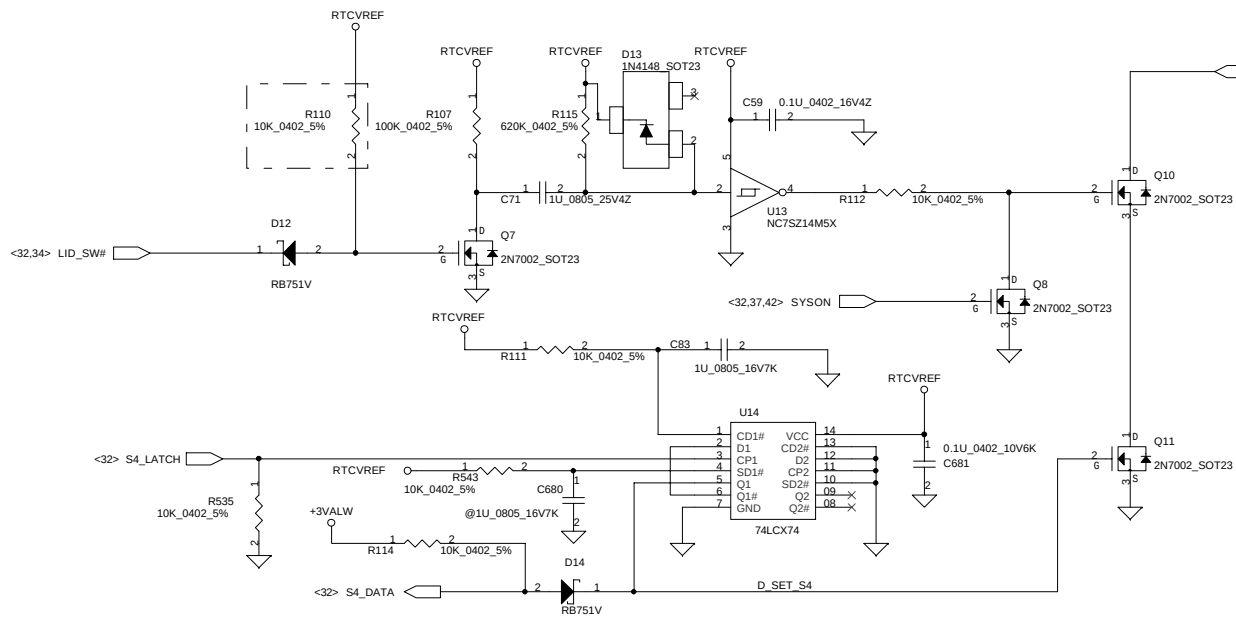


VID_PWRGD



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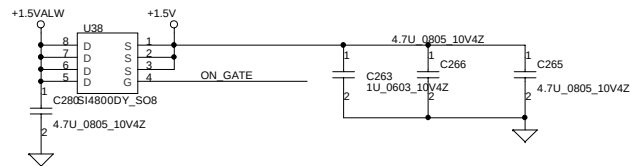
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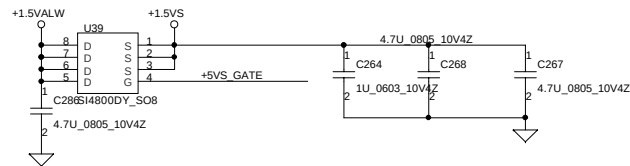
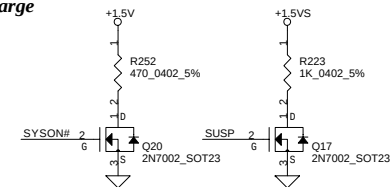
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[illegible]

+1.5VALW To +1.5V Transfer

+1.5VALW To +1.5VS Transfer

+1.5V & +1.5VS Discharge

+3VALW To +3V Transfer

+3VALW To +3VS Transfer

+3V & +3VS Discharge

+5VALW To +5V Transfer

+5VALW To +5VS Transfer

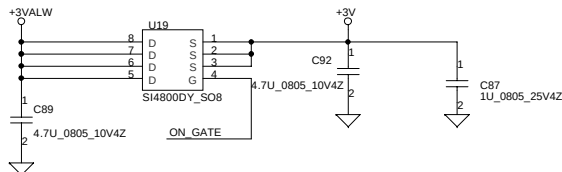
+5V & +5VS Discharge

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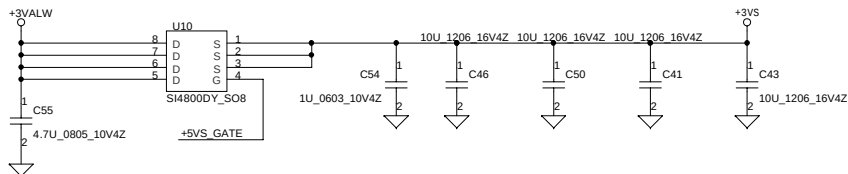
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+1.5VALW To +1.5V Transfer

+1.5VALW To +1.5VS Transfer

+1.5V & +1.5VS Discharge

+3VALW To +3V Transfer

+3VALW To +3VS Transfer

+3V & +3VS Discharge

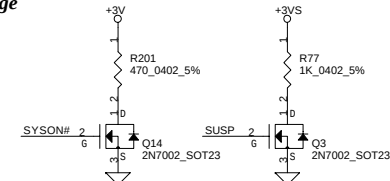
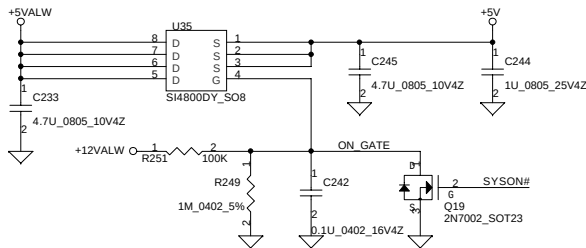
+5VALW To +5V Transfer

+5VALW To +5VS Transfer

+5V & +5VS Discharge

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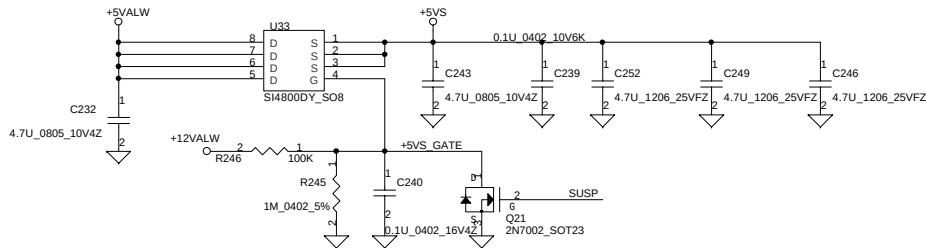
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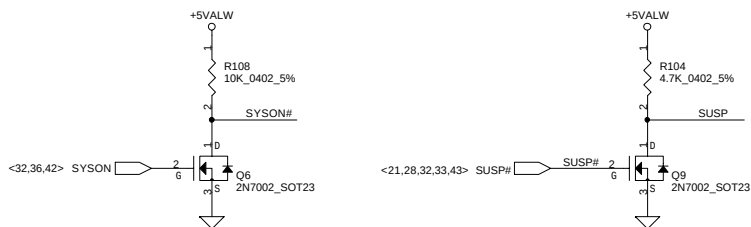
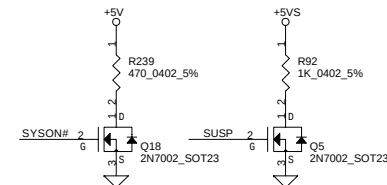
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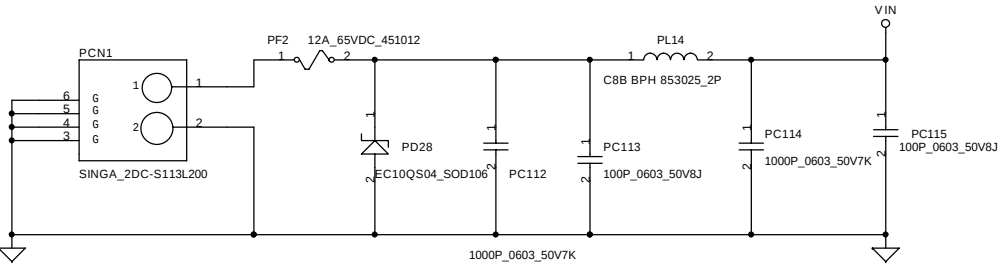
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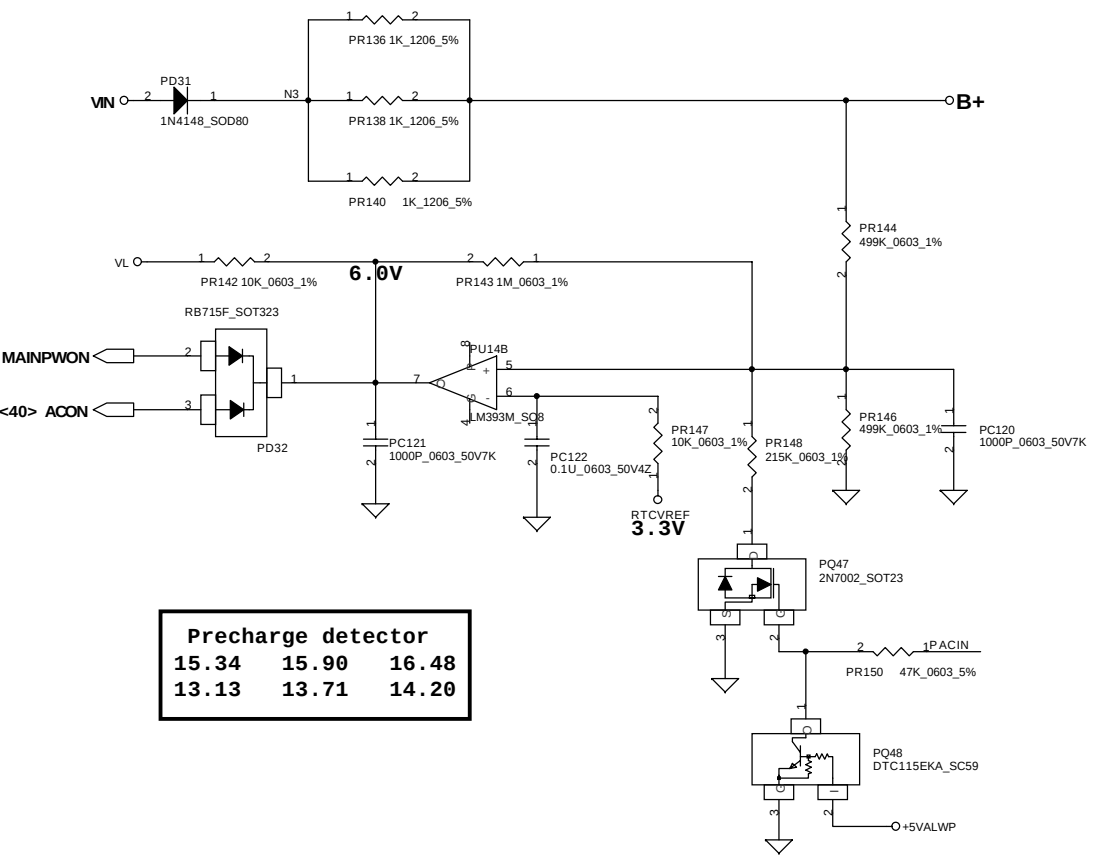
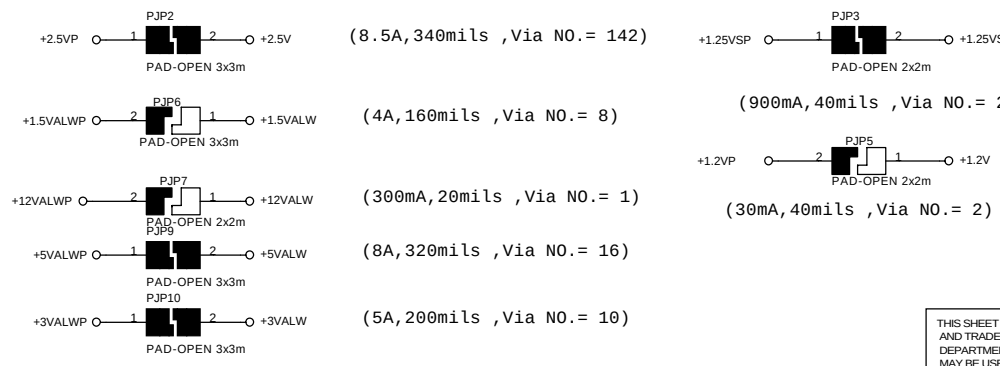
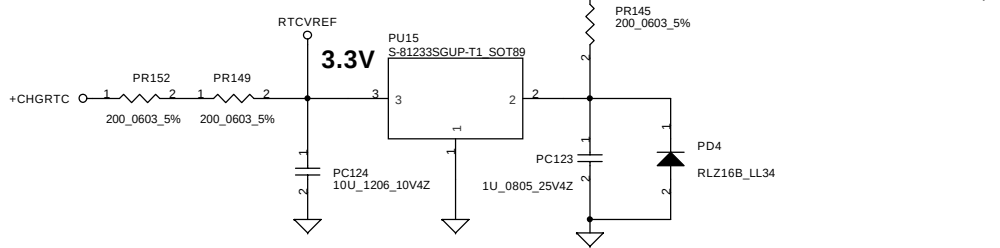
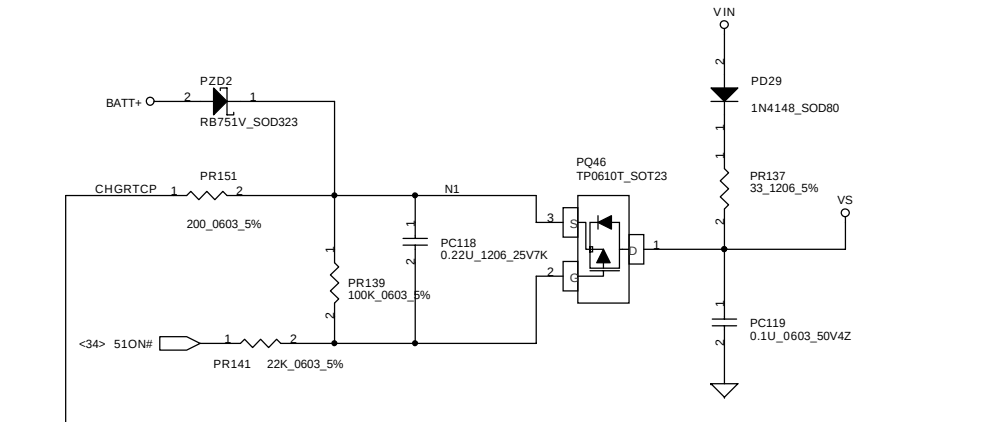
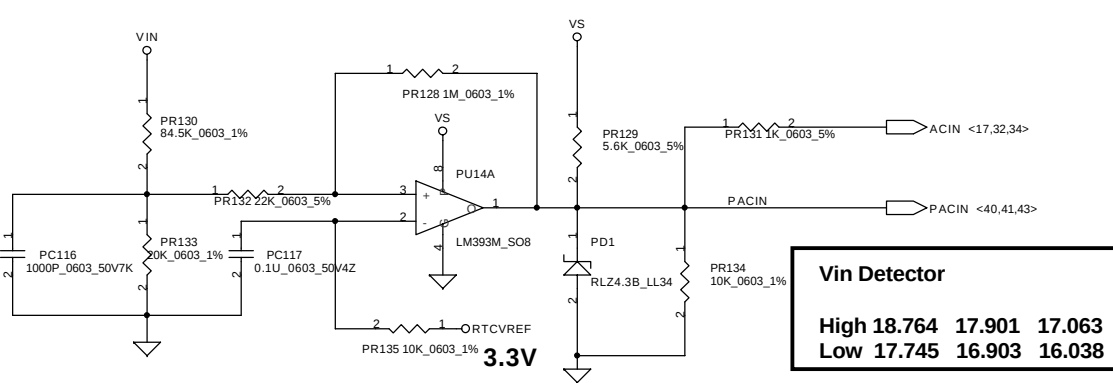
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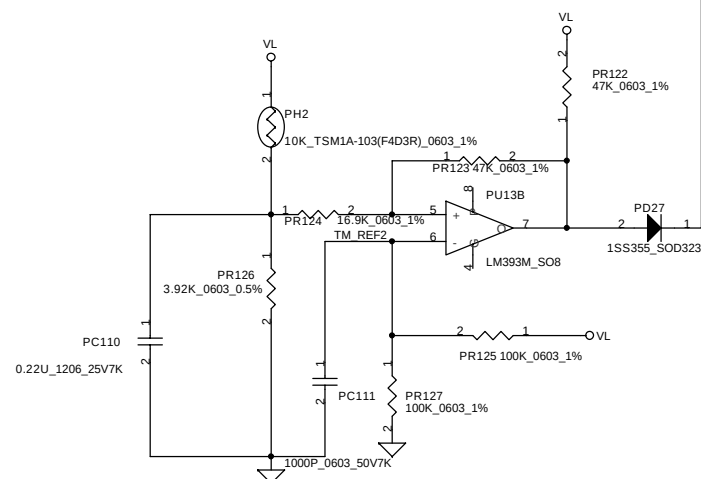
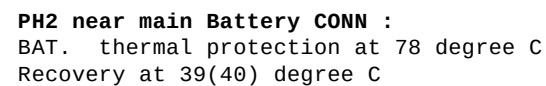
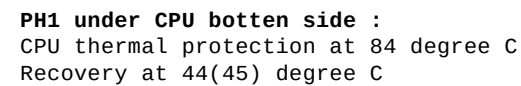


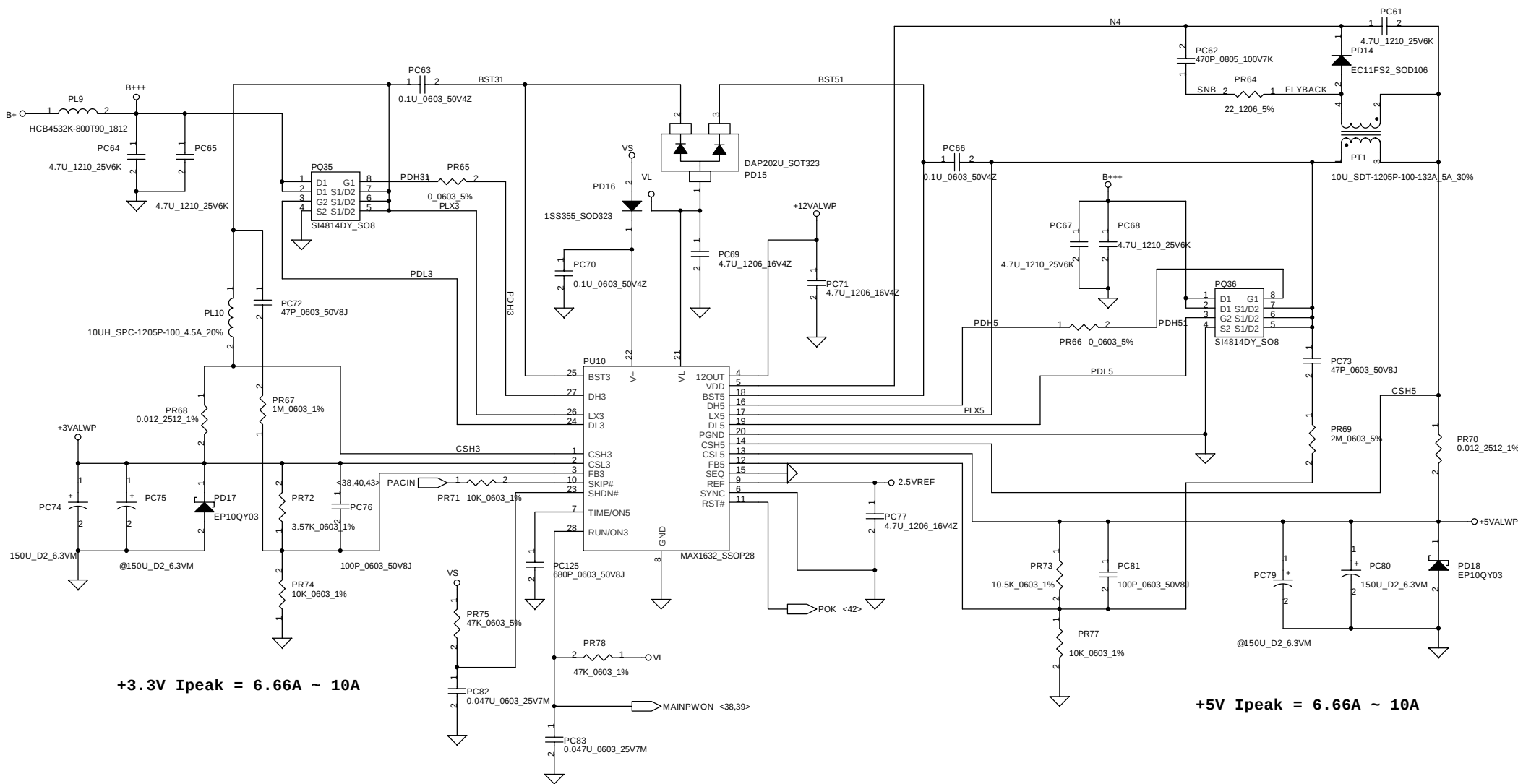
SINGA_2DC-S113L200	120W
SINGA_2DC-S726B201	90W



Precharge detector		
15.34	15.90	16.48
13.13	13.71	14.20

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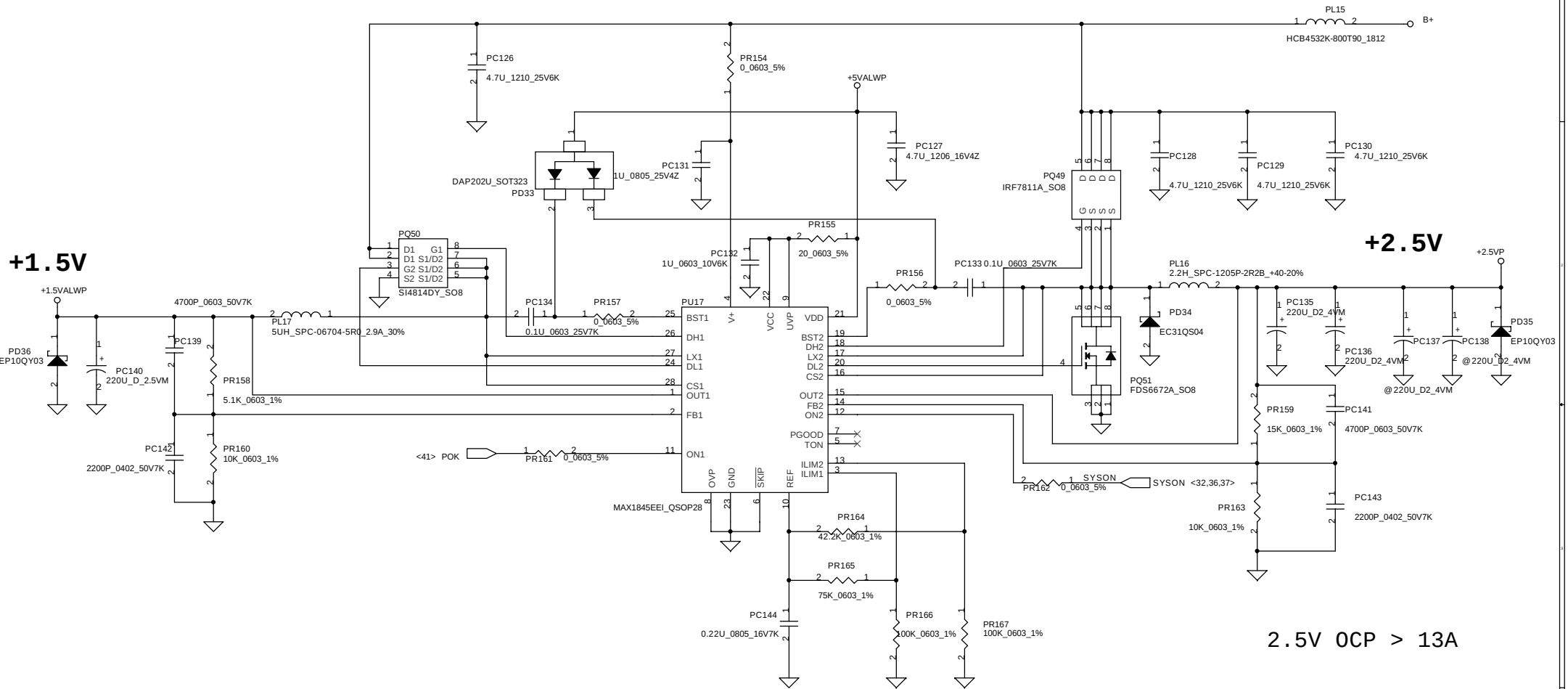




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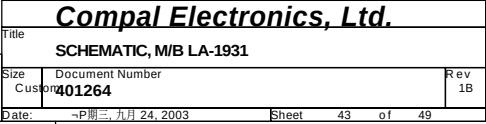
+2.5V/+1.5V

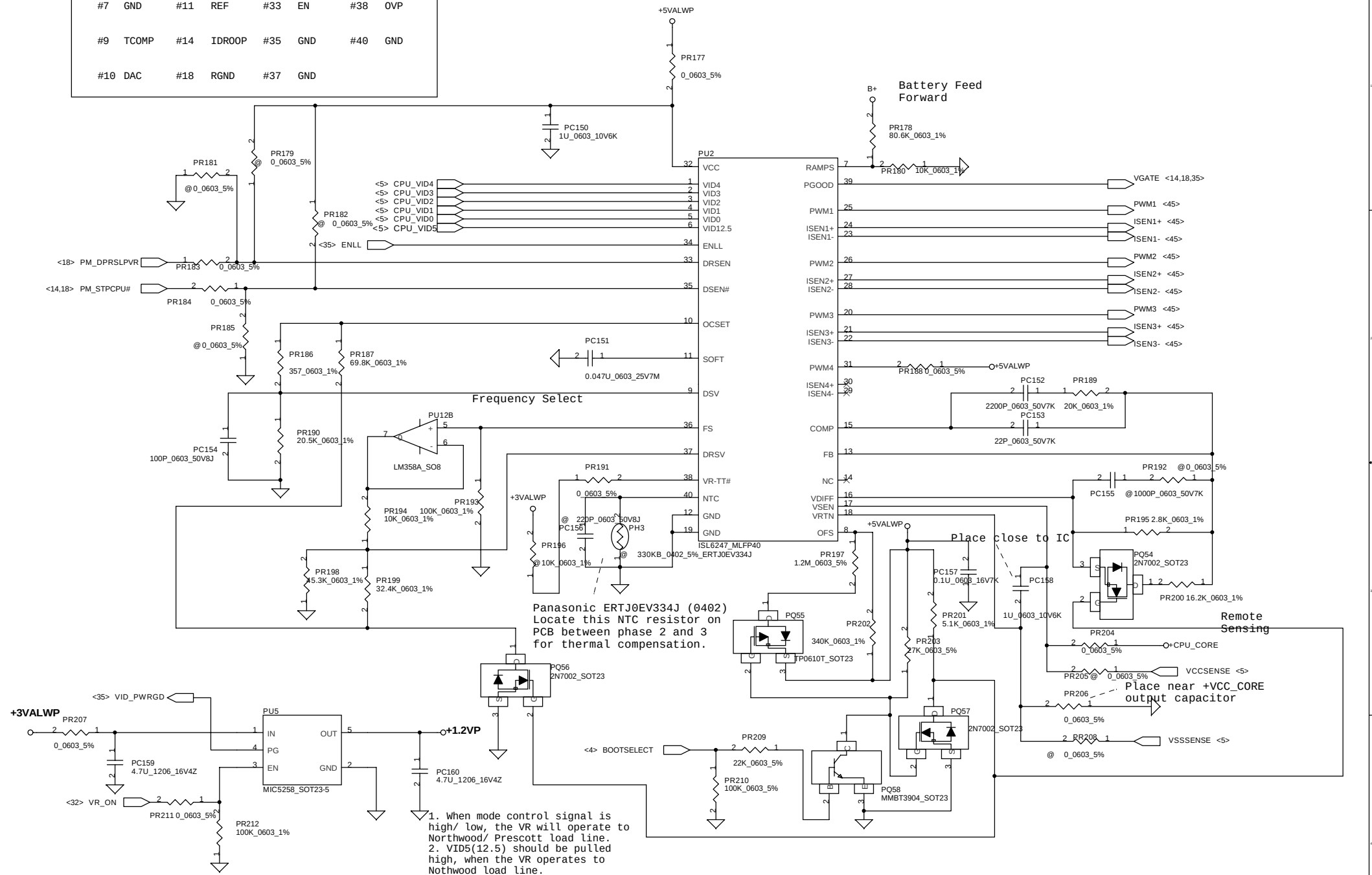


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BOOTSELECT=0 NORTHWOOD

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REV 0.1		
Date	Page	Description
04/10	21	Delete Power interface short line.
04/13	21, 22	Change Card Bus controller as one slote CB1410
	11, 12	Swap RAM data signals.
04/16	29	Add EQ circuit
	43	Add throutholing circuit.
	26, 31	Add FIR and Remove SW DJ cicuit
04/24	17	Add R569 and R570 for Layout Request. Move Signal IRQE#~H# from RP92 to RP91 and del RP92.
	14	CLK-GEN. pin 1(VDD_REF) and pin 46(VDD_CPU_0) change power plan as +3V_VDD. Suggestion from ICS
		C249 and C251 change power plane as +3VDD
04/25	45	PL4 swap pin1 and pin2.
	6	Change CPU Decoupling CAP. from 22U_1210_6.3V6M to 22U_1206_6.3V6M (H=1.6)
	32	1. EC GPIO signal HDD_LED# move from pin114 to pin119. 2. Add signal PM_SLP_S1# on EC GPIO pin115.
04/28	28	Q44 for +5VCD change part name as U55
	8	Del R73, cause it duplicate pull high.
	27	Change C478 and C488 from 150U to 10U
	36	Change R480 from 560K to 620K Ohm
	4	Add R571 for BOOTSELECT
	5	Add R573 for OPTIMIZED/COMPAT#
	18	Add R572 for signal PM DPRSLPVR
04/29		Rename from Layout
04/30	33	R73 0402 -> 0603 and C52 0805 -> 0603
	16	C2, C5, C259, C3, C4, C6, C260, C261 and C262 Link CIS.
	5	Thermal Sensor : Del R62, R61 8.2K-->200Ohm and power +5VS -> +3VS, C27 value 0.1U -> 1U, Sensor power rout direction : +3VS -> R61 -> C27.1 -> U6.1
	17	Add Q40 and Q41, R517 and R518 for SMBus isolate solution.
	8	Change CRT_HSYNC -> INTCRT_HSYNC and CRT_VSYNC -> INTCRT_VSYNC on MGCH terminal.
05/01	8	Change CRT_HSYNC -> INTCRT_HSYNC and CRT_VSYNC -> INTCRT_VSYNC on MGCH terminal.
05/02	33	Remove dummy net on SUSP#.
	16	R28, C277, C278 and C279 modify P/N for CIS link
	17	C215 and C217 modify P/N for CIS link
	22	C145 modify P/N for CIS link
	20	Remove dummy net on XI
	14	R83 and R94 modify P/N for CIS link
	32	CP4 pin2 add connected to GND
05/03	32	CP4 pin2 add connected to GND
05/05	42	PR151 pin1 SYSON signal --> MAINPWON
	8	Swap U26.B6 (INTDDCDA) and U26.G9 (INTDDCCK) --> U26.B6 (INTDDCCK) and U26.G9 (INTDDCDA)
	9	+SDREF circuit move to page 44
	6	Modify Cap.s location same with Layout
	14	Change R129 net from PM_SLP_S3# to PM_SLP_S1#
05/06	16	Add R519 and R520 for EC protect
	20	EEDI_LAN --> EEDI_1394; EECK_LAN --> EECK_1394
	27	Remove R26. Delete USBEN# and U3.3, U3.4, U32.3 and U32.4 connect to GND.
		Delete R30, R279, R258 and R257.
		Change C273, C284 and C646 220U -->150U.
	42	PR151 pin1 SYSON signal --> POK; PU10 pin 11 output POK.
	5	R324 size 0603 -> 0805
05/07	32	U24.175 ATF_INT# --> EC_THERM#
	28	Add L42 between GND and AGND by EMI request.
	17	R408, remove @ for Intel comment.
05/08	5	R56 60.4_0603_1% --> 51.1_0603_1%; R59 102_0603_1% -> 86.6_0603_1%
	35	H19 GNDA -> GND; H31 GND -> GNDA
	37	C242 0.01U -> 0.1U.
	11	JP21 DDR-SO-DIMM link with CIS.
	29	De-pop EQ components, add @ symbol on components.

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Date	Page	Description
05/12	35	Change H31 GND --> AGND and H19 AGND --> GND
	37	R104 and R108 power plane changed, +3VALW --> +5VALW
05/29	40	Change PR100 47.5K-->95.3K
		PR100 47.5K-->95.3K;PQ37,PQ38,PQ39 SI4835DY-->SI4825DY
		PR79 0.015-->0.01; PR86 10K-->100K ;PR90 4.7K-->10K; PR88 29.4K-->33.2K
		Add PR2 95.3K
	38	Change PCN1 90W-->120W
	20	U29 Pin 37 pull up with 4.7K Ohm --> U29 Pin 43
		change X4 footprint same as X2
	16	Add Protect circuit for EC (Add D42, D43 ,D44 and R521)
	32	PWR_SUSP_LED# --> PWR_SUSP_LED
	34	Add reverse circuit for PWR_SUSP_LED (Add Q43 and R522).
	23	change Y2 footprint same as X2
	36	change J1 ~ J6 footprint from JUMP_2MM to 2MM
05/30	35	Add H41 and change H13 H27 size.
06/02	38	Change PL14 value
	39	Change PL13 value
	45	Change PL1 value
	40	Change PQ39 and PL11 value
	11	Add R523, R524, R525 and R526, Del R515
	12	Add R527, R528, R529 and R530
06/03	6	Delete C281, C287, C300, C309, C317, C324, C327 and C330.
06/05	34	Add C648 and C649 for EMI request
	32	Add R531 and R532 for EC floating issue
	8	Add R533 for DVO device detect

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Date	Page	Description
06/12	25	Swap IRQG#_MINI2 and IRQH#_MINI
06/30	30	Change sound resource, cause Headphone without EQ.
07/01	40	Modify PQ38 direction
	28	Add regulator : Add Q44, Q45, Q46, D45 and R536 ~ R539.
		Change C95, C129, C385, C386, C399, C404, C441, C422, C438 and C445 size : 0603 -> 0402.
	29	Change R166, R357, R426, R435, R148, R173, R187, R347, R352, R432, R181 and R346 size : 0603 -> 0402.
	30	Change amplifier from TPA6011A4 to TPA0232.
		Add R534, C651 and C650
		Delete R202, R199, R434 and R442.
		Change C563 1U to 0.47U
		Change VR type from A-Curve to C-Curve.
		Change C184, C212, C213, C219 size 0603 -> 0402.
	14	R129 change net from PM_SLP_S1# to PM_SLP_S3#
		Q13 : 2SC2411K --> 2N7002
		R445 : 10K --> 0 Ohm
	10	Change C491 size : 1210 -> 1206; Change C465 and C468 size : 1210 --> D type
	35	Change SYS_PWROK control signal
	25	SWAP PIRQG#_MINI and PIRQH#_MINI_2
07/09	14	U21 and R128 add '@', and R129 remove '@' CLK_PWD#.
	26	U36, U37, C253 and C254 --> @; Add R541 and 542 --> 0 Ohm
	28	Change Q44 --> U59; Add decoupling CAPs., C668 ~ C679.
	35	Change H13 and H27 size
	30	Change ESD diode type near speaker connector. Change D35 and D33 type, Del D34 and D32.
07/10	36	Change S4 resume function power plane +RTC_VCC -> RTCVREF
		Add R543, C680 and C681
	32	Add C682, reserve for PC97551.
07/16	5	R270 R271 R272 R267 R266 R16 R220 1K_0402_5% --> 10K_0402_5%
	32, 8	Delete R412 R399 R369 R390 R485 R306
	16	R304, R314, R317, R310, C318 1_0603_5% -> 1_0402_5%
	18	R422 1_0603_5% -> 1_0402_5%
07/16	5	Add D46 and D47 for EMI solution
	17	Add D48 for EMI solution
	19	Add D49 for EMI solution
	10	C491 C_1210 -> C_1206
	30	MONO_IN GNDA --> GND
07/18	28	Delete L36, L19, L10 and L42
07/21	30	D33, D34 GND --> GNDA
07/22	35	H31 GNDA --> Non-PDH hole.
	29	EQ-1 and EQ-2 GNDA --> GNDA-EQ
		Add R544 for GNDA <-> GNDA-EQ
		Add L44 L45 for EMI request GND <-> GNDA-EQ
	28	Add L36, L19, L10 and L42 for EMI request GNDA <-> GND

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Date	Page	Description
08/04	28	Reserve C683, C684 and C685 for Audio noise issue R370 --> @ C467 and C458 change as 0.1U for Audio noise issue
08/18	44	PC151 0.033U -->0.047U; PC152 1000P --> 2200P; Add PC153 22P
09/19	44	PR195 2.26K --> 2.8K
09/22	45	PR217 PR221 PR225 48.4K -->32.4K

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