



Compal Confidential

ISKAE LA-3661P Schematics Document

Intel Yonah/Merom with 945GM/943GML/940GML+ DDRII + ICH7M

2006-12-22

REV: 0.1

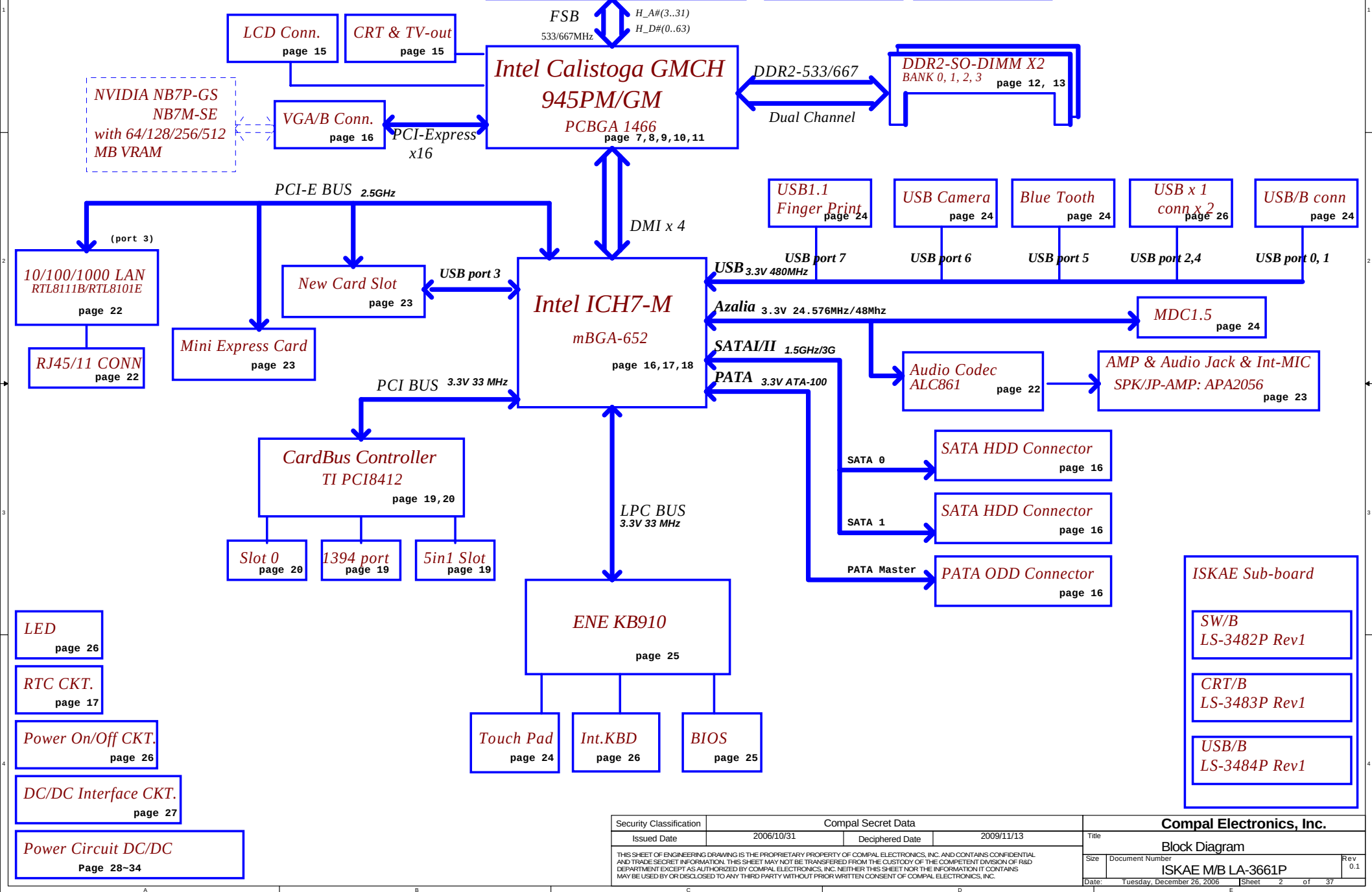
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Compal confidential

Model : ISKAE

File Name : LA-3661P

NAPA Platform



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	+VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
1394	D0	AD20	2	A,B,C
CARD BUS	D4	AD20	2	A,B,C
5IN1	D4	AD20	2	A,B,C

KB910 I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
SM1 24C16	A0H	1 0 1 0 0 0 0 X b
SM1 SMART BATTERY	16H	0 0 0 1 0 1 1 X b
SM2 ADM0132	98H	1 0 0 1 1 0 0 X b
CPU THERMAL MONITOR		

ICH7-M SM Bus address

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table

SKU ID	SKU
0	10 (10E)
1	10C
2	10G
3	10GC
4	10J (10EJ)
5	10CJ
6	10GJ
7	10GCJ

BTO Option Table

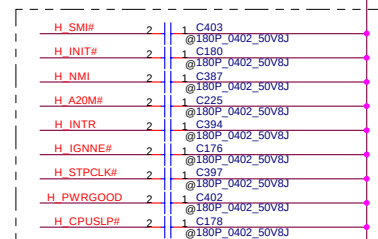
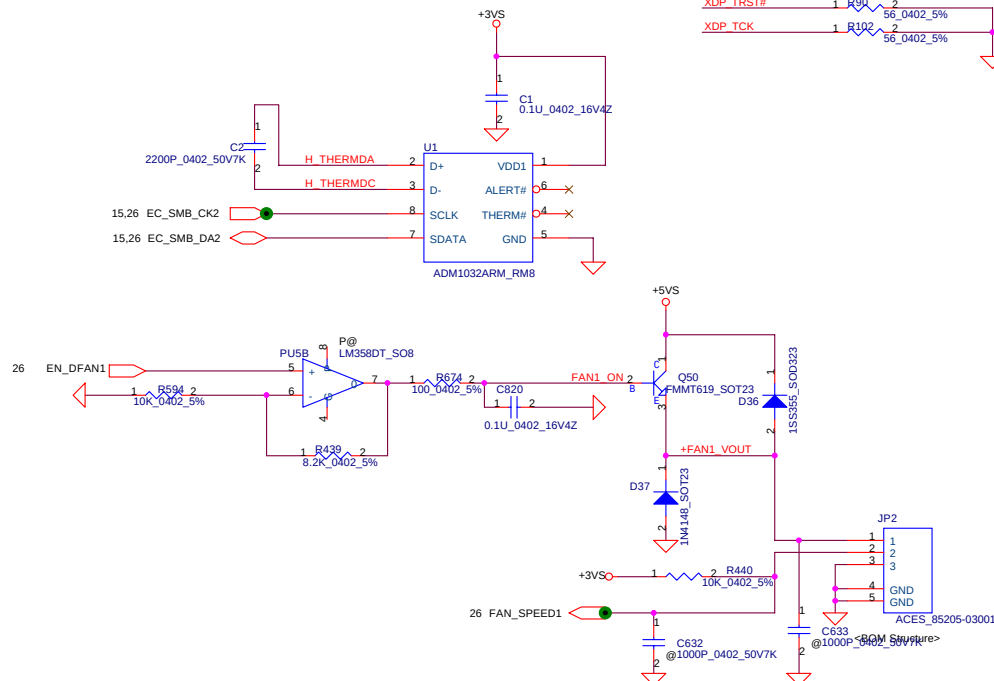
BTO Item	BOM Structure
NEW CARD	NEWCARD@
LAN	100M@ 1000M@
WLAN	KS@
NB	6M@
BT	BT@
MIC	MIC@
CIR	CIR@
FINGER PRINT	FP@
5IN1	5IN1@
CAMERA	CAMERA@
PCMCIA	PCMCIA@
MDC	MDC@



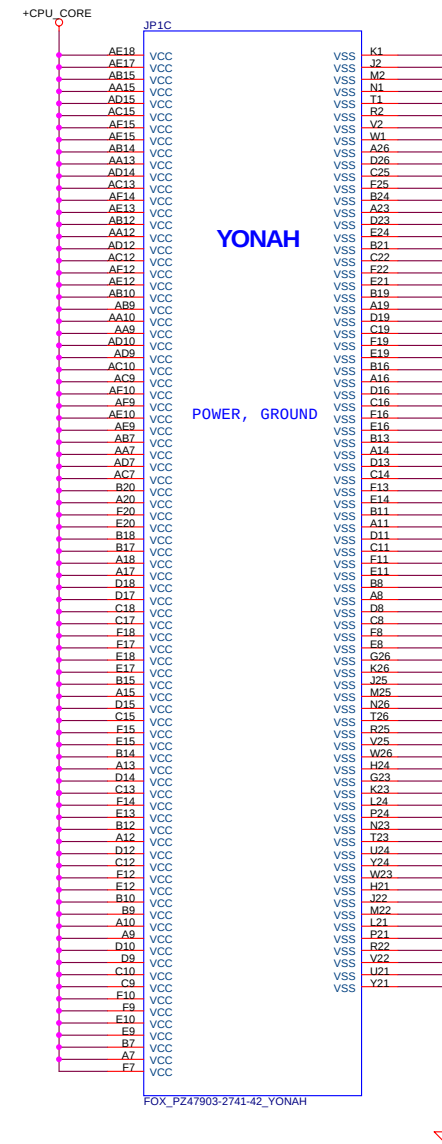
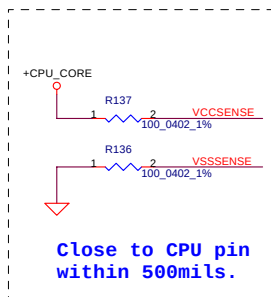
H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil

FOX_P247903-2741-42_YONAH

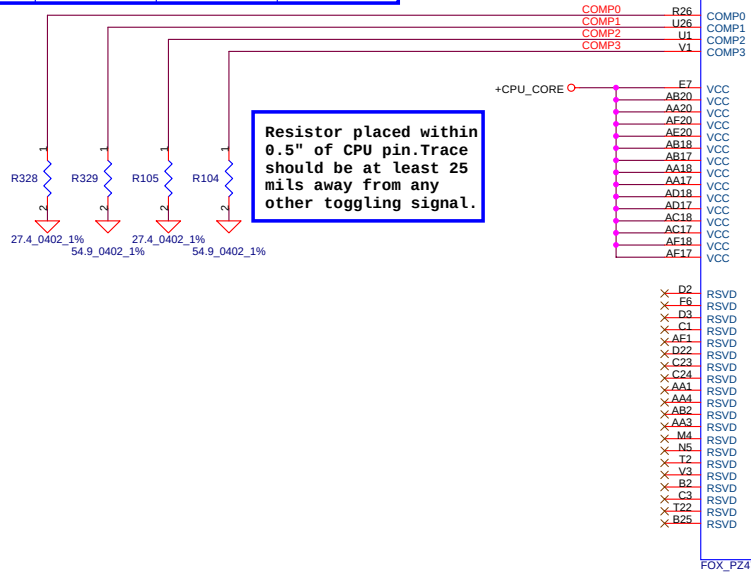
Thermal Sensor ADM1032ARM



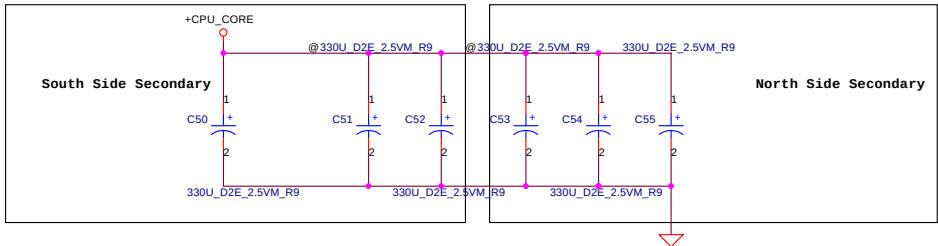
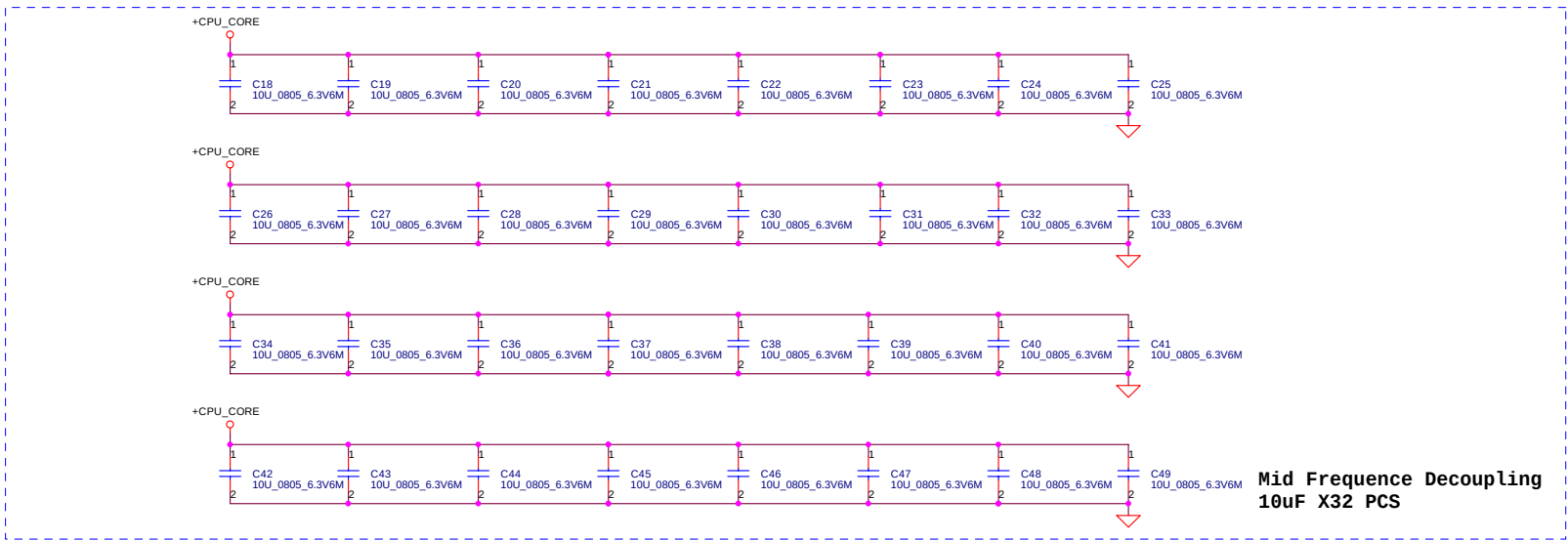
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				Size		Document Number				Rev 0.1	
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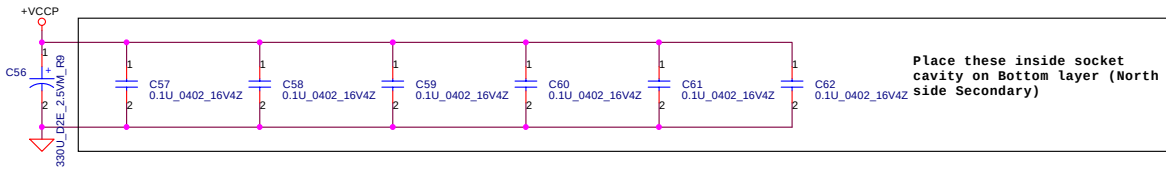
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1



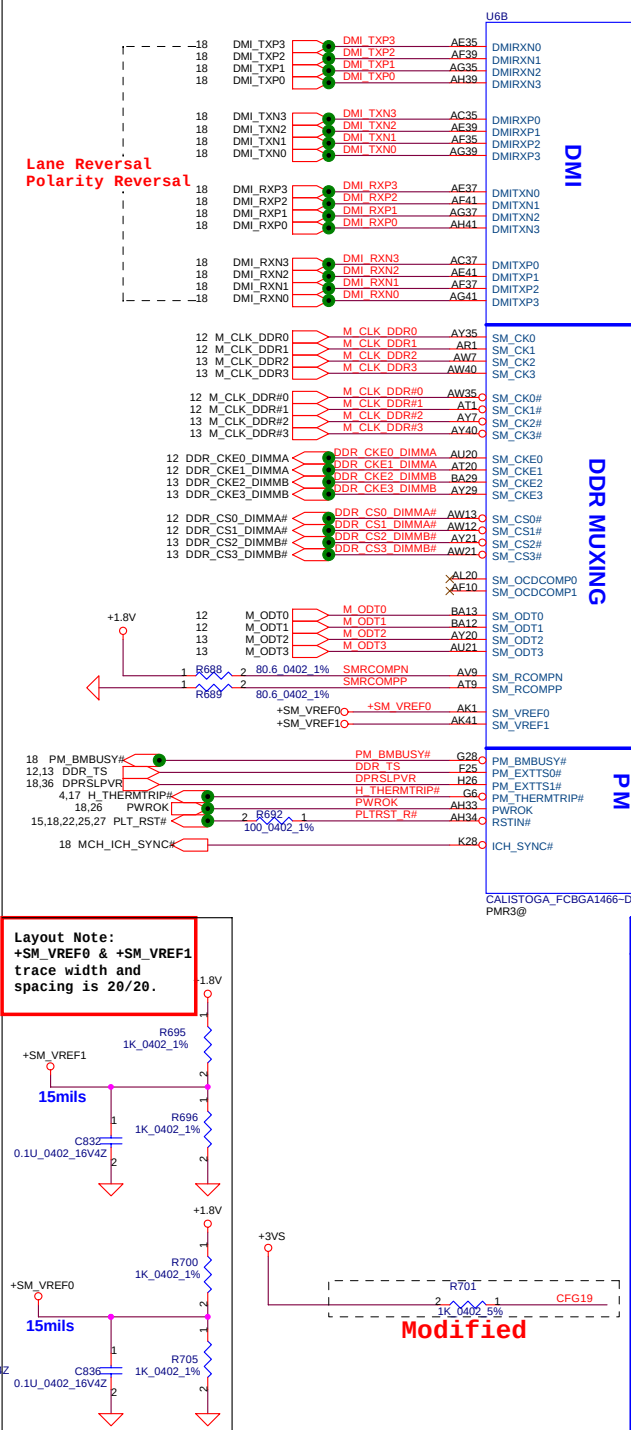
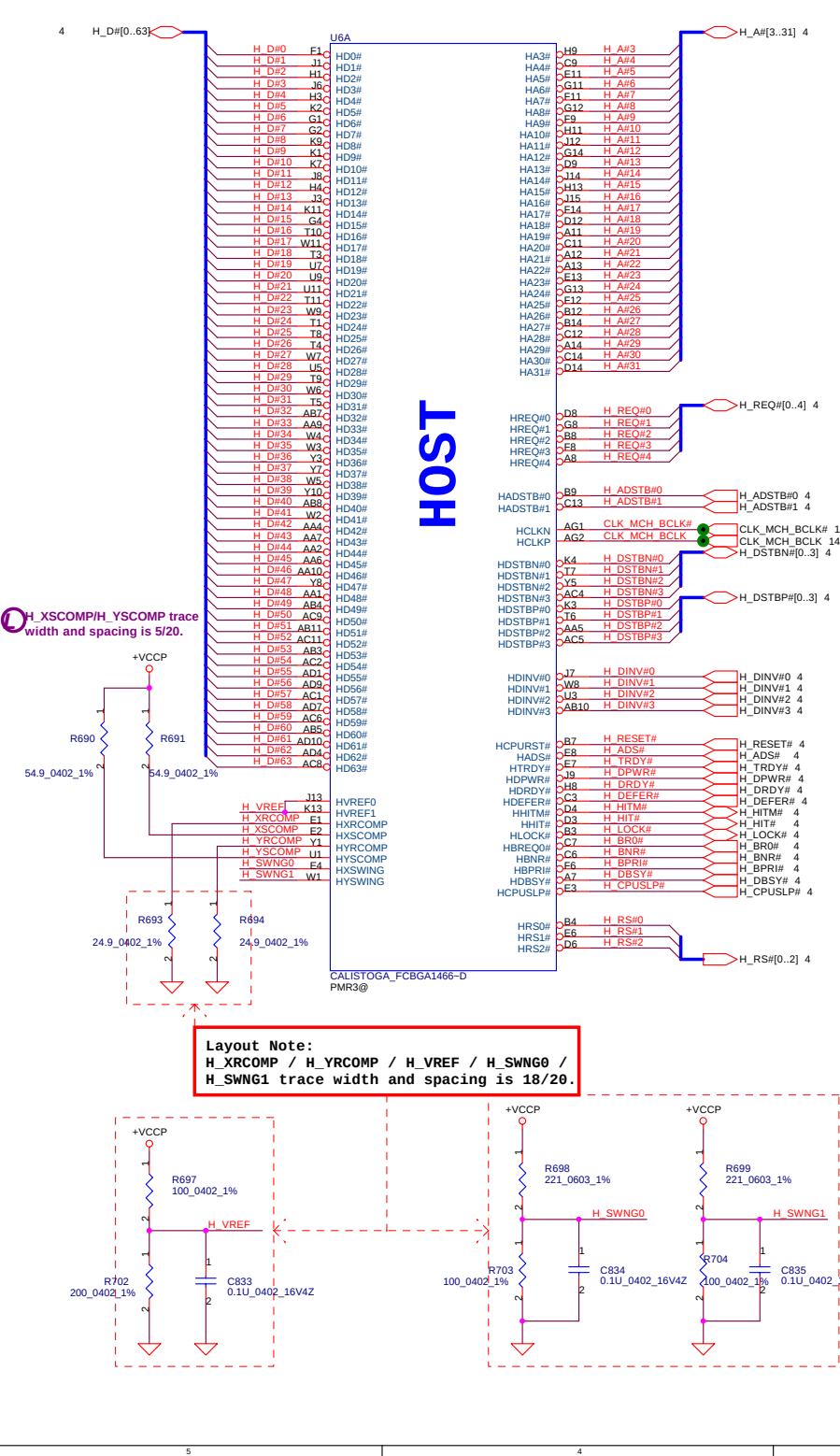
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.



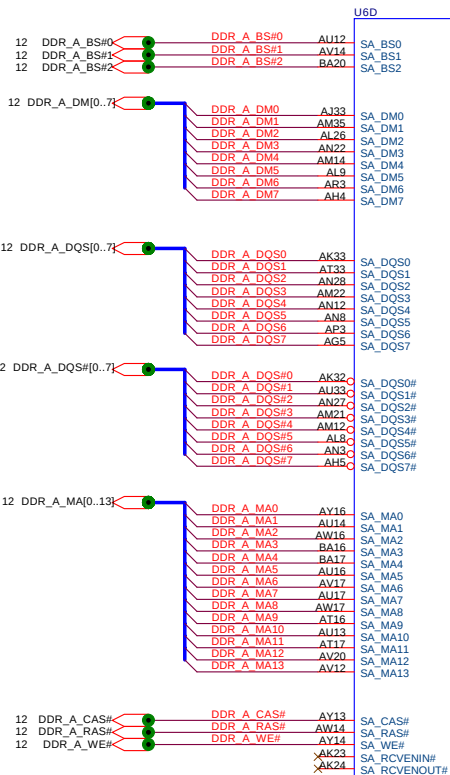
330uF ESR 9m ohm X 6 PCS



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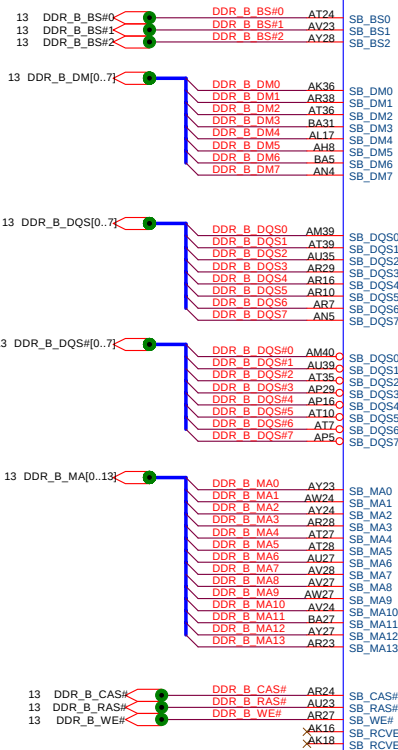
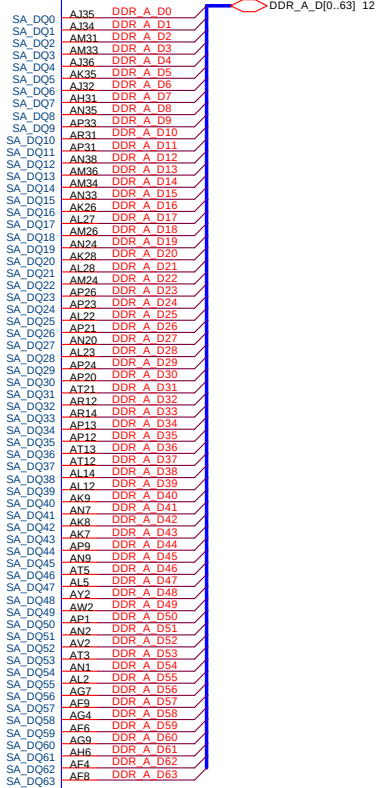
Strap Pin Table		CFG[3:17] have internal pull up CFG[19:18] have internal pull down	
CF6[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB		
CF65	0 = DMI x 2 *1 = DMI x 4 (Default)		
CF67	0 = Reserved *1 = Mobile Yonah CPU (Default)		
CF69	0 = Lane Reversal Enable *1 = Normal Operation (Default)		
CF611	0 = Reserved *1 = Calistoga (Default)		
CF6[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All 2 Mode Enabled *11 = Normal Operation (Default)		
CF616	0 = Dynamic ODT Disabled *1 = Dynamic ODT Enabled (Default)		
CF618	*0 = 1.05V (Default) 1 = 1.5V		
CF619	0 = Normal Operation (Default) *1 = DMI Lane Reversal Enable		
SDVO_CTRLDATA	*0 = No SDVO Device Present (Default) 1 = SDVO Device Present		
CF620 (PCIE/SDVO select)	*0 = Only PCIE or SDVO is operational. (Default) 1 = PCIE/SDVO are operating simu.		



U6D

DDR SYS MEMORY A

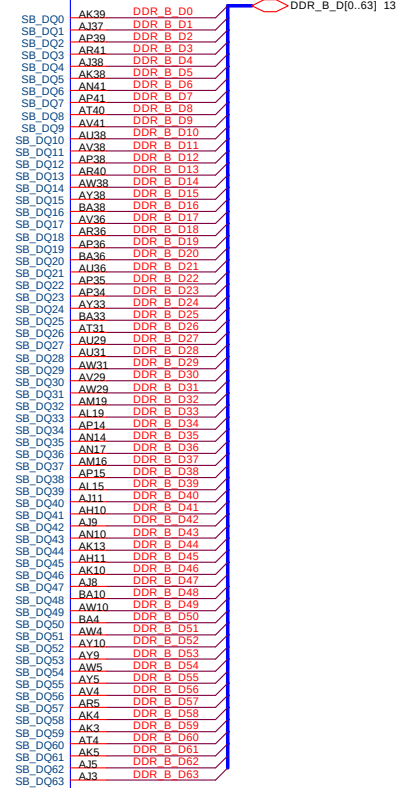
CALISTOGA_FCBGA1466-D
PMR3@



U6E

DDR SYS MEMORY B

CALISTOGA_FCBGA1466-D
PMR3@

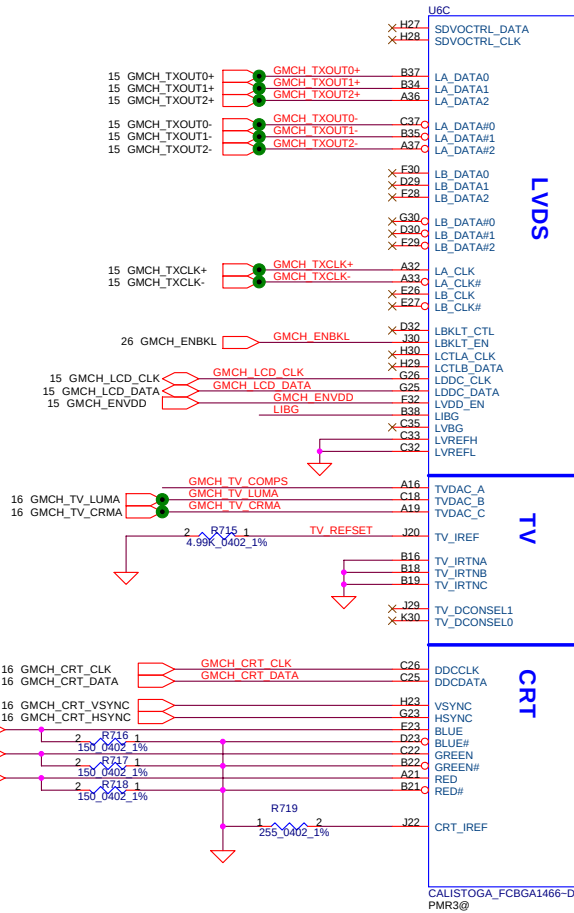
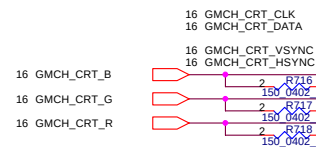
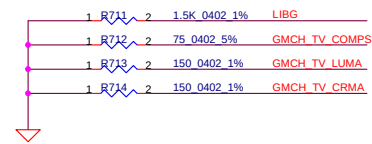
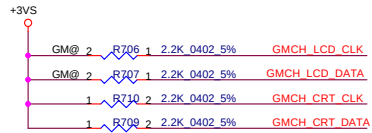


U6E

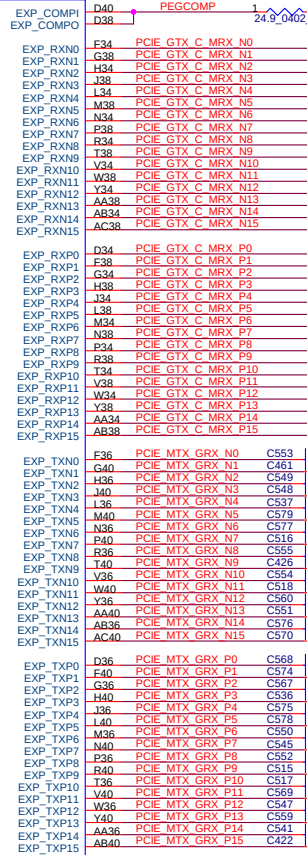
DDR SYS MEMORY B

CALISTOGA_FCBGA1466-D
PMR3@

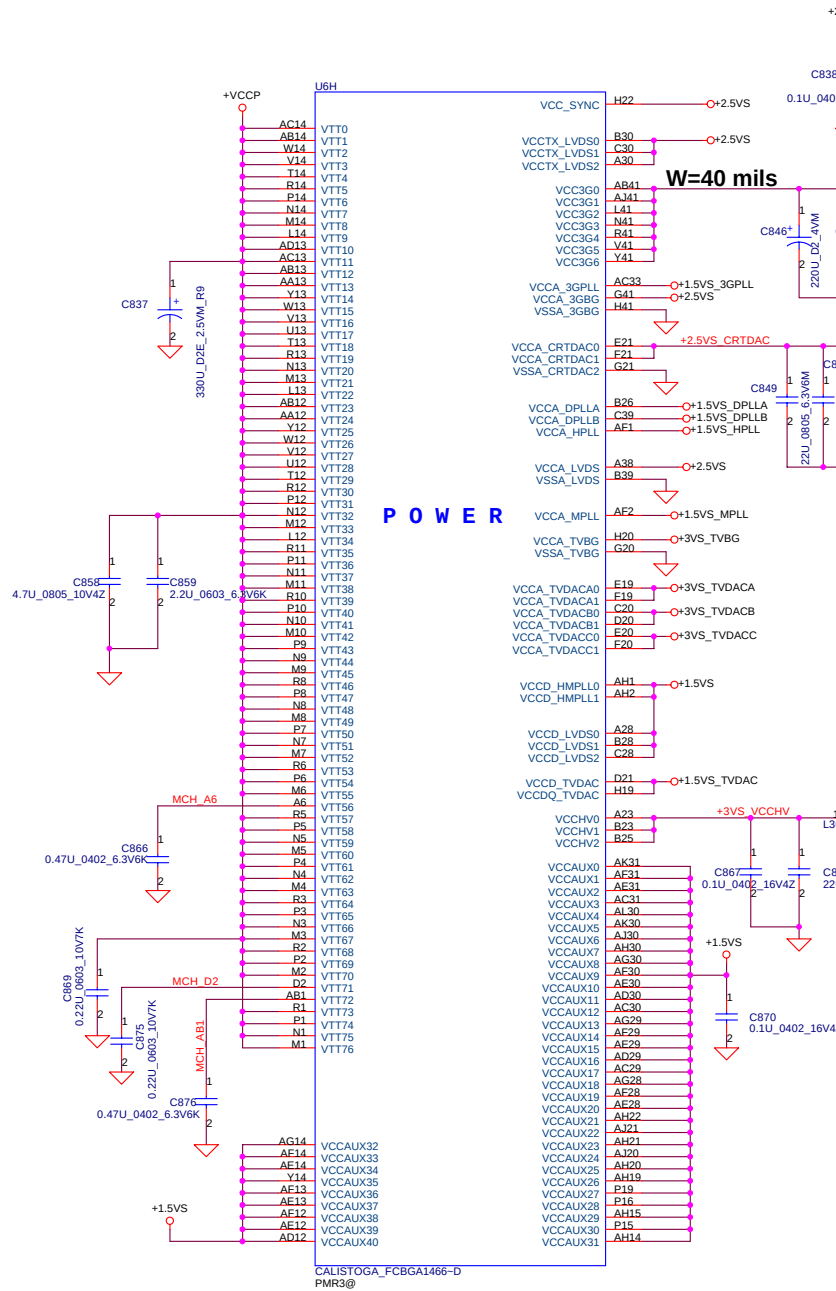
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PEGCOMP trace width and spacing is 18/25 mils.

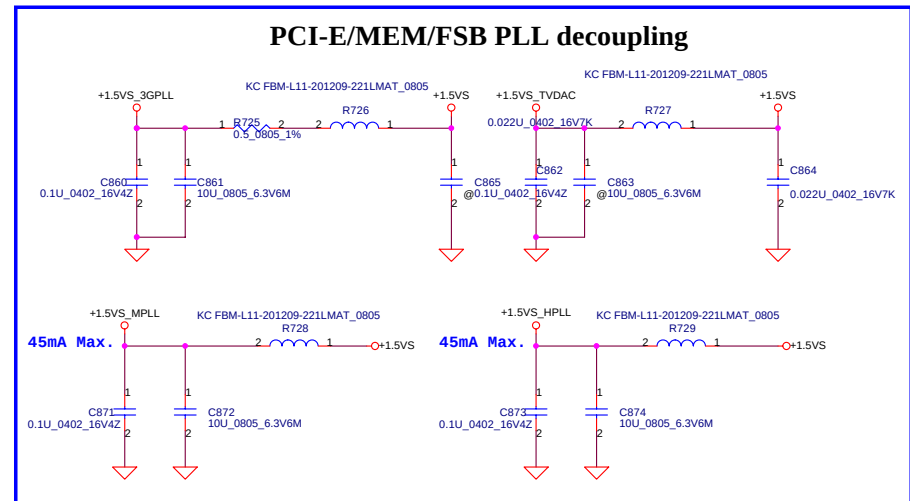


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POWER

W=40 mils



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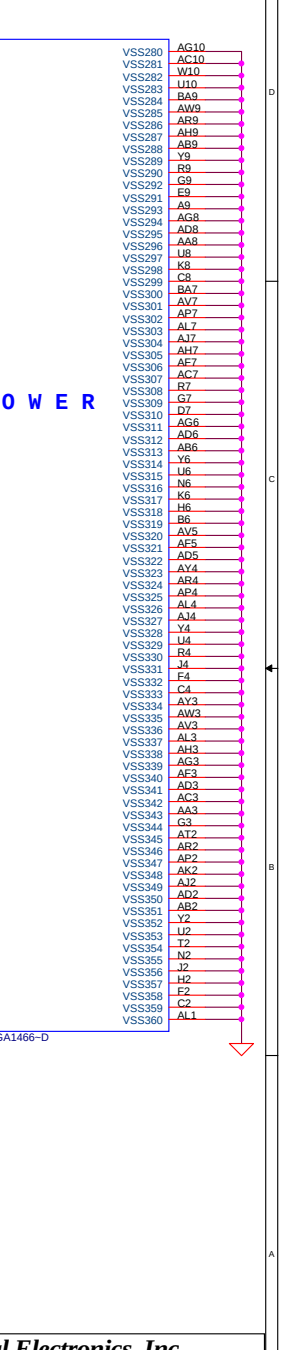
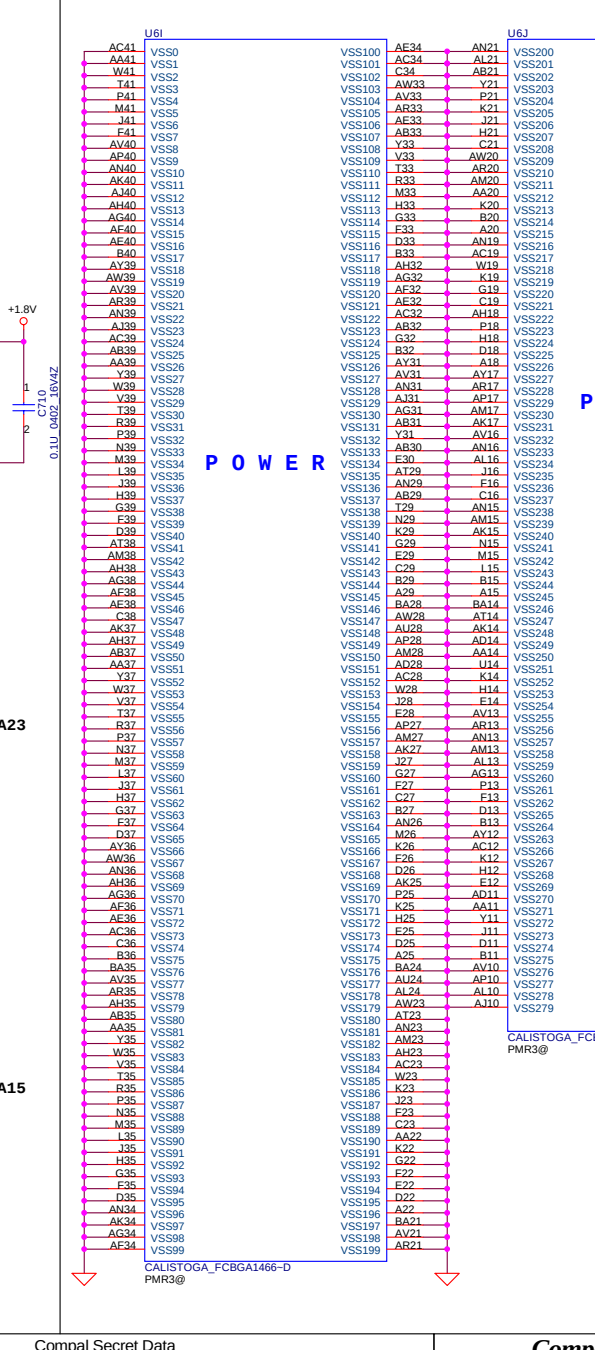
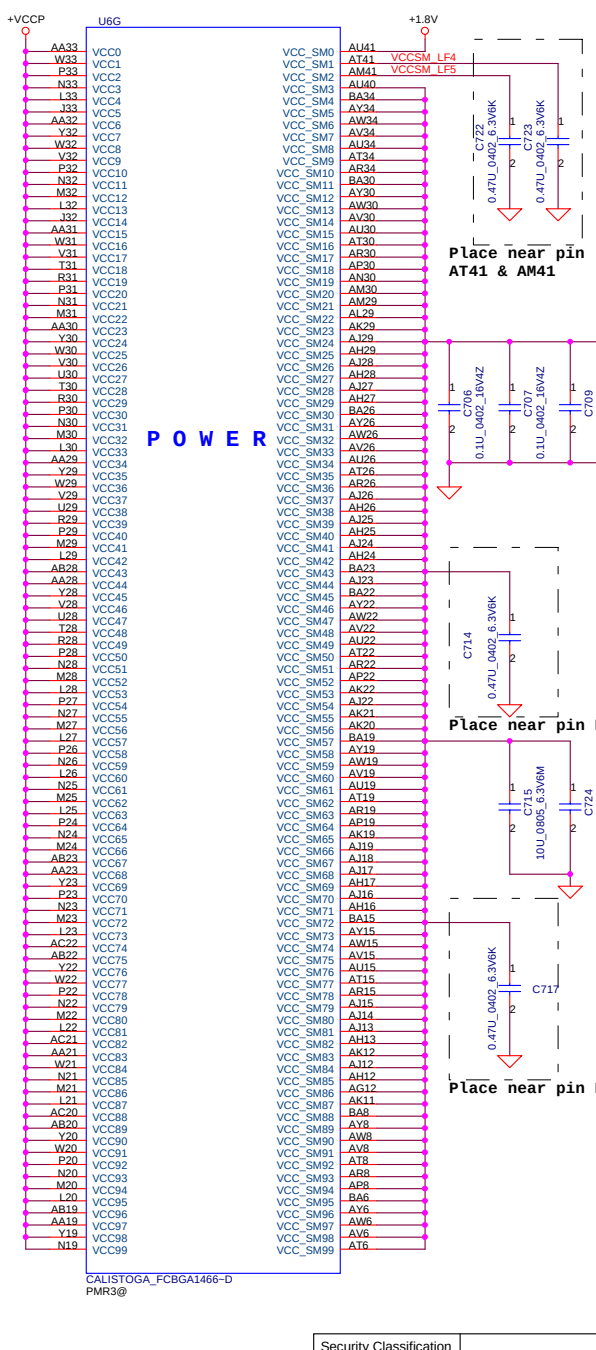
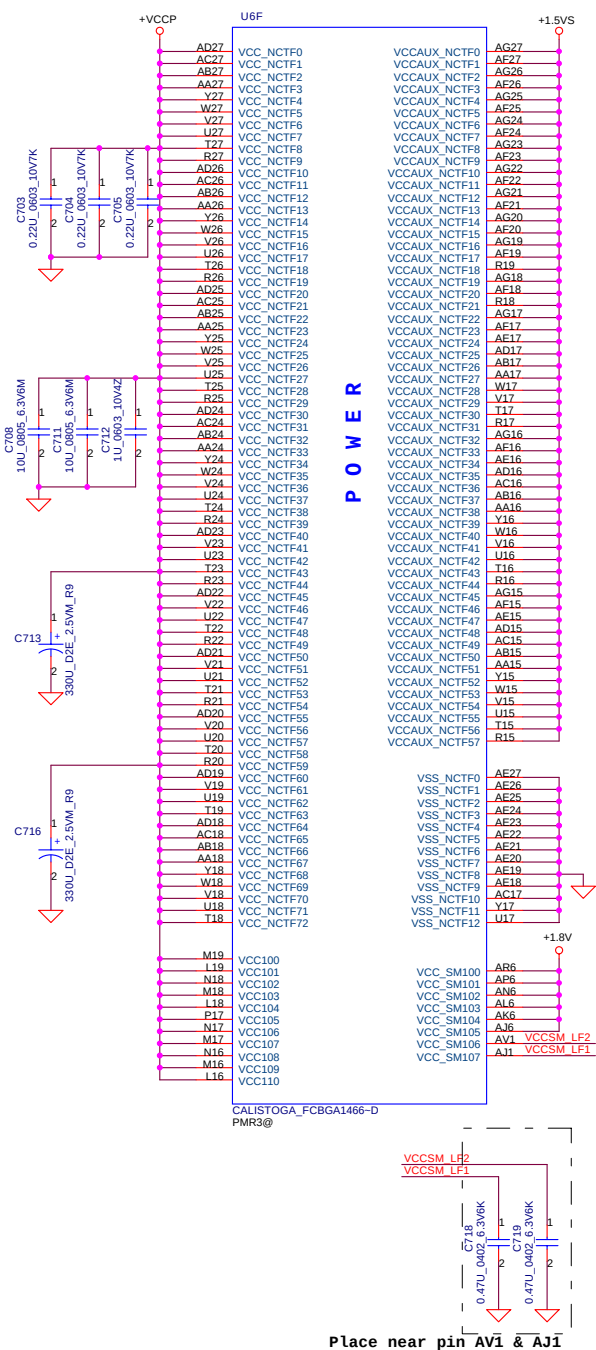
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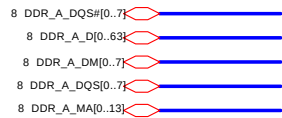
Rev 0.1

POWER

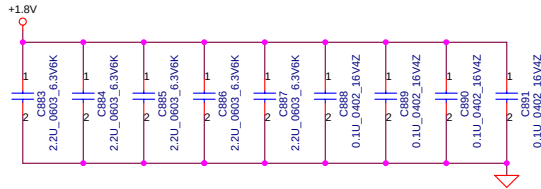


GND

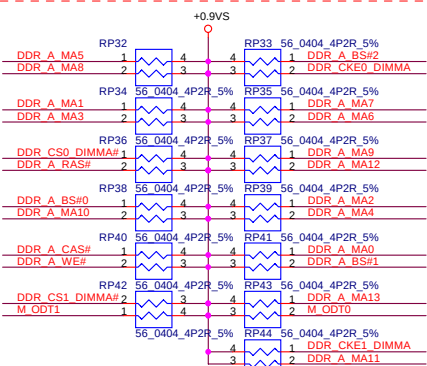
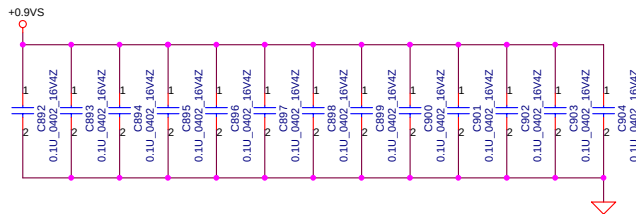
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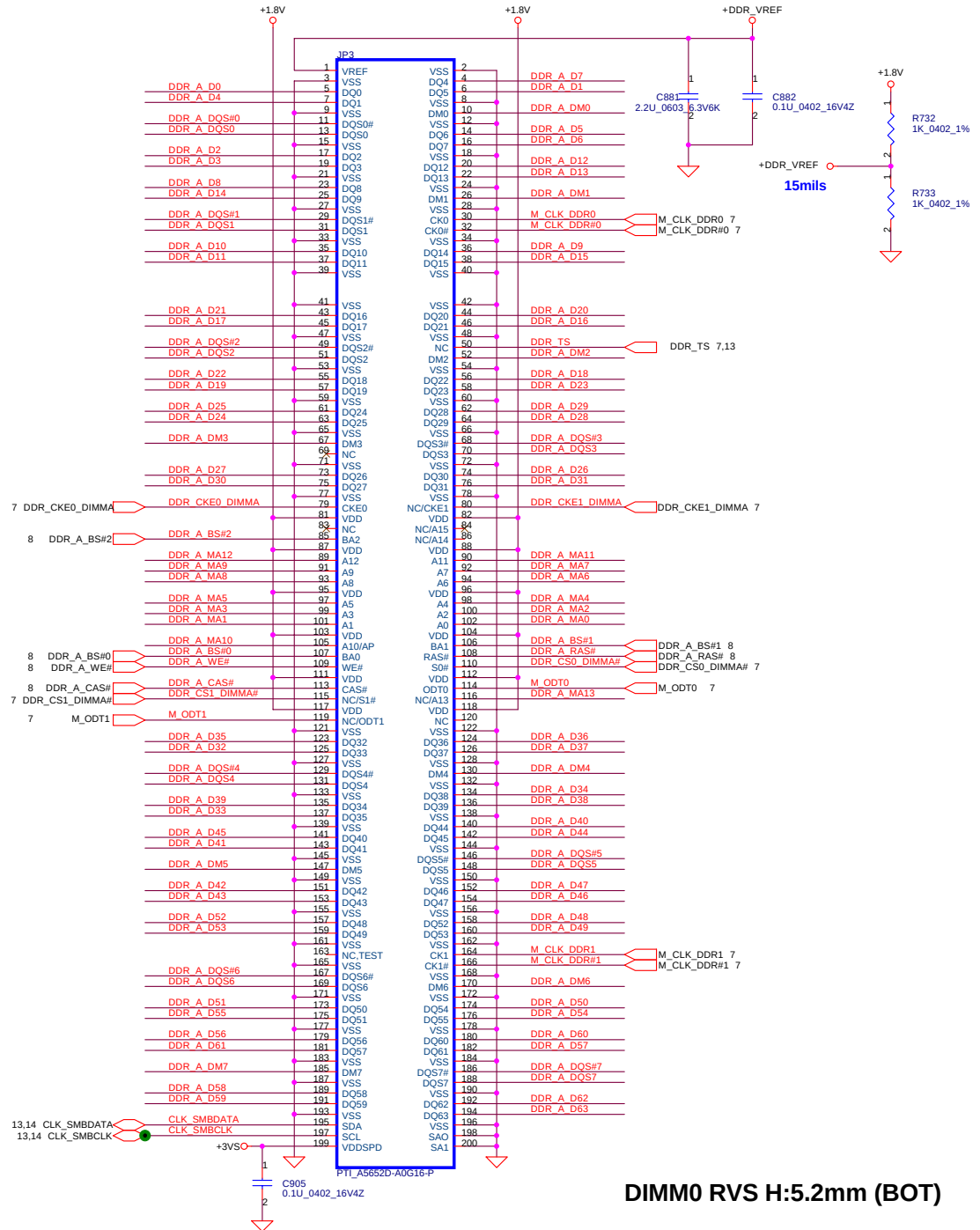
Layout Note:
Place near JP27



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

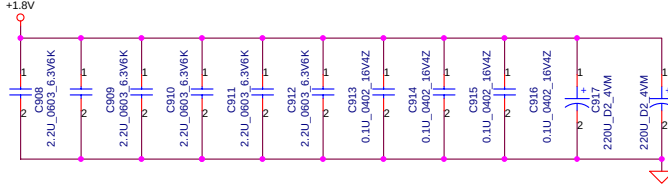


Layout Note:
Place these resistor closely JP27,all trace length Max=1.5"

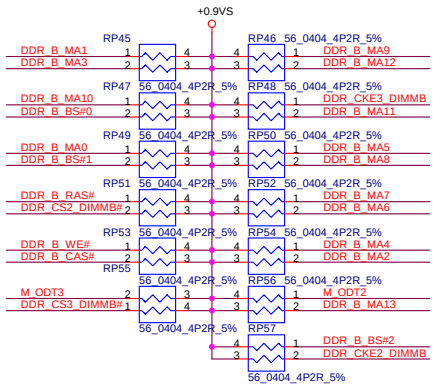
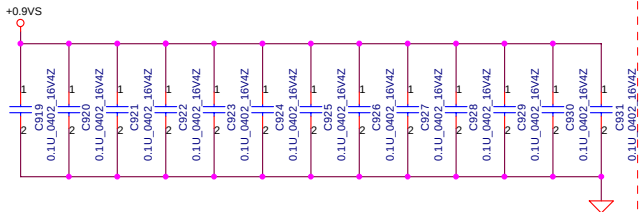


8 DDR_B_DQS#0[0..7] 
8 DDR_B_D[0..63] 
8 DDR_B_DM[0..7] 
8 DDR_B_DQS[0..7] 
8 DDR_B_MA[0..13] 

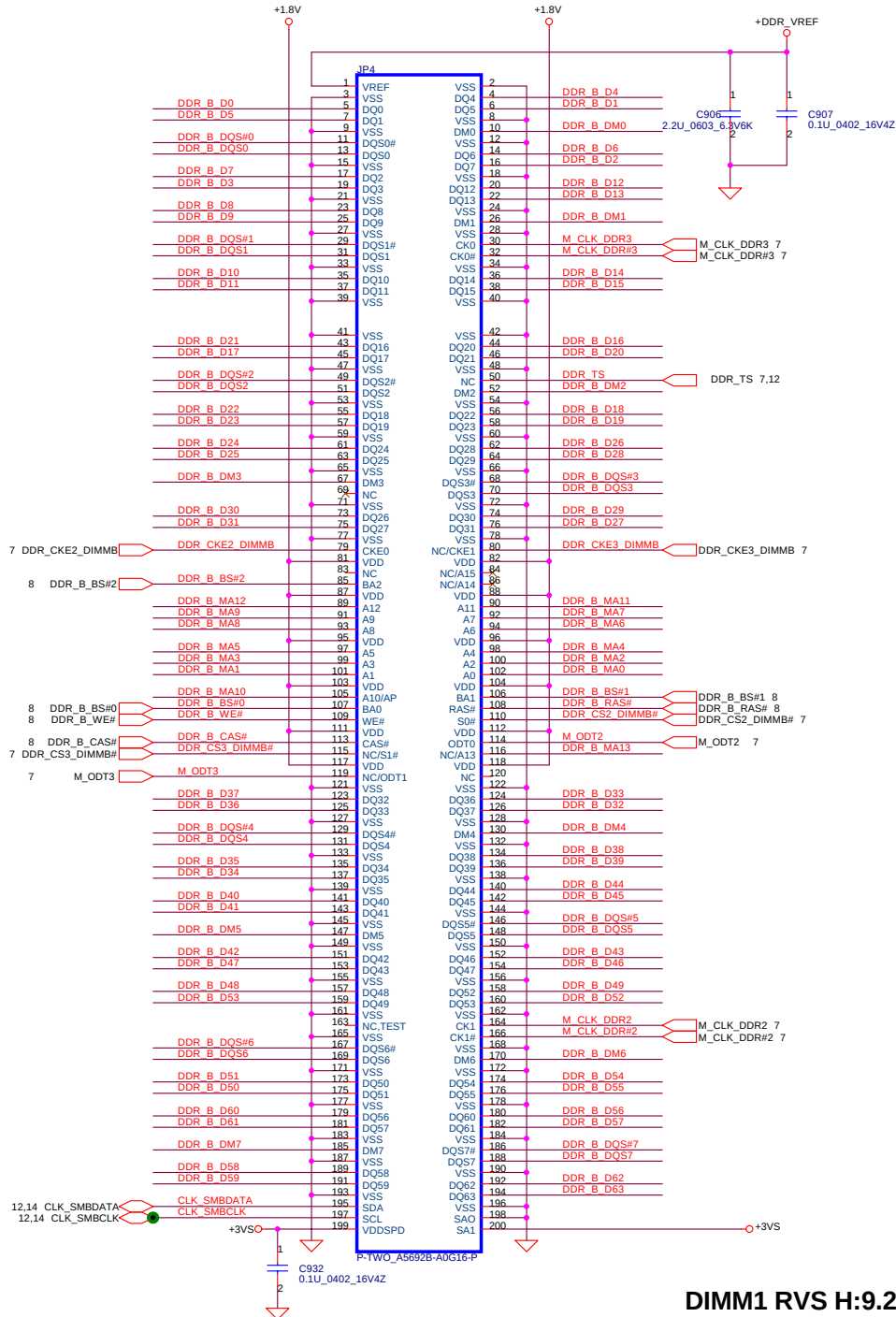
Layout Note:
Place near JP26



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

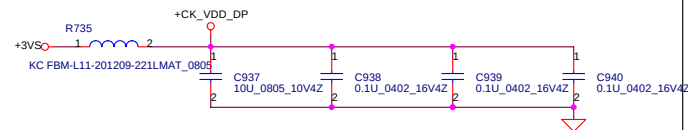


Layout Note:
Place these resistor closely JP26,all trace length Max=1.5"

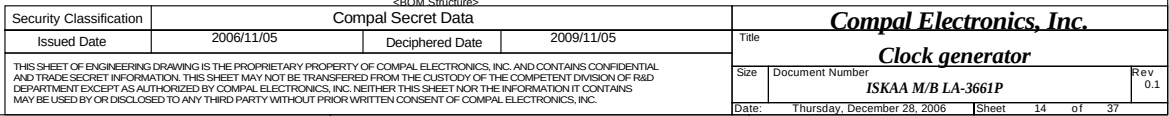


DIMM1 RVS H:9.2mm (BOT)

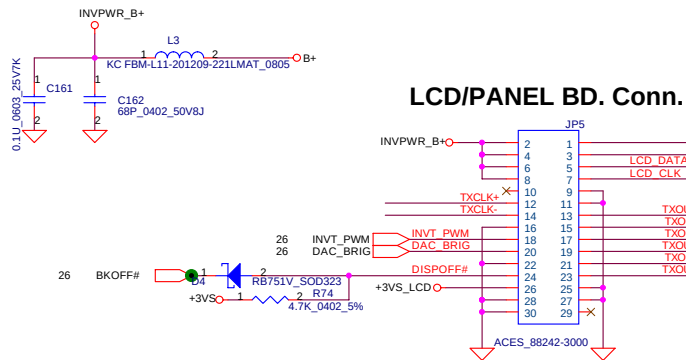
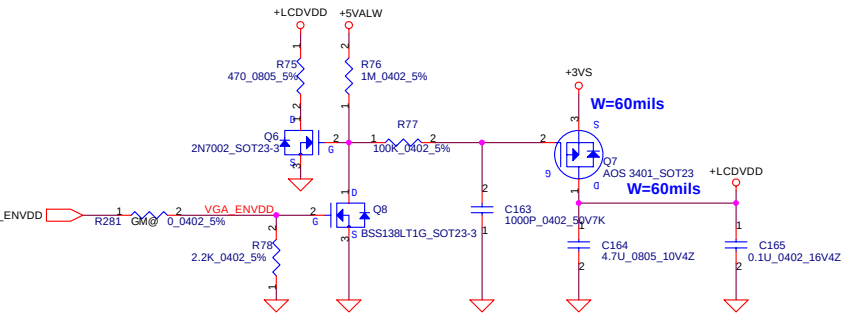
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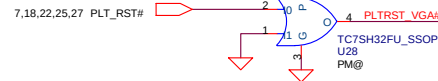
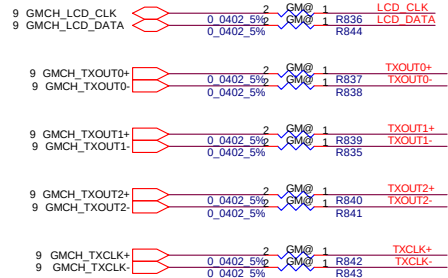
A circuit diagram showing a 10K resistor connected between a +3VS supply and a pin labeled CLK_ENABLE#.



LCD POWER CIRCUIT

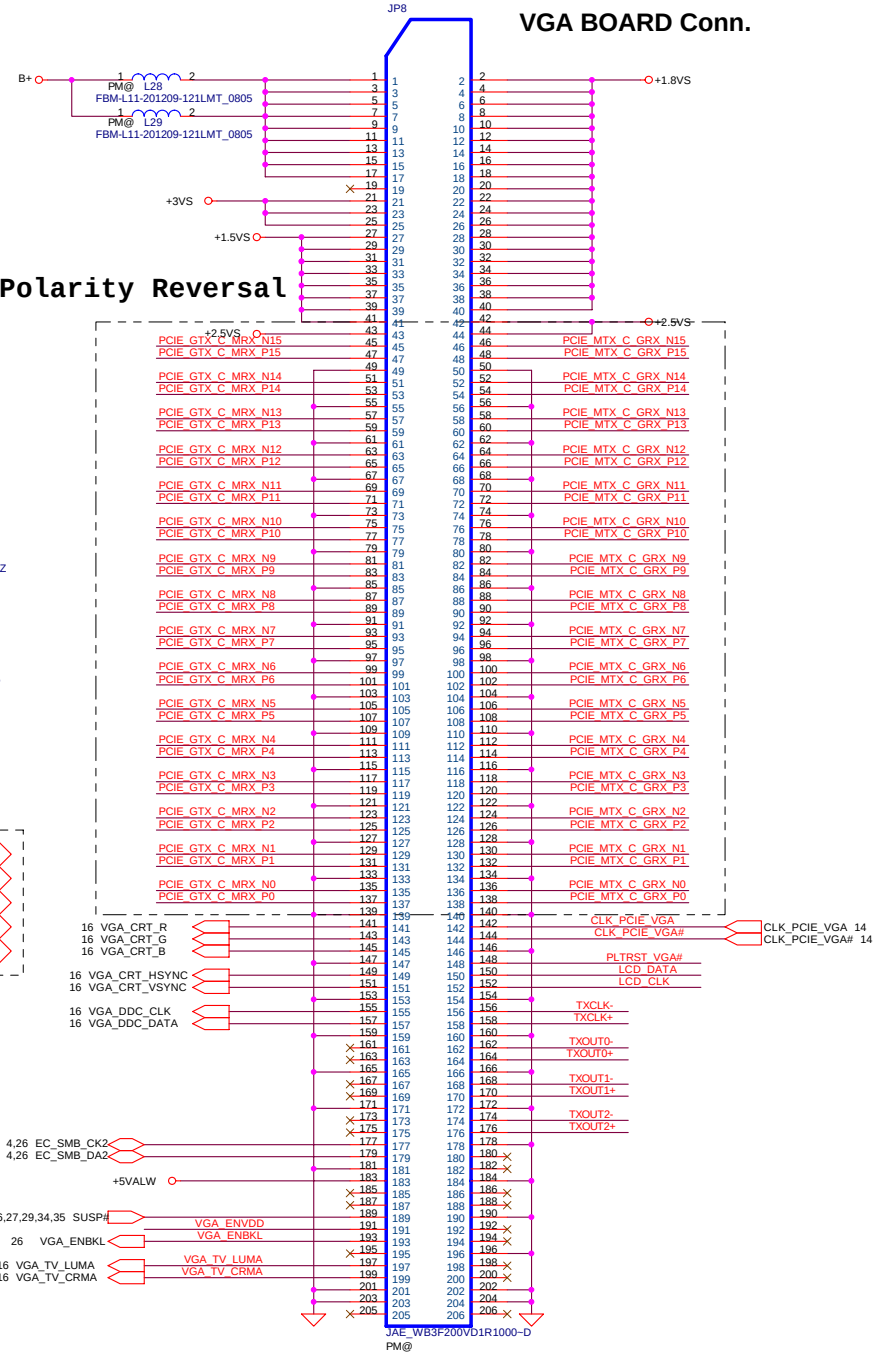


ALL R CLOSE LVDS CONNECTOR



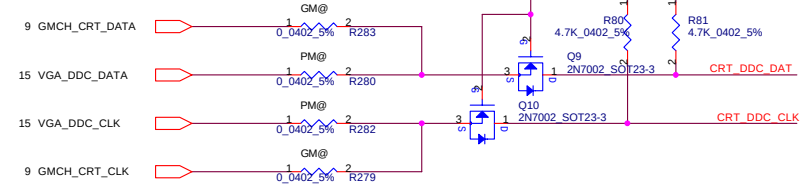
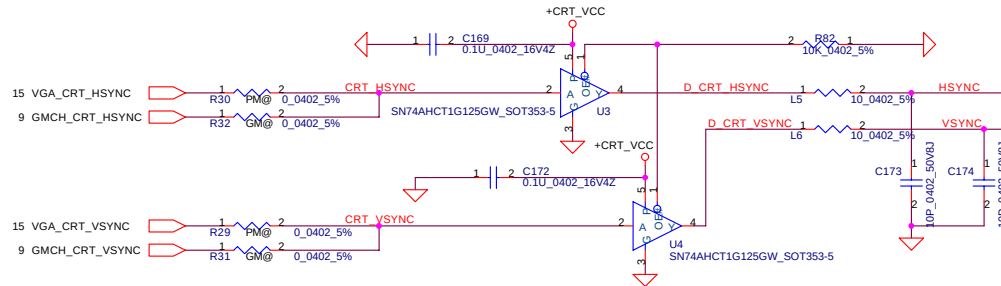
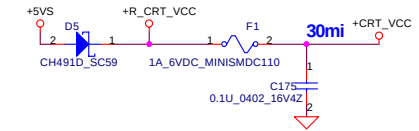
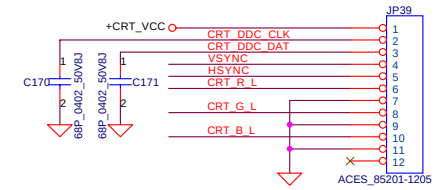
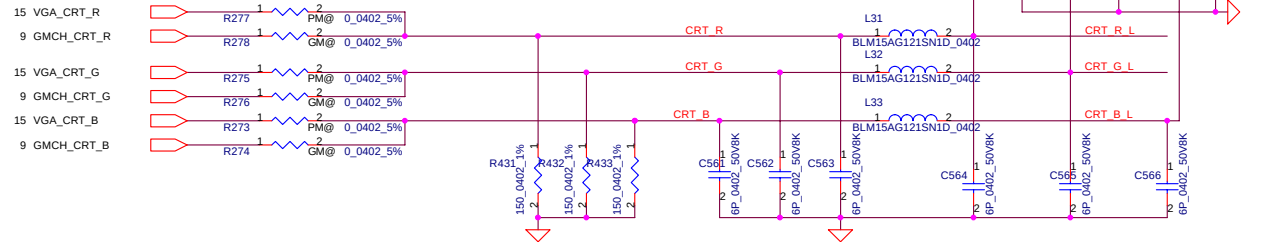
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- 9 PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15]
- 9 PCIE_GTX_C_MRX_N[0..15] PCIE_GTX_C_MRX_N[0..15]
- 9 PCIE_GTX_C_MRX_P[0..15] PCIE_GTX_C_MRX_P[0..15]

Polarity Reversal

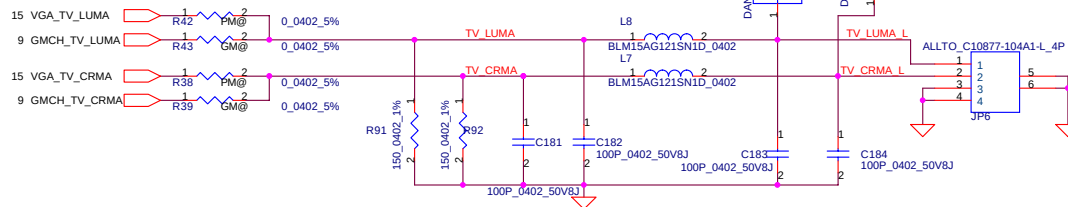


Security Classification				Compal Secret Data				Title			
Issued Date				Deciphered Date				VGA CONN			
2006/08/05				2007/08/05				LA - 3481P			
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Date: Thursday, December 28, 2006				Sheet 15 of 37							

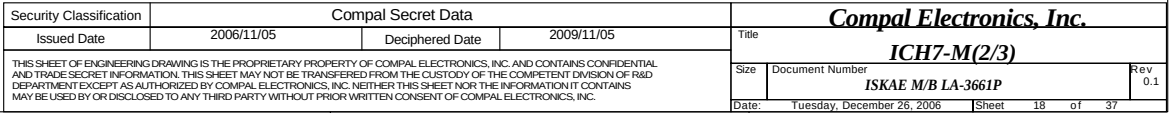
CRT CONNECTOR

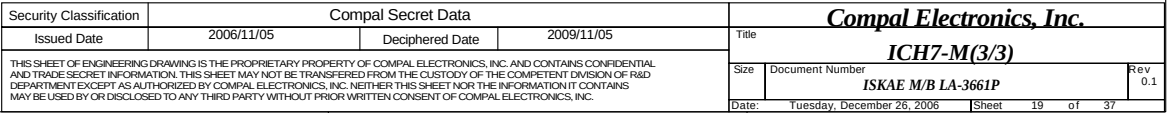


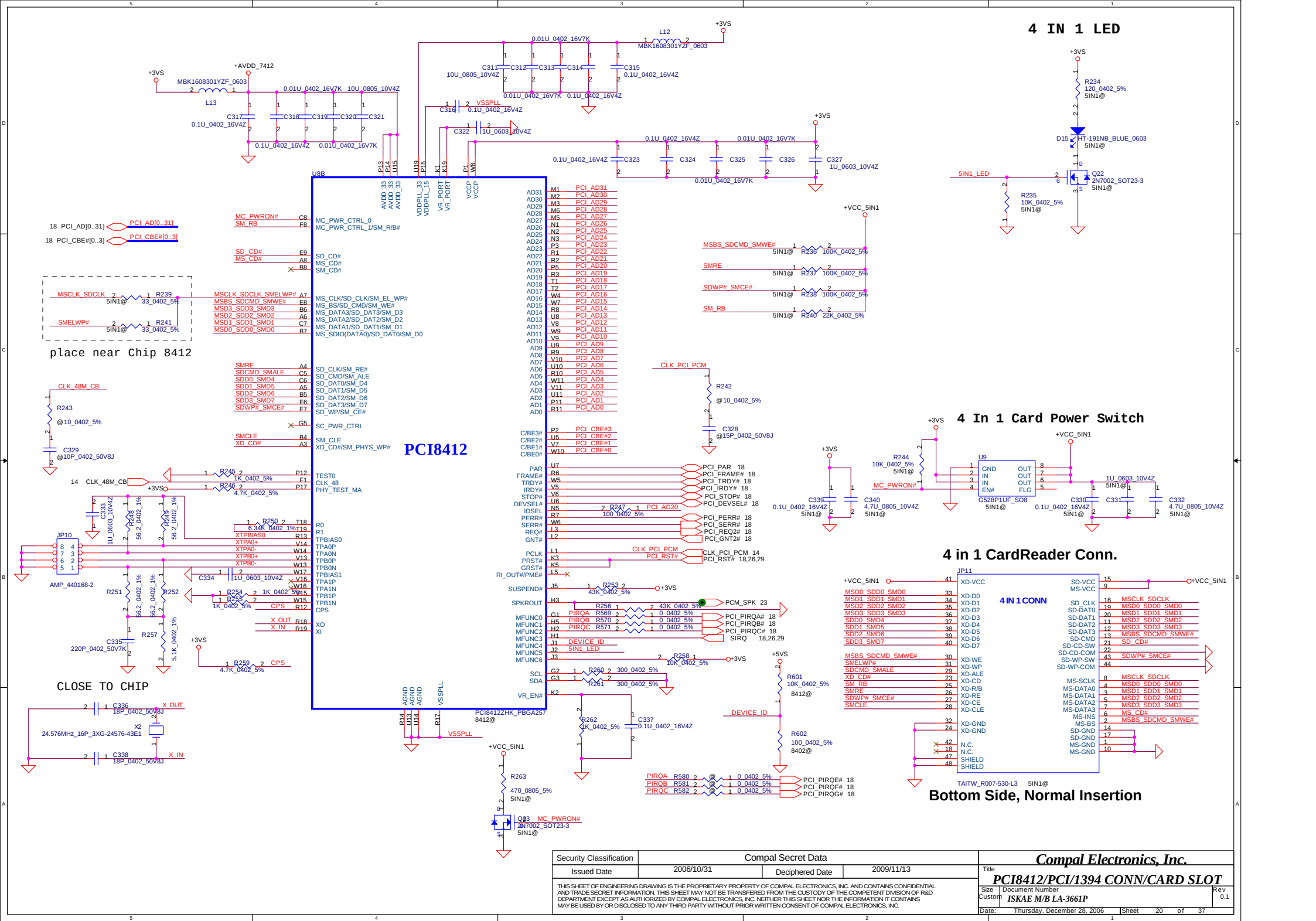
TV-OUT Conn.



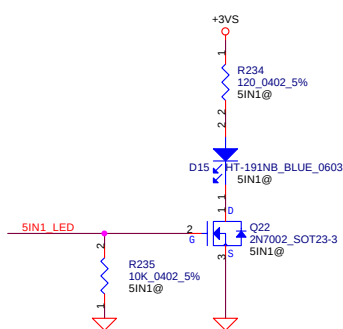
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Issued Date	2006/10/31	Deciphered Date	2009/11/13	Title	
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				0.1	
Date: Thursday, December 28, 2006				Sheet	16 of 37



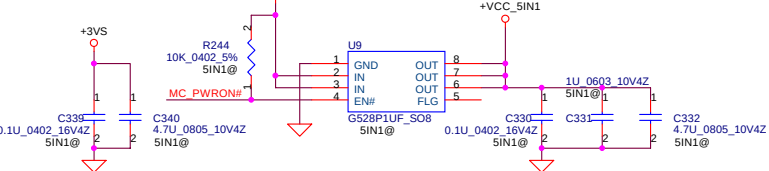




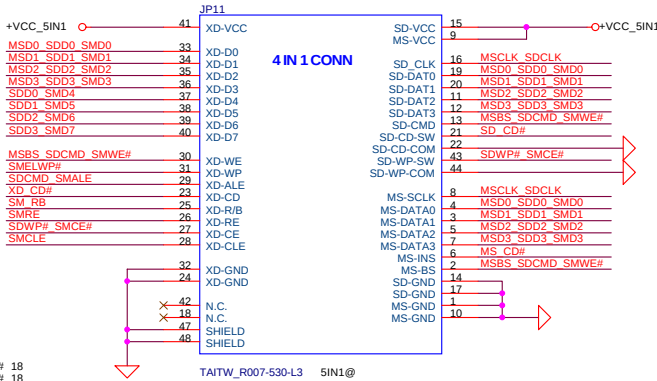
4 IN 1 LED



4 In 1 Card Power Switch



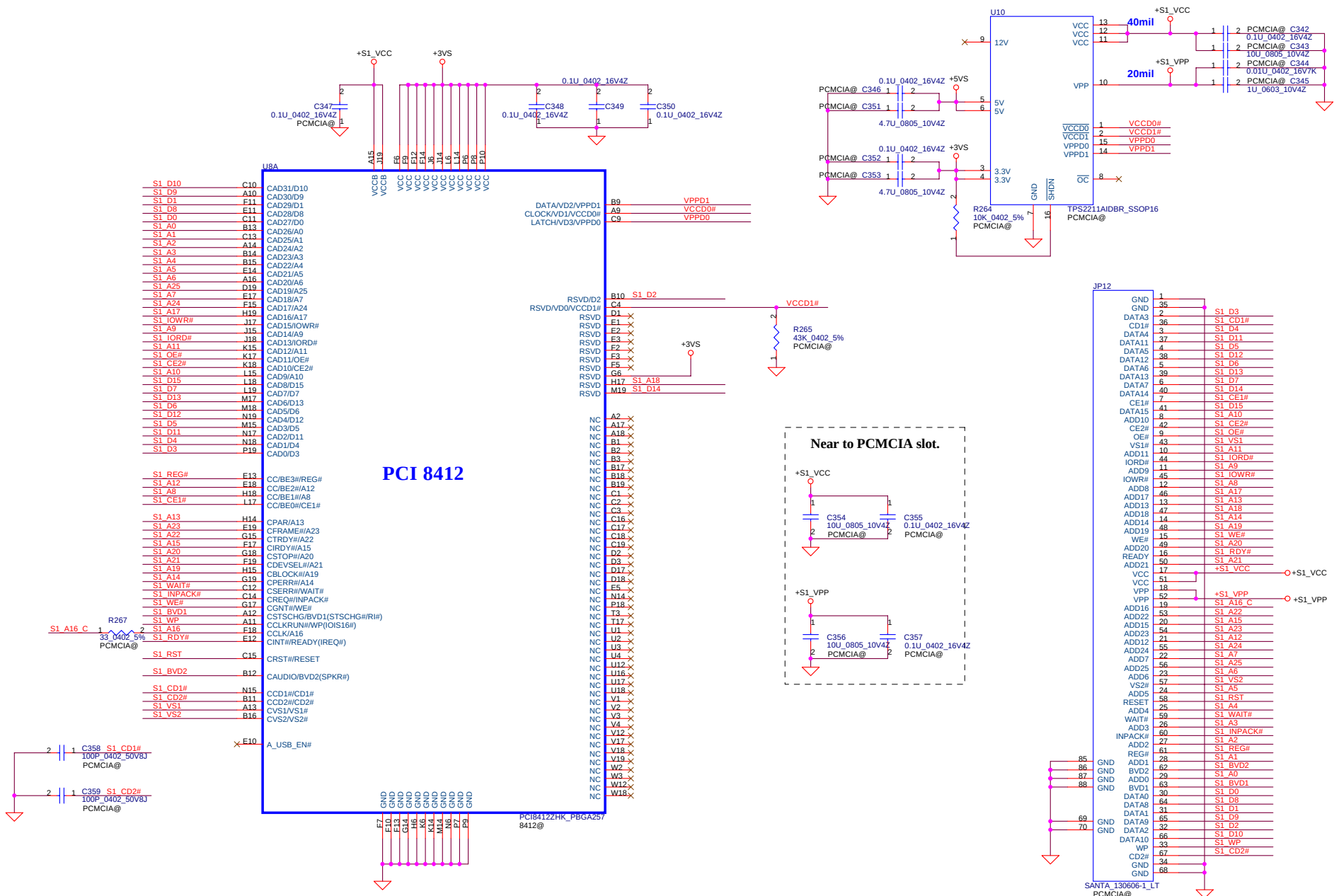
4 in 1 CardReader Conn.



Bottom Side, Normal Insertion

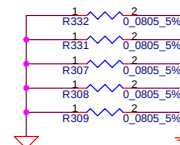
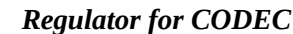
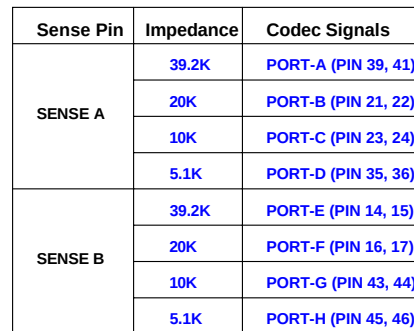
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CardBus Power Switch

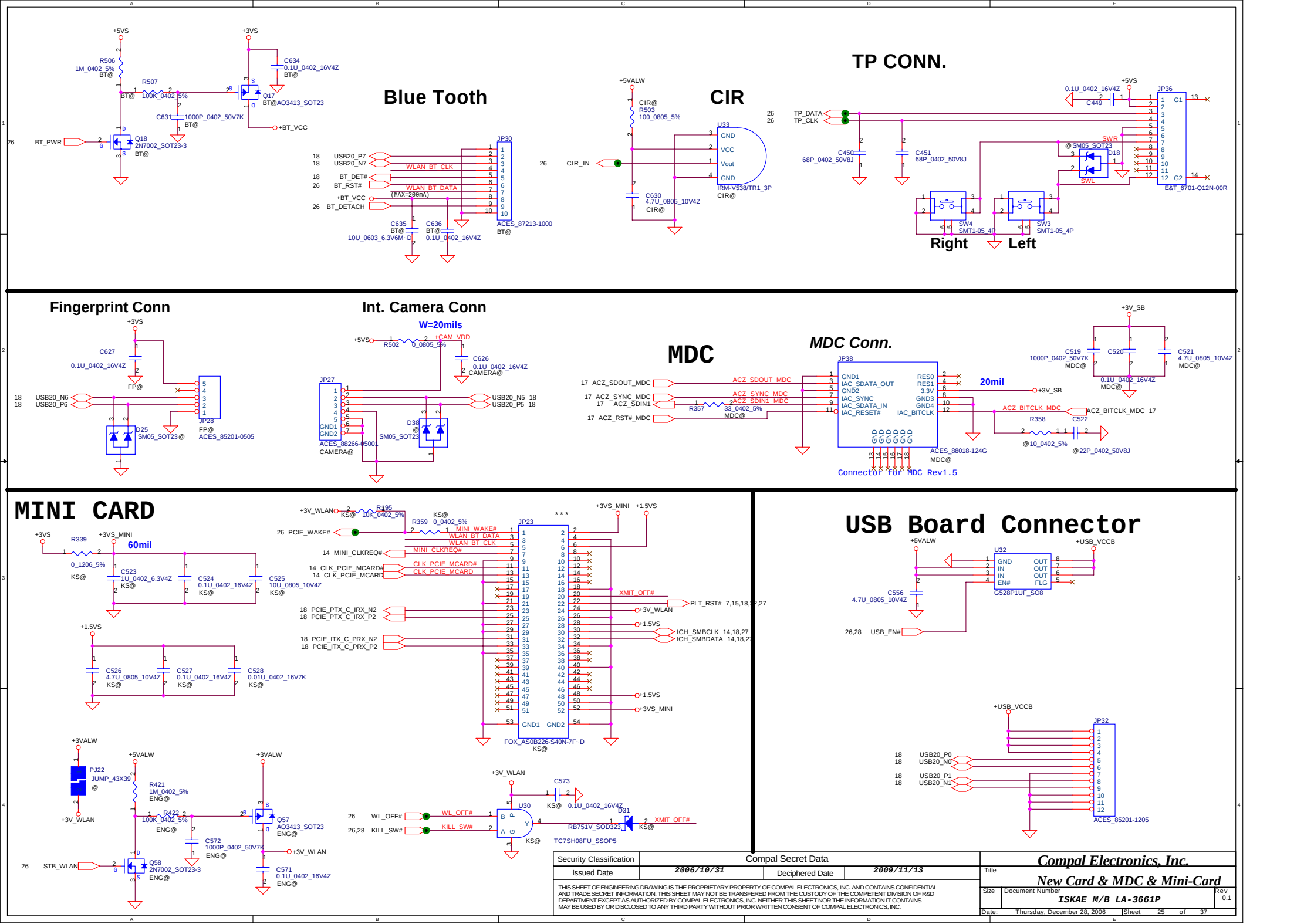


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Issued Date	2006/10/31	Deciphered Date	2009/11/13	Title PCI7412/CB/CB SLOT		
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					ISKAE M/B LA-3661P	0.1
				Date: Tuesday, December 26, 2006		Sheet 21 of 37

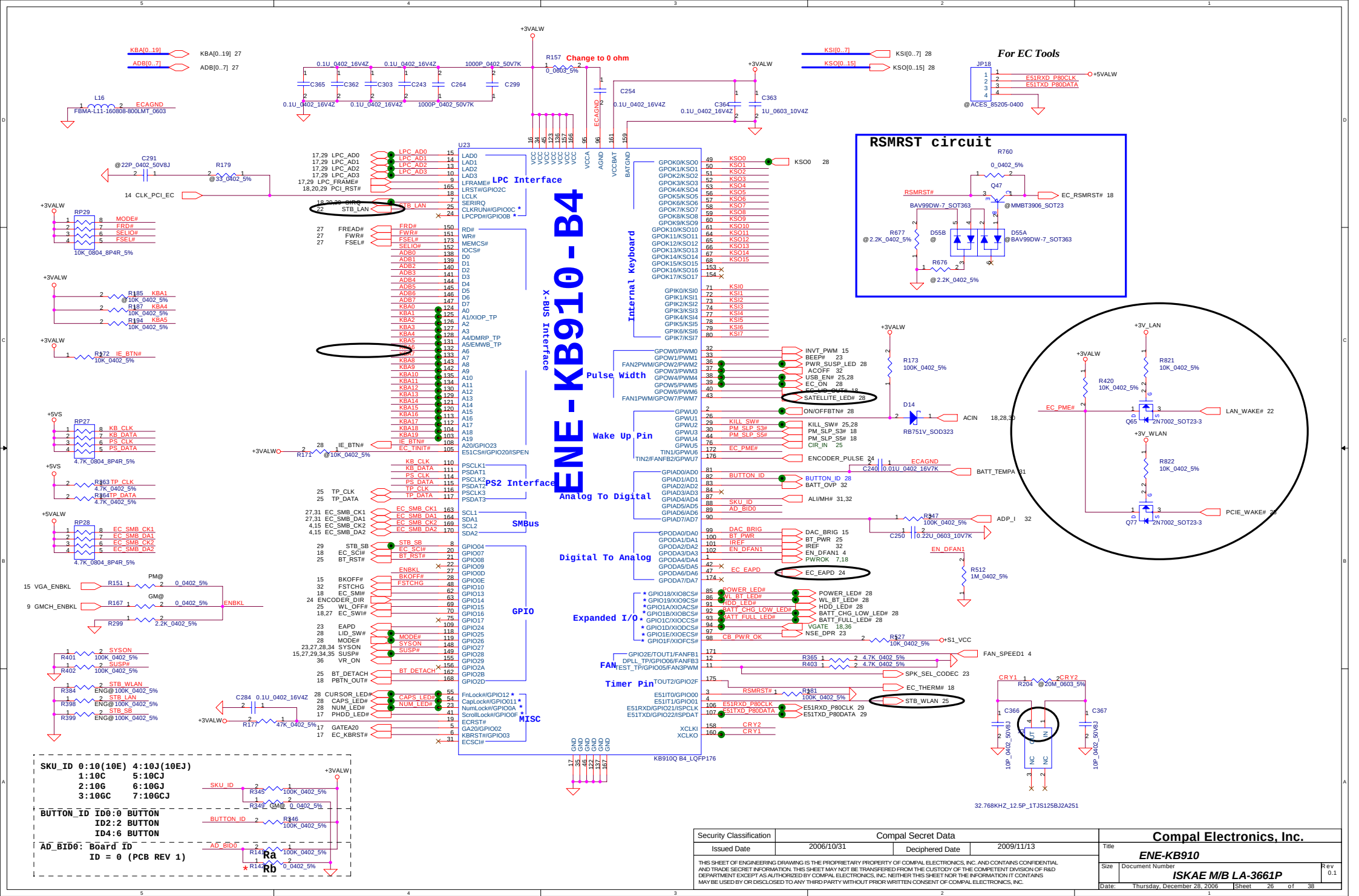
+AVDD AC97 +3VS DVDD



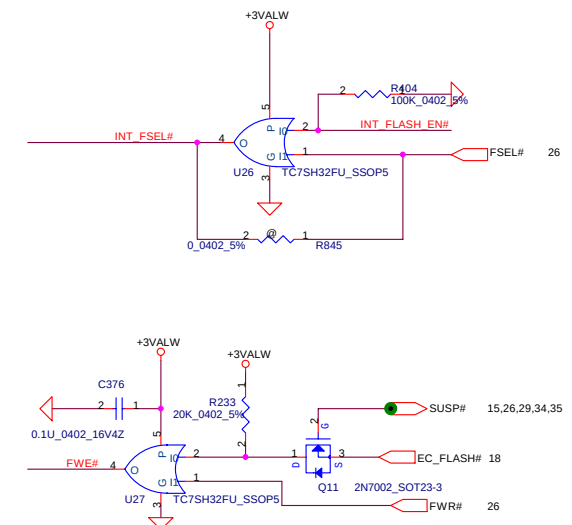
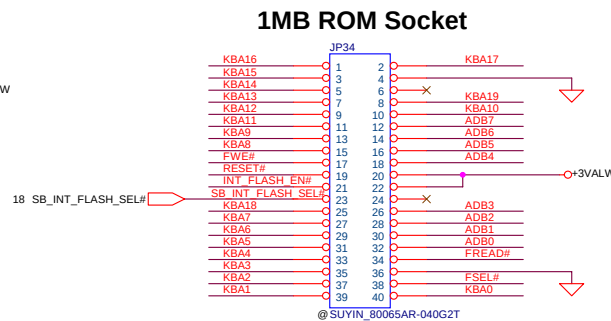
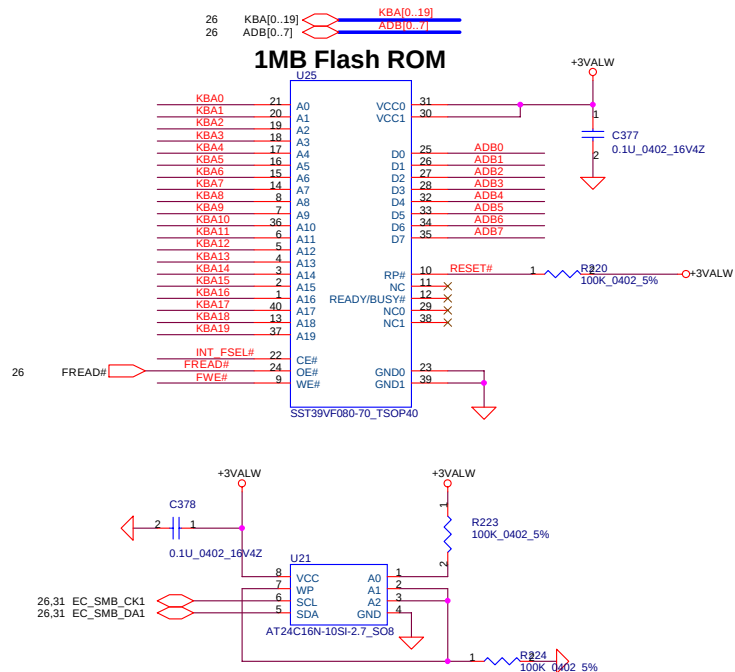
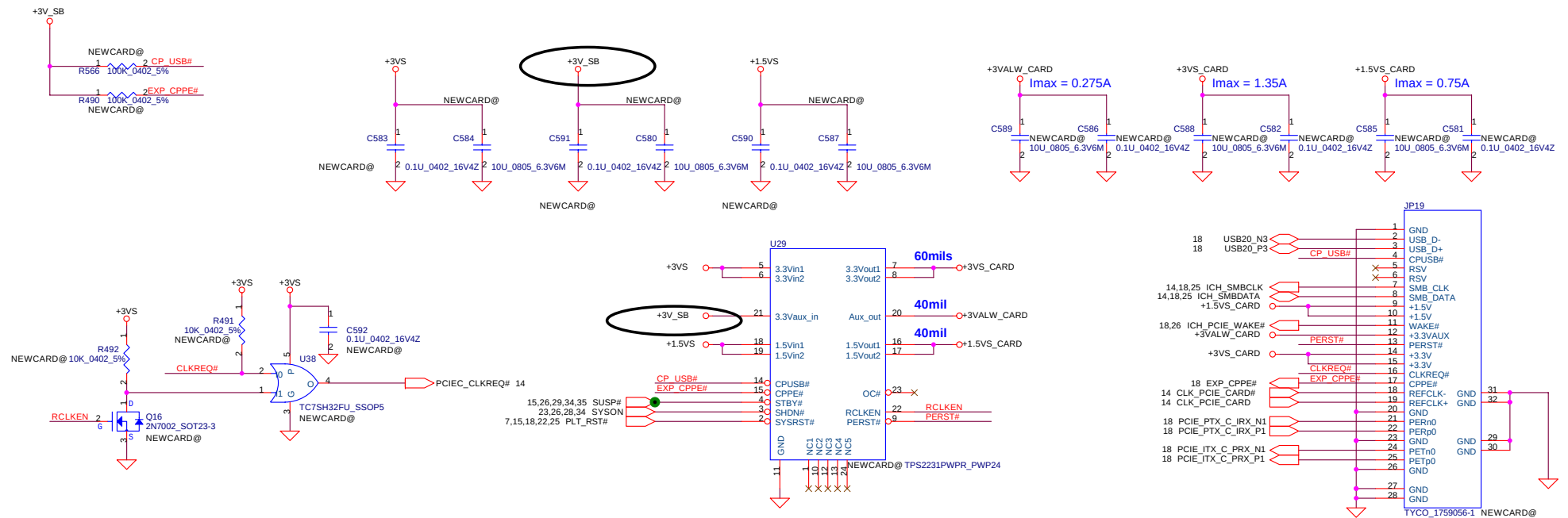
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								Date:		Thursday, December 28, 2006	



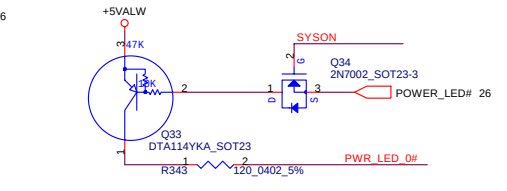
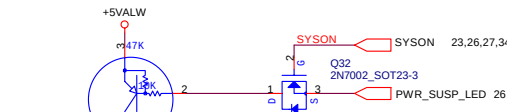
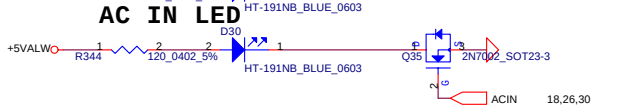
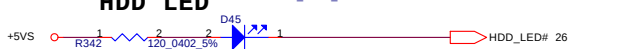
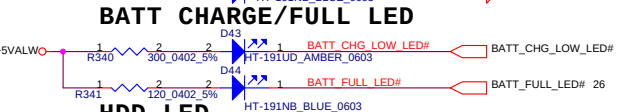
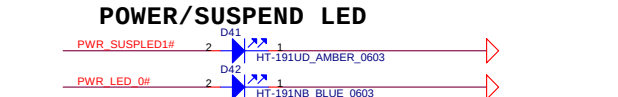
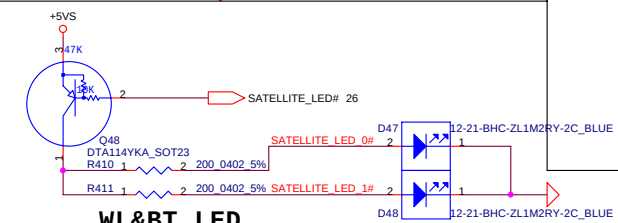
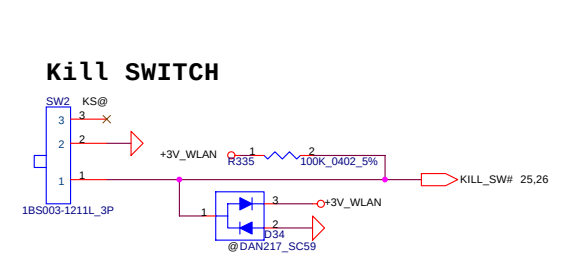
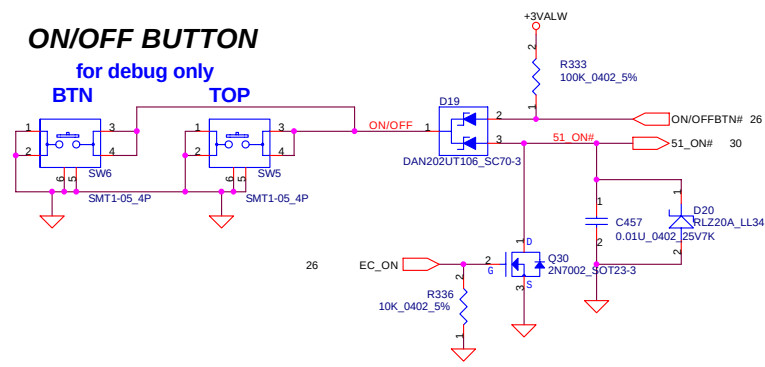
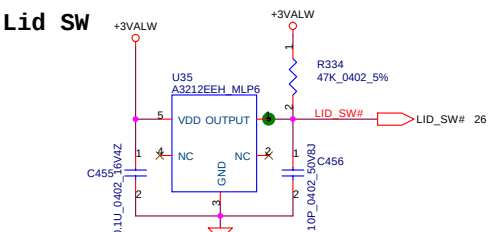
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				Size	Document Number
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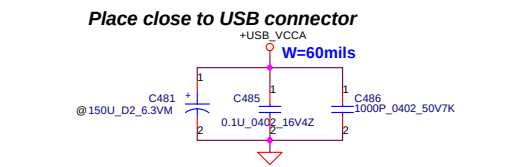
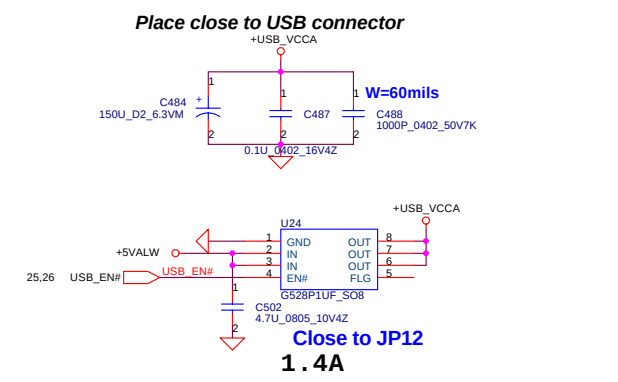
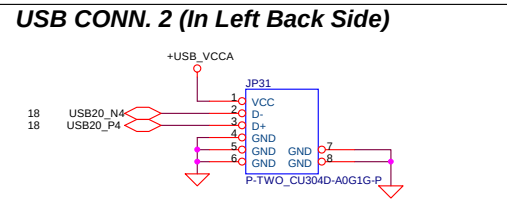
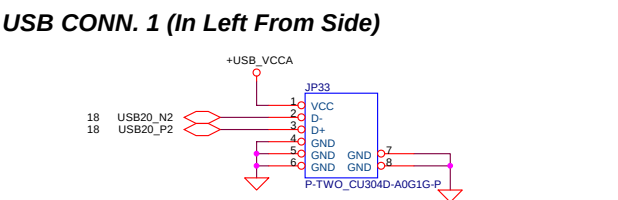
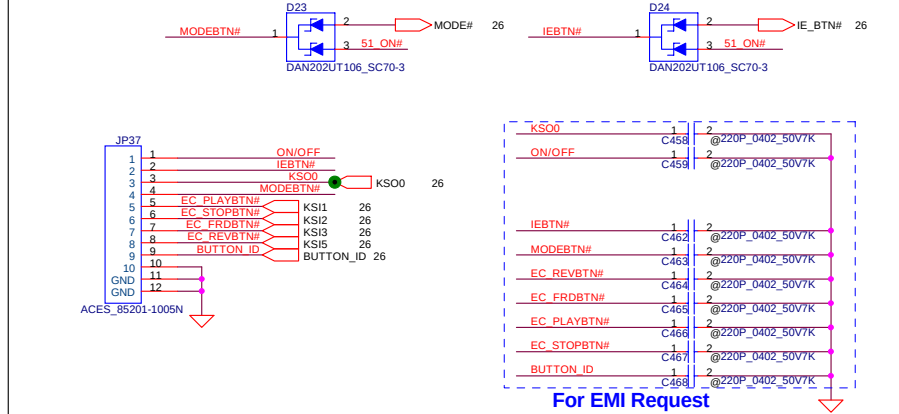
New Card



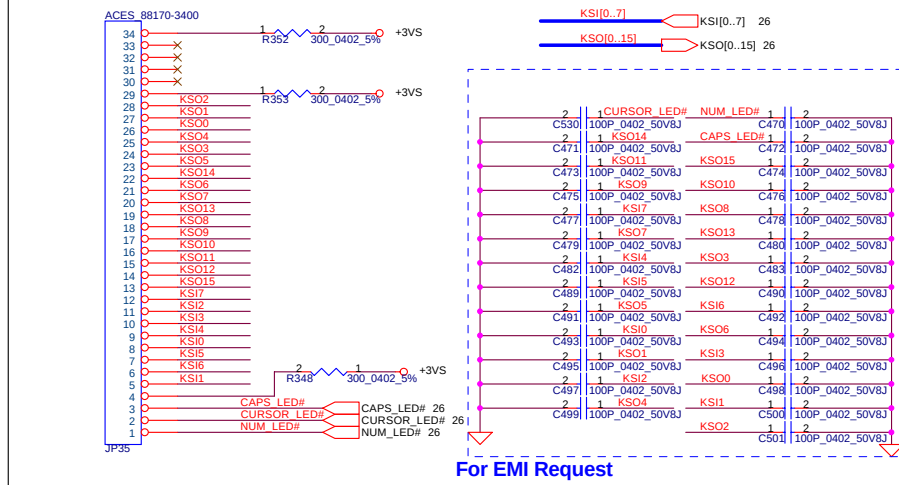
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Issued Date	2006/11/05	Deciphered Date	2009/11/05	Title BIOS/TP-PAD/BT		
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SW/LED Connector

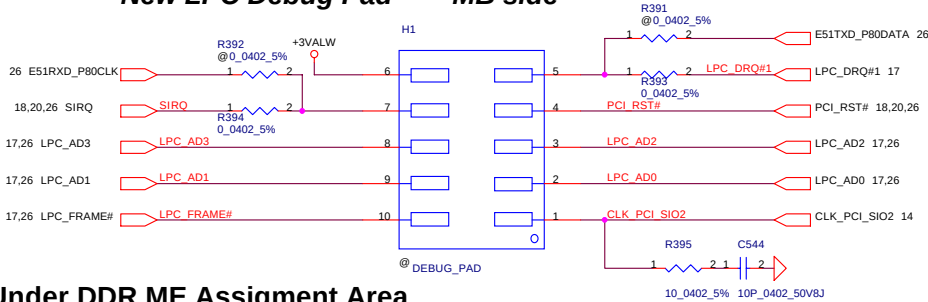


KEYBOARD CONN.



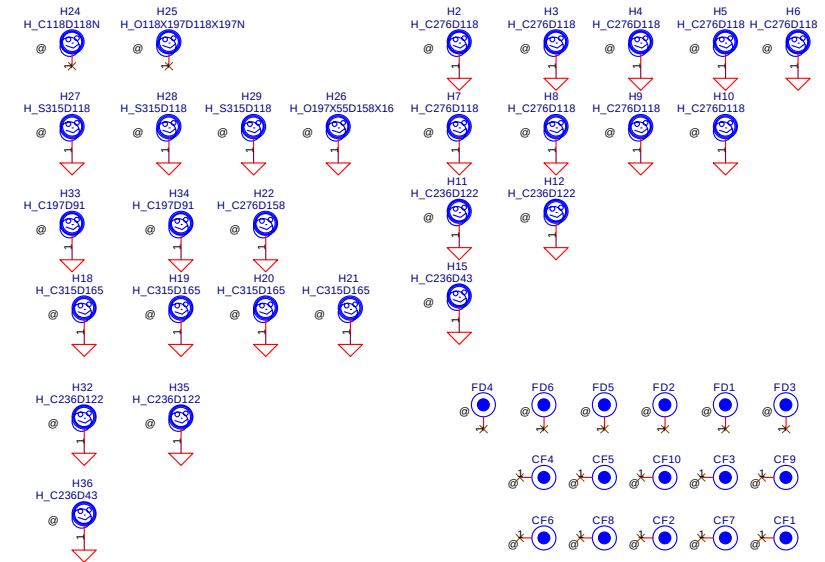
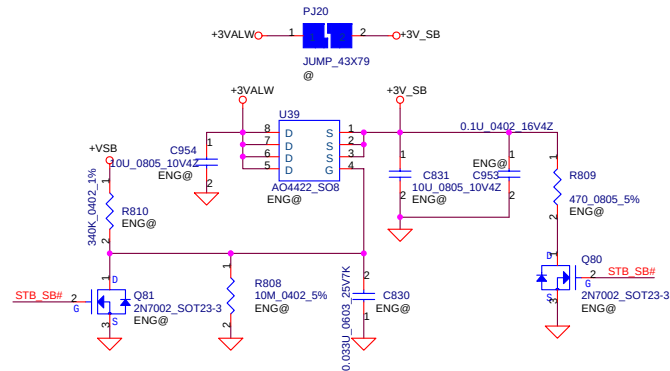
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				Size	Document Number
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New LPC Debug Pad ---- MB side

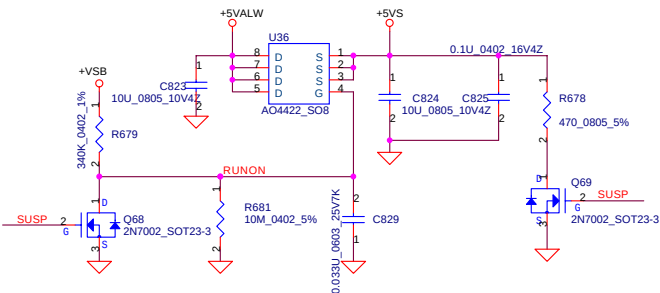


Under DDR ME Assignment Area

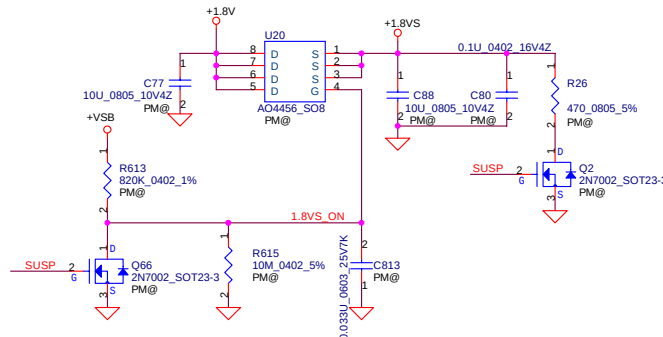
Keep Resistor near Debug Pad and in the same side
Reverse side DIMM ---- Pin 1 keep away DIMM



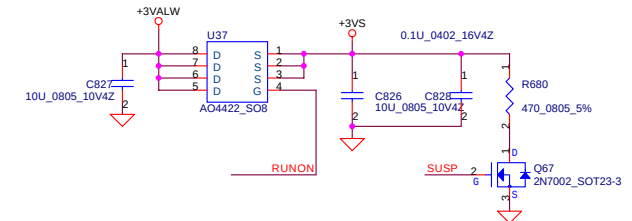
+5VALW to +5VS Transfer



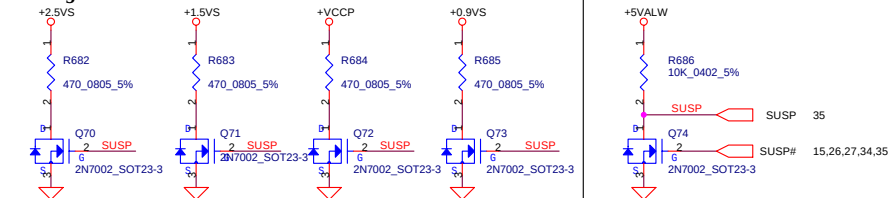
+1.8V to +1.8VS Transfer (Place close to VGA-Connector)



+3VALW to +3VS Transfer

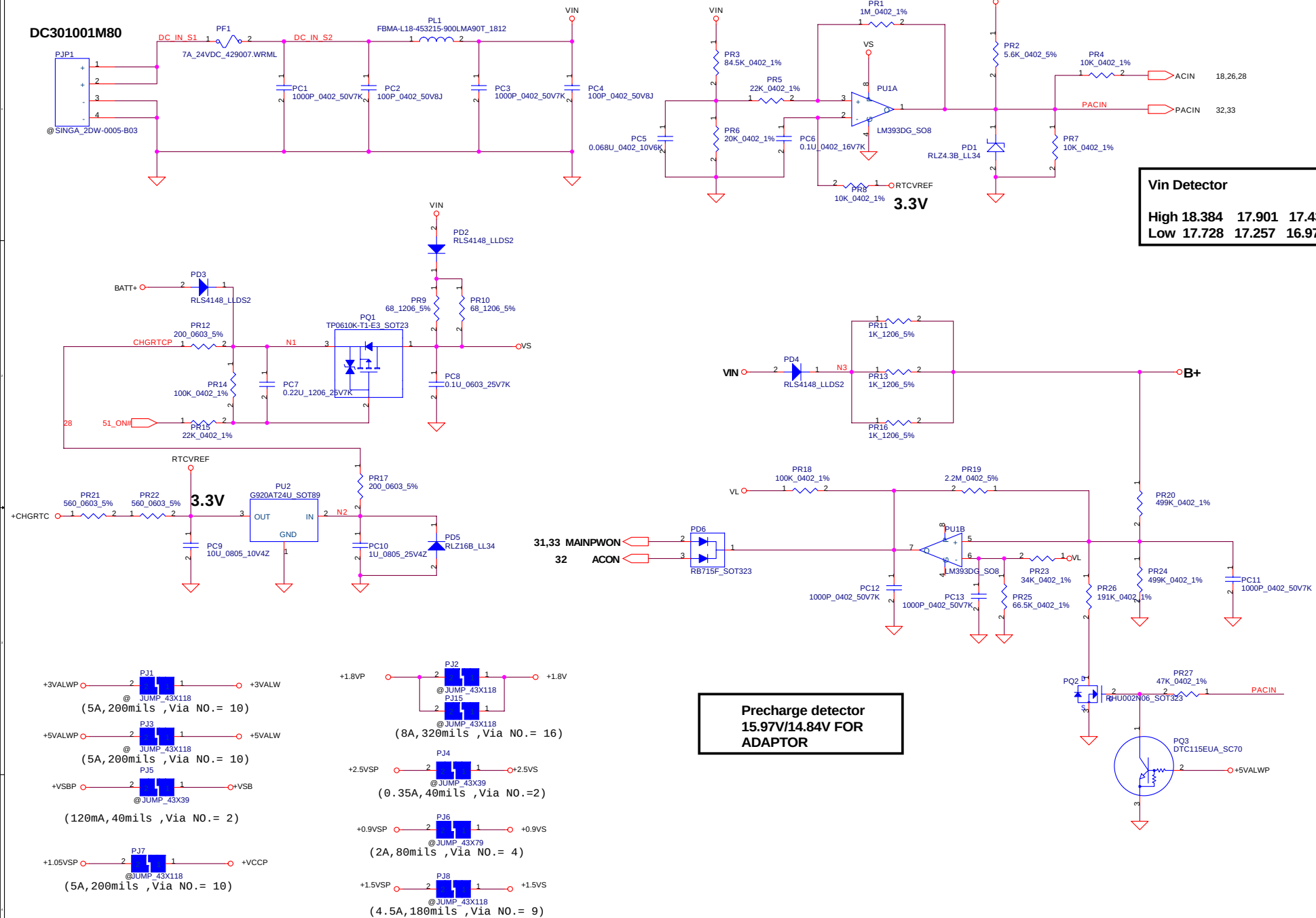


Discharge Circuit



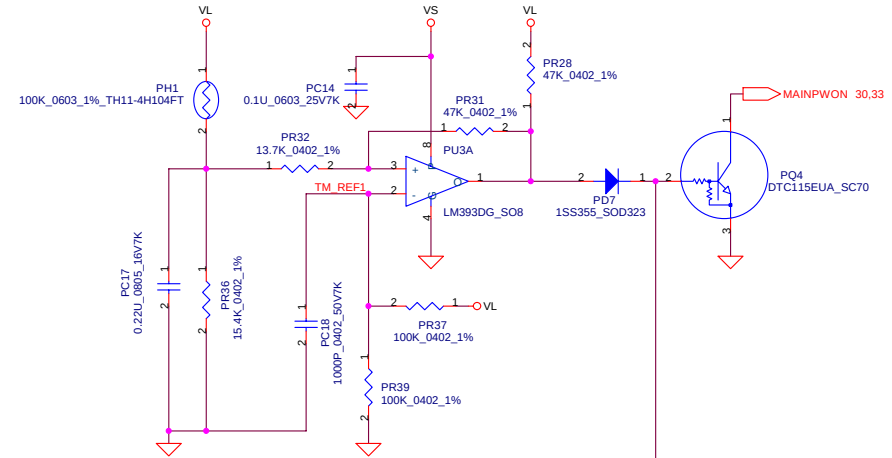
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Issued Date	2006/10/31	Deciphered Date	2009/11/13	DC/DC I/F Debug I/F Screw	
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DC301001M80

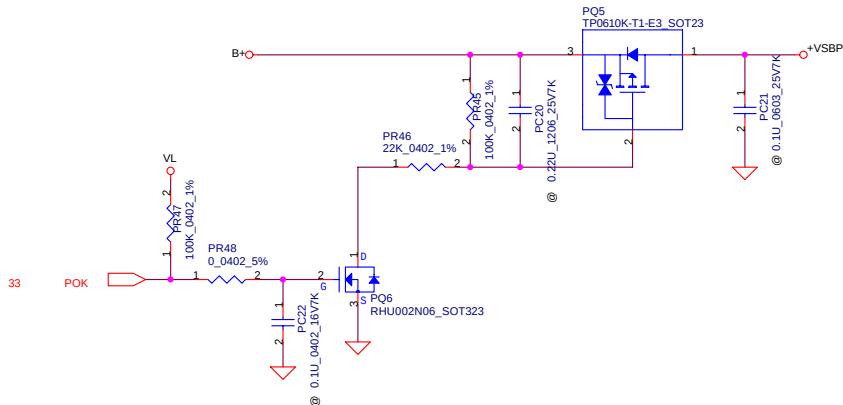
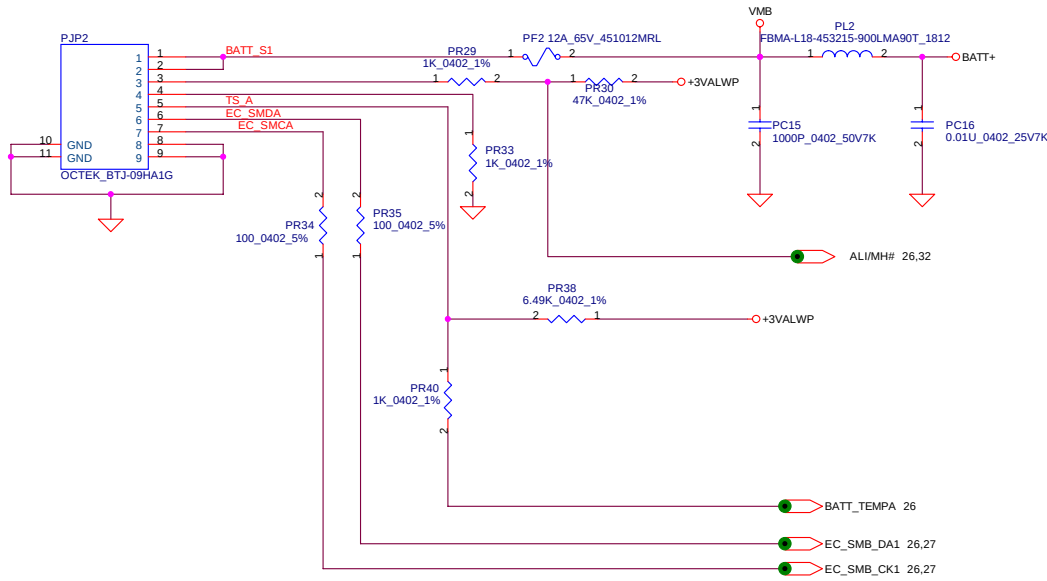
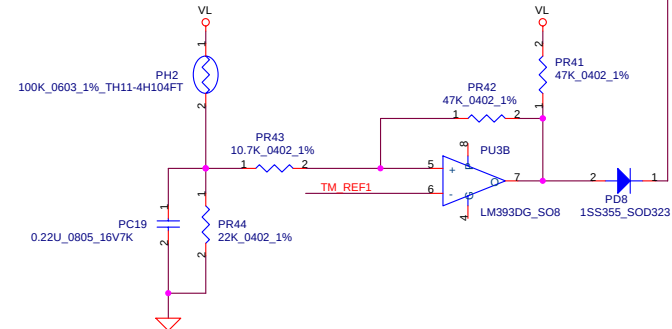


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				Size	Document Number	Rev 0.0
				Date:	Tuesday, December 26, 2006	Sheet 30 of 38

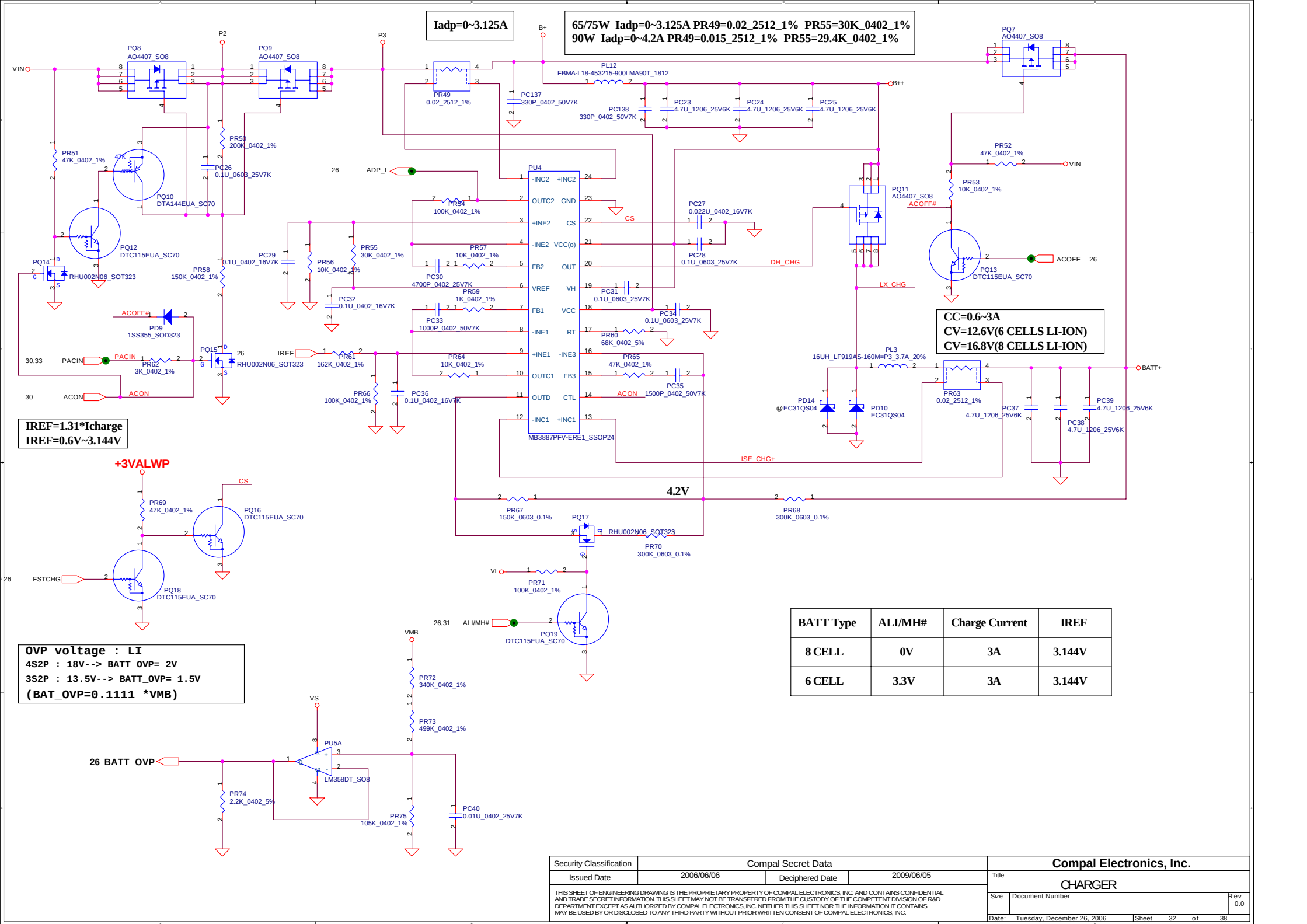
PH1 under CPU botten side :
CPU thermal protection at 87 degree C
Recovery at 48 degree C



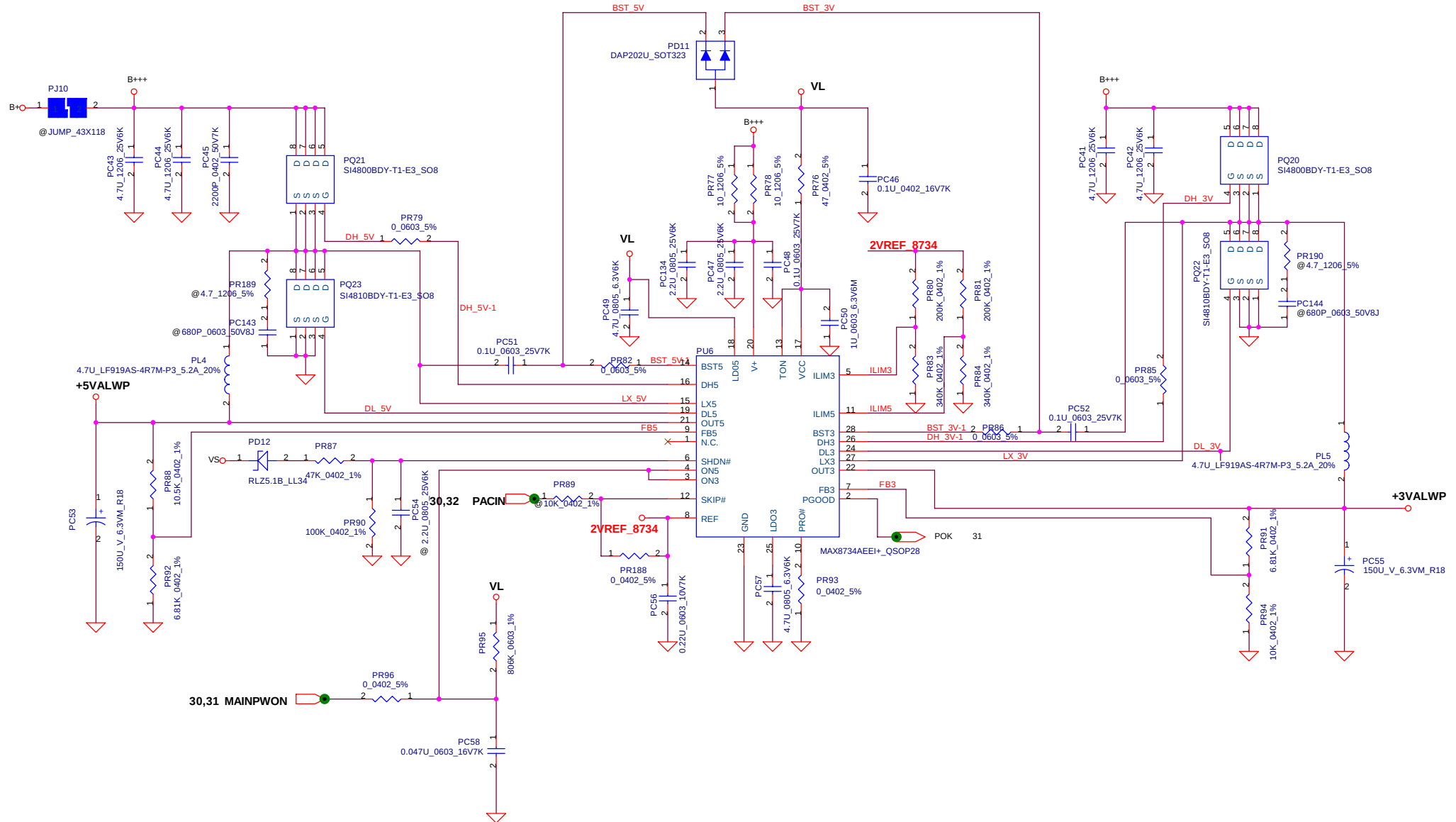
PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C



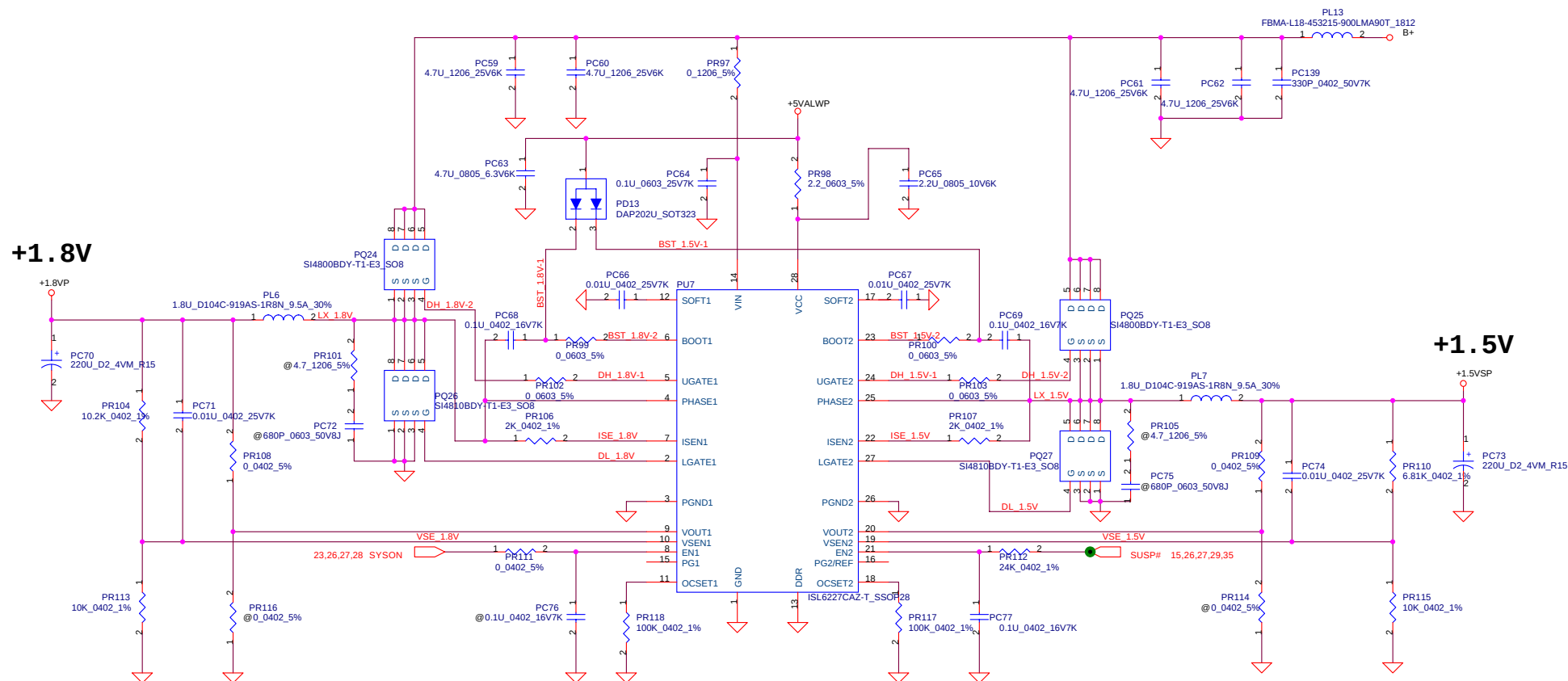
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+3.3VALWP/+5VALWP



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				Date:	Tuesday, December 26, 2006	Sheet	33 of 38



POWER PIR LIST

page Reason for change Modify list

DVT

35	Change +1.05V PWM IC	Change PU8 to ISL6269A(SA00000GU80), add PR122 (0ohm, SD013000080)
36	For EMI team request to add snubber and gate resistor Modify the CUP CORE load line and compensation	Add snuber PR155,PR165(6.8ohm_SD011680880), PC109,PC118(680p_SE024681J80) and gate resistor PR154,PR162(1ohm_SD013100B80) Change PC103 to 0.022u(SE076223K80), PC104 to 2.2u(SE107225K80), PR185 to 4.42K(SD000004J80), PC129 to 0.1u(SE076104K80, add PC126 (0.018U_SE025183J80), delete PC105 and PC106

31	Modify the CPU OTP point from 84 degC to 87 degC for thermal team request	Change PR36 from 22K to 20K(SD034200280)
----	--	--

PVT

32,34, 35,36	For EMI team request to add bead to reduce board band	Add PL12,PL13,PL14(SM010020720);PC137,PC138,PC139(330p_SE074331K80);PC140(680p_SE074681K80);PC141(3300p_SE074332K80)
33	Reduce the power consumption on S3/S4	Add PR188(0_0402_5%) and unpop PR89
36	Solve the high frequency noise.	Change PC99 from 100U to 220U(SF22004M210)

Pre-MP

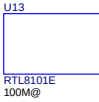
36	For EMI solution	Add PC142 (0.01u_0402)
36	PC99 was interfere with logic low so change to small size	Change PC99 from 220U to 100U and add PC143,PC144(68U_25V).

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		Size Custom	Document Number	0.1		
Date:		Tuesday, December 26, 2006		Sheet	37	of 38

PIR (Product Improve Record)

FOR ISPD

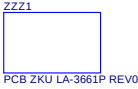
LAN



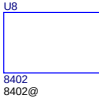
TRANSFORMER



PCB



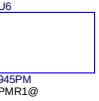
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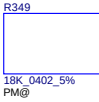
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NB



SKU ID



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