

Compal Confidential

Model Name : P7YE0/P7YH0/P7YS0

File Name : LA-6911P

BOM P/N:43

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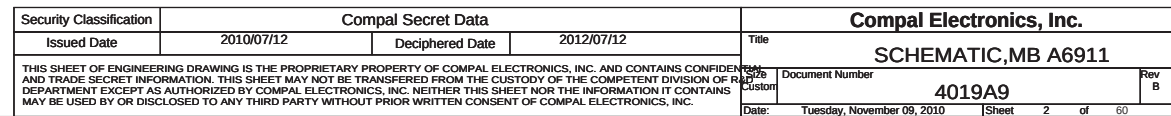
P7YE0/P7YH0/P7YS0 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
ATI Seymour/Whistler/Granville

2010-11-01

REV: 0.3

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	ON	OFF
+1.5VSDGPU	+1.5V to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resistor)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address	VRAM P/N
ChannelA DIMM0 A0	1010 000X	JDIMM1
DIMM1 A2	1010 001X	JDIMM3
ChannelB DIMM0 A4	1010 010X	JDIMM2
DIMM1 A6	1010 011X	JDIMM4

SAM 64*16 900M	SA00004GS10(S IC D3 64M16 K4W1G1646G-BC11 FBGA ABOI)
SAM 64*16 800M	SA000035720(S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABOI)
SAM 128*16 800M	SA00003M060(S IC D3 128M16 K4W2G1646C-HC12 FBGA ABOI)
HYN 64*16 900M	SA000041S10(S IC D3 64MX16 H5TQ1G630FR-11C FBGA ABOI)
HYN 64*16 800M	SA000032420(S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABOI)
HYN 128*16 800M	SA00003VS10(S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABOI)
HYN 64*16 800M	SA0000324G0(S IC D3 64M16 H5TQ1G63DFR-12C FBGA ABOI)

BT Config	GPU config	BACO config
BT SKU: BT@	Whistler: WHIS@	BACO: BACO@
4DIMM config	Seymour: SEYM@	nonBACO: NOBACO@
4 DIMM: 4DIMM@	Granville: GRAN@	Muxless config
LVDS/eDP config	Granville config	Muxless: MUXL@
UMA LVDS: ULVDS@	Granville: GRAN@ (VDDCI)	nonMuxless: NOMUXL@ (DISO,UMAO)
DIS LVDS: DLVDS@	nonGranville: NOGRAN@ (VGA_CORE)	
DIS eDP: DEDP@	GPU Frame config	
	128bit: 128@ (WHIS,GRAN)	
		VRAM BOM Config
		X76264BOL01: 64Mx16x4 Seymour 512M HYN NEW
		X76264BOL02: 64Mx16x4 Seymour 512M HYN OLD
		X76264BOL03: 64Mx16x8 Whistler/Granville 1G HYN NEW
		X76264BOL04: 64Mx16x8 Whistler/Granville 1G HYN OLD
		X76264BOL05: 128Mx16x8 Whistler/Granville 2G HYN
		X76264BOL06: 128Mx16x8 Whistler/Granville 2G SAM
		X76264BOL07: 128Mx16x4 Seymour 1G SAM
		X76264BOL08: 128Mx16x4 Seymour 1G HYN

BOM Config		
* UMA Only LVDS Panel:	BT@/UMAO@/UMA@/ULVDS@/NOMUXL@	+DIMM,USB option
* DIS Only LVDS Panel:	BT@/DIS@/VGA@/DISO@/DLVDS@/NOMUXL@	+X76+GPU +DIMM,USB option
* DIS Only EDP Panel:	BT@/DIS@/VGA@/DISO@/DEDP@/NOMUXL@	+X76+GPU +DIMM,USB option
* Muxless BACO LVDS Panel:	BT@/UMA@/DIS@/VGA@/ULVDS@/BACO@/MUXL@	+X76+GPU(S,W) +DIMM,USB option
* Muxless nonBACO LVDS Panel:	BT@/UMA@/DIS@/VGA@/ULVDS@/NOBACO@/MUXL@	+X76+GPU(G) +DIMM,USB option

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board Id	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

USB Port Table

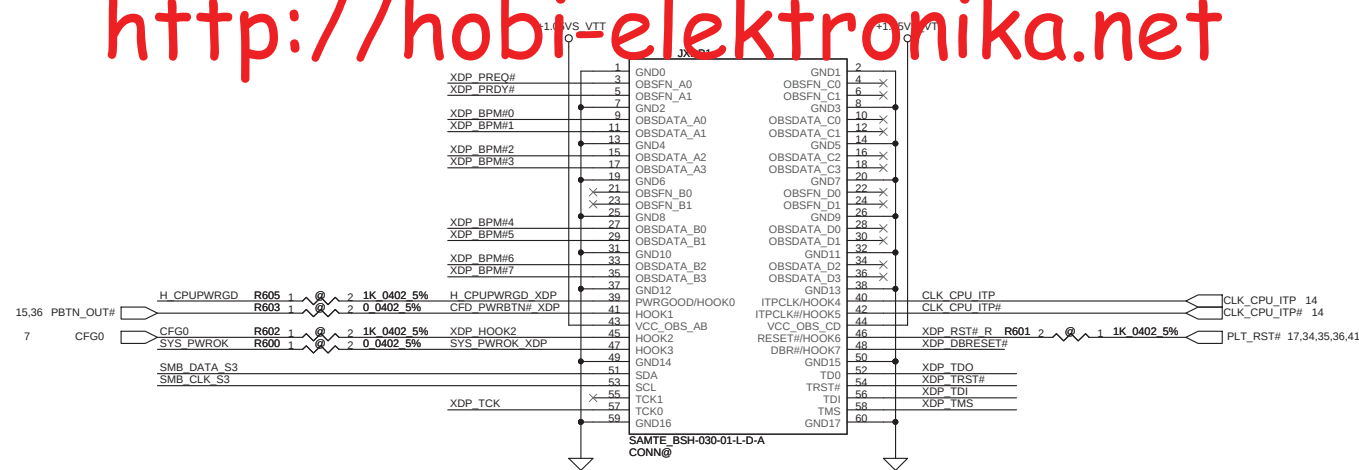
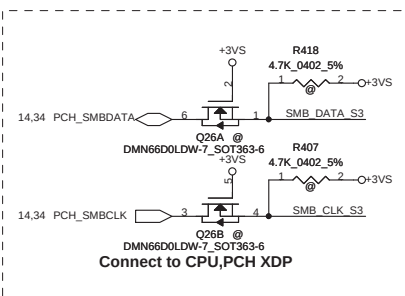
USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B(Right side 2.0 option)
		1	USB/B(Right side 2.0 option)
		2	USB port(left side 2.0)
	UHCI1	3	USB/B(Right side 3.0 option)
		4	
		5	
	UHCI2	6	
		7	
		8	Mini Card(WLAN)
	UHCI4	9	Mini Card
		10	Camera
		11	Card Reader
EHCI2	UHCI5	12	
		13	Blue Tooth

BTO Option Table

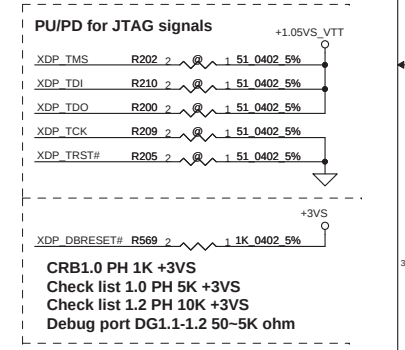
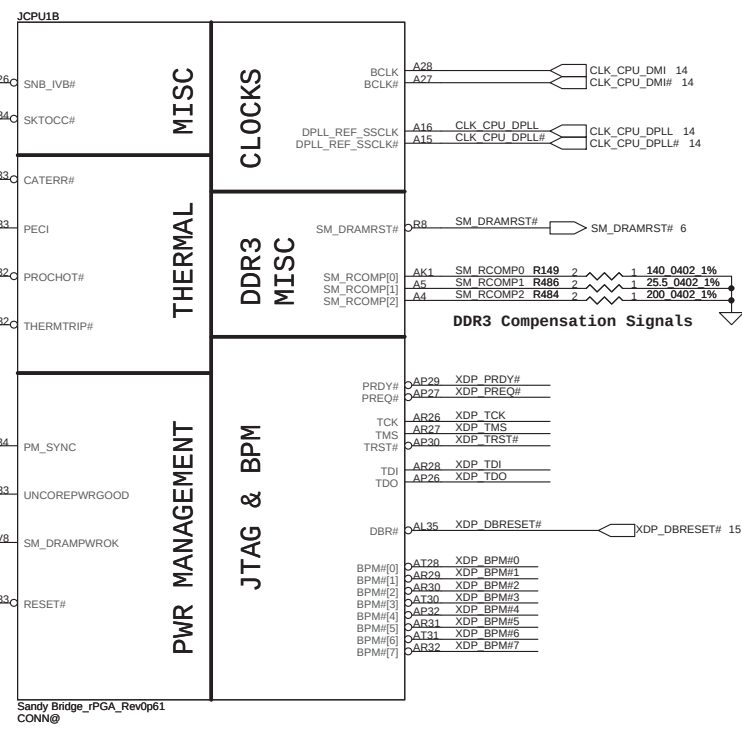
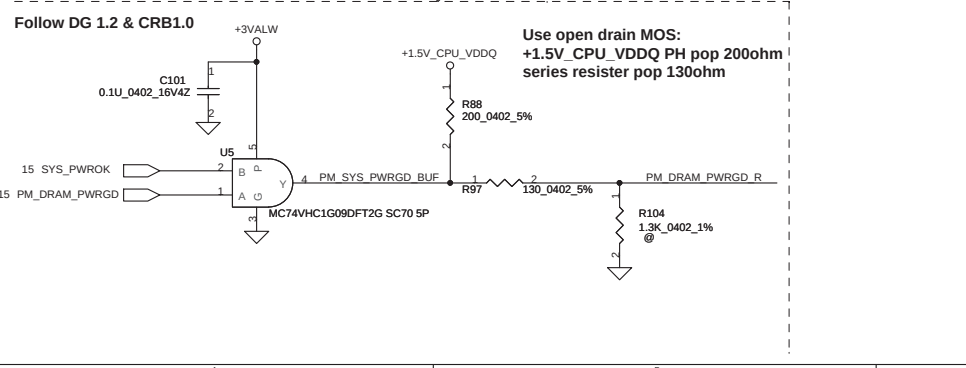
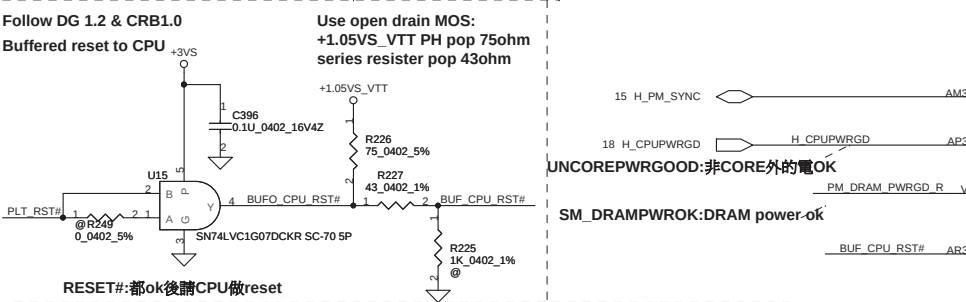
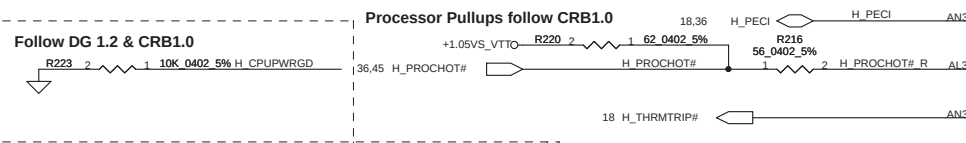
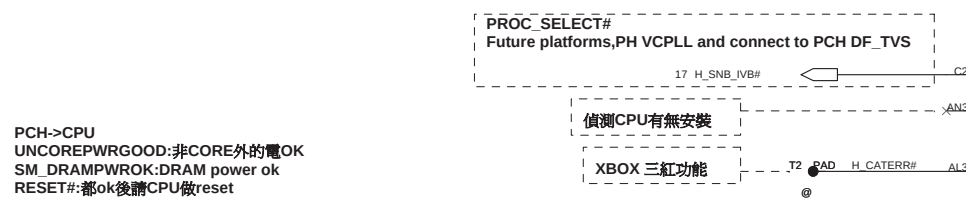
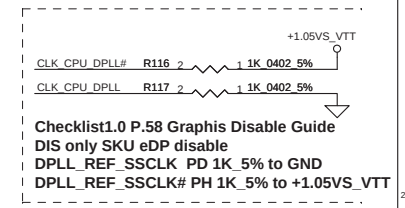
BTO Item	BOM Structure
UMA Only	UMAO@
Muxless/UMA	UMA@
DIS Only	DISO@
Muxless/DIS	DISO@
Muxless/DIS	VGA@
BACO mode	BACO@
nonBACO mode	NOBACO@
VRAM	X76@
128bit VRAM	128@
Granville GPU	GRAN@
Whistler GPU	WHIS@
Seymour GPU	SEYM@
non Granville GPU	NOGRAN@
Blue Tooth	BT@
Connector	CONN@
Unpop	@
DIS eDP	DEDP@
UMA LVDS	ULVDS@
DIS LVDS	DLVDS@
Muxless	MUXL@
non Muxless	NOMUXL@
USB2.0 Conn	USB2@
USB3.0 Conn	USB3@
4 Dimm	4DIMM@

P9, P19, P23, P30-32, P59
P4, P14
P.22-28
P.26 , P.29
P.27, 28
P.27
P.23, P.59
P.59
P.22-26
P.23, P.25
P.35
P.30, 59
P.30
P.18, P.32
P.41
P.41
P.11-12

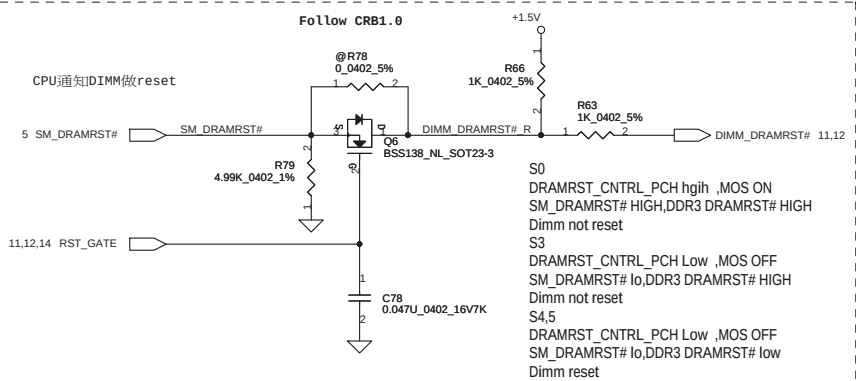
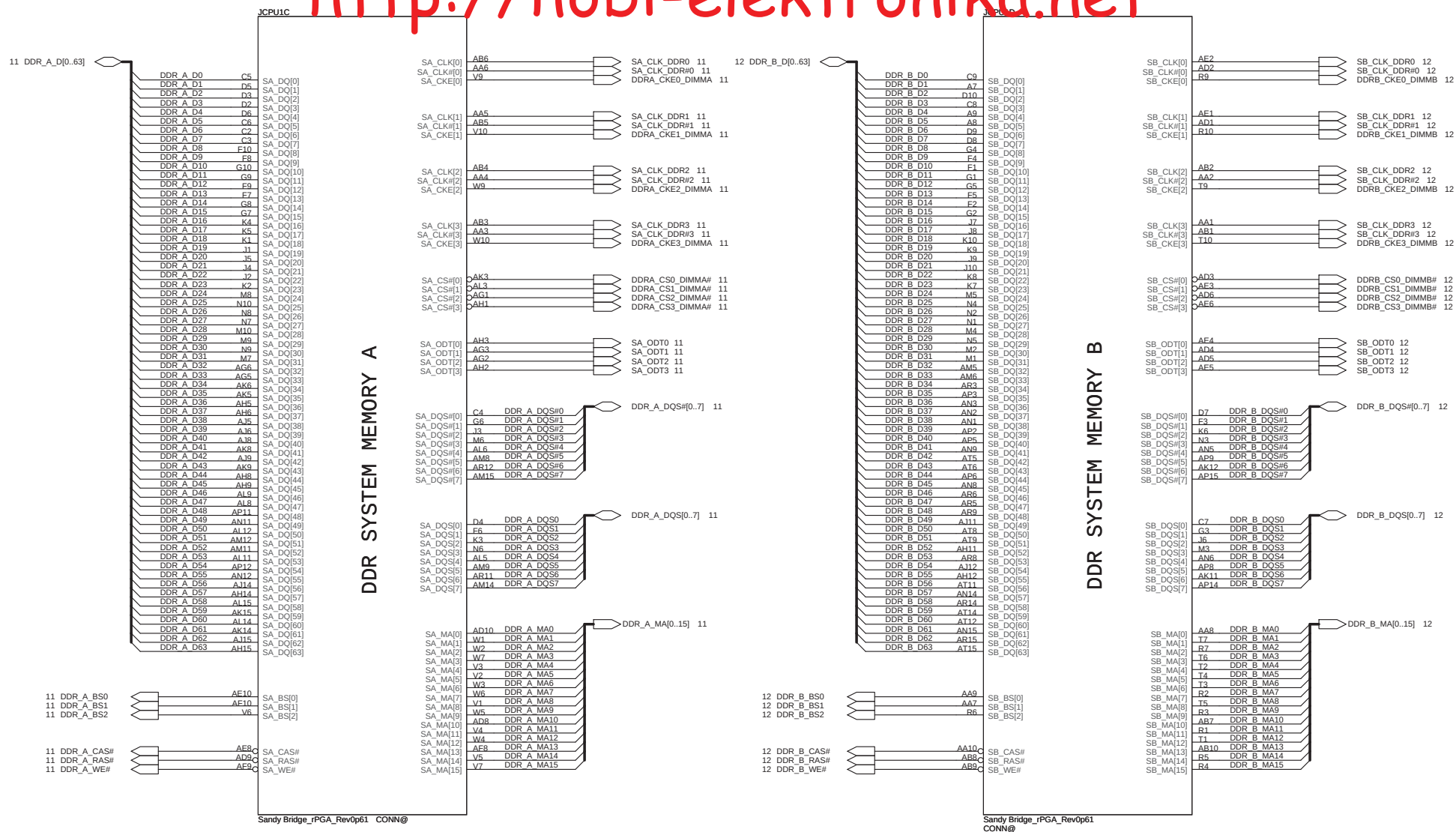
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Debug port DG 0.65–
Note: 1. These signals are optional, can be left as OPEN/No-Connect if debug by Intel will not be needed

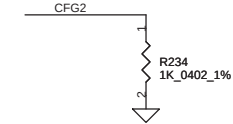


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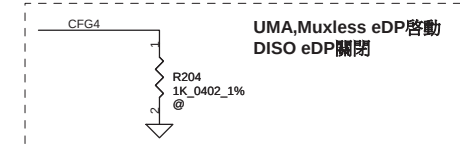


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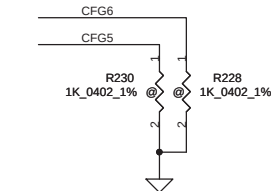
CFG Straps for Processor



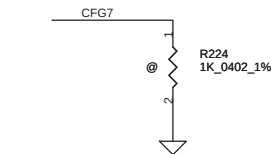
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed



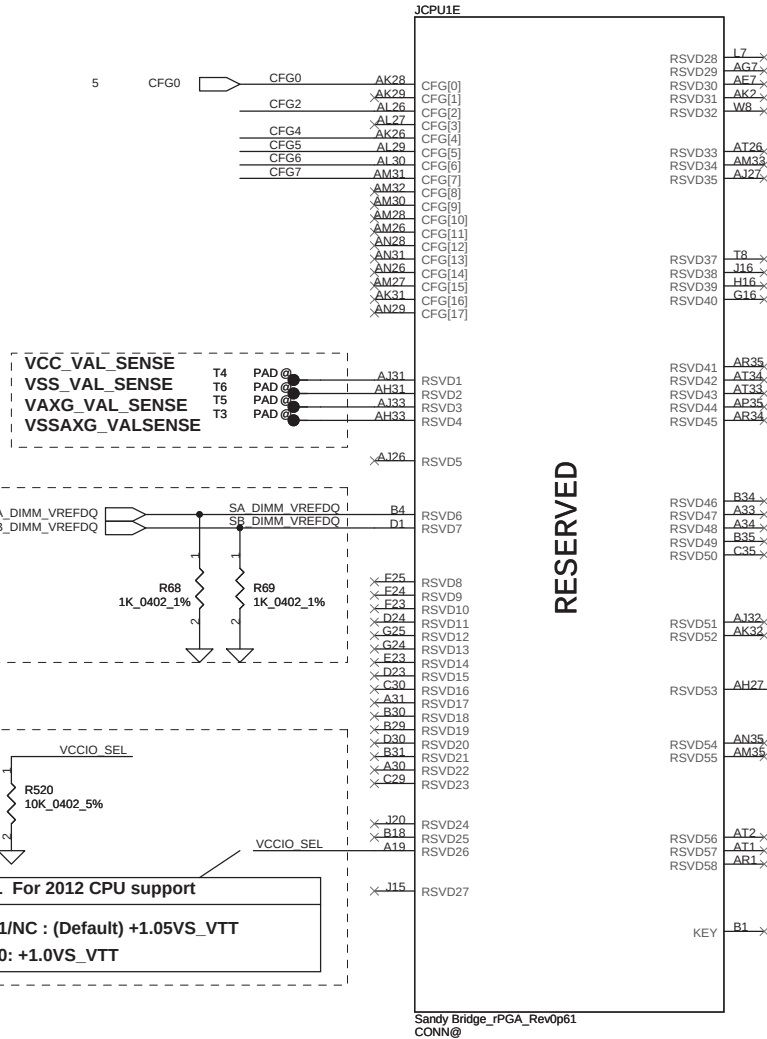
eDP enable	
CFG4	★ 1: Disable 0: Enable



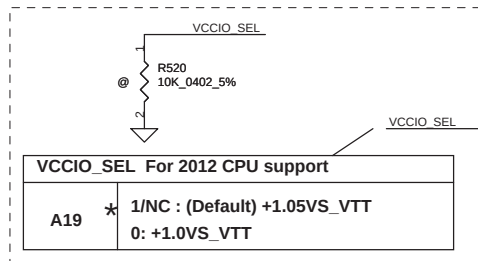
PCIe Port Bifurcation Straps	
CFG[6:5]	★11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express



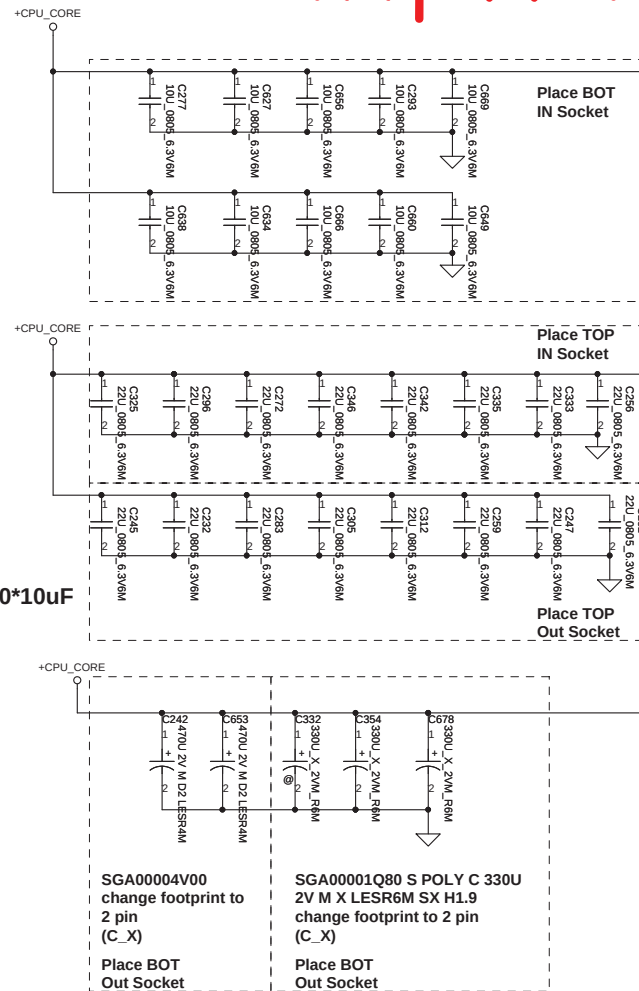
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
For Future CPU M3 support,
Sandy bridge not support M3,
Check list1.0&CRB say can NC



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QC 94A
DC 53A

AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AG25 VCC11
AG24 VCC12
AG23 VCC13
AG22 VCC14
AG21 VCC15
AG20 VCC16
AG19 VCC17
AG18 VCC18
AG17 VCC19
AG16 VCC20
AG15 VCC21
AG14 VCC22
AG13 VCC23
AG12 VCC24
AG11 VCC25
AG10 VCC26
AG09 VCC27
AG08 VCC28
AG07 VCC29
AG06 VCC30
AG05 VCC31
AG04 VCC32
AG03 VCC33
AG02 VCC34
AG01 VCC35
AG00 VCC36
AG00 VCC37
AG00 VCC38
AG00 VCC39
AG00 VCC40
AG00 VCC41
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AG00 VCC43
AG00 VCC44
AG00 VCC45
AG00 VCC46
AG00 VCC47
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AG00 VCC91
AG00 VCC92
AG00 VCC93
AG00 VCC94
AG00 VCC95
AG00 VCC96
AG00 VCC97
AG00 VCC98
AG00 VCC99
AG00 VCC100

CONN@

Sandy Bridge rPGA Rev0p61

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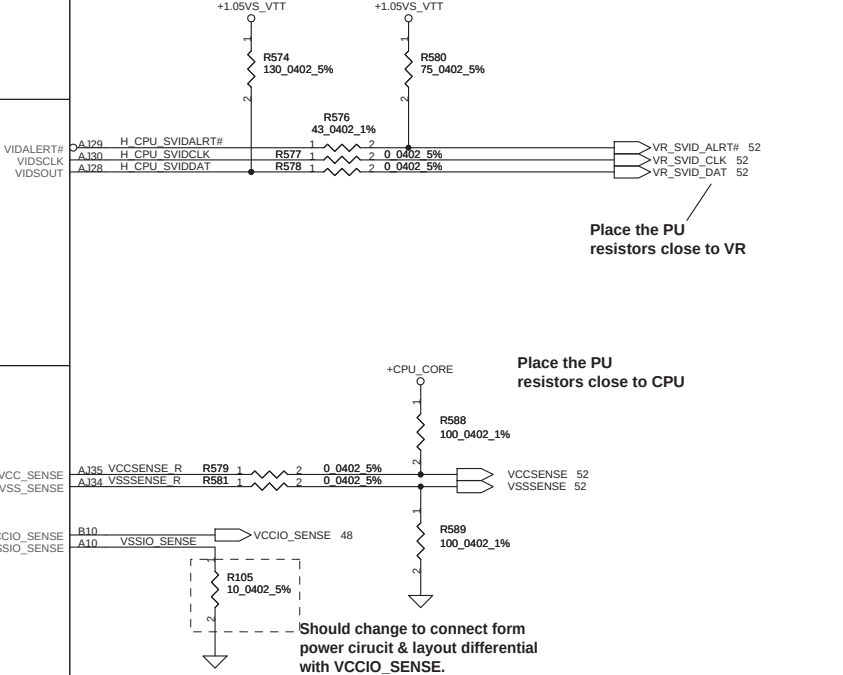
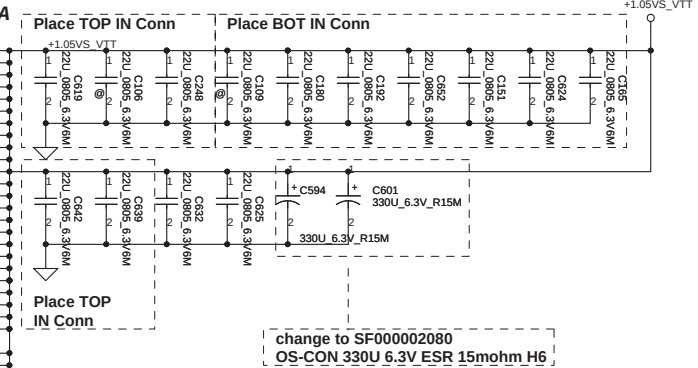
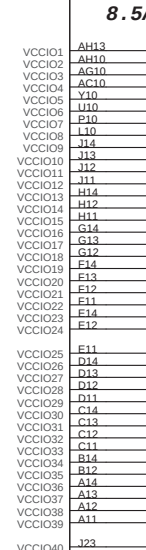
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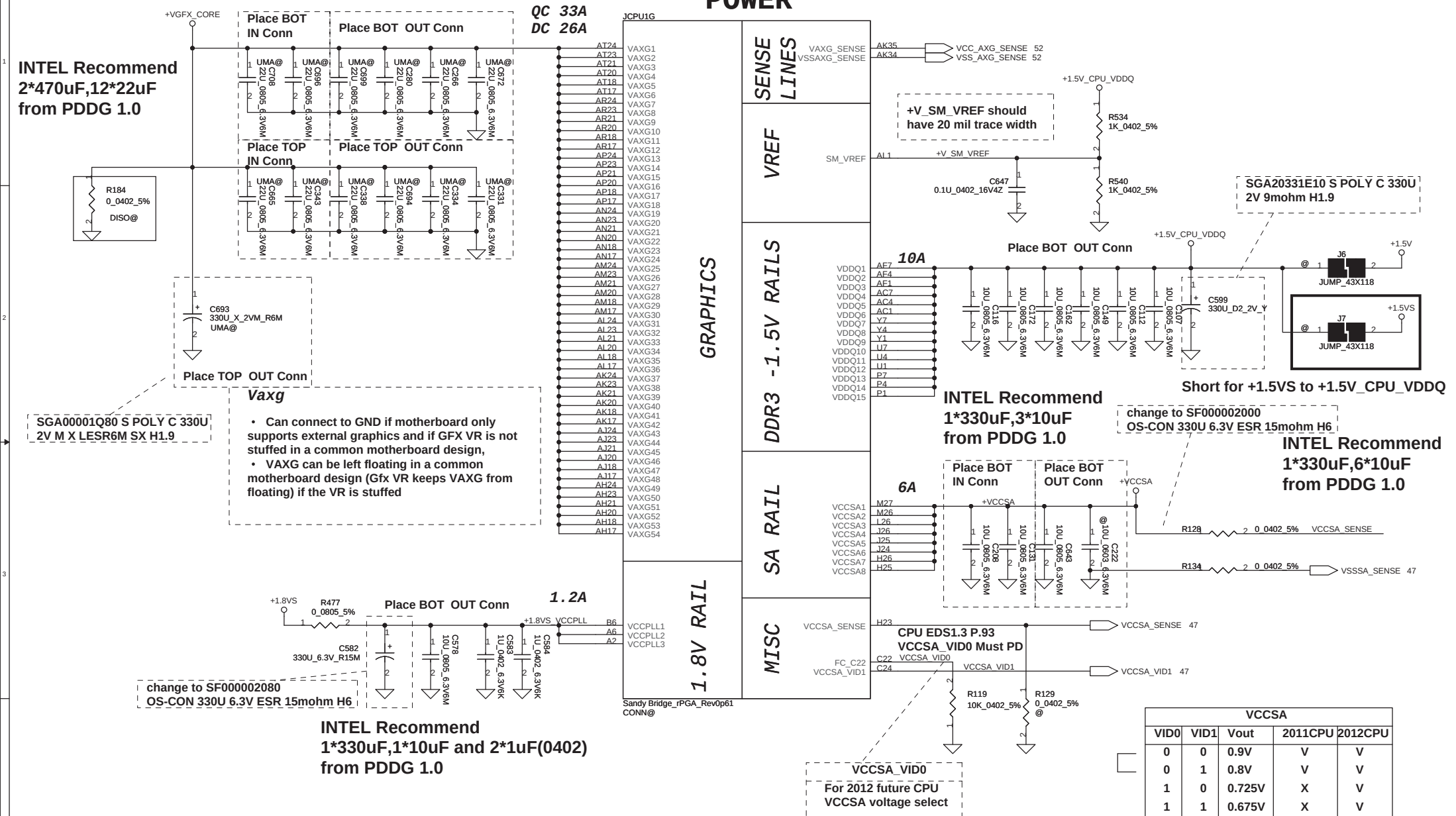
PEG AND DDR

SVID

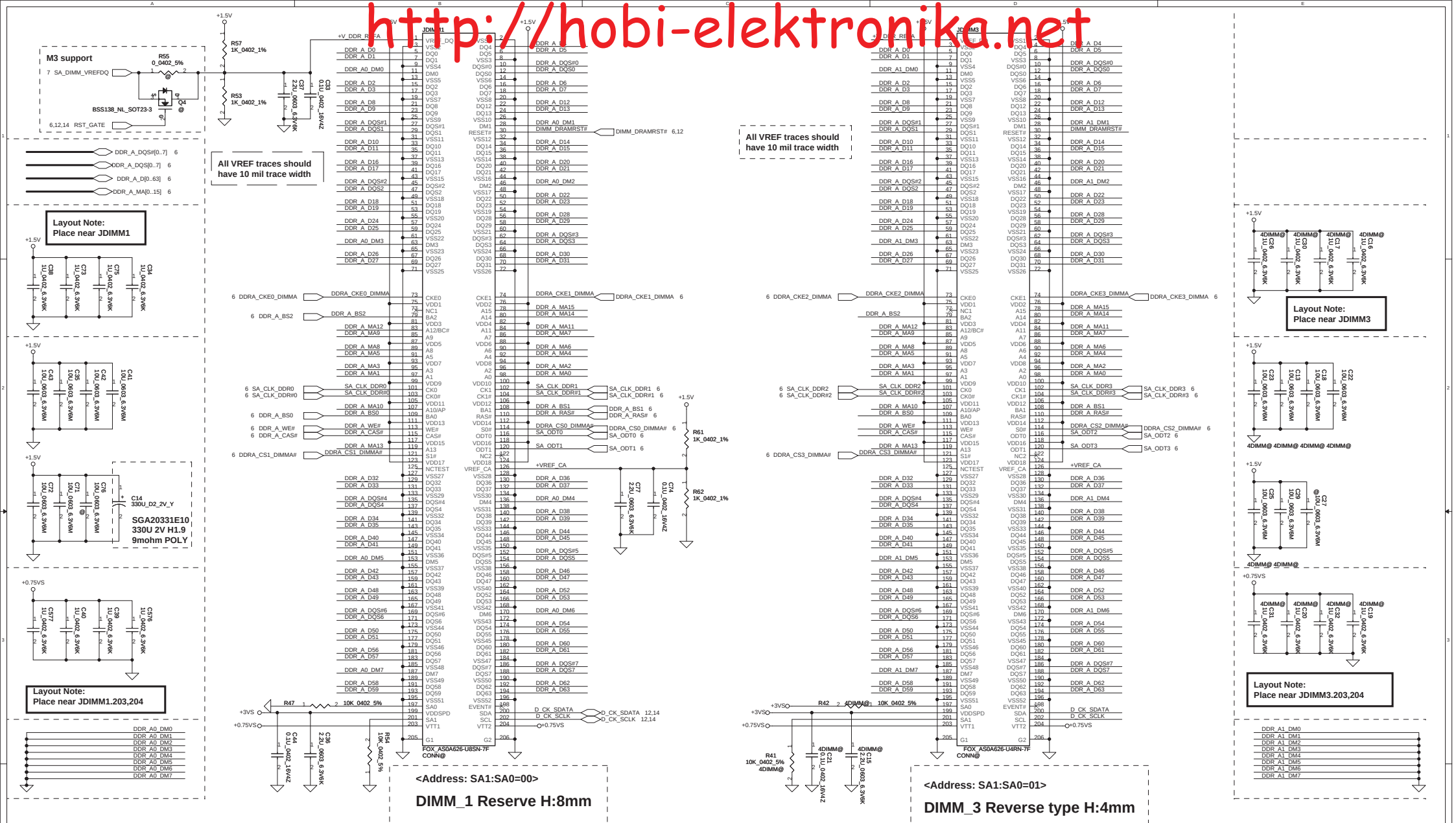
SENSE LINES



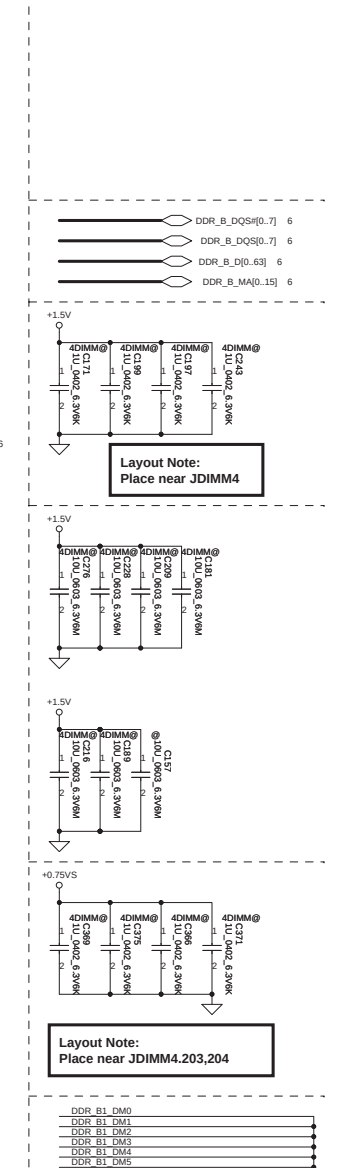
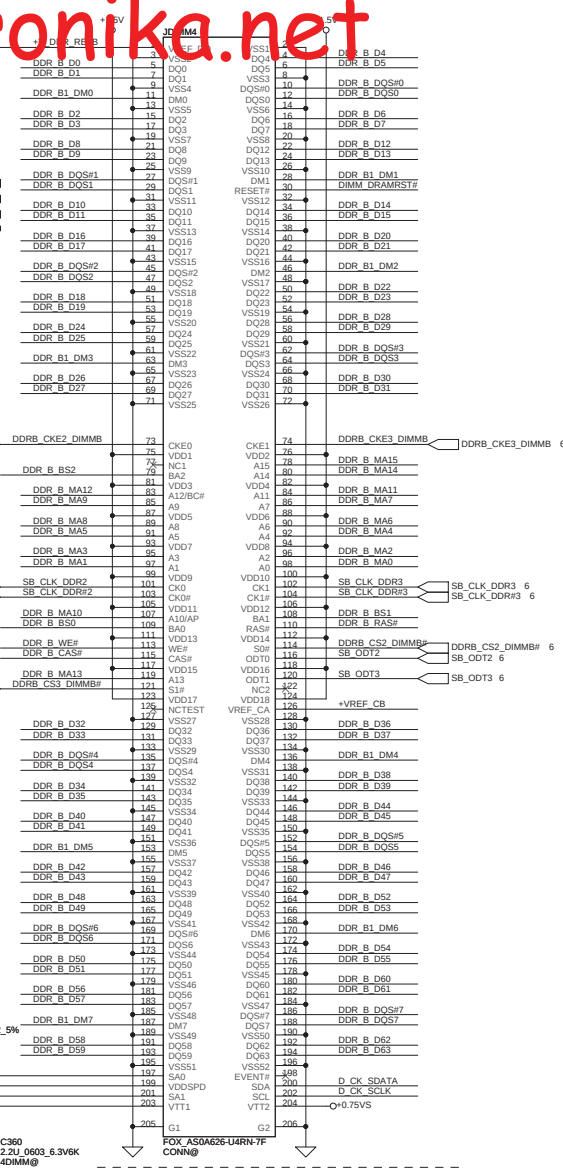
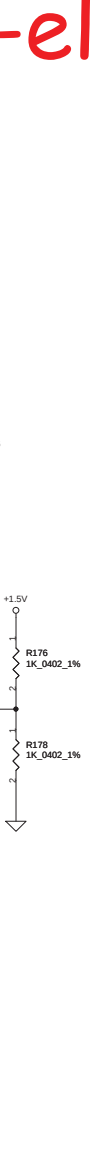
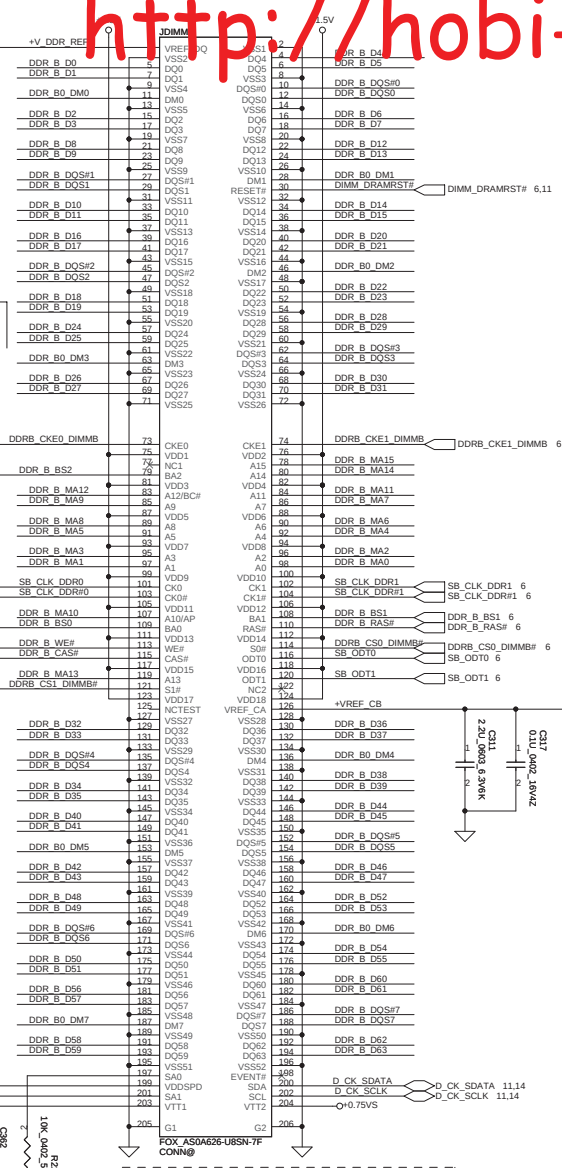
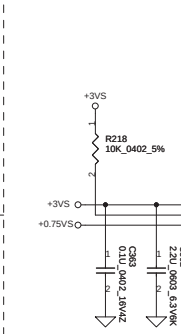
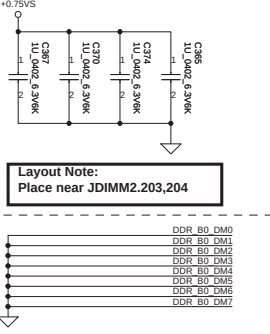
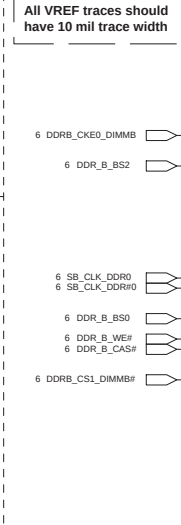
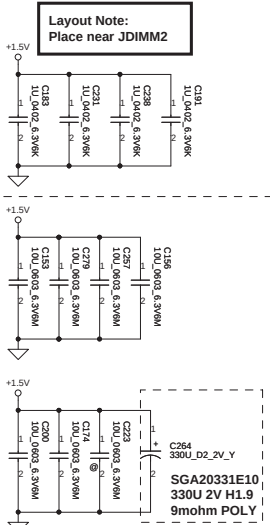
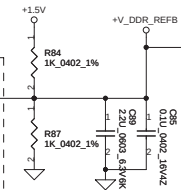
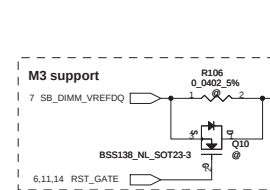
POWER



VCCSA				
VID0	VID1	Vout	2011CPU	2012CPU
0	0	0.9V	V	V
0	1	0.8V	V	V
1	0	0.725V	X	V
1	1	0.675V	X	V

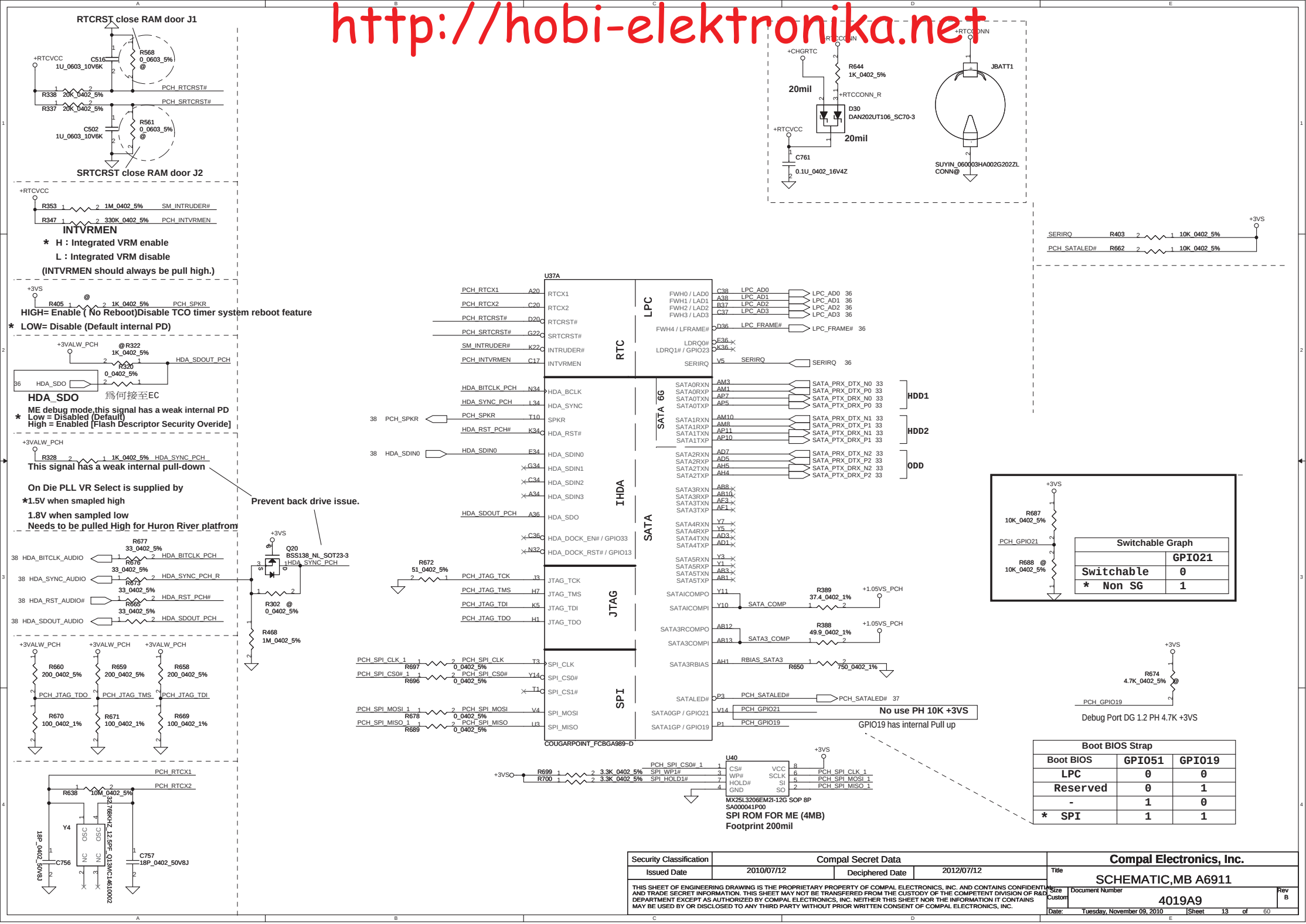


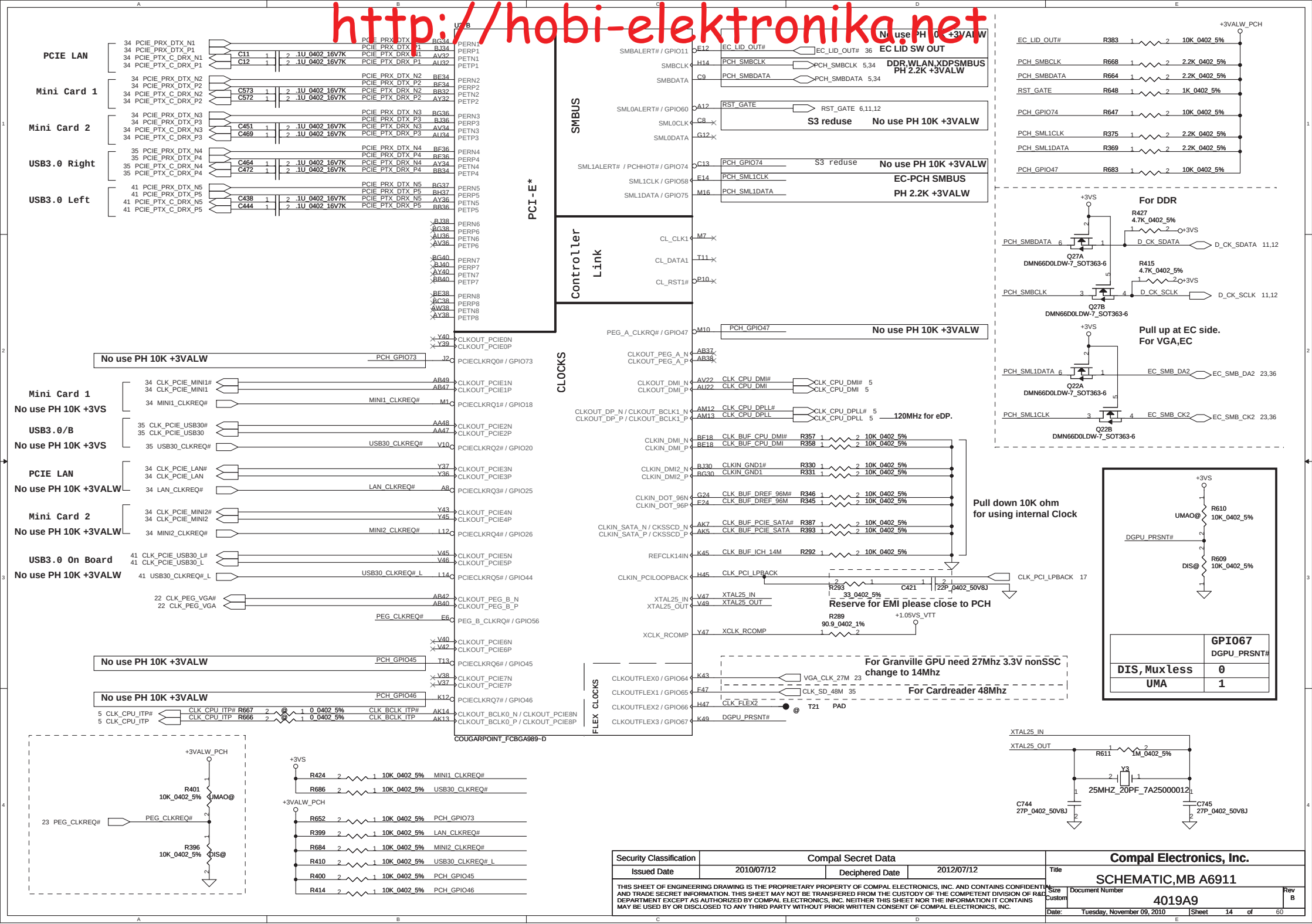
Channel A

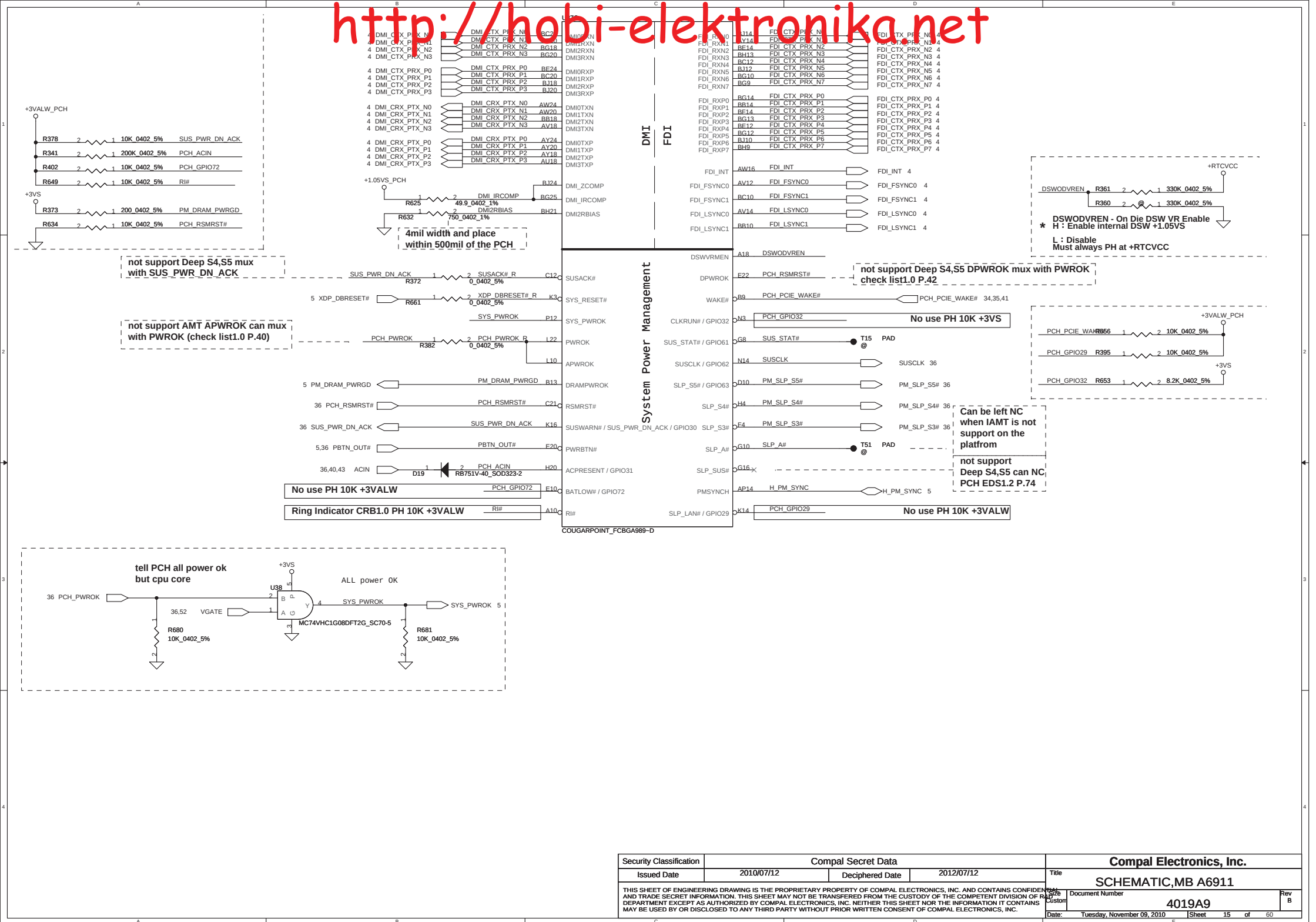


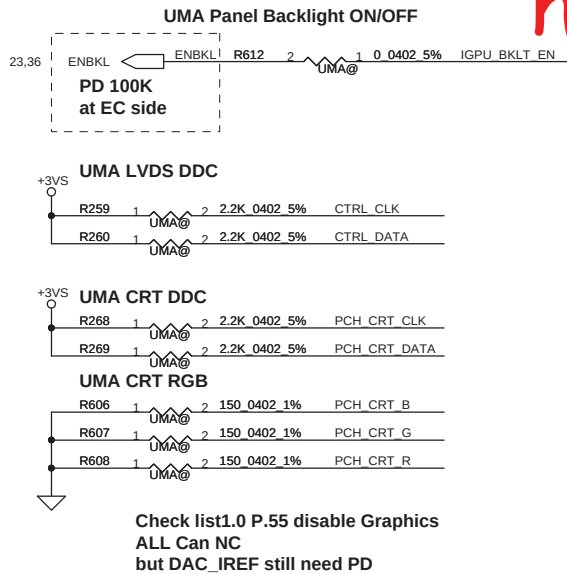
Channel B

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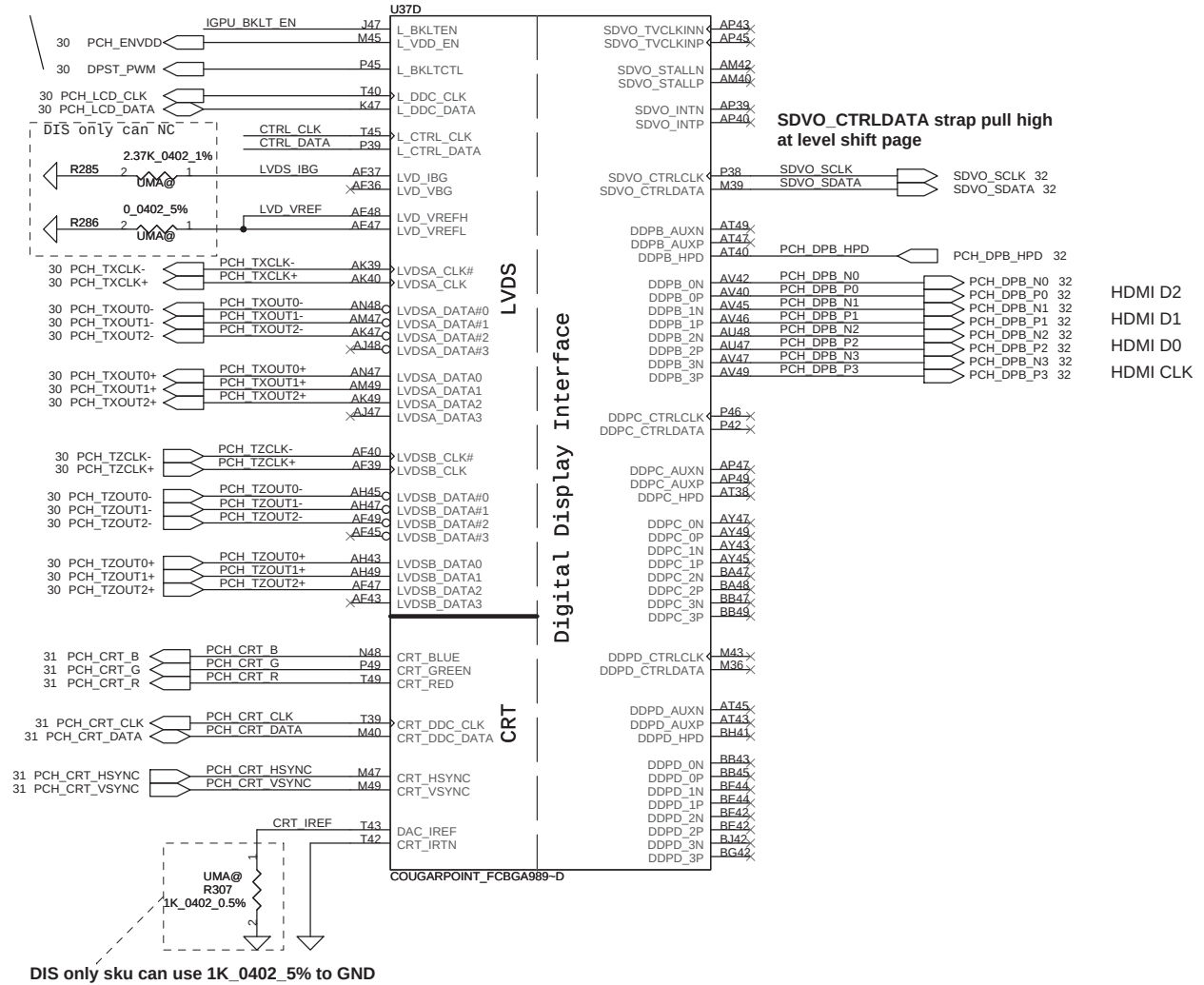




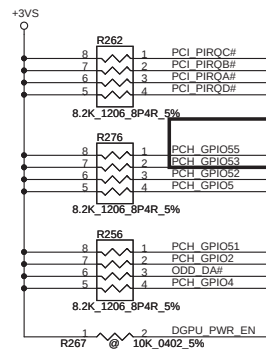
LVDS disable:
DATA/Clock/Control an NC
VCC_TX_LVDS,VCCA_LVDS PD to GND

CRT disable:
DATA/Clock/Control an NC
VCCADAC connect to +3VS

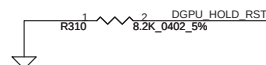
Pull high at LVDS conn side.



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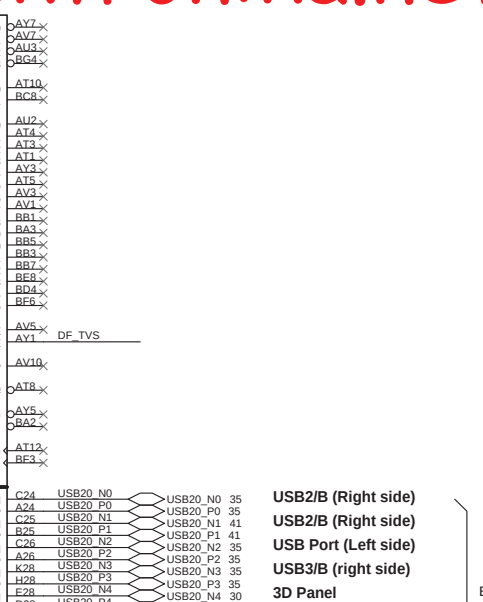
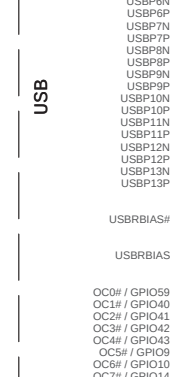
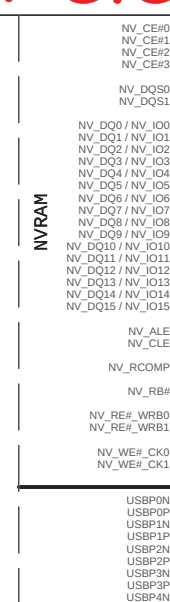
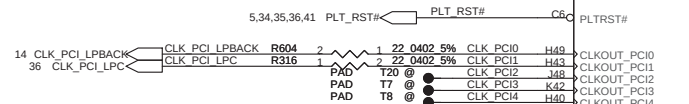
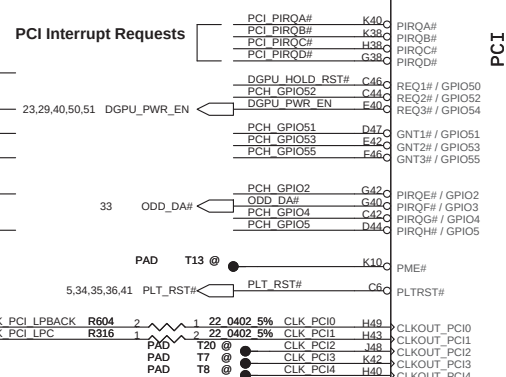
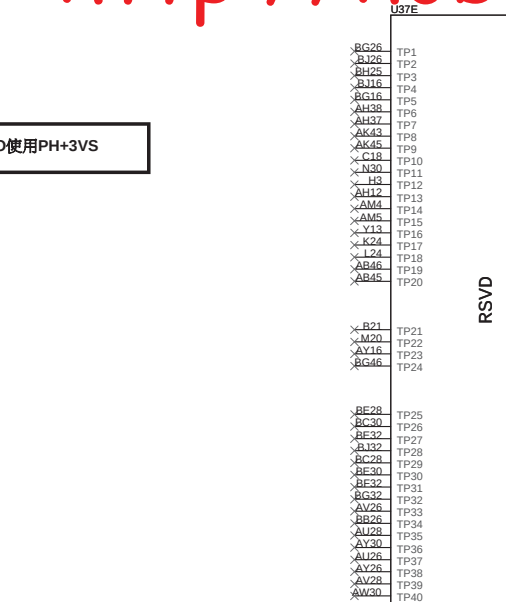
可以不用PH,如做GPIO使用PH+3VS



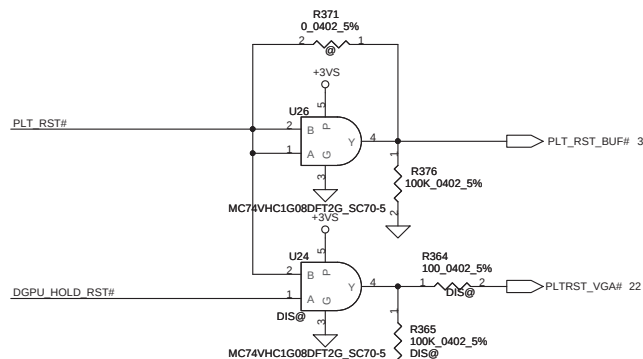
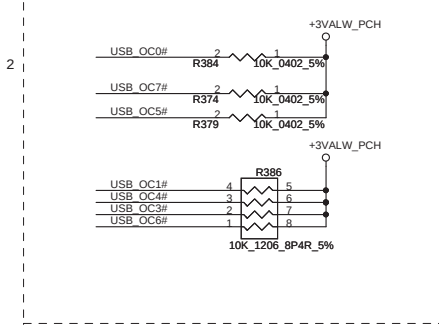
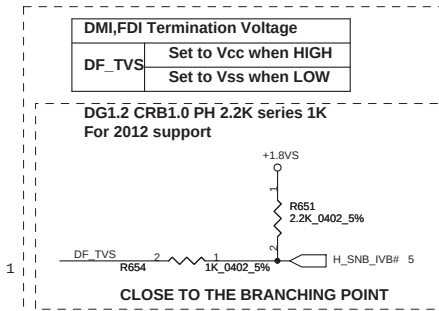
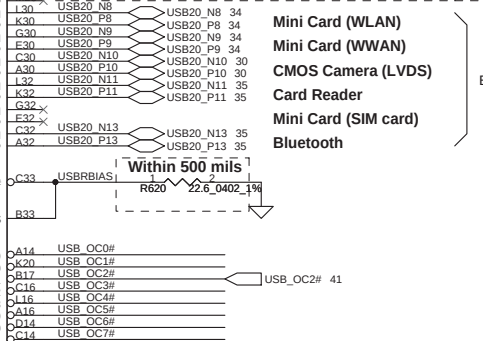
Boot BIOS Strap			
GNT1#/ GPIO51	GPIO19	GPIO51	Boot BIOS
	Bit11	Bit10	Destination
Internal PH	0	1	Reserved
	1	0	PCI
	1	1	SPI *
	0	0	LPC

只剩GPIO的功能沒有strap function
不做GPIO要PH +3VS,如做GPIO PH +3VS

只剩GPIO的功能沒有strap function
無須PH(Internal PH),如做GPIO PH +3VS



Some PCH config not support USB port 6 & 7.



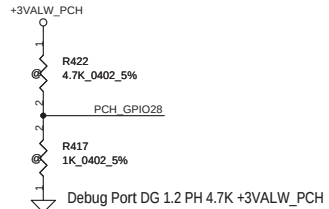
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HDA_SYNC PH(PLL +/-1.5VS)

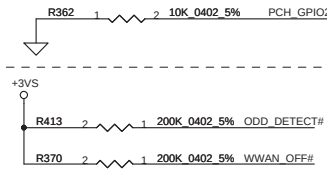
GPIO28

On-Die PLL Voltage Regulator

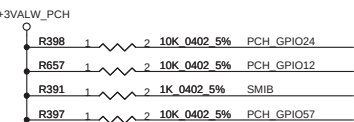
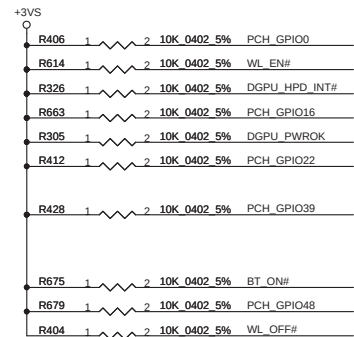
This signal has a weak internal pull up
* H : On-Die PLL voltage regulator enable
L : On-Die PLL Voltage Regulator disable



Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70



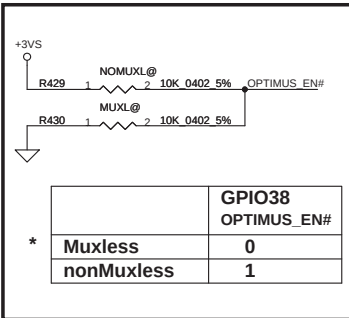
SATA2GP/GPIO36 & SATA3GP/GPIO37
Sampled at Rising edge of PWROK.
Weak internal pull-down.
(weak internal pull-down is disabled
after PLTRST# de-asserts)
NOTE: This signal should NOT be
pulled high when strap is sampled



No use PH 10K +3VS	PCH_GPIO0	T7
No use PH 10K +3VS	35 WL_EN#	A42
No use PH 10K +3VS	32 DGPU_HPD_INT#	H36
	36 EC_SC#	E38
	36 EC_SMI#	C10

No use PH +3VALW	PCH_GPIO12	C4
USB3.0 System management Interrupt signal "SMI#".	35,41 SMIB	G2
No use PH +3VS	PCH_GPIO16	U2

No use PH 10K +3VS	PCH_GPIO22	T5
CRB1.0 PH 10K +3VALW	PCH_GPIO24	E8
No use PD 10K to GND	PCH_GPIO27	F16
No use PH 10K +3VALW	PCH_GPIO28	P8
No use PH 10K +3VS BT ON/OFF	34,35 BT_ON#	K1
No use can NC	PAD T16 @	K4
Can't PH	33 ODD_DETECT#	V8
Can't PH	34 WWAN_OFF#	M5
No use PH 10K +3VS Optimus(L)/ non optimus(H)	OPTIMUS_EN#	N2
No use PH 10K +3VS	PCH_GPIO39	M3
No use PH 10K +3VS	PCH_GPIO48	V13
SATA5GP&TEMP_ALERT# CRB PH 10K +3VSWL_OFF#	WL_OFF#	V3
No use PH +3VALW or PD to GND	PCH_GPIO57	D6



	GPIO38 OPTIMUS_EN#
* Muxless	0
nonMuxless	1

GPIO24 Unmultiplexed
NOTE: GPIO24 configuration
register bits are not cleared by
CF9h reset event.
CRB1.0 PH10K to +3VALW

PAD T47 @	A4	VSS_NCTF_1
PAD T30 @	A44	VSS_NCTF_2
PAD T28 @	A45	VSS_NCTF_3
PAD T27 @	A46	VSS_NCTF_4
PAD T49 @	A5	VSS_NCTF_5
PAD T46 @	A6	VSS_NCTF_6
PAD T50 @	B3	VSS_NCTF_7
PAD T26 @	B47	VSS_NCTF_8
PAD T43 @	BD1	VSS_NCTF_9
PAD T17 @	BD49	VSS_NCTF_10
PAD T44 @	BE1	VSS_NCTF_11
PAD T23 @	BE49	VSS_NCTF_12
PAD T45 @	BE1	VSS_NCTF_13
PAD T18 @	BE49	VSS_NCTF_14

COUGARPOINT_FCBGA989-D

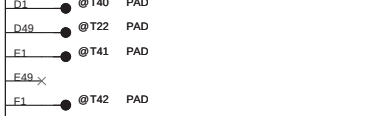
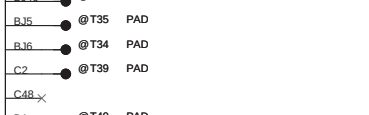
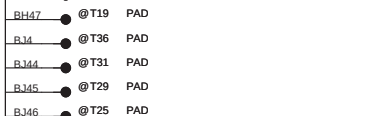
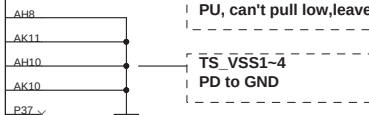
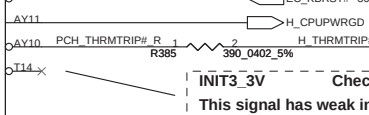
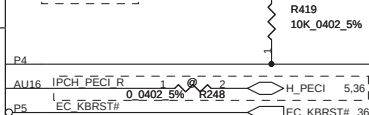
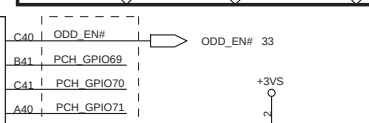
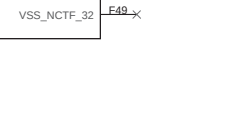
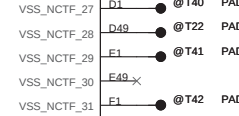
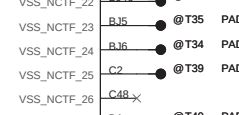
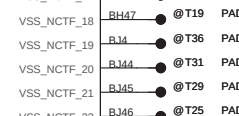
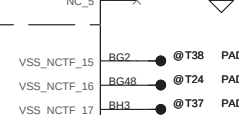
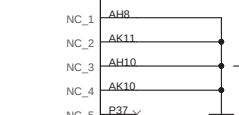
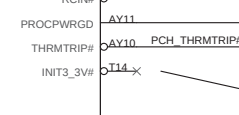
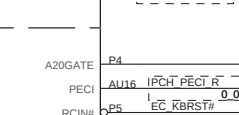
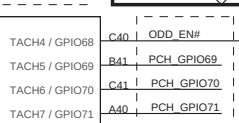
Fan Tachometer Inputs
TACH1-7 only on server
can insted to GPIO



GPIO

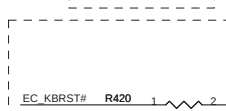
CPU/MISC

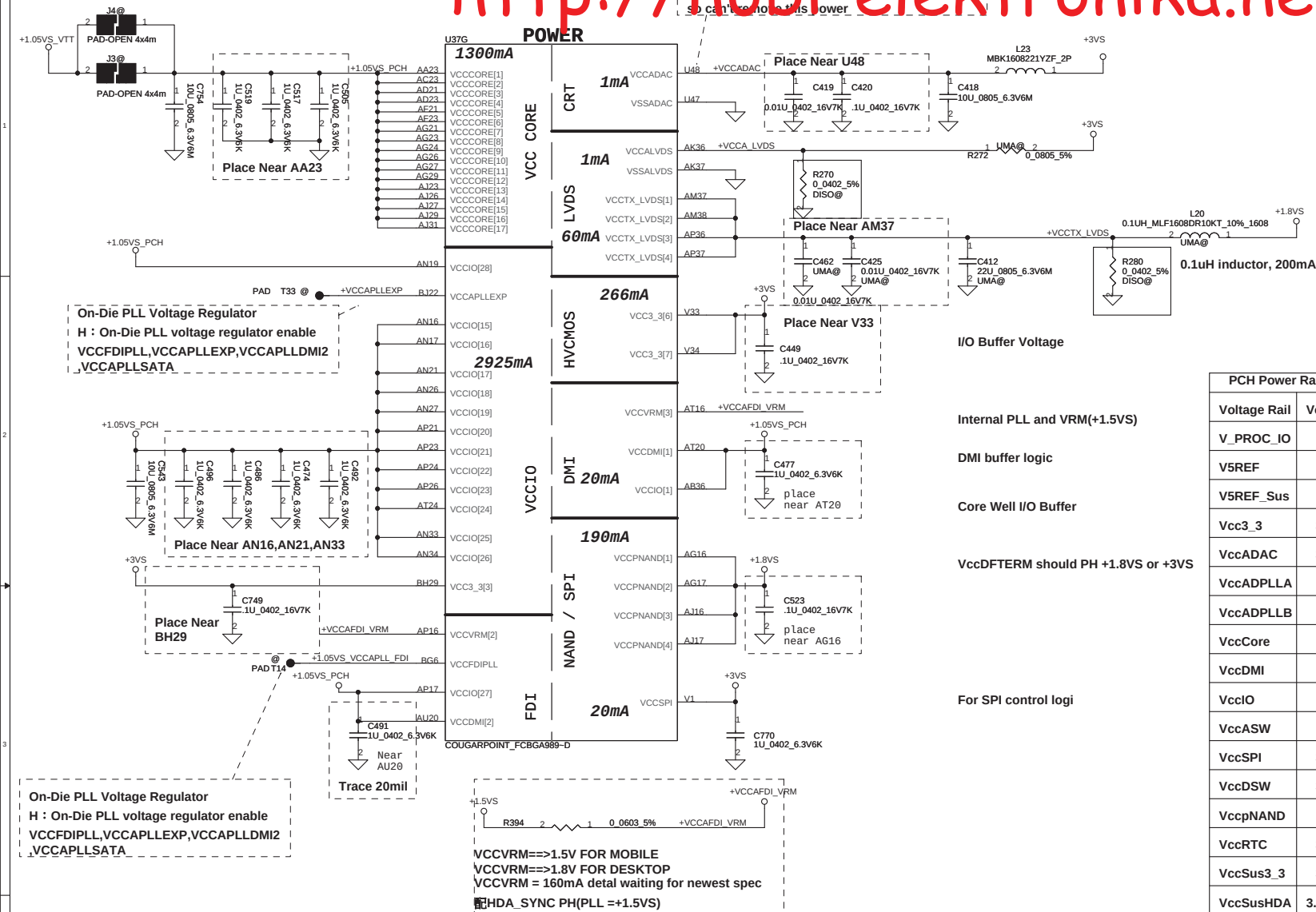
NCTF



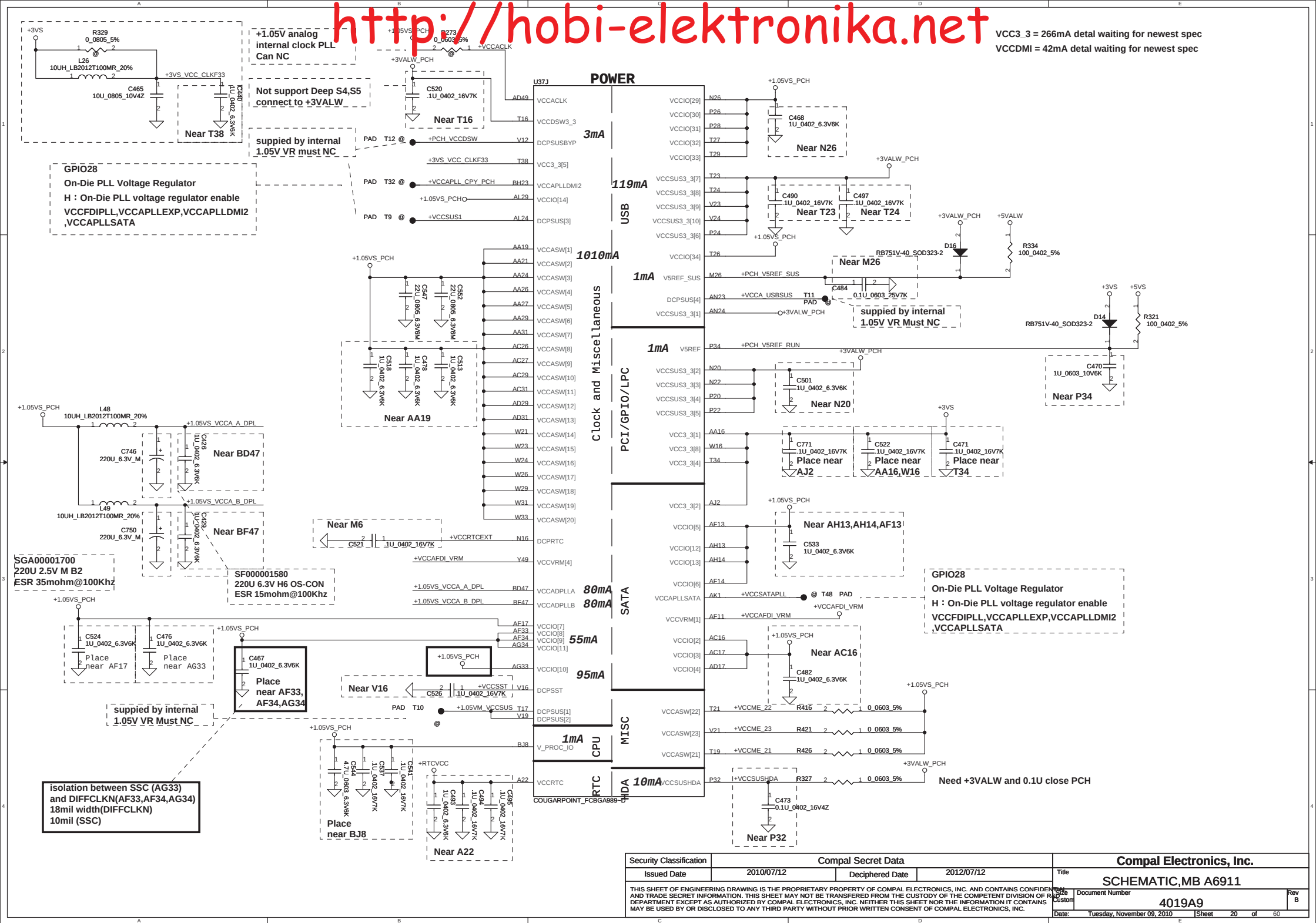
Project ID	GPIO69	GPIO70	GPIO71
* P7YE0	0	0	0
X	0	0	1
X	0	1	0
X	0	1	1
X	1	0	0
X	0	0	1
X	0	1	0
X	0	1	1
X	1	0	0
X	1	0	1
X	1	1	0
X	1	1	1

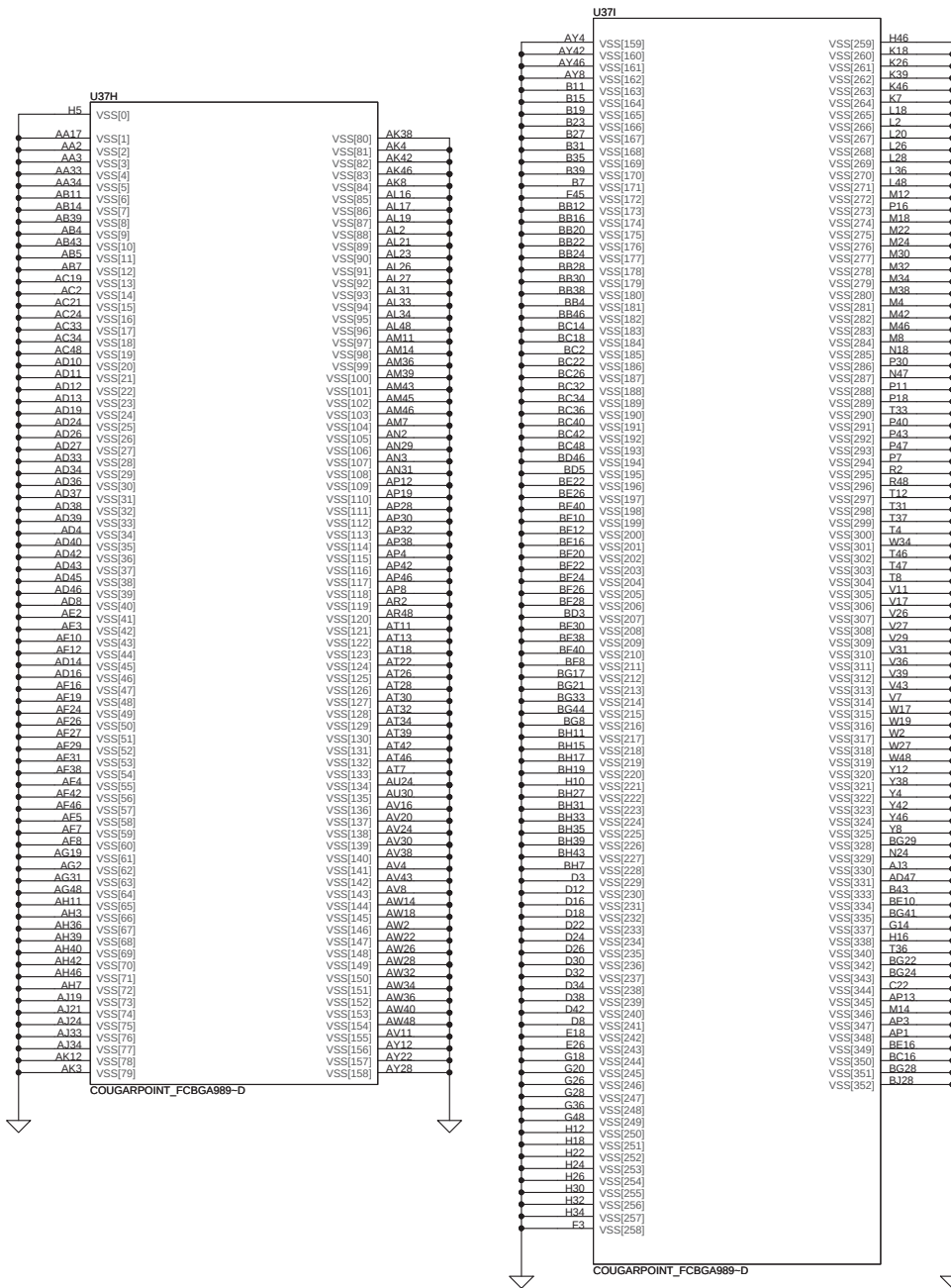
PECI CPU-EC
CTRL+ALT+DEL
non CPU power ok
130c shut sown





PCH Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltage
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)





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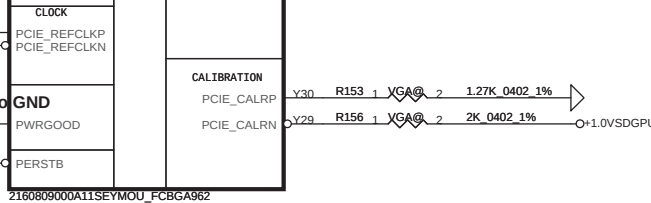
GFX PCIE LINE REVERSAL

<http://hobi-elektronika.net>

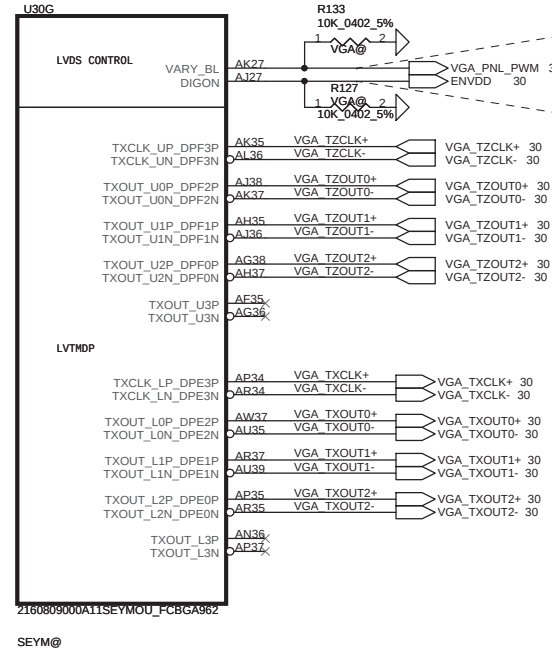
4 PEG_GTX_HRX_N[0..15]
4 PEG_GTX_HRX_P[0..15]
4 PEG_HTX_C_GRX_N[0..15]
4 PEG_HTX_C_GRX_P[0..15]



14 CLK_PEG_VGA
14 CLK_PEG_VGA#
For M96, AH16 is NC
For Boardway,Madison,Park, AH16 must connect to GND
R141 10K 0402 5%
17 PLTRST_VGA#



SEYM@
Park XT P/N : SA00003M570 (S IC 216-0774009 A11 PARK XT S3 631P C38)
Madison Pro P/N : SA00003M360 (S IC 216-0772000 MADISON PRO FCBGA 0FA)
Seymour XT P/N: SA000047H00 (S IC 216-0809000 A11 SEYMOUR XT M2 0FH)

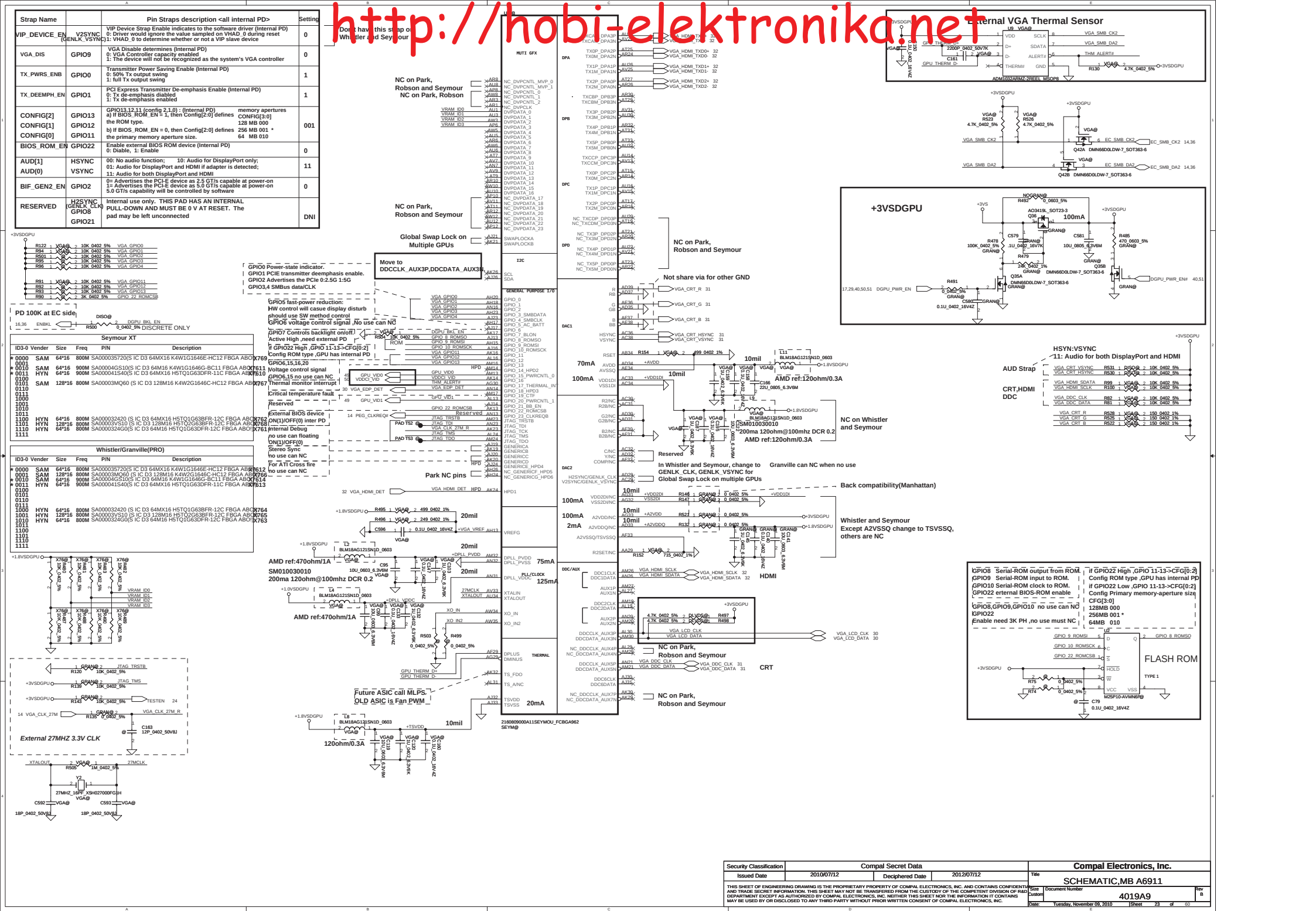


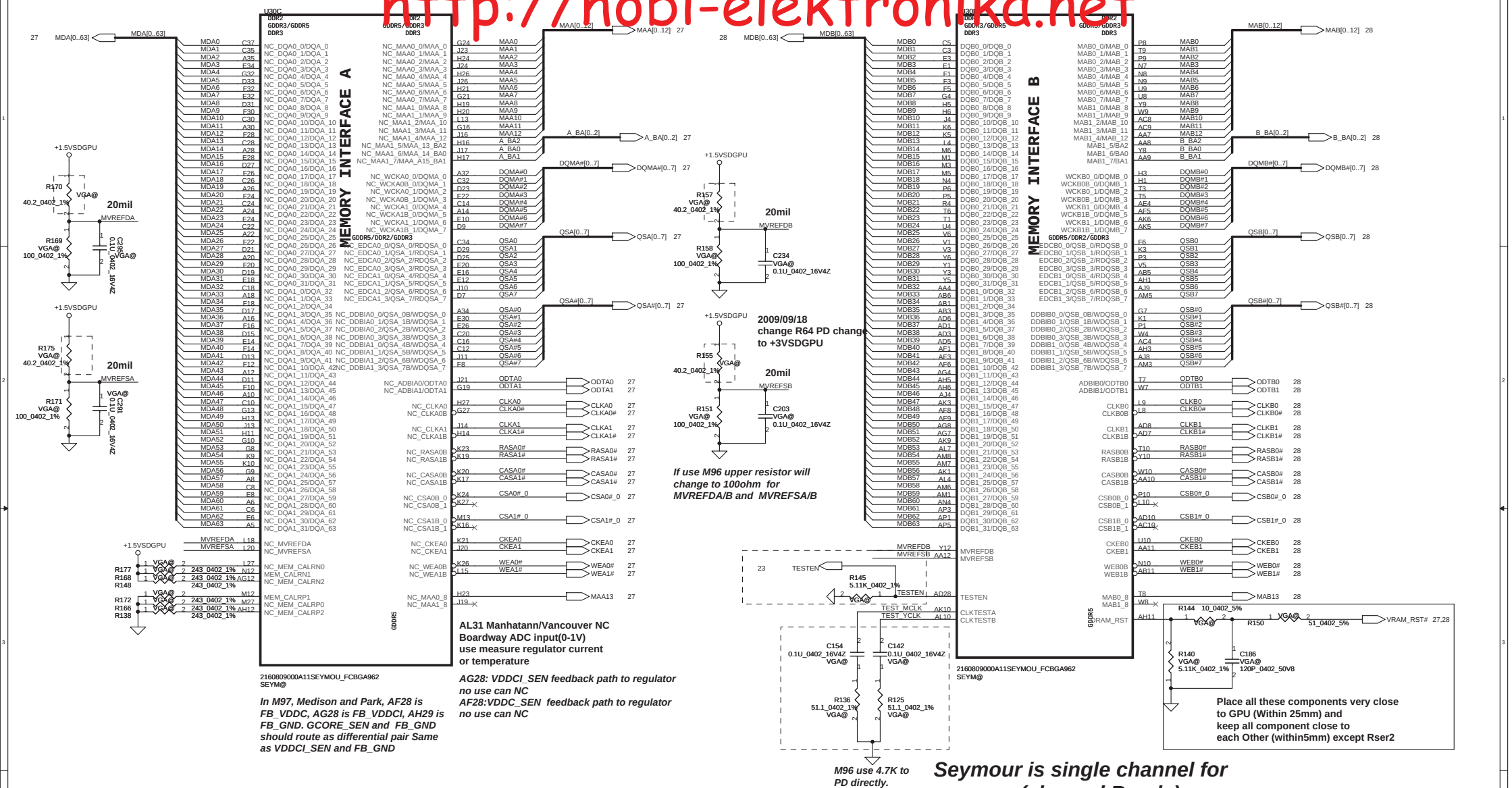
LCD PWM (pulse width modulated)
output to adjust LCD brightness
Active High ,external PD need
Controls panel digital power on/off.
Active High ,external PD need

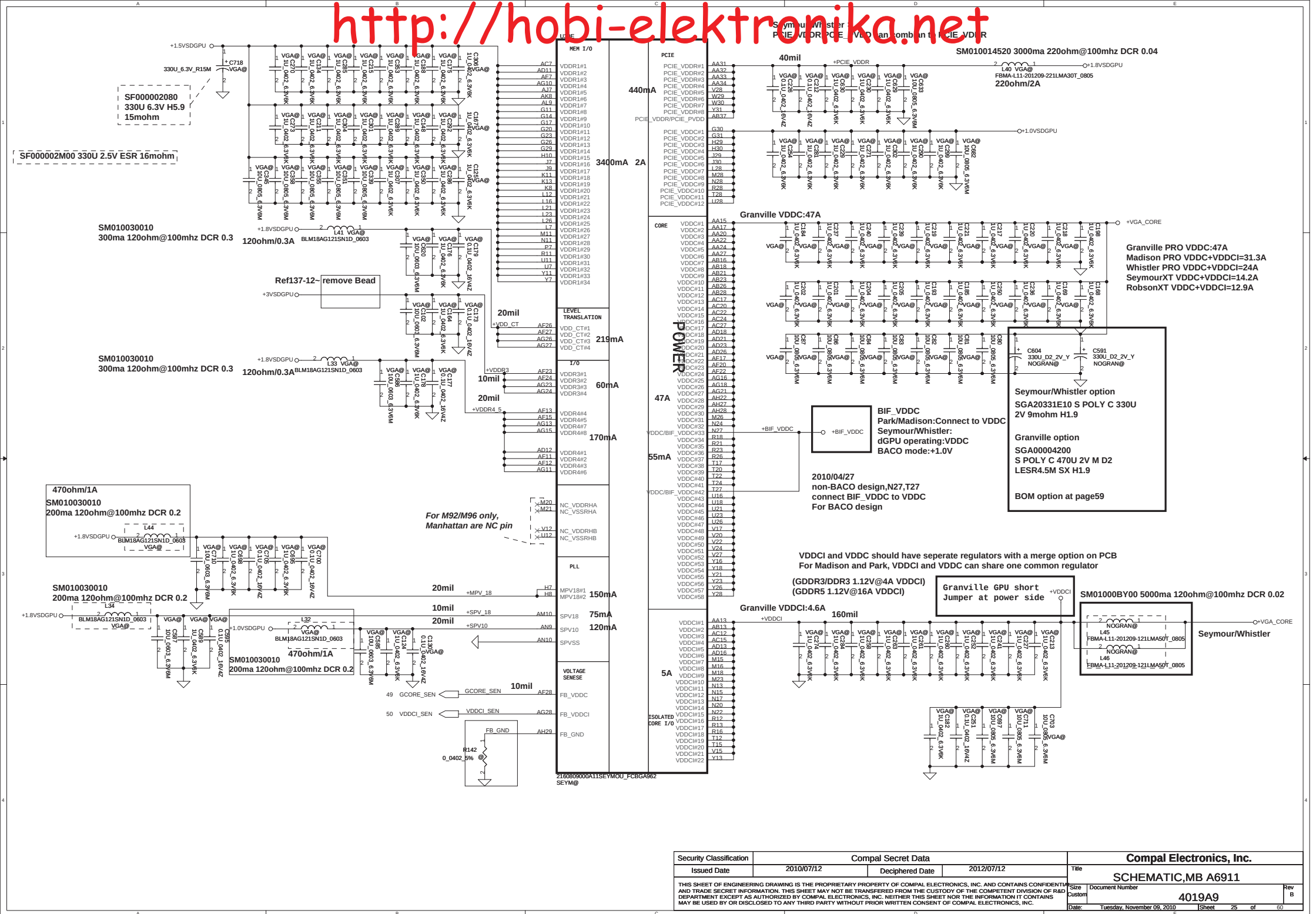
Display Port F config

Display Port E config

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PX_EN needs to be isolated during a scan dump

PD 5.11K at VGA side

PX_EN = 1, For BACO Mode
PX_EN = 0, For Normal Mode

PX_EN:
Connect to PWR to shutdown
VDDC/VDDCI/VDDR1
(VGA_CORE, +1.5VSDGPU)
High in BACO mode

BACO_EN/BACO_EN#:
0: BACO Mode->BACO_EN High->
BIF_VDDC=+1.0VSDGPU(N-MOS),VGA_CORE(P-MOS)

1: Normal mode->BACO_EN# High->
BIF_VDDC=+VGA_CORE(N-MOS),VGA_CORE(N-MOS)

BACO_EN#=1 (BACO mode)
BACO_EN#=0 (Normal mode)
BACO_EN=0 (BACO mode)
BACO_EN=1 (Normal mode)

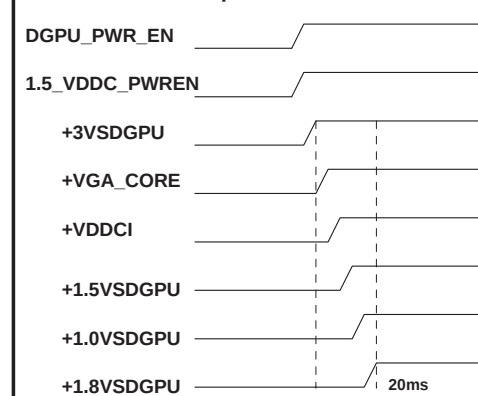
VGA Status Mapping table

	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
BACO_EN#	1	0
BACO_EN	0	1
+3VSDGPU	ON	ON
+1.8VSDGPU	ON	ON
+1.0VSDGPU	ON	ON
+VGA_CORE	ON	OFF
+1.5VSDGPU	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSDGPU

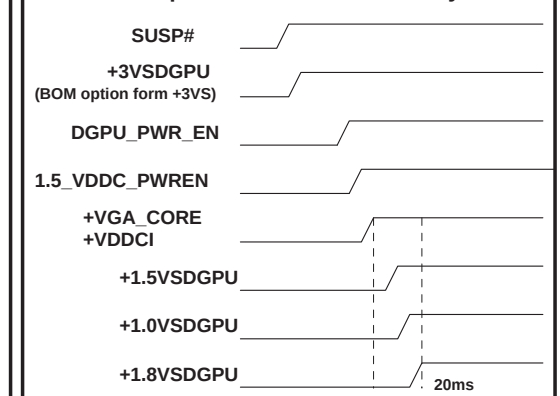
VGA Power Enable Signal Mapping table

	Graville	Whistler and Seymour
+3VSDGPU	DGPU_PWR_EN	SUSP#
+1.8VSDGPU	DGPU_PWR_EN	DGPU_PWR_EN
+1.0VSDGPU	DGPU_PWR_EN	DGPU_PWR_EN
+VDDCI	DGPU_PWR_EN	Combine with +VGA_CORE
+VGA_CORE	DGPU_PWR_EN	1.5_VDDC_PWREN
+1.5VSDGPU	DGPU_PWR_EN	1.5_VDDC_PWREN

Power Sequence of Graville



Power Sequence of Whistler and Seymour



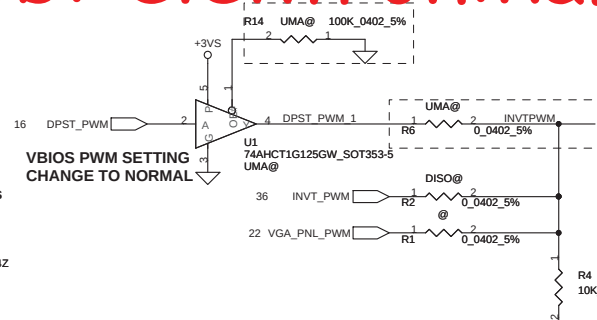
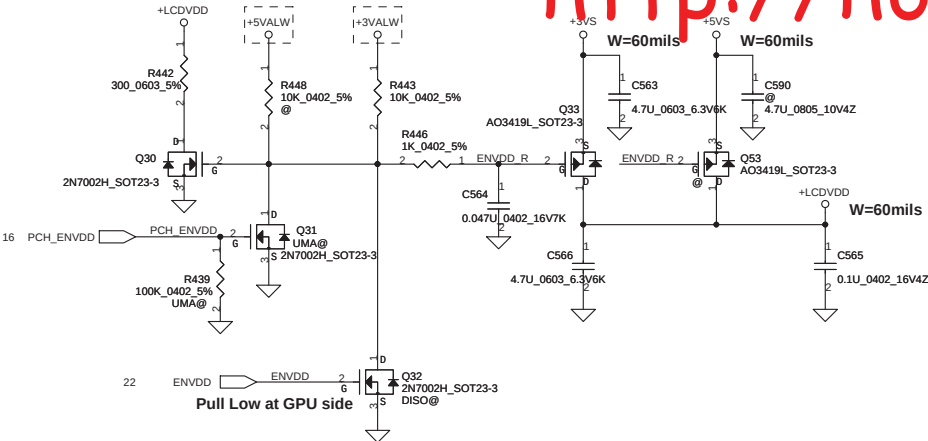
PX_EN = 1, For BACO Mode
BACO_EN=0
BACO_EN#=1(5V)==> BIF_VDDC=+1.0VSDGPU
PX_EN = 0, For Normal Mode
BACO_EN=1(5V) ==> BIF_VDDC=VGA_CORE
BACO_EN#=0

For the MOSFETs on the path of delivering
PCIE_VDDC(+1.0VSDGPU) to
BIF_VDDC Rds on of 140 mOhms or less is required.

For the MOSFETs on the path of delivering VGA_CORE to
BIF_VDDC, Rds on of 21 mOhms or less is required.

100505 change to +3VALW
101029 add +5VALW

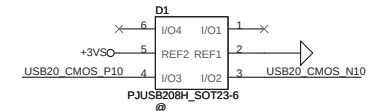
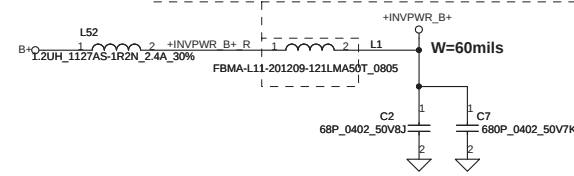
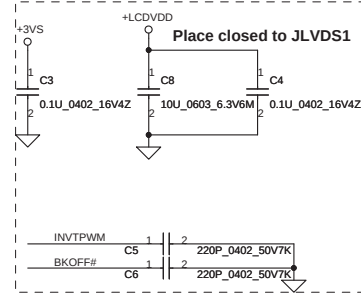
LCD POWER CIRCUIT



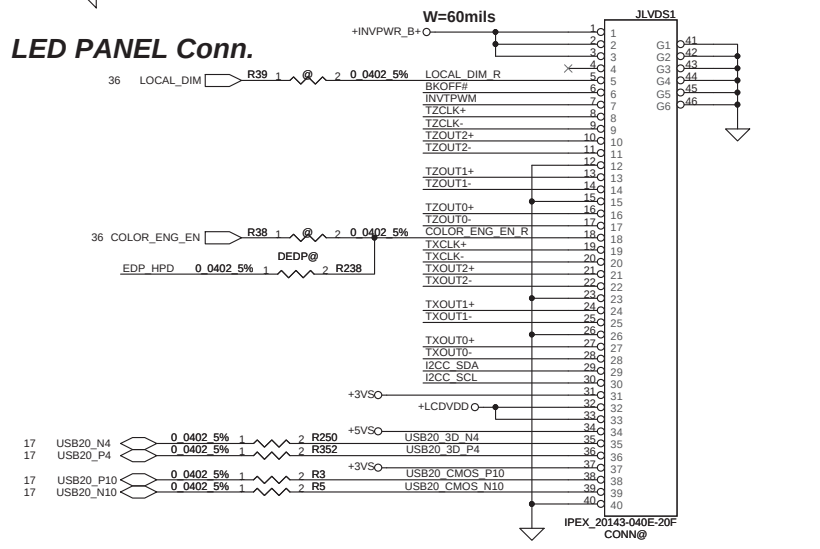
UMA/DIS LVDS/eDP Mapping table		DIS		Panel Conn.
UMA	eDP	LVDS	eDP	
PCH_TXOUT0+		VGA_TXOUT0+		TXOUT0+
PCH_TXOUT0-		VGA_TXOUT0-		TXOUT0-
PCH_TXOUT1+	EDP_TXP1	VGA_TXOUT1+	DP1P	TXOUT1+
PCH_TXOUT1-	EDP_TXN1	VGA_TXOUT1-	DP1N	TXOUT1-
PCH_TXOUT2+	EDP_TXP0	VGA_TXOUT2+	DP0P	TXOUT2+
PCH_TXOUT2-	EDP_TXN0	VGA_TXOUT2-	DP0N	TXOUT2-
PCH_TXCLK+		VGA_TXCLK+		TXCLK+
PCH_TXCLK-		VGA_TXCLK-		TXCLK-
PCH_TZOUT0+		VGA_TZOUT0+		TZOUT0+
PCH_TZOUT0-		VGA_TZOUT0-		TZOUT0-
PCH_TZOUT1+		VGA_TZOUT1+		TZOUT1+
PCH_TZOUT1-		VGA_TZOUT1-		TZOUT1-
PCH_TZOUT2+		VGA_TZOUT2+		TZOUT2+
PCH_TZOUT2-		VGA_TZOUT2-		TZOUT2-
PCH_TZCLK+		VGA_TZCLK+		TZCLK+
PCH_TZCLK-		VGA_TZCLK-		TZCLK-
PCH_I2CC_SCL	EDP_AUXP	VGA_LCD_CLK	AUXP	I2CC_SCL
PCH_I2CC_SDA	EDP_AUXN	VGA_LCD_DATA	AUXN	I2CC_SDA

SM010014520 3000ma 220ohm@100mhz DCR 0.04

SM01000BY00 5000ma 120ohm@100mhz DCR 0.02



LED PANEL Conn.

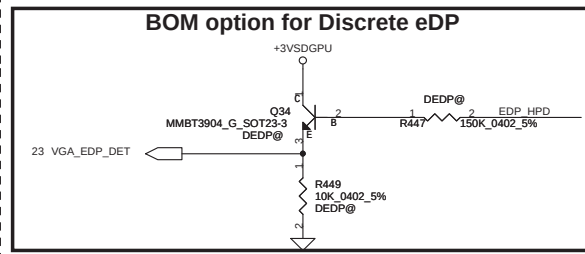


UMA ONLY/Muxless

16 PCH_TXOUT0+	PCH_TXOUT0+	R452	1	ULVDS@	0.0402 5%	TXOUT0+
16 PCH_TXOUT0-	PCH_TXOUT0-	R450	1	ULVDS@	0.0402 5%	TXOUT0-
16 PCH_TXOUT1+	PCH_TXOUT1+	R455	1	ULVDS@	0.0402 5%	TXOUT1+
16 PCH_TXOUT1-	PCH_TXOUT1-	R453	1	ULVDS@	0.0402 5%	TXOUT1-
16 PCH_TXOUT2+	PCH_TXOUT2+	R456	1	ULVDS@	0.0402 5%	TXOUT2+
16 PCH_TXOUT2-	PCH_TXOUT2-	R454	1	ULVDS@	0.0402 5%	TXOUT2-
16 PCH_TXCLK+	PCH_TXCLK+	R458	1	ULVDS@	0.0402 5%	TXCLK+
16 PCH_TXCLK-	PCH_TXCLK-	R457	1	ULVDS@	0.0402 5%	TXCLK-
16 PCH_TZOUT0+	PCH_TZOUT0+	R460	1	ULVDS@	0.0402 5%	TZOUT0+
16 PCH_TZOUT0-	PCH_TZOUT0-	R459	1	ULVDS@	0.0402 5%	TZOUT0-
16 PCH_TZOUT1+	PCH_TZOUT1+	R462	1	ULVDS@	0.0402 5%	TZOUT1+
16 PCH_TZOUT1-	PCH_TZOUT1-	R461	1	ULVDS@	0.0402 5%	TZOUT1-
16 PCH_TZOUT2+	PCH_TZOUT2+	R465	1	ULVDS@	0.0402 5%	TZOUT2+
16 PCH_TZOUT2-	PCH_TZOUT2-	R463	1	ULVDS@	0.0402 5%	TZOUT2-
16 PCH_TZCLK+	PCH_TZCLK+	R467	1	ULVDS@	0.0402 5%	TZCLK+
16 PCH_TZCLK-	PCH_TZCLK-	R466	1	ULVDS@	0.0402 5%	TZCLK-
16 PCH_LCD_CLK	PCH_LCD_CLK	R444	1	ULVDS@	0.0402 5%	I2CC_SCL
16 PCH_LCD_DATA	PCH_LCD_DATA	R445	1	ULVDS@	0.0402 5%	I2CC_SDA

5/4 PCH_LCD_CLK & PCH_LCD_DATA
Pull high 2.2K change to 4.7K

BOM option for Discrete eDP

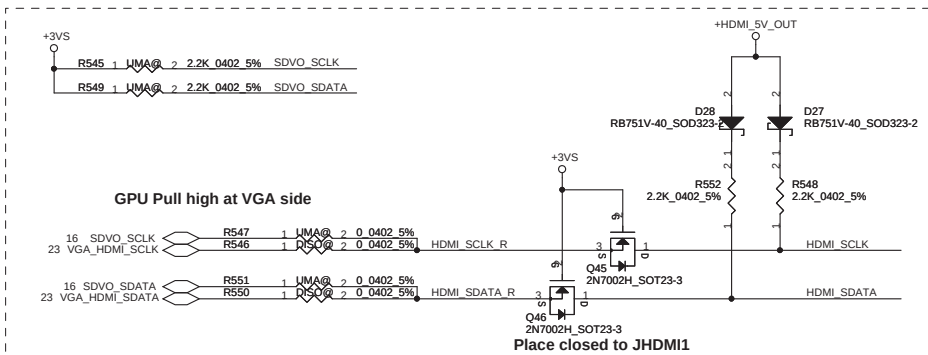
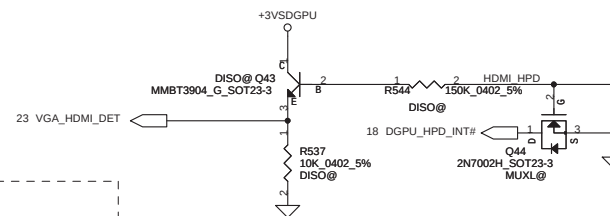
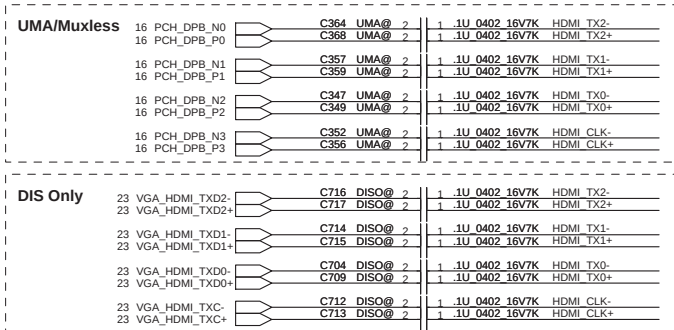
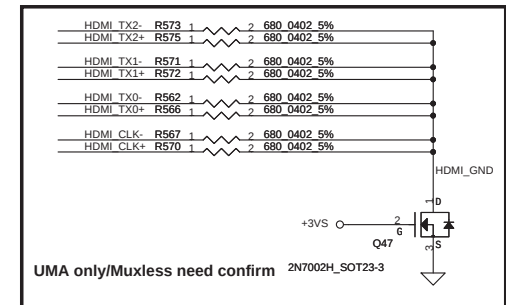
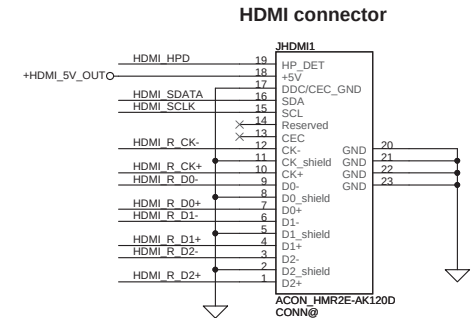
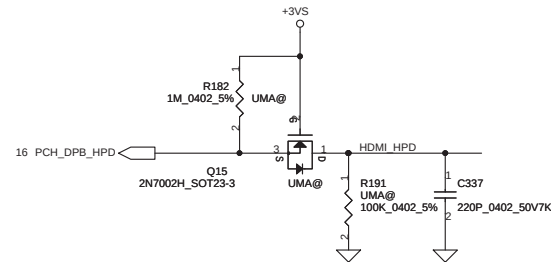


Discrete ONLY

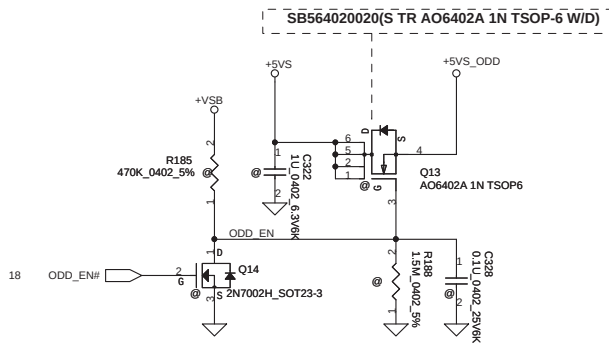
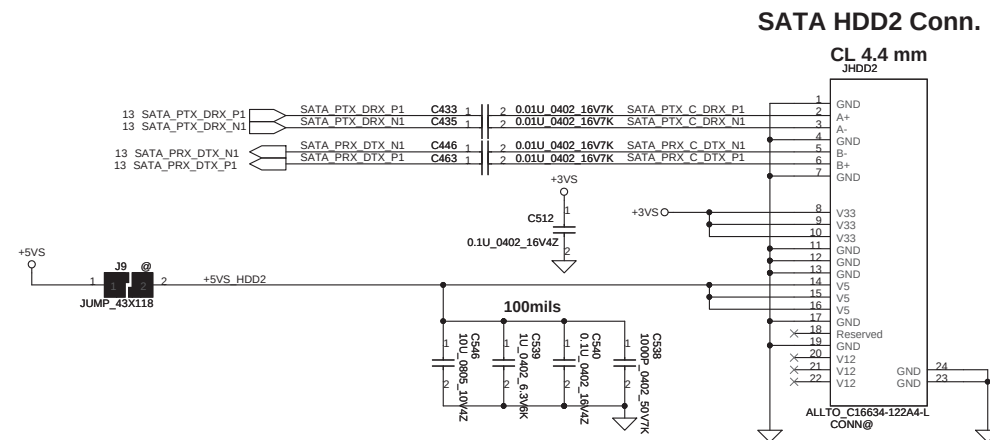
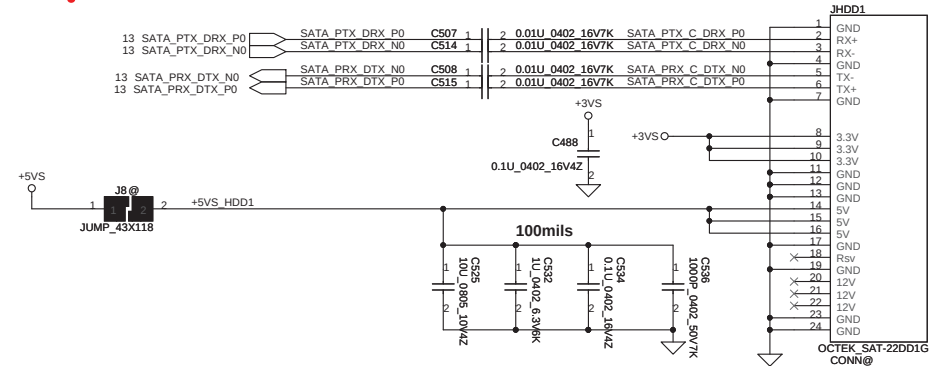
22 VGA_TXOUT0+	VGA_TXOUT0+	R13	1	ULVDS@	0.0402 5%	TXOUT0+
22 VGA_TXOUT0-	VGA_TXOUT0-	R12	1	ULVDS@	0.0402 5%	TXOUT0-
22 VGA_TXOUT1+	VGA_TXOUT1+	R23	1	ULVDS@	0.0402 5%	TXOUT1+
22 VGA_TXOUT1-	VGA_TXOUT1-	R17	1	ULVDS@	0.0402 5%	TXOUT1-
22 VGA_TXOUT2+	VGA_TXOUT2+	R24	1	ULVDS@	0.0402 5%	TXOUT2+
22 VGA_TXOUT2-	VGA_TXOUT2-	R22	1	ULVDS@	0.0402 5%	TXOUT2-
22 VGA_TXCLK+	VGA_TXCLK+	R26	1	ULVDS@	0.0402 5%	TXCLK+
22 VGA_TXCLK-	VGA_TXCLK-	R25	1	ULVDS@	0.0402 5%	TXCLK-
22 VGA_TZOUT0+	VGA_TZOUT0+	R28	1	ULVDS@	0.0402 5%	TZOUT0+
22 VGA_TZOUT0-	VGA_TZOUT0-	R27	1	ULVDS@	0.0402 5%	TZOUT0-
22 VGA_TZOUT1+	VGA_TZOUT1+	R30	1	ULVDS@	0.0402 5%	TZOUT1+
22 VGA_TZOUT1-	VGA_TZOUT1-	R29	1	ULVDS@	0.0402 5%	TZOUT1-
22 VGA_TZOUT2+	VGA_TZOUT2+	R32	1	ULVDS@	0.0402 5%	TZOUT2+
22 VGA_TZOUT2-	VGA_TZOUT2-	R31	1	ULVDS@	0.0402 5%	TZOUT2-
22 VGA_TZCLK+	VGA_TZCLK+	R34	1	ULVDS@	0.0402 5%	TZCLK+
22 VGA_TZCLK-	VGA_TZCLK-	R33	1	ULVDS@	0.0402 5%	TZCLK-
23 VGA_LCD_CLK	VGA_LCD_CLK	R9	1	ULVDS@	0.0402 5%	I2CC_SCL
23 VGA_LCD_DATA	VGA_LCD_DATA	R7	1	ULVDS@	0.0402 5%	I2CC_SDA

Discrete only

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				Document Number	Rev B
Date:	Tuesday, November 09, 2010	Sheet	31	of	60



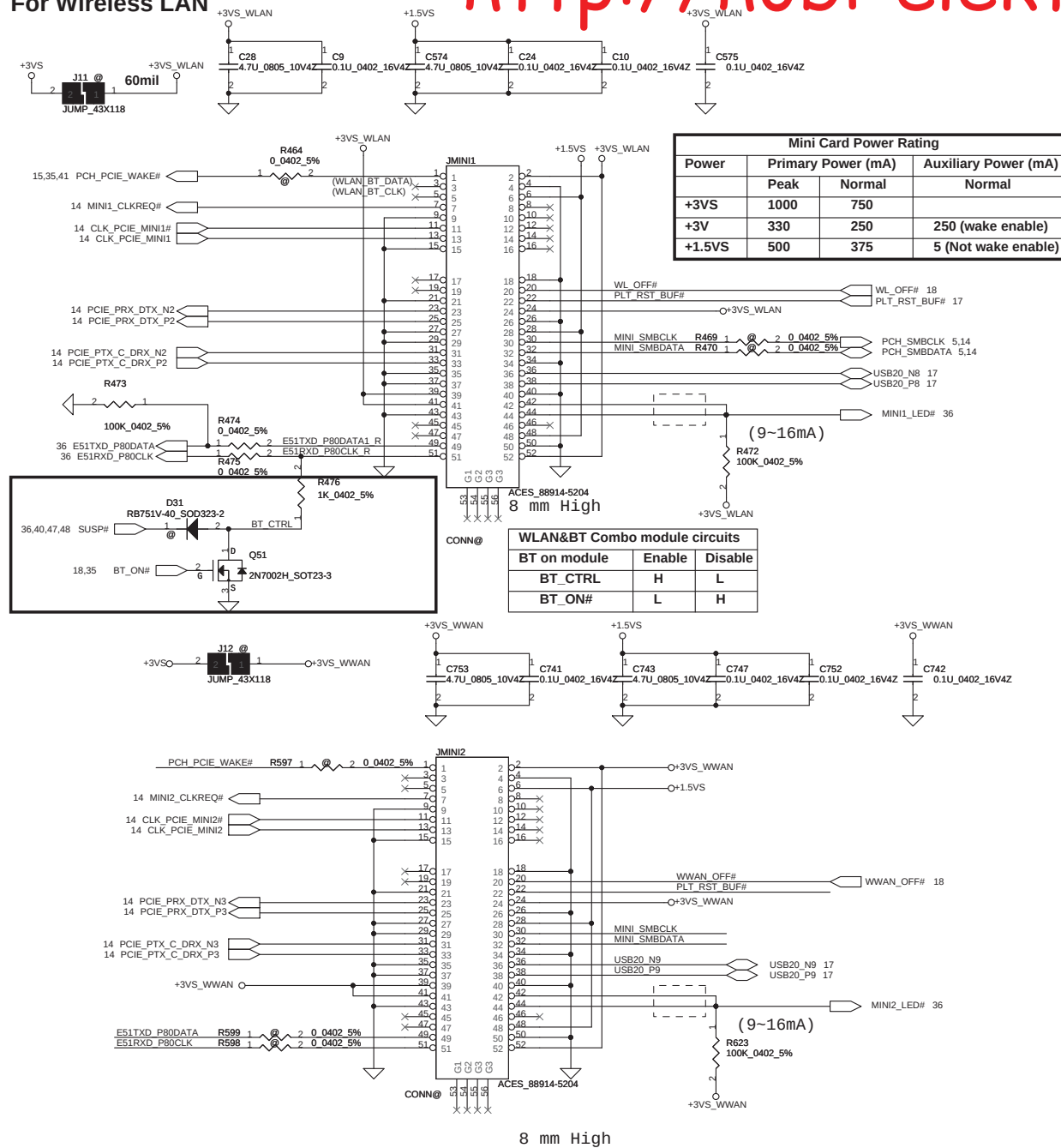
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								Customer	4019A9		
Date:				Tuesday, November 09, 2010		Sheet		32		of 60	



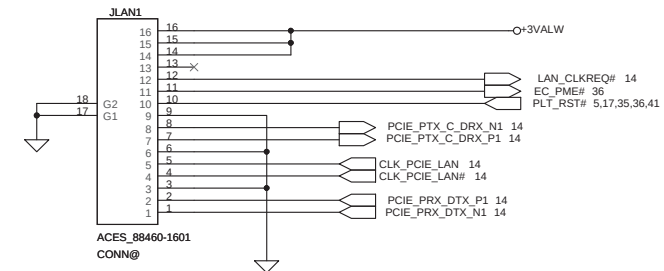
Place Cap near ODD Conn.

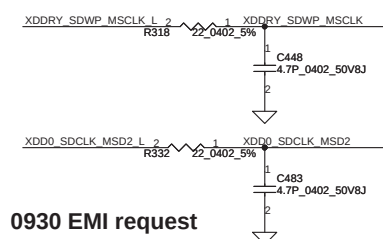
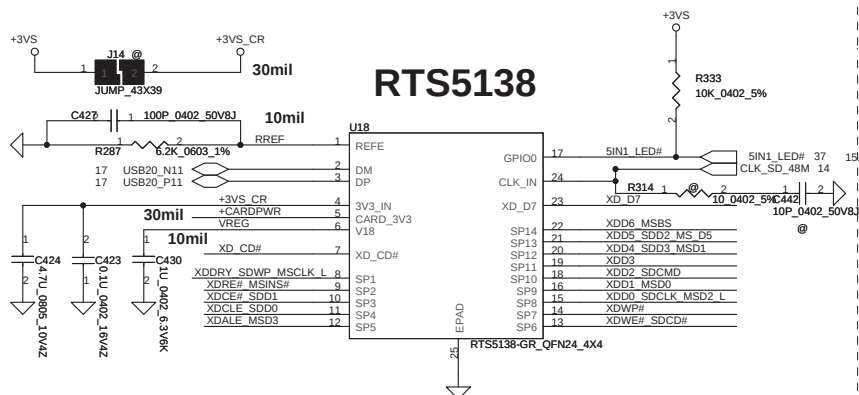
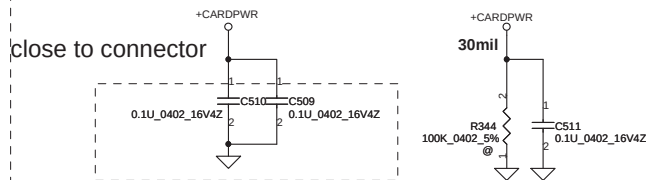
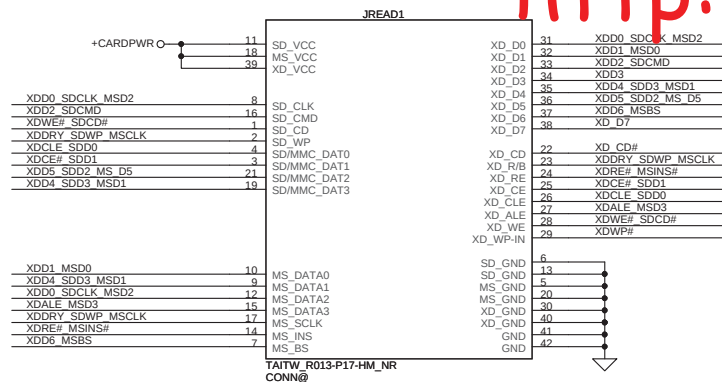
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				Date:	Tuesday, November 09, 2010
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For Wireless LAN



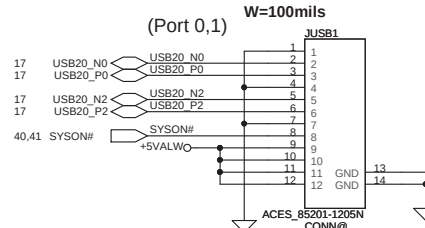
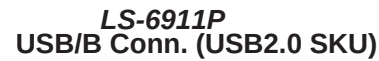
LAN CONN. LS-6912P





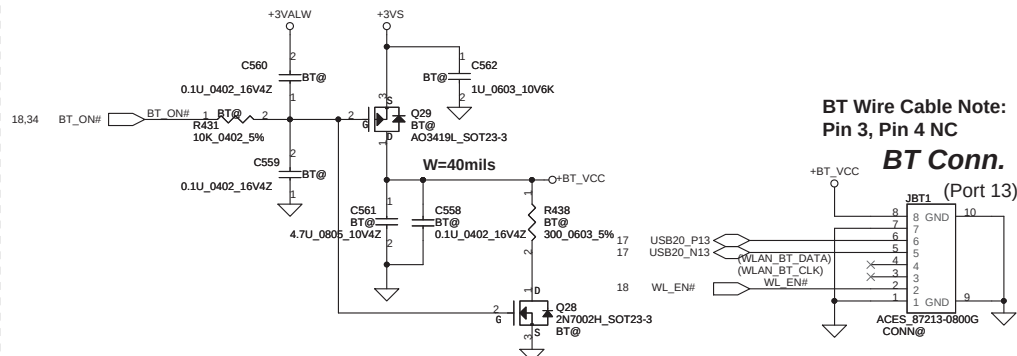
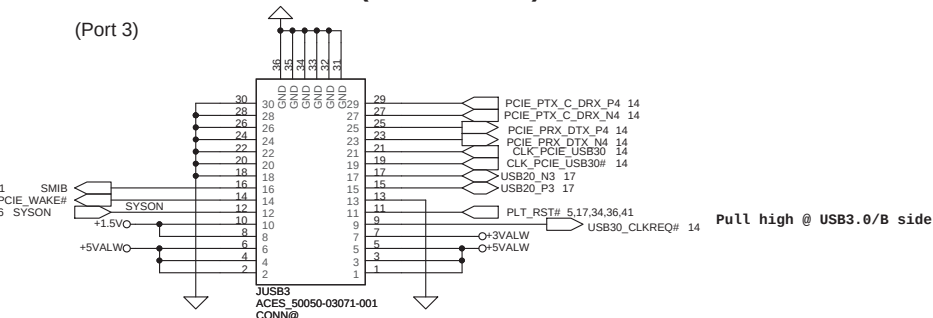
	XD	SD	MS
	XD CD#		
SP1	XD RDY	SD WP	MS CLK
SP2	XD RE#		MS INS#
SP3	XD CE#	SD D1	
SP4	XD CLE	SD D0	
SP5	XD ALE		MS D3
SP6	XD ME#	SD CD#	
SP7	XD WP		
SP8	XD D0	SD CLK	MS D2
SP9	XD D1		MS D0
SP10	XD D2	SD CMD	
SP11	XD D3		
SP12	XD D4	SD D3	MS D1
SP13	XD D5	SD D2	
SP14	XD D6		MS BS
	XD D7		

Share Pin

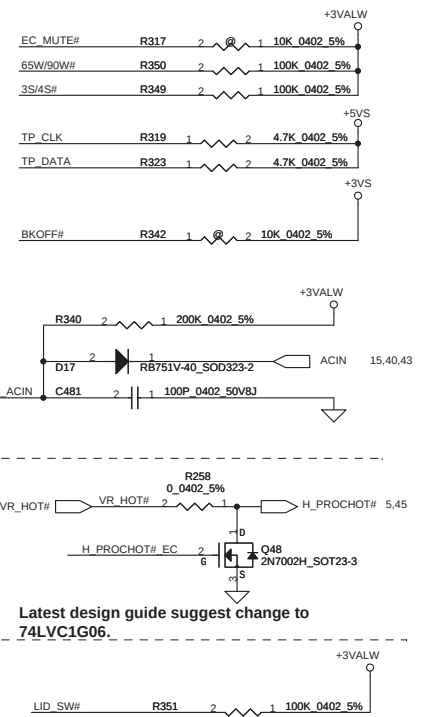
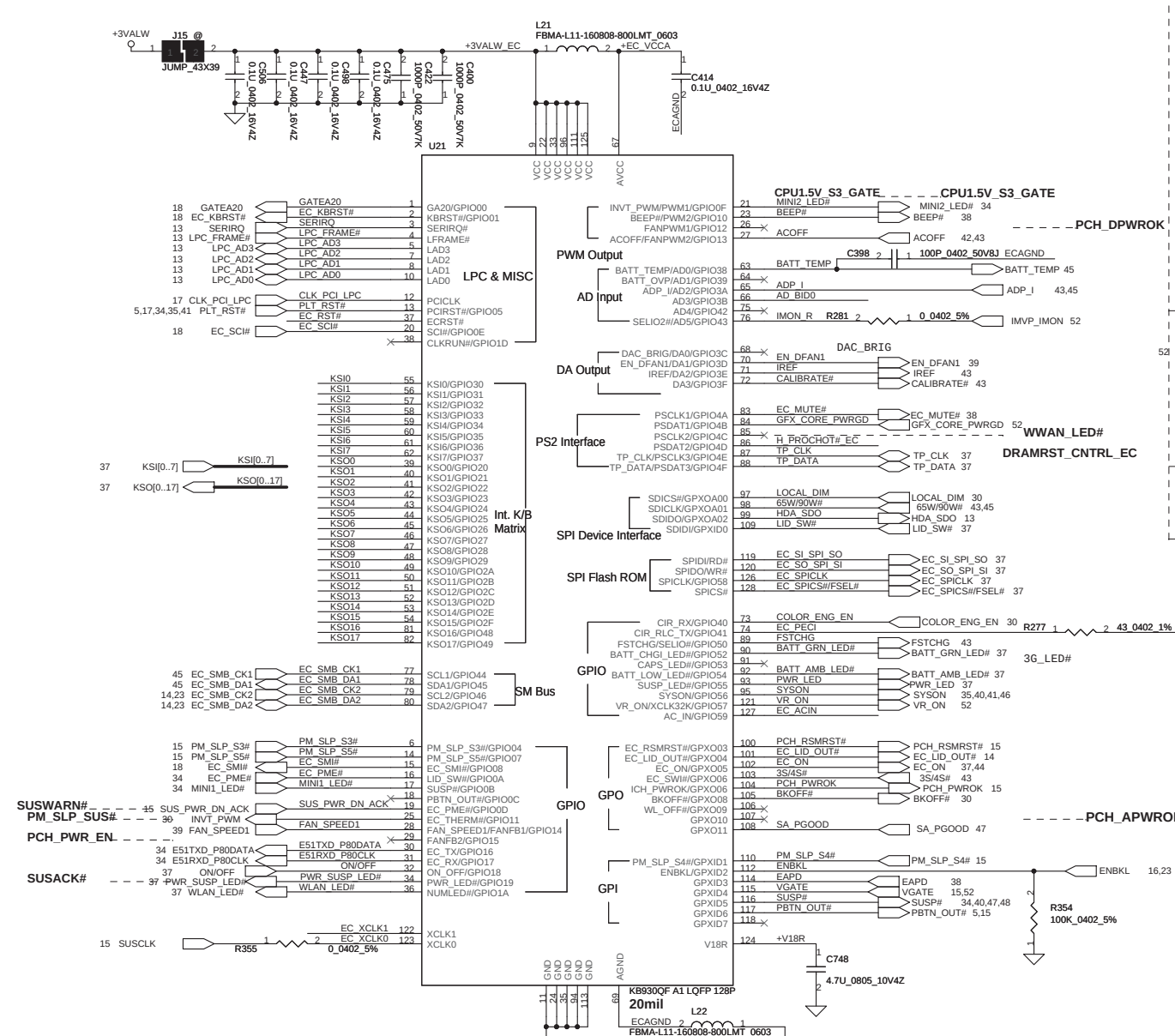
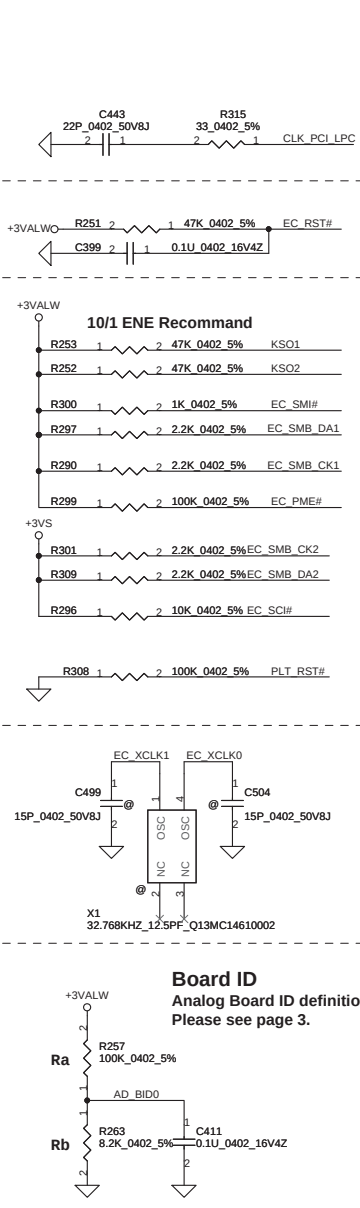


USB/B USB3.0 Conn.(USB3.0 SKU)

(Port 3)



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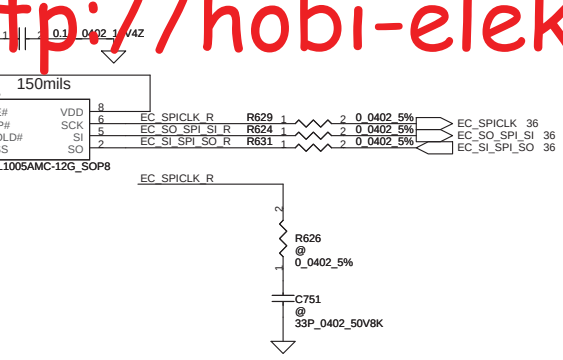
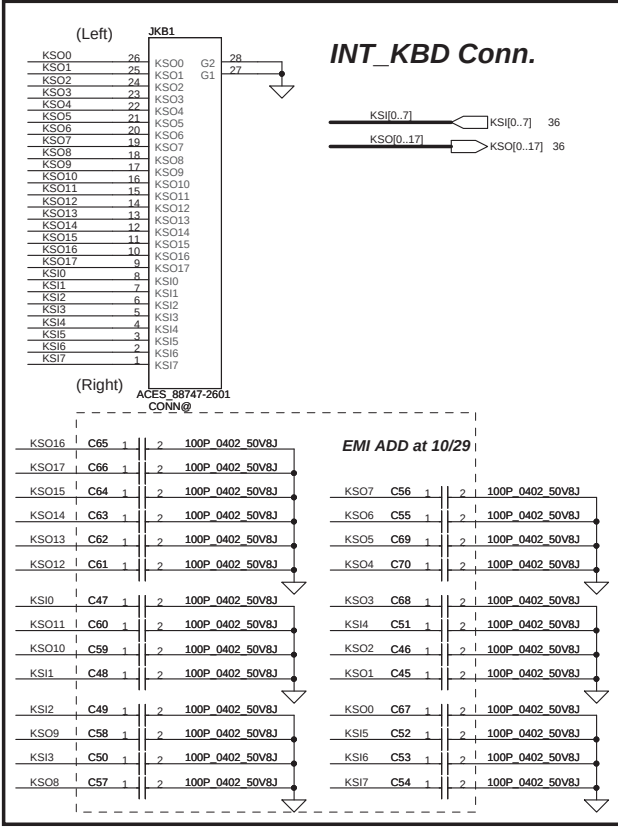


For EC Tools

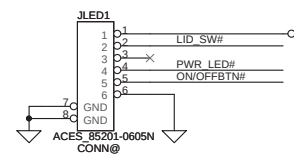
Place on RAM door

The diagram shows a connector labeled JP1 with pins 1 through 4. Pin 1 is connected to +3VALW. Pin 2 is connected to E51RXD_P80CLK. Pin 3 is connected to E51TXD_P80DATA. Pin 4 is connected to E51RXD_P80CLK 34 and E51TXD_P80DATA 34. The connector is labeled ACES_85205-0400.

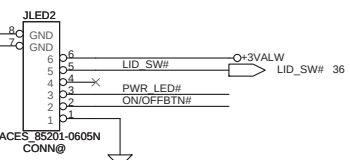
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C		D		Date:	Tuesday, November 09, 2010
				Sheet	36 of 60



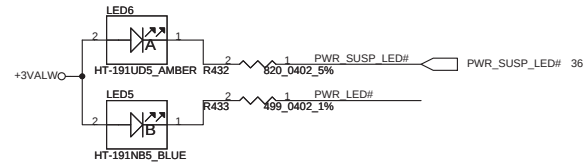
LED/B P7YE0/P7YH0 LS-6913P



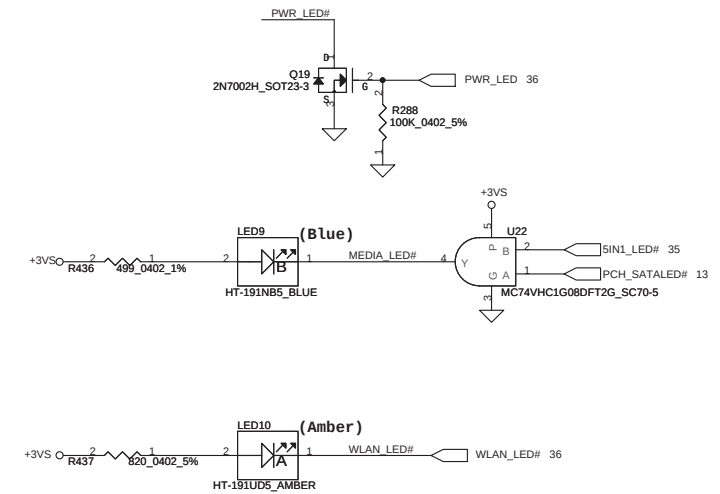
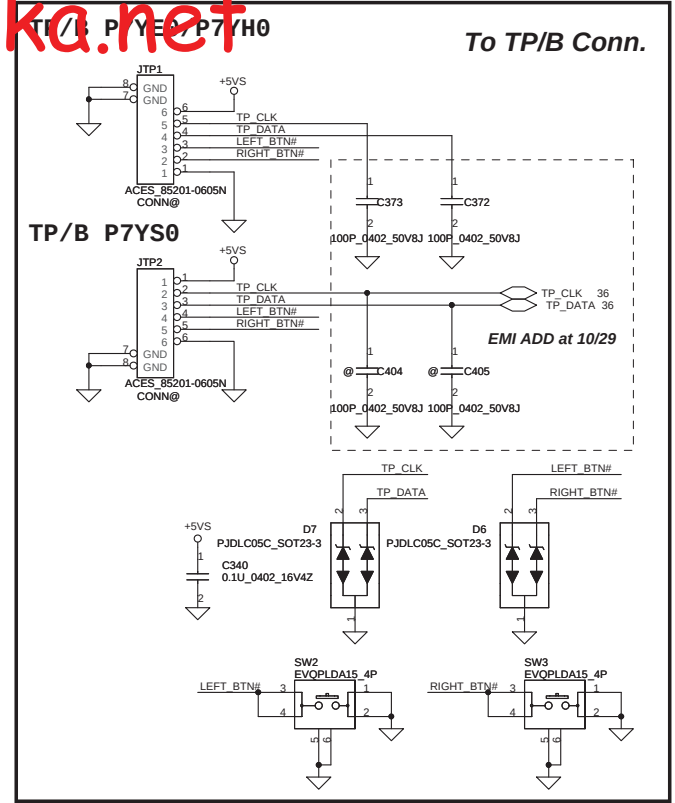
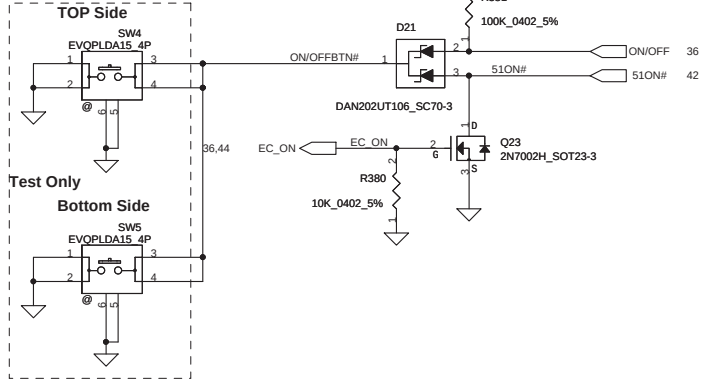
LED/B P7YS0 LS-6913P

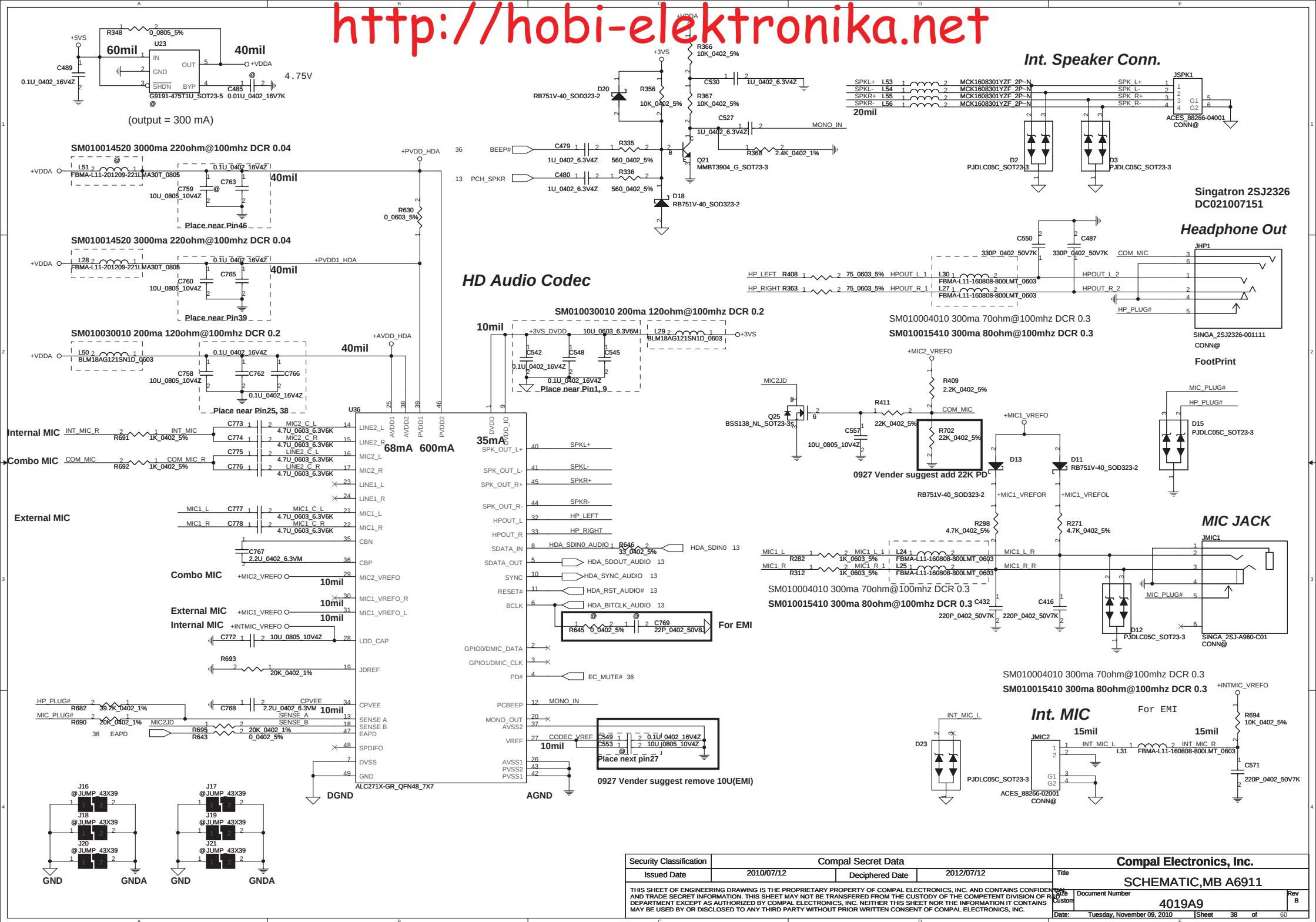


LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue		Blue	Amber		

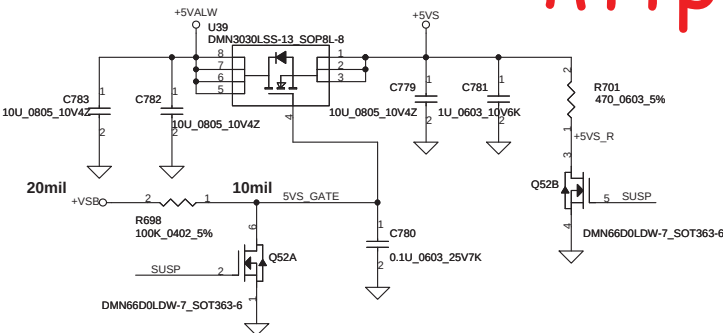


Power Button ON/OFF switch

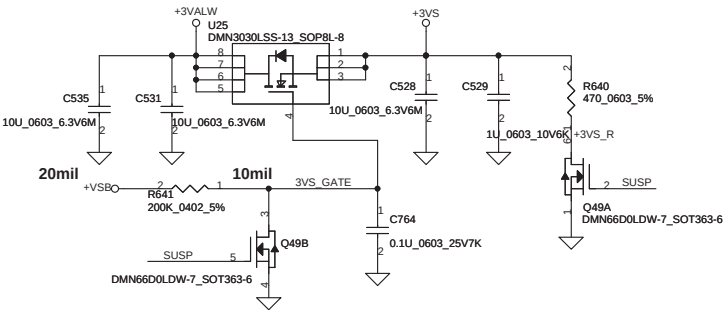




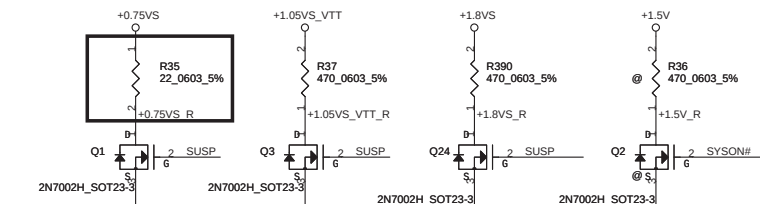
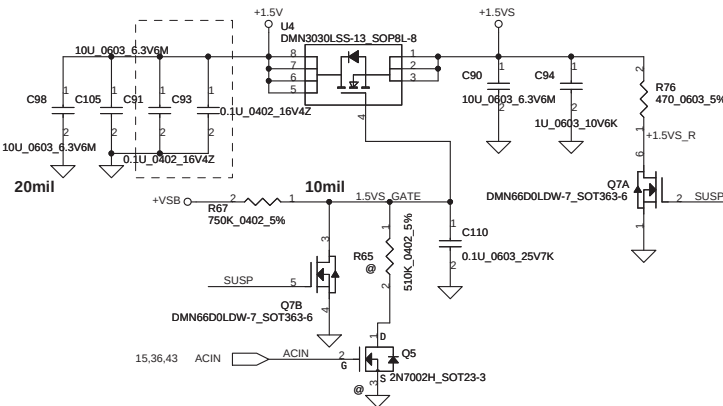
+5VALW TO +5VS



+3VALW TO +3VS

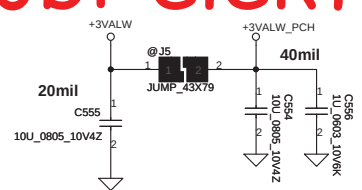


+1.5V to +1.5VS

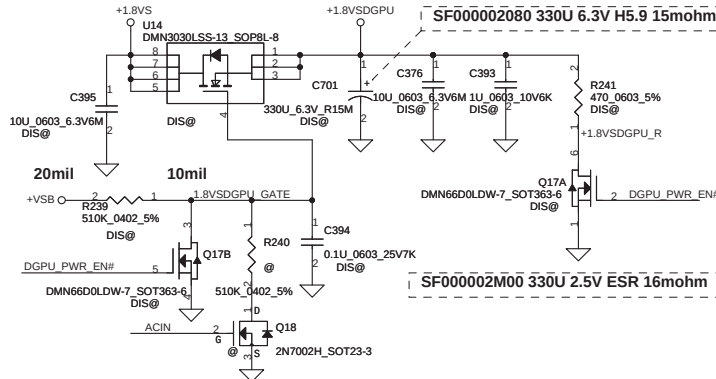


2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge

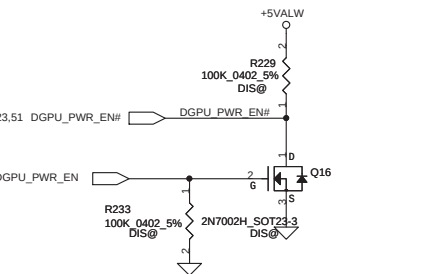
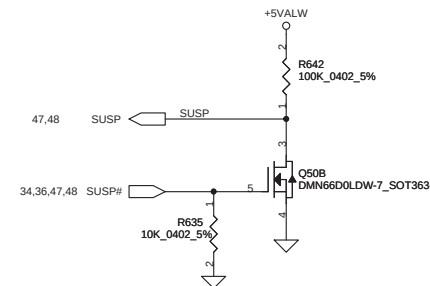
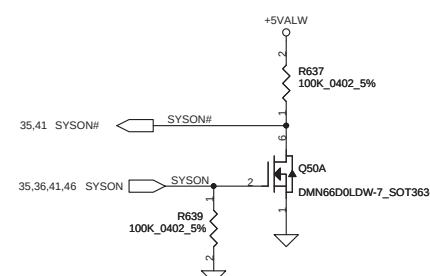
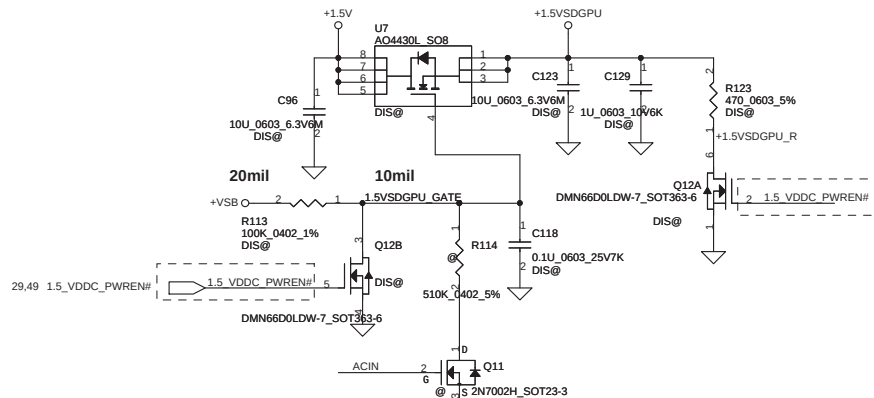
+3VALW TO +3VS_PCH (PCH AUX Power)



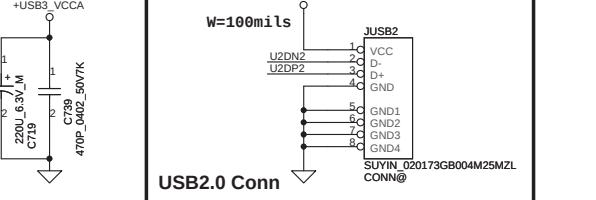
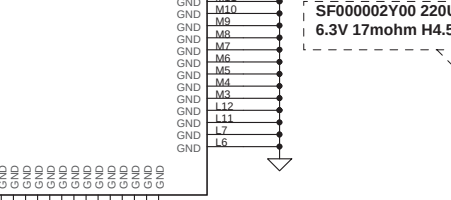
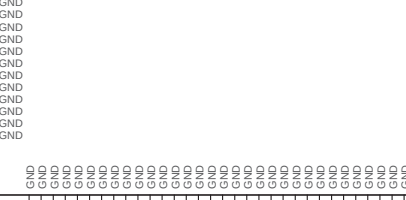
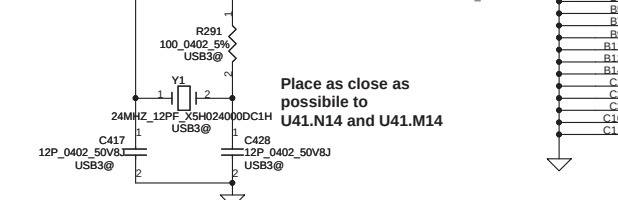
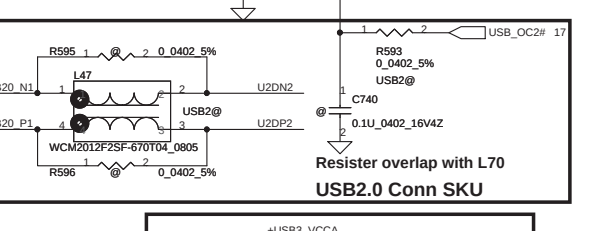
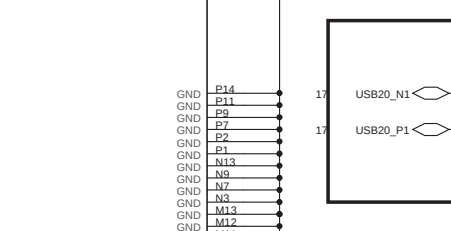
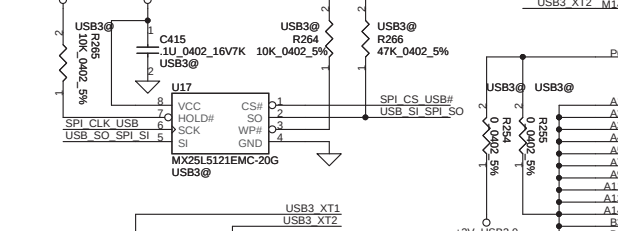
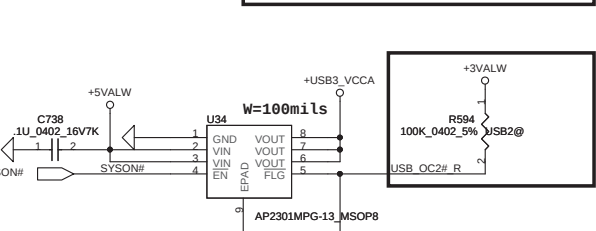
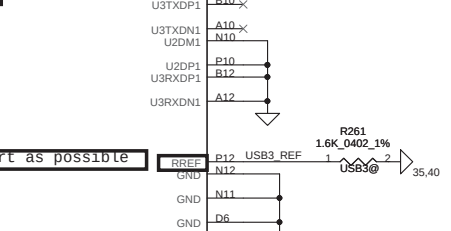
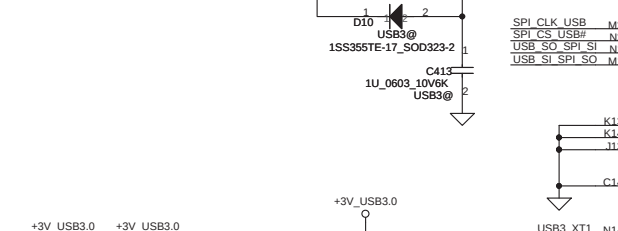
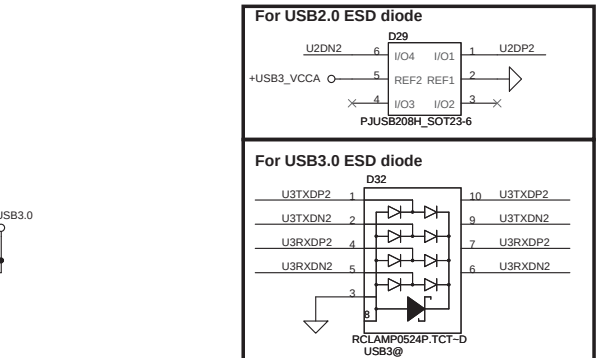
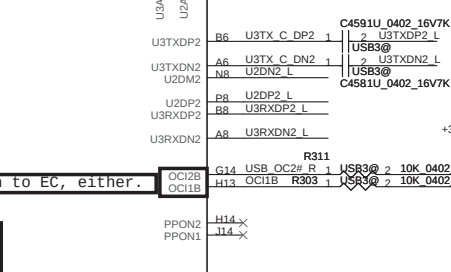
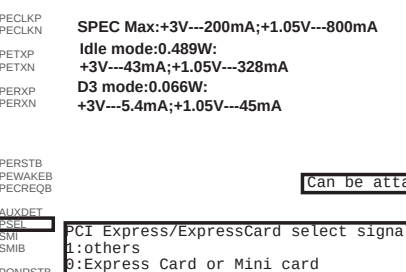
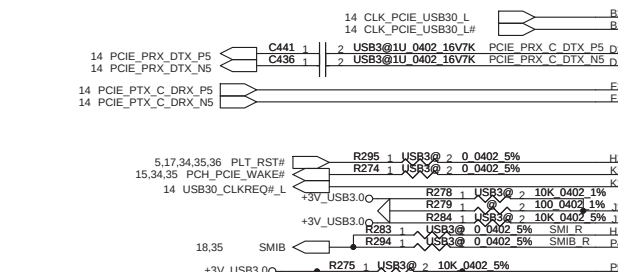
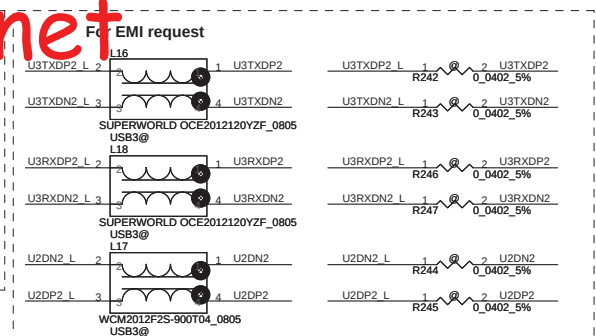
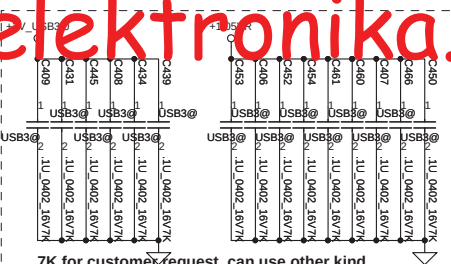
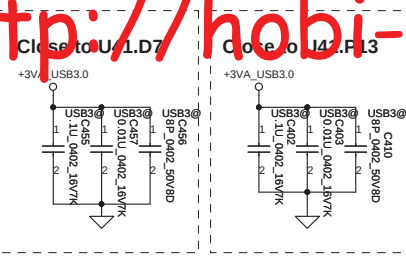
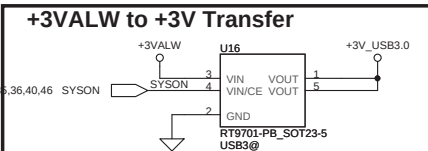
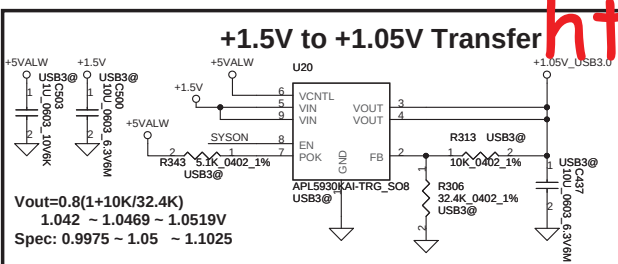
+1.8VS to +1.8VSDGPU for GPU



+1.5V to +1.5VSDGPU for GPU

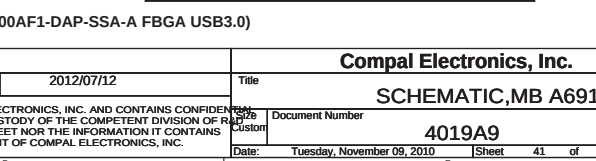
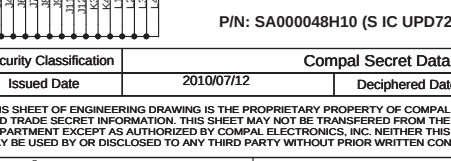
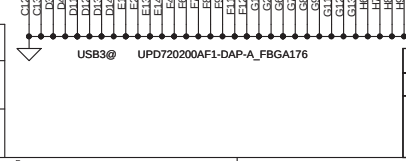


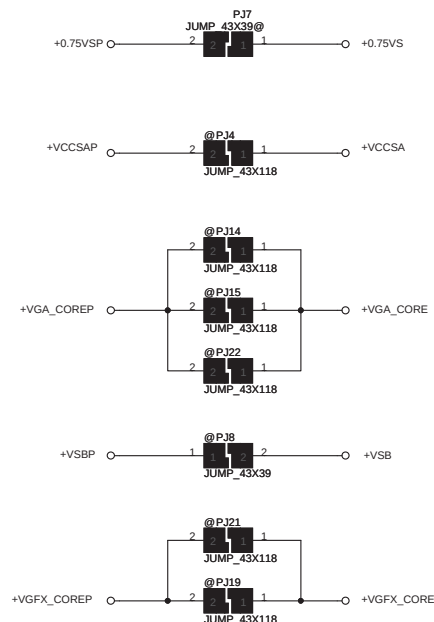
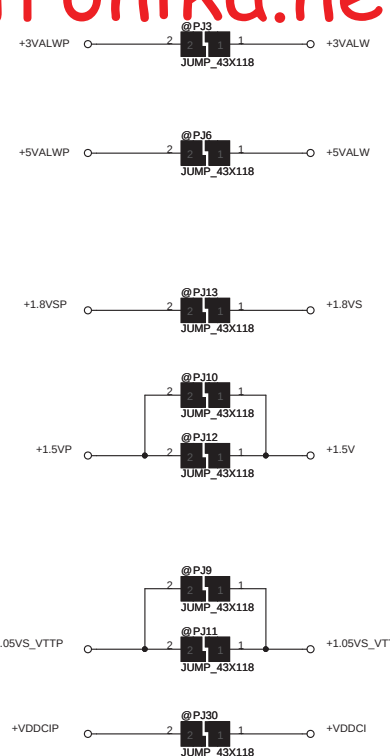
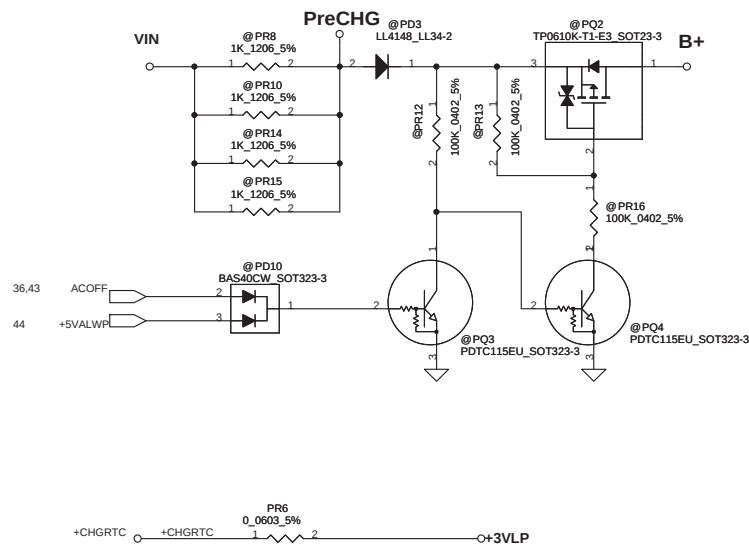
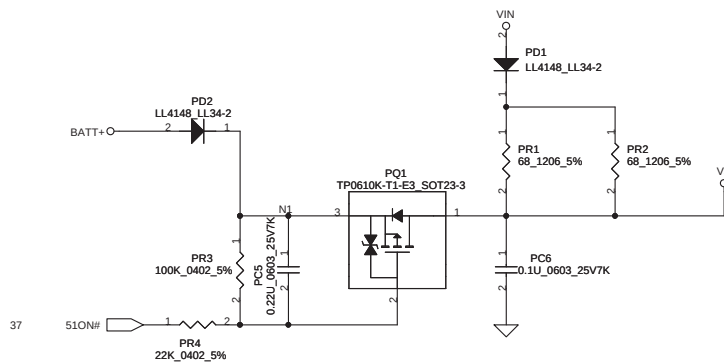
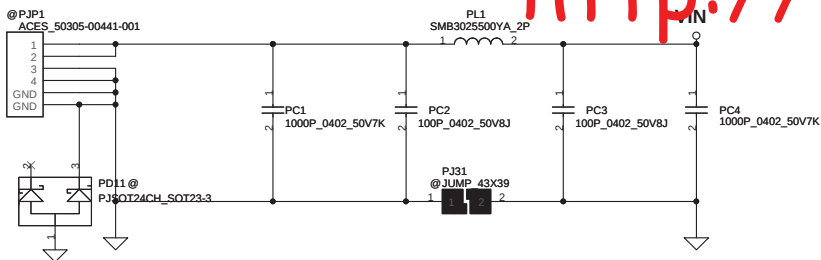
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										4019A9	
										Rev B	
										Date: Tuesday, November 09, 2010	
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Pin compare table for support USB remote wakeup or not

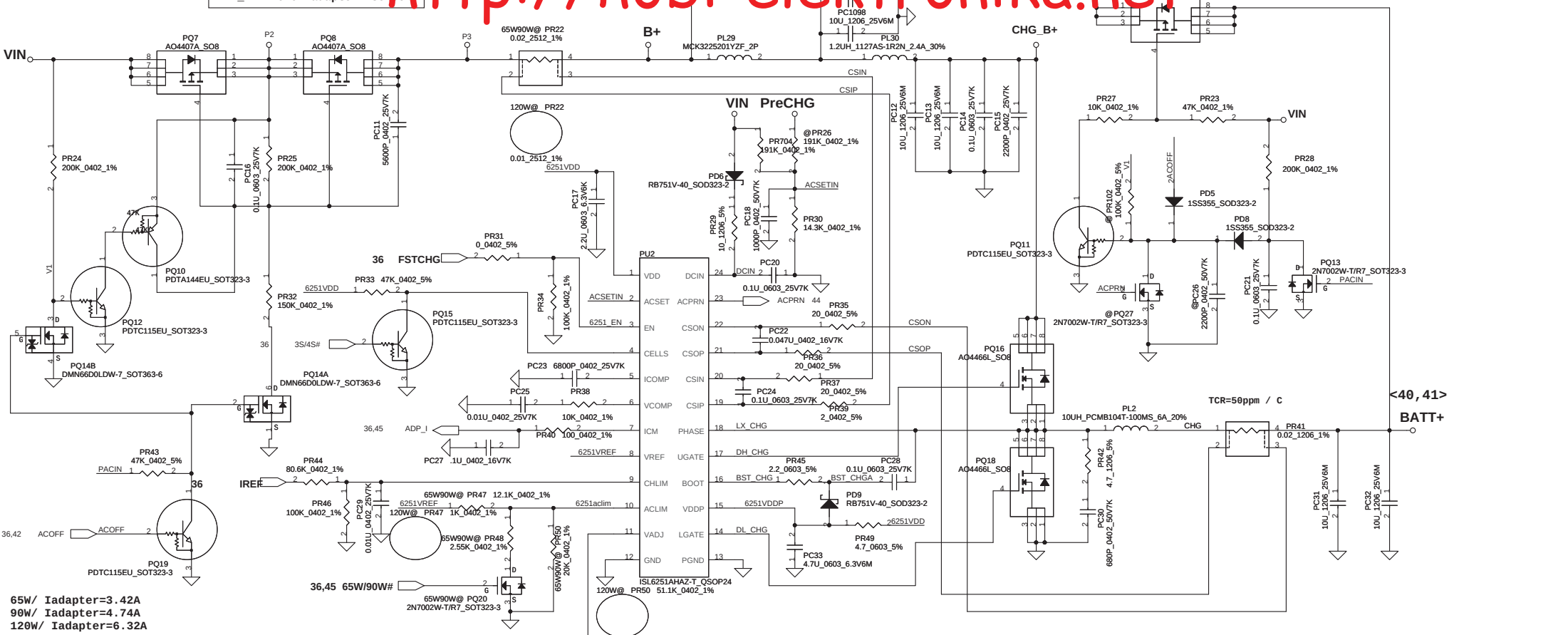
	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y5,R816,C879,C880
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25





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ADP_I = 19.9*Iadapter*Rsense



65W/ Iadapter=3.42A
90W/ Iadapter=4.74A
120W/ Iadapter=6.32A

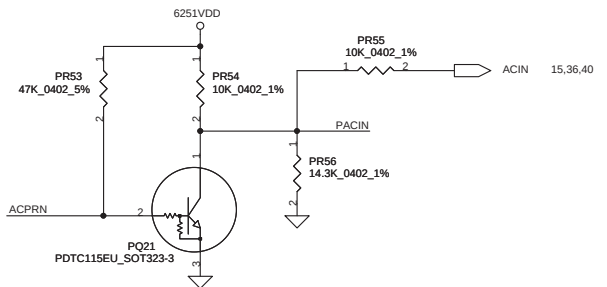
CP mode, for Acer spec, CP=0.85*Iadapter.
For 90W, 65W/90W#Low, Vref=2.39V
 $I_{input} = (1/0.02) (0.05 \cdot V_{acim} / 2.39 + 0.05)$
where $V_{acim} = 1.489V$, $I_{input} = 4.05A$

For 65W, 65W/90W#High
 $I_{input} = (1/0.02) (0.05 \cdot V_{acim} / 2.39 + 0.05)$
where $V_{acim} = 0.37V$, $I_{input} = 2.89A$

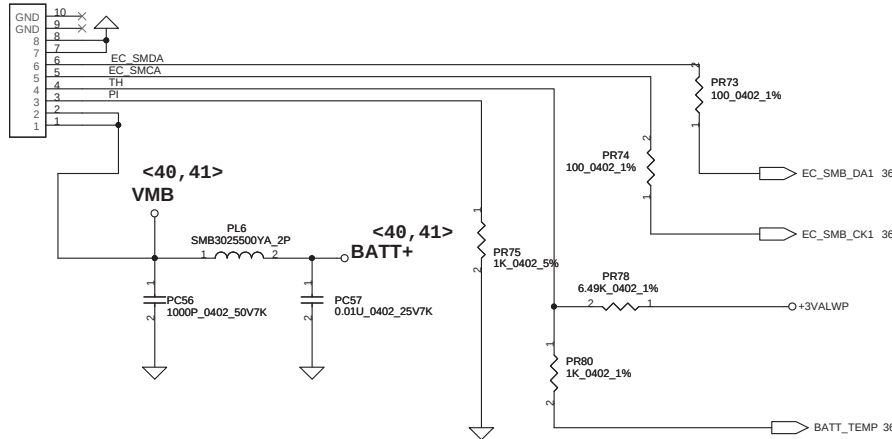
For 120W
 $I_{input} = (1/0.01) (0.05 \cdot V_{acim} / 2.39 + 0.05)$
 $V_{acim} = 2.344V$, $I_{input} = 5.403$

BATT Type	Charging Voltage (0x15)	CV mode	CC=0.6~4.48A
Normal 3S LI-ON Cells	12600mV	12.60V	IREF=0.7224*Icharge IREF=0.43V~3.24V

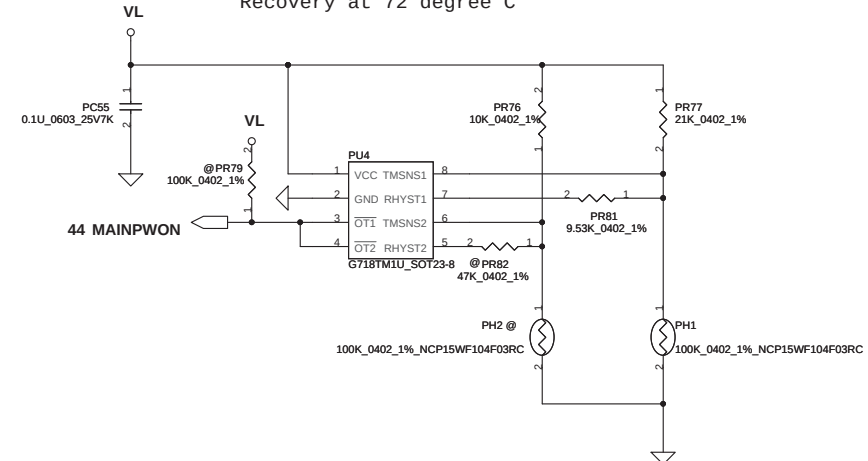
Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K
R2=PR381=31.6K
R=514K//31.6K/(15.4K+3K)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99V
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r+514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+0.175))*Kv/(4.2-(4.2+0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451



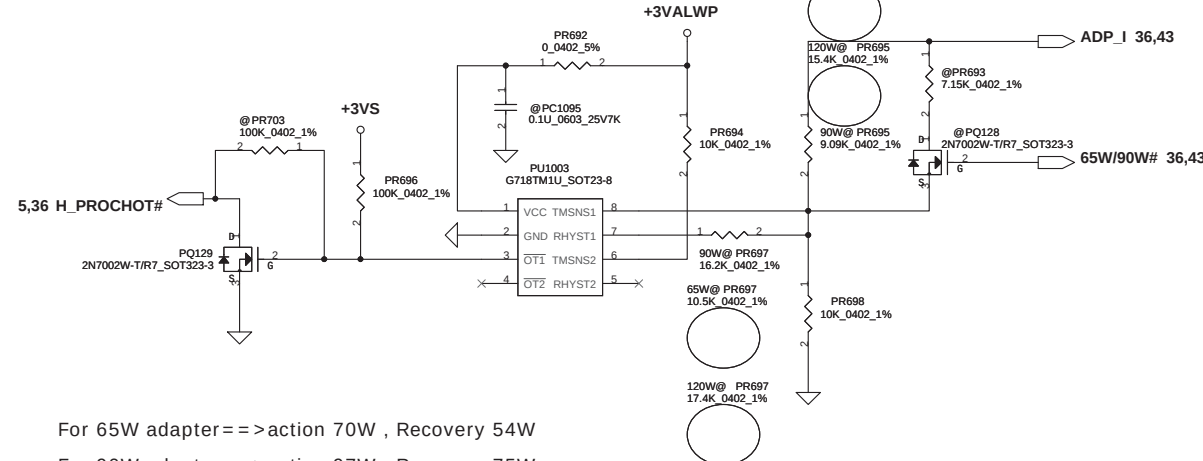
@P3P2
SUYIN_200275GR008G13GZR



PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 72 degree C

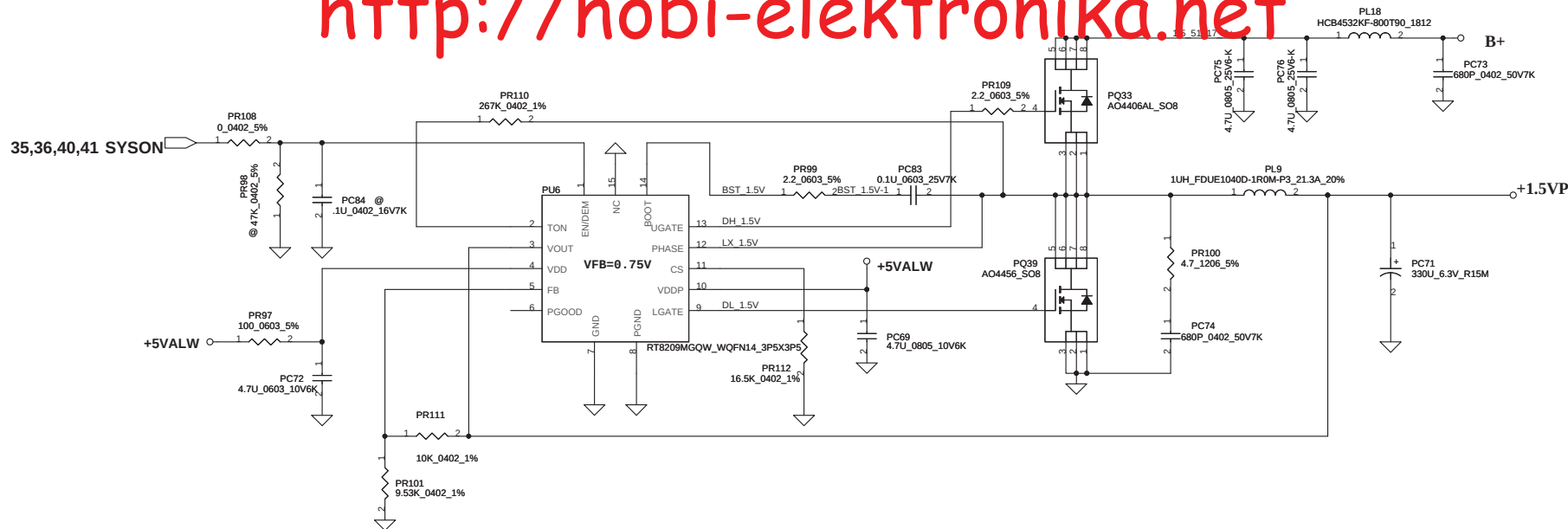


Change 5VALW to 3VALW on DVT



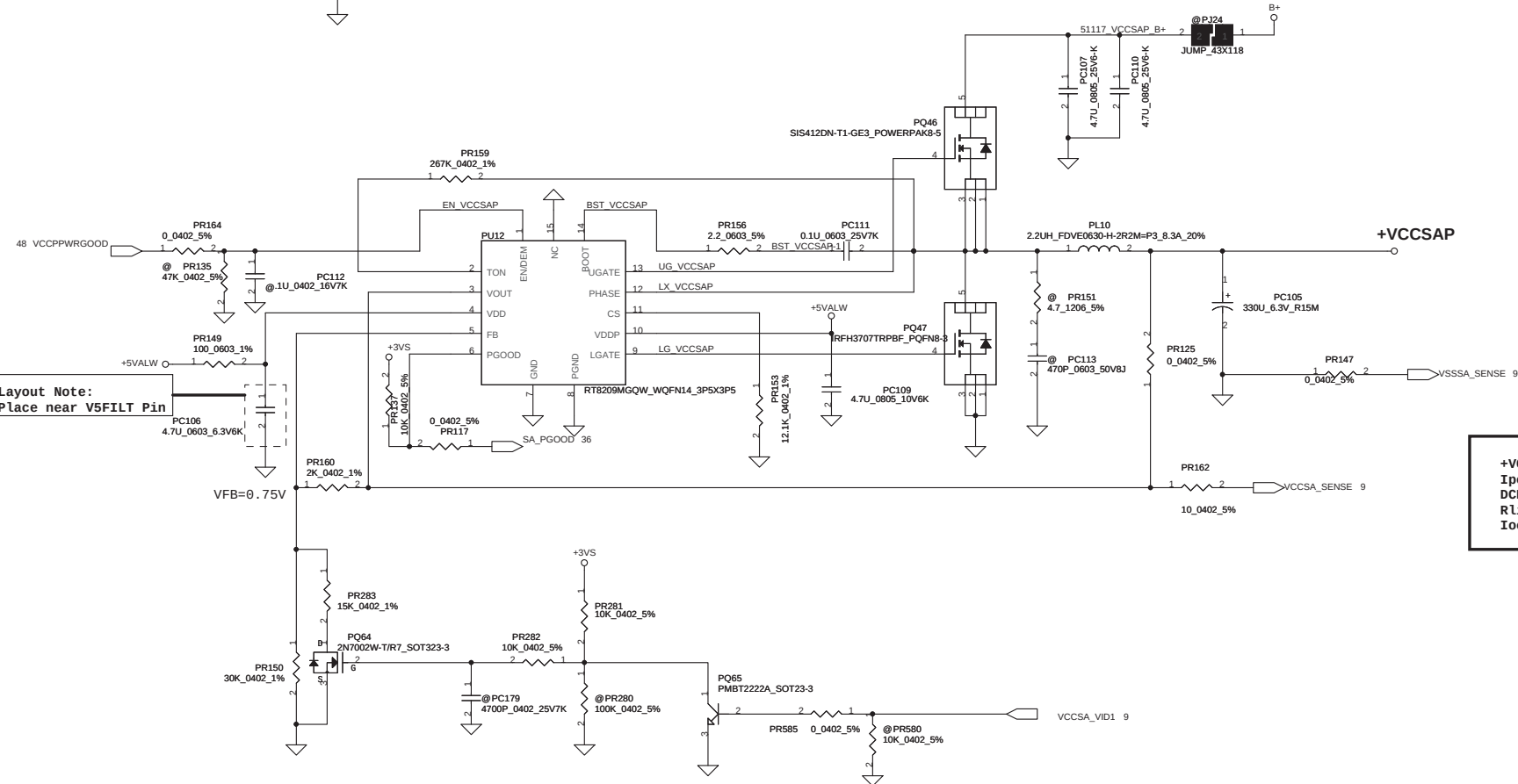
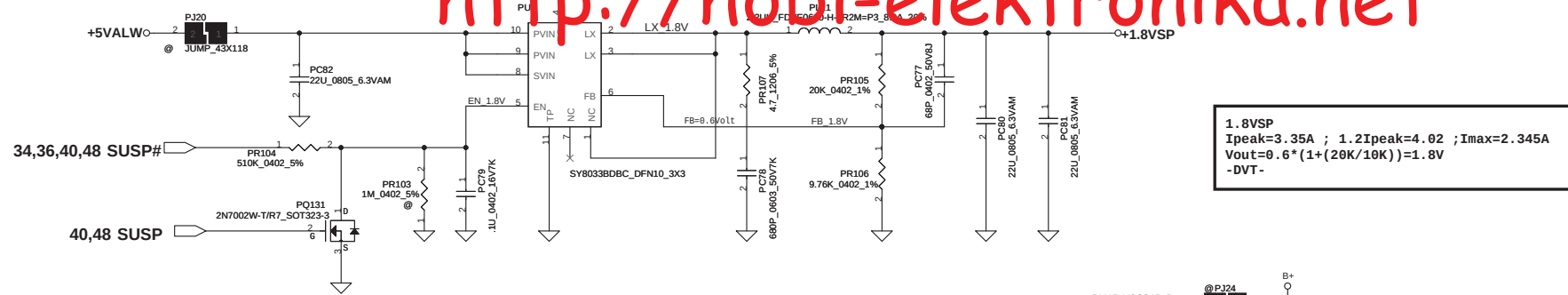
For 65W adapter==>action 70W , Recovery 54W
For 90W adapter==>action 97W , Recovery 75W
For 120W adapter==>action 135W , Recovery 100W

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+1.5VP
 $I_{peak}=21.56A$; $1.2I_{peak}=25.87A$; $I_{max}=15.09A$
 $R_{ton}=267K$, $F_{sw}=298KHz$, $R_{dson}=4.5-5.6mohm$
 $R_{trip}=16.5K$
 $I_{ocp}=25.97A-42.41A$

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				Rev	B



Layout Note:
Place near V5FILT Pin

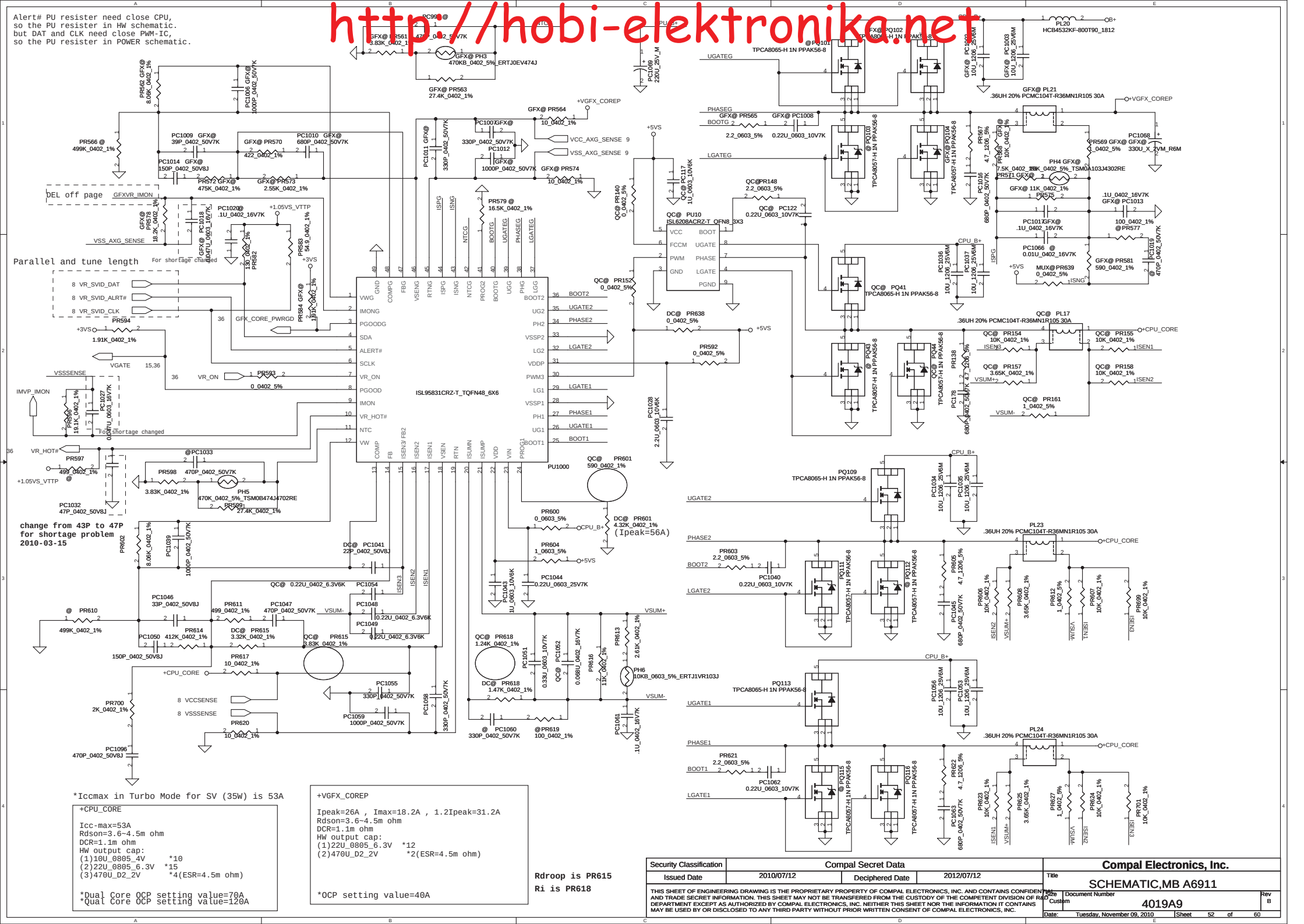
VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012	Required
0	0	0.9 V	Yes/Yes	
0	1	0.8 V	Yes/Yes	
1	1	0.75V	No/Yes	
1	1	0.65V	No/Yes	

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<http://hobi-elektronika.net>

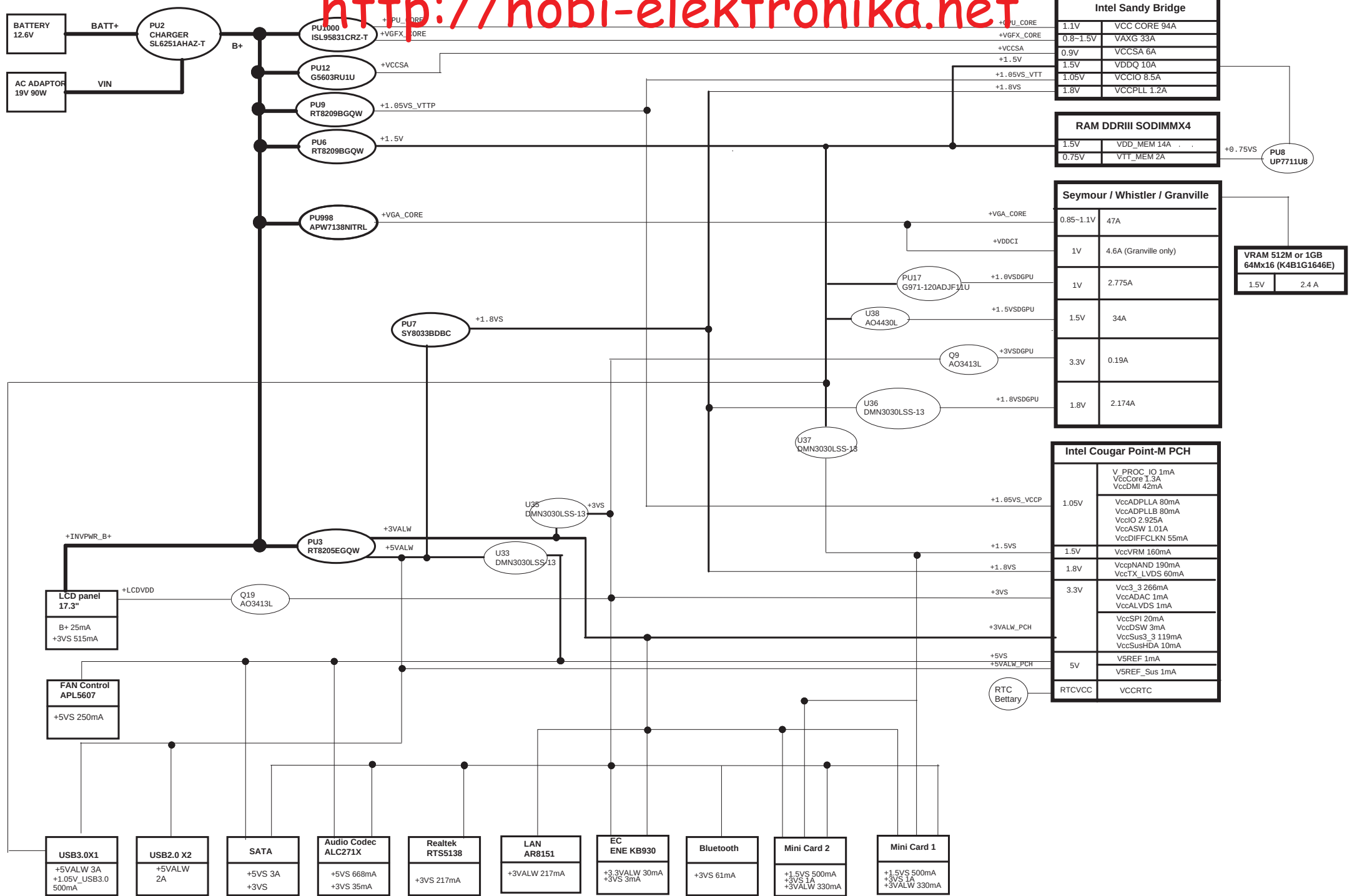
Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.

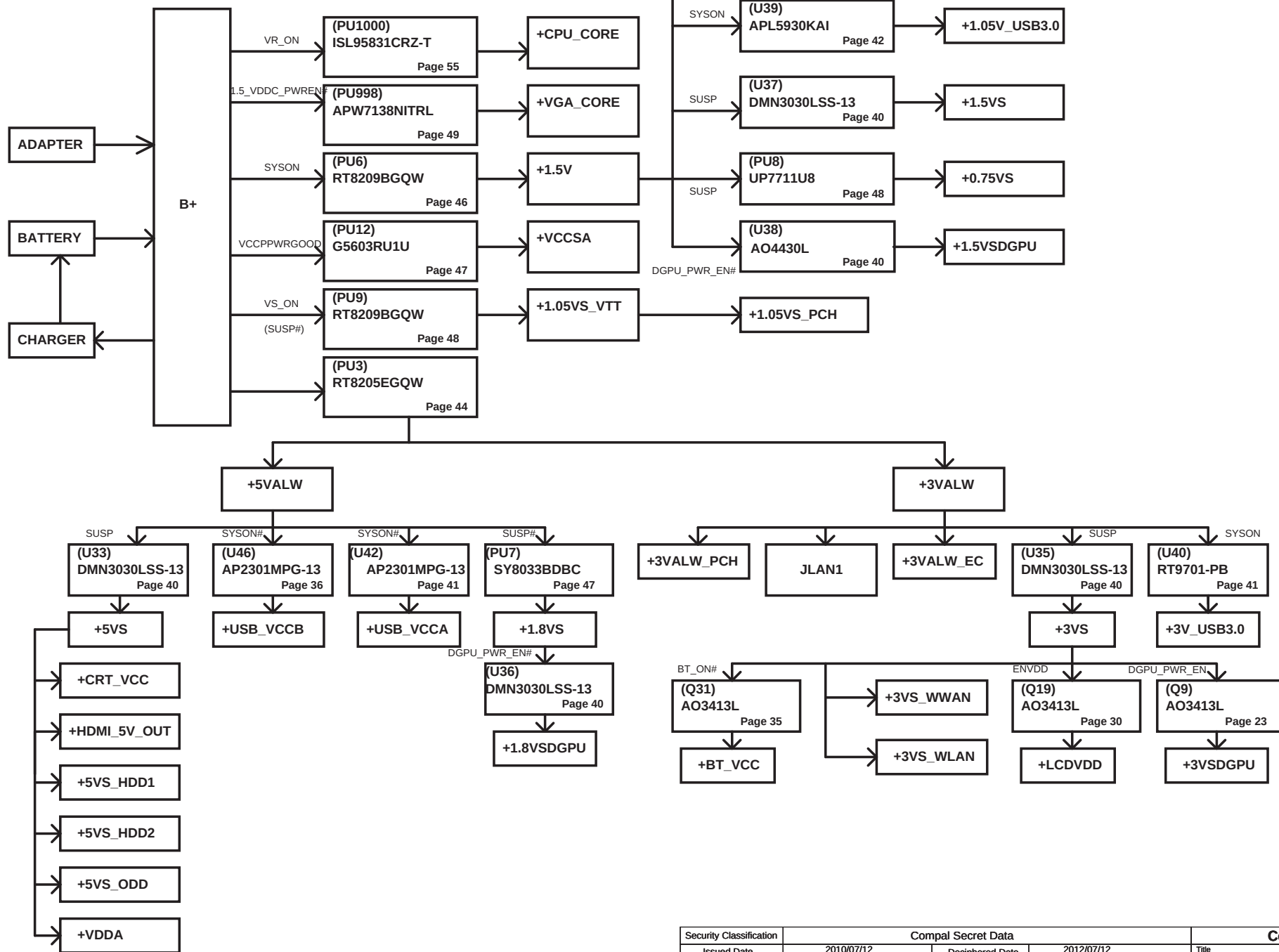


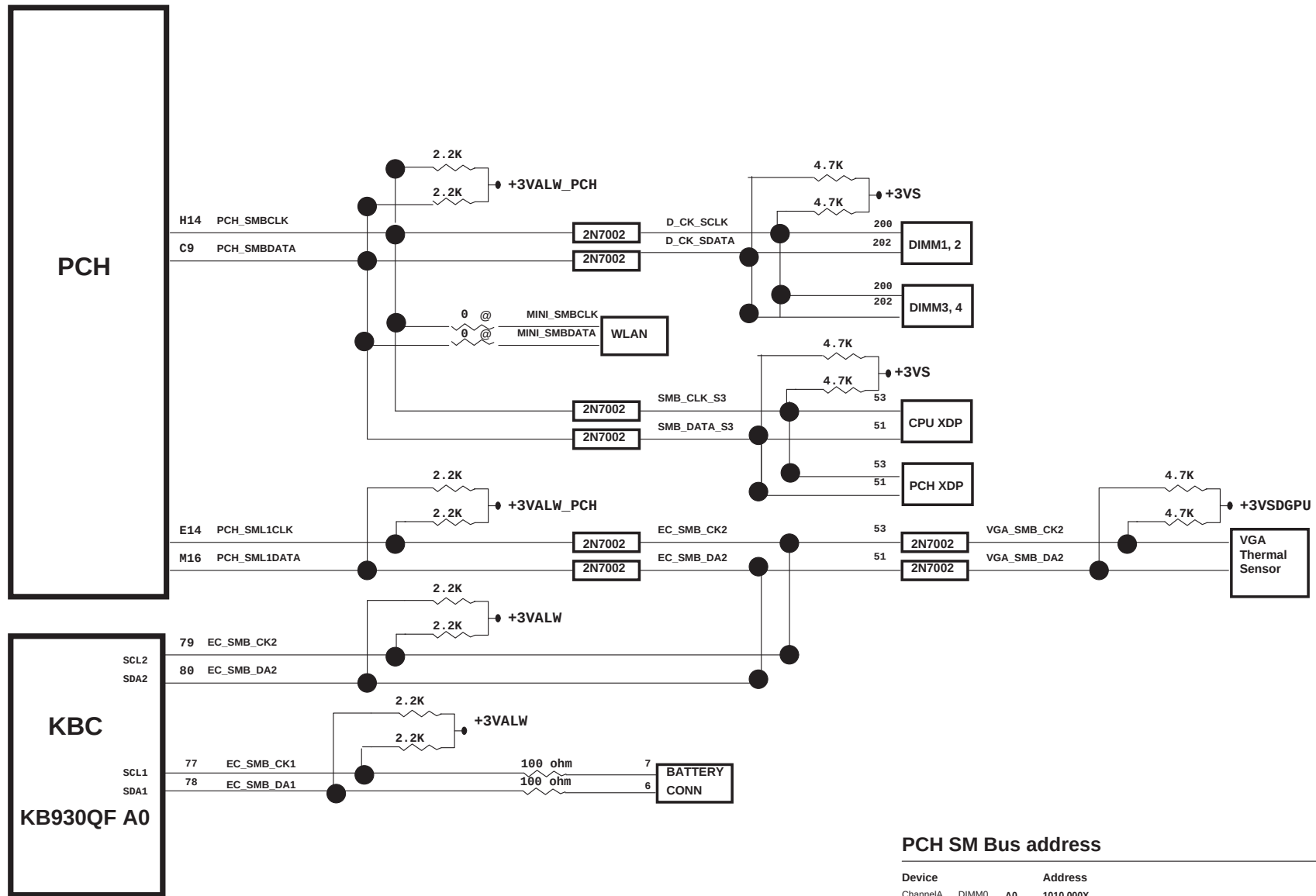
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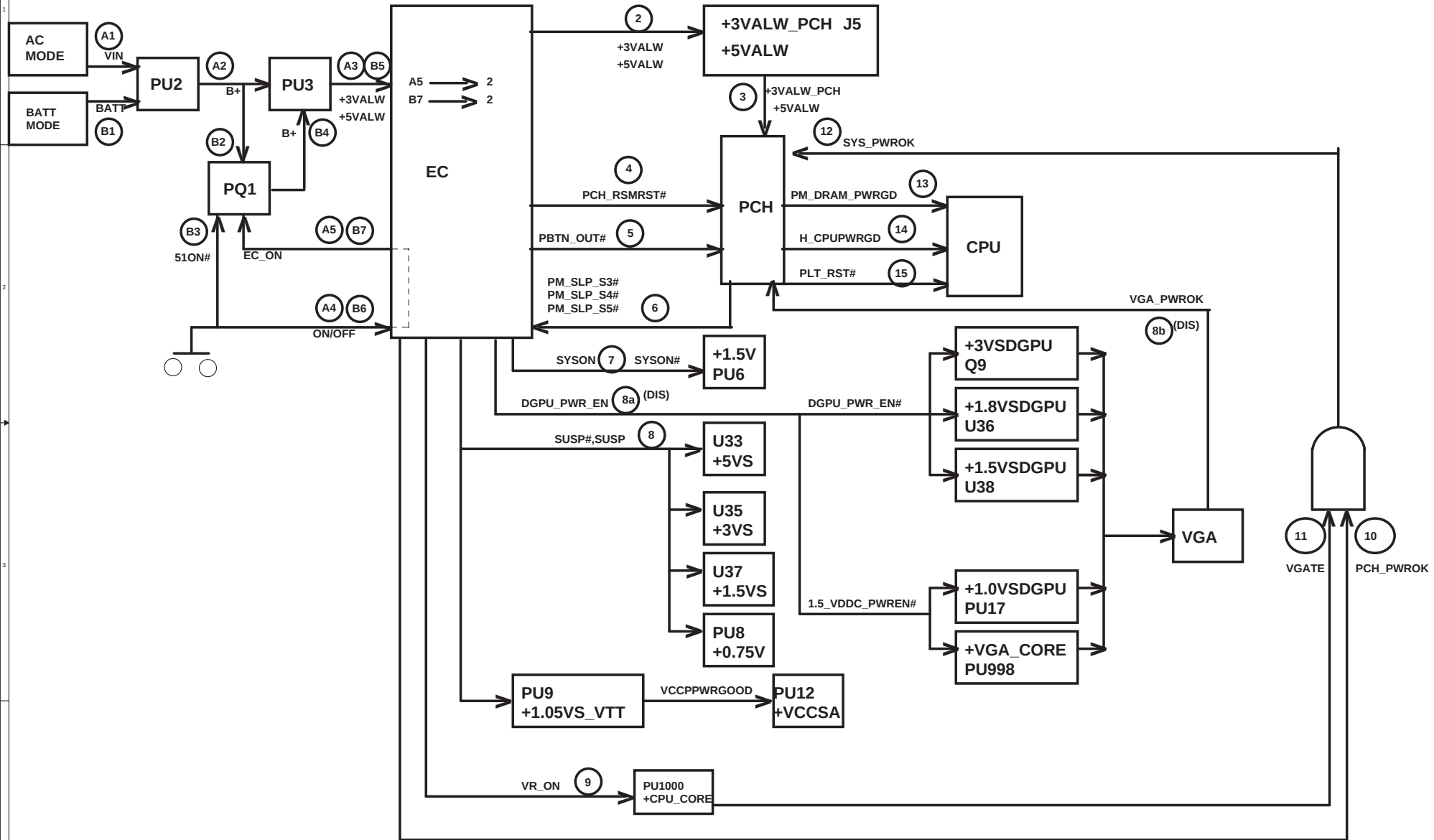
Item	Fixed Issue	Reason for change	Rev. PG#		Modify List	Date	Phase
1	HW increase 1.8V voltage.	HW need to increase 1.8V voltage.	0.1	47	Change PR106 from SD034100280 to SD034976180.	2010/09/23	DVT
2	VGA Granville OVP issue.	Because VGA has happened OVP issue in Granville SKU, that is caused by output capacitor too small. change PC1094 to SGA00004200 to solve it. PC1088 must remove.	0.1	49	Add PC1094 to SGA00004200 and delete PC1088 SF000002000.	2010/09/23	DVT
3	1.8V Power sequence adjust.	HW adjust 1.8V power sequence.	0.1	47	change PR104 from SD028100380 to SD028150380.	2010/09/23	DVT
4	0.75V Power sequence adjust.	HW adjust 0.75V power sequence.	0.1	48	Change PR127 from SD028150380 to SD034267380.	2010/09/23	DVT
5	adjust +1.05VS_VTT power sequence	HW adjust +1.05VS_VTT power sequence	0.1	48	Change PC99 from SE107475K80 to SE076104K80.	2010/09/23	DVT
6	adjust +VDDCI power sequence	HW adjust +VDDCI power sequence	0.1	50	Change PR644 from SD034301380 to SD034100280.	2010/09/23	DVT
7	HW request to delete PR103.	HW request to delete PR103.	0.2	47	Delete PR103 SD028100480.	2010/09/28	DVT
8	PR104 BOM error.	PR104 BOM error for power sequence.	0.2	47	Change PR104 from SD034150380 to SD034510380.	2010/09/28	DVT
9	PR669 BOM error for Seymour only.	PR669 BOM error for Seymour only.	0.2	49	Chnage PR669 from SD034681180 to SD034590180.	2010/09/28	DVT
10	To same as P5WE0 VCCSAP choke.	To same as P5WE0 VCCSAP choke.	0.2	47	Change PL10 from SH000009Q00 to SH00000M700.	2010/09/28	DVT
11	HW request to add PQ130 and PQ131 to speed up to 放电.	HW request to add PQ130 and PQ131 to speed up to 放电.	0.3	47 48	Add PQ130 and PQ131 SB000006800.	2010/10/05	DVT
12	Remove chargeable RTC battery.	We reserve chargeable RTC battery to prevent over heat issue, Thermal team result is pass, so remove chargeable RTC battery.	0.3	42	Delete PR691 SD013000080 Change PR6 from SD013560080 to SD013000080.	2010/10/05	DVT
13	Chnage PL4 and PL5 to TOKO new part.	Chnage PL4 and PL5 to TOKO new part.	0.3	44	Change PL4 and PL5 from SH000006J80 to SH00000MB00	2010/10/05	DVT
14	for ISN issue.	for ISN issue.	0.3	43	Add PL30 SH000009Q00. Delete PL28 SM010018210	2010/10/05	DVT
15	to same as P5WE0 choke.	to same as P5WE0 choke.	0.3	47	Change PL10 and PL11 from SH000009Q00 to SH00000F800	2010/10/05	DVT
16	for QC+25WGPU and QC+35W GPU change CP point.	Becasue Acer deine QC with 25W/35W GPU to be 120W SKU, change CP point to meet Acer request.	0.3	43	Delete PQ20 SB000006800. Delete PR48 SD034255180 Change PR22 from SD000001F00 to SD021100b80.	2010/10/05	DVT
17	for QC+25WGPU and QC+35W GPU change CP point.	Becasue Acer deine QC with 25W/35W GPU to be 120W SKU, change CP point to meet Acer request.	0.3	43	Change PR47 from SD034121280 to SD034100180 Change PR50 from SD034200280 to SD034511280	2010/10/05	DVT
18	Modify adapter throttling at turbo mode setting point.	Modify adapter throttling at turbo mode setting point.	0.3	45	Add PR695 SD034154280 Add PR697 SD034174280	2010/10/05	DVT
19	CPU Transient responds issue.	Change CPU transient reponds RC time constant.	0.4	52	Add PC1052 SE000003J80. Add PC1096 SE071471J80. Add PR700 SD034200180.	2010/10/07	DVT
20	for ISN issue.	for ISN issue.	0.4	43	Change PL30 from SH000009Q00 to SH00000M700.	2010/10/07	DVT
21	Make BOM same as P5WE0.	Make BOM same as P5WE0.	0.4	52	Change PL21,PL23,PL24 from SH000005680 to SH00000HK00.	2010/10/07	DVT
22	BOM loss.	Because BOM Config loss 65@ and 90W@, so miss PR695 and PR697.	0.5	45	Add PR695 SD034909180 9.09K_0402_1% ADD PR697 SD034162280 16.2K_0402_1%	2010/10/26	PVT
23	Modify CPU OCP.	Becuae original design is for 3 phase DC, now change to 2 phase DC, so modify OCP.	0.5	52	Chnage PR618 from SD034698080 to SD000009480	2010/10/26	PVT
24	Modify DC LL.	Because DC OCP was modified, must also update LL of DC.	0.5	52	Chnage PR615 from SD034215180 to SD034332180	2010/10/26	PVT

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PCB

LA-6911P MB Rev0: DA80000LC00
LA-6911P MB Rev1: DA80000LC10
LA-6911P MB with Small Board Rev1: DAZ
LA-6911P REV0 MB

VGA

Granville PRO M2 A12:
SA00004C820(S IC 216-0769024 A12 GRANVILLE PRO ABO!)

WHISLER PRO M2 A11:
SA00004C720(S IC 216-0810005 A11 WHISTLER PRO FCBGA 962P ABO !)

X76

X761@ X76264BOL01 VRAM 512M SAM P7YE0
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)

X762@ X76264BOL02 VRAM 512M HYN P7YE0
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)

X763@ X76264BOL03 VRAM 1G SAM P7YE0
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)

X764@ X76264BOL04 VRAM 1G HYN P7YE0
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)

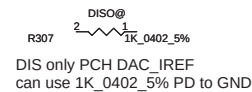
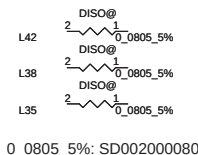
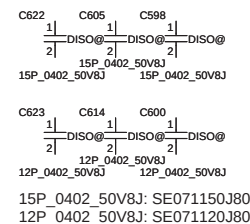
X765@ X76264BOL05 VRAM 2G HYN P7YE0
Hynix : SA00003VS10 (S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABO!)

X766@ X76264BOL06 VRAM 2G SAM P7YE0
Samsung : SA00003MQ60 (S IC D3 128M16 K4W2G1646C-HC12 FBGA ABO!)

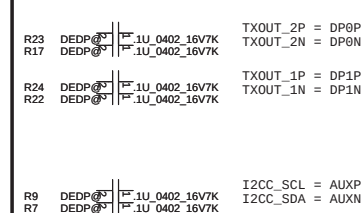
X767@ X76264BOL07 VRAM 1G SAM P7YE0
Samsung : SA00003MQ60 (S IC D3 128M16 K4W2G1646C-HC12 FBGA ABO!)

X768@ X76264BOL08 VRAM 1G HYN P7YE0
Hynix : SA00003VS10 (S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABO!)

CRT Option Components



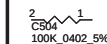
DIS EDP Option Components



Granville VGA_CORE CAP Option



EC susclk/crystal Option Components



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09023:
network
ADD Q8 DMN66D0LDW-7(SB00000D0H0) & change BOM structure to DIS0(DIS0 Granville can't power on issue)
R72 100K_0402_5%(SD028100380)change BOM structure to DIS0(DIS0 Granville can't power on issue)
R674 4.7K PH change BOM structure to @(+3VS GPIO19 leakage)
D31 change BOM structure to @(EC debug CLK leakage)
R531,R530 change BOM structure to DIS0(HSYN:VSYNC 11: Audio for both DisplayPort and HDMI)
ADD C591 C604 BOM option
(Seymour/Whistler option NOGRAN@ SGA20331E10 S POLY C 330U 2V 9mohm H1.9)
(Granville option GRAN@ SGA00004200 S POLY C 470U 2V M D2 LESR4.5M SX H1.9)
C746,C750 change from SF000001500 to SF000001500

Power sequence:
1. BOT (adjust +5VS power sequence)
R698 change from 200K to 100K_0402_5% (SD028100380)
2. BOT (adjust +1.8VS power sequence)
PR104 change from 100K to 510K_0402_5%(SD028510380)
remove PR103 1M_0402_5%
3. TOP (adjust +1.5VS power sequence)
R67 change from 510K_0402_5% to 750K_0402_5%(SD028750380)
4. TOP (adjust +0.75VS power sequence)
PR127 change from 150K_0402_5% to 267K_0402_1%(SD034267380)
5. TOP (adjust +1.05VS_VTT power sequence)
PC99 change from 4.7U to .1U_0402_16V7K (SE076104K00)
6. TOP (adjust +1.5VSDGPU power sequence)
R113 510K change to 100K_0402_1% (SD034100380)
7. BOT (adjust +VDDCI power sequence)
PR644 301K change to 10K_0402_1% (SD034100280)

Power:
PR101 change from 10K to 9.53K (adjust +1.5V power)
PR106 change from 10K to 9.76K (adjust +1.8VS power)
Layout:
D21 channg to SC600000B00 (for sourcer 2nd source)
DEL C590,C603 (DEL colay Cap)
L24,25,27,30,31 change from SM010004010 to SM010015410
BATT Blue light place at front side
H1 change H3P0 to H4P6
DEL LED1,LED2,LED3,LED4

0924:
Q37,Q39,Q40,Q41, change from SB00000FG00 to SB00000FG10
U7 change from SB000007000 to SB000007010
USB3.0 schmetic change to unpop
XDP change to unpop
U19 A10,N10,P10,B12 connect to GND

0925:
R249 change from U15.2 to U15.1(footprint issue)
R105 change form 10K to 10_0402_5%(SD028100A00)
R422 change BOM structure to @(crystal issue debug port1.2)
R422 change +3VS to +3VALW_PCH (GPIO28)
R674 change BOM structure to @(leakage issue debug port1.2)
R674 change +3VALW_PCH to +3VS (GPIO19)
ADD LED11 pop WLAN_LED#(SC500007700) LED12 @ MEDIA_LED#(SC591NB5A30)
LED10 WLAN_LED#(SC500007700) change BOM structure to @
DEL D9,D10 USB3.0 old ESD diode
ADD D32 new USB3.0 ESD diode (SC300001D00)
DEL R238,R250,C401 USB3.0 conn PD resistor & CAP
EMI request:
R595,R596 change to @ L47 change to POP(USB2.0 common mode choke)

0927:
Audio vender suggest:
C913 change BOM structure to @
ADD C702 22K_0402_5%(SD028220280)
change USB conn to USB2.0(SUYIN_020133GB004M25MZL_4P-T)
modify Debug port note(GPIO19 PH +3VS GPIO28 PH +3VALW_PCH)
R667,R666 change BOM structure to @(XDP CLK source)
change SW4,SW5 BOM structure to @ (debug PWRBTN)
change R432,R435,R437 from 1K_0402_5% to 300_0402_5%(orange LED resistor)
change USB3.0 schmetic BOM structure back to USB30
C746,C750 change from SF000001500 to SF000001500
D4,D5 change from SCSH491D010(S SCH DIO CH491DPT SOT-23) to SCS00002000(S SCH DIO RB491D SOT-23 PANJIT)
Q29,Q33,Q36 change from SB934130020(S TR A03413L 1P SOT23-3) to SB000006R10(S TR A03419L 1P SOT23-3)

0928:
DEL R468
JMINI1.24 change power source from +3VS to +3VS_WLAN
DEL R613
JMINI2.24change power source from +3VS to +3VS_WMAN
DEL R352
change power source from +XDPWR_SDPWR MSPWR to +CARDPWR
Q21 change from SB324110080(2SC2411K) to SB039040020(MMBT3904)
Change JUSB2 footprint to "SUYIN_020173GB004M25MZL_4P"
ADD R613 1M PD to GND(HDA_SYNC_PCH_R)
ADD SLP_A# at U37.G10 test point(for DFT request)
ADD JTAG_TDI at U30.AN23 test point(for DFT request)
ADD JTAG_TDO at U30.AM24 test point(for DFT request)
JREA01 change conn from TAITW_R013-P12-HM_44P_NR to TAITW_R013-P17-HM_40P_NR

0929:
E Rechangeable PCH schmatic R424,C591
0930:
R534,R540 change from 100_0402_1% to 1K_0402_5%(SD028100180)(DG1.5 change save cost)
C744,C745 change from 18P_0402_50V8J to 27P_0402_50V8J(SE071270J80)(25Mhz Crystal modify)
R357,R358,R330,R331,R345,R346,R387,R393,R292 change BOM structure to @ (10K_0402_5%)PD to GND(DG1.5 unuse CLK NC)
R666,R667 change BOM structure to @(XDP unuse)
R573,R575,R571,R572,R562,R566,R567,R570 DEL option 499_0402_1% leave 680_0402_5%
R318,R332 change from 0ohm to 22_0402_5%(SD028220A80)
C448,C483 change to 4.7P_0402_50V8J(SE07147AC80)
L47 change to 670hm common mode choke CHENG HANN WCM2012F2SF-670T04(SM070000S80)

1025:
R370,R413 change from SD028100380(100K_0402_5%) to SD028200380(200K_0402_5%)
PCH_GPIO1 change net to WL_EN#
LVDS
Add +5VS (Pin34) & USB20_N4/P4 (Pin35, 36)
change EDP_HP0 to Pin18
PCH side add USB20_N4/P4 (Pin35, 36)

For eDP interface AUX channel, please request Layout routing as differential signal to follow eDP Layout Guide.
(VGA_LCD_CLK & VGA_LCD_DATA / I2CC_SCL & I2CC_SDA)

DEL DDR DM
R50,R58,R59,R48,R56,R51,R60,R49 DIMMA
R39,R52,R44,R43,R46,R39,R45,R40 DIMMA
R77,R73,R109,R112,R180,R181,R192,R206 DIMMB
R64,R83,R108,R115,R179,R183,R189,R208 DIMMB

1026:
C604,C591 change from SGA00004200(470 4.5mohm)to SGA00003N00(470 9mohm)
Pop R257(SD028100380 100K_0402_5%),R622(SD028820180 8.2K_0402_5%) Board ID
R443 change from 100K_0402_5% to 10K_0402_5% (SD028100280)

remove R471,R622(JMINI1,JMINI2 Pin42 0ohm series resistor)
J1,J2 change location to J6,J7
remove R222 0ohm_0402 (H_CPUPWRGD_R)
remove R423,0ohm_0402 (MINI1_CLKREQ#_R)
remove R392 0ohm_0402 (LAN_CLKREQ#_R)
remove R685 0ohm_0402 (MINI2_CLKREQ#_R)
remove R655 0ohm_0402 (WAKE#)
remove R636 0ohm_0402 (PCH_RSMRST#)
remove R377 0ohm_0402 (SUS_PWR_DM_ACK)
remove R339 0ohm_0402 (PBTN_OUT#)
remove R359 0ohm_0402 (DGPU_HOLD_RST#)
remove R16 0ohm_0402 (BKOFF#)
remove R448 0ohm_0402 (VGA_EDP_DET)
remove R533 0ohm_0402 (VGA_HDMI_DET)
remove R627 0ohm_0603 (+SPT_VCC)

ADD R39 0ohm_0402 LOCAL_DIM
ADD R38 0ohm_0402 COLOR_ENG_EN

C242,C653,C332,C354,C678 change footprint to C_X(2pin)

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