

Compal confidential

Schematics Document

Intel portability uFCBGA/uFCPGA

with ATI-RC300M+SB200 core logic

2003-07-10

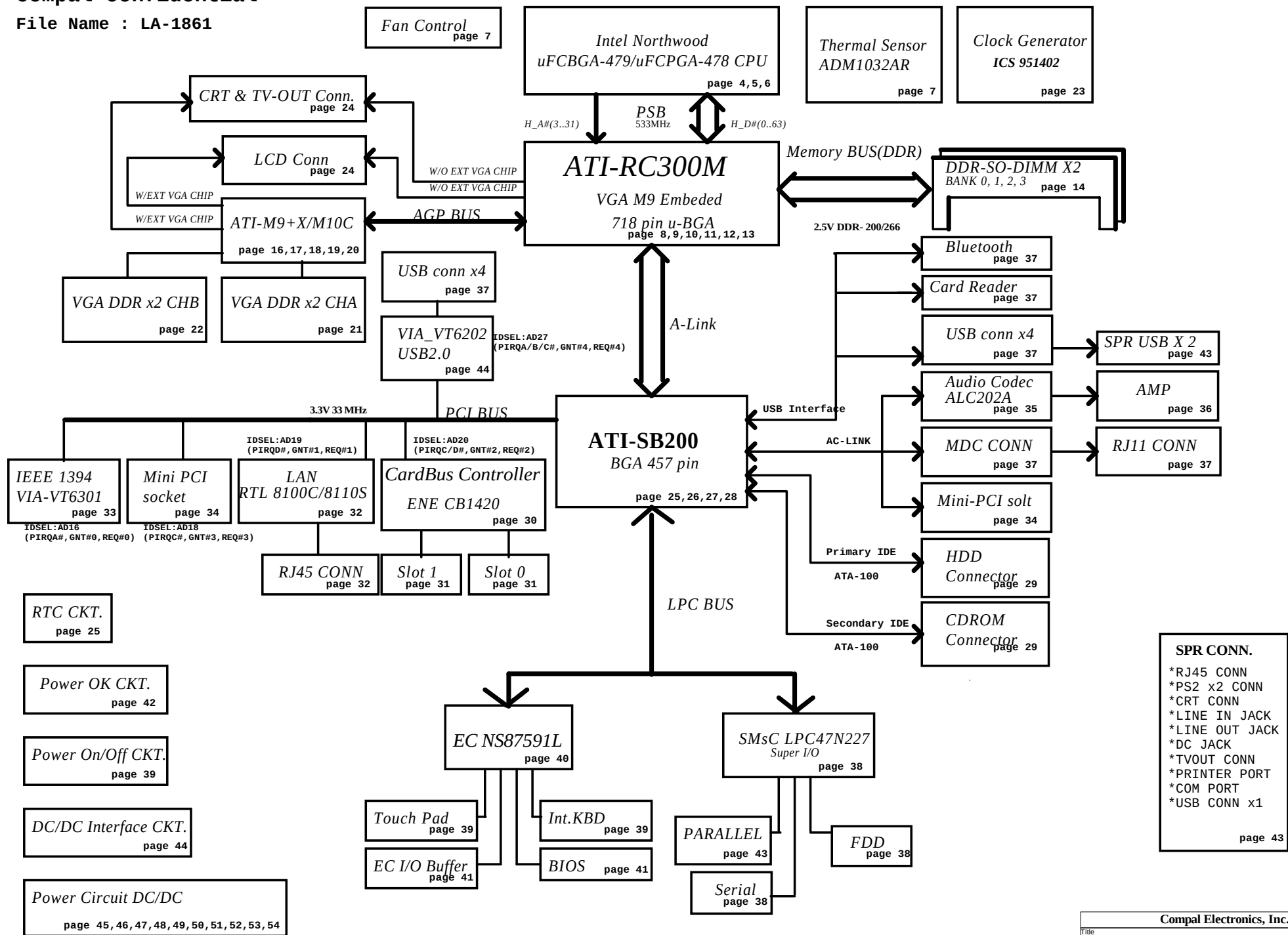
REV:0.4

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Title			
SCHEMATIC, M/B LA-1861			
Size	Document Number		Rev
	401257		0E
Date:	星期三, 七月 30, 2003		Sheet 1 of 61

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File Name : LA-1861



SPR CONN.

- *RJ45 CONN
- *PS2 x2 CONN
- *CRT CONN
- *LINE IN JACK
- *LINE OUT JACK
- *DC JACK
- *TVOUT CONN
- *PRINTER PORT
- *COM PORT
- *USB CONN x1

page 43

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Schematic, M/B LA-1861

Size	Document Number	Rev
	401257	0E
Date:	星期三, 七月 30, 2003	Sheet 2 of 61

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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCVID	The voltage for Processor VID select	ON	OFF	OFF
+1.25VS	1.25V switched power rail for DDR Vtt	ON	OFF	OFF
+1.2VS_VGA	1.2V I/O power rail for ATI-VGA M9+X/M10P.	ON	OFF	OFF
+1.5VS	1.5V I/O power rail for ATI-RS300M/RC300M NB AGP.	ON	OFF	OFF
+1.8VS	1.8V switched power rail for ATI-RS300M/RC300M NB.	ON	OFF	OFF
+2.5VALW	2.5V always on power rail	ON	ON	ON*
+2.5V	2.5V system power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+3V	3.3V system power rail for SB,LAN,CardReader and HUB.	ON	ON	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12VS	12Vswitched power rail on power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
NB Internal VGA	N/A	N/A	A
AGP BUS	AGP_DEVSEL	N/A	A
SOUTHBRIDGE	AD31 (INT.)	N/A	N/A
USB	AD30 (INT.)	N/A	D
AC97	AD31 (INT.)	N/A	B
ATA 100	AD31 (INT.)	N/A	A
ETHERNET	AD24 (INT.)	N/A	C
1394	AD16	0	A
LAN	AD19	1	D
CARD BUS	AD20	2	A/B
Wireless LAN	AD18	3	C
VIA6202 USB20	AD27	4	A/B/C

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 X
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

M9@ : means just build when no external AGP VGA chip build in .

M9+/M10@ : means just build when M9+XC or M10 build in

M9+@ : means just build when M9+XC chip build in .

M10@ : means just build when M10 chip build in .

NSPR@ : means just build when no SPR build in .

SPR@ : means just build when SPR build in .

8100S@ : means just build when 8100S build in .

1394@ : means just build when 1394 build in .

MDC@ : means just build when MDC build in .

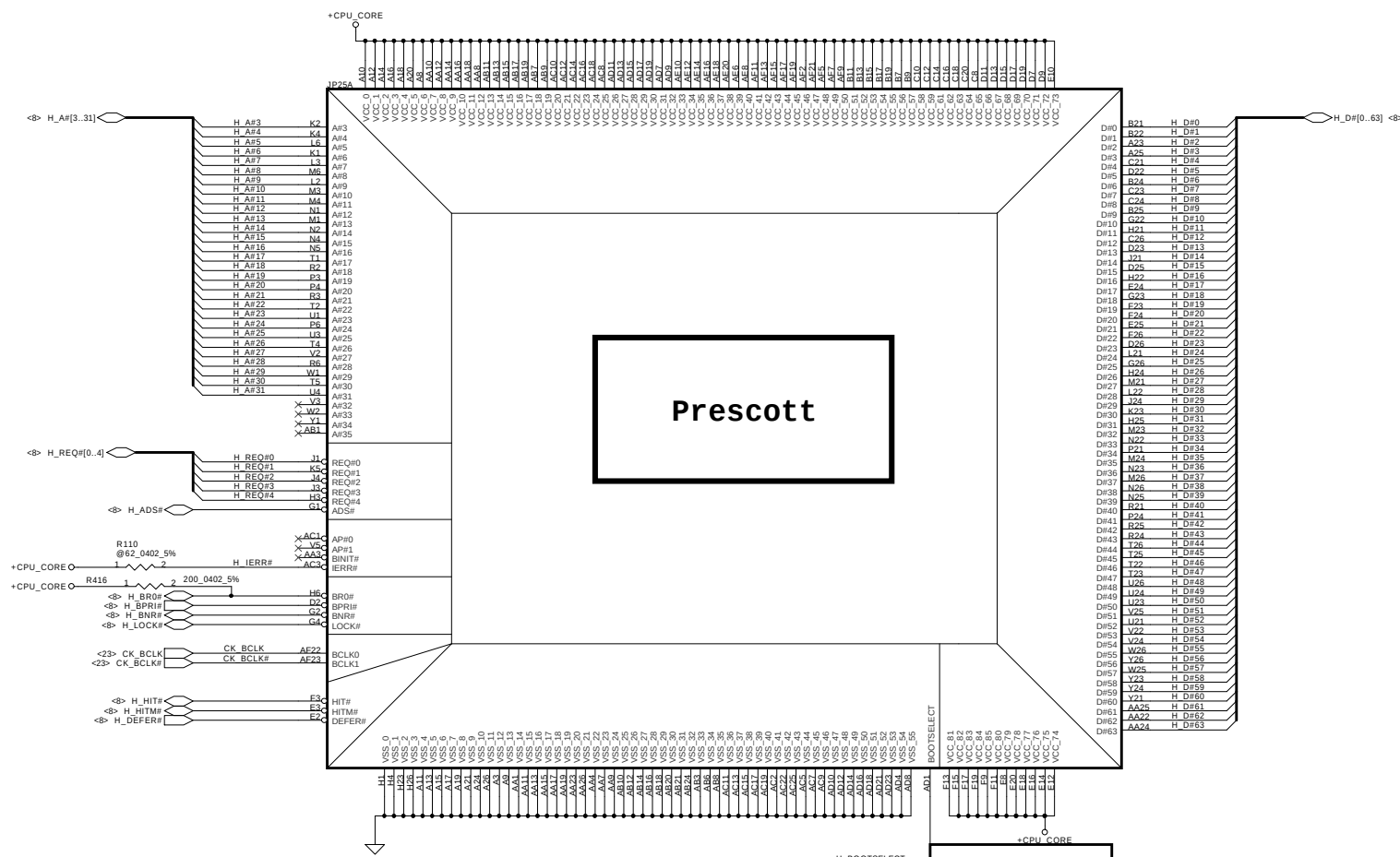
Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	
5	
6	
7	

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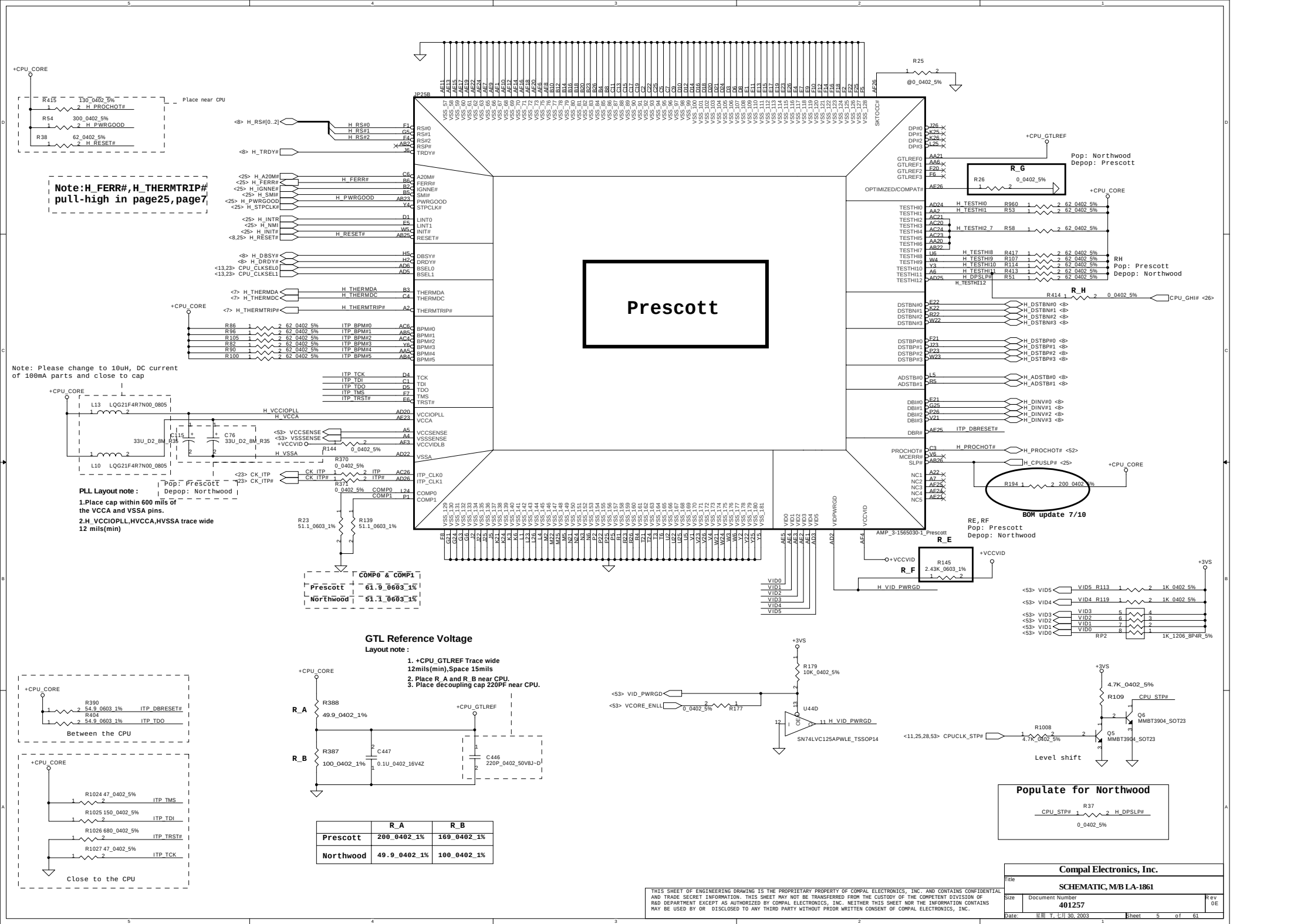
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SCHEMATIC, M/B LA-1861			
Size	Document Number	Rev	
	401257	0E	
Date:	星期三, 七月 30, 2003	Sheet	3 of 61

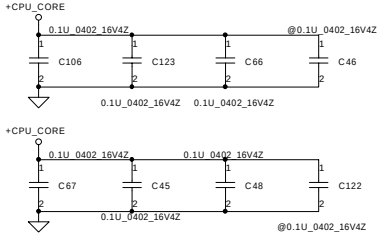
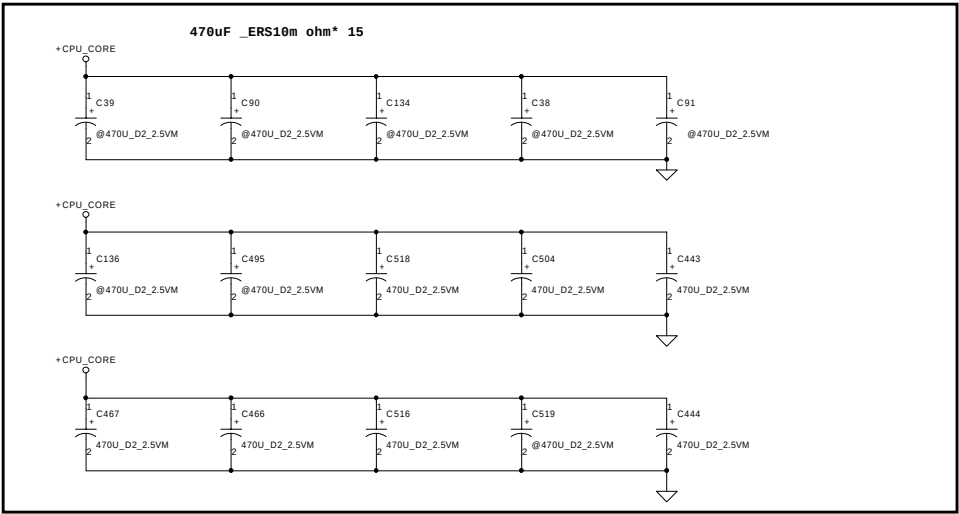
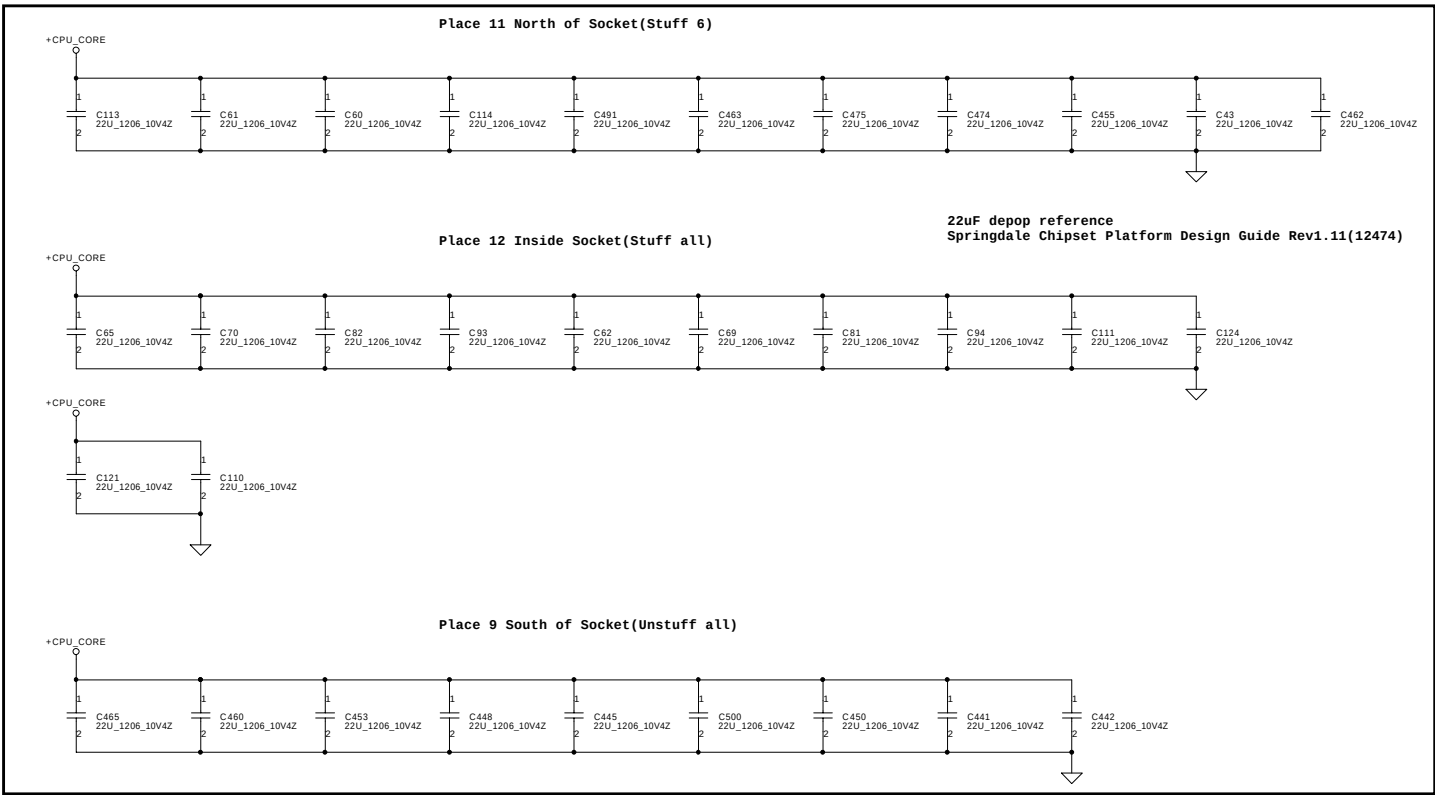


Reference Intel document Desktop P4 Spec.: 10988 P4 0.13u 512KB L2 EMTS Rev.2.0 Desktop Prescott Spec.: 11910 Prescott EMTS Rev.0.5									
Pin number	Northwood Pin name	Comment	Prescott Pin name	Comment	Northwood MT Pin name	Comment	Northwood	Prescott	Northwood MT
A6	TESTHI11	Pull-up 200ohm to +VCC_CORE	TESTHI11	Pull-up 62ohm to +VCC_CORE	GHI#	Connect to PLD CPU/PREF through 0ohm	Pop	Pop	Pop
B6	FERR#	Pull-up 62ohm to +VCC_CORE	FERR#/PBE#	Pull-up 62ohm to +VCC_CORE	FERR#	Pull-up 62ohm to +VCC_CORE	Pop	Pop	Pop
AA20	ITPCLKOUT0	Pull-up 56ohm to +VCC_CORE	TESTHI6	Pull-up 62ohm to +VCC_CORE	ITPCLKOUT0	Pull-up 56ohm to +VCC_CORE	Pop	Pop	Pop
AB22	ITPCLKOUT1	Pull-up 56ohm to +VCC_CORE	TESTHI7	Pull-up 62ohm to +VCC_CORE	ITPCLKOUT1	Pull-up 56ohm to +VCC_CORE	Pop	Pop	Pop
AD2	NC	float	VIDPWRGD	Pull-up 2.43K ohm to +VCCVID	NC	float	Depop	Pop	Depop
AD3	NC	float	VID5	Pull-up 1Kohm to +3VRUN & connect to PWRIC	NC	float	Depop	Pop	Depop
AF3	NC	float	VCCVIDLB	Connect to +VCCVID	NC	float	Depop	Pop	Depop
AD20	VCCA	Connect to CPU Filter	VCCI0PLL	Connect to CPU Filter	VCCA	Connect to CPU Filter			
AE23	VCCI0PLL	Connect to CPU Filter	VCCA	Connect to CPU Filter	VCCI0PLL	Connect to CPU Filter			
AD1	VSS	Connect to GND	BOOTSELECT	CPU determine	VSS	Connect to GND	Pop	Depop	Pop
AE26	VSS	Connect to GND	OPTIMIZED/COMPAT#	float	VSS	Connect to GND	Pop	Depop	Pop
AD25	TESTHI12	Pull-up 200ohm to +VCC_CORE	TESTHI12	Pull-up 62ohm to +VCC_CORE	DPSLP	Connect to PLD through 0ohm	Pop	Pop	Pop

Note: pop in pages3

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Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11
(12474)page239

Decoupling Reference Requirement:
560uF Polymer, ESR:5m ohm(each) * 10
22uF X5R * 32

Compal Electronics, Inc.			
Title		SCHEMATIC, M/B LA-1861	
Size	Document Number	Rev	
	401257	0E	
Date:	日期	T. 七月 30, 2003	Sheet 6 of 61

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Thermal Sensor ADM1032AR

Thermal Sensor ADM1032AR

W=19mil

+3VS

C580

0.1u_0402_16V4Z

R501
@10K_0402_5%

C590

2200P_0402_25V7K

U32

VDD 1

D+ 2

D- 3

THERM# 4

ADM1032AR_SOP8

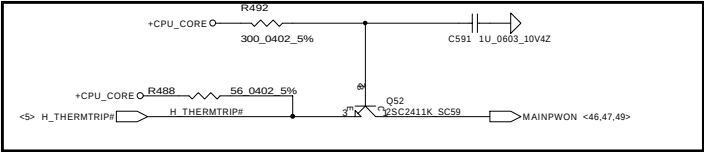
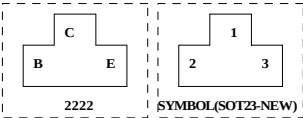
8 H_THERMDA H_THERMDA <4>

7 H_THERMDC H_THERMDC <4>

6 ALERT# EC_SMC_2 <40>

5 THERM# EC_SMD_2 <40>

Address:1001_100X

[illegible][illegible]

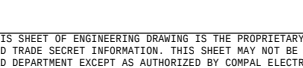
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SCHEMATIC, M/B LA-1861			
Size	Document Number		Rev
	401257		0E
Date:	星期四, 七月 30, 2003	Sheet	7 of 61

Left Column (Pins 1-16 and 19-20):

Pin	Pin Name	Function
1	DDRA DQ7	8 DDRA SDQ7
2	DDRA DQ0	7 DDRA SDQ0
3	DDRA DQ8	6 DDRA SDQ8
4	DDRA DQ5	5 DDRA SDQ5
19	DDRA DQ4	8 DDRA SDQ4
20	DDRA DQ6	7 DDRA SDQ6
1	DDRA DQ1	6 DDRA SDQ1
2	DDRA DQ2	5 DDRA SDQ2
19	DDRA DQ3	8 DDRA SDQ3
20	DDRA DQ0	7 DDRA SDQ0
1	DDRA DQ8	6 DDRA SDQ8
2	DDRA DQ5	5 DDRA SDQ5
19	DDRA DQ9	8 DDRA SDQ9
20	DDRA DQ8	7 DDRA SDQ8
1	DDRA DQ14	6 DDRA SDQ14
2	DDRA DM1	5 DDRA SDM1
19	DDRA DQ12	8 DDRA SDQ12
20	DDRA DQ13	7 DDRA SDQ13
1	DDRA DQ10	6 DDRA SDQ10
2	DDRA DQ5	5 DDRA SDQ5
19	DDRA DQ15	8 DDRA SDQ15
20	DDRA DQ11	7 DDRA SDQ11
1	DDRA DQ20	8 DDRA SDQ20
2	DDRA DQ32	7 DDRA SDQ32
3	DDRA DQ17	6 DDRA SDQ17
4	DDRA DQ16	5 DDRA SDQ16
19	DDRA DQ21	8 DDRA SDQ21
20	DDRA DQ18	7 DDRA SDQ18
1	DDRA DM2	6 DDRA SDM2
2	DDRA DQ22	5 DDRA SDQ22
19	DDRA DQ19	8 DDRA SDQ19
20	DDRA DQ27	7 DDRA SDQ27
1	DDRA DQ28	6 DDRA SDQ28
2	DDRA DQ3	5 DDRA SDQ3
19	DDRA DQ24	8 DDRA SDQ24
20	DDRA DQ25	7 DDRA SDQ25
1	DDRA DQ29	6 DDRA SDQ29
2	DDRA DM3	5 DDRA SDM3

Right Column (Pins 17-18 and 21-28):

Pin	Pin Name	Function
17	DDRA DQ33	8 DDRA SDQ33
18	DDRA DQ36	7 DDRA SDQ36
21	DDRA DQ37	6 DDRA SDQ37
22	DDRA DQ34	5 DDRA SDQ34
23	DDRA DQ38	4 DDRA SDQ38
24	DDRA DQ35	3 DDRA SDQ35
25	DDRA DQ39	2 DDRA SDQ39
26	DDRA DQ35	1 DDRA SDQ35
27	DDRA DQ40	8 DDRA SDQ40
28	DDRA DQ45	7 DDRA SDQ45
21	DDRA DQ44	6 DDRA SDQ44
22	DDRA DQ55	5 DDRA SDQ55
23	DDRA DQ41	4 DDRA SDQ41
24	DDRA DQ42	3 DDRA SDQ42
25	DDRA DQ46	2 DDRA SDQ46
26	DDRA DM5	1 DDRA SDM5
27	DDRA DQ47	8 DDRA SDQ47
28	DDRA DQ43	7 DDRA SDQ43
21	DDRA DQ53	6 DDRA SDQ53
22	DDRA DQ52	5 DDRA SDQ52
23	DDRA DM6	4 DDRA SDM6
24	DDRA DQ56	3 DDRA SDQ56
25	DDRA DQ54	2 DDRA SDQ54
26	DDRA DQ48	1 DDRA SDQ48
27	DDRA DQ50	8 DDRA SDQ50
28	DDRA DQ55	7 DDRA SDQ55
21	DDRA DQ51	6 DDRA SDQ51
22	DDRA DQ57	5 DDRA SDQ57
23	DDRA DQ56	4 DDRA SDQ56
24	DDRA DQ57	3 DDRA SDQ57
25	DDRA DQ62	2 DDRA SDQ62
26	DDRA DM7	1 DDRA SDM7
27	DDRA DQ63	8 DDRA SDQ63
28	DDRA DQ58	7 DDRA SDQ58
21	DDRA DQ59	6 DDRA SDQ59
22	DDRA DQ59	5 DDRA SDQ59



3	2
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Size	Document Number 401257	Rev 0E
Date:	星期三, 七月 30, 2003	Sheet 9 of 61

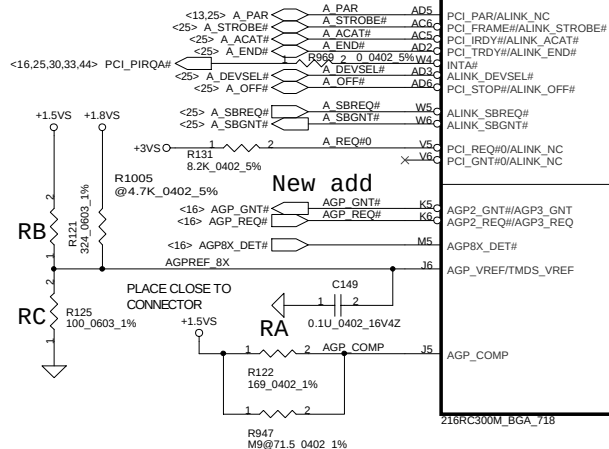
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<13,25> A_AD[0..31] A_AD[0..31]
<25> A_CBE#[0..3] A_CBE#[0..3]

U11C
A AD0 AK5 ALINK_AD0
A AD1 AJ5 ALINK_AD1
A AD2 AJ5 ALINK_AD2
A AD3 AH4 ALINK_AD3
A AD4 AJ3 ALINK_AD4
A AD5 AJ2 ALINK_AD5
A AD6 AH2 ALINK_AD6
A AD7 AH1 ALINK_AD7
A AD8 AG2 ALINK_AD8
A AD9 AG1 ALINK_AD9
A AD10 AE3 ALINK_AD10
A AD11 AE3 ALINK_AD11
A AD12 AE1 ALINK_AD12
A AD13 AE2 ALINK_AD13
A AD14 AE4 ALINK_AD14
A AD15 AE3 ALINK_AD15
A AD16 AE4 ALINK_AD16
A AD17 AE5 ALINK_AD17
A AD18 AC2 ALINK_AD18
A AD19 AC2 ALINK_AD19
A AD20 AC4 ALINK_AD20
A AD21 AB3 ALINK_AD21
A AD22 AB2 ALINK_AD22
A AD23 AB3 ALINK_AD23
A AD24 AB6 ALINK_AD24
A AD25 AA2 ALINK_AD25
A AD26 AA4 ALINK_AD26
A AD27 AA5 ALINK_AD27
A AD28 AA6 ALINK_AD28
A AD29 Y3 ALINK_AD29
A AD30 Y5 ALINK_AD30
A AD31 Y6 ALINK_AD31

PCI Bus 0 / A-Link I/F
PCI BUS 1 / AGP Bus (GPIO , TMD5 , ZVPort)

A_CBE#0 AG4C ALINK_CBE#0
A_CBE#1 AE2 ALINK_CBE#1
A_CBE#2 AC3 ALINK_CBE#2
A_CBE#3 AA3C ALINK_CBE#3



216RC300M_BGA_718

AGP_AD0/TMD2_HSYNC Y2 AGP_AD0
AGP_AD1/TMD2_VSYNC W3 AGP_AD1
AGP_AD2/TMD2_D1 W2 AGP_AD2
AGP_AD3/TMD2_D0 V3 AGP_AD3
AGP_AD4/TMD2_D3 V2 AGP_AD4
AGP_AD5/TMD2_D2 V1 AGP_AD5
AGP_AD6/TMD2_D5 U3 AGP_AD6
AGP_AD7/TMD2_D4 T2 AGP_AD7
AGP_AD8/TMD2_D6 R2 AGP_AD8
AGP_AD9/TMD2_D9 R3 AGP_AD9
AGP_AD10/TMD2_D8 P2 AGP_AD10
AGP_AD11/TMD2_D1 N2 AGP_AD11
AGP_AD12/TMD2_D10 N3 AGP_AD12
AGP_AD13 M3 AGP_AD13
AGP_AD14 M2 AGP_AD14
AGP_AD15 L3 AGP_AD15
AGP_AD16 L1 AGP_AD16
AGP_AD17/TMD1_HSYNC L2 AGP_AD17
AGP_AD18/TMD1_VSYNC K3 AGP_AD18
AGP_AD19/TMD1_DE K2 AGP_AD19
AGP_AD20/TMD1_D0 J3 AGP_AD20
AGP_AD21/TMD1_D1 J2 AGP_AD21
AGP_AD22/TMD1_D2 J1 AGP_AD22
AGP_AD23/TMD1_D3 I3 AGP_AD23
AGP_AD24/TMD1_D4 F3 AGP_AD24
AGP_AD25/TMD1_D5 G2 AGP_AD25
AGP_AD26/TMD1_D6 F2 AGP_AD26
AGP_AD27/TMD1_D9 E2 AGP_AD27
AGP_AD28/TMD1_D8 E1 AGP_AD28
AGP_AD29/TMD1_D11 D2 AGP_AD29
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AGP_AD31 AGP_AD31

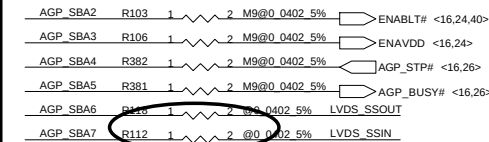
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AGP2_ADSTB0/AGP3_ADSTB0/TMD2_CLK# U2 AGP_ADSTBS_0 <16>
AGP2_ADSTB0/AGP3_ADSTB0/TMD2_CLK G3 AGP_ADSTBS_1 <16>
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AGP2_CBE#1/AGP3_CBE#1/TMD2_DE D1 AGP_CBE#1
AGP2_CBE#2/AGP3_CBE#2 D1 AGP_CBE#2
AGP2_CBE#3/AGP3_CBE#3/TMD1_D5 D1 AGP_CBE#3

AGP2_IRDY#/AGP3_IRDY#/GPIO0/2C_CLK R6 AGP_IRDY# <16>
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AGP2_STOP#/AGP3_STOP#/GPIO0/2C_DATA T5 AGP_STOP# <16>
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AGP2_WBF#/AGP3_WBF# N5 AGP_WBF# <16>

AGP2_SBA0/AGP3_SBA0/GPIO0/VDDC CNTL0 C3 AGP_SBA0
AGP2_SBA1/AGP3_SBA1/GPIO1/VDDC CNTL1 C2 AGP_SBA1
AGP2_SBA2/AGP3_SBA2/GPIO2/LVDS_BLON# D4 AGP_SBA2
AGP2_SBA3/AGP3_SBA3/GPIO3/LVDS_DIGON# E4 AGP_SBA3
AGP2_SBA4/AGP3_SBA4/GPIO4/STP AGP# F6 AGP_SBA4
AGP2_SBA5/AGP3_SBA5/GPIO5/AGP_BUSY# F5 AGP_SBA5
AGP2_SBA6/AGP3_SBA6/GPIO6/LVDS_SSOUT G6 AGP_SBA6
AGP2_SBA7/AGP3_SBA7/GPIO7/LVDS_SSIN G5 AGP_SBA7

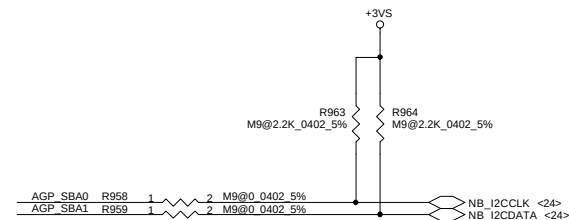
AGP_ST0 L6 AGP_ST0
AGP_ST1 M6 AGP_ST1
AGP_ST2 L5 AGP_ST2

AGPAND LVDS MUXED SIGNALS



BOM update 7/18 for EMI

For integrated graphics



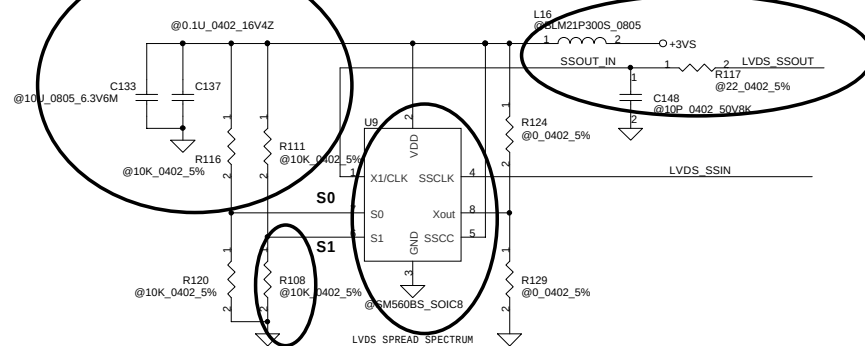
SST Ratio Selection Table for SM560

Input Freq. Range	S1=1 S0=M	S1=0 S0=1	S1=1 S0=1	S1=M S0=1
	2.5%	1.9%	1.2%	1.0%
60~70MHz	2.4%	1.8%	1.1%	0.9%
70~80MHz	2.3%	1.6%	1.1%	0.9%
80~100MHz	2.0%	1.4%	1.0%	0.8%
100~108MHz	1.8%	1.3%	0.8%	0.6%

BOM update 7/18 for EMI

"1"= Pull-up ; "0"= Pull-Down ;
"M"= Pull-up & Pull-Down

BOM update 7/18 for EMI



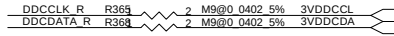
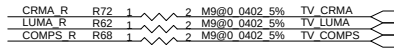
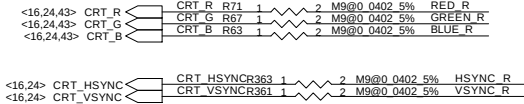
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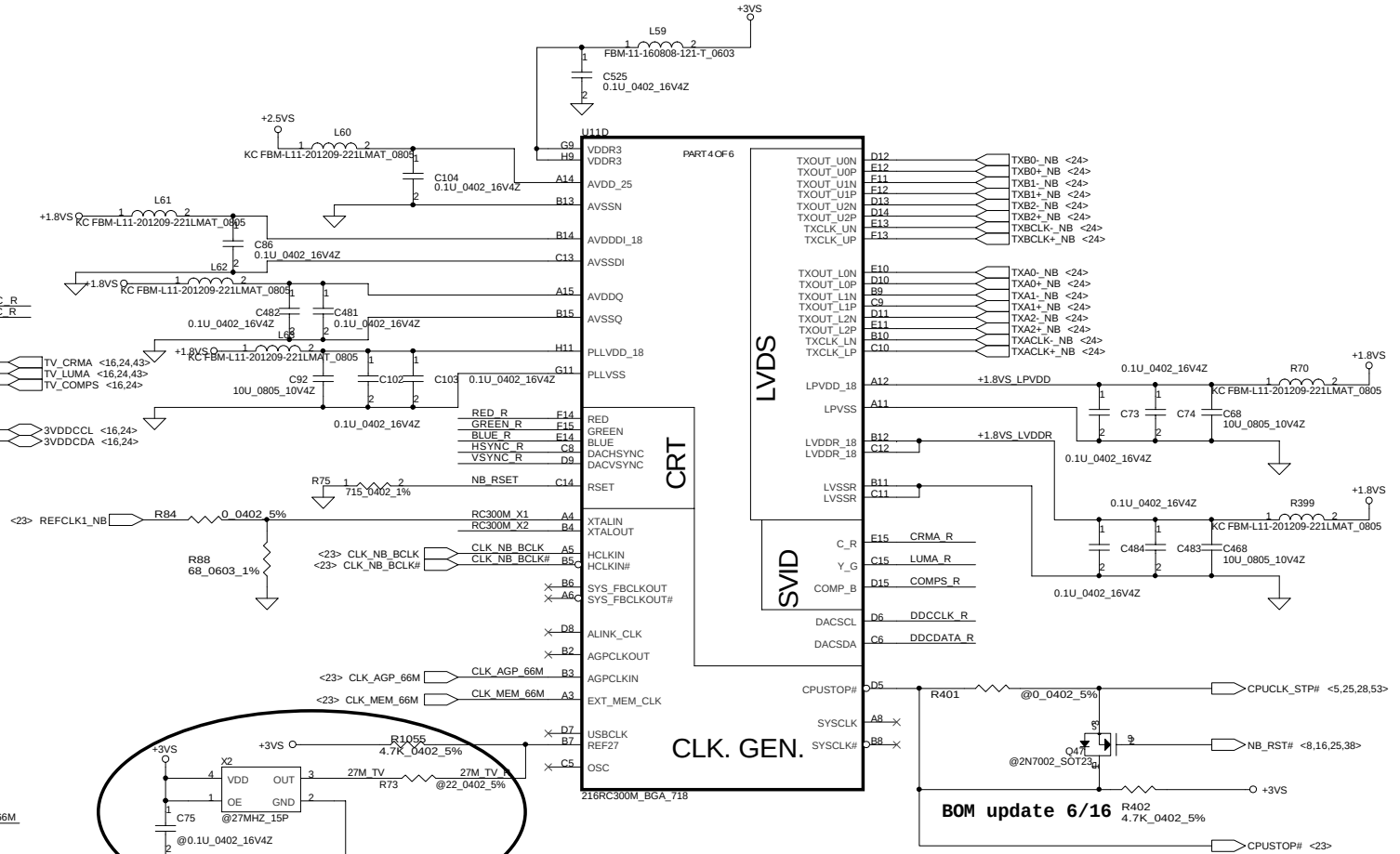
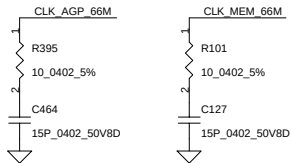
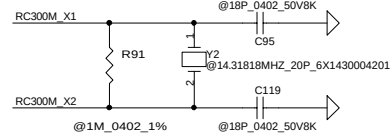
Title	Document Number	Rev
	401257	0E
Date	星期三, 七月 30, 2003	Sheet 10 of 61

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Note: PLACE CLOSE TO (NB CHIP)

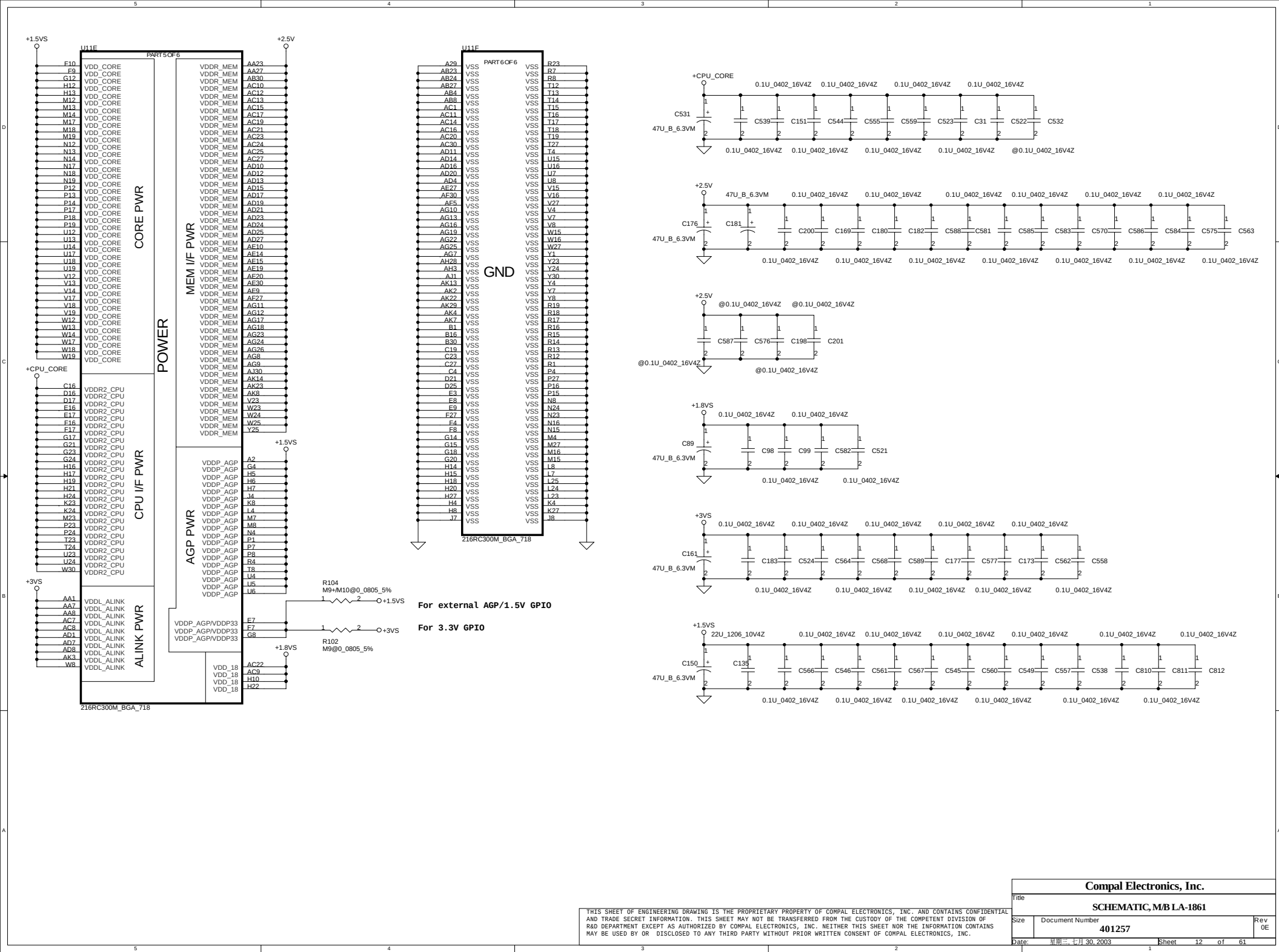


Note: PLACE CLOSE TO (NB CHIP)



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Title			
SCHEMATIC, M/B LA-1861			
Size	Document Number	Rev	
	401257	0E	
Date:	星期三, 七月 30, 2003	Sheet	11 of 61



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Compal Electronics, Inc.			
Title			
SCHEMATIC, M/B LA-1861			
Size	Document Number		Rev
	401257		0E
Date:	星期三, 七月 30, 2003		Sheet 12 of 61



A_AD[31..30] : FSB CLK SPEED

DEFAULT: 01
00: 100 MHZ
01: 133 MHZ
10: 200MHZ
11: 166 MHZ

A_AD29: STRAP CONFIGURATION

DEFAULT:1
0: REDUCEDE SET
1: FULL SET

A_AD28: SPREAD SPECTRUM ENABLE

DEFAULT:0
0: DISABLE
1: ENABLE

A_AD27: FrcShortReset#

DEFAULT: 1
0: TEST MODE
1: NORMAL MODE

A_AD26 : ENABLE IOQ

DEFAULT: 1
0: IOQ=1
1: IOQ=12

A_AD25/A_AD17 : CPU VOLTAGE[1..0]

DEFAULT: 00
00: 1.05V
01: 1.35V
11: 1.75V
10: 1.45V

A_AD24 : MOBILE CPU SELECT

DEFAULT: 1
0: BANIAS CPU
1: OTHER CPU

A_AD23 : CLOCK BYPASS DISABLE

DEFAULT: 1
0: TEST MODE
1: NORMAL

A_AD22 : OSC PAD OUTPUT PCICLK

DEFAULT : 1
0: OSC CLK OUT
1: PCICLK OUT

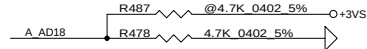
A_AD21 : AUTO_CAL ENABLE

DEFAULT : 1
0: DISABLE
1: ENABLE

A_AD20 : INTERNAL CLK GEN ENABLE

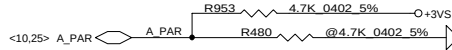
DEFAULT : 0
0: DISABLE
1: ENABLE

<10,25> A_AD[0..31] A_AD[0..31]
<10,25> A_CBE#[0..3] A_CBE#[0..3]



A_AD18 : ENABLE PHASE CALIBRATION

DEFAULT: 0
0: ENABLE
1: DISABLE

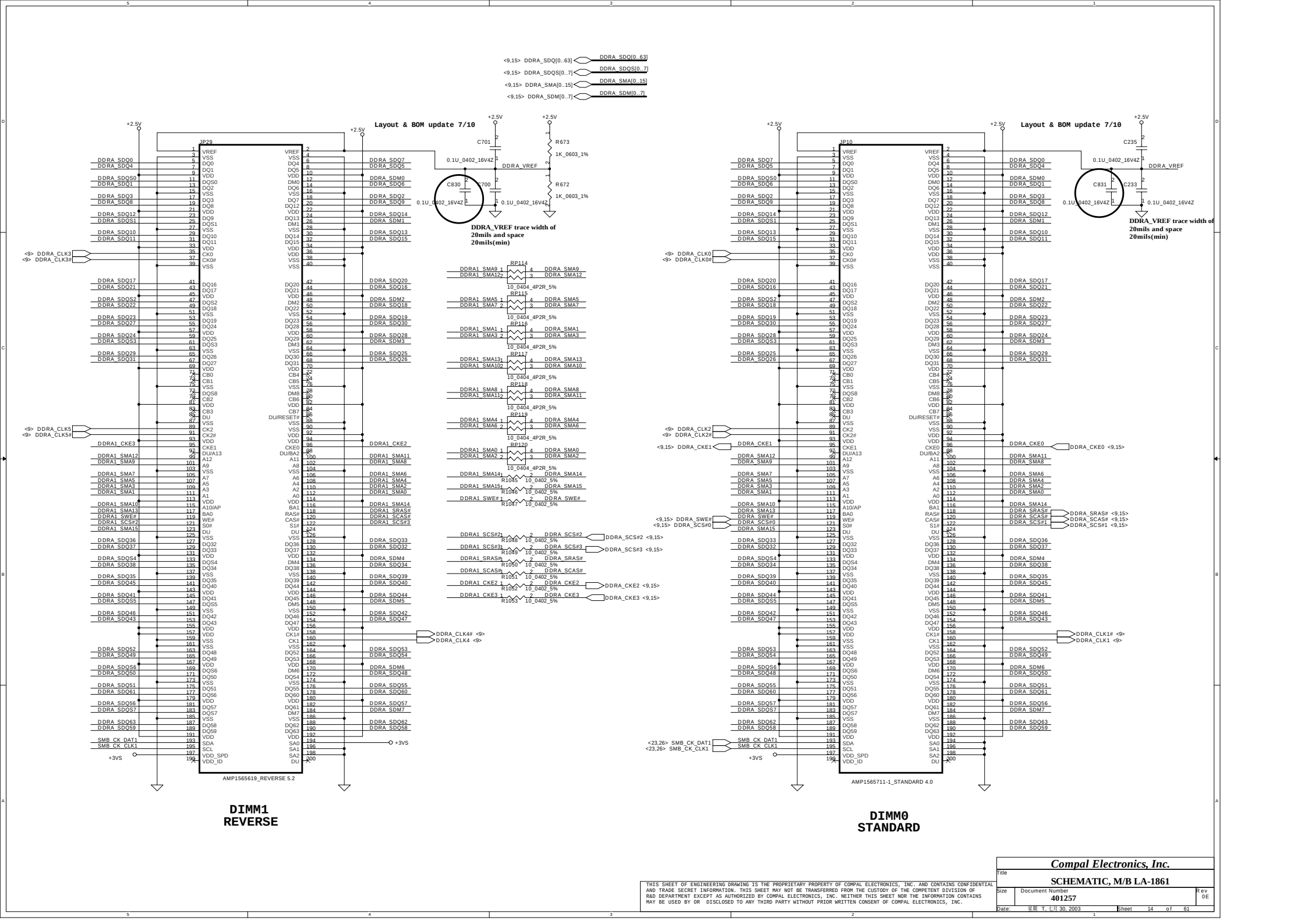


PAR: EXTENDED DEBUG MODE

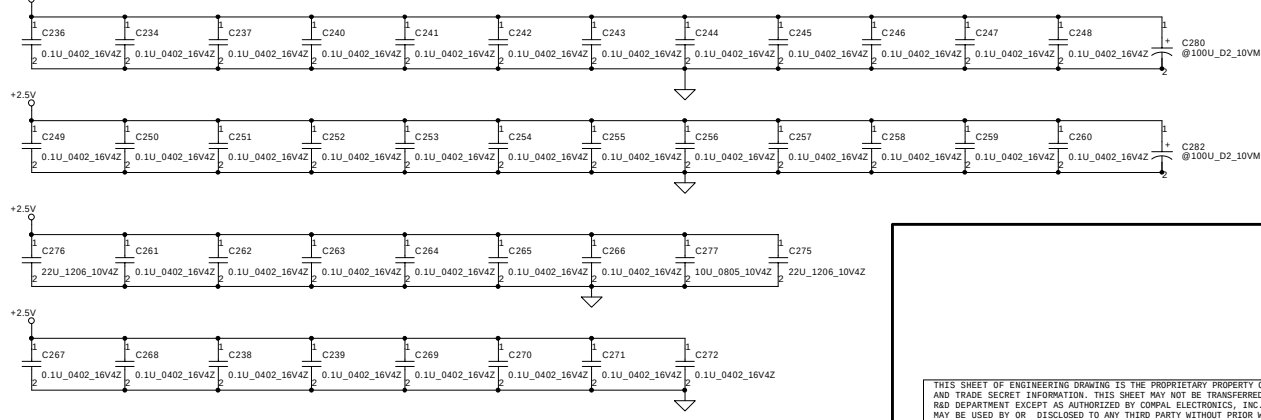
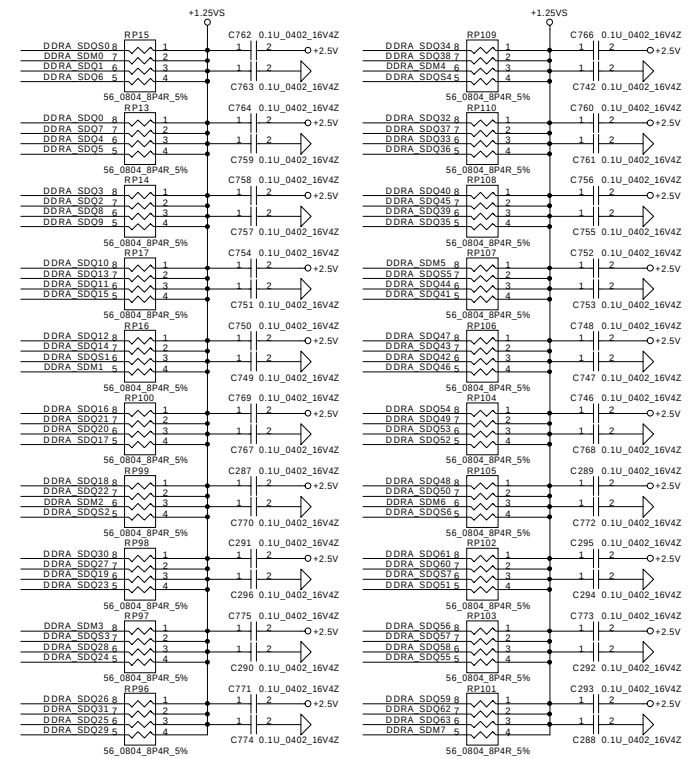
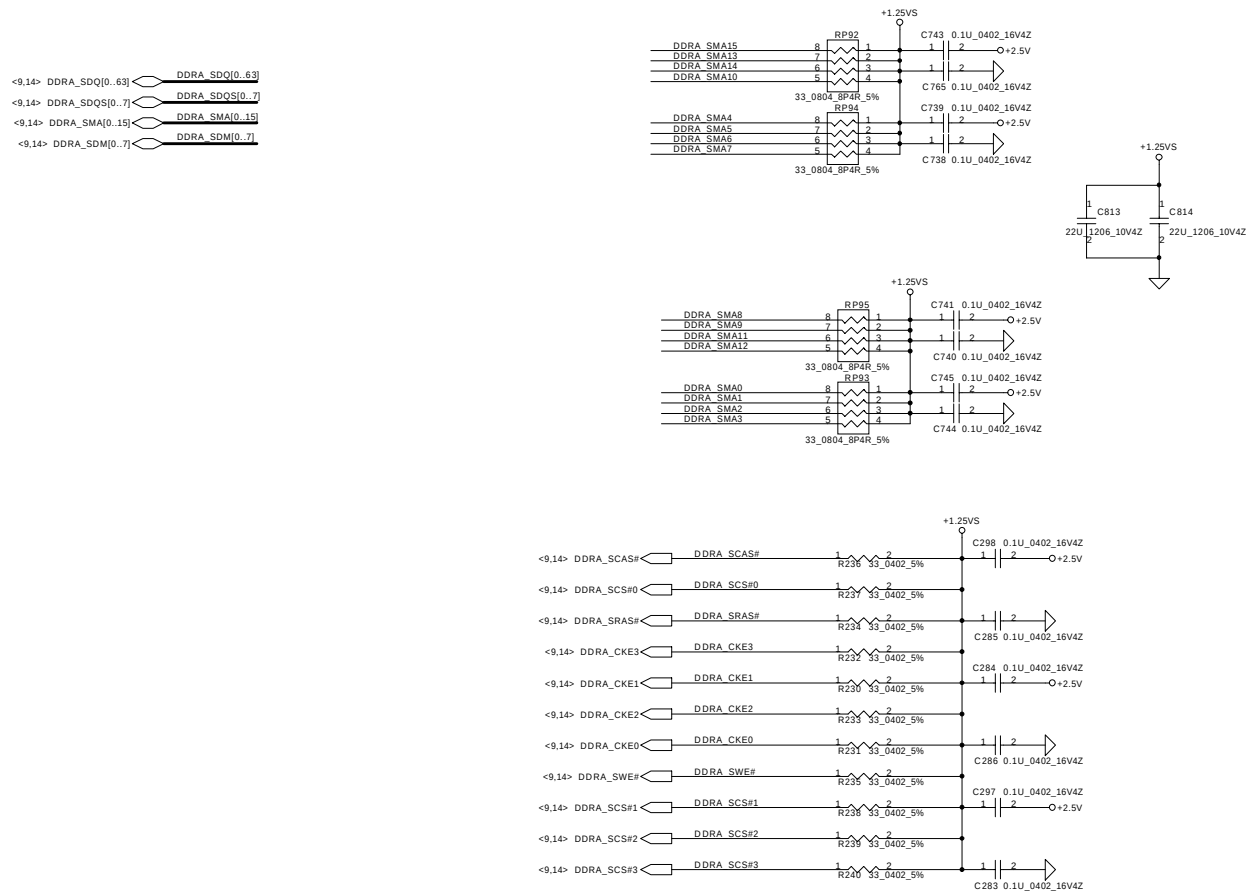
DEFAULT : 1
0: DEBUG MODE
1: NORMAL

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Title			
SCHEMATIC, M/BLA-1861			
Size	Document Number		Rev
	401257		0E
Date:	星期三, 七月 30, 2003	Sheet	13 of 61



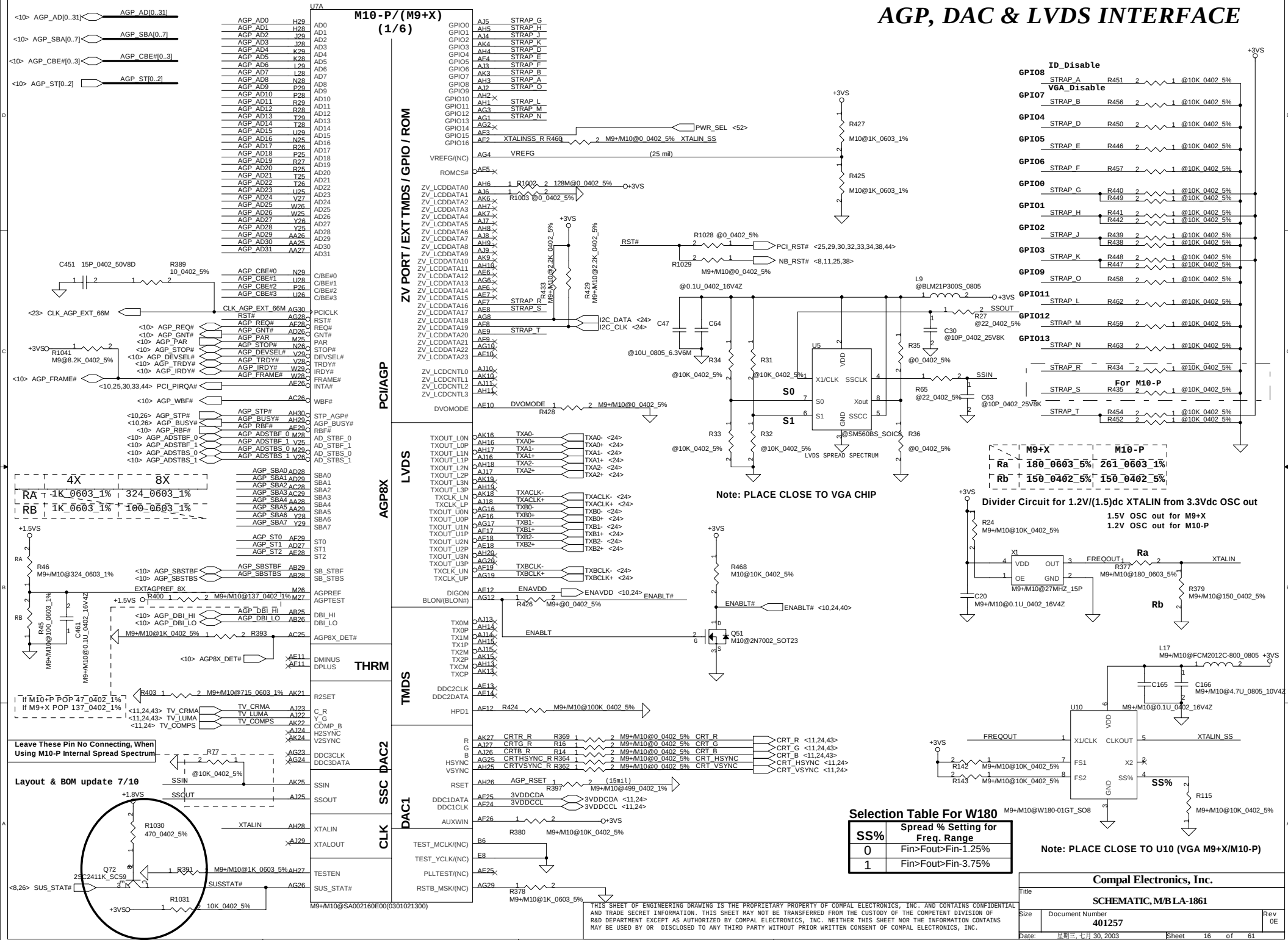
DDR Termination resistors & Decoupling caps



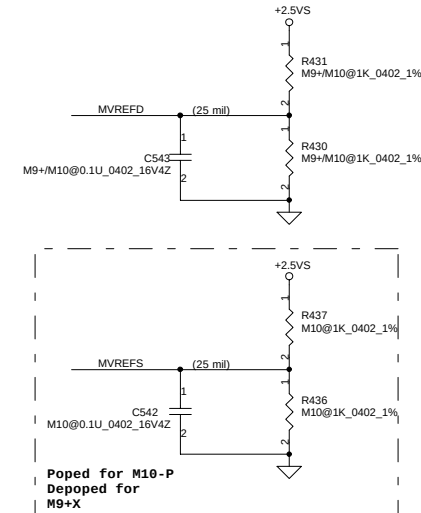
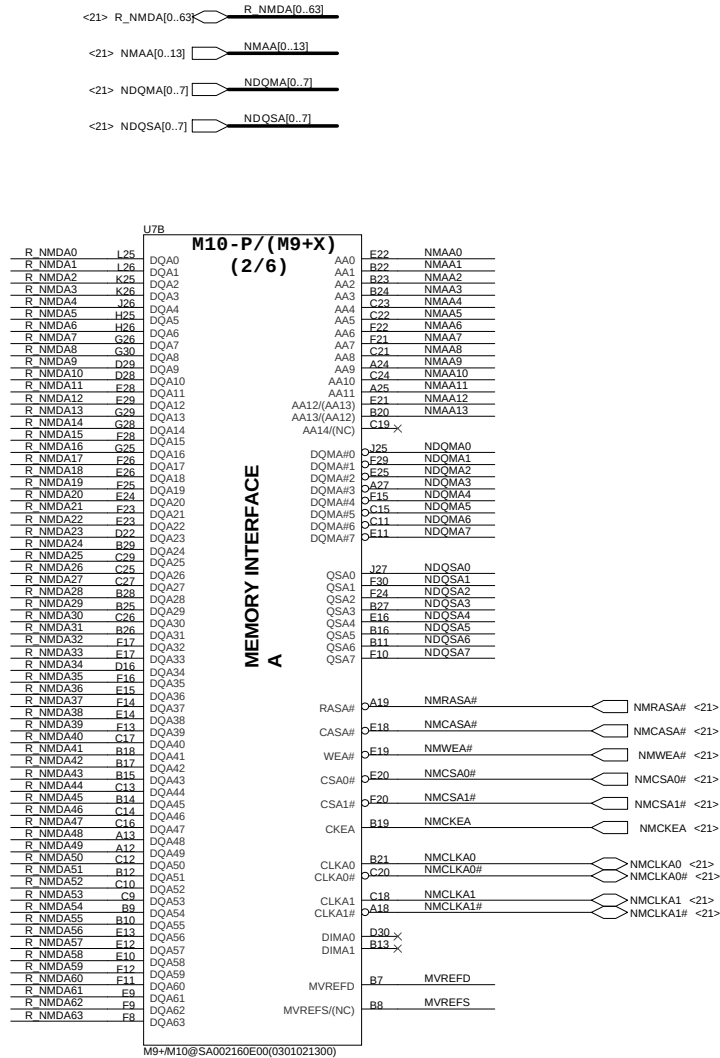
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Title			
SCHEMATIC, M/B LA-1861			
Size	Document Number		Rev
	401257		0E
Date:	星期日, 七月 30, 2003	Sheet	15 of 61

AGP, DAC & LVDS INTERFACE



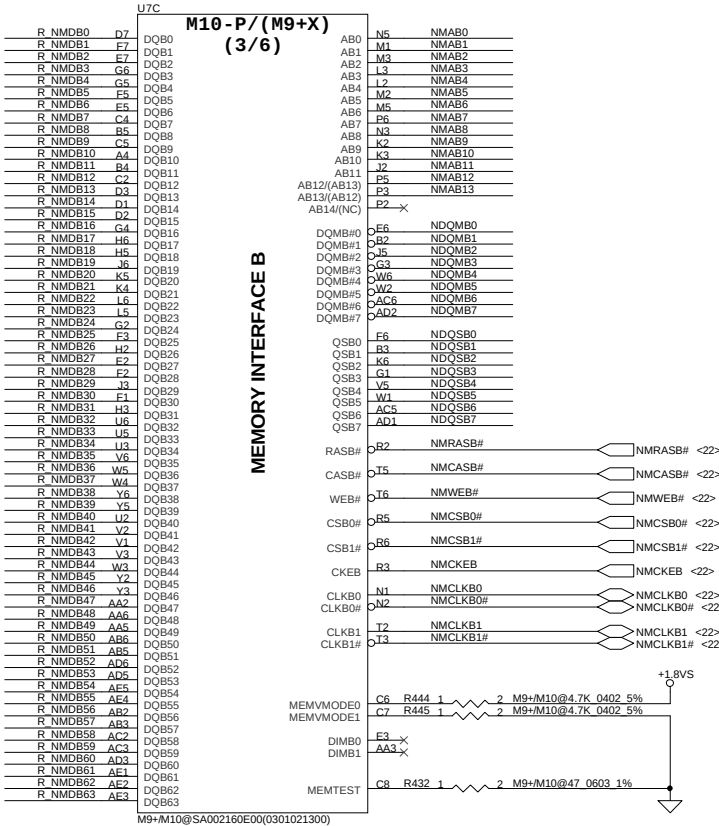
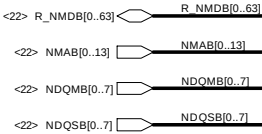
MEMORY INTERFACE A



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Title			
SCHEMATIC, M/BLA-1861			
Size	Document Number	Rev	
	401257	0E	
Date:	星期三, 七月 30, 2003	Sheet	17 of 61

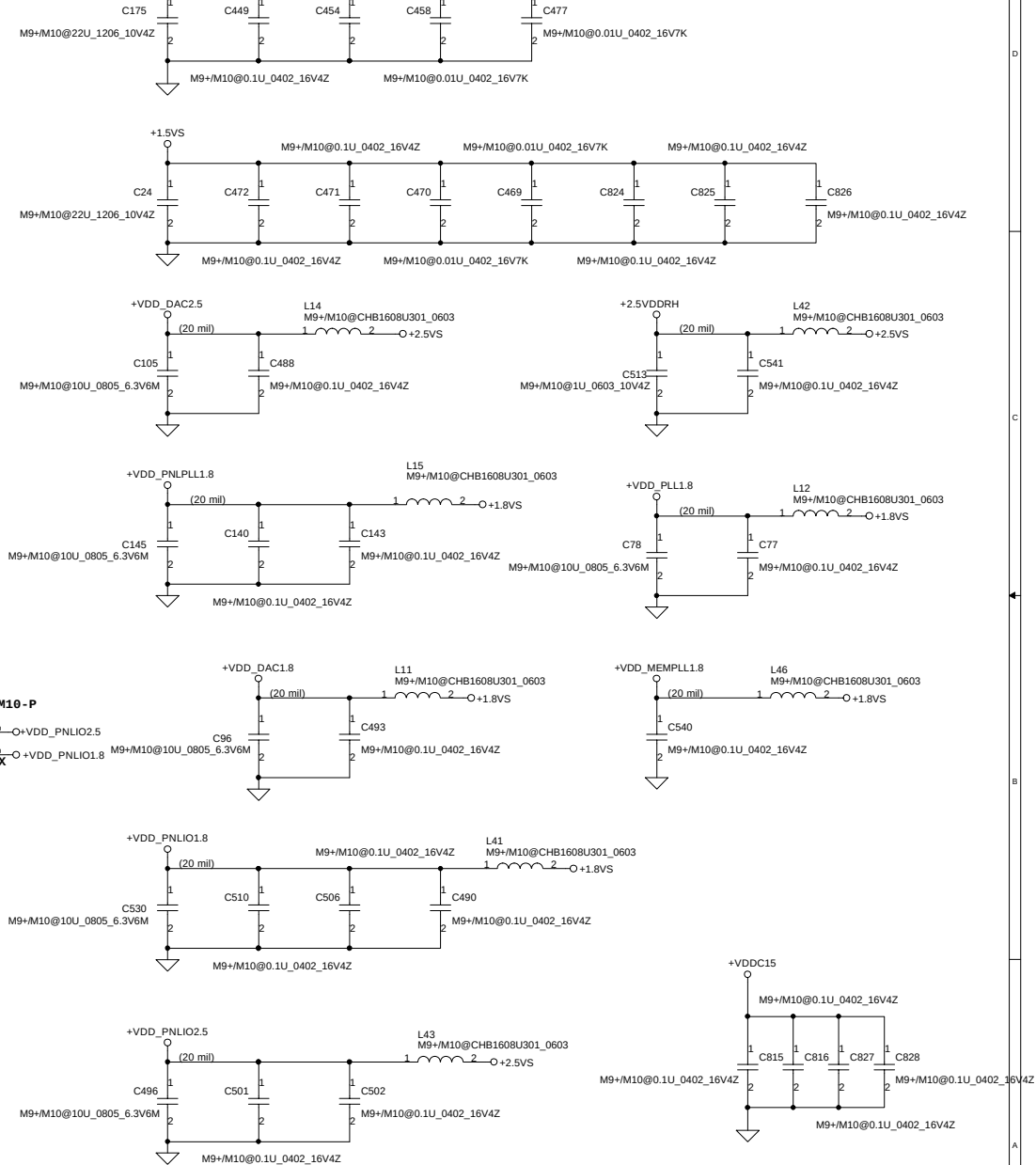
MEMORY INTERFACE B



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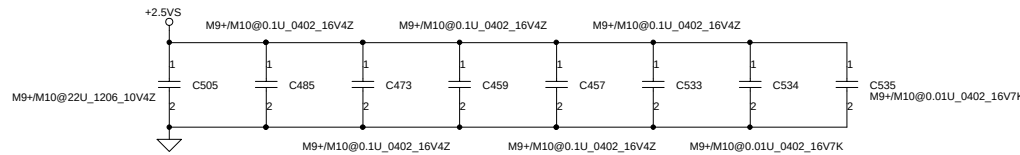
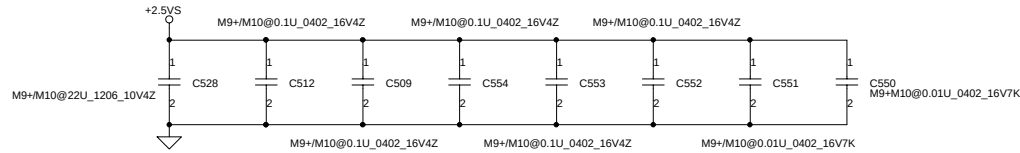
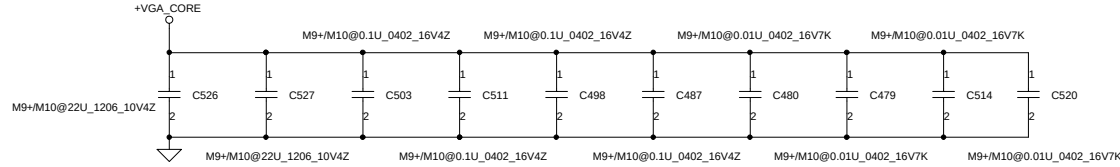
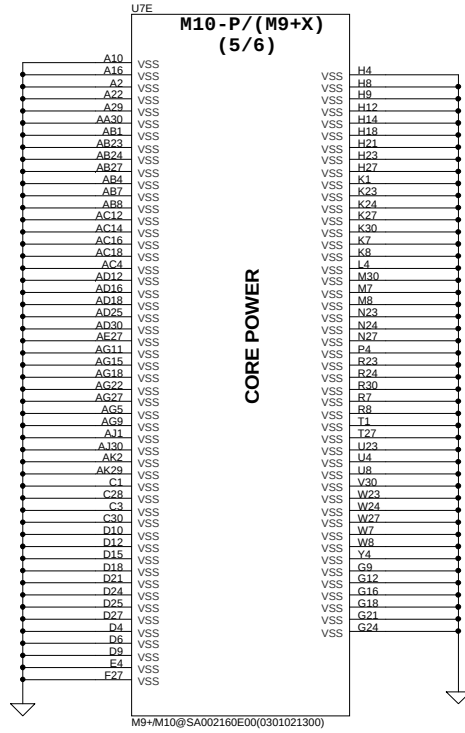
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Title			
SCHEMATIC, M/B LA-1861			
Size	Document Number	Rev	
	401257	0E	
Date:	星期三, 七月 30, 2003	Sheet	18 of 61

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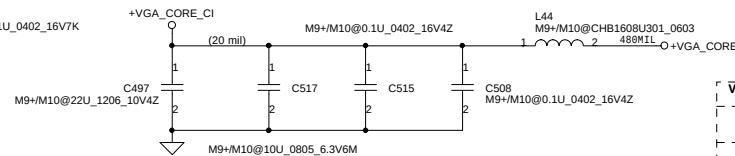
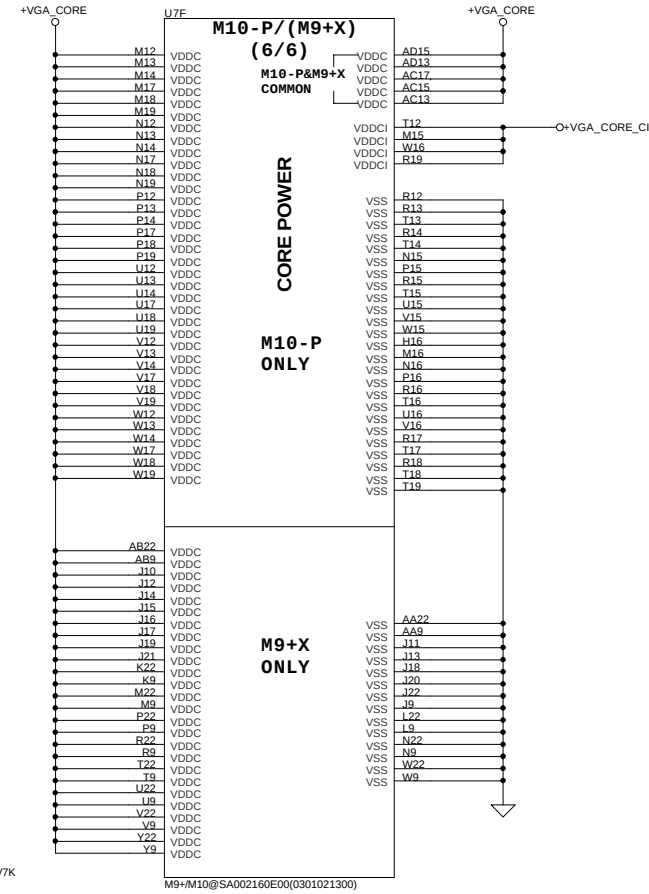


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Title			
SCHEMATIC, M/B LA-1861			
Size	Document Number		Rev
	401257		0E
Date	Sheet		of
星期三, 七月 30, 2003	19		61

POWER INTERFACE



As close as possible to related pin



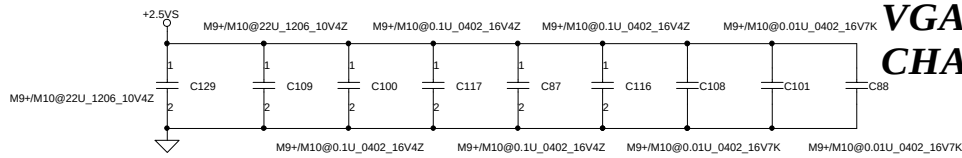
As close as possible to related pin

VGA_CORE for M10P	VGA_CORE for M9+
1.2	1.5V
1.0	1.25V

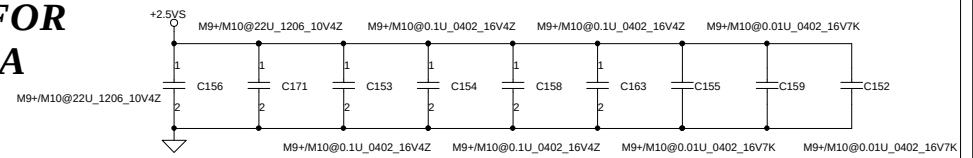
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Title			
SCHEMATIC, M/BLA-1861			
Size	Document Number	Rev	
	401257	0E	
Date:	星期三, 七月 30, 2003	Sheet	20 of 61

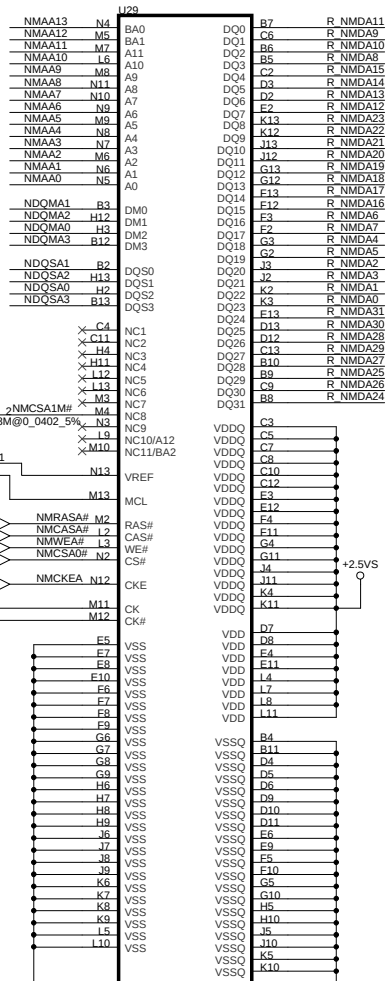
PGA DDR FOR CHANNEL A



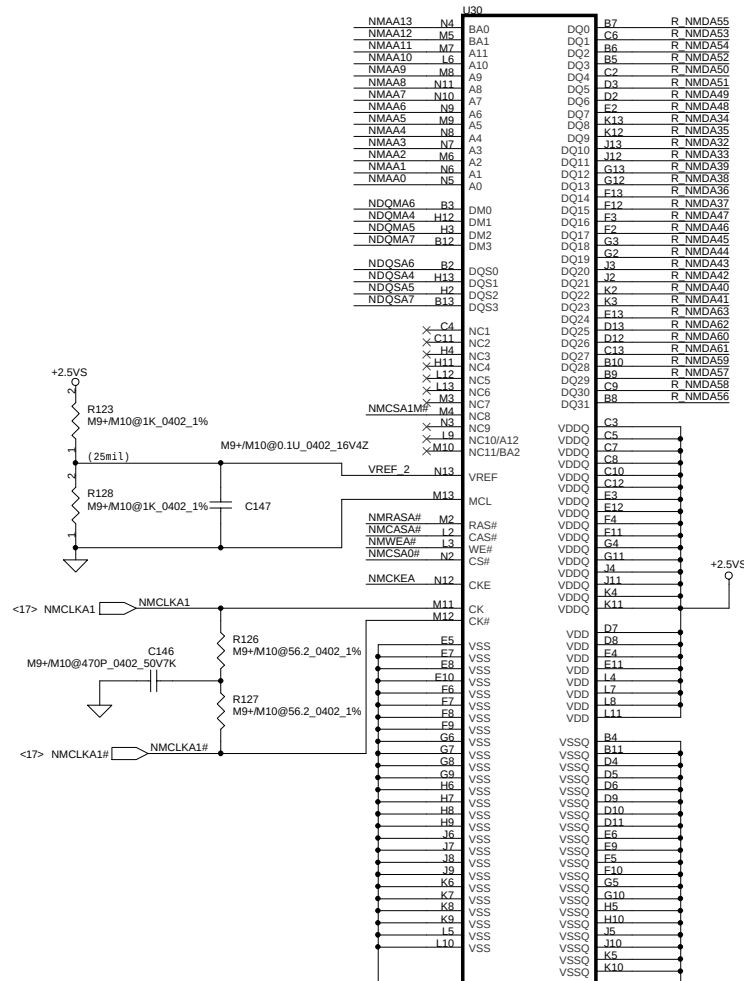
As close as ppossible to related pin



As close as possible to related pin



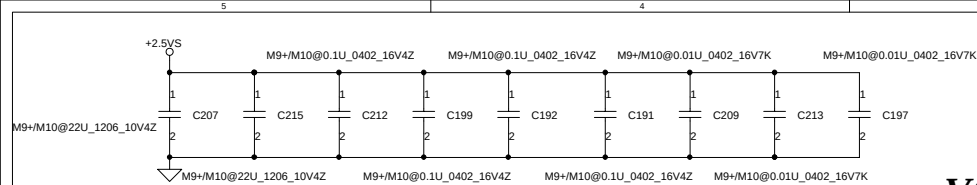
M9+/M10@K4D263238A_FBGA144



M9+/M10@K4D263238A_FBGA144

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Title			
SCHEMATIC, M/B LA-1861			
Size	Document Number		Rev
	401257		0E
Date:	星期三, 七月 30, 2003		Sheet 21 of 61

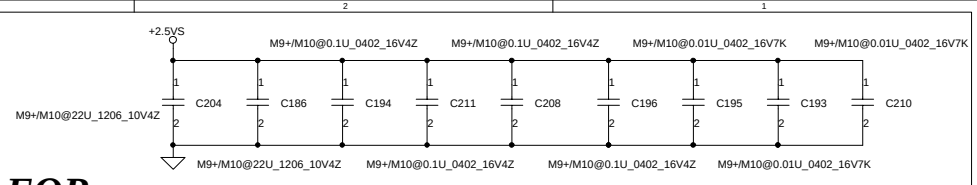
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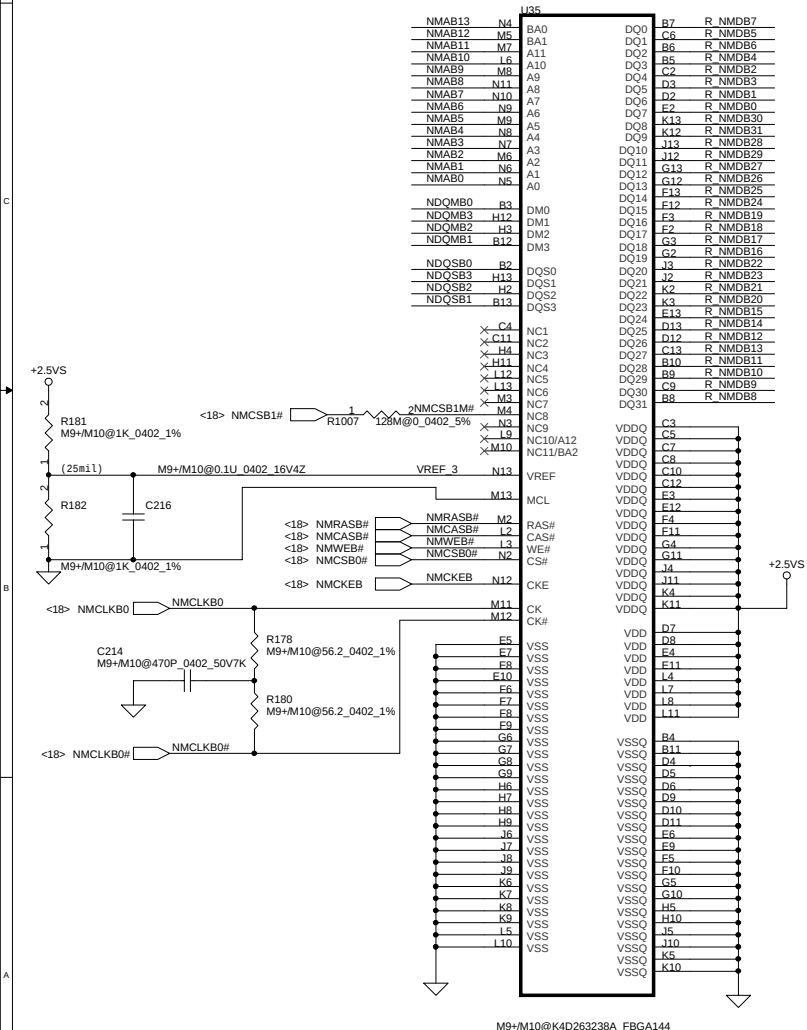
As close as possible to related pin



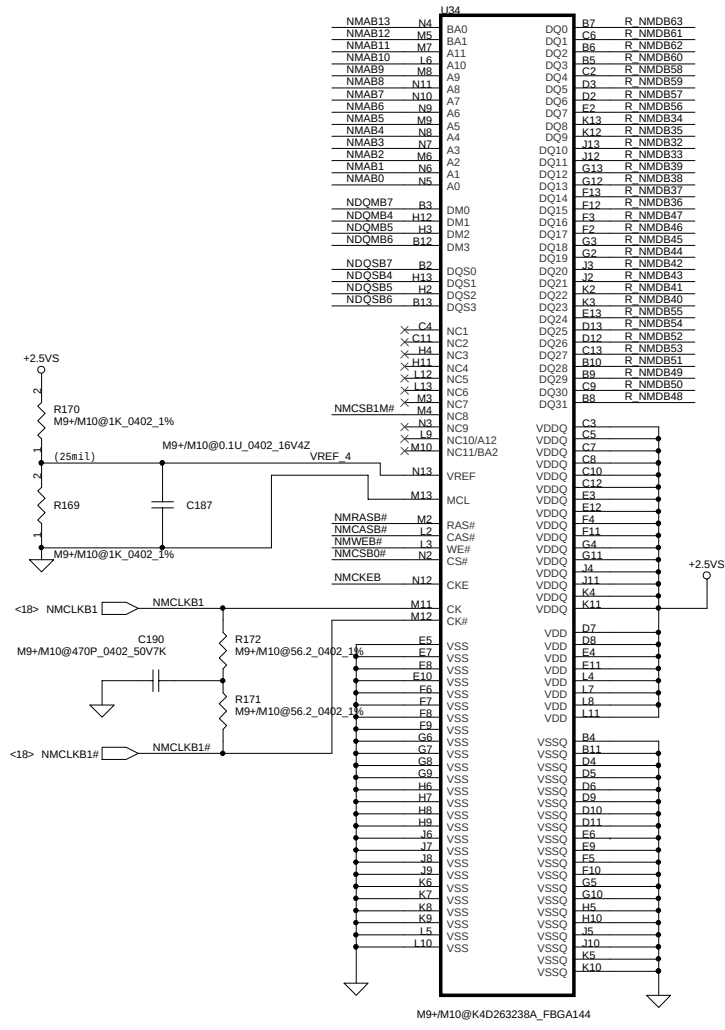
VGA DDR FOR CHANNEL B



As close as possible to related pin



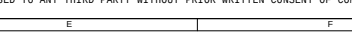
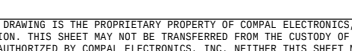
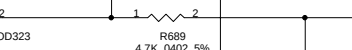
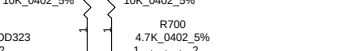
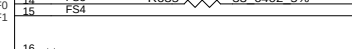
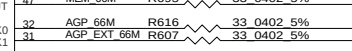
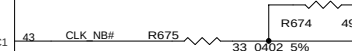
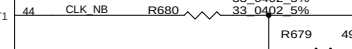
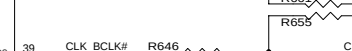
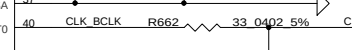
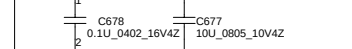
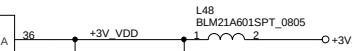
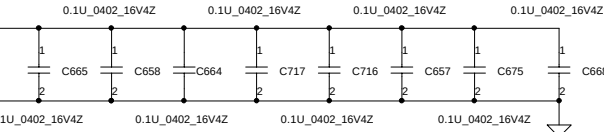
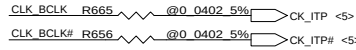
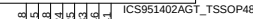
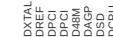
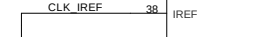
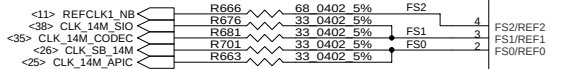
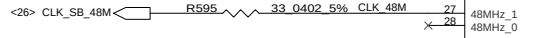
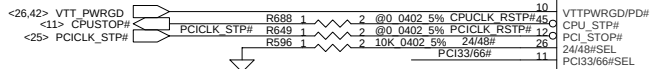
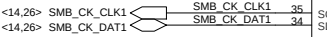
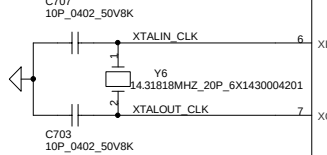
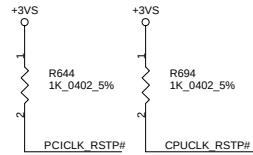
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M9+/M10@K4D263238A_FBG1A44

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Title			
SCHEMATIC, M/BLA-1861			
Size	Document Number	Rev	
	401257	0E	
Date:	星期三, 七月 30, 2003	Sheet	22 of 61

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CLOCK FREQUENCY SELECT TABLE

FS4	FS3	FS2	FS1	FS0	CPU	MEM	With Spread Enabled...
0	0	0	1	0	200	200	
0	0	0	0	1	133	133	Spread OFF OR Center spread +/-0.3%
0	0	0	0	0	100	100	

Note: 0 = PULL LOW
1 = PULL HIGH

A-LINK FREQ

PC133/66# = HIGH	66MHZ
PC133/66# = LOW	33MHZ

A_AD[31..30] : FSB CLK SPEED

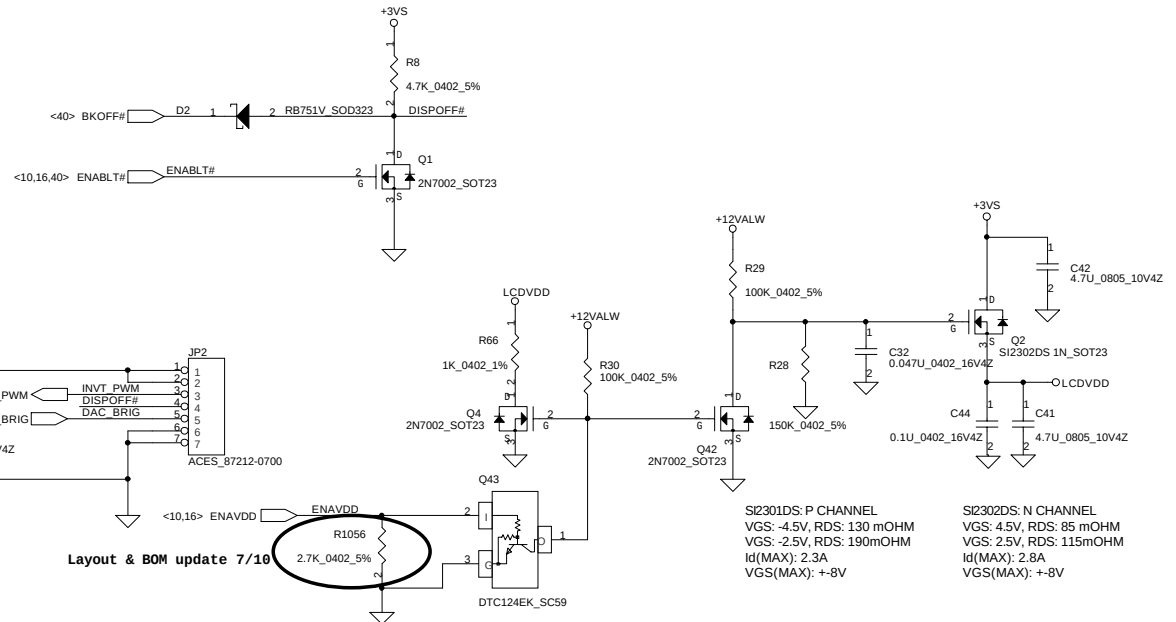
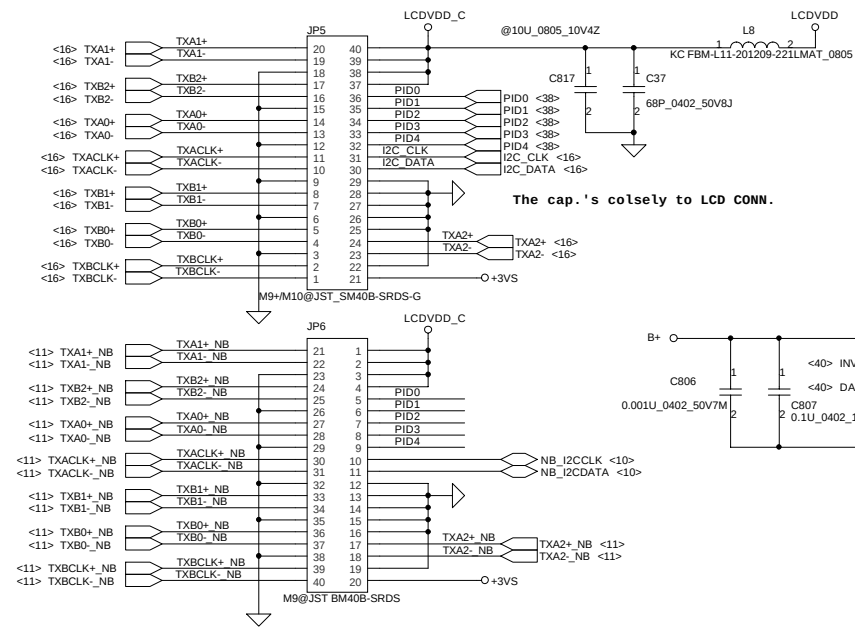
DEFAULT: 01

00: 100 MHZ
01: 133 MHZ
10: 200MHZ
11:166 MHZ

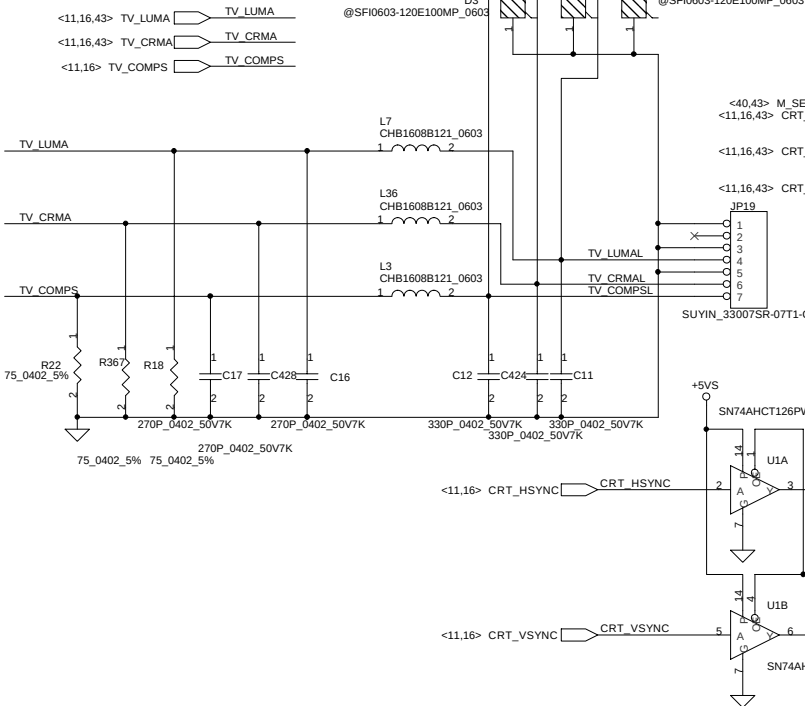
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SCHEMATIC, M/B LA-1861		
Size	Document Number	Rev
	401257	0E
Date:	星期三, 七月 30, 2003	Sheet 23 of 61

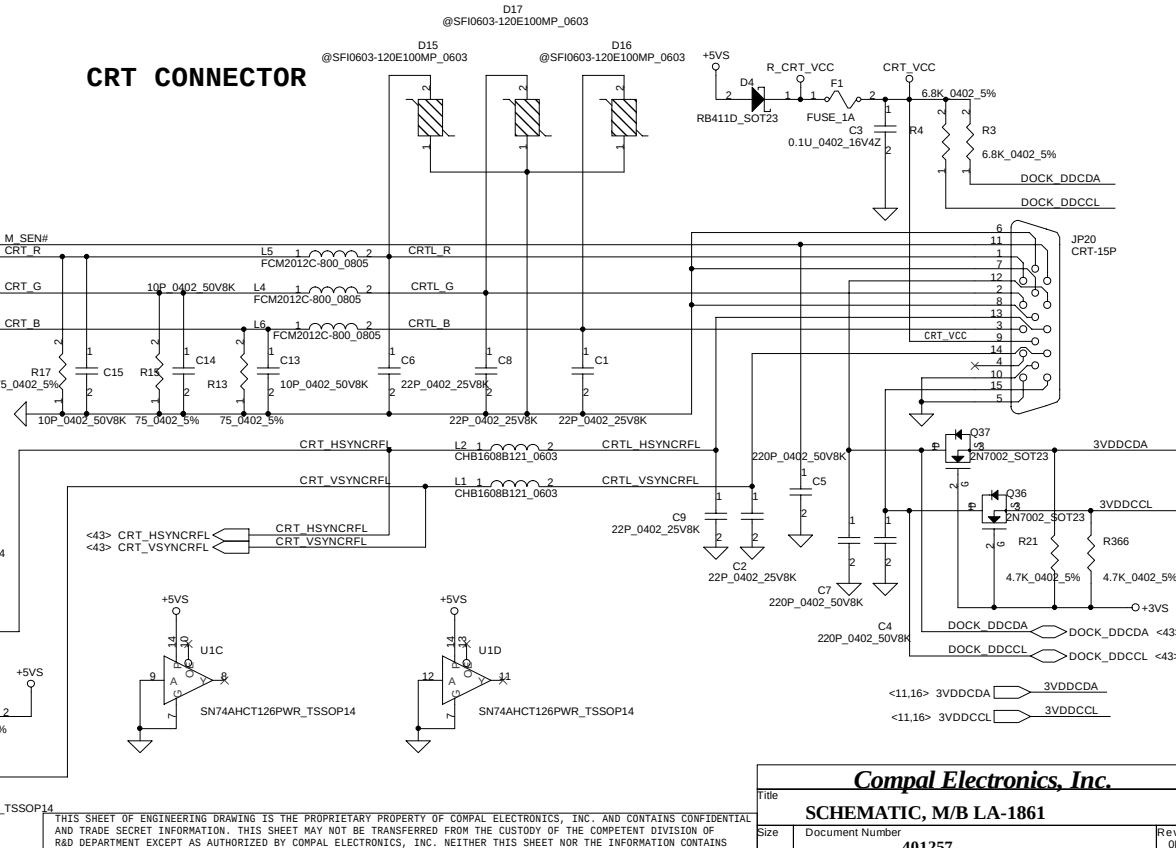
LCD CONN



TV_OUT CONNECTOR



CRT CONNECTOR

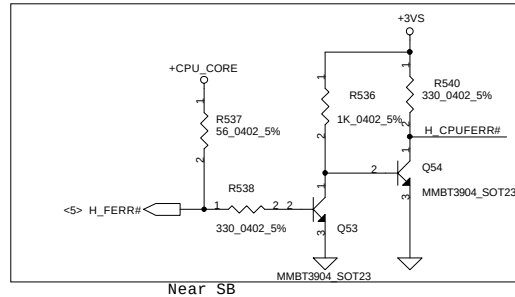


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SCHEMATIC, M/B LA-1861			
Size	Document Number	Rev	
Custom	401257	0E	
Date	星期三, 七月 30, 2003	Sheet	24 of 61

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<10,13> A_AD[0..31] A_AD[0..31]
<10> A_CBE#[0..3] A_CBE#[0..3]

Layout note:
Trace length of PCI_CLK_R + PCI_CLK_FB should
be less than 200 mils.



<23> CLK_ALINK_SB CLK_ALINK_SB
R207 8.2K 0402 5% NBRST#
PULL DOWN FOR S3

CLK_ALINK_SB
R200 10.0402 5%
C228 15P 0402 50V8D

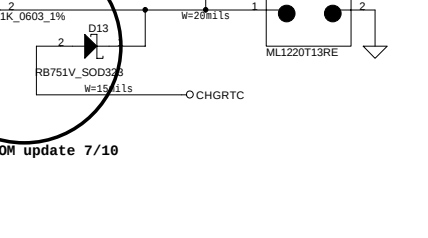
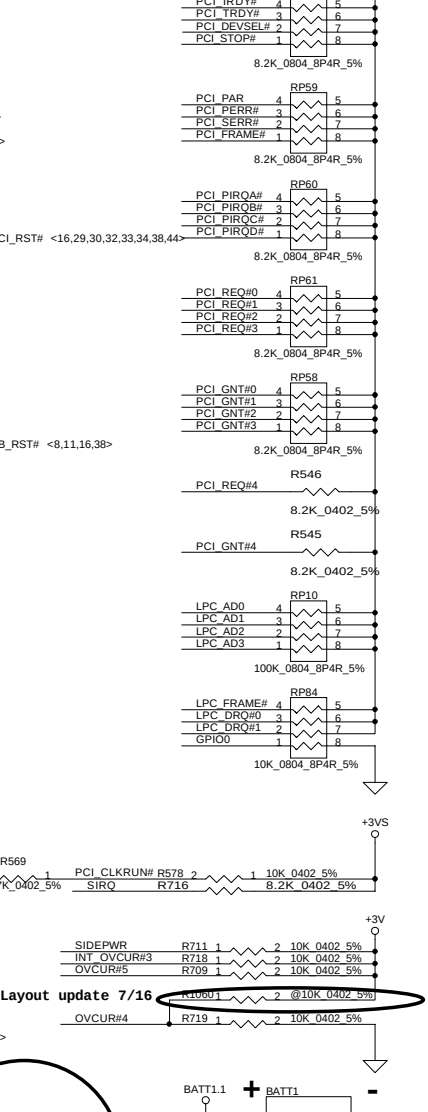
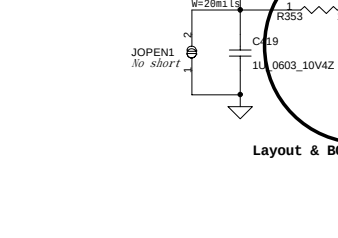
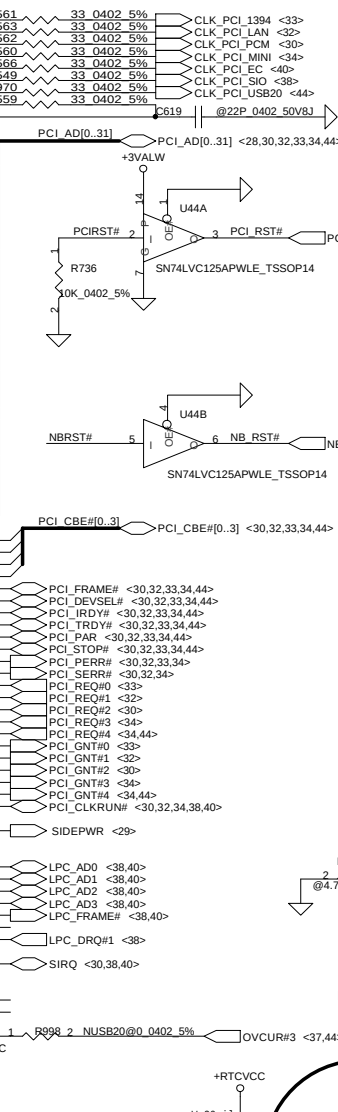
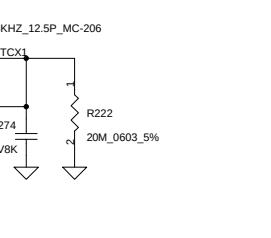
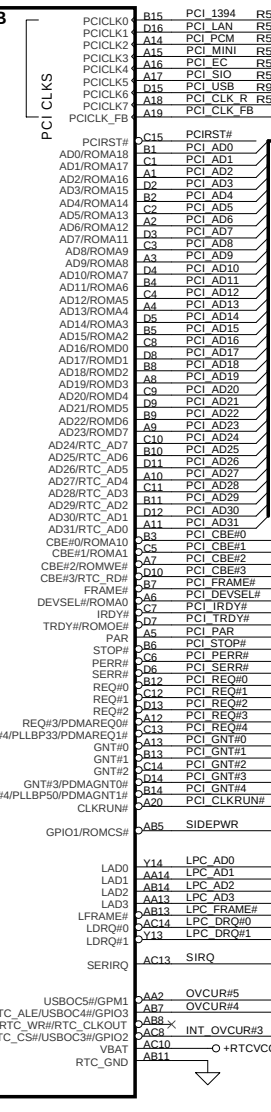
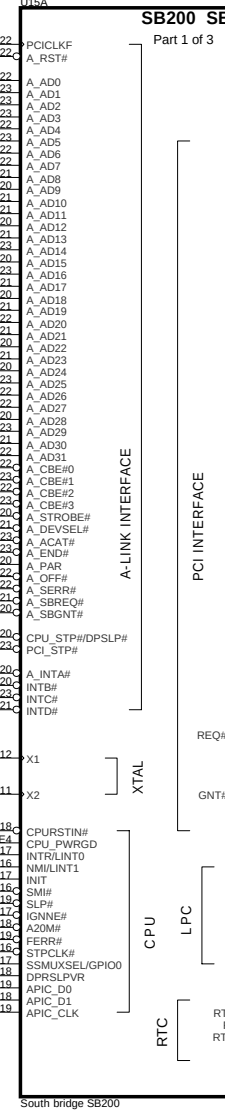
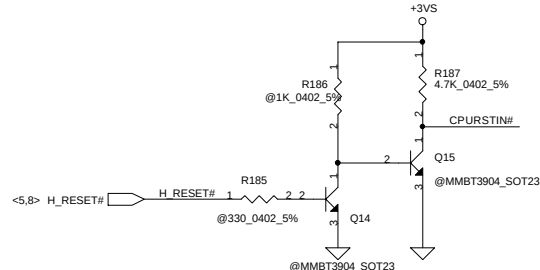
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<10> A_ACAT# A_ACAT#
<10> A_END# A_END#
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<10> A_OFF# A_OFF#
<10> A_SERR# A_SERR#
<10> A_SREQ# A_SREQ#
<10> A_SBGNT# A_SBGNT#

<5,11,28,53> CPUCLK_STP# CPU_STP#/#DPSLP#
<23> PCICLK_STP# PCICLK_STP#
<10,16,30,33,44> PCI_PIRQA# PCI_PIRQA#
<30,44> PCI_PIRQB# PCI_PIRQB#
<34,44> PCI_PIRQC# PCI_PIRQC#
<32,34> PCI_PIRQD# PCI_PIRQD#

H_INIT# R191 1 2 200 0402 5%
H_A20M# R193 1 2 200 0402 5%
H_INTR# R192 1 2 200 0402 5%
H_NMI# R189 1 2 200 0402 5%
H_SMI# R188 1 2 200 0402 5%
H_STPCLK# R195 1 2 200 0402 5%
H_IGNNE# R190 1 2 200 0402 5%

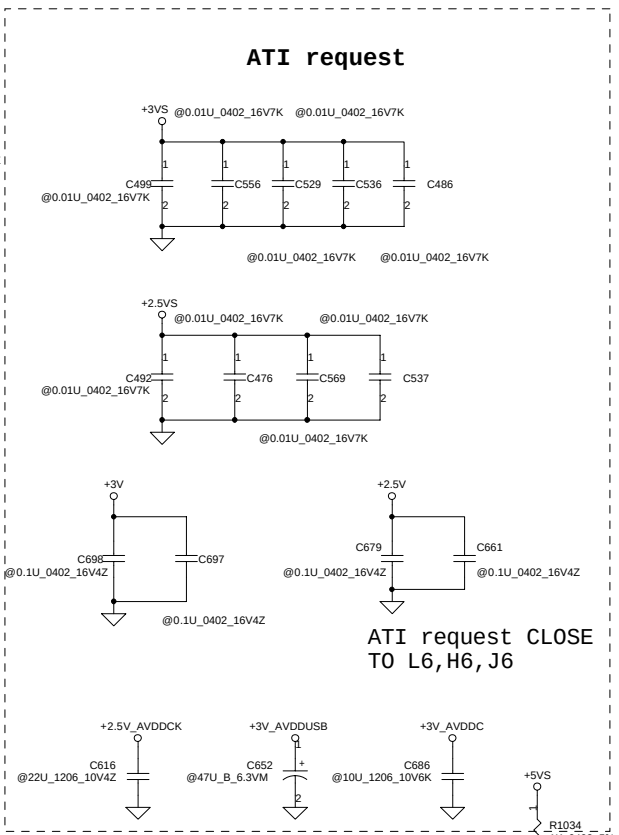
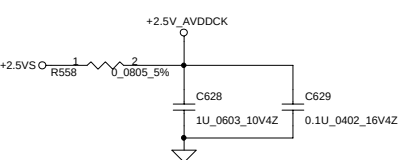
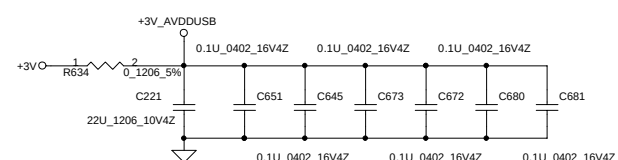
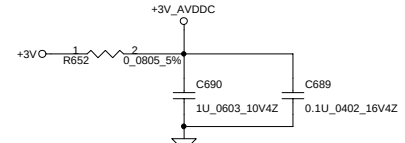
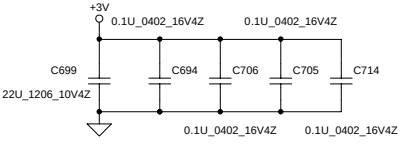
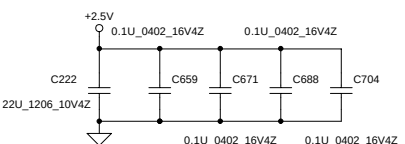
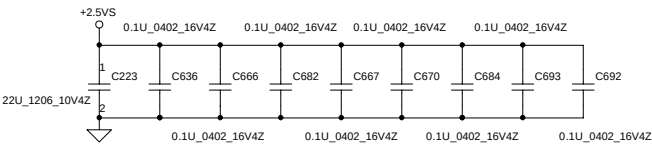
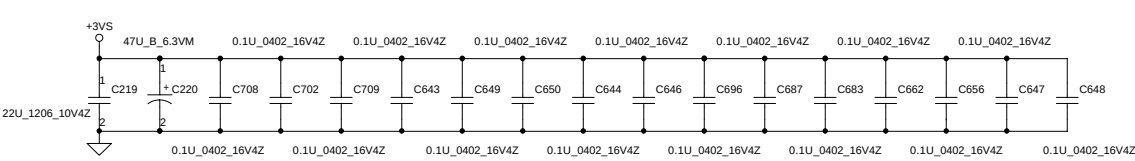
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H_INIT# C819 180P 0603 50V8J
H_INTR# C621 180P 0603 50V8J
H_NMI# C622 180P 0603 50V8J

PLACE CLOSE TO CPU SOCKET

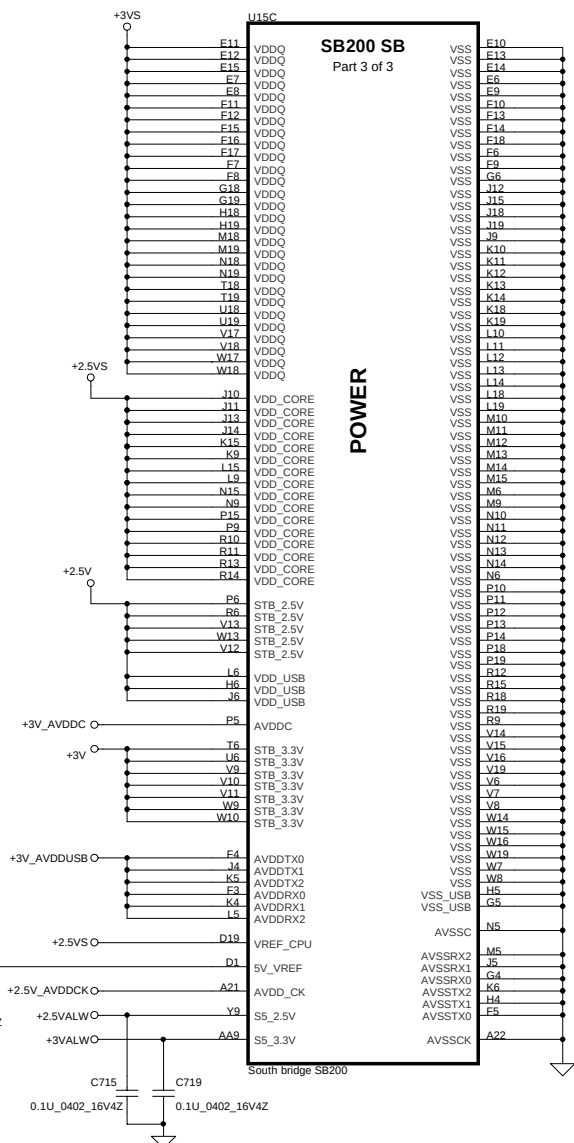


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SCHEMATIC, M/BLA-1861			
Title	Document Number	Rev	OE
	401257		
Date	星期三, 七月 30, 2003	Sheet	25 of 61

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ATI request CLOSE TO L6,H6,J6

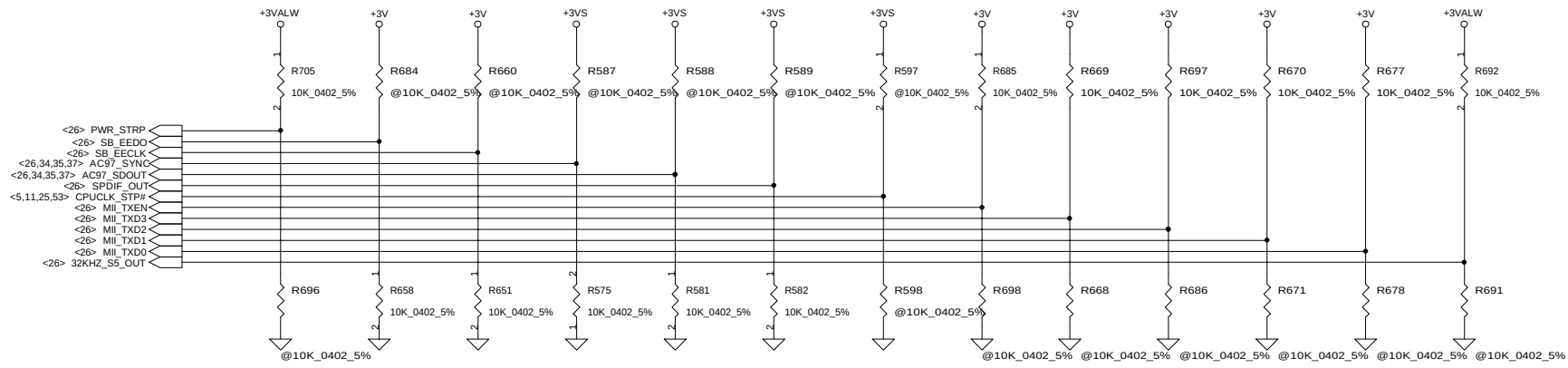


SB200 SB
Part 3 of 3

POWER

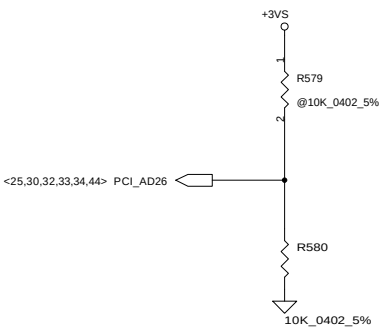
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Title			
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Size	Document Number	Rev	
	401257	OE	
Date:	星期三, 七月 30, 2003	Sheet	27 of 61

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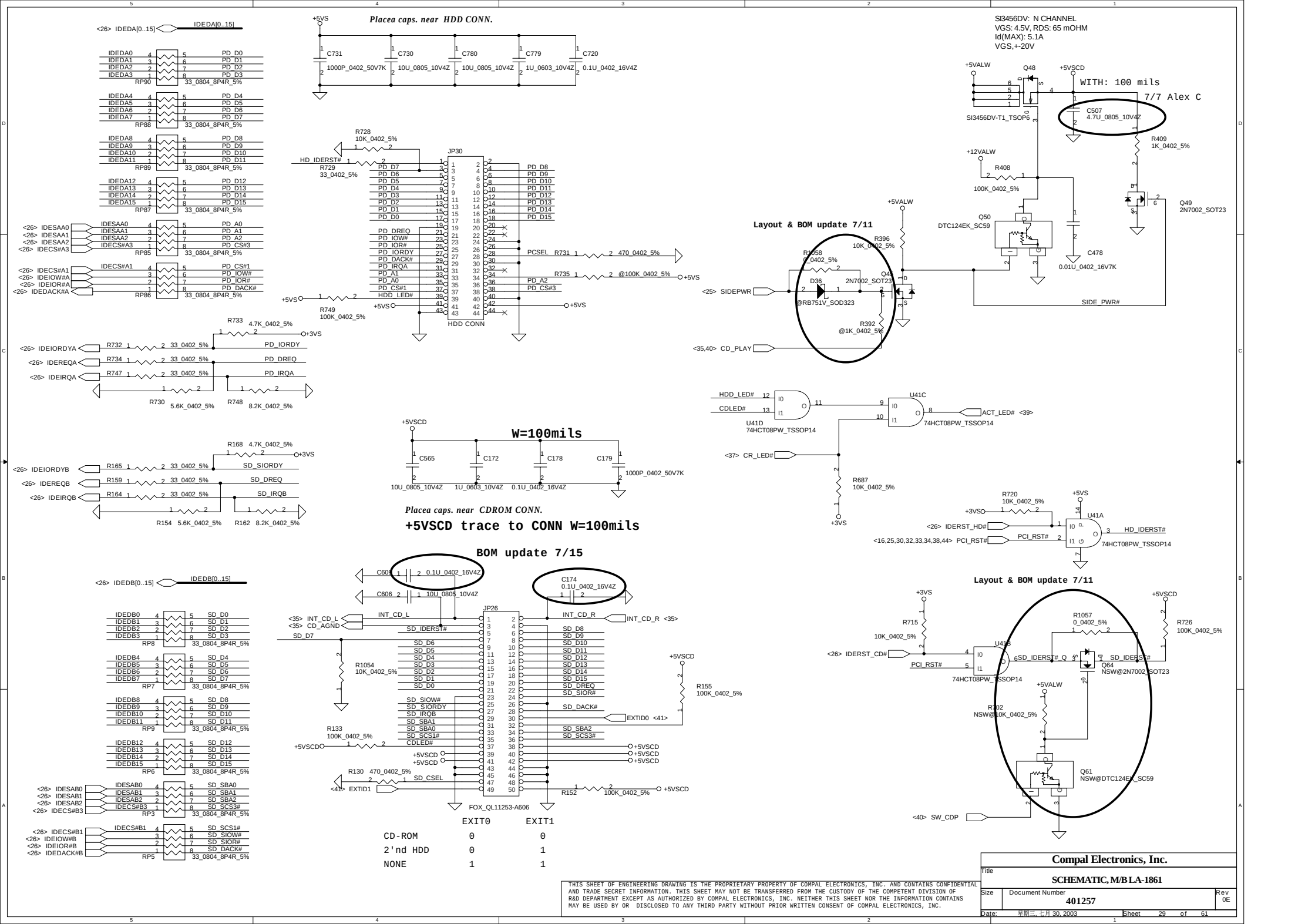


REQUIRED SYSTEM STRAPS

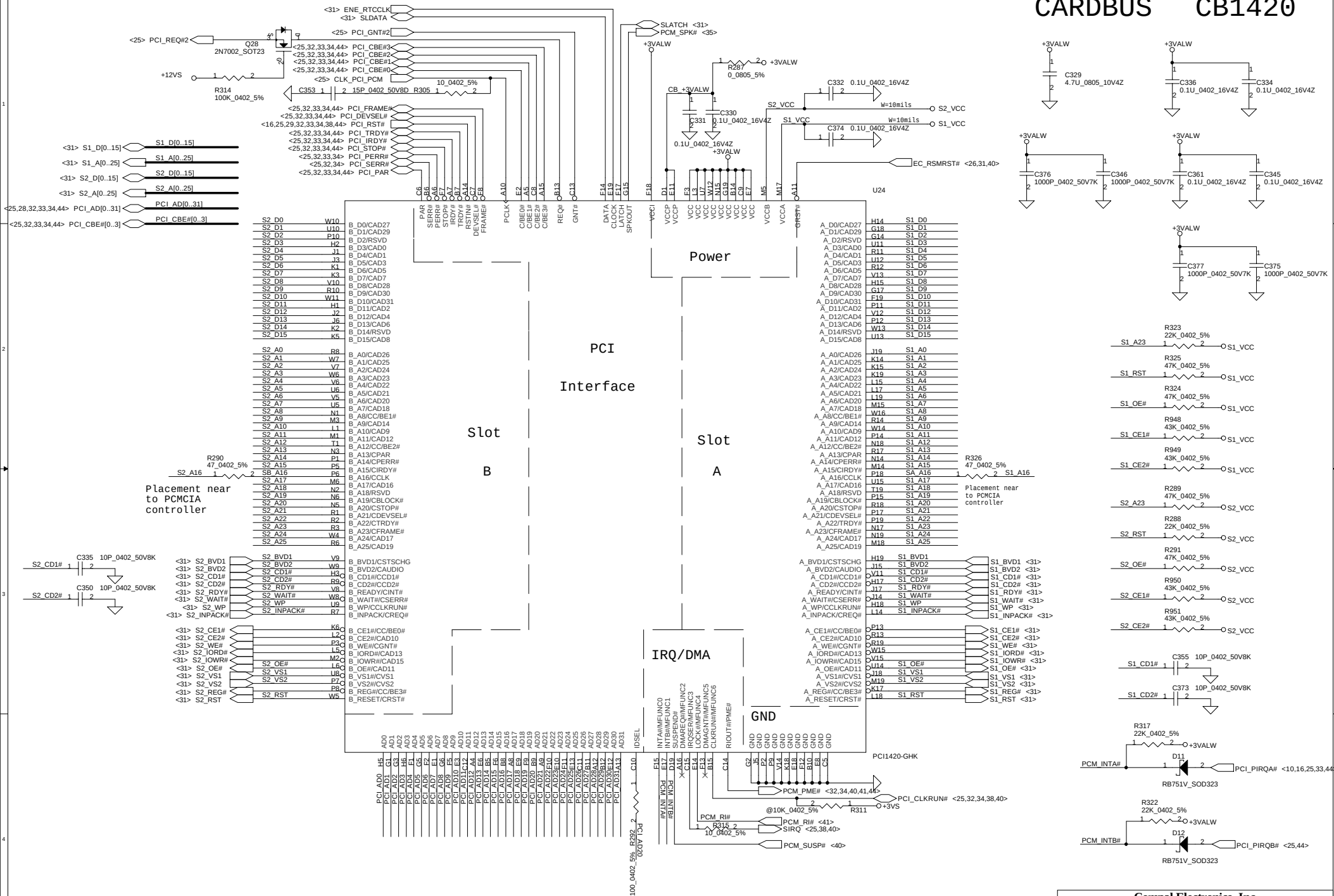
	PWR_STRP	IGN DEBUG EEDO	EECK	AC_SYNC	AC_SDOOUT	SPDIF_OUT	SPEEDSTEP CPU_STP#	FREQLTCH TX_EN	ETHERNET TXD[3:0]	32KHZ_S5
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	ROM ON PCI BUS DEFAULT	INIT ACTIVE HIGH	33MHz NB BUS DEFAULT	SIO 24MHz	ENABLE SPEED STEP	DISABLE CPU FREQ SETTING DEFAULT	PROCESSOR FREQ MULTIPLIER	32KHZ OUTPUT FROM SB200 (INT RTC) DEFAULT
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	ROM ON LPC BUS	INIT ACTIVE LOW (Piii) DEFAULT	HI SPEED A-LINK	SIO 48MHz DEFAULT	DISABLE SPEED STEP DEFAULT	ENABLE CPU FREQSETTING		32KHZ INPUT TO SB200 (EXT RTC)



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CARDBUS CB1420

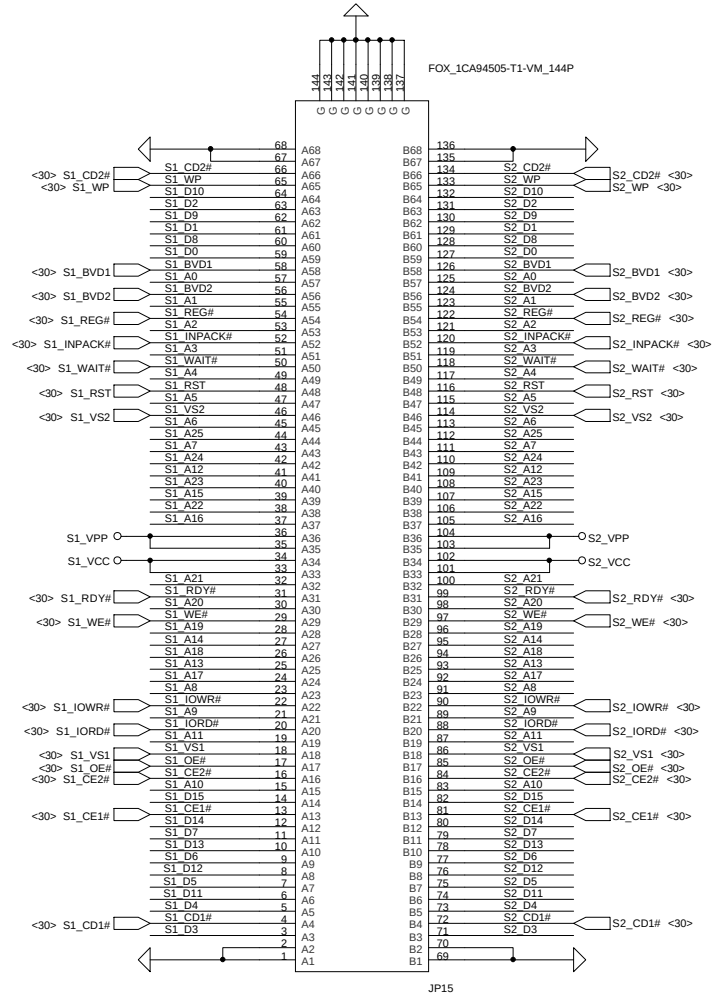
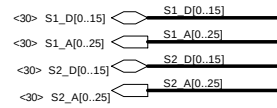


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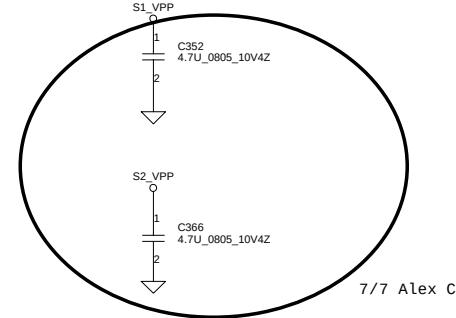
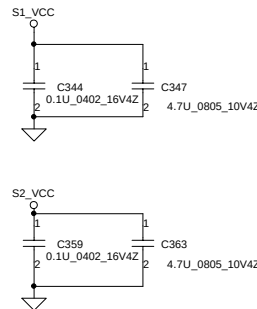
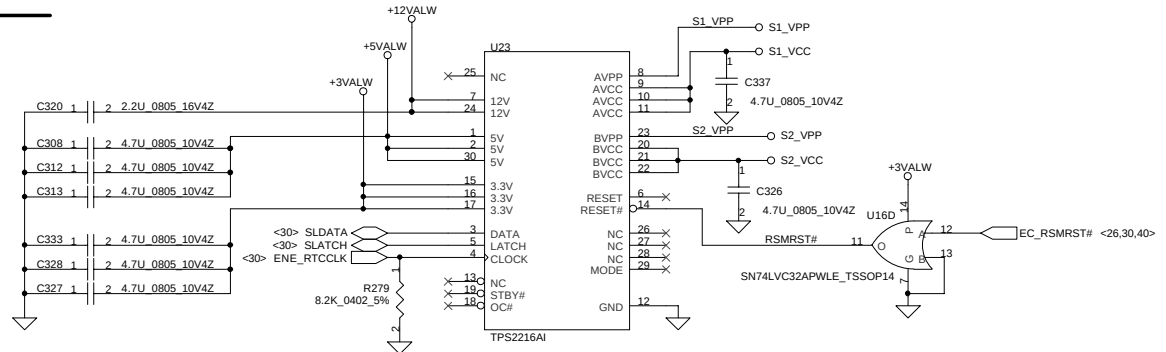
Compal Electronics, Inc.			
Title			
SCHEMATIC, M/B LA-1861			
Size	Document Number		Rev
	401257		0E
Date:	星期三, 七月 30, 2003	Sheet	30 of 61

CARDBUS

SOCKET

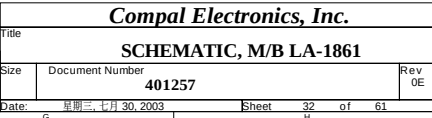


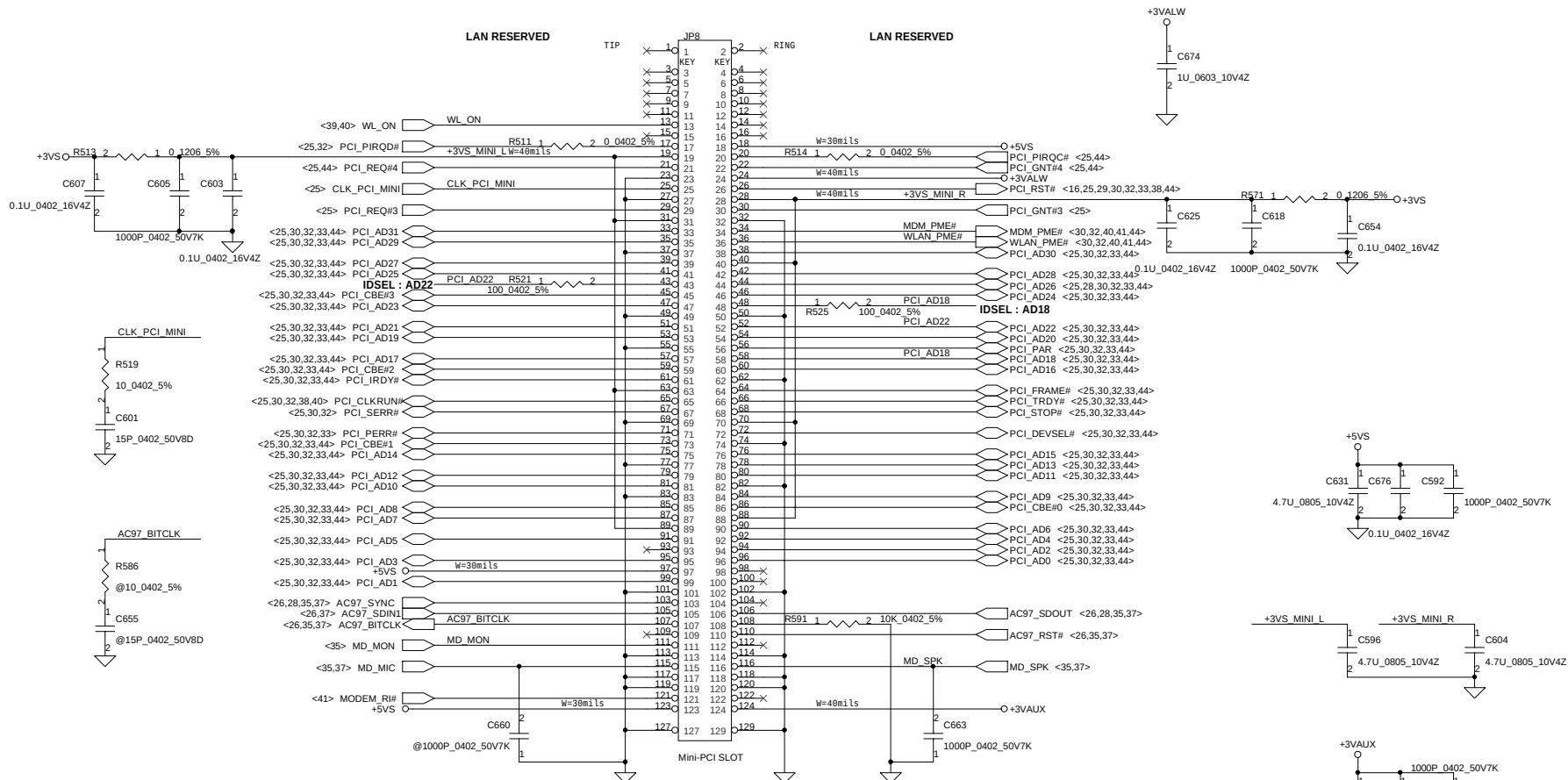
PCMCIA POWER CTRL.



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Title			
SCHEMATIC, M/BLA-1861			
Size	Document Number	Rev	
	401257	0E	
Date:	星期三, 七月 30, 2003	Sheet	31 of 61

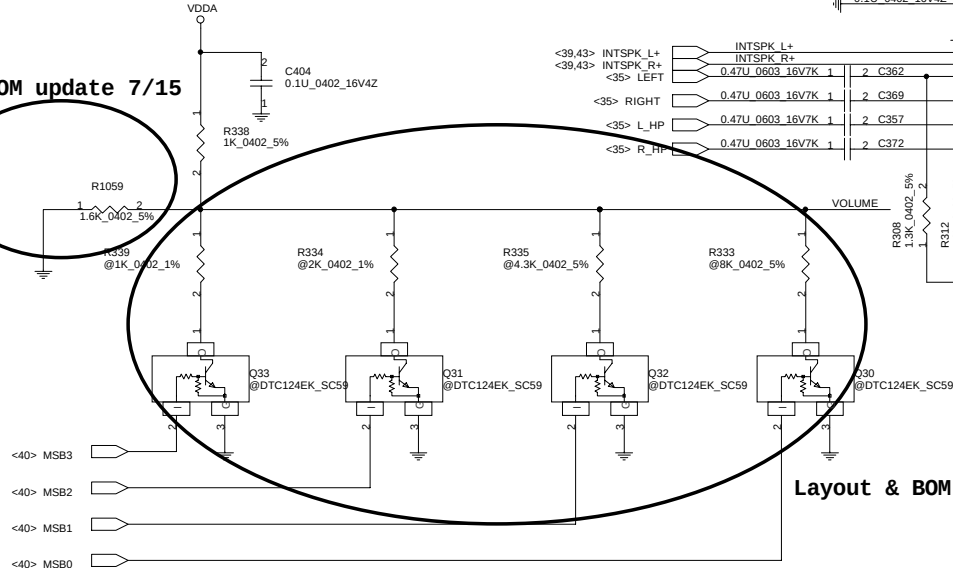




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Title			
SCHEMATIC, M/B LA-1861			
Size	Document Number	Rev	
	401257	0E	
Date:	星期三, 七月 30, 2003	Sheet	34 of 61

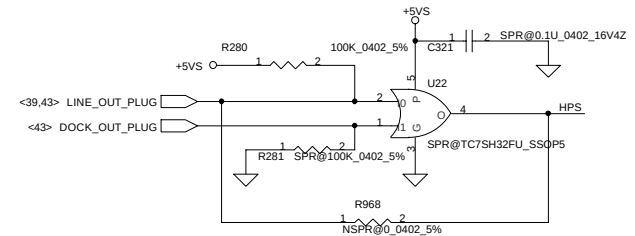
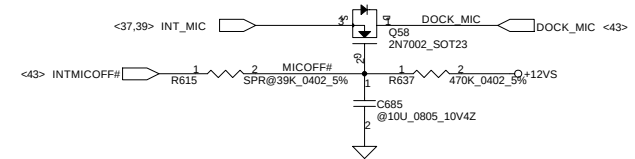
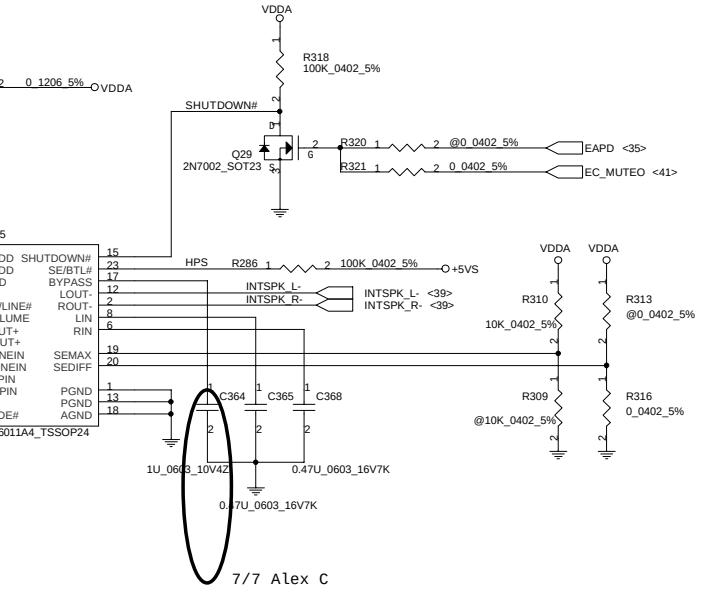
BOM update 7/15



Layout & BOM update 7/15

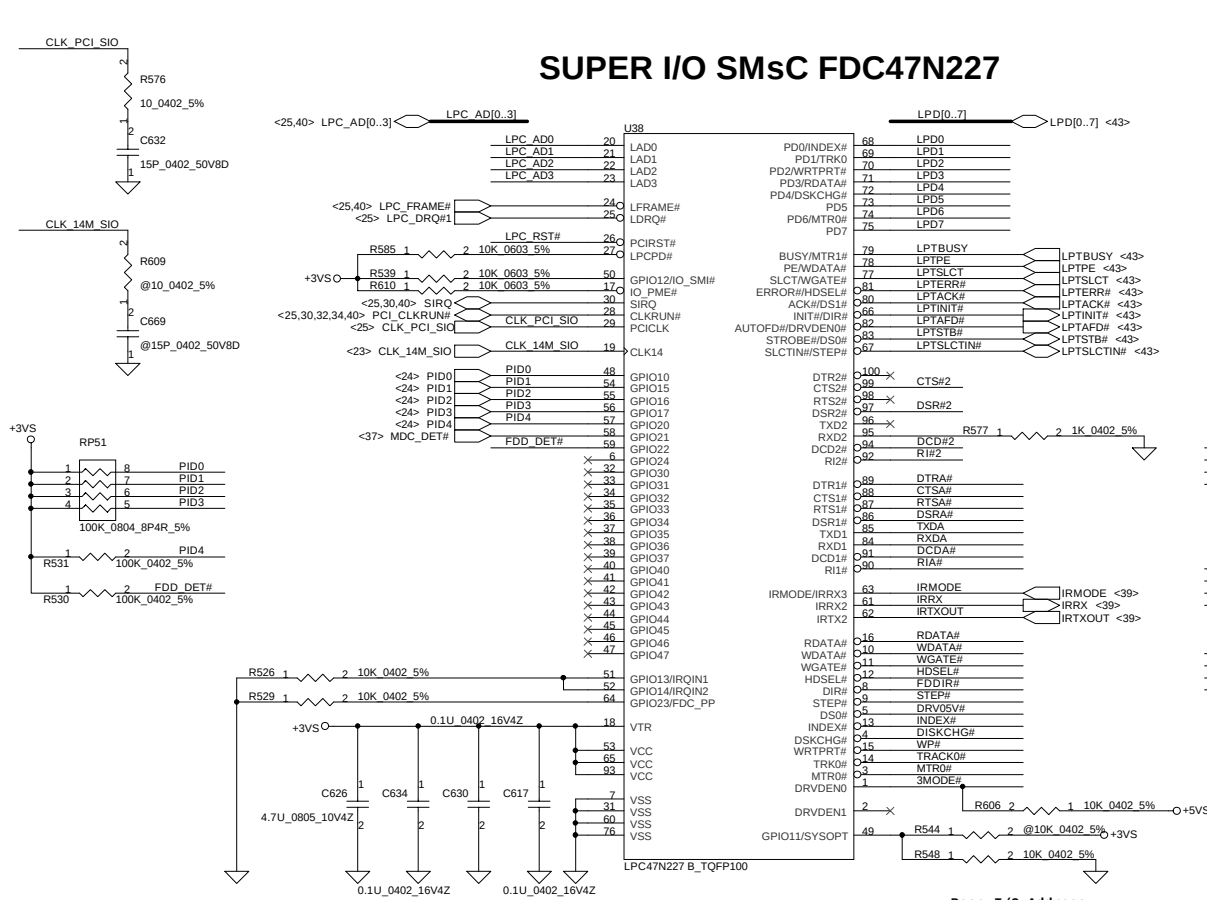
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0	0	0	1	4.7225	20	14
0	0	1	0	4.47	20	14
0	0	1	1	4.34	20	14
0	1	0	0	4.0485	20	14
0	1	0	1	3.86	20	14
0	1	1	0	3.719	20	14
0	1	1	1	3.56		
1	0	0	0	3.4	14	8
1	0	0	1	3.272	12	6
1	0	1	0	3.1659	10	4
1	0	1	1	3.05	8	2
1	1	0	0	2.938	6	0
1	1	0	1	2.84		
1	1	1	0	2.76		
1	1	1	1	2.67		

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Title			
SCHEMATIC, M/B LA-1861			
Size	Document Number	Rev	
	401257	0E	
Date:	星期三, 七月 30, 2003	Sheet	36 of 61

SUPER I/O SMsC FDC47N227

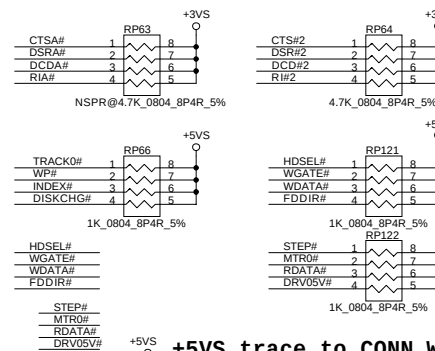
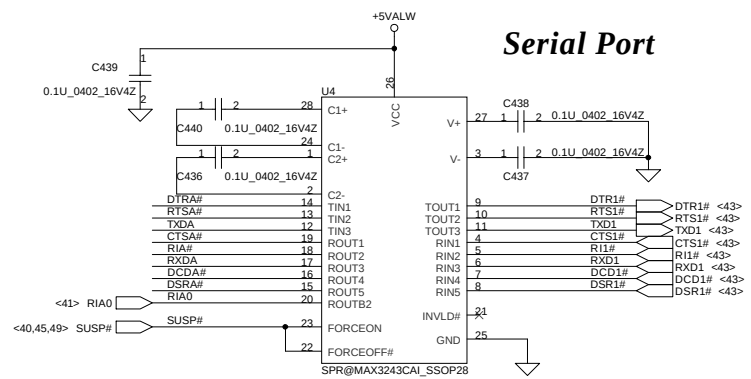


Base I/O Address

0 = 02Eh

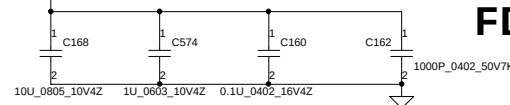
* 1 = 04Eh

Serial Port

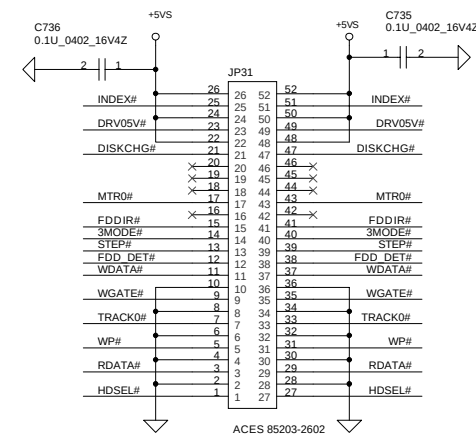


+5VS trace to CONN W=100mils

FDD CONN.



Placea caps. near FDD CONN.



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Title	SCHEMATIC, M/B LA-1861
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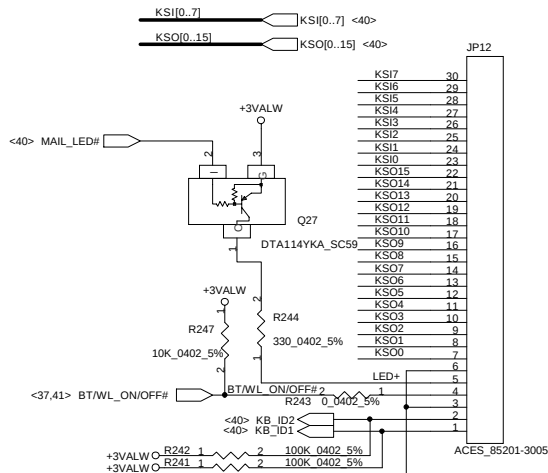
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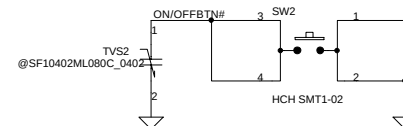
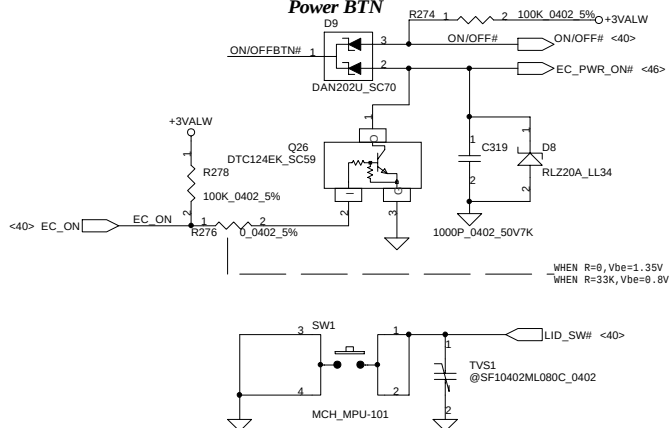
Date:	星期三, 七月 30, 2003	Sheet	38	of	61
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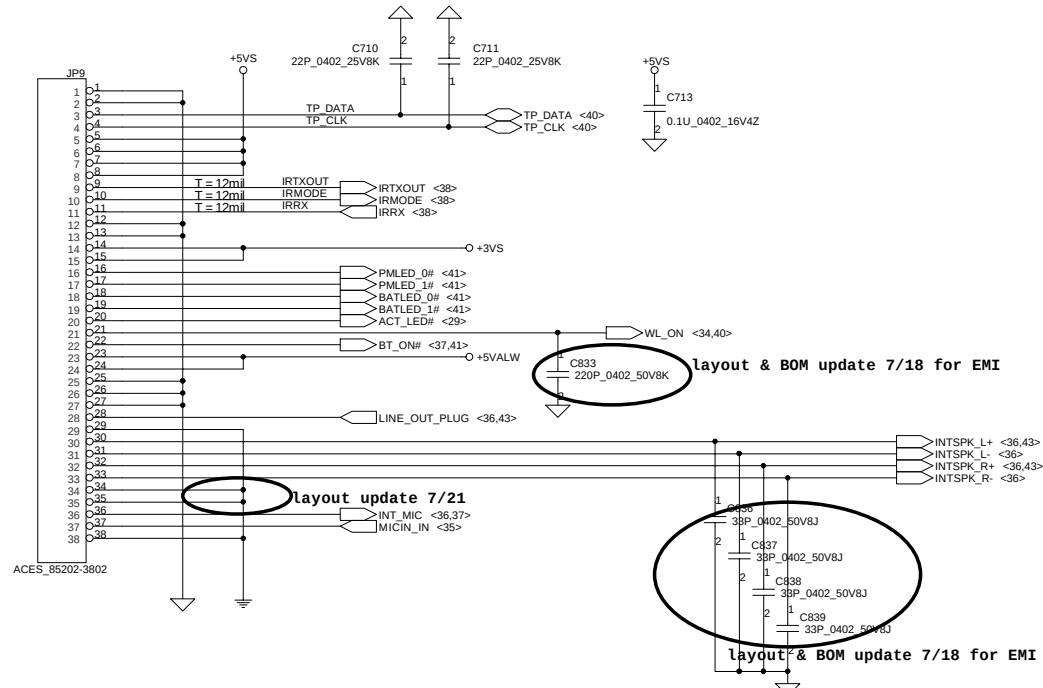
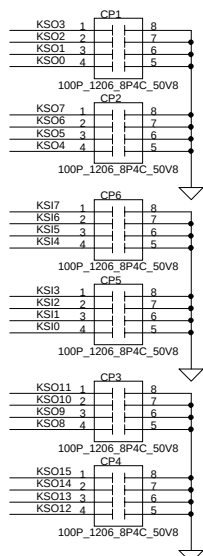
INT_KBD CONN.



Power BTN



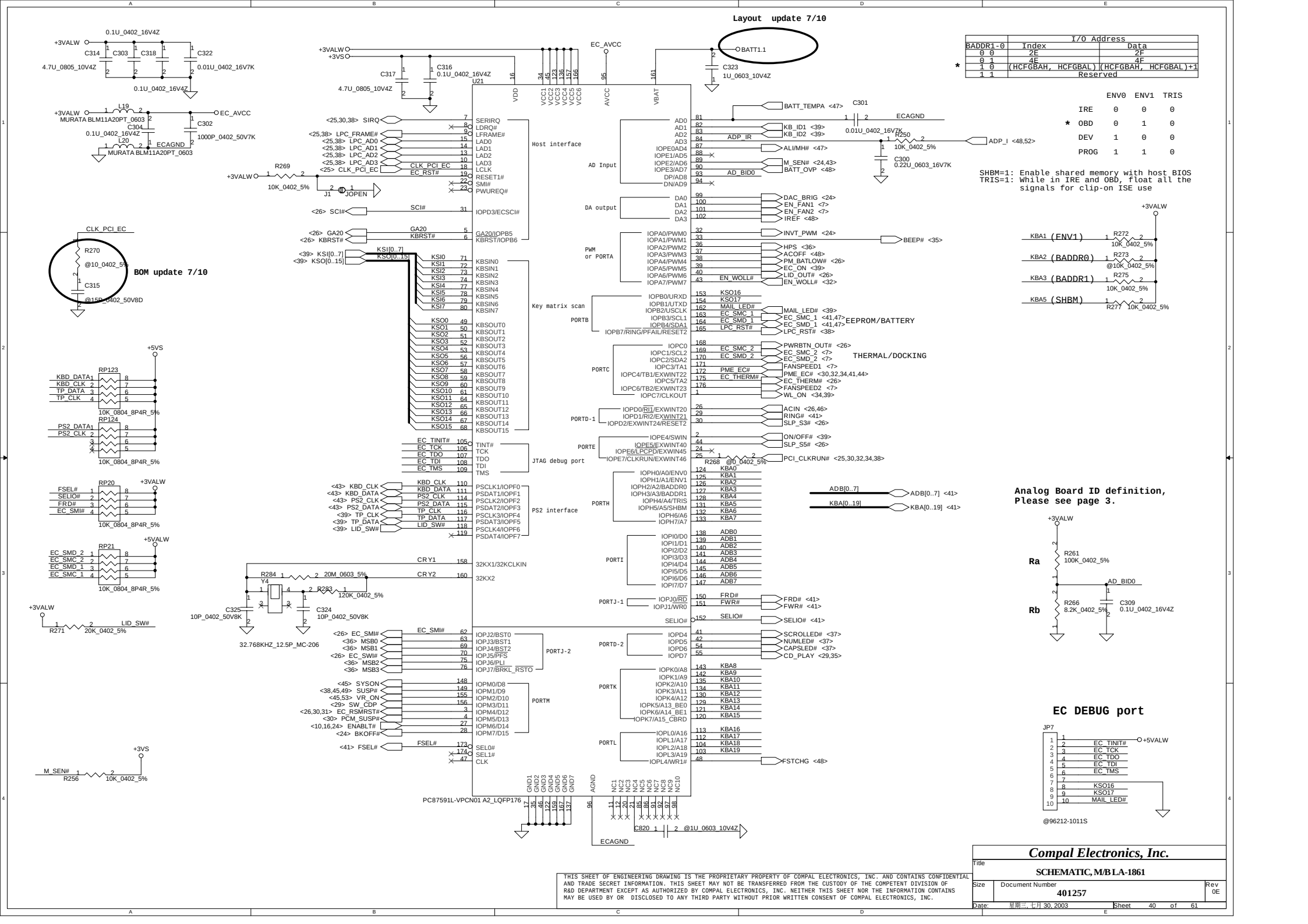
Touch Pad & Status LED Conn.

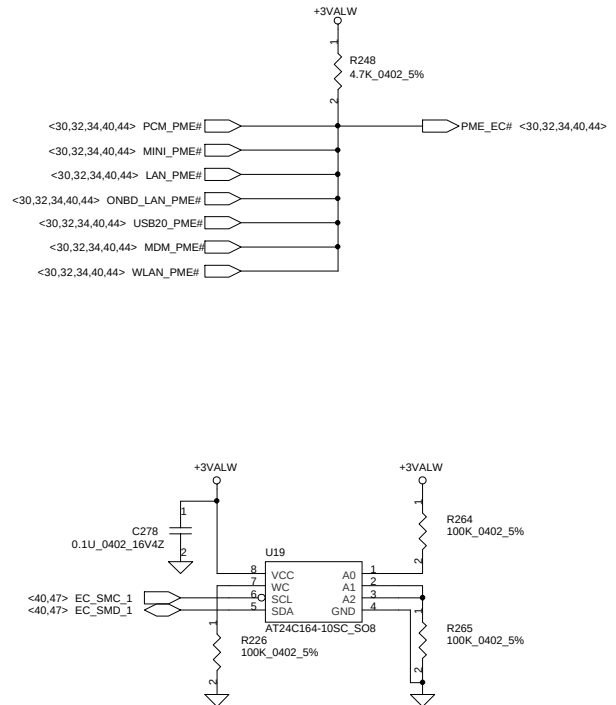
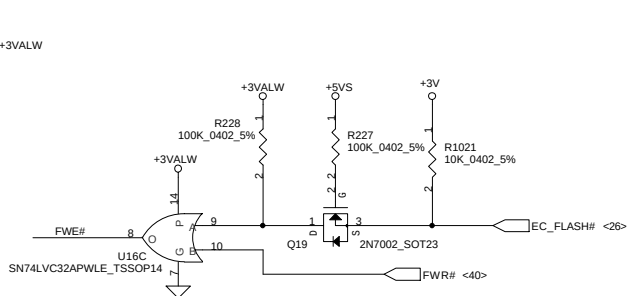
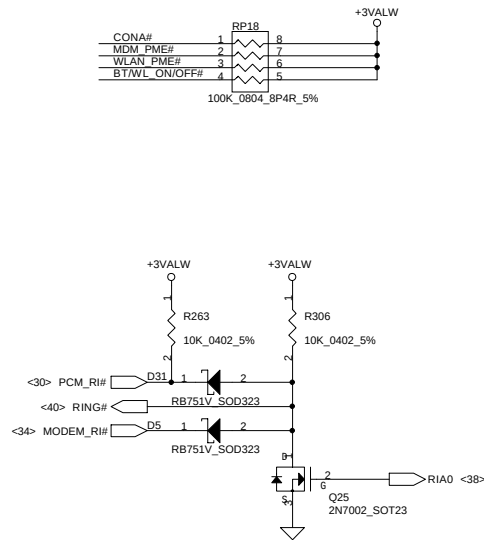


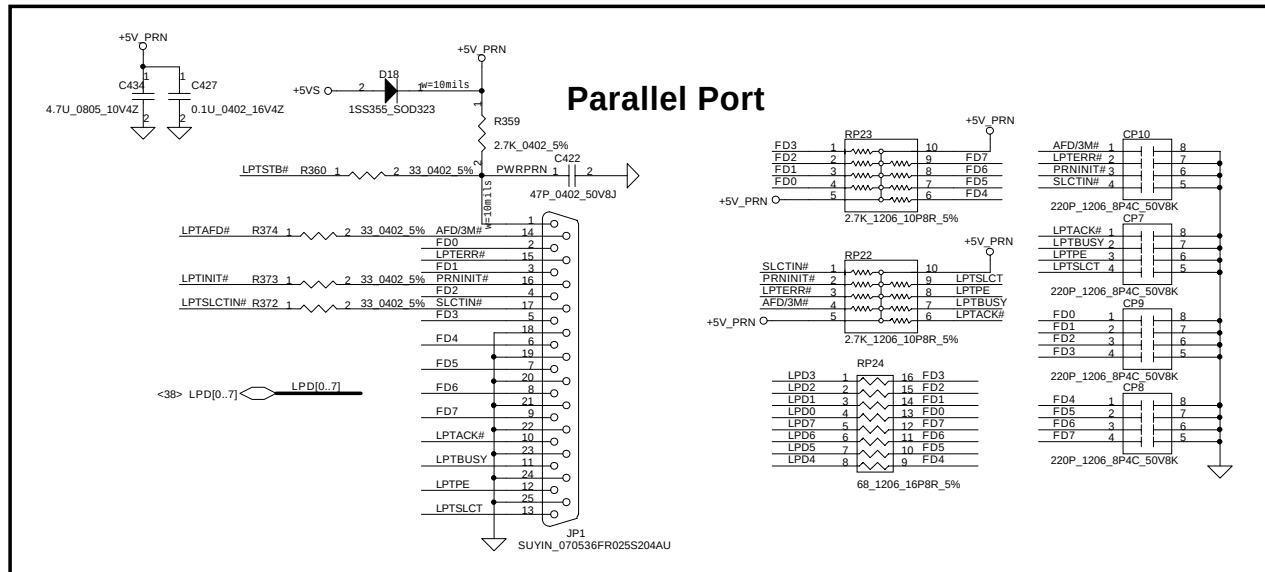
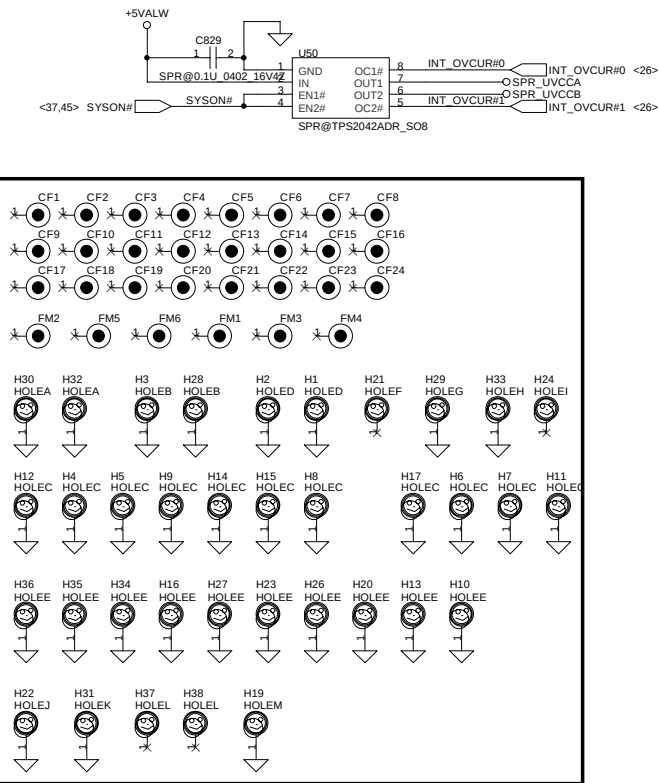
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Title			
SCHEMATIC, M/BLA-1861			
Size	Document Number	Rev	
	401257	0E	
Date:	Rev	Sheet	of
2003.07.30	三	39	61

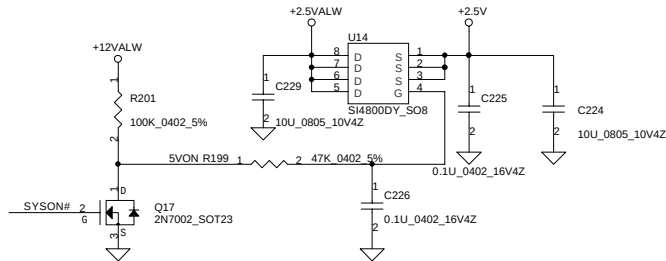
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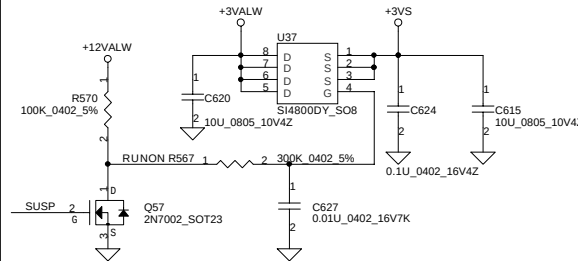




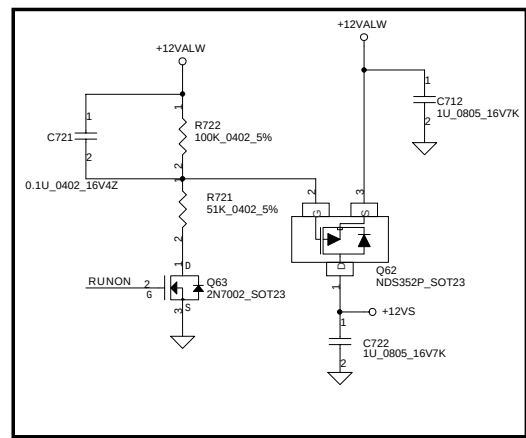
+2.5VALW to +2.5V Transfer



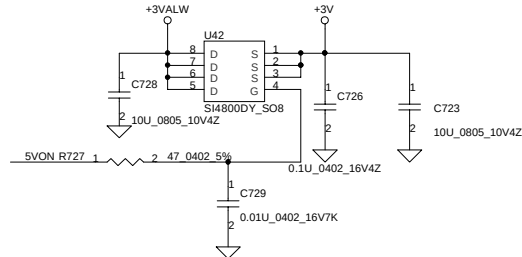
+3VALW to +3VS Transfer



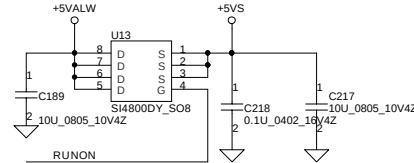
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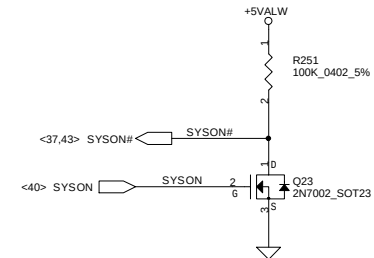
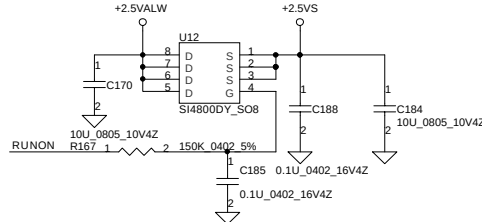
+3VALW to +3V Transfer



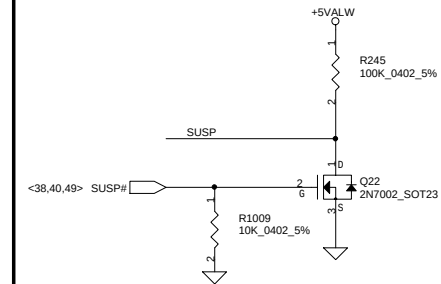
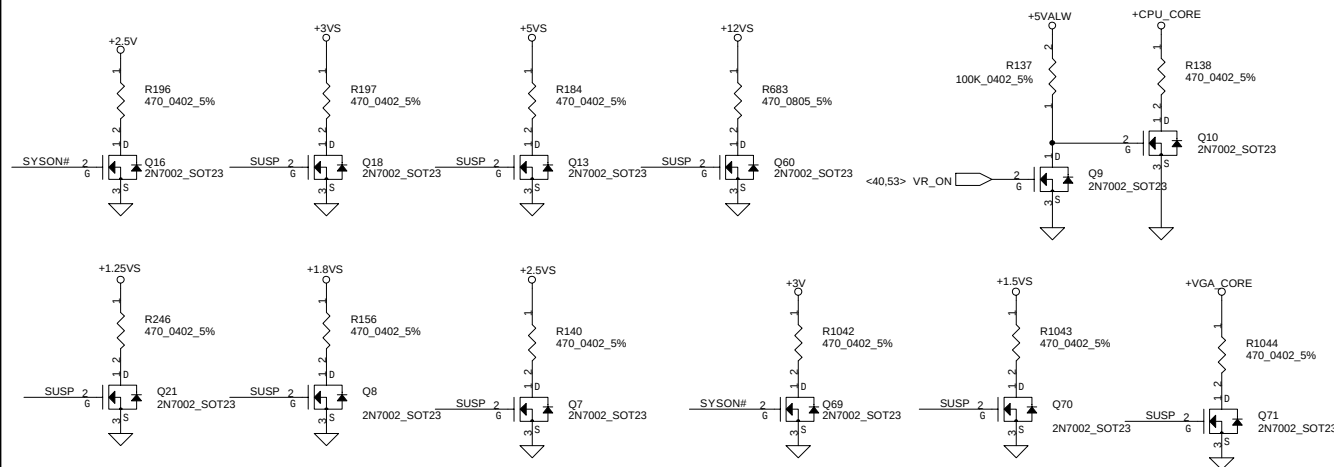
+5VALW to +5VS Transfer



+2.5V to +2.5VS Transfer

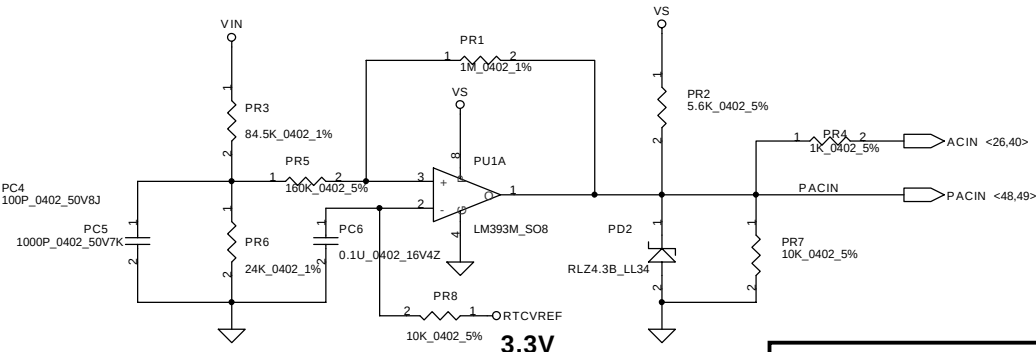
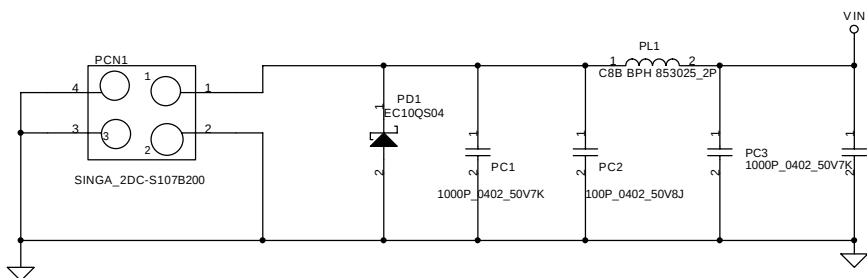


Discharge circuit



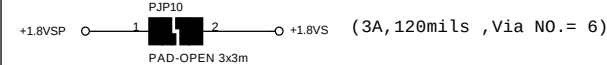
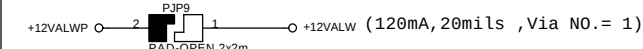
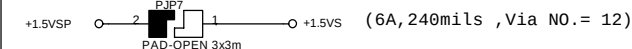
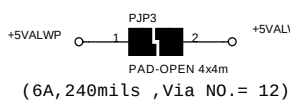
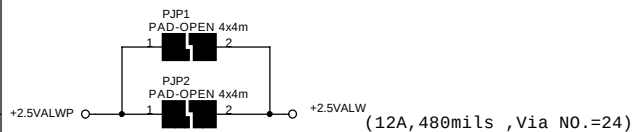
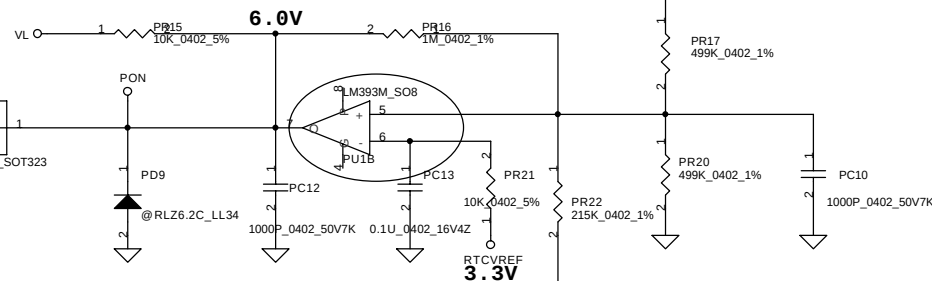
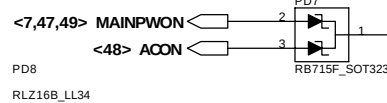
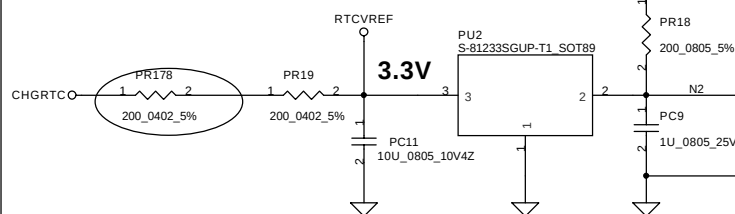
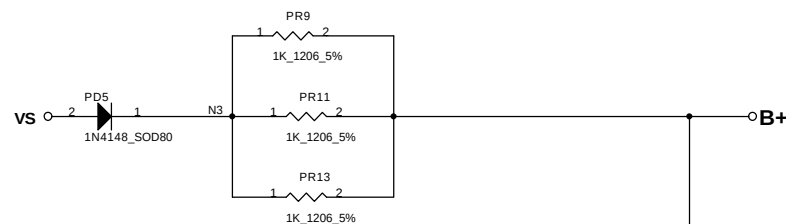
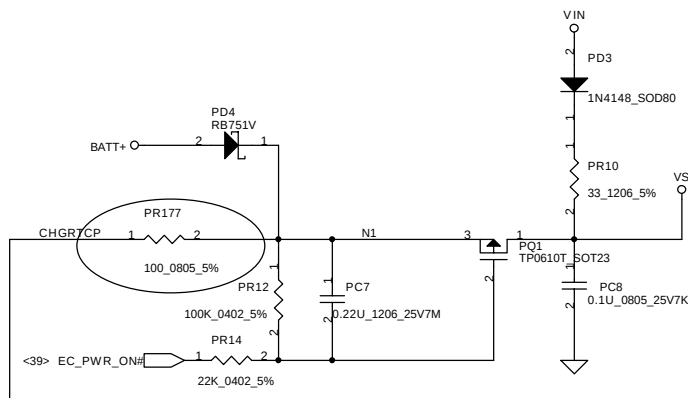
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Title			
SCHEMATIC, M/B LA-1861			
Size	Document Number	Rev	
	401257	0E	
Date:	星期三, 七月 30, 2003	Sheet	45 of 61



Vin Detector

High 17.58
Low 14.11



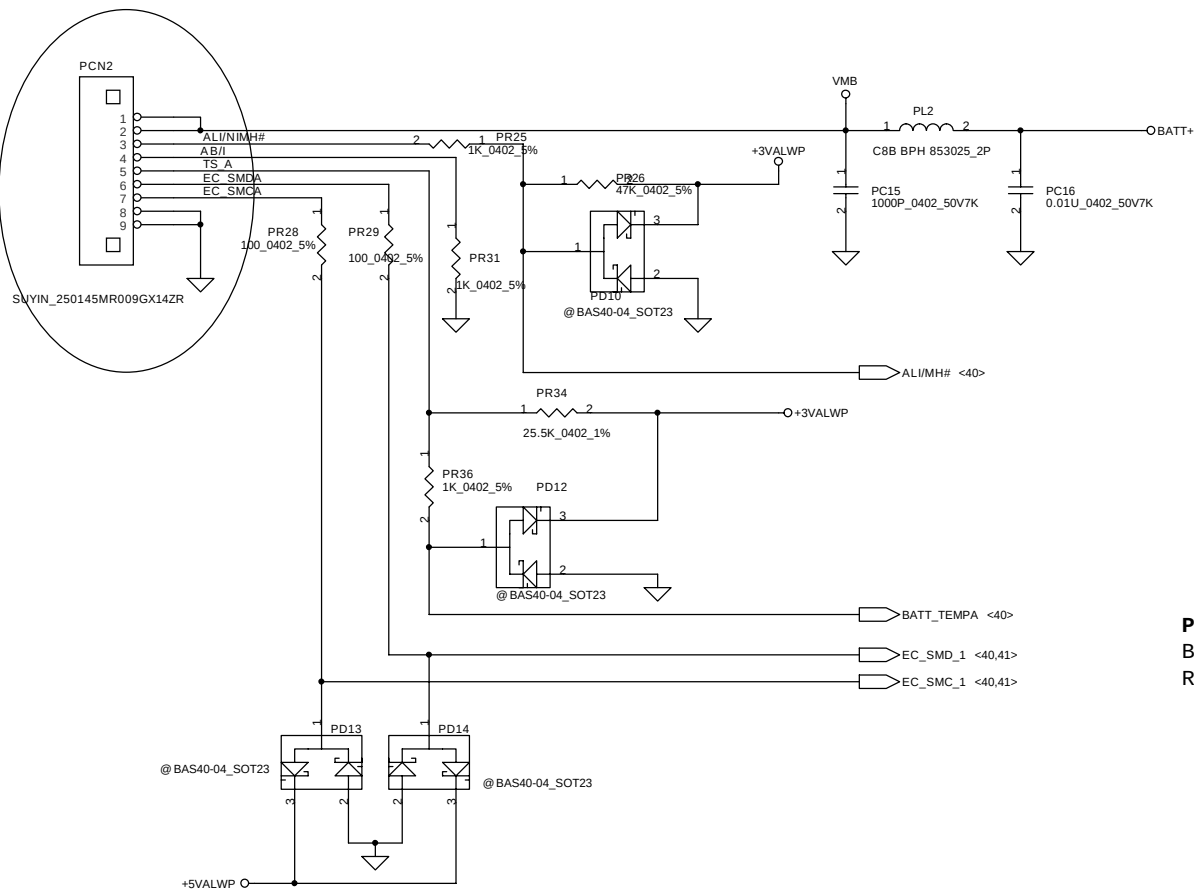
Precharge detector

15.34 15.90 16.48
13.13 13.71 14.20

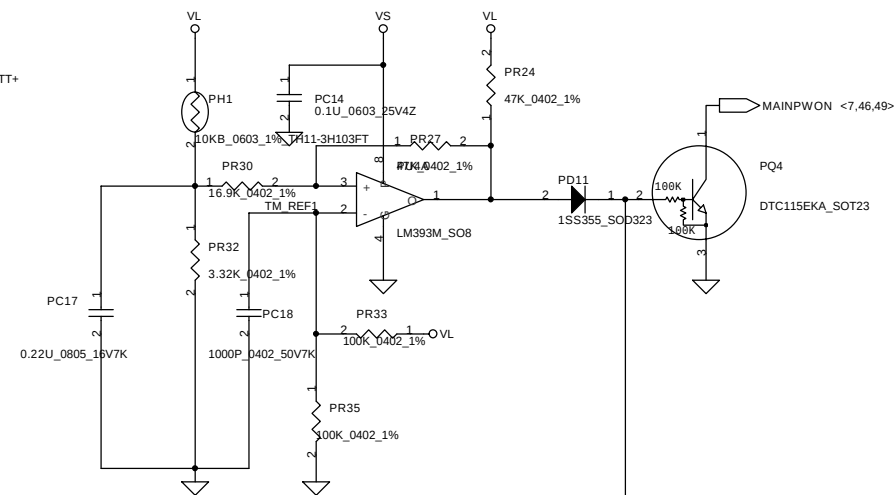
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Title			
SCHEMATIC, M/BLA-1861			
Size	Document Number		Rev
	401257		0E
Date:	~P圖三, 七月 30, 2003		Sheet 46 of 61

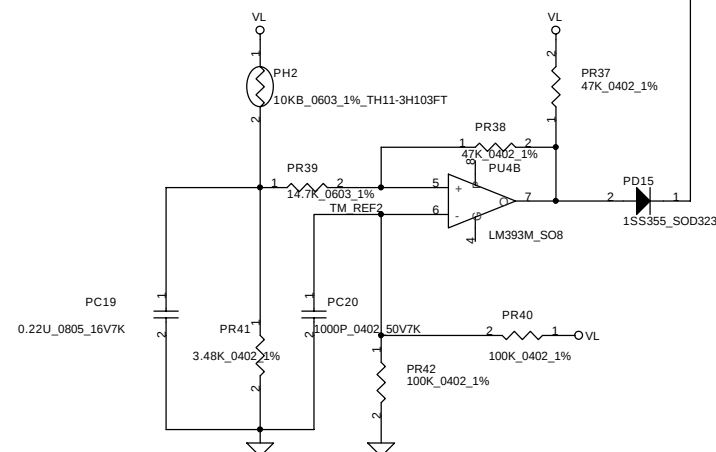
CHANGE CONNECTER



PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C

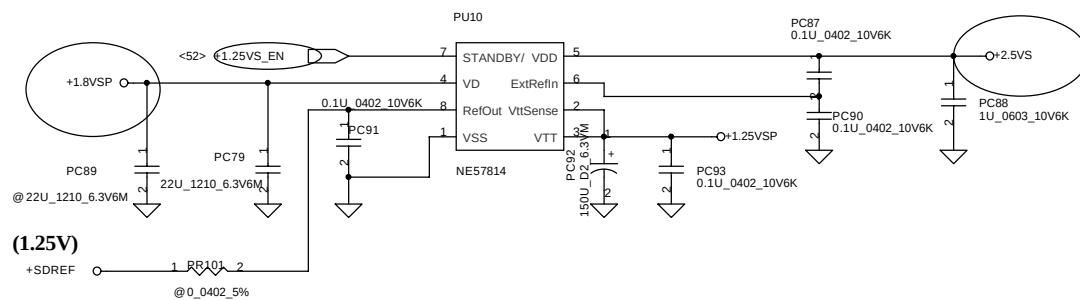
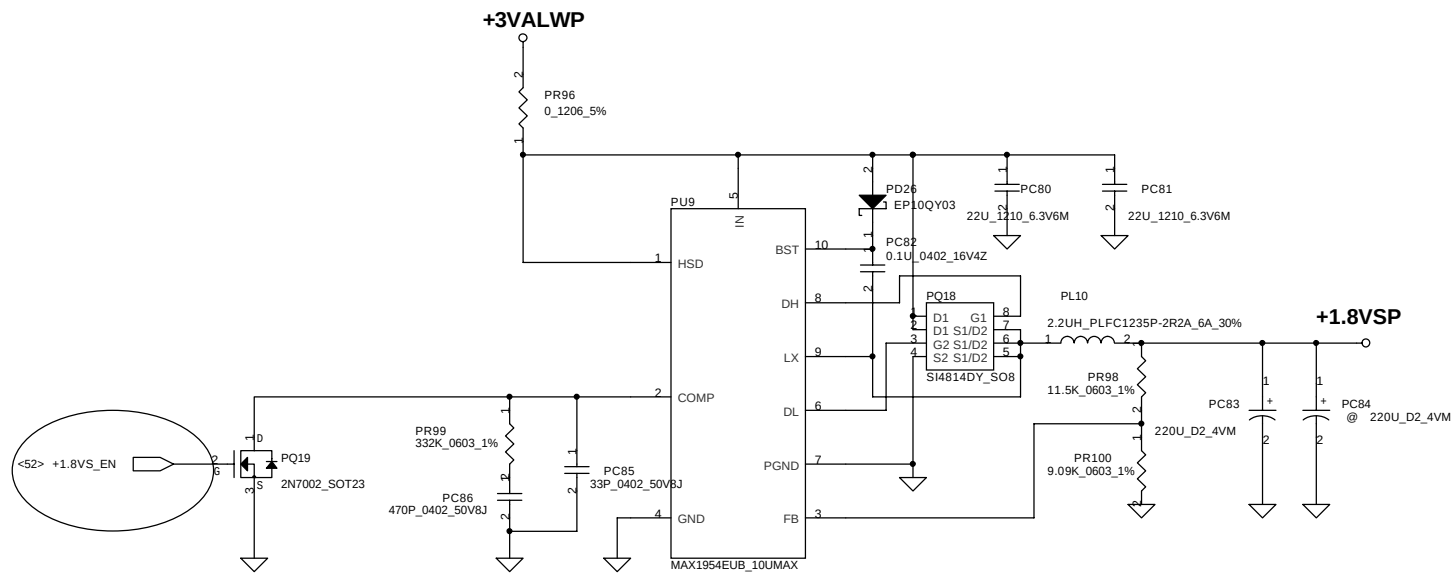


PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C



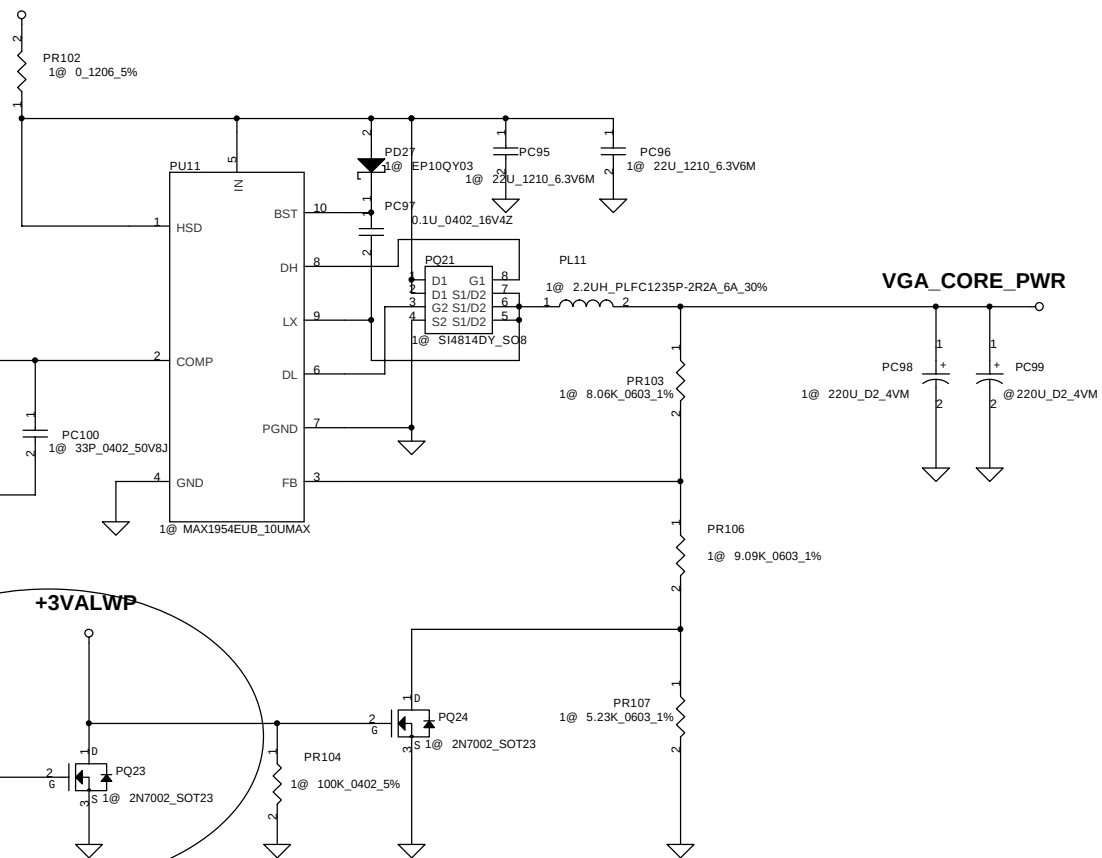
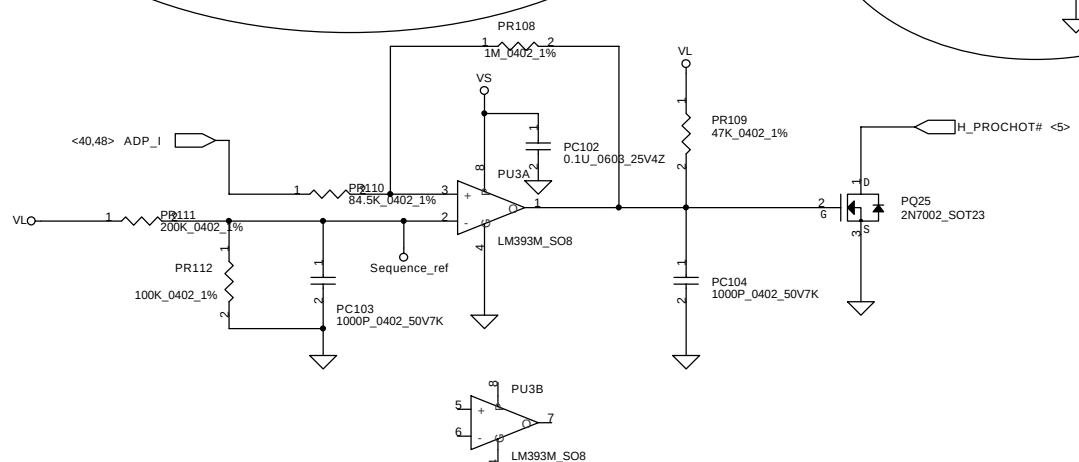
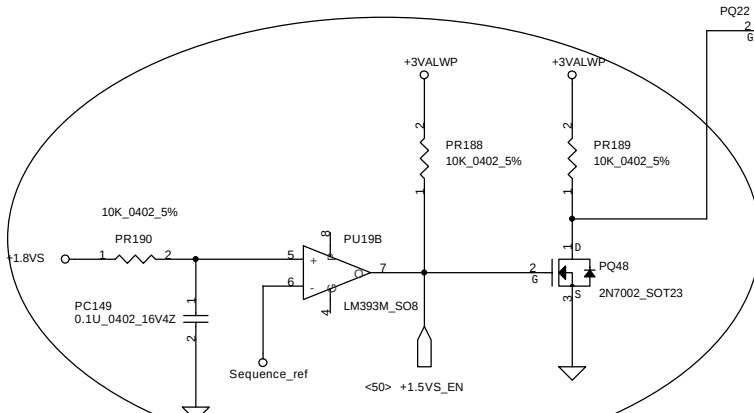
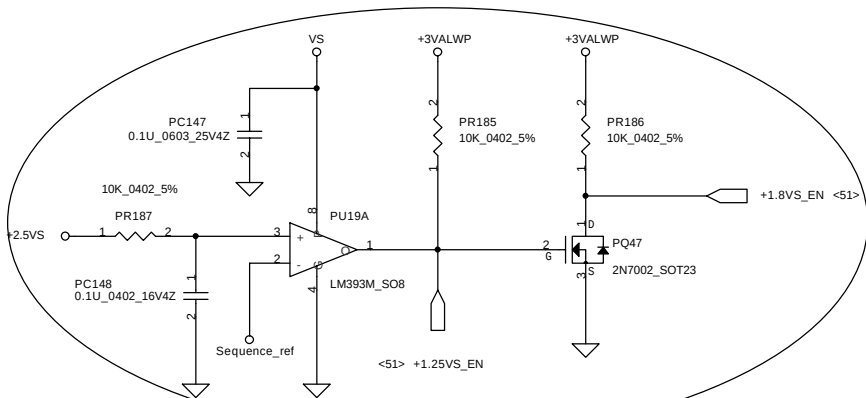
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Title		SCHEMATIC, MBLA-1861	
Size	Document Number	401257	
Date:	~P圖三, 七月 30, 2003	Sheet	47 of 61



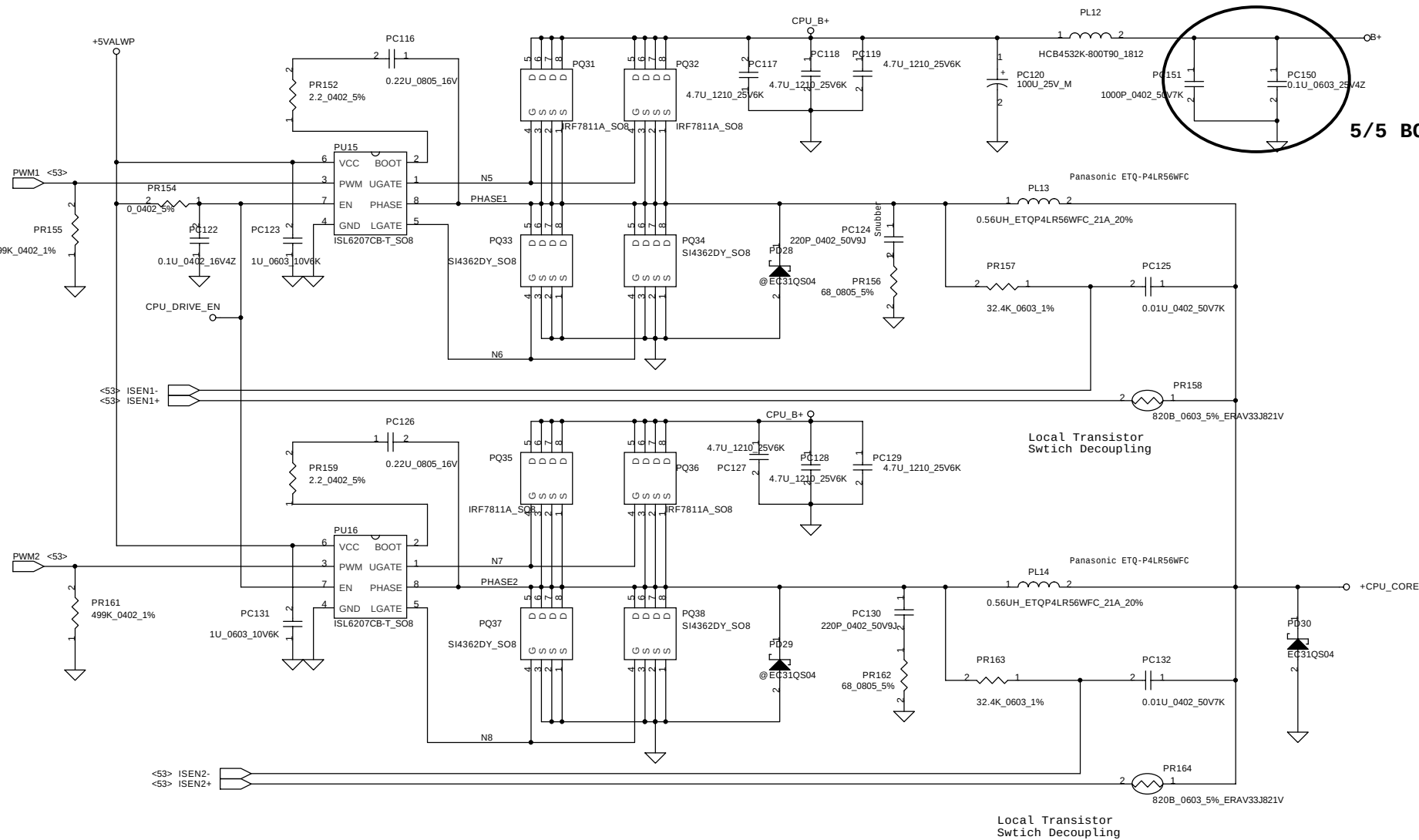
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Title			
SCHEMATIC, M/BLA-1861			
Size	Document Number		R ev
	401257		0E
Date:	~P版三, 七月 30, 2003		Sheet 51 of 61



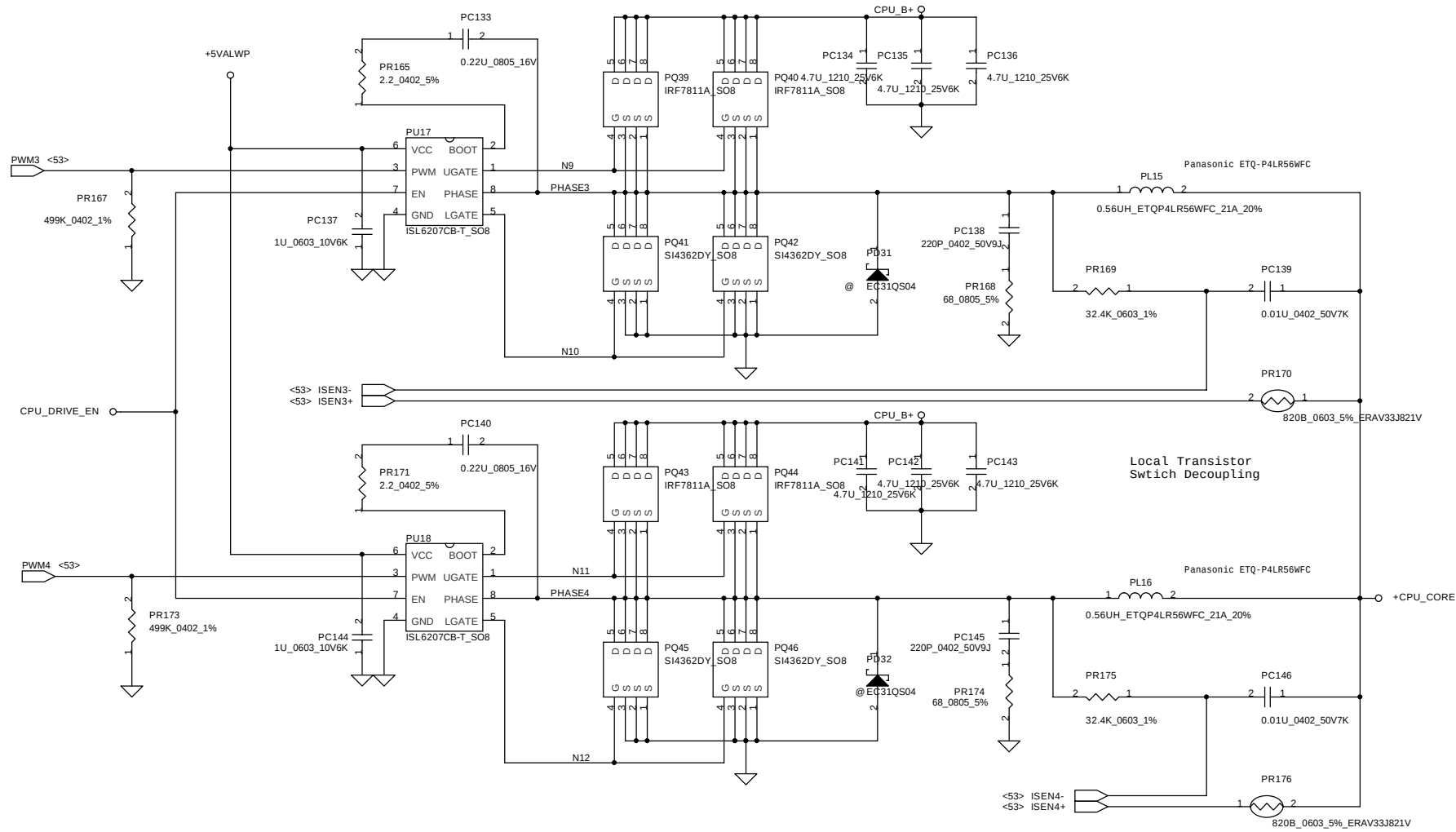
POWER_SEL	VGA_CORE for M9+	
L	1.5V	PR103 = 8.06K_0603_1%
H	1.25V	PR107 = 5.23K_0603_1%

POWER_SEL	VGA_CORE for M10P	
L	1.2V	PR103 = 4.64K_0603_1%
H	1.0V	PR107 = 4.87K_0603_1%



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Title		SCHEMATIC, M/BLA-1861	
Size	Document Number	Rev	
	401257	0E	
Date:	~P圖四 七月 31, 2003	Sheet	54 of 61



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Title			
SCHEMATIC, M/BLA-1861			
Size	Document Number		Rev
	401257		0E
Date:	~P圖四 七月 31, 2003		Sheet 55 of 61

MODIFY PIR LIST

1. Modify the Block Diagram for schematic page swap . (Page 2)
2. Modify ATI chip related schematic for recomend demo schematic and layout action . (Page 8~23)
2. Modify LAN chip related schematic for Model SPEC changed . (Page 33,34)

For B test

2003/4/10

1.Modify Q48 join to C507 (Page 29)

2003/4/15

1.SGA19471D00 470u 2.5V D4 change to SGA20471D00 470u 2.5V D2

2003/4/22

- 1.Page5 change R23/R139 footprint and form 51.1_0402 to 51.1_0603(BOM&layout update)
- 2.Page7 net name FANSPEED1 and FANSPEED2 swap(layout update)
- 3.Page8 change R132 from 49.9_0402 to 24.9_0402(BOM update)
- 4.Page8 change R134 from 24.9K_0402 to 49.9_0402(BOM update)
- 5.Page10 change R958.1 contact to AGP_SBA0(BOM&layout update)
- 6.Page10 change R959.1 contact to AGP_SBA1(BOM&layout update)
- 7.Page10 new add R963/R964 2.2K_0402(BOM&layout update)
- 8.Page10 new add R969 0_0402 for ATI INTA# issue(BOM&layout update)
- 9.Page10 new add R1005 4.7K_0402 pull-high +1.8VS for internal VGA Vref power(BOM&layout update)
- 10.Page11 change R84 to 0_0402 and R88 to 68_0603(BOM update)
- 11.Page12 R104 for external VGA, R102 for internal VGA(BOM control)
- 12.Page13 New add D32/D33 RB751V, Add R147(BOM update)
- 13.Page13 del R146/R493(layout update)
- 14.Page13 R476/R150 change to @(BOM update)
- 15.Page13 R475/R151 change to Pop(BOM update)
- 16.Page16 new add R1002/R1003 for VGA 128M DRAM(BOM&layout update)
- 17.Page17 U7.F20 new add trace NMCSA1#
- 18.Page18 U7.R6 new add trace NMCSB1#
- 19.Page23 change R666 from 33_0402 to 68_0402, change R699/R703 from 1K_0402 to 10K_0402, change R689/R700 from 10K_0402 to 4.7K_0402(BOM update)
- 20.Page23 new add D34/D35 RB751V(BOM&layout update)
- 21.Page24 chnage U1.14 from CRT_VCC to +5VS(layout update)
- 22.Page24 chnage R5.2 from GND to +5VS(layout update)
- 23.Page25 del R717 and RP84.1 contact to GPIO0(layout update)
- 24.Page25 chnage R718.1 contact to INT_OVCUR#3(layout update)
- 25.Page25 add R998 0_0402(BOM&layout update)
- 26.Page25 add R970 22_0402 for add external USB2.0 PCI clock (BOM&layout update)
- 27.Page26 add R1004 10K_0402 for VCORE_PWRGD pull-high +3V(BOM&layout update)
- 28.Page26 del RP11 and add R961/R962 10K_0402(BOM&layout update)
- 29.Page26 add R999/R1000/R1001 0_0402 for extrenal ovcur option(BOM&layout update)
- 30.Page29 Q48 pin1.2.5.6/R396.2/R702.1 contact to +5VALW for sw_cdplay power(layout update)
- 31.Page32 change R95.2 contact to R59.2(layout update)
- 32.Page35 del C415(BOM update)
- 33.Page35 U27 pin34 pull-high R965 0_0402 to VDDA for codec by pass mode(BOM&layout update)
- 34.Page37 del L39/L40/L54/L51 and add R971~R978 for external USB2.0 option(BOM&layout update)
- 35.Page36 add R968 for CY30/BY31 BOM option(BOM&layout update)
- 36.Page39 JP9 Footprint update for factory request(layout update)
- 37.Page40 U21 pin3,4 swap(layout update)
- 38.Page40 AD_BID0 for Board ID update(BOM update)
- 39.Page21 U29/U30 pin M4 add NMCSA1# and add R1006 0_0402 for external VGA 128M RAM option(BOM&layout update)

40.Page22 U34/U35 pin M4 add NMCSB1# and add R1007 0_0402 for external VGA 128M RAM option(BOM&layout update)

41.Page17/18 del R85, R81, R89, R97, R484, R483, R485, R486(BOM&layout update)

42.Page32 JP21 Footprint update for CIS(layout update)

43.Page25 remove R711 from page26 to page25

44.Page41 add RP113 100K 8P4R_0804 100K_0402(BOM&layout update)

45.Page44 all new add for external USB2.0(BOM&layout update)

46.Y3, Y4 footprint update(layout update)

47.D9 footprint update(layout update)

48.page32 R69.2 contact to V1.8_LAN for LAN vender updater(layout update)

49.page32 R94.1 contact to LANVDD(layout update)

50.page32 R60/R49/C55/C52 BOM option(BOM update)

2003/4/24

1.page5 Add R1008 for speedstep issue(BOM&layout update)

2.page25/40 Y3/Y4 pin define update(layout update)

2003/4/25

1.page31 add resume for carbus issue(layout update)

2.page26 del R215 for R216 only(BOM&layout update)

2003/4/30

1.page45 add R1009 for SUSP#(BOM&layout update)

2.page32 add R1010 for LAN transformer issue(BOM&layout update)

2003/5/02

1.page40 change HPS from U21 88pin to 36pin(layout update)

2.page43 change JP24 pin7/8/9/10 to MDI0-/MDI0+/MDI1-/MDI1+ (layout update)

3.page43 USB20P2+ and USB20P2- swap(layout update)

4.page38 del RP1/RP91(BOM&layout update)

5.page23 del R605(BOM&layout update)

6.page28 change R598 to @ and del @ for R597(BOM update)

7.page37 add R1011~R1018 for USB2.0 option(BOM&layout update)

2003/5/05

1.page11 del R74, C84(layout update)

2.page25/30/32/33/34/38/40/44 add AC termination

R305, C353, R61, C40, R520, C608, R519, C601, R576, C632, R270,

C315, R981, C784, R200, C228 for EMI request(BOM update)

3.page25 change damping resistor

R561, R563, R562, R560, R566, R549, R970, R559 to 33 ohm(BOM update)

4.page11/16 add AC termination R395, C464, R101, C127, R389, C451 for EMI request(BOM update)

5.page11/16 add AC termination R395, C464, R101, C127, R389, C451 for EMI request(BOM update)

6.page35 add AC termination C415 for EMI request(BOM update)

7.page7 add FAN Cap C641, C640, C633, C623 for EMI request(BOM update)

8.page24 new add Cap C806, C807 for EMI request(BOM&layout update)

9.page43 new add Cap C808 for SPR PS2 issue(BOM&layout update)

10.page27 change cap R634 footprint to 0_1206(BOM&layout update)

2003/5/14

1.R702 from 100K change to 10K (BOM update)

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Title			
SCHEMATIC, M/B LA-1861			
Size	Document Number	Rev	
	401257	OE	
Date:	星期三, 七月 30, 2003	Sheet	56 of 61

For B2 test

2003/5/22

1. Page13 R147.1 connect to R473.2, R489.1 connect to R502.2 (layout update)

2003/6/09

1. Page7 C623/C633 update footprint 0402 type (layout update)
2. Page45 R199, R567, R167 update value for power sequence delay (BOM update)
3. Page25 del R569 for PCI_CLKRUN# pull_high (Layout & BOM update)
4. Page25 Add R578 for PCI_CLKRUN# pull_high (Layout & BOM update)
5. Page30 Del R311 for PCI_CLKRUN# pull_high (BOM update)
6. Page40 Del R268 for EC591 not need (BOM update)
7. Page29 add D36 for SIDE_PWR leakage current (layout & BOM update)
8. Page10 Del R1005 it's not need (BOM update)
9. Page41 Add R1021 for EC_FLASH# pull_high (Layout & BOM update)
10. Page26 Add R1022 pull_high (Layout & BOM update)
11. Page26 R956 pin1 contact to GND (Layout update)
12. Page8 add R1023 (BOM update)
13. Page8 Del R173, R479, Q12 for change to @ (BOM update)

2003/6/11

1. Page5 R1008 change to 4.7K_0402 for follow HR60 (BOM update)
2. Page5 Q5, Q6 change to MMBT3904 for follow HR60 (BOM update)
3. Page5 del RP4 for ITP update (BOM update)
4. Page5 add R1024 47_0402, R1027 47_0402, R1025 150_0402, R1026 680_0402, R390 54.9_0603_1%, R404 54.9_0603_1% for ITP update (Layout & BOM update)
5. Page6 del C122, C46 for cost down (BOM update)
6. Page12 del C576, C588, C201, C198 for cost down (BOM update)
7. Page12 Change C150 to 47U_B (Layout & BOM update)
8. Page12 add C810, C811, C812 0.1U_0402 for +1.5VS (BOM update)
9. Page15 add C813, C814 22U_1206 for +1.25VS (Layout & BOM update)
10. Page15 del C280, C282 for cost down (BOM update)
11. Page16 add @ R1028 contact to PCI_RST# for RST# option (Layout update)
12. Page16 add R1029 0_0402 contact to NB_RST# for RST# option (Layout & BOM update)
13. Page16 add @ R1030 for M9+ SUS_STAT# option (Layout update)
14. Page16 add R1031 10K_0402 for M9+ SUS_STAT# pull-high +3VS (Layout & BOM update)
15. Page17, 18 del R405, R407, R420, R421, R466, R467, R465, R464 (BOM update)
16. Page19 Add C815, C816 for +VDDC15 (Layout & BOM update)
17. Page20 Del C497 for cost down (BOM update)
18. Page21 Del RP25, RP26, RP27, RP28, RP29, RP30, RP31, RP32, RP33, RP34, RP35 for cost down (Layout & BOM update)
19. Page21, 22 Del RP36, RP37, RP38, RP39, RP40 for cost down (Layout & BOM update)
20. Page21, 22 Del RP41, RP42, RP43, RP44, RP45, RP46, RP47, RP48, RP49, RP50 for cost down (Layout & BOM update)
21. Page22 Del RP52, RP53, RP54, RP55, RP56, RP57 for cost down (Layout & BOM update)
22. Page21 Del R384, R394, R418, R385, R383, R398, R410, R386 for cost down (Layout & BOM update)
23. Page21 Del R505, R453, R474, R509, R506, R455, R461, R508 for cost down (Layout & BOM update)
24. Page22 Del R516, R534, R497, R524, R518, R535, R496, R522 for cost down (Layout & BOM update)
25. Page22 Del R523, R498, R533, R515, R527, R499, R532, R517 for cost down (Layout & BOM update)
26. Page23 Change U40 pin10 contact to VTT_PWRGD (Layout update)
27. Page24 Add C817 10U_0805 for LCDVDD_C power (Layout & BOM update)
28. Page25 Add C818, C819 180P_0603 (Layout & BOM update)
29. Page25 Add C621, C622 180P_0603 (BOM update)
30. Page26 Add R1032, R1033 10K_0402 for PWRBTN_OUT pull-high and SB_EEDI pull-down (Layout & BOM update)

31. Page26 Del R208, R209 8.2K_0402 (Layout & BOM update)
32. Page26 Change R224, R219, R707, R708 to 8.2K_0402 (BOM update)
33. Page26 Del R1004 10K_0402 (Layout & BOM update)
34. Page44 Add R997 0_0402 (BOM update)
35. Page44 R997 pin1 contact to LPC_SMI# for DOS mode USB support (Layout update)
36. Page27 Add D37 RB751V, R1034 1K_0402 (Layout & BOM update)
37. Page27 Change C219, C223, C222, C699 to 22U_1206 (Layout & BOM update)
38. Page28 Add R685, R669, R697, R670, R677 10K_0402 (BOM update)
39. Page28 Del R698 10K_0402 (BOM update)
40. Page40 Add C820 for EC97591 option (Layout update)
41. Page42 Add R253 0_0402 (BOM update)
42. Page42 Del R229, R745, R746, Q67, C299, C281, Q20, Q24, (BOM update)
43. Page42 Change R252 to 330K_0402 (BOM update)
44. Page42 Change C307 to 0.1U_0402 (BOM update)
45. Page42 Add R1035 1K_0402, R1036 10K_0402, C821 0.1U_0603, Q68 2N7002 (Layout & BOM update)
46. Page43 Add R1037, R1038, R1039, R1040 0_0402 for SPR LAN option (Layout & BOM update)

2003/6/12

1. Page43 Change R979, R980 contact to JP24 pin21, 20 for USB trace option (Layout update)
2. Page43 Change R979, R980, L37, L38 to 0_0402 for SPR USB option (Layout & BOM update)
3. Page37 Change L32, L33, L34, L35, L53, L55, L50, L52 to 0_0402 for SPR USB option (Layout & BOM update)
4. Page26 Del R638, R647, R613, R640, R601, R611, R593, R603, R553, R551, R555, R550 for ATI DOC_PA_218IXP0T1 request (BOM update)
5. Page24 JP5, JP6 reverse for ME update (Layout update)

2003/6/12

1. Page32 Del U6 Pin114, 113 (schematic update)
2. Page32 Q44, Q46 from 2SB1197 change to 2SB1188 (Layout & BOM update)
3. Page32 U28 from 24ST0023P change to H5007 (H1285)
4. Page32 C10 1000P_0402_50V7K change to 1000P_1206_2KV7K (Layout & BOM update)

2003/6/16

1. page11 Add L59, L60, L61, L62, L63 0805 type NB power bed (Layout & BOM update)
2. page11 Change R399, R70 type to 0805 for NB power bed (Layout & BOM update)
3. page11 Del Q47 for change to @ (BOM update)

2003/6/17

1. Page24 JP5, JP6 reverse again for ME update (Layout update)
2. page40 Change C820 to 0603 type (Layout update)

For B2 test

2003/6/18

1. Page8 Add C822 D2 type for CPVDD power(Layout update)
2. Page16 Add R1041 8.2K_0402 AGP_FRAME# pull-high to +3VS(Layout & BOM update)
3. Page45 Add R1042, Q69 / R1043, Q70 / R1044, Q7 , for +3V, +1.5VS, +VGA_CORE discharge circuit(Layout & BOM update)
4. Page8 add C823 0.1u_0402 for ATI recommand
5. Page19 add C824, C825, C826 0.1U for 1.5VS
C828, C827 0.1U for +VDDC15

2003/6/19

1. Page32 U28 +-pair reverse(Layout update)
2. Page14 add RP114, RP115, RP116, RP117, RP118, RP119, RP120, R1045, R1046, R1047, R1048, R1049, R1050, R1051, R1052, R1053 for ATI DDR
recommand(Layout & BOM update)
3. Page23 R688 pin1 contact to U40 pinD5(Layout update)
4. Page42 C821 change to 0402 type(Layout & BOM update)
5. Page8 Update C822(Layout update)
6. Page43 Update L34, L38 to JP24 NET name.

2003/6/20

1. Page34 add C663 for audio noise(BOM update)

2003/6/22

1. Page25 R187 change to 4.7K for 4/22 ATI review update(BOM update)
2. Page25 GPI00, OVCUR#4 pull-down for 4/22 ATI review update(Layout update)
3. Page26 del R1033 for 4/22 ATI review update(BOM update)
4. Page26 R706 pull-high to +3V for 4/22 ATI review update(BOM update)
5. Page28 R579 pull-high to +3VS for 4/22 ATI review update(Layout update)
6. Page28 del R597(CPU_STP# strap not need) for 4/22 ATI review update(BOM update)
7. Page29 Change R732, R734, R747, R165, R159, R164 to 33_0402 for 4/22 ATI review update(BOM update)
8. Page29 SD_D7 Add R1054 10k_0402 Pull-down for 6/22 ATI review update(Layout & BOM update)

2003/6/24

1. Page38 Del RP65 for cost down(Layout & BOM update)
2. Page38 Add RP0121, RP122 for cost down(Layout & BOM update)
3. Page40 Add RP0123, RP124 for cost down(Layout & BOM update)
4. Page40 Del RP19 for cost down(Layout & BOM update)

2003/6/25

1. Page43 change SPR USB power source(Layout update)

2003/6/26

1. Page43 add U50, C829 for SPR USB power switch(Layout & BOM update)
2. Page26 add R659, C659 for EMI request(BOM update)

2003/7/01

1. Page16 add R1030 0_0402 for S3 SUS_STAT# issue(BOM update)
2. Page16 del R1031 for S3 SUS_STAT# issue(BOM update)

For C test

2003/7/07

1. Page36 C364 from 1U_0402 change to 1U_0603 (Layout & BOM update)
2. Page31 C366, C352 from 4.7U_1206 change to 4.7U_0805 (Layout & BOM update)
3. Page29 C507 from TAN4.7U_0805 change to 4.7U_0805 (Layout & BOM update)
4. C170, C184, C189, C217, C224, C229, C277, C615, C620, C677, C718, C723, C728 from 10U_1206 change to 10U_0805 (Layout & BOM update)
5. C68, C92, C168, C406, C416, C420, C468, C565, C606, C730, C780, C637, C642 from 10U_1206 change to 10U_0805 (Layout & BOM update)

2003/7/10

1. Page5 change R194 from 62_0402 to 200_0402 for ATI recommend(BOM update)
2. Page8 change R80 from 412_0402 to 330_0805_1% for ATI recommend(BOM update)
3. Page11 del M9@ C75/X2/R73 ATI recommend(BOM update)
4. Page11 add R1055 4.7K_0402 for ATI recommend(Layout & BOM update)
5. Page16 add Q72 for SUSSTAT# level shift and ATI recommend(Layout & BOM update)
6. Page16 add R1031 10K_0402 for SUSSTAT# level shift and ATI recommend(BOM update)
7. Page16 change R1030 to 470_0402 for SUSSTAT# level shift and ATI recommend(BOM update)
8. Page24 add R1056 2.7K_0402 for ENAVDD pull-down and ATI recommend(Layout & BOM update)
9. Page25 change D13 to RB751V for ATI recommend(Layout & BOM update)
10. Page40 change +RTCVCC to BATT1.1 for ATI recommend(Layout update)
11. Page8 del C97 for CEL CPU can't BOOT issue(BOM update)
12. Page40 del R270/C315 for can't BOOT issue(BOM update)
13. Page32 update Q44/46 footprint(Layout update)
14. Page14 add C830/C831 for ATI recommend(Layout & BOM update)

Compal Electronics, Inc.			
Title		SCHEMATIC, M/B LA-1861	
Size	Document Number	Rev	
Custom	401257	0E	
Date	星期二, 七月 30, 2003	Sheet	58 of 61

For C test

2003/7/11

- 1. Page29 add R1057 0_0402 for cost down(Layout & BOM update)
- 2. Page29 del Q64/R702/Q61 for cost down(BOM update)
- 3. Page29 del D36 for cost down(BOM update)
- 4. Page29 add R1058 for cost down(BOM update)
- 5. Page35 del R295/Q34 for cost down(BOM update)

2003/7/15

- 1. Page35 add C832_1U_0603 for MIC noise issue(Layout & BOM update)
- 2. Page35 Change C379 form 0805 to 0603(Layout & BOM update)
- 3. Page35 add C410 form audio noise(BOM update)
- 4. Page29 add C609/C174 form audio noise(BOM update)
- 5. Page36 add R1059 form audio AMP(Layout & BOM update)
- 6. Page36 del R339/R334/R335/R333/Q30/Q31/Q32/Q33 form audio AMP(BOM update)
- 7. Page36 R338 change to 1K_0402(BOM update)

2003/7/18

- 1. Page39 add C833/C836/C837/C838/C839 for EMI request(Layout & BOM update)
- 2. Page10 DEL R118/R112/U9/L16/R117/C148/R111/R108/R116/C137/C133 for EMI request(BOM update)
- 3. Page35 add R1061 2.2K_0402(Layout & BOM update)
- 4. Page35 change JP9 pin34/35 to (Layout update)
- 5. Page26 RP12 from 10k change to 2.2K (BOM update)

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Title			
SCHEMATIC, M/B LA-1861			
Size	Document Number		Rev
Custom	401257		0E
Date	星期三, 七月 30, 2003		Sheet 59 of 61

Version change list (P.I.R. List)

Page 1 of 1

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B Ver.
1		modify for RTC battery	46	Del PD6(RLZ3.6B) and add PR177(100_0805_5%) Add PR178(200_0603_5%)	EVT
2		For ME change battery connector	47	change P/N: from DC040012310 to DC040012330	EVT
3		Modify +1.5VSP ripple and OCP +2.5ALWP output voltage	50	change PL8 from 5U_SPC-06704-5R0_2.9A to 2U_SPC-SPC-07040-2R0_6A change PC73 from 150U/4V(ESR=45) to 150U/6.3V(ESR=18) change PR93 from 102K_0402_1% to 16.2K_0402_1% add PR179(5.1K_0402_1%) add PR181(10K_0402_1%) add PR180(15K_0402_1%) add PR182(9.53K_0402_1%)	EVT
4		add power sequence circuit for HW requirement	52 50	add PU19 LM393M_S08 add PC147 0.1U_0603_50V add PC148 0.1U_0603_50V add PC149 0.1U_0603_50V add PR187 10K_0603_5% add PR185 10K_0603_5% add PR186 10K_0603_5% add PR183 0_0402_5% add PR184 0_0402_5% add PR188 10K_0603_5% add PR189 10K_0603_5% add PR190 10K_0603_5% add PQ47 2N7002_S0T23 add PQ48 2N7002_S0T23	EVT
5		add VGA_CORE power select for HW requirement	52	add PQ23 2N7002_S0T23(for DBY31)	EVT
6		change CPU_CORE boost resister value for EMI requirement	54 55	change PR152 , PR159 , PR165 , PR171 from 0_0603_5% to 2.2_0603_5%	EVT
7		Add by pass cap. for EMI requirement	54	Add PC150 0.1U_0603_50V Add PC151 1000P_0603_50V	EVT
8		For BOM error	51	Change PR98 vaule from 4.87K_0603_1% to 11.5K_0603_1%	EVT
9		Change Battery side OTP point to 79C for thermal requirement	47	Change PR39 from 16.9K_0603_1% to 14.7K_0603_1% Change PR41 from 3.32K_0603_1% to 3.48K_0603_1%	DVT
10		Delete CPU_CORE IC's OTP function	53	Delete PR132,PC111	DVT
11		Add snubber for EMI requirement	54,55	Add 68_0805_5% at PR156,PR162,PR168,PR174 Add 220P_0603_50V at PC124,PC130,PC138,PC145	DVT
12		Change Material	49,50	Change PC53,PC58,PC73 from SGA19151330(H2.8) to SGA20151320(H1.9)	DVT

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Title	SCHEMATIC, M/B LA-1861		
Size	Document Number	Rev	
Custom	401257	0E	
Date	星期三, 七月 30, 2003	Sheet	60 of 61

10

9

8

7

6

5

4

3

2

1

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B Ver.
14		To prevent surge current at CPU_CORE	54,55	Add 499K_0603_5% at PR155,PR161,PR167,PR173	PVT

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Title		
SCHEMATIC, M/B LA-1861		
Size	Document Number	
Custom	401257	
Date:	星期三, 七月 30, 2003	Rev OE
Sheet		61 of 61

10

9

8

7

6

5

4

3

2

1