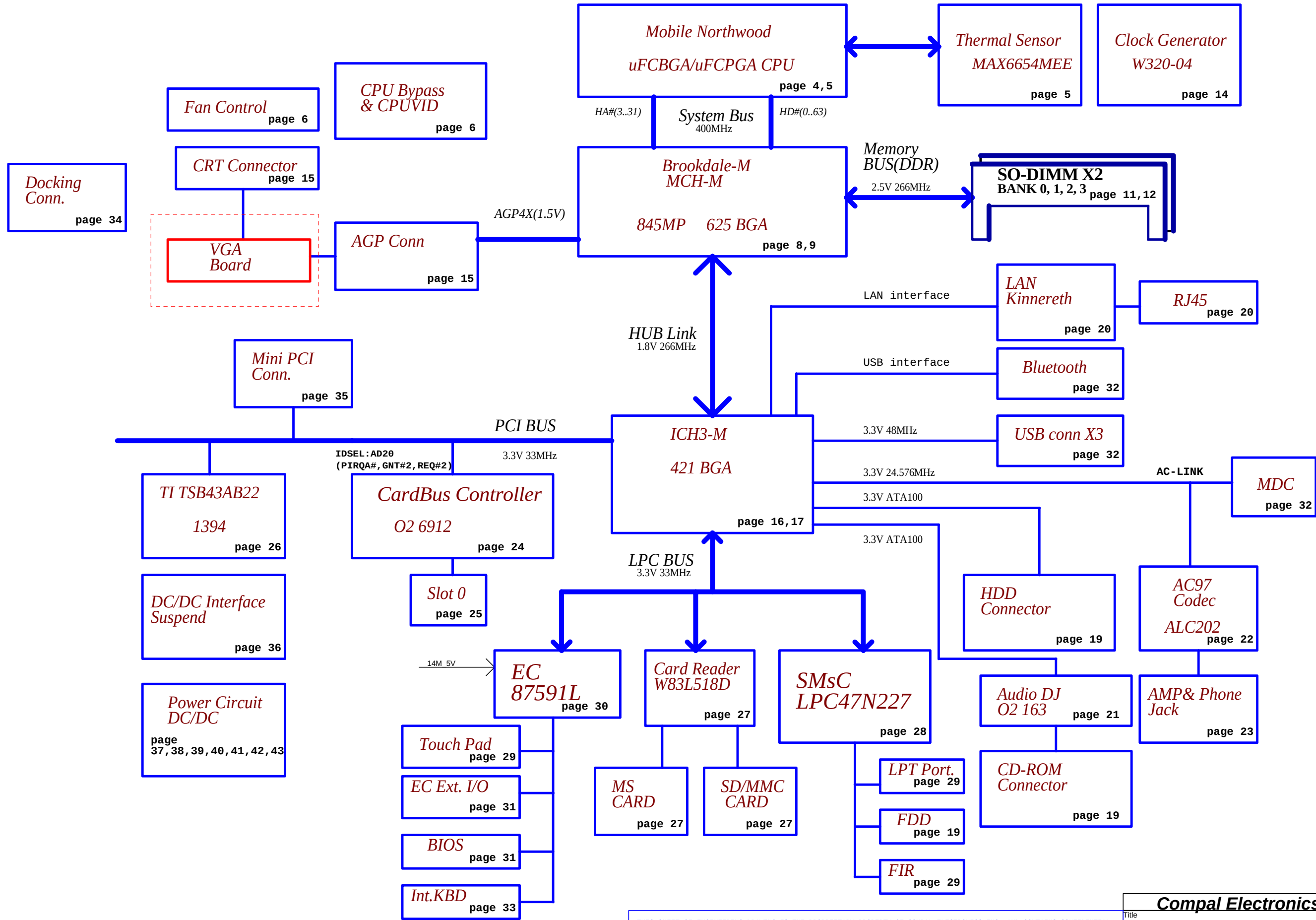


LA-1511 REV1.0 Schematics Document

uFCBGA/uFCPGA Northwood with Brookdale chipset(845MP+ICH3-M)

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Title	SCHEMATIC, M/B LA-1511	
Size	Document Number	Rev
Custom	401224	0B
Date:	星期三, 八月 21, 2002	Sheet 1 of 43



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Title	SCHEMATIC, M/B LA-1511	
Size	Document Number	Rev
401224		0B
Custom		
Date:	星期三, 八月 21, 2002	Sheet 2 of 43

Power Managment table

Signal State	+3VALW +5VALW +1.8VALW +12VALW	+3V +5V +2.5V	+12VS +5VS +3VS +2.5VS +1.8VS +1.5VS +1.2VP +CPU_CORE +1.25VS +1.25VS_VGA
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

	NB Chip Rev	SB Chip Rev

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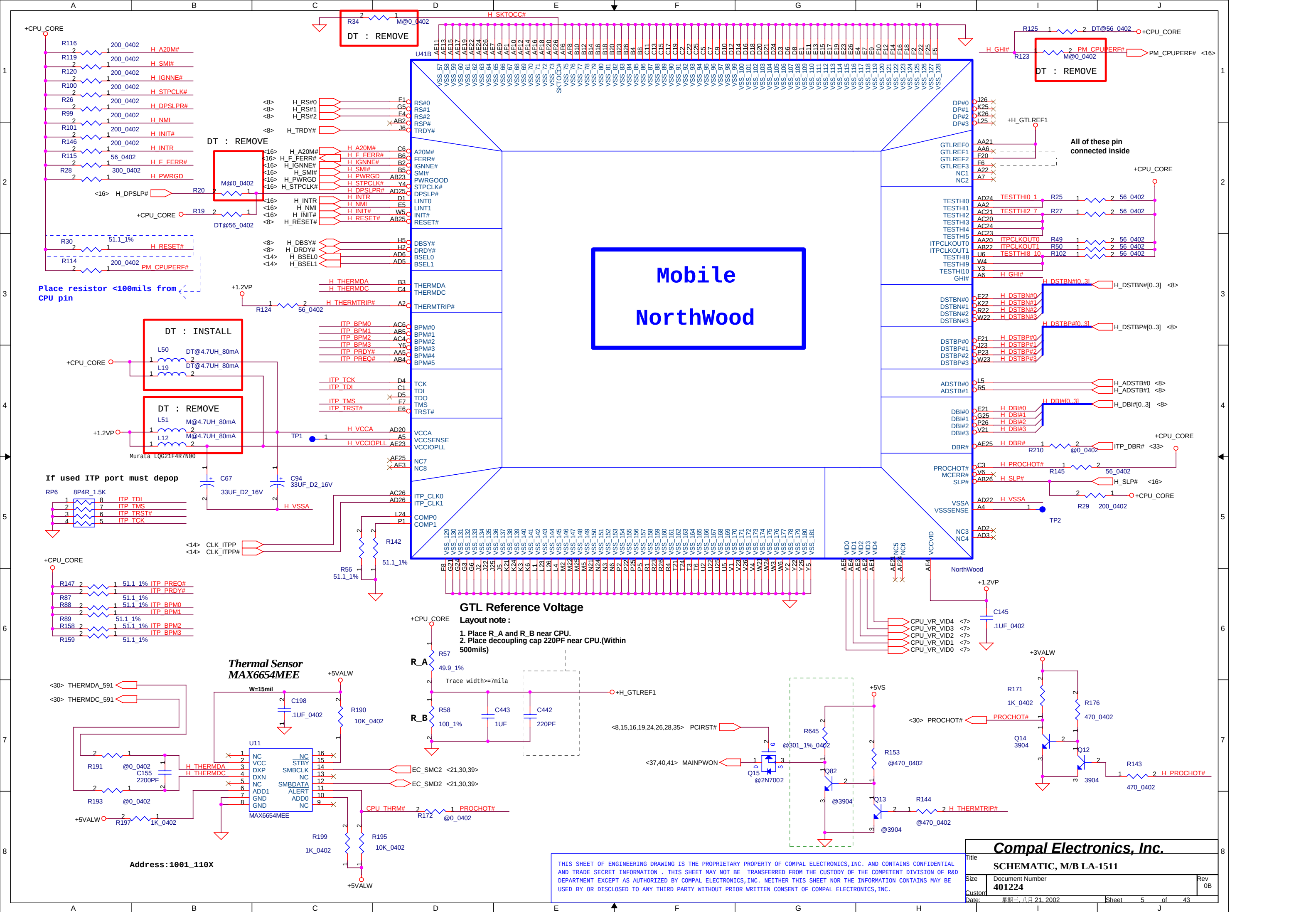
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Custom

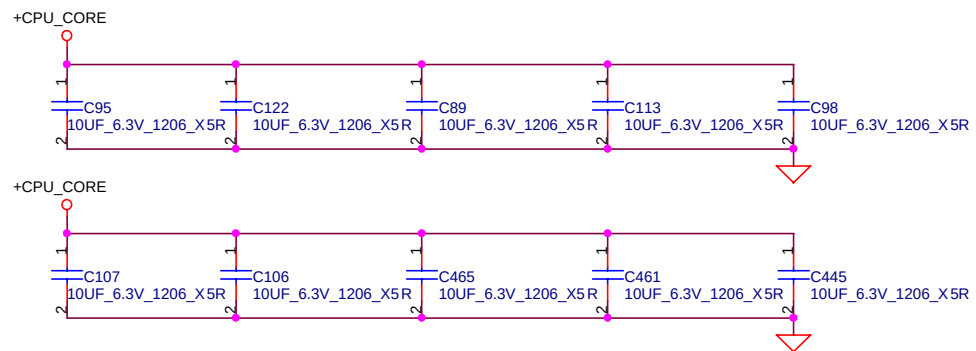
Date: 星期三, 八月 21, 2002

Sheet 3 of 43

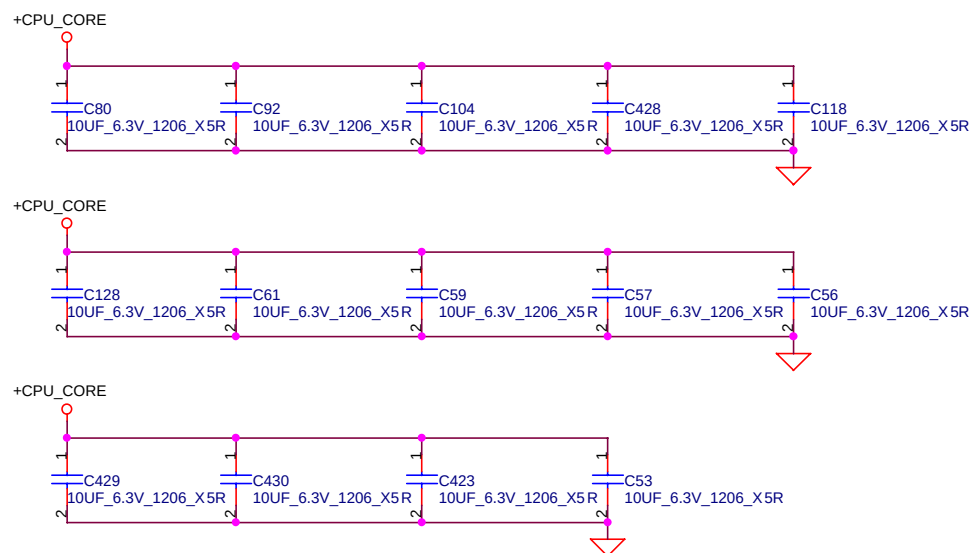


Layout note :
Place close to CPU, Use 2~3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

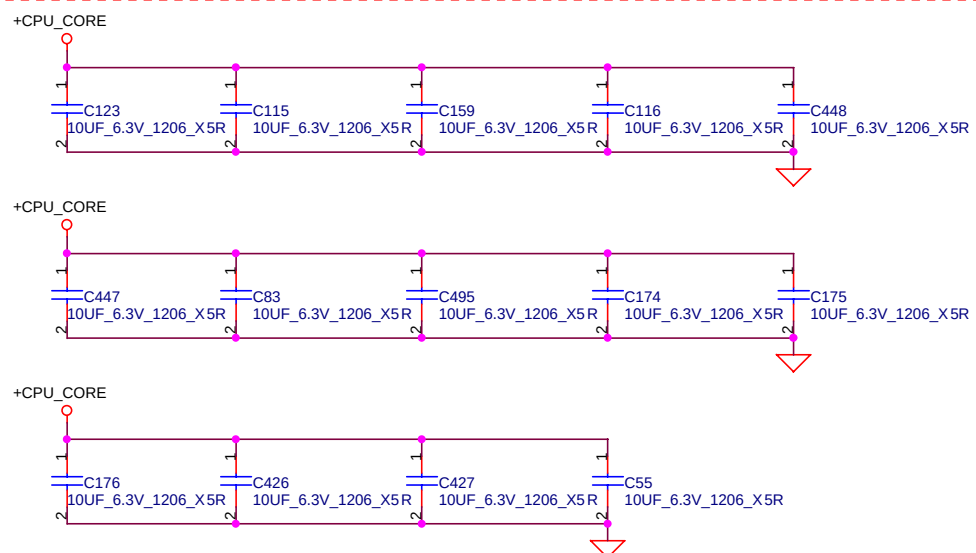
Please place these cap in the socket cavity area



Please place these cap on the socket north side



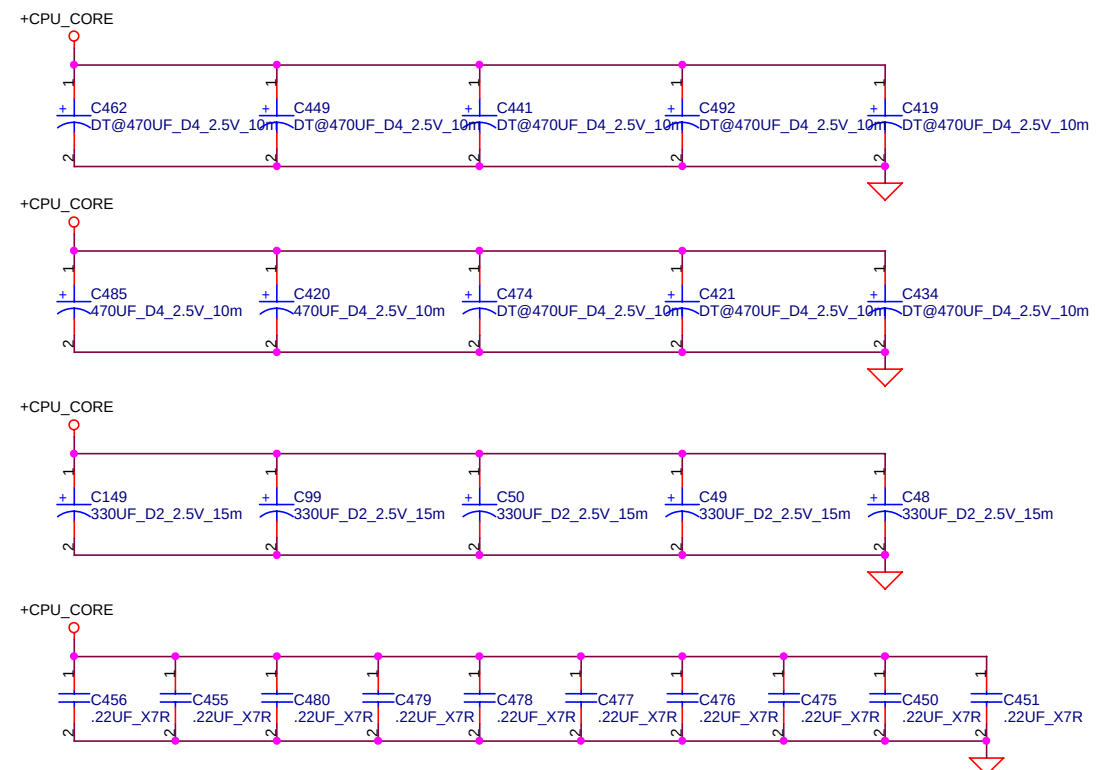
Please place these cap on the socket south side



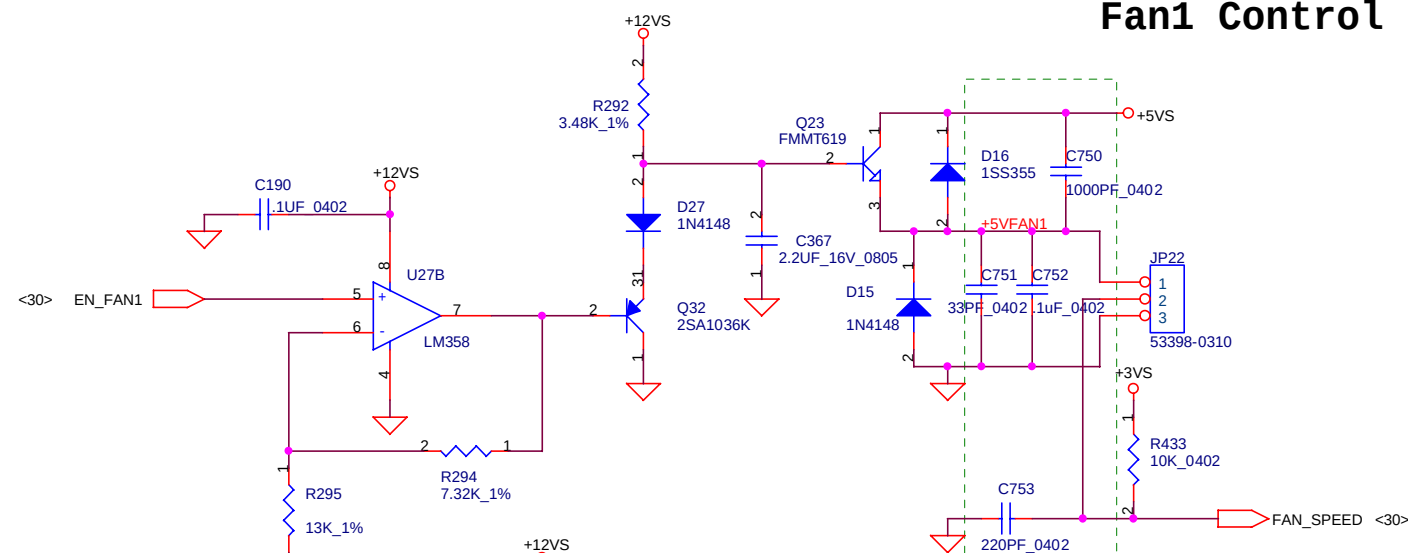
Layout note :
Place close to CPU power and ground pin as possible (<1inch)

For Desktop's CPU:
ESR total=0.75m ohm
C total=6350uF

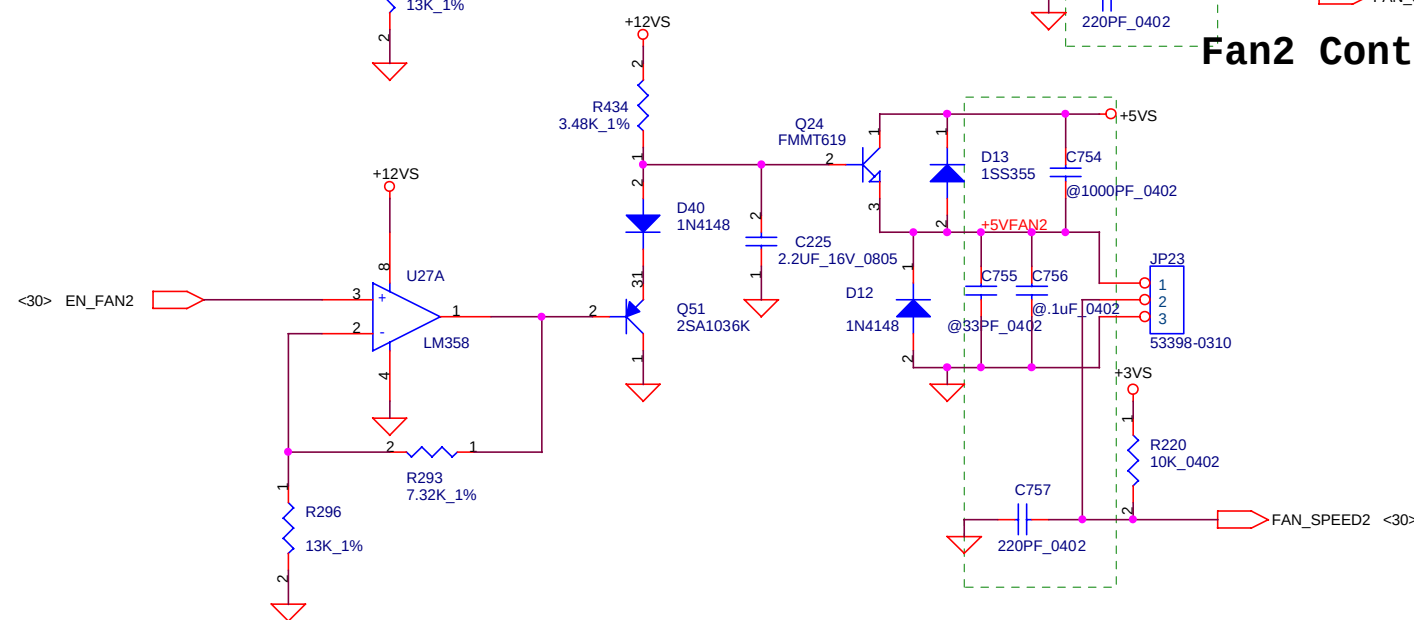
For Mobile's CPU:
ESR total=1.875m ohm
C total=2590uF



Fan1 Control circuit



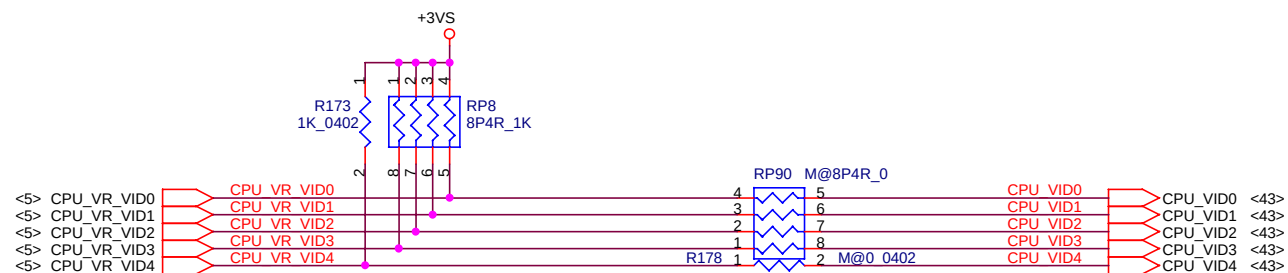
Fan2 Control circuit



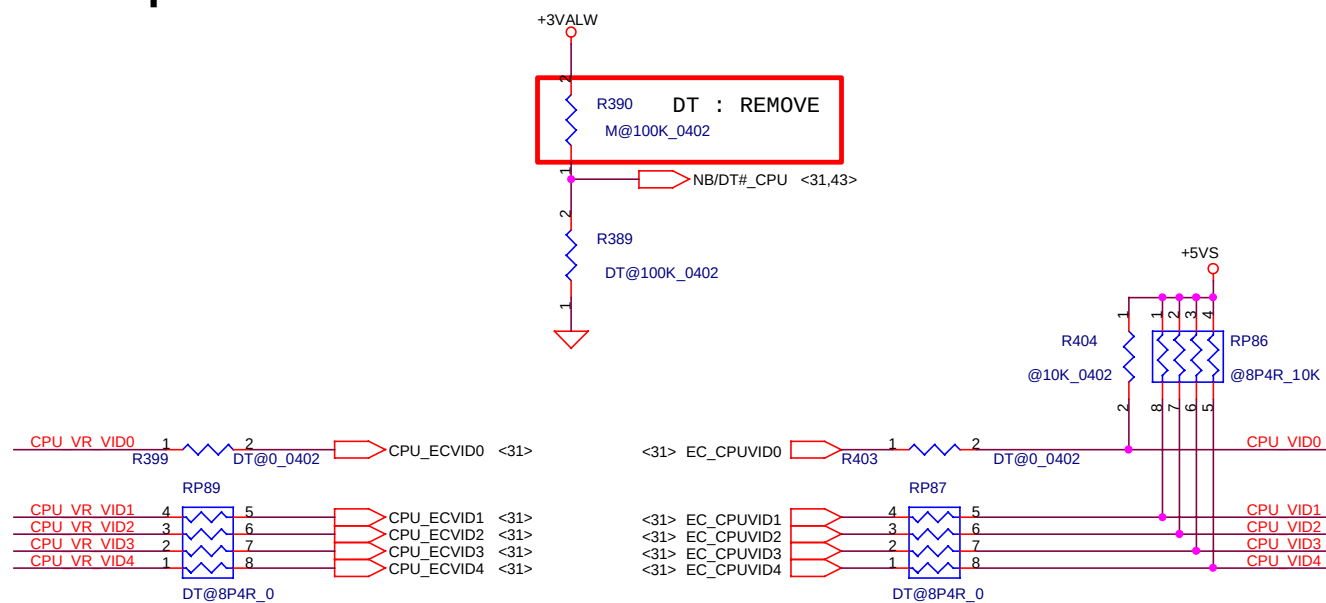
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Title	SCHEMATIC, M/B LA-1511	
Size	Document Number	Rev
Date:	401224	0B
星期三, 八月 21, 2002	Sheet	6 of 43

For Mobile CPU



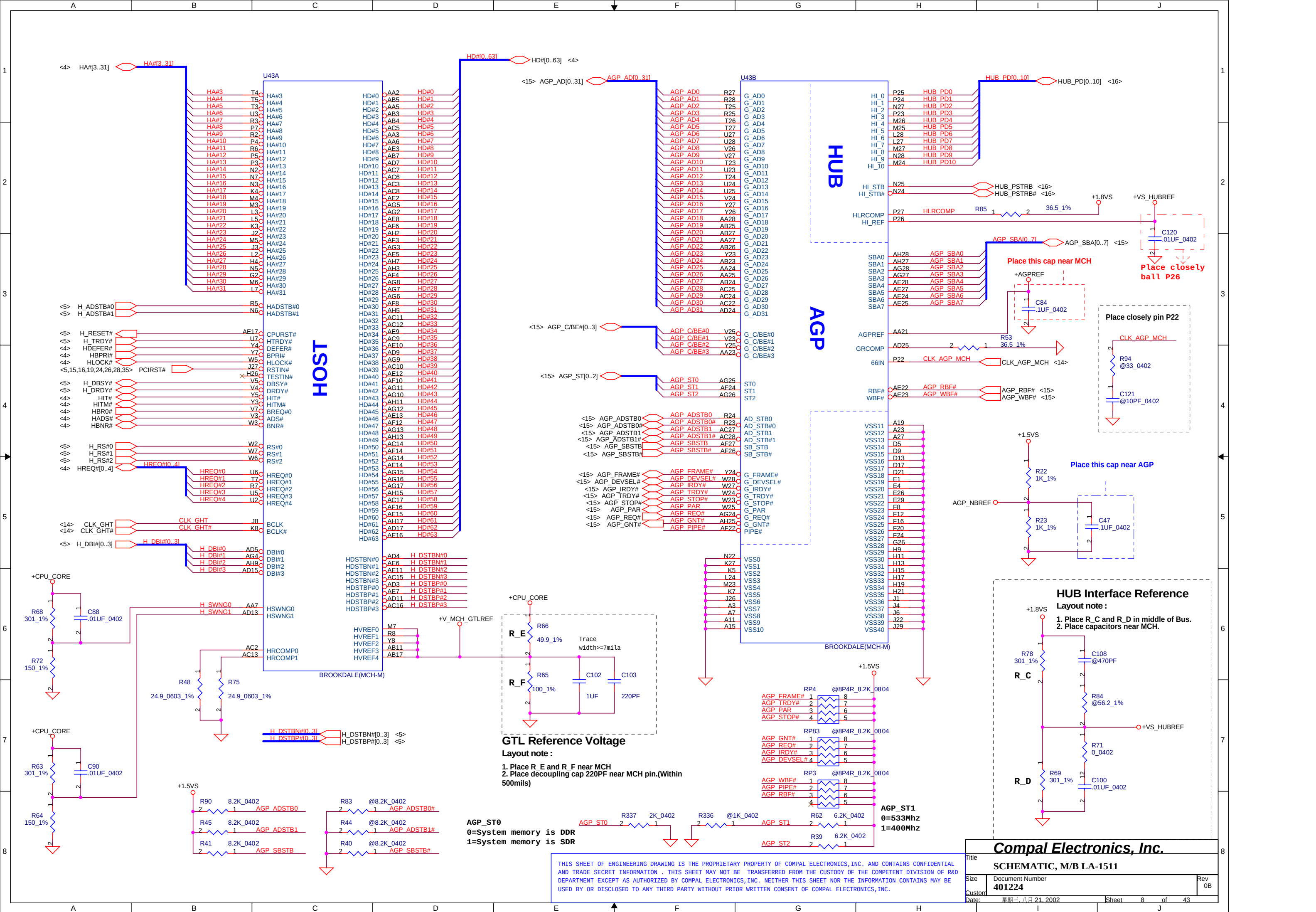
For Desktop CPU

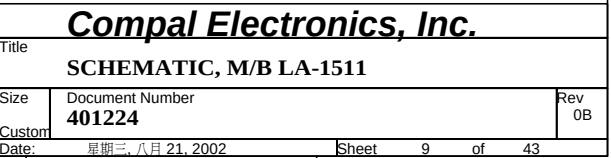


	Mobil CPU					Destop CPU				
NB/DT_CPU	1					0				
VID	4	3	2	1	0	4	3	2	1	0
VCC										
1.750V	0	0	0	0	0	0	0	1	0	0
1.700V	0	0	0	0	1	0	0	1	1	0
1.650V	0	0	0	1	0	0	1	0	0	0
1.600V	0	0	0	1	1	0	1	0	1	0
1.550V	0	0	1	0	0	0	1	1	0	0
1.500V	0	0	1	0	1	0	1	1	1	0
1.450V	0	0	1	1	0	1	0	0	0	0
1.400V	0	0	1	1	1	1	0	0	1	0
1.350V	0	1	0	0	0	1	0	1	0	0
1.300V	0	1	0	0	1	1	0	1	1	0
1.250V	0	1	0	1	0	1	1	0	0	0
1.200V	0	1	0	1	1	1	1	0	1	0
1.150V	0	1	1	0	0	1	1	1	0	0
1.100V	0	1	1	0	1	1	1	1	1	0
1.050V	0	1	1	1	0	X	X	X	X	X
1.000V	0	1	1	1	1	X	X	X	X	X
0.975V	1	0	0	0	0	X	X	X	X	X
0.950V	1	0	0	0	1	X	X	X	X	X
0.925V	1	0	0	1	0	X	X	X	X	X
0.900V	1	0	0	1	1	X	X	X	X	X
0.875V	1	0	1	0	0	X	X	X	X	X
0.850V	1	0	1	0	1	X	X	X	X	X
0.825V	1	0	1	1	0	X	X	X	X	X
0.800V	1	0	1	0	1	X	X	X	X	X
0.775V	1	1	0	1	0	X	X	X	X	X
0.750V	1	1	0	0	1	X	X	X	X	X
0.725V	1	1	0	1	0	X	X	X	X	X
0.700V	1	1	0	1	1	X	X	X	X	X
0.675V	1	1	1	0	0	X	X	X	X	X
0.650V	1	1	1	0	1	X	X	X	X	X
0.625V	1	1	1	1	0	X	X	X	X	X
0.600V	1	1	1	1	1	X	X	X	X	X
VRM output off						1	1	1	1	1

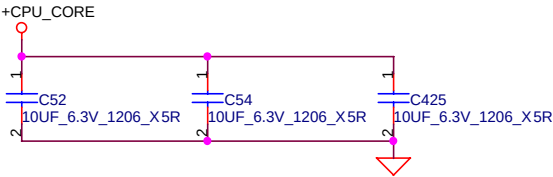
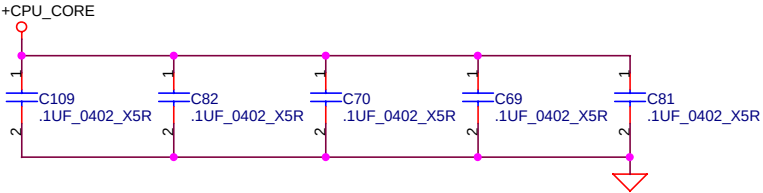
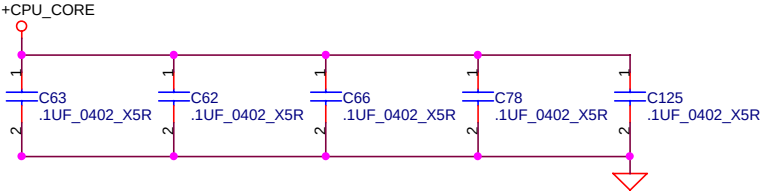
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Title	SCHEMATIC, M/B LA-1511	
Size	Document Number	Rev
401224		0B
Date:	星期三, 八月 21, 2002	Sheet 7 of 43

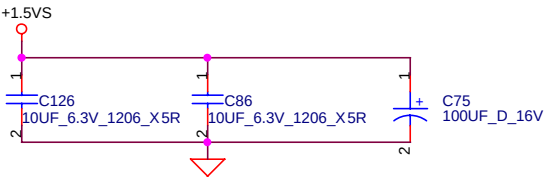
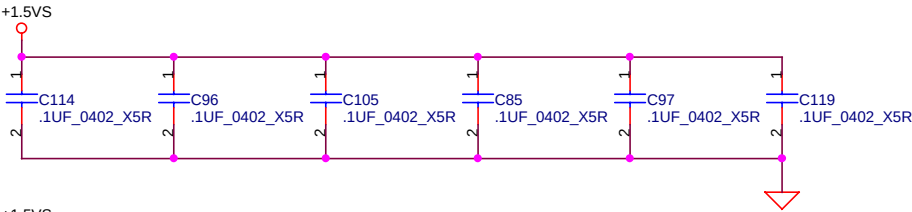




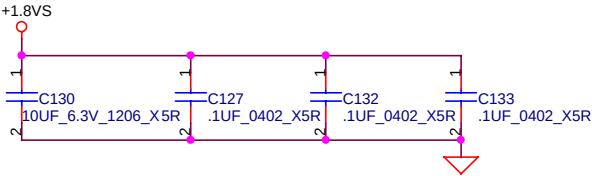
Layout note : Processor system bus
Distribute as close as possible
to MCH Processor Quadrant.(between VTTFSB and VSS pin)



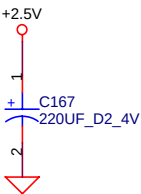
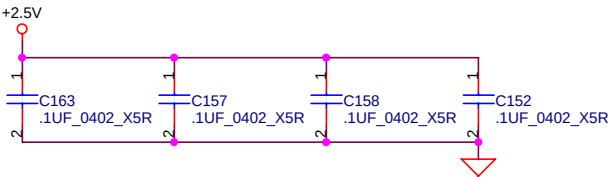
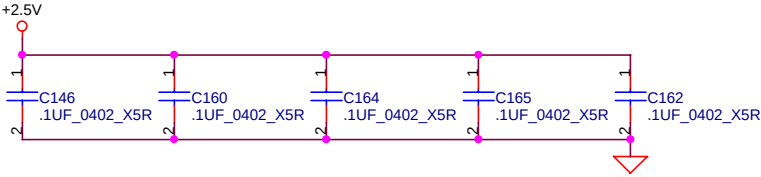
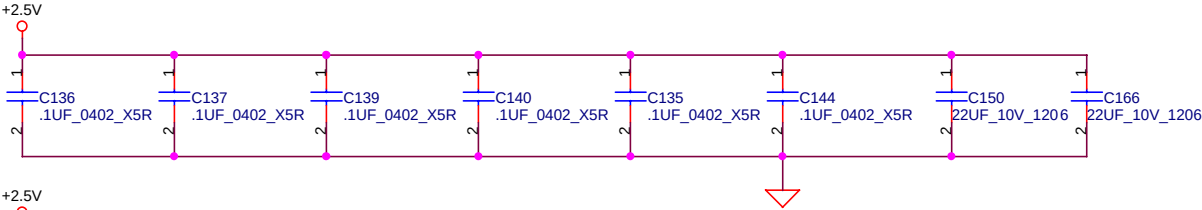
Layout note : AGP/CORE
Distribute as close as possible
to MCH Processor Quadrant.(between VCCAGP/VCCCORE
and VSS pin)



Layout note : Hub-Link
Distribute as close as possible
to MCH Processor Quadrant.(between VCCHL and VSS pin)



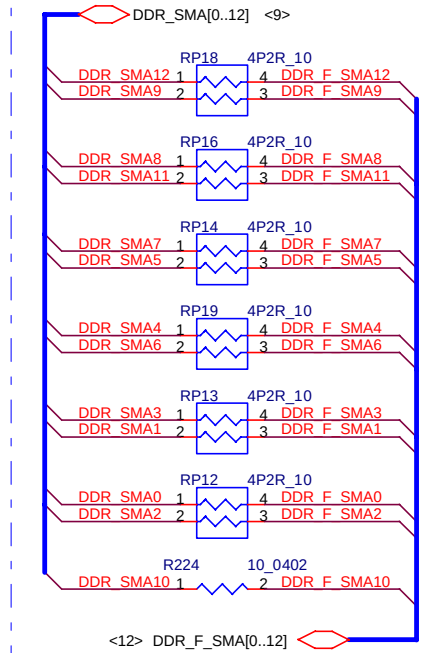
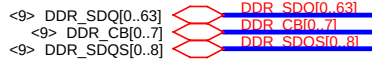
Layout note : DDR Memory interface
Distribute as close as possible
to MCH Processor Quadrant.(between VCCSM and VSS pin)



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Compal Electronics, Inc.		
Title	SCHEMATIC, M/B LA-1511	
Size	Document Number	Rev
	401224	0B
Custom Date:	星期三, 八月 21, 2002	Sheet 10 of 43

Place these resistor
closely DIMM0,
all trace length<750mil

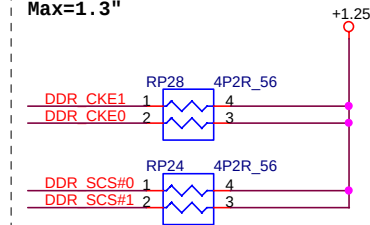


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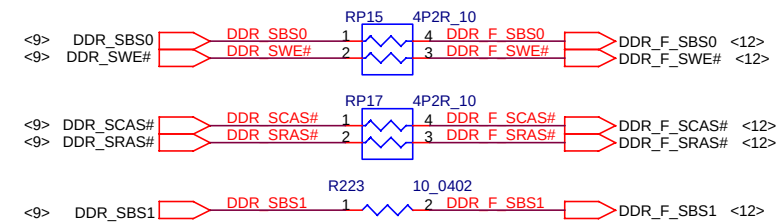
|         Layout note
|         Place these resistor
|         closely DIMM0,
|         all trace length<=750mil

```

Layout note
Place these resistor
closely DIMM0,
all trace length
Max=1.3" +1.25VS

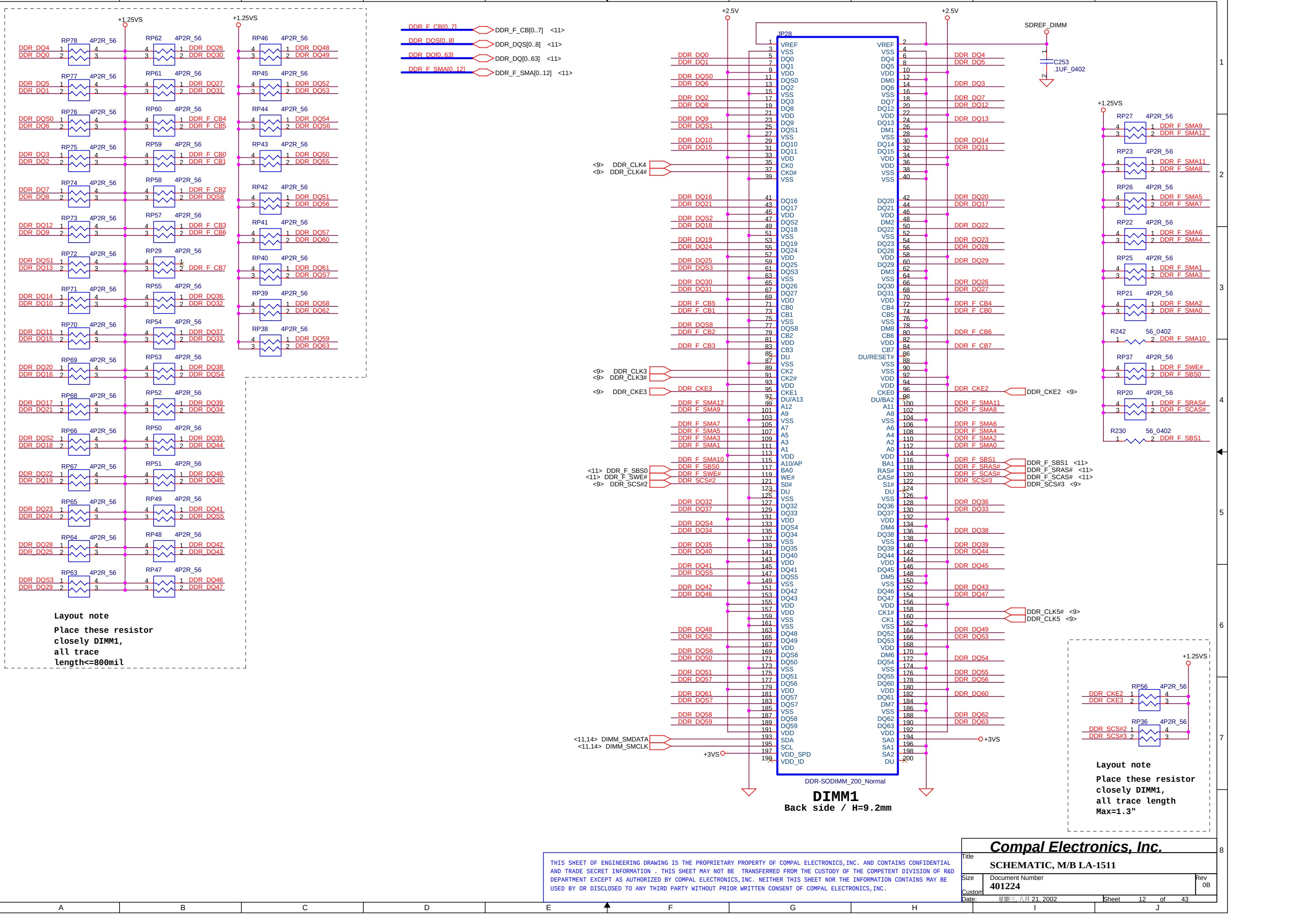


Layout note
Place these resistor
closely DIMM0,
all trace
length<=750mil



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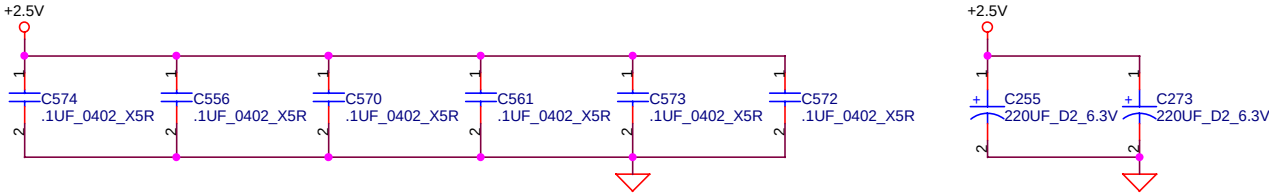
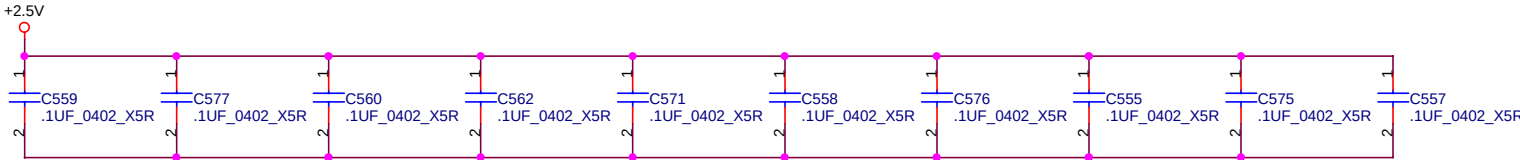
Compal Electronics, Inc.			
Title			
SCHEMATIC, M/B LA-1511			
Size	Document Number		
Custom	401224		
Date:	星期三, 八月 21, 2002	Sheet	11 of 43
			Rev 0B



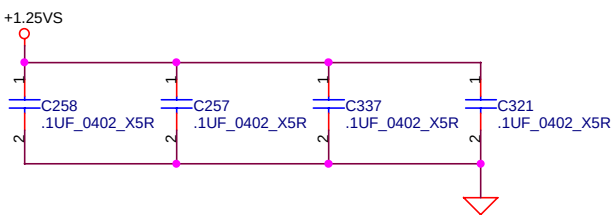
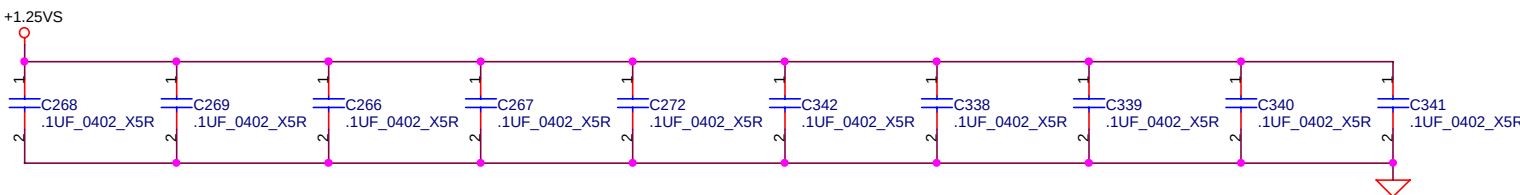
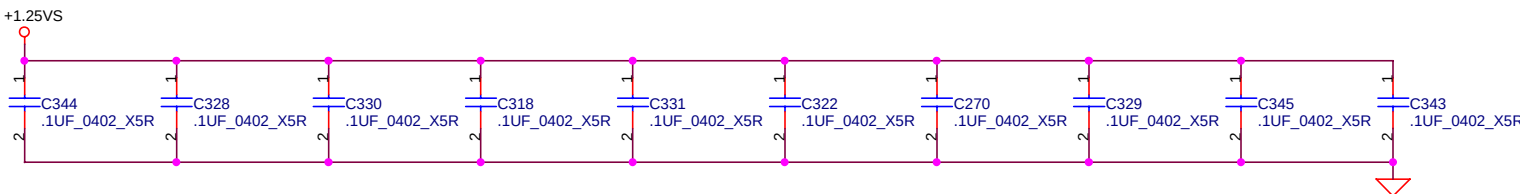
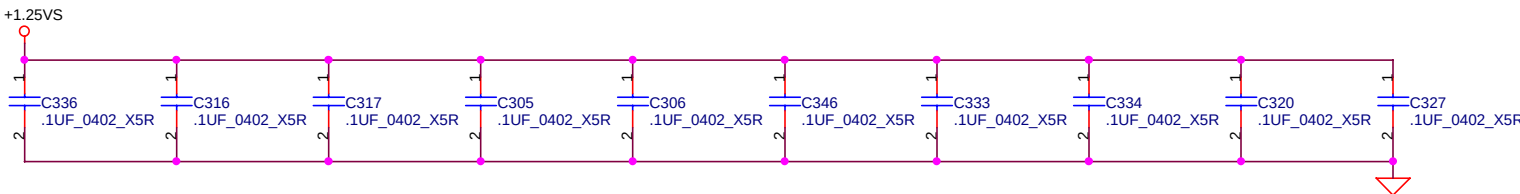
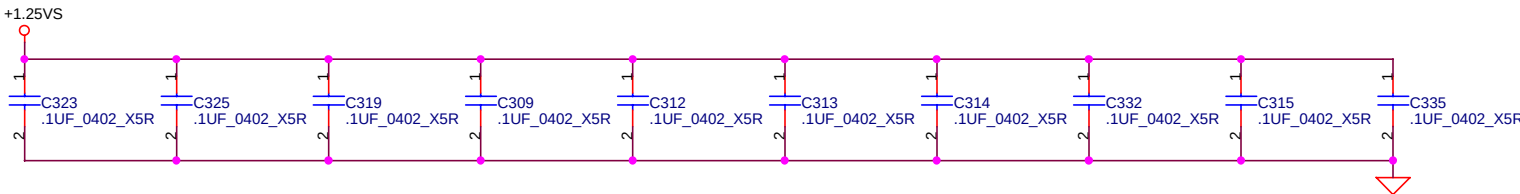
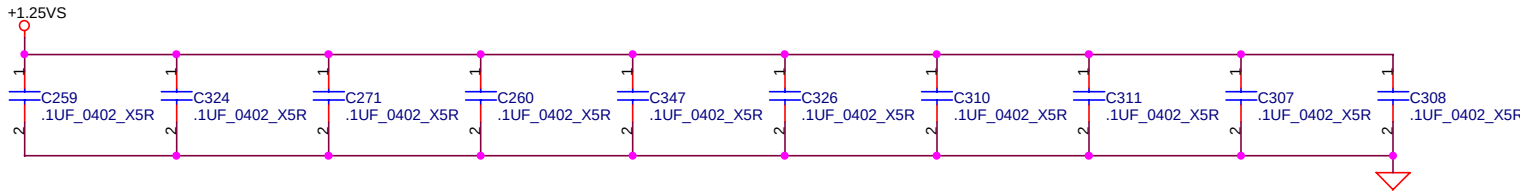
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Title SCHEMATIC, M/B LA-1511			
Size	Document Number 401224		Rev 0B
Custom			
Date:	星期三, 八月 21, 2002	Sheet	12 of 43

Layout note :
Distribute as close as possible
to DDR-SODIMM.



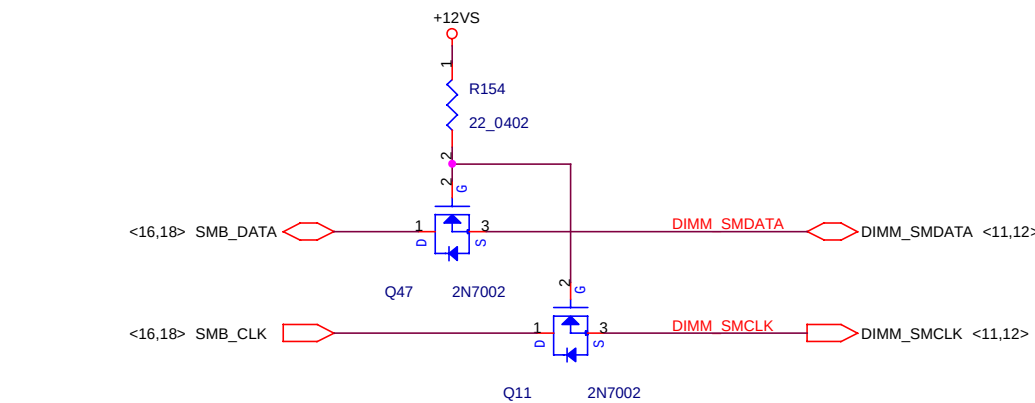
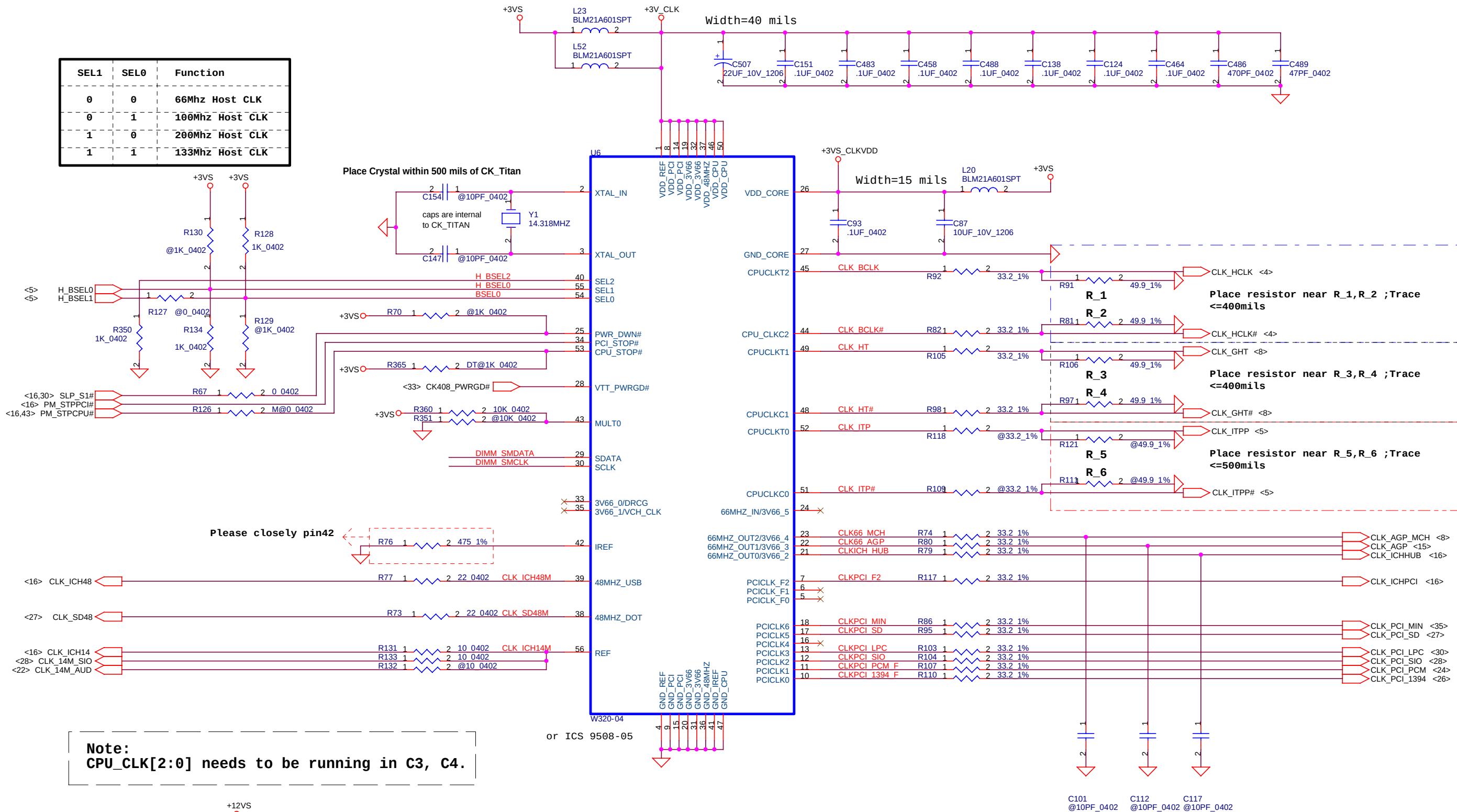
Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25V



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Title			SCHEMATIC, M/B LA-1511		
Size	Document Number				Rev
	401224				0B
Custom	Date: 星期三, 八月 21, 2002				Sheet
	13				of
	43				

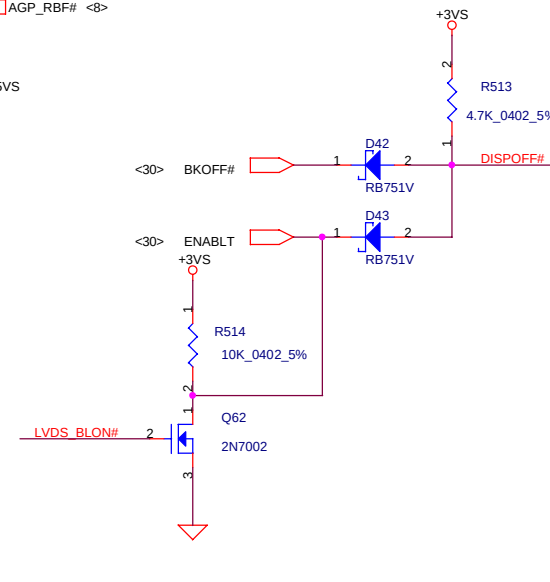
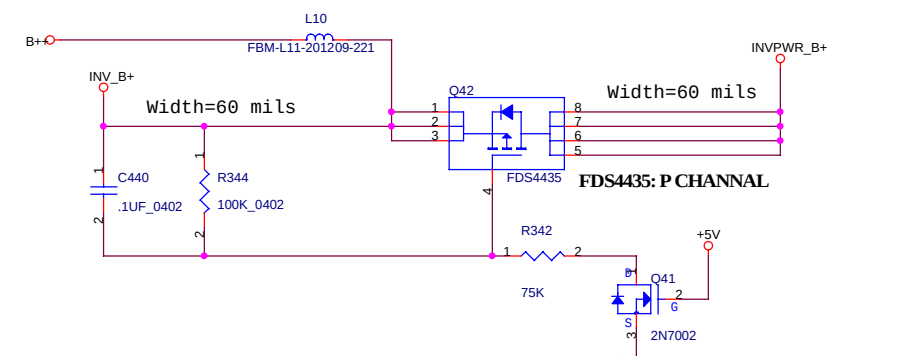
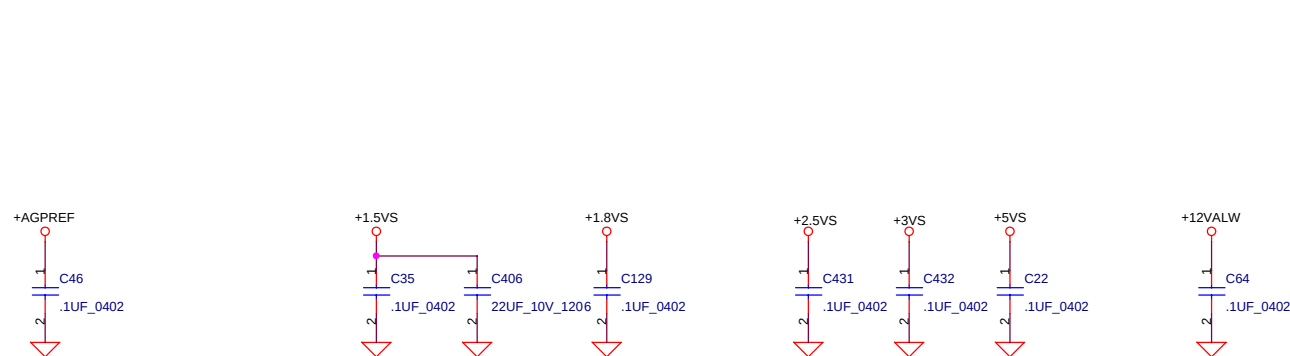
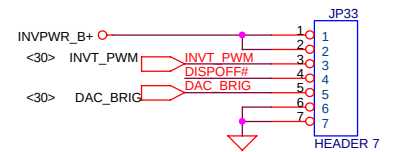
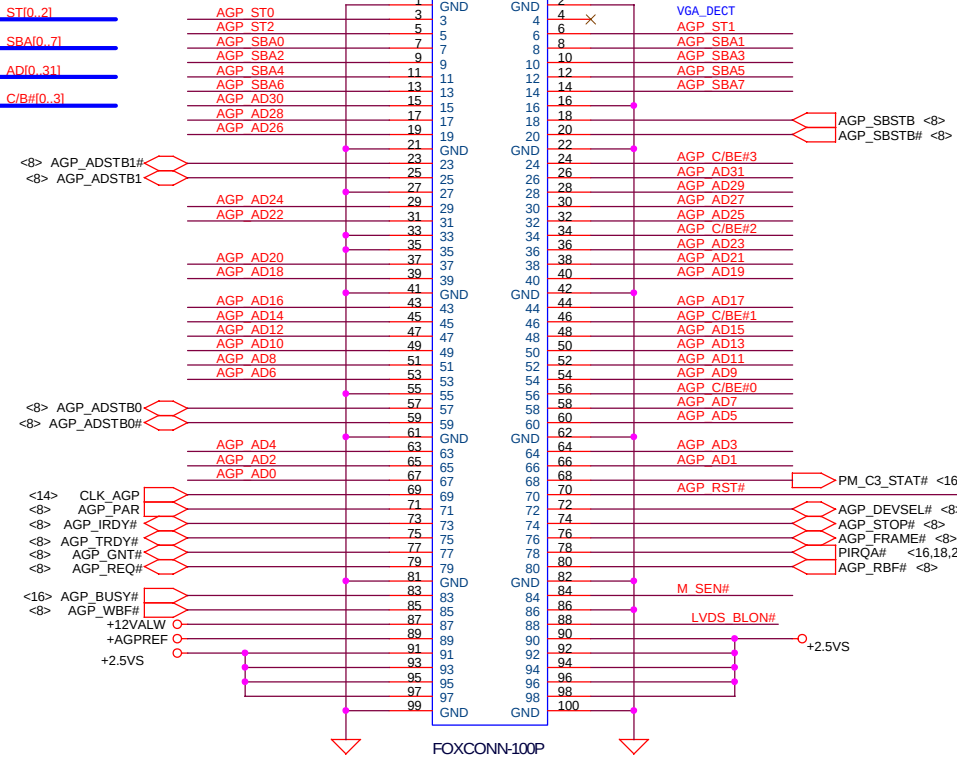
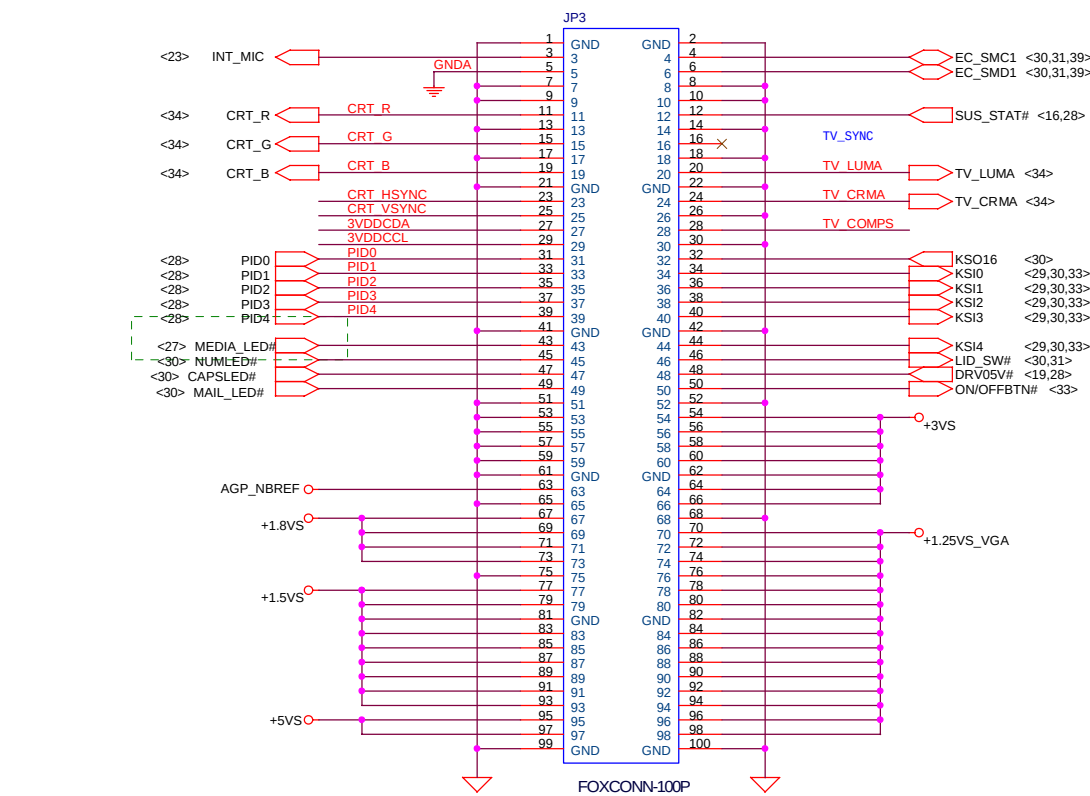
SEL1	SEL0	Function
0	0	66Mhz Host CLK
0	1	100Mhz Host CLK
1	0	200Mhz Host CLK
1	1	133Mhz Host CLK



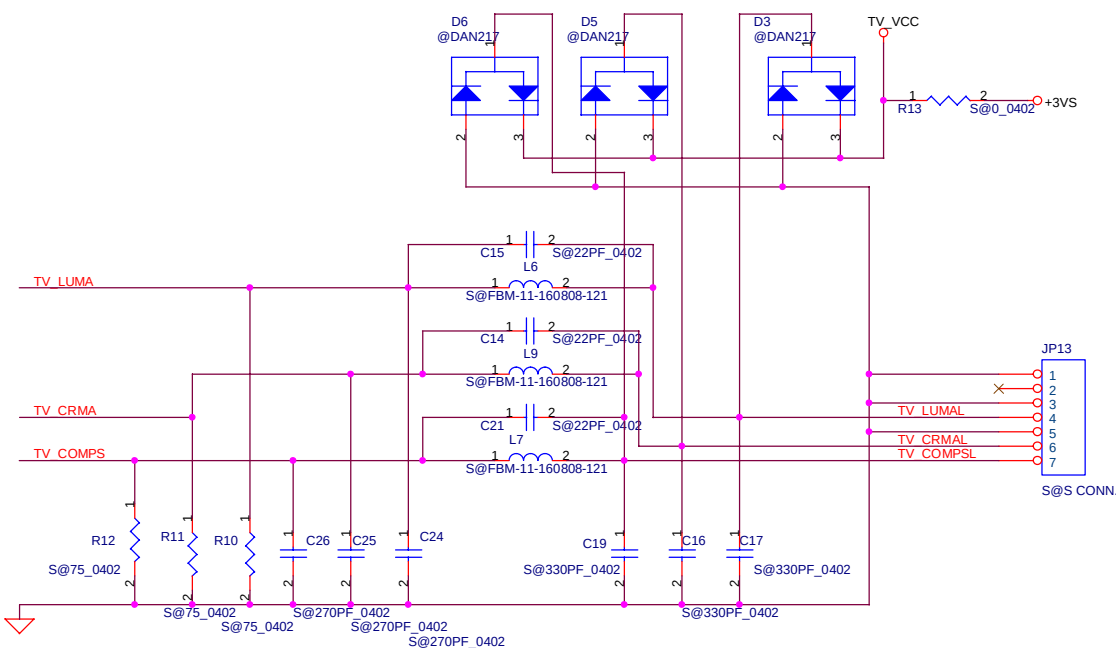
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Size 401224	Document Number	Rev 0B
Custom Date: 星期三, 八月 21, 2002	Sheet 14 of 43	

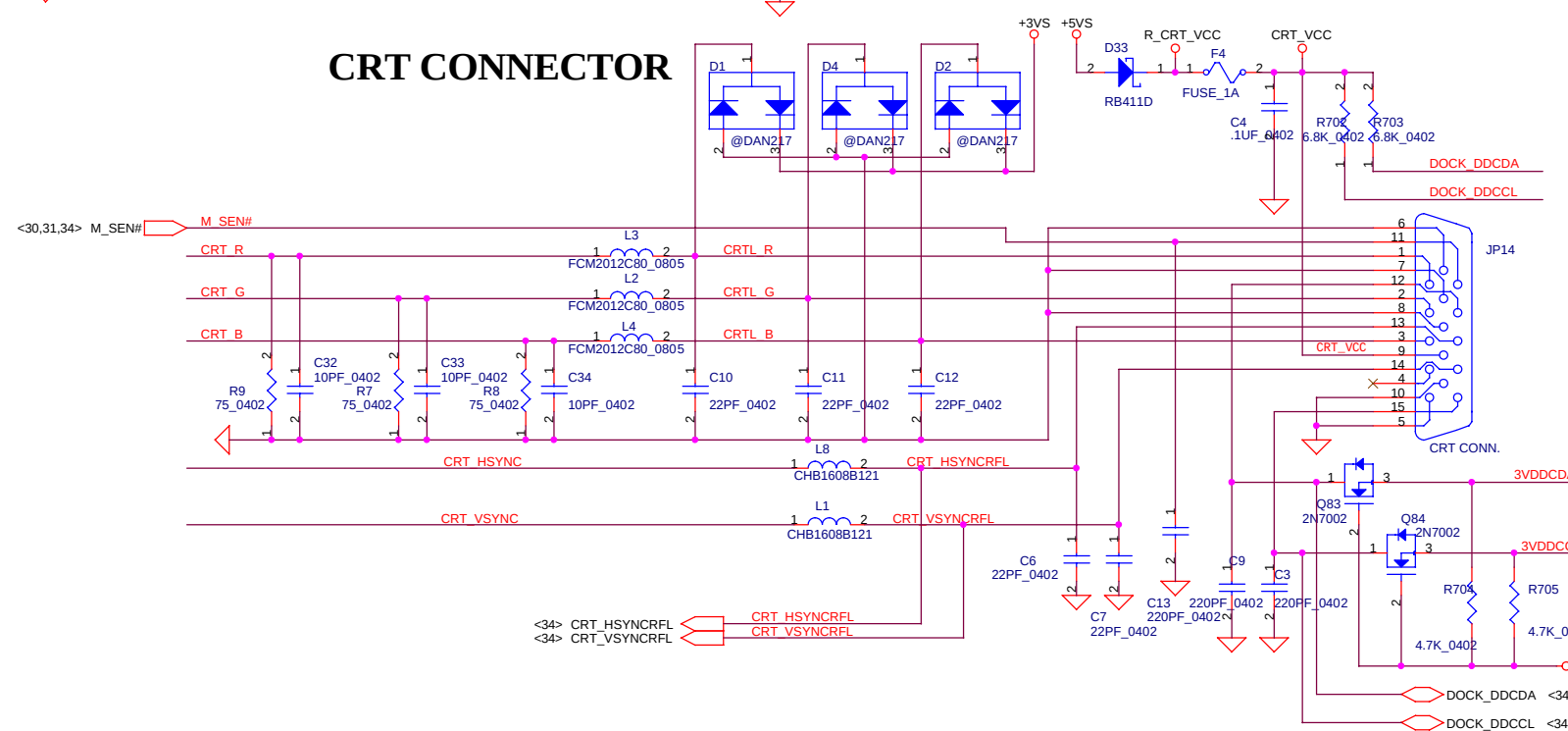
AGP 100X2 Pin connector



TV_OUT CONNECTOR

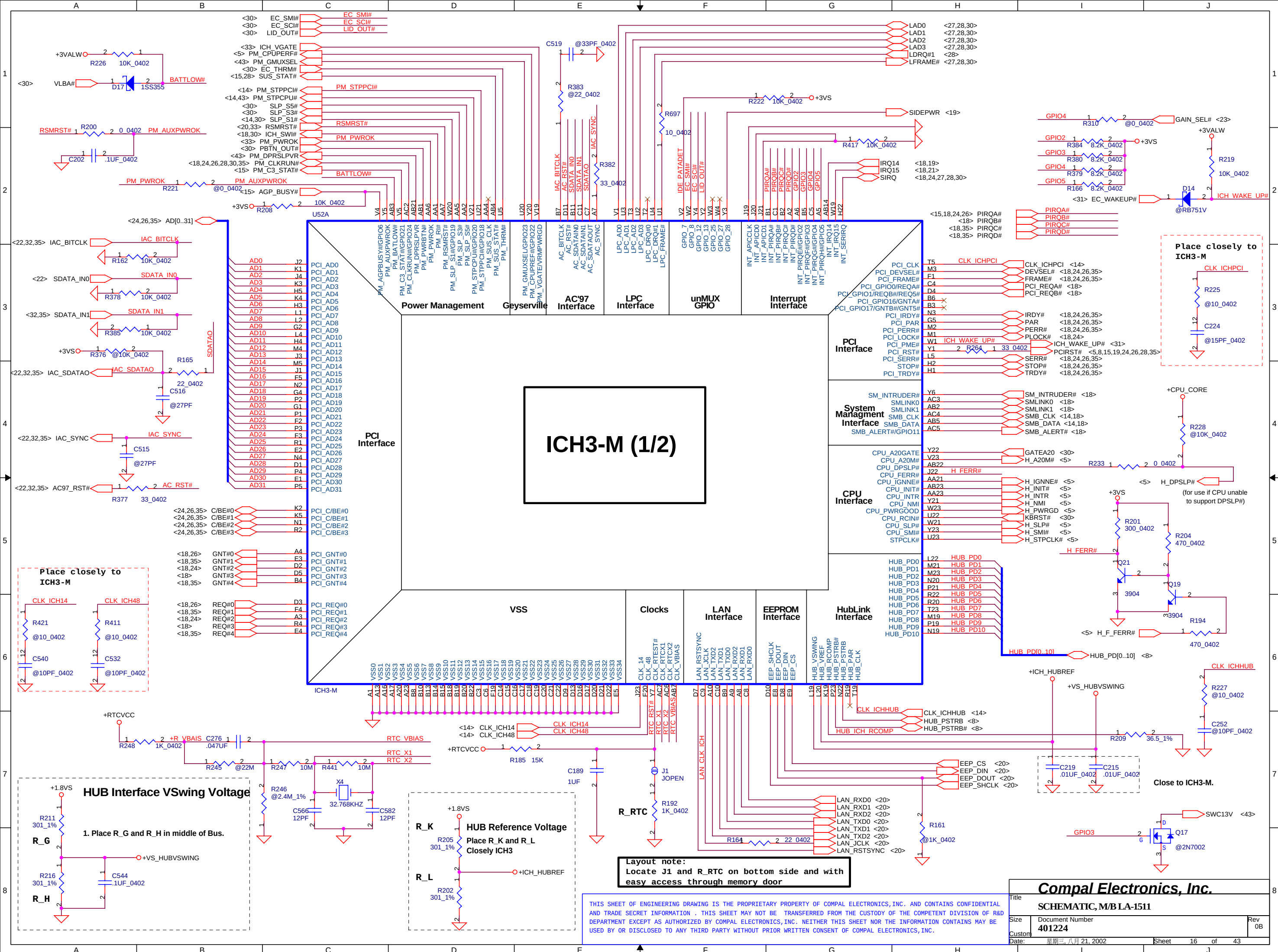


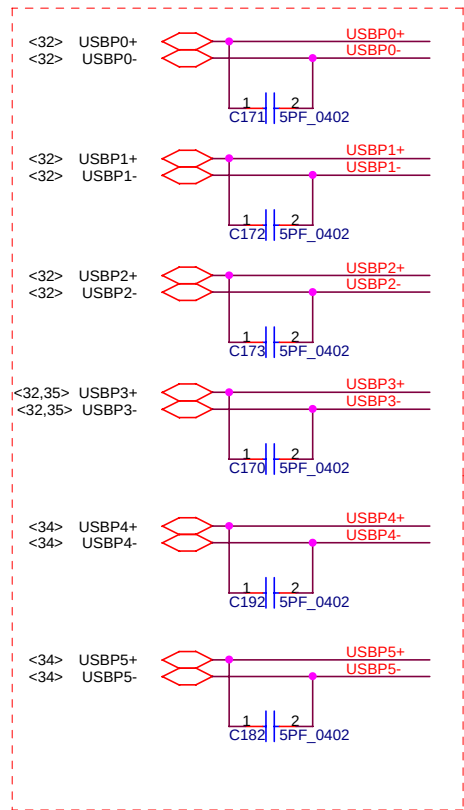
CRT CONNECTOR



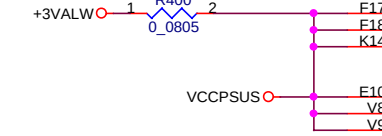
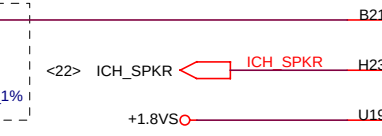
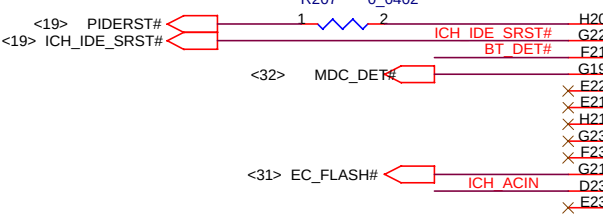
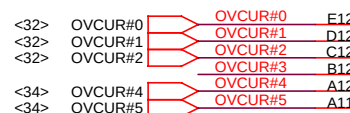
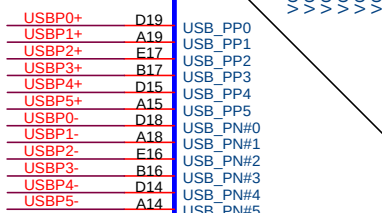
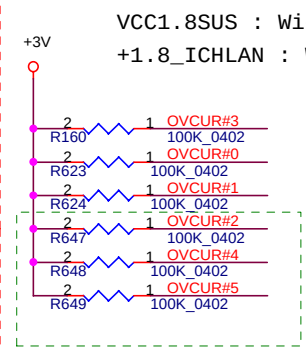
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Compal Electronics, Inc.			
Title SCHEMATIC, M/B LA-1511			
Size	Document Number 401224		Rev 0B
Date	Date 星期三 八月 21, 2002		Sheet 15 of 43

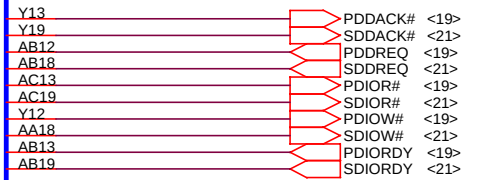
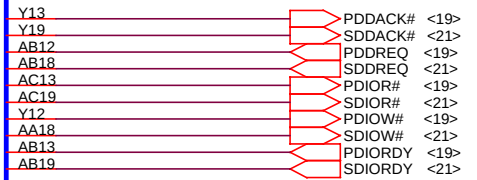
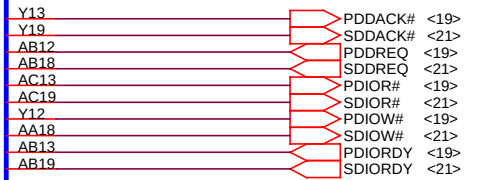
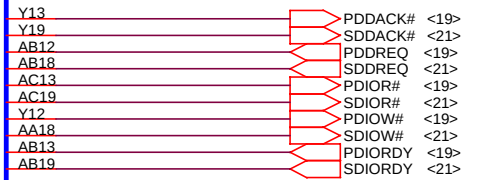
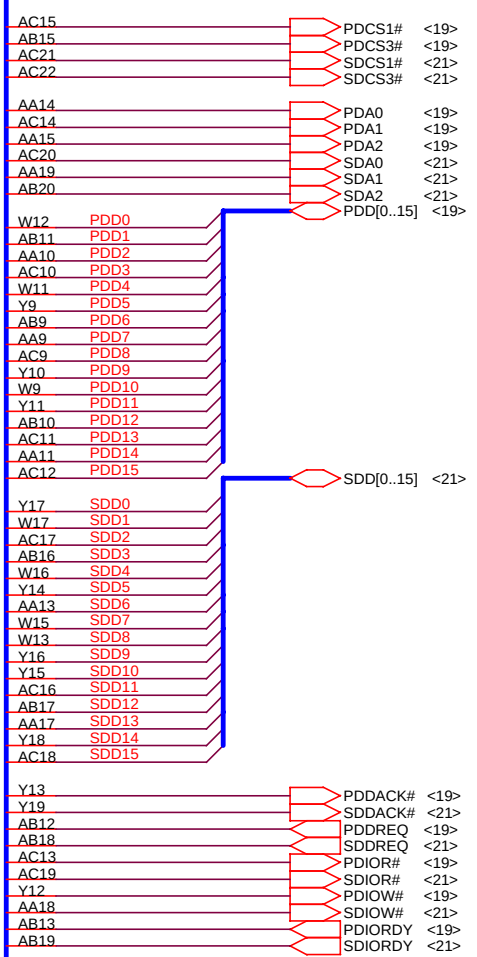
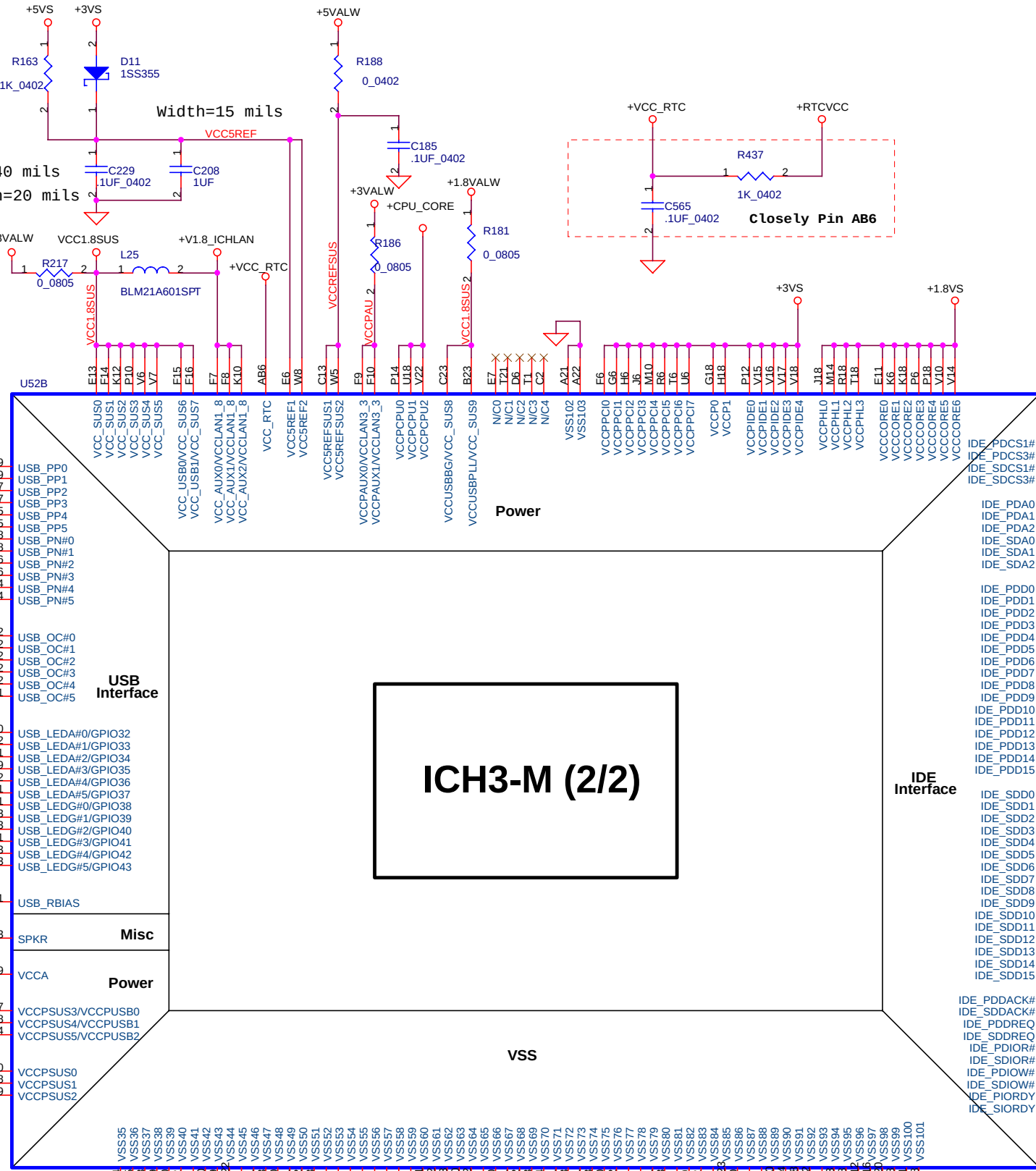
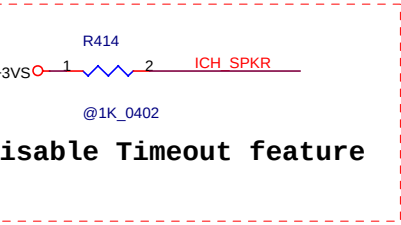




Layout note The Cap close to ICH3-M(< 1 inch)

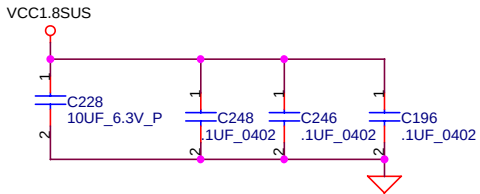
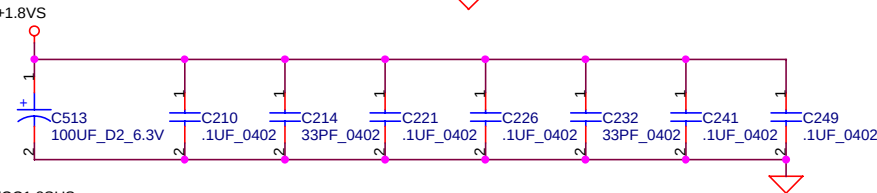
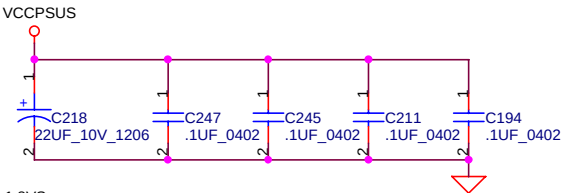
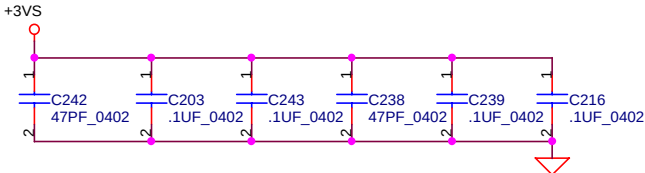
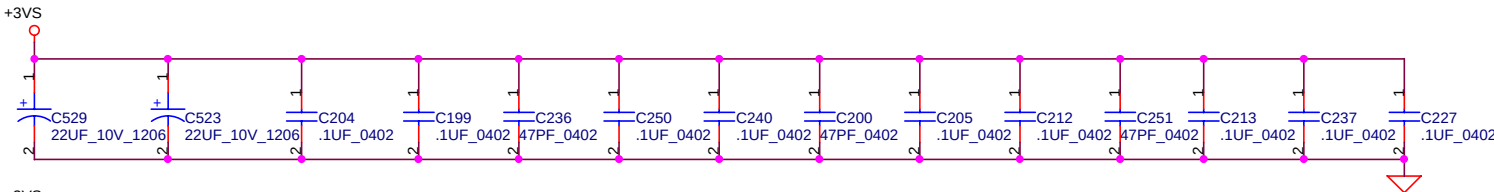
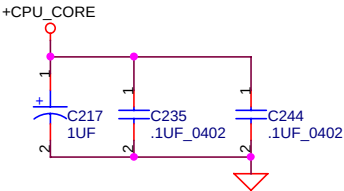
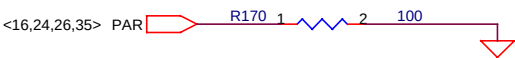
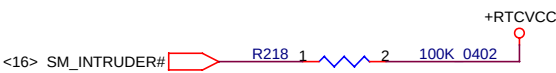
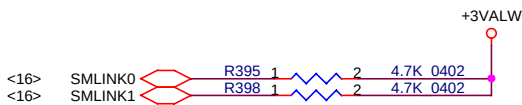
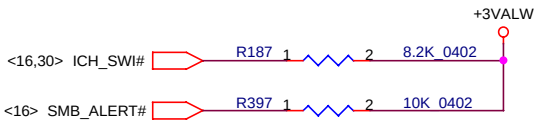
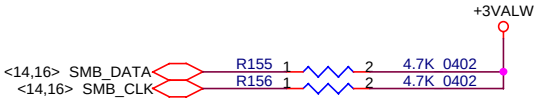
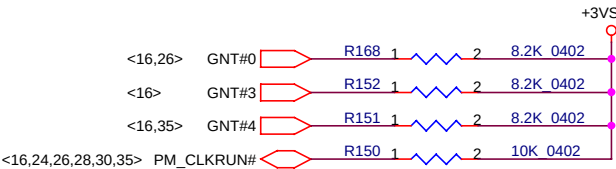
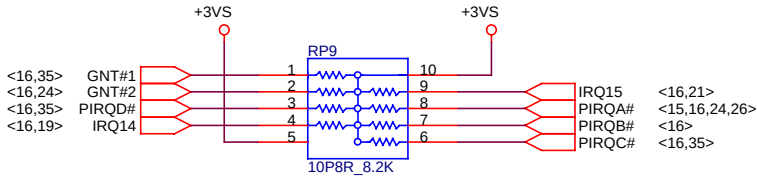
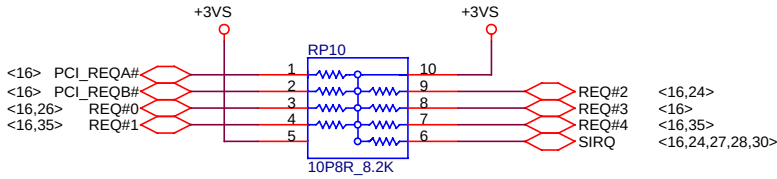
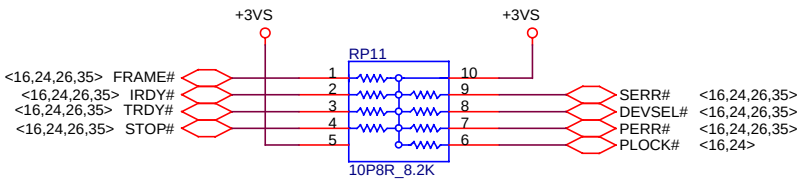


Note: R376=22.6_1% for B0(QB63 part)
R376=18.2_1% for B0(QB62 & SL5LF part)



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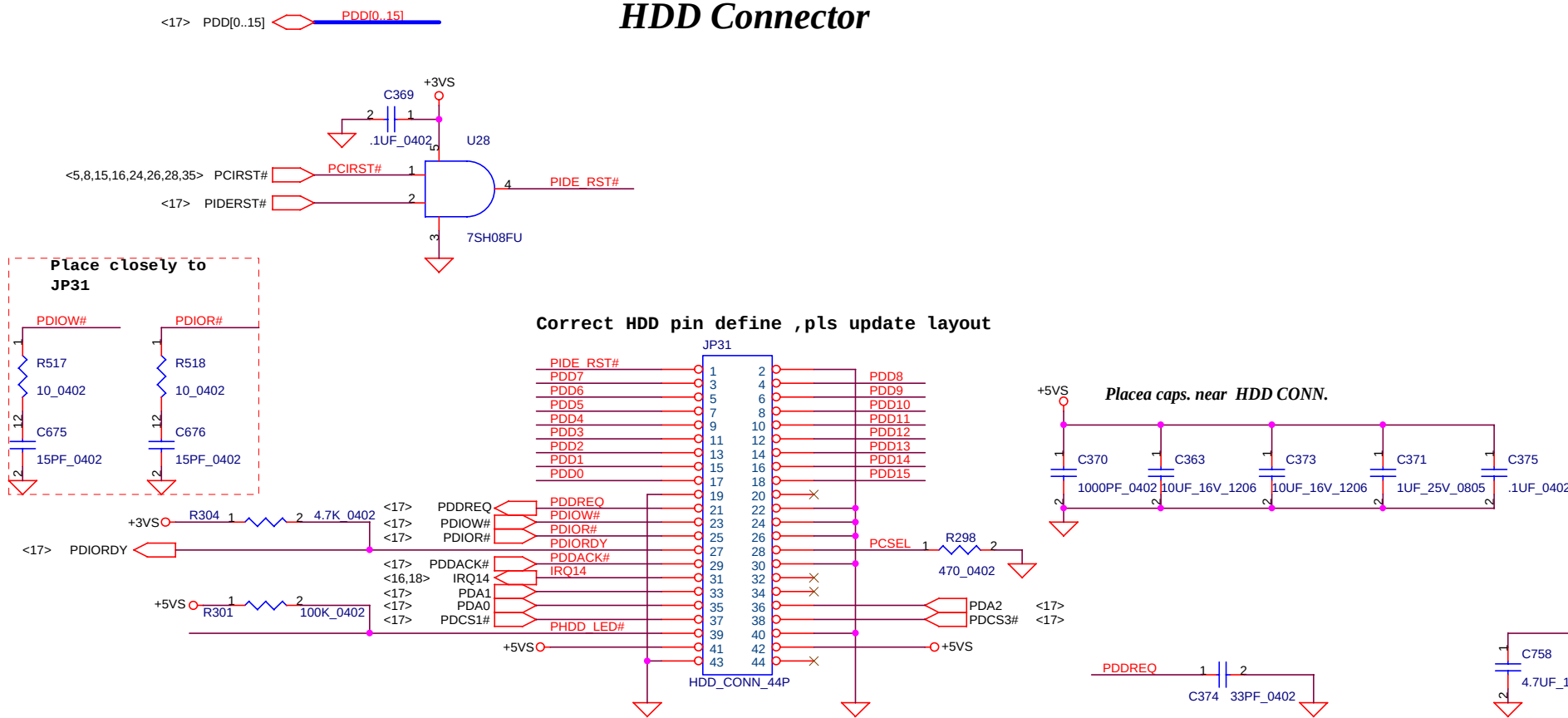
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SCHEMATIC, M/B LA-1511			
Size	Document Number		Rev
	401224		OB
Custom			
Date:	星期三, 八月 21, 2002	Sheet	17 of 43



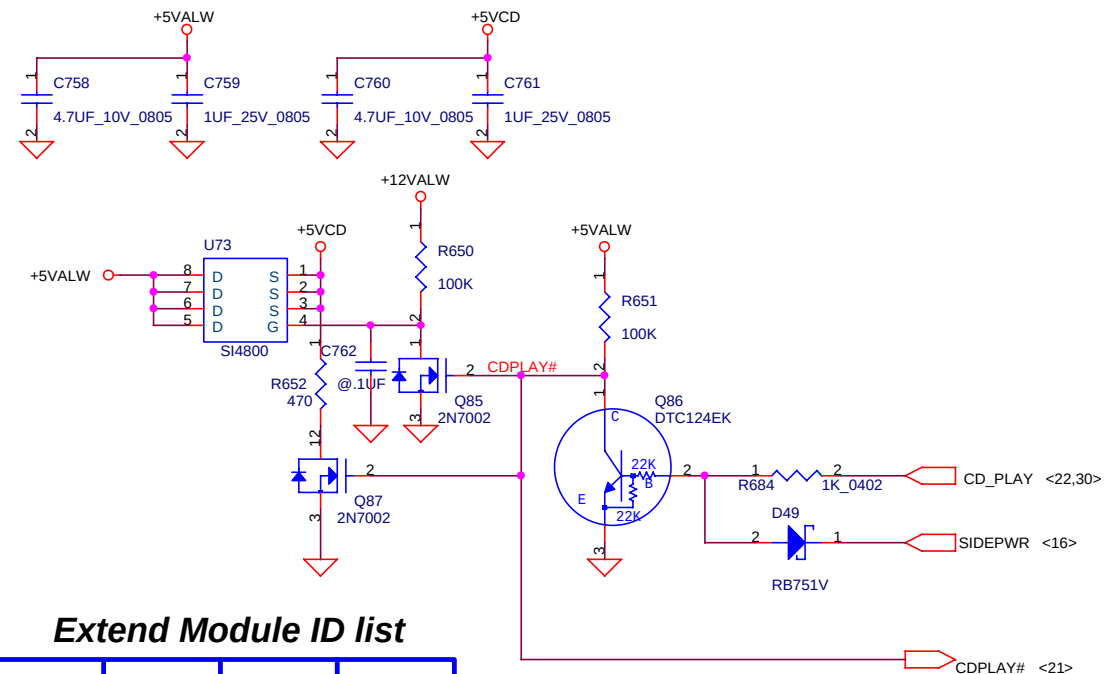
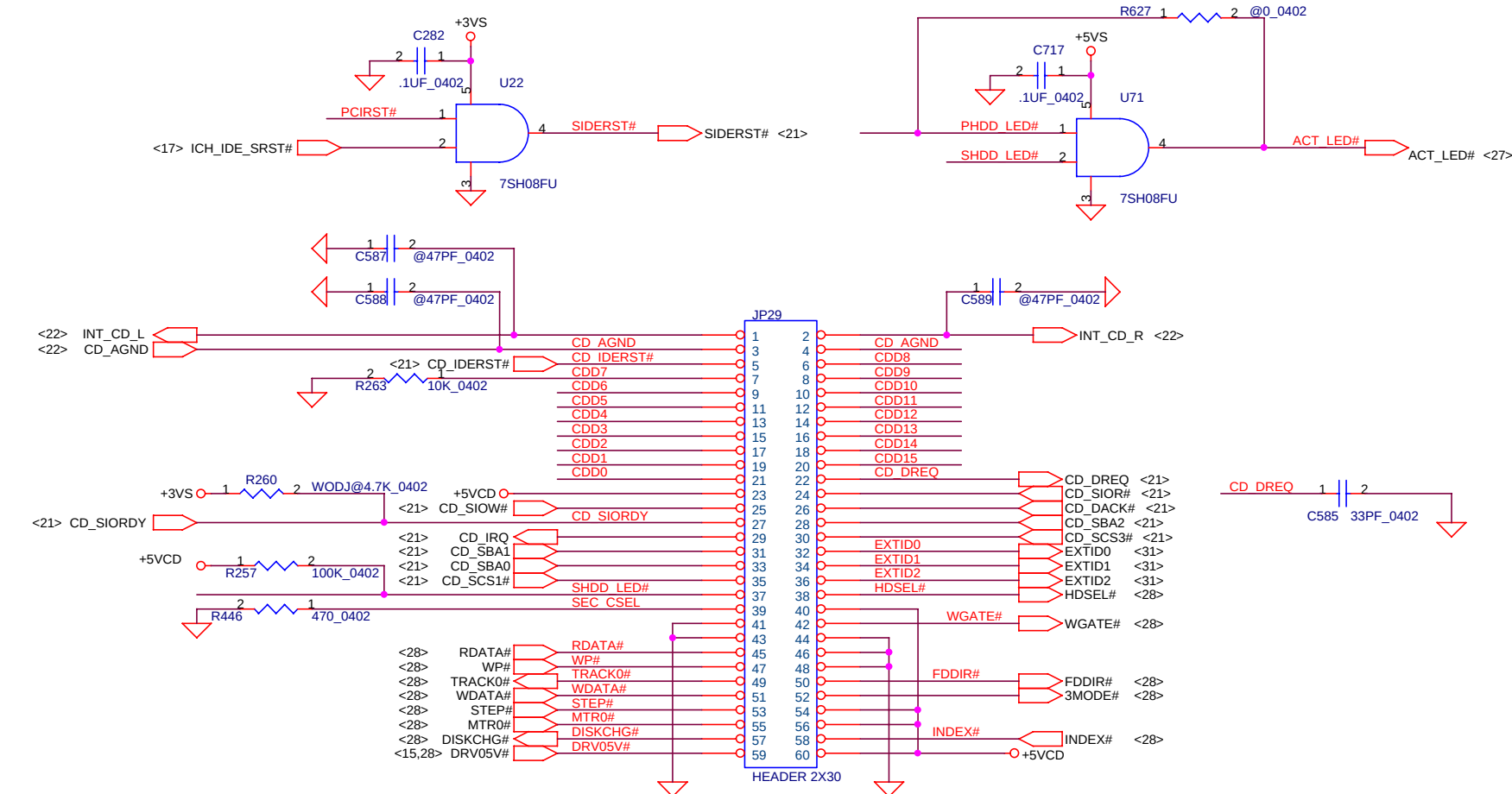
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Title			
SCHEMATIC, M/B LA-1511			
Size	Document Number		Rev
	401224		0B
Custom			
Date:	星期三, 八月 21, 2002		Sheet 18 of 43

HDD Connector



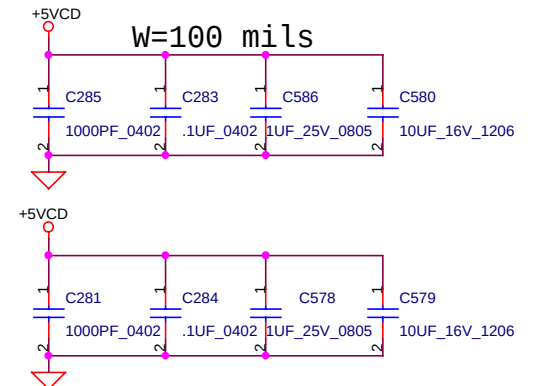
CD-ROM Connector



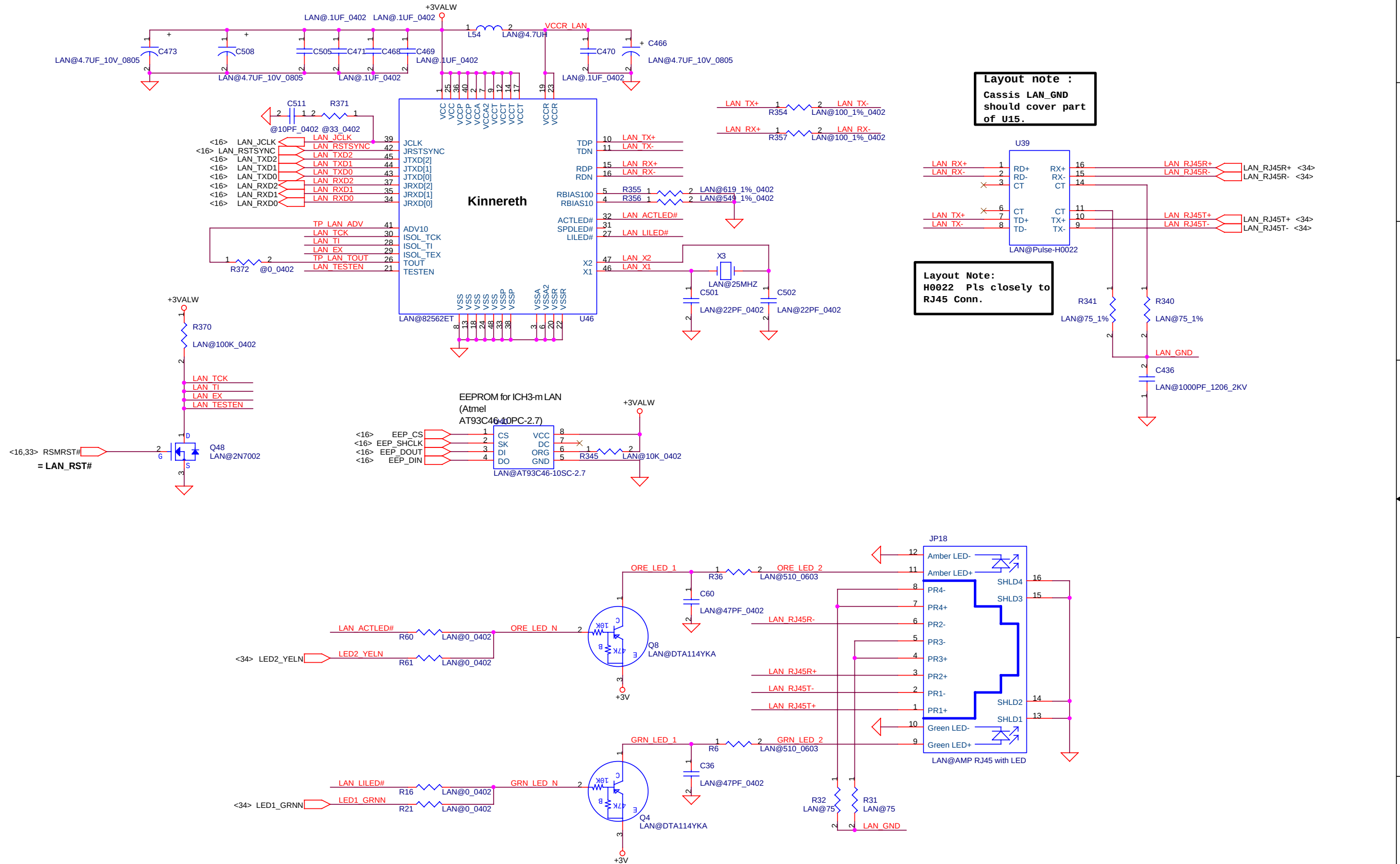
Extend Module ID list

DEVICE	EXTID2	EXTID1	EXTID0
FDD	0	0	0
CD-ROM	0	0	1
LS-120	0	1	0
2'nd HDD	0	1	1
NONE	1	1	1

**Placea caps. near CDROM
CONN.**

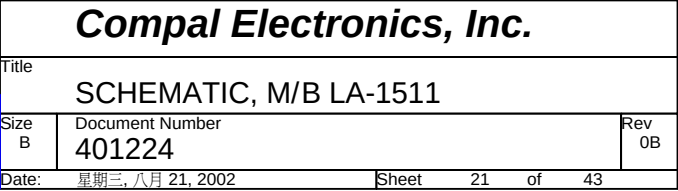


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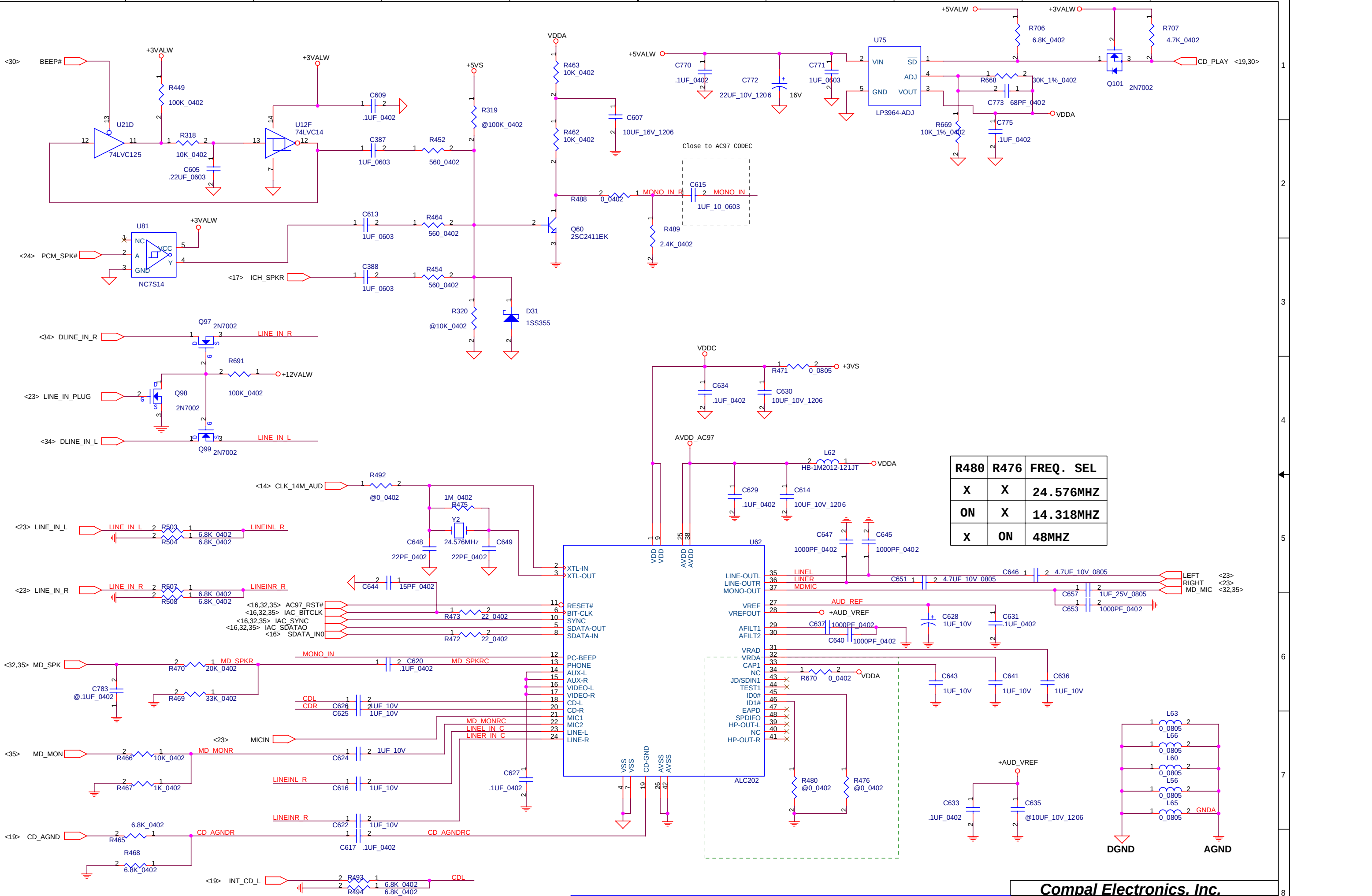


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Title	SCHEMATIC, M/B LA-1511		
Size	Document Number	Rev	
Custom	401224	OB	
Date:	星期三, 八月 21, 2002	Sheet	20 of 43
	2		1



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R480	R476	FREQ. SEL
X	X	24.576MHZ
ON	X	14.318MHZ
X	ON	48MHZ

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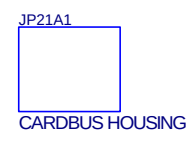
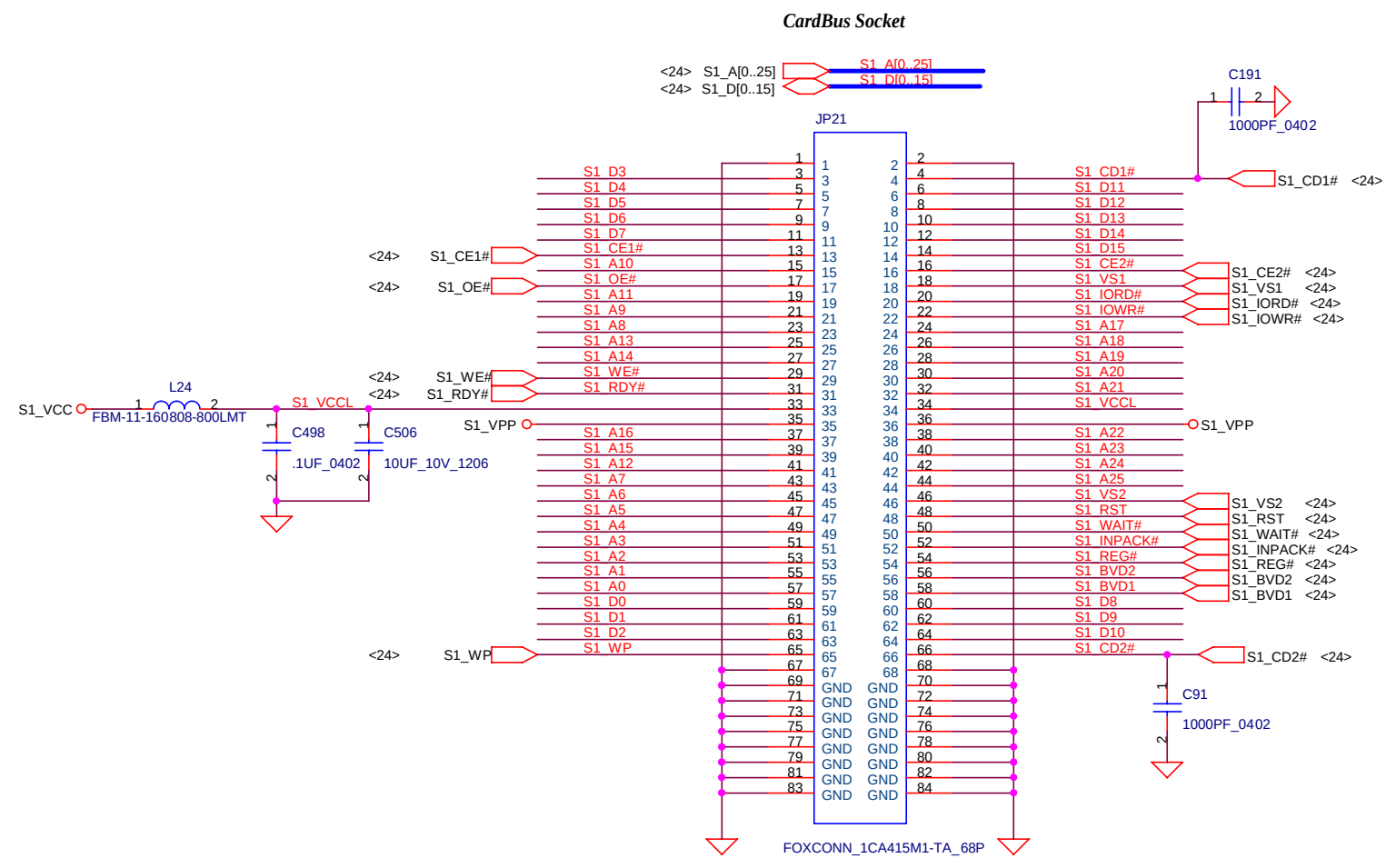
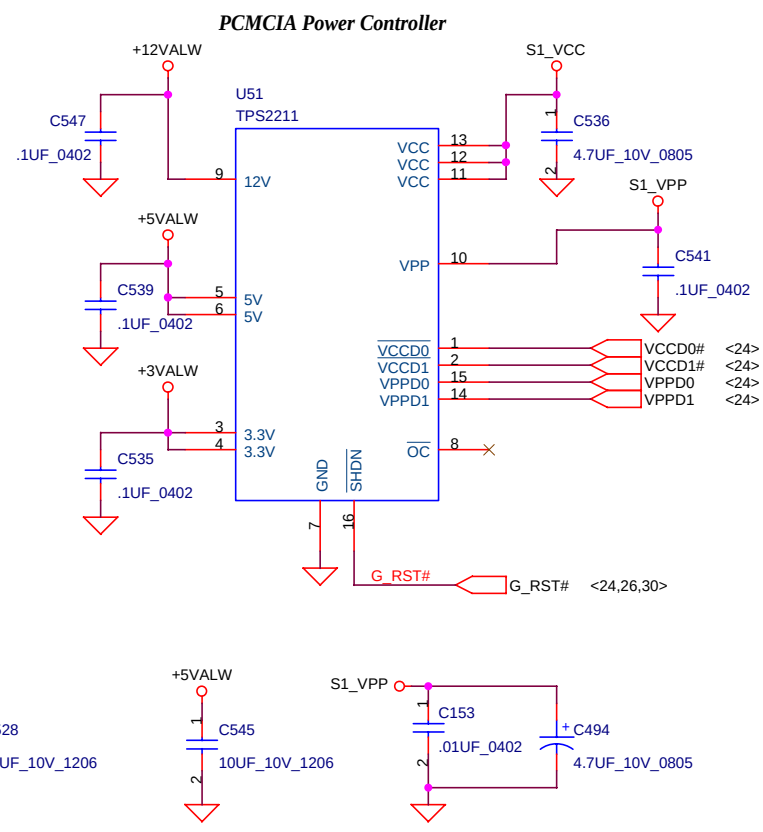
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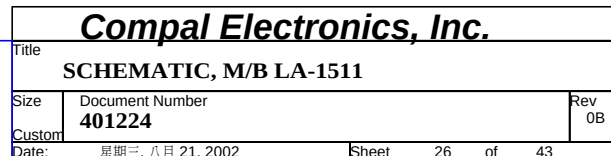
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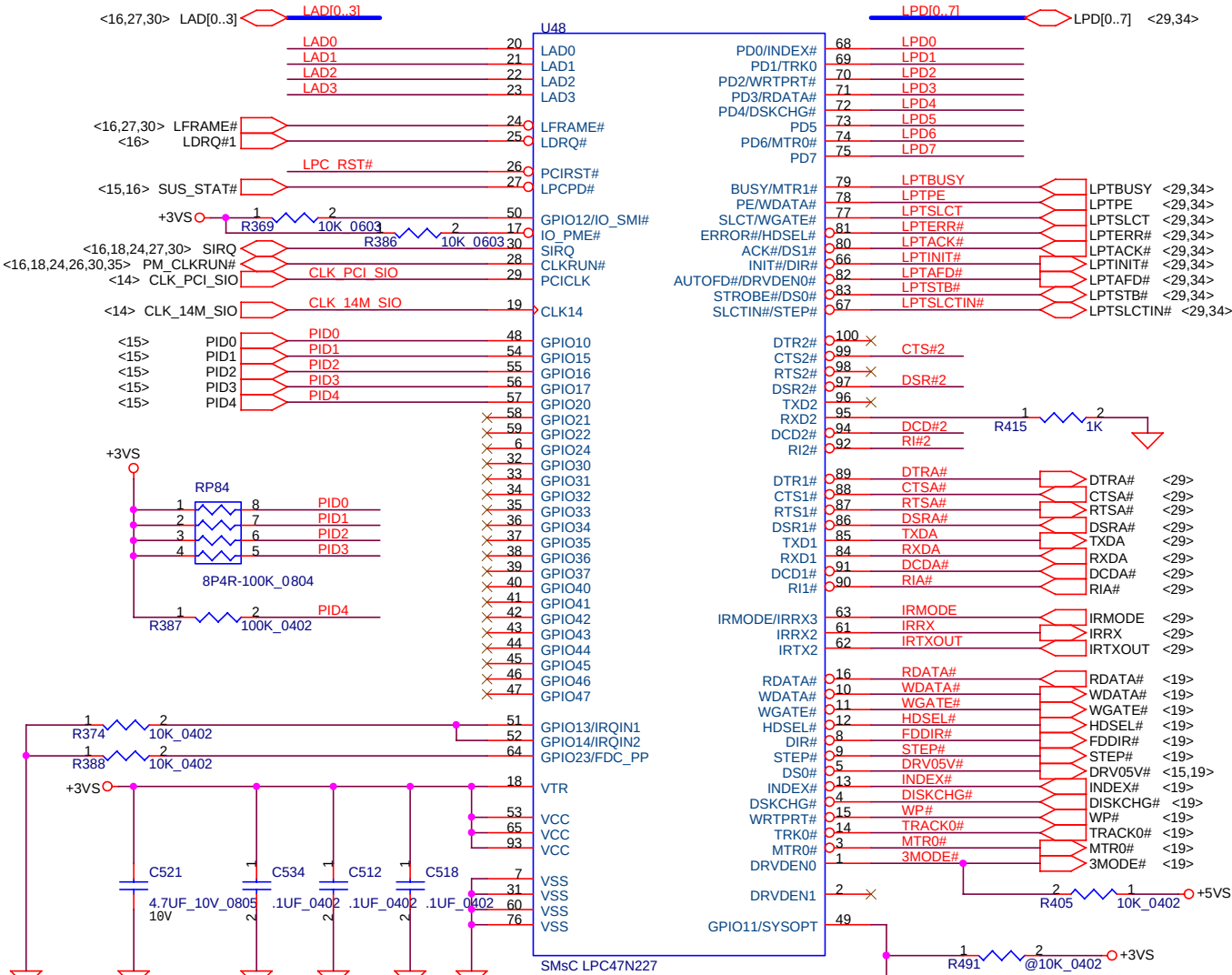
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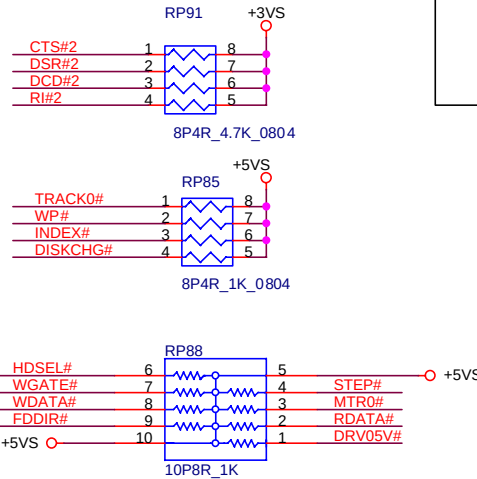
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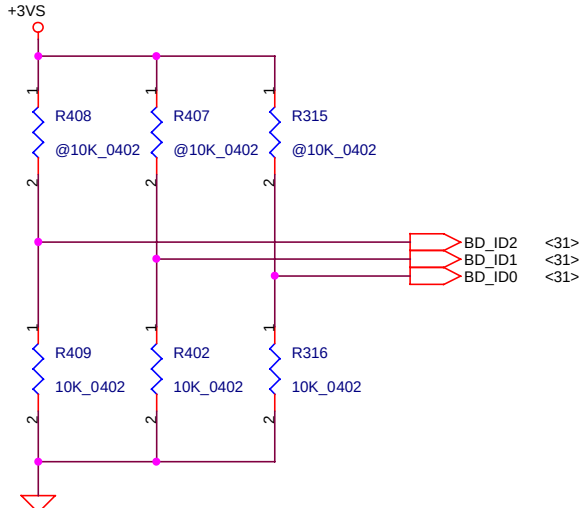
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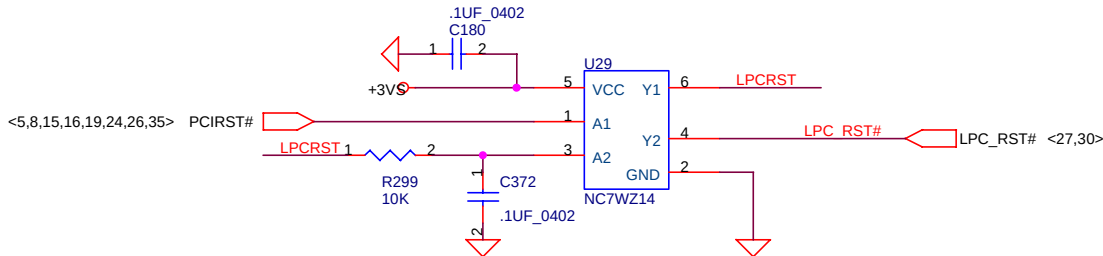
	Base I/O Address
0	= 02Eh
* 1	= 04Eh



BOARD ID



	BD_ID2	BD_ID1	BD_ID0
SST	0	0	0
PT	0	0	1
ST	0	1	0
QT	0	1	1



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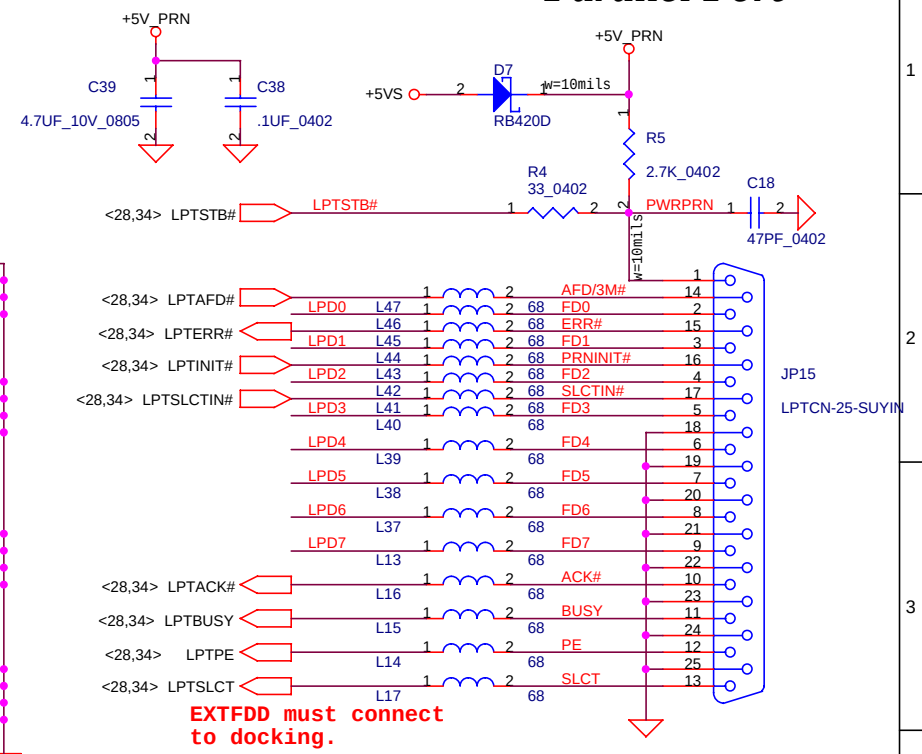
Size	Document Number
	401224

Rev
0B

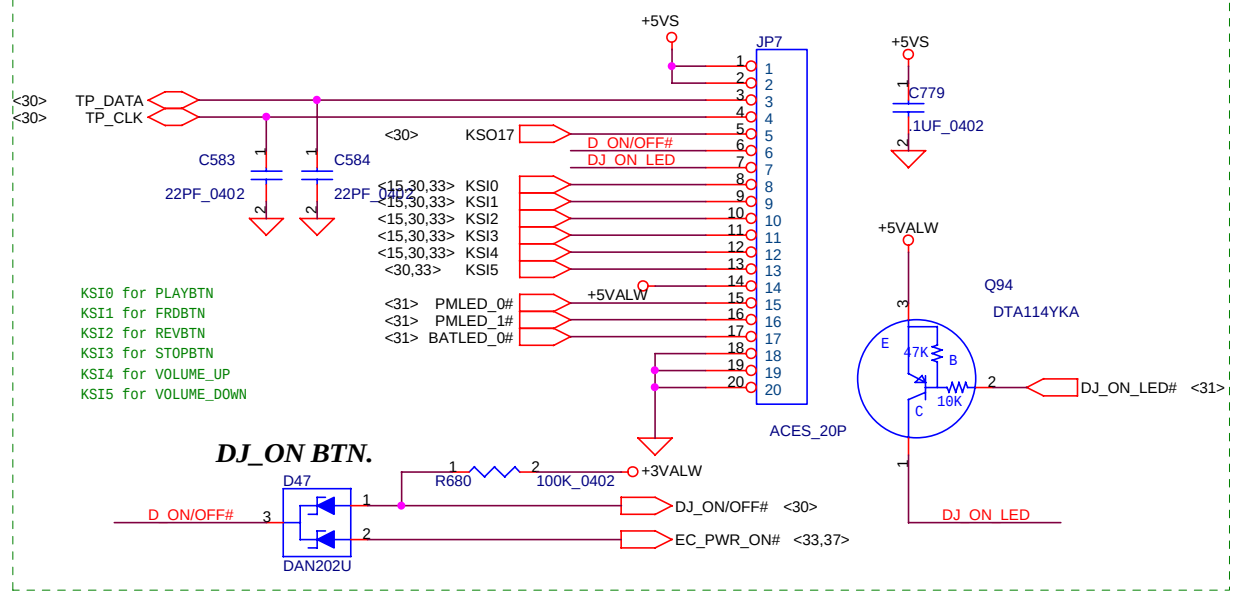
星期三, 八月 21, 2002

Sheet 28 of 43

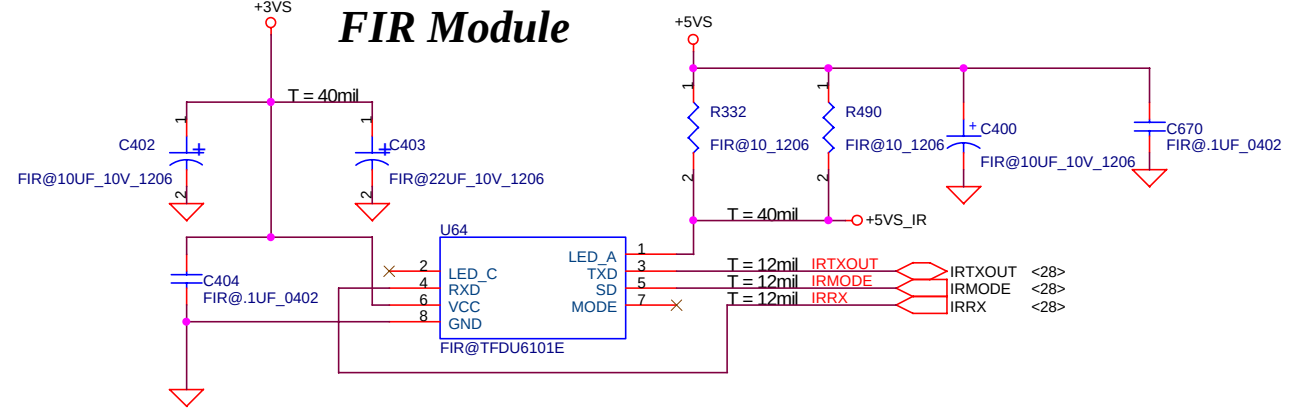
Parallel Port



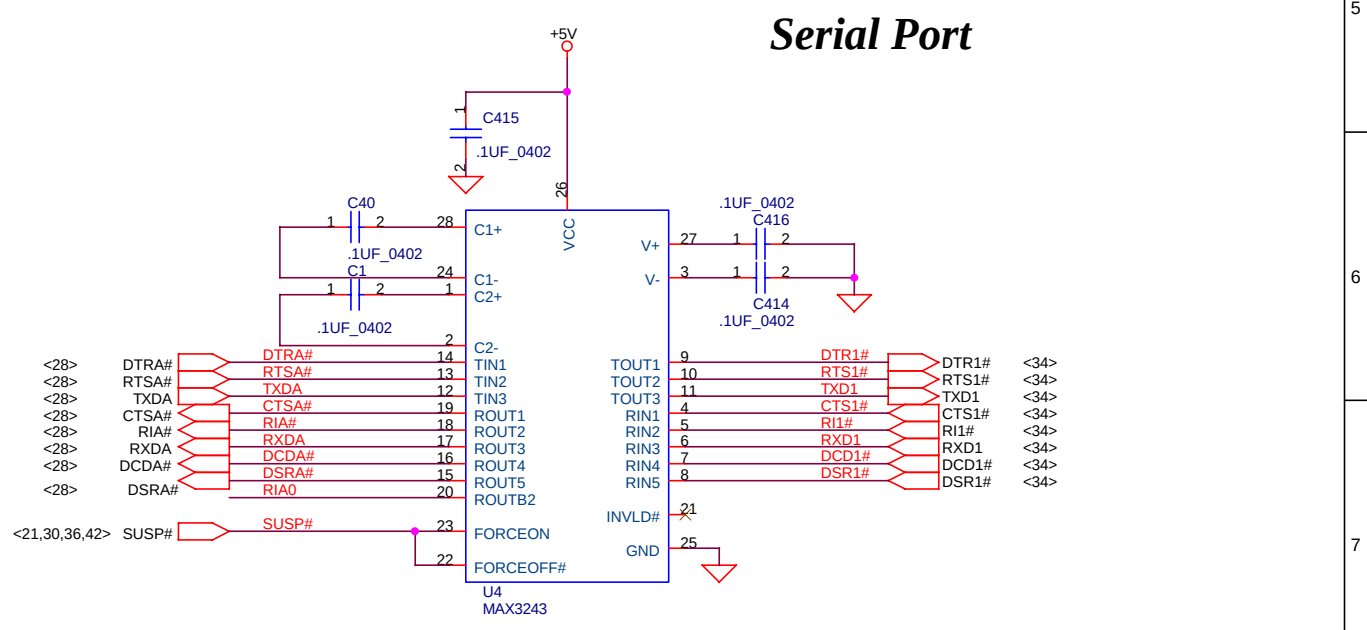
Touch Pad & Status LED Conn.



FIR Module



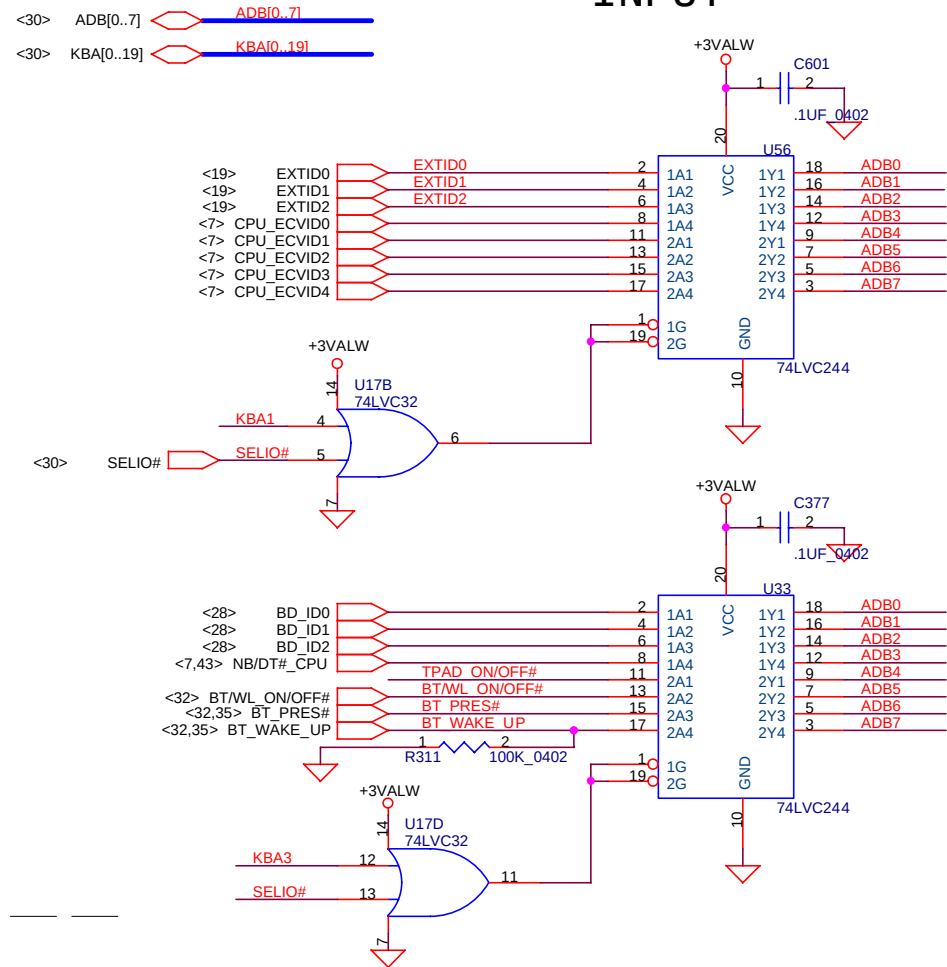
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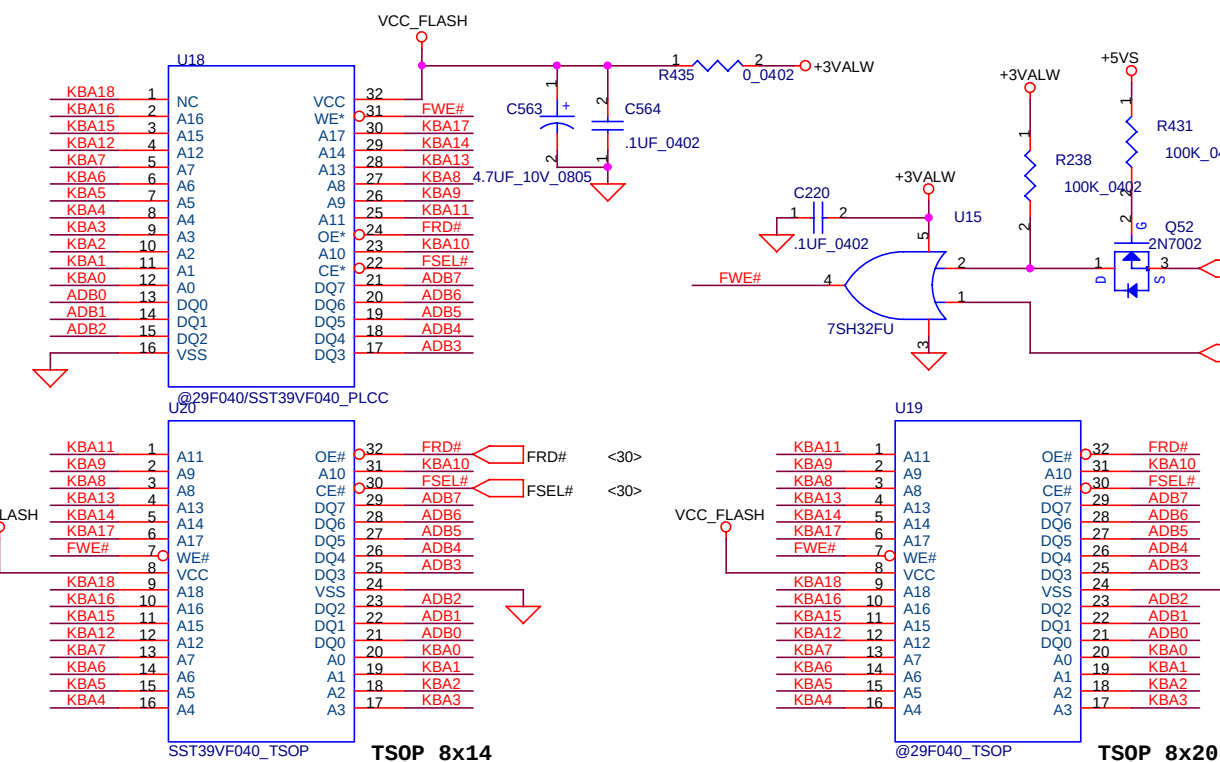
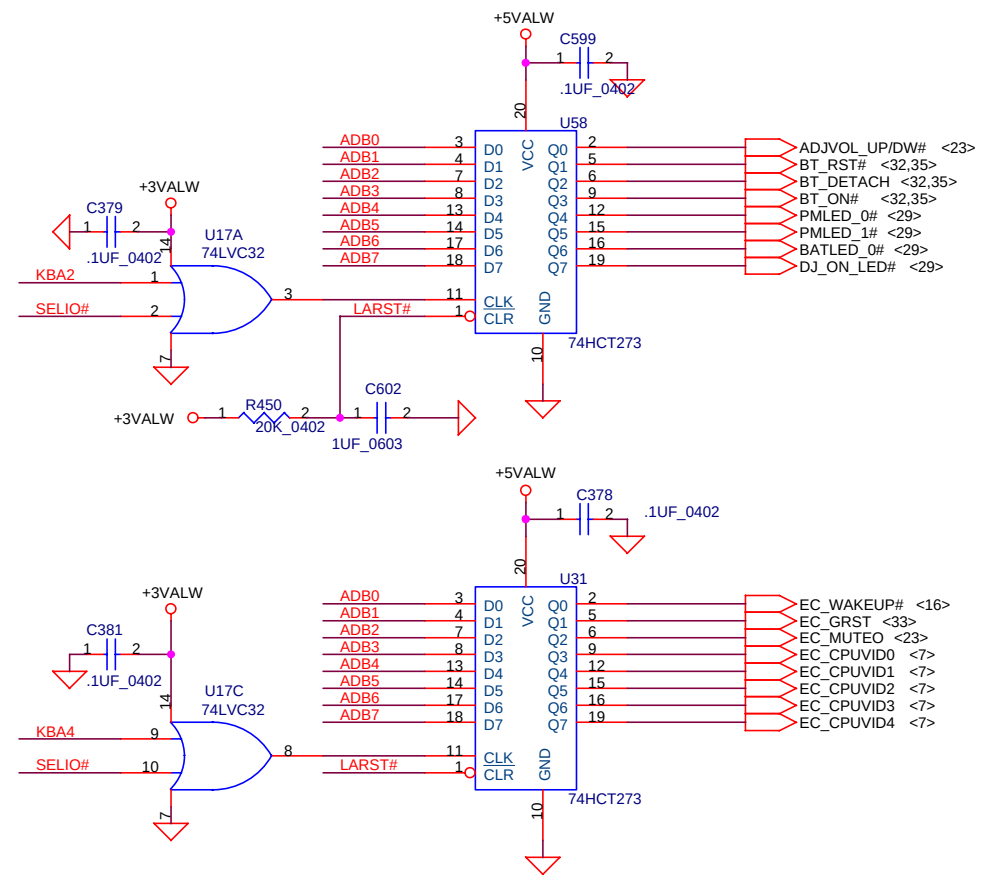
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Title	SCHEMATIC, M/B LA-1511	
Size	Document Number	Rev
401224		0B
Custom		
Date:	星期三, 八月 21, 2002	Sheet 29 of 43

INPUT



OUTPUT

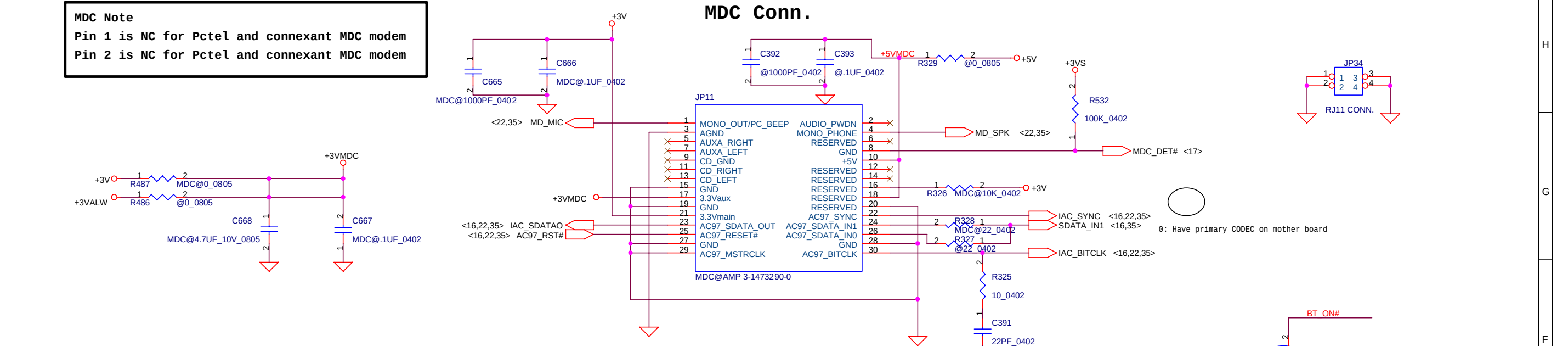


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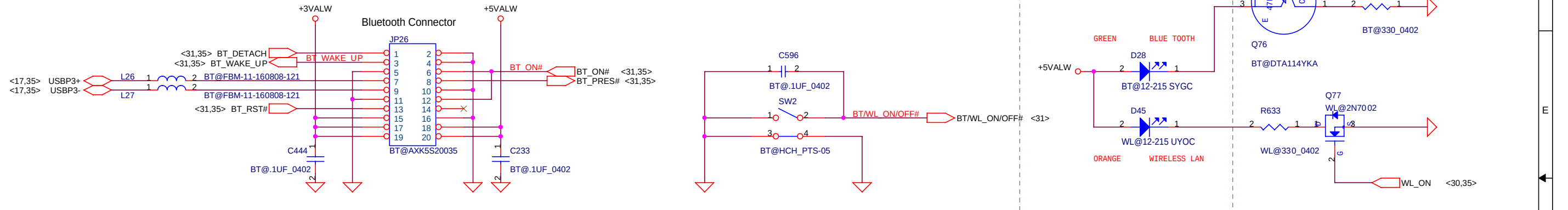
Compal Electronics, Inc.		
SCHEMATIC, M/B LA-1511		
Title Size Document Number 401224 Date 星期三, 八月 21, 2002	Rev 0B	Sheet 31 of 43

MDC Note
Pin 1 is NC for Pctel and connexant MDC modem
Pin 2 is NC for Pctel and connexant MDC modem

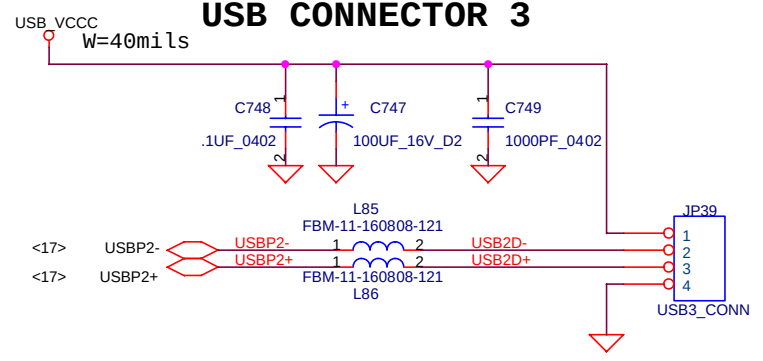
MDC Conn.



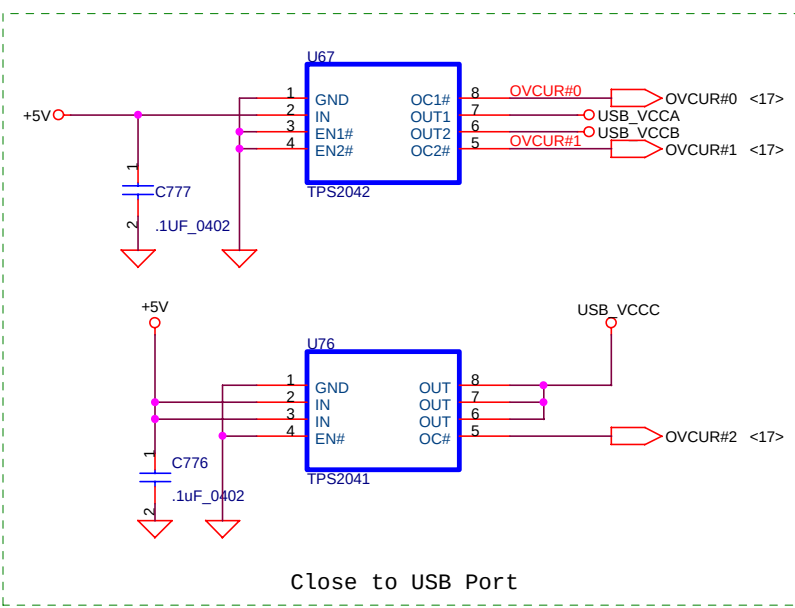
BlueTooth Interface



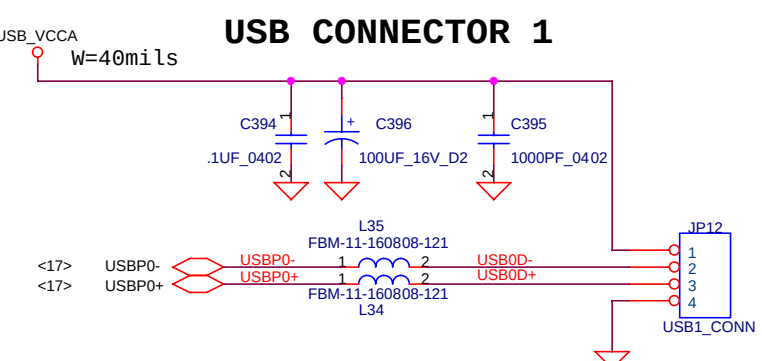
USB CONNECTOR 3



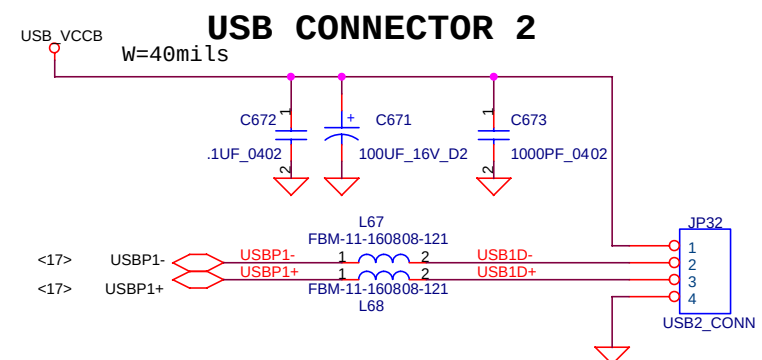
Close to USB Port



USB CONNECTOR 1



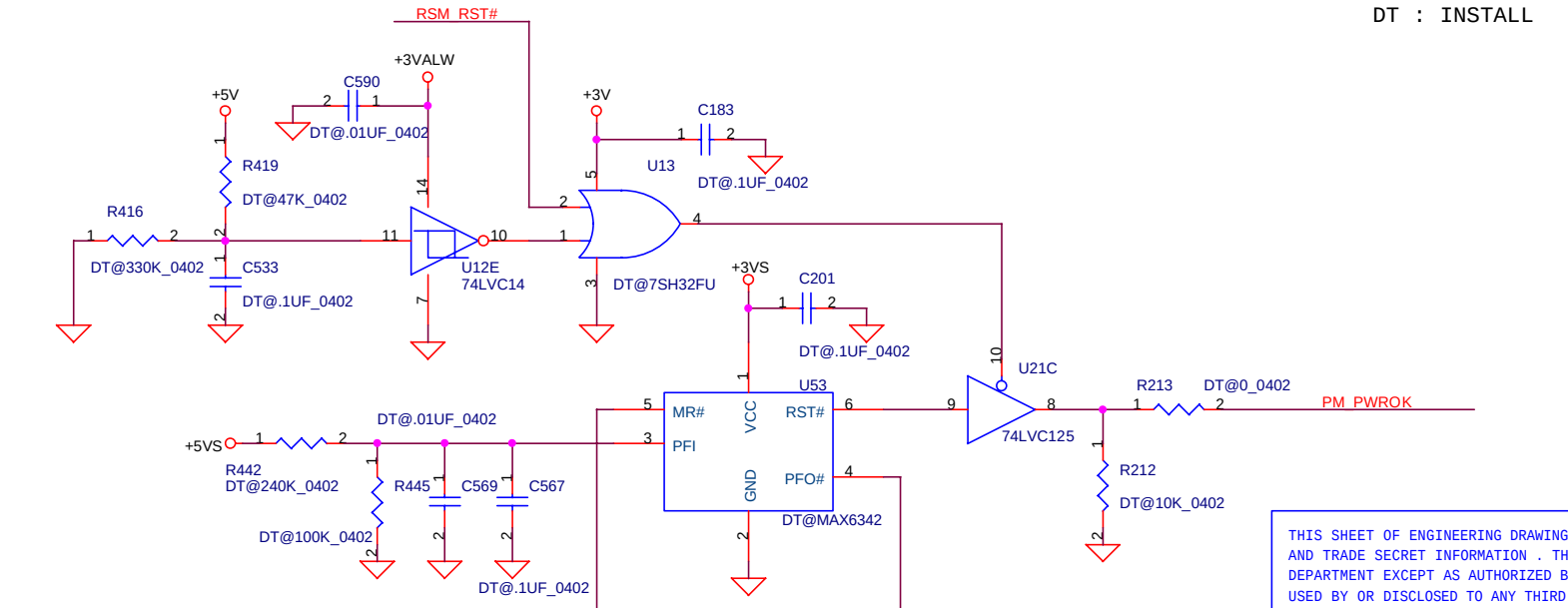
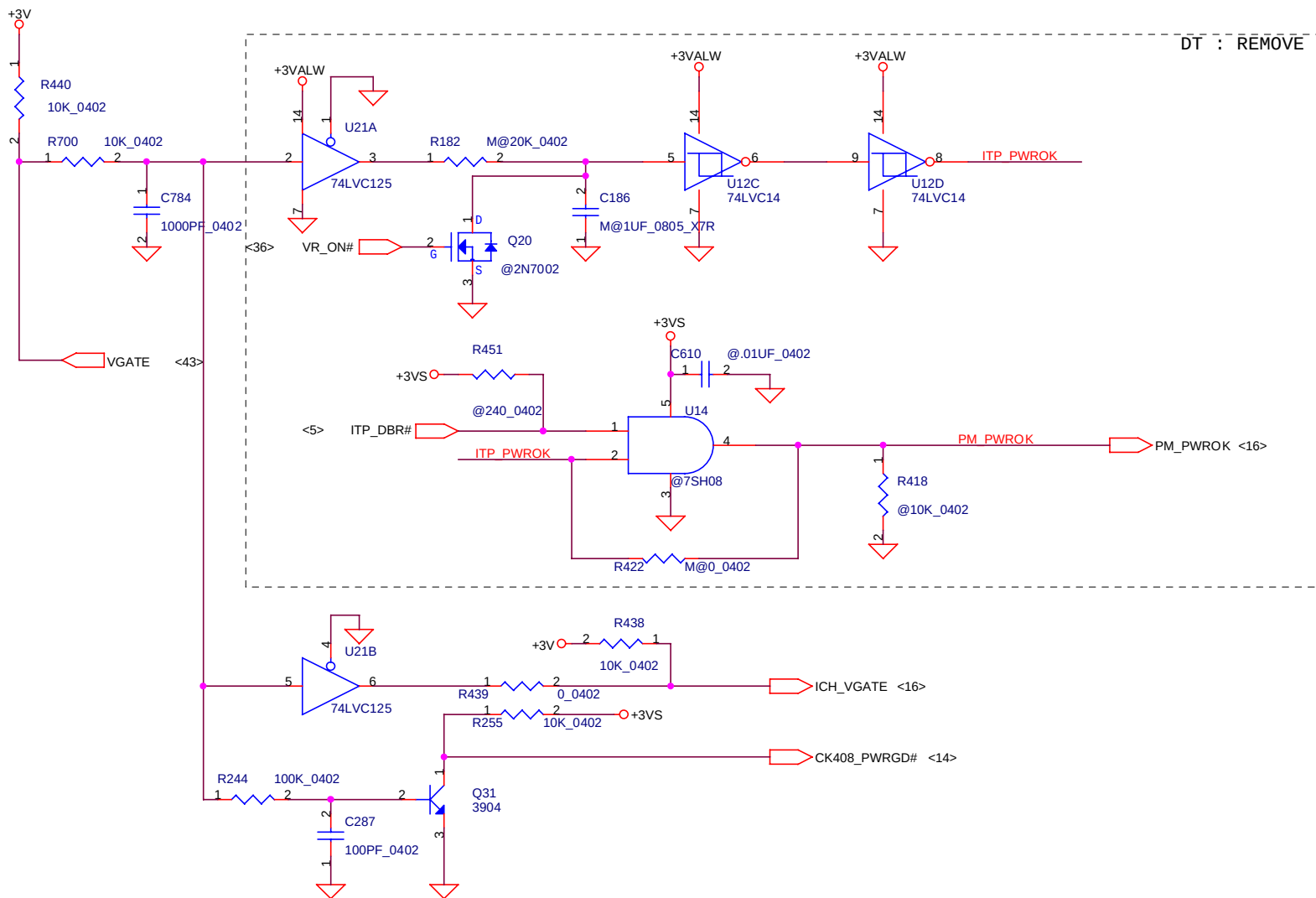
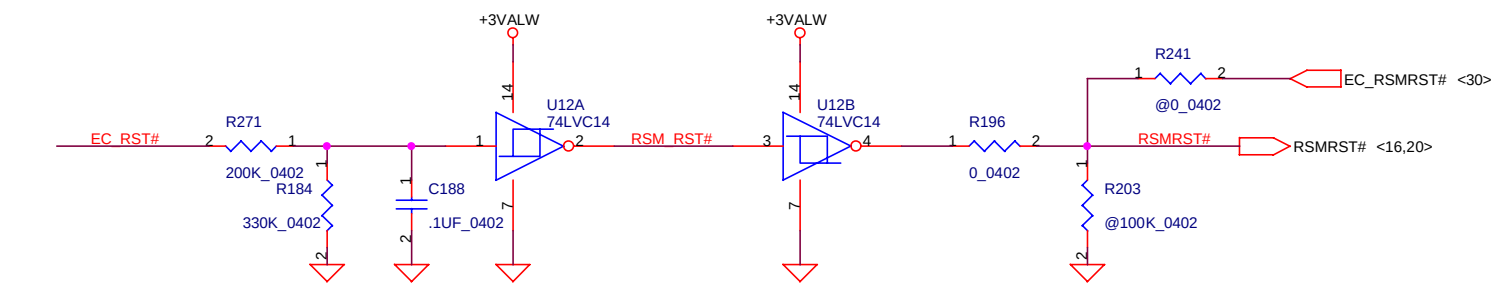
USB CONNECTOR 2



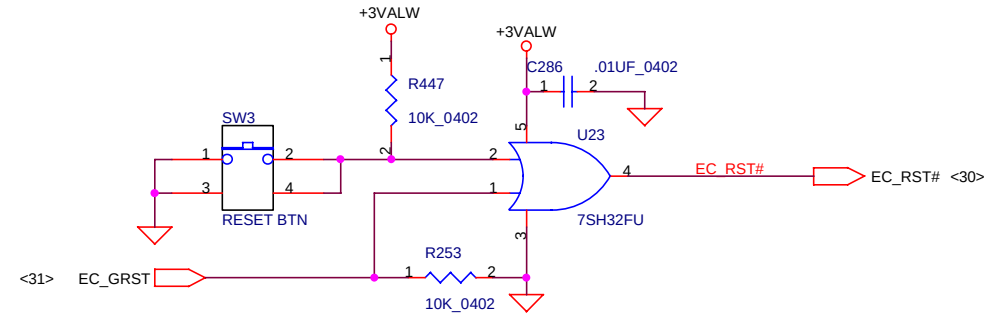
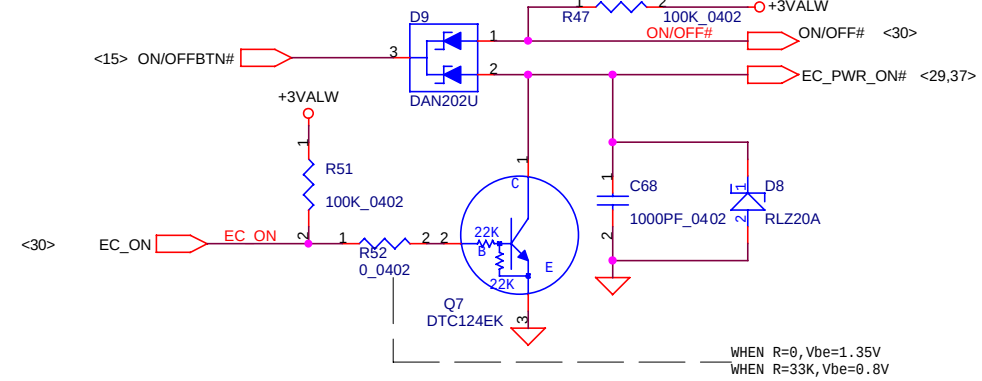
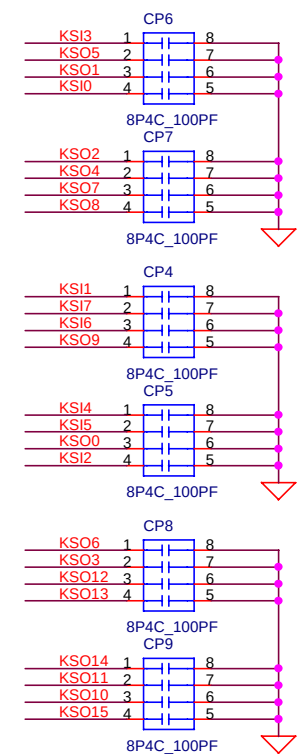
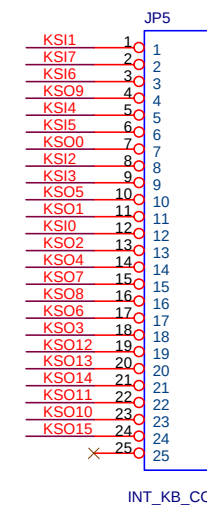
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Title		
SCHEMATIC, M/B LA-1511		
Size	Document Number	Rev
401224	401224	0B
Custom	Date:	Sheet
	星期三, 八月 21, 2002	32 of 43

Power ON Circuit



Reset Button

**Power BTN****INT_KBD CONN.**

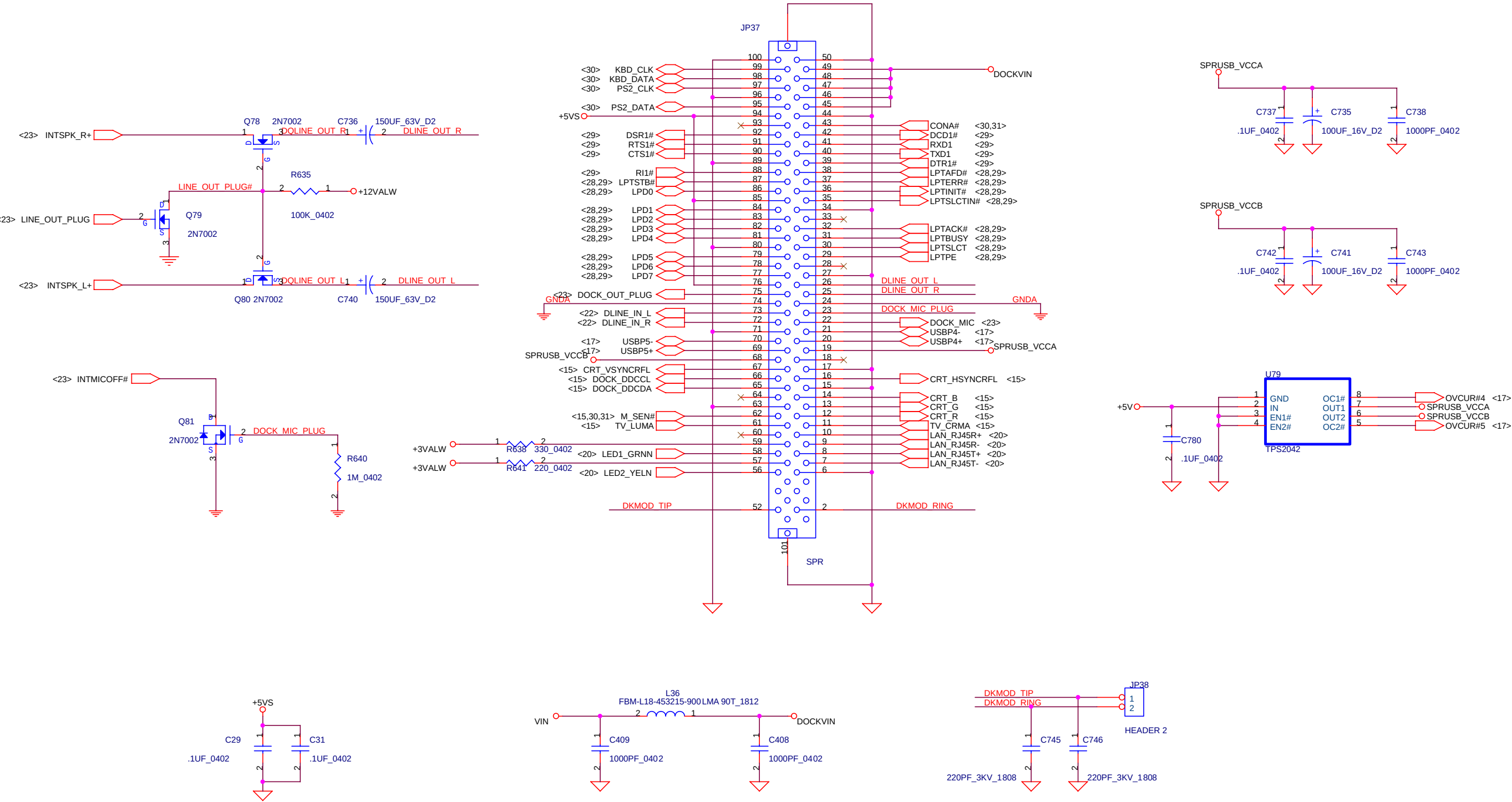
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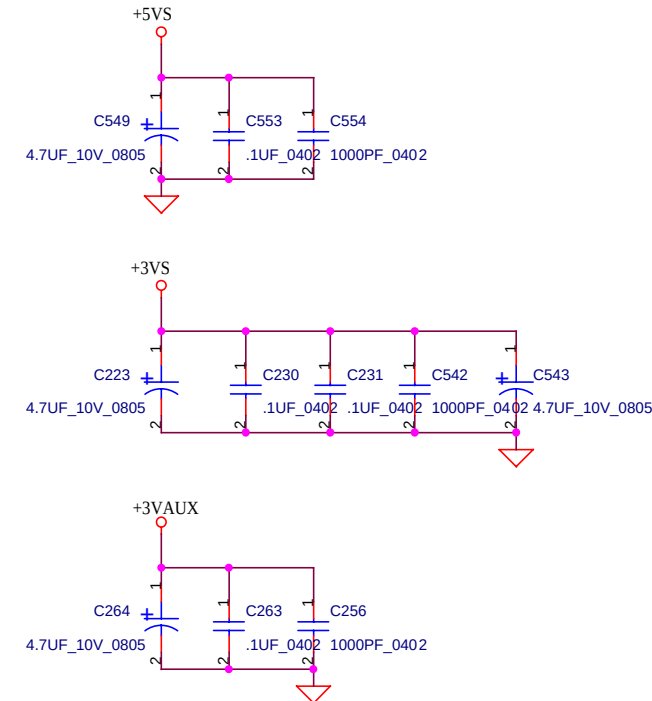
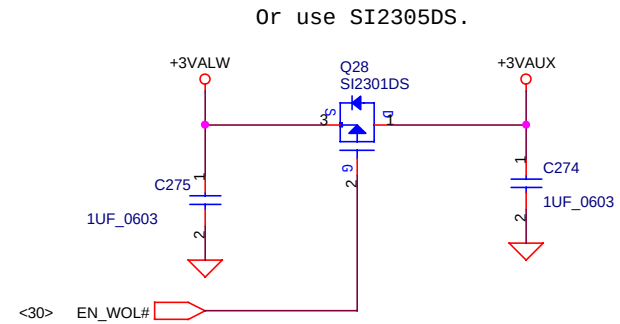
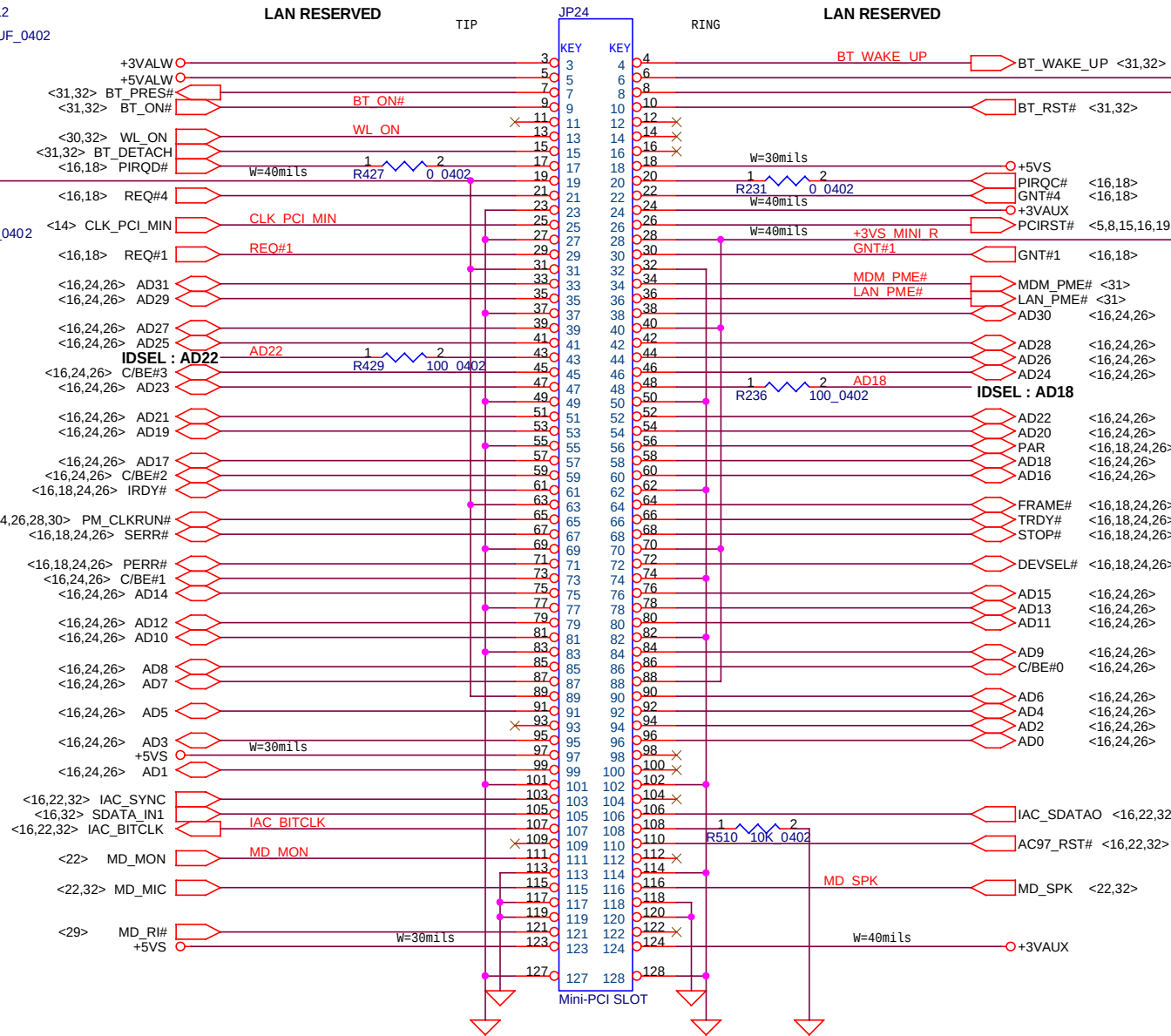
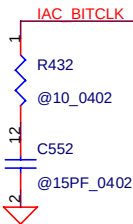
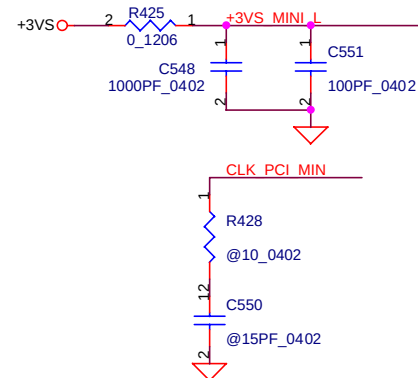
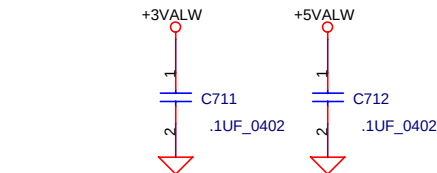
SCHEMATIC, M/B LA-1511

Size	Document Number	Rev
Custom	401224	0B
Date:	星期三, 八月 21, 2002	Sheet 33 of 43

DOCKING 204 PIN

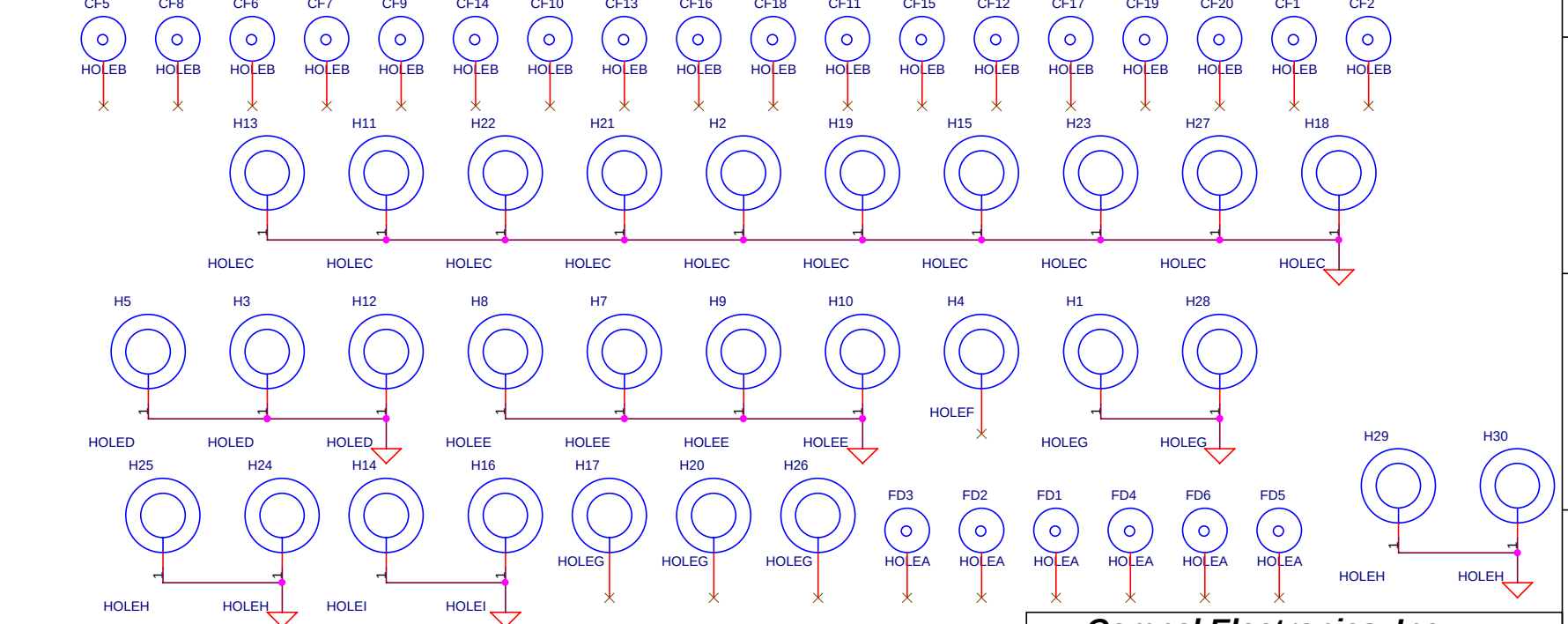
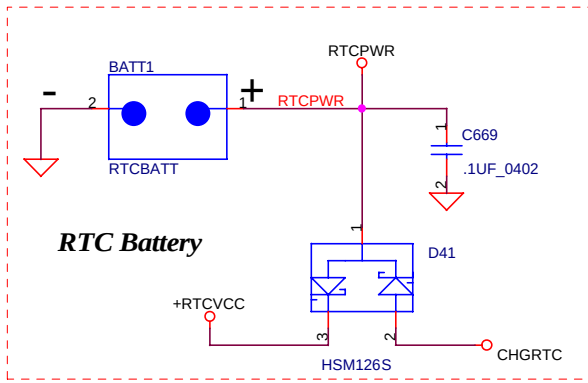
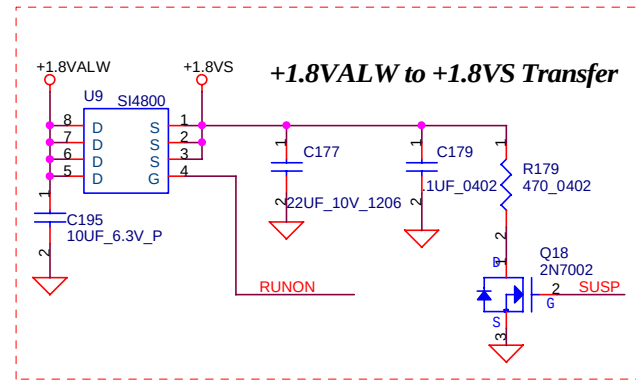
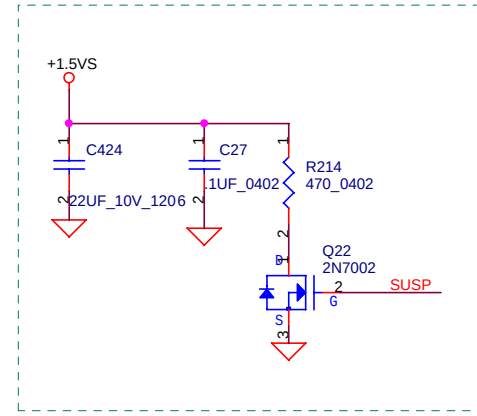
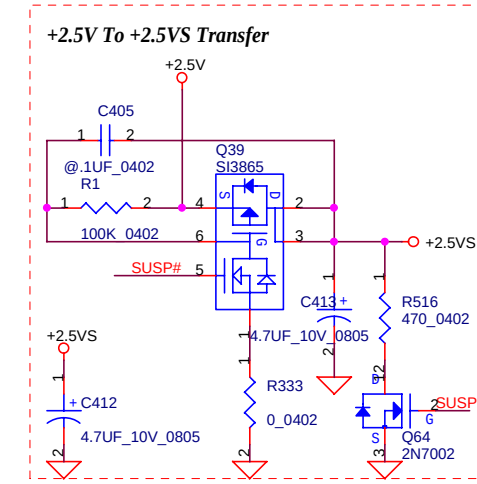
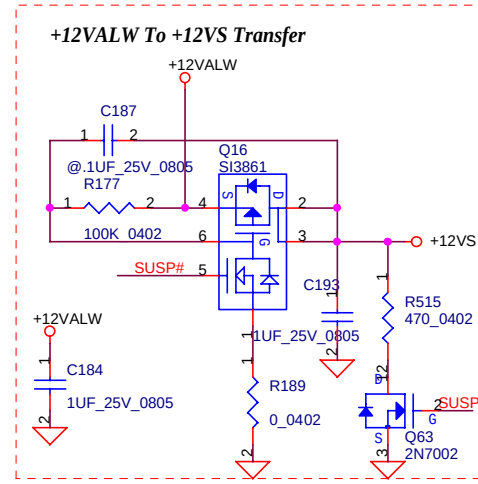
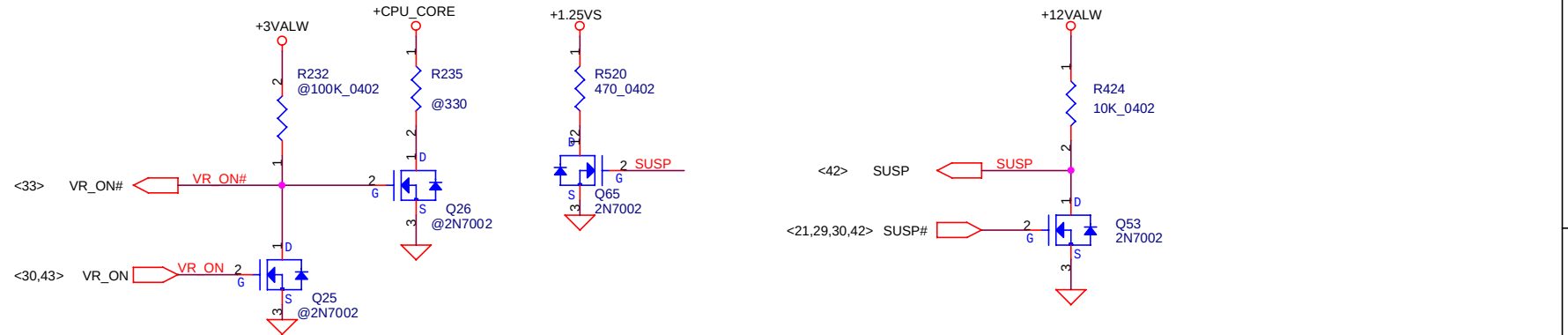
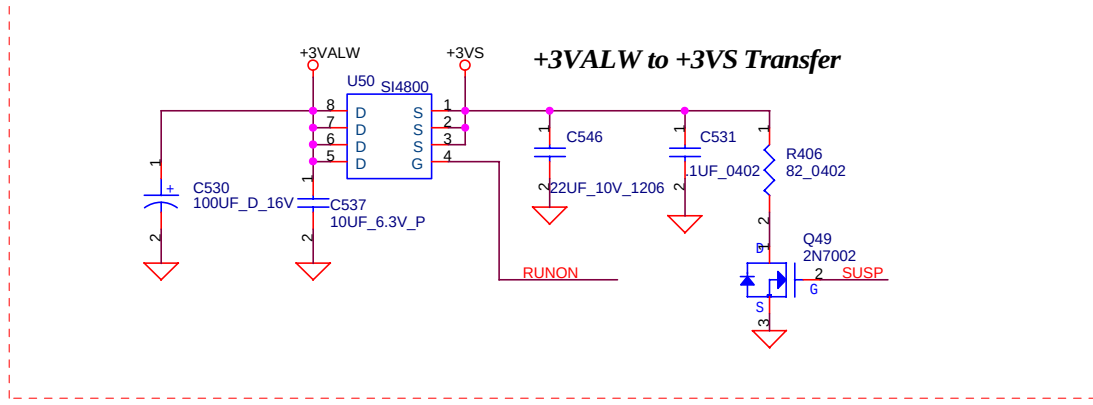
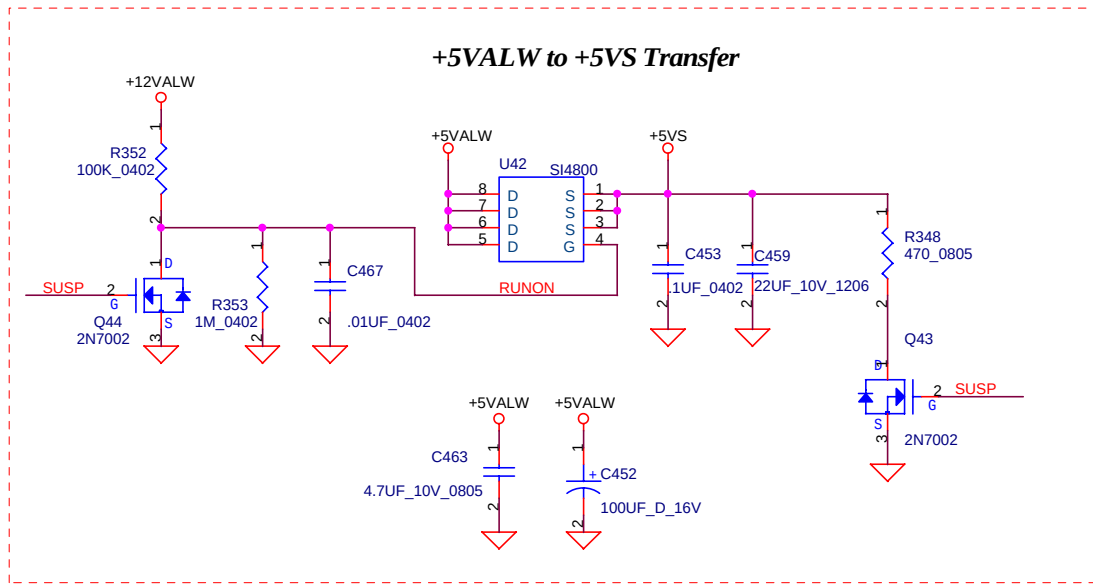
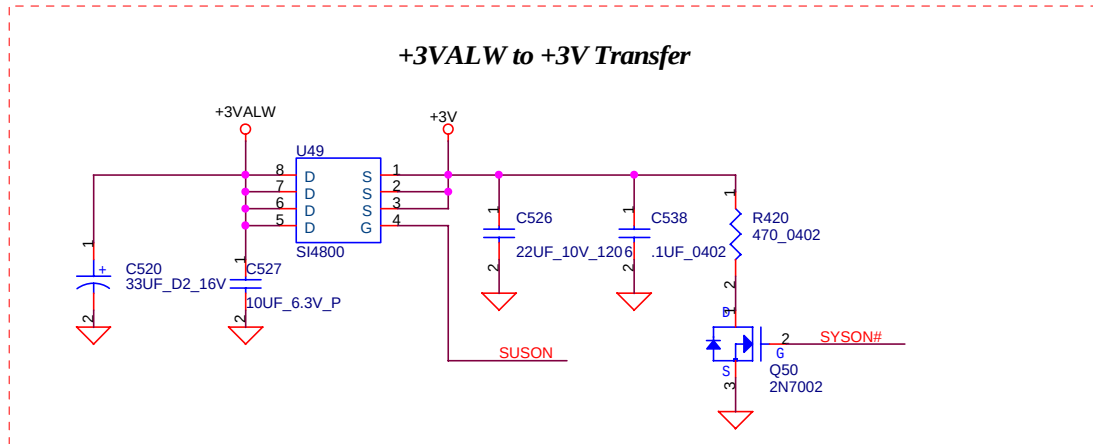
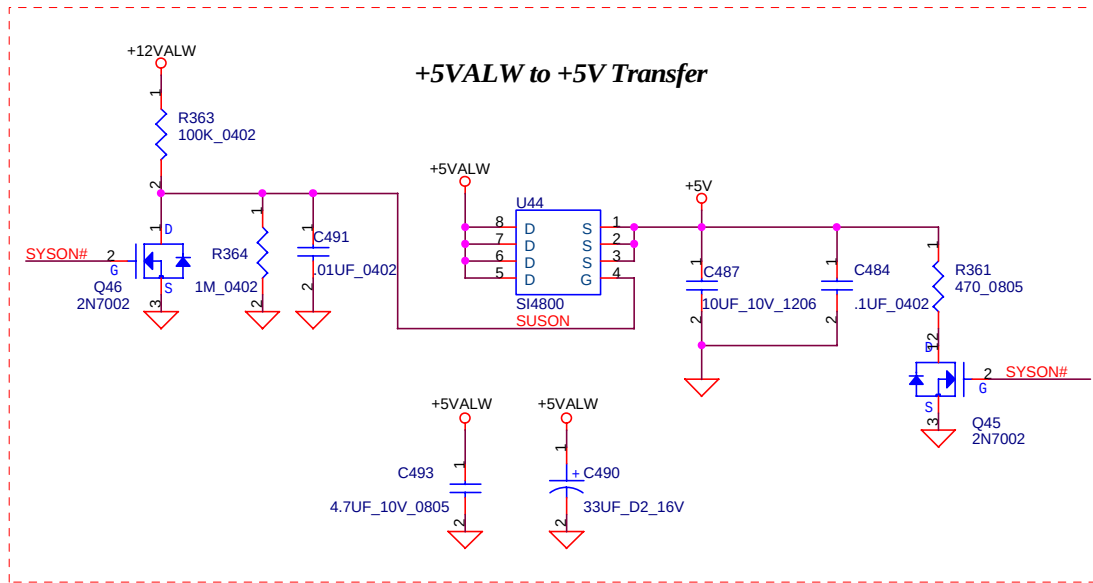


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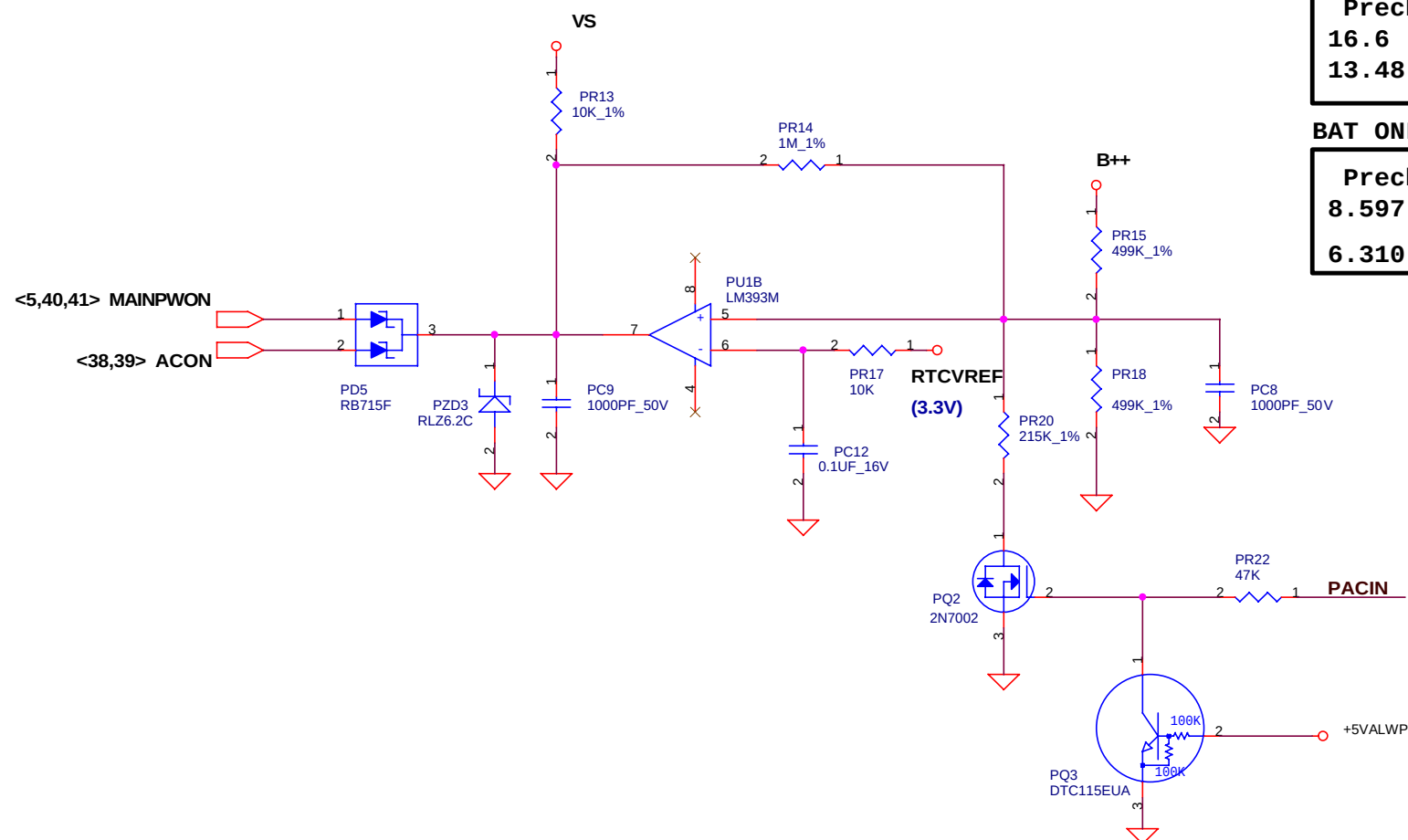
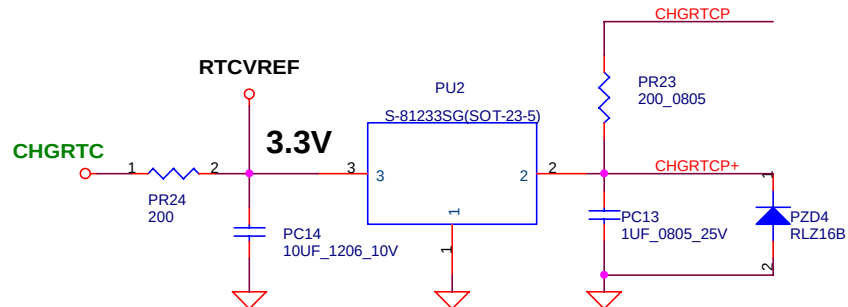
Compal Electronics, Inc.			
Title			
SCHEMATIC, MB LA-1511			
Size	Document Number		Rev
	401224		0B
Custom			
Date:	星期三, 八月 21, 2002		Sheet 35 of 43

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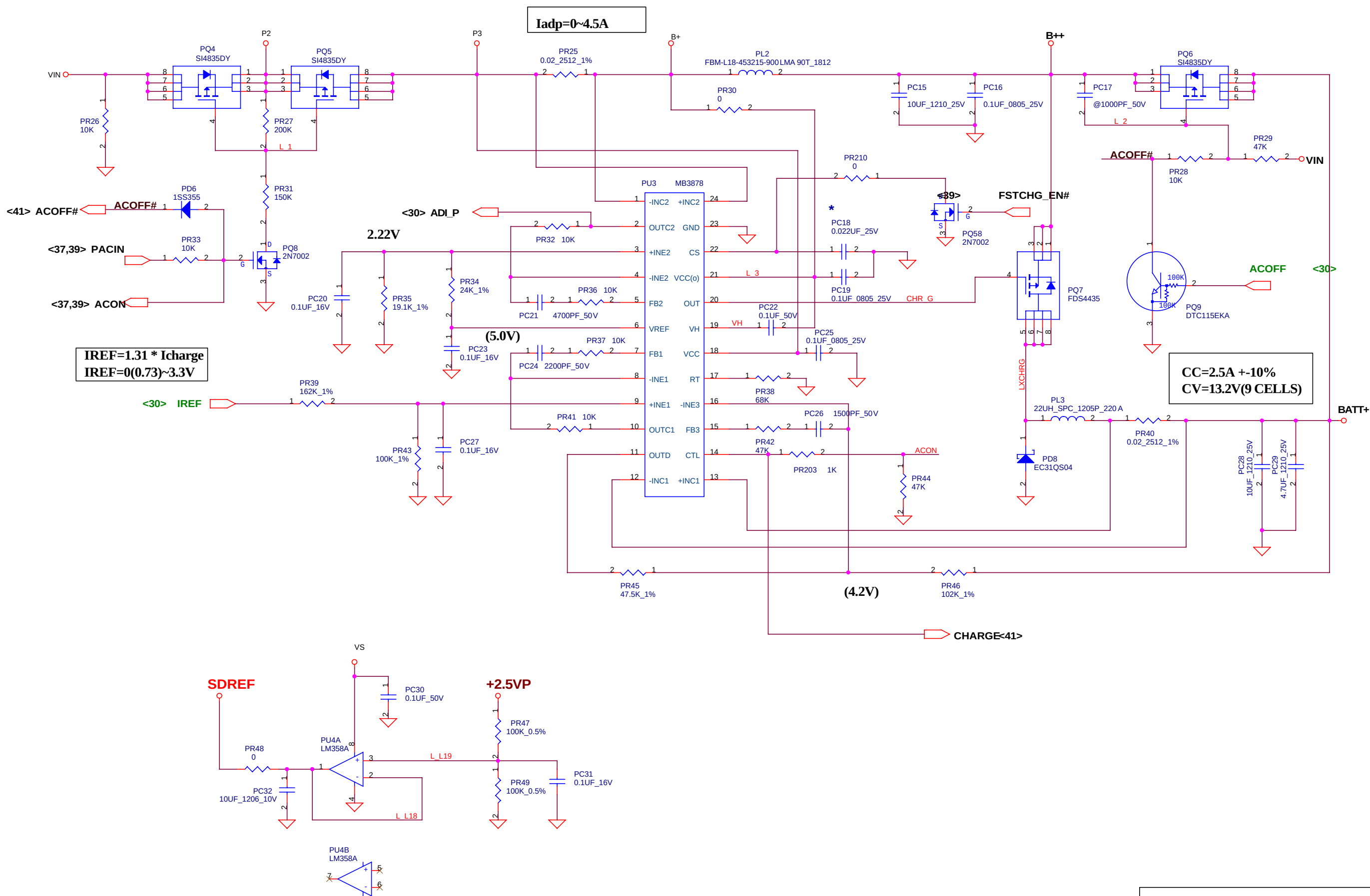


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Title	SCHEMATIC, M/B LA-1511	
Size	Document Number	Rev
	401224	0B
Custom		
Date:	星期三, 八月 21, 2002	Sheet 36 of 43

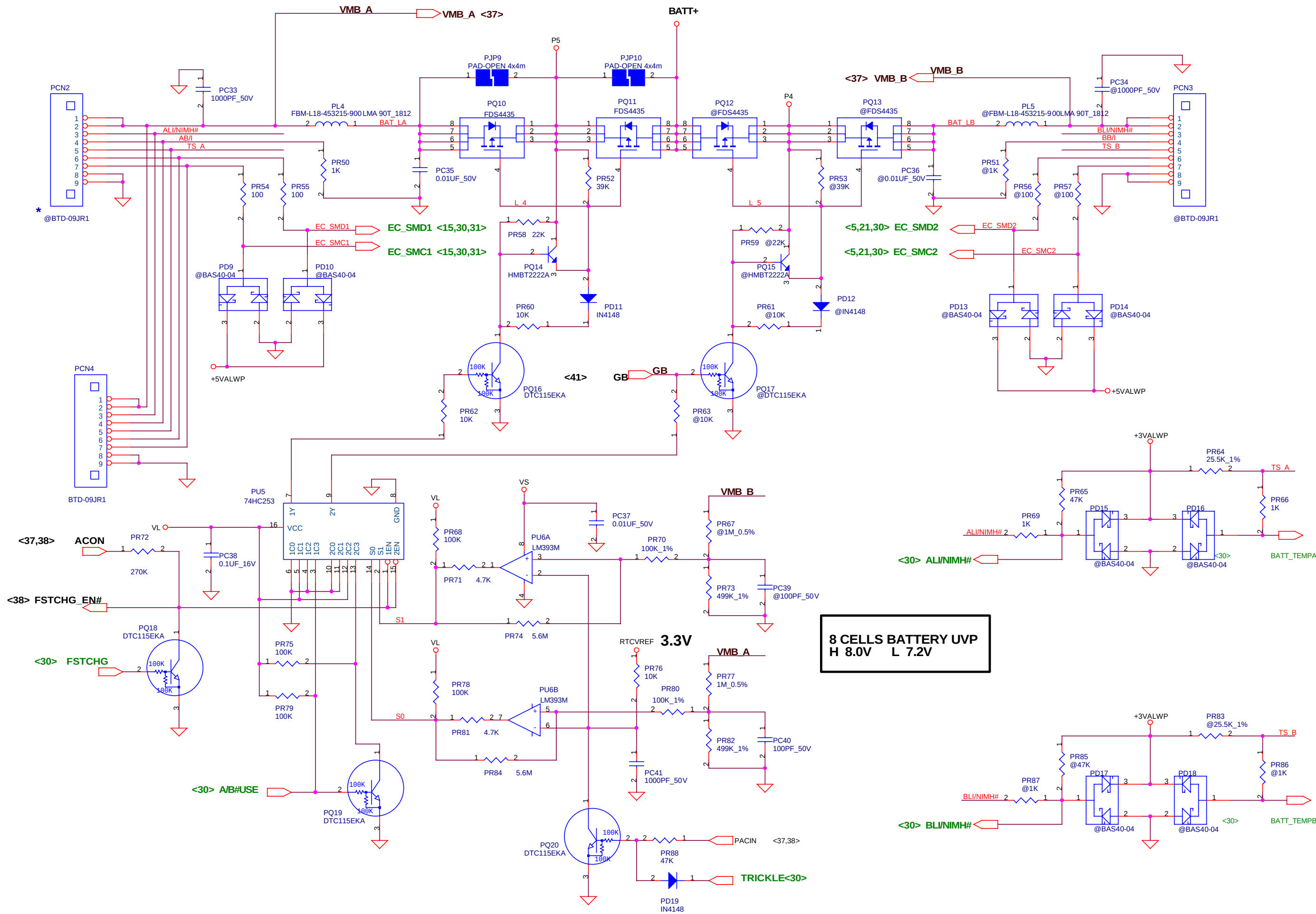


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6.310	6.101	5.683



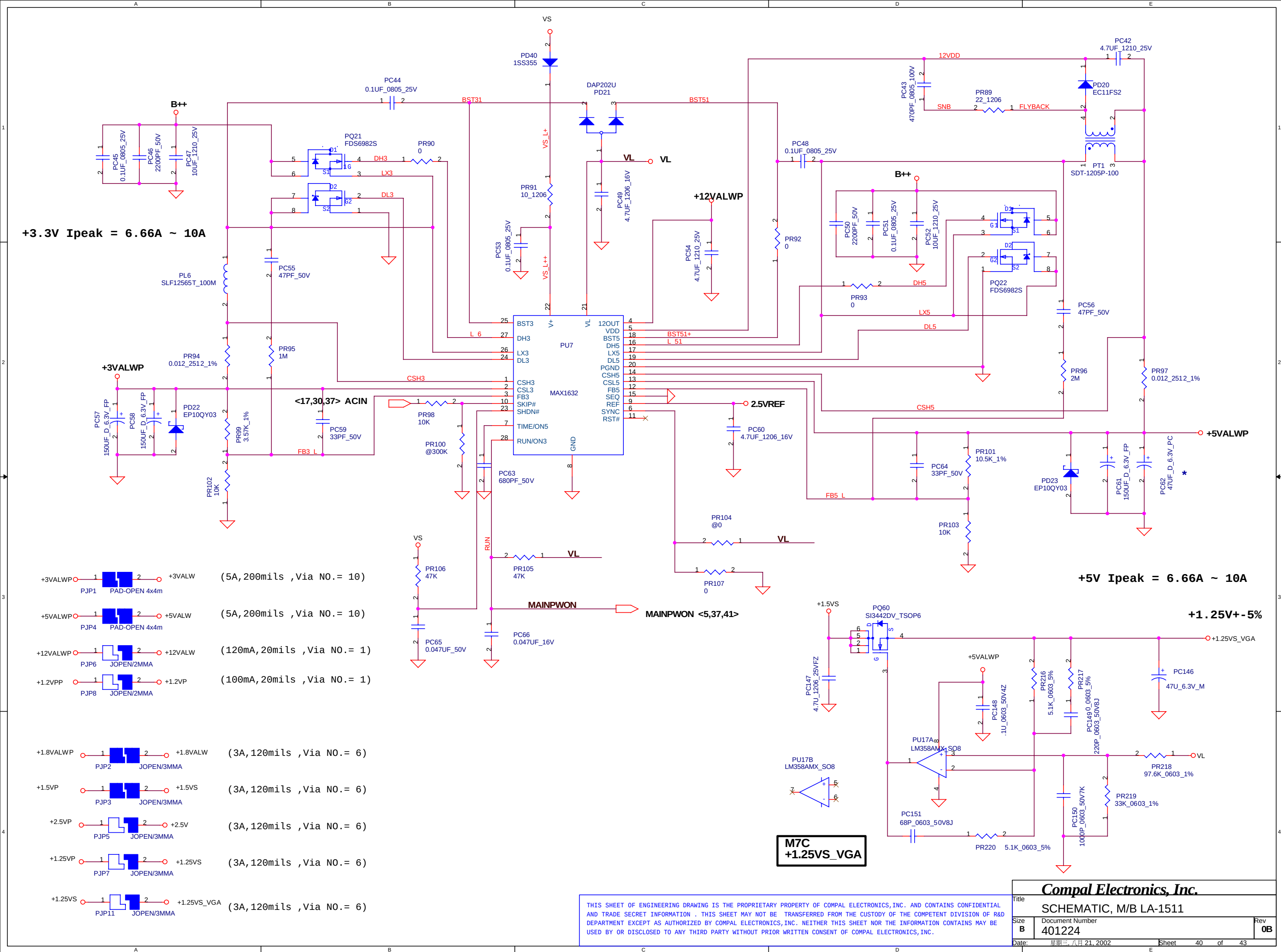
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Compal Electronics, Inc.		
SCHEMATIC, M/B LA-1511		
Size	Document Number	Rev
B	401224	0B
Date:	星期三, 八月 21, 2002	Sheet 38 of 43

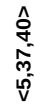


8 CELLS BATTERY UVP
H 8.0V L 7.2V

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CPU thermal protection at 90(91)+-3 degree C
Recovery at 50(51)+-3 degree C



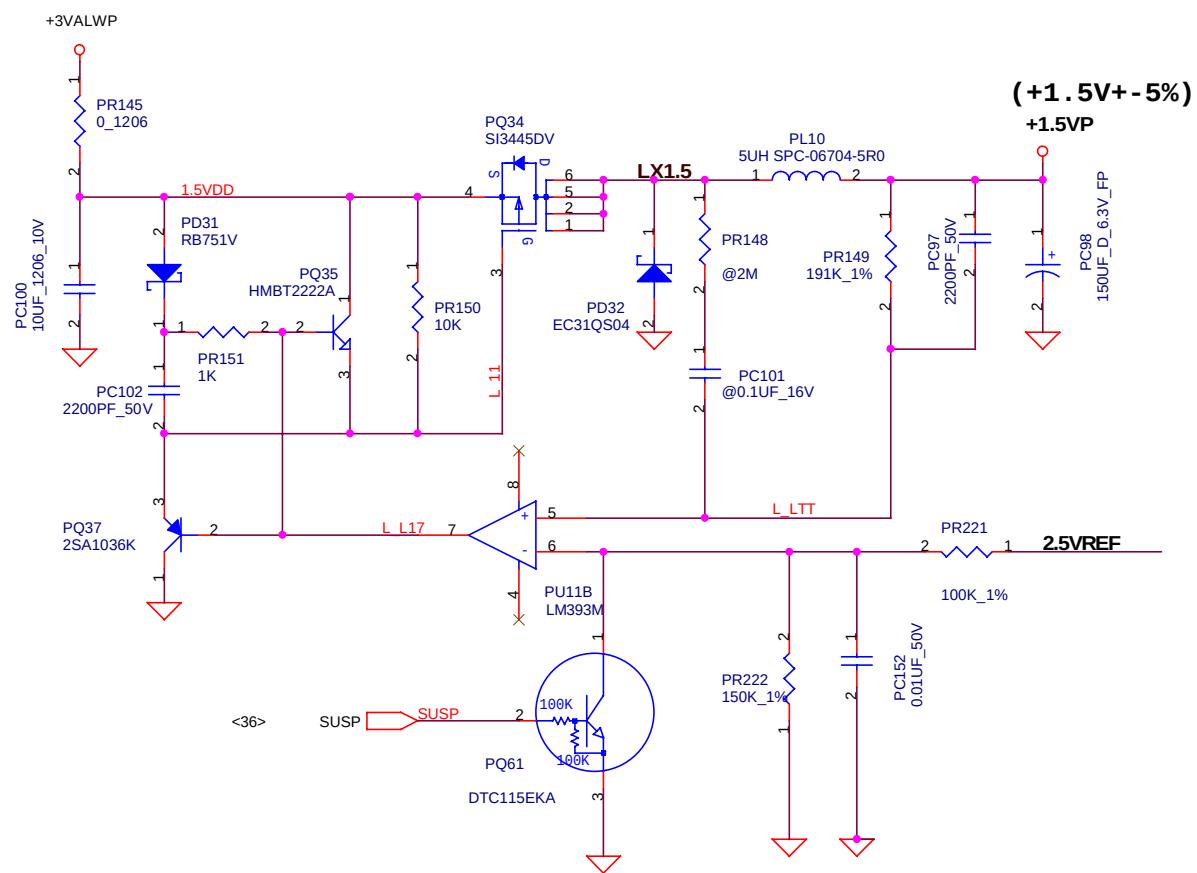
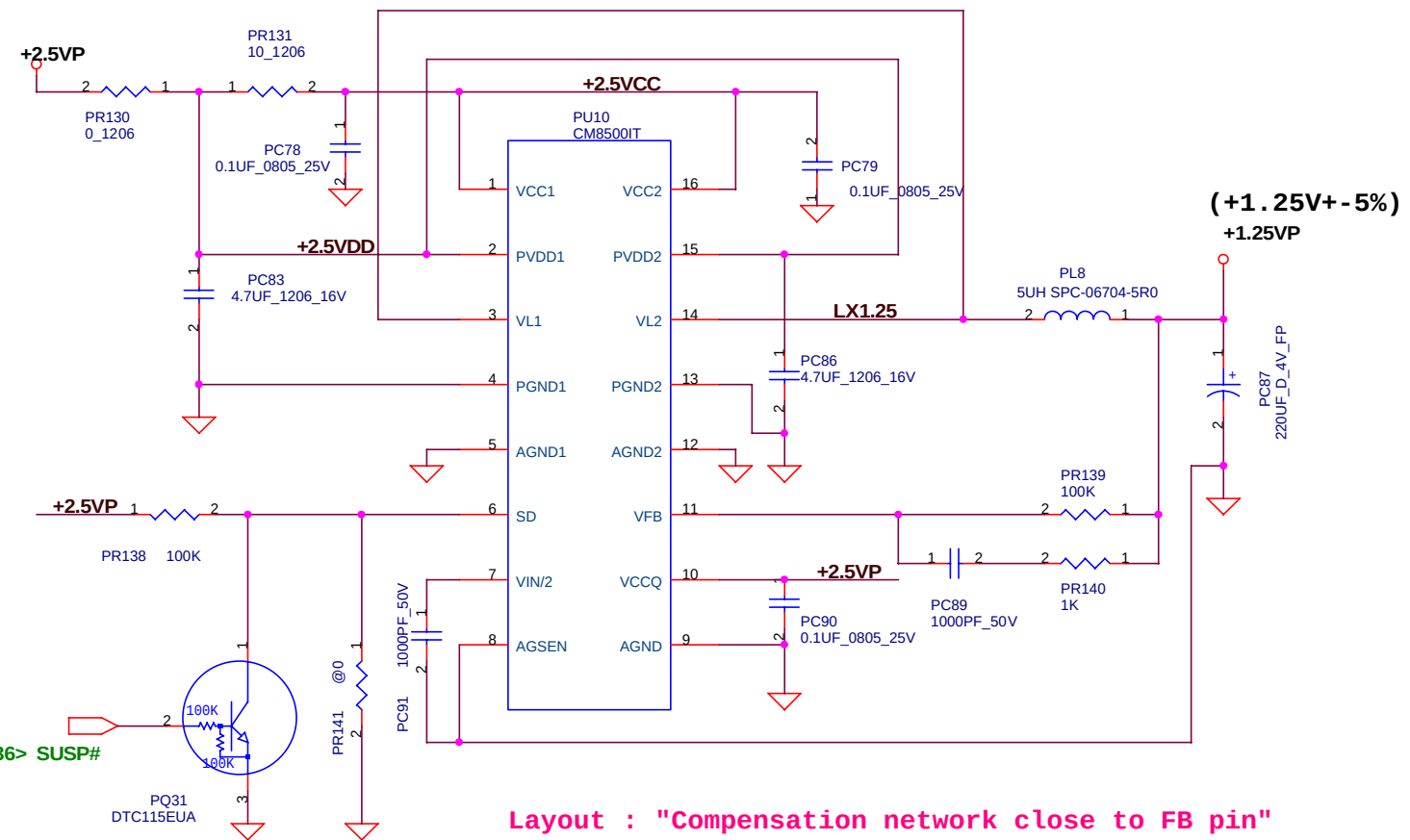
BAT. thermal protection at 85(86) $\pm$ 3 degree C
Recovery at 50(51) $\pm$ 3 degree C



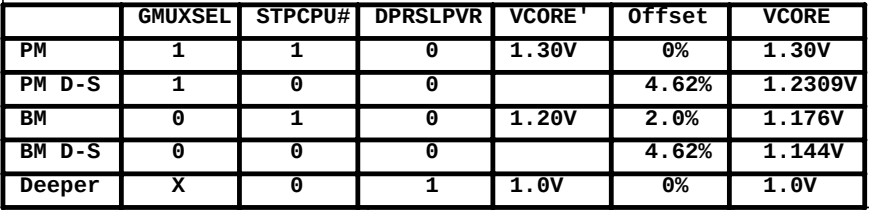
BATTERY Charger OVP : 13.56V



Date: 星期三, 八月 21, 2002 Sheet 41 of 43



Compal Electronics, Inc.			
Title	SCHEMATIC, M/B LA-1511		
Size B	Document Number 401224	Rev 0B	
Date: 星期二, 八月 21, 2002	Sheet	42	of 43



Compal Electronics, Inc.			
Title			
SCHEMATIC, M/B LA-1511			
Size B	Document Number 401224		Rev 0B
Date: 星期三, 八月 21, 2002	Sheet	43	of 46